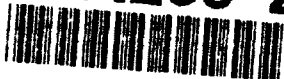④

Annual Letter Report

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Growth, Characterization and Device Development in
Monocrystalline Diamond Films

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13. ABSTRACT (Maximum 200 words)

Silicon-germanium films have been grown by electron-beam deposition on naturally occurring p-type semiconducting diamond(001) substrates. As evidenced by low-energy electron diffraction and scanning tunneling microscopy, the SiGe layers were polycrystalline. Corresponding current-voltage (I-V) measurements conducted at room temperature demonstrated the formation of a low-barrier rectifying contact. Consistent with the observed low-barrier height, the I-V measurements recorded at 300 °C exhibited ohmic-behavior. In addition, subsequent post-growth annealing of the SiGe contacts at 850 °C in ultra-high vacuum showed an apparent degradation in the I-V characteristics. Microwave performance of p-type diamond MESFET's is under investigation. A simulation program is being developed to enable a realistic evaluation of diamond MESFETs for high temperature and RF power applications. The program currently accounts for incomplete activation and will eventually account for all physical phenomena believed to be significant, including thermal and breakdown effects.

14. SUBJECT TERMS diamond thin films, device modeling, MESFET, MOSFET, JFET, FET, bias, acceptor impurity, microwave performance, Pisces-IIB, Teflon, SiGe, p-type diamond, I-V measurements			15. NUMBER OF PAGES 21
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Table of Contents

I. Introduction

Diamond as a semiconductor in high-frequency, high-power transistors has unique advantages and disadvantages. Two advantages of diamond over other semiconductors used for these devices are its high thermal conductivity and high electric-field breakdown. The high thermal conductivity allows for higher power dissipation over similar devices made in Si or GaAs, and the higher electric field breakdown makes possible the production of substantially higher power, higher frequency devices than can be made with other commonly used semiconductors.

In general, the use of bulk crystals severely limits the potential semiconductor applications of diamond. Among several problems typical for this approach are the difficulty of doping the bulk crystals, device integration problems, high cost and low area of such substrates. In principal, these problems can be alleviated via the availability of chemically vapor deposited (CVD) diamond films. Recent studies have shown that CVD diamond films have thermally activated conductivity with activation energies similar to crystalline diamonds with comparable doping levels. Acceptor doping via the gas phase is also possible during activated CVD growth by the addition of diborane to the primary gas stream.

The recently developed activated CVD methods have made feasible the growth of polycrystalline diamond thin films on many non-diamond substrates and the growth of single crystal thin films on diamond substrates. More specifically, single crystal epitaxial films have been grown on the {100} faces of natural and high pressure/high temperature synthetic crystals. Crystallographic perfection of these homoepitaxial films is comparable to that of natural diamond crystals. However, routes to the achievement of rapid nucleation on foreign substrates and heteroepitaxy on one or more of these substrates has proven more difficult to achieve. This area of study has been a principal focus of the research of this contract.

At present, the feasibility of diamond electronics has been demonstrated with several simple experimental devices, while the development of a true diamond-based semiconductor materials technology has several barriers which a host of investigators are struggling to surmount. It is in this latter regime of investigation that the research described in this report has and continues to address.

In this reporting period SiGe films have been grown via the co-deposition of Si and Ge on natural single crystal diamond (001) substrates. In addition, mono- and polycrystalline diamond FETs have been numerically modeled. The following subsections detail the experimental procedures for each of the aforementioned studies, discuss the results and provide conclusions and references for these studies. Note that each major section is self-contained with its own figures, tables and references.

II. Growth and Characterization of SiGe Contacts on Semiconducting Diamond Substrates

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A. Introduction

At present, there is a significant scientific and technological interest in the fabrication of stable ohmic and high-temperature rectifying contacts on diamond [1, 2]. To date, several metals, [3, 4] refractory metal silicides [5] and semiconductors [6] have been investigated as appropriate contact materials to semiconducting single crystal diamond substrates. In particular, the authors have demonstrated that the deposition of heteroepitaxial films of Ni on diamond exhibit excellent high-temperature rectifying properties [4]. Indeed, similar studies conducted on post-growth annealed $TiSi_2$ contacts on diamond have also shown rectification at high-temperature [5]. Moreover, it has also been recently demonstrated by Venkatesan et al. [6] that highly doped polycrystalline Si contacts fabricated on semiconducting diamond substrates form stable high-temperature rectifying diodes. In particular, the Si/diamond heterostructure also affords the potential of fabricating novel heterojunction devices which can be integrated with existing Si-based processing technologies.

In the present study we report initial results pertaining to the growth and characterization of SiGe contacts deposited on natural p-type semiconducting diamond C(001) substrates.

B. Experimental Procedure

Commercially supplied (D. Drucker & ZN.N.V) low-resitivity ($\sim 10^4$ $\Omega \cdot$ cm, p-type) semiconducting natural diamond (surface orientation (001)) substrates were chemically cleaned. The cleaning procedure included boiling $CrO_3 + H_2SO_4$ (heated to 200 °C) for 10 min. followed by immersion in aqua regia (3HCl +1HNO$_3$) and standard RCA cleaning solutions. Following cleaning, the samples were mounted on a Mo sample holder and transferred into the

electron-beam evaporation chamber. The base pressure in the system was typically 2×10^{-10} Torr. Prior to deposition, the substrates were heated to 550 °C for 5 minutes to thermally desorb both water vapor and possibly physi-adsorbed gas contaminants. On cooling to room temperature an unreconstructed (1×1) low-energy electron diffraction (LEED) pattern was observed from the C(001) surface. The substrate temperature was maintained at 550 °C and the SiGe films were grown by the co-deposition of Si and Ge using electron beam evaporation. The corresponding Si and Ge fluxes were calibrated to obtain SiGe layers with a 5% Ge composition. By employing a stainless steel shadow mask several SiGe dots of ~200 nm in thickness and 3×10^{-3} cm^2 in area were fabricated. Subsequent post-growth *in-situ* annealing of the samples was performed at a temperature of 850 °C at 10^{-8} Torr for 30 min.

C. Results and Discussion

Examination of the as-grown films by LEED failed to obtain an ordered surface structure. Indeed, an inspection of the SiGe films by *ex-situ* scanning tunneling microscopy (STM) showed a highly textured surface morphology which indicated that the deposited layers were polycrystalline, as shown in Figure 1. The STM image was obtained in the constant current mode with a tip bias of 2 V. The presence of small polycrystalline grains of ~100 nm is clearly evident. The corresponding rms surface roughness of the deposited layer has been determined to be ~ 5 nm. Also, it was apparent that the SiGe films exhibit excellent adhesion properties with the underlying diamond substrate. In contrast, STM images of the annealed films were much more difficult to obtain due to their higher resistivity. As shown in Figure 2, the surface morphology of the annealed films was significantly smoother with a corresponding rms surface roughness of ~ 3 nm and an apparent increase in grain size.

Shown in Figure 3 is the Raman spectrum of the SiGe films obtained at room temperature using an Ar$^+$ ion laser (514.5 nm) excitation source. Clearly observed are two distinct phonon peaks pertaining to Si and Ge at 518 cm^{-1} and 300 cm^{-1}, respectively. It is interesting to note that the corresponding SiGe phonon mode, indicative of alloy formation (near 400 cm^{-1}) was not observed. The absence of the SiGe phonon mode would tend to suggest an apparent segregation and clustering of Si and Ge during growth. Differences in the Si and Ge surface mobilities and/or surface energies on the chemically cleaned diamond C(001) surface during the initial stages of growth may account for this behavior [7]. Further studies are currently in progress to study this growth phenomena. Following the high-temperature ultra-high vacuum annealing step only the Si phonon peak was observed in the Raman spectrum. The absence of the Ge phonon mode in the layer was attributed to the evaporation of Ge during thermal annealing.

Current-voltage (I-V) measurements were obtained by mounting the diamond substrates on a Cu plate using Ag paint to form a large area back contact and applying a bias to the SiGe
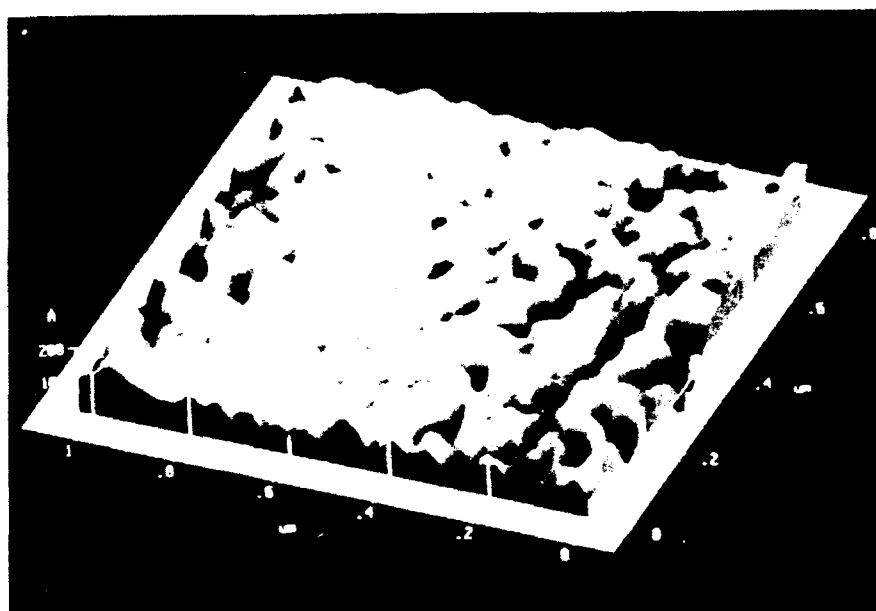
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Figure 1.   Topographic (constant current) STM micrograph of the surface morphology of the SiGe film deposited on natural diamond C(001) substrates.
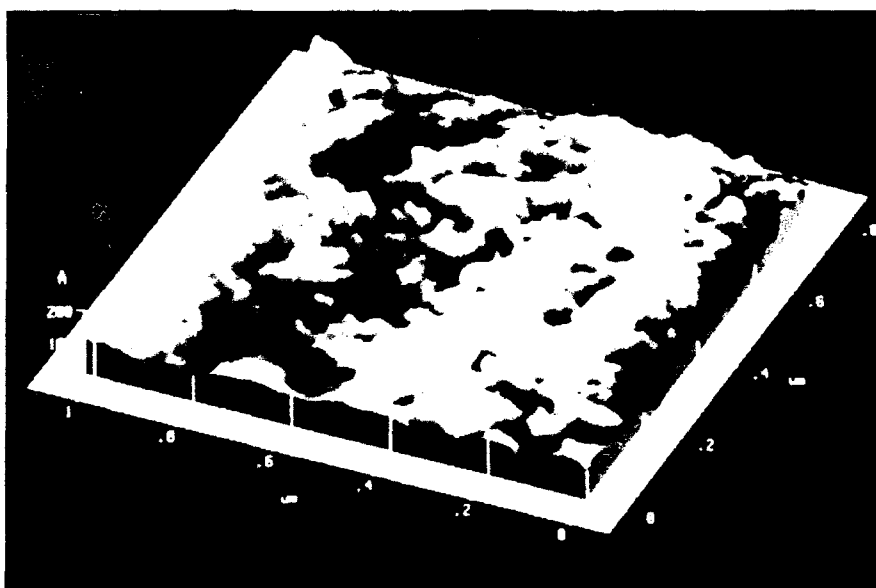

Figure 2.   Topographic (constant current) STM micrograph of the surface morphology of the as-deposited SiGe film following a high-temperature anneal at 850 °C in a vacuum of 10^{-8} Torr for 30 min.
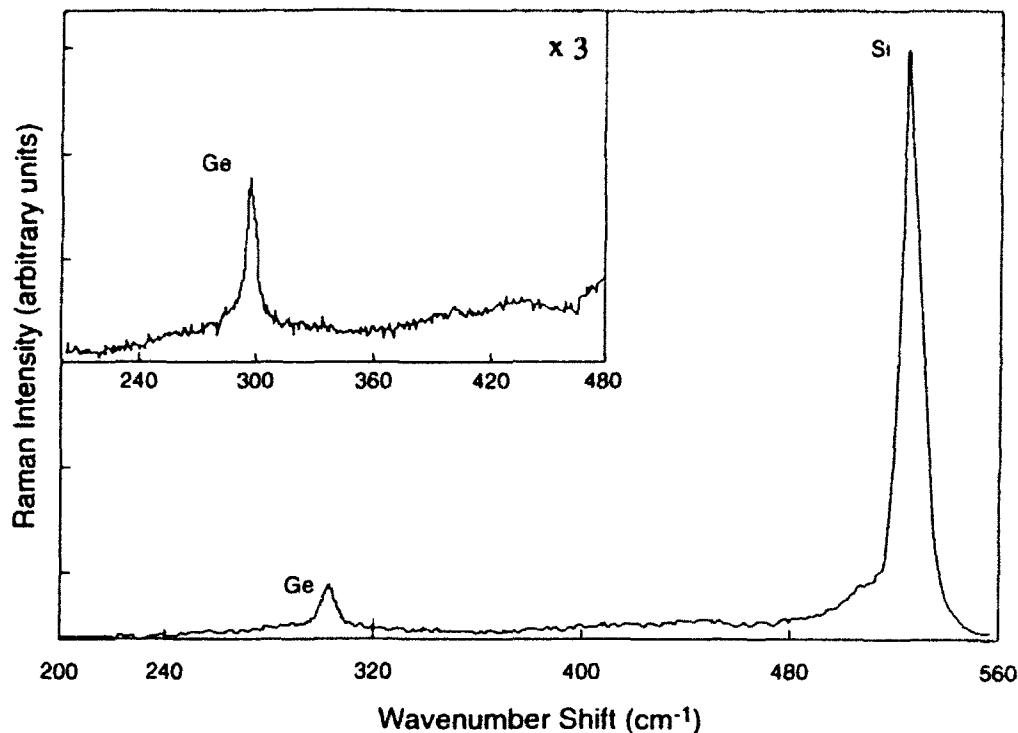
Figure 3.   Raman spectrum of the SiGe film deposited on natural C(001) diamond
             substrates.

contact using a W probe. The room temperature I-V characteristics obtained for the as-deposited SiGe contacts on semiconducting diamond substrates are shown in Figure 4. The rectifying character of the SiGe contact is clearly evident. From the I-V measurements a small forward bias turn-on voltage of ~ 0.6 V was estimated. The corresponding reverse bias leakage current density was measured to be ~1.56×10^{-6} A / cm^2 at 20 V. Moreover, from the apparent linear region of the semilogarithmic plot of the forward characteristics an ideality factor n of 2.5 was calculated. This high n value may be an indication that the current conduction at the SiGe/diamond interface is not governed by a thermionic emission mechanism. It is interesting to note that similar observations have also been reported for Ni, $TiSi_2$ and Si contacts on semiconducting diamond C(001) substrates (4-6). In each of these studies current conduction appeared to be dominated by a space charge limited current (SCLC) mechanism. Consistent with the small turn-on voltage and the relatively high reverse leakage current, the corresponding I-V measurements recorded at 300 °C exhibit ohmic-like behavior.

Shown in Figure 5 is the corresponding I-V characteristics for the high-temperature annealed SiGe contacts recorded at 25 °C. Clearly, in comparison with the as-deposited films, the rectifying behavior of the annealed SiGe contacts has been degraded. In particular, the forward bias turn-on voltage has been significantly reduced. From the I-V measurements a forward bias turn-on voltage of ~ 0.2 V has been estimated. Also, the reverse bias leakage current has increased to ~22 nA which corresponds to a current density of 7.3×10^{-6} A/cm^2 at 20 V. In addition, corresponding I-V measurements conducted at 300 °C showed ohmic-like behavior.
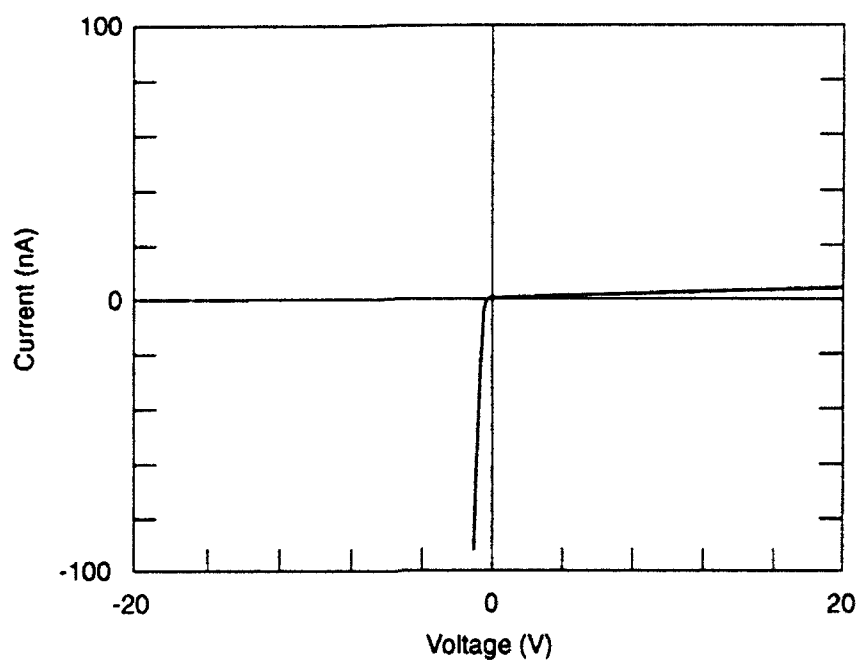
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Figure 4.   Linear plot of the current-voltage (I-V) characteristics of the SiGe contacts on semiconducting diamond C(001) substrates. Measurements were conducted at 20 °C.
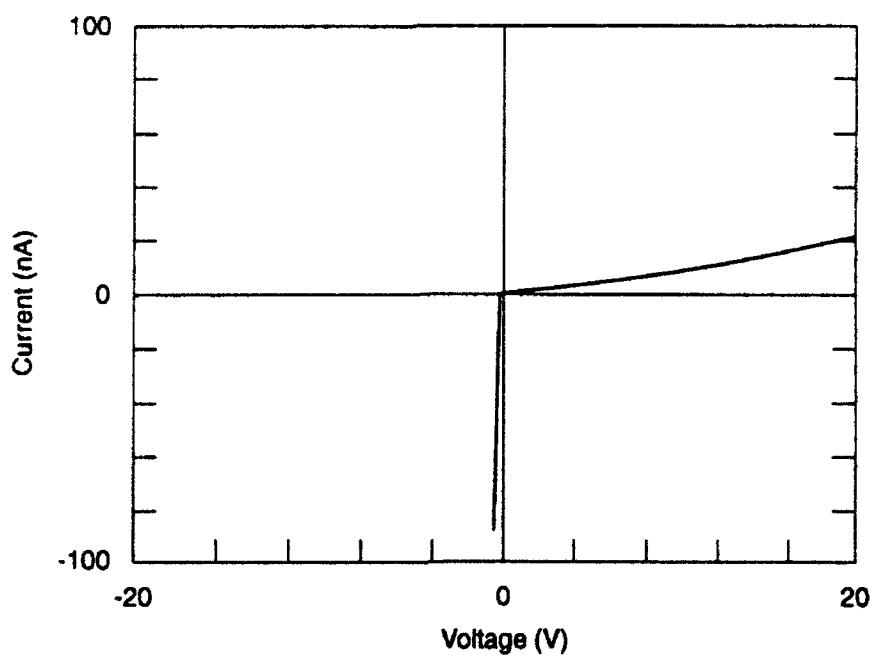

Figure 5.   I-V characteristics of the Post-growth high-temperature annealed SiGe contacts at 25 °C.

6

D. Conclusions

In summary SiGe films have been grown by the co-deposition of Si and Ge on natural single crystal diamond C(001) substrates. As evidenced by LEED and STM analysis, the as-deposited films are polycrystalline. The I-V measurements of the SiGe contacts have demonstrated rectifying characteristics at room temperature. However, for measurements conducted at 300 °C the I-V characteristics exhibit ohmic-like behavior. Furthermore, it has also been demonstrated that subsequent post-growth annealing of the contacts has degraded the I-V characteristics.

E. Future Research Plans

Optimize the substrate cleaning procedure and growth conditions to achieve epitaxial SiGe films. Measurement of the bandgap offset between the SiGe contacts and the single crystal diamond substrate utilizing ultraviolet photoelectron spectroscopy (UPS).

Acknowledgements

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III. Modeling of Microwave MESFET Electronic Devices Fabricated from Semiconducting Diamond Thin Films

A. Introduction

The NCSU physics-based MESFET model [3] has been extended to other device structures and materials by interfacing it with PISCES-IIB and an advanced model of breakdown being incorporated into a separate version of the code.

Consideration of insulated-gate FETs and other structures is important for this MESFET project because of the present difficulty producing good metal-semiconductor junctions with diamond. During development of the model, validation requires comparison with experimental measurements and much of the existing diamond device data is for insulated-gate FETs.

Thermal effects are important for devices using diamond as a material because of its potential for high temperature operation and because of the high activation energy of the usual doping, boron. PISCES-IIB [4] is a general two-dimensional device simulator developed at Stanford, as currently enhanced and supported by Silvaco International. This combined system was begun in summer of 1992 and is still under development.

As of March, 1993, the new model is capable of reproducing experimental DC IV curves and predicting RF performance of experimental diamond FETs at a wide range of temperatures with proper treatment of incomplete activation effects.

The combined system successfully reproduced DC IV curves for three experimental FETs fabricated in monocrystalline and polycrystalline diamond. Boron was the acceptor impurity in all three experimental p-type MOSFETs, but the three devices were of diverse origin and structure. The first was fabricated from naturally occurring single-crystal diamond that has been ion-implanted [2]; the second from homo-epitaxially grown single crystal diamond [1]; and the third from epitaxially grown polycrystalline diamond [5]. For all three cases, the new code modeled incomplete activation and extended previous MESFET simulations to monocrystalline and polycrystalline MOSFETs. Previous simulations predicted substantial increase in output power for single crystal MESFETs [6] using the NCSU large-signal MESFET model, but those predictions assumed complete carrier activation. RF predictions were produced somewhat later, but the simulated RF performance was poor for the experimental devices.

Most recently, encouraging DC and RF simulations were performed for a proposed MESFET design. These results will be presented for the first time in this report.

The advanced breakdown model, which includes both surface and avalanche currents, was begun in spring 1992 and has continued. In future work, we will combine thermal effects and breakdown effects.

B. Investigation Procedure

Our experimental approach was to replace the intrinsic FET model of TEFLON, the NCSU large-signal MESFET simulator [3] with a model of the MOSFET written in Pisces-II [4].

TEFLON combines a sophisticated analytic approximation of the physics in the gate region of a MESFET with harmonic balance to predict large-signal RF performance of realistic microwave circuits.

The physics of the diamond MOSFET channel is similar to the physics currently modeled by TEFLON for the GaAs MESFET. The questions of interest for large-signal or RF applications of diamond MOSFETs are also similar to those addressed by TEFLON, such as predicting gain as a function of input power, estimating power-added efficiency, and calculating output power into saturation. Realistic high-frequency simulation of a FET must include an embedding circuit, which we modeled conventionally as linear, lumped-element input and output microwave circuits. We use the harmonic balance routines of TEFLON to solve the nonlinear FET circuit simultaneously with the linear embedding circuit. In addition, we include realistically adjusted values for parasitic elements around the intrinsic FET.

TEFLON is a quasi-static approximation that used dc values of currents and capacitances I_d, I_g, C_{gs}, and C_{ds} tabulated as function of the biases V_{gs} and V_{ds}. These values are computed using Pisces IIB, accounting for incomplete carrier activation.

Pisces is a two-dimensional device modeling and simulation program developed at Stanford [4]. Pisces employs a finite-difference approach which is too slow to be directly interfaced with a harmonic balance routine. However, Pisces is well suited to analysis of dc device behavior, including the estimation of I-V curves and gate capacitances. Pisces supports some RF simulations with simple embedding circuits, but not the rich set of RF circuit simulations that TEFLON supports.

We have developed a combined simulation program including Pisces to simulate dc I-V curves and other relevant dc behavior in the diamond MOSFET gate region, TEFLON to simulate RF behavior from dc I-V curves, and an interface between the two programs.

C. Results

We have validated on data from three actual devices of diverse origin and structure. Experimental p-type MOSFETs have been fabricated from naturally occurring single-crystal diamond that has been ion-implanted [2], from homo-epitaxially grown single crystal diamond [1], and from epitaxially grown polycrystalline diamond [5]. Boron was the acceptor impurity in all the devices. We are not aware of device quality n-type diamond at this time.

We have validated the PISCES part of the simulator with dc measurements of three different diamond FETs:

1. a boron-doped homoepitaxially grown single-crystal device fabricated at Penn State [1],

9

2. an ion-implanted homoepitaxially grown single-crystal device fabricated at the Naval Ocean Systems Center (NOSC) [2], and

3. a boron-doped heteroepitaxially grown polycrystalline diamond fabricated at Kobe Steel Electronic Materials Center in North Carolina [5].

We have also considered a diamond JFET device.

The Penn State device reported by Grot, Gildenblat, and Badzian is a recessed gate naturally doped p-type MOSFET [1]. This device was fabricated using ECR plasma etching of an active layer. Most of the parameters required for the simulation were reported: oxide thickness of 100 nm, gate length of 5 micron, gate width of 30 micron, active layer thickness of 0.8 micron, recess depth of 0.2 micron. The doping concentration of the active layer was determined to be about 1.2×10^{16} cm^{-3}. This number corresponds to 0.1% hole ionization at room temperature.

The dc simulation was performed at a temperature of 473°K so that a direct comparison with the experimental results could be performed. Because measured hole mobility of 280 cm^2/V-sec was given only at room temperature in the Penn State report, the mobility was adjusted for high temperature operation. Alternative physical models were considered and sensitivity to material parameters was numerically explored.

It was found that an incomplete ionization model was most critical for agreement between simulation and measured data. Good simulation of the diamond single-crystal device required a high value of acceptor energy level (Ea=0.37 eV). Figure 1 shows the I-V curve simulated at Vg=0 and Vg=70 v. The drain current at Vds=–50 v for zero gate bias and Vds=70 v are about 5.2 μA/μm and 2.8 μA/μm, respectively. These values are in good agreement with the experimental results of 3.8 μA/μm and 1.0 μA/μm, respectively.

The NOSC device reported by Hewett, et. al. is an ion-implanted p-type Insulated-Gate FET fabricated from a single crystal thin film diamond, epitaxially grown on a naturally occurring diamond substrate [2]. A multiple implant scheme was used to provide an approximately uniformly doped active layer of about 210 nm in thickness. The device was fabricated in a concentric ring structure with 1000 um wide gate in outer diameter (600 μm of inner diameter). The gate length was 1 μm. All the materials parameters and physical model functions were the same as before, except that the room temperature free hole concentration and mobility were taken to be the measured values of 5×10^{15} cm^{-3} and 30 cm^2/V-sec, respectively.

The I-V characteristics at room temperature are shown in Figure 2. Current saturation is clearly observed. The simulated I-V curves agree with experiment, except for pinch-off. Pinch-off in the actual device was observed at a gate bias of approximately +12 v, but is harder to obtain in simulation. This may be due to our simple models of free carrier density and mobility in the multiply ion-implanted device. Actual doping profiles are not uniform. In future
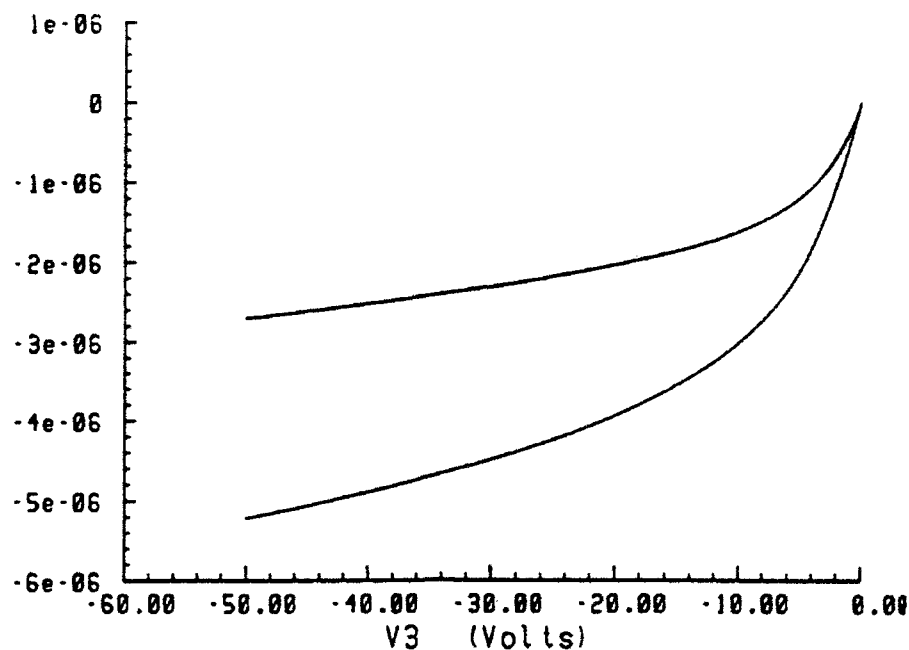
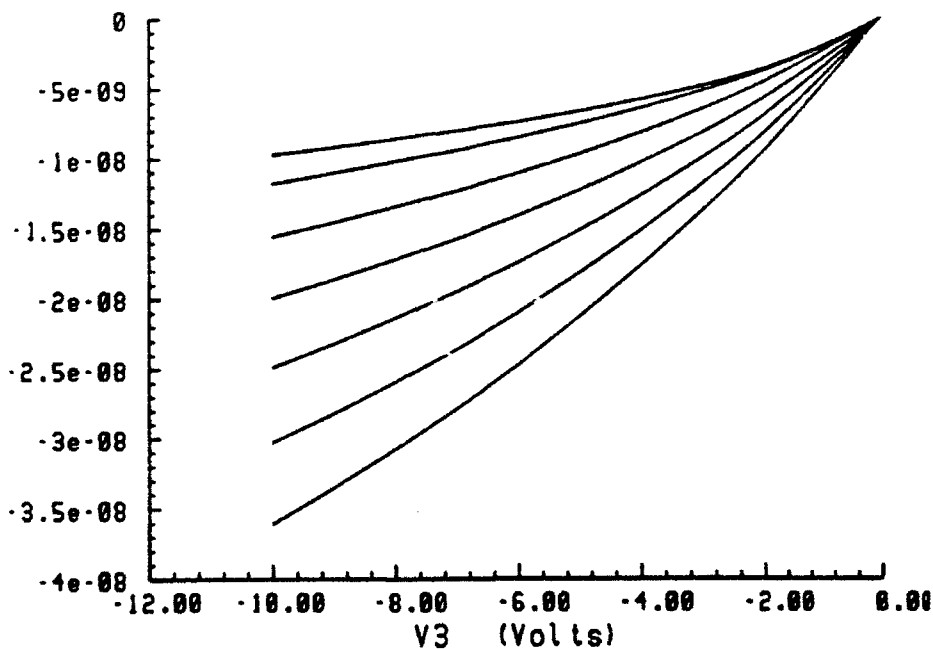Figure 1.   Drain current versus drain voltage for the Penn State device for Vg=70 v (top curve) and Vg=0 v (bottom curve).

Figure 2.   Drain current versus drain voltage for the NOSC device for Vg=12 v (top curve) to Vg=0 v (bottom curve) in steps of -2 v.

research, we will use optimization techniques to obtain more accurate and realistic values for the material parameters from the performance of the diamond devices.

The Kobe device reported by Tessmer et. al. is a synthetic device [5]. This was the first device which exhibits saturation and pinch-off in a polycrystalline diamond FET. A 0.5 μm thick active layer of p-type diamond was grown by adding diborone in the gas phase. Boron concentration was measured to be about 7×10^{16} cm^{-3}. The device was fabricated in a concentric ring structure with nominal gate length of 2 μm and gate width of 314 μm.

The I-V characteristic at 423 $^\circ$K shows pentode-like behavior, as indicated in Figure 3. The drain current is very low, about 10 pA/mm at Vg=0 v and Vds=–20 v. The simulated and measured data are in good agreement.

The simulations indicate that polycrystalline diamond may have an effective boron activation energy of about 0.65 eV, rather than the 0.37 eV expected for single crystal material. The increase may be due to the trapping of carriers at the grain boundaries at doping concentrations of around 7×10^{16} cm^{-3}. This would indicate a barrier height at the grain boundary of about 0.3 eV in this device (grain size of 3 μm).

We have also conducted preliminary simulations of a diamond JFET assuming that an n-type dopant may be found. Figure 4 shows that at room temperature, the I-V characteristics of diamond JFETs shown strong space-charge limited behavior. At higher temperature, the behavior may become more pentode-like due to an increased number of free carriers. Also, the shape of the I-V curve is sensitive to the geometry of the channel, i.e., the gate length to the channel width ratio.

D. RF Performance Predictions

The RF simulations performed for the NOSC device in the previous section produced disappointing results. This monocrystalline, homoepitaxial, insulated-gate FET fabricated at NOSC and reported by Hewett, et al. has a gate capacitance of about 0.3 pF, which is reasonable for the structure, but is disproportionately large compared to a very low value of Idss=45 mA for a 1000 mm gate width device. This unfortunate condition at room temperature results from low carrier activation and low mobility.

Monocrystalline diamond with high mobility will appear as the technology progresses. With improved materials, better metal-semiconductor junctions may also appear. Much better RF performance is likely for diamond MESFETs with higher mobility and possibly higher operating temperatures. In order to investigate this possibility, the device of Figure 5 was simulated with the parameters at three temperatures as shown in Table I. The DC IV characteristics for operation at 300 $^\circ$C, 500 $^\circ$C and 650 $^\circ$C are shown in Figures 6, 7, and 8, respectively. The increase in channel current and transconductance at elevated temperature is due to the increase in activation. In particular, the performance improvement at 650 $^\circ$C is most
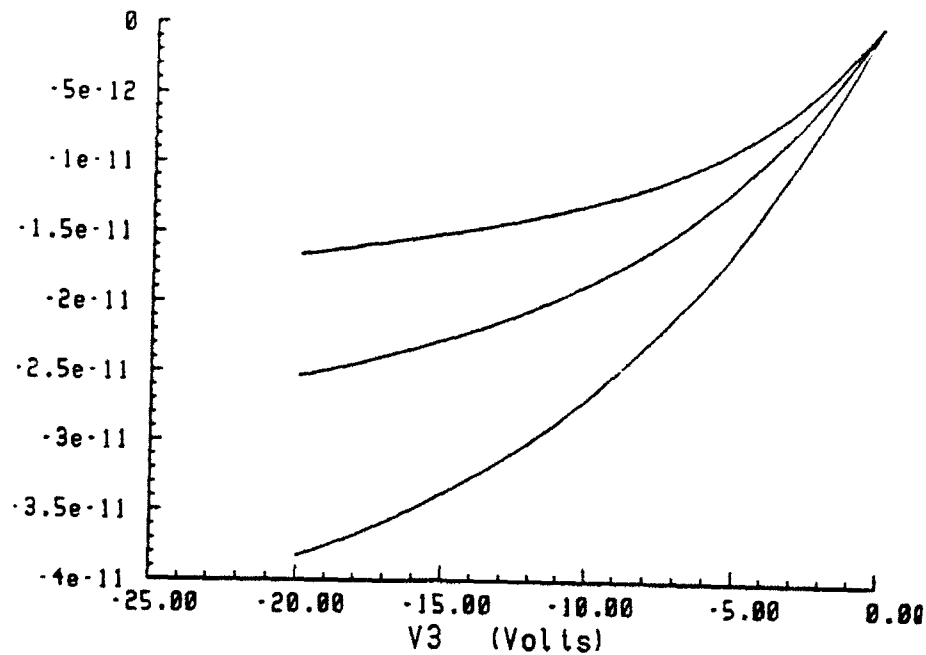
PISCES-II 9009R

Figure 3.   Drain current versus drain voltage for the Kobe Device at T=423 °K for Vg=10 v (top curve) to Vg=0 v (bottom curve) in steps of -5 v.
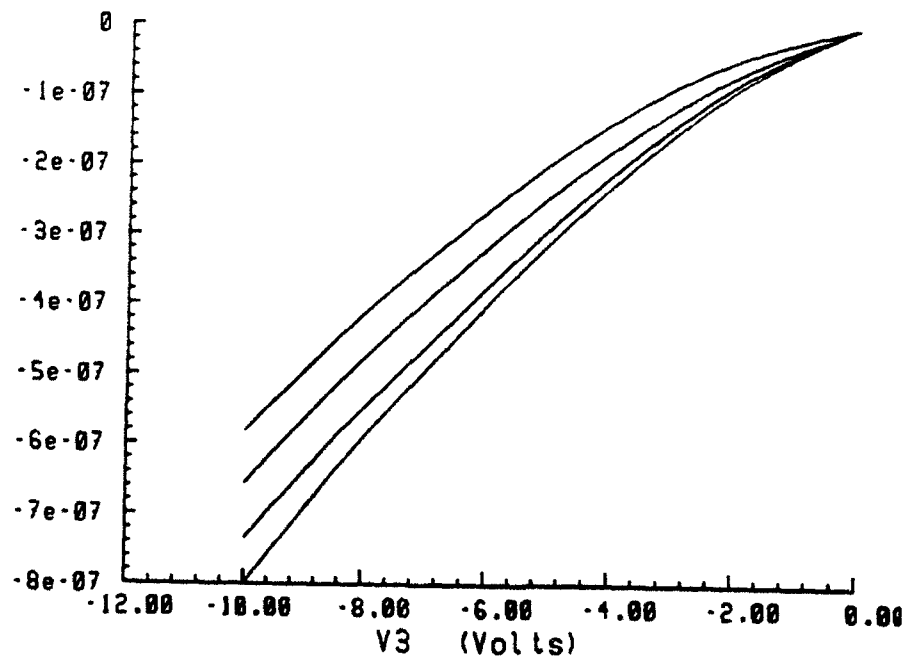
PISCES-II 9009R

Figure 4.   Triode-like drain current versus drain voltage for the diamond JFET for Vg=6 v (top curve) to Vg=0 v (bottom curve) in steps of -2 v.
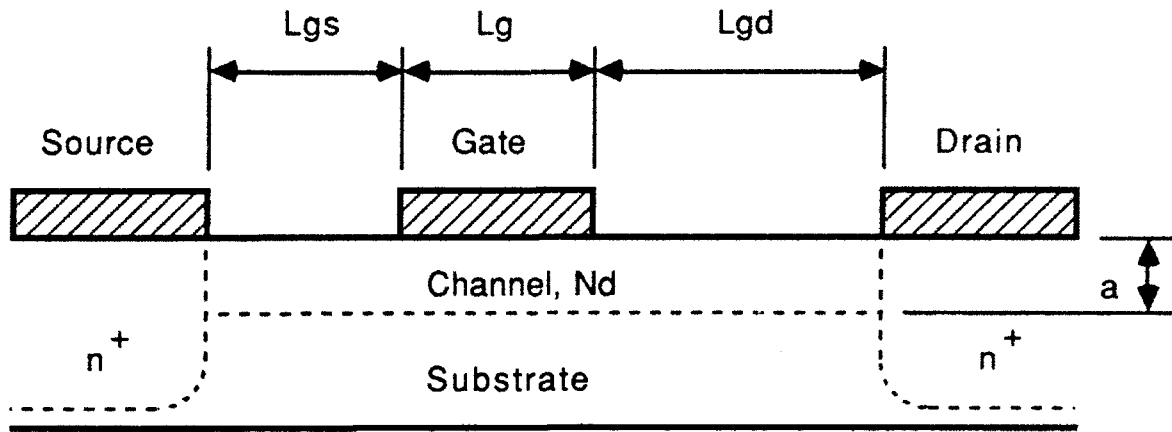
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Figure 5.   Structure for a proposed P-channel diamond MESFET.

Table I. MESFET Parameter Values

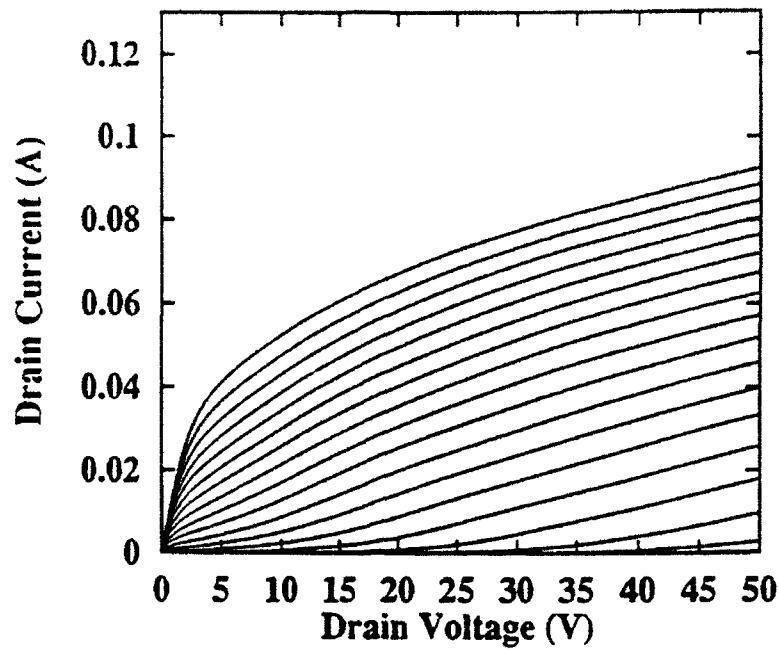| Parameter	Value		
	300°C	500°C	650°C
L_g (μm)	0.5	0.5	0.5
W (mm)	1	1	1
L_{ds} (μm)	1	1	1
L_{gs} (μm)	1	1	1
N_d $(cm\text{-}3)$	4×10^{17}	4×10^{17}	4×10^{17}
n^+ (cm^{-3})	10^{19}	10^{19}	10^{19}
a (μm)	0.15	0.15	0.15
$\Phi_{bi}(Au)$ (eV)	1.71	1.68	1.68
R_c $(\Omega\text{-}cm\text{-}2)$	~10^{-4}	~10^{-4}	~10^{-4}
μ_p $(cm^2/V\text{-}sec)$	600	100	83
v_s (cm/sec)	1.08×10^7	0.86×10^7	0.83×10^7
κ_{th} $(W/^oK\text{-}cm)$	30	14	11
Θ $(^oK/W)$	0.73	1.57	2.03

Figure 6.   DC I-V Characteristics for the P-Channel MESFET at 300 °C (Gate Bias Voltages start at Vg=0 v and are in 1 v steps).
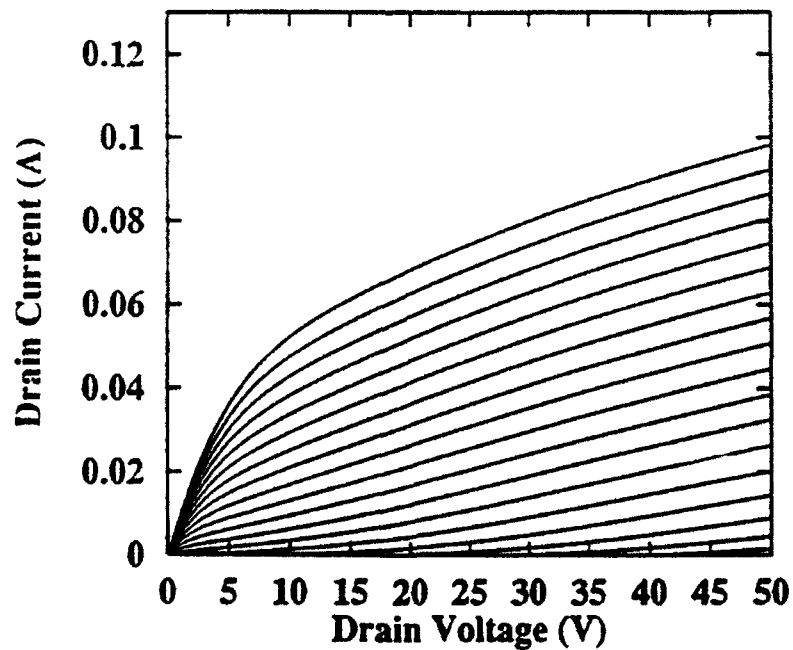

Figure 7.   DC I-V Characteristics for the P-Channel MESFET at 500 °C. (Gate Bias Voltages start at Vg=0 v and are in 1 v steps).
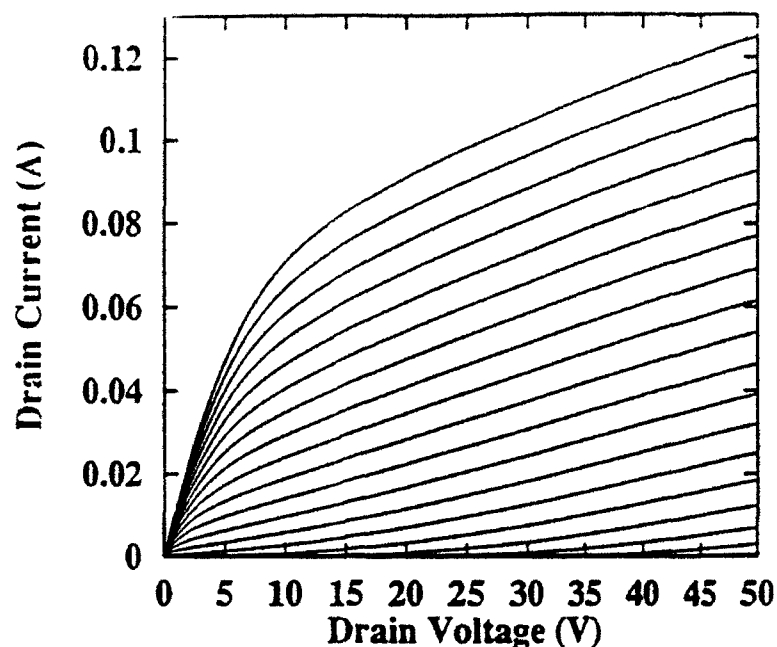
15

Figure 8.   DC I-V characteristics for the P-channel MESFET at 650 °C. (gate bias voltages start at Vg=0 v and are in 1 v steps).

pronounced due to significant activation of charge carriers at this temperature. The increase in free hole density dominates over the decrease in hole transport at the elevated temperature. RF simulations for the device operated in a class A amplifier at 4 GHz are shown in Figures 9, 10, and 11 for operation at the three temperatures. As shown, the diamond MESFET is capable of good RF performance. The device produces about 25.5 dbm of RF output power and about 17% power-added efficiency, essentially independent of operation temperature. Again, this is due to increased activation compensating for reduced hole transport at the elevated temperature. The linear gain increases from about 5 db at 300° C to about 8 db at 650° C. These results are encouraging and indicate that diamond power MESFETs have significant potential, especially for high temperature operation where devices fabricated from conventional semiconductors cannot be operated.
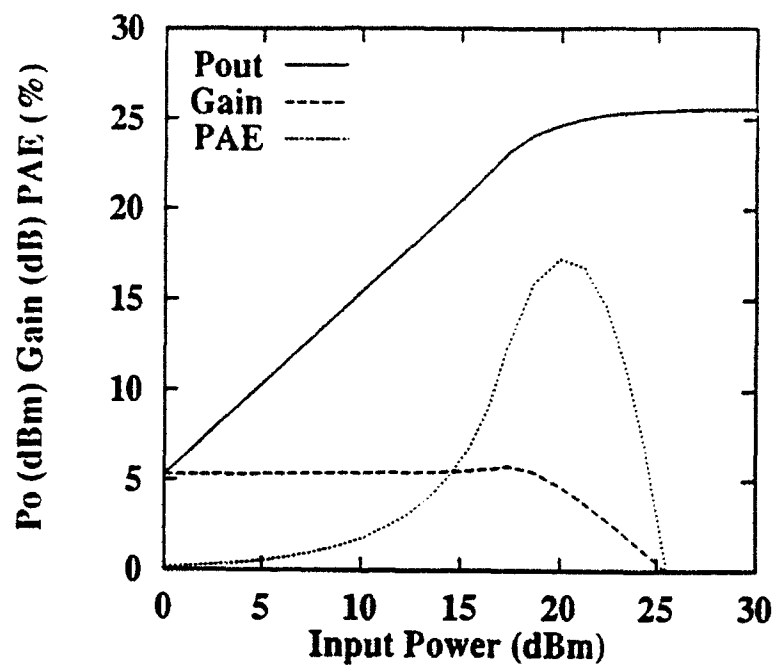
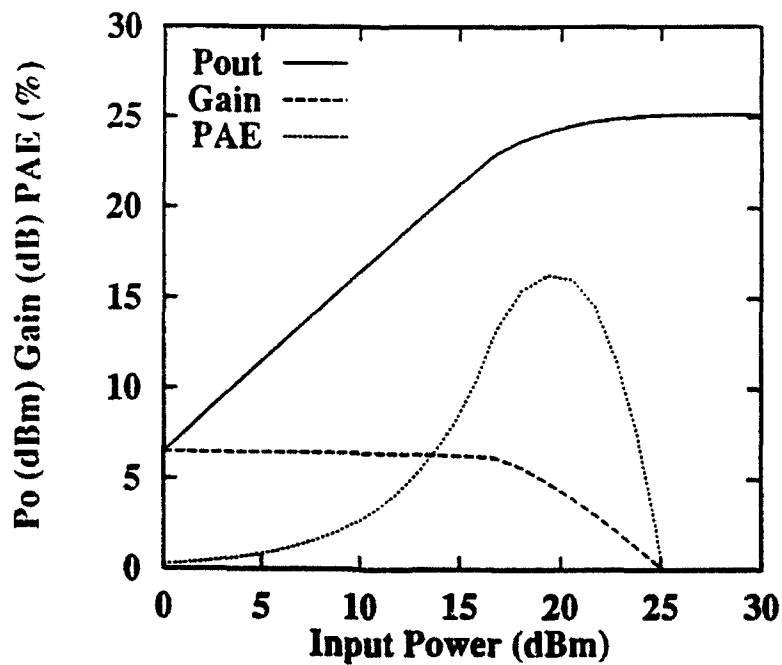Figure 9.   RF Performance for the P-Channel MESFET at 300 °C.

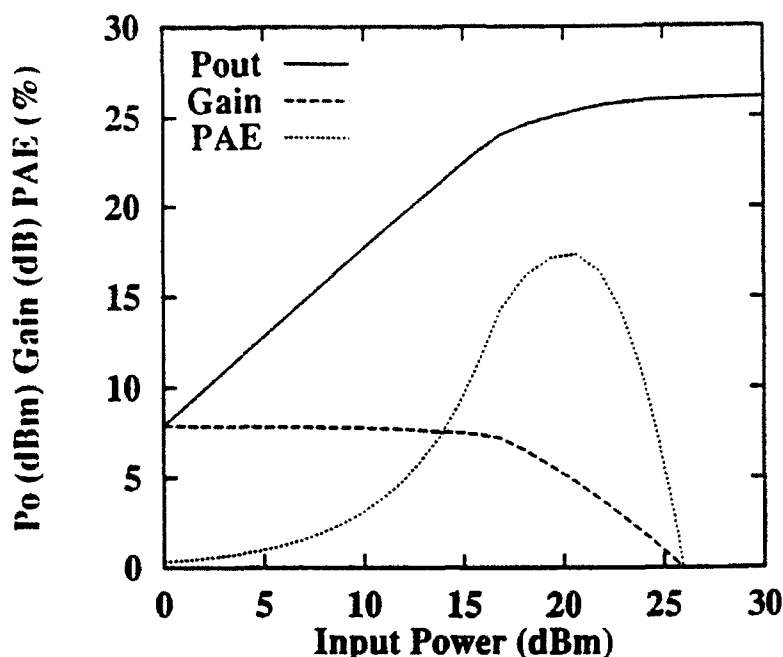Figure 10.   RF Performance for the P-Channel MESFET at 500 °C.

17

Figure 11.   RF performance for the P-channel MESFET at 650 °C.

E. Discussion

Our simulated dc I-V curves for each device agree well with the corresponding measurements as shown in the Figures. Pentode-like or triode-like behavior occurs at the appropriate active carrier levels. The active carrier density depends upon doping level and temperature because of the dependence of activation on temperature. There also appears to be significant dependence of the shape of the I-V curves on bound change at the interface because of backgating. Since bound charge depends upon processing and fabrication technology, the simulations may require recalibration for different fabrication processes.

The DC curves at all three temperatures indicate high currents with the highest currents at the highest temperature (650 °C). As the temperature rises, two antagonistic effects compete. The carrier activation increases and the mobility decreases. It appears that the two effects cancel to large extent, as observed in the essentially temperature independent DC and RF performance.

F. Conclusions

Polycrystalline and monocrystalline diamond FETs have been numerically modeled. Agreement with experiment confirms present understanding of the major physical processes in these devices. Allowing for the tradeoff between increased activation and reduced mobility, promising RF performance is predicted for diamond FETs.

G. Future Research Plans and Goals

Single-crystal diamond MESFETs will be simulated in more detail. The effects of bound charge at the surface and the channel/substrate interface will continue to be investigated. The RF operation of the devices over a range of operating temperatures will be further examined.

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