

Northeast Semiconductor, Inc.

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September 30, 1992

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Dr. Erhard Schimitschek, Scientific Officer  
ATTN: Code 808  
REF: N00014-91-C-0222  
Naval Ocean Systems Center  
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Re: Contractor : Northeast Semiconductor, Inc.  
Address : 767 Warren Road, Ithaca, NY 14850  
Req. No. : s405811srv02/17 APR  
Contract No. : N00014-91-C-0222  
Report Date : September 30, 1992  
Report Title : 8th Monthly Technical Report  
Period Covered : 09/01/92 through 09/30/92

Dear Dr. Schimitschek:

Northeast Semiconductor, Inc. encloses its Eighth Monthly Technical Report (Line Item #0002) pursuant to the provisions of contract Section B entitled, "Supplies or Services and Prices/Costs" for the period of September 1, 1992 through September 30, 1992.

**Innovative Techniques for the Production of Low Cost 2D Laser Diode Arrays**

1.0 OBJECTIVE

The primary objective of this program is to develop a low cost, high yielding methodology for processing, packaging and characterization of MBE grown two dimensional high power laser diode arrays. Projected increases in overall yield of AlGaAs diode lasers would reduce manufacturing cost from the current \$10 to \$20 per peak watt to below \$3 per peak watt. Emphasis will be placed on innovative packaging techniques that will utilize recent advances in diamond heat sinking technology.

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## 2.0 PROGRAM METHOD AND SCHEDULE

This program consists of four phases which will demonstrate reduced manufacturing cost and improved device performance of NSI's MBE laser diode arrays. The four phases listed below will result in milestones in processing, packaging, and testing along with delivery of the specified number of 5-bar laser arrays.

(i) Concept phase: Conceptual design and organization of this phase II program. NSI will utilize the current side cooled package to manufacture 5-bar laser diode arrays for base line evaluation. (Deliverables: 3 5-bar arrays.)

(ii) Backplane phase: Investigation of backplane cooling technologies that incorporate BeO, W/Cu and CVD diamond materials. This phase will also include the completion of room temperature photoluminescence development. (Deliverables: 5 5-bar arrays.)

(iii) Optimize Backplane phase: Investigate and optimize various backplane technologies. This will involve evaluating different packaging materials and processes pertaining to thick films, copper, direct bond copper to BeO, W/Cu and CVD Diamond. Feasibility and cost will be dominant factors. (Deliverables: 5 5-bar arrays.)

(iv) Liquid Cooled phase: The best proven backplane technology developed to date will be incorporated into a innovative liquid cooled assembly. Due to the numerous potential backplane schemes, this package type will be specifically designed to be compatible with the preferred backplane technology chosen. (Deliverables: 5 5-bar arrays.)

The following global issues not mentioned above will be investigated continuously throughout all four phases of this program:

- (1) design and development of a mask set to increase processing and packaging yields,
- (2) development and updating of MBE growth software,
- (3) design and development of an in-house facet coating station,
- (4) evaluation of different facet coating materials,
- (5) development of automated tests,
- (6) life test and burn-in development.

The master schedule for this program is shown in Table 1. Revisions have been made effectively delaying the second set of deliverables until the end of November. Each phase will require



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wafer growth, processing, assembly and test. The schedule shows the estimated number of sample fabrications and tests, as well as the time of hardware deliverables and reports.

### 3.0 PROGRESS THIS PERIOD

#### 3.1 Wafer Growths

This past month, NSI's MBE facility conducted numerous experiments to define optimal laser growth conditions. Due to lower than desired room temperature photoluminescence (PL) intensities associated with laser material from the new facility, a series of cladding layer experiments were performed. The test wafers grown consisted of undoped, thin layers simulating the actual laser structure but only taking half as long to grow. Growth parameters explored were substrate temperature, arsenic beam flux, and superlattice relationships to PL intensities. Greater than 500X improvement was achieved in quantum well PL intensities as a result.

Several single layer GaAs and AlGaAs dopant calibration samples were also grown. Hall measurements indicated lower than expected dopant concentrations in the  $Al_{0.45}Ga_{0.55}As$  layers. Tests conducted on the GaAs layers corresponded to expected values and proved to be confidently reproducible. Investigation will continue this month to characterize the dopant behavior in AlGaAs layers grown in the new facility. Laser wafers are currently being grown with corrections factored into the structure to account for the lower dopant concentration in the AlGaAs cladding layers.

#### 3.2 Processing

Efforts this past month focused on improvements pertaining to the metalization of NSI's laser wafers. More stringent visual inspection of the laser diode bar facets, over the past two months, indicated that the largest failure mechanism was associated with defects related to the p-side metalization. Defects ranged from facet coat "shadowing" by protruding metal to physical encroachment of the emitting regions has a result of hinging and stretching of the metalization. An experiment was initiated in which fifteen samples with different metals, thicknesses, and annealing cycles were evaluated (see figure #1). The goal of the exercise was to identify possible alternatives that utilized thinner metalization and/or metalization without the "soft" pliable Au while providing a solderable surface. Seven of the schemes mentioned in figure #1 provided a solderable surface using 70In/30Pb and RA flux. All seven that passed utilized Au as the final layer with the last two samples using only 1/2 the Au thickness. Further samples are planned to be fabricated to determine the minimum amount of gold that can still provide the solderable surface on the p-side. These test will also be repeated in NSI's high temperature vacuum furnace without flux.

This will simulate the actual bonding procedure used for laser diode bars.

Minor difficulties were experienced with adhesion of Ti/Pt/Au deposited onto BeO backplanes. This metalization layer provides the solderable surface to secure the laser diode submounts to the backplane. All three of the first batch processed exhibited poor adhesion and were unacceptable for packaging. A more rigorous cleaning and bake-out procedure has improved the adhesion.

### 3.3 Testing

Considerations this month have gone into a conceptual design of a test vehicle for the individual submounts that will be utilized in the backplane package. Obstacles that must be overcome include the small physical part size and insuring a good n-side contact to the top of the laser diode bar. Probe card and metal impregnated elastomer technology will be explored.

### 3.4 Assembly and Packaging

Dimensional accuracy of the laser diode submount was the largest factor this past month in packaging. Figure #2 shows the wide variation in the CVD diamond submounts that were to be used in the first set of backplane deliverables. The nominal value for thickness and width were 250 $\mu$ m and 570 $\mu$ m respectively. The variations shown are totally unacceptable. To improve dimensional accuracy, future diamond submounts were to be sorted and possibly lapped by the vendor. No new diamond pieces have arrived at this time. The inability to deliver and poor product quality produced by our selected CVD diamond manufacturer has forced NSI to explore different vendors.

Prototypes utilizing W/Cu submounts have been fabricated on direct bond copper indexed backplanes. The backplanes are electroplated with approximately 15 $\mu$ m of 100% In for bonding the submounts to the indexed stripes. Construction of these samples has aided in the mechanical design of fixturing that will be needed for proper assembly. A "comb" fixture has been design and is currently being fabricated to position the submounts on the indexed backplane. This design takes advantage of the surface tension of the solder on the backplane to self align the submounts.

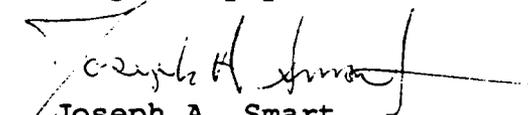
## 4.0 PLANS FOR OCTOBER

NSI will continue to evaluate different metalization schemes for both the P and N sides of the laser diode bar. Emphasis will be placed on decreasing the thickness of Au to reduce hinging and encroachment of metalization near the emitting regions.

Packaging efforts will focus on fabrication of backplane cooled laser diode arrays. New fixturing should arrive early in

October to aide in the assembly of these units. Addition CVD diamond, Cu, and W/Cu submount vendors will be contacted to insure delivery of acceptable piece parts for this program.

Very truly yours,



Joseph A. Smart,  
Principal Co-Investigator  
Northeast Semiconductor, Inc.

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Encl: 1 Copy of 8th Monthly Technical Report

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DEPARTMENT : LASER PRODUCT LINE PROJECT(S) : ONR PHASE II N00014-91-C-0222	KEY ○ : Start Task ◇ : Milestone △ : Completion Date 1 ▽ : Completion Date 2	DATE : SEPTEMBER 30, 1992 PREPARED BY : GEOFFREY T. BURNHAM APPROVED BY :																								
		1991				1992				1992																
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PAGE 1 of 2 MILESTONES																										
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SYSTEM QUALIFICATION																										
WAFER STARTS																										
REVIEW INCOMING INSPECTION																										
UPDATE GROWTH SOFTWARE																										
WAFER PROCESSING																										
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DEVELOP ROOM TEMP PL TEST																										
DEVELOP FACET COATING																										
PACKAGING																										
1-BAR SUBMOUNTS																										
5-BAR ARRAYS																										
CURRENT																										
Cu BACKPLANE																										
CVD DIAMOND																										
EGW COOLED																										
TESTING																										
DEVELOP AUTOMATED TESTS																										
LIFE TESTS/BURN-IN																										

TABLE 1. MASTER SCHEDULE FOR SBIR PHASE II  
 CONTRACT NO. N00014-91-C-0222



SAMPLE NUMBER	METAL TYPE	METALIZATION	MEASURED THICKNESS	ANNEAL CYCLE	APPEARANCE AFTER ANNEAL	SECOND METALIZATION	TOTAL THICKNESS	COMMENTS	SOLDER TEST
1A	P-metal control	Ti-300,Pt-1200, Au-2000	3510Å	60sec-300°C(A) 20sec-420°C(A)	gold - good			thick hinges peels off	PASS
1B	P-metal	Ti-300,Pt-1200, Au-2000	3510Å	180sec-380°C(B) 10sec-430°C(B)	gold - good			thick hinges peels off	PASS
2A	N-metal control	Ge-330,Au-670, Ni-330, Au-2500	4538Å	A	gold - hazy				FAIL
2B	N-metal	Ge-330,Au-670, Ni-330, Au-2500	4538Å	B	gold - hazy				FAIL
3A	N-metal	Ge-330,Au-670	1250Å	A	speckled silver - gold	Ti-300,Pt-1200, Au-2000	4965		PASS
3B	N-metal	Ge-330,Au-670	1250Å	B	speckled silver - gold	Ti-300,Pt-1200, Au-2000	4965		PASS
4A	N-metal	Ge-330,Au-670, Pt-1200, Au-2000	4810Å	A	silver speckle				FAIL
4B	N-metal	Ge-330,Au-670, Pt-1200, Au-2000	4810Å	B	silver speckle				FAIL
5A	P-metal	Ti-300,Pt-1200	1384Å	A	silver				FAIL
5B	P-metal	Ti-300,Pt-1200	1384Å	B	silver				FAIL
6A	N-metal	Ge-330,Au-670	1250Å	A	uniform silver - gold	Ti-300,Pt-1200	2634		FAIL
6B	N-metal	Ge-330,Au-670	1250Å	B	uniform silver - gold	Ti-300,Pt-1200	2634		FAIL
7A	N-metal	Ge-330,Au-670, Pt-1200,Au-2500		B	silver - gold	Ti-200,Pt-1200 Au-1000			PASS
7B	P-metal	Ti-300,Pt-1200, Au-1000		B	gold				PASS
8A	P-metal	Ti-300,Pt-1200, Au-1000		No Anneal	gold				PASS

FIGURE #1 METALIZATION EXPERIMENT  
 CONTRACT NO. N00014-91-C-0222

PIECE NUMBER	THICKNESS $\mu\text{m} \pm 5\mu\text{m}$		WIDTH $\mu\text{m} \pm 5\mu\text{m}$	
	left	right	left	right
1	330	330	606	608
2	300	300	604	604
3	460	324	550	550
4	418	300	590	590
5	346	378	566	566
6	304	330	550	550
7	302	344	550	550
8	270	288	588	586
9	336	466	570	570
10	372	390	572	578

FIGURE #2 MEASURED CVD DIAMOND DIMENSIONS  
CONTRACT NO. N00014-91-C-0222