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Quarterly Progress Report
for

**Design and Packaging of Fault Tolerant
Optoelectronic Multiprocessor Computing Systems**

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University of California, San Diego
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Principal Investigator:

Sing H. Lee
(619) 534-2413

Program Manager:

William Miceli
(703) 696-4715

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1, Introduction

During this quarter, we continued our efforts on (i) studying alignment schemes for packaging and fabricating components for CMTM packaging, (ii) creating generalized e-beam fringe writing algorithms for automatically generating different types of HOEs for optical interconnects, and (iii) design of switching elements in twin butterfly networks with parallel testing features built-in. The results are summarized below.

2. Progress Summary

2.1 Opto-Electronic Packaging

In order to reduce the the volume of the opto-electronic packaged systems, it is necessary to achieve low f-number lenses. One method of achieving low f-number optical elements is to utilize stacks of several higher f-number lenses. Last quarter we have investigated the alignment of microstructures on the opposite side of a substrate. During this quarter we are investigating the alignment of stacking two diffractive elements on two substrates facing each other (Fig.1). One conventional approach is to print alignment mask on the surfaces of the two substrates and align them by viewing through the microscope of a mask aligner. Another approach which is more accurate is to use Moire patterns, as shown in Fig.1. Linear gratings were printed on the surface of the substrates by using e-beam writer. When the surfaces of the substrates are stacked on top of each other, the superposition of the two gratings will produce a Moire interference pattern, which is very sensitive to the misalignment of the two gratings. Assuming grating period of $0.8 \mu\text{m}$, a lateral alignment accuracy of $0.2 \mu\text{m}$ and an angular alignment accuracy of 10^{-4} radians can be expected. By using grating grooves etched into both substrates, some space is created for applying UV curing epoxy without creating an unwanted intermediate layer between the substrate surfaces. As soon as the substrates are aligned, a UV light source

can be used to cure the epoxy. The experiments will be carried out next quarters.

On building a packaged CMTM (Correlation Matrix-Tensor Multiplier) system, we have started the fabrication of the two linear gratings and two fresnel lenses on the same surface of an optical flat. Due to the need for the very fine alignment and small feature sizes (approaching $1 \mu\text{m}$) for operation at 514.5 nm , we are utilizing a e-beam direct write method for the multilevel phase micro-optics. In this way, we can achieve alignment accuracies of $0.1 \mu\text{m}$ between masking steps. In order to determine the etch time for the desired depth in a Reactive Ion Beam Etcher, an etch rate analysis for the low expansion glass was under taken. Samples were etched for 30 sec, 1.5 min, 2.5 min, and 3.5 min. A statistical procedure was used to find the best fit linear etch rate. We have also designed a second packaged CMTM system for IR (800-850nm) operation. The IR system will permits compactness, since laser diode can be used.

To take advantage of in-situ recording in photorefractive crystals (PRCs) for self alignment, we began to investigate various methods of applying PRCs to optoelectronic packaging. The three possible packaging schemes (shown in Fig.2) that use PRCs as the key components are being designed. In the first scheme [Fig.2.(a)], a reflective volume holographic lens is recorded in a PRC which images an input array onto the output detector array. In the second scheme [Fig.2.(b)], a 4×4 lenslet array is recorded in two separate PRCs; arbitrary one-to-one, one-to-many and many-to-one interconnections can be realized by properly controlling the off-axis angles of the collimated beam inside the substrate during recording and holographic superposition. In the third scheme [Fig.1.(c)], the input array is imaged onto the PRC, in which the Fourier transformed interconnection weights for each input pixel are stored locally with respect to the position of the corresponding input pixels; the Fourier transform of the reconstruction gives the weighted output array. We plan to assemble these three packaged systems and demonstrate their self-alignment capability next quarters.

2.2 Opto-Electronic CAD

In order to create a CAD system, in which given a netlist, array of different HOEs can be generated automatically, we need to create generalized algorithms to generate the different types of fringes (for different HOEs) needed for e-beam fabrication. Because the e-beam machine is capable of creating trapezoids with only several discrete angles, generalized algorithms for creating such HOEs are not trivial. Fig.3 shows various graphical shapes of e-beam data required to create a linear grating, cylindrical lens and spherical lens.

Next quarter our research will continue on: (1) development of CGH CAD fringe drawing algorithms for different types of fringes, (2) modular design of analytic type CGHs and extend the design to numeric type CGHs for optical interconnects, (3) continued investigation of layout algorithms for solving the PE or CGH placement problem in an interconnect network.

2.3 Fault Tolerance and Testing in Opto-electronic Computing

We have generated an optoelectronic netlist for a 16-node twin butterfly interconnection network so that development of physical layout algorithms can commence. Twin butterfly is most noted not only for low contention but also for its fault tolerance. Fault tolerant operation requires that the switching elements (SE) in the interconnection network be designed for efficient testing and reconfiguration after the network has been packaged and put to use.

We have outlined the switch element design for parallel testing to support fault tolerant operation in a twin butterfly interconnection network in the last quarterly report. To explain about the testability of our SE design, we assumed the stuck fault model for the SLMs and detectors. In this model, an interconnect is assumed to be shorted to the power supply (stuck-at-1, or s-a-1) or shorted to the ground (stuck-at-0, or s-a-0). This simple model has also been extensively used in testing conventional digital

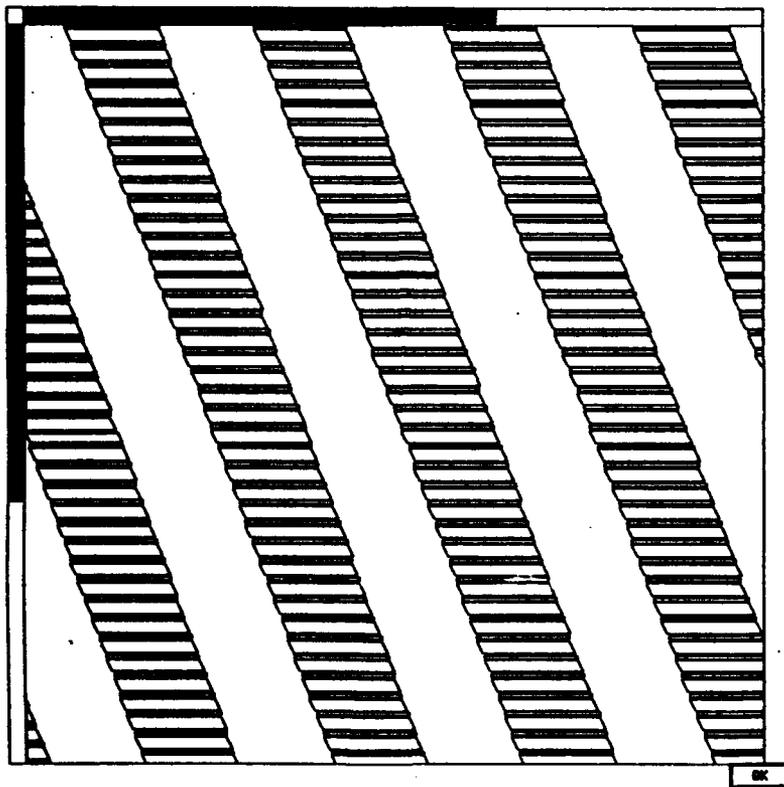
circuits. The basic approach is to assume a particular interconnect stuck at logical 1, for example, and try to provide the necessary system input to force this interconnect to logical 0. If the observed output confirms that the state of this interconnect is at logical 0, then we can conclude this interconnect is not stuck at logical 1. We have to perform another test on whether the interconnect is stuck at 0 before concluding it is fault free. Both s-a-1 and s-a-0 tests are repeated for all interconnects within a circuit to detect and locate faults. We have added extra circuitry in the switching element design in order to supply the test pattern to the optoelectronic I/O of each SE and to observe the result through the modulators. This addition facilitates parallel optical testing of the optoelectronic I/O on the entire chip. In addition to stuck-at faults, the test strategy we are studying also tests for bridging fault between the detectors, which is the shorting between neighboring detector signals at the multiplexer.

The CMOS logic in design that is dominated by the message queue is also subject to imperfect fabrication. However, the overhead to fully test the CMOS circuitry (which will be many more modulators and detectors and a much more complicated control scheme) outweigh the benefit gained. We therefore consider only functional testing of the message queues to achieve balance between fault coverage and grain size. We are now investigating the control mechanism to achieve automatic fault masking and reconfiguration of the twin butterfly network.

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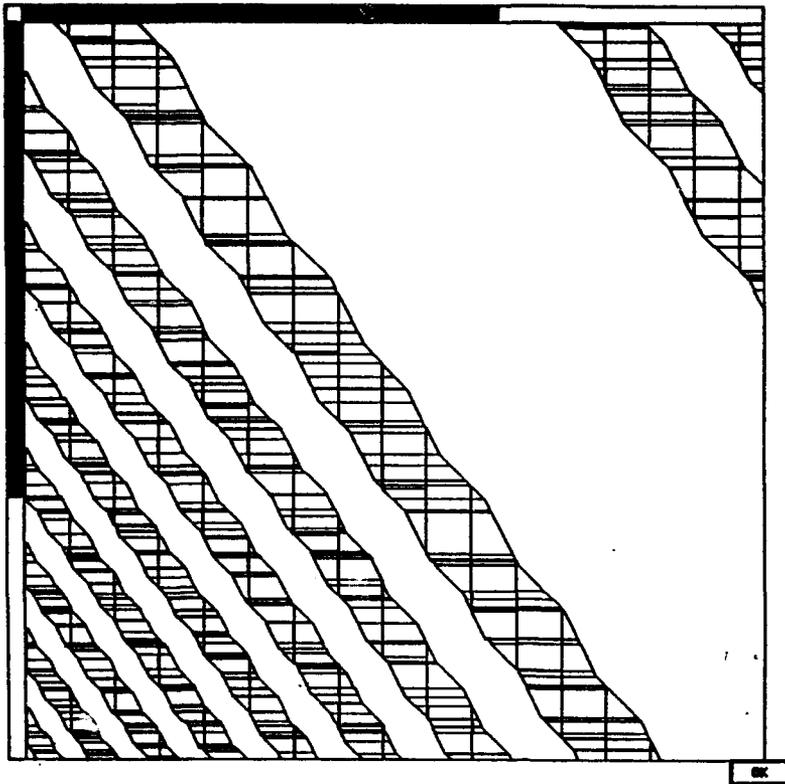
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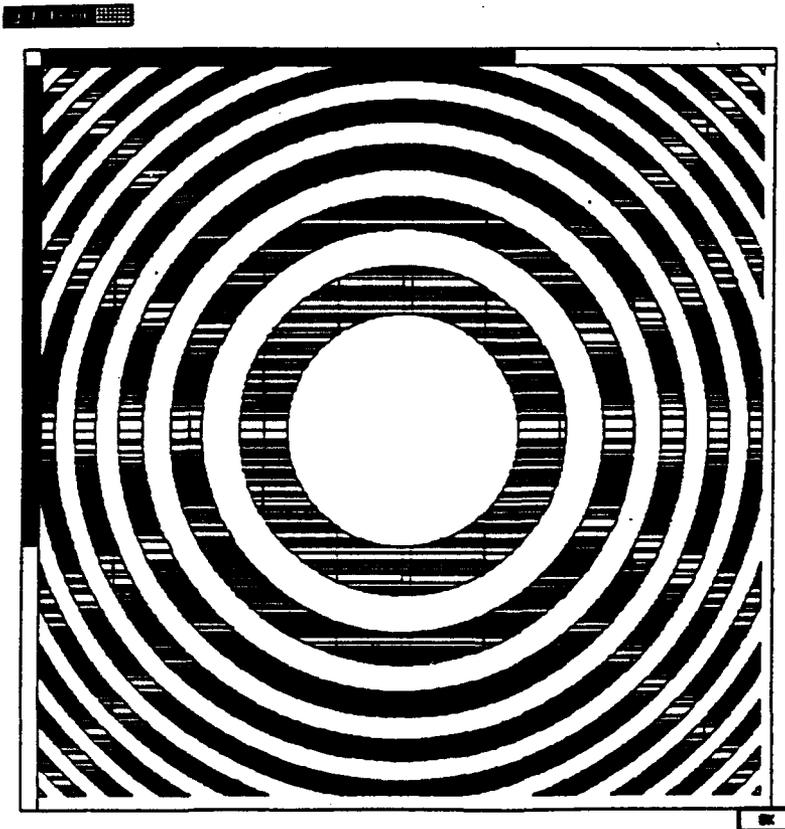


(a)

Fig.3. Graphical shapes of e-beam data on (a) linear grating, (b) cylindrical lens and (c) spherical lens, taken from the computer screen. The e-beam writing algorithms control the orientation of the lines.



(b)



(c)