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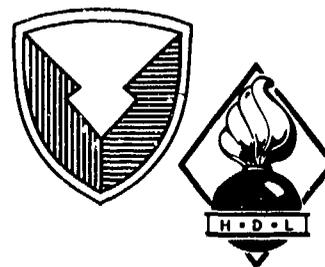
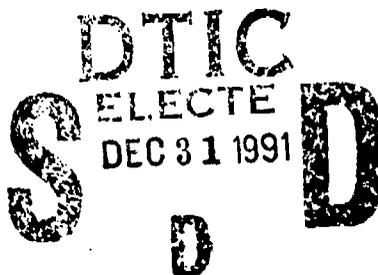
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Preparation of Ferroelectric Samples for Electrical and Radiation Characterization Studies

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13. ABSTRACT (Maximum 200 words) Procedures have been developed for preparing ferroelectric film samples for electrical and radiation characterization. The procedures discussed herein focus on quick turnaround of samples and the ability to handle a number of different kinds of ferroelectric materials and substrates. New methods of defining the sputtered platinum electrodes and attaching the sample die to suitable packages are also discussed.				
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Contents

1. Introduction	5
2. Substrate Preparation	6
3. Capacitor Fabrication Procedure	7
4. Mounting and Bonding of Ferroelectric Samples	10
5. Conclusions	11
Acknowledgements	12
References	12
Distribution	15

Figures

1. Ferroelectric capacitor cross section.....	5
2. Shadow mask and holder	8
3. Sputtered platinum electrodes on PZT	8
4. Etched PZT sample with electrodes.....	9
5. Mounted and bonded ferroelectric sample.....	11

Table

1. Samples used for fabricating ferroelectric capacitors.....	6
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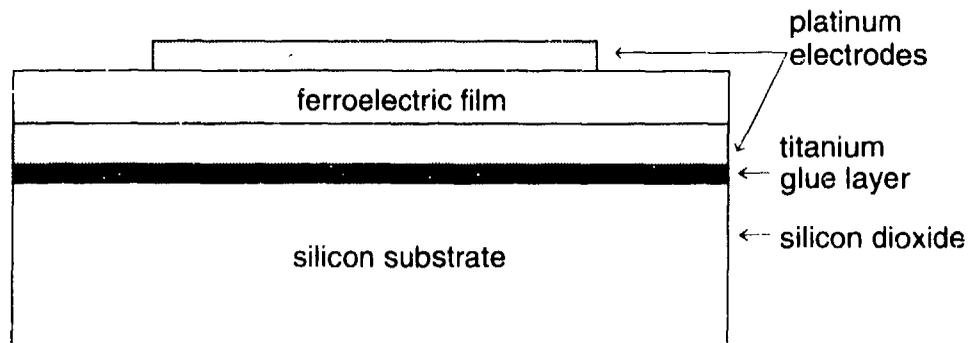
1. Introduction

Techniques have been developed for preparing ferroelectric films for electrical characterization studies and radiation hardness assessments. In recent years, considerable interest has been rekindled in the use of these ferroelectric materials in nonvolatile memory applications [1-3]. The evaluation of such characteristics as dielectric constant, coercive field, remanent polarization, fatigue, retention, and radiation hardness are especially critical to assessing the use of these materials in nonvolatile memories intended for Army advanced electronics systems [4-5]. The procedures discussed in this report are intended to provide suitable test samples quickly so as to maximize the number of different samples that can be evaluated. Evaluating many different samples in a given time is of particular importance, since no single ferroelectric material has yet emerged as the optimum material for nonvolatile memory applications, and many different material samples must therefore be studied.

The basic structure used for both electrical and radiation hardness evaluations is the ferroelectric capacitor shown in figure 1. The bottom part of this structure, which serves as the physical support for the capacitor, is a silicon wafer that has been thermally oxidized to provide an insulating layer. The actual capacitor structure consists of a suitable bottom metal electrode, the ferroelectric film, and the top metal electrode whose area defines the capacitor value. The capacitor can be probed directly or mounted and bonded into suitable packages for testing.

Many different ferroelectric samples were prepared during the course of this effort. Some were obtained with the ferroelectric layer already deposited onto a suitable conducting layer on a thermally oxidized silicon substrate, although a few samples were obtained with the ferroelectric deposited directly on a sapphire substrate. In other cases, the oxidized silicon substrates with a conducting layer were prepared

Figure 1. Ferroelectric capacitor cross section.



at the laboratory and then sent out for the ferroelectric application. The ferroelectric layers evaluated were deposited either by a sol-gel spin-on process or by laser ablation [6-9]. Table 1 lists the various types of ferroelectric materials used during this effort, as well as the relative thicknesses and deposition methods.

Table 1. Samples used for fabricating ferroelectric capacitors

Sample type	Deposition method	Film thickness (kÅ)
PZT on platinum	sol-gel	2-8
PZT on sapphire	sol-gel	4.5-7.2
PZT on platinum	laser ablation	2-20

2. Substrate Preparation

Silicon wafers having $\langle 100 \rangle$ orientation, of various resistivities and dopant types, were used as suitable substrates for the ferroelectric material applied by outside sources. These wafers were first degreased with trichloroethane, acetone, and isopropanol sprays. This process was followed by a 10-minute "piranha" bath, consisting of three parts sulfuric acid to one part hydrogen peroxide, after which the wafers were subjected to a full RCA clean [10]. Just before the oxidation step, a commercial rinser/dryer was used to rinse the wafers to better than 16-M Ω resistivity and then dry them in a heated nitrogen atmosphere. The cleaned silicon wafers were thermally oxidized to produce oxide layers 800 to 2500 Å thick. For the thinner layers up to about 1000 Å, a dry oxidation process was used; for the thicker layers, a pyrogenic steam process was used. Since the oxide thickness and growth conditions were not critical, the procedure used to oxidize the wafers depended upon the availability of the process furnace tube when the oxidations were performed.

Because of its many desirable properties, platinum was chosen as the material for both the bottom and top electrodes. The platinum electrode was deposited in a multitarget sputtering system. Because platinum adheres poorly to silicon dioxide, a glue layer is required to provide a thermally and physically stable metal electrode. For this work, the glue layer was titanium, which was sputtered to a thickness of approximately 300 Å. Immediately following the glue layer deposition (without breaking vacuum), platinum was sputtered to a thickness of between 1500 and 2000 Å. The sputtering system was pumped down to a pressure of 4×10^{-4} Pa before sputtering. A total input power of 60 W across a 12.7-cm diameter target, a 1.33-Pa pressure of argon, and a separation of approximately 1.5 cm between the sputtering target and the substrate were the sputtering conditions for both the glue layer and the platinum.

As an evaluation of the suitability of the prepared substrates for the subsequent ferroelectric material processing, test samples of the metallized substrates were placed in a rapid thermal processing system and ramped from room temperature to 700 °C in oxygen, maintained at 700 °C for 20 minutes, and then allowed to cool to about 250 °C before being removed into the room ambient. Visual inspection of the platinum metal showed no apparent degradation as a result of the thermal cycling.

3. Capacitor Fabrication Procedure

For quick turn-around preparation, all samples were cut to less than 1.2-cm square, so that they could be mounted in the special fixture designed to clamp together the sample and shadow mask that defined the upper electrode geometry. Obtaining well-defined geometries using a shadow mask in sputtering systems can be very difficult, because the high kinetic energy of the sputtered particles tends to force them under the edges of the shadow mask wherever mask-to-substrate contact is poor. Because of these problems, silicon wafers were used for making the shadow mask, since they are extremely flat and can be micromachined to produce the precise openings needed to define the capacitor top electrode [11]. We fabricated silicon shadow masks from 2-mil-thick <100> silicon wafers using silicon micromachining techniques to produce an array of square openings 6 mils on a side. The holder and a photomicrograph of a section of the silicon shadow mask are shown in figure 2. After the sample and shadow mask are mounted and secured in the fixture, the assembly is placed in the sputtering system for the platinum deposition.

Two thickness ranges of platinum were used for the samples prepared during the course of this work. Top platinum electrodes of approximately 1500-Å thickness were deposited for electrical characterization and radiation hardness studies. In addition, some samples were also prepared for photovoltage measurements. For these measurements, the platinum thickness was reduced to approximately 200 Å to permit light to penetrate the electrode. At the same time as the thin electrode deposition, clear glass cover slides were also coated so that the actual thickness of the electrodes could be measured. However, the thickness measurement was difficult to obtain by typical profilometer methods because of the lack of a definitive step at the platinum edge. Nevertheless, the slides provided a means to assess the light transmission characteristics of the thin electrodes. Figure 3 shows a typical ferroelectric sample with the sputtered shadow mask electrodes.

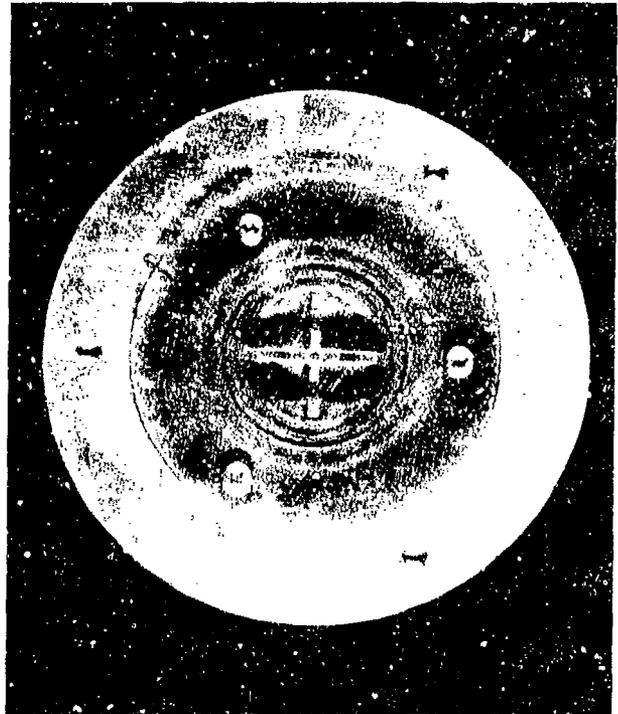
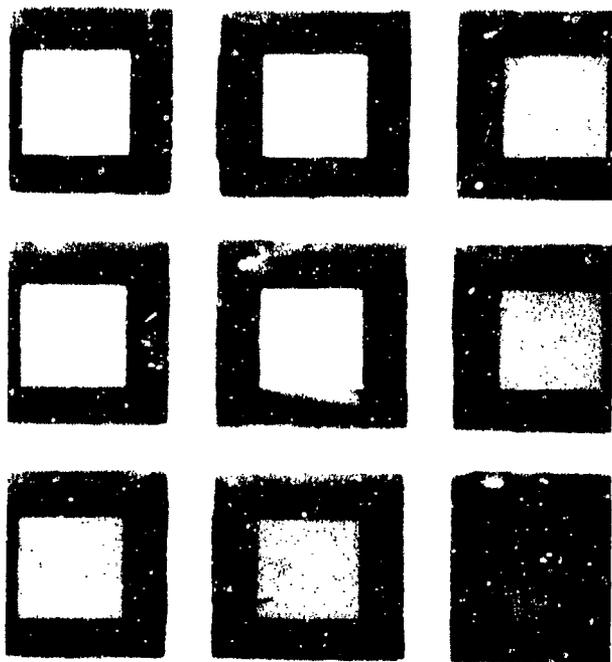


Figure 2. Shadow mask and holder.

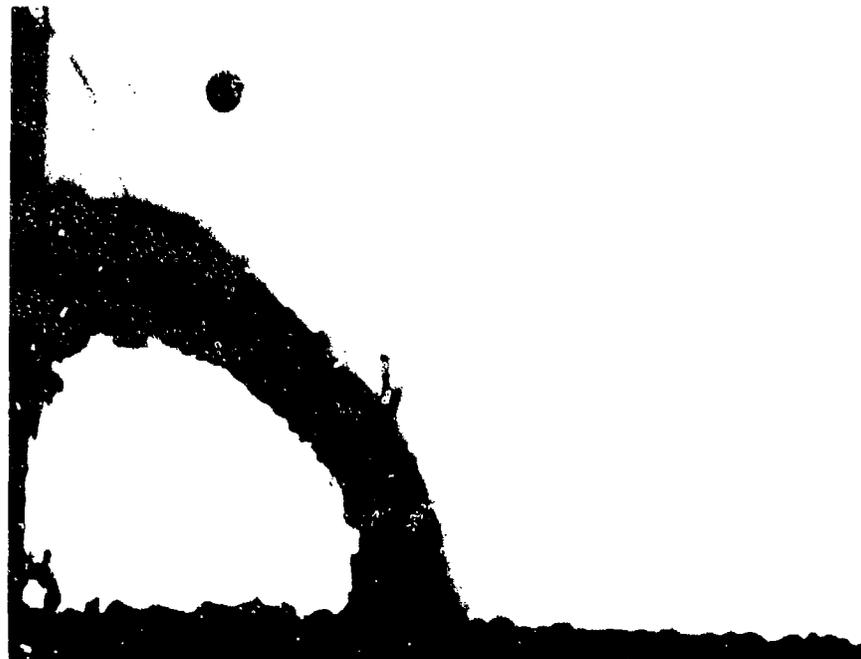
Figure 3. Sputtered
platinum electrodes
on PZT.

Following the top electrode deposition, it was necessary to remove a small region of the ferroelectric film to expose the bottom platinum electrode. For the lead zirconate titanate (PZT) ferroelectric films, we accomplished this removal by placing a very small drop of either 7:1 buffered HF etch or straight HF on the sample. The etchant was allowed to completely evaporate, and a drop of 5-percent nitric acid was then placed on the remaining lead-rich residue to further clear the region. Depending on the thickness and composition of the film, this process was repeated if necessary until no further change was noticed. For the barium titanate films, straight HF alone was employed.

For many samples, this chemical etching procedure was sufficient to completely expose the bottom platinum. For other samples, the area had to be lightly mechanically scrubbed with the back end of a wooden cotton swab stick or a metal probe to completely remove the residue. The step formed between the PZT layer and the underlying exposed platinum provided a convenient way of measuring the thickness of the PZT film with a profilometer. A ferroelectric sample with the top electrodes and exposed bottom electrode is shown in figure 4.

For the samples that were intended to be probed directly, the above procedures completed the fabrication process. However, a number of electrical and radiation hardness characterization studies required that the samples be mounted and bonded into suitable packages.

Figure 4. Etched PZT sample with electrodes.



Because the sample size used in the shadow mask holder is larger than the cavity size of the packages, the platinum sputtered samples were manually scribed into smaller pieces with a diamond scribing fixture.

4. Mounting and Bonding of Ferroelectric Samples

Several issues had to be addressed so that the various ferroelectric samples being prepared could be adequately mounted and bonded. Because a few of the ferroelectric samples obtained were prepared on sapphire substrates, a die-mounting procedure that could be used with silicon as well as nonsilicon samples was desirable. Initially, sample die were mounted in 16-pin dual in-line packages (DIP's) with a two-part epoxy die attach method. Sufficient epoxy is placed in the package cavity so that when the die is pressed into the epoxy, some of the epoxy squeezes out and covers the lower portion of the edge of the die. This epoxy must be cured by being baked in an air atmosphere oven. For the initial work, a 90-minute bake at 100 °C was routinely used. Later on, lower bake temperatures with longer times were also employed. However, despite the different curing procedures, considerable difficulty was experienced with all samples during the subsequent wire-bonding operation, which used a thermosonic wire bonder. It was observed that most of the ball bonds failed to stick to the top and bottom platinum electrodes. In addition, a portion of the platinum electrodes directly under the gold ball often pulled off during the bonding process. These problems were so severe on the thermosonic bonder that an older thermocompression bonder was tried, since it was believed that the ultrasonic energy was somehow causing bond failures with the gold wire to platinum metal bond. Using this older bonder, we were able to obtain some good bonds, but the vast majority failed, as on the thermosonic unit.

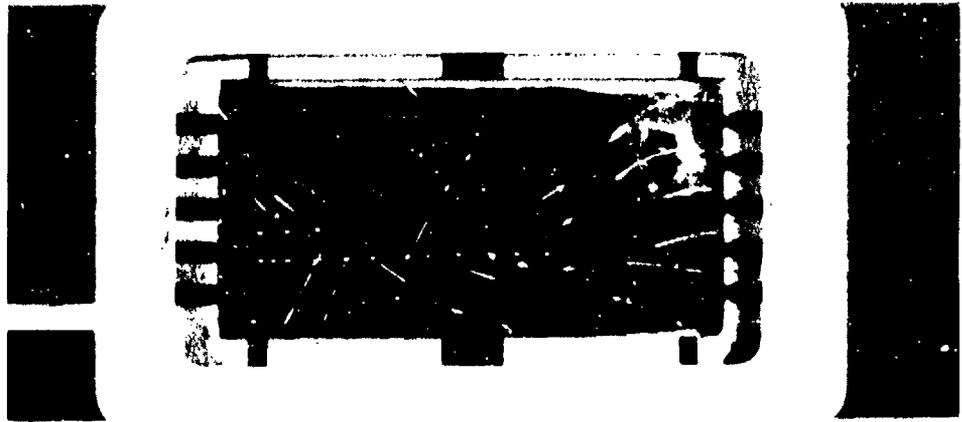
After considerable investigation, we determined that the most probable cause of the bonding problems was the two-part epoxy that was used to attach the die in the packages. Apparently, during the curing process, the organics that are driven out of the epoxy cause significant surface contamination to the platinum, thereby interfering with the bonding operation. In an attempt to prevent this problem, a new die-attach material, DITAC QL 3500 IC Adhesive, recently introduced by Du Pont Electronics, was obtained and tried for mounting the ferroelectric samples. This new product is a thermoplastic adhesive that requires no separate curing step. In addition, there is virtually no outgassing of solvents from the adhesive that could contaminate the surface of the sample.

For this application, a nonconducting version of the adhesive was obtained in the form of a sheet. In use, a small piece of adhesive the size of the die is cut from the sheet and placed in the center of the cavity of the package. The sample die is then placed on top of the adhesive, and the package placed on the chuck of the bonder, which is maintained at a temperature of 150 °C for the bonding operation. It was found that for this bonder, a low ultrasonic power setting yielded very acceptable results, with most of the bonds sticking well to the top platinum electrodes. As a result of the initial success with the new die-attach adhesive, this material is now used for all ferroelectric sample mounting. A mounted and bonded ferroelectric sample in a 16-pin DIP is shown in figure 5.

5. Conclusions

The procedures discussed here have been used to successfully prepare ferroelectric samples, both bonded and unbonded, for electrical and radiation hardness characterization studies. The rapid turn-around of samples prepared in this fashion has enabled a large number of different ferroelectric materials on silicon and nonsilicon substrates to

Figure 5. Mounted and bonded ferroelectric sample.



be evaluated in a minimum amount of time. During the course of the work described herein, a need developed for smaller top electrodes than were being prepared, so that higher frequency measurements could be employed for fatigue and other electrical studies. Efforts are currently under way to prepare silicon shadow masks to provide top platinum electrodes that are on the order of 50 μm or less on a side to address the requirement for a smaller top electrode.

Acknowledgements

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