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FAILURE MECHANISMS IN GaAs ICs: THE EFFECTS OF DEEP TRAPS

General Electric Company

Paul A. Martin

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13. ABSTRACT (Maximum 200 words)

GaAs FETs, 1 x 150 μm and 100 x 400 μm, were subjected to accelerated stress tests. The samples were of two types; with and without a buried p-layer. The life tests were of two types: a storage test at 250C; and a DC-biased life test at 225-235C. The FETs were characterized prior to and during the life tests using DLTS, I-V characteristics, C-V profiling, Drift Mobility profiling, and backgating. Buried p devices degraded more slowly initially. There is substantial loss of carriers and significant degradation of the drift mobility. There is substantial loss of carriers and significant degradation of the drift mobility. The concentration of EL2 was seen to increase near the device surface, and a new trap emerged near the end of the life tests with an energy in the 0.6 - 0.7 range. Recommendations for further work are included.

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FINAL REPORT EVALUATION

Failure Mechanisms in GaAs ICs: The Effects of Deep Traps

This effort was the result of a Program Research and Development Announcement in the area of Failure Mechanisms in GaAs ICs. Understanding the failure mechanisms in GaAs FETs, and ICs is a necessary first step in reducing the effects of those mechanisms and improving the reliability of systems which employ them. General Electric has investigated the deep traps in GaAs MESFETs during biased and unbiased life tests. The FETs were characterized by I-V, C-V, drift mobility profiling, and DLTS.

Through the comparison of the results from the FET characterization methods (1-V, C-V, drift mobility, and DLTS), this effort has provided some key insights into the evolution of deep trap concentrations, and has provided the first observation of the development of a trap during accelerated life tests.

It is hoped that this effort will spawn further work in this area, so that the understanding of the role of deep traps in FET reliability is advanced and their effects may be eliminated.

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1.0   Introduction

The reliability of the GaAs FET has improved over the years as degradation mechanisms have been identified and their respective solutions implemented. Table 1-1 lists the major GaAs FET degradation mechanisms, and some of the solutions developed to offset them. Channel degradation, the last mechanism listed in the table, does not have a solution listed.

Degeneration of the active channel region has been observed and apparently determines the ultimate useful life of the FETs. It appears to be associated with the accumulation of defects in the GaAs channel, either through local defect generation or by diffusion of defects from nearby interfaces. The same type of phenomenon is observed in GaAs laser diodes and accounts for their ultimate lifetime [1].

This degradation mechanism occurs slowly enough so that GaAs FETs can have useful lives in excess of 10^6 hours at channel temperatures as high as 150°C [2]. Lifetimes at higher temperatures are much shorter, however; for high power applications, the temperature of the device must be restricted to permit an acceptable lifetime. A better understanding of the mechanism involved might permit its elimination or minimization, and allow the reliable operation of GaAs FETs at higher temperatures.

High concentrations of point defects in the channel or channel-substrate interface have been associated with a number of harmful device performance effects, though not in a reliability context. Immorlica and co-workers found substantial backgating and premature saturation of output power in implanted FETs, which showed a high trap density in the substrate interface. Other devices without these problems showed trap densities an order of magnitude lower as measured by deep level transient spectroscopy (DLTS) [3]. Van Rees and co-workers found similar results in a VPE power FET which they traced to hole traps [4]. In both cases, drift mobility profiling showed a drop in mobility at the edge of the active region.

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A number of workers have demonstrated the advantages of a buried p-type implant under the implanted FET channel [5-9]. Such an implant will sharpen the electron distribution and introduce a substantial potential barrier which improves confinement in these structures. Co-implantation of a p-type dopant has been credited with reduction of substrate trapping effects by isolating the active channel from traps in the semi-insulating substrate. Buried p layers have also been proposed for the reduction of backgating in implanted structures.

Work in the GE Electronics Laboratory has confirmed the advantages of this technique. We have found that the p layer gives superior device performance and reduced backgating. Deep level concentrations were no higher than those found in the absence of the p layer, and no additional levels were introduced. Isolation of the active region from trapping effects provides a strong incentive for the study of p layers as a possible solution to trap related failure mechanisms. If, over time, the trap concentration in the substrate or at the substrate-active layer interface increases substantially, the use of such a buried p layer should substantially reduce the sensitivity of the device to these added traps.

We report a study which uses several materials characterization techniques to study the FET channel as the devices are aged. We use a high temperature thermal stability test and a DC life test to age the devices over a period of 1000 hours, while removing the devices periodically to investigate the evolution of material characteristics of the channel. In doing so, we conducted a systematic study of both the evolution of deep trapping centers during a life test of ion implanted GaAs FETs and the effect of these centers on the performance of the devices. We used Deep Level Transient Spectroscopy (DLTS) to measure the deep level concentrations as a function of time. We also used a number of materials characterization techniques, including CV profiling and drift mobility profiling, to study the effect of these levels on materials characteristics, and backgating measurements to determine their effect on the operation of the device in an integrated circuit.

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2.0 Device Descriptions and Life Test Procedures

2.1 Implantation and annealing

The implants for this project were designed using a finite difference solution to Poisson's equation to insure that the buried p layer would be fully depleted, and that the resulting sheet densities of the two wafers (p and no p) would be similar. Wafer I89-205-1 had a 1.2×10^{12} cm^{-2} Be implant at 110 kV and 7.48×10^{12} cm^{-2} Si implanted at 100 kV. Wafer I89-217-2 had a single implant of 6.7×10^{12} cm^{-2} Si at 100 kV. Both wafers were annealed at 890° C for 10 seconds in the Heatpulse 410 rapid thermal annealer with Ar forming gas as carrier gas. After the annealing, the wafers were inspected under high intensity lamp and microscope for surface morphology to insure that there was no surface decomposition. Electrochemical profiling was also performed to provide the carrier concentration profiles. As shown in Figures 2-1 and 2-2, the two wafers had profiles (peak concentration, position, etc.) very similar to each other except that the wafer with buried p layer showed a sharper tail as predicted.

2.2 Device fabrication

A four layer photolithographic mask set was used consisting of mesa, ohmic metal, gate metal, and dielectric via (passivation) masks. The depth of the mesa etch was approximately 0.94 µm. Specific contact resistivity for ohmic contacts averaged 3.903×10^{-6} ohm-cm^2 for Wafer I89-205-1, and 2.365×10^{-6} ohm-cm^2 for Wafer I89-217-2. Ohmic contact metallization consisted of (in order of deposition) Ni-100Å, Ge-300Å, Au-600Å, Ag-1000Å, and Au-1800Å. The gate recess etch was adjusted to yield I_{DSS} of about 0.67 times the original gateless current; for 100 x 400 µm devices the resultant current averaged 77 mA for Wafer I89-205-1 and 85 mA for Wafer I89-217-2. Gate metal was Ti-500Å, Pt-500Å and Au-6500Å. Silicon nitride passivation was deposited 1550Å thick except over the bonding pads.

The devices were separated and mounted onto separate carriers with high temperature conductive epoxy. Alumina test pads were also mounted on the

carriers and wedge-bonded to device terminals using 0.7 mil gold wires. Since each mask site was numbered, each device could be identified during the ensuing tests.

Two device designs were used for this project. The first, a conventional 1 x 150 μm FET, was used for DC I-V measurements and backgating measurements. The backgate was located at a right angle to the gate at a distance of 16 μm. The second device, a 100 x 400 μm FAT FET, was used for C-V, DLTS and drift mobility profiling. The use of the FAT FET was necessary to provide sufficient gate capacitance for the materials characterization measurements. The device layouts are shown in Figures 2-3 through 2-5.

2.3 Life Test Procedure

A total of over forty devices were subjected to life tests. Additional devices were tested throughout the project as controls, but not subjected to the life test. The devices (excluding control devices) were divided in half and subjected to two types of tests. The high temperature thermal stability test was simply storage at high temperature, while the high temperature DC test occurred at high temperature under operating conditions.

For the thermal stability test, devices were placed in a single oven. The four groups of devices from each design and wafer were kept in separate trays to avoid misidentification. Temperature was maintained at 250°C for the duration of the test. Dry nitrogen gas was used to purge the oven constantly at a flow rate of 14 SCFH. Devices were inserted and taken out of the oven at room temperature, and purging gas was present whenever the temperature was elevated.

DC test devices were mounted in separate fixtures and tested ten at a time. Each fixture had its own bias circuitry, purging gas connections, and temperature control. Dry nitrogen flow rate for a group of ten fixtures was 5 SCFH; it was maintained constantly while the temperature was elevated. The temperature of each fixture was adjusted using a model to account for

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channel temperature rise due to power dissipation [10]. Using this model, FATFET (100 x 400 μm) temperature was maintained at 235°C, and 1 x 150 μm device temperature was maintained at 225°C. Electrical bias was adjusted to the following voltages: Drain: +3v., Gate: 0v., Backgate: -2v., and Source: 0v. During the tests, voltage and current readings were taken by computer every hour, and temperature was adjusted once a day.

A summary of device classes and life tests is shown in Table 2-1. With a minimum of five devices in each class, a reasonable amount of statistical analysis is possible at reasonable cost. Characterization of devices was performed after 0, 24, 168, 500 and 1000 hours of life tests. I-V measurements were performed on all devices. Backgating measurements were performed on all 1 x 150 μm devices. C-V and drift mobility profiling were performed on all 100 x 400 μm devices. Due to the amount of time consumed, DLTS was performed on two 100 x 400 μm devices from each class. Initial DLTS scans were performed on four 100 x 400 μm devices from each class to insure that the two chosen for further study were indeed typical of the group. The actual devices used are listed in Tables 2-2 and 2-3. The device identification numbers are furnished on the mask set, and are for identification only.

3.0   Characterization Results

3.1   I-V Characteristics

Degradation of I_{DSS} is summarized in Table 3-1. I_{DSS} degradation is expressed as a percentage of the original value before the life test. We can make a number of observations on the basis of these data:

Comparing thermal stability devices to dc life test devices, we observe that among 1 x 150 μm devices the two types degraded at close to the same rate, although the thermal stability devices degraded a bit more quickly. Among the 100 x 400 μm devices, however, there is a dramatic difference. In this group, the thermal stability devices degraded much more quickly.

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Comparing devices with and without buried p layers, we observe a consistent trend. The buried p devices degrade more slowly at first, later overtaking the devices without buried p.

One would normally expect the DC life test devices to degrade at the same rate or faster than the thermal stability devices. Although many workers have observed the creation and motion of defects due to the presence of current in a device [11-14], we are unaware of any work establishing the retardation of device failure due to the presence of current. There is an extensive literature describing the annealing of defects in the presence of current, but in every case this involves recombination mechanisms, in which both electrons and holes are present in the device [14-16]. In the absence of minority carrier injection (i.e. when the p^+-n diode was not pulsed to forward bias) there was no enhancement of defect annealing. In the present device, holes are not present, and this is an important distinction. A recombination event occurring at the defect liberates an amount of energy comparable to the band gap, and can be repeated an arbitrary number of times. A trapping event involves only one band edge, releasing a correspondingly smaller quantum of energy, and only one (or possibly two) electron(s) can be trapped at a time. Thus the energy available for defect annealing or motion is correspondingly smaller in the absence of holes. In any case, EL2 (the major defect observed in this work) would be a poor candidate for annealing, since it has been established that EL2 is stable under electron-hole recombination [17].

Another possible cause is differences in life test procedure. In an effort to maintain identical channel temperatures, the DC life test was conducted at a lower temperature than the thermal stability test. The temperatures used (225°C for the 1 x 150 μm FETs and 235° C for the 100 x 400 μm FETs) were calculated from a model to account for the channel temperature rise due to power dissipation [10]. The parameters of this model (notably, thermal resistance) are subject to some uncertainty, raising the possibility that the calculated rise in channel temperature was not as great as predicted by the model.

There is also a difference in the details of the nitrogen purge configuration. (The nitrogen purge replaces the encapsulation of the device in the field, displacing oxygen and preventing oxidation of the device.) The thermal stability test is performed without device fixtures; the devices simply rest on a tray in the oven with nitrogen flowing throughout the chamber. The DC life test devices, on the other hand, are mounted in fixtures which supply the bias voltage to the devices, and nitrogen is introduced through a hose connected to the fixture and opening directly above the device. Because of the difference in configuration, we can expect the DC life test devices to experience a much higher localized flow of nitrogen even if flow rates into the oven are comparable. This is not an entirely credible mechanism, however, as it does not explain the difference between 1 x 150 µm and 100 x 400 µm devices. Since the current and current density in the 1 x 150 µm devices is much higher, one would expect current related degradation to occur much more quickly in the 1 x 150 µm devices.

An alternative explanation is provided by other workers. Würfl and Hartnagel studied the evolution of TiPtAu Schottky contacts on semi-insulating GaAs with XPS sputtering measurements of atomic species near the surface. They found diffusion of Ga into the Ti layer, and diffusion of Ti into the GaAs, accompanied by the degradation of the reverse voltage characteristic of the Schottky diode, resulting in early reverse breakdown of the junction [18]. They reasoned that Ti acted as a donor in the GaAs, transforming the Schottky into an ohmic contact. The effect was enhanced by imposition of voltage on the junction. In our case, there is no evidence that the Schottky is turning into an ohmic contact. It is likely, however, that the loss or compensation of carriers taking place in all our devices is to some extent counteracted in the dc life test by the addition of Ti donors from the Schottky. Unfortunately, this is speculative, since the role of Ti as a shallow donor has not been firmly established [19]. In addition, Ti diffusion does not explain the accelerated development of defects found in the thermal stability devices as compared to the DC life test devices, as described below. Contact effects would, however, explain the difference between 1 x 150 µm and 100 x 400 µm devices. This may be an effect based on the area of the device, since the long gate length device would tend to

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drive any interdiffusion in a one-dimensional pattern, while the short gate
length device would give rise to interdiffusion in a spreading pattern
dominated by edge effects, resulting in more diffuse defect concentrations.
A complete explanation of these data may require a number of mechanisms,
such as a combination of interdiffusion and a faulty temperature model.

From these data, the devices with buried p layers tend to degrade more
slowly during the initial phase of the DC life test, but overtake the other
devices in degradation after 500 to 1000 hours. The same trend is observed
in the thermal stability test, with the crossover point occurring earlier
(observed at the 168 hour test). Since the early portion of the life test
simulates the useful lifetime of the device, this indicates the possible use
of a buried p layer in extending the useful life of ion implanted FETs.
More work needs to be done, however, as the two device types are within a
standard deviation of each other.

3.2 C-V Profiling and Drift Mobility Profiling

A digital variable frequency LCR meter was used to perform C-V profiling.
This measurement is included to measure any compensation of the shallow
donors by the emerging deep levels. Campbell and co-workers observed such
compensation in studies of heat treated GaAs [20]. Reduction of carrier
concentration, accompanied by a reduction in I_{DSS}, is also widely observed
in the degradation of GaAs MESFETs. We see such a reduction in carrier
concentration in the present study as well, as shown in Figures 3-1 through
3-4. The C-V profiles differ from the electrochemical profiles in Figures
2-1 and 2-2 because the C-V profiles are done on the fabricated device,
which has a recessed gate.

As an additional check for signs of channel degradation, we measured the
drift mobility profile. A drop in the mobility near the active
channel/substrate interface has been linked with the existence of interface
traps and results in degraded rf performance of power devices [3,4].
Representative profiles are shown along with the C-V results in Figures 3-1
through 3-4. The initial (0 Hour) profiles show a difference between the

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buried p device and the device without buried p. The devices without buried p show a mobility which rises as the electron concentration falls, peaking between 1500 and 2000 Å. Devices with buried p layers show the same trend, except that the mobility in the buried p region is depressed by the compensation of the buried p layer, moving the mobility peak closer to the surface of the device.

For both device types, the drift mobility tends to drop over most of the device as the life test proceeds, particularly after the 500 and 1000 hour tests. For the devices with buried p layers, the entire mobility profile drops with elapsed time. In the case of Figure 3-2 there is a slight rise in mobility from 0 to 24 hours, but this is within experimental error. For the devices without buried p layers, the behavior is more complex; the mobility rises near the surface while it falls further into the bulk. This behavior continues until the 1000 hour test (DC test) or the 500 hour test (thermal stability), when the mobility falls again in this region. This indicates that the behavior of the material near the surface is different from the evolution of the material in the bulk.

It is clear from these data that the drop in I_{DSS} is due not only to the loss of carriers but also to the loss of mobility of those carriers remaining. This is a sign of some compensation mechanism, such as a defect or impurity. These results would tend to support a compensation model in which the compensating impurities entered first from the substrate, rather than from the Schottky. Devices with buried p layers show relatively stable mobility profiles in the early phases of the test, losing mobility only after 168 hours (thermal stability test) to 500 hours (dc test). In this case, the buried p layers tend to stabilize tne device against the initial phase of degradation. In the case of the devices without buried p layers, the mobility nearer the surface of the device falls at about the same time as the observation of the new trap in DLTS at significant concentrations. This may be a sign that the new trap is important in reducing mobility in the latter stages of the life test.

The initial rise in drift mobility towards the surface of the devices without buried p layers is not understood. By combining the measurements of carrier concentration and mobility and comparing to theoretical calculations of mobility as a function of concentration and compensation, it is possible to estimate a compensation ratio from these data. The technique is less accurate at room temperature than at 77K, and should be treated with suspicion for non-homogeneous samples [21]. Nevertheless, it is clear from this technique that the initial mobility near the surface of the devices without p layers reflects some initial compensation. We estimate that the compensation ratio $(N_D^i - N_A^i)/n$ (total ionized donors and acceptors divided by carrier concentration) near the surface of device I0306 (Fig. 3-1) is about 5 initially, decreasing to a minimum value of 2 after 168 hours, remains at 2 after 500 hours and increases again to 3.5 after 1000 hours. The source of the initial compensation is unknown, but may be process related.

3.3 DLTS

Deep Level Transient Spectroscopy (DLTS) [22] was used to measure deep level concentrations as the life test proceeded. This technique produces a complete characterization of the defect's electrical interaction with the energy bands of the host crystal, including trap concentration, energy level within the band gap and capture cross section. The technique will typically detect defect concentrations as low as $10^{-4}N_D$ for levels deeper than about 0.1 eV from the band edge. DLTS was performed on 100 x 400 μm FETs to provide adequate capacitance for the measurement. Current transient DLTS was attempted on the 1 x 150 μm FETs [23], but was not successful due to the predominance of surface-related "hole trap" signals masking the signals from the true deep levels [24].

Calculating the concentration of deep levels from DLTS data is made difficult in this case because of the extremely non-uniform distribution of the background dopant. Concentration calculations also are complicated by partial filling of the defect at the edge of the space charge region [25], an effect not included in the earlier literature. Neglect of this effect

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results in conclusions about trap concentrations which cannot be trusted
[26]. Following the analysis of Steivenard and Vuillaume [27], we use the
measured carrier concentration to calculate numerically the conduction band
profile at bias points used for the profiling measurement, accounting for
edge effects in the presence of nonuniform background dopant concentrations.
Simple Debye length-type calculations are inadequate in such cases, as they
assume a uniform dopant concentration.

Typical DLTS spectra of unaged devices with and without buried p layers are
shown in Figures 3-5 and 3-6. A number of spectra are superimposed on each
plot, representing different rate windows used by the system. The samples
without buried p implants show a spectrum dominated by EL2 (Figure 3-5).
This is to be expected for devices implanted into LEC GaAs. EL2 is the main
electron trap found in GaAs grown by most growth techniques, with MBE as the
only exception [28]. In LEC GaAs, EL2 compensates the residual carbon
acceptors and is responsible for the semi-insulating behavior of this
material. Because of the importance of a semi-insulating substrate for high
speed performance of GaAs devices, this is one instance where a deep trap is
technologically beneficial. EL2 is believed to be related to the As_{Ga}
antisite defect (As on a Ga site), and may be either the isolated As_{Ga} or a
more complex defect with As_{Ga} at its core. Gatos and Lagowski [29] have
performed the most detailed measurements of energy level and capture cross
section, reporting 0.814 eV and $2.6x10^{-13}$ cm^2, respectively. There is,
however, an entire family of defects related to EL2 with energy levels
ranging as low as 0.76 eV. We measured an energy level of 0.734 eV and a
capture cross section of $1.95x10^{-14}$ cm^2, which is reasonably close to the
published values. The energy levels were monitored throughout the life
test, and did not vary substantially. Neither the published activation
energies we quote here nor the energy levels we measured were corrected for
the temperature dependance of the capture cross section.

The samples with buried p implants show an EL2 signal plus one large peak
which appears from its sign to be a hole trap. (See, for example, Figure
3-6. The dotted line designates a negative DLTS signal, corresponding to a
negative-going capacitance transient, commonly associated with the emission

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of holes from a trap in the depletion region.) Observation of a hole trap in these structures is not expected, since holes are not present. In fact, this signal cannot be assigned to a discrete defect, since it does not form a well-defined DLTS peak, and it is not possible to extract an activation energy. We demonstrate that this signal is a parasitic effect related to the ohmic contact. Shiau and co-workers at Stanford University have observed minority carrier DLTS peaks caused by AC capacitance in the ohmic contact [30]. Such capacitance can be defect related, as the ohmic contact conducts by defect aided tunneling through a thin Schottky barrier in highly doped material. This effect is minimized by maximizing the ratio of ohmic contact area to Schottky contact area. This is demonstrated on the present device; the ohmic contact can be made to both source and drain, or to only one of these contacts. If the ohmic contact area is decreased in this way by a factor of two, the hole trap signals are increased by a factor of 7. All DLTS measurements for this program were made with both source and drain ohmic contacts to minimize the parasitic "hole trap" signal. Even in this configuration, the devices with buried p layers show an EL2 signal which is less than that of the devices without buried p by a factor of 10. We believe this to be a parasitic effect caused by interference from the "hole trap" signal of opposite sign. No quantitative measurements were possible on the buried p devices until the parasitic signal disappeared later in the test. This occurred after 500 hours in the case of the thermal stability devices, and after 1000 hours in the case of the DC life test devices. We attribute the disappearance of these "hole trap" signals to an evolution in the characteristics of the ohmic contact over the course of the life test. We cannot be more specific about this without more detailed studies. It would be interesting, for example, to include in the life test a TLM-type structure to evaluate the impedance (not just the specific resistance) of the ohmic contacts as the structure is aged. Examples of DLTS spectra after 1000 hours are shown in Figures 3-7 through 3-10.

As the life tests proceeded, we observed redistribution of the primary electron trap, EL2, as shown in Figures 3-11 through 3-18. The initial EL2 profile (before aging of the device, labeled as 0 hours in the figures) shows some depletion of EL2 concentration towards the surface, caused by

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outdiffusion during the implant anneal. This is as expected, as the outdiffusion of EL2 under heat treatment has been widely documented and attributed to loss of As from the surface [31]. As the devices are aged, EL2 concentration near the surface tends to increase with time. For the devices with buried p layer, we include only the later measurements, after the disappearance of the "hole trap" signals. The 500 and 1000 hour profiles show the EL2 concentration increasing toward the surface, in agreement with the later results for devices without buried p layers. One possible explanation for this change in EL2 concentration is the outdiffusion of gallium atoms, encouraging gallium vacancies and thus EL2. In the absence of the gate, such effects have been observed to be passivation dependant [32]. Under a TiPtAu gate, gallium outdiffusion has been observed as a result of interactions with the metallization [18].

It may appear surprising that EL2 would diffuse out of the sample at high temperatures (900° C during the implant anneal) and back into the sample at moderate temperatures (250° C during the life test). The reason for this is the existence of two constituent atoms (As and Ga) in the GaAs lattice and the sensitivity of EL2 concentration to the stoichiometry of the GaAs crystal. Preferential outdiffusion of Ga occurs at moderate temperatures such as those of a life test, and results in an As rich stoichiometry, favoring the formation of EL2. Preferential As outdiffusion requires substantially higher temperatures, and drives the stoichiometry in the opposite direction, annihilating EL2 in the resulting Ga-rich region. The difference lies not with the diffusion rates of Ga or of As (both of which can be expected to increase with temperature) but in the difference between the two diffusion rates, and therefore in the stoichiometry of the GaAs left behind.

A new trap was also observed in these devices during the latter stages of the life tests. Measured energy levels, capture cross sections (σ) and concentrations are summarized in Tables 3-2 through 3-5. There is a great variation in the measured energy levels, due to the fact that this trap occurs in the DLTS spectrum as a shoulder on the larger EL2 signal. This makes resolution of the smaller peak very difficult. In an effort to

resolve this peak, we attempted to fit the DLTS spectrum numerically to two peaks and extract peak positions from ' ? fit. The effort proved very time consuming and unsuccessful. The only ftware available for this purpose resided on a different computer, and in olved fits to photoluminescence-type line shapes. To do the job properly would involve extensive software development, a project which was beyond the scope of this work. Fortunately, the DLTS spectra are digitized and stored on disc, so that this task may be attempted at a later time.

We believe the most likely energy level to be in the 0.6-0.7 eV range. The data are listed from the earliest measurable observation of the new trap. It is observed first in the thermal stability devices without p layer after 168 hours. In the thermal stability devices with buried p layers, it is visible after 500 hours, when the parasitic "hole trap" signals suddenly disappear. (In this case, the trap could have been introduced earlier, obscured by the parasitic signals.) In the DC Life test devices, the new trap is observed as a shoulder on the EL2 peak after 500 hours for the devices without buried p layers, but the peak could not be resolved. The new trap is measurable in devices with and without buried p layers after 1000 hours. The uncertainty in capture cross section is considerable for all DLTS measurements made in this program. This is a problem inherent in the use of Arrhenius plots to measure the capture cross section. Unless more accurate (and more time-consuming) methods are used, one can only estimate the order of magnitude of capture cross sections from the Arrhenius plot.

Identification of the new trap is not possible at this time. The closest candidate in the established literature is the defect E4 created by 1 MeV electron irradiation of GaAs with an energy level of 0.71 eV and a capture cross section of 8.3×10^{-13} cm^2 [33]. The nature of this defect is unknown, although there is some evidence that it is associated with a $As_{Ga} - V_{As}$ complex [34]. Outdiffusion of Ga would make available the Ga sites needed for formation of this complex. A more recent candidate is a level identified by localized vibrational modes (LVM) in infared absorption experiments as one charge state of the $O-V_{As}$ complex in GaAs, between 0.57

eV and 0.75 eV below the conduction band edge [35]. The latter defect was not identified by electrical means, and the two ionization energies (electrical and optical) may not be identical, so the $0-V_{As}$ possibility is more speculative. (By "one charge state", we refer to the fact that defects, like atoms, can bind a number of electrons, each with its own energy level. In the semiconductor defect literature, these states are referred to by reference to the charge of the defect center when the electron state is full or unoccupied. In the case of the $0-V_{As}$ complex, it is thought that there are two levels in the GaAs band gap. Skowronski et al. attribute the 0.57-0.75 eV level to the -/0 charge state of $0-V_{As}$, namely that state which is negatively charged when occupied and neutral when empty.)

Since we postulate the presence of Ga outdiffusion as an explanation for the change in EL2 concentration, one would expect to see a defect corresponding to the isolated Ga vacancy in the DLTS results. Unfortunately, despite Lang's early work [36], there is no consensus on the identification of any DLTS signals as representing the Ga vacancy [37,38]. Thus we cannot speculate on the presence or absence of the isolated Ga vacancy on the basis of DLTS results alone. We should note, however, that the Ga vacancy is thought by many to be an acceptor [39,40], raising the possibility that this is one source of compensation in the channel.

The concentration of the new trap, and the change in concentration of EL2 are not sufficient by themselves to account for the change in electron concentration as measured by C-V profiling. In fact, numerical calculations indicate that acceptor levels are needed to reduce electron concentration, where EL2 is widely known to be a deep donor.

3.4 Backgating

A large number of workers have shown that backgating is caused by deep trapping effects at the channel-substrate interface. The backgating measurement is therefore included to measure the effect of deep levels on integrated circuit performance. To measure the backgating effect, the drain

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and substrate currents were measured simultaneously as a function of the backgate voltage. Typical backgating spectra, showing the evolution of backgating with time, are shown in Figure 3-19 through 3-22. We plot I_{DS} as a function of backgate voltage normalized to I_{DSS}. The deterioration of I_{DSS} with device age is thus removed from the data, allowing us to focus on the backgating effect itself.

A number of trends are noticeable. First, the backgating effect becomes more pronounced as the devices are aged. Second, even before aging, the buried p devices show more backgating than the devices without buried p. This is in contrast to published work, and to our previous findings, which indicate a diminished backgating effect in the presence of a buried p layer [41]. The contradiction may be due to variations in the surface conditions of the device, which are known to have a considerable effect on backgating [42]. Third, the buried p devices show a more pronounced backgating effect than those without buried p.

4.0   Discussion

There are a number of possible explanations for the loss of carriers and of carrier mobility:

First, we could be losing Si atoms by diffusion into the Schottky barrier metallization, or diffusion deeper into the substrate. We have no direct evidence of this, and we believe it unlikely at the temperatures used in this study. Nevertheless, the possibility cannot be ruled out.

Second, the donors could be compensated by defects or impurities which cannot be seen by DLTS. These could include either shallow acceptors, which would not be visible to DLTS under any circumstances, or deeper levels, which might not be visible due to the interaction of the finite Schottky barrier height and the detailed behavior of the quasi Fermi level under pulsed bias [43]. One possibility for this is Au diffusing from the Schottky barrier. Even though the Pt barrier should prevent this, other workers have observed diffusion of Au through the Pt barrier[18], as well as

through other barrier layers [44]. Au forms a deep acceptor level in GaAs, as well as a shallow acceptor level [13]. The shallow level would not be visible to DLTS; the deep level (at E_v + 0.4 eV) could be too deep, with respect to the conduction band, to be seen [43]. Since the shallow level is believed to be formed in complex with Ga vacancies [19], and we have indirect evidence of outdiffusion of Ga through the changes in EL2 profiles, formation of the shallow Au acceptor is a reasonable explanation for these results.

Third, the evolution of EL2 profiles near the surface points to the outdiffusion of Ga into the gate. Isolated Ga vacancies are thought to be acceptors in GaAs [39,40]. If the outdiffusion of Ga is reflected in isolated Ga vacancies as well as in the formation of EL2, this may account for some of the compensation without the need for Au diffusion.

Fourth, the evolution of drift mobility profiles indicates that compensation enters first from the substrate. Devices with buried p layers are more stable against this initial phase of degradation than are devices without buried p layers. The source of compensation from the substrate is unknown. During the latter stages of the life test, there may be a second degradation mechanism which affects the surface of the device more strongly.

5.0   Conclusions

The buried p devices seem to degrade more slowly during the initial phase of the test. The difference is small, and more work is required to substantiate this effect.

We see a substantial loss of carriers over time, as measured by C-V profiling, as well as significant loss of drift mobility, as measured by drift mobility profiling. Both of these effects are involved in the loss of current through the devices.

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We see an increase in EL2 concentration near the surface of the device. After analysis of the literature, we believe this is due to diffusion of Ga atoms into the gate, encouraging the formation of EL2.

Toward the end of the life test, a new trap emerges with an activation energy of 0.6 - 0.7 eV. This trap has not been identified, although we have listed a number of candidates.

The concentration of the new trap and the increase in concentration of EL2 are not sufficient to account for the decrease in carriers observed. The occurrence of the new trap is, however, coincident with an increased degradation of drift mobility, for which it may be responsible.

6.0   Suggestions for further work

To eliminate inadequate nitrogen purging as a possible source of enhanced degradation in the thermal stability study, it would be useful to repeat this study in the DC test fixtures.

While we have indirect evidence of Ga outdiffusion through the DLTS results, our discussion of Ti and Au diffusion is purely speculative, based on plausibility and the results of other workers. It would be best investigated by profiling these devices with Auger electron spectroscopy and SIMS and determine the extent (if any) of interdiffusion between the gate metallization and the GaAs channel. Auger would either prove or disprove Ga outdiffusion and any other interaction with the gate metallization. Presence of Ga outdiffusion does not constitute proof of isolated Ga vacancies, however, since the microstructure would remain uncertain. Ga vacancies could complex with impurities, combine with excess As to form As_{Ga} antisites, etc. (In fact, it is just this sort of complex behavior which causes the increase in EL2 concentration observed in this work.) Definitive identification of isolated Ga vacancies or any other specific microstructure which might be associated with Ga outdiffusion will have to await further work. The SIMS measurements would also investigate the possibility of Si

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diffusion, and allow us to search for any impurities responsible for compensation.

The new trap observed in this work is evidence of channel degradation. It does not appear, however, that the new trap forms quickly enough or in sufficient concentrations to be completely responsible for the observed degradation in device performance. It is possible, however, that it contributes to the loss of mobility in the latter stages of the life test. If the source of this defect could be identified, it could shed additional light on the underlying physical processes occurring during the life test, particularly if Ga or As vacancies are involved. It would also be interesting to investigate the formation of this defect at other temperatures, since the formation of Ga and As vacancies is highly temperature dependant.

The first step in identification of the new trap is clearly to establish the energy level and (if possible) the capture cross section with much greater accuracy. This could be done by any number of ways, including the fitting of the DLTS spectrum with true DLTS line shapes, performing multiexponential fits to the isothermal capacitance transient [45], or any number of procedures which have been proposed for this sort of problem [46]. An accurate measurement of capture cross sections would involve analysis of DLTS peak height dependance on DLTS pulse duration, so that the capture process could be studied directly. This analysis would be complicated in the present case, since capture rates are proportional not only to the capture cross section, but also to the local concentration of electrons available for capture. In an ion implanted structure, the rapidly varying electron concentration would have to be taken into account. The purpose of measuring energy levels and capture cross sections is to make comparisons to the literature, where detailed capture cross section measurements are relatively rare. Thus the measurement of the capture cross section may not be critical, at least in the initial stage of this work.

Further identification of the new trap would be guided by the initial results. If stoichiometric related defects are believed to be involved

(these would include Ga vacancies, As vacancies, Ga or As interstitials, antisites and related complexes) annealing experiments under conditions designed to encourage either Ga or As preferential outdiffusion would be particularly revealing. Such experiments, as well as careful attention to Ga:As ratios during the growth process, provided some of the first keys to the identification of EL2 [28]. To test an identification with the electron irradiation defect E4, the sample could simply be irradiated with electrons to produce E4 and provide a direct, in situ comparison. If impurities are suspected, a number of techniques are available, including implantation of the suspect atoms, and careful SIMS measurements. All these experiments, while revealing, would not identify the detailed microstructure of the defect. They would, however, provide enough useful information to interpret the physical processes involved in the aging of these devices.

For purposes of engineering devices like those fabricated for this study, the impact on the ultimate microwave performance throughout the device life is of great interest and is often investigated by lumped element circuit models. Coefficients which represent each element of the model may be adjusted 1) to optimize a given characteristic before fabrication, or 2) to adjust the model to fit a physical device. At the present time, a few such models are agreed upon to represent a GaAs MESFET in microwave applications [47]. It is possible to extract model coefficients using microwave scattering parameter measurements to identify trends in these coefficients over the useful life of a device. It would be very useful to circuit engineers, because they could then optimize a circuit design to accommodate possible variations through different stages of the device lifetime.

7.0   References

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Table 1-1 GaAs FET Failure Mechanisms and Solutions

Failure Mechanisms	Solutions
1. Al/Au Intermetallic Formation	All gold system, effective barrier.
2. Electromigration	Gold metal, control current density, nitride passivation.
3. Contact Degradation	Barrier layer to prevent Ga outdiffusion.
4. Metal Surface Migration	Passivation with nitride.
5. Oxidation of GaAs	Passivation with nitride.
6. Gate burn-out	Refractory gate, proper handling.
7. Drain burn-out	N^+ ledge near drain, passivation with nitride
8. Interdiffusion of Gate Metal & GaAs	TiPt, TiW, Al gates.
9. Degradation of Active Region	–

Table 2-1. Summary of Devices and Life Tests Performed

Device Type	Thermal Stability		DC Life Test	
	No P	P	No P	P
FAT FET	5	5	5	5
1 μm FET	5	5	5	5

Table 2-2
List of Devices Studied
1 x 150 μm FETS

1 x 150 High Temp Stability			1 x 150 DC Test	
		Wafer I89-205-1 (Buried P-Layer)		
C0307*	G0507		E0507*	I0407
F0406	A0508		D0407	B0408
F0408	D0509		F0407	I0408
		Wafer I89-217-2 (No Buried P-Layer)		
I0406*	I0506		F0306*	H0408
C0508	B0507		F0307*	I0408
E0407	I0507		I0307	A0508
H0407	B0608		B0308	

* control device (not aged)

Table 2-3
List of Devices Studied
100 x 400 μm FATFETS

100 x 400 High Temp Stability			100 x 400 DC Test	
		Wafer I89-205-1 (Buried P-Layer)		
H0406*	G0408		C0307*	F0308
D0407	G0506		E0307	A0408
D0408	G0509		I0307	B0408
		Wafer I89-217-2 (No Buried P-Layer)		
D0306*	G0307		B0308*	H0407
G0306	A0308		G0407*	A0408
A0307	I0308		A0508*	B0408
			I0306	G0506

* control device (not aged)

Table 3-1 I_{Dss} Degradation During Life Tests

Device Type	Mean I_{Dss} Degradation (%) After			
	24 h	168 h	500 h	1000 h
Thermal Stability Test Devices				
150 μm P	-6.31	-28.90	-54.48	-58.32
150 μm no P	-7.02	-28.87	-46.83	-46.27
400 μm P	-6.68	-69.02	-94.10	-96.61
400 μm no P	-23.72	-93.25	-94.98	-95.45
DC Life Test Devices				
150 μm P	-4.41	-16.40	-52.73	-66.75
150 μm no P	-5.44	-25.70	-37.97	-42.29
400 μm P	-1.44	-6.03	-50.51	-77.87
400 μm no P	-1.55	-17.37	-80.55	-92.59

Table 3-2
New Trap DLTS Results
Energy Levels (E_i) Capture Cross Sections (σ) and Concentrations (N_T)
I89-217-2 (No P) DC Life Test

Device No.	500 Hours	1000 Hours
B0408	Observed, not measurable	$E_i = 0.474 \pm 0.067$ eV $\sigma = 1.3 \times 10^{-16} \pm 2.9 \times 10^{-16}$ cm^2 $N_T = 1.5 \times 10^{14}$ cm^{-3}
G0506	Observed, not measurable	$E_i = 0.393 \pm 0.104$ eV $\sigma = 8.1 \times 10^{-18} \pm 2.7 \times 10^{-17}$ cm^2 $N_T = 1.3 \times 10^{14}$ cm^{-3}

Table 3-3
New Trap DLTS Results
Energy Levels (E_i) Capture Cross Sections (σ) and Concentrations (N_T)
I89-205-1 (P Layer) DC Life Test

Device No.	1000 Hours
B0408	$E_i = 0.697 \pm 0.052$ eV $\sigma = 2.6 \times 10^{-13} \pm 4.7 \times 10^{-13}$ cm^2 $N_T = 1.0 \times 10^{16}$ cm^{-3}
A0408	$E_i = 0.669 \pm 0.102$ eV $\sigma = 9.2 \times 10^{-14} \pm 3.2 \times 10^{-13}$ cm^2 $N_T = 1.0 \times 10^{16}$ cm^{-3}

Table 3-4
New Trap DLTS Results
Energy Levels (E_i) Capture Cross Sections (σ) and Concentrations (N_T)
I89-217-2 (No P) Thermal Stability Test

Device No.	168 Hours	500 Hours	1000 Hours
IO308	$E_i = 0.601 \pm 0.021$ eV $\sigma = 1.4 \times 10^{-14} \pm 2.3 \times 10^{-15}$ cm^2 $N_T = 5 \times 10^{14} - 1 \times 10^{15}$ cm^{-3}	$E_i = 0.733 \pm 0.079$ eV $\sigma = 3.2 \times 10^{-12} \pm 8.8 \times 10^{-12}$ cm^2 $N_T = 5 \times 10^{16}$ cm^{-3} at surface 5×10^{15} in bulk	$E_i = 0.669 \pm 0.048$ eV $\sigma = 4.7 \times 10^{-14} \pm 6.8 \times 10^{-14}$ cm^2 $N_T = 4.67 \times 10^{16}$ cm^{-3} at surface 3.7×10^{16} cm^{-3} in bulk
AO308	$E_i = 0.629 \pm 0.035$ eV $\sigma = 1.4 \times 10^{-14} \pm 1.7 \times 10^{-14}$ cm^2 $N_T = 1 \times 10^{15}$ cm^{-3}	$E_i = 0.697 \pm 0.054$ eV $\sigma = 1.0 \times 10^{-12} \pm 1.9 \times 10^{-12}$ cm^2 $N_T = 4 \times 10^{16}$ cm^{-3} at surface 1×10^{16} cm^{-3} in bulk	$E_i = 0.613 \pm 0.1$ eV $\sigma = 2.6 \times 10^{-14} \pm 8.8 \times 10^{-14}$ cm^2 $N_T = 1.5 \times 10^{16}$ cm^{-3} at surface 8.6×10^{15} cm^{-3} in bulk

Table 3-5
New Trap DLTS Results
Energy Levels (E_i) Capture Cross Sections (σ) and Concentrations (N_T)
I89-205-1 (P Layer) Thermal Stability Test

Device No.	500 Hours	1000 Hours
G0509	$E_i = 0.658 \pm 0.012$ eV $\sigma = 8.6 \times 10^{-14} \pm 3.4 \times 10^{-14}$ cm^2 $N_T = 1.3 - 1.8 \times 10^{15}$ cm^{-3}	$E_i = 0.535 \pm 0.029$ eV $\sigma = 8.4 \times 10^{-16} \pm 7.9 \times 10^{-16}$ cm^2 $N_T = 2.4 \times 10^{15}$ cm^{-3} at surface 4.7×10^{14} cm^{-3} in bulk
D0408	$E_i = 0.666 \pm 0.033$ eV $\sigma = 3.2 \times 10^{-14} \pm 3.5 \times 10^{-14}$ cm^2 $N_T = 1.0 \times 10^{16}$ cm^{-3}	$E_i = 0.705 \pm 0.047$ eV $\sigma = 1.7 \times 10^{-13} \pm 2.7 \times 10^{-13}$ cm^2 $N_T = 3.2 \times 10^{17}$ cm^{-3} at surface 8.3×10^{15} cm^{-3} in bulk

Fig. 2-1. Electrochemical Profile of 189-217-2 (No Buried P Player)
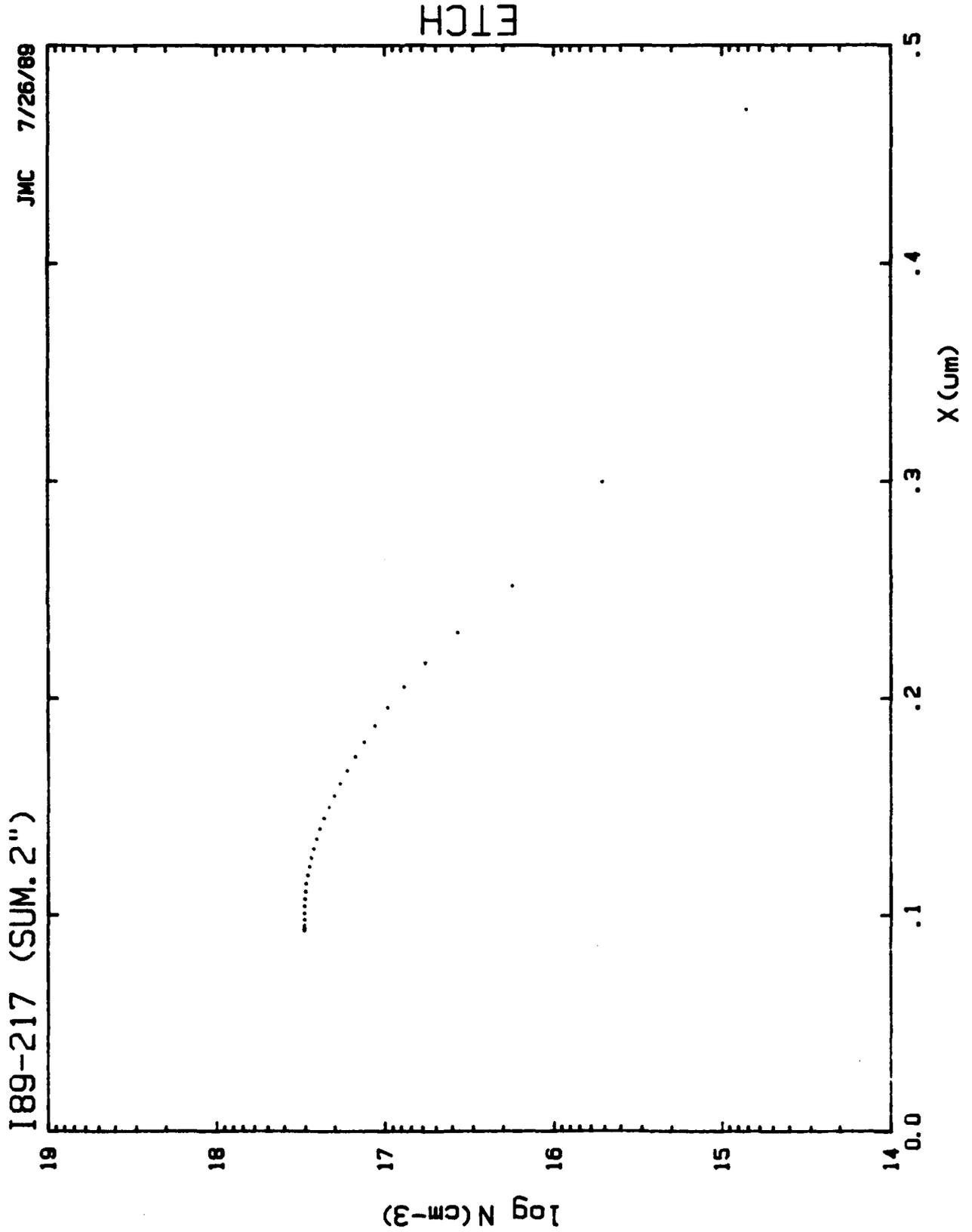
Fig. 2-2. Electrochemical Profile of 189-205-1 (Buried P Layer)
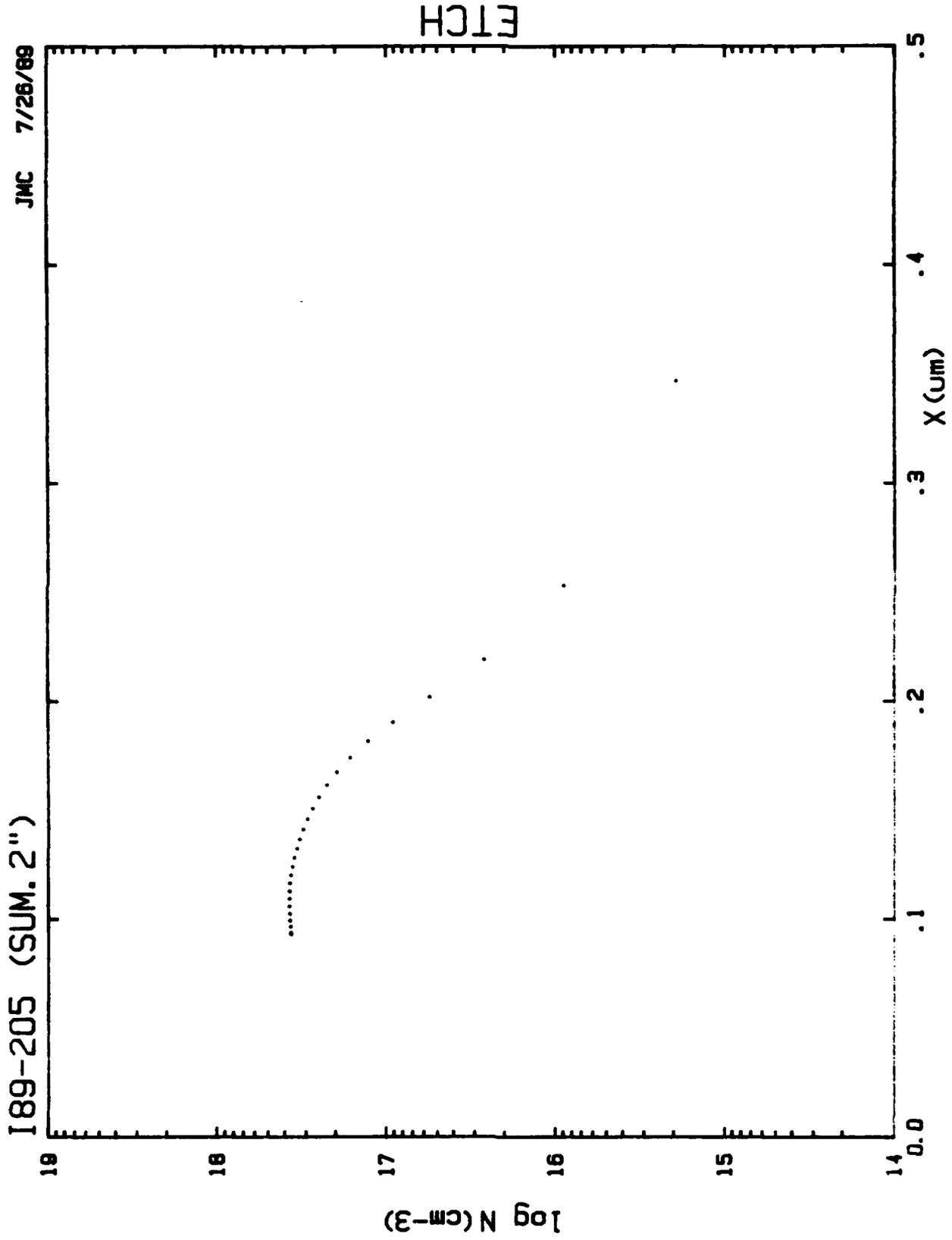
Fig. 2-3.　1 x 150um FET Layout

Sidegate

Source

Gate

Drain
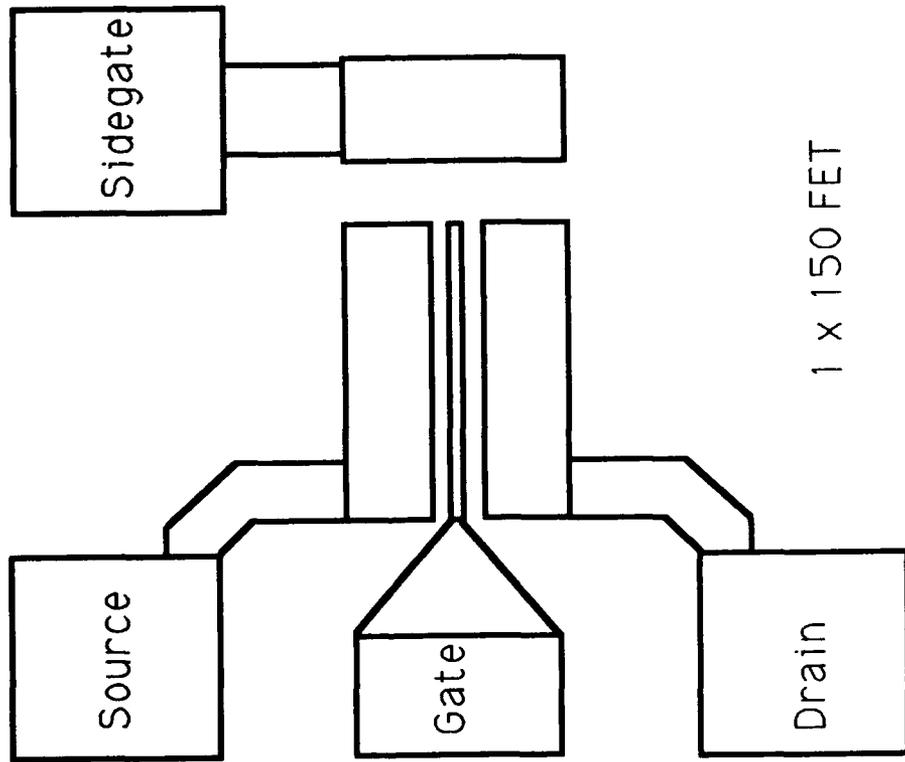
1 x 150 FET

Gate Dimensions: 1 x 150μm
Sidegate Distance: 16μm

34

Fig. 2-4. 100 x 400um FET Layout

Source

Gate

Drain
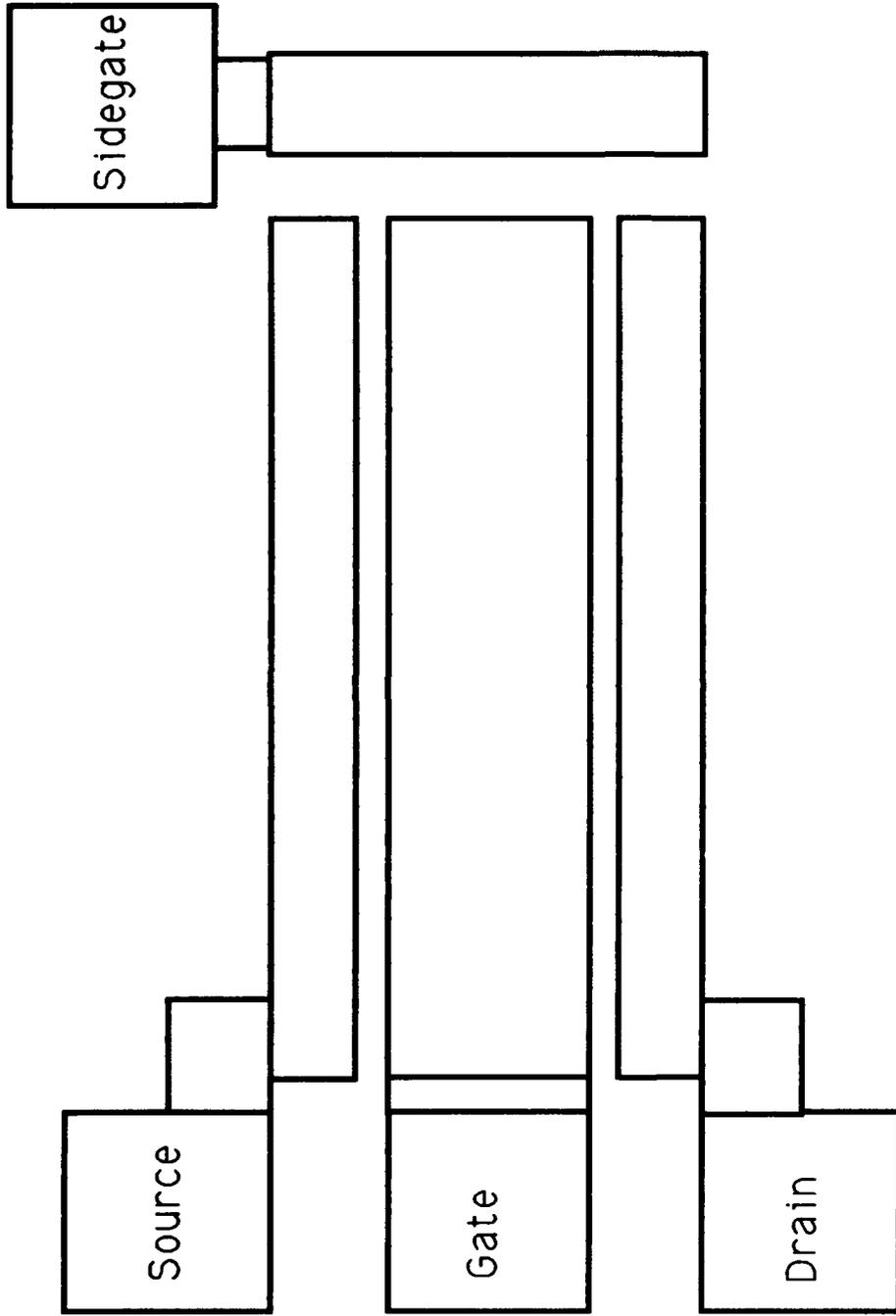
Sidegate

100 x 400 FATFET

Gate Dimensions: 100 x 400μm
Sidegate Distance: 16μm

Fig. 2-5.   1 x 150 μm FET Marked with Bias Used During DC Life Test

drain
bias=+3V

gate
bias=0V

source
bias=0V

mesa

buried p-layer (if used)

sidegate
mesa

sidegate
bias=2V

Substrate
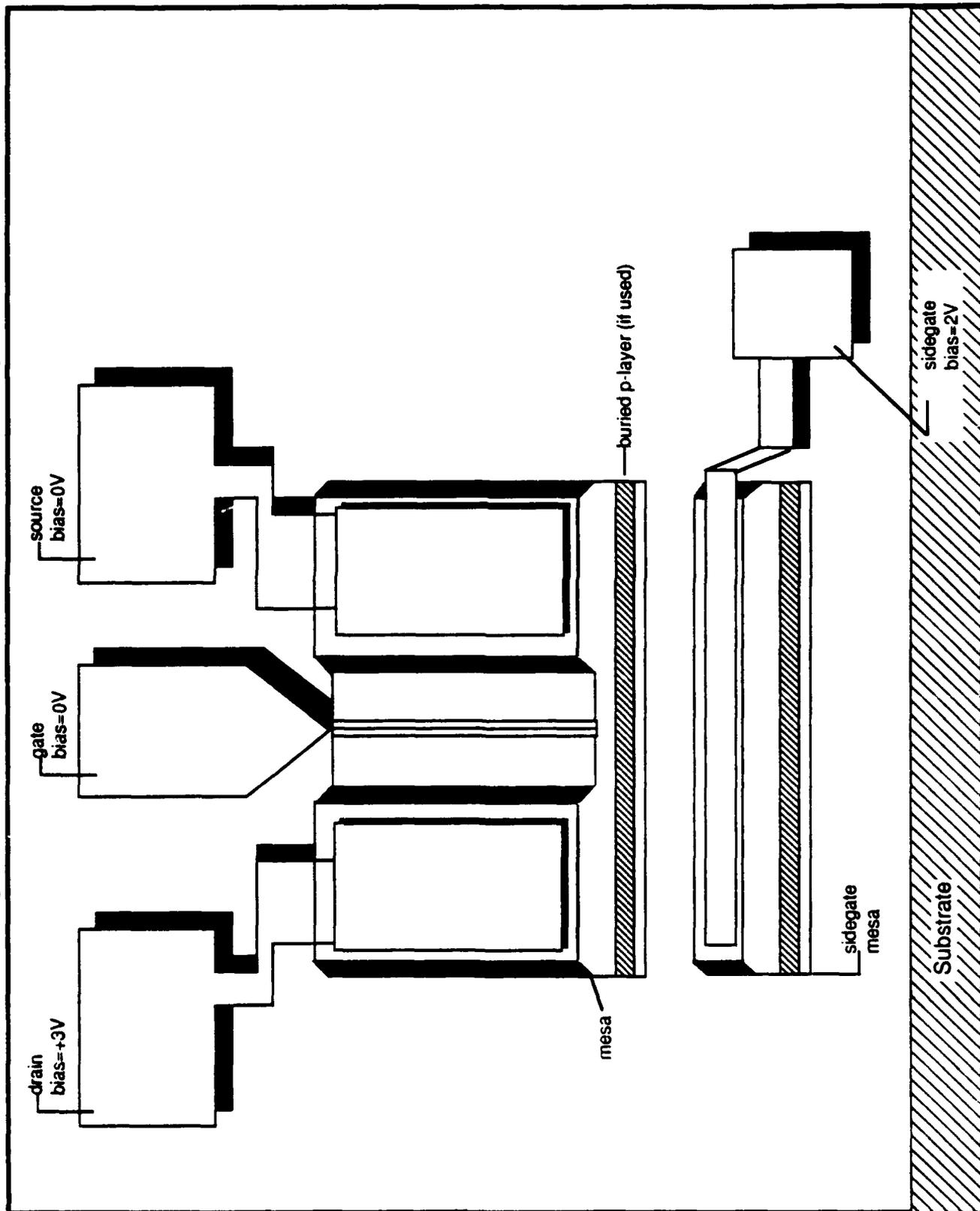
Fig. 3-1. C-V, Drift Mobility Profiles: DC Test, No P 10306

GE Electronics Laboratory: Deep Trap Study
Wafer No. I89-217-2   Device No. I0306
Test: DC Test.
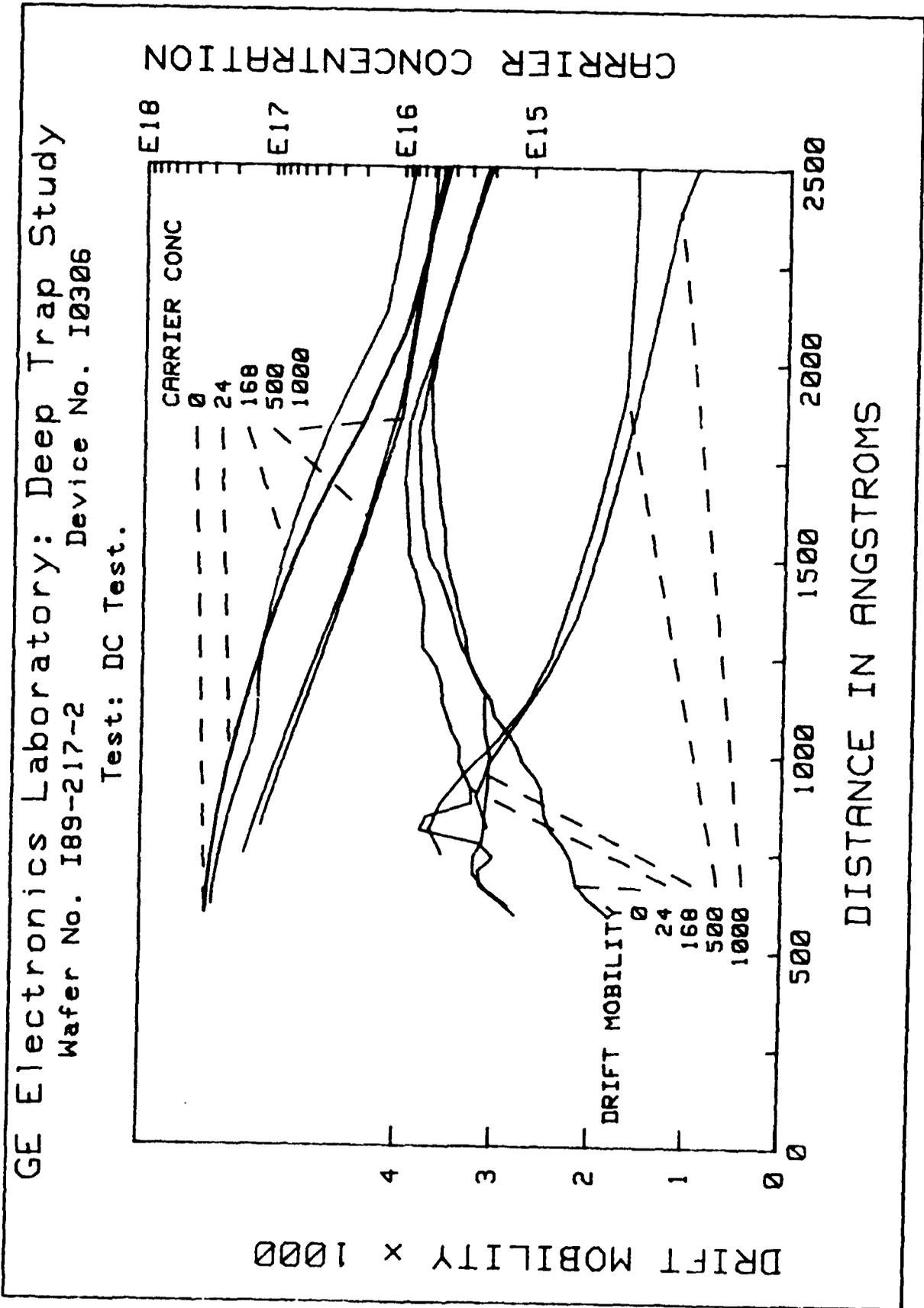
Fig. 3-2. C-V, Drift Mobility Profiles: DC Test, P   F0307

GE Electronics Laboratory: Deep Trap Study
Wafer No. I89-205-1   Device No. F0307
Test: DC Test.
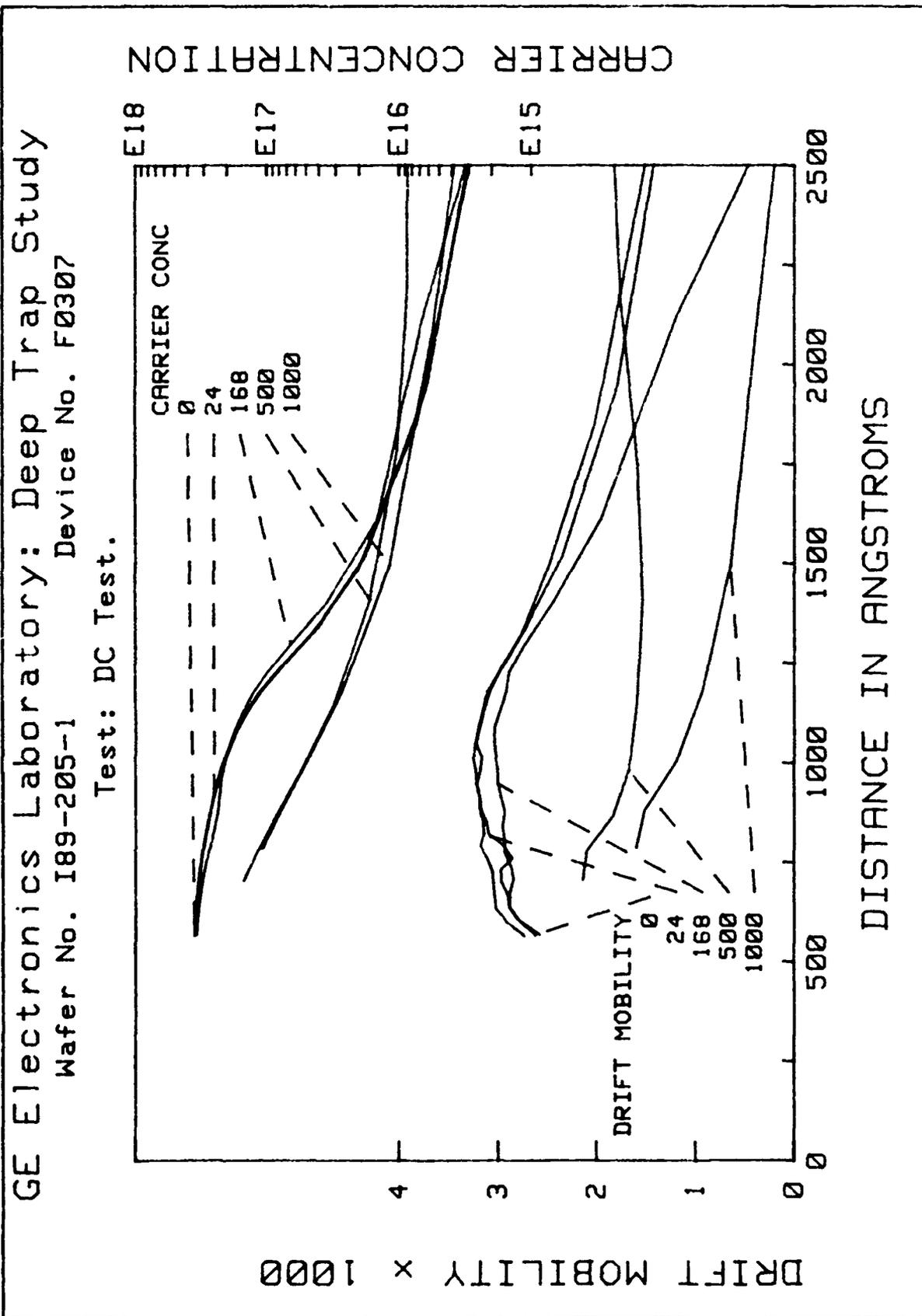
Fig. 3-3. C-V, Drift Mobility Profiles: Thermal Stability, No P   G0306

GE Electronics Laboratory: Deep Trap Study
Wafer No. I89-217-2   Device No. G0306
Test: High Temperature Stability.

CARRIER CONC
0
24
168
500
1000

DRIFT MOBILITY
0
24
168
500
1000

CARRIER CONCENTRATION

DRIFT MOBILITY × 1000

DISTANCE IN ANGSTROMS
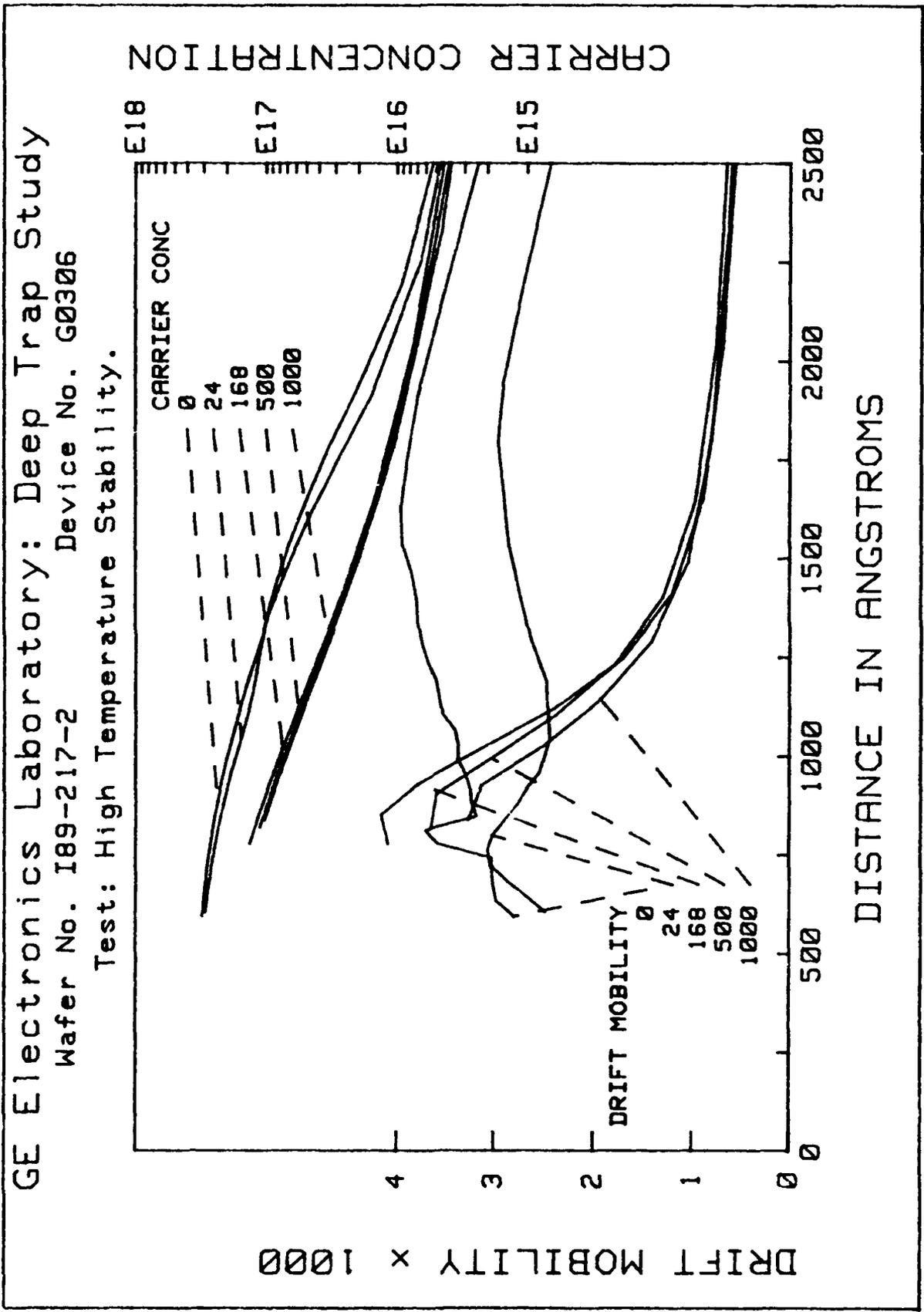
Fig. 3-4. C-V, Drift Mobility Profiles: Thermal Stability, P   D0407
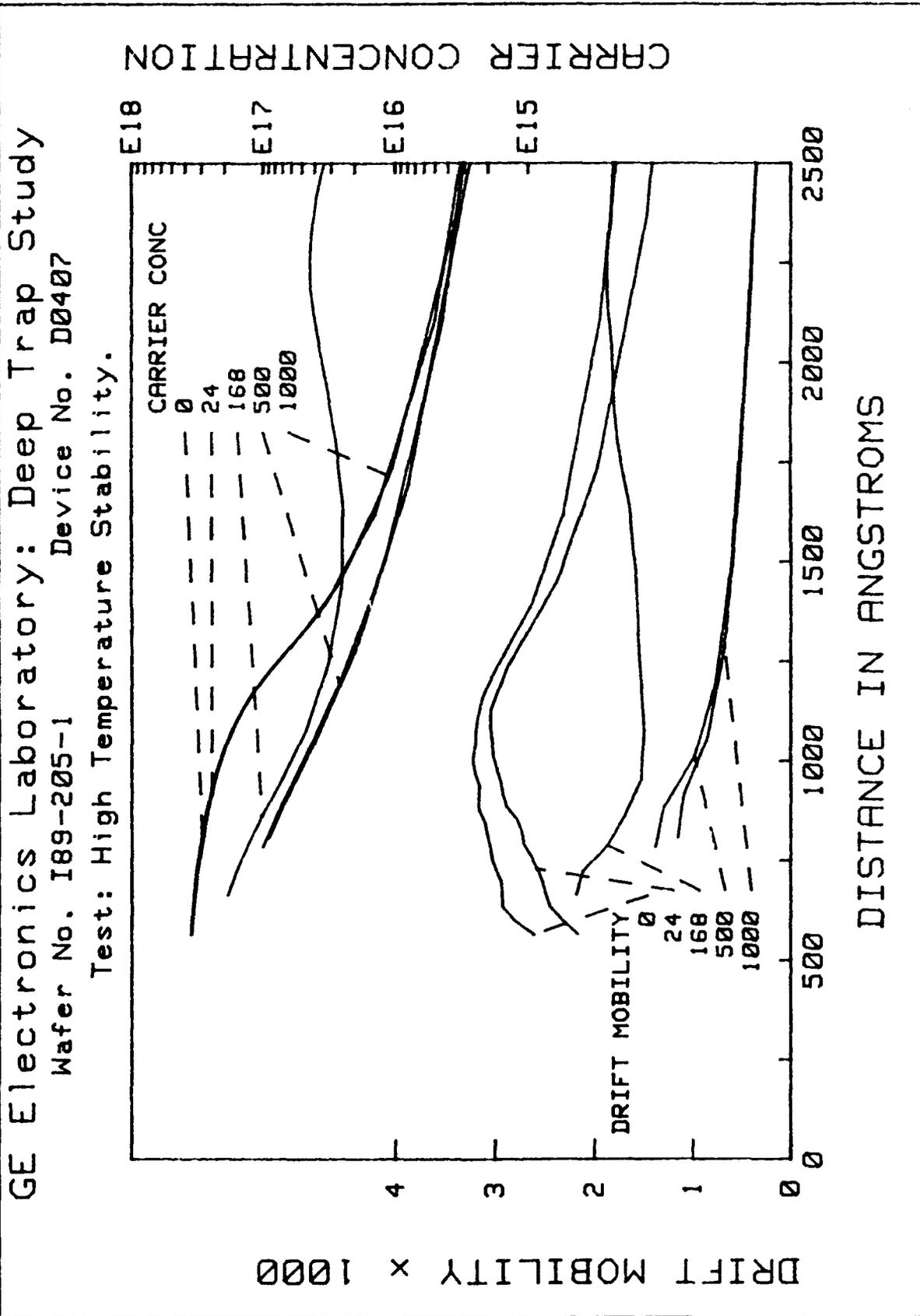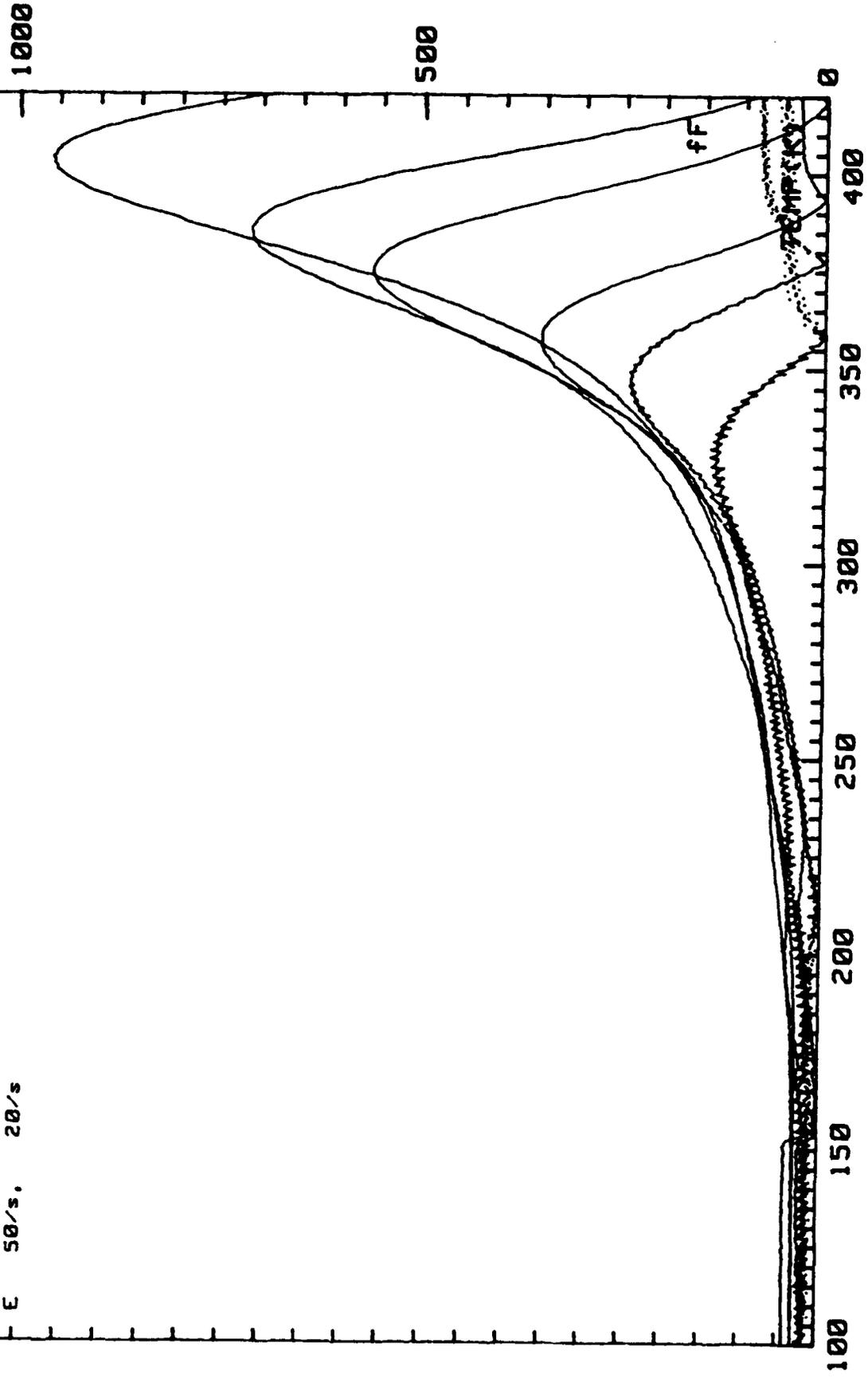
FIGURE 3-5. Initial DLTS Spectrum: No P (DC Test) G0506

41
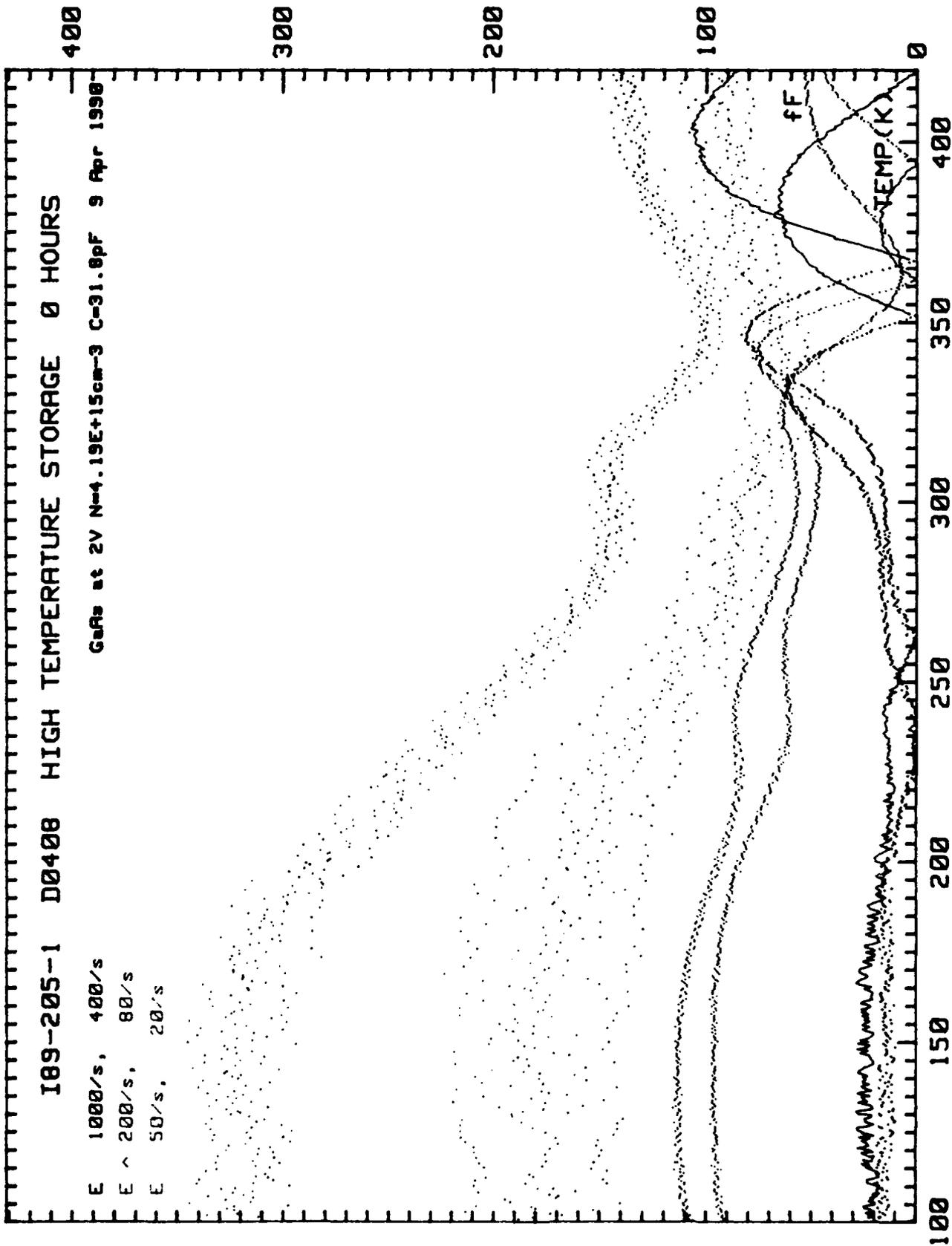
FIGURE 3-6. Initial DLTS Spectrum: P (Thermal Stability)   D0408
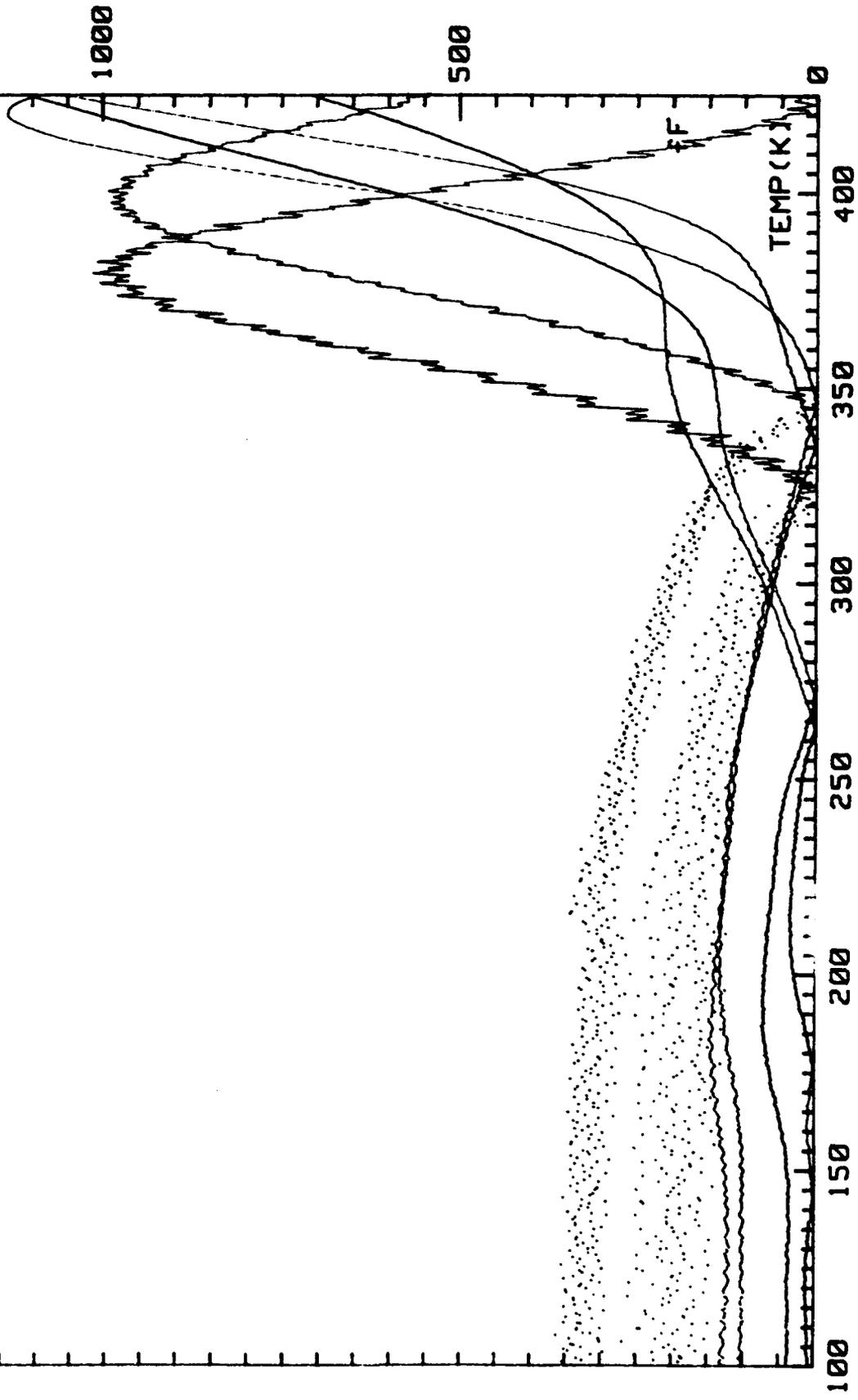
FIGURE 3-7. Final DLTS Spectrum 1000 Hours DC Test, No P   G0506

43
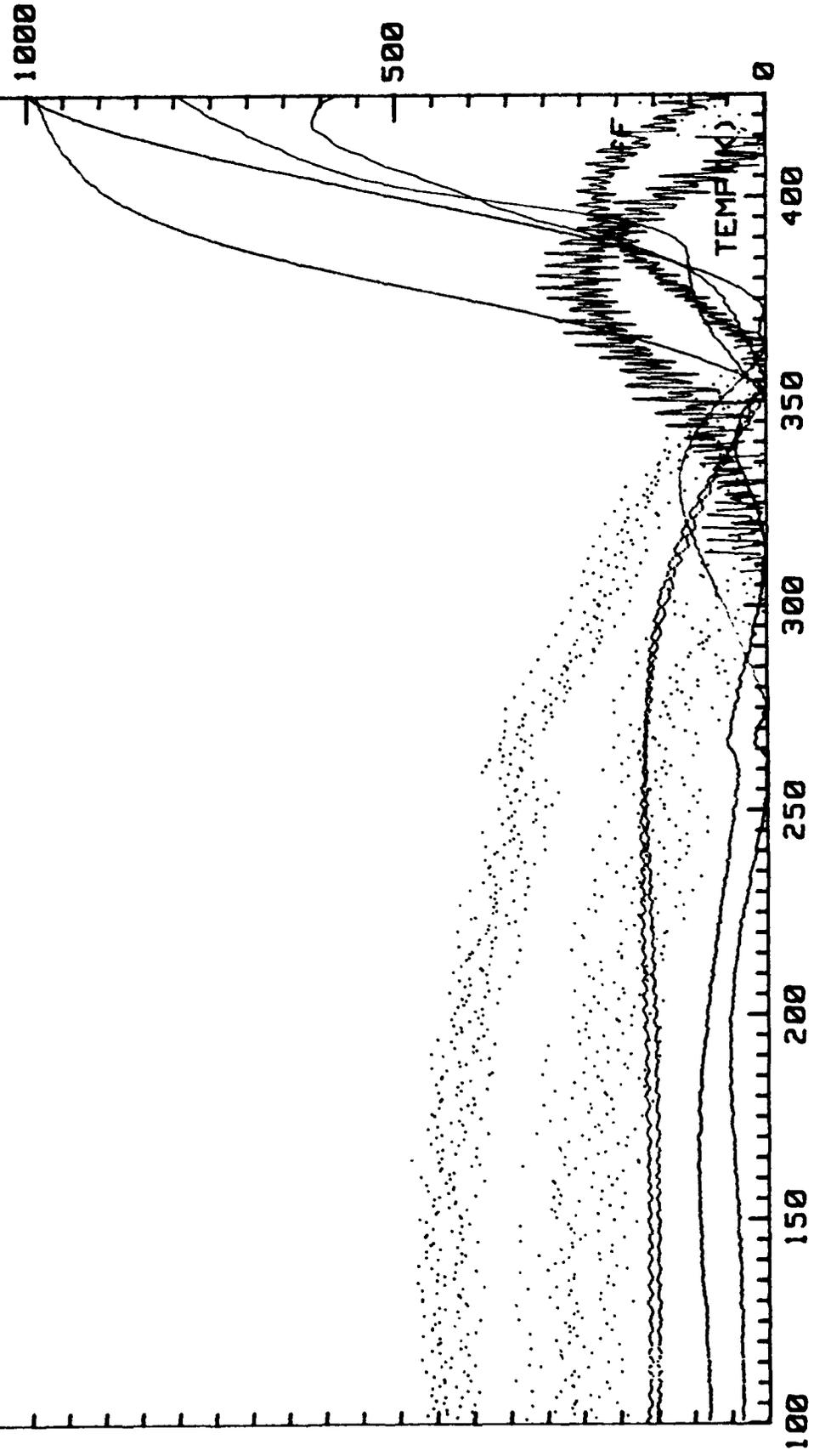
FIGURE 3-8. Final DLTS Spectrum 1000 Hours DC Test, P   B0408
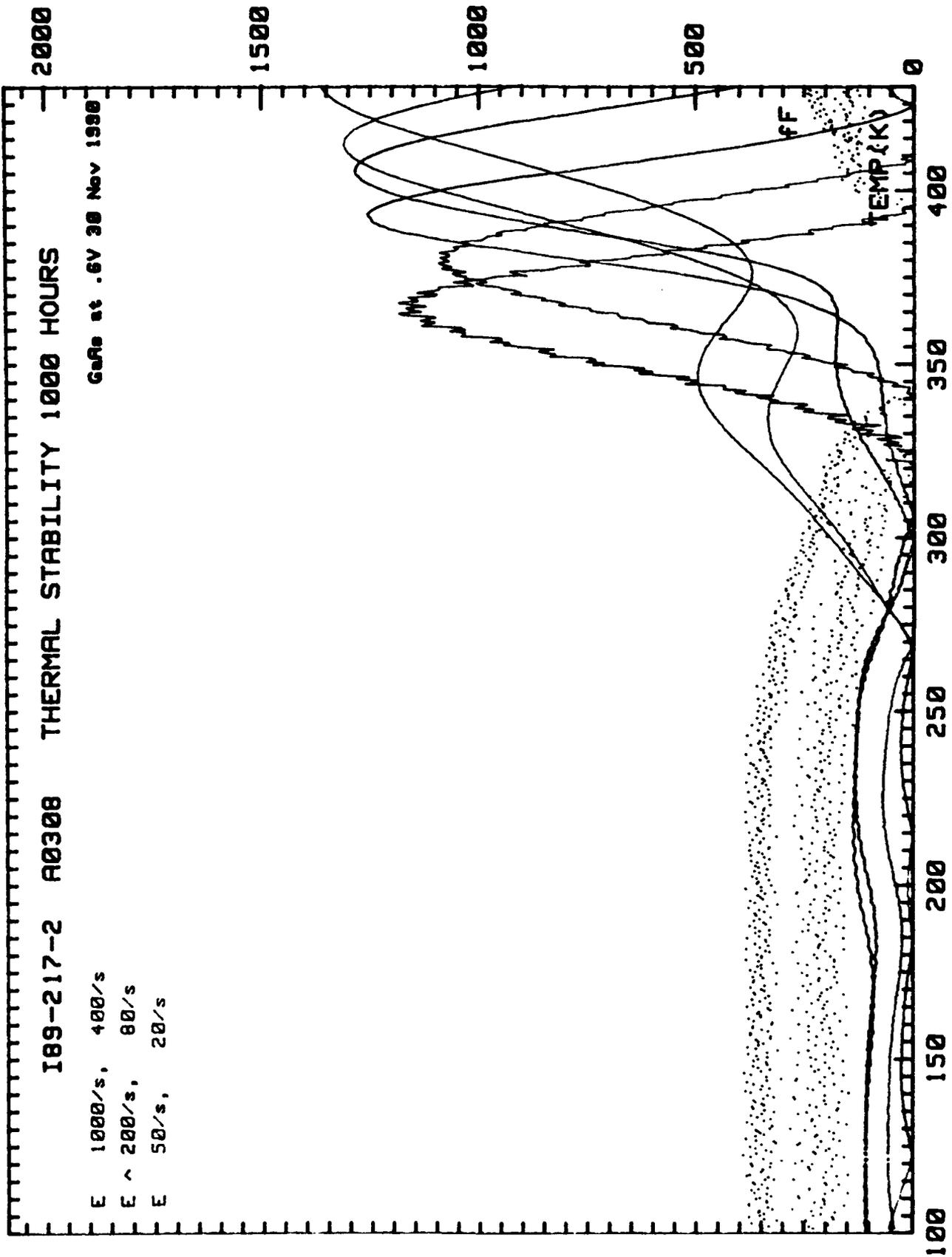
FIGURE 3-9. Final DLTS Spectrum 1000 Hours Thermal Stability, No P A0308
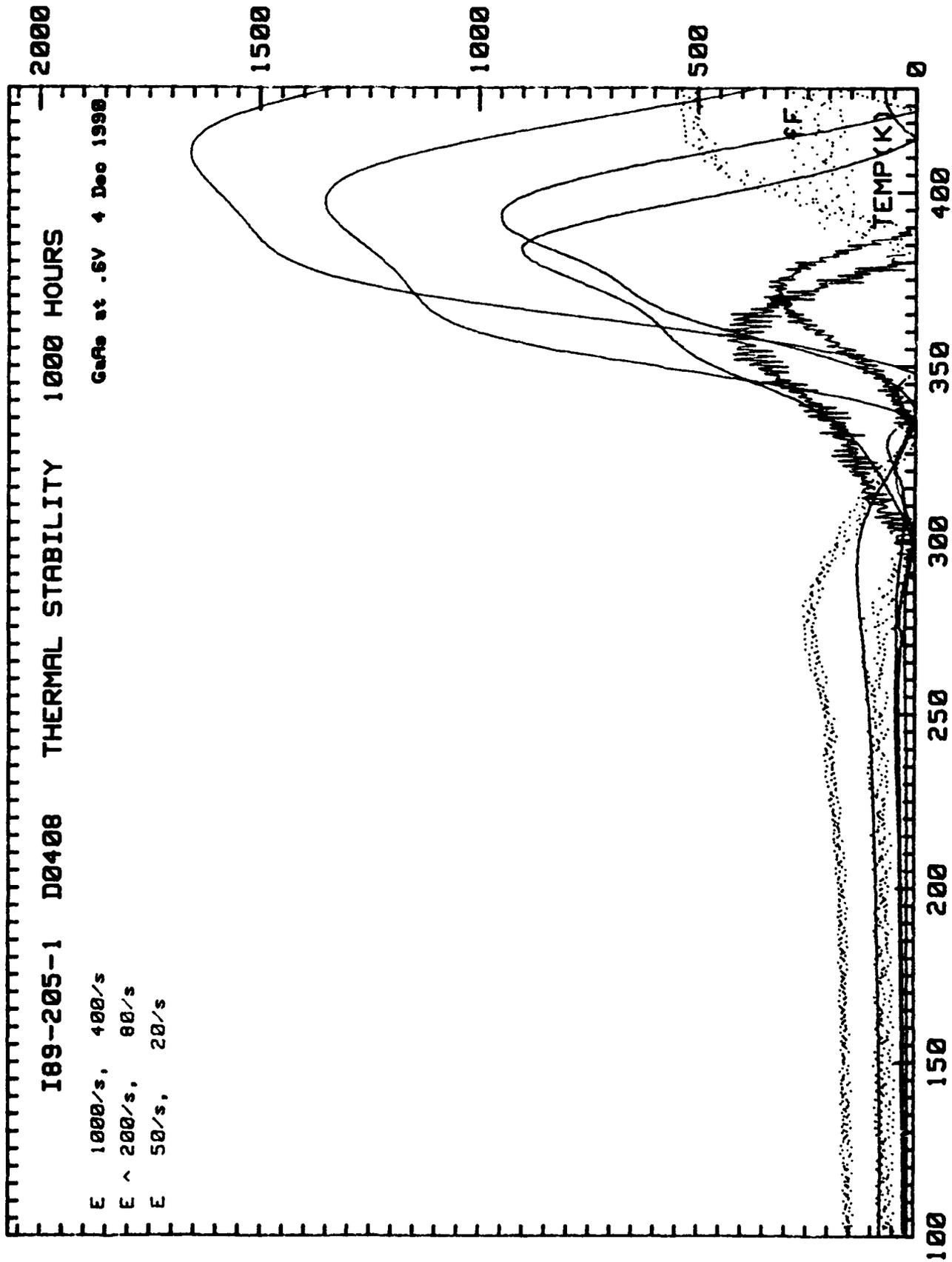
FIGURE 3-10. Final DLTS Spectrum 1000 Hours Thermal Stability, P   D0408

G0506   No P   DC Test   EL2 Profiles
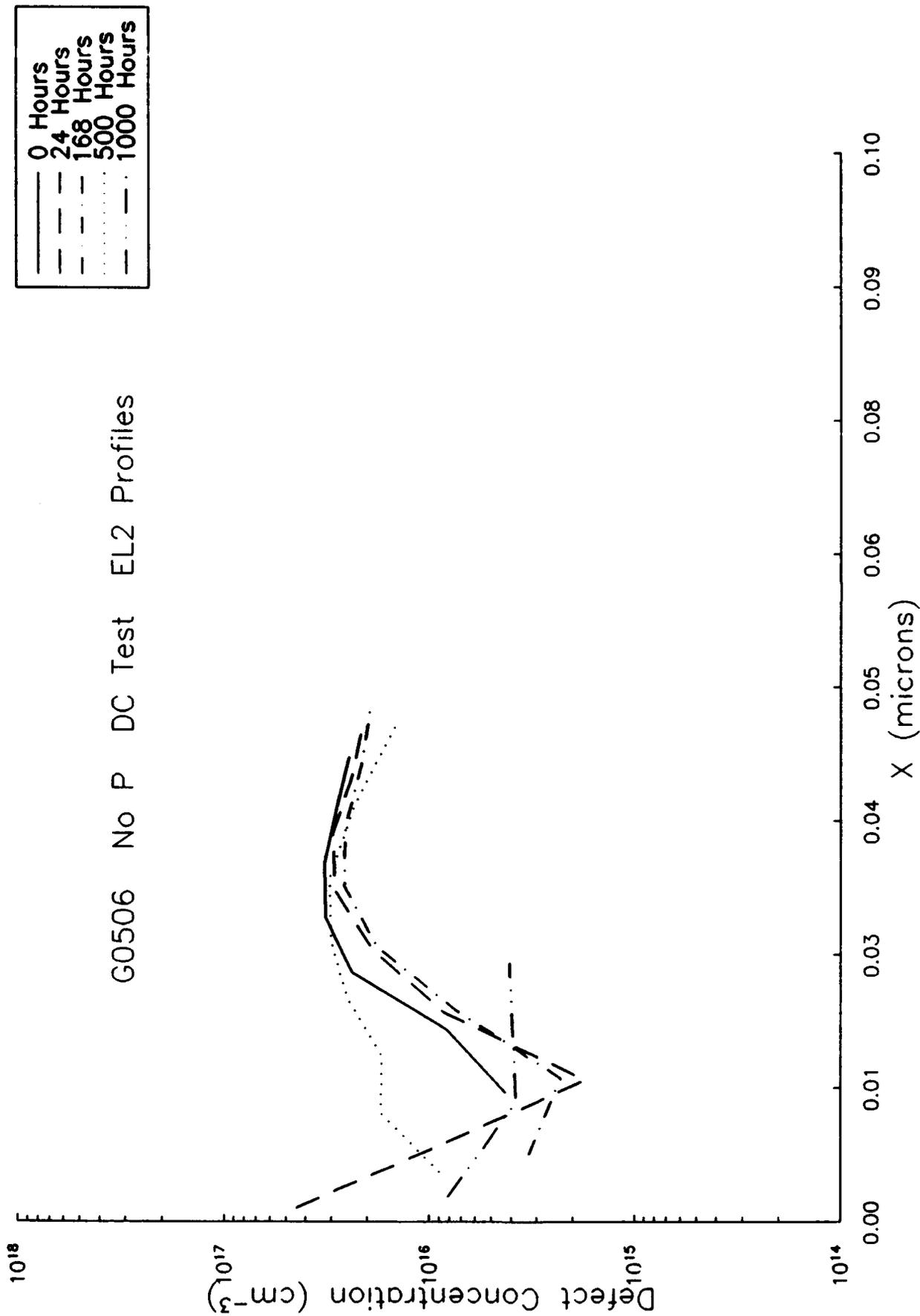
FIGURE 3-11. EL2 Profiles: DC Test, No P   G0506

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B0408 No P DC Test EL2 Profiles
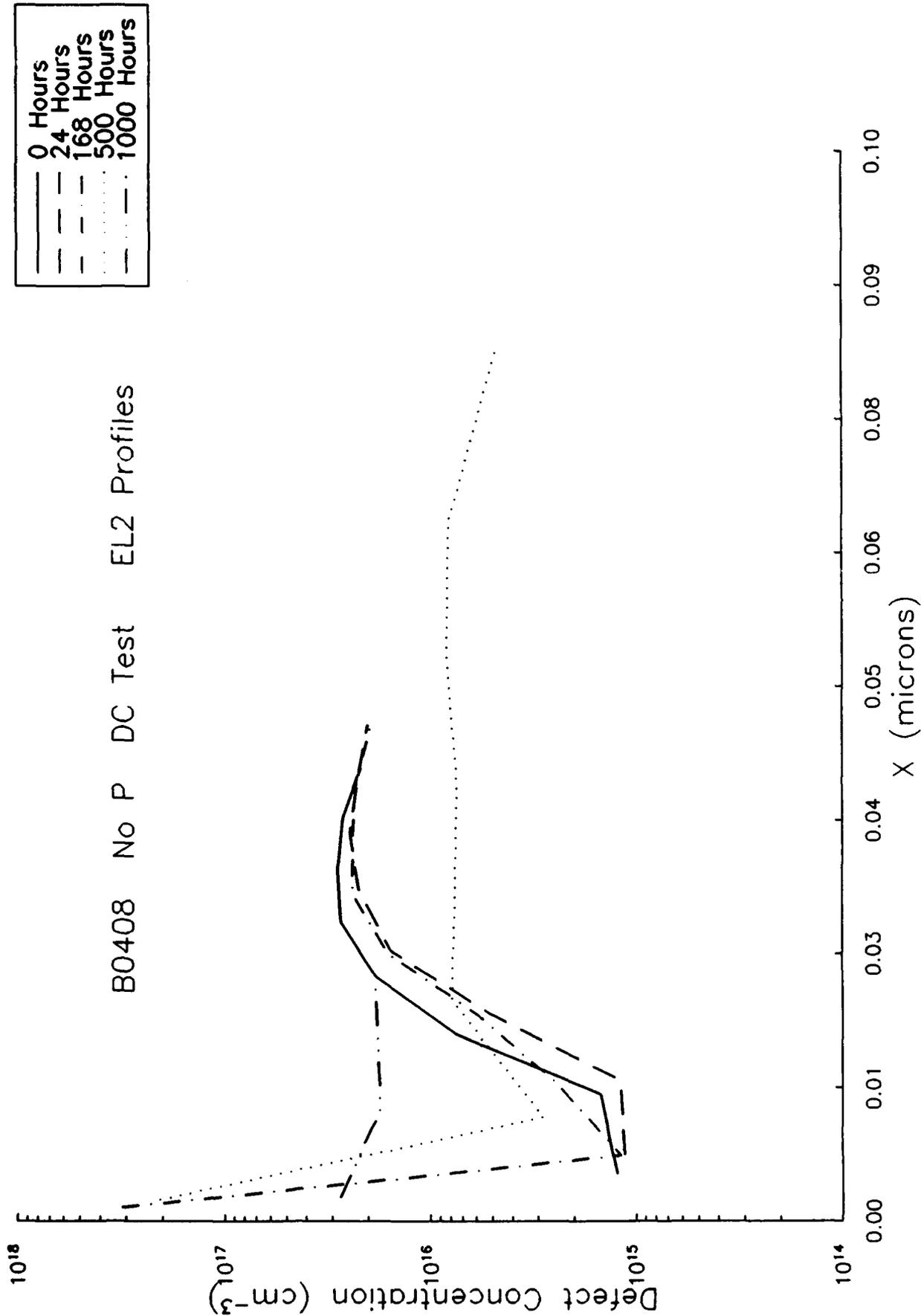
FIGURE 3-12. EL2 Profiles: DC Test, No P B0408

48
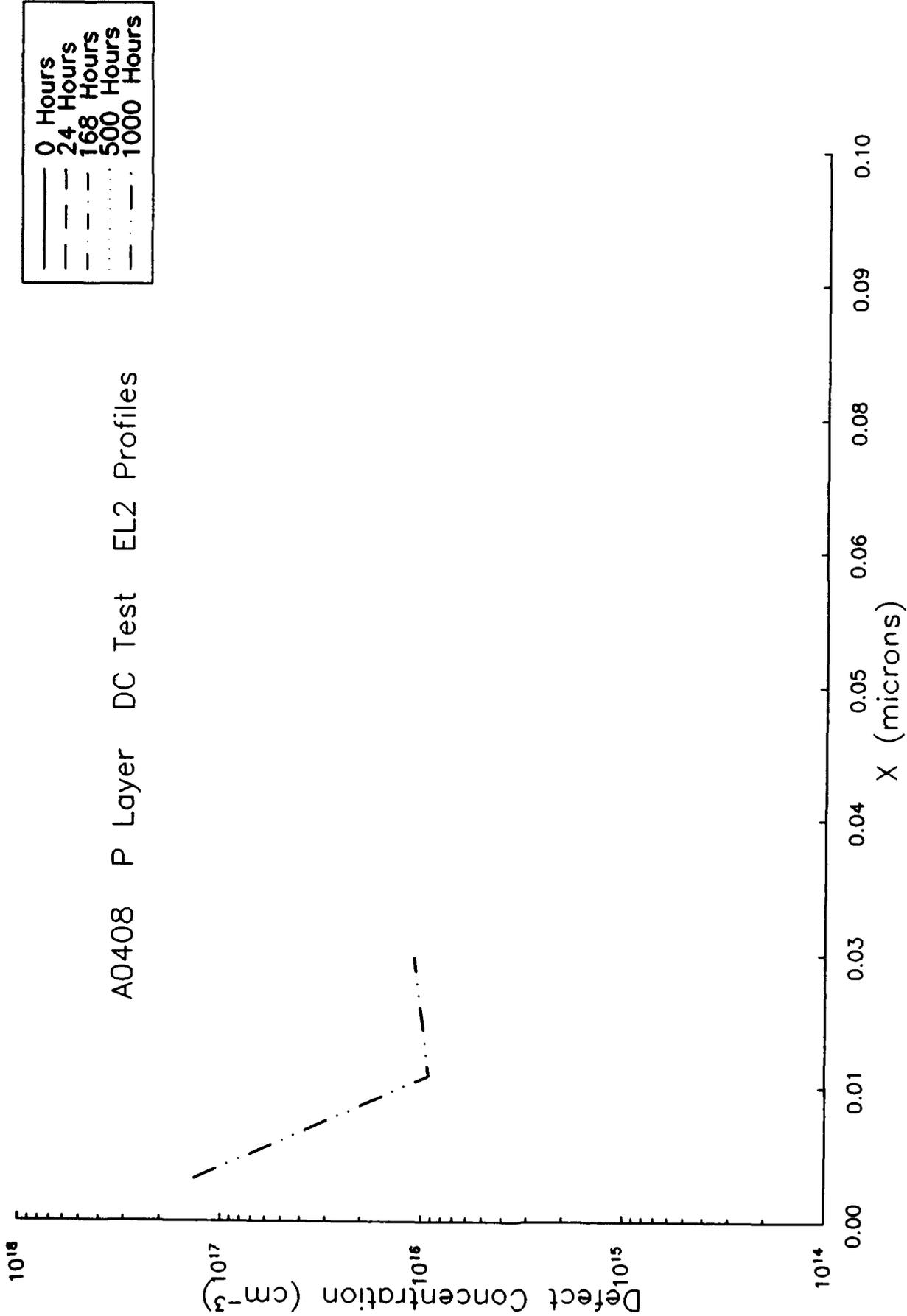
FIGURE 3-13. EL2 Profiles: DC Test, P   A0408

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B0408   P Layer   DC Test   EL2 Profiles

Defect Concentration (cm^{-3})

X (microns)

Legend:
0 Hours
24 Hours
168 Hours
500 Hours
1000 Hours
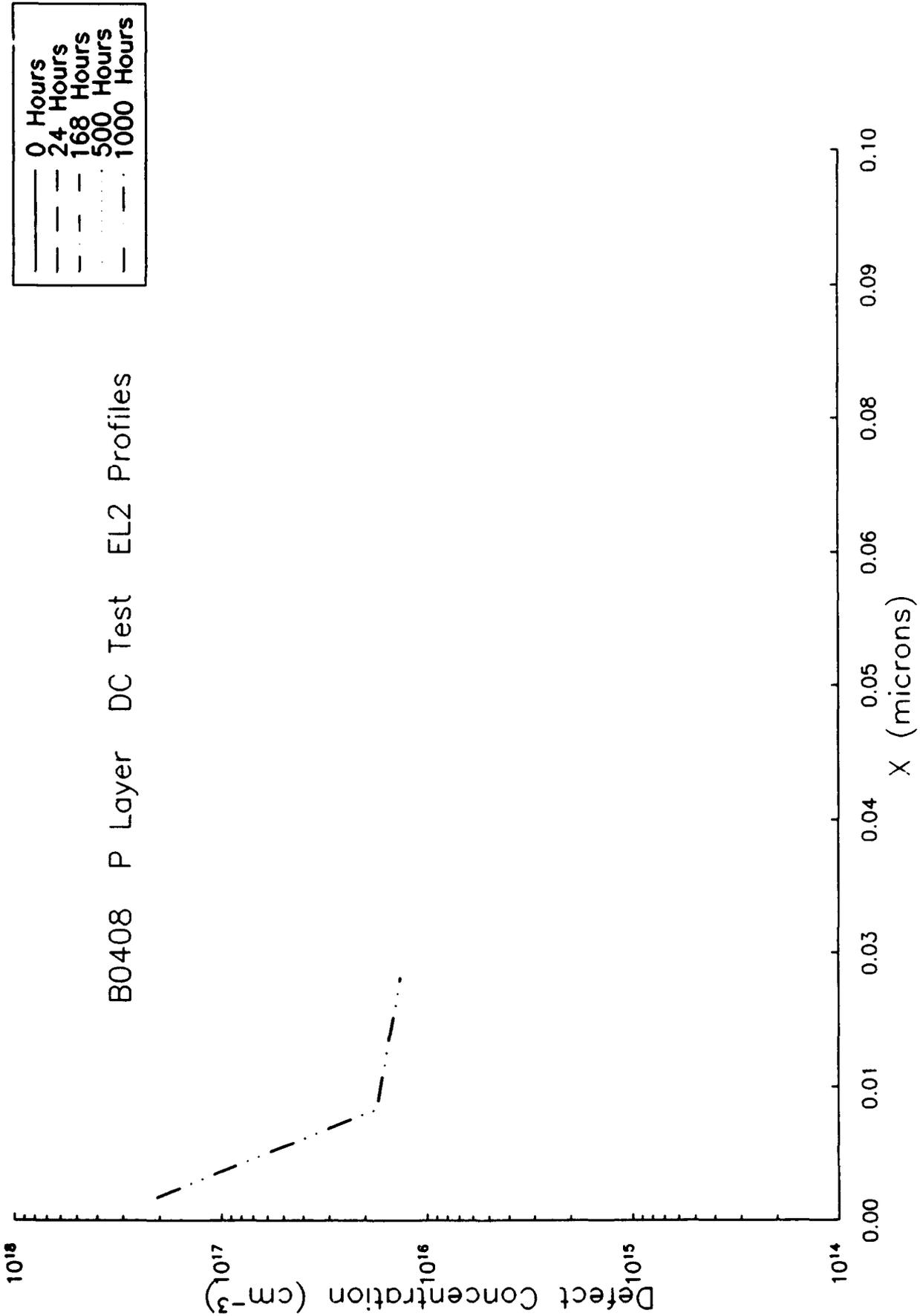
FIGURE 3-14. EL2 Profiles: DC Test, P   B0408

50

A0308 No P Thermal Stability EL2 Profiles
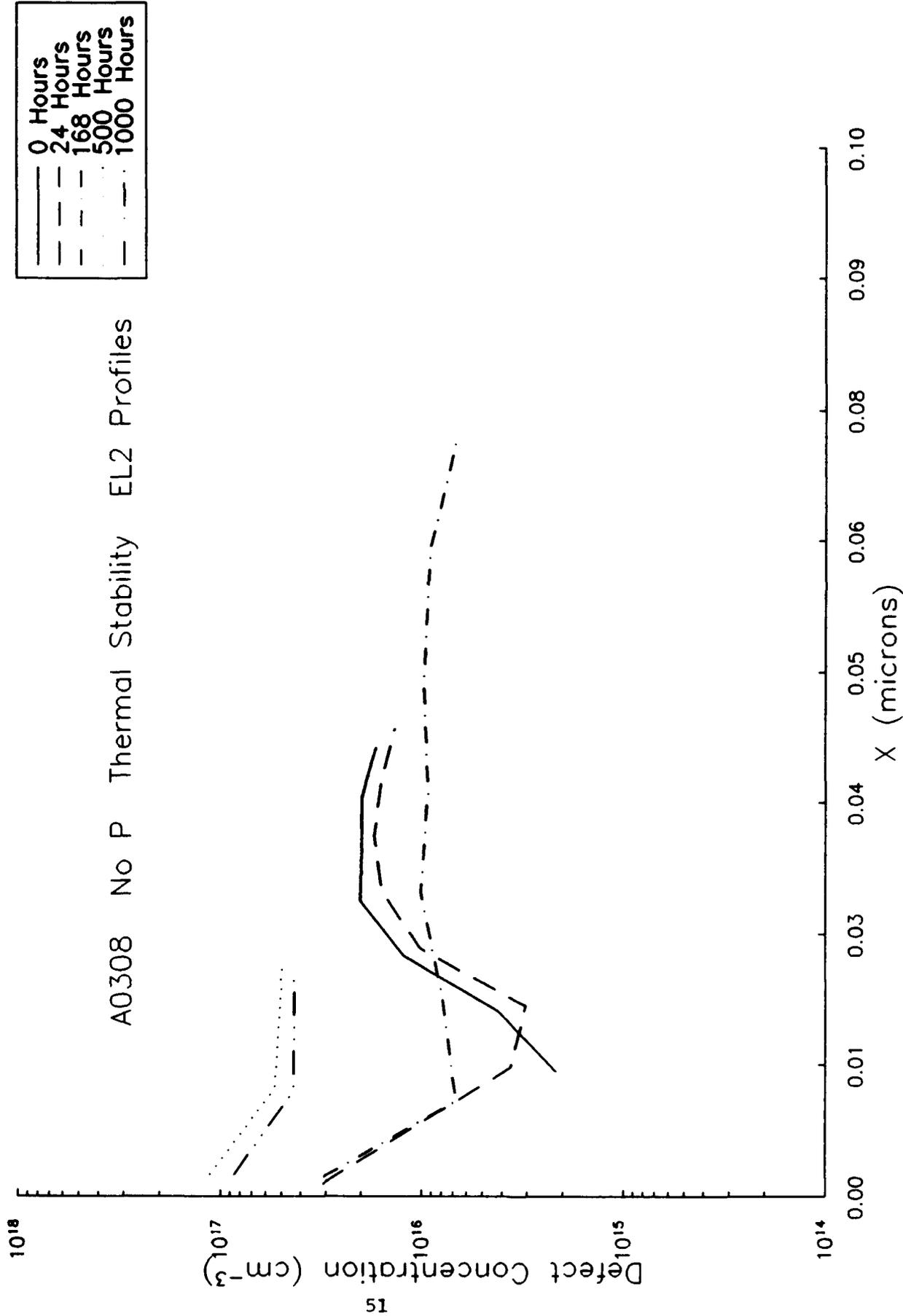
FIGURE 3-15. EL2 Profiles: Thermal Stability, No P   A0308

51

I0308 No P Thermal Stability EL2 Profiles

Legend:
- 0 Hours
- 24 Hours
- 168 Hours
- 500 Hours
- 1000 Hours

X-axis: X (microns)

Y-axis: Defect Concentration (cm^{-3})
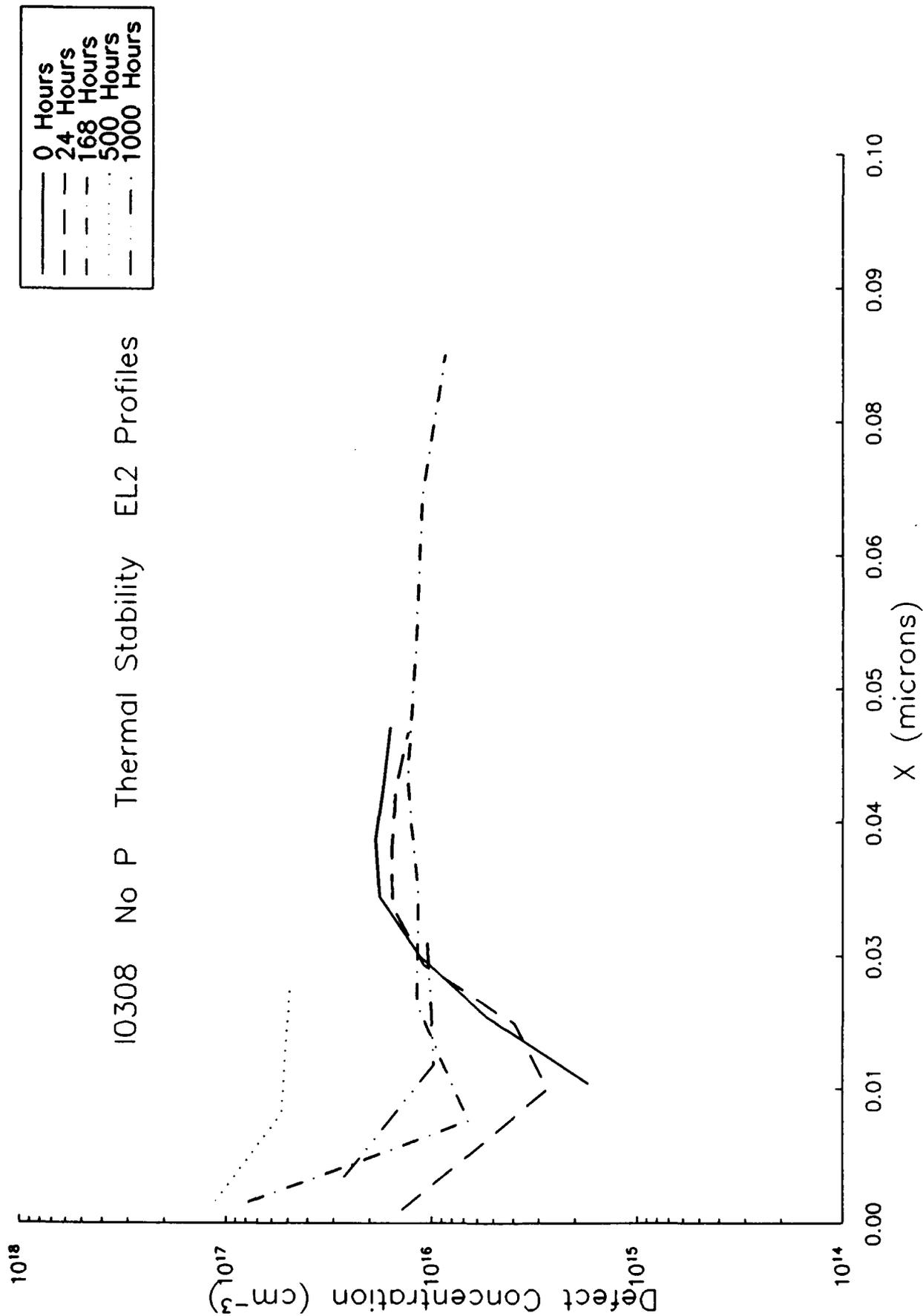
FIGURE 3-16. EL2 Profiles: Thermal Stability, No P   I0308

52

D0408 P Layer Thermal Stability EL2 Profiles

Legend:
- 0 Hours
- 24 Hours
- 168 Hours
- 500 Hours
- 1000 Hours

Defect Concentration (cm^{-3})

X (microns)
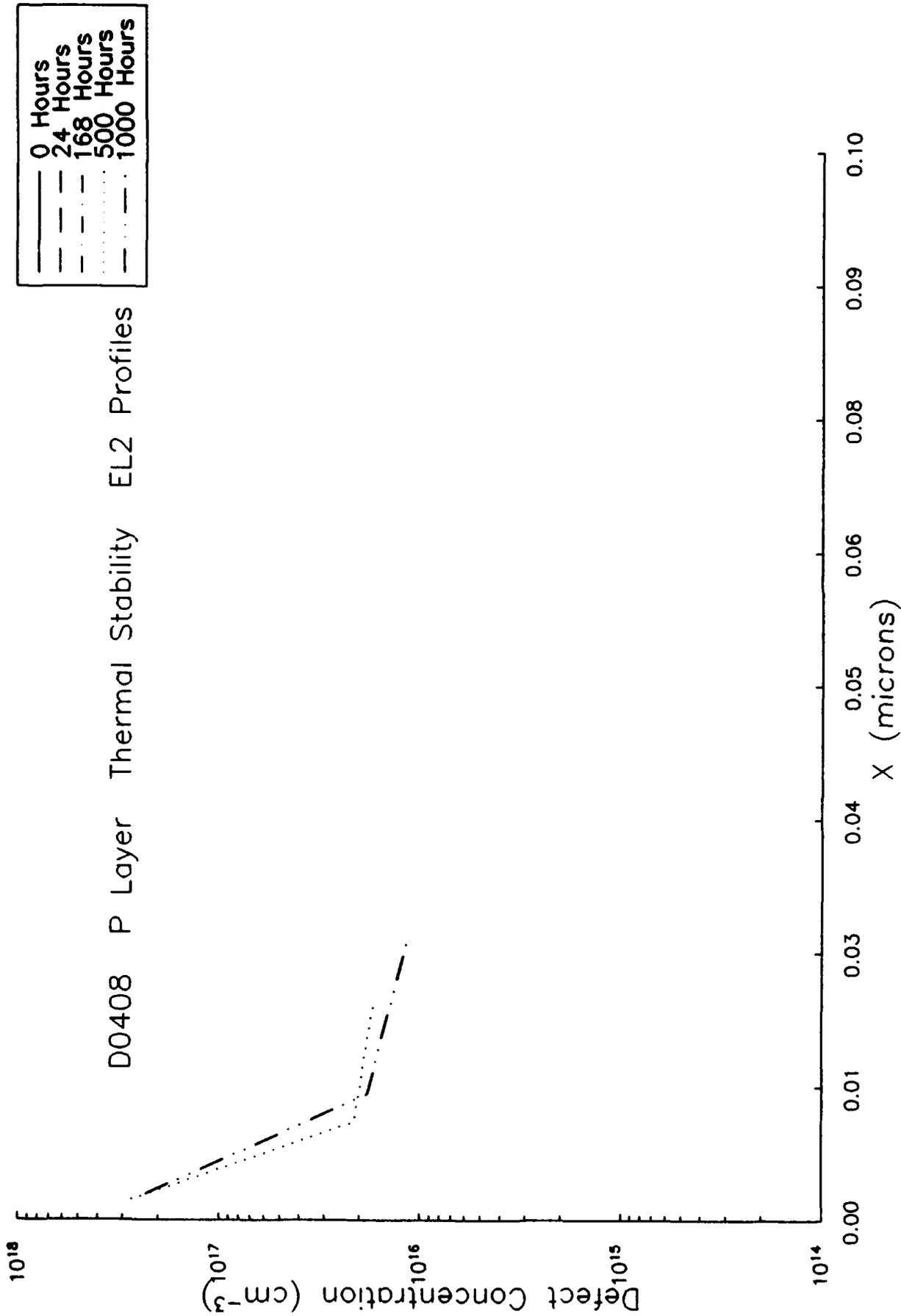
FIGURE 3-17. EL2 Profiles: Thermal Stability, P D0408

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G0509 P Layer "Thermal Stability EL2 Profiles
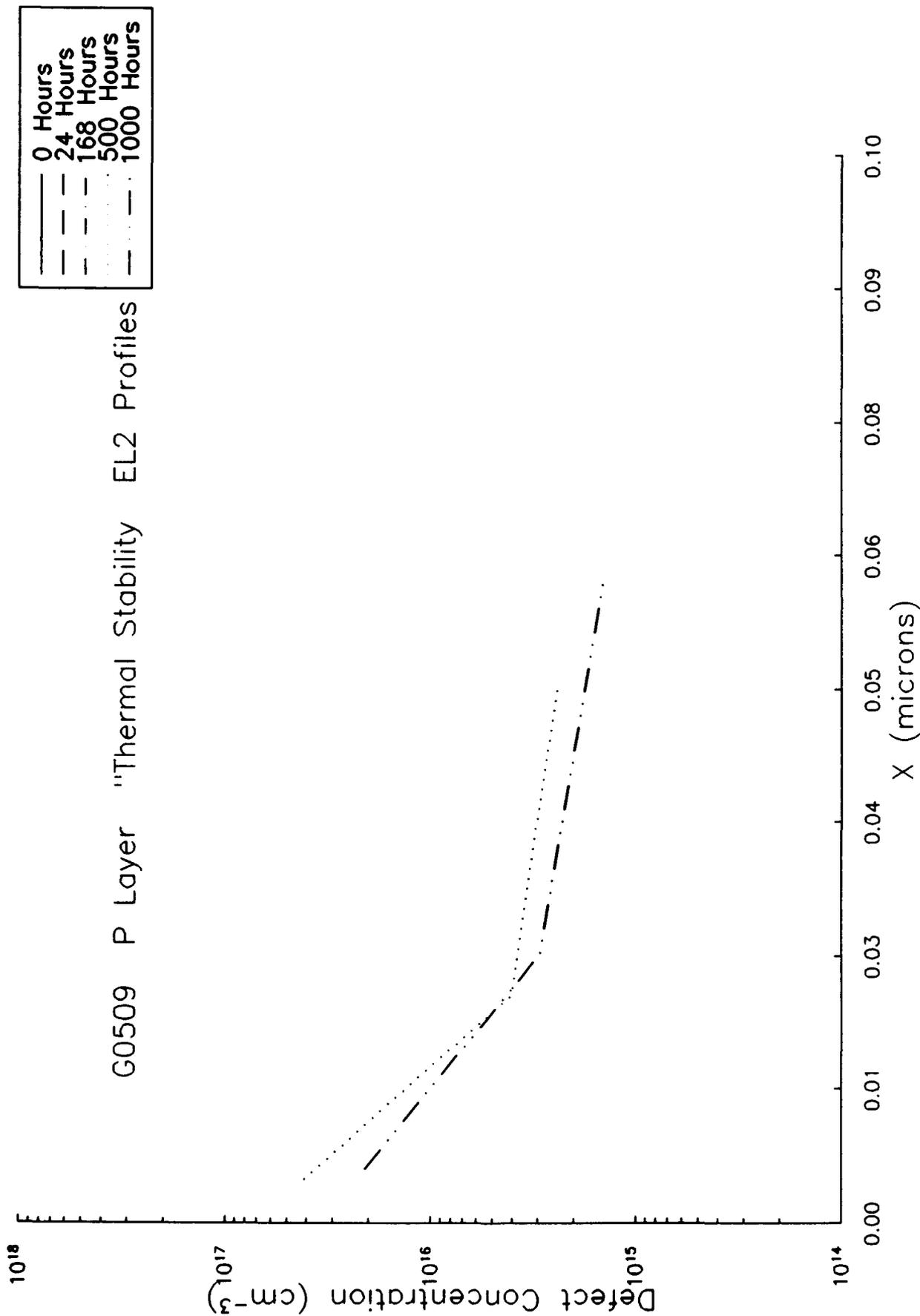
FIGURE 3-18. EL2 Profiles: Thermal Stability, P G0509

54
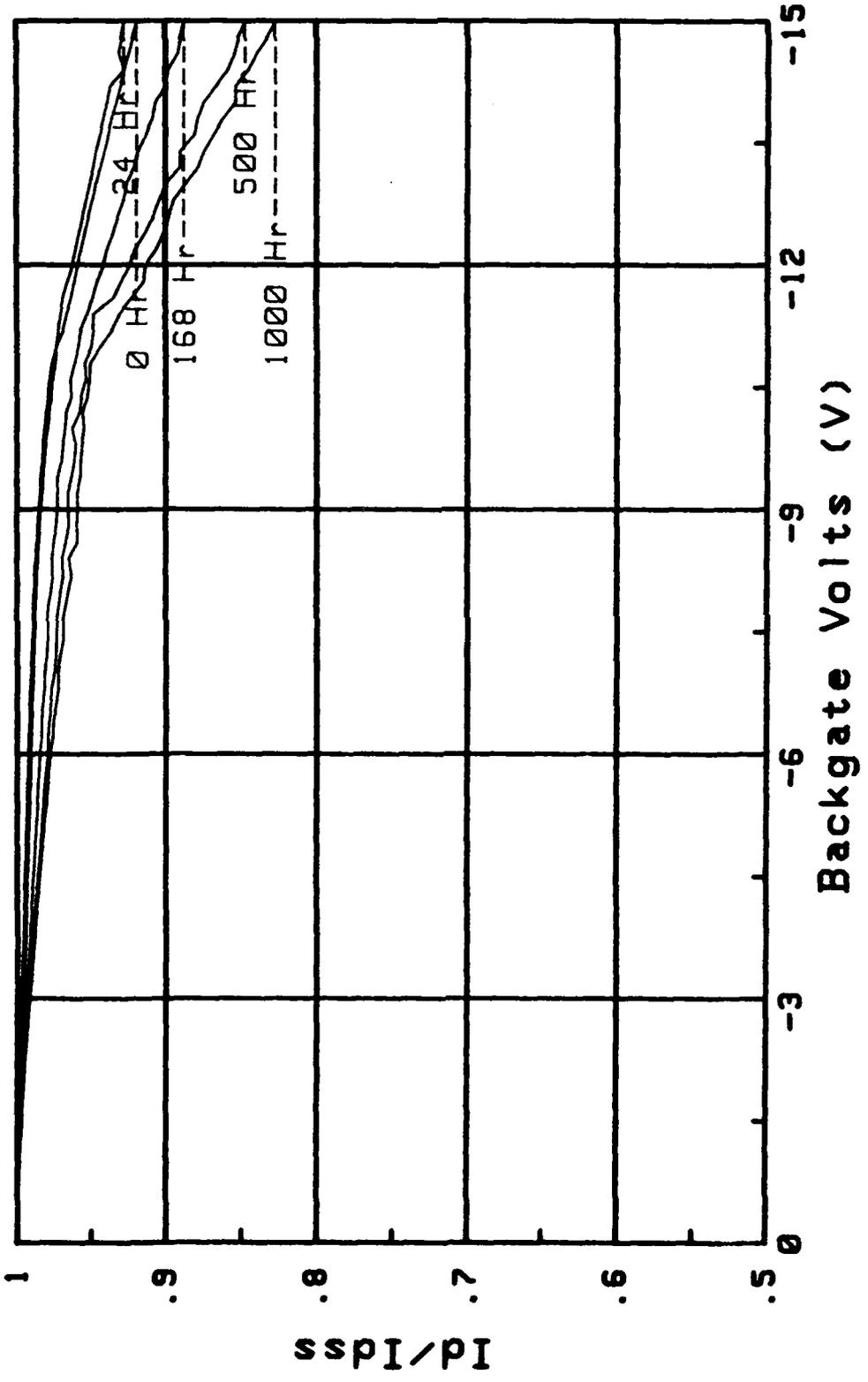
FIGURE 3-19. Backgating: DC Test, No P   I0408

FIGURE 3-20. Backgating: DC TestP   I0407
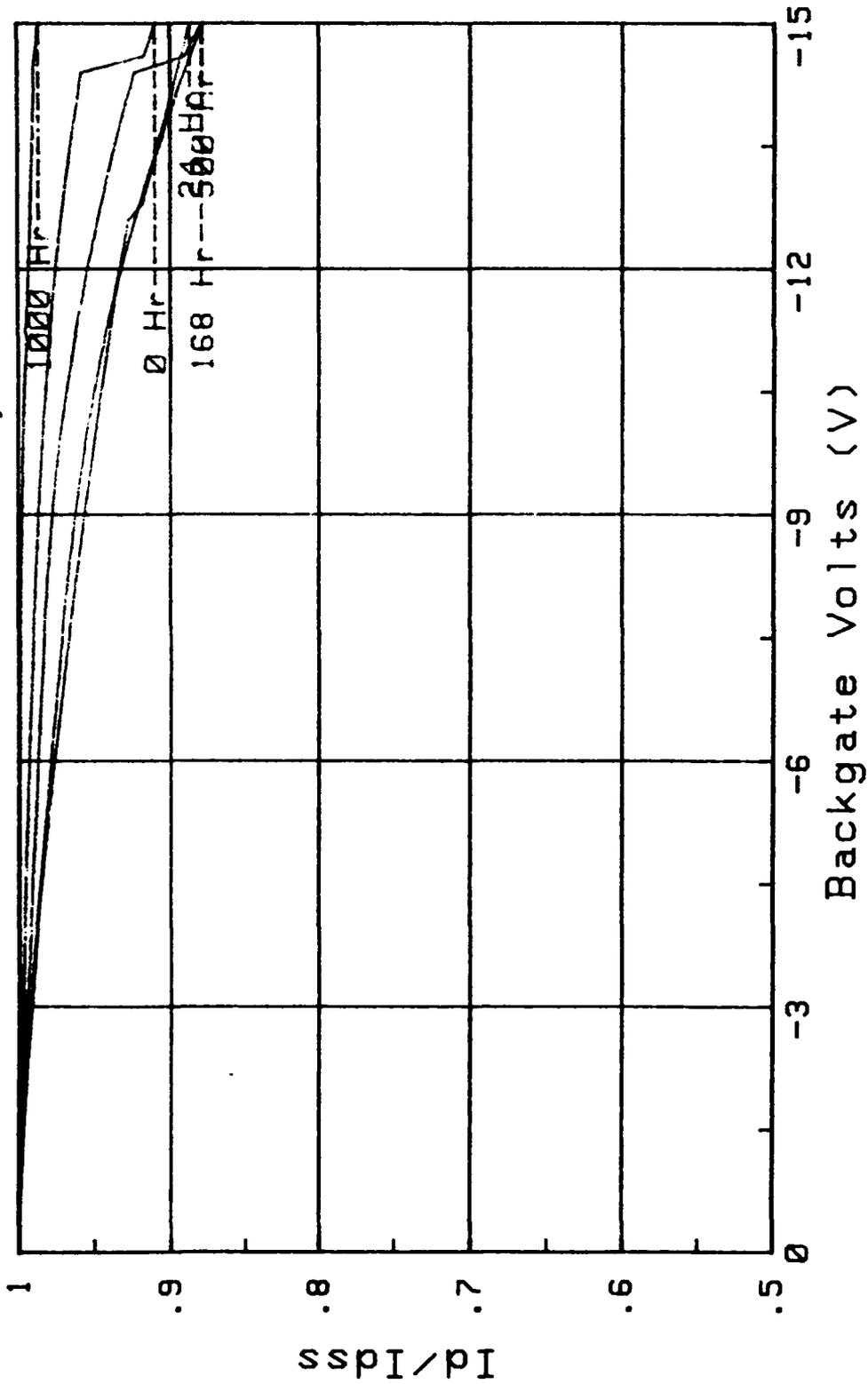
FIGURE 3-21. Backgating: Thermal Stability, No P   H0407
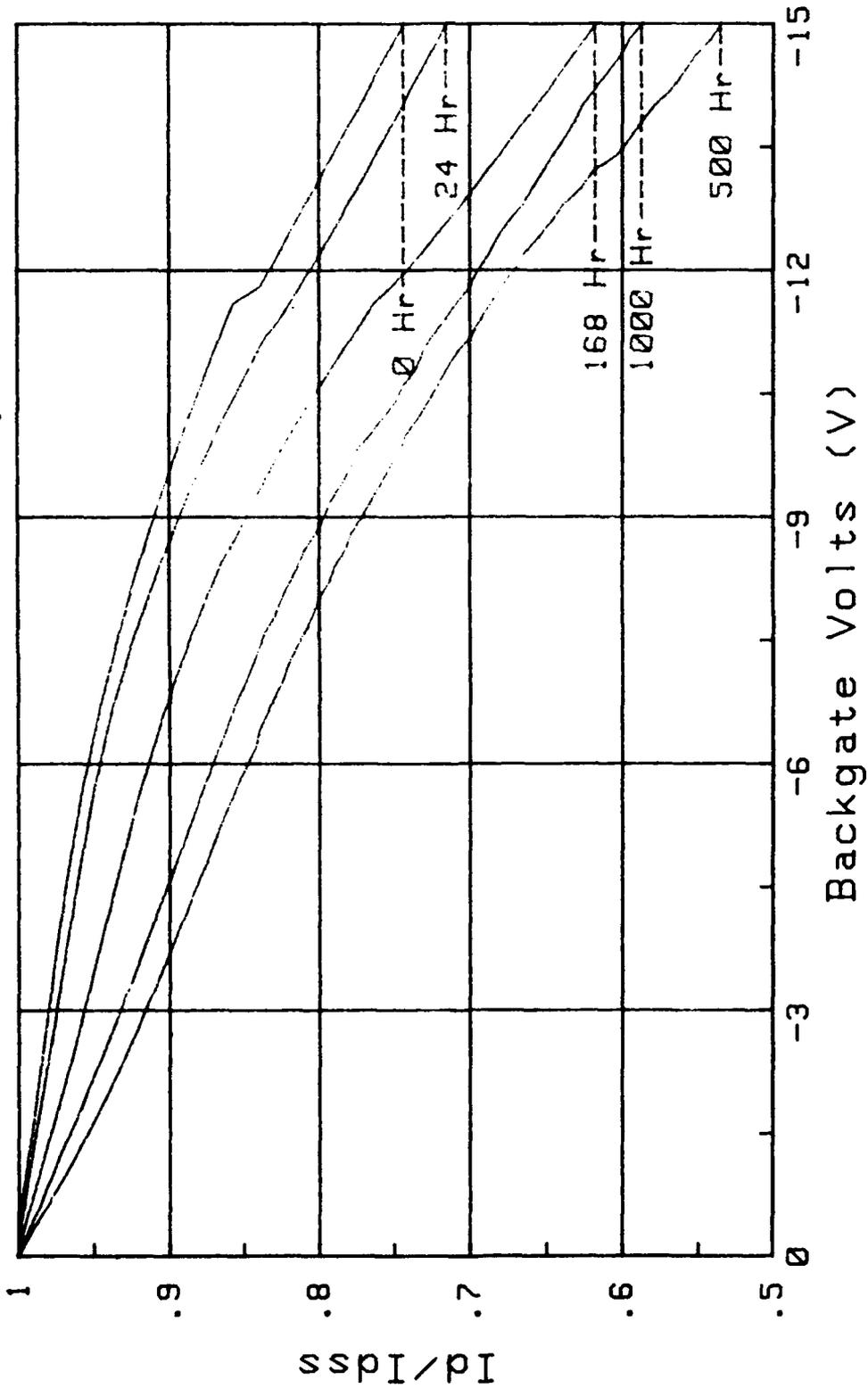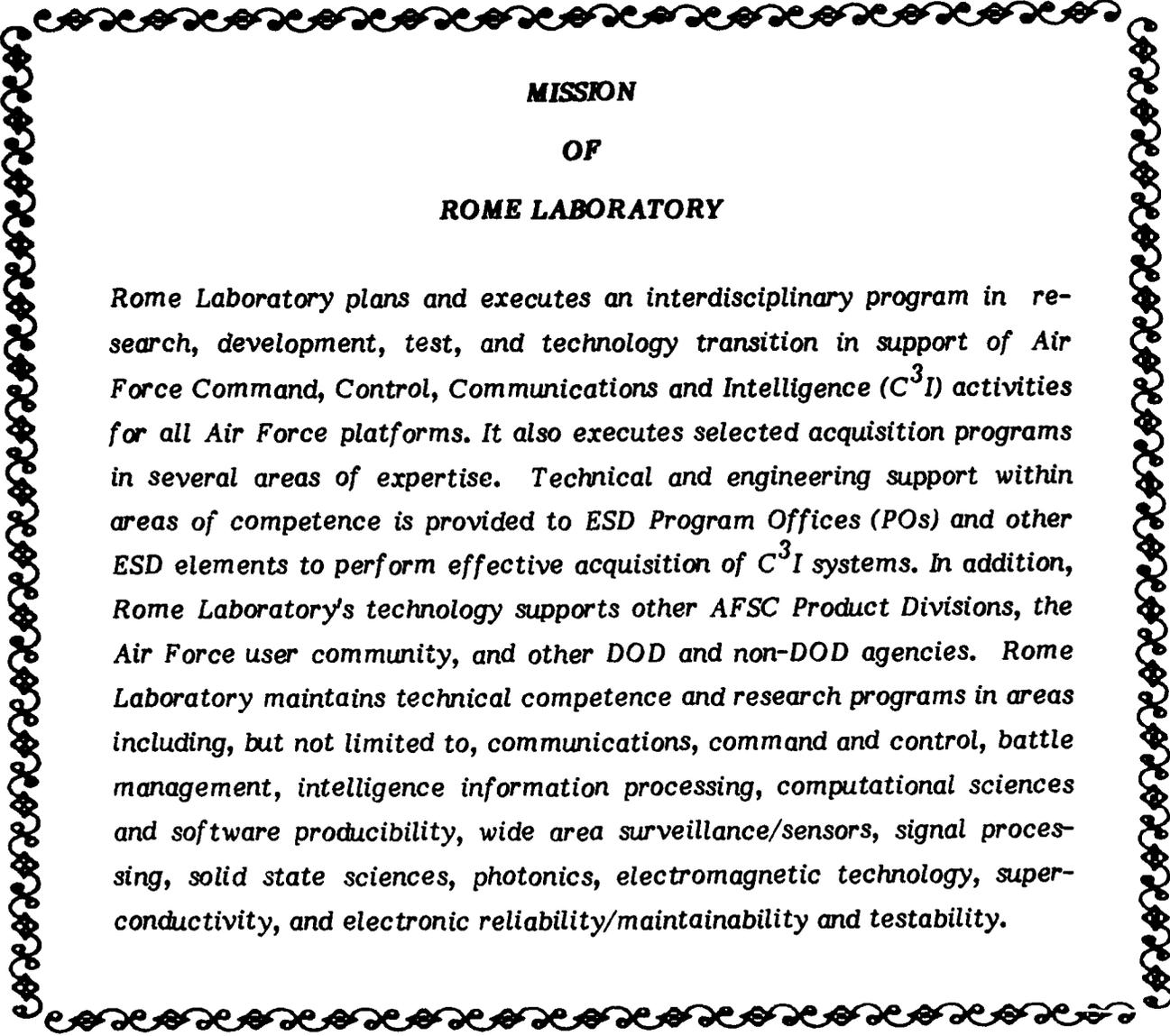
FIGURE 3-22. Backgating: Thermal Stability, P B0507

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