

Naval Research Laboratory

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AD-A237 271



NRL Memorandum Report 6843

## Analysis of FIN Line Feasibility for W-Band Attenuator Applications

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June 11, 1991



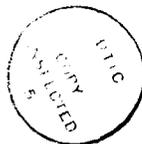
91-02862



REPORT DOCUMENTATION PAGE			Form Approved OMB No 0704-0188		
Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503					
1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE 1991 June 11	3. REPORT TYPE AND DATES COVERED Final (1989 to present)			
4. TITLE AND SUBTITLE Analysis of FIN Line Feasibility for W-Band Attenuator Applications			5. FUNDING NUMBERS 62233N RM 33R60 WU-DN 580-058		
6. AUTHOR(S) J. A. Molnar					
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Naval Research Laboratory 4555 Overlook Ave., Washington, D.C. 20375-5000			8. PERFORMING ORGANIZATION REPORT NUMBER  NRL Memorandum Report 6843		
9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)  Naval Ocean System Center San Diego, CA			10. SPONSORING / MONITORING AGENCY REPORT NUMBER		
11. SUPPLEMENTARY NOTES					
12a. DISTRIBUTION / AVAILABILITY STATEMENT  Approved for public release; distribution unlimited.			12b. DISTRIBUTION CODE		
13. ABSTRACT (Maximum 200 words)  A study was performed that examines the feasibility of developing an electronically adjustable attenuator for W-band instrumentation applications. All common transmission line structures are considered. An analysis of the merits of each transmission line structure is presented. A fin line structure is presented as having the greatest probability for success. PIN diodes are presented as the most frequently used device for attenuation and control applications. An analysis of the structural, electromagnetic and circuit characteristics was performed. The analysis presented indicates that forward biased, shunt mounted PIN diodes in a fin line structure is a viable approach for continuing investigation for the specified instrumentation application. The conclusions are supported by earlier works that are reviewed in this report.					
14. SUBJECT TERMS Attenuation                      Fin line Instrumentation                PIN Diodes W-Band                            Electronic control			15. NUMBER OF PAGES 68	16. PRICE CODE	
17. SECURITY CLASSIFICATION OF REPORT UNCLASSIFIED	18. SECURITY CLASSIFICATION OF THIS PAGE UNCLASSIFIED	19. SECURITY CLASSIFICATION OF ABSTRACT UNCLASSIFIED	20. LIMITATION OF ABSTRACT SAR		

## CONTENTS

INTRODUCTION.....	1
APPLICATION.....	1
DESIGN CONSIDERATIONS FOR ELECTRONICALLY CONTROLLED ATTENUATOR... 2	
Transmission Line Background .....	2
Fin Line Structure.....	3
Physical Considerations in Fin Line Application.....	4
Summary of Physical Characteristics Analysis.....	6
Pin Diode Characteristics .....	6
Pin Diode Physical Characteristics.....	6
Pin Diode Circuit Characteristics.....	7
Pin Diode Attenuator.....	7
Circuit Configuration .....	7
Effects of Different Biasing States .....	7
Multiple Diodes.....	8
Diode Spacing .....	8
SUMMARY OF THE MODELING ANALYSIS .....	9
FINAL CONSIDERATIONS.....	10
REFERENCES .....	10
APPENDIX - CAD Analysis of a WR-10 Fin Line Variable Attenuator.....	27



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## LIST OF TABLES

<u>Table</u>		<u>Page</u>
1	Qualitative comparison of various transmission lines.....	13
2	Qualitative comparison of various planar transmission lines.....	14

## LIST OF FIGURES

<u>Figure</u>		<u>Page</u>
1	Useful operating ranges of various transmission lines for microwave and millimeter wave circuits .....	12
2	Basic fin line structures .....	15
3	Fin line housing proposed by Meier .....	15
4	Normalized guide wavelength $\lambda/\lambda_0$ and characteristic impedance Z versus percentage change in substrate thickness d and dielectric constant $\epsilon_r$ .....	16
5	Typical field lines for basic fin line structures .....	16
6	Effect of finite metalization on the propagation characteristics of unilateral fin line.....	17
7	Normalized guide wavelength $\lambda/\lambda_0$ and characteristic impedance Z versus frequency of unilateral fin line .....	17
8	Effect of displacing the slot on the normalized guide wavelength $\lambda/\lambda_0$ and characteristic impedance Z.....	18
9	Normalized guide wavelength $\lambda/\lambda_0$ and characteristic impedance Z versus frequency of unilateral fin line with laterally displaced dielectric substrates (dielectric closest to metal wall) .....	18
10	Normalized guide wavelength $\lambda/\lambda_0$ and characteristic impedance Z versus frequency of unilateral fin line with laterally displaced dielectric substrates (fin closest to metal wall).....	19
11	Schematic representation of fin line displaying taper and quarter-wave transformer characteristics.....	19
12	(a) Circular arc taper (b) Geometrical parameters for drawing circular arcs.....	20

## LIST OF FIGURES (Cont'd)

<u>Figure</u>		<u>Page</u>
13	Comparison between various taper contours for an example at 34 GHz .....	20
14	(a) Single-section quarter-wave transformer using protrusions, (b) single-section quarter-wave transformer using notches, (c) equivalent homogeneous waveguide model.....	21
15	Two-section quarter-wave transformer using: (a) step protrusions and (b) step notches.....	21
16	Typical planar PIN diode.....	22
17	Typical doping profile for a p <sup>+</sup> -p-n <sup>+</sup> diode .....	22
18	PIN diode I-V characteristics .....	23
19	RF Electrical Models of PIN Diode.....	23
20.a	Series mounted diode attenuator configuration .....	24
20.b	Parallel mounted diode attenuator configuration.....	24
21	Transmission behavior of W-band series type PIN attenuator (Series configuration).....	24
22	Transmission behavior of W-band parallel type PIN attenuator (Shunt configuration).....	25
23	Circuit diagram for pi-network .....	25

## LIST OF (APPENDIX) FIGURES

<u>Figure</u>		<u>Page</u>
1	The geometry of the fin line structure that is the basis of the variable stepped attenuator.....	29
2	The placement of the PIN diodes in 1, 2, 3 and 4-diode attenuator configurations .....	30
3	The model of a 3-diode fin line attenuator.....	31
4	The PIN diode circuit models: a) the reverse or zero-bias model, b) the forward bias model.....	32

## LIST OF (APPENDIX) FIGURES (Cont'd)

<u>Figure</u>		<u>Page</u>
5	Fin line attenuator return loss, insertion loss, and input impedance for a single reverse-biased PIN diode with the parameters $L=0.0$ nH and $C=0.02$ pF.....	34
6	Fin line attenuator return loss, insertion loss, and input impedance for a single reverse-biased PIN diode with the parameters $L=0.02$ nH and $C=0.02$ pF.....	35
7	Fin line attenuator return loss, insertion loss, and input impedance for a single reverse-biased PIN diode with the parameters $L=0.05$ nH and $C=0.02$ pF.....	36
8	Fin line attenuator return loss, insertion loss, and input impedance for a single reverse-biased PIN diode with the parameters $L=0.1$ nH and $C=0.02$ pF.....	37
9	Two-diode attenuator results for the reverse biased case. The spacing between the diodes was found by optimizing $ S_{11} $ . $M=11.5$ mils, $C=0.02$ pF, and $L=0.02$ nH.....	39
10	Three-diode attenuator results for the reverse biased case. The spacing between the diodes was found by optimizing $ S_{11} $ . $M_1=M_2=14.6$ mils, $C=0.02$ pF, and $L=0.02$ nH.....	40
11	Four-diode attenuator results for the reverse biased case. The spacing between the diodes was found by optimizing $ S_{11} $ . $M_1=M_3=13.9$ mils, $M_2=19.0$ mils, $C=0.02$ pF, and $L=0.02$ nH.....	41
12	Two-diode attenuator results for a larger spacing in the reverse biased case. The spacing between the diodes was found by optimizing $ S_{11} $ . $M=58.2$ mils, $C=0.02$ pF, and $L=0.02$ nH.....	42
13	One-diode attenuator characteristics with $40 \mu\text{A}$ of bias current. $R=125 \Omega$ , $L=0.02$ nH.....	44
14	Two-diode attenuator characteristics with $40 \mu\text{A}$ of bias current. $R=125 \Omega$ , $L=0.02$ nH. Reverse biased spacings are used with $M=11.5$ mils.....	45
15	Two-diode attenuator characteristics with $40 \mu\text{A}$ of bias current. $R=125 \Omega$ , $L=0.02$ nH. Forward biased spacings are used with $M=24.4$ mils.....	46
16	Three-diode attenuator characteristics with $40 \mu\text{A}$ of bias current. $R=125 \Omega$ , $L=0.02$ nH. Reverse biased spacings are $M_1=M_2=14.64$ mils.....	47
17	Three-diode attenuator characteristics with $40 \mu\text{A}$ of bias current where $R=125 \Omega$ , $L=0.02$ nH. Forward biased spacings are $M_1=M_2=20.6$ mils.....	48
18	Four-diode attenuator characteristics with $40 \mu\text{A}$ of bias current where $R=125 \Omega$ , $L=0.02$ nH. Reverse biased spacings are $M_1=M_3=13.9$ mils and $M_2=19.0$ mils.....	49

## LIST OF (APPENDIX) FIGURES (Cont'd)

<u>Figure</u>		<u>Page</u>
19	Four-diode attenuator characteristics with 40 $\mu$ A of bias current where $R=125 \Omega$ , $L=0.02$ nH. Forward biased spacings are $M_1=M_3=7.0$ mils and $M_2=23.2$ mils.....	50
20	Three-diode attenuator characteristics with 120 $\mu$ A of bias current where $R=50 \Omega$ , $L=0.02$ nH. Reverse biased spacings are $M_1=M_2=14.6$ mils.....	51
21	Three-diode attenuator characteristics with 120 $\mu$ A of bias current where $R=50 \Omega$ , $L=0.02$ nH. Forward biased spacings are $M_1=M_2=20.6$ mils .....	52
22	Three-diode attenuator characteristics with 7 $\mu$ A of bias current where $R=500 \Omega$ , $L=0.02$ nH. Reverse biased spacings are $M_1=M_2=14.6$ mils.....	53
23	Three-diode attenuator characteristics with 7 $\mu$ A of bias current where $R=500 \Omega$ , $L=0.02$ nH. Forward-biased optimized spacings are $M_1=M_2=20.6$ mils. ....	54
24	A 300 mil waveguide to fin line linear taper .....	55
25	Simulation of a 300 mil long linear taper using $N=6$ sections .....	56
26	Simulation of a 300 mil long linear taper using $N=10$ sections.....	57
27	Simulation of a 300 mil long linear taper using $N=16$ sections.....	58
28	Simulation of a 300 mil long linear taper using $N=20$ sections.....	59
29	Simulation of a 300 mil long linear taper using $N=25$ sections.....	60

# ANALYSIS OF FIN LINE FEASIBILITY FOR W-BAND ATTENUATOR APPLICATIONS

## INTRODUCTION

Control components perform the essential function of distributing and limiting the propagation of electronic signals. This is true for all frequencies and also for DC. Devices such as switches, phase shifters and attenuators control and direct the flow of microwave or millimeter wave signals through some form of transmission medium. Several factors must be considered when designing a control component for a system application. Specifically, this report discusses issues contemplated in the design of an attenuator for a W-band application. The application, precision metrology, imposes additional requirements for consideration. Since the device is to operate at W-band, both the physical and electrical constraints of the design are considered.

In general, control components possess a mechanical, ferromagnetic or electronic [1, 2] distribution element. Mechanically controllable attenuators are available in rectangular waveguide for precision metrology applications at W-band. These devices are bulky and are not easily adapted to automated measurement configurations. Ferromagnetic attenuators are sensitive to transmission directions and require switching times of  $< 0.01$  seconds [3]. They are somewhat heavier than the mechanically variable attenuator, because of the magnet weight. Electronic attenuators generally are smaller, weigh less and can be stepped faster than the other types of variable attenuator, but they are less precise than a mechanical attenuator.

## APPLICATION

The goal of the project is to develop a precision electronic attenuator with a large dynamic range. This device is used for precision measurements. One application is to control the output power level from a signal generator. Another is to increase the work capacity by automating calibration capabilities. In both of these applications precision and repeatability are important.

A design goal is established for the deliverable attenuator. The attenuator must operate over the entire W-band. As such, it must have WR-10 flange parts for input and output to the device. This requirement originates from the use of WR-10 rectangular waveguide to minimize losses in the transmission structure of system designs. Since the attenuator is a stand-alone component that would find application in diverse system designs it must be compatible with a standard transmission medium.

The attenuator must have an attenuation range of 0-60 dB. Attenuation steps of 10 dB are required with an accuracy of  $\pm 1.5$  dB at the lowest step. The inaccuracy should not exceed  $\pm 3.0$  dB at the 60 dB step. Insertion loss should be  $\sim 1.5$  dB in the 0 dB step setting. SWR should be  $< 2.0$ . Repeatability should be  $\sim 0.1$  dB. The design must be suitable for incorporation into automated instrumentation configurations. This requires that the attenuator be electronically controllable and has reasonable stepping speeds on the order of  $< 1$  ms. It also must be small (i.e., 4 cm x 4 cm) and light (i.e.,  $< 0.5$  lbs.), since it may be integrated into portable instruments  $< 50$  lbs. Finally, since in the end application portability is desired, it must meet MIL-T-28800D shock and vibration specifications.

The final design will be a tradeoff of the specified characteristics. Generally, the physical design most suited to this application is the electronically steppable attenuator. This type of attenuator can

accommodate both the electrical performance and the physical constraints. A mechanical attenuator can meet all of the attenuation characteristics, but it is unlikely that automating this type of attenuator with a control motor will allow it to meet the stepping, size and weight requirements of the specification. The ferromagnetic attenuator suffers in basically the same areas: size, weight and stepping speed. Additionally it is undesirable to have a unidirectional attenuator, such as the ferromagnetic attenuator.

In conclusion, only the electronically adjustable attenuator is suitable for this precision measurement instrumentation application. Another aspect of this project will assess the new attenuator for use in calibration applications. The electronic stepping capability will reduce errors currently introduced by changing the physical connection to fixed attenuators, and greatly increase the speed of calibration.

## DESIGN CONSIDERATIONS FOR ELECTRONICALLY CONTROLLED ATTENUATOR

The selection of the attenuation method only begins the design process. Many other design decisions must occur and each must be made with consideration to the specification described for the device. The form of transmission line that will be used to implement the design is critical and must be decided first. This is a complex decision because of the great variety of transmission media available. In general, the selection is based on many factors, but often the most important is the empirical information presented in the work of other researchers, who have implemented the various transmission media.

Selection of the attenuating device and the circuit design are next in priority. A semiconductor device is most appropriate for the intended implementation. There are numerous semiconductor devices available for frequencies below 18 GHz, but a more limited set of devices for millimeter wave applications exists. There are only two devices which have been used successfully for applications in millimeter wave control electronics: PIN diodes and FETs [2]. Designers have predominantly used PIN diodes to develop electronically controllable attenuators. Reducing the selection to a single type of semiconductor device decreases the number of choices available, but detailed design simulations must still be performed to determine the required parameters for this PIN diode application.

The next two sections provide background on the transmission media and semiconductor device selection processes.

### Transmission Line Background

Numerous types of transmission lines are available. Each has certain distinct advantages and disadvantages, depending upon the application. To determine the transmission line which best suits the application for a given frequency range, the following criteria are considered:

1. Low loss or high unloaded Q,
2. Low radiation loss,
3. Low dispersion,
4. Maximum achievable bandwidth,
5. Ease of bonding solid-state devices in the case of active components,
6. Ease of integration,
7. Adequate power handling,
8. Ease of fabrication and low cost of manufacturing [4].

Using these criteria, various transmission lines can be assessed to determine their most useful operating range. Figure 1 summarizes the analysis of the operating frequency ranges for numerous popular transmission lines. Tables 1 and 2 attempt to coarsely classify each transmission line using the specified criteria. In Fig. 1 the solid line part of each transmission line's operating range indicates that no extraordinary precautions are needed to utilize this type of transmission line, while the dashed part of the line indicates where it is substantially more difficult to implement. With the proper precautions and design considerations each of the transmission lines has demonstrated applicability over the indicated frequency range. As seen in Fig. 1, rectangular waveguide, microstrip line, suspended stripline, suspended microstrip, fin line and dielectric integrated guides have demonstrated their utility over the entire W-band. These transmission lines are all planar, with the exception of the rectangular waveguide.

By examining Table 1, it is evident that the rectangular waveguide has many positive propagation characteristics, such as low loss, which makes it a desirable transmission line. However, for the attenuator application, losses are not considered a high priority since the actual transmission length will be short. The ease of integration and physical constraints have a higher priority. It is considerably more difficult to fabricate any device in a rectangular waveguide because of the physical tolerances that must be observed and met.

The stripline has good propagation characteristics, but Table 2 indicates that they are not good for incorporating chip type devices. Primarily, it is harder to incorporate devices into the physical geometry of the stripline than it is to incorporate devices into the other structures. As a result, fabrication costs would be greater for a stripline design, thus, less favored.

The dielectric integrated guides also have some disadvantages in fabricating circuits, as seen in Table 1. In this case, the greater effort required to fabricate the device makes it a less effective design, and more costly.

This leaves the microstrip and the fin line designs. Both are quite feasible for the design. The microstrip has certain advantages in that it has found widespread usage. It is very useful for integrating components (particularly in series) and interfacing with other devices, except rectangular waveguides. Since the attenuator must be integrated with a general rectangular waveguide this final point is important because a special transition will be needed with the microstrip type of lines. The fin line requires no special transition since it is mounted in a rectangular waveguide and the taper of the fin line provides the transition.

Bhat and Koul adequately summarize the advantages of the fin line for application in the 30 - 100 GHz frequency band:

1. *The dimensions of the circuit in the 30-100 GHz frequency band are compatible with beam-lead and chip devices, thus offering the potential for construction of passive and active integrated circuits;*
2. *The guide wavelength is longer than in a microstrip, thus permitting less stringent dimensional tolerances;*
3. *It permits easy transition to a standard rectangular waveguide, and operates over the entire bandwidth of the waveguide; and*
4. *Low loss propagation [13]."*

The work of others [14-21] also indicates that a fin line is a promising transmission line structure for the development of an attenuator.

The other transmission line structures displayed merit and conceivably an attenuator could be developed in them also.

In the assessment, two other proposals utilized other structures: rectangular waveguide [22] and coplanar waveguide [23]. As a fall-back position, either of these proposals or a microstrip design could be investigated further if some unforeseen difficulties arise in the fin line design.

### **Fin Line Structure**

Fin line can alternately be thought of as a slotline being placed in a rectangular waveguide or as a ridged rectangular waveguide with a thin dielectric film placed on the ridge. Structurally, the waveguide is split along the broad wall and the slotline is inserted into a groove in the guide. The waveguide is then reassembled to complete the mounting. Essentially the circuit elements can be fabricated using planar technology on the slotline. Inscription into the waveguide then provides direct compatibility with the mechanical structure of the waveguide and adds the shielding effect to the slotline. The fin line acts as an

E-plane transmission line. The basic fin line structures are shown in Fig. 2, where there are four variants: unilateral, bilateral, insulated and antipodal.

Each type of fin line has characteristics that make it more appropriate for a particular application. The insulated fin line has advantages over the others when active components must be biased [23]. The bilateral fin line provides greater values of  $Q$  than the other fin line structures, making it more suitable for filter applications [8]. Antipodal fin line can be used to achieve lower impedance than the others [2]. These characteristics also have to be considered in the final design, since each supports somewhat different propagation parameters. However, since this study is still in the initial stages, the unilateral fin line will be used for the initial design analysis. Assumptions will be made based on a housing structure similar to Fig. 3 proposed in Meier's paper [8].

### *Physical Considerations in Fin Line Application*

In addition to defining the transmission line structure, numerous other details must be defined in the final design. These include details such as the type of dielectric used for the fin line substrate. Considerations must be made regarding the mechanical and electrical properties of the dielectric as well as the thickness. The properties of the metallic fins also have physical and electrical significance. The dimensions of the slot and its orientation in the waveguide structure also affect the propagation characteristics. Since the fin line is to be integrated with other waveguide devices and transmission sections, it is necessary to ensure a good transition and to reduce reflections. These transitions must be considered in the design model. Since these considerations have not been implemented in the design model yet, the concerns they present will be discussed briefly. Further analysis of their effect will be presented in later reports.

#### **Dielectric**

Many different dielectrics can be used. In general, a dielectric should be chosen that has a low dielectric constant and low loss. The low loss feature is obvious; the other is less obvious. Permittivity should be low at millimeter wave frequencies to maintain the guide wavelength large enough to alleviate any design limitations resulting from the tolerances imposed by a small guide wavelength [16]. Both copper-clad RT-duroid™ 5880 ( $\epsilon_r = 2.22$ ) [14] and fused quartz [16] ( $\epsilon_r = 3.78$ ) have been applied at these frequencies. Both dielectrics have good electrical properties. The mechanical properties are much different. RT-duroid™ 5880 is a soft material which can be clamped easily in a waveguide fixture. Fused quartz is a rigid material, thus, mechanically greater tolerances must be observed when using quartz to prevent damage to the fin line when clamping [25]. Some researchers [26], however feel that a rigid material is better, since the softer dielectrics can be deformed by the mechanical mounting structure.

The effect of relative change in the dielectric constant and thickness is seen in Fig. 4 [27]. This figure indicates that increasing the dielectric constant reduces the normalized guide wavelength and decreases the characteristic impedance. Similarly, an increased thickness of the dielectric has the same effect. However, owing to the relative slope of the two sets of lines, changing the thickness does not affect design to the same degree.

#### **Fin Metalization**

Metalization is required to produce the fin pattern on the dielectric, producing the guided wave structure. As a result of the guide structure, electromagnetic field patterns possess the form shown in Fig. 5 [8].

Both copper and gold are used for the fins. Areas to consider in the selection of the metalization are conductor losses, conductor thickness, adhesiveness to the dielectric, and ease of bonding to components in the fin line.

Both copper and gold are good conductors, so their use implies the minimum allowable losses. Some care must be taken in the selection of the metal since not all metals adhere equally to all dielectric substrates. This concern becomes relevant when considering that a device will be bonded to the metal fin. As such, the type of bond should not require a difficult processing step. It should allow for a strong bond

with minimal likelihood of separating the fin from the substrate during bonding. The type of bonding performed may introduce additional capacitance or inductance into the attenuator. The preferred methods of bonding beam-lead diodes are thermal compression and parallel gap welding.

Thickness has the effect of changing the characteristic impedance as seen in Fig. 6 [29].  $Z_0$  decreases as the metal thickness increases. Thickness will also affect the bonding and adhesion of the metals, and this must be considered in the design.

### Geometric Orientation of Fin Line

In considering the geometric orientation, three quantities are discussed: slot width, asymmetric slot positioning in centrally located fin line, and asymmetric fin line positioning in the waveguide. Each area provides its own contribution to the characteristic impedance and normalized guide wavelength. The effect of each must be considered in a particular design and is not readily combinational. When combining these or any of the other parameters discussed, they should be considered within the framework of other design parameters.

*Slot Width* — Ultimately, the slot must not be smaller than the devices which must be mounted within the slot. The slot width can have a significant effect on both the characteristic impedance and the guide wavelength. In Fig. 7 [30] the relationship of guide wavelength and characteristic impedance is displayed. The characteristic impedance varies only slightly over the W-band frequency range for a particular slot width. Decreasing the width reduces the characteristic impedance. Similarly, the guide wavelength decreases with reduced slot sizes and with increased frequency.

*Slot Displacement For Centered Unilateral Fin Line* — In this case, the fin line is still positioned in the center of the rectangular waveguide. The slot is displaced off center. Figure 8 [31] displays the effect when varying the slot position at a lower frequency (34 GHz), but the effect should be similar for a fin line in WR-10. In this figure the effect of the displacement is symmetric so  $S$  is simply the deviation from the centered slot. Increasing the displacement has the effect of increasing the characteristic impedance. The guide wavelength first increases and then decreases as the slot is displaced from the center. As illustrated in this graph, displacement from the center is not necessarily desirable.

*Displacement Of Fin Line In The Waveguide* — Normally the fin line would be centered in the waveguide. This analysis considers displacement in both directions. Two cases are presented. The first moves the fins closer to the waveguide wall and the dielectric further away. The second moves the fins off center in the opposite direction. Figure 9 [32] displays the first case and Fig. 10 [33] the second case. Both cases are illustrated for narrow slot widths at WR-28. Both cases display similar characteristics; this results from the electric fields being closely contained across the slot [30], as is indicated in Fig. 5.

Note that analysis of geometric orientation effects only becomes necessary if a slight deviation from the centered unilateral fin line will greatly enhance the design. Otherwise, one would restrict the analysis to the symmetric fin line structure.

*Waveguide To Fin Line Transition* — The characteristic impedance of the fin line is anticipated to be larger than the characteristic impedance of the WR-10 waveguide. As such, a transition structure must be used to reduce reflections. In general, the width of the slot increases over some distance to the full width of the waveguide, forming a taper. At this point there is a discontinuity in the dielectric at the point where the fin line ends. The discontinuity of the dielectric is minimized by introducing one or two quarter-wave transformer sections [33]. Figure 11 illustrates the waveguide to fin line transition, displaying both the taper and the quarter-wave transformer [33].

*Taper Transition* — Bhat and Koul [34] discuss detailed analytical methods for designing the taper, but indicate that often the design resulting from this analysis is not easily realizable in an actual device. Furthermore, experimentally, the taper does not require critical dimensional tolerances. As such, they present an empirical method using a circular arc taper. The circular taper is shown in Fig. 12 [35]. A comparison of the empirical circular taper is made with the analytical solutions developed for the taper; these are shown in Fig. 13 [36]. As can readily be seen, the empirical solution compares well with the solutions derived from the various theoretical impedance structures.

*Dielectric Transition* — A transition is required for the dielectric because propagation of the wave is transforming from air fill rectangular waveguide to a fin line which is printed on a dielectric material. Practically, the loss should be small, but designers have attempted to reduce the reflection loss further by using one or two quarter-wave step transformers. Improvements on the order of 5 dB have been made over an entire band with a single quarter-wave transformer [5]. Two quarter-wave transformer steps are intended to provide matching over a broader bandwidth [38]. Examples of the single step and double step quarter-wave transformers are shown in Figs. 14 and 15, respectively.

#### *Summary of Physical Characteristics Analysis*

The previous analysis points out that several conditions must be considered as a model progresses to a stage where fabrication can begin. The point of the analysis is to reduce time and material costs inherent to fabricating working devices.

As a starting point, the model to this point conforms to normal features found for fin line designs. It uses a unilateral, symmetric, centered thin-slot fin line. It uses a quartz dielectric as the fin line substrate and either gold or copper for the metalization. Some form of taper, probably circular arc, is assumed for the fin line transition. A quarter-wave transformer in the dielectric is also assumed. All of these features have been modeled [41], except the transitions, that will be considered as modeling progresses. The model for the attenuator — the fin line incorporated with the PIN diode — will be presented in the sections following the presentation of the PIN diode characteristics.

#### **Pin Diode Characteristics**

While both PIN diodes and FETs have been cited as being viable candidates for an attenuating element [2], only the PIN diodes will be discussed for the present design. This choice is based upon the numerous references [14-20] that work with PIN diode at W-band frequencies for control applications. The parasitics resulting from FETs generally make them unsuitable for this frequency band. This is viewed as adequate cause to discuss PIN diodes alone in reference to the attenuator design. The final design will borrow from the previous work performed on W-band attenuators.

Two areas will be discussed in this section. First, the physical mechanism of the PIN diode will be briefly introduced. Second, the implementation of the PIN diode as a circuit element will be presented.

#### *Pin Diode Physical Characteristics*

The PIN diode is composed of an intrinsic layer (undoped) between two doped regions, one p- and one n- doped. An example of the diode is shown in Fig. 16 and its doping profile is seen in Fig. 17. Due to the large intrinsic area, the device capacitance is very low. This makes it insensitive to changes in reverse bias. In the reverse bias mode the breakdown voltage is very large, but in the forward bias mode the resistance becomes quite small,  $\sim 1 \Omega$  [42].

The resistivity of the intrinsic layer is large ( $1000 \Omega\text{-CM}$ ) and is usually slightly doped with p- or n-type material. Thus it is  $\pi$ -type or n-type, respectively. Assuming a  $\pi$ -type layer, during forward biasing conditions carriers are injected from both regions into the  $\pi$ -layer. The carrier concentration decreases with depth in the  $\pi$ -layer due to recombination. If the carrier lifetime (the period before recombination) is large and the  $\pi$ -layer is not too thick, then the  $\pi$ -layer will become filled with carriers and its resistivity will become small. As a result, the effect of low diode resistance occurs for forward bias. For this to happen the carrier lifetimes in the  $\pi$ -layer must be greater than the period of the operating frequency. As a result, PIN diodes are good high frequency devices and poor low frequency devices [1]. The I-V characteristics of the PIN diode are displayed in Fig. 18 [43].

### *Pin Diode Circuit Characteristics*

An equivalent circuit for the PIN diode is shown in Fig. 19 [43]. These models can be used in the analysis of the circuit using the fin line transmission structure.

### **Pin Diode Attenuator**

Having described the fin line transmission structure and the PIN diode, the basic elements of the attenuator can now be incorporated into a full model. In this model many things must still be determined, such as: series or short orientation of diodes, reverse/forward bias operational characteristics, physical reality of design considering diode characteristics, number of diodes, and diode placement. The following sections summarize this analysis. Analysis details are provided in the Appendix.

### *Circuit Configuration*

PIN diodes may be either series mounted as in Fig. 20.a or shunt mounted as in Fig. 20.b. In the series mounting case the attenuation occurs when the diode is forward biased and is a result of the parallel resonance of the short-circuited stub and the PIN diode's inductance. When reverse biased, the loading is provided by the diode capacitance; low attenuation results. For the shunt configuration, when the diode is reverse biased the shunt impedance is high and little attenuation occurs. By forward biasing the diode, this nearly shorts the transmission line, resulting in attenuation [15,18,19]. The effect is different in each case. For the series configuration, the Q that results from the parallel resonance in the forward bias mode severely limits the bandwidth, as seen in Fig. 21 [15]. The shunt diode placement yields broad band performance, as shown in Fig. 22 [15]. Note that in both cases the insertion loss achieved in the respective non-attenuating states is approximately 2.0 dB.

Gupta points out a third possible configuration, a pi- network, as shown in Fig. 23 [45]. The advantage of this layout is improved matching capability. The resistance values of the diodes can be accurately controlled to provide a match to the transmission line. An implementation of this circuit configuration has not yet been found in the literature. This could be an additional area of modeling investigation. The work performed to date has concentrated on the parallel configuration.

### *Effects of Different Biasing States*

Two primary objectives of the design exist. One is to minimize the insertion loss when the diode is unbiased or reverse biased. The second is to maximize the achievable attenuation while considering the requirement that attenuation variations should be small across the band.

In the reverse bias case, with a single diode, the only control available in evaluating the insertion loss is in the lead inductance. The capacitive effects result from junction and packaging capacitance that cannot be altered when designing components, unless a special batch of diodes is fabricated for the application. This was generally unfeasible because of cost constraints. Thus, an analysis was performed to evaluate the effect of lead inductance on the insertion loss. A capacitance of 0.02 pF was assumed. This was compatible with the specifications of practical devices, reference M/A-COM specification sheet [43]. For the model a quartz substrate was used, and a slot width of 5 mils applied. The size of the diode was on the order of the slot width. The desire to minimize the slot width results from the desire to reduce the characteristic impedance to achieve a large bandwidth. For the analysis, this model varied the lead inductance between 0 and 0.1 nH. Even with zero lead inductance, a 1.5 dB insertion loss at 75 GHz resulted from line loading. This increased to 3.5 dB at 110 GHz. The insertion loss was found to increase with lead inductance. This was because the net shunt reactance increased the mismatch, producing the insertion loss. The increased lead inductance caused a resonance to occur at ~ 112 GHz for the 0.1 nH inductance. As such, a minimum lead inductance of 0.02 nH was applied to all subsequent modeling. This value accounts for the likelihood of inductances being present in any practical design [41].

In the forward bias case, modeling revealed that high values of attenuation could not be achieved with a single diode [41]. This was confirmed in the literature [46]. As pointed out, to reduce reflections additional diodes are required to supply matching [1].

## *Multiple Diodes*

As previous analysis suggests, multiple diodes are required to increase attenuation and to improve matching characteristics. The following sections consider the effects of multiple diodes in forward and reverse bias configurations.

### **Reverse-bias Multiple-diode Analysis**

The models analyzed in this section consist of 2, 3 and 4 diodes in shunt configurations. The indicated fin line structure was used. Two types of modeling were performed; one minimized the reflection coefficient and the other maximized the transmission coefficient. All modeling and analysis are performed using the Hewlett-Packard Microwave Design Software (MDS) package [41].

The models produced similar results except that in some cases the maximized transmission loss model produced physically unrealizable results. This will be discussed in a later section on diode spacing.

In summary, the insertion loss did not exceed 2.3 dB for any number of diodes considered. A greater concern that arose from this analysis was that matching could not be achieved over the entire band for the diode combinations considered. Matching was achieved for roughly one quarter of the band with the 2- and 4-diode models and one tenth of the band with the 3- diode model [41, 47].

### **Forward-bias Multiple-diode Analysis**

This analysis was made using the optimized spacing parameters resulting from the reverse bias model. The significant result was that when compared at the same diode bias, a 4-diode configuration provides greater attenuation (~16.2 - 17.0 dB over the band) than a 2- or 3-diode configuration (7.1 - 7.9 dB and 12.0 - 12.8 dB respectively) [41, 47].

## *Diode Spacing*

The literature indicates that multiple diodes in a fin line should be placed with quarter wavelength spacing [8,14,16, 46]. Models developed in this analysis use several different criteria: minimization of the reflection coefficient, maximization of the transmission coefficient and optimization of matching in the forward bias state. Symmetric diode positioning was imposed on the design. The results of each form of spacing are discussed.

### **Minimized Reflection Coefficient Spacing - Reverse Bias**

Results for these analysis criteria indicated an optimal spacing of 57.2 mils. This required a center-to-center diode spacing of > 20 mils, which is a physically realizable situation. Increasing the spacing has the effect of reducing the bandwidth of the device [41].

In the reverse bias mode, insertion losses of 1.3 dB (2 diode), 2.3 dB (3 diode) and 2.1 dB (4 diode) were obtained [41].

In the forward bias mode, for this model, the attenuation yielded was ~ 4.0 dB less than an equivalent optimization for forward bias [41].

### **Maximized Transmission Coefficient - Reverse Bias**

As noted in the section on multiple diodes, this form of optimization yielded spacings similar to those obtained from the maximized reflection coefficient optimization except for the 3-diode case. This was a design model that required diode spacings smaller than the customary size of PIN diodes. As a result, this model was discarded from further analysis [41].

## Forward Bias Spacing Optimization

This form of optimization was found using the sum of the magnitude of both port reflection coefficients ( $|S_{11}| + |S_{22}|$ ). This tactic was used to ensure symmetry in the spacing and to ensure an equally good impedance match at both ports. This second requirement arose from the requirement for equal bi-directional attenuation [41].

This model yielded improved flatness in insertion loss and return loss. Additionally, the impedance match provided was better. As noted earlier, an increase of  $\sim 4.0$  dB was indicated for all multiple diode cases using the forward bias diode spacing [41].

## SUMMARY OF THE MODELING ANALYSIS

The analysis of the diode spacing indicated several important points. First, the spacing of the diodes must be close to achieve reduced insertion losses. Increasing the spacing greatly reduces the bandwidth. It is still questionable whether quarter-wave spacing has advantages, since this was not rigorously considered. It does appear that irrespective of the form of spacing optimization used, the actual spacing will require close diode positioning. Second, the forward bias spacing optimization has the effect of improving flatness. Finally, the spacing resulting from the forward bias optimization produced a larger maximum attenuation than other methods. While the performance suggested by the forward bias spacing optimization was promising, the actual analysis did not explicitly reconsider the reverse bias situation after achieving the forward bias performance. Further analysis should consider both the quarter-wave spacing effect and the effect of the forward bias optimization on reverse bias conditions.

The modeling analysis presented several other important considerations. First, efforts should be sought to minimize lead inductance in prototype devices. The effect of lead inductance may limit the actual number of diodes that can be used to achieve the attenuation specification. Measures to reduce lead inductance should be employed. This includes minimizing the slot width to roughly the size of the diode, and using bonding techniques to enhance the ability to make nondestructive bonds as close to the diode body as possible.

Both forward and reverse bias characteristics of the diodes must be considered in the design. The analysis indicates that achieving active attenuation characteristics by forward biasing the diodes is easier than achieving low losses in the "non-attenuating" reverse bias state. This assertion results from the characteristics displayed for insertion loss and transmission line matching.

Multiple-diode configuration modeling suggests that they may better reduce reflections than the single diode configuration. This assertion is supported by Gupta's recommendation [1] for a pi-network. It is also suggested in the work of others [46] that the use of different diode biases for multiple-diode configurations can be used to enhance the matching. With regard to matching, some authors [46] suggest the use of a bilateral fin line to enhance the ability to perform matching by bias control. As noted earlier, the bilateral fin line provides other possible advantages: reduced characteristic impedance and increased single mode bandwidth.

In addition, consideration of other parameters in modeling may also enhance the characteristics of the attenuator. Areas to consider should be: reducing the dielectric constant, reducing the dielectric thickness or narrowing the slot width.

Matching of the attenuator can possibly be accounted for in the fin line-to-waveguide transition. Two areas of analysis should be considered further in this regard: fin taper and dielectric step transformer. While important, it is unlikely that consideration of these parameters will yield a match over the full band.

Further efforts on this project will improve and refine the modeling analysis of the fin line PIN diode attenuator. When a suitable design has been developed, fabrication of the device will be performed.

A final observation refers back to the first pages of this report. This observation considered transmission line structures for this effort, and chose fin line because of advantages it had in fabrication

and loss characteristics at W-band. As is shown by the modeling analysis, this selection is justified. However, considering potential conflicts in component spacing, it appears that while fin line is entirely proper to use for a W-band application, extension of the fin line to substantially higher frequencies could meet some of the same difficulties that other transmission lines experience at W-band. This has the effect of substantiating the information contained in Fig. 1.

## FINAL CONSIDERATIONS

The goal of this analysis was to achieve a practical device for W-band measurement and calibration applications. This device has the requirement of being electronically controllable. This report would be incomplete if it did not at least consider the availability of suitable PIN diodes to achieve the design. At least three suitable PIN diodes have been found with characteristics that would make it suitable for use in the resulting design. The models are M/A-COM MA4P800, Alpha Industries, Inc. DSG6405, and Hewlett-Packard HPND-4005. Each of these diode modes had the appropriate capacitance.

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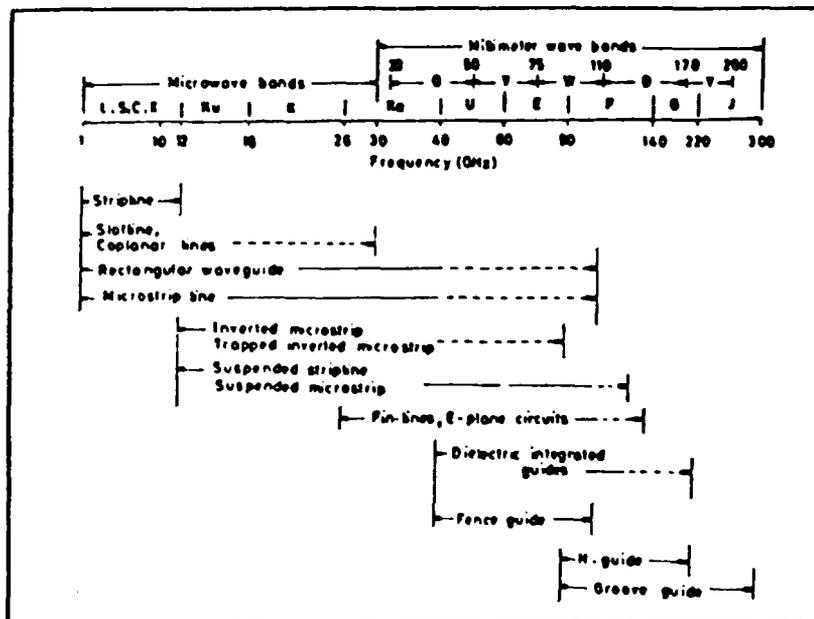


Fig. 1 — Useful operating ranges of various transmission lines for microwave and millimeter wave circuits [4]

Characteristic	Coax [5]	Waveguide Rectangular [5]	Strip-line [5]	Micro-strip [5]	Ridged Waveguide [5]	Dielectric Guide [5]	Slot Line	Coplanar Waveguide	Covered Micro-Strip [5]	Fin Line
Transmission Loss	Medium	Low	High	High	Low	Low	Low [11]	Medium [11]	High [6]	Low [8]
Radiation Loss	None	None	None	Medium	None	High	High	Medium [11]	None	Low [8]
Dispersion	None	Medium	None	Low	Medium	High [12]	Medium [7]	Medium [10]	Low [5]	Medium
Bandwidth	High	Low	High	High	Medium	Low	High [9]	High	High [5]	High [8]
Bonding Solid State Devices	Medium	Medium	Easy	Easy	Hard	Medium	Easy [6]	Easy [6]	Easy [6]	Easy [8]
Integration	Hard	Hard	Fair	Easy	Hard	Easy	Easy [6]	Easy [6]	Easy [6]	Easy [8]
Power Handling	Medium	High	Low	Low	Medium	High	Low [5]	Low [5]	Low [5]	Low [5]
Fabrication	Medium	Medium	Easy	Easy	Hard	Easy	Easy [6]	Easy [6]	Easy [6]	Easy [8]

Table 1 - Qualitative comparison of various transmission lines

Configuration	Typical impedance range (ohms)	Unloaded Q-factor ( $Q_U$ )	Radiation loss	Dispersion	Other features
Stripline	20-120	high (500)	none	negligible	Excellent for passive components, inconvenient for incorporation of chip devices
Microstrip line Slotline	20-100 50-200	medium (250) low (100)	low high	small large	Widely used in MICs and MMICs Suitable for shunt mounting of chip devices and fabrication of nonreciprocal ferrite components
Suspended stripline	40-150	high	none	small	Suitable for high-Q passive components; operation can be extended to millimeter wave frequencies
Suspended microstrip	40-150	high	low	small	Useful at higher microwave and millimeter wave frequencies
Inverted microstrip	25-130	high	low	small	Suitable for high-Q passive components, inconvenient for mounting active devices
Coplanar Waveguide	40-150	low	medium	medium	Easy connection of series and shunt elements, useful for MMICs and nonreciprocal ferrite components
Coplanar strips	40-250	low	medium	medium	Easy connection of series and shunt elements, useful for MMICs

Table 2 - Qualitative comparison of various planar transmission lines [4]

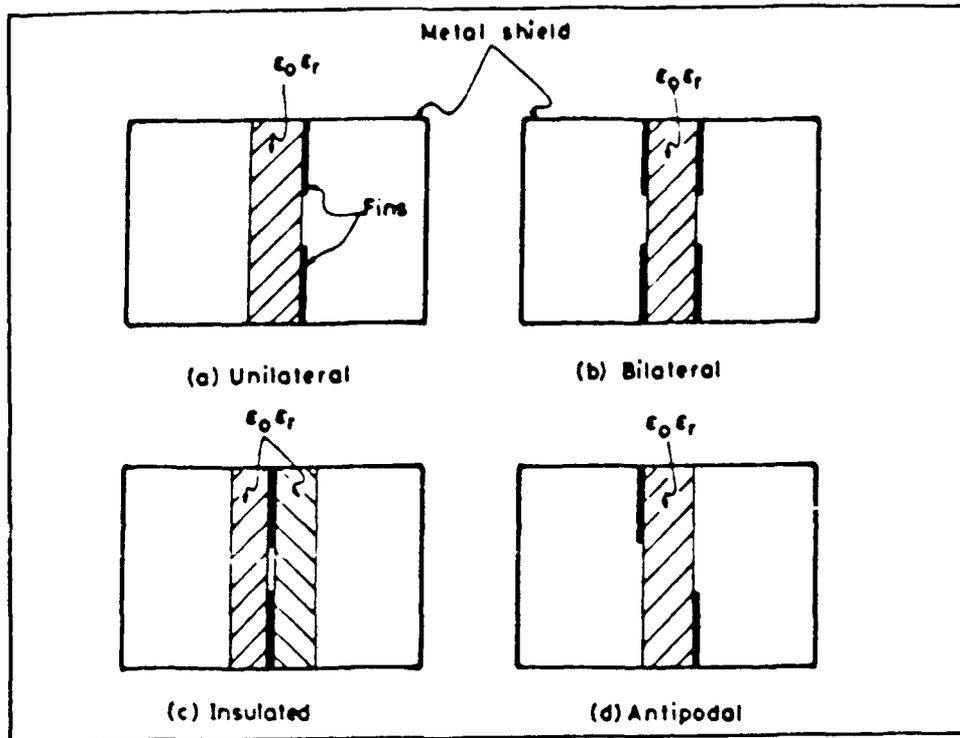


Fig. 2 — Basic fin line structures [10]

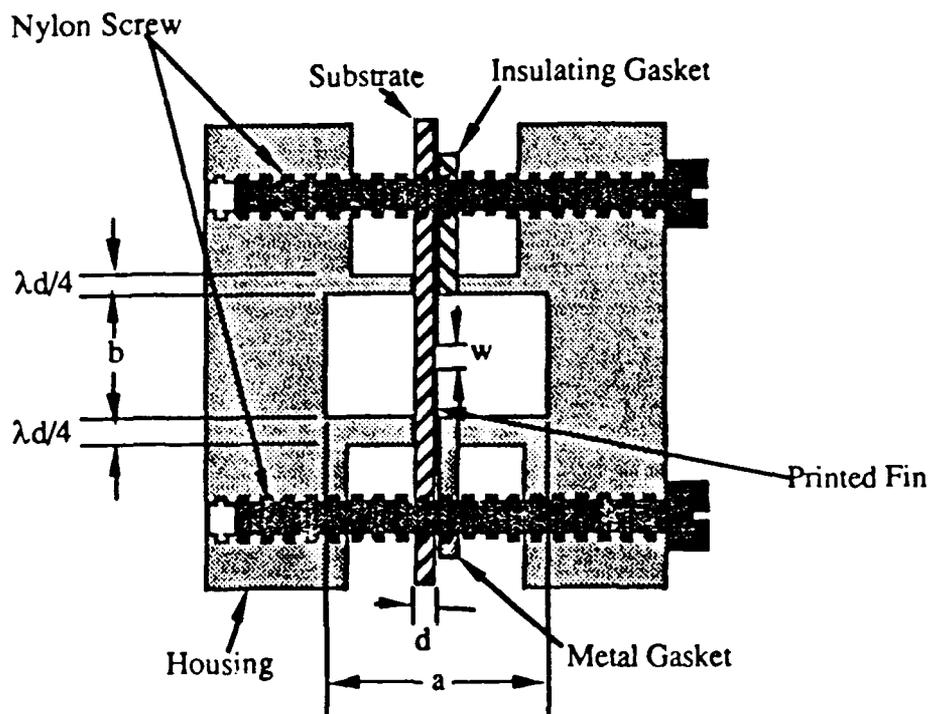


Fig. 3 — Fin line housing proposed by Meier [8]

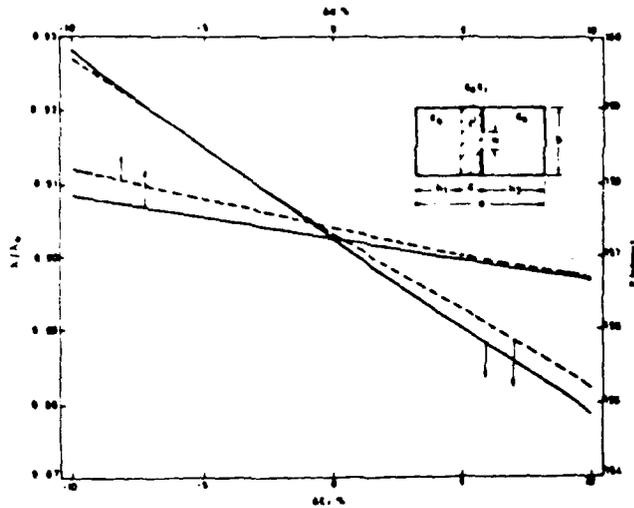


Fig. 4 — Normalized guide wavelength  $\lambda/\lambda_0$  and characteristic impedance  $Z$  versus percentage change in substrate thickness  $d$  and dielectric constant  $\epsilon_r$ .

$\epsilon_r = 2.22$      $d = 0.254$  mm  
 $w = 0.2$  mm     $h_2 = h_1 + d$   
 frequency = 34 GHz    wavelength = WR-28  
 $\lambda/\lambda_0$  ————  $Z$  ———— [27]

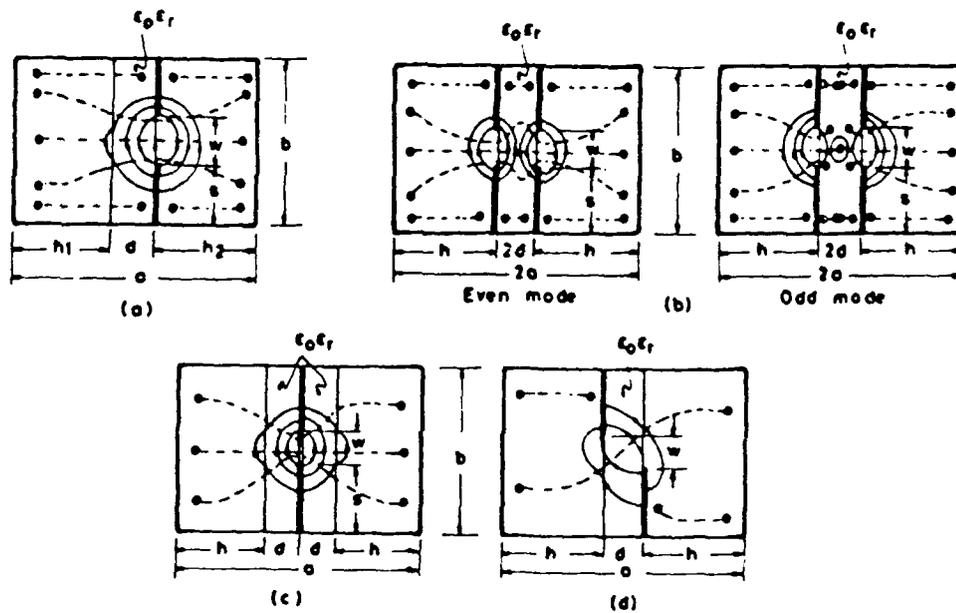


Fig. 5 — Typical field lines for basic fin line structures

(E — H —)

- (a) unilateral fin line
- (b) bilateral fin line
- (c) insulated fin line
- (d) antipodal fin line

[27]

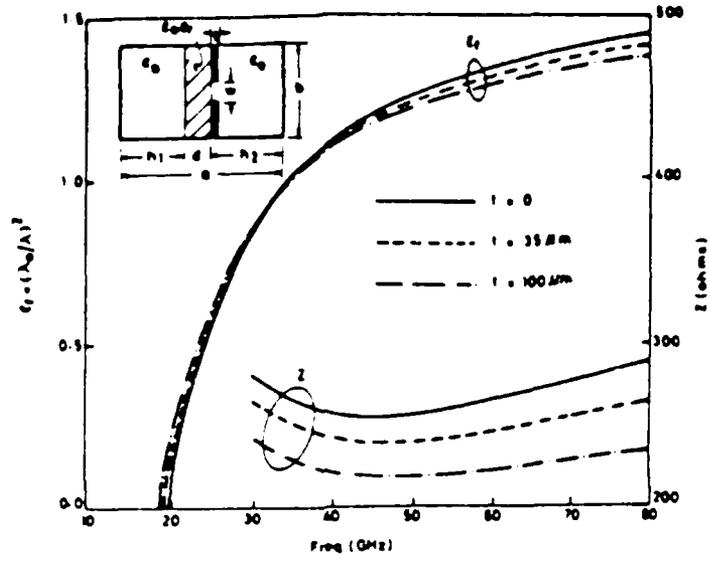


Fig 6 - Effect of finite metalization on the propagation characteristics of unilateral fin line

$\epsilon_r = 3.8$        $h_1 = 0.089$  in  
 $d = 0.005$  in       $h_2 = 0.094$  in  
 $b = 0.094$  in       $w/b = 0.2$       [29]

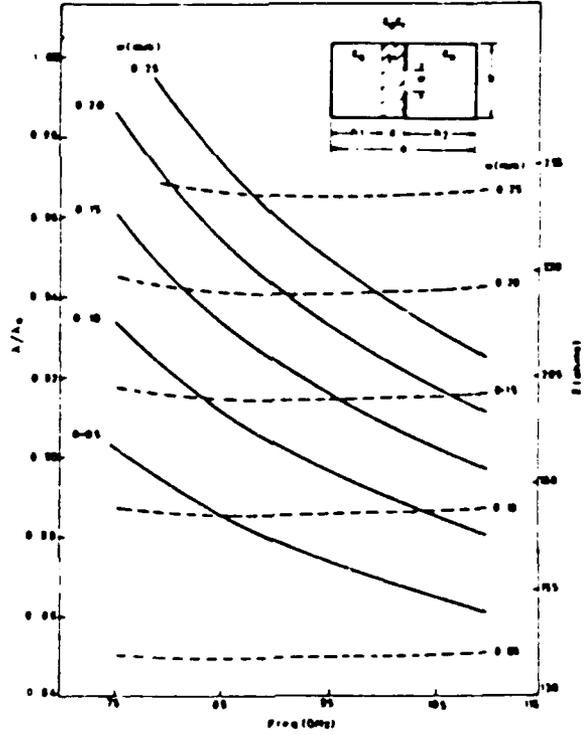


Fig. 7 - Normalized guide wavelength  $\lambda/\lambda_0$  and characteristic impedance

Z versus frequency of unilateral fin line:

$\epsilon_r = 2.22$        $d = 0.127$  mm  
 $h_1 = 1.143$  mm       $h_2 = 1.27$  mm  
 wavelength = WR-10

$\lambda/\lambda_0$  ——— Z - - - [30]

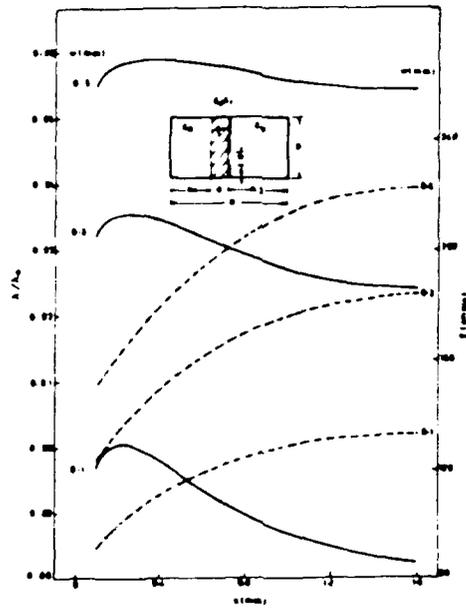


Fig. 8 — Effect of displacing the slot on the normalized guide wavelength  $\lambda/\lambda_0$  and characteristic impedance  $Z$ :

$\epsilon_r = 2.22$                        $d = 0.254$  mm  
 $h_1 = 3.302$  mm                 $h_2 = 3.556$  mm  
 frequency = 34 GHz        waveguide = WR-28  
 $\lambda/\lambda_0$  —————         $Z$  - - - - -

(31)

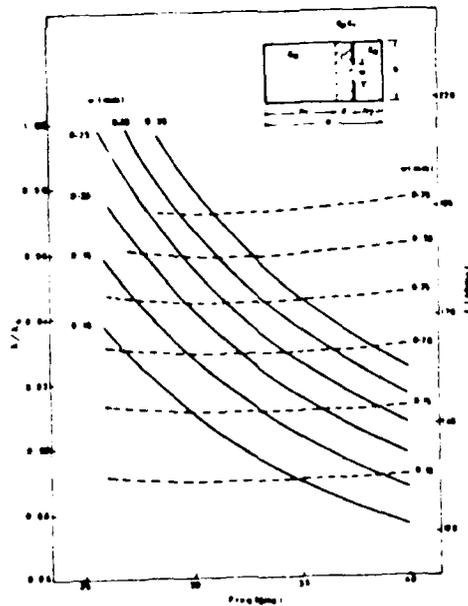


Fig. 9 — Normalized guide wavelength  $\lambda/\lambda_0$  and characteristic impedance  $Z$  versus frequency of unilateral fin line with laterally displaced dielectric substrate:

$\epsilon_r = 2.22$                        $d = 0.254$  mm  
 $h_1 = 5.08$  mm                 $h_2 = 1.778$  mm  
 waveguide = WR-28  
 $\lambda/\lambda_0$  —————         $Z$  - - - - -

(32)

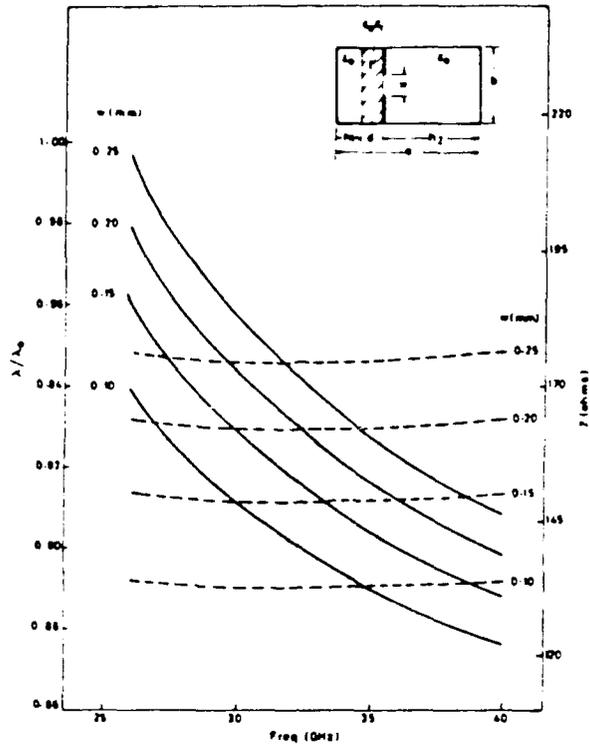


Fig. 10 — Normalized guide wavelength  $\lambda/\lambda_0$  and characteristic impedance  $Z$  versus frequency of unilateral fin line with laterally displaced dielectric substrate:

$\epsilon_r = 2.22$        $d = 0.254$  mm  
 $h_1 = 1.524$  mm     $h_2 = 5.334$  mm  
 waveguide = WR-28  
 $\lambda/\lambda_0$  ————       $Z$  - - - - -

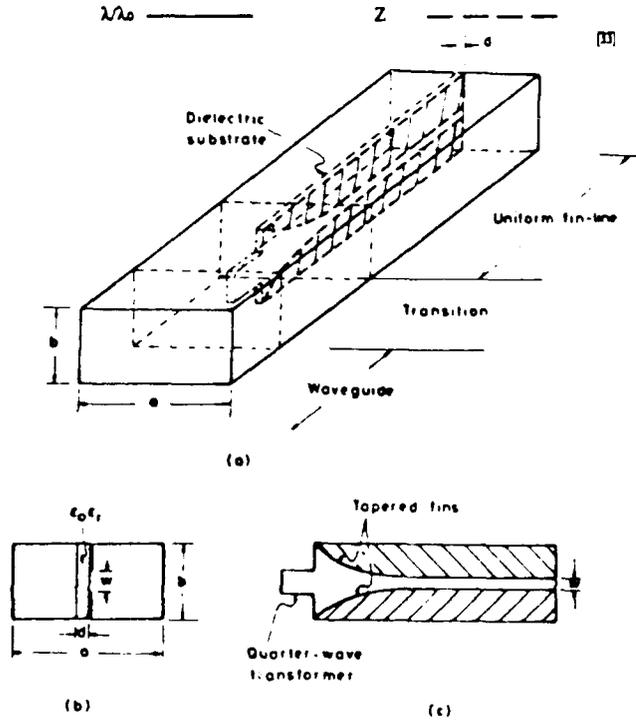
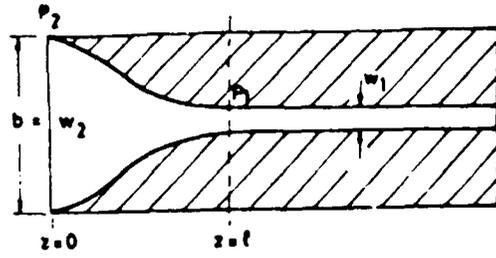
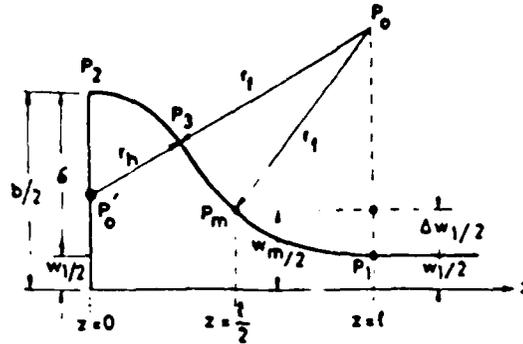


Fig. 11 — Schematic representation of fin line displaying taper and quarter-wave transformer characteristics [33]



(a)



(b)

Fig. 12 — (a) Circular arc taper (b) Geometrical parameters for drawing circular arcs [35]

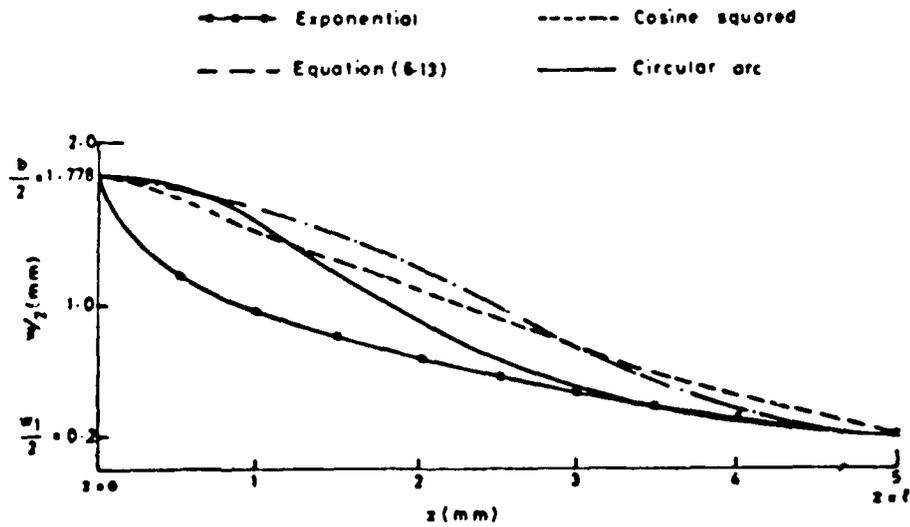
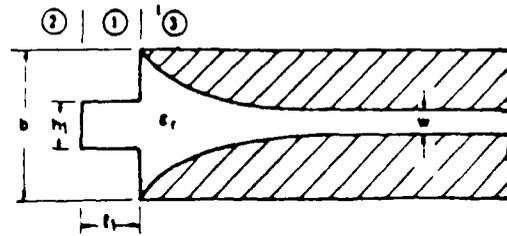
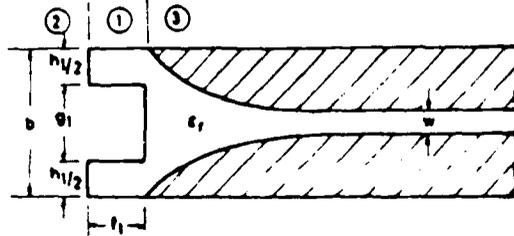


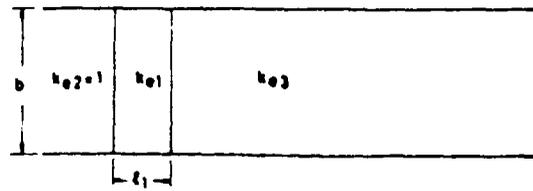
Fig. 13 — Comparison between various taper contours for an example at 34 GHz [36]



(a)

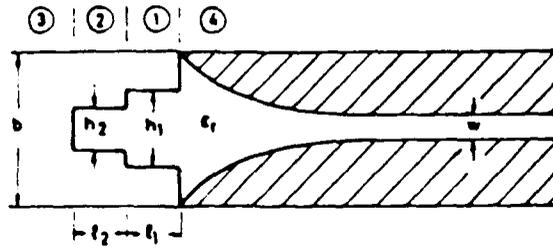


(b)

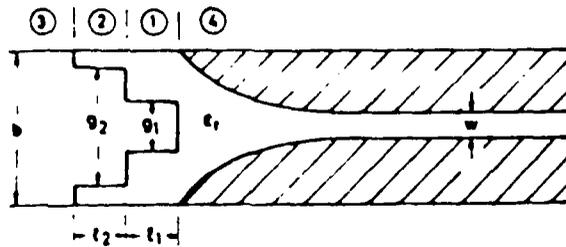


(c)

Fig. 14 — (a) Single-section quarter-wave transformer using protrusions, (b) single-section quarter-wave transformer using notches, (c) equivalent homogeneous waveguide model [39]



(a)



(b)

Fig. 15 — Two-section quarter-wave transformer using: (a) step protrusions and (b) step notches [39]

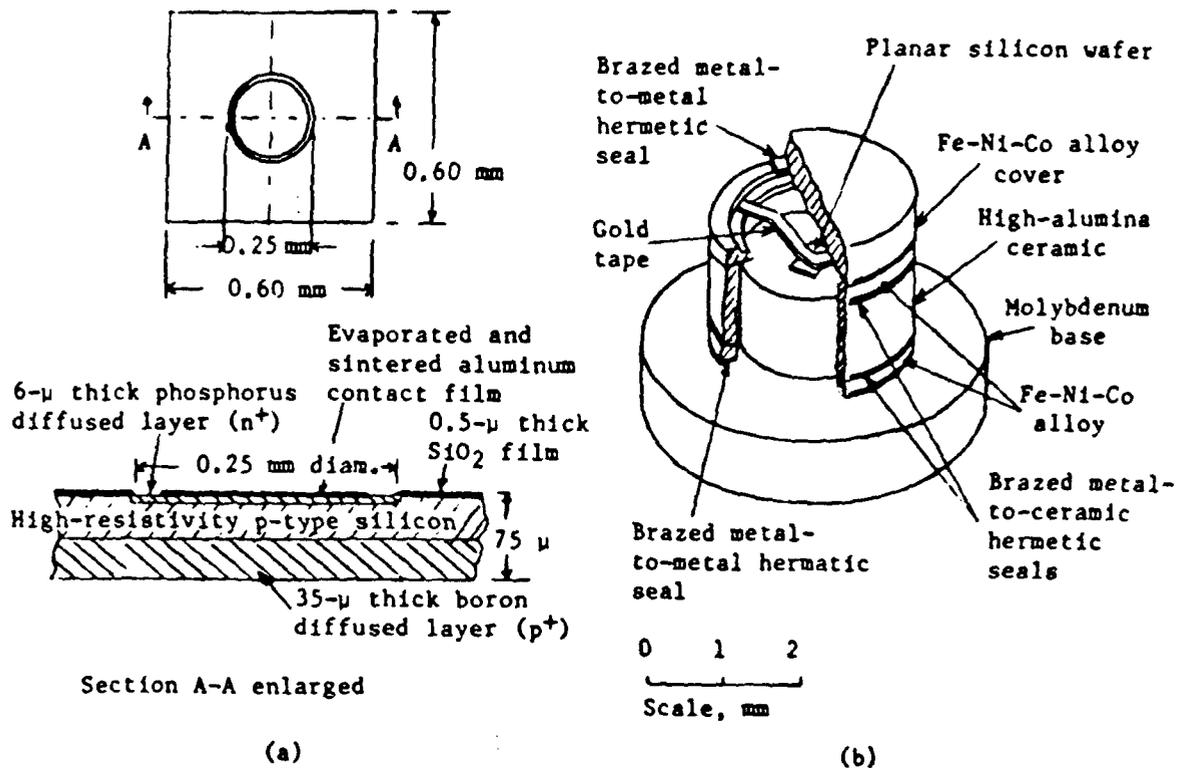


Fig. 16 — Typical planar PIN diode[42]

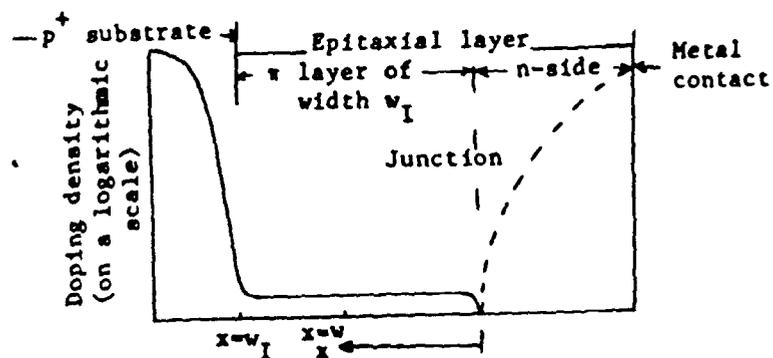


Fig. 17 — Typical doping profile for a  $p^+p-n^+$  diode [42]

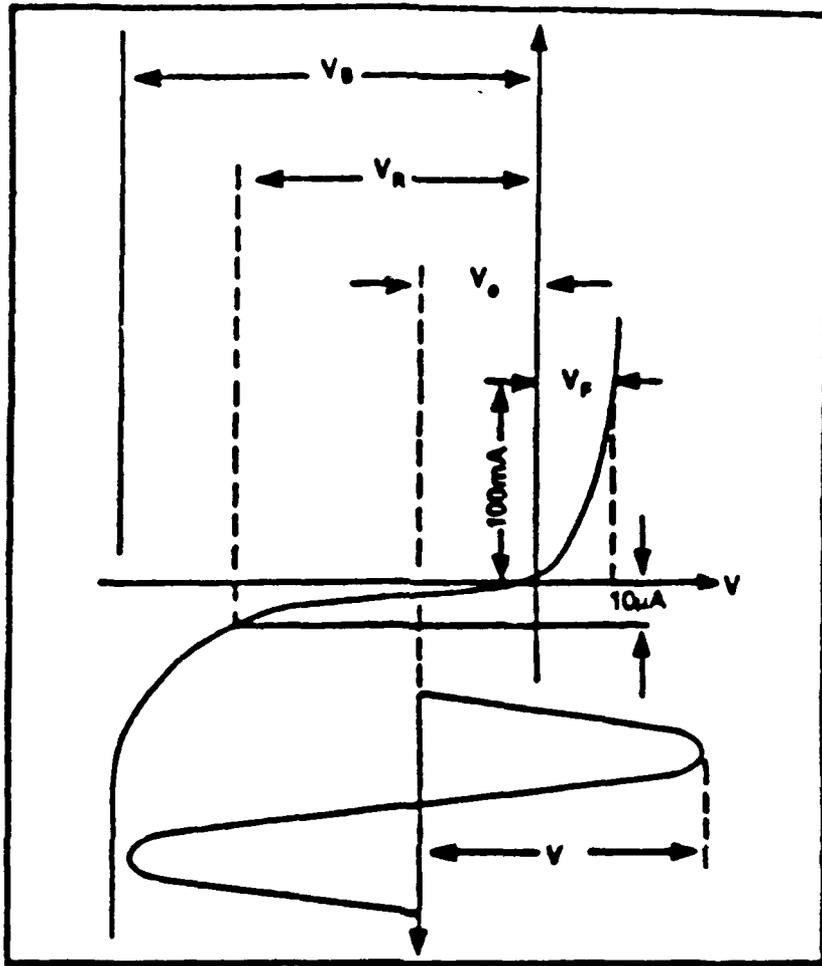


Fig. 18 — PIN diode I-V characteristics [43]

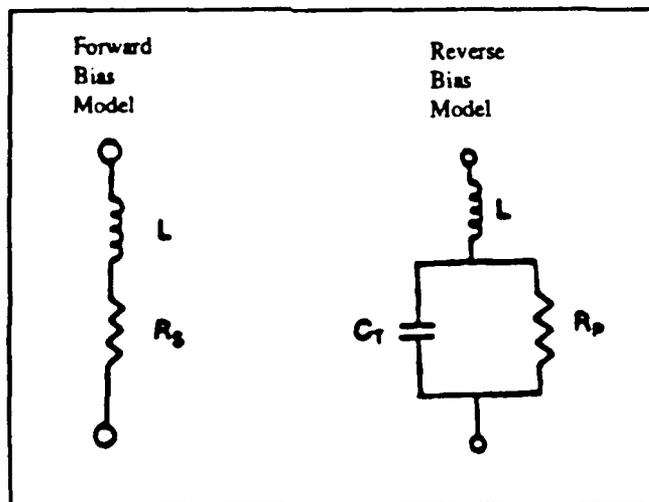


Fig. 19— RF Electrical Models of PIN Diode [43]

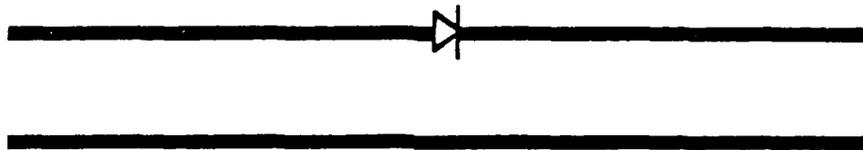


Fig. 20.a — Series mounted diode attenuator configuration

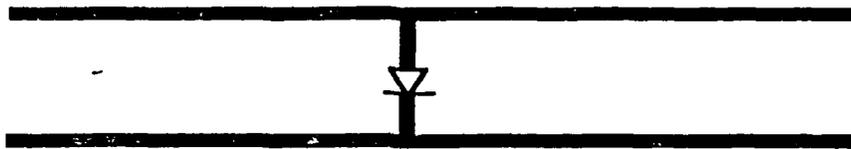


Fig. 20.b — Parallel mounted diode attenuator configuration

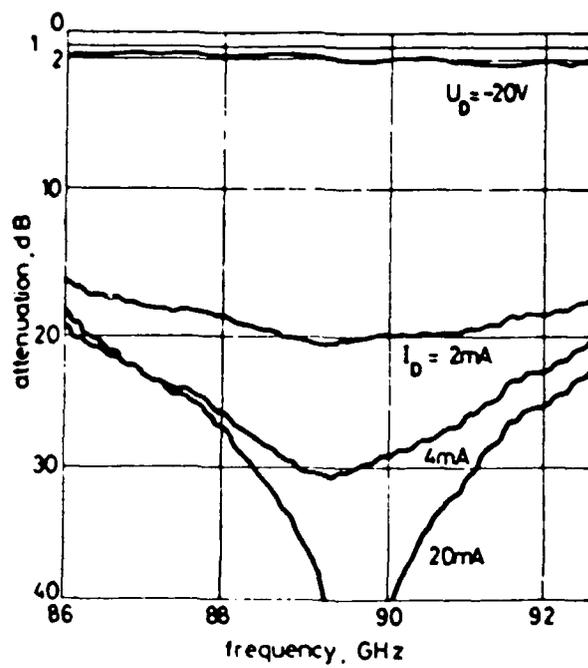


Fig. 21 - Transmission behavior of W-band series type PIN attenuator (Series Configuration) [18]

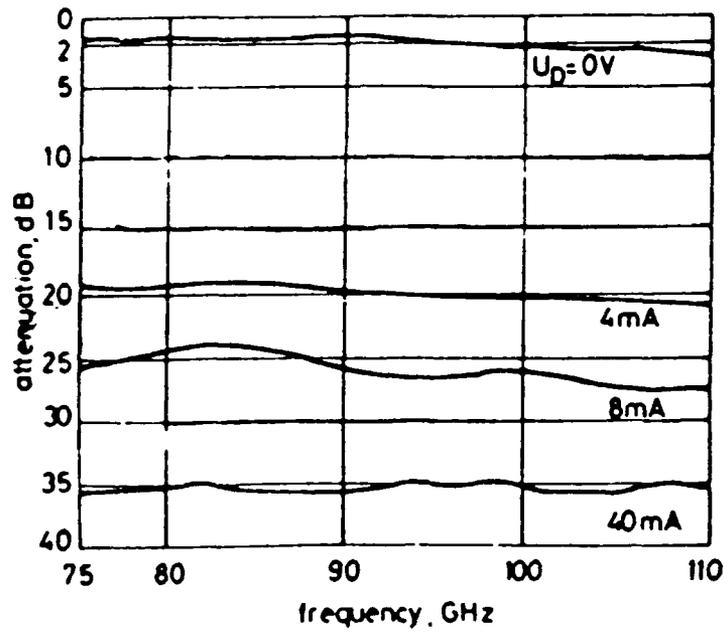


Fig. 22 - Transmission behavior of W-band parallel type PIN attenuator (Shunt Configuration) [18]

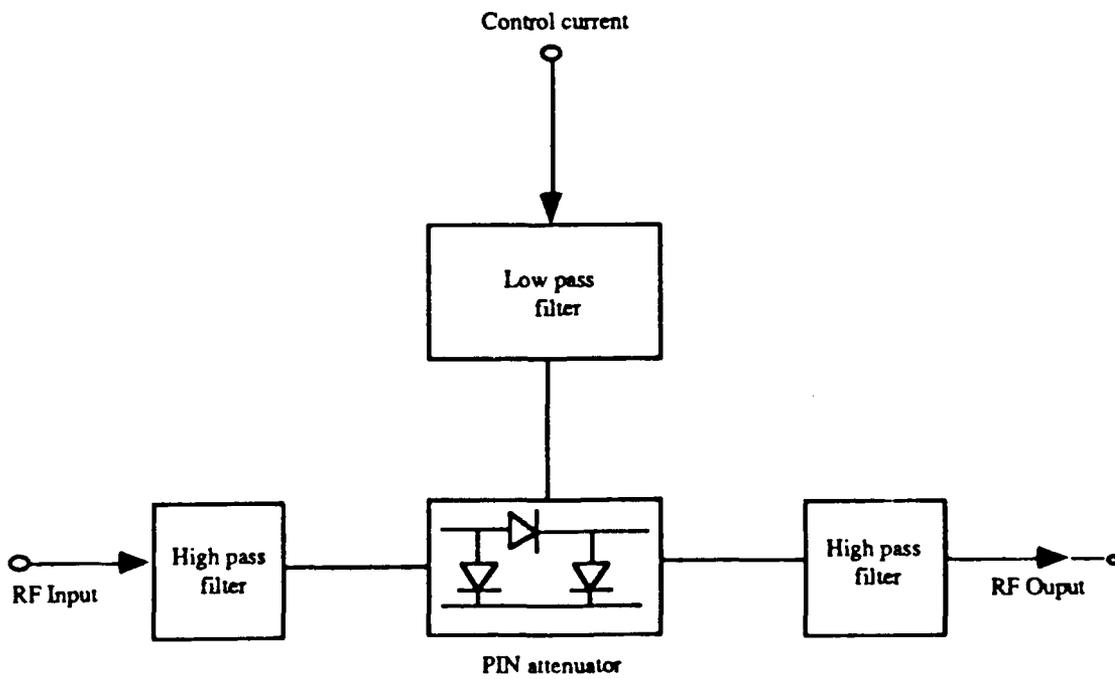


Fig. 23 — Circuit diagram for pi-network

## **APPENDIX**

### **CAD ANALYSIS OF A WR-10 FIN LINE VARIABLE ATTENUATOR**

## SECTION 1 INTRODUCTION

This report is a summary of the work that has been performed at NIST on the Coaxial Step Attenuator Check Standards project (CCG #197a). This report focuses on an attenuator structure, consisting of various combinations of PIN diodes connected in shunt across a unilateral fin line structure. Various aspects of the fin line attenuator are dealt with in sections 2,3,4, and 5. Section 2 deals with the geometry of the unilateral fin line structure, along with a brief explanation of its operation. The models for the forward and reverse biased diodes are also presented. In section 3, the Hewlett-Packard Microwave Design Software (MDS) is used to model the effects of lead inductance on the characteristics of an attenuator structure with one PIN diode in the zero or reverse biased case. Then, in section 4, optimized results are given for 1,2,3, and 4 diode clusters. In section 5, the attenuator characteristics are presented for forward biased diodes with a current of  $I=40 \mu\text{A}$ . Optimized results are displayed for 2,3, and 4 diode clusters. In addition to the  $40 \mu\text{A}$  results, the attenuator characteristics for a three diode attenuator are examined for bias currents greater than and less than  $40 \mu\text{A}$  in order to see if optimizing at  $40 \mu\text{A}$  can result in good characteristics at other bias levels. Section 6 deals with the simulation of a 300 mil long linear taper by means of a stepped series of short transmission lines. In section 7 conclusions and recommendations, which are based on the MDS analyses, are given.

## SECTION 2-FIN LINE ATTENUATOR GEOMETRY AND PIN DIODE MODELS

Fig. 1 depicts the geometry of the unilateral fin line structure which is the basis of the variable attenuator. The unilateral fin line consists of a rectangular waveguide section containing a longitudinally-mounted dielectric substrate material with a relative dielectric constant  $\epsilon_r$ . As an inspection of Fig. 1 indicates, two metalized fins are bonded symmetrically to the same side of a substrate material with a small gap in between. In order to provide efficient coupling between the rectangular waveguide sections and the fin line sections, gradual tapers are provided at each end of the fin line structure. As is indicated in Fig. 1, the length of the tapered sections are denoted by  $L_{\text{taper}}$ . The presence of gradual tapers between the fin line section and the rectangular waveguide are required to ensure a good impedance match as well as a low insertion loss. The substrate material has a thickness  $D$ ; the gap between the fins has a width  $G$ ; and the distances from the fins to the two waveguide walls are  $W_1$  and  $W_2$ , respectively. In all of the cases considered in this report, the fins are assumed to be placed symmetrically with respect to the waveguide walls ( $W_1=W_2$ ).

WR-10 waveguide is assumed in all of the structures that are dealt with here. This waveguide has the dimensions  $a=100$  mils and  $b=50$  mils, and it operates with a single  $\text{TE}_{10}$  mode over the entire 75-110 Ghz band. The substrate is quartz with a relative dielectric constant of  $\epsilon_r=3.78$  and a thickness  $D=5.0$  mils. Quartz has been selected on account of its excellent electrical properties such as

low electrical losses and its relatively low dielectric constant.

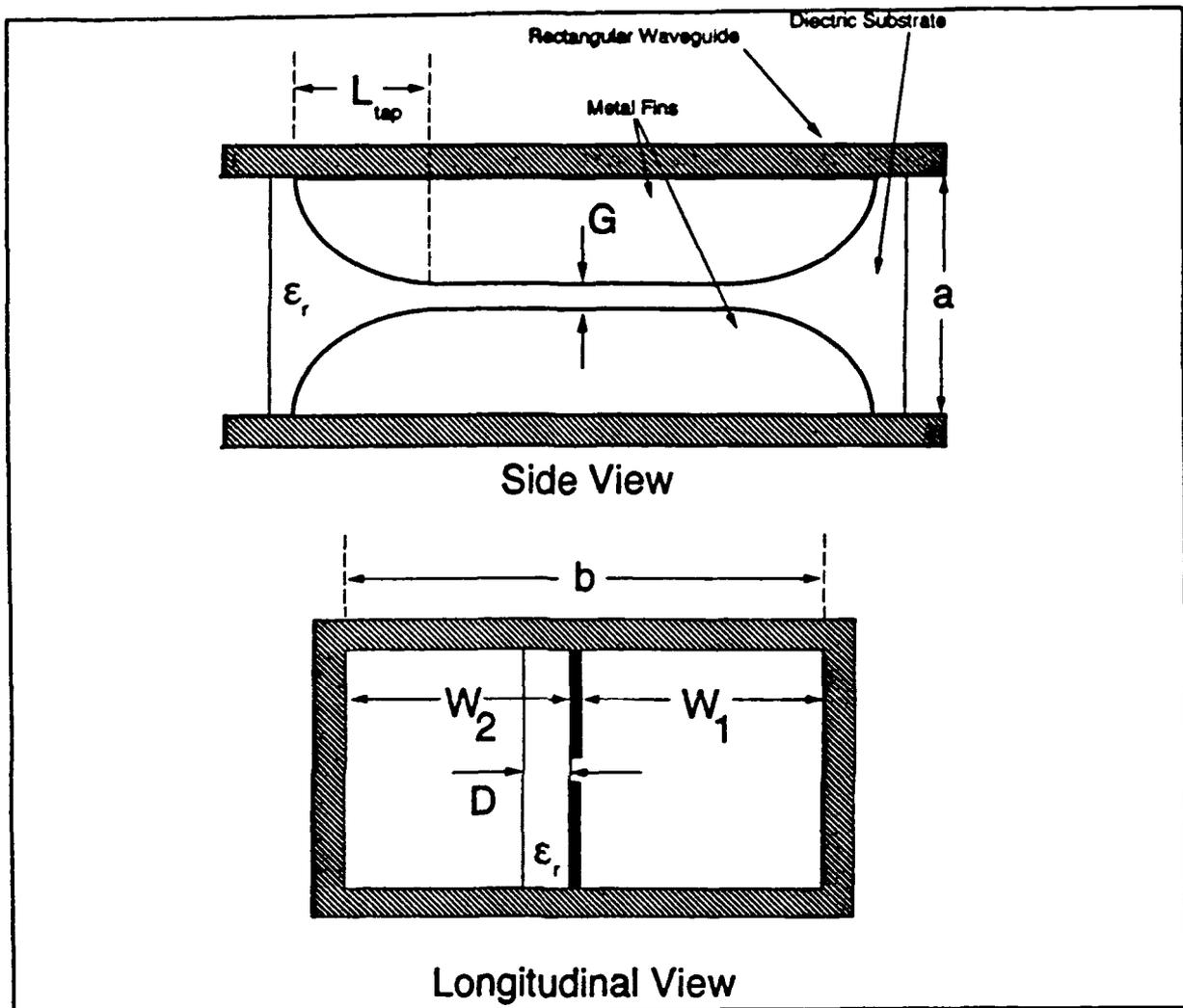


Figure 1. The geometry of the fin line structure that is the basis of the variable stepped attenuator.

Also, quartz has excellent mechanical rigidity that makes it very suitable for mounting in WR-10 waveguide. Although a soft substrate such as Duriod possesses superior electrical properties (such as a smaller loss tangent and a lower dielectric constant) to those of quartz, soft substrates do not have the necessary rigidity to be mounted accurately in the waveguide. Now a thicker substrate such as 10 mil quartz would provide a lot more mechanical strength, but it would also support two propagating modes on the fin line structure, instead of one. The presence of two propagating modes would make the design of the attenuator impossible, so one is limited to a maximum quartz substrate thickness of about 5 mils in order to ensure a single propagating fin line mode.

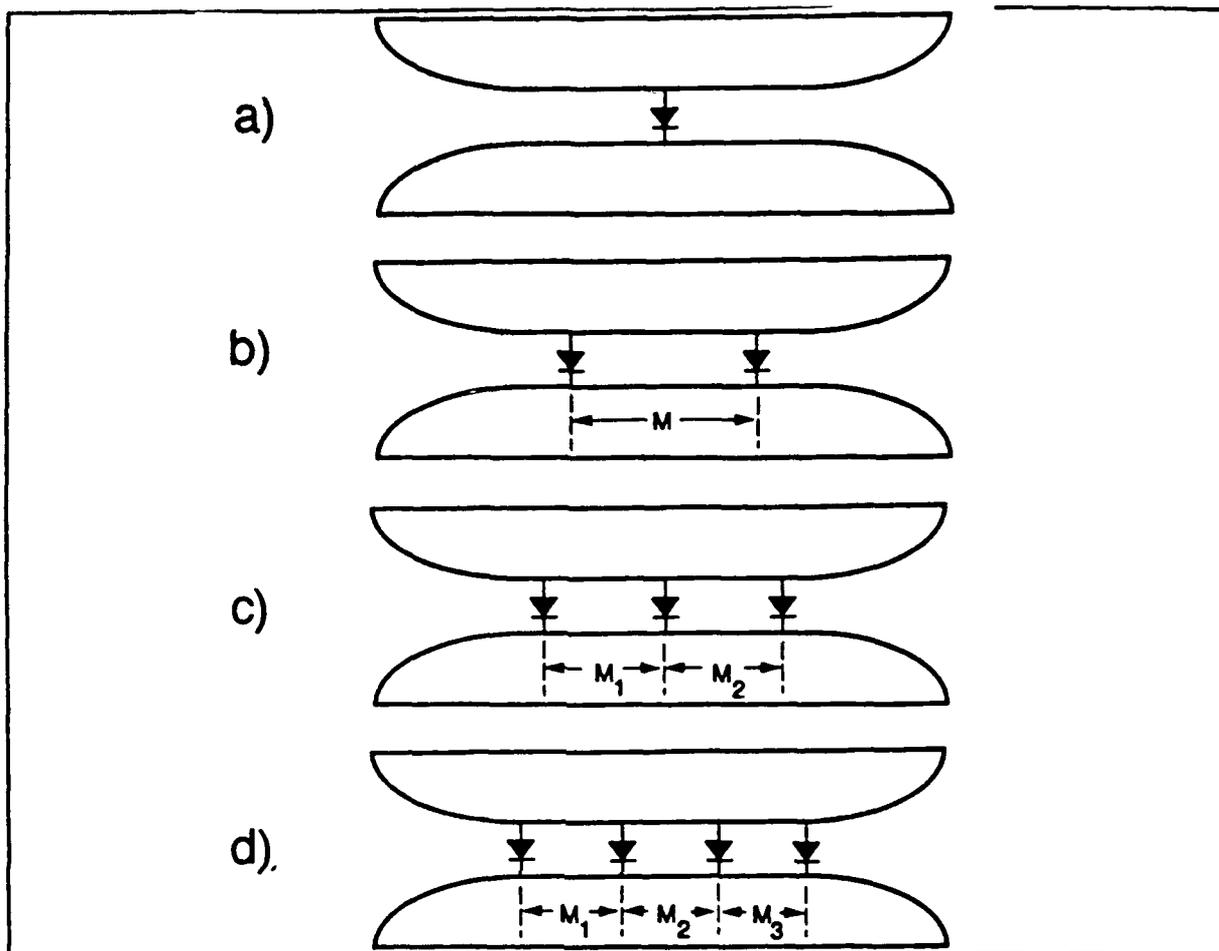


Figure 2. The placement of the PIN diodes in 1,2,3, and 4-diode attenuator configurations.

One way to make a variable attenuator on a fin line structure is to connect PIN diodes in shunt across the gap between the two metallic fins. Figs. 2 a-d depicts fin line attenuator structures that have 1,2,3, and 4 diodes. A one diode structure is shown in Fig. 2a. The variable attenuation characteristics of this structure, as well as all of the others, are obtained by applying a continuously variable bias current through the PIN diode which controls the diode electrical properties. This results in continuously variable attenuation characteristics. Fig. 2b depicts a two diode structure in which the PIN diodes are spaced a distance  $M$  apart. The diode spacing  $M$  can be determined by various optimization procedures that are dealt with in later sections. A three diode attenuator structure is depicted in Fig. 2c. Here the three diodes are separated by the distances  $M_1$  and  $M_2$ . These two distances can also be set by a number of optimization criteria. A four diode attenuator is shown in Fig. 2d. In this figure, four diodes are

separated by the distances  $M_1$ ,  $M_2$ , and  $M_3$  which can also be found by various optimization criteria.

In order to determine the characteristics of the attenuator, the fin line transmission structure and the associated PIN diodes must be modeled along with the tapered sections. The quantities of primary interest in this case are the insertion loss  $|S_{12}|$ , the return loss  $|S_{11}|$ , and the input reflection coefficient  $S_{11}$ . Structural symmetry (with respect to the longitudinal direction) is assumed in this case so that  $S_{11}=S_{22}$ . The fin line is modeled as a dispersive transmission line whose characteristic impedance  $Z_c(f)$  and guide wavelength  $\lambda_g(f)$  are both a function of frequency and geometry. The effects of the PIN diodes are modeled by attaching (bias) current dependent impedances to the transmission line structure as is shown for a three diode structure in Fig. 3.

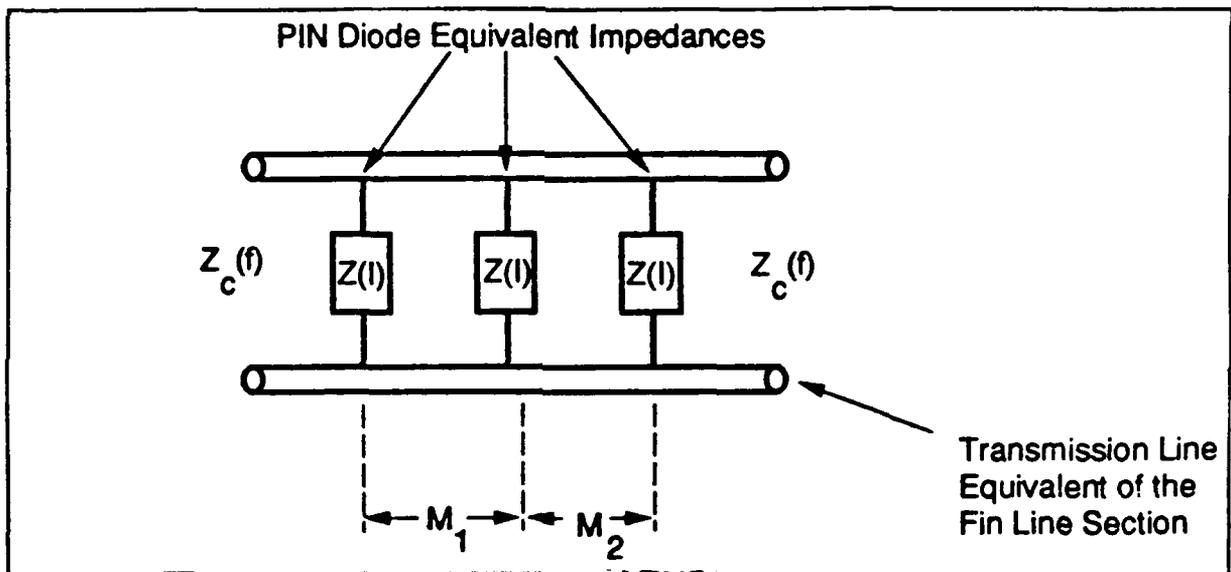


Figure 3. The model of a 3-diode fin line attenuator.

The impedance properties of the PIN diodes are a function of the bias currents of the PIN diodes. In the reverse or zero bias case, the impedance of the PIN diode can be simulated by the simple series LC circuit shown in Fig. 4a. Here the series inductance  $L$  is due mainly to the lead inductance of the PIN diode, and the capacitance arises from a combination of reverse junction capacitance and package parasitic effects. As will be seen in the next section, the loading effects of a PIN diode can be very significant in the zero or reverse bias case. In the forward biased case, the PIN diode can be modeled as a simple series RL network as is shown in Fig. 4b. In this case, the resistive component  $R$  is a current dependent resistance, and the inductance  $L$  is due to the lead inductance effects. These models account for the bulk of the loading effects produced by the presence of beam lead PIN diodes.

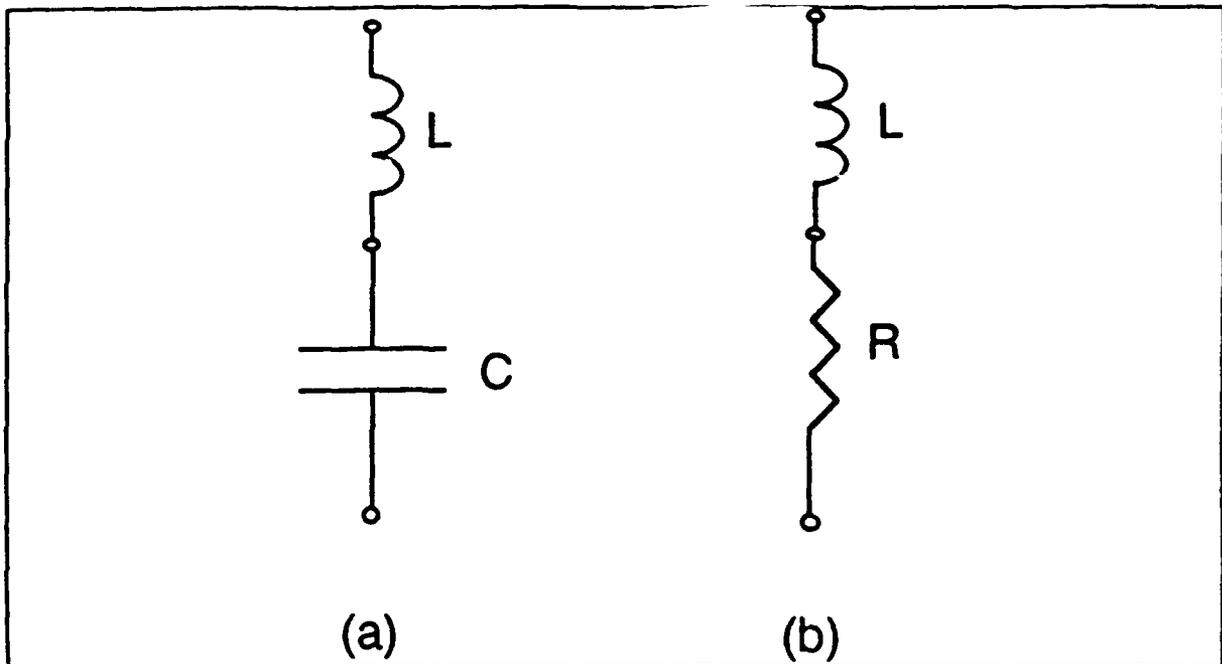


Figure 4. The PIN diode circuit models. a) The reverse or zero-bias model. b) The forward bias model.

In order to simulate the effects of the fin line to waveguide tapers, one could either analyze the effects accurately using a full-wave electromagnetic simulator and incorporate the S-parameter results of this analysis into HP MDS, or one could simulate the taper by a sufficient number of electrically short fin line transmission lines. Since the issues of the taper design have not yet been fully explored, a gradual taper will be assumed for the purpose of determining the attenuator characteristics. Therefore, the effects of the taper on the attenuator characteristics will be deferred until a later report. It should be noted that if losses are ignored, a gradual enough taper will have virtually no effect on the behavior of the attenuator. Thus, the most significant characteristics of the fin line attenuator can be obtained by completely ignoring the taper effects. The simulation of a waveguide to fin line to waveguide structure is dealt with in section 6 of this report.

### SECTION 3-EFFECTS OF LEAD INDUCTANCE ON A REVERSE BIASED, ONE DIODE STRUCTURE

In order to fabricate an attenuator prototype, beam lead PIN diodes will be connected across the fin line gap. One suitable candidate is the M/A-COM MA 4P800 silicon beam lead diode which has a total reverse capacitance (junction+parasitic effects) of  $C=0.020$  pF. The lead inductance of this PIN diode is strongly dependent on the lead lengths as well as the proximity effects of the fins. Based on results available in the literature and manufacturer's data, the

lead inductance can lie anywhere in the range  $0.01 \text{ nH} \leq L \leq 0.1 \text{ nH}$  for gap widths in the range of  $5 \leq G \leq 10$  mils. Now a lower limit of  $G=5$  mils occurs because of the size of the diode packaging. Also, there is a 10 mil upper limit on the fin line gap in order to avoid excessive lead inductances and to minimize the characteristic impedance of the fin line. Now the characteristic impedance of a fin line structure decreases as the gap width becomes smaller, and the bandwidth of the resulting attenuator structure is increased. Thus the smallest gap width that will accommodate the PIN diode package is the most desirable since a relatively large bandwidth is required. There are a wide variety of possibilities for lead inductance values. In order to obtain a better estimate of the lead inductance value, it will be necessary to perform measurements on a prototype attenuator structure and extract the diode equivalent parameters. The significance of the lead inductance value, therefore, can be grasped fully by studying the attenuator characteristics as a function of a variable lead inductance.

Results are depicted in Figs. 5-8 for a single, reversed biased diode connected across the fin line. In these results as well as others, the conductors are assumed to be perfectly conducting and dielectric losses are ignored. The diode model used in these cases corresponds to that of Fig. 4b with  $C=0.02 \text{ pF}$  and  $L=0.0, 0.02, 0.05, 0.1 \text{ nH}$ . In all of these plots the PIN diode is assumed to be connected across a 5 mil wide gap ( $G=5$  mils) on a 5 mil thick quartz substrate ( $\epsilon_r=3.78$ ). As an inspection of these plots reveals, the attenuator characteristics are significantly influenced by the lead inductance and the reverse capacitance. A study of Fig. 5 indicates that a significant insertion loss and a mismatch are introduced by the reverse capacitance of PIN diode, even when there are no assumed lead inductance effects. This fact comes as no surprise since the characteristic impedance of the fin line is approximately  $135 \Omega$  from 75-110 GHz and the reactance of the  $0.02 \text{ pF}$  capacitance is  $86 \Omega$  at 92.5 GHz. This capacitive reactance is a significant load on a  $135 \Omega$  line as can readily be observed in Fig. 5, where the return loss varies from 5 dB at 75 GHz to 3.5 dB at 110 GHz. The insertion loss, which is generated by reflections from the purely reactive load, varies from 1.5 dB at 75.0 GHz to 2.8 dB at 110 GHz. The effects of an increasing lead inductance can be readily observed by inspecting Figs. 6-8. Adding lead inductance in series with the reverse junction capacitance reduces the net shunt reactance across the fin line, thereby increasing the insertion loss and the impedance mismatch. If the lead inductance is increased sufficiently, the inductive and capacitive reactances cancel each other, which effectively places a RF short circuit across the line. The results of a resonance that occurs at 112.5 GHz, due to a  $0.1 \text{ nH}$  lead inductance can be seen in Fig. 8. In this figure, the insertion loss is 28 dB at 110 GHz with virtually no return loss. As these results indicate, the lead inductance must be kept well below  $0.1 \text{ nH}$  in order to avoid resonance effects.

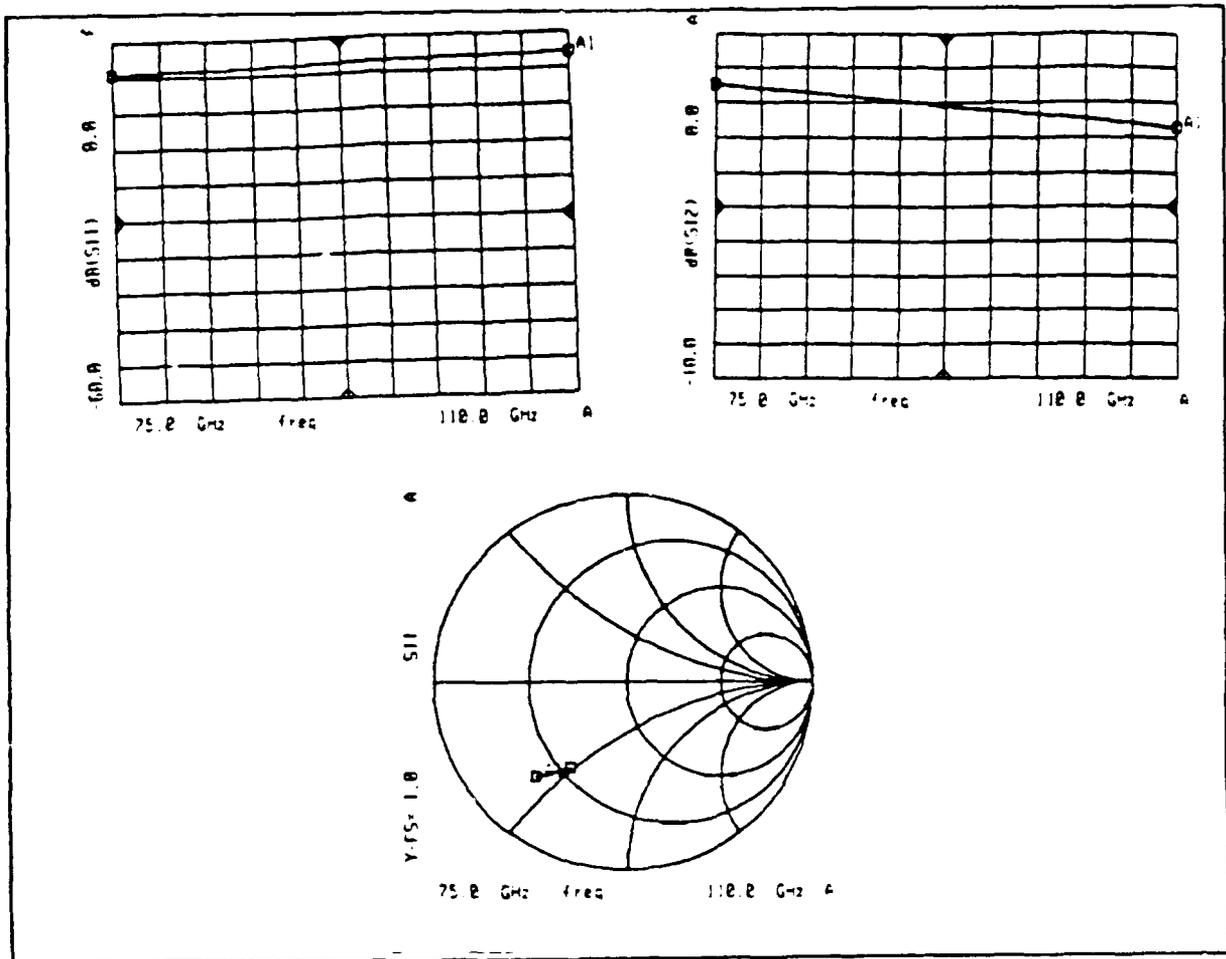


Figure 5. Fin line attenuator return loss, insertion loss, and input impedance for a single reverse-biased PIN diode with the parameters  $L=0.0$  nH and  $C=0.02$  pF.

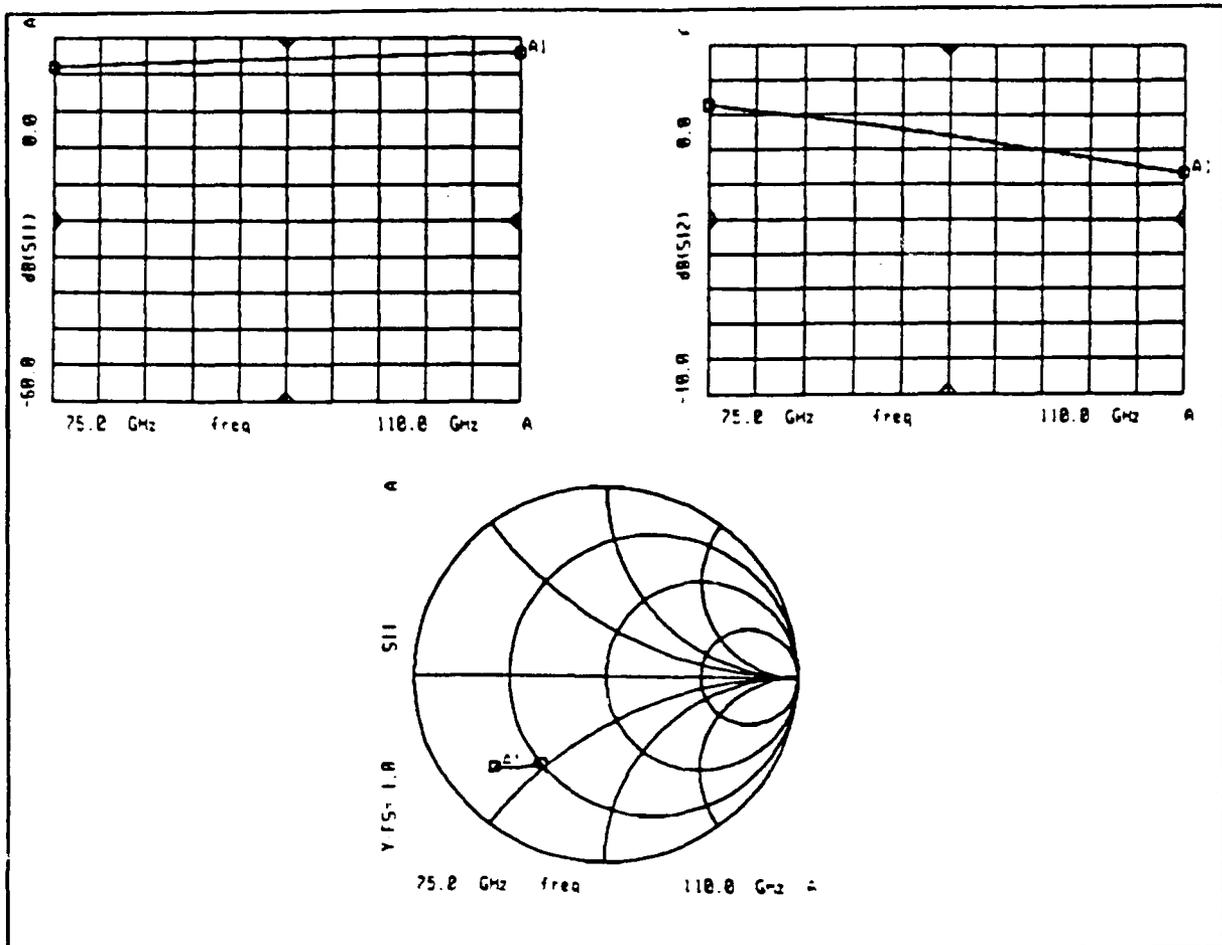


Figure 6. Fin line attenuator return loss, insertion loss, and input impedance for a single reverse-biased PIN diode with the parameters  $L=0.02$  nH and  $C=0.02$  pF.

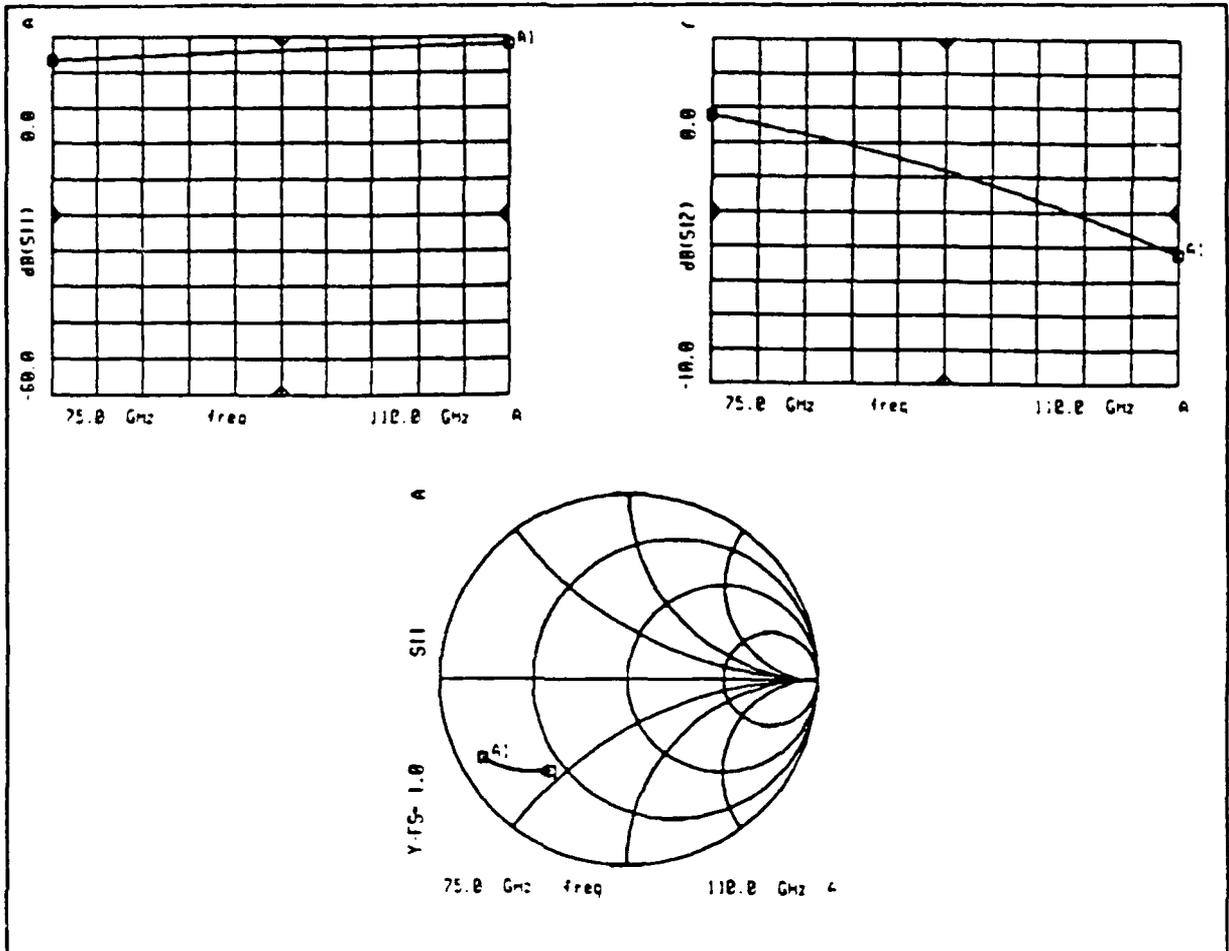


Figure 7. Fin line attenuator return loss, insertion loss, and input impedance for a single reverse-biased PIN diode with the parameters  $L=0.05$  nH and  $C=0.02$  pF.

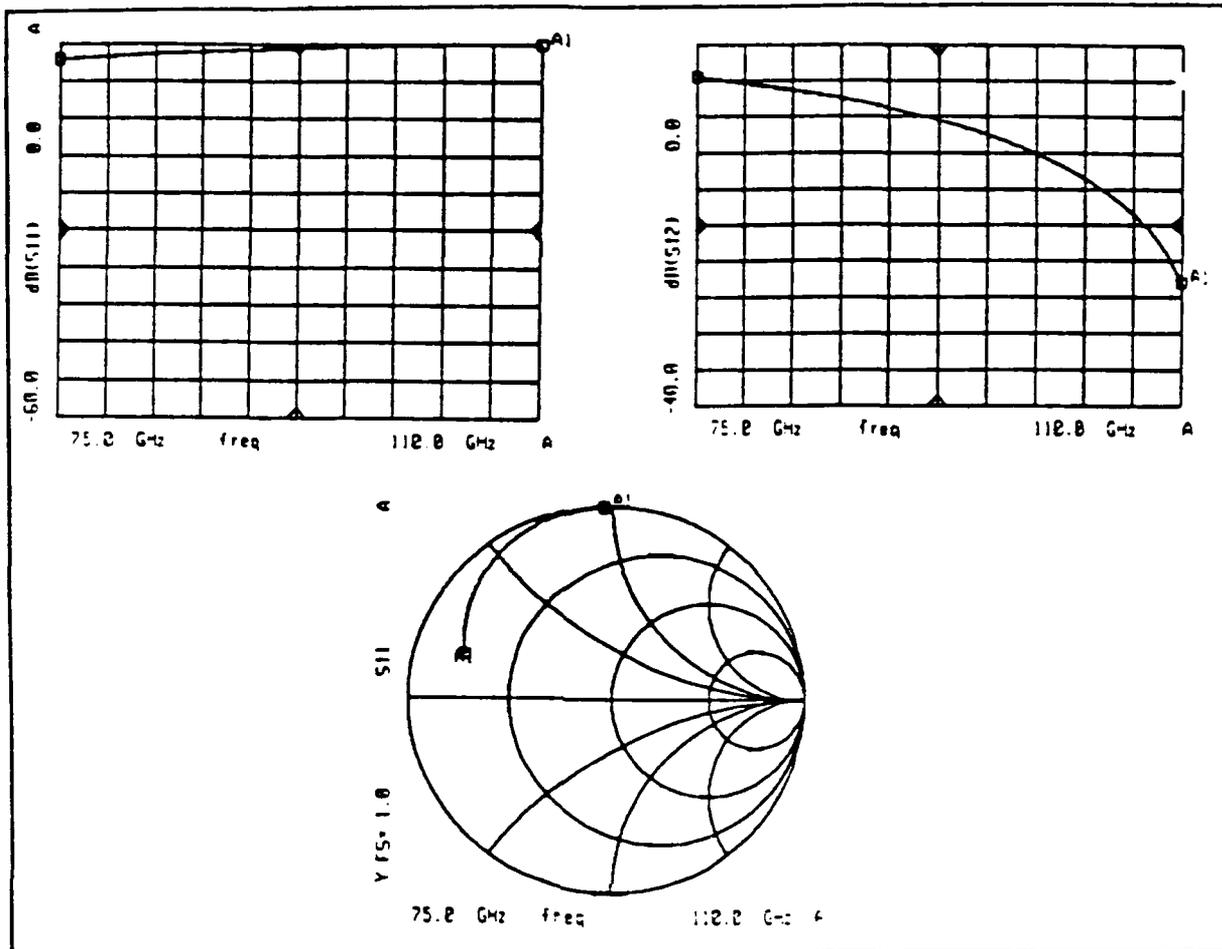


Figure 8. Fin line attenuator return loss, insertion loss, and input impedance for a single reverse-biased PIN diode with the parameters  $L=0.1$  nH and  $C=0.02$  pF.

#### SECTION 4-REVERSE BIASED MULTIPLE DIODE RESULTS

In this section, the attenuator characteristics for 2,3, and 4 reverse biased PIN diode clusters are presented. As was seen in the last section, the loading effect of one reverse biased PIN diode can be quite significant. When multiple diodes are connected in shunt across the fin line structure, the problem of loading becomes more severe. Because of this, the spacings of the diodes must be placed so that a low insertion loss and a high return loss occur. Determining the diodes locations when the loading effects are so pronounced is not a trivial issue, particularly when a good impedance match and a low insertion loss are desired across the entire 75-110 GHz band. Thus a trial and error approach to the placement of the diodes is quite unproductive, particularly when there are either three or four diodes in a cluster. A much more efficient way to find the proper location of the diodes is to

utilize an optimization routine that will vary the diode spacings until either  $|S_{11}|$  is minimized or  $|S_{12}|$  is maximized. In principle, optimizations could also be carried out with respect to any combination or function of these circuit S-parameters, although there are no other obvious choices that are readily apparent. Figs. 9-11 depict the optimized results that are obtained when the diode spacings are found by minimizing  $|S_{11}|$  by means of the gradient optimizer that is contained in the HP MDS software package. The optimizer performed a least squares analysis at 100 evenly spaced frequency points throughout the 75-110 GHz band. In these plots, the lead inductance is assumed to have a nominal value of 0.02 nH and a reverse capacitance of 0.02 pF. Unlike the one diode case, an inspection of the curves shows that a good match is achieved over about a quarter of the band for two diode and four diode clusters, and about a tenth of the band for a three diode attenuator. Thus the reactive loading of the diodes is too heavy to obtain a good match across the entire band. The resulting insertion loss varies from 0-1.3 dB for the two diode attenuator, 0-2.3 dB for a 3 diode attenuator, and 0-2.1 dB for a 4 diode attenuator. The reason that 0 dB insertion loss levels are obtained is due to the fact that dielectric and metallic losses have not been accounted for in the MDS analysis. As can be seen from an inspection of the results, the center-to-center diode spacings do not exceed 20 mils. The diodes, therefore, have to be spaced fairly closely in order to achieve adequate bandwidths. If the diodes are spaced further apart, the bandwidth is reduced greatly. This phenomenon can be observed in Fig. 12 for a two diode attenuator. In this case, the optimizer minimized the reflection coefficient  $|S_{11}|$  for spacings in the range  $30 \leq M \leq 100$  mils. The optimal value for the spacing M is 57.2 mils. With this larger spacing, the insertion loss exhibits variations of greater than 5 dB across the entire band. Also, this attenuator has only about half of the impedance bandwidth of the more closely spaced two diode attenuator configuration. It is imperative to keep the PIN diode spacings close in order to achieve the required bandwidth.

In addition to optimizing with respect to the reflection coefficient magnitude, attempts were made to find spacings which would maximize the transmission coefficient magnitude. In the two diode case, the results are almost the same as the previous reflection results. In fact the reflection and transmission spacings differ by less than 0.1 mil. There are no discernable differences between the two sets of curves. In the three diode case, the resulting diode spacings were smaller than the diode package dimensions, which is not an acceptable solution. Similar close spacings were obtained for a four diode attenuator. Even if it were possible to connect the PIN diodes at distances smaller than the package dimensions (by bending the beam leads for instance), the modeling procedures that are being used here would probably not be valid anyway. Minimizing the reflection coefficients yields much more reasonable diode spacings as well as a much greater certainty of success with the modeling procedures.

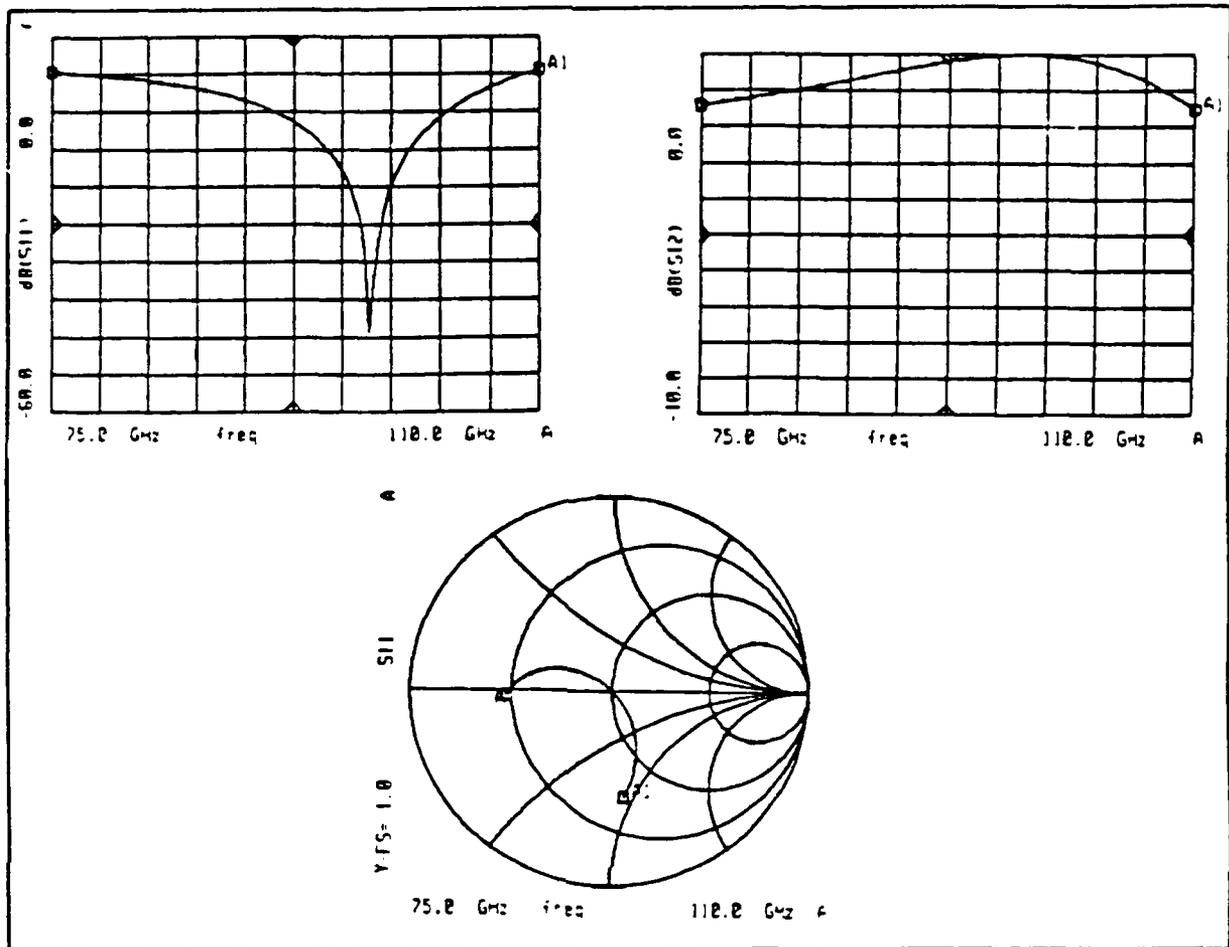


Figure 9. Two-diode attenuator results for the reverse biased case. The spacing between the diodes was found by optimizing  $|S_{11}|$ .  $M=11.5$  mils,  $C=0.02$  pF, and  $L=0.02$  nH.

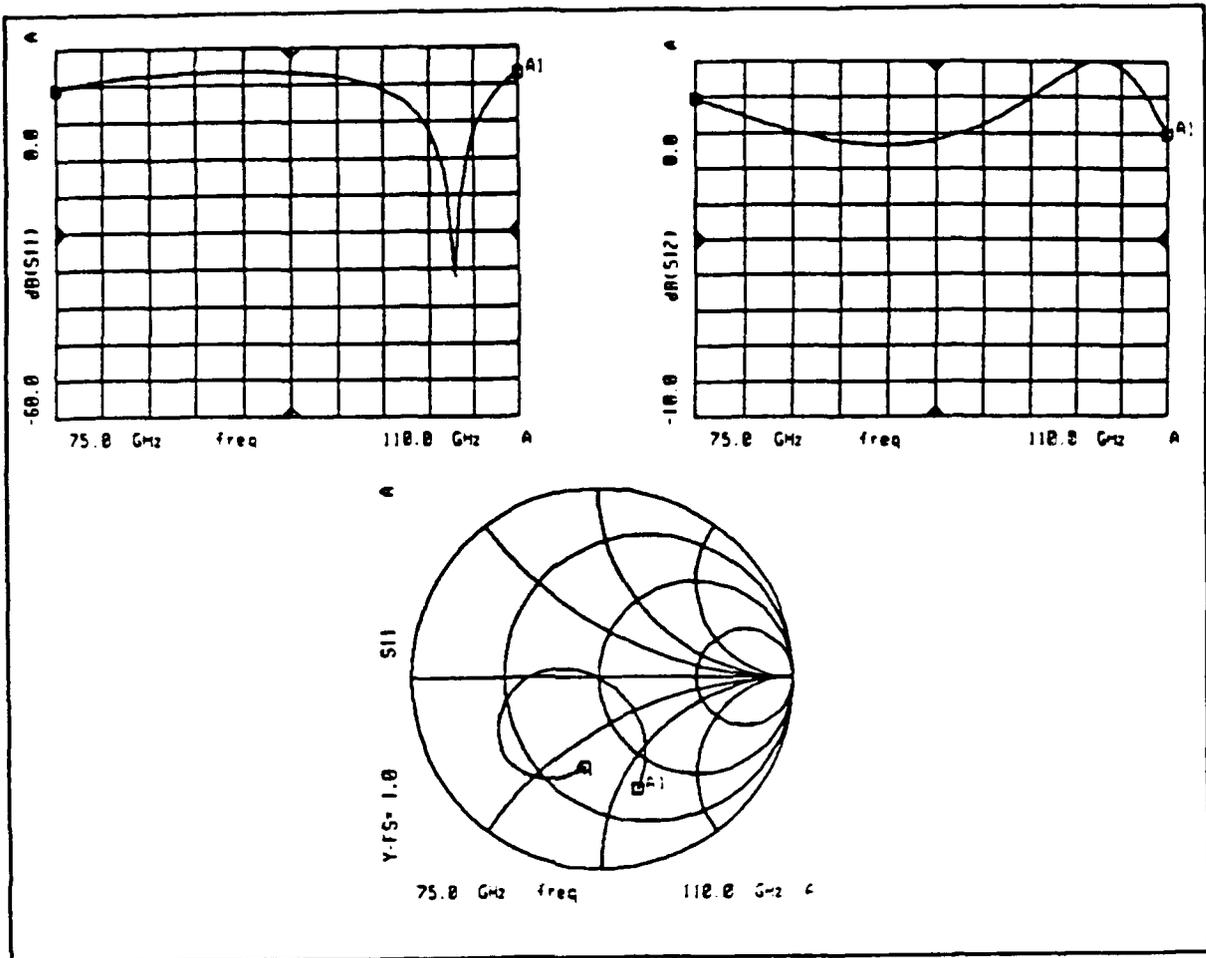


Figure 10. Three-diode attenuator results for the reverse biased case. The spacing between the diodes was found by optimizing  $|S_{11}|$ .  $M_1=M_2=14.6$  mils,  $C=0.02$  pF, and  $L=0.02$  nH.

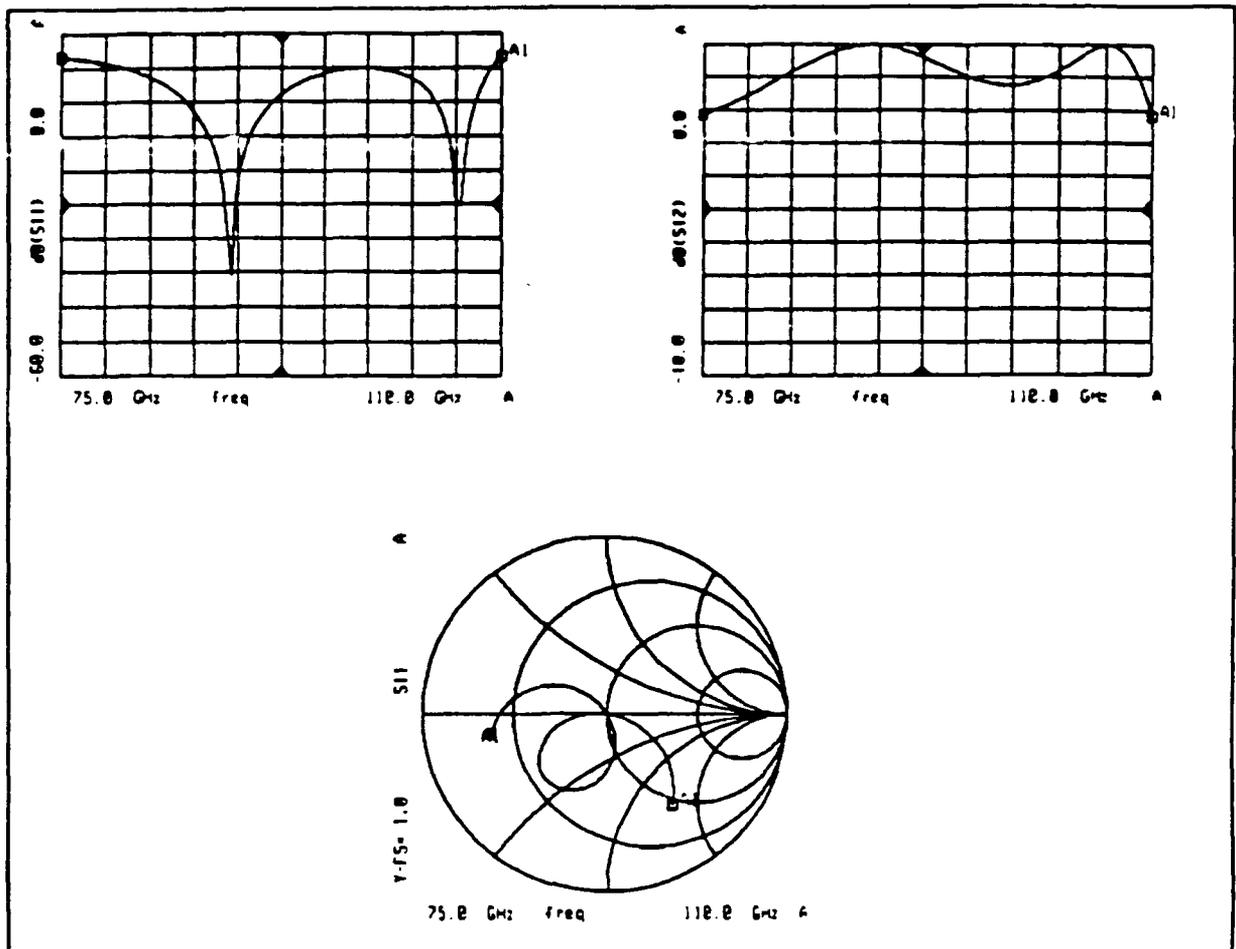


Figure 11. Four-diode attenuator results for the reverse biased case. The spacing between the diodes was found by optimizing  $|S_{11}|$ .  $M_1=M_3=13.9$  mils,  $M_2=19.0$  mils,  $C=0.02$  pF, and  $L=0.02$  nH.

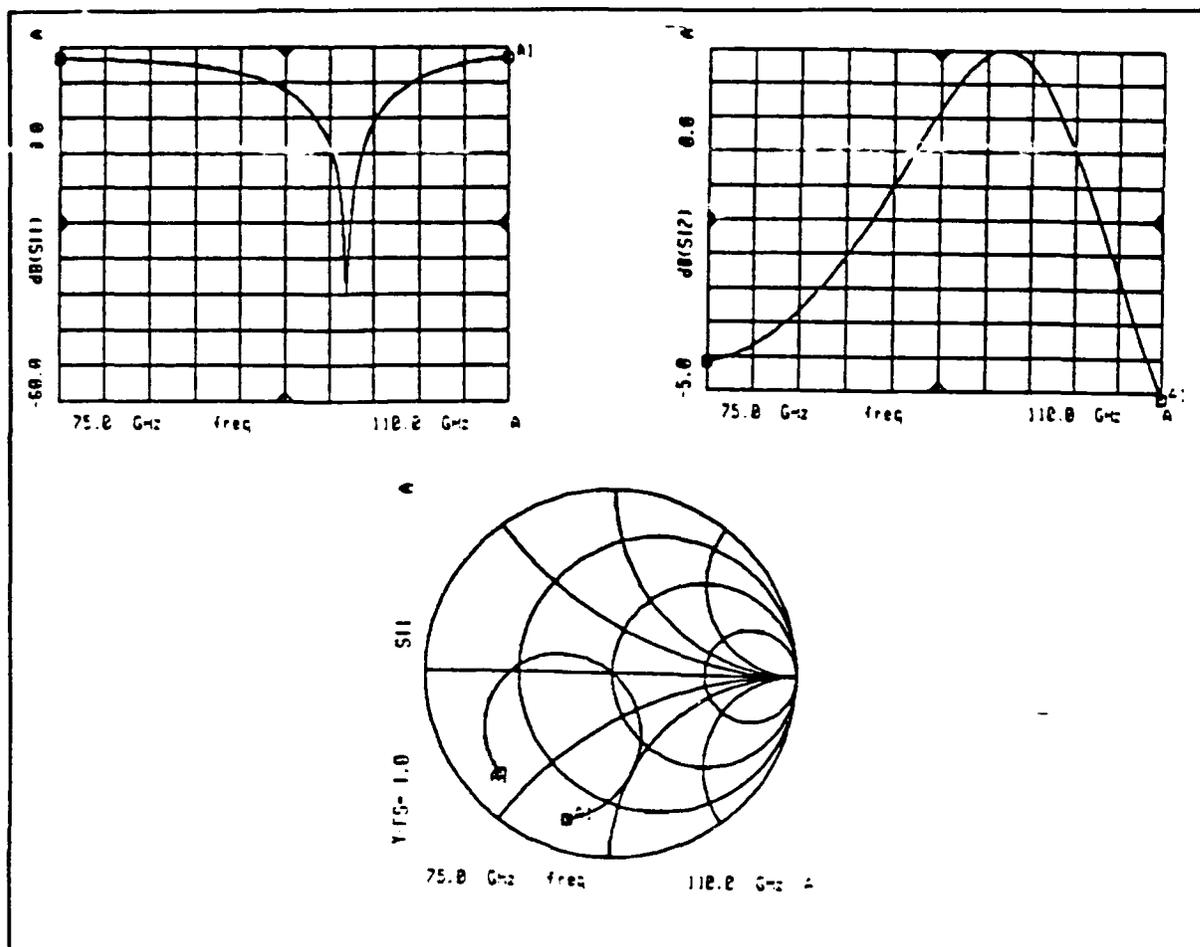


Figure 12. Two-diode attenuator results for a larger spacing in the reverse biased case. The spacing between the diodes was found by optimizing  $|S_{11}|$ .  $M=58.2$  mils,  $C=0.02$  pF, and  $L=0.02$  nH.

#### SECTION 5-ATTENUATOR RESULTS WITH FORWARD BIASED DIODES

In this section, results are presented for various attenuator prototypes with 1,2,3, and 4 diode clusters. In all cases, a nominal lead inductance of 0.02 nH has been assumed; and the forward bias model of Fig. 4b is utilized. The diode spacings in the multiple diode configurations have either been determined by the previously derived reverse biased results or from additional optimizations performed on forward biased diodes. Optimizing in the forward biased case is not as straight forward as in the reverse biased case. This is due to the infinite number of possibilities for selecting a bias current. The approach used here is to set the bias current so that the return loss is approximately 10 dB, which corresponds to an input SWR of about 2.0. It turns out that setting  $R_s=125 \Omega$  (which corresponds to  $I=40 \mu A$ ) yields a return loss in the neighborhood of 10 dB for the 1,2,3, and 4 diode attenuator

configurations. Since optimizations have been performed at only one bias current, additional attenuator characteristics are presented for a three diode attenuator with the same diode spacings for bias currents other than 40  $\mu\text{A}$ .

Figs. 13-19 depict 1, 2, 3, and 4 diode results at  $I=40 \mu\text{A}$ . In the multiple diode cases, results for diode spacings that have been determined from an optimization in the reverse biased mode are compared with forward biased optimized attenuator characteristics. The latter spacings have been found by optimizing the sum of the magnitudes of both of the port reflection coefficients ( $|S_{11}|+|S_{22}|$ ) at  $I=40 \mu\text{A}$ . The optimization in this case has been carried out with respect to the sum of both port reflection coefficient magnitudes in order to avoid asymmetrical diode spacings in the three ( $M_1, M_2$ ) and four-diode ( $M_1, M_2$ ) attenuator structures. Symmetrical attenuator structures are necessary to ensure an equally good impedance match at both ports. As an inspection of the multiple diode results indicate, the forward biased optimized diode spacings yields an improvement in port impedance match as well as much flatter insertion loss characteristics. For instance for a three diode attenuator, a 1.5 dB improvement is noted in the return loss and the insertion loss varies approximately 0.25 dB across the band instead of 0.8 dB with the reverse biased spacings. The attenuators that have been optimized under forward biased conditions not only have flatter insertion loss characteristics, but  $|S_{12}|$  is also nearly symmetric about the mid band frequency of 92.5 GHz. It is also interesting to note that when forward biased spacings are used, approximately 4 dB of additional attenuation is obtained for each additional PIN diode that is added to the circuit. Similar behavior is noted when back biased spacings are used, but  $|S_{12}|$  is consistently higher with forward biased spacings.

Figs. 20-23 show three diode attenuator characteristics with  $I=120 \mu\text{A}$  and  $I=7 \mu\text{A}$ . Figs. 20 and 21 depict the results at 120  $\mu\text{A}$ , and Figs. 22 and 23 show the characteristics at 7  $\mu\text{A}$ . As was the case previously, diode spacings have been determined from a back biased optimization and a forward biased optimization at 40  $\mu\text{A}$ . The results are quite gratifying because the forward biased diode spacings yield relatively flat insertion loss characteristics and a better port impedance match. Thus the advantages that are gained by optimizing at 40  $\mu\text{A}$  are maintained at bias currents that are both greater and less than the nominal value of 40  $\mu\text{A}$ .

These results indicate that far superior port impedance match and insertion characteristics can be obtained if the diode spacings are optimized at 40  $\mu\text{A}$  and the attenuator is then operated exclusively with the PIN diodes forward biased at various values of  $I$ . Designing the attenuator to operate in this fashion will greatly aid in meeting the attenuator target specifications.

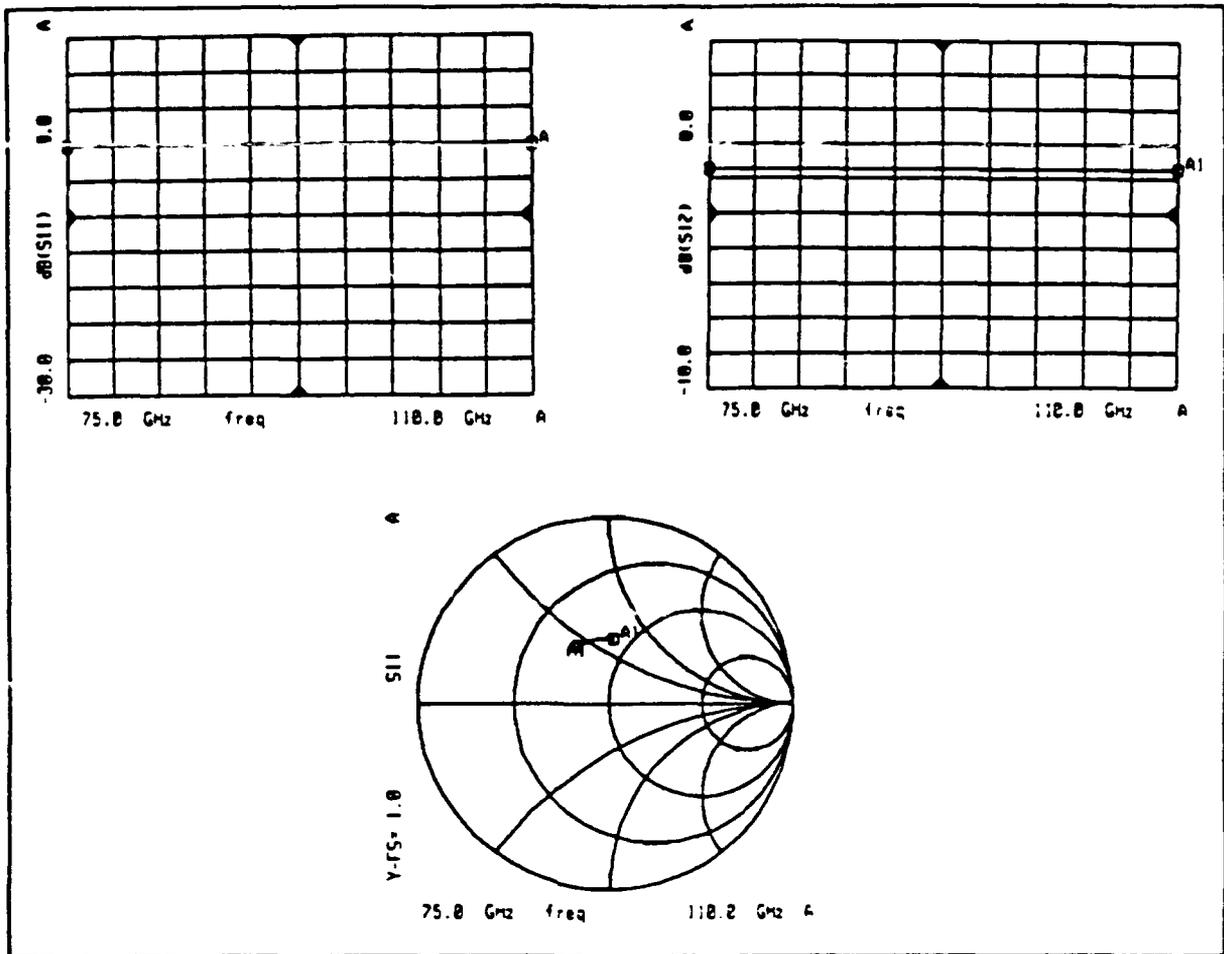


Figure 13. One-diode attenuator characteristics with 40  $\mu$ A of bias current.  $R=125 \Omega$ ,  $L=0.02$  nH.

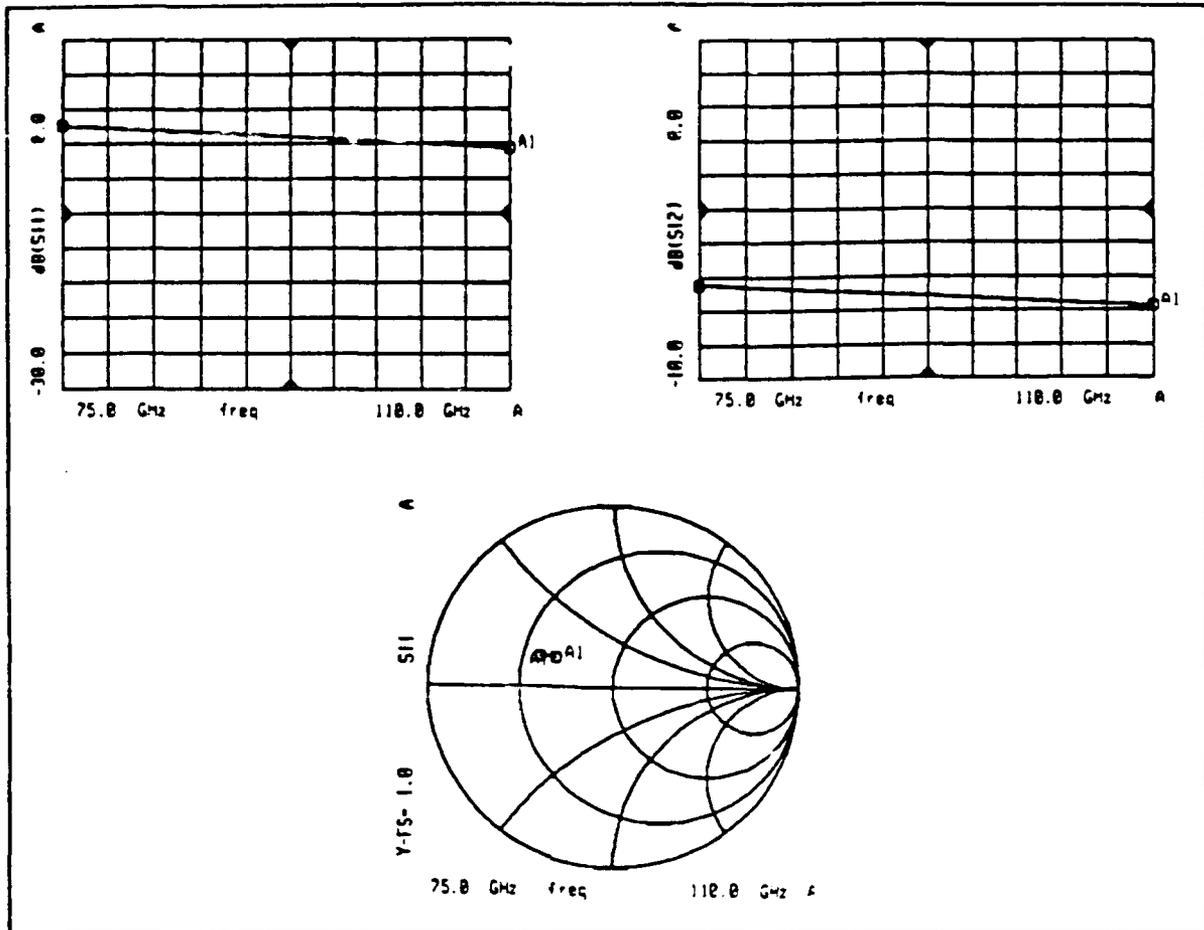


Figure 14. Two-diode attenuator characteristics with  $40 \mu\text{A}$  of bias current.  $R=125 \Omega$ ,  $L=0.02 \text{ nH}$ . Reverse biased spacings are used with  $M=11.5 \text{ mils}$ .

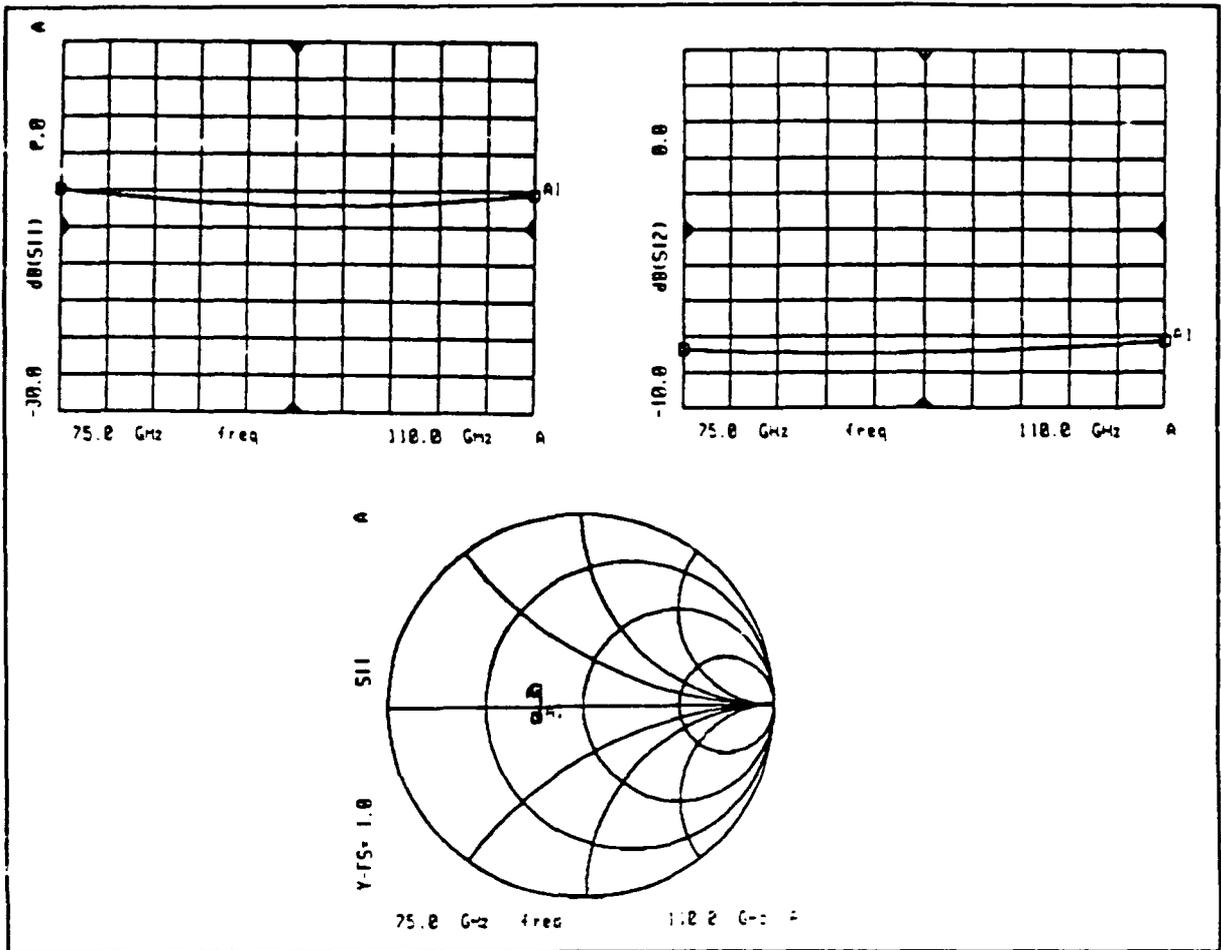


Figure 15. Two-diode attenuator characteristics with  $40 \mu\text{A}$  of bias current.  $R=125 \Omega$ ,  $L=0.02 \text{ nH}$ . Forward biased spacings are used with  $M=24.4 \text{ mils}$ .

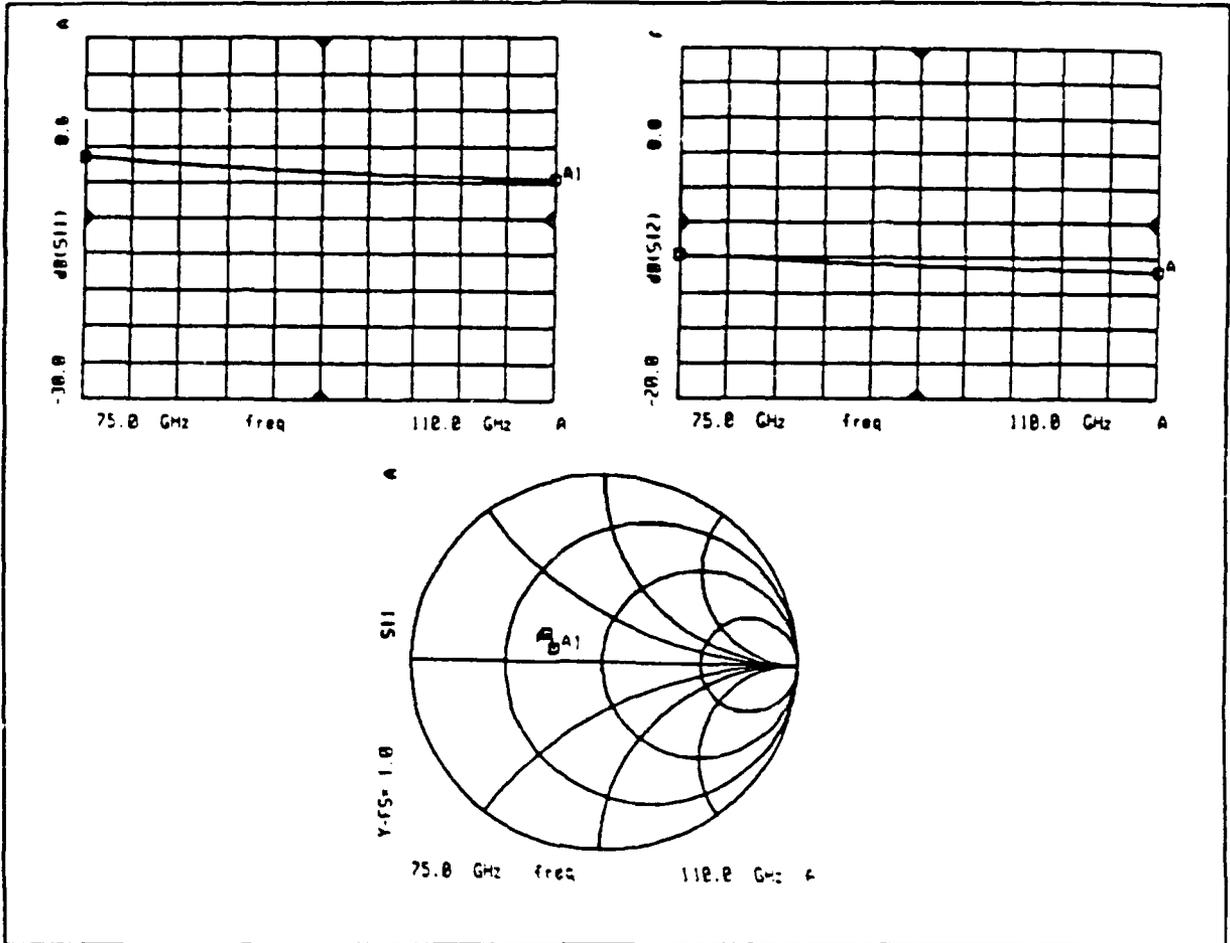


Figure 16. Three-diode attenuator characteristics with 40  $\mu$ A of bias current.  $R=125 \Omega$ ,  $L=0.02$  nH. Reverse biased spacings are  $M_1=M_2=14.64$  mils.

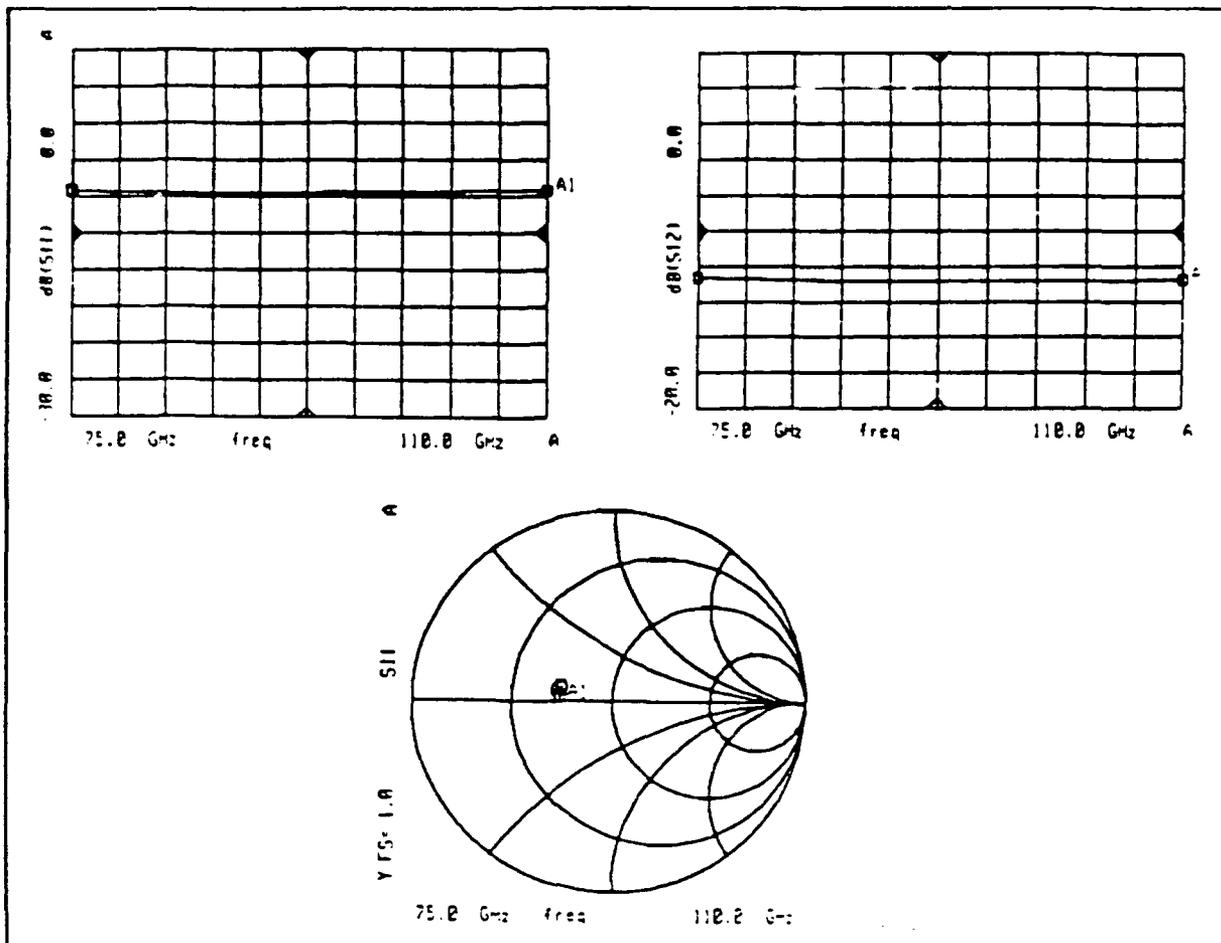


Figure 17. Three-diode attenuator characteristics with  $40 \mu\text{A}$  of bias current where  $R=125 \Omega$ ,  $L=0.02 \text{ nH}$ . Forward biased spacings are  $M_1=M_2=20.6 \text{ mils}$ .

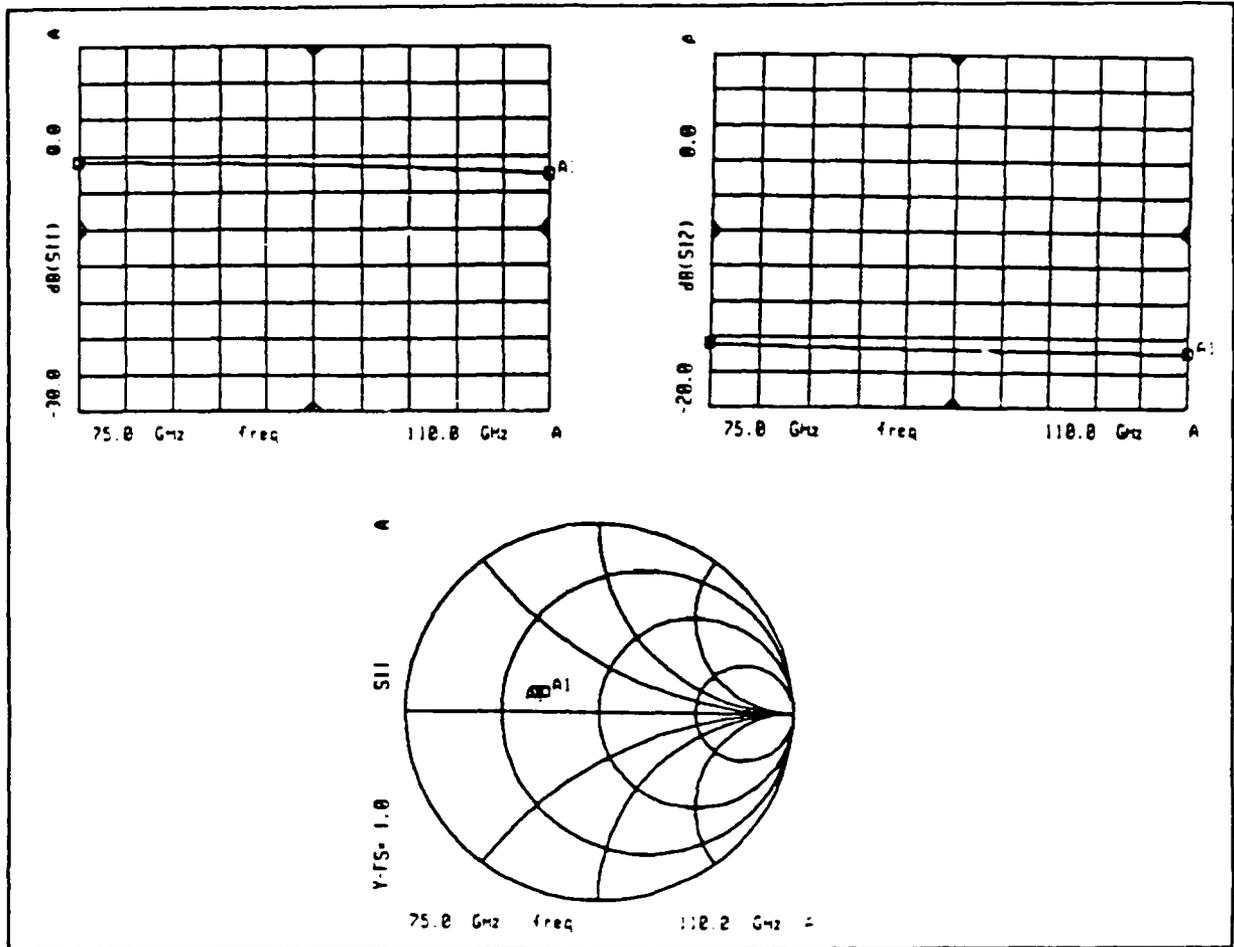


Figure 18. Four-diode attenuator characteristics with 40  $\mu$ A of bias current where  $R=125 \Omega$ ,  $L=0.02$  nH. Reversed biased spacings are  $M_1=M_3=13.9$  mils and  $M_2=19.0$  mils.

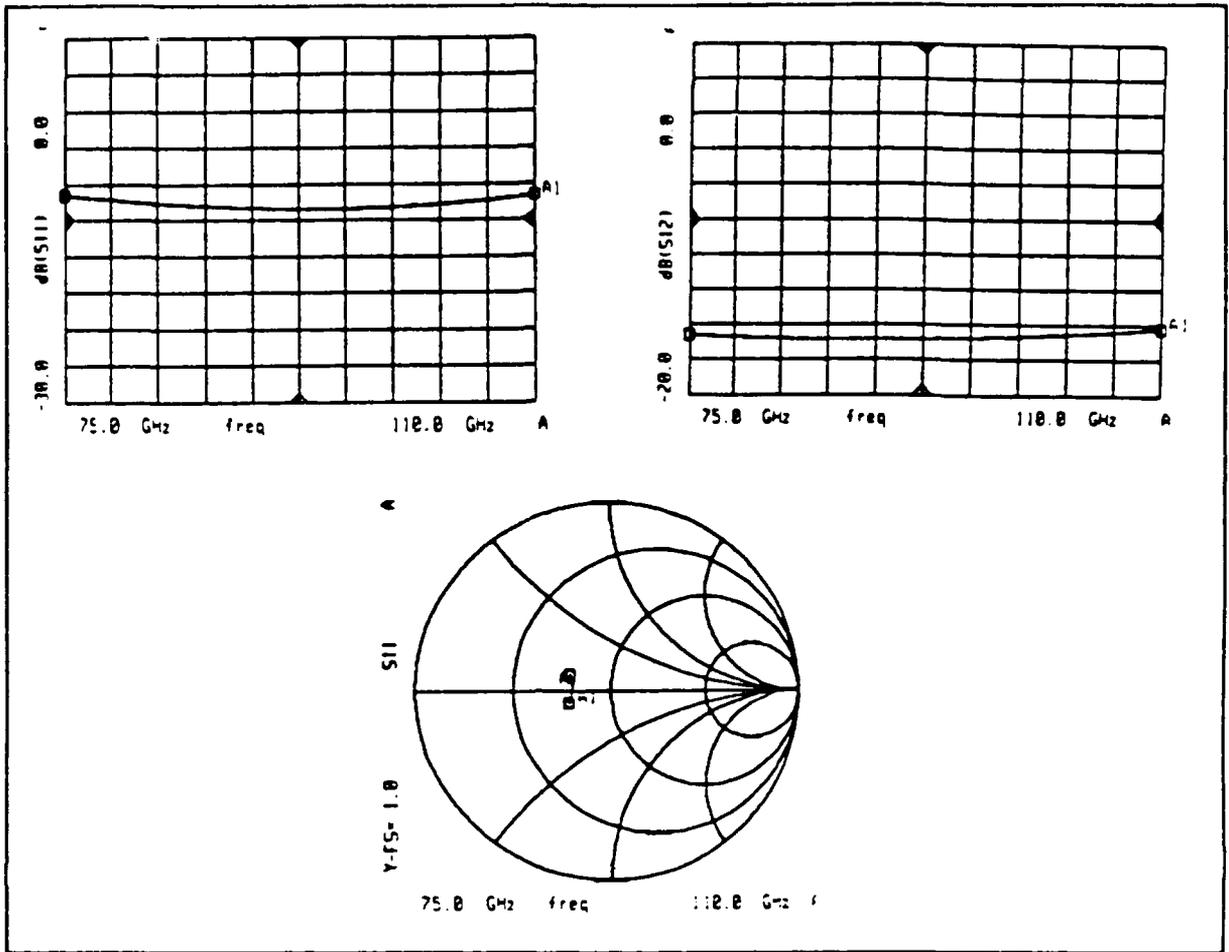


Figure 19. Four-diode attenuator characteristics with  $40 \mu\text{A}$  of bias current where  $R=125 \Omega$ ,  $L=0.02 \text{ nH}$ . Forward biased spacings are  $M_1=M_3=7.0 \text{ mils}$  and  $M_2=23.2 \text{ mils}$ .

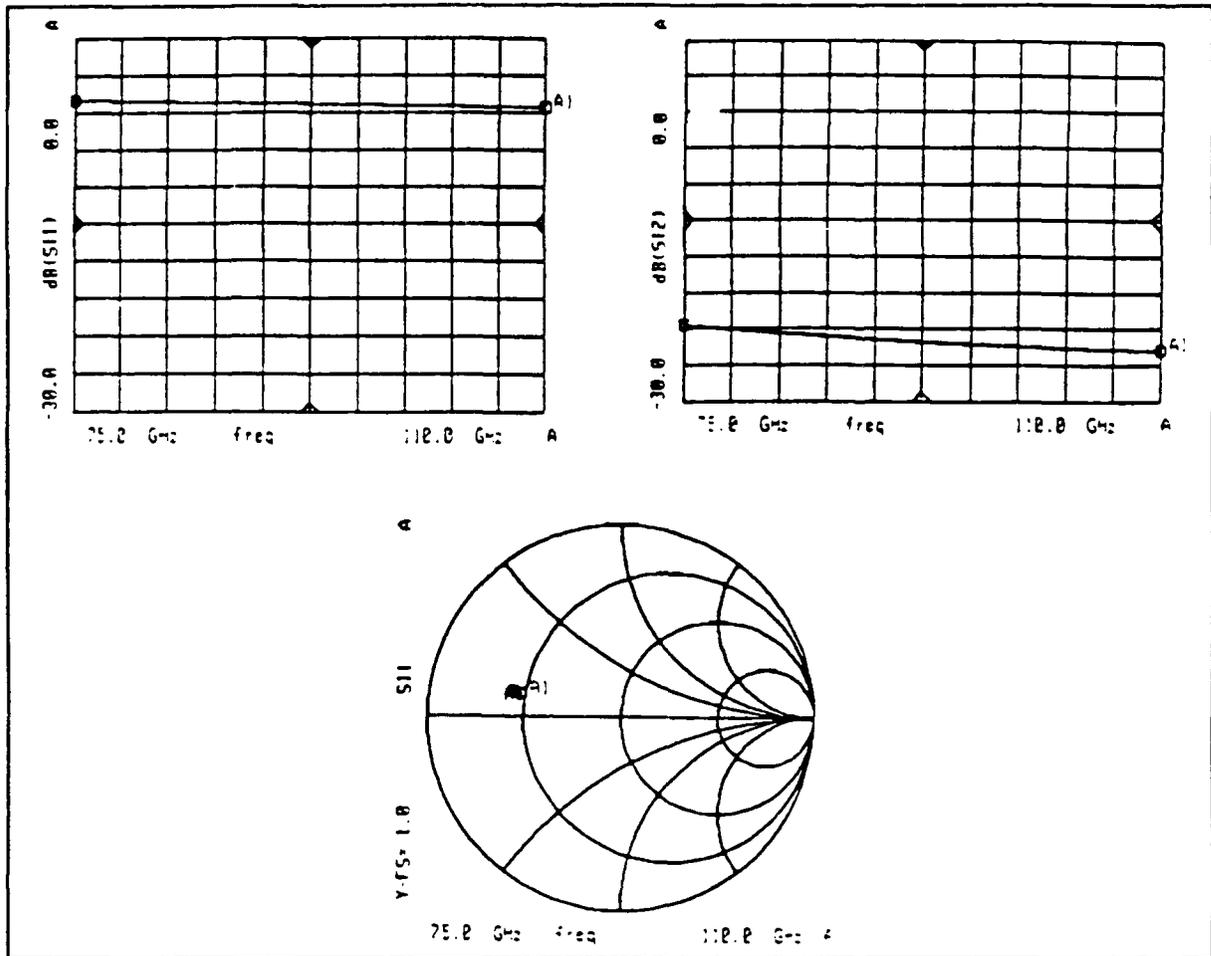


Figure 20. Three-diode attenuator characteristics with 120  $\mu\text{A}$  of bias current where  $R=50 \Omega$ ,  $L=0.02 \text{ nH}$ . Reverse biased spacings are  $M_1=M_2=14.6 \text{ mils}$ .

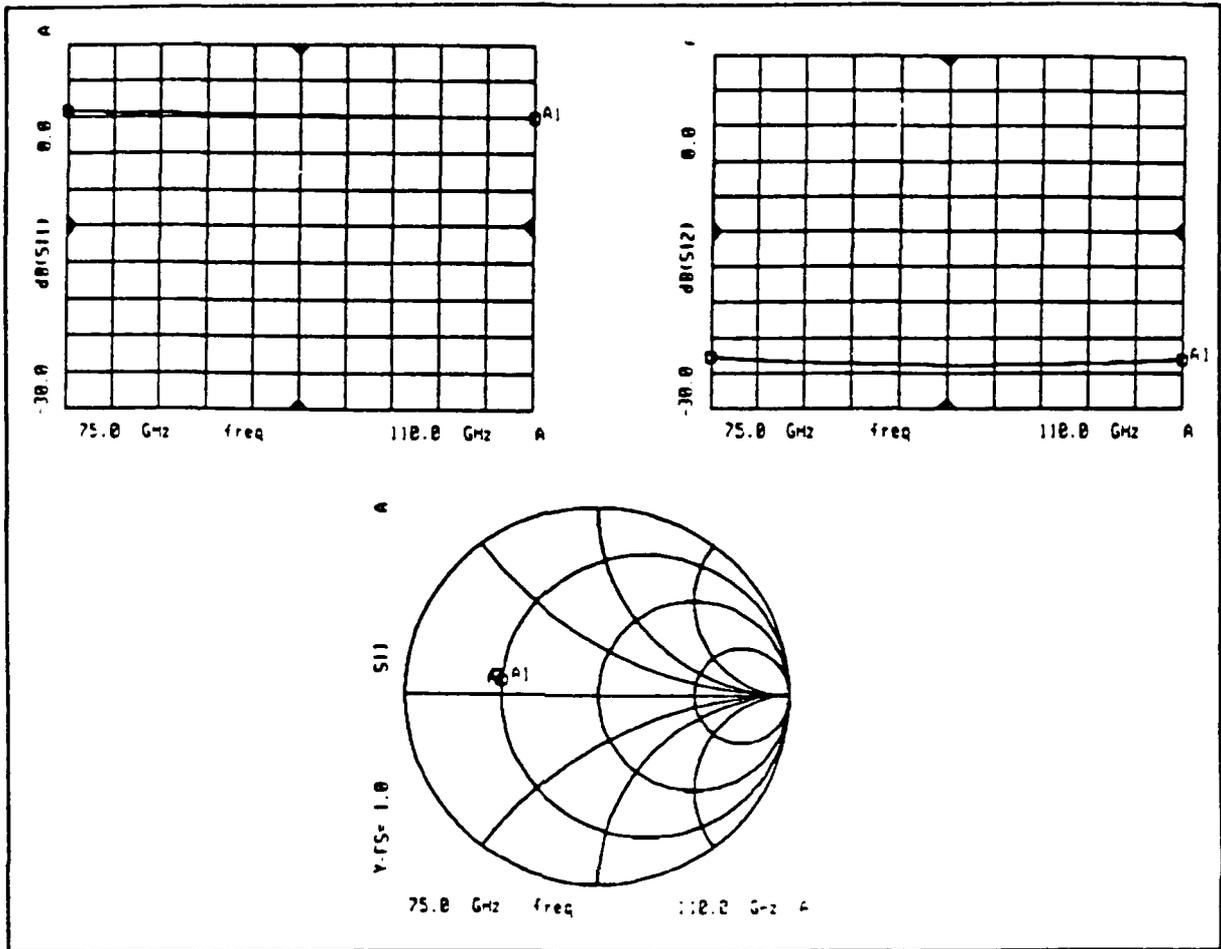


Figure 21. Three-diode attenuator characteristics with  $120 \mu\text{A}$  of bias current where  $R=50 \Omega$ ,  $L=0.02 \text{ nH}$ . Forward biased spacings are  $M_1=M_2=20.6 \text{ mils}$ .

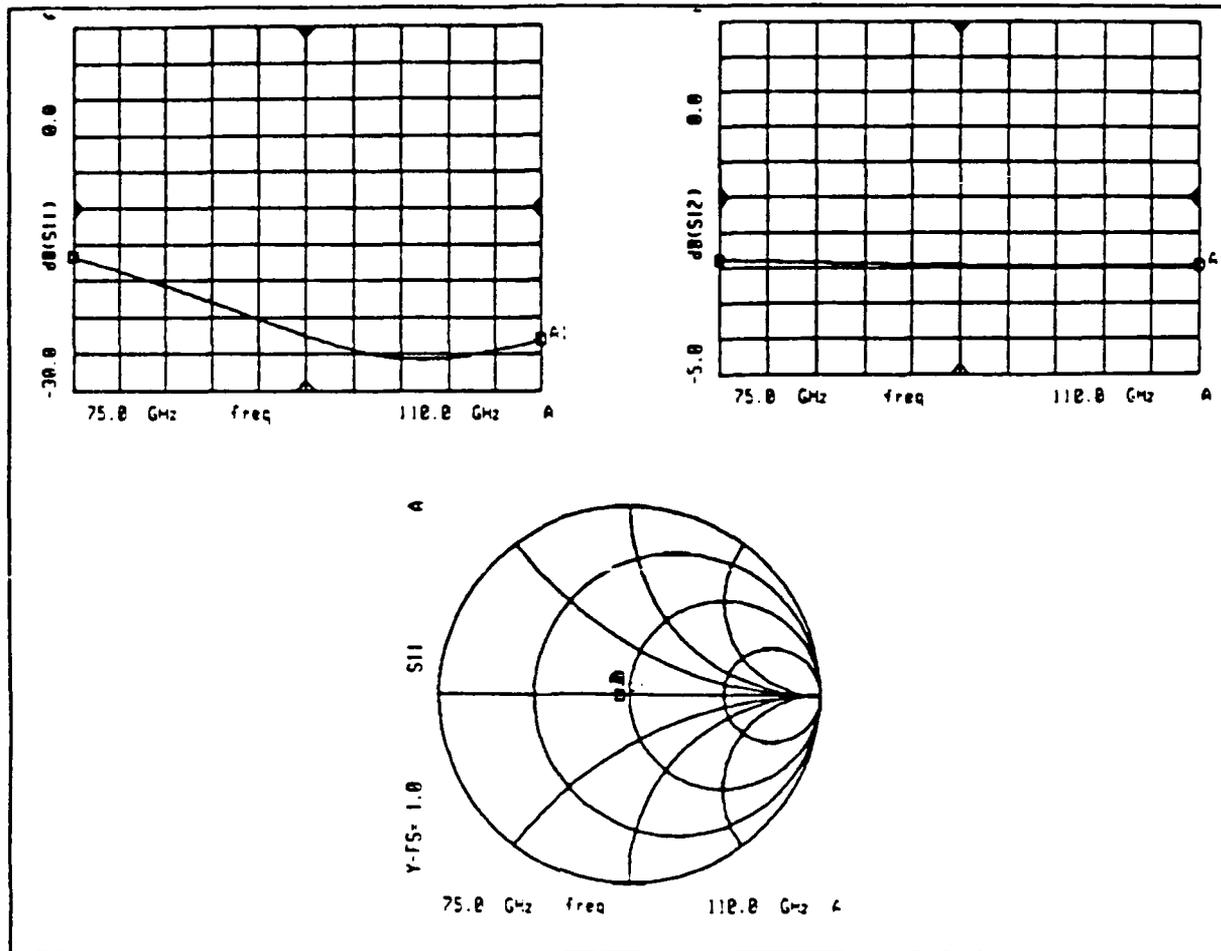


Figure 22. Three-diode attenuator characteristics with 7  $\mu$ A of bias current where  $R=500 \Omega$ ,  $L=0.02$  nH. Reverse biased spacings are  $M_1=M_2=14.6$  mils.

#### SECTION 6-LINEAR TAPER SIMULATION USING HP MDS

Although the issue of the rectangular waveguide to fin line taper has not yet been fully explored, it is interesting to note that HP MDS can be used to simulate the effects of a taper. Fig. 24 depicts a structure that provides a geometrically linear taper from the rectangular waveguide that is 50 mils high to a fin line section with a 5 mil gap. The substrate is assumed to be 5 mils thick with  $\epsilon_r=3.78$ . In this particular case, each of the two taper regions are 300 mils long, and the fin line section is assumed to be 1000 mils long. The rectangular waveguide reference ports, at which the attenuator S-parameters are evaluated, are located 1000 mils from the beginning of the taper region. Both of the tapered regions can be simulated using MDS by replacing the tapers by a series of short cascaded fin line transmission lines as is depicted in Fig. 24 for  $N=5$ . In the case of a linear taper, this process is straight

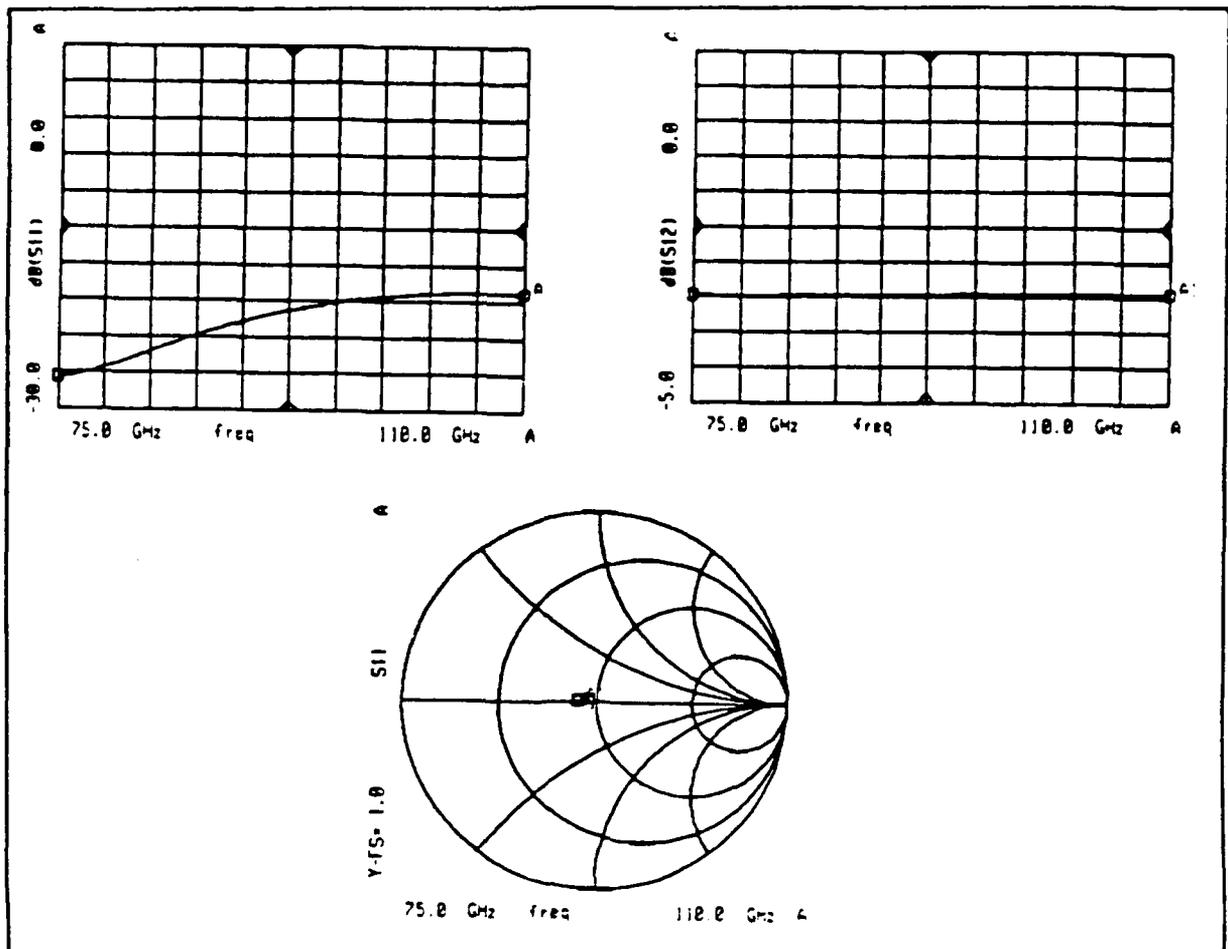


Figure 23. Three-diode attenuator characteristics with  $7 \mu\text{A}$  of bias current where  $R=500 \Omega$ ,  $L=0.02 \text{ nH}$ . Forward-biased optimized spacings are  $M_1=M_2=20.6 \text{ mils}$ .

forward, and a Fortran program has been developed at NIST to determine the length and the gap width of each of the  $N$  short fin line transmission line sections.

MDS simulations for a 300 mil long taper are shown in Figs. 25-29 for  $N=6, 10, 16, 20$ , and 25 sections. As can be seen from the return and insertion loss data, convergence in the results can be seen in the  $N=16, 20$ , and 25 plots. 25 sections are more than adequate in order to simulate this 300 mil linear taper. Now there is no clear rule of thumb on determining the required number of sections in order to simulate a taper, so one should simply increase the number of sections until convergence is observed. Whether or not this approach is accurate will be determined by comparing these results with those of a more accurate full-wave simulator.

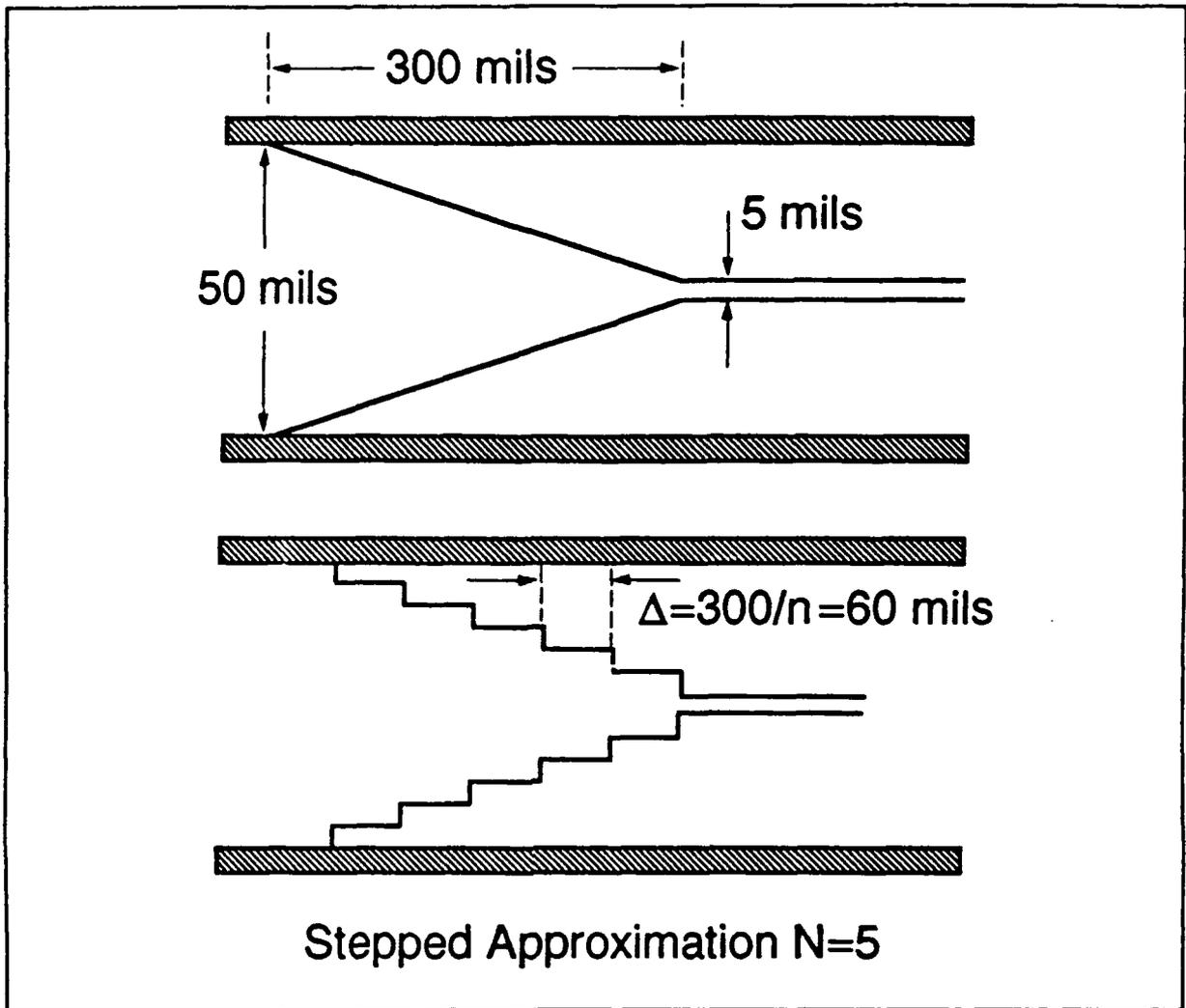


Figure 24. A 300 mil waveguide to fin line linear taper.

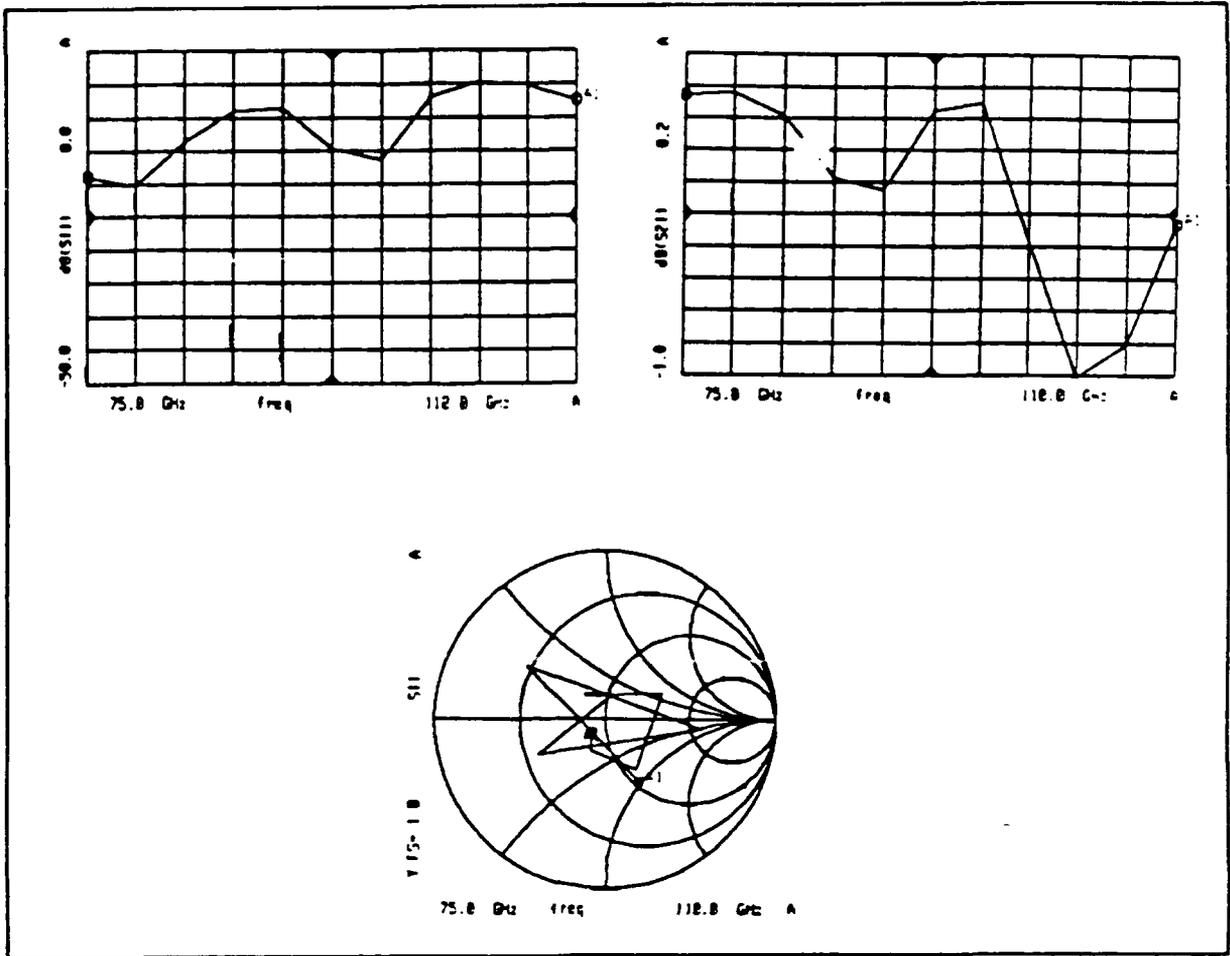


Figure 25. Simulation of a 300 mil long linear taper using N=6 sections.

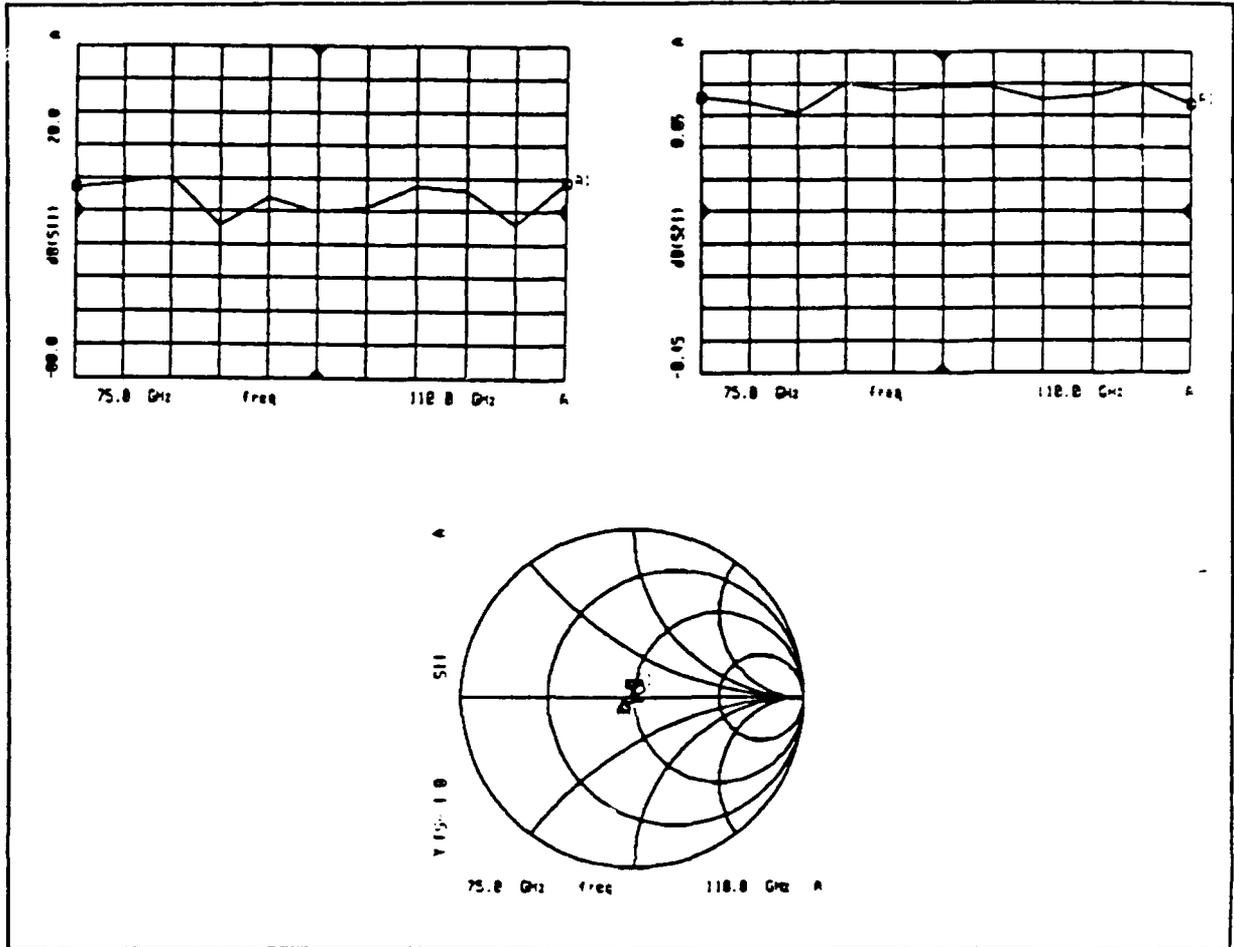


Figure 26. Simulation of a 300 mil long linear taper using  $N=10$  sections.

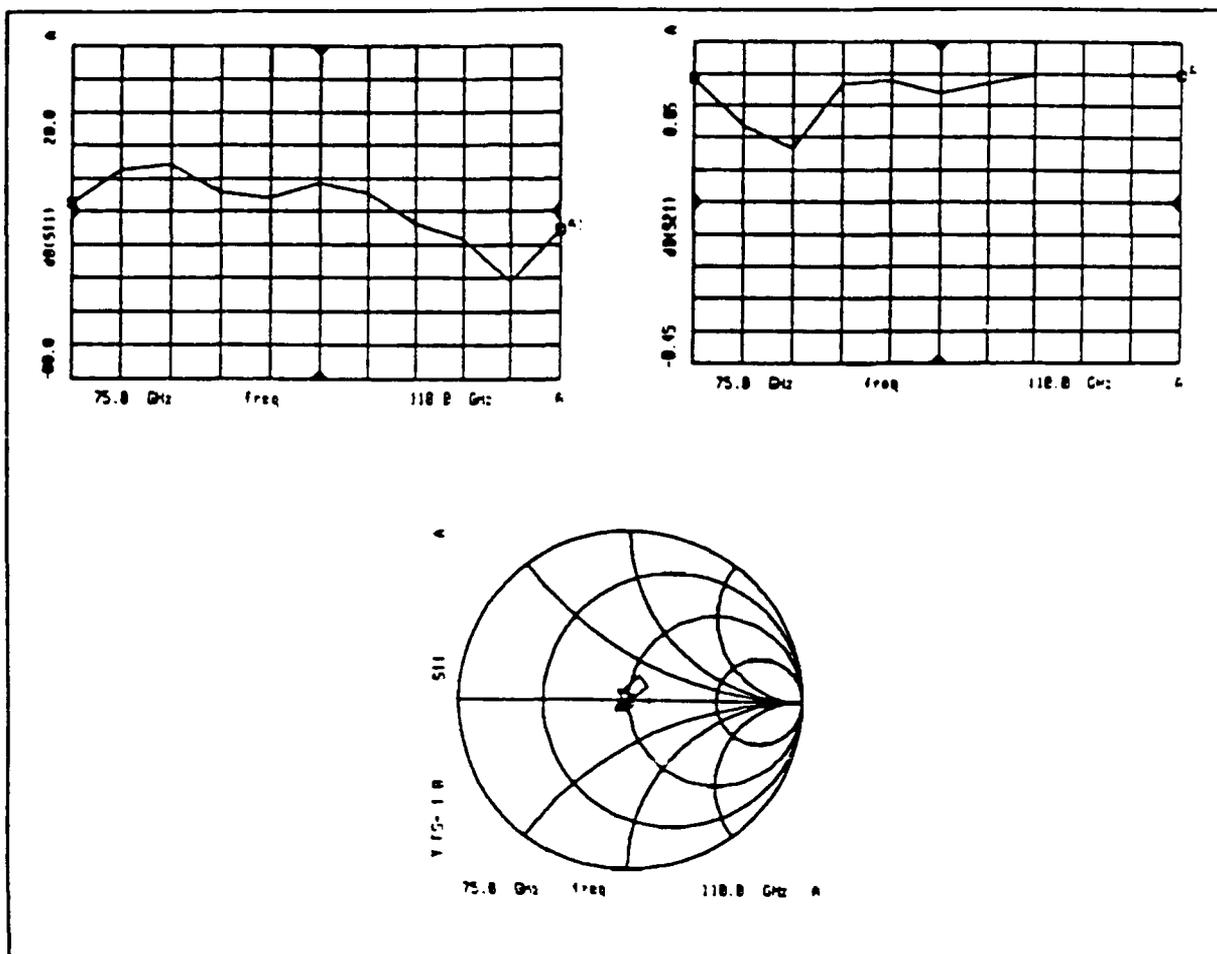


Figure 27. Simulation of a 300 mil long linear taper using N=16 sections.

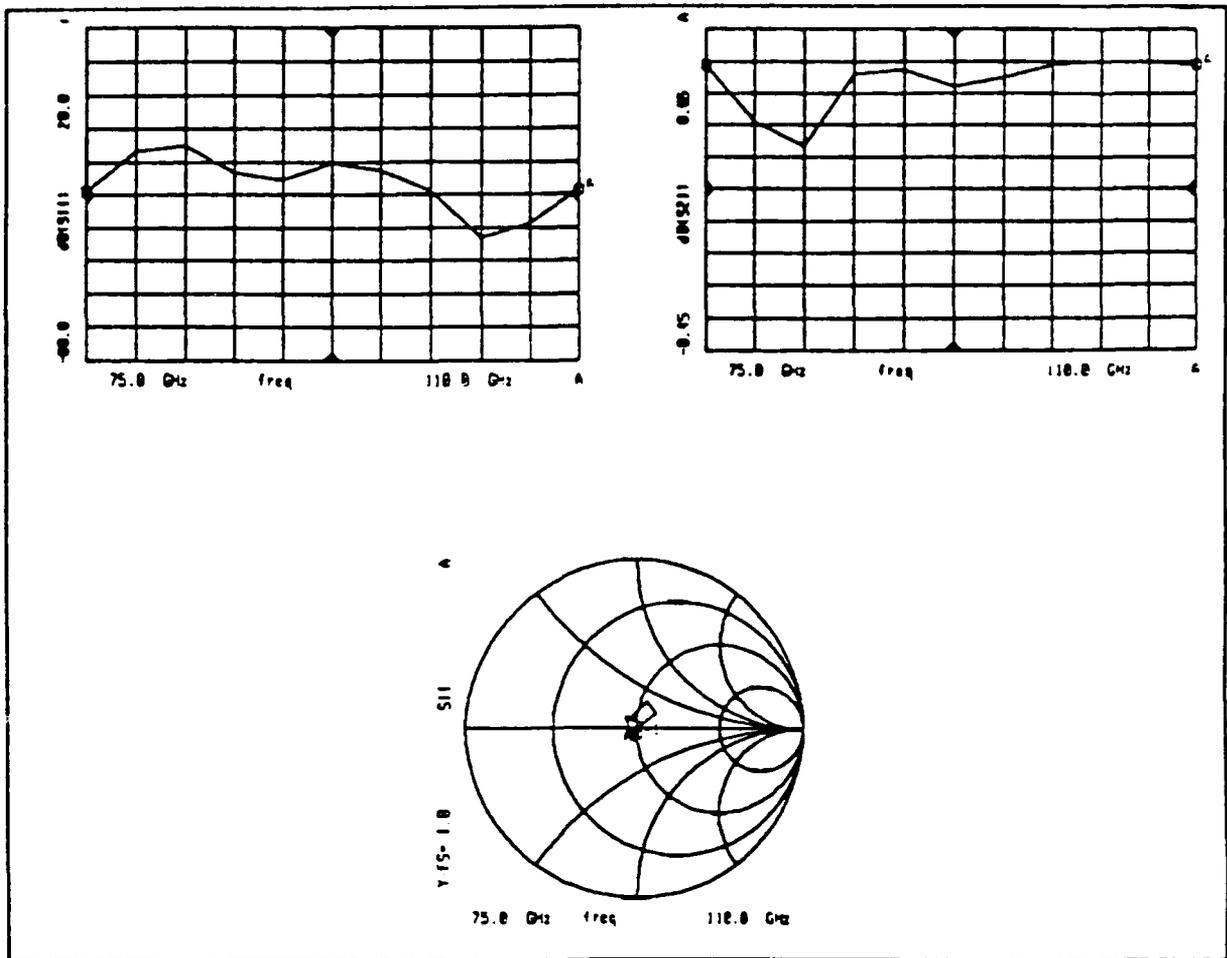


Figure 28. Simulation of a 300 mil long linear taper using N=20 sections.

## CONCLUSIONS

The MDS results have revealed much useful information about the design of a fin line attenuator with shunt-connected PIN diodes. First, if the diode parameters are accurate and the modeling procedure is correct, one of the most useful insights of the MDS analysis is to operate the attenuator with the PIN diodes always in the forward biased mode. If the diode spacings are optimized in the forward biased mode, operating the attenuator in this fashion can yield good impedance bandwidths as well as very flat insertion loss characteristics. Due to the significant reactive loading of reverse-biased PIN diodes, neither flat insertion loss characteristics nor good impedance bandwidths can be achieved by either zero or back biasing the PIN diodes. As the forward biased results indicate, excellent attenuator characteristics for 2, 3, and 4 diode configurations can be achieved by optimizing the diode characteristics with respect to the sum of the magnitudes of the

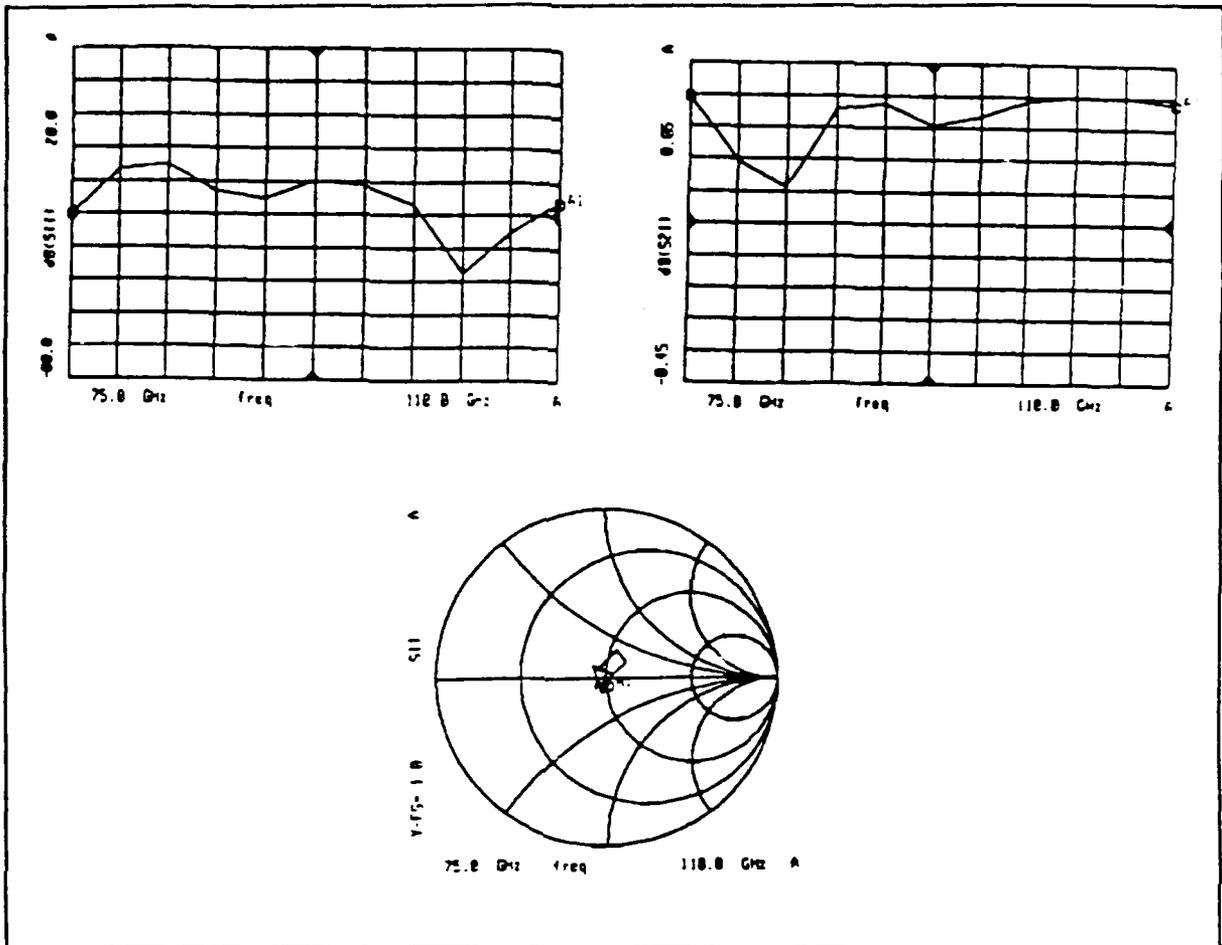


Figure 29. Simulation of a 300 mil long linear taper using  $N=25$  sections.

port reflection coefficients. Markedly inferior results are generated by using reverse-biased optimized diode spacings. Thus it will be necessary to operate the variable attenuator with the diodes forward biased in order to either achieve or approach the required attenuator specifications. The results also show that the diode spacings must not be too large in order to maintain the required bandwidths. Now closely spaced diodes limit the maximum achievable attenuation, due to the generation of fringe fields in the neighborhood of the PIN diodes. If higher maximum attenuation levels are desired, the diode spacings must be increased in order to reduce the effects of the fringe fields which reduces the bandwidth. This tradeoff between bandwidth and maximum achievable attenuation will have to be investigated further. It is also interesting to see that the effects of a linear taper can be simulated using a cascaded series of transmission lines. Although this approach ignores the reactive effects due to the taper, at least some of the loading effects of a finite length taper can be accounted for using MDS. If a more accurate characterization is

required, then it will be necessary to simulate the taper using full-wave techniques.