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A ROBOTIC TACTILE SENSOR INCORPORATING
SILICON PLANAR TECHNOLOGY, A
PIEZOELECTRIC POLYVINYLIDENE FLUORIDE
FILM, AND ON-CHIP SIGNAL PROCESSING

THESIS

Robert C. Fitch, Jr., Captain, USAF

AFIT/GE/ENG/90D-21

DEPARTMENT OF THE AIR FORCE

AIR UNIVERSITY

AIR FORCE INSTITUTE OF TECHNOLOGY

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This research effort pursued the design, fabrication, and test of a robotic tactile sensor. The VLSI integrated circuit (IC) portion of the sensor included a 7 x 7 array of metal electrodes which were individually connected to identical MOSFET amplifiers. A 25 μm thick patch (6 mm x 6 mm) of piezoelectric polyvinylidene fluoride (PVDF) film was attached to the array with a non-conductive adhesive, thereby creating an array of taxels. Charge, generated by the PVDF film, was detected by the amplifiers. The outputs of these amplifiers were connected to on-chip signal processing circuitry designed to produce a single stream of serial data. A problem with the signal processing circuit circumvented the proper operation of the entire IC. Therefore, an external multiplexer was used to analyze the performance of a 3 x 3 array of taxels located in the center of the 7 x 7 array. The key factor affecting the performance of the sensor was establishing a uniform initial charge state condition across the 3 x 3 array. Schemes for manifesting this condition were examined as well as characterization of taxel load response. A fundamental image recognition process successfully recognized an applied shape by comparing the pre-load, load, and post-load multiplexed output of the array.

Piezoelectric Materials Piezoelectric Transducers
Tactile Sensing Robotic Sensors   161
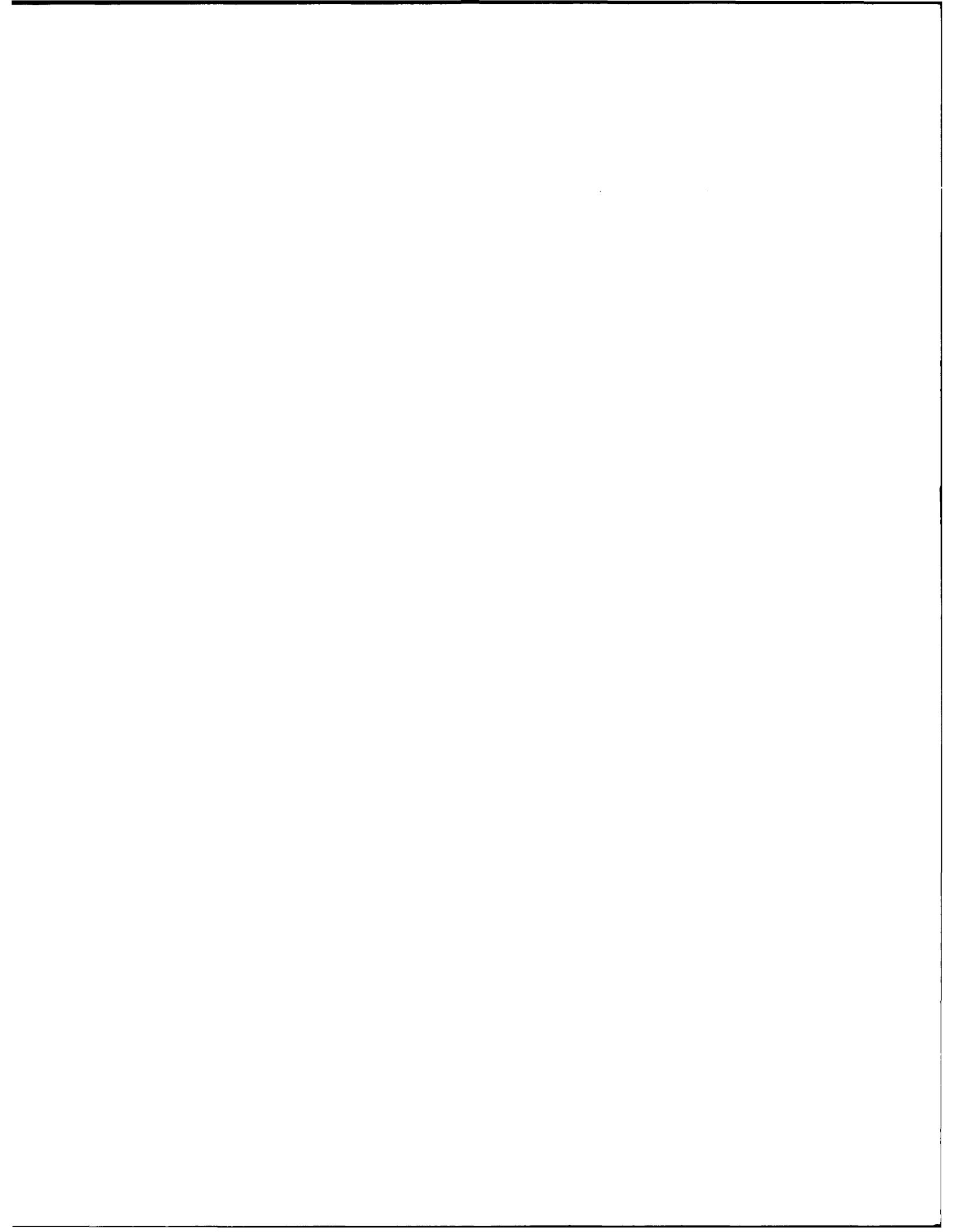
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THESIS

Presented to the Faculty of the School of Engineering

of the Air Force Institute of Technology

Air University

In Partial Fulfillment of the

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Master of Science in Electrical Engineering

Robert Carl Fitch, Jr., B.S.

Captain, USAF

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Abstract

This research effort pursued the design, fabrication, and test of a robotic tactile sensor. The VLSI design tools SPICE, MAGIC, and ESIM were used to design the integrated circuit (IC) portion of the sensor. The IC included a 7 x 7 array of metal electrodes (each measuring 400 μm by 400 μm) which were individually connected to identical MOSFET amplifiers. A 25 μm thick patch (6 mm x 6 mm) of piezoelectric polyvinylidene fluoride (PVDF) film was attached to the array with a non-conductive adhesive, thereby creating an array of taxels (force transducing sites). Charge, generated by a taxel load, was detected by the MOSFET amplifiers. The outputs of these amplifiers were connected to on-chip signal processing circuitry (a 49-channel analog multiplexer clocked by a 555-timer) designed to produce a single stream of serial data emanating from one pin on the IC package.

A problem with the signal processing circuit circumvented the proper operation of the entire IC. Therefore, an external multiplexer was used to analyze the performance of a 3 x 3 array of taxels located in the center of the 7 x 7 array.

The key factor affecting the performance of the sensor was establishing a uniform initial charge state condition across the 3 x 3 array. Schemes for manifesting this condi-

tion were examined as well as characterization of the tax-

els' load response. A fundamental image recognition process

was evaluated. This process successfully recognized an

applied shape by comparing the pre-load, load, and post-load

multiplexed output of the array to verify which taxels were

activated by the load.

A ROBOTIC TACTILE SENSOR INCORPORATING SILICON PLANAR TECHNOLOGY, A PIEZOELECTRIC POLYVINYLIDENE FLUORIDE FILM, AND ON-CHIP SIGNAL PROCESSING

I. Introduction

Background

Presently, several research centers in the United States and around the world are attempting to develop tactile imaging technology that will render robots a sense of touch. This 'intelligence' will be gathered by the robot with a tactile sensor. If the tactile sensors are mounted, for example, on the robot's fingertips, then force feedback from the sensors will indicate how tightly an object has been grasped. Additionally, these sensors, which are composed of a two-dimensional array of closely spaced force sensing elements, should be capable of fundamental image sensing, thus rendering a robot with the ability to identify the shape of an object in its grasp.

The principle of tactile sensing utilized in this research is based on the deformation of a planar piezoelectric polymer material while under an applied stress. A pure force sensor typically utilizes a piezoresistive or piezoelectric material where the applied force is proportional to the change in resistance or the voltage potential generated by charge produced in the

material, respectively (Regtien, 1989:92). Other force sensors incorporate optical, ultrasonic, magnetic, mechanical displacement, or capacitive means to measure the deformation of the material (Harmon, 1982:5-17). The piezoelectric tactile sensor developed in this effort was a continuation of the previous theses accomplished by Captains David Pirolo, Rocky Reston, and Douglas Ford (Pirolo, 1987; Reston, 1988; Ford, 1988).

A fundamental cross-sectional view of the tactile sensor is shown in Figure 1-1. The piezoelectric thin film material, polyvinylidene fluoride (PVDF), is bonded to an array of metal electrodes. The entire array measures 5.2 mm by 5.2 mm; however, only a small section of the array is shown in the diagram. The silicon integrated circuit is the harbinger of the electrode array, charge signal amplifiers, and signal processing circuitry. Charge generated by the stressed polymer is accumulated by the metal electrodes; this small voltage is then amplified by the MOSFET amplifiers which are connected to each of the lower electrodes via a metal-1 line (Reston, 1988:3-4). The metal-1 conductor is isolated from the PVDF film with a dielectric passivation layer of silicon dioxide (SiO_2).

Problem Statement

A multiplexed, piezoelectric tactile sensor will be designed, fabricated, and characterized with respect to its ability to detect the magnitude and shape of an applied
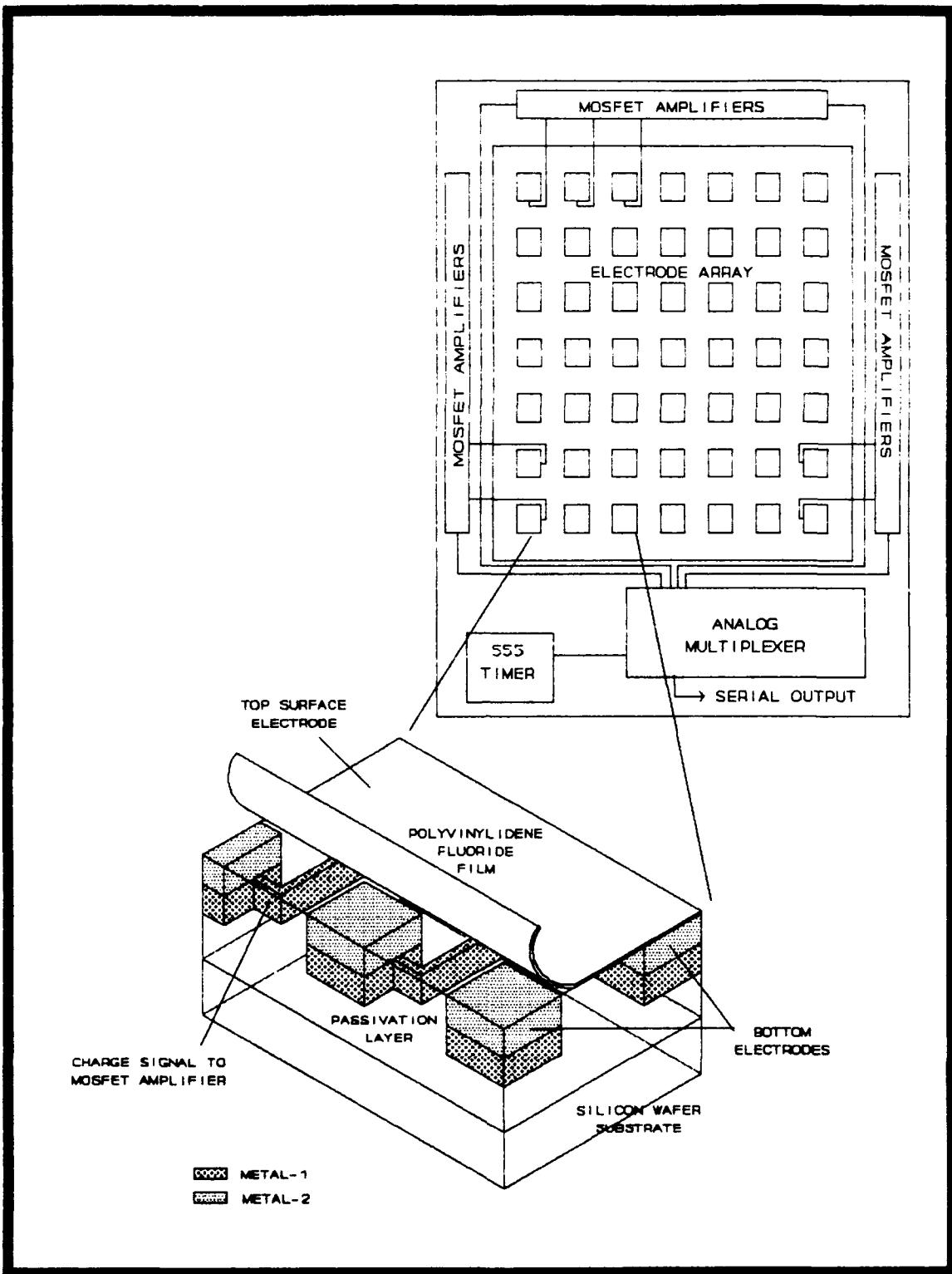
Figure 1-1. Cross-sectional view of the indicated portion of the tactile sensor's electrode array.

load. A 25 μm thick piece of polyvinylidene fluoride film
will act as the charge generating polymer which will be
attached (via an adhesive) to the aluminum electrode array
in the silicon integrated circuit.

Scope of the Effort

This research effort will focus on the following
critical areas:

Electrode Array Initial Bias State. Previous efforts
have revealed that biasing the input electrodes which are
coupled to the charge amplifiers is a difficult problem
(Ford, 1988:VI-3). Nevertheless, this bias is critical for
establishing a homogeneous charge state initial condition
throughout the two-dimensional array of the sensing
elements. Any existing stress in the PVDF film due to its
adherence to the array structure or a prior loading
condition may cause the pre-loading initial condition
potential among the electrodes to differ. This variance
must be minimized by properly biasing each amplifier to
establish a linear and time-invariant DC operating point.

Modular Design Concept. The overall size of the
integrated circuit (IC) will be confined to an area
measuring 7.9 mm by 9.2 mm. The design of the tactile
sensor IC will include signal processing components which
can be isolated from the charge signal amplifier circuitry,
should the signal processing circuitry prove to be
disfunctional. The option for external processing of the

charge signals will also be included.

Film Adhesion Evaluation. Epoxy, acrylic-, urethane-, and silicon-based liquids used to conformally passivate printed circuit boards will be evaluated as potential PVDF film adhesives. The ability of these adhesives to couple charge to the MOSFET gate electrodes and to establish a robust mechanical bond to the electrode array will be evaluated.

Assumptions

The following assumptions will be made as a baseline for this research effort:

(1) The 25 μm thick PVDF film will isolate and minimize crosstalk between nearest neighbor electrodes. Any existing crosstalk due to the fringing field or leakage current between electrodes will be quantified experimentally to determine its effect on the sensor's performance.

(2) The adhesive which bonds the PVDF film to the array will have electrical characteristics that do not compromise the charge generating properties of the PVDF film. That is, the film will generate a sufficient quantity of charge which can be detected by the charge signal amplifiers.

(3) The 132-pin ICs fabricated by MOSIS will function according to the SPICE and ESIM analyses performed during the IC design process.

(4) The test fixture, fabricated by the AFIT model

shop, will be capable of applying test loads with various shapes ranging in weight from 1 gram to 100 grams. The contacting planar surface of each load shape will form a uniform interface with the IC array at their initial contact and throughout the full application of the test load.

Approach

The approach will include the design of the integrated circuit, the fabrication of the tactile sensor, and the performance evaluation of the circuit and the sensor, independently.

The integrated circuit will be designed using the VLSI (Very-Large-Scale Integrated Circuit) CAD (Computer Aided Design) tools MAGIC, ESIM, and SPICE. The die size of the integrated circuit will be limited to an area measuring 7.9 mm by 9.2 mm. The major portion of the IC will consist of a 7 by 7 array of equally spaced and sized electrodes surrounded by charge signal amplifiers. The remaining space will be reserved for the signal processing circuitry.

The Metal-Oxide Semiconductor Implementation Service (MOSIS) will fabricate the integrated circuit. Upon receipt, the finished ICs will be tested in the Cooperative Electronics and Materials Processing Laboratory. Once proper operation of the ICs is established, the tactile sensors will be fabricated by attaching the PVDF film to the electrode array. Tactile sensor performance tests will then follow.

Order of Presentation

Chapter II examines robotic tactile sensing, its relationship to human tactile sensing, and some of the methods being investigated to accomplish transduction. The salient characteristics of piezoelectric polyvinylidene fluoride film, its production, and a model for its piezoelectric activity are discussed in Chapter III. Chapter IV describes the integrated circuit design methodology and tactile sensor fabrication procedures. The performance evaluation of the integrated circuit and the fabricated tactile sensor are described in Chapter V. The results and analysis of the test data are also discussed in Chapter V. Chapter VI concludes the significant findings of this research effort and makes recommendations for follow-on research. The Appendices include lists of materials and equipment used in this thesis effort, as well as supplementary data and graphs obtained during the performance evaluation of the sensor.

II. Robotic Tactile Sensors

Introduction

Research efforts concerning robotic tactile sensor development are attempting to provide robots with a level of intelligence that will ultimately allow them to manipulate and identify objects in their grasp. The advancement of robotic systems critically depends upon the successful realization of a tactile sensor capability and its integration with the existing complicated robotic control systems. The "Air Force Studies Board 1989 Report on Advanced Robotics for Air Force Operations" clearly states the need for research and development in the areas of image, force, and position sensing for robotic systems (Air Force Studies Board National Research Council, 1989:1). Future Air Force robotic applications, such as aircraft flight line maintenance, will require robots to possess a high degree of flexibility and manual dexterity, only achievable through the integration of robotic tactile sensors.

This chapter examines the tactile sensing capabilities of the human skin to establish a baseline for the anticipated robotic tactile sensor features. Also discussed are the desirable characteristics of robotic tactile sensors and the promising solutions being researched to achieve these capabilities.

Background

Tactile Sensor Definition. A tactile sensor consists of elementary force sensors (or taxels) densely arrayed in one or two dimensions and is capable of image sensing through the simultaneous determination of a contacting object's force distribution and position measurements (Regtien, 1989:94). The ideal robotic tactile sensor has been described by Professor Leon D. Harmon as a teachable, not completely preprogrammed, "black-box" package, capable of 3-dimensional pattern recognition independent of its position and orientation (Harmon, 1982:3-5). Today's most advanced tactile sensor's performance falls far short of this ideal, but research efforts are on-going to more closely emulate the ideal tactile sensing capabilities of the human skin.

Human Skin Tactile Sensing Capability. Touch is one of the five basic human senses, and the skin utilizes nine different touch sensors. Each sensor responds to a particular external stimuli, such as heat or pressure. These sensors are located within the three layers of skin: the outermost layer, or epidermis; the dermis; and the innermost layer, or hypodermis.

Contained within these layers are the nine types of touch receptors: free nerve endings, Merkel's discs, Ruffini end-organs, Meissner's corpuscles, Pacinian corpuscles, Krause's corpuscles, hair end-organs (tactile hair), Golgi
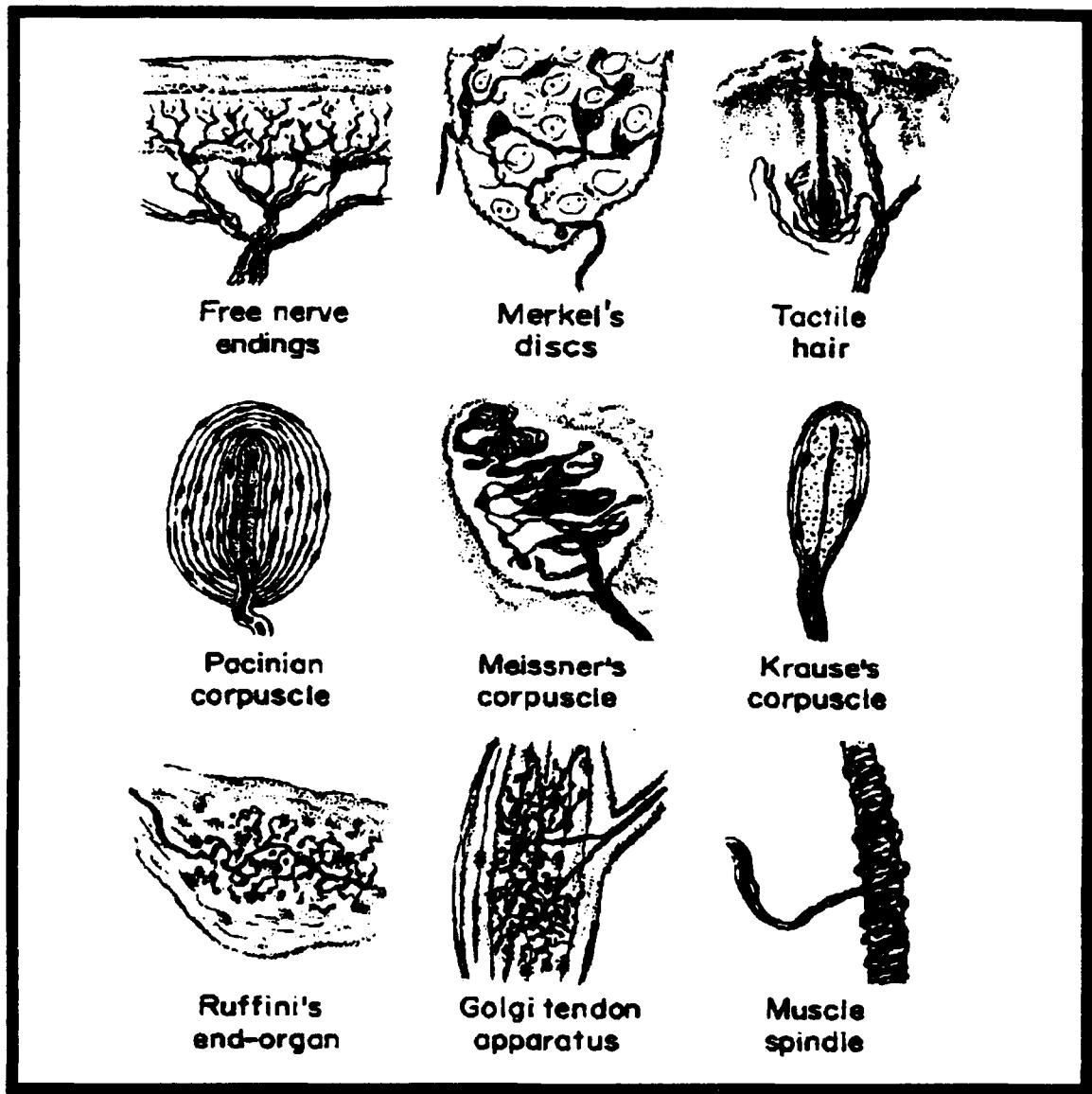
Figure 2-1. Sensory nerve endings of the human skin
(Guyton, 1976:641).

tendon apparatus, and muscle spindle (Yardley and Baker,

1986:48; Guyton, 1976:641). Each of these somatic sensory

nerve endings is shown in Figure 2-1.

These sensors are capable of sensing six tactile

sensory modalities: simple touch, normal and shear force,

contact force distribution, slip, heat flow, and vibration

(Kynar, 1984:79-80). The action of the human hand grasping
a golf ball and placing it on a tee represents a typical
example of sensor utilization.

The thumb and fingers of the hand, once in close
proximity to the golf ball, will make the initial contact.
Minimal deformation of the skin occurs, and the free nerve-
endings in the outer epidermal layer detect simple touch and
slip. The free-nerve endings detect heat flow to and from
the object (Yardley and Baker, 1986:48).

As the hand exerts more force, the skin begins to
conform to the shape of the ball. The Merkel discs, which
lie deep within the epidermis, begin to detect the small
ridges (textural detail) on the object's surface.
Compliance of the skin allows the hand to grasp the ball.
The Ruffini end-organs facilitate the sensation of continual
deformation of the skin while the Meissner's corpuscles
detect the finer ridges and bumps on the object. The hand
discovers, through the Pacinian corpuscles, that level of
the minimal normal or shear force which is required to pick-
up the golf ball (Yardley, 1986:48; Guyton, 1976:640-642).

The spatial resolution of the indentations on the
golf ball are detected by Meissner's corpuscles, which can
detect and spatially resolve features on the order of 1 mm.
Many interconnections exist between these corpuscles through
which sensor signals are processed before going to the brain
(Yardley and Baker, 1986:48).

The ability to sense vibration, which is a measure of

the rate of change of establishing contact with an object, gives the hand an added advantage in determining the object's identity. Finally, the Pacinian corpuscles detect the low-level induced vibration as the ball slips from the fingertips and is eased onto the tee (Yardley and Baker, 1986:48). As illustrated in this example, much of human tactile sensing involves the active manipulation of an object, and not just simple touch.

The complex interconnections, specific locations, and multiple responses of the skin's touch receptors all combine to give human skin the ability to sense an object's shape, texture, and temperature (Guyton, 1976:640-642). Incorporation of these touch receptors and modalities into a robotic tactile sensor is the logical approach being pursued by most researchers to provide robots with a complete tactile sensing capability.

Robotic Tactile Sensors

Robotic tactile sensors are termed exteroceptive because they provide the robot with information about its environment (Regtien, 1989:92). The three classes of exteroceptive sensors are binary, scalar, and image, of which robotic tactile sensors belong to the latter category (Regtien, 1989:92). Binary sensors are event detectors or safety devices, such as reed switches. Scalar sensors acquire metric information such as force or thermal properties. Image sensors are capable of determining the

shape of 1, 2 or 3-dimensional objects (Regtien, 1989:92-94).

Robots may utilize tactile sensors either passively or actively. In the passive sensing mode, the object is presented to a larger, fixed sensor, such as a platform. The active sensing mode involves probing an object with a sensor that is smaller than the object (Yardley and Baker, 1986:52).

Requirements of Robotic Tactile Sensors. The following requirements for robotic tactile sensors parallel the functional capabilities of the human hand (Barth, 1986:18; Pennywitt, 1986:182-184; Nicholls and Lee, 1989:4-5):

1. The sensor will be composed of an array of 50 to 200 sensor elements spaced approximately 1 mm center-to-center.

2. The sensor will be compliant and conform to a fingertip and the object it contacts.

3. The sensor will have a high dynamic range (that is, it will transduce forces ranging from 1 to 1000 grams which may be applied to each sensing element). Also, forces above 1000 grams, within reason, will not damage the sensor.

4. The sensor will have no hysteresis, high durability, and the ability to sense temperature.

5. The sensor will respond quickly to stimuli (data sampling rates or a bandwidth of approximately 100 Hz) and process this data locally. Ideally, the sensor will produce a somatotopic map which can be transmitted to the robot's

central processor.

6. The sensor will detect shear forces to indicate the degree of slip associated with a grasped object.

7. The sensor will be cost effective.

To date, all of these requirements have not been successfully incorporated in any of the exploratory tactile sensor concepts. However, numerous sensors possessing different capabilities may be utilized on one robot to more closely model the human hand.

Categories of Robotic Tactile Sensors. Tactile sensors can be categorized as either piezoelectric sensors, piezoresistive sensors, optical sensors, or capacitive sensors.

Piezoelectric Tactile Sensors. Piezoelectric tactile sensors rely on detecting the charge produced by a polyvinylidene fluoride (PVDF) thin polymer film caused by an externally applied load. Deformation of the film, which is attached to an array of electrodes, results in charge accumulation at the electrodes. The amount of charge generated varies linearly with the film's deformation over a limited range. Electronic circuitry is typically used to measure and process the quantity of charge at each electrode. The signals generated by this circuitry are used to produce three-dimensional plots which represent the shape of an object causing the film deformation.

Figure 2-2 illustrates a tactile sensor which detects the charge generated by two layers of PVDF film. Although
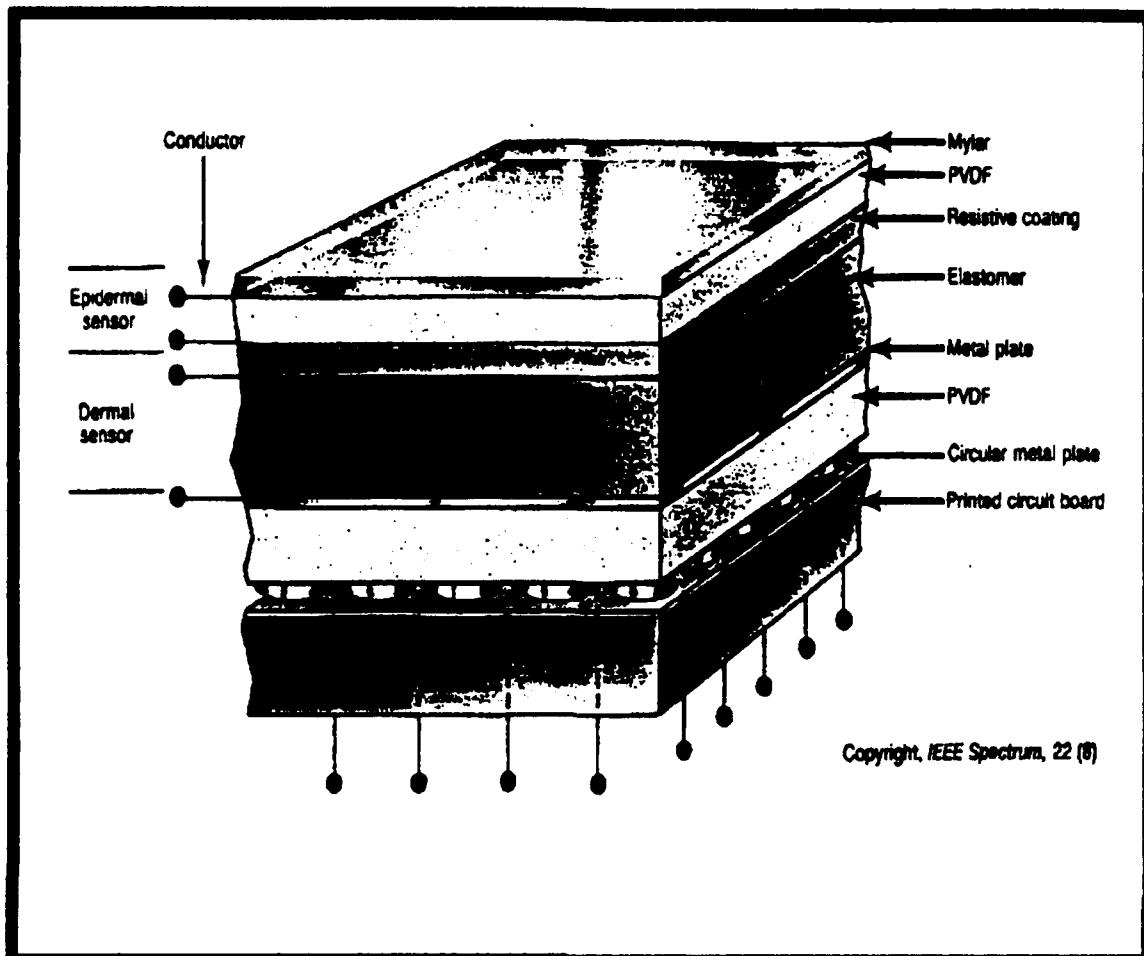
Figure 2-2. PVDF tactile sensor developed at the University of Pisa (Pennywitt, 1986:200).

this design is mounted on a printed circuit board, monolithic silicon integrated circuit technology is often used to provide a solid platform for the sensor array and the signal processing circuitry (Pennywitt, 1986:196-200).

Advantages of piezoelectric tactile sensors include high durability and conformity, excellent linearity, low hysteresis, good resolution (less than 1 mm), and high dynamic range (4000:1) (Pennywitt, 1986:185; Nicholls and Lee, 1989:19). A disadvantage with the design is its

susceptibility to electromagnetic interference. Also row-column scanning circuitry designed to collect the charge generated by individual taxels is very difficult to implement, and charge dissipation inhibits the static response of the sensor (Pennywitt, 1986:185).

Piezoresistive Tactile Sensors. Piezoresistive tactile sensors are similar to strain gauges which use conductive elastomers. A resistive sensor which images dental occlusions is shown in Figure 2-3. The overlapping rows and columns of conductors are made from conductive ink which is screen printed on a Mylar substrate. Force exerted by teeth clamping onto the grid will cause the contact area between the underlying rows and columns to increase, thereby decreasing the resistance (Podolff, 1989:41-47).

External row and column scanning circuitry detects the changes in resistance at the row and column contact points. These data points are processed by a computer which generates a 3-dimensional display of the dental occlusion (Podolff, 1989:44).

Piezoresistive sensors can detect static forces, but generally have significant hysteresis and are nonlinear. Force sensitivity as small as 5 grams and a spatial resolution of 0.6 mm has been achieved; however, dynamic range (1 to 100 grams) is sacrificed for the high sensitivity (Pennywitt, 1986:185).

Optical Tactile Sensors. Optical tactile sensors modulate light in response to the deformation of optical
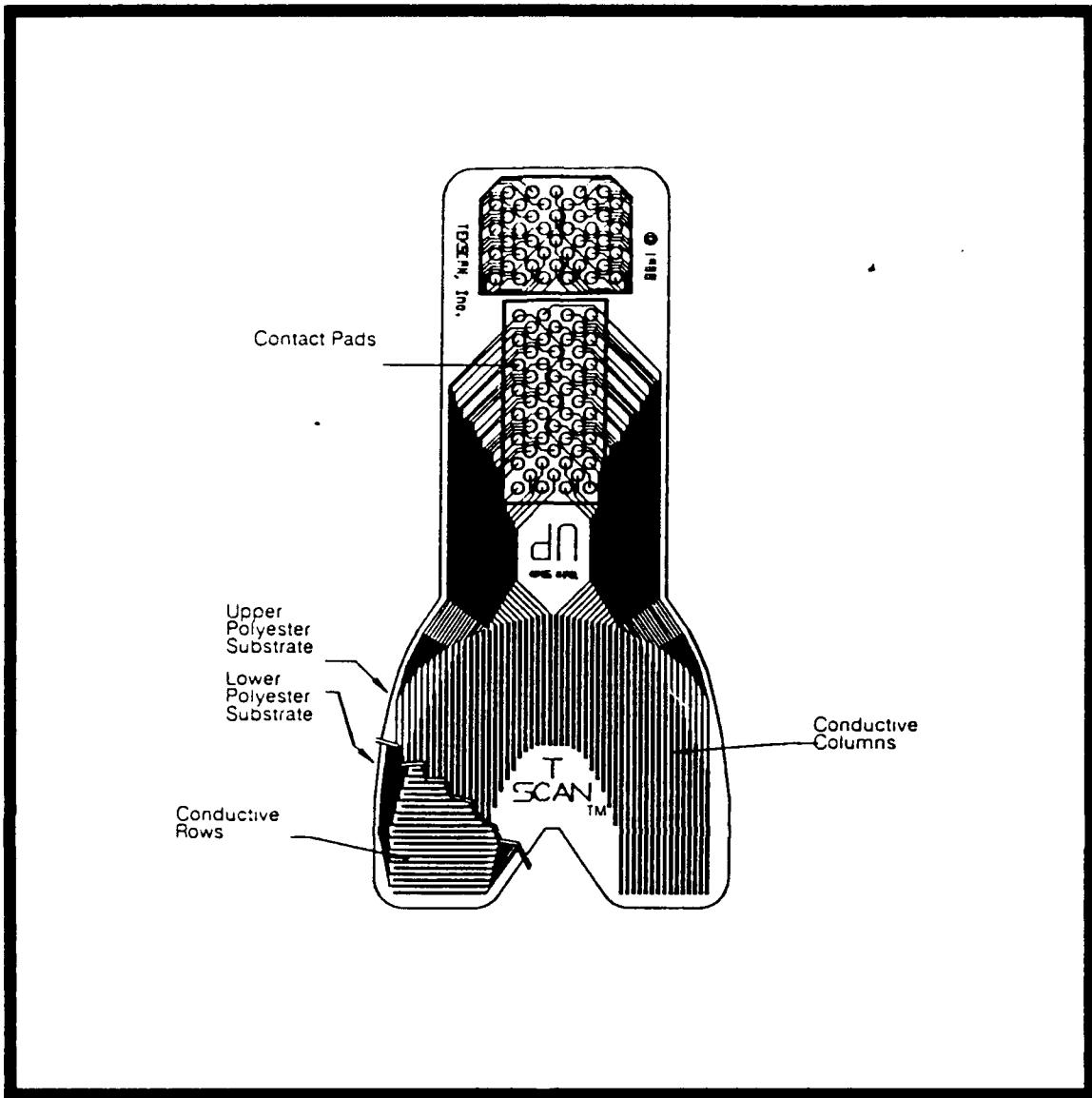
Figure 2-3. Resistive tactile sensor which images dental
occlusions (Podolff, 1989:42).

fibers or elastomeric material. A recently developed

sensor, shown in Figure 2-4, utilizes four overlapping

layers of fiber optic cables. When compressed, microbends

in the fibers modulate the internal propagating light which

is detected by diode photodetectors (Jenstrom, 1989:239-

240).
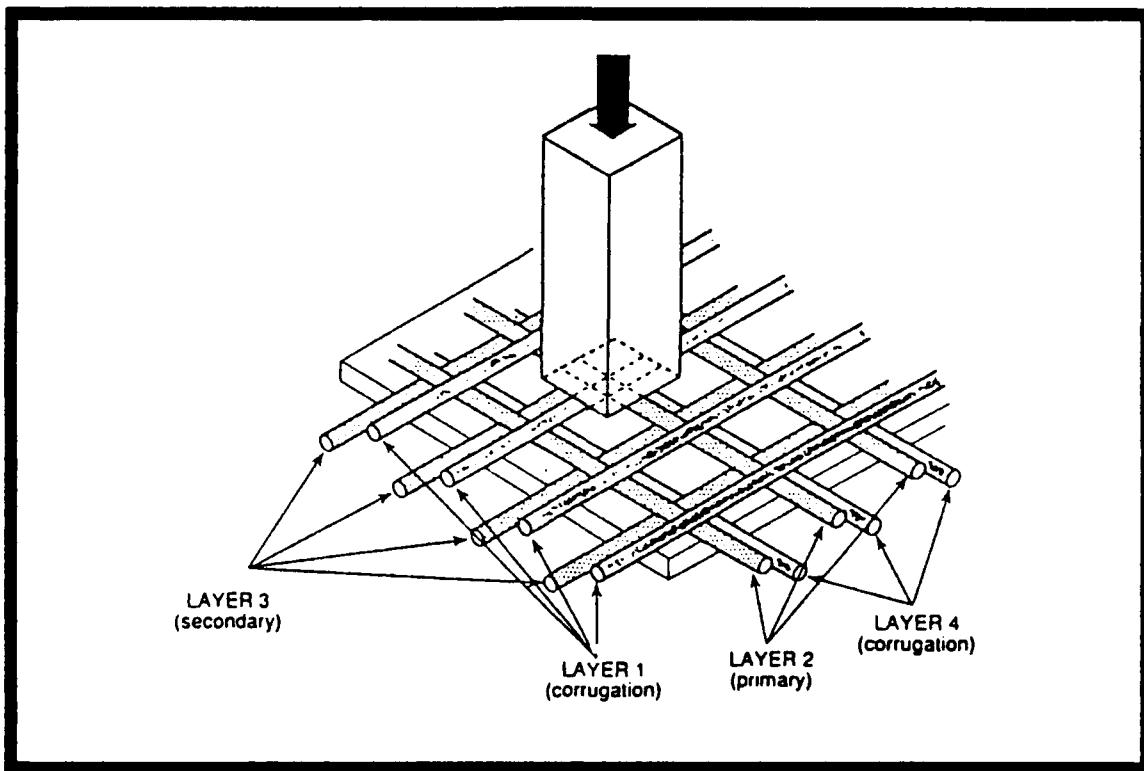
Figure 2-4.   Fiber optic cables arrayed in an optical
tactile sensor (Jenstrom, 1989:240).

        This sensor has a force resolution of 0.2 grams with a

spatial resolution of 2 mm.   The load range for the sensor

is 5 grams to 400 grams, and its bandwidth 250 Hz.   Optical

tactile sensors generally possess acceptable spatial

resolution, low hysteresis, and are virtually immune to

electromagnetic interference (Pennywitt, 1986:185).   Spatial

resolution is limited by the diameter of the optical fibers.

        Capacitive Tactile Sensors.   Capacitive tactile

sensors employ force sensing capacitors to detect applied

loads.   These sensors provide high sensitivity and excellent

spatial resolution.   One imaging cell in a 32 x 32 element

capacitive tactile sensor is shown in Figure 2-5.   Its
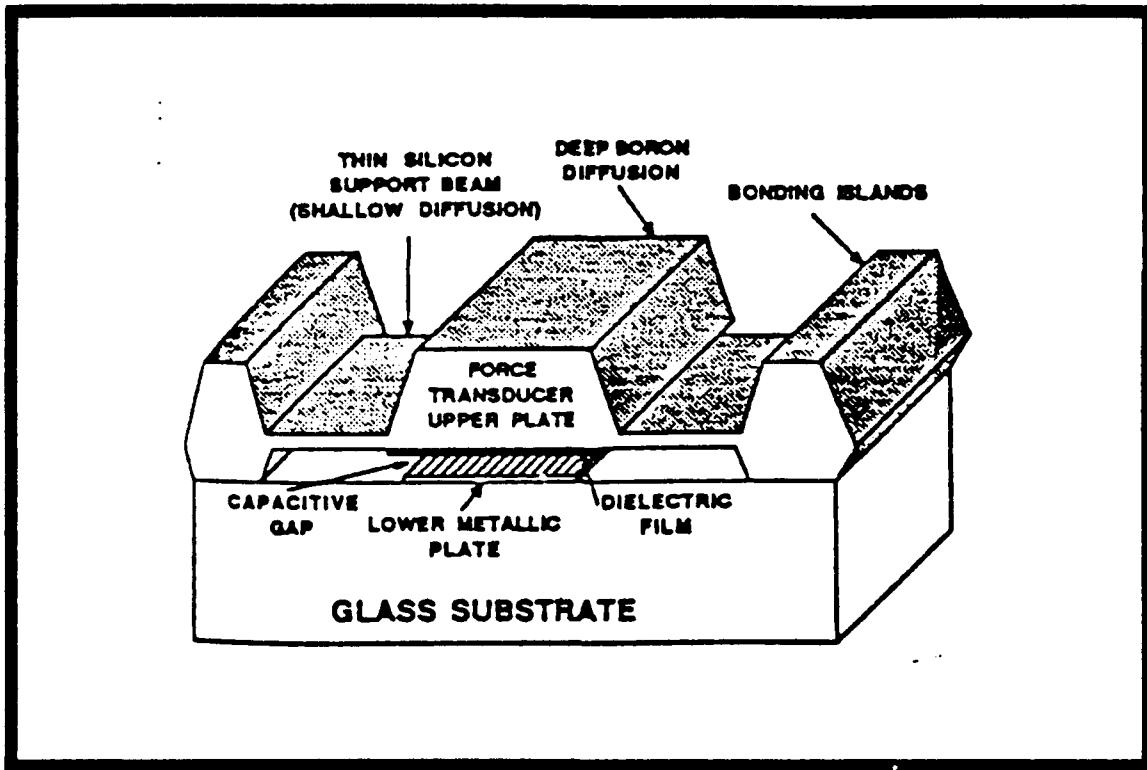
Figure 2-5. Capacitive tactile sensor's imaging cell (Suzuki, 1988:675).

sensitivity is 0.45 pF/gram with a maximum load of 1 gram. Signal processing of the data from these elements is similar to the technique utilized with piezoelectric tactile sensors. The device has negligible hysteresis due to the small capacitance of each cell, but it offers no conformality with an object that is contacted (Suzuki, 1988:674-677).

Conclusion

The challenge remains to incorporate the versatility of human tactile sensing modalities into a unified tactile sensing system. This system should possess high spatial

resolution (taxel spacing of 1 mm center-to-center), high
bandwidth (at least 100 Hz), a wide dynamic range (1 to 1000
grams), and no hysteresis. Since minimal energy should flow
out of the system being measured, the sensor should be
several times more compliant than a contacting object.
Energy is force times displacement; therefore, the sensor
should also be of sufficient stiffness to avoid displacement
of the sensor's surface. High durability is the final
requirement which is essential for a robot performing in a
harsh industrial setting. Presently, the specific
application dictates the type of sensor chosen for the task,
but with continued research, the universal tactile sensor
will be achieved.

III. Polyvinylidene Fluoride Film

Polyvinylidene fluoride (PVDF or PVF_2) is a
ferroelectric polymer whose piezoelectric and pyroelectric
effects (both being the strongest of all known polymers
(Lovinger, 1983:1115)) have been exploited in numerous
sensor applications such as high-frequency ultrasonic
transducers, audio frequency transducers, infrared sensors,
and robotic proximity and tactile sensors. PVDF thin films
are physically robust, flexible, lightweight, chemically
resistant to moisture and most contaminants, and readily
shaped and attached to complex morphologies (Kynar, 1983:5).
Its relatively high electrical impedance motivates coupling
this material with the high input impedance afforded by
complementary metal-oxide-semiconductor circuits (Chatigny
and Robb, 1986:52). For these reasons, PVDF film was chosen
as the force transducing medium in this research effort.
Therefore, this chapter examines the piezoelectric effect
and the morphology of PVDF film.

Piezoelectricity in PVDF

In 1969, Kawai discovered that a strong piezoelectric
effect could be induced in PVDF by applying a large direct
current electric field across the film (Kawai, 1969:975).
Eighty-nine years earlier, the Curie brothers had discovered
that piezoelectricity was a fundamental intrinsic property
of many crystals, ceramics, and polymers (Taylor, 1985:3).

For a material to be piezoelectric, it must undergo a change in electrical polarization as it responds to a mechanical stress (Sensors, 1988:20). This phenomenon is called the direct piezoelectric effect. The converse piezoelectric effect results when the piezoelectric material manifests strain in response to an applied electric field (Bottom, 1982:55-56). Of the 32 crystal classes, only the noncentrosymmetric crystal classes exhibiting polarization, some when stressed and others when unstressed, are technically termed piezoelectric (Lovinger, 1983:1115). There are 20 piezoelectric crystal classes (Wang and others, 1988:1).

Ten of the 32 crystal classes are pyroelectric. Electrical polarization is induced in these crystals as their temperature changes (Chatigny and Robb, 1986:50). Bergman *et al* and Wada *et al*, in 1971, independently discovered the pyroelectric effect in polarized PVDF film. Two forms of pyroelectricity exist: primary and secondary pyroelectricity (Kepler and Anderson, 1978:4490). Primary pyroelectricity is the electrical response which results from a change in the film's temperature as the film's volume is held constant. If the film's volume is allowed to change as a result of a temperature change, the resulting electrical response is termed secondary pyroelectricity (Wang and others, 1988:62). This secondary pyroelectric effect results from piezo-electricity. It is important to understand the crystalline structure, orientation, and

production of PVDF to better understand the origins of
piezoelectricity and pyroelectricity in PVDF film.

Morphology of PVDF

Polyvinylidene fluoride forms from the monomer
vinylidene fluoride, $CH_2 = CF_2$, in an addition
polymerization reaction (Wang and others, 1988:9). A
catalyst causes the monomers to link together, thus forming
longchain molecules with large molecular weights,
approximately equal to 10^5 amu, and a repeat unit of 2000
(Sessler, 1981:1596). The chemical reaction initiated by
the catalyst is given by:

$$n[CH_2 = CF_2] \rightarrow - [CH_2CF_2]_n - \quad where\ n > 1000.$$
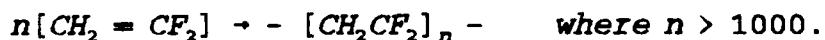
The resulting morphology of the polymer is a direct result
of the polymerization process used (typically a suspension
or emulsion process). Addition polymerization reactions are
classified as gas, liquid, or solid phase depending upon the
phase in which the polymer exists during the reaction. The
most common addition reaction is liquid phase polymerization
(Wang, 1988:10).

Differences in molecular weight, molecular weight
distribution, melting point, percent crystallinity, degree
of regularity, and spherulite size can arise during
polymerization. Melt grown crystals form spherical
aggregates called spherulites (Wang and others, 1988:41).
These entities consist of lamellar crystals which grow
radially outward from the nucleus as shown in Figure 3-1.
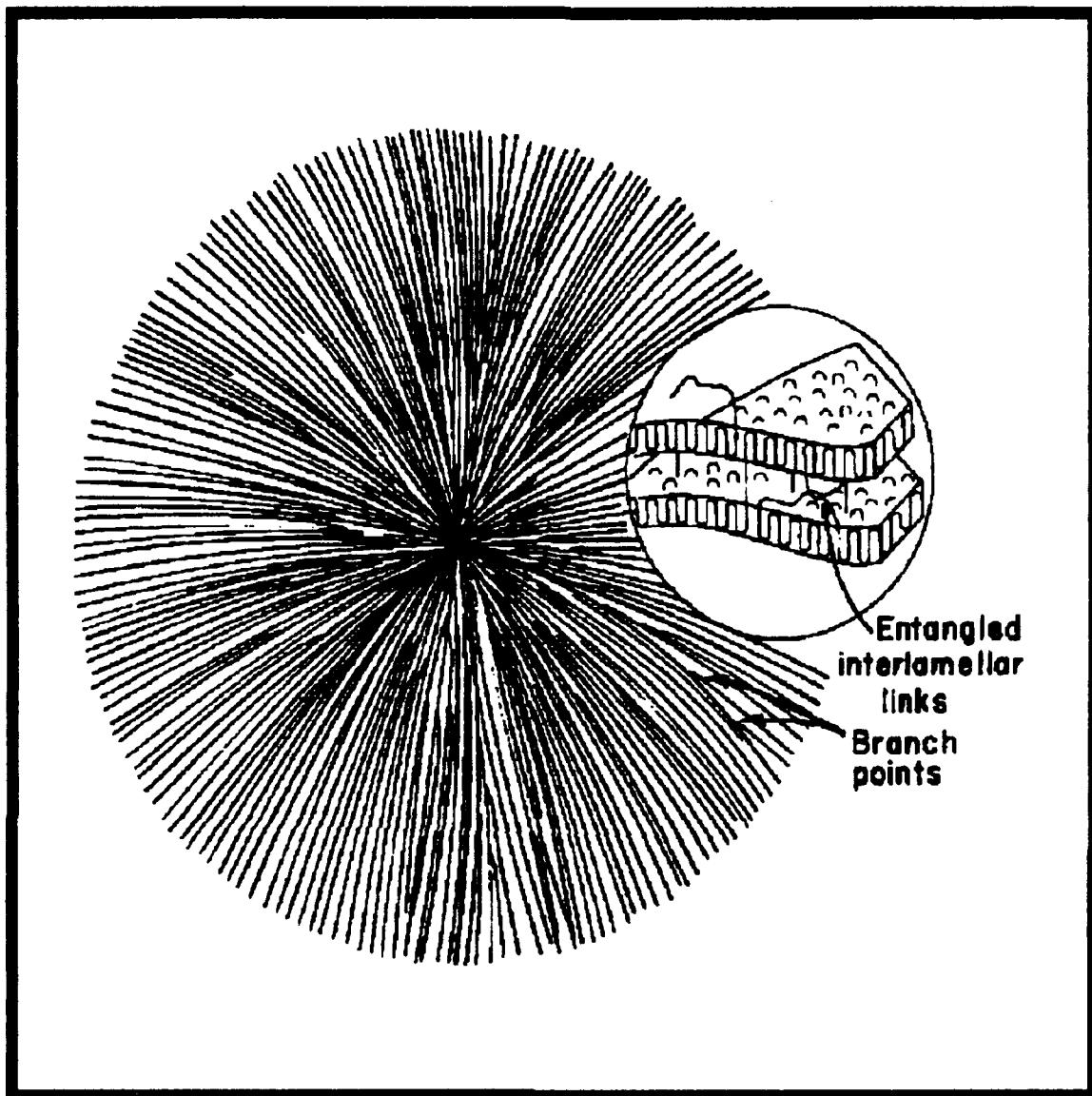
Figure 3-1.   Schematic drawing of the crystalline and
amorphous structures with lamellar crystal growth (Wang,
1988:43).

The crystallographic axis is frequently parallel to the

radius, and the amorphous, non-crystallographic material

between the folded lamellar crystals consists of tie

molecules, cilia, low molecular weight molecules, and

copolymer units (Wang and others, 1988:42-43).   The

amorphous material comprises approximately 50 percent of the total mass of PVDF.

The polymer chain forms various conformations as a result of rotation of the hydrogen or fluorine van der Walls bonds relative to a single carbon bond. The lowest potential energy bond is called the trans or (T) arrangement. The next two higher energy minima are called gauche (G) and gauche prime (G') arrangements (Wang and others, 1988:45). It is through combinations of the trans, gauche, and gauche prime energies of the molecules within the polymer chain that the PVDF conformations form.

Alpha-Phase PVDF. The alpha-phase (or Form II) of PVDF is most commonly formed when the material is crystallized upon cooling from the melt. This phase is nonpolar relative to the normal axis of the molecular chain, and its unit cell molecular structure, which contains two chains, is shown Figure 3-2. The third dimension of the orthorhombic unit cell, perpendicular to the page, is 4.62 angstroms. The large arrows indicate the polarization direction of the material's dipoles relative to the normal of the molecular axis which is internally compensated (Lovinger, 1983:1117). The alpha-phase configuration of PVDF is the lowest potential energy configuration (called the TGTG' configuration) of the five known polymorphs. All dipoles are normal to the carbon chain backbone.

Beta-Phase PVDF. Beta-phase PVDF (or Form I), shown in Figure 3-3, is used in piezoelectric and pyroelectric
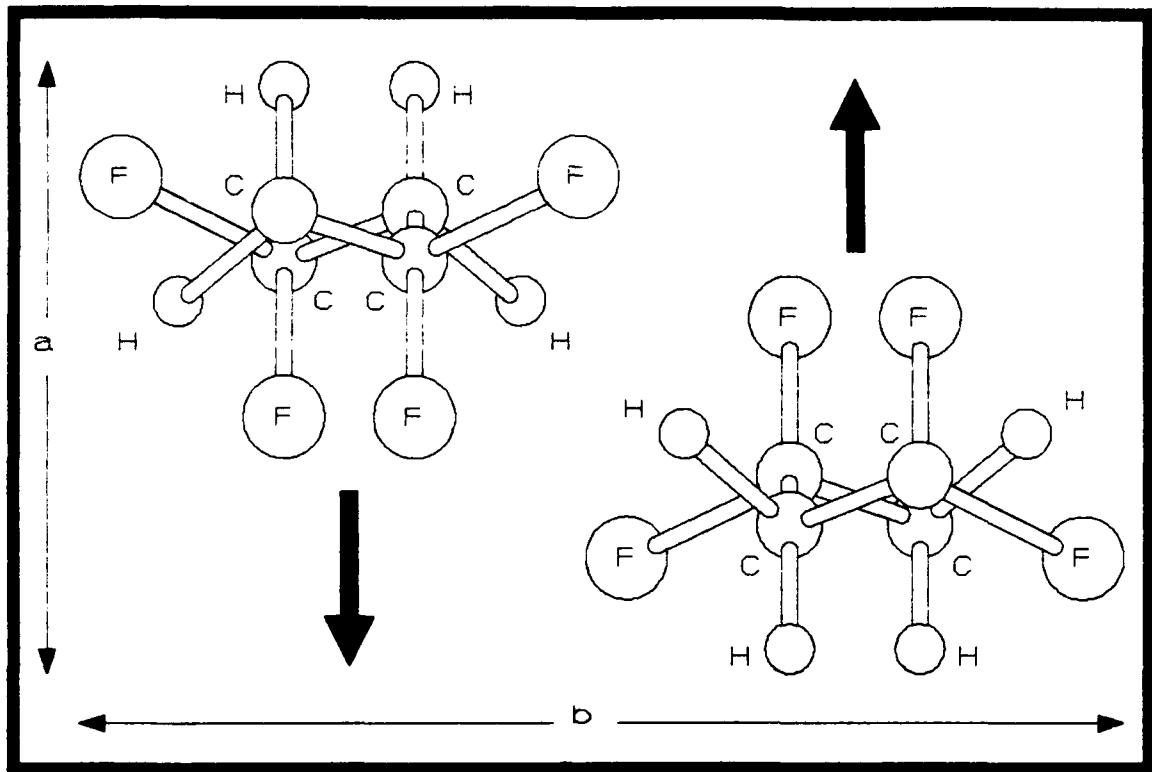
Figure 3-2. Unit cell of alpha-phase (II) PVDF (Lovinger, 1983:1117).

transducer applications. The unit cell for this phase is also orthorhombic with its third dimension equal to 2.56 angstroms. The phase's configuration is all-trans or zigzag TTTT' with chains arranged such that all the fluorine atoms are on one side of the carbon chain, and all the hydrogen atoms are on the other (Meixner and others, 1986:108). This series-aiding arrangement exhibits the largest dipole moment. However, as the chains pack within the crystalline structure they become randomly oriented, and they combine to reduce the net dipole moment to essentially zero. Special processing techniques are employed when making PVDF film to orient and maintain a net dipole moment within the film.
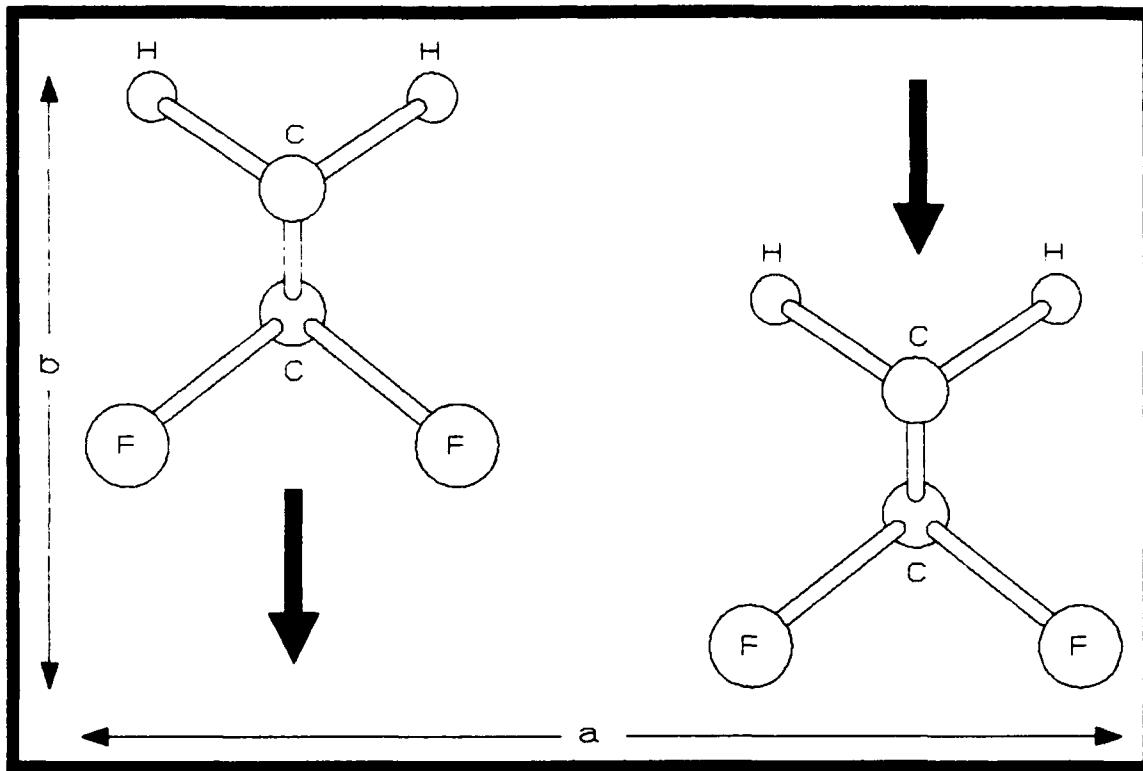
Figure 3-3. Unit cell of the beta-phase (I) of PVDF
(Lovinger, 1983:1117).

Production of Beta-Phase PVDF Film.

Manufacturing techniques such as chill wheel extrusion,
solvent casting, and thermal lamination are used to produce
PVDF films (Marcus, 1985a:894). Figure 3-4 shows alpha-
phase PVDF film being extruded and oriented by the chill
wheel extrusion method (Wang and others, 1988:23). Beta-
phase PVDF film is produced by stretching and poling alpha-
phase film. Both uniaxially and biaxially oriented films
are produced by the following techniques: hot roll relaxing;
drafting, oven stretching and tentering; and compression
rolling. After one of these orientation techniques is used,
the film is thermally or corona poled to further increase
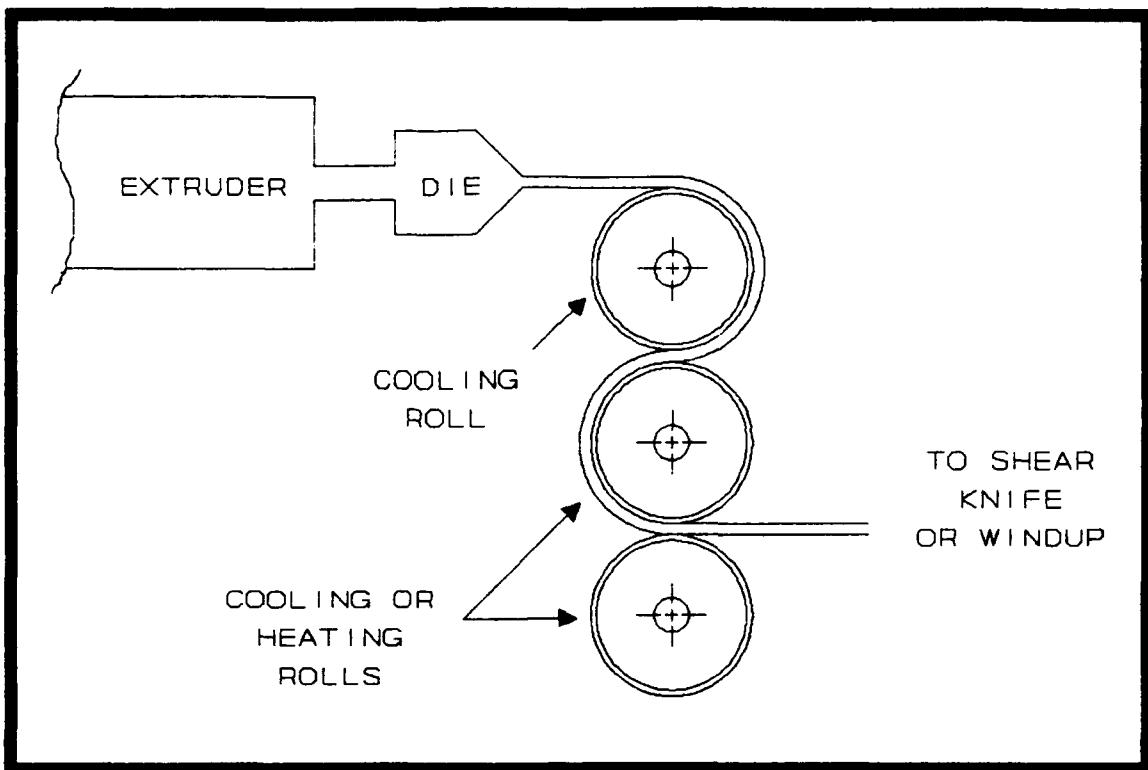
Figure 3-4. Chill wheel extrusion method (Wang and others, 1988:23).

the piezoelectric and pyroelectric activity of the film (Brown, 1988:25).

Uniaxial or biaxial elongation of the film improves several physical properties of the film, such as bulk modulus, stiffness, and recovery. As the film is rolled or stretched from three to five times its original length at temperatures below the crystallization temperature, the spherulite structures of Figure 3-1 are deformed and the molecular chains are oriented parallel to the stretch direction (Wang and others, 1988:43).

Poling PVDF film produces a permanent polarization or orientation of the molecular dipoles within the polymer

(Brown, 1988:25). Three common methods of poling include thermal, corona, and high field room temperature poling.

In thermal poling, a direct current electric field spanning 30 - 120 V/μm is applied across the film's thickness dimension. The field is applied for a duration of 15 - 120 minutes while the temperature is elevated to 80 - 130 °C. After this time period has elapsed, the temperature is lowered to 10 - 40 °C while the electric field remains applied. The polarization, therefore, depends upon the applied field, poling temperature and poling time (Sessler, 1981:1598). The maximum polarization attained is 2 μC/cm^2 for electric fields on the order of 2 MV/cm.

Corona poling can be accomplished in several seconds by applying a large potential corona discharge near the surface of the PVDF film. The opposite side of the film must be grounded. Corona charging at temperatures higher than room temperature tend to produce more thermally stable films (Wang and others, 1988:31-32). The polarization achieved by the corona discharge process attains a saturation value of 12 μC/cm^2 for fields on the order of 1 MV/cm.

High field room temperature poling (9 MV/cm for at least 5 seconds) can produce films with a polarization of 31 μC/cm^2. This technique for poling PVDF is simple and convenient to implement (Wang and Seggern, 1983:4602).

PVDF film becomes a useful transducer material after proper orientation and poling. The film's piezoelectric and pyroelectric activity depends upon the crystalline

3-9

structure, film orientation, temperature, the magnitude of the applied electric field, and the duration of poling (Marcus, 1985:724). The most common method of producing polarized PVDF film involves the combination of mechanical stretching and mechanical poling (Lovinger,1983:1118).

The properties of the finished PVDF film are a direct result of the manufacturing process. Important properties of the film include the following: thermal capacity, specific heat, thermal conductivity, glass transition temperature, volumetric thermal expansion, water absorption, Young's modulus, acoustic impedance, electrical impedance, electromechanical coupling constant, capacitance, electrical permittivity, piezoelectric strain coefficients, piezoelectric stress coefficients, and pyroelectric coefficients. Typical values for 28 μm thick, biaxially oriented PVDF film are listed in Appendix B. The next section examines the derivation of the piezoelectric constants.

Piezoelectric Constants

The origin of piezoelectricity and pyroelectricity in polymers is thought to be primarily the result of a net polarization within the bulk polymer. However, the presence of space charge and heterogeneities are considered to have secondary effects (Wang and others, 1988:58). Two previous tactile sensor theses (Reston, 1988; Ford, 1989) elucidate these atomic and macroscopic perspectives of piezoelectricity. This section is intended to present a

definition of the piezoelectric constants and to annotate
the typical nomenclature for these constants found in the
literature.

The poling process previously described produces a net
dipole moment within the PVDF film whose surface charge
density is referred to as the remnant polarization (Wang and
others, 1988:51). Stresses on the film will cause strains
which, in turn, affect the film's piezoelectric response.

Normal stresses (σ_x, σ_y, and σ_z) and shear stresses (τ_{xy},
τ_{xz}, τ_{yx}, τ_{yz}, τ_{zx}, and τ_{zy}) applied to a cube of polyvinylidene
fluoride are shown in Figure 3-5. For the normal stresses,
the subscript indicates the direction of the applied force.
The first subscript for the shear stress variable represents
the direction normal to the surface under shear. The second
subscript indicates the direction of the applied shear
force. Since the shear stresses on opposing faces of the
cube are equivalent ($\tau_{xy} = \tau_{yx}$, $\tau_{yz} = \tau_{zy}$, and $\tau_{xz} = \tau_{zx}$), the
six stress components for the cube will be denoted X_1
through X_6 for the stresses τ_x, τ_y, τ_z, τ_{xy}, τ_{yz}, and τ_{xz},
respectively.

As previously noted, the PVDF film exhibits both a
direct piezoelectric effect and a converse piezoelectric
effect. The equations which describe the film's
electromechanical behavior involve understanding the effects
which contribute to the net charge density (D) and
polarization (P) of the film.

The following equation describes the charge density (D)
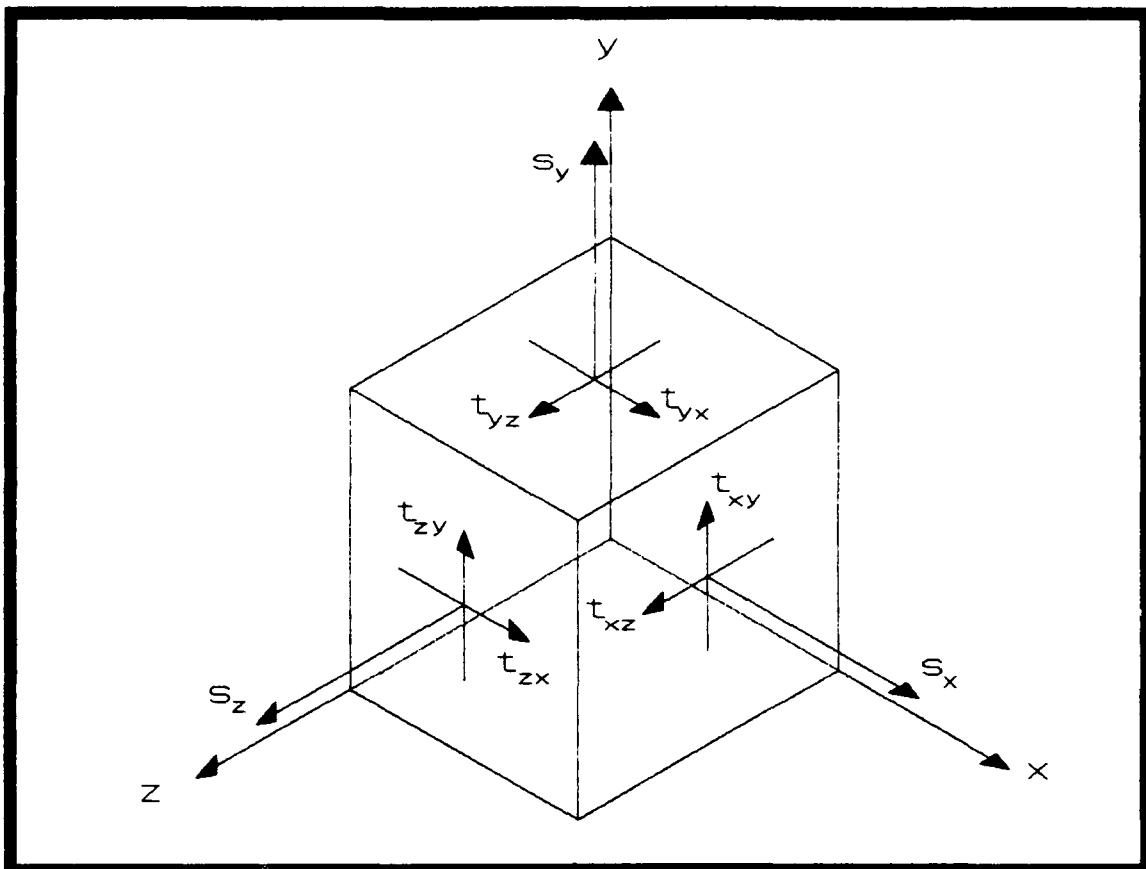
Figure 3-5. Normal and shear stress components on a cube of PVDF.

on the surface of the film as a function of an applied

electric field (Kynar, 1983:40) for a film under constant

stress X:

$$D = \varepsilon^X E$$

(3-2)

where

D = charge density (C/cm^2)
E = electric field (V/cm)
ε = PVDF permittivity (F/cm).

The electrical permittivity with the superscript X indicates

that this value corresponds to the film's permittivity when

the stress on the film is constant. The net polarization on the film will also change due to the piezoelectric nature of the film. The charge density for an applied stress will vary according to (Kynar, 1983:41):

$$D=dX$$ (3-3)

where d is the piezoelectric charge or stress constant defined by (Wang and others, 1988:54):

$$d = (\partial D/\partial X)\big|_{(E=0)}.$$ (3-4)

These two effects combine linearly to yield the net charge density of the film given by (Kynar, 1983:41):

$$D=dX+\varepsilon^X E.$$ (3-5)

The charge density (D) can be measured as a short circuit current between the top and bottom surfaces of the PVDF film. An applied electric field or mechanical stress will, therefore, affect the value of the current which flows. When the electric field applied is zero but a stress is applied, the resulting charge density is equivalent to the polarization. This applied stress can be related to a mechanical strain (S) of the film according to (Bottom, 1982:44):

$$X=cS$$ (3-5)

where
c = stiffness tensor (N/cm^2)
S = mechanical strain (unitless).

Solving equation (3-5) for X and substituting the result into equation (3-4) yields:

$$D = dcS + \varepsilon^X E. \qquad (3-6)$$

The piezoelectric strain or charge constant (e) is defined as:

$$e = (\partial D / \partial S)|_{(E=0)}. \qquad (3-7)$$

Therefore, by substituting equation (3-6) into (3-7) and differentiating, the piezoelectric strain and stress constants (e and d, respectively) are found to be related by the equation $e = dc$. The generalized piezoelectric voltage constants (g and h) are defined as follows (Wang and others, 1988:54):

$$h = (\partial E / \partial S)|_{(D=0)} \qquad (3-8)$$

$$g = (\partial E / \partial X)|_{(D=0)} \qquad (3-9)$$

where
  g = piezoelectric voltage or strain constant
      (Vcm/N or cm^2/C)
  h = piezoelectric voltage or stress constant (V/m
      or N/C).

In general, the constants d, e, g, h, and c are tensors because of the anisotropic nature of the PVDF film. The piezoelectric constants are typically specified using matrix notation. For example, the piezoelectric d-tensor is (Wang and others, 1988:55):

$$d_{ij} = \begin{pmatrix} 0 & 0 & 0 & 0 & d_{15} & 0 \\ 0 & 0 & 0 & d_{24} & 0 & 0 \\ d_{31} & d_{32} & d_{33} & 0 & 0 & 0 \end{pmatrix} \qquad (3-11)$$

where the (i) subscript 1, 2 or 3 denotes the x, y , or z

direction, and the (j) subscript 1, 2, 3, 4, 5 or 6 denotes

the direction of the applied stress (1, 2, or 3

corresponding to x, y, or z) or the applied shear (4, 5, or

6 corresponding to the shear stress about the x, y, or z

axis).

Modeling Piezoelectricity in PVDF

Numerous attempts have been undertaken to accomplish

the difficult task of modeling the piezoelectricity in PVDF.

These efforts are predicated on assumptions concerning the

degree of crystallinity present (that is, the polymer is a

mixture of crystalline structures embedded in an amorphous

phase). Other parameters which vary include film

temperature, electrical permittivity (complex) of the

crystalline phase, and electrical permittivity (complex) of

the amorphous phase. The majority of models agree that at

least 50% of the film's piezoelectricity originates from

dimensional changes in the film's thickness (Wang and

others, 1988:61-62). This idea is strongly supported by

experimental data.

The other contributors to the piezoelectric effect

originate from changes in the sample's dipole moment for a

constant film thickness (Broadhurst and Davis, 1984:10).
One such contributor is the electrostriction of the
crystalline structure which is thought to account for 22 to
45% of the film's piezoelectricity (Wang and others,
1988:61). Other factors include: the number of dipoles in
the crystalline phase which depend upon the applied stress;
the ferroelectric order parameter, which is the difference
between the number of dipoles parallel and antiparallel to
the crystal's moment; the shape of the crystals which have
been modeled as thin crystals, spheres, and disks; and the
changes in librational amplitude which primarily affect the
hydrostatic piezoelectric constant d_h ($d_h = d_{31} + d_{32} + d_{33}$)
(Broadhurst and Davis, 1981:10-12). Libration is defined
as:

> A real or apparent very slow oscillation of a
> satellite as viewed from the larger celestial body
> around which it revolves. (Morris, 1979:753)

Large librational amplitudes are observed only for dipoles
with large dipole moments (Broadhurst and Davis, 1984:12).

Wada and Hayakawa derived the following model for the
piezoelectric voltage constant (e). The model takes into
account the effects of strain on electrical permittivity,
film thickness, film volume, and the spontaneous
polarization of crystalline spheres embedded in an isotropic
matrix, and is given by (Wada and Hayakawa, 1981:115):

$$e = P_s \left[\left(\frac{\varepsilon_{sp}}{(2\varepsilon + \varepsilon_{sp})} \right) \left(\frac{\kappa}{\varepsilon} - \frac{\kappa_{sp} I}{\varepsilon_{sp}} \right) - \frac{\partial(\ln l)}{\partial S} \right] + \Phi \left(\frac{3\varepsilon}{2\varepsilon + \varepsilon_{sp}} \right) e_{sp} I \quad (3-12)$$

where

P_s = spontaneous polarization of the whole film
ϕ = volume fraction of spheres
l = film thickness
ε = dielectric constant of the film
ε_{sp} = dielectric constant of the sphere
κ = electrostriction constant $(\partial \varepsilon / \partial s)$
r = ratio of strain in sphere to strain in whole film
e_{sp} = piezoelectric constant of the sphere

and the subscript sp denotes spherical crystallites. P_s is defined according to the following equation:

$$P_s = \frac{N}{Al}\left(\frac{3\varepsilon}{2\varepsilon + \varepsilon_{sp}}\right) v P_{sc} = \phi\left(\frac{3\varepsilon}{2\varepsilon + \varepsilon_{sp}}\right) P_{sc} \qquad (3\text{-}13)$$

where

N = number of spheres
A = area of the contacting electrode
P_{sc} = spontaneous polarization of spheres
v = volume of film sample.

The ratio of strain in the sphere to strain in the whole film is defined by:

$$g = \frac{5G}{3G + 2G_{sp}} \qquad (3\text{-}14)$$

where

G = elastic modulus.

The piezoelectric constant of an individual spherulite is

$$e_{sp} = \frac{1}{v}\frac{\partial(v P_{sc})}{\partial S_{sp}} = P_{sc}\left(\frac{\partial \ln v}{\partial S_{sp}} + \frac{\partial \ln P_{sc}}{\partial S_{sp}}\right). \qquad (3\text{-}15)$$

This model accounts the strain dependence of ε, l, v, and P_{sc}. However, the model neglects the libration amplitude, and it assumes that trapped space charges lie on the folded chain surface of the crystallite, and thus, add to the

dipoles within the crystallite.

Pyroelectricity is defined by the pyroelectric equation (p) given by the following equation (Wada and Hayakawa, 1981:115):

$$p = \left(\frac{1}{A}\right)\frac{\partial(AP_s)}{\partial T} \qquad (3\text{-}16)$$

where T is the temperature in degrees Kelvin, and p has units of coulombs per square meter per degree Kelvin. The pyroelectric coefficient (p) is a function of the rate of change of temperature. Pyroelectricity can be similarly modeled with respect to piezoelectricity according to the temperature dependence of ε, l, v, and P_{sc} (Wada and Hayakawa, 1984:116).

The true origins of piezoelectricity within the PVDF film material are not yet fully understood; however, some of the possible contributors have been discussed. The impetus behind understanding which mechanisms cause the piezoelectric effect within the PVDF film is primarily that of modifying the molecular structure to obtain a better performing film.

IV. Design and Fabrication Procedures

This chapter is divided into two major sections: the design of the integrated circuit and the tactile sensor fabrication procedures. In the first section, the design procedures utilized to synthesize the major subcomponents of the sensor are discussed. The second section includes a description of the procedures used to characterize the piezoelectric activity of the PVDF film and the procedures for fabricating the tactile sensor.

Integrated Circuit Design

A block diagram of the tactile sensor integrated circuit design is shown in Figure 4-1. The major components of the design include 49 MOSFET amplifiers, a 49-channel analog multiplexer, and a variable frequency clock (1 Hz to 1 kHz) to drive the multiplexer circuit. Each electrode charge signal amplifier is located a common distance from its corresponding sensing electrode. The actual electrode matrix (7 rows by 7 columns) measures 5.2 mm by 5.2 mm. An opening in the glass passivation layer exposes the array of electrodes and facilitates attaching the 25 μm thick patch of PVDF film which measures 6 mm by 6 mm. Each matrix electrode is 400 μm square, and the separation between these electrodes is 400 μm. The metal line between each matrix electrode and its corresponding MOSFET amplifier was designed to have the same shape and length as was
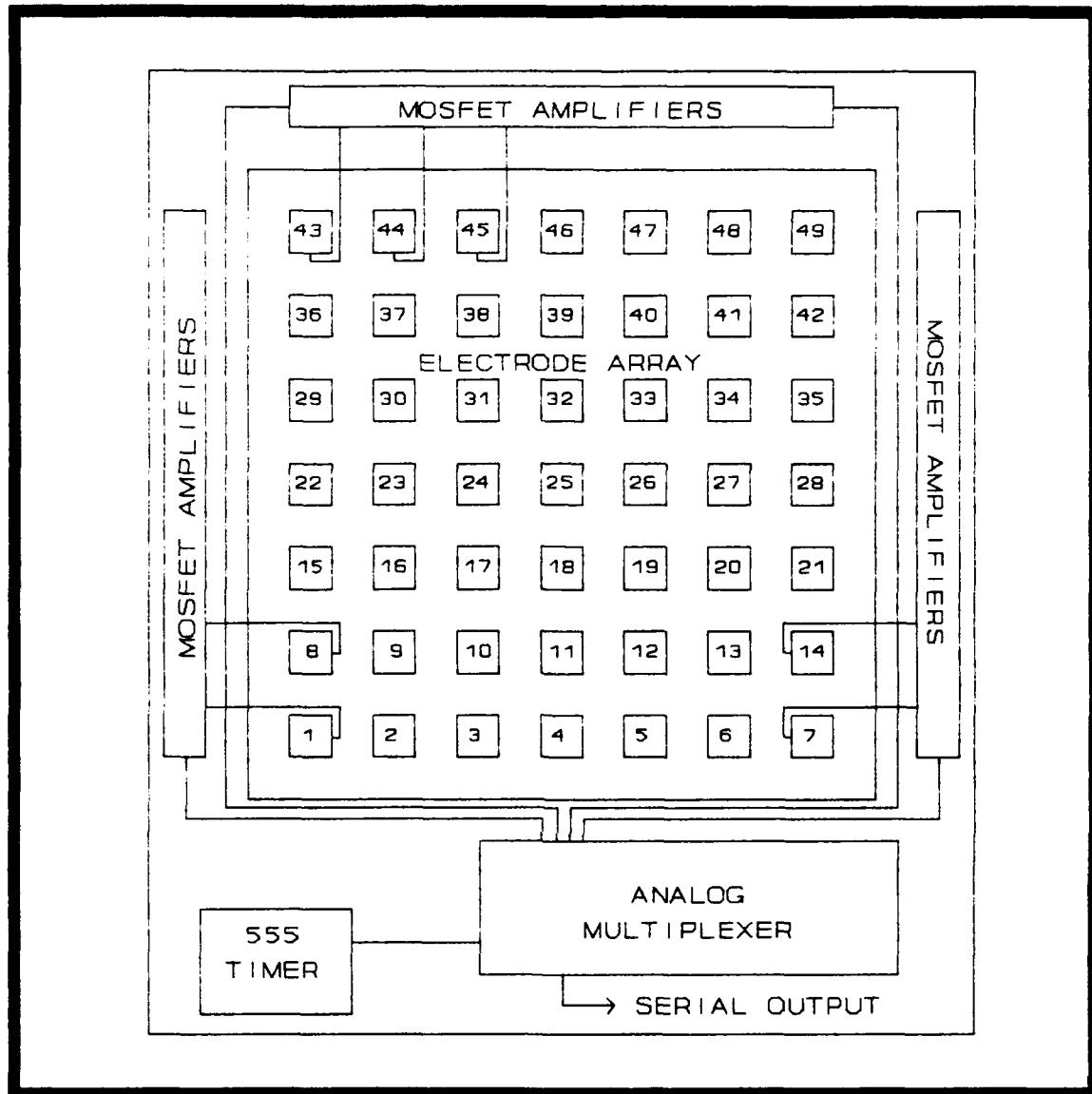
Figure 4-1. Block diagram of the tactile sensor integrated circuit.

practically feasible. Only seven metal line connections are
shown for simplicity.

MOSFET Amplifier Design. The MOSFET amplifier operates
as a buffer between the high impedance of the PVDF film and
the smaller impedance of the multiplexer circuit at the
output of the amplifier. The gate region of each MOSFET

4-2

transistor has a floating gate input with a near infinite
input resistance and a capacitance of 10^{-12} farads;
therefore, its RC time constant is compatible with that of
the PVDF film (Ford, 1989:V-13).

The design of the amplifier was an iterative process
which utilized the design tools of SPICE and MAGIC. SPICE
was used to properly size the transistors' gate length and
width, source and drain diffusion areas, and the value of
the bias resistors. Captain Reston, in his thesis,
demonstrated that the amplifier was an effective device for
amplifying the electrode charge signal generated by the PVDF
film (Reston, 1988:4-8). The matrix electrodes' charge
signal amplifiers were properly sized to correspond to the
anticipated input voltage generated by the PVDF film while
under a mechanical load, given by the following equation
(Kraus, 1984:69,70):

$$V = \frac{d_{33} t F}{\varepsilon A} \qquad (1-1)$$

where

d_{33} is the piezoelectric charge constant (16 pC/N)
t is the thickness of the PVDF film (0.0025 cm)
F is the magnitude of the applied load (N)
ε is the permittivity of the PVDF film (10.6×10^{-13} F/cm)
A is the area of an electrode (cm^2).

For 400 μm by 400 μm electrodes and loads which span 1 to
100 grams, the expected PVDF film generated voltage should
span 0.224 to 22.4 volts, respectively. Therefore, an

amplifier which produces a linear output for an input range
spanning 0 to 23 volts was desired. However, to limit power
consumption by the device, and therefore device heating, the
maximum supply voltage was limited to 10 volts. Hence, the
amplifier was designed to operate linearly from 0 to 10
volts.

Figure 4-2 is a schematic drawing of the MOSFET
amplifier whose transistor parameters and resistor values
are:

$$\text{gate length} = 2 \ \mu\text{m}$$
$$\text{gate width} = 8 \ \mu\text{m}$$
$$\text{source area} = 48 \ \text{pm}^2$$
$$\text{drain area} = 48 \ \text{pm}^2$$
$$R = 5000 \ \Omega.$$

A SPICE deck detailing critical parameters used in the
analysis of the amplifier is included in Appendix D. The n-
channel, enhancement-mode transistor parameters exemplify
the values for a typical MOSIS CMOS fabrication run. The
results of the SPICE analysis are illustrated in Figure D-1.
The linear region of the plot extends from approximately 2.5
to 9 volts and the supply current drawn by the amplifier is
2 milliamperes. Figure E-1 of Appendix E is the
corresponding Caltech Intermediate Format (CIF) plot of the
amplifier. The MAGIC VLSI layout editing tool was used to
produce a visual description of the various mask layers
required to fabricate the amplifier. From this layout, a
CIF file was made which describes the location of rectangles
that describe the various mask layers of the IC. The MOSIS
vendor uses this CIF file to produce photolithographic
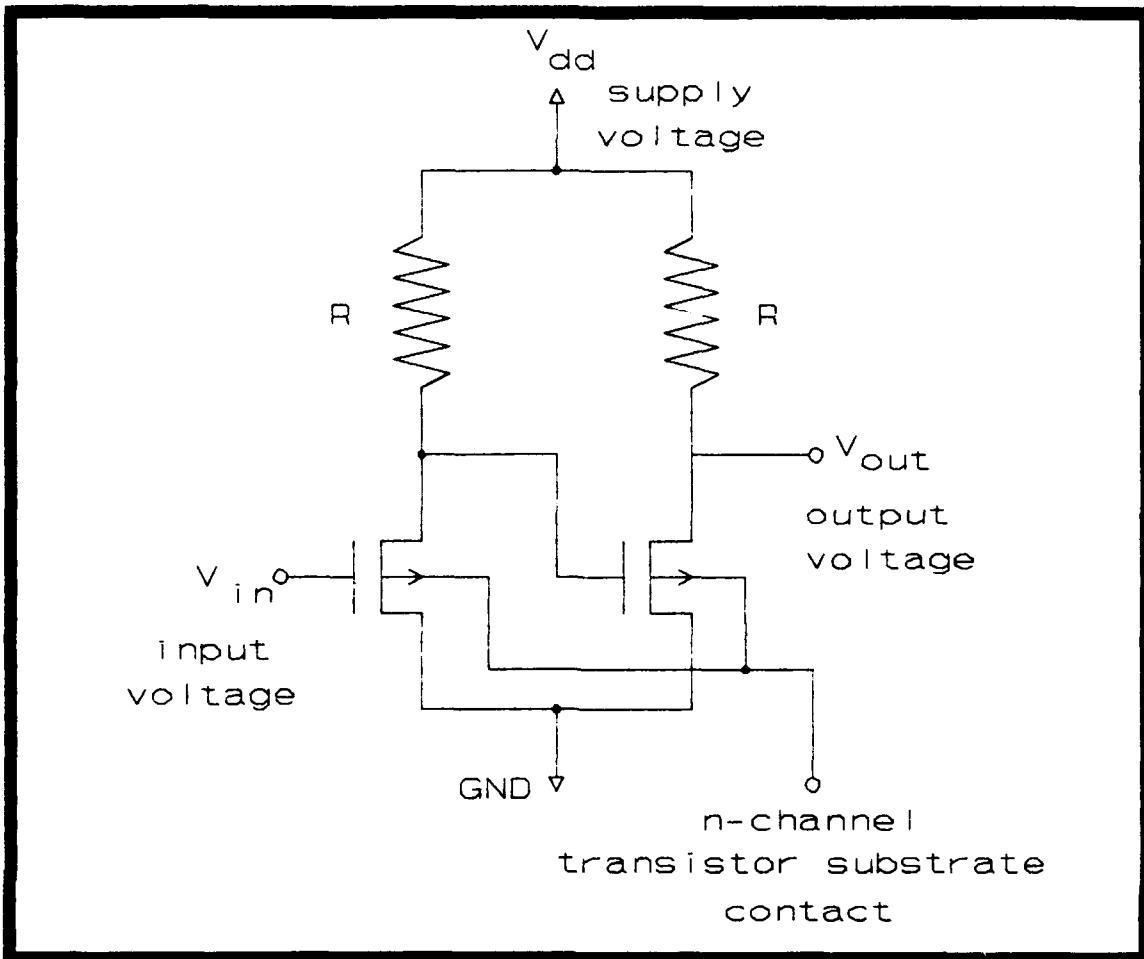
Figure 4-2.   Schematic drawing of the MOSFET amplifier.

masks.   The CIF plot is a black and white rendition of the MAGIC file description.

As previously noted, biasing the input electrodes which are coupled to the charge amplifiers is a difficult problem. A schematic of the MOSFET amplifier biasing schemes to be investigated in this investigation is shown in Figure 4-3. The gate of each amplifier should have a uniform voltage prior to the film's deformation (that is, a constant bias level should exist across the electrode matrix).   This
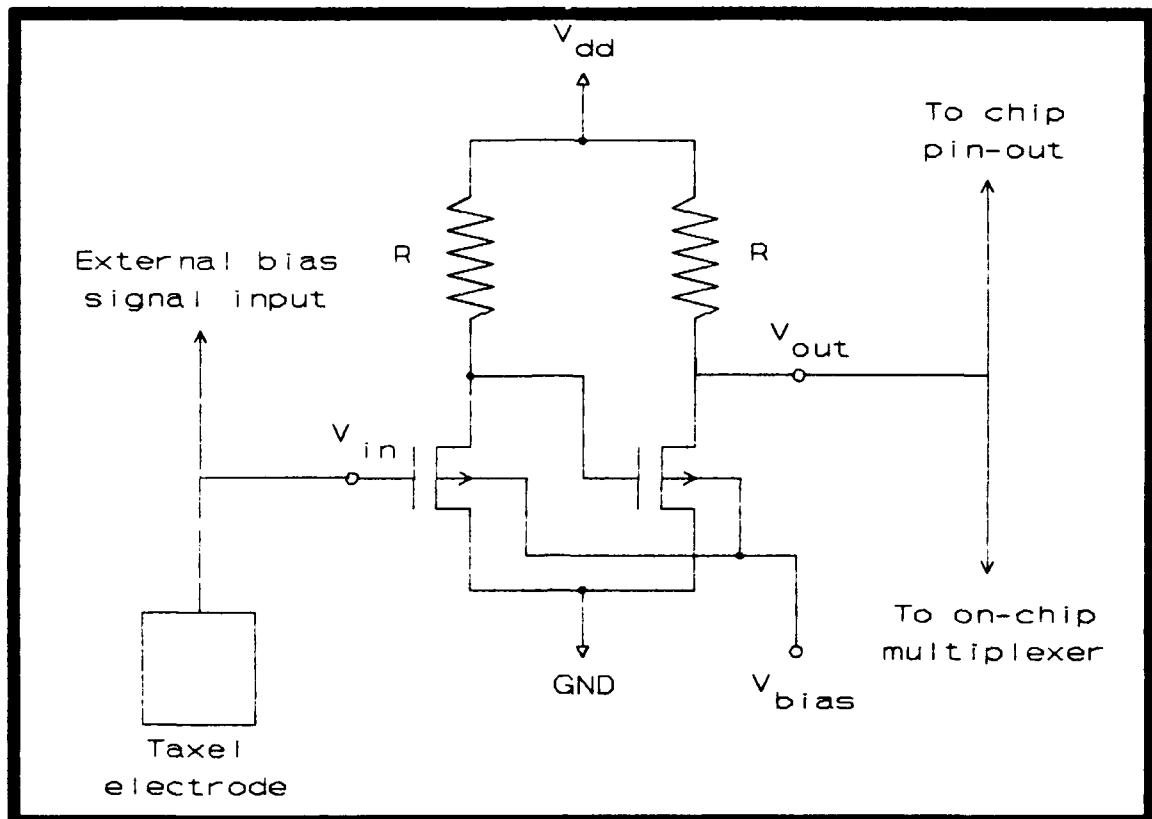
Figure 4-3.   Charge signal amplifier biasing schemes.

voltage is measured relative to the top, metallized surface
of the PVDF film. Any existing stress in the PVDF film due
to its adherence to the array structure or residual
deformation from an earlier applied load may cause the
potential on the electrodes to vary. This variance can be
minimized by properly biasing each amplifier to establish a
linear and time-invariant DC operating point. The first
biasing scheme will be performed in a manner similar to
those used by Captains Reston and Ford, whereby they applied
a voltage to the input of the MOSFET gates and across the
PVDF film to establish a uniform initial charge state at
each amplifier's input. However, instead of using the

Micromanipulator Probe to apply this voltage to a test pad on the IC, the new IC will include 49 external pins which connect directly to the inputs of each amplifier. Reed switches will be used to isolate these inputs from, or connect them to, the biasing voltage source. This design will facilitate the process of applying a bias to the amplifiers, and it should provide a uniform charge state on each electrode throughout the taxel array.

The second biasing scheme will provide an external pin connection to the p-well which contains the n-channel transistors of the amplifier. A bias signal applied to the p-well (a negative voltage relative to the substrate's potential and a positive potential relative to ground) will increase the bias across the amplifier.

Design of the Analog Multiplexer Circuit. The multiplexer shown in Figure 4-4 was designed to be driven by an on-chip clock or an external clock signal. The 49 output signals from the analog taxel amplifiers are connected in parallel to the analog multiplexer. The analog signals pass, in succession, through the multiplexer; one signal each clock pulse. Multiplexing is accomplished by selecting one of the seven rows of electrodes and then sequentially selecting the seven columns. Each row is scanned in this manner until all 49 signals pass through the multiplexer.

The analog signals from the amplifiers pass through transmission gates which are sequentially selected by row and column drivers. The row and column drivers are selected
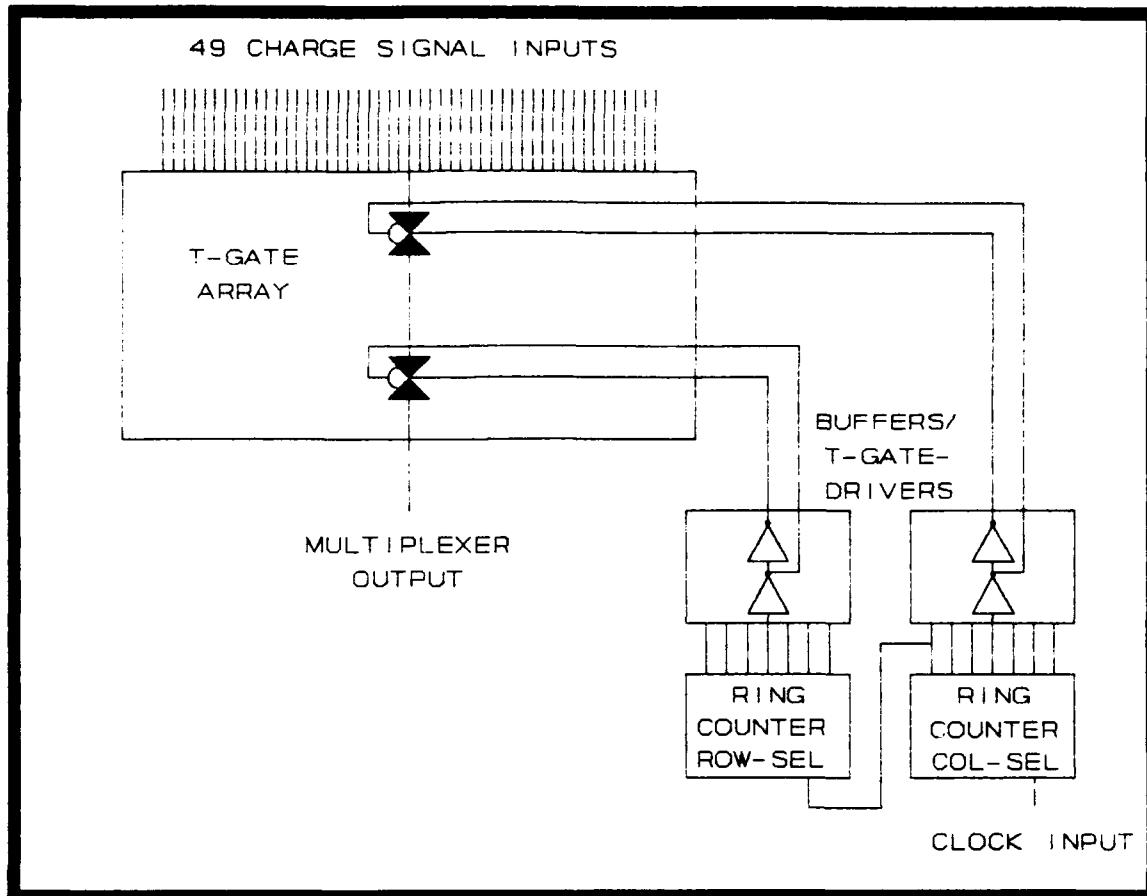
Figure 4-4. Analog multiplexer circuit.

by two seven-stage ring counters. The clock signal is fed
to one of the ring counters, and the output from the final
stage of the driven ring counter acts as the clock signal
for the second ring counter. The designs of each
subcomponent (transmission gate, D flip-flop, buffer/driver)
of the multiplexer circuit are discussed in the following
sections.

Design of the Transmission Gates. The purpose of
the transmission gate in the overall multiplexer design is
to allow the analog signal from the charge signal amplifier

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to pass, with minimal degradation, to the output of the multiplexer.

A schematic of the transmission gate is shown in Figure 4-5. The analog signal passes through the n-channel and p-channel MOSFETS when the control signals are high and low, respectively (the n-channel transistor has the controlling input labelled PHI). The analog signal is not allowed to pass when the control signals are low and high, respectively. The SPICE parameters for the transmission gates are listed in Appendix D.

The SPICE analysis involved placing a piecewise-linear signal on the input line of the transmission gate and activating the control lines. These results are shown in Figure D-2, and they indicate no degradation of the signal;
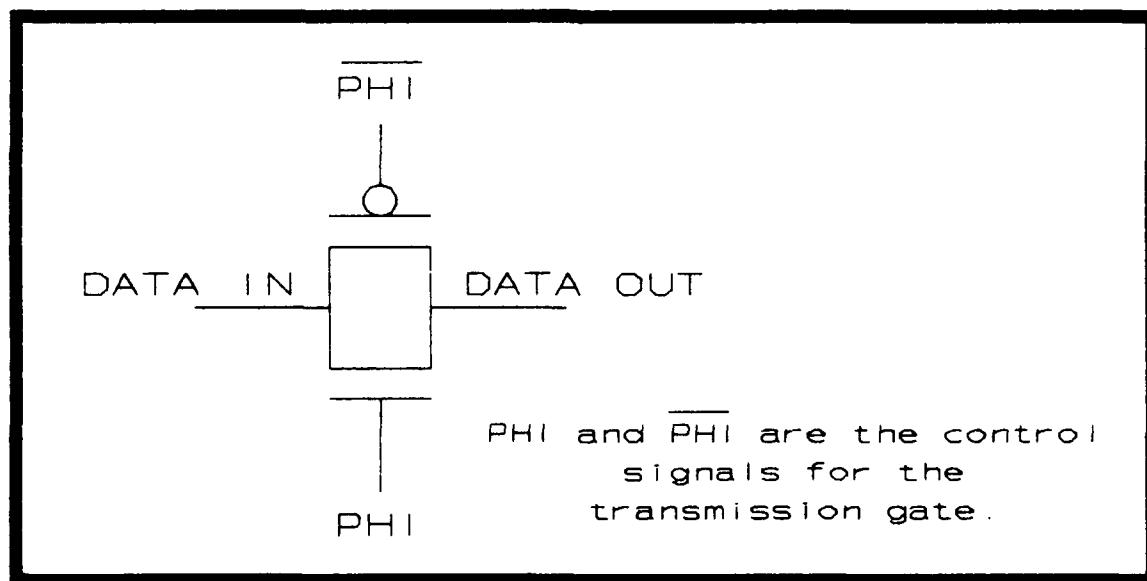
Figure 4-5. Schematic of the analog transmission gate.

that is, the output signal followed the input almost exactly. A CIF plot of the transmission gate is shown in Figure E-2.

Design of the Settable/Resettable D Flip-Flop.
The D flip-flop is the building block of the two ring counters which select the row and column drivers of the multiplexer. A schematic of the flip-flop is shown in Figure 4-6. The first section serves as the set/reset portion of the overall flip-flop. A high signal to the SET input will make the data going into the second section of the flip-flop go high. Conversely, a high signal to the CLEAR input will send in a low signal. Data sitting on the DATA input to the second section of the flip-flop will be clocked through this section when the clock pulse goes high. Normal operation of the flip-flop occurs when both the SET and CLEAR inputs are low, and the data is allowed to flow directly through the set/reset section to the flip-flop section.

Appendix D includes the SPICE deck used to simulate the operation of the D flip-flop. The circuit was tested by setting the CLEAR input high while the DATA input signal transitioned between a high and low signal level as shown in Figure D-3. The output line transitioned low and remained low following the first clock pulse. Similarly, the SET input was tested, and the output remained high (see Figure D-4). When both the SET and CLEAR inputs were tied low, the signal on the DATA input line properly flowed to the output

4-10
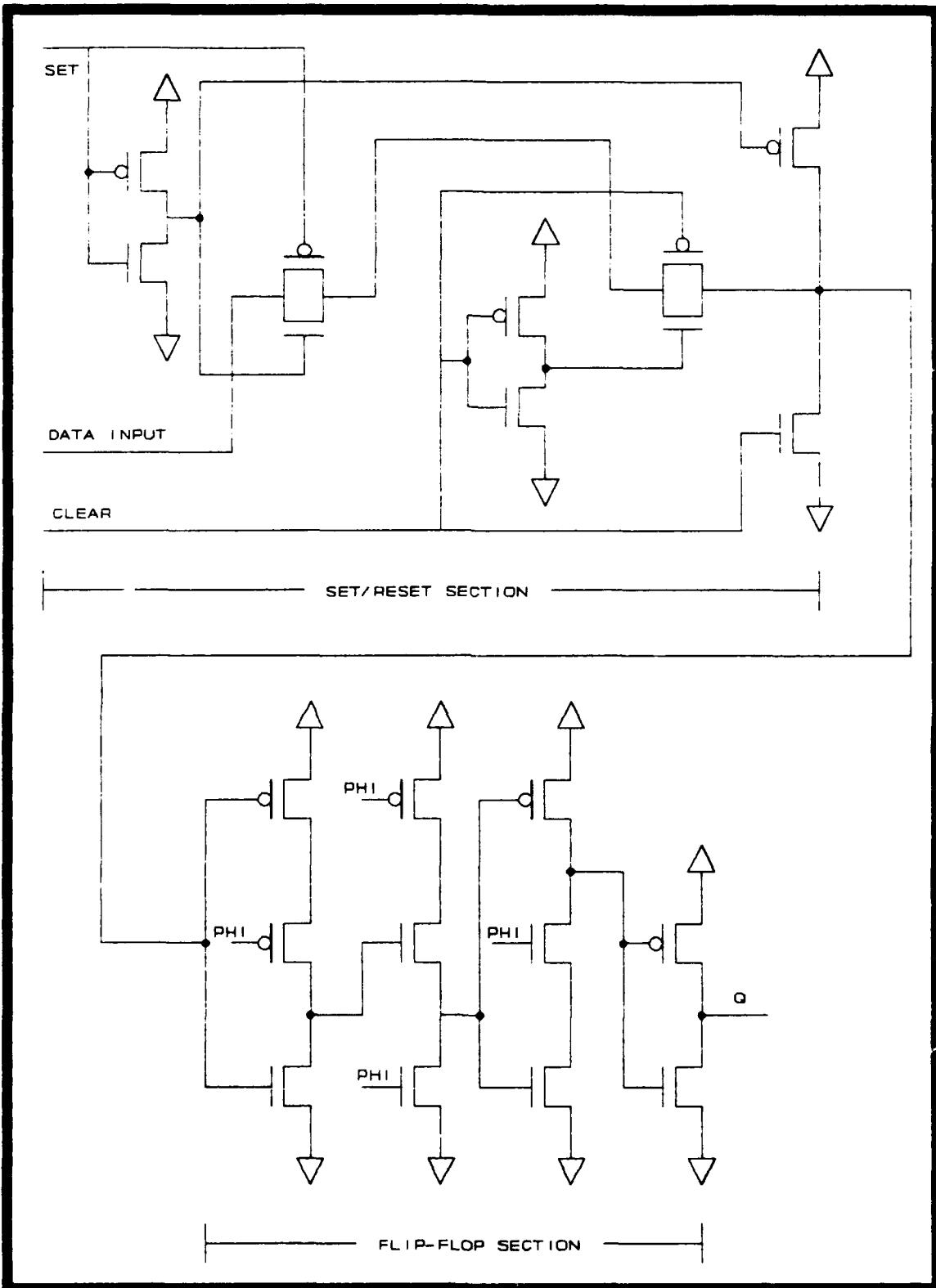
Figure 4-6. Schematic of the D flip-flop design.

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on the positive edge of each clock pulse (see Figure D-5).

A CIF plot of the flip-flop is shown in Figure E-3. An ESIM analysis of the flip-flop verified correct performance of the MAGIC layout and corresponding CIF file.

The ring counter is made by forming a chain of seven flip-flops where the output of one flip-flop feeds the input of the next. By clearing all the flip-flops in the chain, and then setting one flip-flop's output high, a high signal will ring around the chain in unison with the pulses from the clock input.

Design of the Transmission Gate Drivers. The
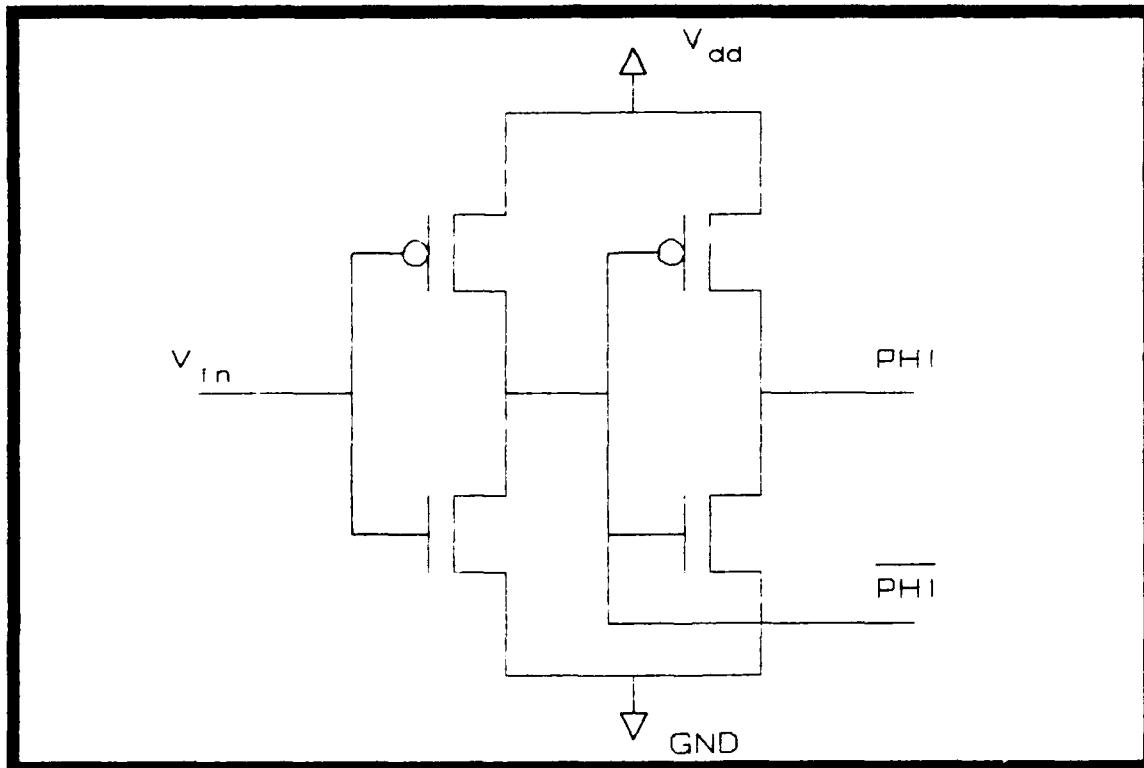
Figure 4-7. Schematic of the transmission gate driver.

transmission gate drivers serve as buffers between the ring

counters and the transmission gates. The output from each

flip-flop of both ring counters is inverted twice, and these

voltages serve as the control signals for the transmission

gates. Figure 4-7 is a schematic of the drivers. SPICE and

ESIM analyses were performed to verify the analysis of the

performance

Design of the Clock Circuit. The clock circuit was

implemented with a conventional 555-timer design which

utilizes an external resistor/capacitor network to control

the clock rate.

A schematic of the 555-timer circuit is shown in Figure

4-8 (Allen, 1987:652). The design consists of three

resistors, two comparators, a latch, three inverters, and a

MOSFET transistor. The three resistors act as a voltage

divider for the negative input of comparator A, and the

positive input of comparator B. For a supply voltage of 5

volts, the voltage at the negative input of comparator A is

3.33 volts, given equivalent values for R. Similarly, the

voltage at the positive input of comparator B is 1.67 volts.

The initial condition of the circuit is: transistor M1 is in

the off state; the output of comparator A is high; the

output of comparator B is low; and the timer's output is

high. As the latch output transitions from high to low, the

first inverter which follows the latch turns on transistor

M_1. Therefore, the external resistor/capacitor network

discharges through transistor M1. The threshold level at
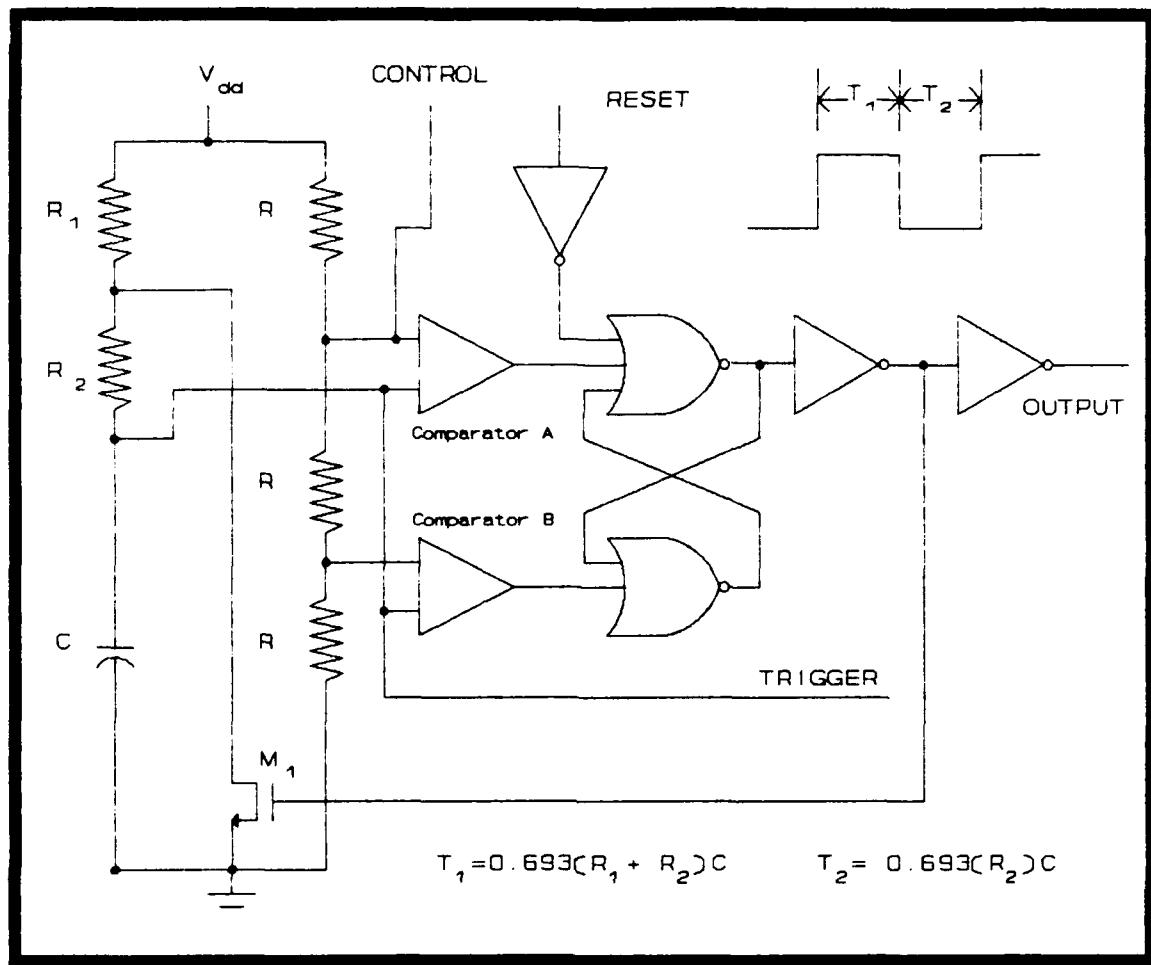
Figure 4-8. Design of the 555-timer clock circuit (Allen, 1987:652).

the positive input of comparator A drops below 3.33 volts, and the output of the timer goes low. The entire cycle repeats approximately at the charge and discharge rate of the external resistor/capacitor network. A limit on these rates is attained when the RC time-constant of the external network approaches the delay time seen representative of comparators, latch, and first inverter stage.

Design of the Comparator Circuit. The comparator is a differential transconductance amplifier comprised of

4-14

four transistors and one resistor. The circuit generates an
output current which is a function of the difference between
two input voltages.
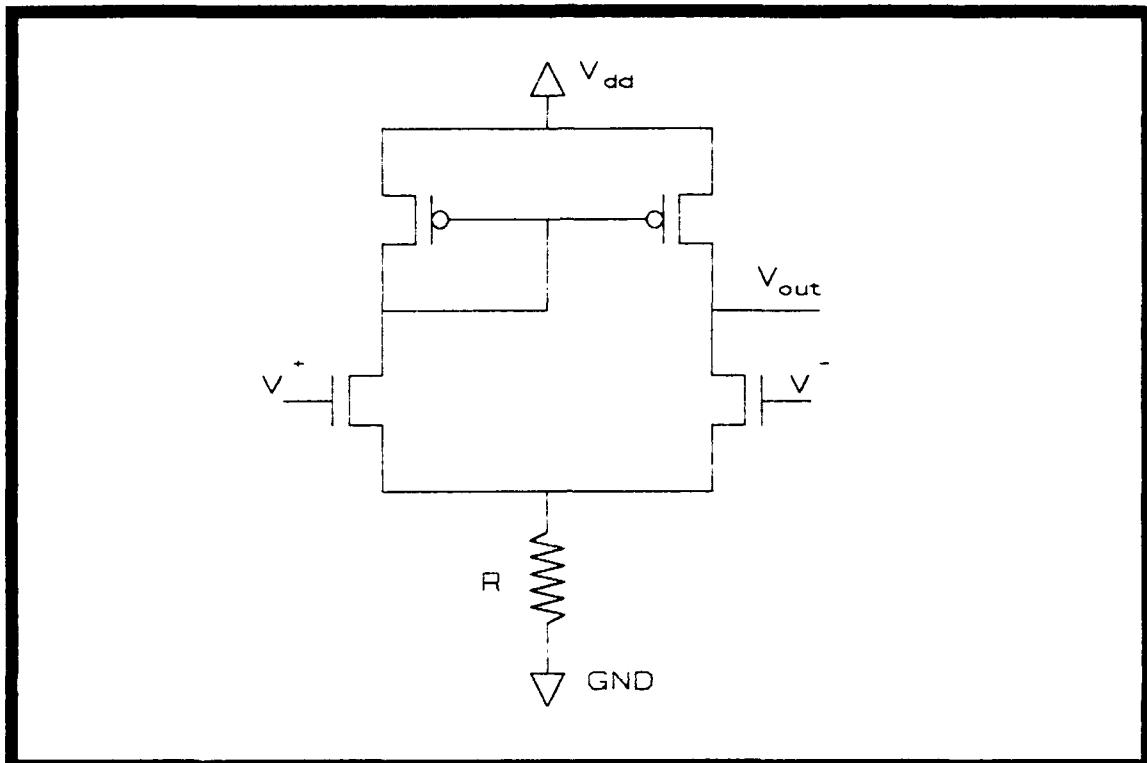
Figure 4-9.   Schematic of the 555-timer's differential
amplifier circuit.

A schematic of the comparator is shown in Figure 4-9.
Resistor R is 264 ohms, and the p-channel transistors have
gate lengths three times larger than the n-channel
transistors (12 μm versus 4μm).   The results of the SPICE
analysis are shown in Figure D-7.   The CIF plot of the
circuit is included in Figure E-4.

3-Input NOR Gate Design.   The NOR gate is the
building block of the latch circuit within the 555-timer's
design.   The three-input NOR gate was designed so that a

reset line could be included as shown in the schematic of the timer circuit (Figure 4-8).

The NOR gate shown in Figure 4-10 was analyzed in SPICE. The output transitioned high only when all three inputs were low. These NOR gates were then integrated into
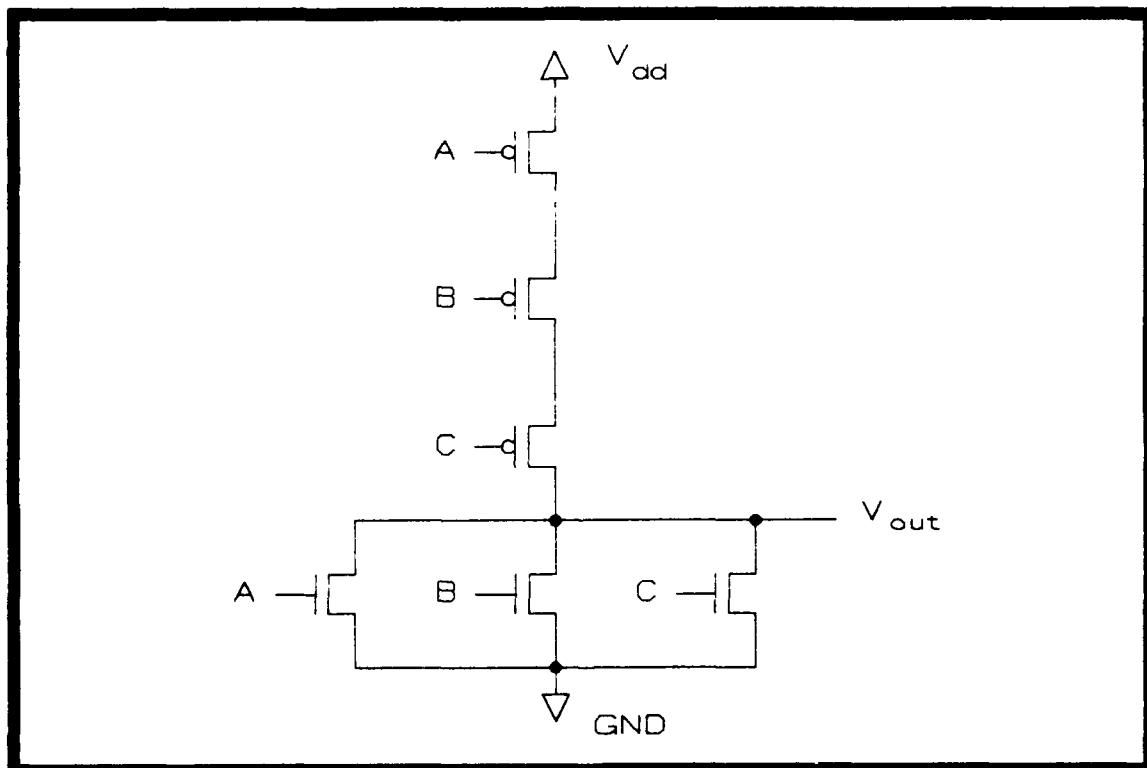
Figure 4-10.   Three-input NOR gate.

the latch portion of the timer and tested in SPICE. Figures D-8 and D-9 show the response of the individual NOR gates and the latch circuit, respectively.

An ESIM analysis of the NOR gate revealed proper operation of the layout shown in Figure E-5. The final consideration in the design of the 555 timer was the buffer

circuit to interface the timer with a load. The buffer was simply three inverters in a chain where each inverter increased in size along the chain. These inverters produced an output of sufficient power to drive the capacitive load of the ring counters.

Modular Design Concept. All elements of the multiplexing scheme were implemented as modular blocks which could be isolated from the system should they malfunction. This design concept correspondingly routed all 49 amplifier signals to 49 external pins on the IC. These signals could then be independently recorded by external data processing equipment. Also, each electrode was independently connected to an external pin on the IC.

Test Probe Design

Captains Ford and Reston used the micromanipulator probe to apply loads to the tactile sensor. Captain Ford expressed two major concerns in his thesis involving the application of loads to the tactile sensor array: (1) repeated application of the shape to a precise location (area of taxels) was difficult; (2) uniform contact of the shape with the surface was difficult (that is, it was difficult, for example, to ensure a square shape which covered the area of four taxels and weighed 40 grams distributed ten grams on each taxel).

To overcome these difficulties, the te t probe depicted in Figure 4-11 was designed and fabricated. The AFIT Model
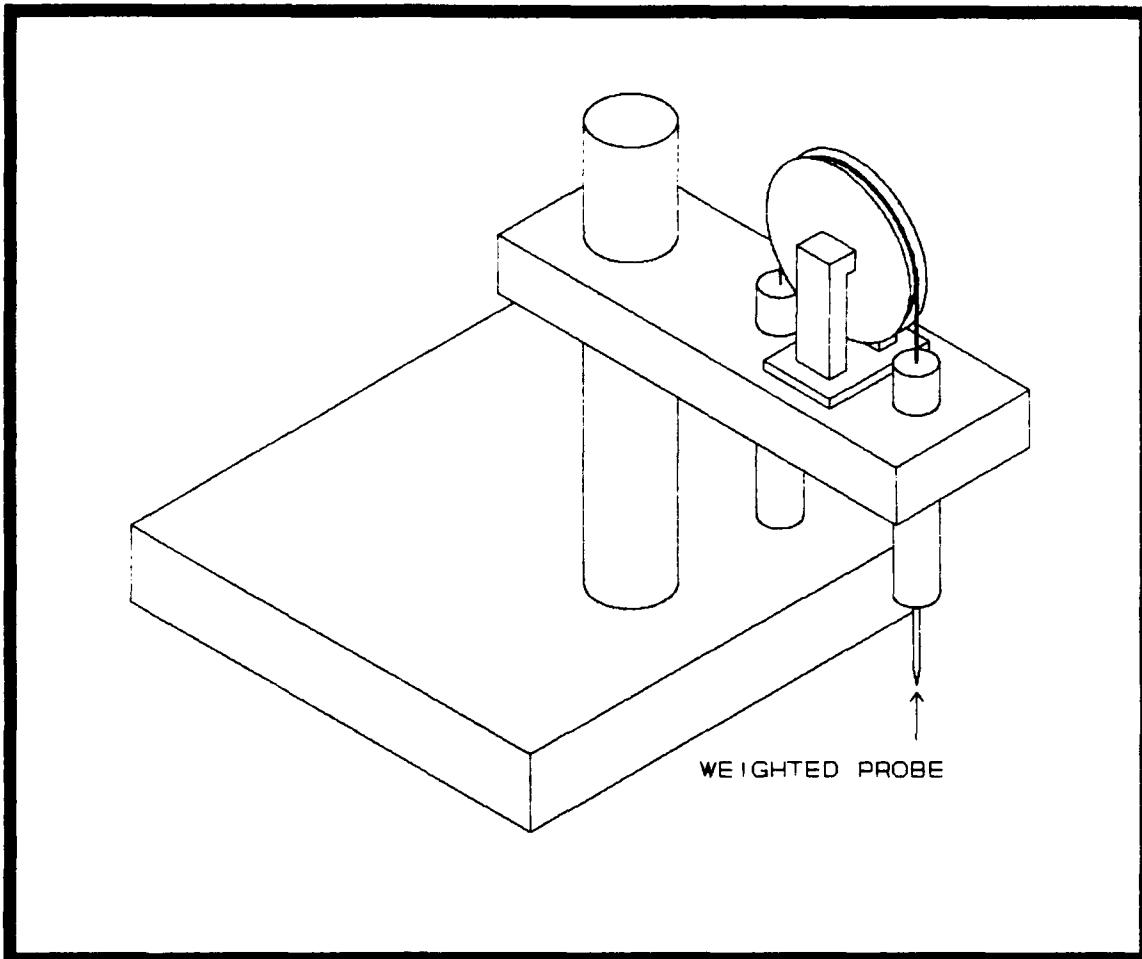
Figure 4-11.   Test probe fixture.

Shop fabricated the device from the mechanical drawings in
Appendix C. The device consists of two cylindrical weights
suspended with a stainless steel ball chain which rides in a
grooved pulley. The front cylinder holds the test shape
while the back cylinder serves as the counterweight.

The front cylinder contains a collet (Figure C-3) which
holds a stainless steel threaded ball/rod extension. The
test shape is threaded onto the ball/rod extension. A
spring within the cylinder is normally compressed by the cap

on the collet and the inner lip of the cylinder wall.
Therefore, the collet will clamp around the ball portion of
the ball/rod extension and not allow the shape to move. A
set screw in the cylinder wall contacts the beveled edge of
the cap on the end of the collet. By tightening this screw,
the spring is further compressed, thereby allowing the
collet to loosen. The shape can then be properly adjusted
to sit uniformly on the tactile sensor's array surface.
When this adjustment is correct, the set screw is loosened,
the collet tightens, and the ball/rod and shape are locked
into place.

The back cylinder contains brass counterweights (nine
ten gram weights, one five gram weight, and five one gram
weights) which can be readily removed to obtain loads
ranging from 1 to 100 grams in increments of 1 gram.
Therefore, repeated application of a uniform load ranging
from 1 gram to 100 grams to a precise location on the taxel
array is ensured. Figure 4-12 contains a black-and-white
photograph of the completed test probe fixture.

Characterization of PVDF Film.

Concurrent with the IC fabrication process, the 25 μm
thick PVDF film was characterized to determine its
polarization (KYNAR, 1983:29). The surface of the film
which develops a positive charge when the film is compressed
was the side attached to the electrode array. This surface
was also unmetallized. The film polarization detection
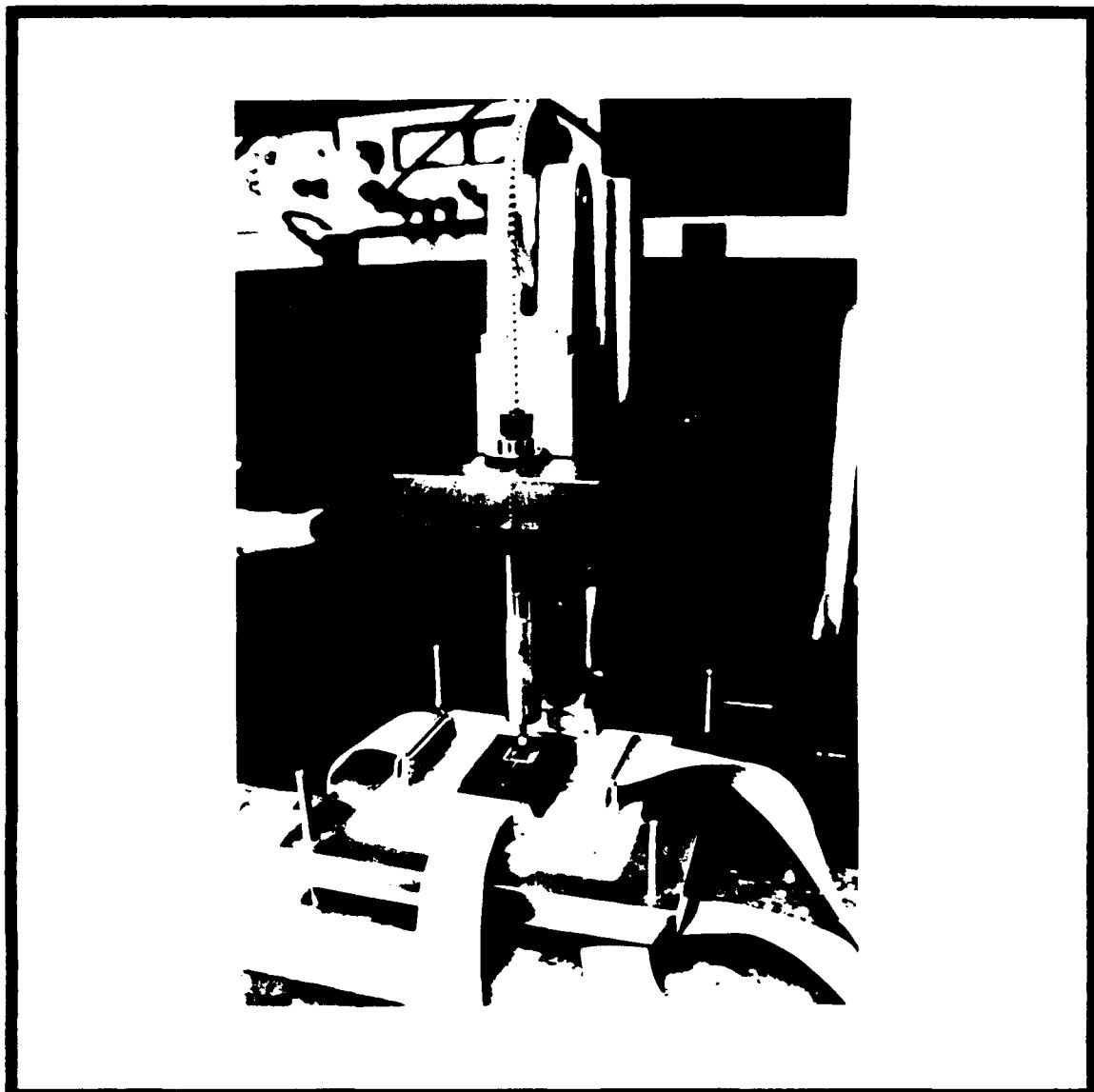
Figure 4-12.   Black-and-white photograph of the test probe fixture.

procedure was implemented as follows:

(1)   A 6 mm by 6 mm piece of the PVDF film was cut from a larger 8 by 11 inch sheet of film (one side of the large sheet was marked in one corner with indelible ink for orientation purposes; the same side of the smaller piece of film was similarly marked).

(2) A thermal evaporation process was used to
partially cover a glass slide with aluminum electrodes as
shown in Figure 4-13. A strip of conductive copper tape was
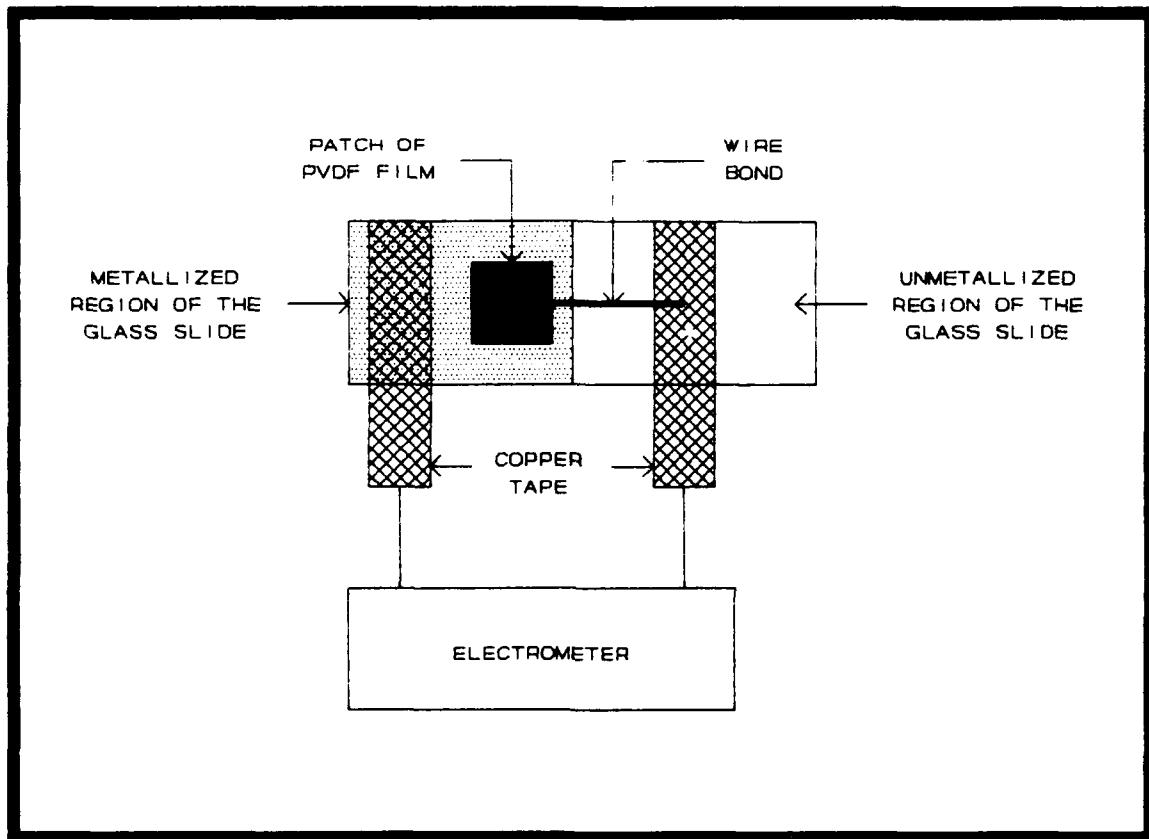
Figure 4-13. PVDF film polarization detection procedure.

then attached to the aluminum.

(3) The piece of PVDF film was then attached to the
glass slide with acrylic adhesive as shown.

(4) A piece of copper tape was attached to the un-
metallized portion of the glass slide, and a 1-mil diameter
wire was wire-bonded from the tape to the top surface of the
film.

(5) The voltage source of the Keithley Electrometer was connected to the bottom surface of the film.

(6) The input probe of the electrometer was in-turn connected to the top surface of the film.

(7) A fixed load was applied to the film, and the voltage detected by the electrometer was recorded on the digitizing oscilloscope as shown in Figure 4-14. The IEEE-
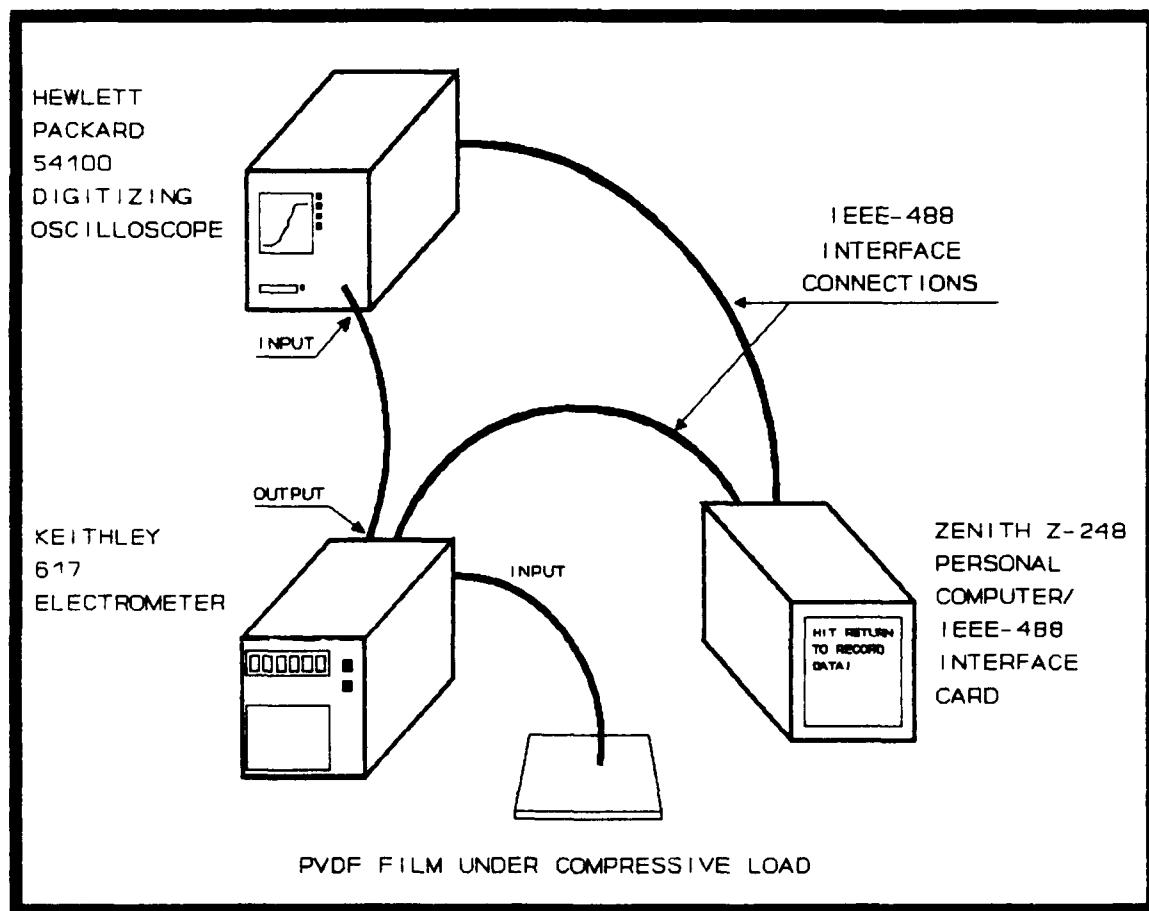
Figure 4-14. Instrumentation for capturing the voltage response of the PVDF film to an applied load.

488 bus was used to transmit this data to a Zenith Z-248

personal computer where the data was stored on disc. The
BASIC computer code used to process the data is listed in
Appendix F. If the signal was positive, then the top
surface of the film was marked to indicate that the metal on
that surface needed to be removed with a wet chemical
etchant.

(8) If the signal detected was negative, the film
orientation was reversed, the load was re-applied, and the
electrometer then detected a positive response signal. The
newly oriented upper film surface was marked for subsequent
etching as described in the following step.

(9) The proper side of the large sheet of PVDF film
was etched with ferric chloride, rinsed in deionized water,
and dried with nitrogen. Then, 6 mm by 6 mm pieces were cut
from the sheet and stored in preparation of the tactile
sensor fabrication.

Tactile Sensor Fabrication.

The size of the integrated circuit (IC) was confined to
an area measuring 7.9 mm by 9.2 mm. Epoxy, acrylic-,
urethane-, and silicon-based liquids used to conformally
passivate printed circuit boards were used as PVDF film
adhesives. Once proper operation of the integrated circuit
was attained, the tactile sensor was fabricated. Initially,
a drop of adhesive from a 3cc syringe was place directly on
the silicon electrode array. These attempts of adhering the
film to the silicon surface of the tactile sensor resulted

4-23

in excess adhesive leaking onto the bond wires of the IC die
and compromising its electrical performance. This was an
undesirable condition because of the adhesive's finite
electrical conductivity. Therefore, the procedure was
modified, and the contoured adherence of the film to the
electrode structure shown in the photograph in Figure 4-15
was obtained consistently.

The revised PVDF film attachment procedure was
implemented using the following process:
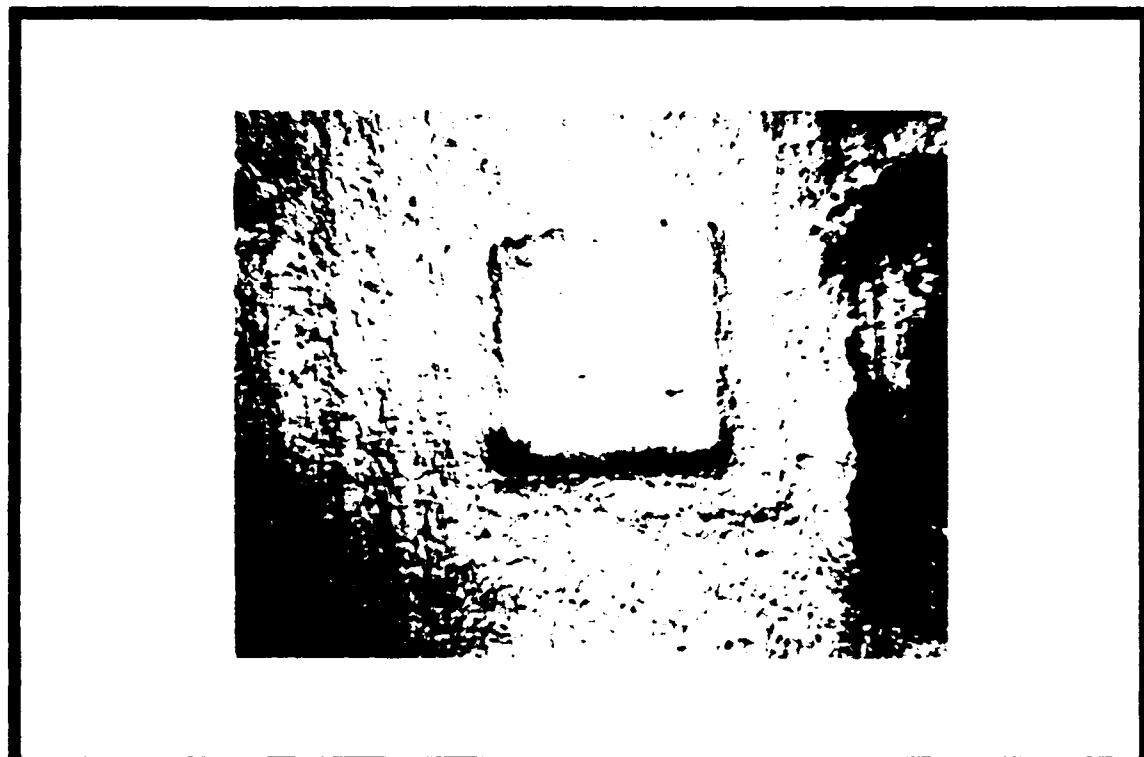
Figure 4-15. Photograph illustrating the strong impression of
the metal electrode beneath the attached PVDF film.

(1) The charge on a 6 mm by 6 mm PVDF film sample was
neutralized by immersing it in an electrically-grounded

solution composed of 200 ml of de-ionized water and 1 drop of HCl.

(2) Nitrogen gas was used to thoroughly dry the PVDF film.

(3) One drop of silicon oil was centered on a 6.5 mm by 6.5 mm glass slide and spun at 5000 RPM for ten seconds.

(4) One drop of adhesive from a 3 cc syringe was placed in the center of the film and spun at 5000 RPM for 15 seconds to produce a thin film of adhesive on the PVDF film.

(5) The square piece of PVDF film and glass slide were transferred to and properly centered on the taxel array.

(6) To ensure proper bonding of the PVDF film to the taxel array, the IC, film, glass slide, and spacer were sandwiched between the compressive force (F) supplied by a paper binder clip depicted in Figure 4-16.

(7) The entire package was then transferred to the evacuation system and exposed to a pressure of 100 microns of mercury for 30 minutes. This process eliminated trapped molecules from beneath the film and caused it to be snugly drawn against the electrode structure.

(8) The adhesive was then cured at 65 degrees Centigrade for one hour.

(9) The sensor was then examined under an optical microscope to discern the overall quality of the bonded PVDF film (for example, detection of lifted edges or bulges in the film).

The final sensor preparation step was to attach a 1-mil
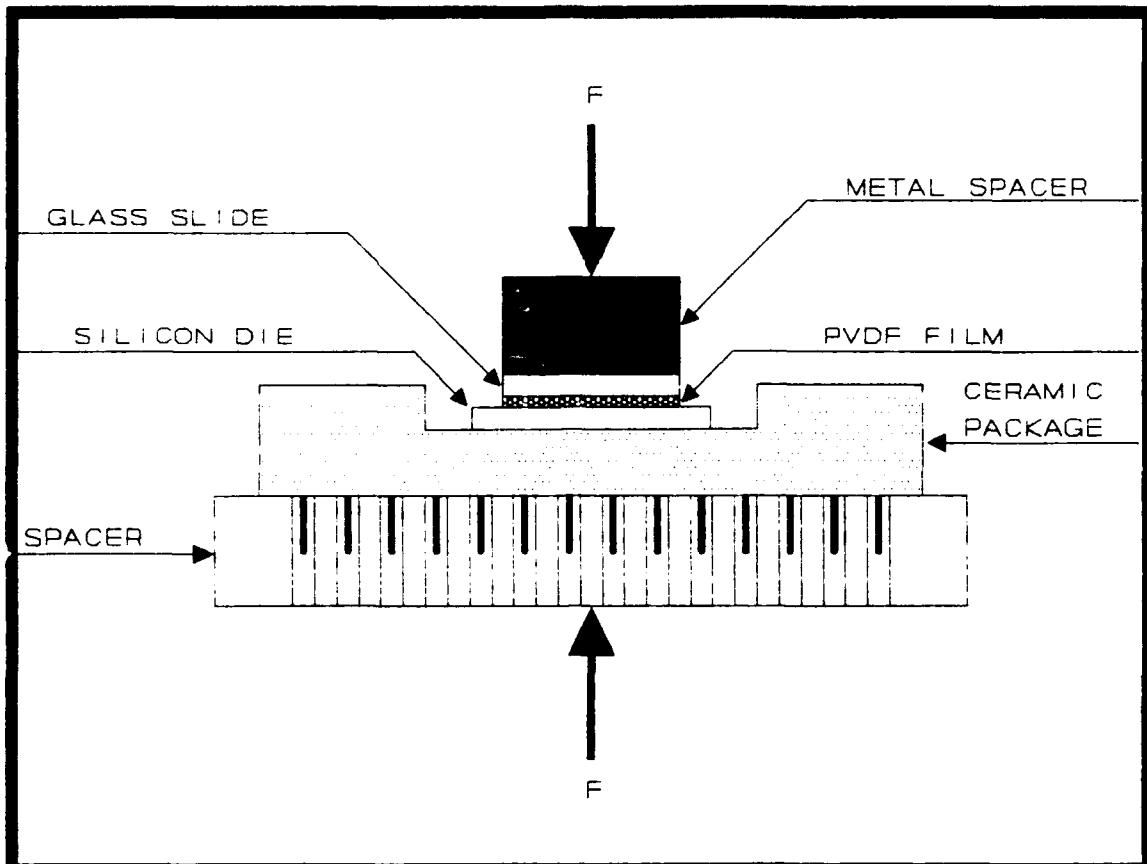
Figure 4-16. Compression technique for bonding the PVDF film to the aluminum electrode array on the silicon die.

wire from the top surface electrode of the PVDF film to a gold wire bond pad on the ceramic package of the IC. Silver paint was used to attach the wire to the top surface electrode. The other end of the wire was then wire bonded to the gold bond pad. The completed integrated circuit, minus the attached PVDF film, is shown in the black-and-white photograph of Figure 4-17. Figure 4-18 is a black-and-white photograph of the completed tactile sensor.
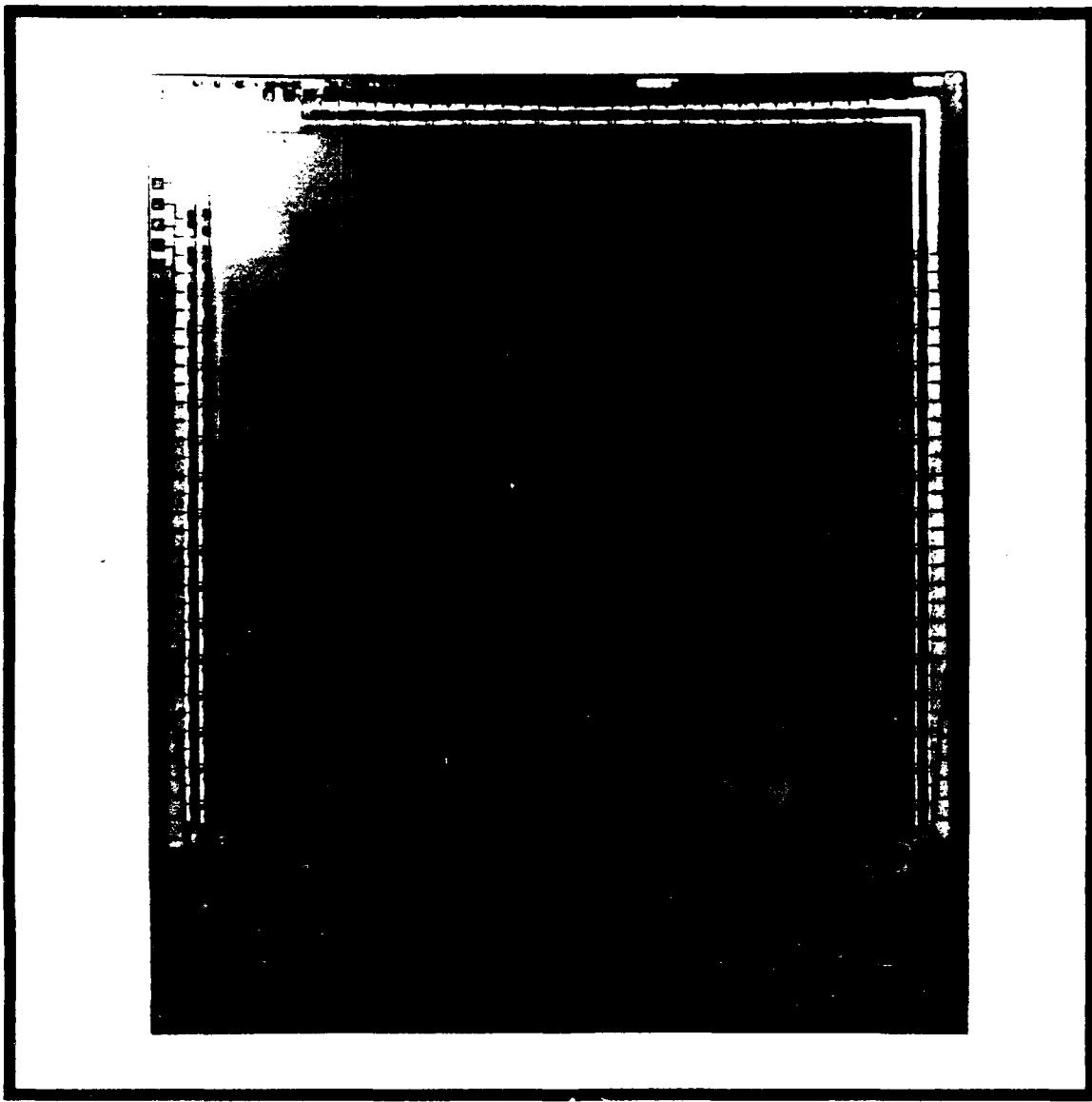
Figure 4-17. Black-and-white photograph of the integrated circuit die prior to attachment of the PVDF film.
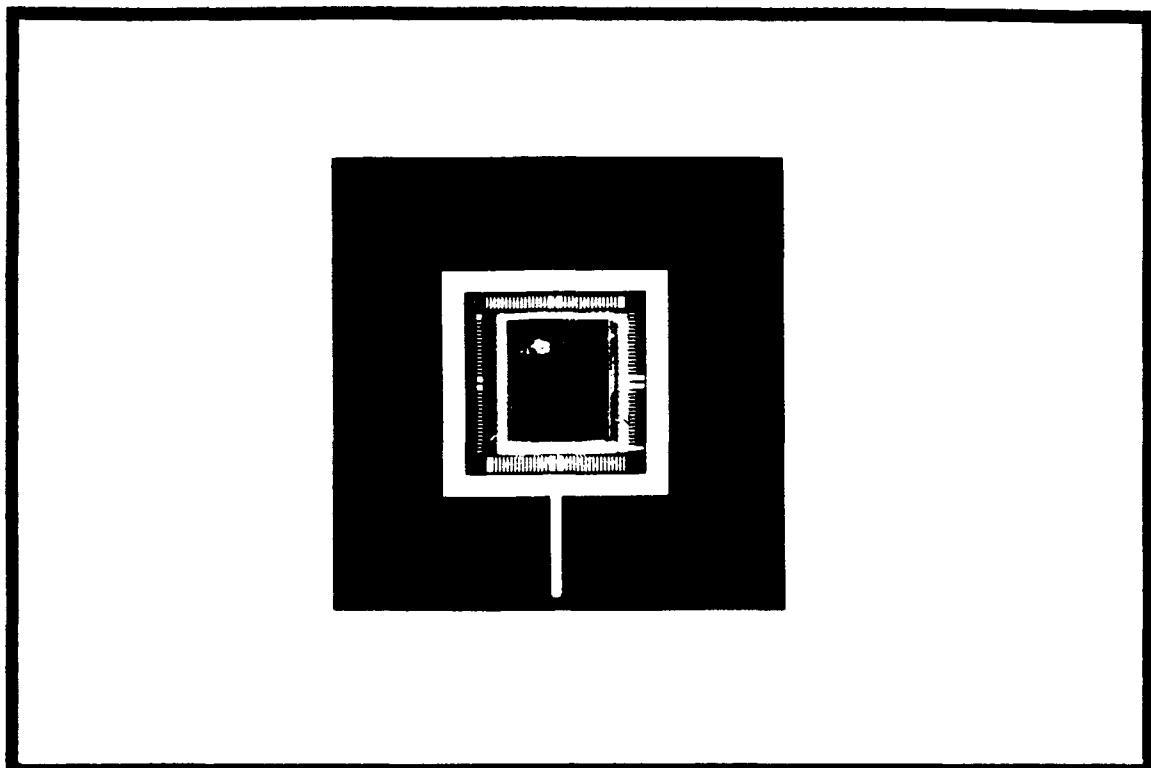
Figure 4-18. Black-and-white photograph of the completed
tactile sensor.

V. Test and Evaluation Procedures and Experimental Results

This chapter discusses the test and evaluation procedures implemented to initially analyze the performance of the integrated circuit (IC). Once the PVDF film was attached to the tactile sensor's electrode array, the performance of individual taxels and a small cluster of three taxels was evaluated. The results of these experiments will be discussed in detail. A discussion of the performance of the adhesives utilized is also included.

Integrated Circuit Performance Evaluation Procedures

The ICs received from MOSIS underwent a rigorous visual inspection, followed by a comprehensive electrical performance test and evaluation process. The first task involved inspecting the ICs for visible defects, such as broken or missing wire bonds; an optical microscope enhanced the inspection process. An initial sample lot of eight ICs was inspected, and no defects were detected except for some minor scratches on the electrode array. The array has no passivation layer (that is, a glass layer was specified in the CIF file) to facilitate the attachment of the PVDF film. Therefore, proper handling care was utilized throughout all the IC performance tests.

Next, the major components of the tactile sensor (amplifiers, multiplexer, and clock) were evaluated for proper

operation. The MOSFET amplifiers were analyzed first, followed by the multiplexer, and finally, the clock.

MOSFET Amplifiers. The expected theoretical DC operating point of the amplifiers was determined by using a Multimeter (Fluke, model 77/AN) to determine the amplifier's resistor values. The resistance values of 80 resistors were recorded (ten resistors from each IC), and their average value was 4100 Ω. To determine if this value would degrade the theoretical response of the amplifier, the 5000 Ω value utilized in the amplifier SPICE model discussed in Chapter IV was replaced by the 4100 Ω value. The results indicated no change in the amplifier's response.

A Semiconductor Parameter Analyzer (Hewlett Packard, model HP 4145) was used to apply a linear signal (increasing from 0 to 10 volts) to amplifier number-30 on chip number-1 and to measure its output characteristics. This amplifier corresponds to electrode number-30 as shown in Figure 4-1. The results were recorded on a computer disc using the test configuration shown in Figure 5-1. The BASIC computer program utilized to implement this test and to collect the data is listed in Appendix F.

These characteristics were then compared to the SPICE analysis performed during the sensor's design. The initial results indicated that the amplifier was not performing correctly, as shown by the results plotted in Figure 5-2. Although the input/output curve has the expected shape, a careful inspection of the output voltage level reveals that

IEEE-488
INTERFACE
CONNECTION

SEMICONDUCTOR
PARAMETER
ANALYZER

ZENITH Z-248
PERSONAL
COMPUTER/
IEEE-488
INTERFACE
CARD

HIT RETURN
TO RECORD
DATA!

TACTILE SENSOR
UNDER TEST
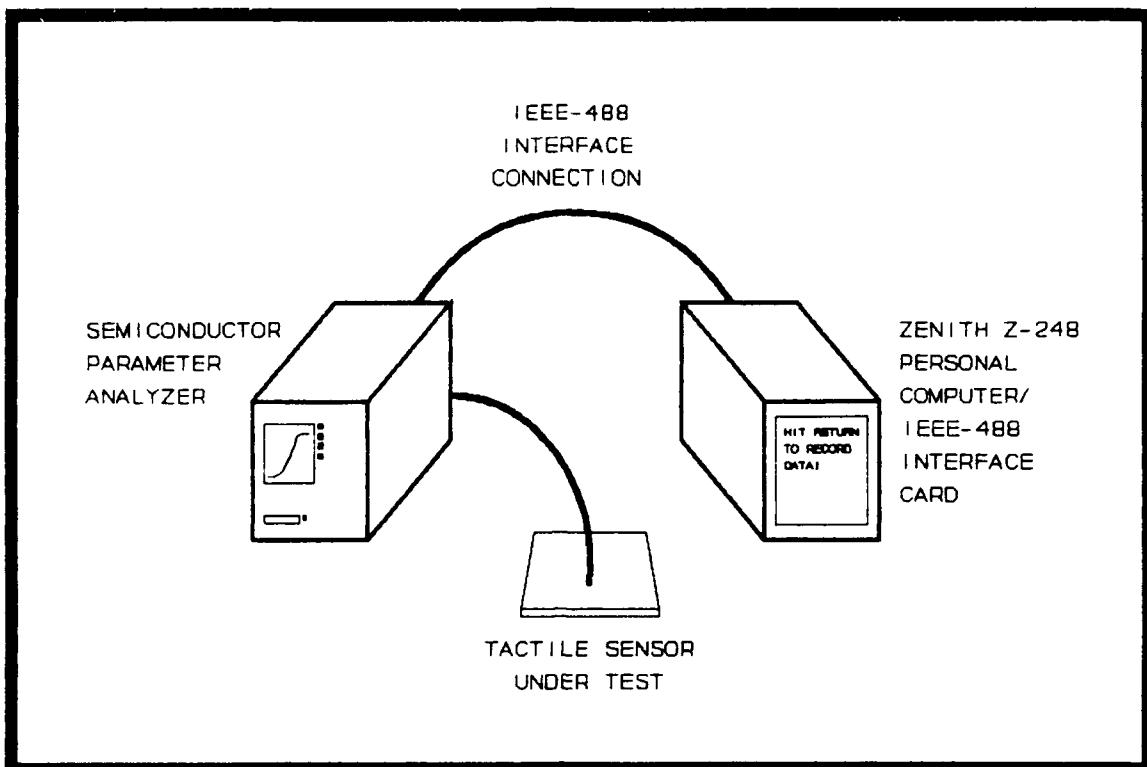
Figure 5-1. Instrumentation for recording the output response
of the charge signal amplifiers.

the amplifier attained a saturation value of only 1.17 volts

for an input level greater than 3 volts. Five additional

amplifiers on chip number-1 and -2 on each of chips number-

2, number-3, and number-4 were analyzed, and they all re-

sponded the same as amplifier number-30. Consequently, a

troubleshooting scheme was implemented to determine why the

amplifiers were not functioning correctly.

The first step in the diagnosis of the amplifier prob-

lem was to determine if the MOSFETs themselves were func-

tioning correctly. In the design process, microprobe test

pads were strategically located next to each amplifier, thus

providing access to the MOSFETs' drain contacts. Using the
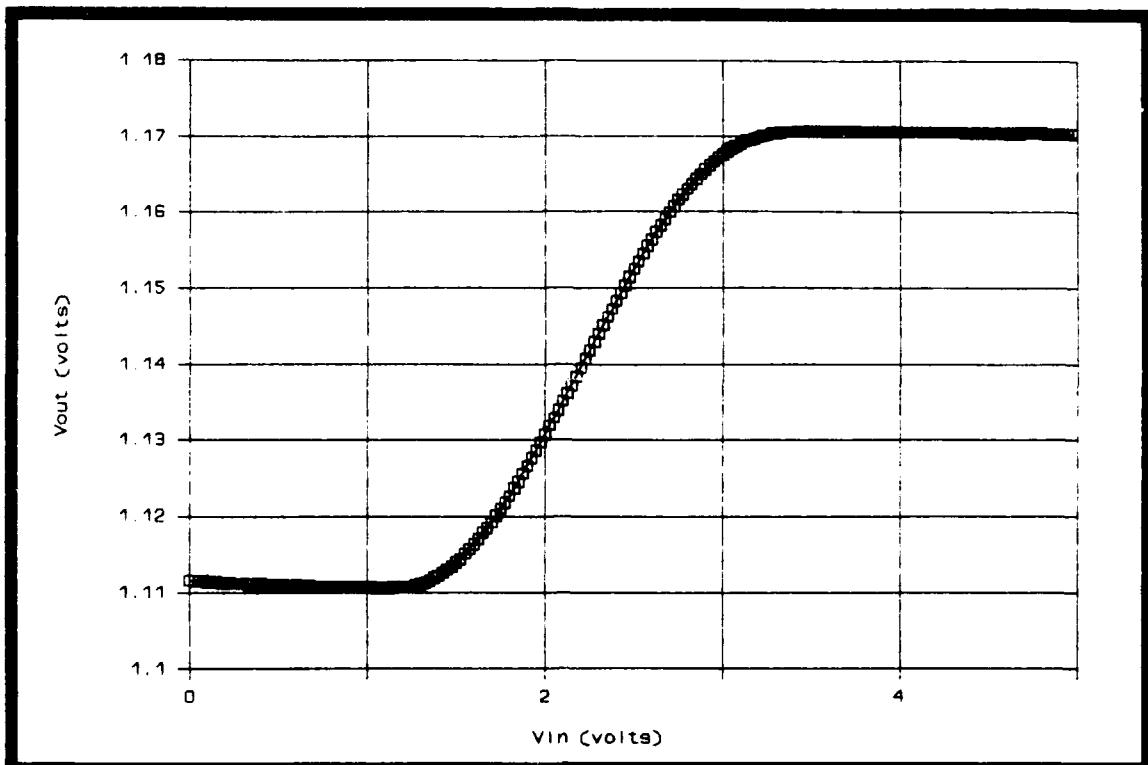
Figure 5-2.   Degraded output response of MOSFET amplifier
number-30 on chip number-1.

micromanipulator probe station, a 0.5 μm diameter microprobe
was gently placed on the exposed metal of the test pads.
The semiconductor parameter analyzer was then used to apply
a drain voltage through this probe connection. A gate
voltage was applied to the input stage MOSFET through the
external pin of the IC package. Similarly, the source of
the transistor was grounded through an external pin connect-
ed to the GND of all the amplifiers. By sweeping the drain-
to-source voltage from 0 to 10 volts for each of five gate
voltages (0, 1, 2, 3, and 4 volts), the MOSFET drain-to-
source voltage versus drain current curves were obtained.
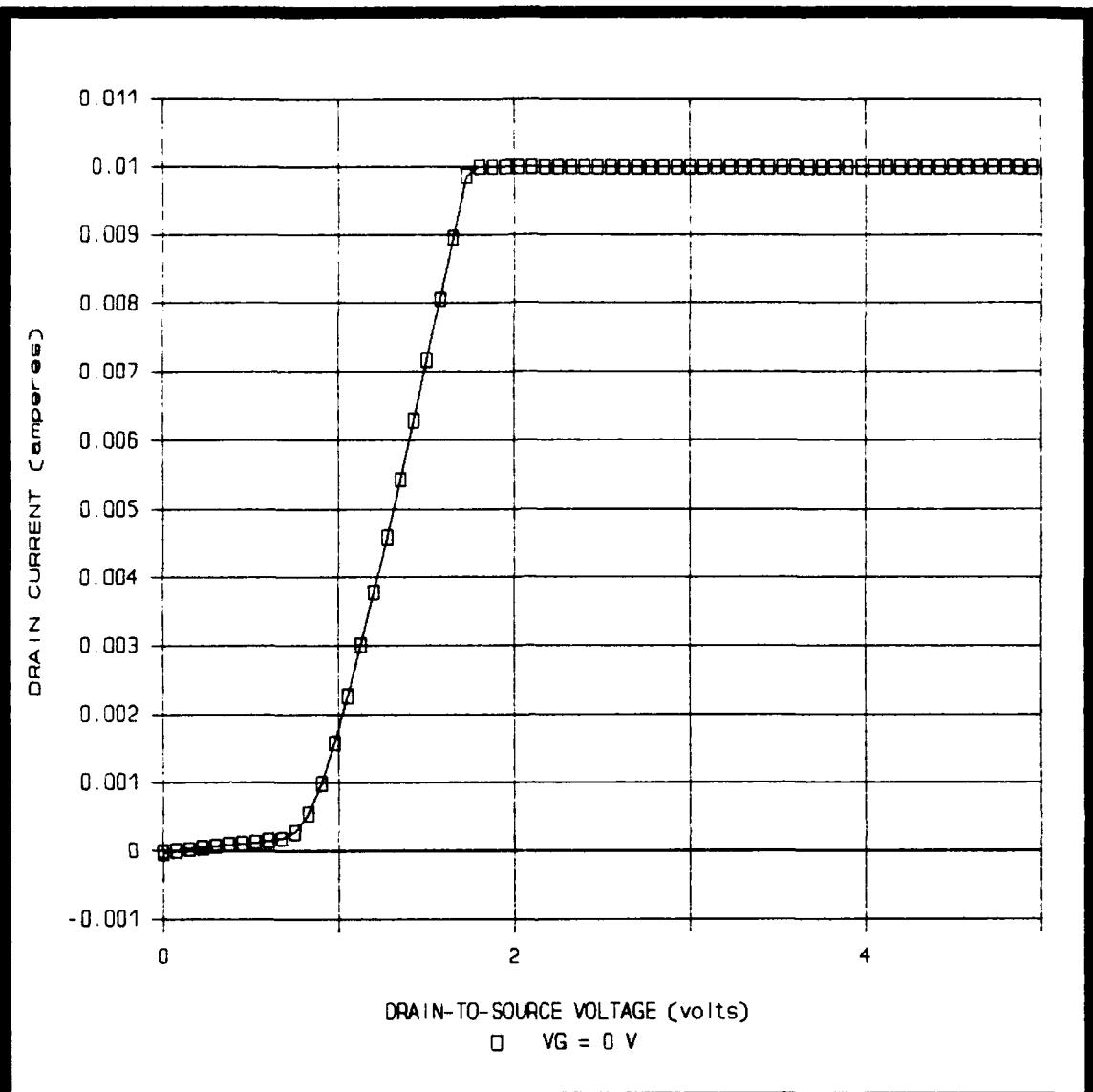
Figure 5-3. Characterization curve for the input stage MOSFET amplifier number-1 of chip number-1 depicting the diode action displayed by the input and output MOSFET transistors.

Figure 5-3 shows the transfer function curve of the input stage MOSFET. The device initially behaved as a MOSFET, but at 0.7 volts, the current rose sharply to the maximum value for the test configuration (10 mA). This diode-effect manifested itself in all of the input stage

MOSFETs examined (5 on each of chips number-1, number-2, and number-3). The output stage MOSFETs were also analyzed, and they displayed the same characteristics. Therefore, either the MOSFETs were incorrectly fabricated or they were being affected by other circuitry on the IC.

Isolation of the individual MOSFETs was required to ensure that they were not being affected by other circuitry on the IC. The MOSFET amplifiers are only connected to the transmission gate array of the multiplexer circuit (that is, the drain of each output stage MOSFET is tied, by way of a metal-1 line, directly to the input of a transmission gate). Consequently, the microprobe station's ultrasonic cutter was utilized to carefully cut through this metal line to ensure isolation from the transmission gate array.

The MOSFET characterization was repeated on the input and output stage MOSFETs. This time, the transistors behaved correctly. The amplifier also operated as expected. An actual comparison of the amplifier response curve with the SPICE analysis reveals insignificant degradation in the output level of the amplifier. Figures 5-4 and 5-5 show the typical response for all of the transistors and amplifiers when the amplifier output lines could be totally severed from the transmission gate array.

Cutting this metal-1 line proved to be a very challenging task in 'silicon microsurgery'. If the cut was made too deep, the metal line was connected to the substrate, since metal-1 is only insulated from the n-type silicon substrate
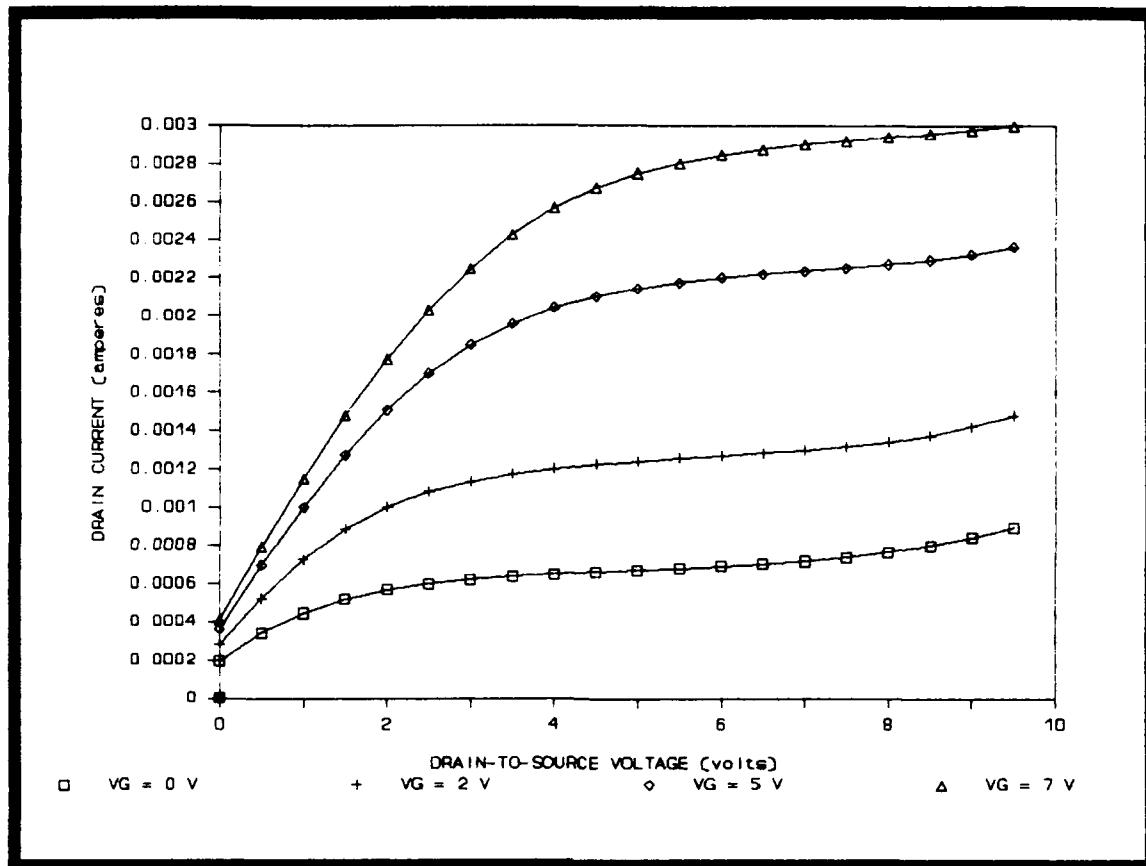
Figure 5-4. Characterization curve for the isolated input stage MOSFET transistor of amplifier number-20 on chip number-1.

with a thin layer of SiO_2. If the cut was not made deep enough, the metal line was not severed.

It is noted that prior to making any cuts in the silicon, the analog multiplexer circuit was evaluated to determine if the transmission gate array could be totally turned off, which would essentially produce the same effect as isolating the transmission gate array from the amplifier. However, as discussed in the next section, the transmission gate array could not be turned off.
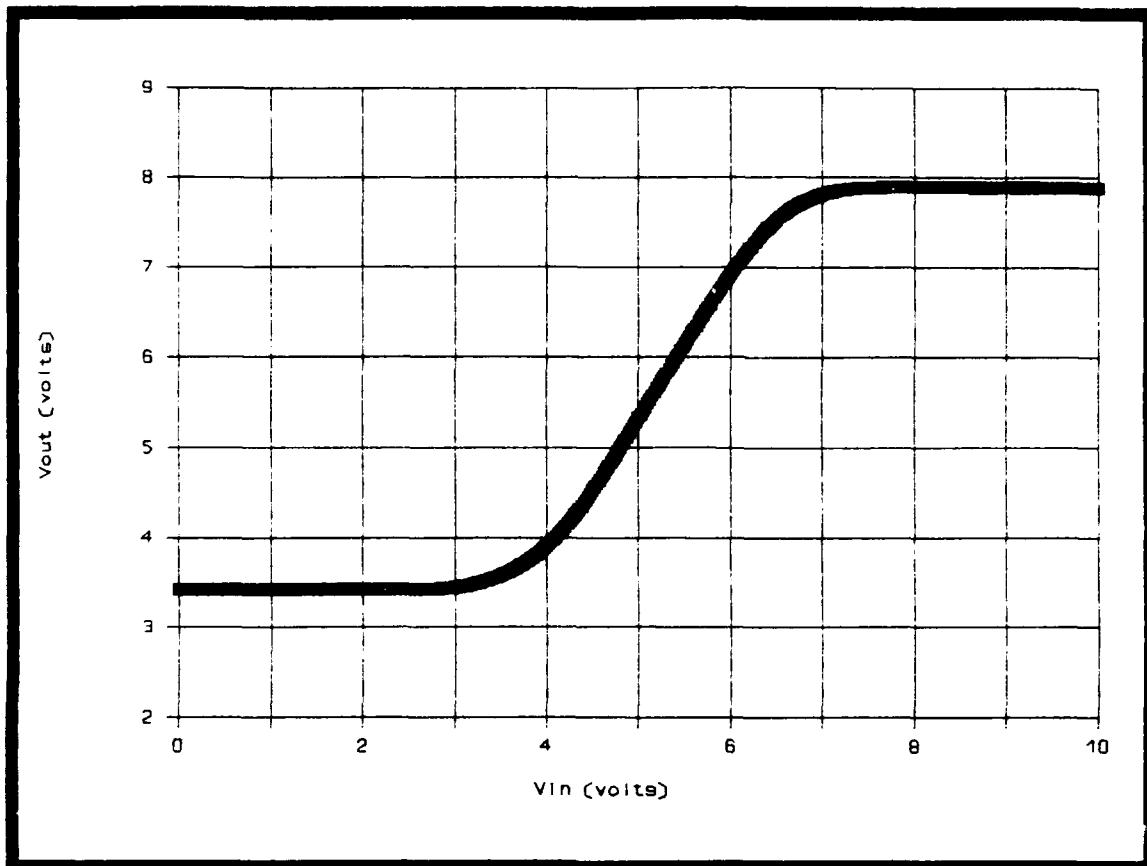
Figure 5-5. Response curve of MOSFET amplifier number-7 on chip number-2 after being severed from the transmission gate array.

Analog Multiplexer Circuit. The multiplexer circuit requires a 10 volt power supply for the ring counter portion of the circuit. The integrated circuit was fabricated using the MOSIS, 2-micron, p-well process; therefore the n-type substrate was tied to 10 volts. The p-wells were tied to ground, thereby reverse biasing the pn-diodes which exist between the p-wells and the substrate. The transmission gate array was similarly supplied with power and ground connections.
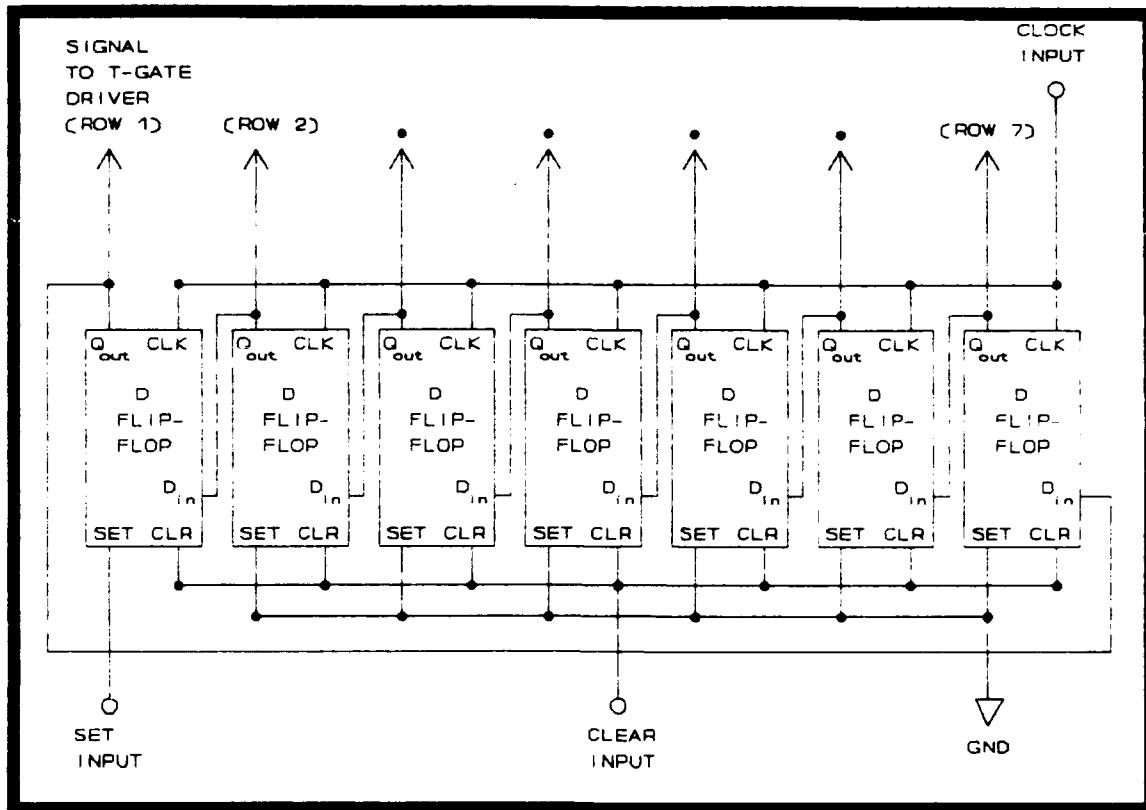
Figure 5-6. Ring counter configuration to generate row-select signals.

To test the operation of the multiplexer circuit, the SET line shown in Figure 5-6 was tied low, and the CLEAR line was tied high in an attempt to clear all the flip-flops. Any residual charge on the gates of transistors due to the fabrication process can cause an undesirable initial condition in the ring counter, thus affecting the transmission gate array's initial state. Clearing the ring counter should have eliminated this condition.

A 1 Hz clock signal was applied to the clock port of the multiplexer, and the output of the first flip-flop in the row ring counter was monitored on the digital storage

oscilloscope. The output stayed low, which was a correct response. Next, the CLEAR input was tied low, and the SET input was tied high for one clock pulse to initiate a high input state which would cycle through the ring counter. However, even when the SET input was tied high for several clock cycles, the output went high only when the SET line was high. The clock pulse had no effect on the flip-flop action.

The output of this flip-flop was designed to provide the clock signal for the column ring counter. Without the proper operation of this flip-flop, the multiplexer circuit had no chance of operating correctly. The flip-flop design was fabricated in a separate MOSIS fabrication run; therefore, the flip-flop will be further analyzed to determine the source of the problem.

Clock Circuit. Evaluation of the clock circuit revealed positive results. The clock circuit was evaluated after connecting an external resistor/capacitor (RC) network to the integrated circuit. The digital storage oscilloscope was connected to the output of the clock circuit to record the clock's oscillation frequency. This data was recorded with the same test configuration used to characterize the PVDF film.

Various RC networks were evaluated to determine if the circuit would oscillate in the range spanning 1 Hz to 1 Khz. Figure 5-7 is a display of the clock output for R_1 = 5 KΩ, R_2 = 100 KΩ, and C = 100 nF. The displayed frequency is 59
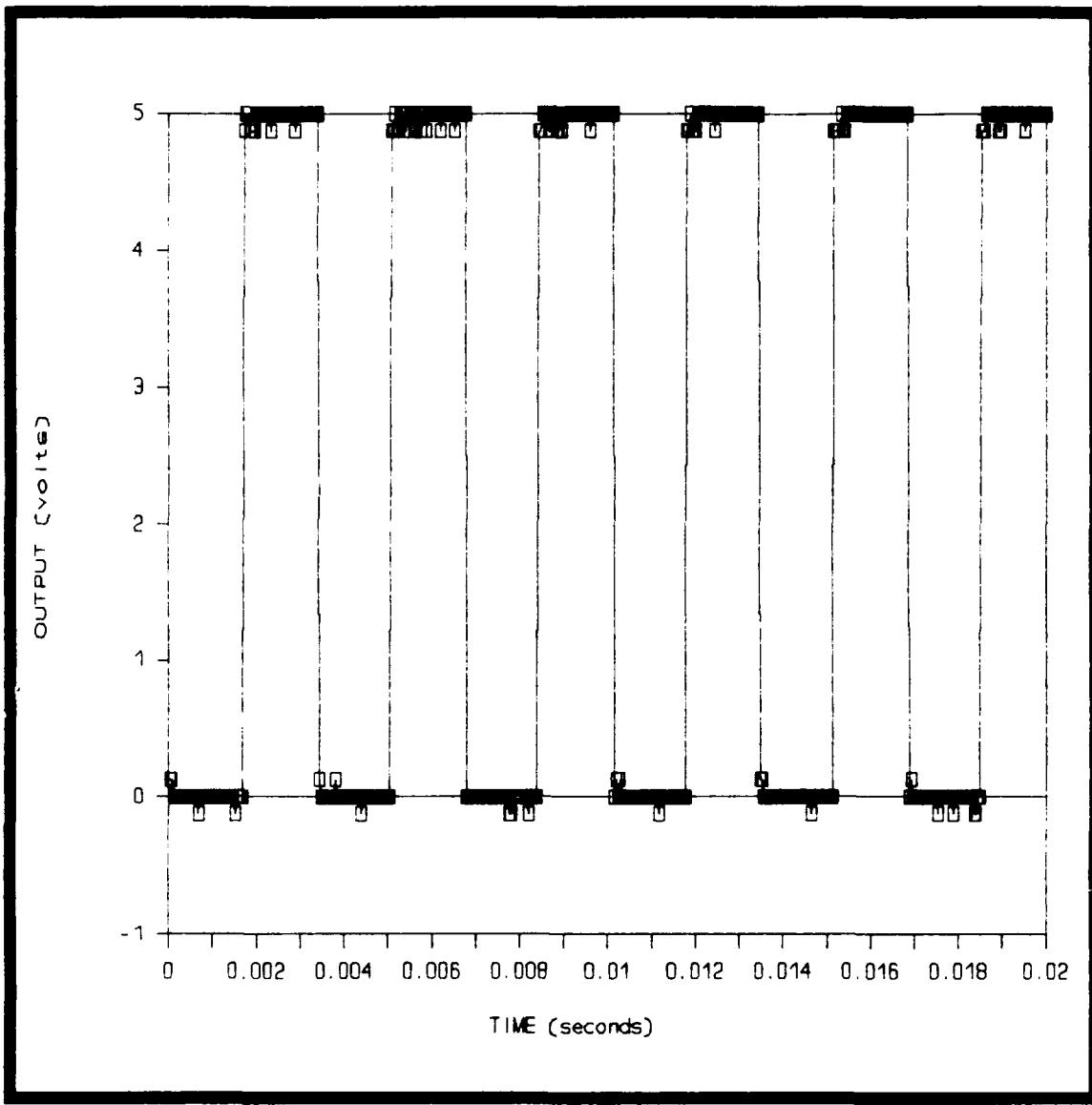
Figure 5-7.   Timing   waveform   produced   by   the   555-timer
circuit.

Hz (a clock period of 0.0169 s). Using the formulas shown

in Figure 4-8, the period of the signal for the above values

is calculated as follows:

$$T = T_1 + T_2 = 0.693(R_1 + R_2)C + 0.693(R_2C) \; s$$

$$T = 0.693(150 \; K\Omega)(100 \; nF) + 0.693(100 \; K\Omega)(100 \; nF)$$

$$T = 0.01039 + 0.0069 = 0.0172 \; s$$

This period corresponds to a frequency of 57.7 Hz which agrees very closely with the measured value. Nine tests were run with various RC networks, and the maximum oscillation frequency measured was 116 KHz. The pulse width of the clock pulse could be varied by changing the sizes of resistors R_1 and R_2. Duty cycles spanning 35 to 50 percent were measured.

Tactile Sensor Testing

Following the proper performance verification of the amplifiers, the tactile sensor was fabricated as previously described. The first set of ICs (number-1 through number-8) were used to refine the PVDF film adhesion process. The metal-1 output lines on ICs number-9 through number-16 were severed with the ultrasonic cutter, and the film was attached with urethane adhesive. Of these eight sensors, two (number-14 and number-16) resulted in testable devices (that is, a 3 x 3 array of taxels in the center of the array functioned correctly). Tactile sensor testing then proceeded in four stages: (1) PVDF film charge state tests; (2) individual taxel load response characterization; (3) electrode crosstalk tests; (4) shape recognition test with DC biased amplifiers.

PVDF Film Charge-State Tests. The initial charge state for a 3 x 3 electrode array was evaluated by multiplexing the outputs from these nine amplifiers and displaying the response on the digital storage oscilloscope. The
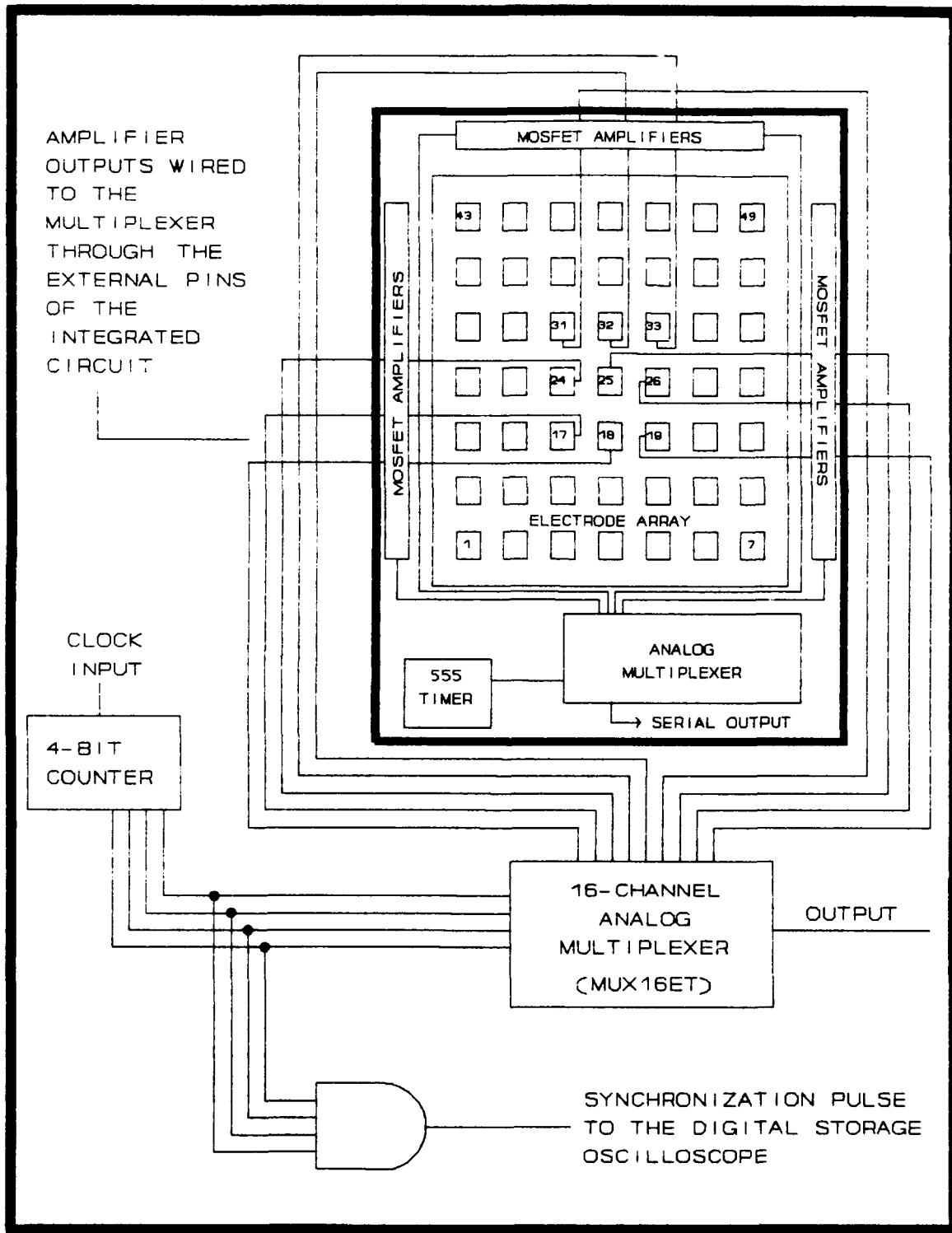
Figure 5-8. Schematic drawing illustrating the 3 x 3 taxel array and their associated MOSFET amplifiers with connections to the external analog multiplexer circuit through pin-outs on the IC package.

analog multiplexer circuit shown in Figure 5-8 was imple-
mented on a digital logic, solderless breadboard, and the
multiplexer was clocked at 1000 Hz.

The nine taxels evaluated are also shown in Figure 5-8.
Three amplifiers from the left and right columns, and three
from the top row of amplifiers were used. The synchroniza-
tion pulse from the TTL logic circuitry provided the trigger
for the digital storage oscilloscope. The order in which
the taxels were sampled by the multiplexer was: 18, 17, 24,
33, 32, 31, 25, 26, and 19.

The multiplexed output is shown in Figure 5-9 for chip
number-16. A 0.9 volt variation in an electrodes' initial
charge state was observed, therefore a 2-volt dc bias signal
was applied to each of the nine electrodes in an attempt to
equilibrate the charge state of the array. This variation
was due to the voltage drop in the V_{dd} line supplying power
to the 49 amplifiers.

However, when the input bias was removed, it was noted
that the output of each amplifier quickly dropped to its
value before the input bias was applied. This behavior
indicated that the charge placed between the PVDF film and
the gate input of the MOSFET was quickly being dissipated.
Subsequent load tests of individual taxels revealed that
loads in excess of 300 grams were required to elicit a
response from the taxel.

Figure 5-10 depicts the rapid decay rate of a taxel's
output after a 10-volt bias input has been removed. The
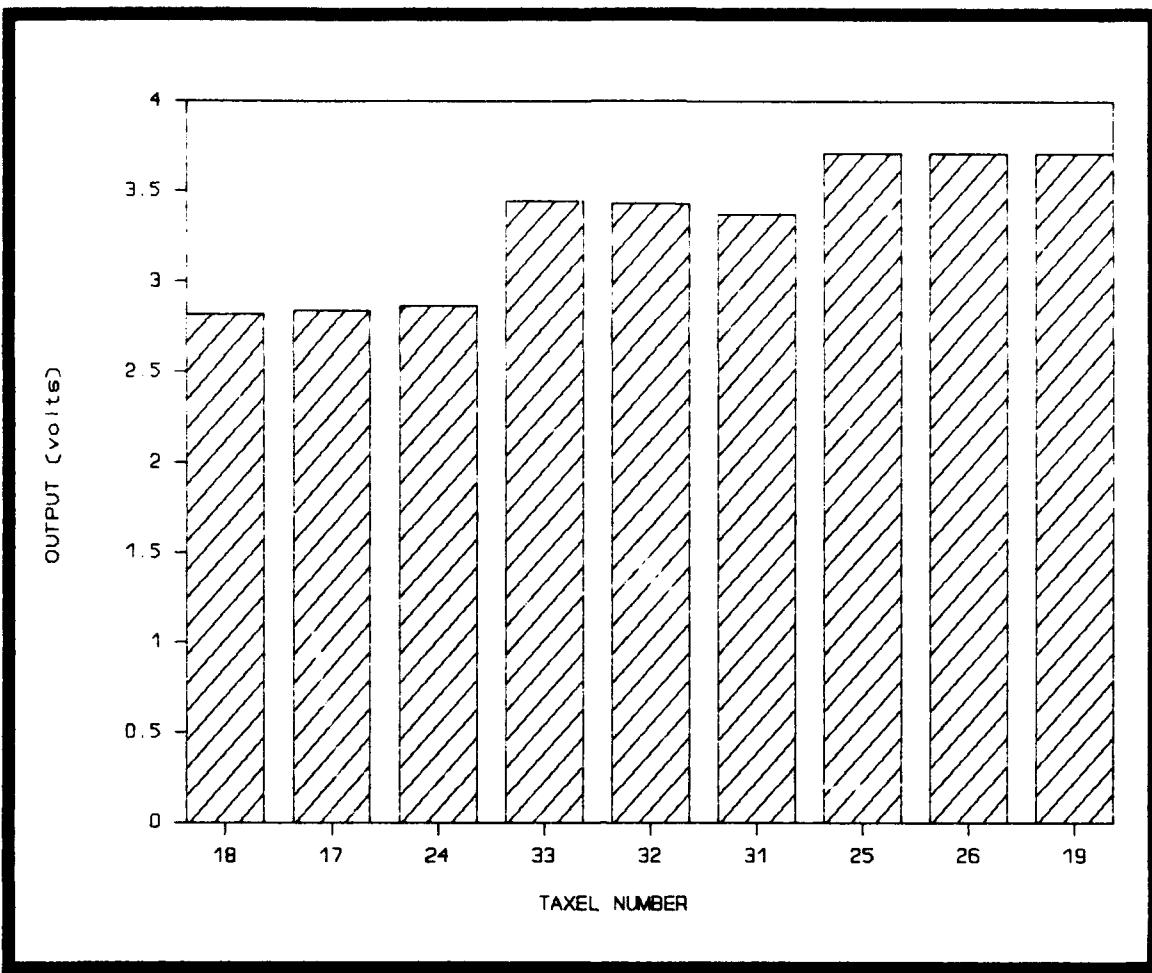
Figure 5-9. Multiplexed output of the 3 x 3 array of taxels
numbered 18, 17, 24, 33, 32, 31, 25, 26, and 19.

response of the taxel to a variable load (one which oscil-

lates between 0 and 300 grams) is shown in Figure 5-11. As

depicted in the plot, the taxel became sensitized during

this decay period, but the applied load sensitivity is much

less than the required level of 1 to 3 grams. The superpo-

sition of the decay rate observed in Figure 5-10 onto Figure

5-11 indicates that the load force had minimal effect on the

charge leakage rate.
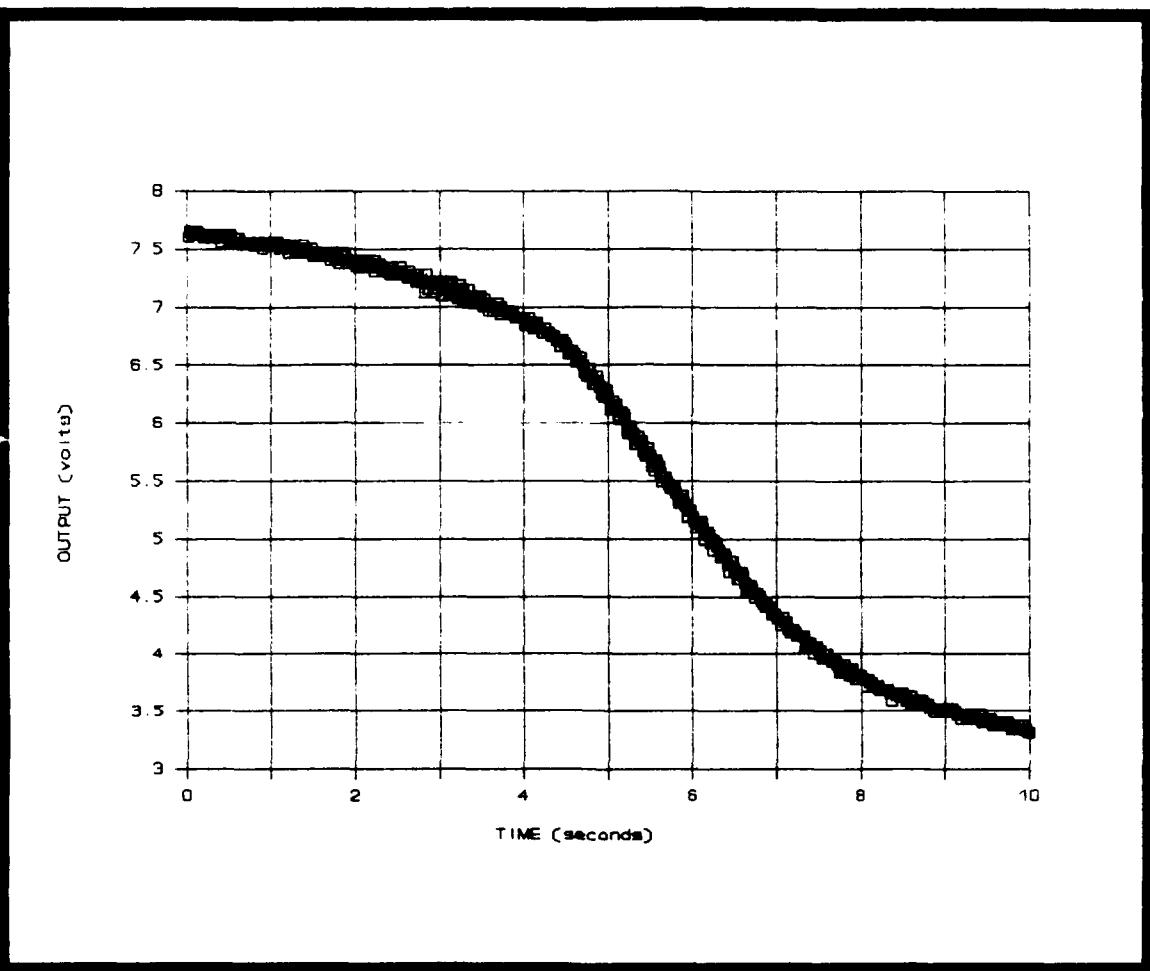
Figure 5-10. Output signal decay for MOSFET amplifier
number-23 on chip number-5 indicating a rapid charge leakage
rate.

Diagnosis of Charge Leakage Phenomenon. A solu-
tion to the charge leakage problem, presumably caused by an
undesirable resistance path to ground, was to locate and
eliminate that path. The path could have existed on the IC
die, or since the electrodes were all connected to off-chip
reed switches, the path could also have existed off-chip.

The resistance path from the IC's MOSFET gate contact
to the external reed switch, illustrated in Figure 5-12, in-
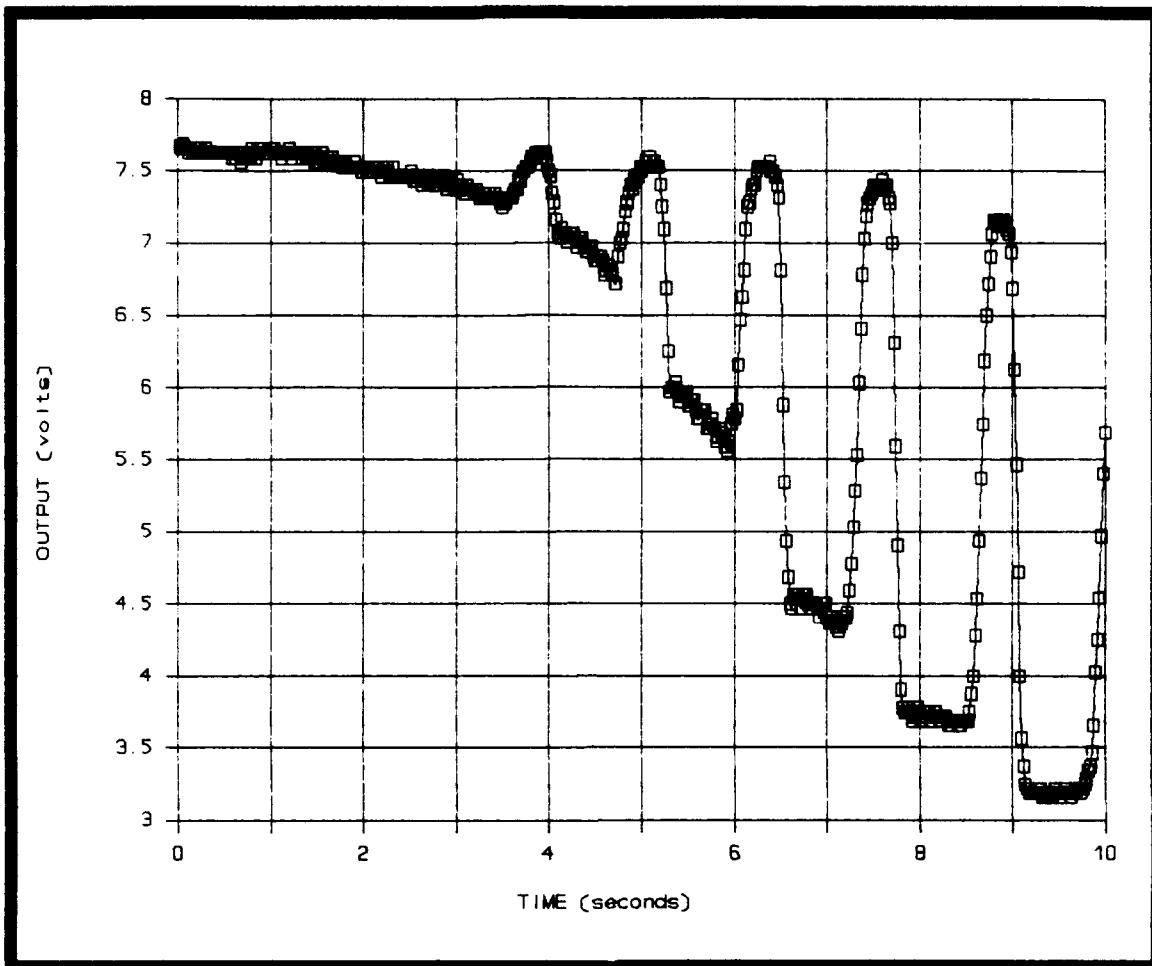
Figure 5-11. Response of taxel number-23 on chip number-5 to a variable load (one which oscillates between 0 and 300 grams) after removing an applied dc-bias of 10 volts.

cluded the following components: taxel electrode, metal run from the electrode to the on-chip wire bond pad, on-chip wire bond pad, 1-mil wire bond, gold wire bond pad on the IC ceramic package, 132-pin grid-array IC socket, printed circuit card, ribbon cable, and reed switch. Therefore, working towards the electrode from the reed switch, components were sequentially removed, and the response was re-evaluated. Removing the reed switch, ribbon cable, printed circuit
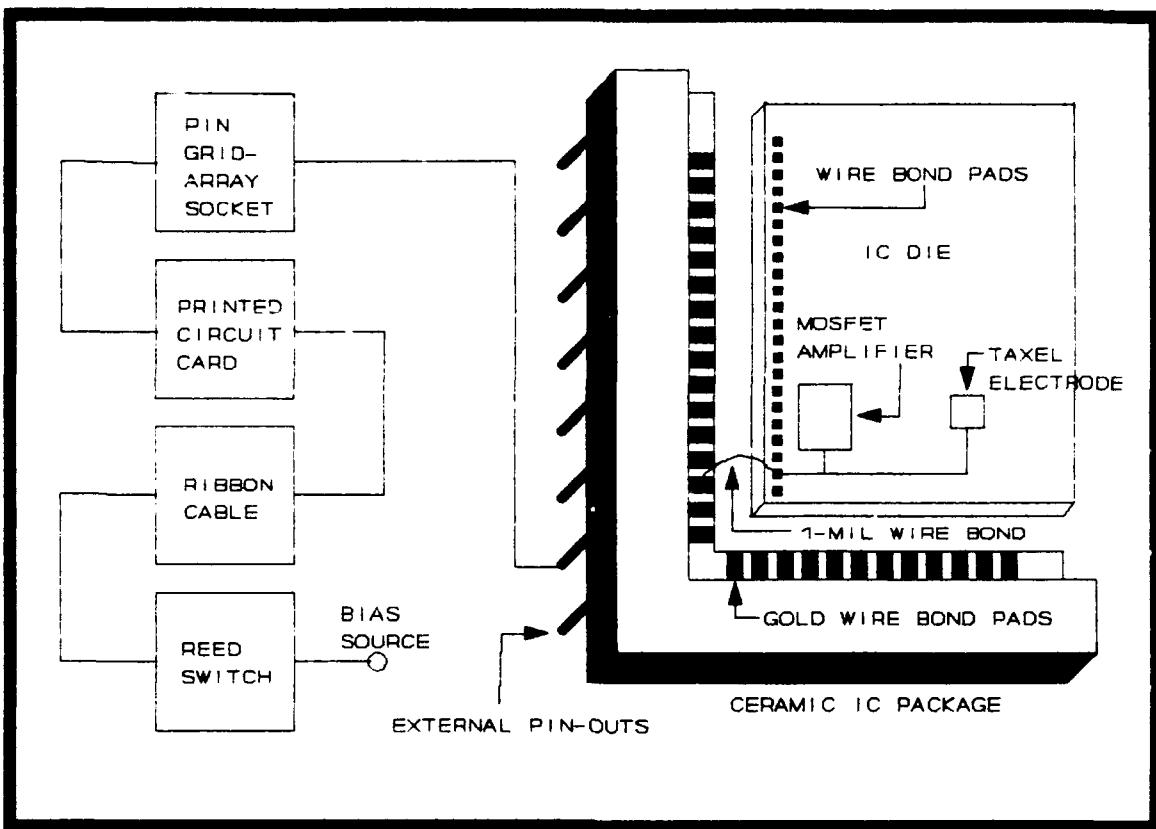
Figure 5-12. Components included in the resistance path from the external reed switch to the taxel electrode.

card and IC socket had no effect on the observed, initially marginal performance of the taxels.

The only connection remaining was the 1-mil wire bond, and that was the answer. Removal of the wire bond resulted in fully functional taxels; the charge did not leak at the previously astounding rate. This situation meant that the charge was leaking from the IC die through a resistance path within or on the surface of the IC ceramic package itself.

The final step was to locate this resistance path using the electrometer. The resistance between the gold wire bond pads located along the periphery of the chip cavity of the

IC package varied from approximately 10^7 Ω to 10^{12} Ω. These
pads were isolated from the silicon die because the wire
bonds to these pads from the die were removed. This resis-
tance caused an impedance mismatch between the PVDF film and
that between any two gold wire bond pads. Any charge gener-
ated by the film simply leaked through the conductive path
between the gold wire bond pads.

Further analysis revealed the probable cause of this
resistance path. Acetone was used to purge the silicon
surface of any debris prior to attaching the PVDF film to
the electrode array structure. The debris resulted from the
ultrasonic probe cuts made into the silicon to isolate the
transmission gate array from the amplifiers. Also, initial
attempts to attach the PVDF film were not always successful;
therefore, the adhesive remaining on the silicon die had to
be removed. Once again, acetone was used to remove the
adhesive. In both cases, when the acetone dried, it depos-
ited a residue of particles on the IC package. These parti-
cles provided a leakage path for the charge generated by the
PVDF film.

Therefore, an IC package which had not been processed
through the tactile sensor fabrication steps was analyzed to
determine the resistance between adjacent gold, wire bond
pads. The resistance was consistently on the order of
10^{13} Ω, the same value found when the bond wires were re-
moved from a processed sensor. Thus, by removing the wire
bonds connecting the taxel electrodes to the external cir-

cuitry, the taxels operated correctly and were character-
ized, as discussed in the next section.

Taxel Characterization Tests. The voltage re-
sponses of 15 taxels (six from chip number-14, and nine from
chip number-16) were recorded for loads ranging from 3 grams
to 81 grams. The adhesive used to attach the film for both
of these sensors was urethane (Miller Stephenson Chem. Co.,
urethane coating MS-472). Figure 5-13 illustrates a cross-
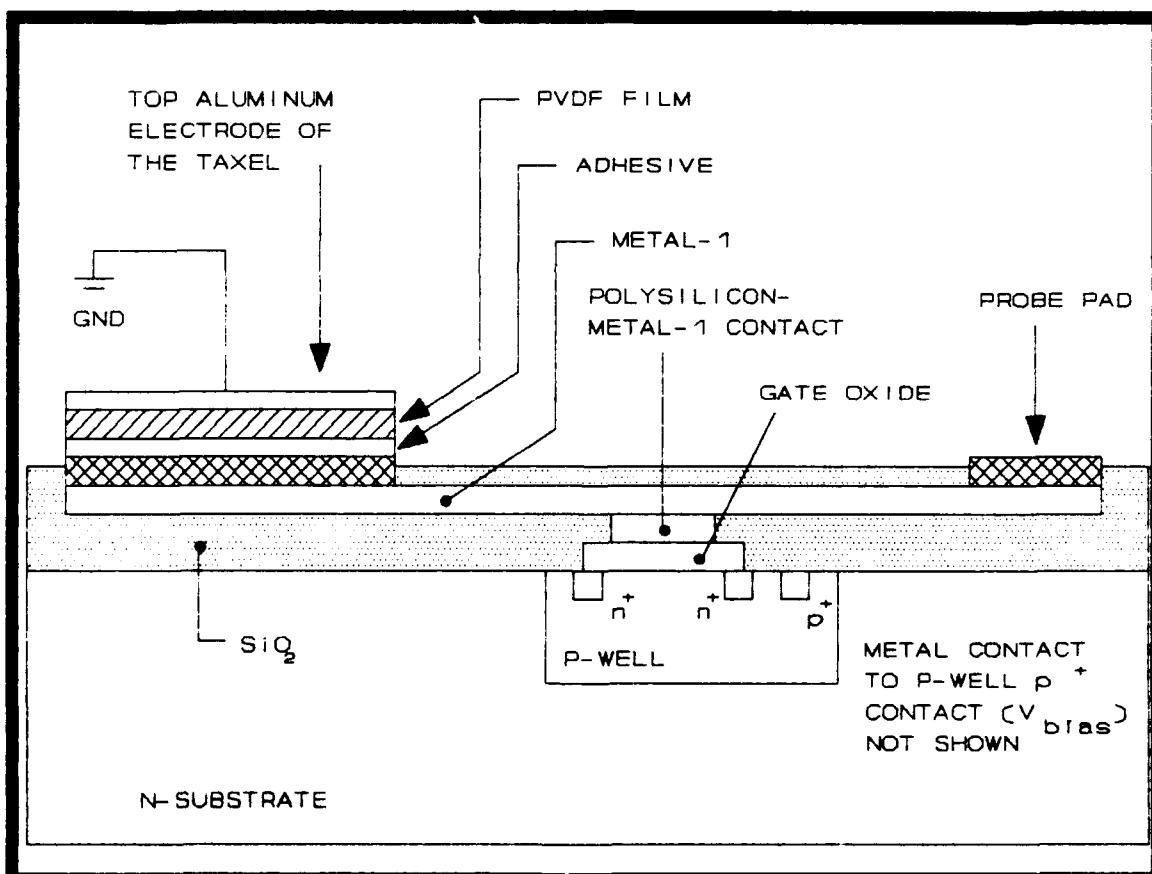
Figure 5-13. Cross-sectional view of the PVDF film attached
to a taxel electrode with its metal connections to the
amplifier's input gate contact and probe pad.

sectional view of the silicon die with the PVDF film attached to the taxel electrode.

The top surface of the PVDF film was grounded, as was the p-well containing the charge-signal amplifiers. The diagram shows the input stage MOSFET's gate contact and its associated probe pad. A taxel was biased by touching a charged microprobe to this 100 μm by 100 μm probe pad which connects to the taxel electrode. When the microprobe was removed, the charge remained trapped between the high impedance of the amplifier's gate input and the large impedance of the PVDF film. The duration which the charge remained trapped was a function of the quantity of charge injected.

The response of taxel number-24 on chip number-16 is illustrated in Figure 5-14. Here a 4-volt dc bias was applied to the taxel for one second, after which a 40-gram load was applied. Three tests were performed, and the equilibrated response in each case was 7.5 volts. Appendix G presents the response of this taxel to a 40-gram load for bias voltages of 1, 2, 2.5, and 3 volts (Figures G-1, G-2, G-6, and G-3, respectively). In all cases, the bias voltage was applied for one second, and then it was removed.

Analysis of the curves in Figure 5-14 reveals that the load was applied at time zero. The taxel output rose to 7.5 volts, indicating a taxel response time of approximately 0.75 seconds. For tests 1, 2, and 3, the load was removed at different times, but in all three cases, the response decayed to its equilibrium value in approximately 1.5 sec-
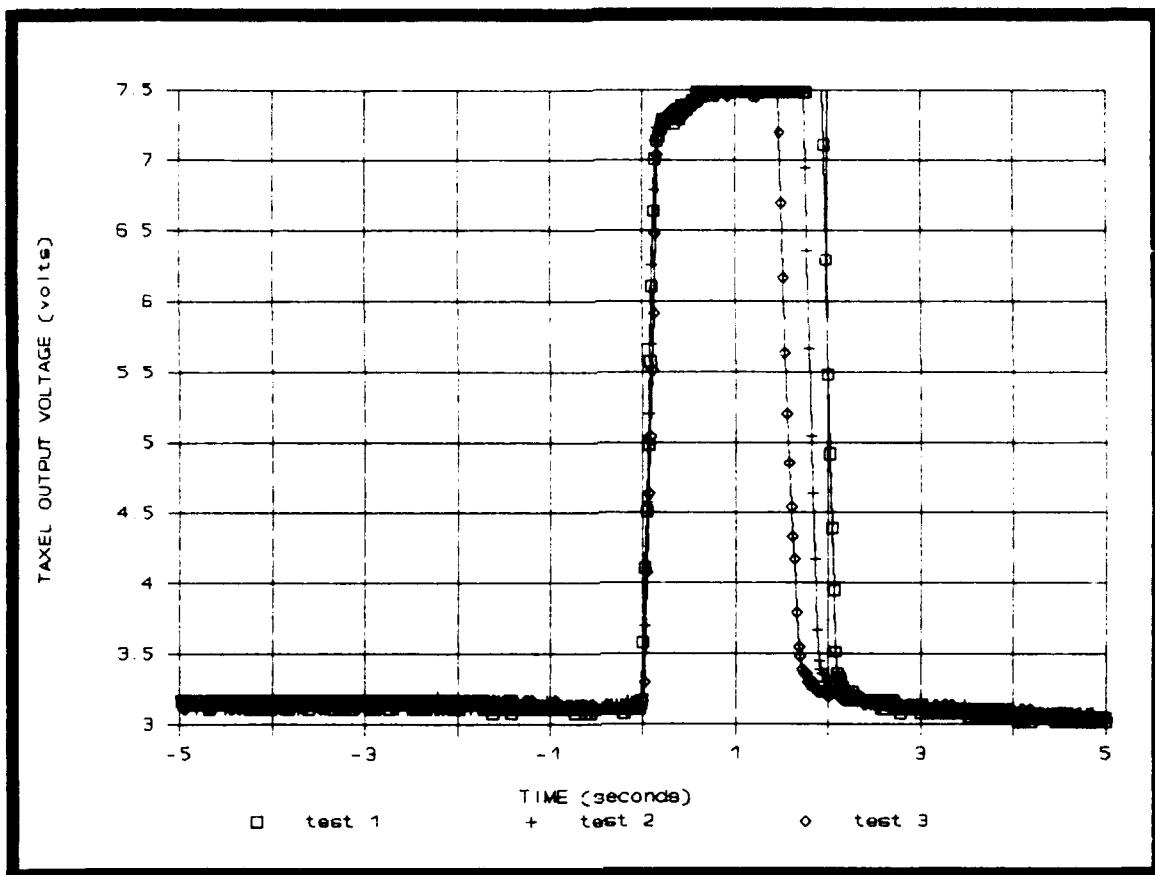
Figure 5-14. Response of taxel number-24 on chip number-16 to a 40-gram load for a 4-volt bias signal (for the three tests shown, the load was applied at time zero and then removed approximately 1.75 seconds later).

onds (recovery time).

PVDF Film Biasing Considerations. A 10-volt dc bias, applied to the electrode for one second, resulted in the taxel remaining active for approximately three minutes. A 2.5-volt dc bias, applied for one second, created one minute of activity. In addition, the 2.5-volt dc bias level produced the most linear and largest dynamic range of voltage output. At this bias level, loads ranging from 3 to 81 grams could be discerned. Bias signals smaller than 2.5

volts created a taxel which could detect larger forces before the amplifier output reached its saturation value of 7.6 volts. However, the minimum force which the taxel could resolve increased above 3 grams. Bias signals greater than 2.5 volts created a very sensitive taxel (one which could detect 1 gram loads), but the amplifier reached saturation below the 81-gram level.

Figure 5-15 shows a linear least-squares fit to the data obtained from the nine taxels. The responses shown resulted from applying 3, 16, 40 and 81 gram loads after biasing the taxel with 2.5 volts for approximately one second. Appendix G contains plots of these responses (Figures G-4, G-5, G-6, and G-7, respectively).

The other biasing schemes analyzed during this evaluation were the p-well bias of the amplifiers and the PVDF film's upper electrode bias. Since the upper electrode was connected to an external pin on the IC package, the film could be biased relative to any one of the lower 49 electrodes. The application of a 0 to 10-volt dc bias to the upper electrode had no noticeable affect on the performance of individual taxels. A 0 to 10-volt dc bias applied to the p-well of the MOSFET amplifiers simply shifted their output from 2.5 to 3.5 volts when the inputs to the amplifiers were grounded. This bias only decreased the amplifier's voltage range to saturation.

Electrode Crosstalk Tests. This test evaluated the degree of charge coupling between electrodes. The
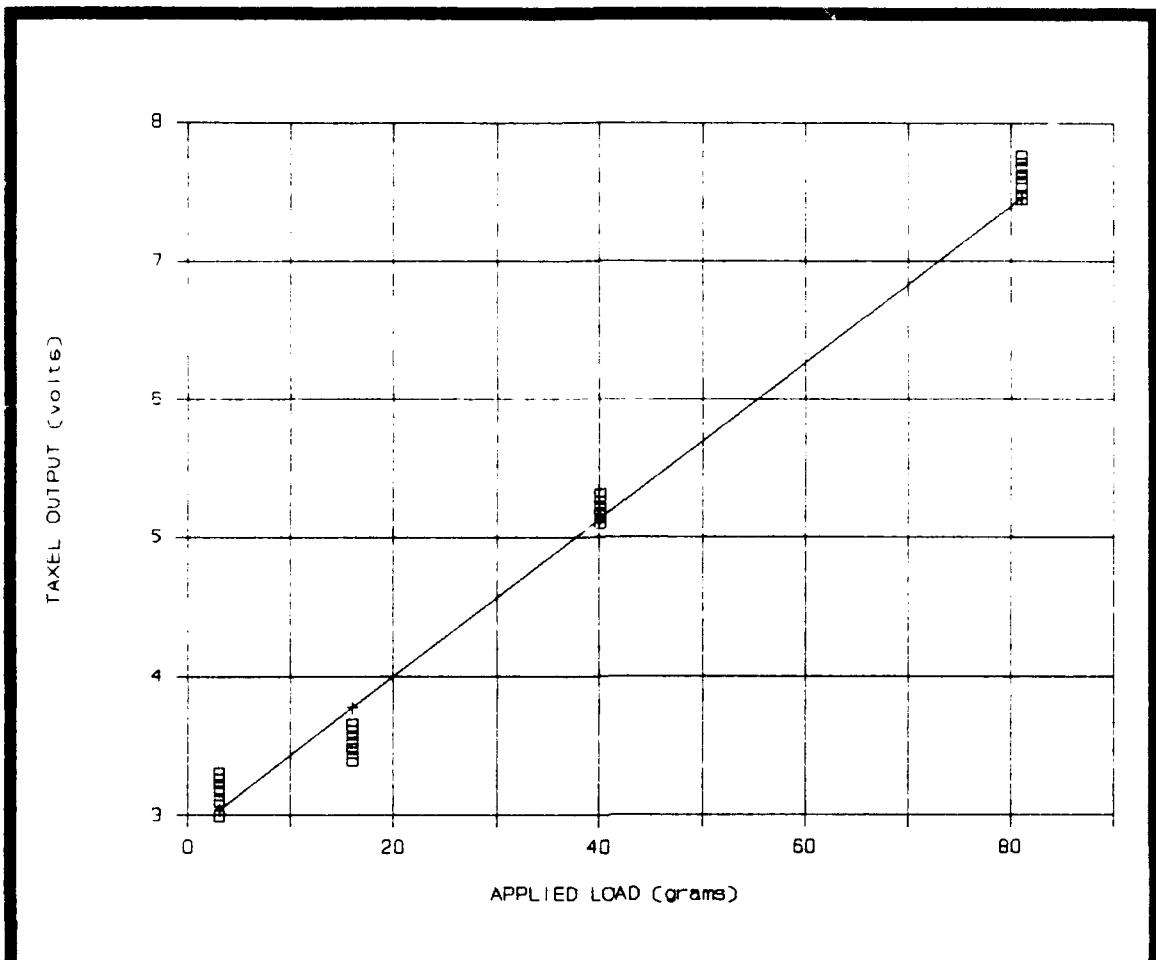
Figure 5-15. Linear least-squares fit to the output responses of nine taxels for loads ranging from 3 to 81 grams (a 2.5-volt dc bias was applied for one second prior to each test).

micromanipulator was used to apply an 81-gram load to taxel number 25-on chip number-16. The multiplexer's output was then recorded on the digital storage oscilloscope as shown in Figure 5-16. Comparison of this figure with the array's initial condition of Figure 5-9 reveals no coupling between nearest-neighbor taxels. The remaining eignt taxels were similarly activated, and no coupling was detected.
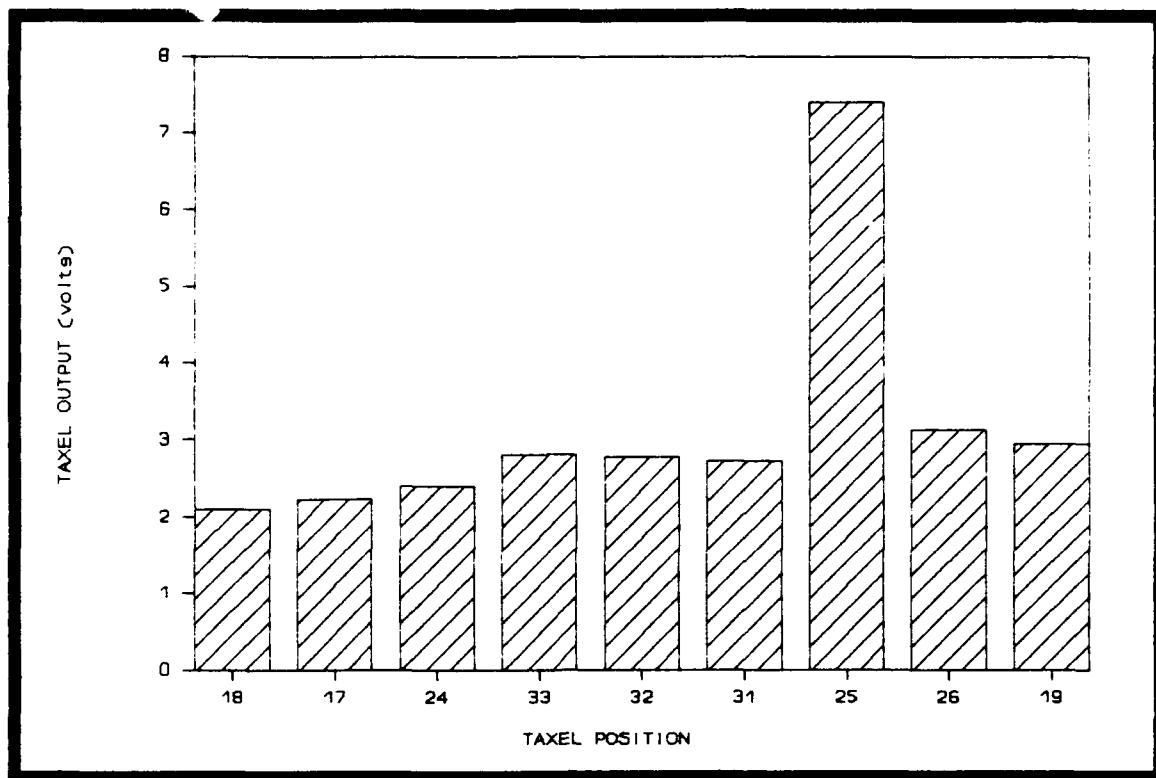
Figure 5-16. Response of taxel number-25 on chip number-16 to an 81-gram load.

Shape Recognition Tests with DC Biased Amplifiers. This final test was designed to determine if a shape applied to the 3 x 3 array could be recognized and its weight determined. Figure 5-17 illustrates the location and size of the applied load, which was a small triangular piece of a glass microscope slide. The surface of the glass slide was extremely flat; therefore, contact with the underly! g taxels was uniform.

The test was initiated by applying a 10-volt dc bias to taxels 33, 32, and 31, in that order, with the micromanipulator microprobe. Each taxel's output quickly rose to its maximum value when the bias signal was applied. When the
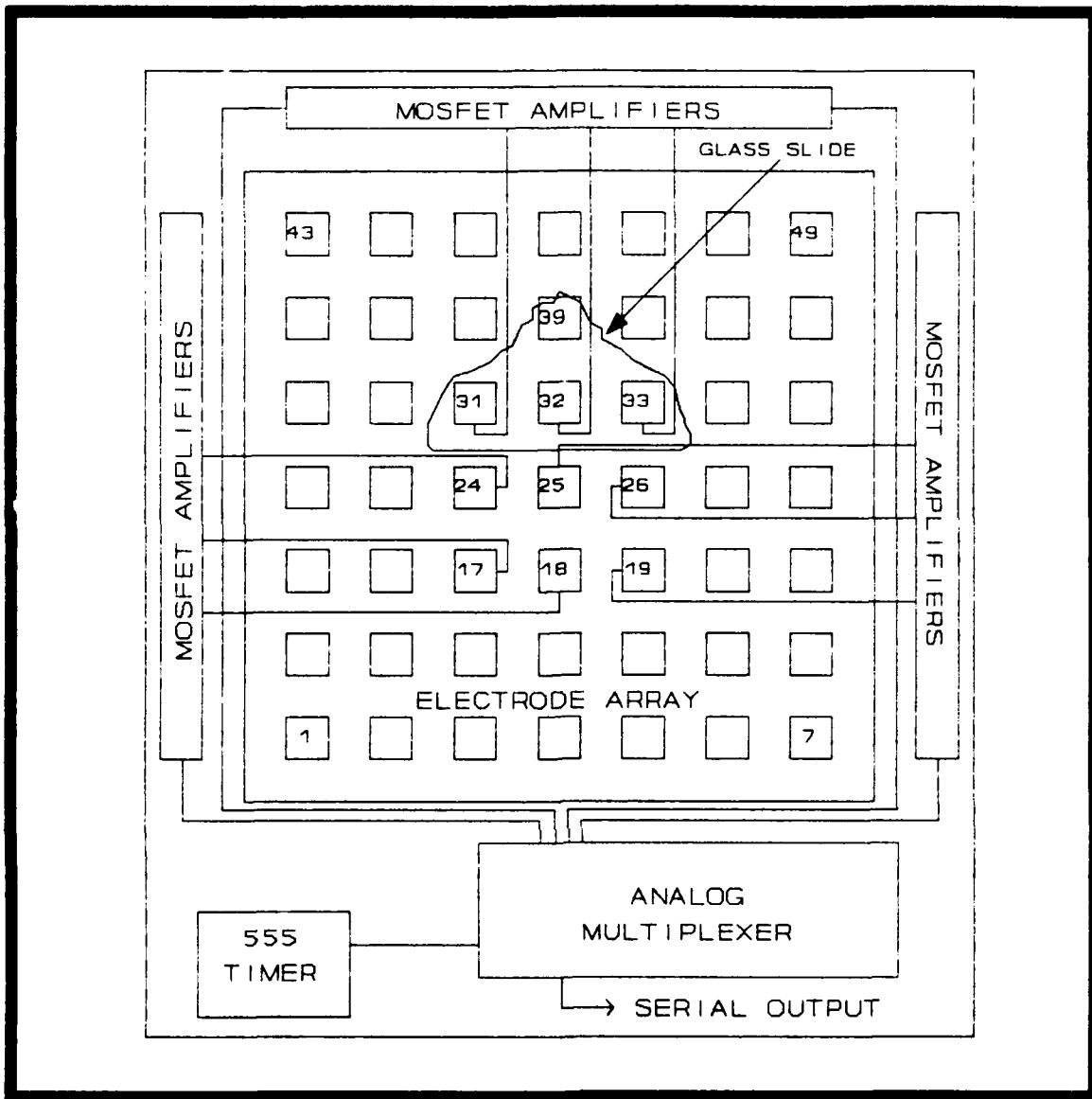
Figure 5-17.   Location of the glass slide for the shape recognition test.

probe was removed, the taxel's response started to decay. The output of taxel 32 had a slower decay rate compared to taxel 31 and taxel 33, as can be seen in Figure 5-18.

The taxel's output decay rate from an initial bias of 10 volts was approximately three minutes; therefore, suffi-cient time existed to obtain the pre-load, load, and the
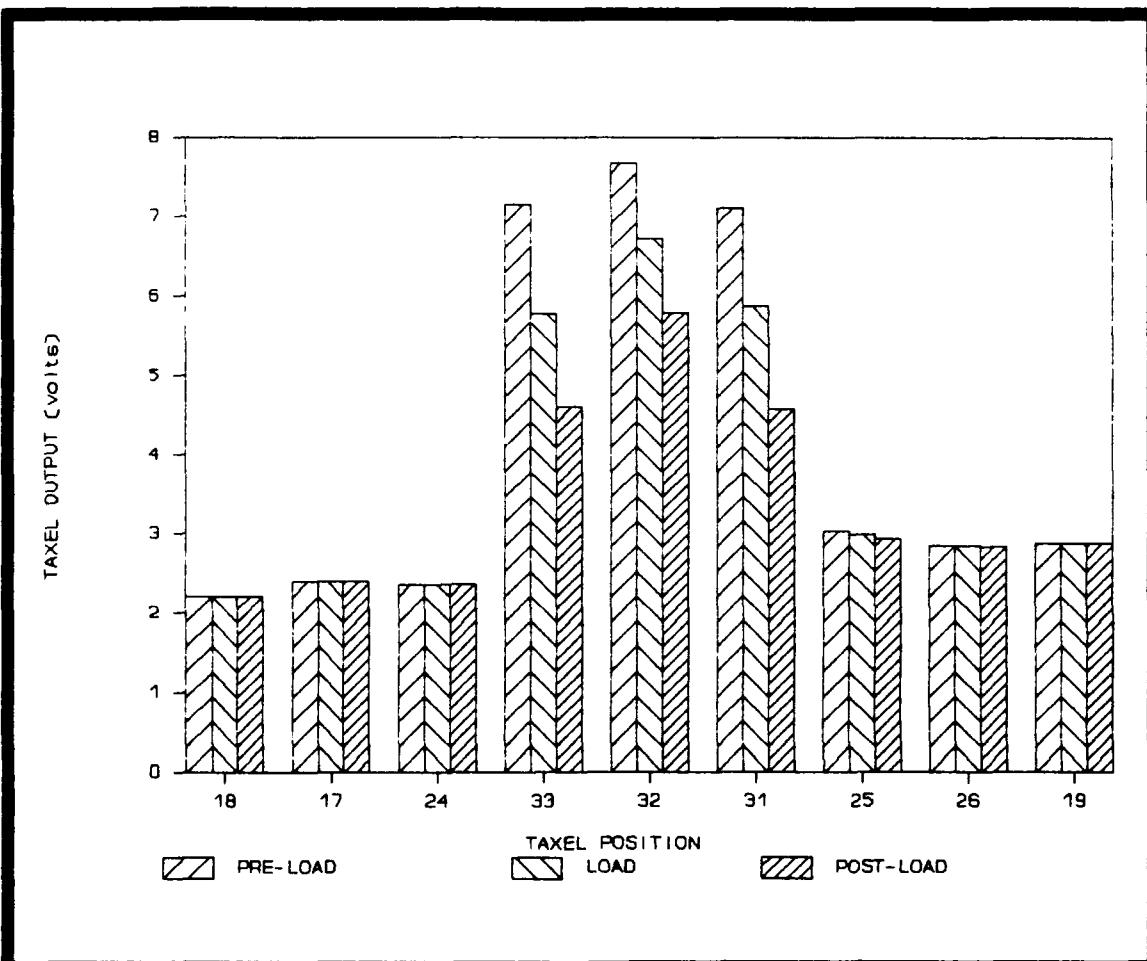
Figure 5-18. The pre-load, load, and post-load multiplexed responses of the 3 x 3 taxel array for chip number-16 recorded approximately 30 seconds, one-minute, and one-minute thirty-seconds, respectively, after a 10-volt dc bias was applied.

post-load multiplexed recordings of the array. After all three taxels were charged, the pre-load condition of the array was stored on the computer's disc. At this point, the taxel outputs had decayed to approximately the 2.5-volt dc bias level. A force of 75 grams was subsequently applied to the center of the glass slide, and the multiplexed output was recorded. Finally, the load was removed, and the array's post-load multiplexed output was recorded. Appendix H

includes the three tests performed in this manner for chip
number-14.

The average output value for these three tests, with
the load applied, was between 3.5 and 3.75 volts. Using
these output values with the graph in Figure 5-15, the ap-
plied weight per taxel corresponds to approximately 18
grams. Multiplying this number by four, since the slide
contacted four taxels, implies that the total weight applied
was 72 grams.

Comparing the relative magnitude of the multiplexed
signals for the pre-load, load, and post-load conditions,
indicates that taxels 31, 32, and 33 were all contacted by
an external force. This comparison provides digital affir-
mation that the taxels were activated due to the application
of a load, as illustrated in Figure 5-19.

PVDF Film Adhesives

The primary factors affecting the utility of a particu-
lar adhesive were examined during the tactile sensor fabri-
cation procedures and tests. These factors included ease of
application, mechanical bond effectiveness and compliance,
and electrical coupling capacity.

The acrylic, urethane, silicon resin, and photoresist
(Shipley Photoposit 1400-17) adhesives were readily applied
to the PVDF film by spin-coating them onto the PVDF film. A
sufficiently thin film of adhesive was formed when one drop
of adhesive (from a 3 cc syringe) was spun onto the PVDF
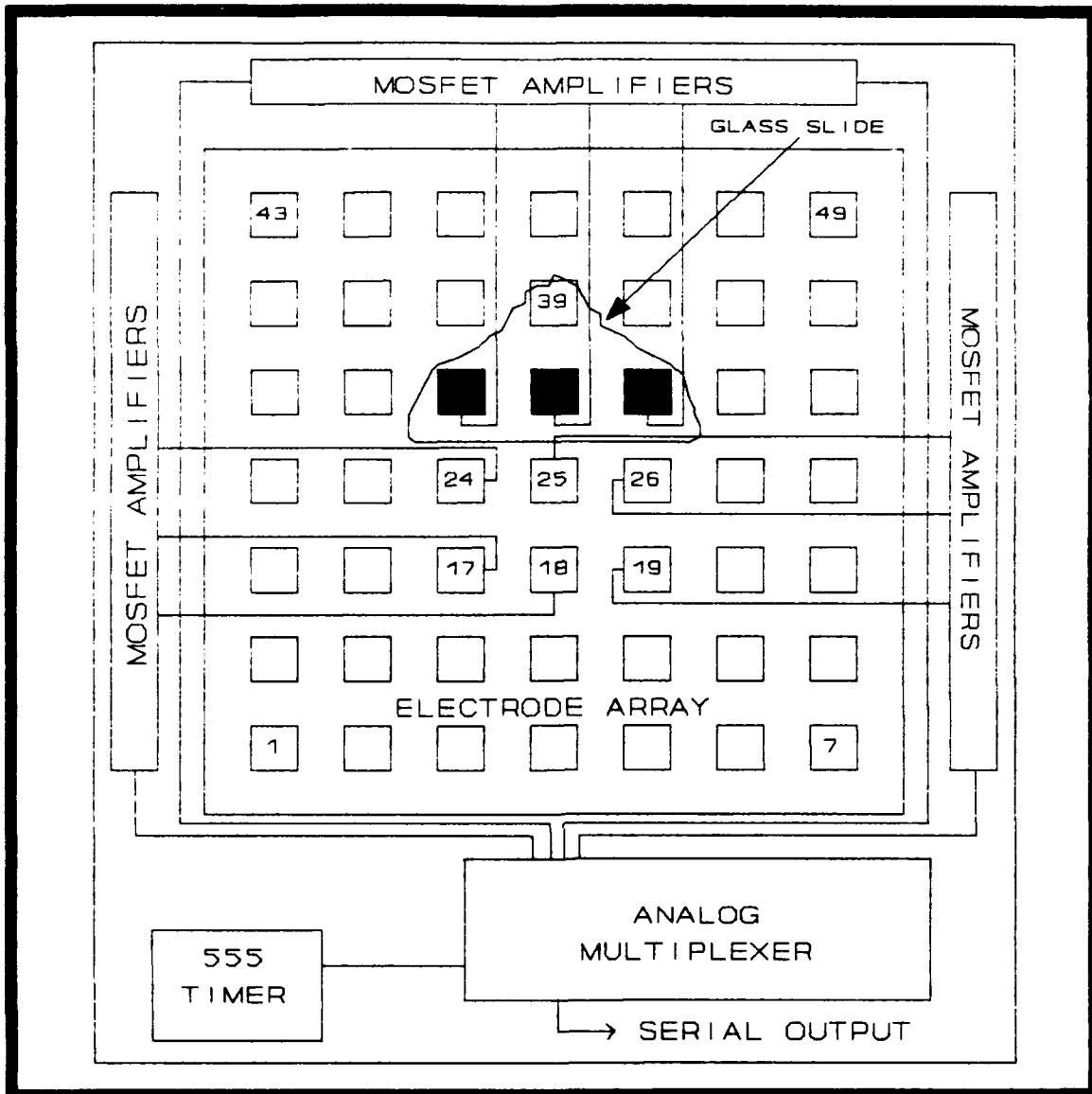
Figure 5-19. Application of a 72-gram triangularly-shaped load to three functional taxels (31, 32, and 33) and one non-functional taxel (39). (The dark squares indicate those taxels which responded to the load).

film at 5000 rpm for ten seconds. The acrylic bond became

brittle when cured, and the PVDF film separated from the

electrode array within one day of its application. Epoxy

(Epon 828 Resin, Miller Stephenson) was extremely viscous;

therefore, it was difficult to prevent excess epoxy from

contacting the bond pads and wires on the chip. The bond formed by the epoxy was strong, but a method of applying a sufficiently small amount of epoxy was not formulated. A silicon resin bond was never successfully obtained, and the residue from this adhesive could not be removed from the electrode array. Photoresist performed essentially the same as urethane, but the urethane bond was stronger and lasted in excess of one month. The photoresist bond deteriorated after one week.

Electrically, urethane was the only adhesive tested, and there existed no noticeable charge coupling between electrodes with this adhesive.

VI. Conclusions and Recommendations

Conclusions

The goal of this research effort was to design, fabri-
cate, and test an integrated circuit tactile sensor. The
integrated circuit design included 49 MOSFET amplifiers,
each with a 400 μm x 400 μm aluminum electrode connected to
the gate contact of the input MOSFET transistor. A 6 mm x
6 mm patch of 25 μm thick polyvinylidene fluoride (PVDF)
film was attached to the 7 x 7 electrode array, thus produc-
ing 49 individual force transducing sites called taxels.

Additional circuitry was included on the IC to provide
a multiplexed output of all 49 MOSFET amplifiers. However,
all of this circuitry did not function properly. The 555
timer circuit produced a stable clock waveform to drive the
multiplexer, but an error internal to the multiplexer's
flip-flop resulted in a nonfunctional multiplexer. There-
fore, an external multiplexer circuit was connected to the
outputs of the amplifiers.

Diagnosis of a "diode effect" at the output of each
amplifier revealed that total isolation of the multiplexer
from the outputs of the charge amplifiers was required to
negate this effect and produce functional amplifiers. Nine
amplifiers were completely isolated from the on-chip multi-
plexer, thus reducing the tactile array size to 3 x 3. The
multiplexed response of this array was sufficient to analyze

6-1

the primary goal of this research: to study the effects of biasing the charge amplifiers.

Both the amplifier p-well bias and the PVDF film's top electrode bias schemes proved to be inadequate methods of providing a uniform charge state across the entire 3 x 3 array. The bias method which manifested the highest degree of pre-load taxel response uniformity involved applying a bias signal directly to the gate contact of the input MOSFET of the amplifier. The injection of charge at this node was essential; otherwise, the taxel did not respond to an applied load (unless the load exceeded 300 grams; that is, 300 grams per taxel distributed across 49 taxels is equivalent to 14,700 grams or 32 pounds, an impractical applied weight).

However, the discovery, diagnosis, and rectification of an undesirable loss mechanism resulted in a fully functional 3 x 3 tactile array. The charge loss mechanism due to the leakage resistance path discovered to exist between the gold bond pads on the integrated circuit ceramic package was eliminated by removing the wire bonds which connect these pads to the gate contact inputs of the amplifier's MOSFET transistors.

Individual taxels were characterized, and the average response from 9 taxels resulted in a nearly linear output for loads spanning 3 gram to 81 grams. Crosstalk between nearest-neighbor taxels did not manifest itself during any of the tests.

Finally, the ability to recognize shapes with the small array was verified by applying a 75-gram load across four taxels. The shape was triangular, and its weight was distributed across three taxels within the active 3 x 3 array and one taxel outside the array. A 10-volt dc bias signal was applied to each taxel, and the taxel's output was allowed to decay. During this decay period, the multiplexed response of the array was recorded before the load was applied, when the load was applied, and after the load was applied. Comparison of these three values for each taxel revealed an approximately equal difference between successive scans. Therefore, shape recognition can be readily accomplished by rapidly scanning the tactile array and calculating the differences between successive scans (see Figure 5-19).

Recommendations

Future efforts should concentrate on devising a method of applying a bias signal to the gate input of the amplifiers. An external bias signal must be applied to the MOSFET taxel electrodes via the package's bond wires; therefore, special care must be taken to avoid contaminating the gold bond pads of the ceramic package. A silicon rubber coating, placed on all of these pads before fabrication of the sensor begins, may protect the pads during processing.

The on-chip multiplexer circuit should be designed and fabricated as a separate MOSIS fabrication run. This proce-

dure would eliminate the problems involved with isolating the multiplexer from the amplifiers, should the multiplexer not function correctly.

The urethane PVDF film adhesive provided the best electrical and mechanical bonding properties. The mechanical bond remained stable for one month; however, additional study of the long-term durability of this adhesive is required.

A less complex and more reproducible method of grounding the top PVDF film electrode is required. Silver paint is difficult to apply in a sufficiently small quantity such that taxels are not covered by the paint. Space will become available on the silicon IC die as a result of transferring the multiplexer on another IC; therefore, the patch of PVDF film can be increased in size to cover this area also. Accordingly, the silver paint contact can then be made far away from the tactile array. These suggestions will facilitate the fabrication process as well as increase the time during which the biasing problem can be examined more closely.

Appendix A: Materials and Equipment

Table A-1. List of Materials.

Materials
MOSIS Circuits
Solef PVDF Film (25 μm thick)
De-ionized Water
Glass Microscope Slides
Isopropyl Alcohol
Concentrated (37%) HCl
Ferric Chloride
Shipley Photoposit 1400-17 Photoresist
Dow Corning 3140 Room Temperature Vulcanizing (RTV) Silicone Coating Dow Corning Corp. Midland, MI 48640
Silver Conductor Paint
Acrylic (MS-467), Silicon (MS-462), Urethane (MS-472) Conformal Coatings, and Coating Remover (MS-114) Miller-Stephenson Chem. Co. Geroge Washington Highway Danbury, CT 06810
Epoxy, Epon 828 Resin Miller-Stephenson Chem. Co. George Washington Highway Danbury, CT 06810

Table A-2. List of Equipment.

Equipment
Test Probe Fixture and Weights
Scalpel
Syringe
Protoboard
Fluke 77/AN Multimeter John Fluke Manufacturing Co Everett, WA
HP 4145 Semiconductor Parameter Analyzer Hewlett Packard Company Colorado Springs, CO
Keithley 617 Electrometer Keithley Instruments, Inc. Cleveland, OH
HP 54100 Digital Storage Oscilloscope Hewlett Packard Company Colorado Springs, CO
Zenith Z-248 Data Collection Computer (with IEEE-488 Interface) Zenith Data Systems Glenview, IL
Micromanipulator Model 6200 Microprobe Station The Micromanipulator Company, Inc. Carson City, NV
Micromanipulator Model 450/360 VM Manipulators (3) The Micormanipulator Company, Inc. Carson City, NV
HP6205B Power Supply Hewlett Packard Company Colorado Springs, CO
Pulse Generator Model 148 Wavetek, Inc. San Diego, CA
TV909 Aluminum Wedge Bonder MECH-EL Industries, Inc. Woburn, MA
DV602 Electron Beam Vacuum Deposition System Denton Hill, NJ

Appendix B: PVDF Film Characteristics

Table B-1. Typical Electrical and Mechanical Properties of PVDF Film (Kynar, 1983:49).

Property	Value
Capacitance	417 pF/cm^2 (for 28 μm thick film, $\varepsilon/\varepsilon^0 = 12$)
Thermal Capacity	1.3 J/gm°K
Specific Heat	2.4 x 10^6 J/m^3°K
Thermal Conductivity	0.13 W/m°K
Glass Transition Temperature	-40 °C
Acoustic Impedance	2.7 x 10^6 kg/m^2-s
Electrical Impedance	1000 Ω (for A = 100 cm^2, t = 6 μm, 1000 Hz)
Volumetric Thermal Expansion	4.2 x 10^{-4} /°K
Electromechanical Coupling Constant k_{33}	19 % (at 1kHz)
Electrical Permittivity ε_r	11 - 13
Pyroelectric Coefficient	-25 x 10^{-6} C/m^2°K
Water Absorption	0.02 % H$_2$O
Young's Modulus	2 x 10^9 N/m^2
Piezoelectric charge constant d_{33}	16 pC/N
Tensile Strength	180 MPa

Table B-2. PVDF Film Chemical Resistance (Reston, 1988:C-1)

Chemical	Conditions to Induce an Effect
Acetone	Not Recommended
Acetone (10% in Water)	125°F
Butyl Acetate	80°F
Ferric Chloride	275°F
Hydrochloric Acid Concentrated	275°F
Isopropyl Alcohol	140°F
Methyl Ethyl Ketone	Not Recommended
Silicone Oil	250°F
Xylene	200°F
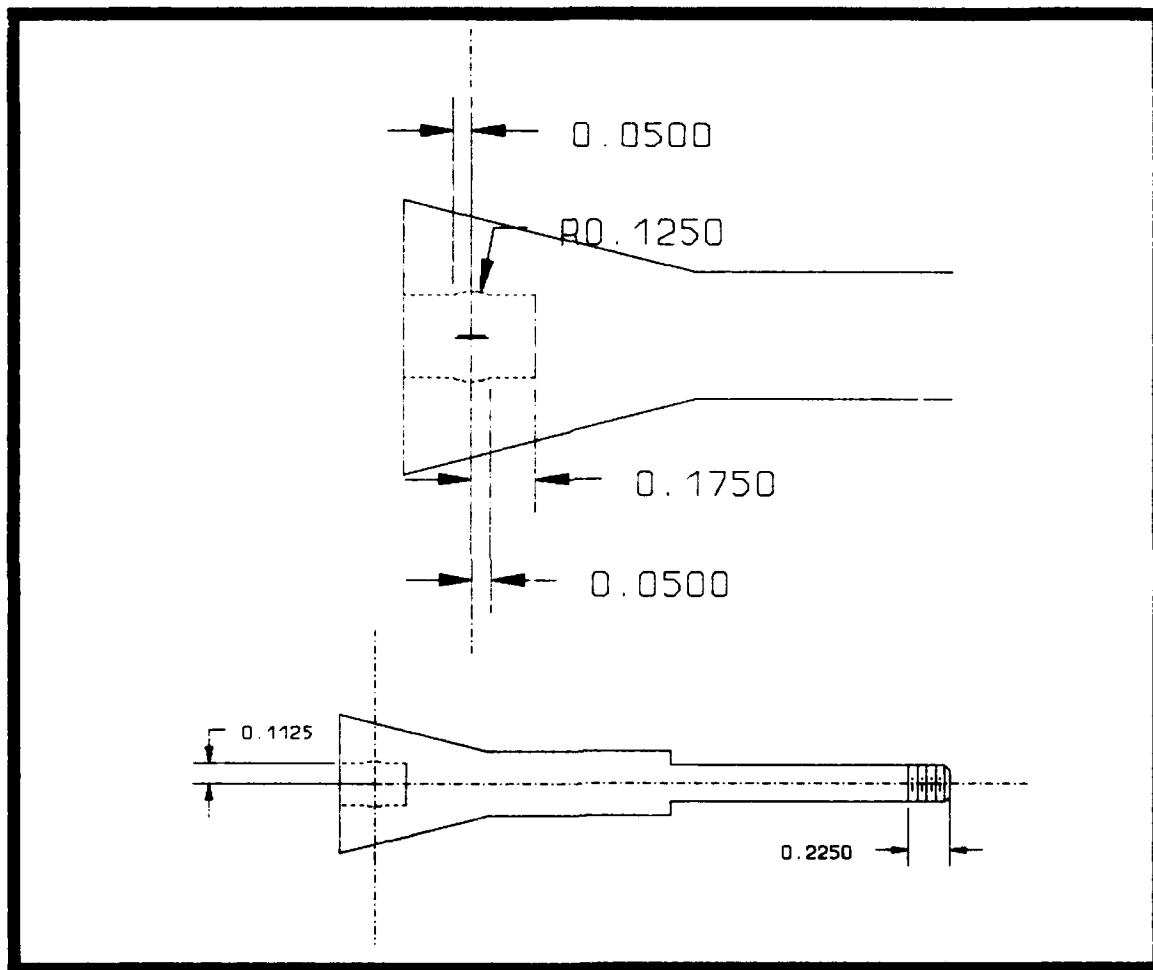
Figure C-1. Front view (bottom schematic) of the collet and
an exploded view of it's left side (top schematic). (Units
are inches).
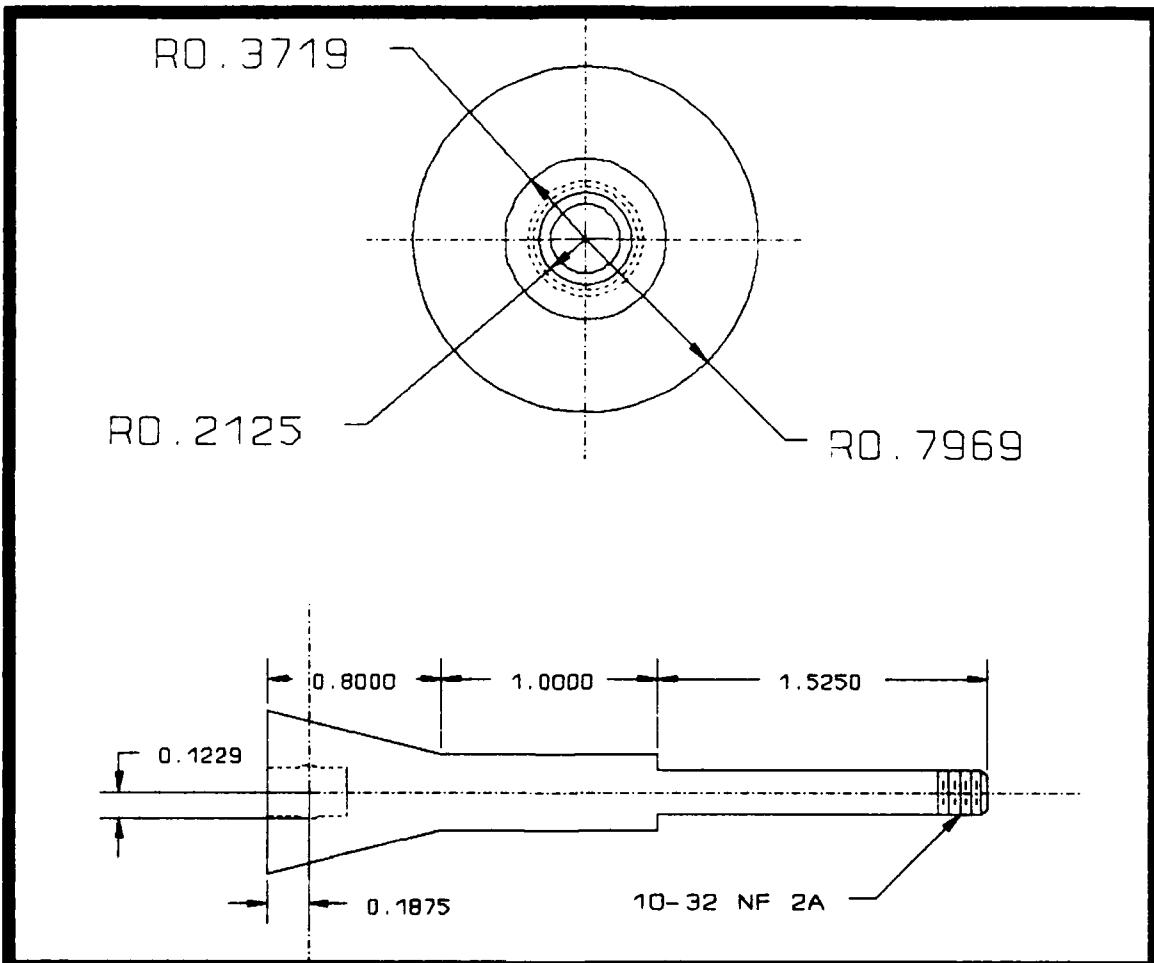
Figure C-2. Top view (bottom schematic) of the collet and an exploded end view (top schematic) of the collet's left side. (Dimensions are in inches).
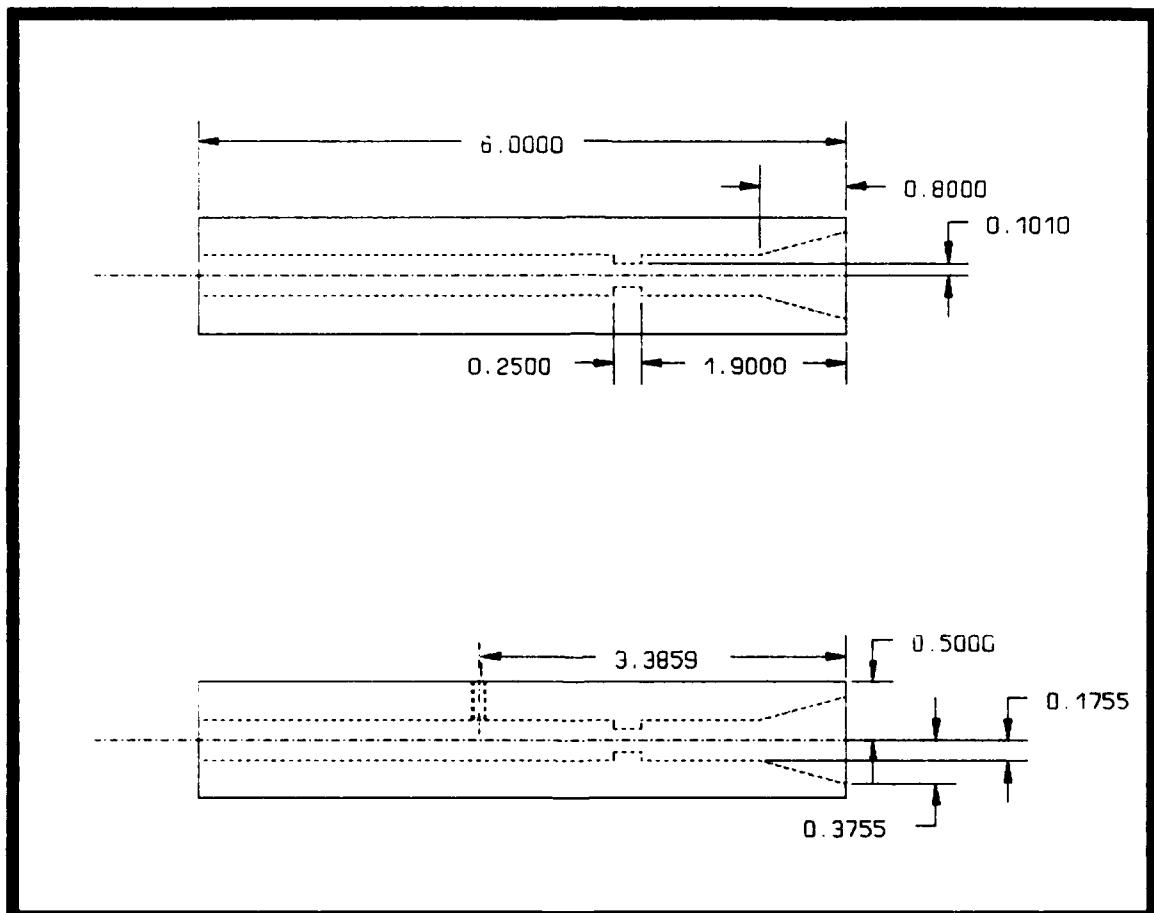
Figure C-3. Dimensions of the collet holder (Dimensions are in inches).
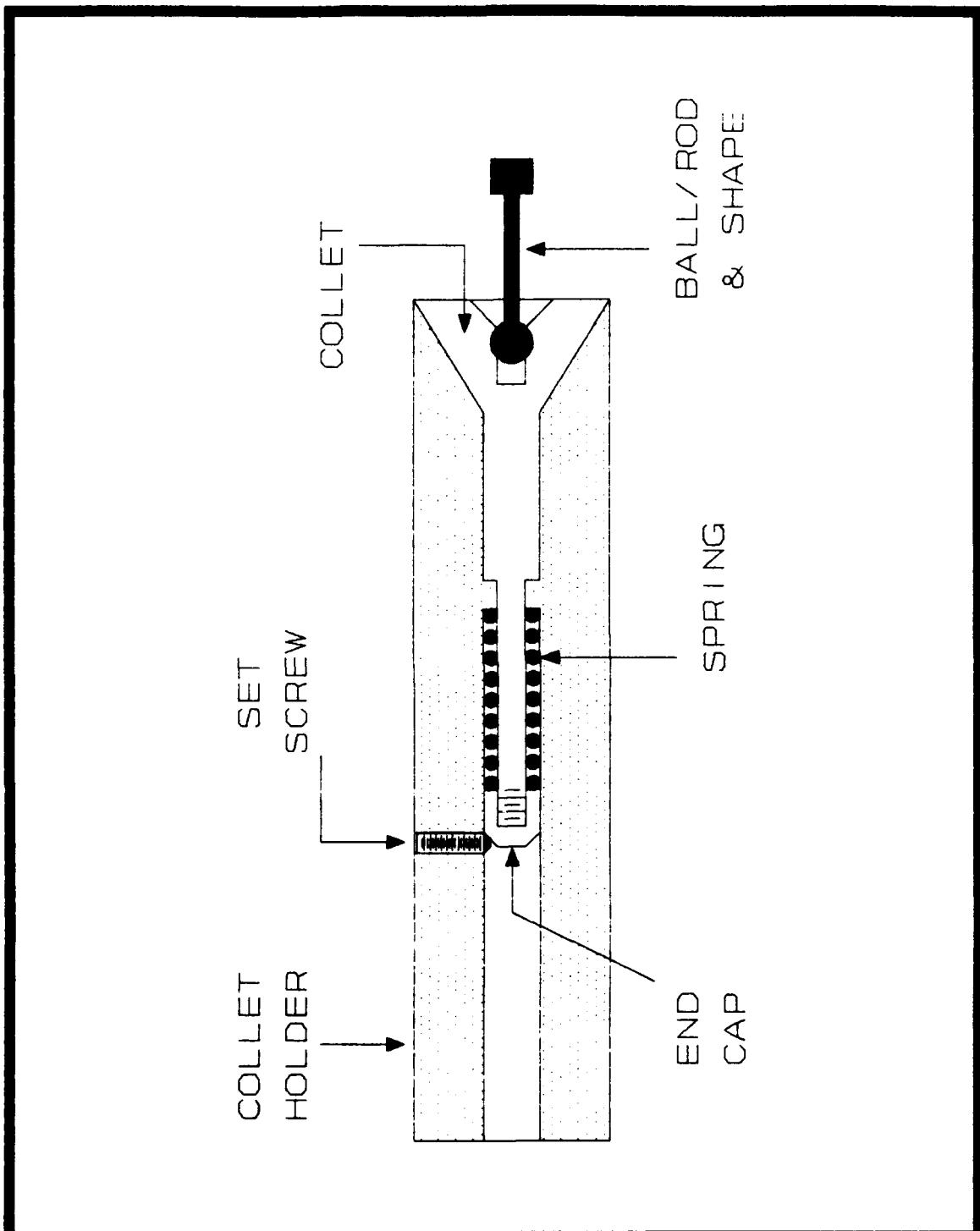
Figure C-4. Assembly of the collet, ball/rod and shape, and collet holder.

Appendix D: SPICE Parameters and Plots

The following transistor model cards were used for all of the SPICE decks listed in this Appendix.

```
.model P pmos level=4
+ vfb = -.49449 lvfb = .0473111 wvfb = -.078748
+ phi = .711038 lphi = 0 wphi = 0
+ k1 = .549022 lk1 = -.1098 wk1 = .211133
+ k2 = .0225369 lk2 = .0133462 wk2 = .0214418
+ eta = -.011378 leta = .0599553 weta = .0109074
+ muz = 173.524 dl = .502141 dw = -.20323
+ u0 = .129663 lu0 = .0395758 wu0 = -.089559
+ u1 = .0282132 lu1 = .288861 wu1 = -.13103
+ x2mz = 7.49207 lx2mz = -3.3077 wx2mz = 4.43137
+ x2e = -.00081113 lx2e = -.0023066 wx2e = -.0029608
+ x3e = .000855699 lx3e = -.003979 wx3e = -.00061957
+ x2u0 = .00634967 lx2u0 = -.0021908 wx2u0 = .00304801
+ x2u1 = .000525933 lx2u1 = .00057697 wx2u1 = .00896684 + mus
= 187.23 lmus = 89.9055 wmus = -19.539
+ x2ms = 7.00102 lx2ms = -.47434 wx2ms = 8.73424
+ x3ms = -.14304 lx3ms = 11.6728 wx3ms = -7.9883
+ x3u1 = -.016595 lx3u1 = .00351738 wx3u1 = .00384252
+ tox = .028 temp = 27 vdd = 5
+ cgdo = 3.09624e-10 cgso = 3.09624e-10 cgbo = -2.50626e-10 +
xpart = 1
+ n0 = 1 ln0 = 0 wn0 = 0
+ nb = 0 lnb = 0 wnb = 0
+ nd = 0 lnd = 0 wnd = 0
+ rsh = 20.58 cj = .0004015 cjsw = 5.023e-10
+ js = 1.e-08 pb = .8 pbsw = .51
+ mj = .4465 mjsw = .2705 wdf = 0
+ dell = 0
.model N nmos level=4
+ vfb = -.78837 lvfb = -.021873 wvfb = -.12029
+ phi = .801437 lphi = 0 wphi = 0
+ k1 = 1.05382 lk1 = .0864105 wk1 = .588742
+ k2 = -.0087349 lk2 = .0845206 wk2 = .0774966
+ eta = -.0025165 leta = .00946697 weta = .00706382
+ muz = 431.198 dl = .7921 dw = -.11735
+ u0 = .051871 lu0 = .0428904 wu0 = -.035902
+ u1 = .0252047 lu1 = .608867 wu1 = -.34032
+ x2mz = 11.1852 lx2mz = -22.808 wx2mz = 38.2982
+ x2e = -.00020831 lx2e = -.0062271 wx2e = -.00071188
+ x3e = .000225369 lx3e = -.000686 wx3e = -.0042937
+ x2u0 = .00301681 lx2u0 = -.014095 wx2u0 = .0297249
+ x2u1 = -.0021476 lx2u1 = .00786076 wx2u1 = .004818
+ mus = 412.323 lmus = 259.338 wmus = 37.6417
+ x2ms = 4.86473 lx2ms = -19.202 wx2ms = 69.3915
+ x3ms = -2.6586 lx3ms = 47.7003 wx3ms = -13.265
+ x3u1 = -.002006 lx3u1 = .0668089 wx3u1 = -.019504
+ tox = .028 temp = 27 vdd = 5
```

```
+ cgdo = 4.88415e-10 cgso = 4.88415e-10 cgbo = -1.44718e-10 +
xpart = 1
+ n0 = 1 ln0 = 0 wn0 = 0
+ nb = 0 lnb = 0 wnb = 0
+ nd = 0 lnd = 0 wnd = 0
+ rsh = 20.58 cj = .0004015 cjsw = 5.023e-10
+ js = 1.e-08 pb = .8 pbsw = .51
+ mj = .4465 mjsw = .2705 wdf = 0
+ dell = 0
*
.OPTIONS DEFL=1.2U DEFW=6U DEFAS=45P DEFAD=45P
+ITL1=500 ITL4=30 ABSTOL=100P VNTOL=100U CHGTOL=1E-12
+NOPAGE RELTOL=.004 CPTIME=15000
```

```
*CHARGE SIGNAL AMPLIFIER TEST
M1 3 2 0 1 N L=2U W=8U AS=48P AD=48P
M2 4 3 0 1 N L=2U W=8U AS=48P AD=48P
R1 5 3 5K
R2 5 4 5K
VBIAS 1 0 DC 0v
VCC 5 0 DC 10v
VAIN 2 0 PWL(0ms 0 10ms 0 30ms 10 40ms 10 60ms 0)
.END
```
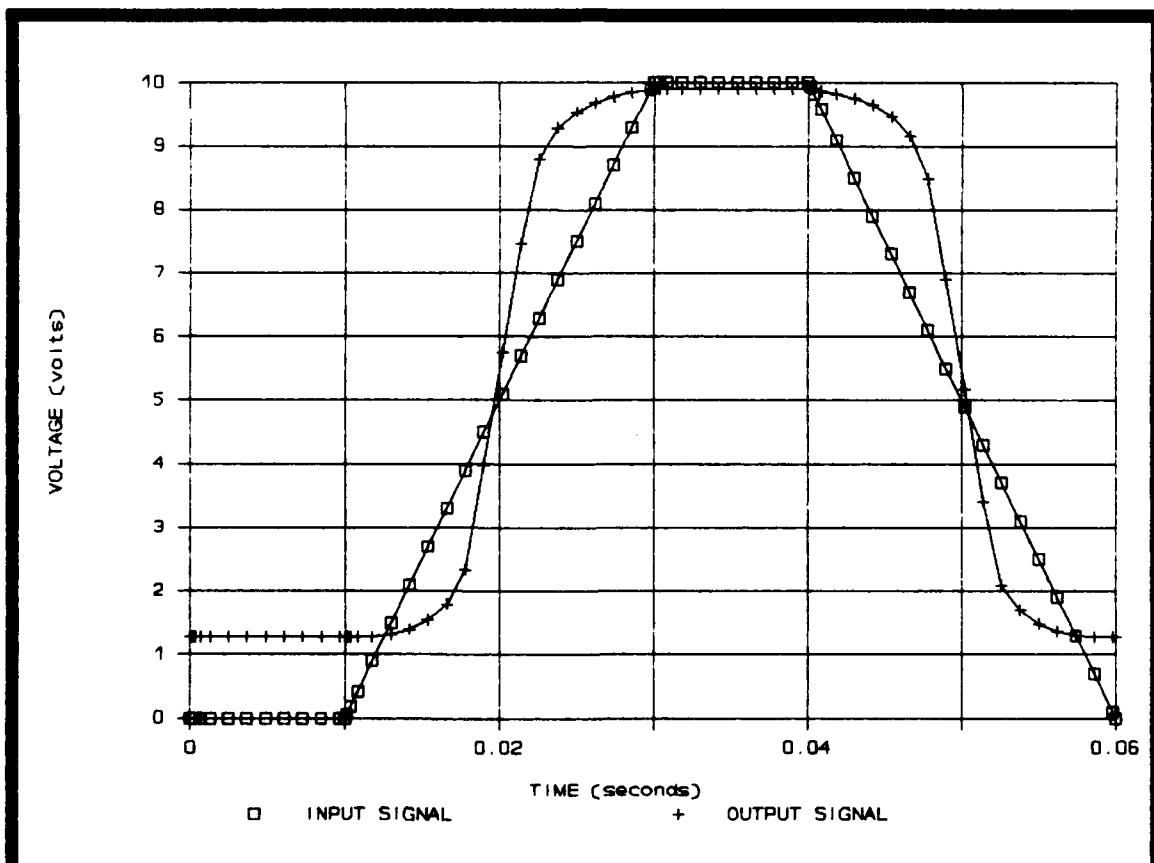

Figure D-1. Charge signal amplifier's output response to a piecewise-linear input.

```
*TRANSMISSION GATE


VCC 5 0 5
M1 2 3 1 5 P L=2U W=8U AS=40P AD=40P PS=26U PD=26U
M2 2 4 1 0 N L=2U W=6U AS=30P AD=30P PS=22U PD=22U
VA 1 0 PWL (Ons 0 10ns 0 20ns 10 30ns 0 40ns 0)
VC 4 0 PULSE 0 5 1ns 1ns 1ns 40ns 80ns
VCN 3 0 PULSE 5 0 1ns 1ns 1ns 40ns 80ns
.END
```
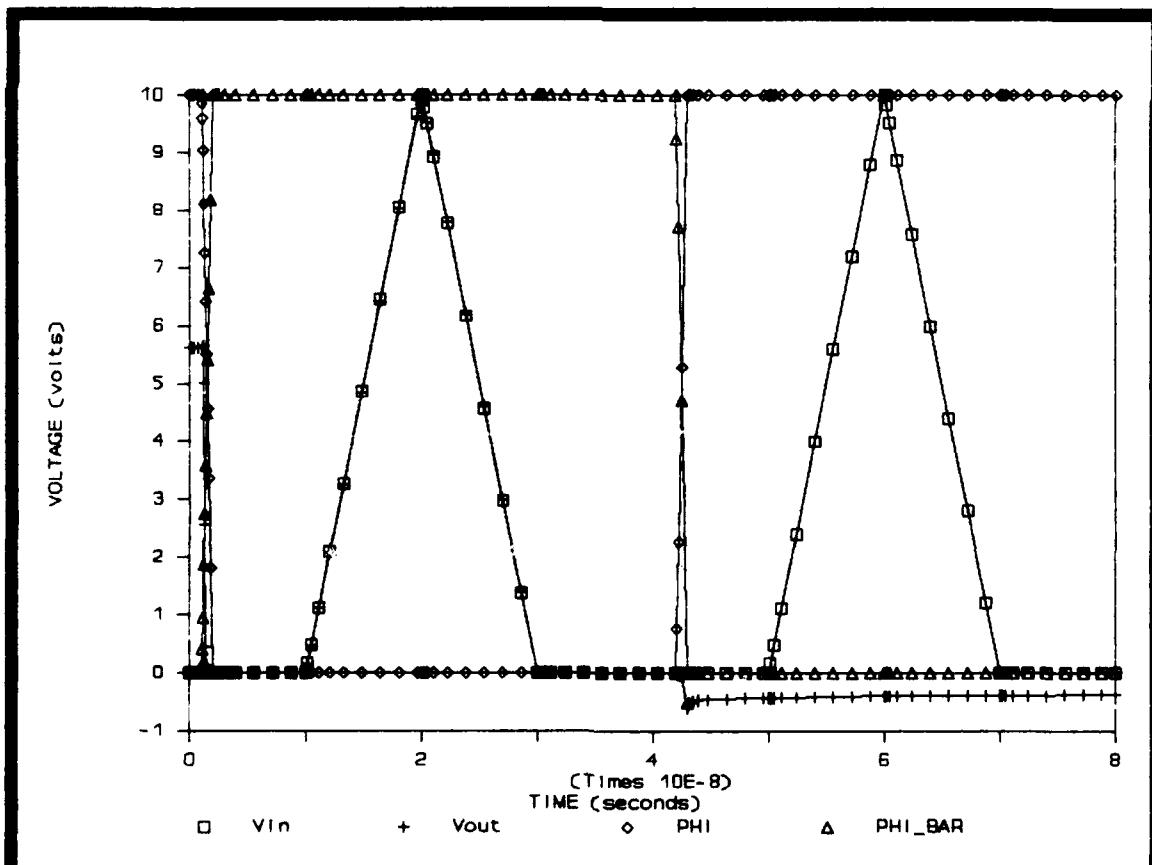

Figure D-2. Analog transmission gate response to a piecewise-linear input signal.

```
ROWDRIVER TEST
Vcc    1000 0 dc 5
*INVERTER
*IN=100 OUT=200 Vcc=300 GND=400
.subckt inverter 100 200 300 400
M1     300    100    200    300    P    L=6U W=20U AS=80P AD=120P
M2     200    100    400    400    N    L=6U W=10U AS=40P AD=60P
.ends subckt
*
XINVERTERA 20    40    1000    0    inverter
XINVERTERB 40    60    1000    0    inverter
VTEST 20 0 PWL(Ons 0 5ns 0 6ns 5 15ns 5 16ns 0)
*VTEST    20    0    PWL(Ons 0 10ns 0 11ns 10 20ns 10 21ns 0)
```
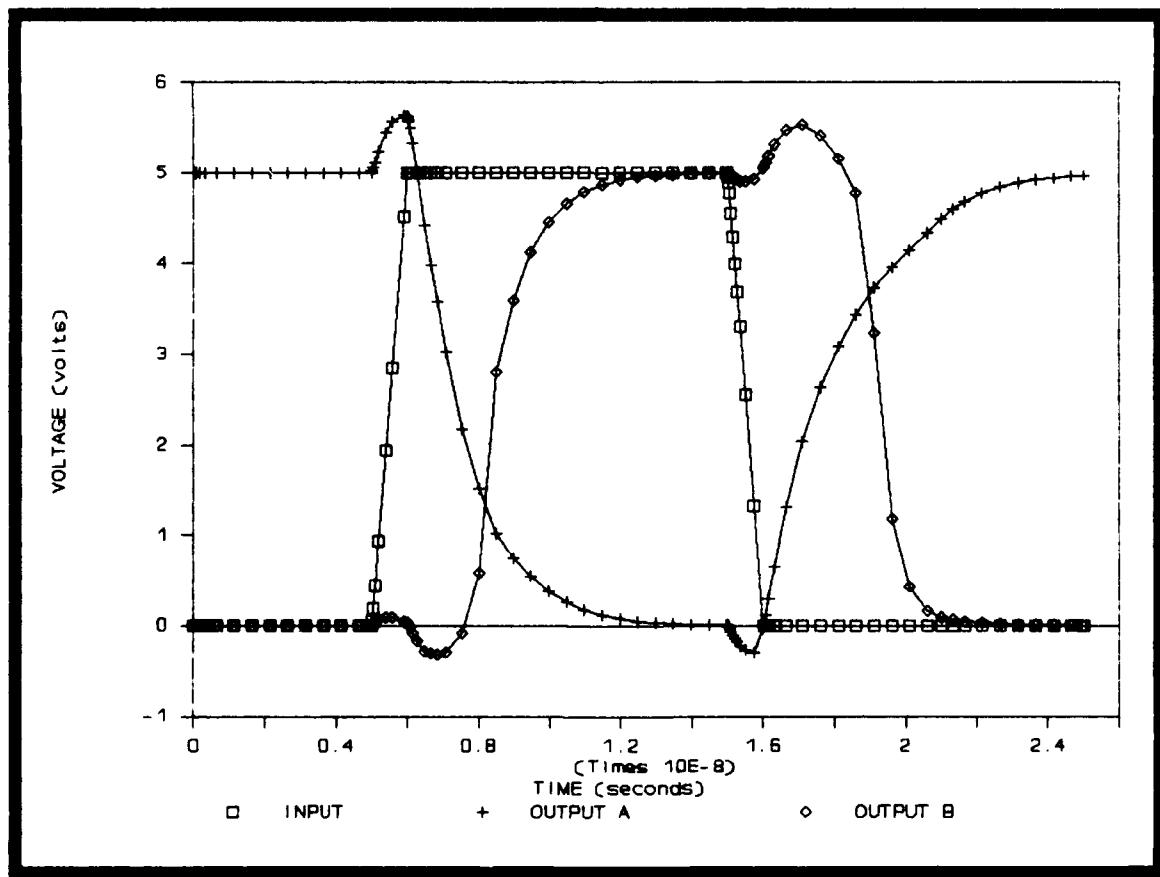

Figure D-3.   Driver circuit for transmission gates.

```
* TEST OF D FLIP-FLOP WITH T-GATE SET AND CLEAR INPUTS
*
*
* SUBCIRCUITS
*
*   LOAD CIRCUIT FOR TESTS
*       1n=1 GND=2 Vdd=3
.subckt LOAD 1 2 3
MPULLDOWN 3 1 4 3 p L=2U W=6U      AS=30P AD=30P   PS=26U   PD=26U
MPULLUP   4 1 2 2 n L=2U W=18U     AS=90P AD=90P   PS=42U   PD=42U
.ends subckt
*
*   INPUT DRIVER FOR TESTS
*       1n=1 GND=2 Vdd=3 out=4
.subckt INPUT_DRIVER 1 2 3 4
MPULLDOWN 3 1 5 3 p L=2U W=6U      AS=30P AD=30P   PS=26U   PD=26U
MPULLUP   5 1 2 2 n L=2U W=18U     AS=90P AD=90P   PS=42U   PD=42U
MPULLu    3 5 4 3 p L=2U W=12U     AS=60P AD=60P   PS=34U   PD=34U
MPULLd    4 5 2 2 n L=2U W=36U     AS=180P AD=180P   PS=82U
PD=82U
.ends subckt
*
*
* P_CMOS
*       1n=1 clock=2 GND=3 Vdd=4 out=5
.subckt P_CMOS 1 2 3 4 5
Mp1 4 1 6 4       p L=2.0U W=8.0U      AS=8P  AD=40P  PS=10U
PD=26U
Mp2 6 2 5 4       p L=2.0U W=8.0U      AS=40P AD=8P   PS=26U
PD=10U
Mn1 5 1 3 3       n L=2.0U W=4.0U      AS=20P AD=20P  PS=18U
PD=18U
.ends subckt
*
*   C_CMOS
*       1n=1 clock=2 GND=3 Vdd=4 out=5
.subckt C_CMOS 1 2 3 4 5
Mp3 4 2 5 4       p L=2.0U W=4.0U      AS=20P AD=20P  PS=18U
PD=18U
Mn2 5 1 6 3    n L=2.0U W=4.0U    AS=4P AD=20P  PS=6U  PD=18U
Mn3 6 2 3 3    n L=2.0U W=4.0U    AS=20P AD=4P  PS=18U  PD=6U
.ends subckt
*
* N_CMOS
*       1n=1 clock=2 GND=3 Vdd=4 out=5
.subckt N_CMOS 1 2 3 4 5
Mp5 4 1 5 4       p  L=2.0U W=4.0U      AS=20P AD=20P  PS=18U
PD=18U
Mn4 5 2 6 3       n  L=2.0U W=4.0U      AS=4P   AD=20P  PS=6U
PD=18U
Mn5 6 1 3 3       n  L=2.0U W=4.0U      AS=20P AD=4P   PS=18U
PD=6U
.ends subckt
```

```
*
*   inverter
*     in=1 GND=2 Vdd=3 out=4
.subckt inverter 1 2 3 4
MPULLup   3 1 4 3 p L=2U W=4U     AS=20P AD=20P   PS=18U   PD=18U
MPULLdn   4 1 2 2 n L=2U W=4U     AS=20P AD=20P   PS=18U   PD=18U
.ends subckt
*
* T-gate SET&CLEAR CONTROL
*     D_in=1 SET=2 CLEAR=3 GND=4 Vdd=5 out1=6
.subckt T_SET_CLEAR 1 2 3 4 5 6
Mp1  1 2 7 5 p L=2.0U W=4.0U     AS=4P  AD=20P   PS=6U    PD=18U
Mp2  7 3 6 5 p L=2.0U W=4.0U     AS=20P AD=4P    PS=18U   PD=6U
Mp3  5 2 9 5 p L=2.0U W=4.0U     AS=20P AD=20P   PS=18U   PD=18U
Mp4  5 9 6 5 p L=2.0U W=4.0U     AS=20P AD=20P   PS=18U   PD=18U
Mp5  5 3 8 5 p L=2.0U W=4.0U     AS=20P AD=20P   PS=18U   PD=18U
Mn1  1 9 7 4 n L=2.0U W=4.0U     AS=4P  AD=20P   PS=6U    PD=18U
Mn2  7 8 6 4 n L=2.0U W=4.0U     AS=20P AD=4P    PS=18U   PD=6U
Mn3  9 2 4 4 n L=2.0U W=4.0U     AS=20P AD=20P   PS=18U   PD=18U
Mn4  6 3 4 4 n L=2.0U W=4.0U     AS=20P AD=20P   PS=18U   PD=18U
Mn5  8 3 4 4 n L=2.0U W=4.0U     AS=20P AD=20P   PS=18U   PD=18U
.ends subckt
*
*   Voltage Supply
*
Vdd 10000 0 DC 5
*
* INPUT signals
*
VD_in  1 0   pulse (0 5 0ns 2ns 2ns 20ns 40ns)
*                        1111____1111____
VClock 2 0   pulse (0 5 5ns 2ns 2ns 10ns 20ns)
*                        _1_1_1_1_1_1_1_1_
VSET       3 0  PWL(0ns 0    23ns 0    25ns 0    33ns 0       35ns
0)
VCLEAR     4 0  PWL(0ns 0    49ns 0    51ns 0    74ns 0       76ns
0)
*
* THE TEST CIRCUIT:
XD_input 1 0 10000   10 INPUT_DRIVER
XClock   2 0 10000   20 INPUT_DRIVER
Xset     3 0 10000   30 INPUT_DRIVER
Xclear   4 0 10000   40 INPUT_DRIVER
*
* Control add-on for the SET&CLEAR function:
XSET     10  30   40      0 10000     11      T_SET_CLEAR
*
*
Xleft    11  20   0 10000     300      P_CMOS
Xmiddle 300  20   0 10000     400      C_CMOS
Xright  400  20   0 10000     500      N_CMOS
XQ_out  500       0 10000     600      inverter
*
```

```
*
*

Xload          600        0  10000          LOAD
*
.1c  v(10)=0  v(11)=0    v(300)=0  v(400)=0  v(500)=0  v(600)=0
*
.END
```
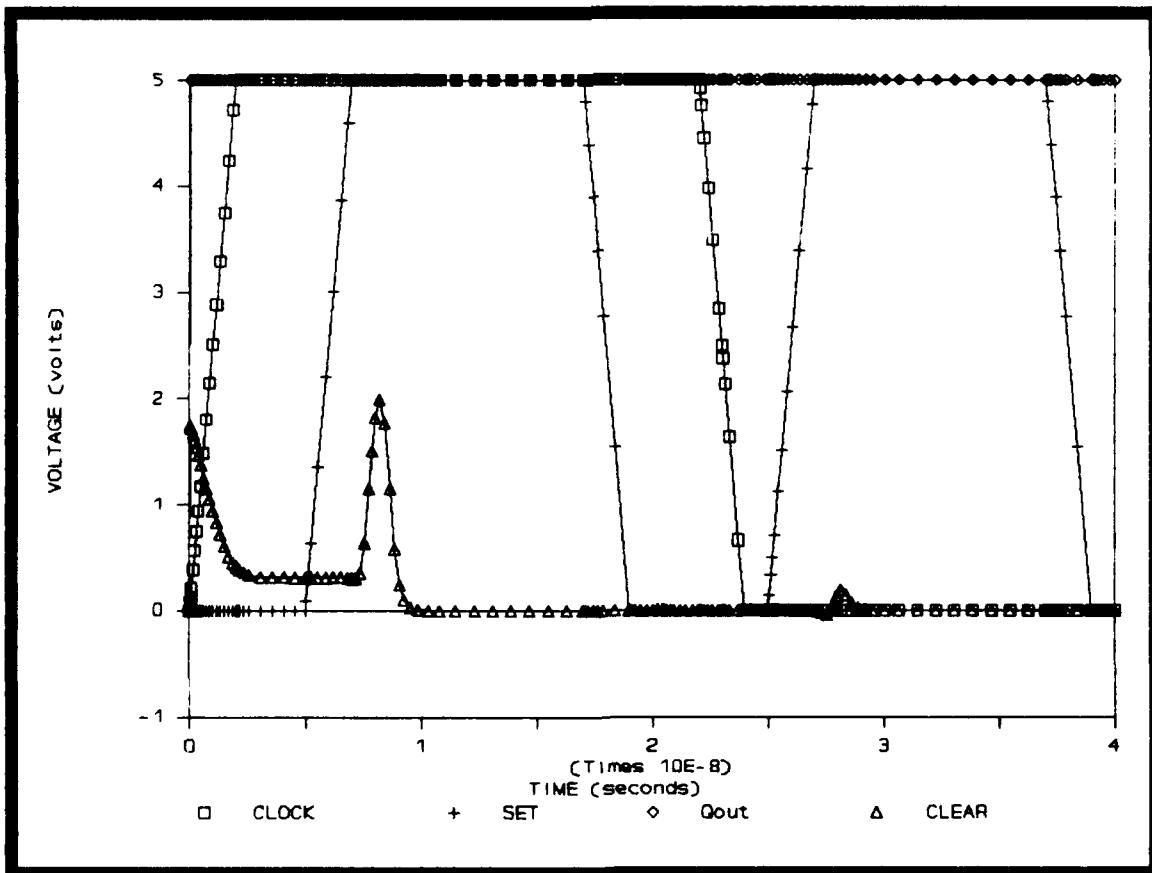

Figure D-4.   D flip-flop response to a clear input.
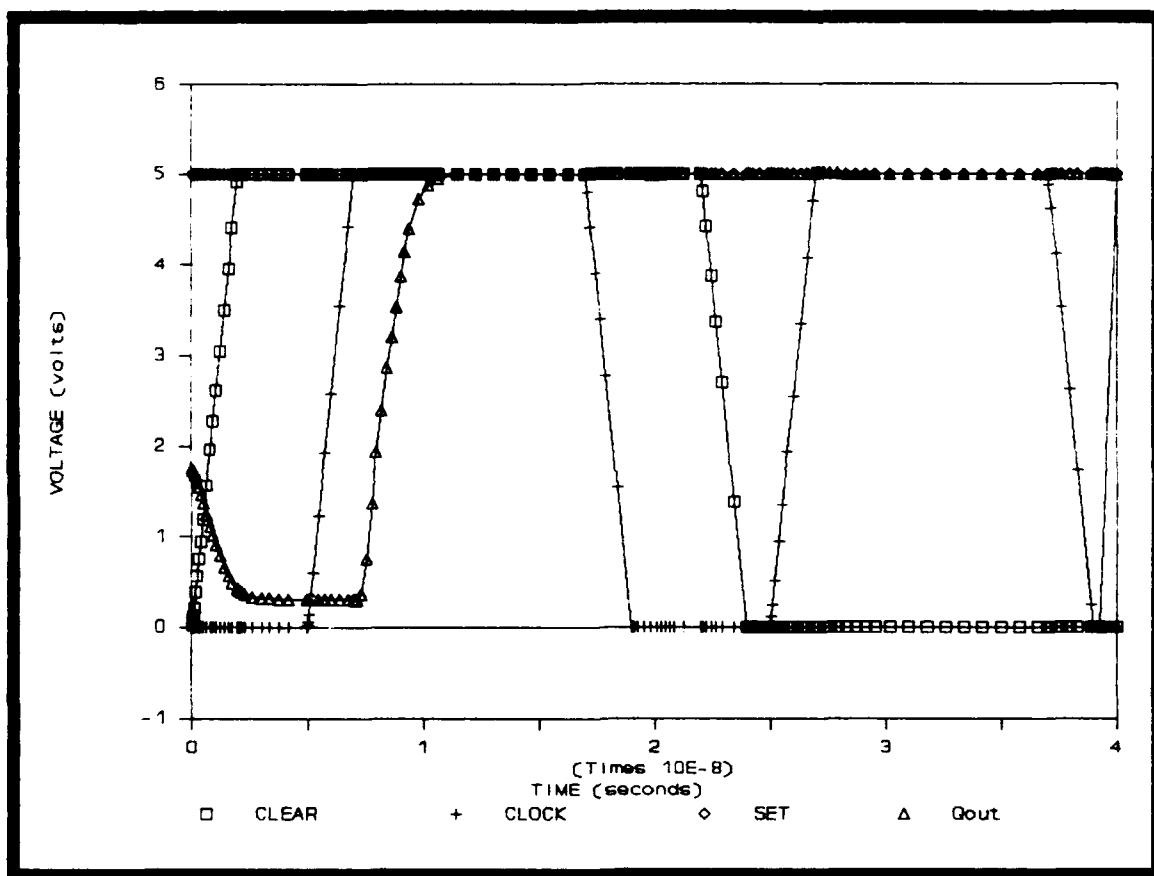
Figure D-5. D flip-flop response to a set input.
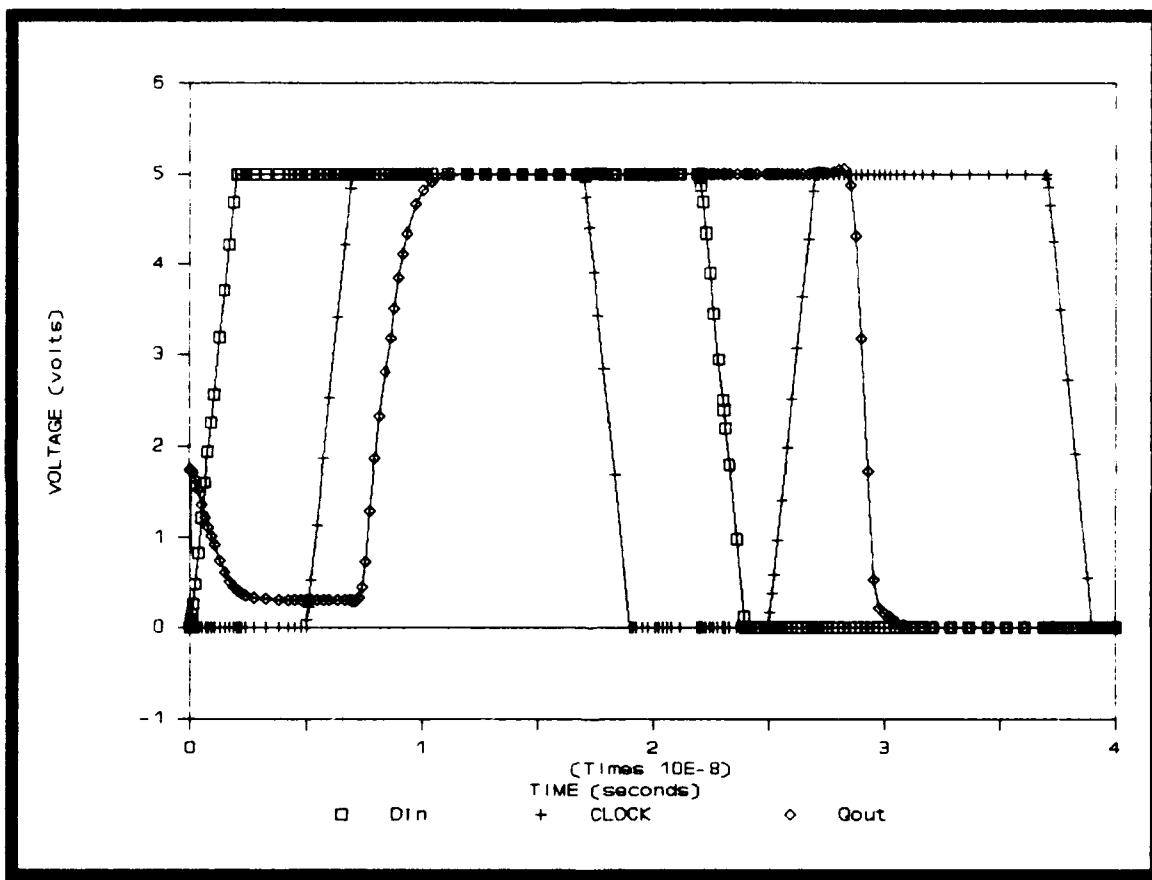
Figure D-6. D flip-flop data transmission operation.

```
COMPARATOR CIRCUIT

Vcc    1000   0   dc   5v
*
*A=100  B=200  OUT=300  Vcc=400  BASE=500
.subckt diffamp   100 200 300  400 500
M1      55     100   500    500    N   L=2U  W=4U
M2      300    200   500    500    N   L=2U  W=4U
M3      400    55    55     400    P   L=2U  W=12U
M4      400    55    300    400    P   L=2U  W=12U
R       500    0     0.264k
.ends subckt
*
XDIFFAMP1   100 200 300   1000 0 diffamp
V+    100    0   PWL(Ons 0 20ns 5 40ns 5 60ns 0)
V-    200    0   PWL(Ons 0 20ns 0 40ns 5 60ns 5)
*
.END
```
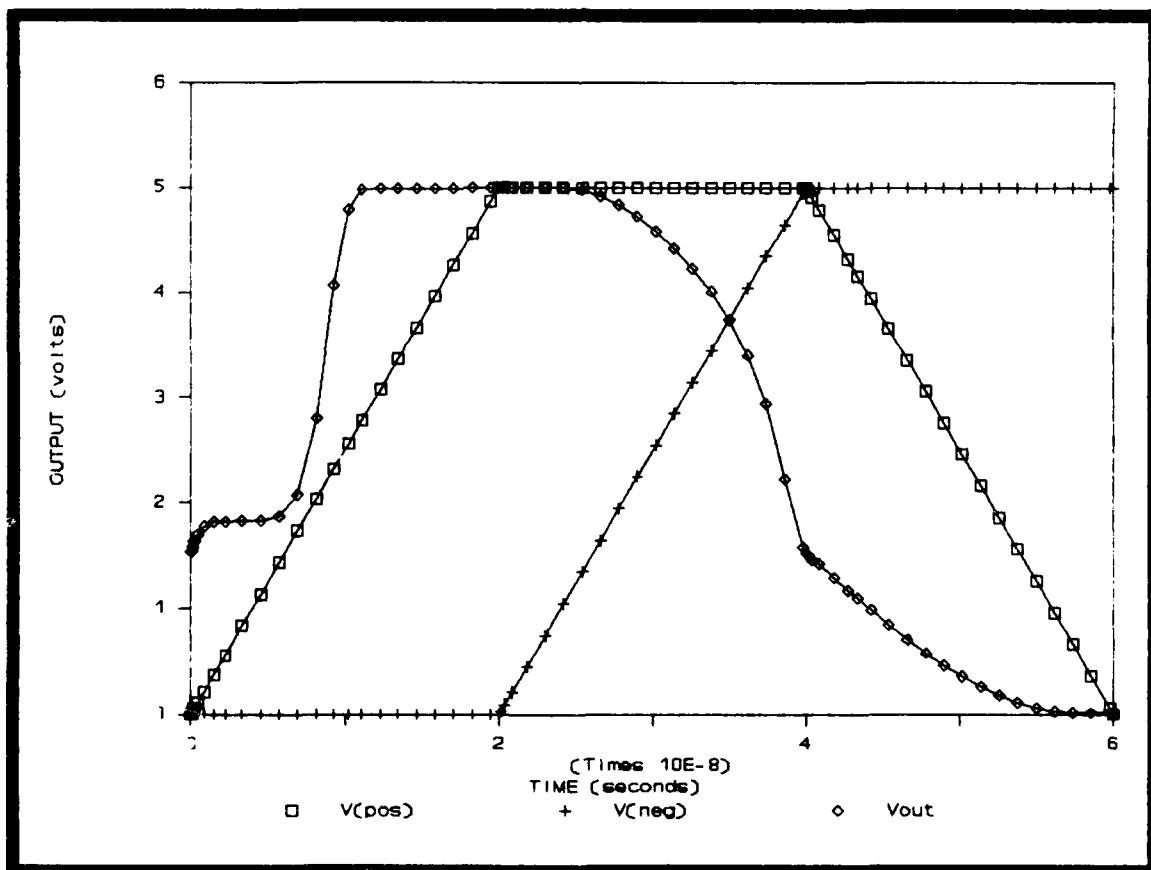

Figure D-7. Comparator circuit operation.

```
3-INPUT NORGATE
*
VCC     1000   0   dc   5v
*
*3-INPUT NOR GATE
*A=100 B=150 C=200 OUT=300 VCC=400 GND=500
.subckt norgate3_in    100  150  200  300  400  500
M1     400    200    198    400    P    L=2U  W=12U
M2     198    150    199    400    P    L=2U  W=12U
M3     199    100    300    400    P    L=2U  W=12U
M4     300    100    500    500    N    L=2U  W=4U
M5     300    150    500    500    N    L=2U  W=4U
M6     300    200    500    500    N    L=2U  W=4U
.ends subckt
*
XNORGATE    100  150  200  300  1000  0  norgate3_in
*
VA   100 0 PWL (Ons 0 10ns 0 11ns 5 20ns 5 21ns 0)
VB   150 0 PWL (Ons 0 20ns 0 21ns 5 30ns 5 31ns 0)
VC   200 0 PWL (Ons 0 30ns 0 31ns 5 40ns 5 41ns 0)
.END
```
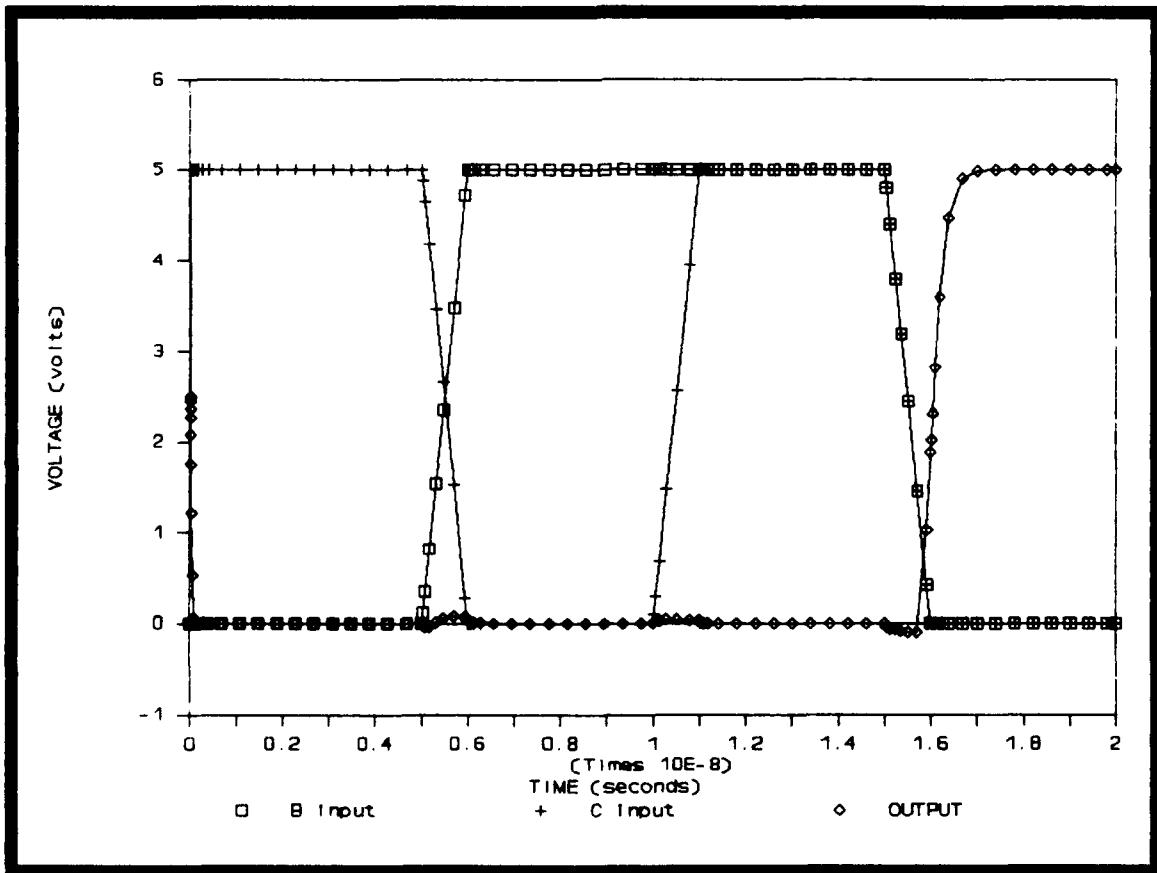

Figure D-8. 3-Input NOR gate response.

```
*LATCH UTILIZING TWO 3-INPUT NORGATES
VCC     1000   0   dc   5v
*
*3-INPUT NOR GATE
*A=100 B=150 C=200 OUT=300 VCC=400 GND=500
.subckt norgate3_in   100  150  200  300  400  500
M1      400   200   198   400   P   L=2U  W=12U
M2      198   150   199   400   P   L=2U  W=12U
M3      199   100   300   400   P   L=2U  W=12U
M4      300   100   500   500   N   L=2U  W=4U
M5      300   150   500   500   N   L=2U  W=4U
M6      300   200   500   500   N   L=2U  W=4U
.ends subckt
XNORGATE1   21   24   0  23   1000   0   norgate3_in
XNORGATE2   23   22   0  24   1000   0   norgate3_in
*
VA   21   0   PWL(Ons 0 5ns 0 6ns 5 10ns 5 11ns 0 16ns 0 17ns 5)
VB   22   0   PWL(Ons 0 10ns 0 11ns 5 15ns 5 16ns 0)
```
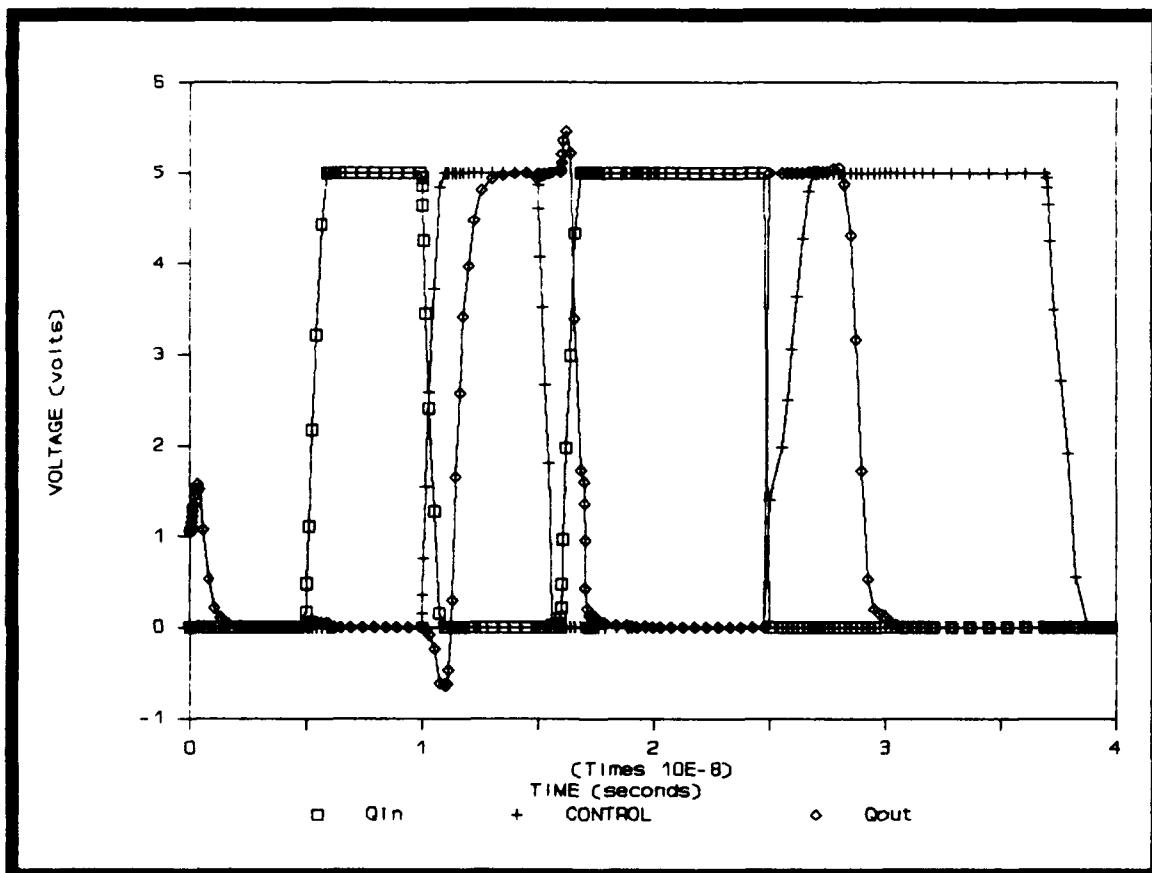

Figure D-9.   Latch response utilizing the 3-input NOR gates.
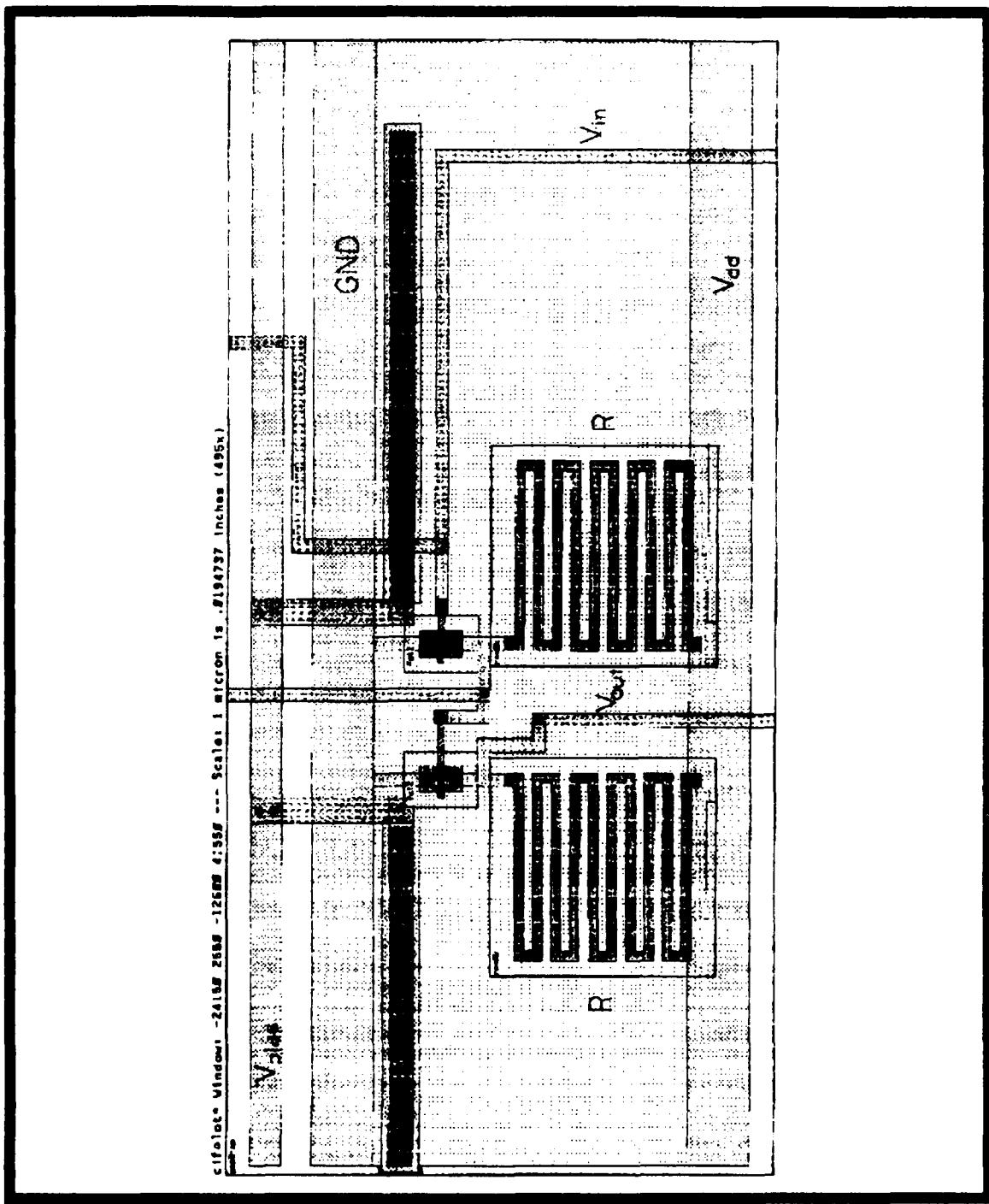
Figure E-1. Charge signal amplifier layout.

cifplot* Window: -76 54 -29 57 --- Scale: 1 micron is .09844 inches (27 ox)
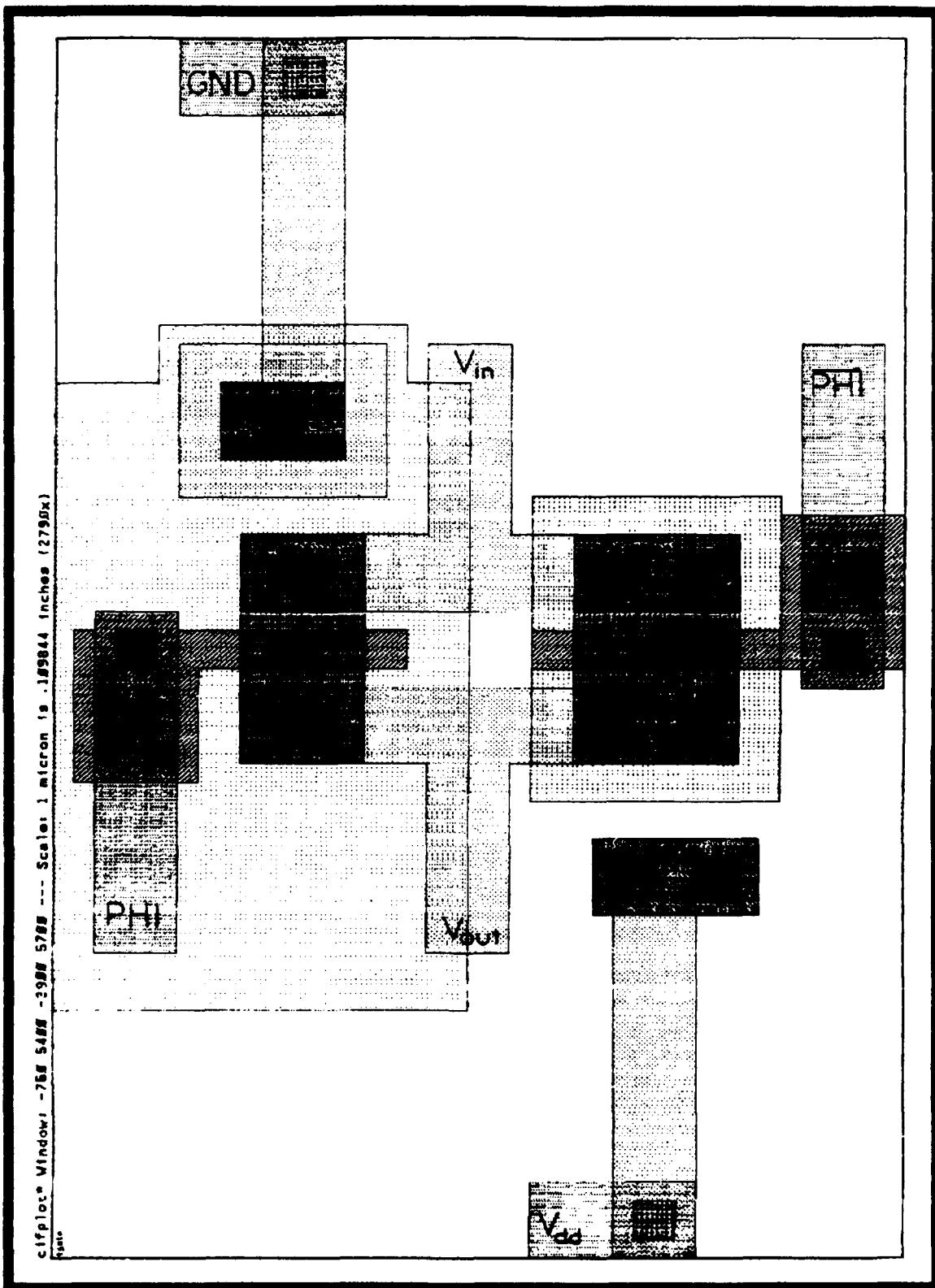
Figure E-2.   Transmission gate layout.
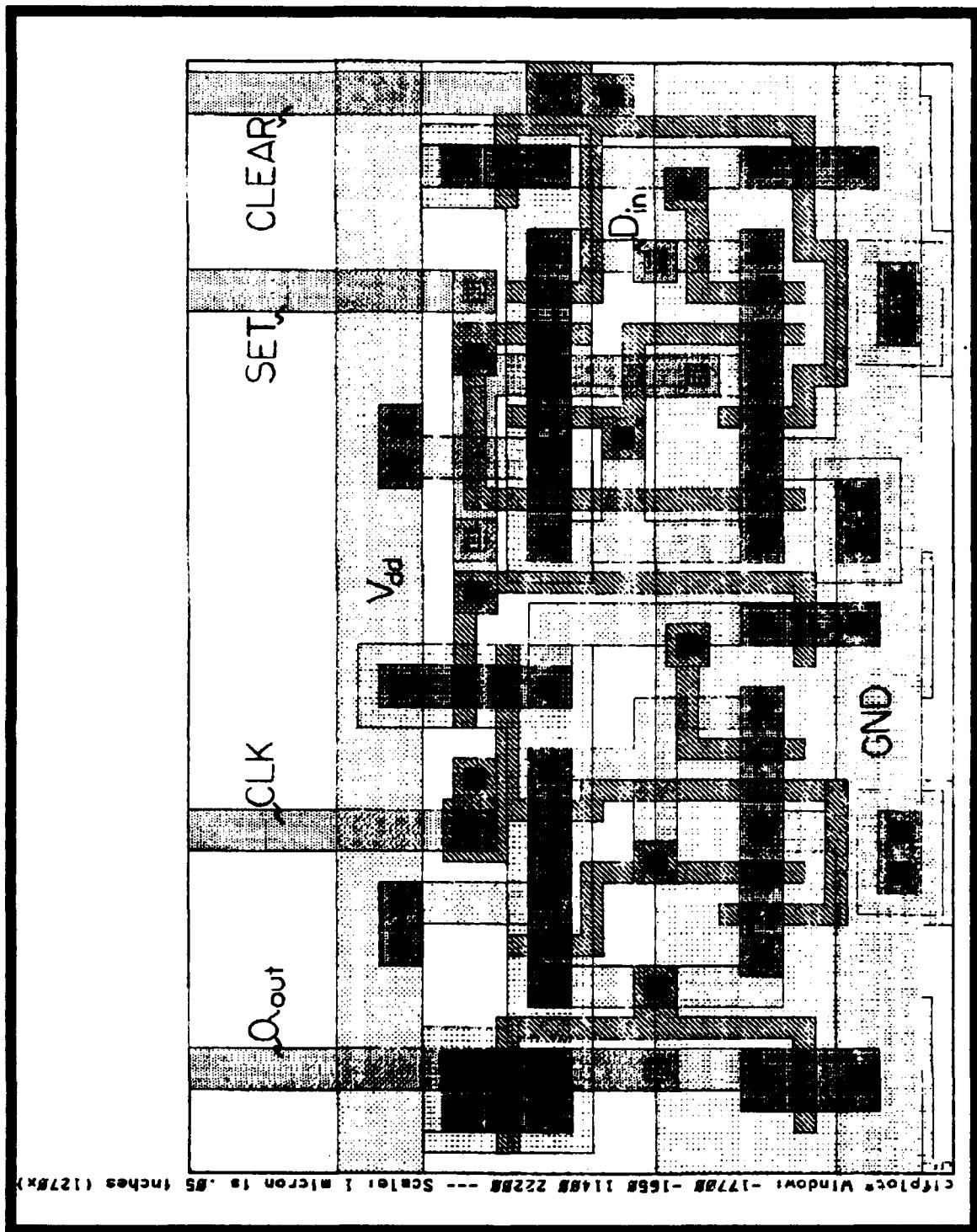
Figure E-3.   D Flip-Flop layout.
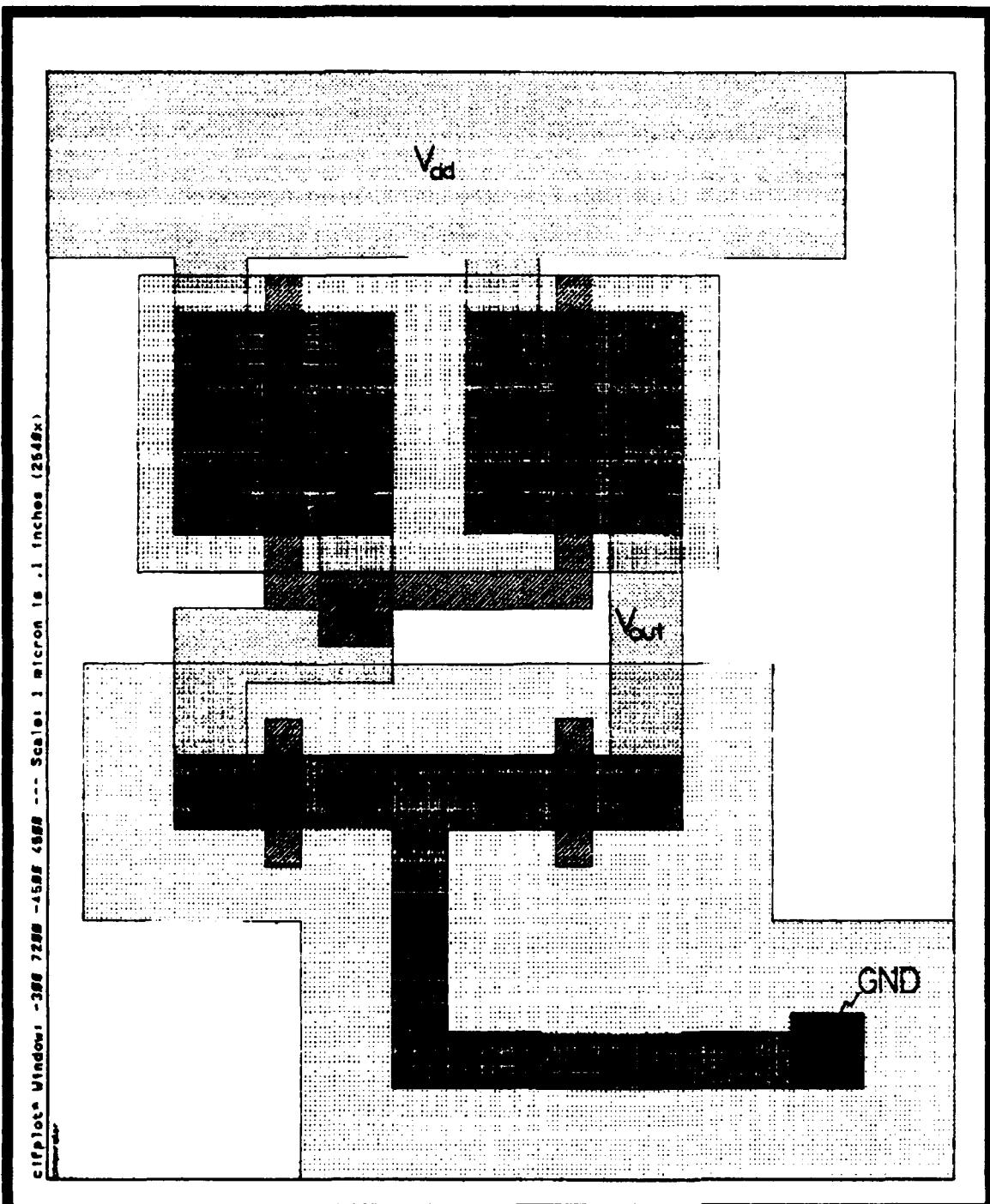
Figure E-4.   Comparator circuit layout.
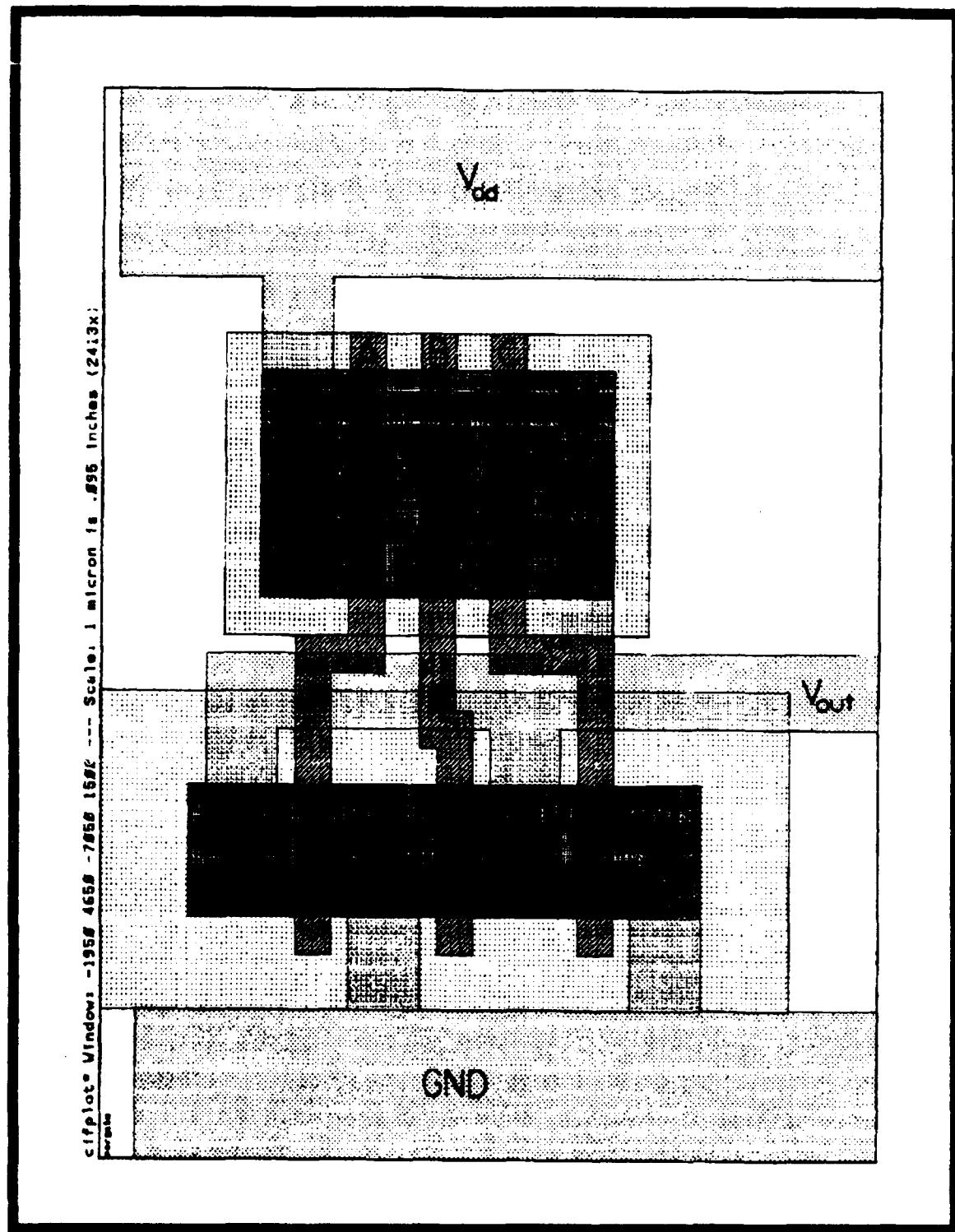
Figure E-5. 3-Input NOR gate layout.

Appendix F: BASICA Instrumentation Driver Programs

The following program controlled the IEEE-488 Interface bus, the Keithley 617 Programmable Electrometer, and the HP 54100 Digital Storage Oscilloscope for the film characterization tests, the taxel characterization tests, and the shape recognition tests.

```
10   'HPSCOPE.BAS",A
20
'================================================================
30   '
40   'IEEE488 DEVICE DRIVER EXAMPLE PROGRAM
50   '
60   'BASICA
70   '
80   '(HPSCOPE.BAS)
90   '
100  'Serial Poll with STRING transfer
110  '
120  'MetraByte Corporation
130  '
140
'================================================================
150  '
160  '
170  CLS : KEY OFF: LOCATE 25, 1: PRINT "Press any key to
     exit program";
180  LOCATE 1, 1
190  '
200  'This is an example of reading data from the device
     numbered DEV2%, in this
210  'case a FLUKE MODEL 617 PROGRAMMABLE ELECTROMETER
220  'To run with a different device number, change command
     strings in
230  'lines refering to DEVICE DEV2%.
240  '
250  '##### Establish communication with device driver #####
260  '
270  OPEN "$DV488" FOR OUTPUT AS #1
280  PRINT #1, "BUFFERCLEAR"
290  OPEN "$DV488" FOR INPUT AS #2
300  ON ERROR GOTO 1540
310  '
320  '##### Initialize MBC-488 board using "SYSCON" command
330  '
340  PRINT #1, "SYSCON MAD1=3 CIC1=1 BA1=&H300"
350  DEV1% = 15
360  DEV2% = 27
370  '
```

```
380 '##### Set ELECTROMETER and HP DIGITIZING OSCILLOSCOPE
    into REMOTE #####
390 '
400 PRINT #1, "REMOTE ",DEV1%
410 PRINT #1, "REMOTE ",DEV2%
420 '
430 '##### Set TIMEOUT (timeout time=0.056 x A%) #####
440 '
450 A% = 100
460 PRINT #1, "TIMEOUT", A%
470 '
480 '##### ZERO CHECK OF ELECTROMETER AND LOCKOUT PROMPT
490 INPUT; "LOCKOUT THE ELECTROMETER?", B$
500 C$ = "YES"
510 IF B$ = C$ THEN 530 ELSE
520 PRINT "THE ELECTROMETER IS NOT LOCKED OUT":GOTO 550
530 PRINT "THE ELECTROMETER IS LOCKED OUT"
540 PRINT #1, "LOCKOUT", DEV2%
550 CMD$ = "C1XZ1XCOXZOX"
560 PRINT #1, "OUTPUT ", DEV2%, " $ +", CMD$
570 CMD$ = "STOP"
580 PRINT #1, "OUTPUT ",DEV1%," $ +", CMD$
590 CMD$ = "RESET"
600 PRINT #1, "OUTPUT ",DEV1%," $ +", CMD$
610 CMD$ = "AUTOSCALE"
620 PRINT #1, "OUTPUT ",DEV1%," $ +", CMD$
630 CMD$ = "DISP GRAT GRID"
640 PRINT #1, "OUTPUT ",DEV1%," $ +", CMD$
650 CMD$ = "CHAN 1 RANGE .4"
660 PRINT #1, "OUTPUT ",DEV1%," $ +", CMD$
670 CMD$ = "TIMEBASE SENS 0.5"
680 PRINT #1, "OUTPUT ",DEV1%," $ +", CMD$
690 CMD$ = "TRIGGER LEVEL -0.3
700 PRINT #1, "OUTPUT ",DEV1%," $ +", CMD$
710 CMD$ = "ACQUIRE TYPE AVERAGE COUNT 8 POINTS 500"
720 PRINT #1, "OUTPUT ",DEV1%," $ +", CMD$
730 CMD$ = "TIMEBASE MODE SINGLE"
740 PRINT #1, "OUTPUT ",DEV1%," $ +", CMD$
750 LAP = 150 ' Fifteen second delay for instrument to
    process configuration data.
760 INCREMENT = .1
770 TO = TIMER : D$=DATE$
780 T1 = TO
790 WHILE LAP <> 0
800    WHILE (T1 < (TO + INCREMENT))
810    T1 = TIMER : IF D$<>DATE$ THEN T1=T1+86400!
820    WEND
830 D$=DATE$ : TO=TO+INCREMENT : IF TO>=86400! THEN
    TO=TO-86400! : T1=T1-86400!
840 LAP = LAP - 1
850 WEND
860 INPUT; "PRESS (S) TO STORE THE DATA OR (A) TO MAKE
    ANOTHER MEASUREMENT"; D$
```

```
870 IF D$ = "S" THEN GOTO 880 ELSE GOTO 450
880 CMD$ = "STORE CHANNEL 1, MEMORY 1"
890 PRINT #1, "OUTPUT ",DEV1%," $ +", CMD$
900 CMD$ = "STOP"
910 PRINT #1, "OUTPUT ",DEV1%," $ +", CMD$
920 INPUT "FILENAME FOR CHANNEL 1 DATA"; DF$
930 OPEN "O", #3, DF$
940 CMD$="WAVEFORM SOURCE MEMORY1 FORMAT ASCII"
950 PRINT #1, "OUTPUT ",DEV1%," $ +", CMD$
960 R$ = SPACE$(15)
970 CMD$ = "POINTS?"
980 PRINT #1, "OUTPUT ",DEV1%," $ +", CMD$
990 PRINT #1, "ENTER 15 $ +"
1000 INPUT #2, R$
1010 PNTS=VAL(R$)
1020 PRINT "Number of Points = ", PNTS
1030 CMD$ = "YREF?"
1040 PRINT #1, "OUTPUT ",DEV1%," $ +", CMD$
1050 PRINT #1, "ENTER 15 $ +"
1060 INPUT #2, R$
1070 YREF = VAL(R$)
1080 CMD$ = "YINC?"
1090 PRINT #1, "OUTPUT ",DEV1%," $ +", CMD$
1100 PRINT #1, "ENTER 15 $ +"
1110 INPUT #2, R$
1120 YINC = VAL(R$)
1130 CMD$ = "YOR?"
1140 PRINT #1, "OUTPUT ",DEV1%," $ +", CMD$
1150 PRINT #1, "ENTER 15 $ +"
1160 INPUT #2, R$
1170 YORG = VAL(R$)
1180 CMD$ = "XINC?"
1190 PRINT #1, "OUTPUT ",DEV1%," $ +", CMD$
1200 PRINT #1, "ENTER 15 $ +"
1210 INPUT #2, R$
1220 XINC = VAL(R$)
1230 CMD$ = "XOR?"
1240 PRINT #1, "OUTPUT ",DEV1%," $ +", CMD$
1250 PRINT #1, "ENTER 15 $ +"
1260 INPUT #2, R$
1270 XORG = VAL(R$)
1280 CMD$ = "XREF?"
1290 PRINT #1, "OUTPUT ",DEV1%," $ +", CMD$
1300 PRINT #1, "ENTER 15 $ +"
1310 INPUT #2, R$
1320 XREF = VAL(R$)
1330 PRINT YINC, YORG, YREF, XINC, XORG, XREF
1340 X$ = SPACE$(15)
1350 Y$ = SPACE$(15)
1360 CMD$ = "DATA?"
1370 PRINT #1, "OUTPUT ",DEV1%," $ +", CMD$
1380 FOR I = 1 TO PNTS
1390     PRINT #1, "ENTER 15 $ +"
```

```
1400     INPUT #2, Y$
1410     X =(I*XINC)+XORG
1420     Y = ((VAL(Y$)-YREF)*YINC)+YORG
1430     WRITE #3, X, Y
1440 NEXT I
1450 CLOSE #3
1460 CMD$ = "LOCAL"
1470 PRINT #1, "OUTPUT ",DEV1%," $ +", CMD$
1480 '
1490 '
1500 'KX$ = INKEY$: IF KX$ = "" THEN GOTO 960
1510 KEY ON
1520 CLOSE
1530 STOP
1540 IF (ERR <> 68) AND (ERR <> 57) THEN PRINT "BASIC ERROR
     # "; ERR; " IN LINE "; ERL: STOP
1550 INPUT #2, E$
1560 PRINT "$DV488 driver returned error number - ", E$
1570 INPUT #2, E$
1580 PRINT E$
1590 INPUT #2, E$
1600 PRINT E$
1610 END
```

The following program controlled the IEEE-488 GPIB
Interface bus and the HP 4145 Semiconductor Parameter
Analyzer for the MOSFET characterization tests and the
amplifier characterization tests.

```
5   REM  THIS PROGRAM WILL "CAPTURE" THE SCREEN ON THE HP4145
10  REM  INITIALIZE THE 488 VARIABLES
15  DEF SEG=&HC400
20  INIT%=0
30  TRANSMIT%=3
40  RECIEVE%=6
50  SEND%=9
60  SPOLL%=12
70  ENTER%=21
80  HP4145%=2: MYADDR%=21
90  SYSCON%=0
99   REM initialize the card
100 CALL INIT%(MYADDR%,SYSCON%)
105 REM GET THE DRAIN VOLTAGE DATA
110 PRINT " "
115 INPUT "ENTER THE INITIAL VIN VOLTAGE:  ",VD1
120 INPUT "ENTER THE VIN VOLTAGE STEP SIZE:  ",VDS
125 INPUT "ENTER THE NUMBER OF STEPS:  ",VDNS
130 PRINT " "
135 REM GET THE GATE VOLTAGE DATA
140 INPUT "ENTER THE INITIAL BIAS VOLTAGE:  ",VG1
145 INPUT "ENTER THE BIAS VOLTAGE STEP SIZE:  ",VGS
```

```
150 INPUT "ENTER THE NUMBER OF STEPS:  ",VGNS
155 PRINT " "
160 REM GET THE VOUT DATA
165 REM DETERMINE THE NUMBER OF CURRENT POINTS TO FETCH
170 POINTS=VDNS*VGNS
172 OPTION BASE 1
173 REM DIMENSION THE ARRAY TO HOLD THE DATA
175 DIM A(POINTS)
180 PRINT "RETRIEVING THE VOUT VOLTAGE VALUES FROM HP4145"
185 PRINT " "
190 GOSUB 500
260   REM COMBINE THE THREE SETS OF DATA INTO THE FINAL
      OUTPUT
265   INPUT "ENTER THE NAME OF FILE TO STORE DATA:  ", N$
270   OPEN "O", #1, N$
275   VD=VD1
276   VG=VG1
280   DIM OUTDATA(VDNS,VGNS)
282   FOR K=1 TO VGNS
285        FOR J=1 TO VDNS
287             OUTDATA(J,K)=A(J +(K-1)*VDNS)
290        NEXT J
292   NEXT K
293   REM WRITE THE OUTPUT FILE
294   PRINT#1,VD1,
295   FOR K=1 TO VGNS
296        IF K>1 THEN VG=VG+VGS
297        PRINT#1,CHR$(9);VG,
298   NEXT K
299   PRINT#1,""
300   FOR J=1 TO VDNS
301        IF J>1 THEN VD=VD+VDS
302        PRINT#1,VD,
303        FOR K=1 TO VGNS
310                PRINT#1,CHR$(9);OUTDATA(J,K),
320           NEXT K
321        PRINT#1,""
325   NEXT J
330 CLOSE #1
335 PRINT "ALL DONE" :SYSTEM
340 STOP
500 REM SUBROUTINE TO TRANSFER DATA FROM HP4145 TO PC
501 CALL SPOLL%(HP4145%,POLL%,STATUS%)
506 S$="UNL UNT"
507 CALL TRANSMIT(S$,STATUS%)
508 S$="BC"
509 CALL SEND%(HP4145%,S$,STATUS%)
510 S$="DO 'VOUT'"
520 CALL SEND%(HP4145%,S$,STATUS%)
530 S$="MLA TALK 2"
540 CALL TRANSMIT%(S$,STATUS%)
545 TEMP$=SPACE$(13)
550 FOR I=1 TO POINTS
```

```
560 CALL RECIEVE%(TEMP$,LENGTH%,STATUS%)
571 A(I)=VAL(RIGHT$(TEMP$,12))
580 NEXT I
585 S$="UNL UNT"
586 CALL TRANSMIT%(S$,STATUS%)
590 RETURN
600 END
```

Appendix G: Taxel Characterization Results
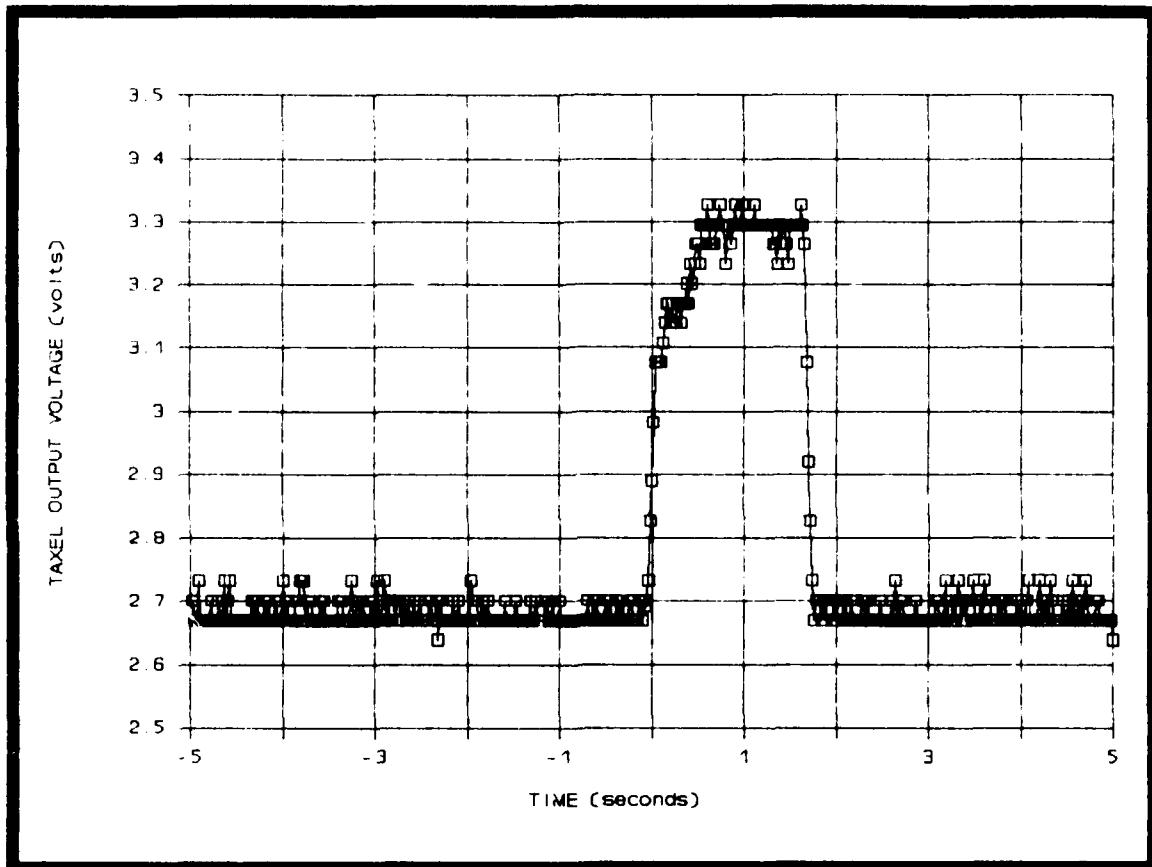
Figure G-1. Response of taxel number-24 on chip number-16 to a 40-gram load for a dc bias signal of 1 volt applied to the taxel for 1 second and then removed. (The load was applied at time zero and removed 1.75 seconds later).
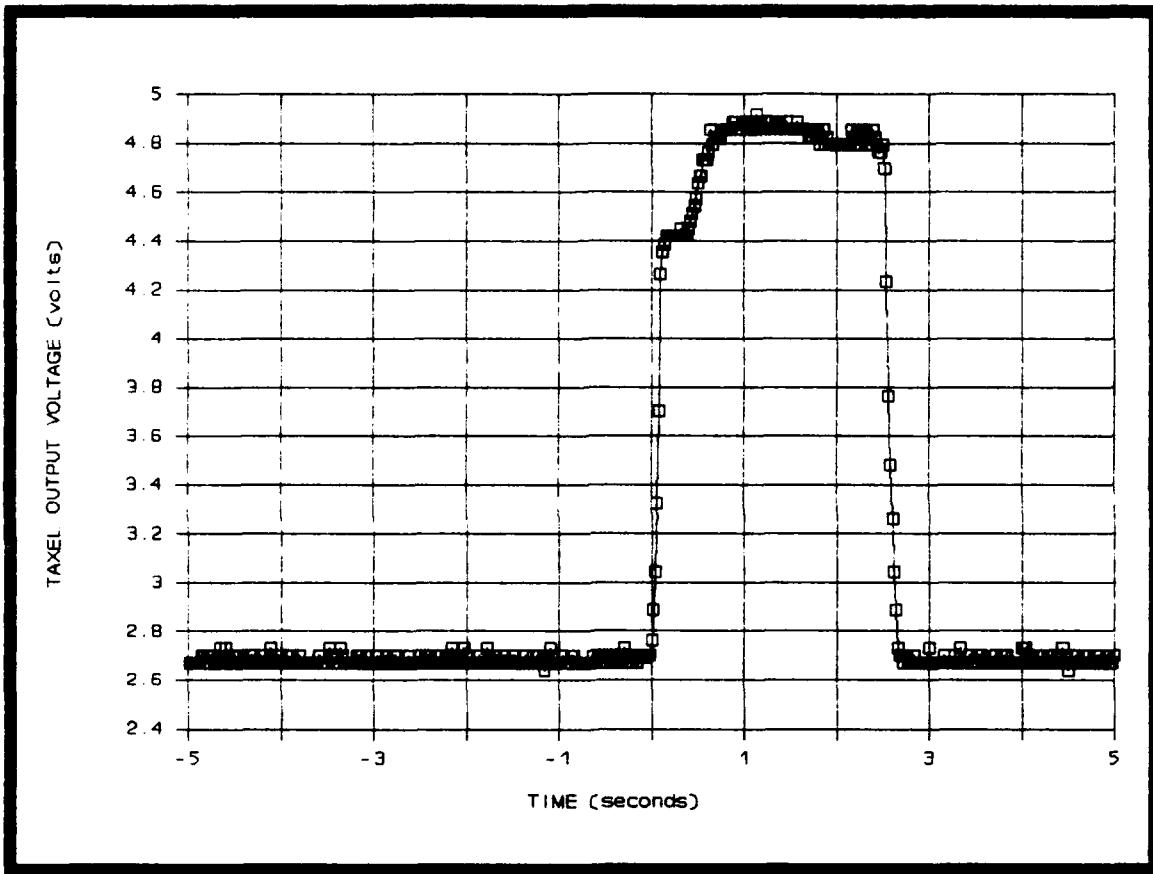
Figure G-2. Response of taxel number-24 on chip number-16 to a 40-gram load for a dc bias signal of 2 volts applied to the taxel for 1 second and then removed. (The load was applied at time zero and removed 2.45 seconds later).
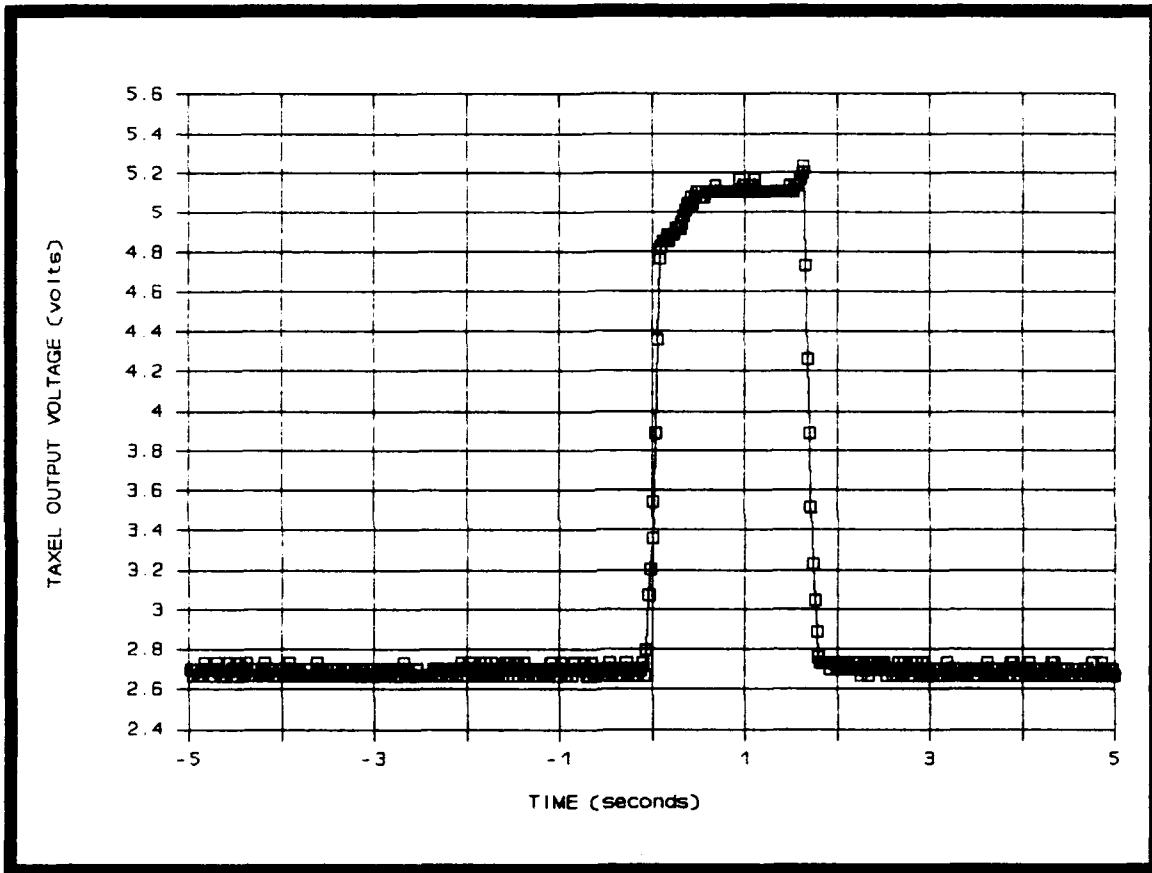
Figure G-3. Response of taxel number-24 on chip number-16 to a 40-gram load for a dc bias signal of 2.5 volts applied to the taxel for 1 second and then removed. (The load was applied at time zero and removed 1.75 seconds later).
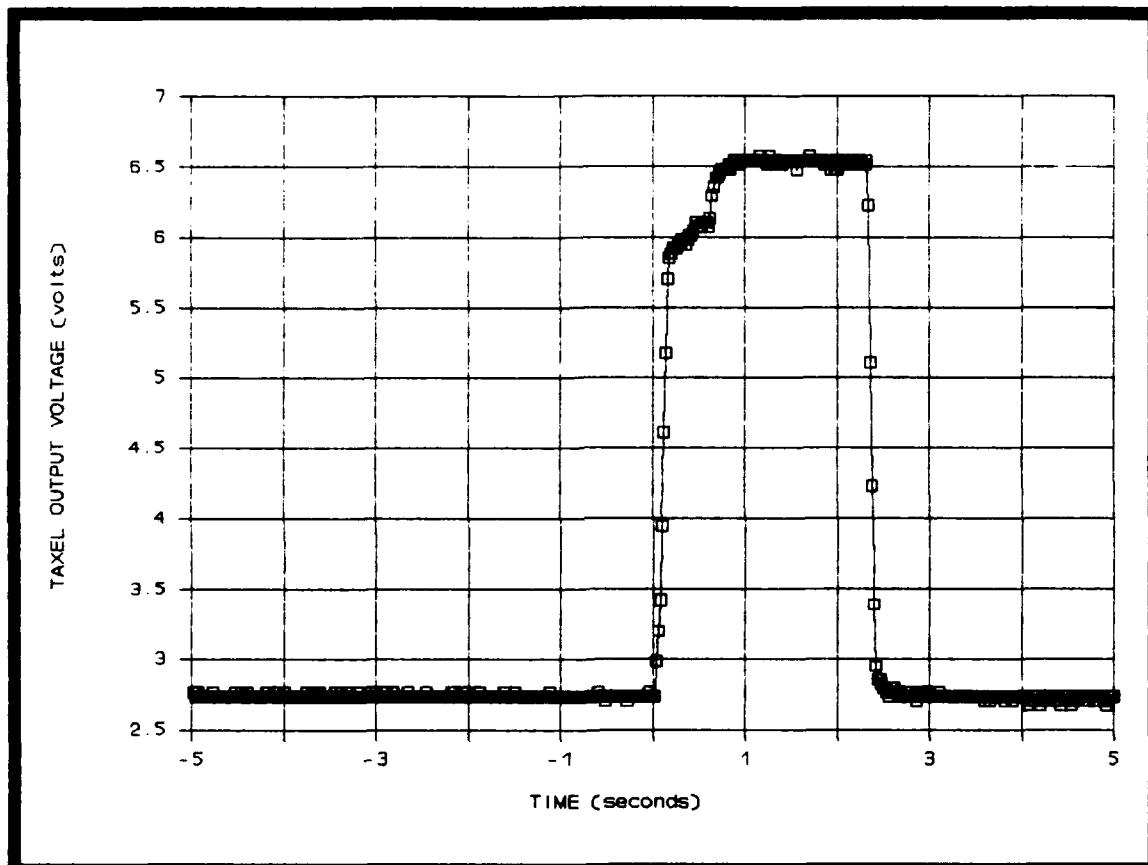
Figure G-4. Response of taxel number-24 on chip number-16 to
a 40-gram load for a dc bias signal of 3 volts applied to the
taxel for 1 second and then removed. (The load was applied at
time zero and removed 2.25 seconds later).
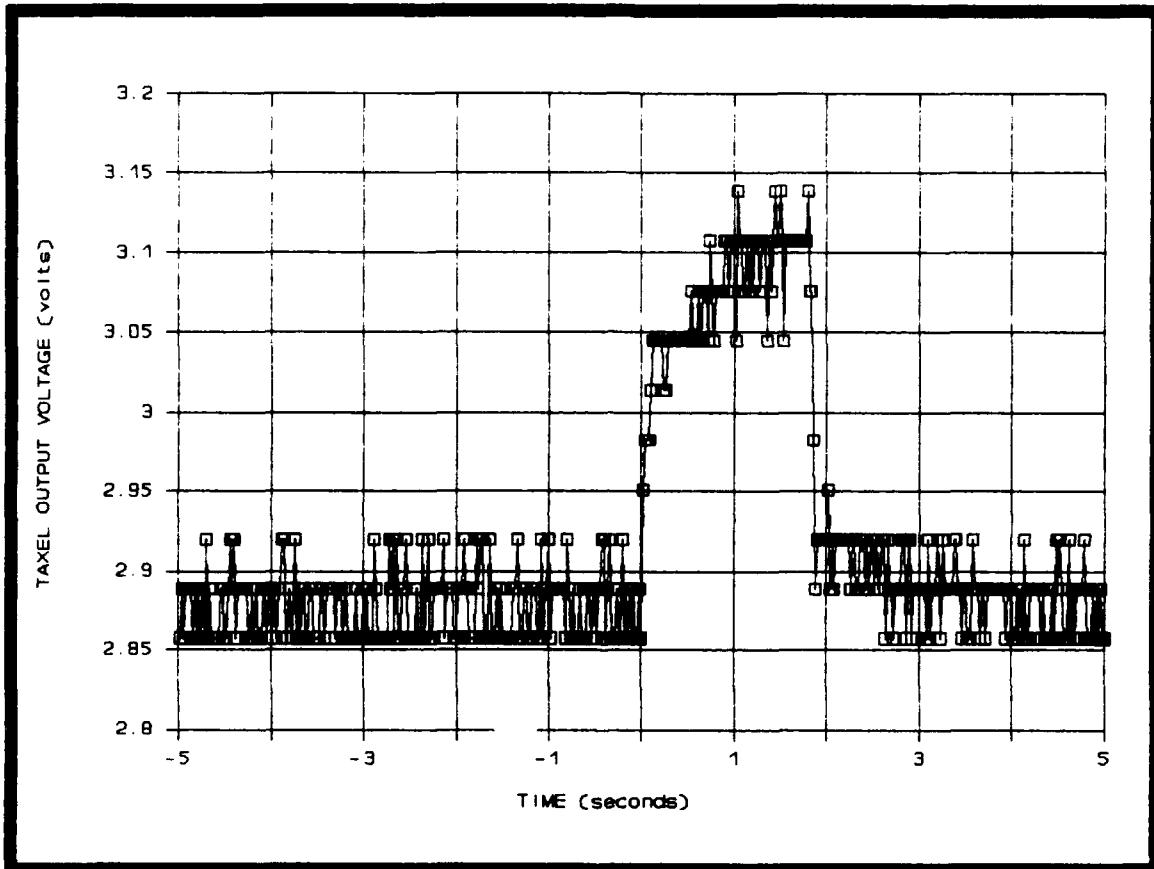
Figure G-5. Response of taxel number-25 on chip number-16 to a 3-gram load for a dc bias signal of 2.5 volts applied to the taxel for 1 second and then removed. (The load was applied at time zero and removed 1.75 seconds later).
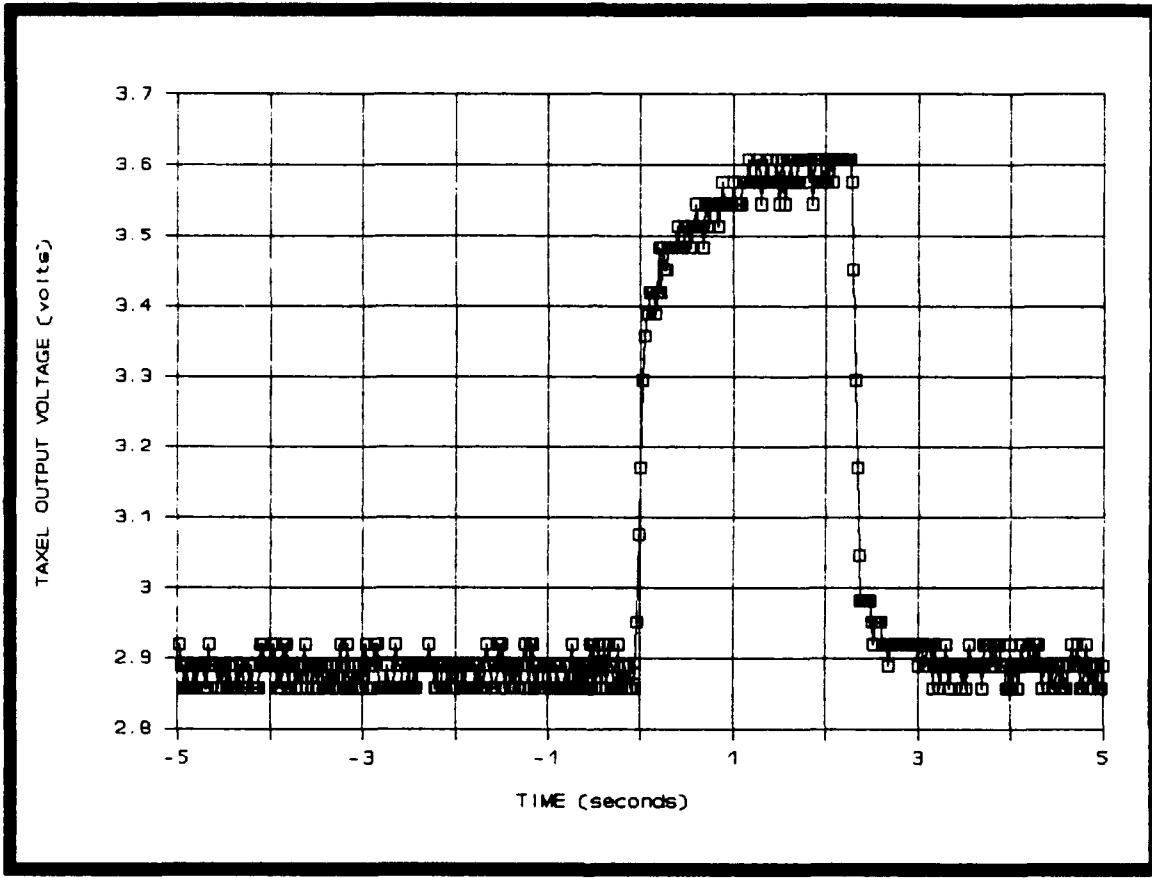
Figure G-6. Response of taxel number-25 on chip number-16 to a 16-gram load for a dc bias signal of 2.5 volts applied to the taxel for 1 second and then removed. (The load was applied at time zero and removed 1.25 seconds later).
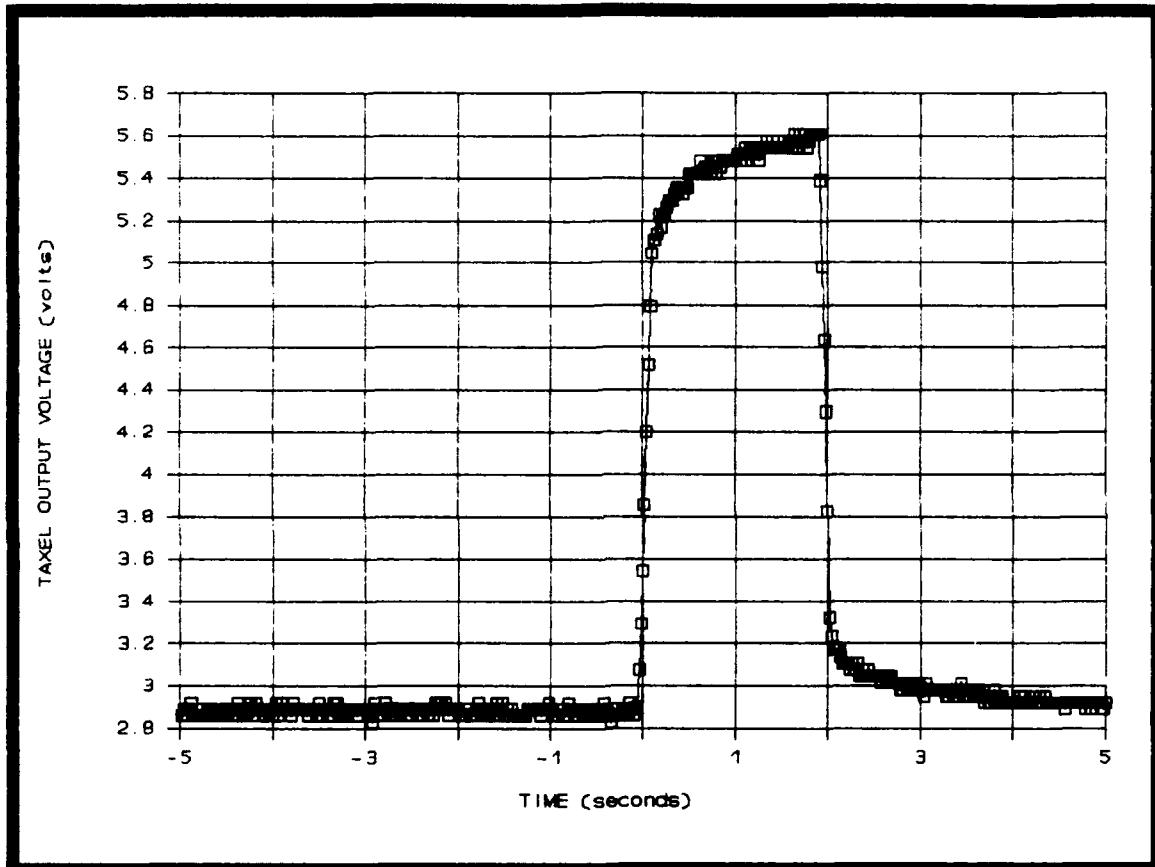
Figure G-7. Response of taxel number-25 on chip number-6 to
a 40-gram load for a dc bias signal of 2.5 volts applied to
the taxel for 1 second and then removed. (The load was
applied at time zero and removed 1.95 seconds later).
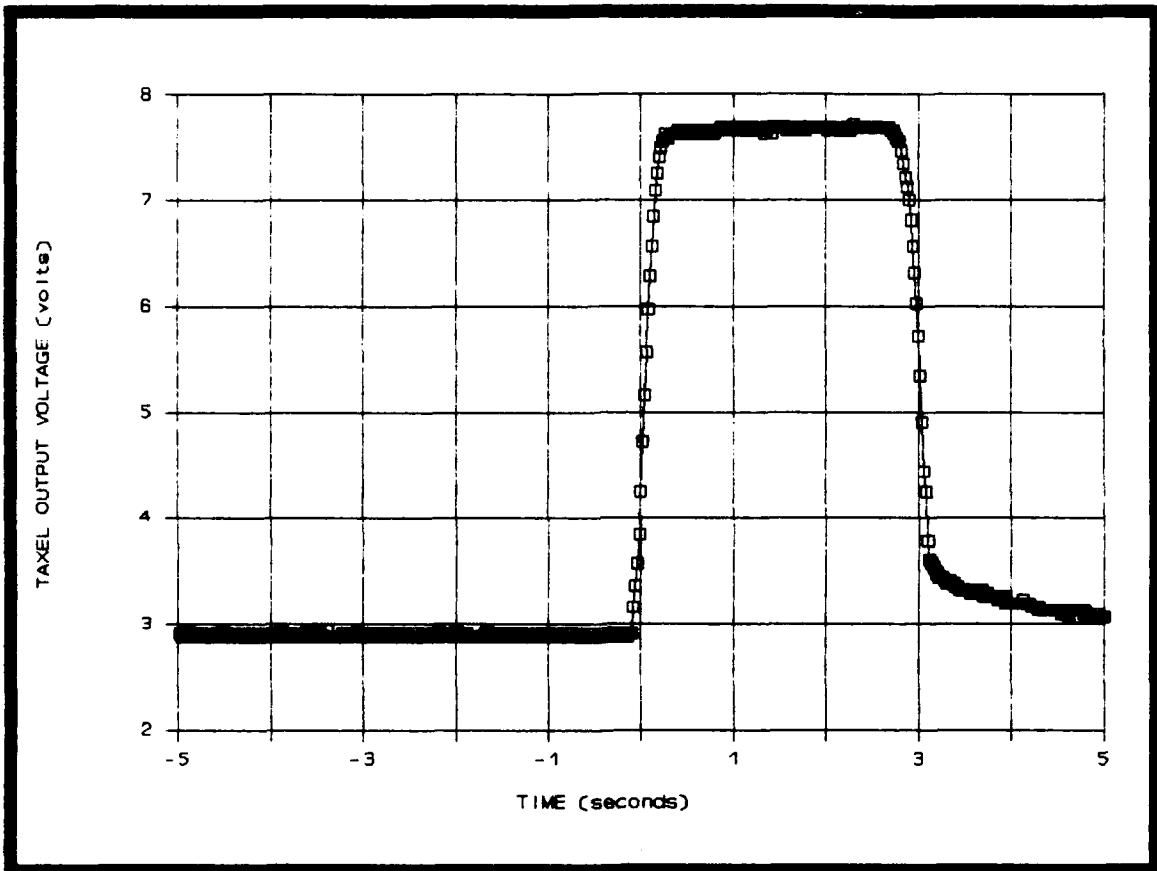
Figure G-8. Response of taxel number-25 on chip number-16 to an 81-gram load for a dc bias signal of 2.5 volts applied to the taxel for 1 second and then removed. (The load was applied at time zero and removed 1.75 seconds later).

Appendix H: Shape Recognition Test
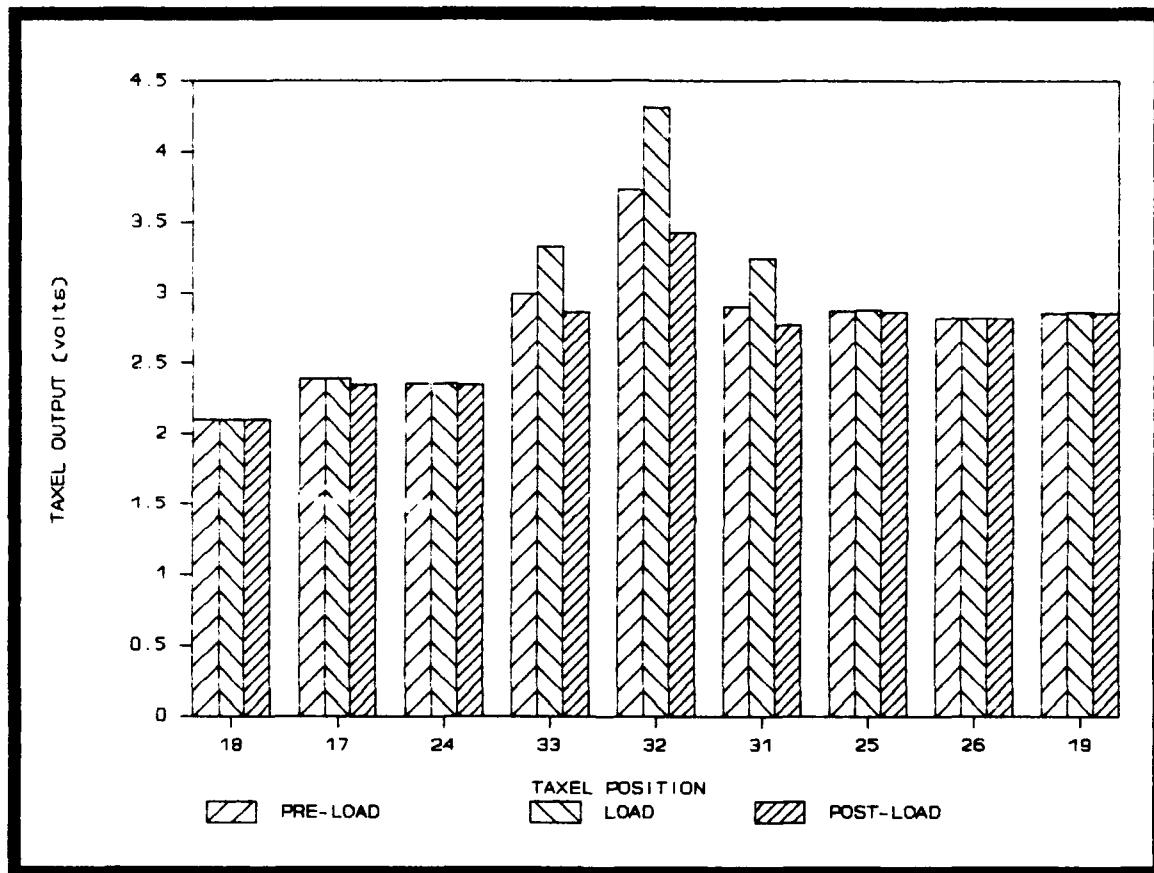
Figure H-1. The pre-load, load, and post-load multiplexed responses of the 3 x 3 taxel array for chip number-16 recorded approximately 1.0, 1.5, and 2.0 minutes, respectively, after a 10-volt dc gate bias was removed. (Test 1).
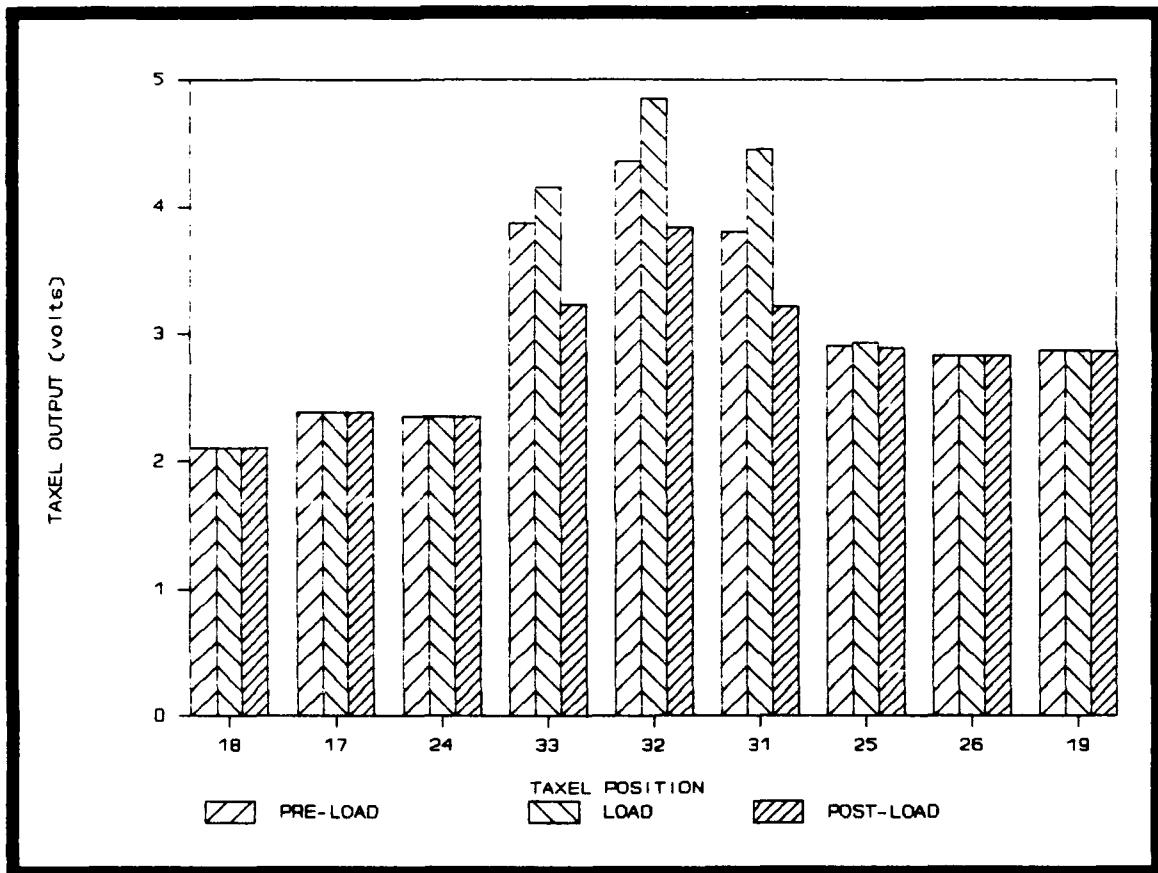
Figure H-2. The pre-load, load, and post-load multiplexed responses of the 3 x 3 taxel array for chip number-16 recorded approximately 1.0, 1.5, and 2.0 minutes, respectively, after a 10-volt dc gate bias was removed. (Test 2).
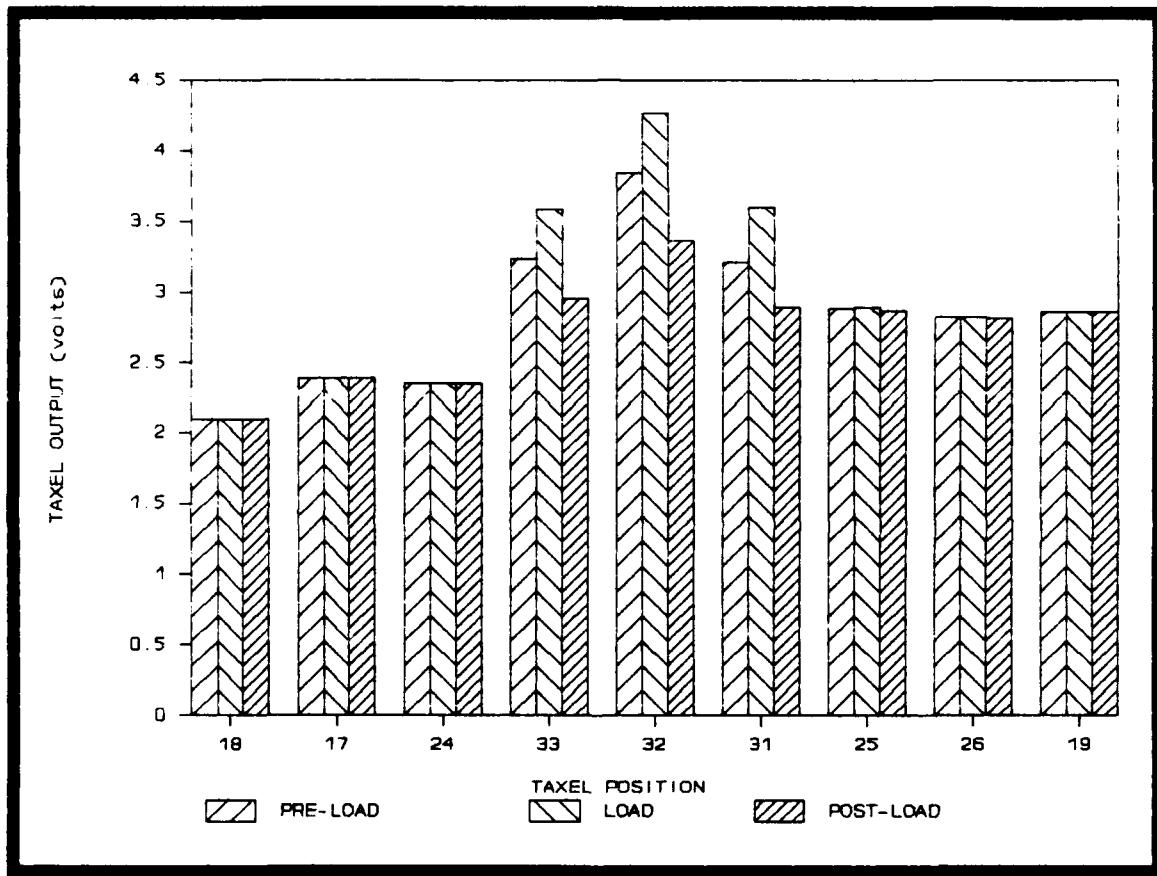
Figure H-3. The pre-load, load, and post-load multiplexed responses of the 3 x 3 taxel array for chip number-16 recorded approximately 1.0, 1.5, and 2.0 minutes, respectively, after a 10-volt dc gate bias was removed. (Test 3).

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Vita

Captain Robert C. Fitch, Jr. ███████████████████ ██████████████████ He graduated from Tunkhannock Area High School, Tunkhannock, Pennsylvania in 1979. Four years later he graduated from the Pennsylvania State University with a Bachelor of Science in Mechanical Engineering. He attended Officer Training School and was commissioned in 1984. Afterwards, he completed an AFIT assignment to Louisiana Tech University where he received a Bachelor of Science in Electrical Engineering in 1985. From there he was assigned to the 6545th Test Group at Hill Air Force Base Utah and served as an Airborne Remote Control Officer aboard a C-130 aircraft and also as a Test Instrumentation Engineer/Project Manager. He left Utah in May 1989 to attend the School of Engineering at the Air Force Institute of Technology.

(cont)

→ Robotics; Piezoelectric material/transducers; Silicon/integrated circuits; Polymeric films; Polyvinylidenes /thin films; Theses; Shape/touch/ recognition; Flip flop circuits;

Test and evaluation; Image processing; Analogs/multiplexing; Metal oxide semiconductors; Field effect transistors; Very large scale integration. (mm)