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A NEW MULTI-DECODER PLA DESIGN

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19. ABSTRACT (Continue on reverse if necessary and identify by block number)
A multi-decoder design for PLA devices is introduced and found to be superior to both two decoder ROM and single decoder PLA devices in implementing a special class of Boolean expressions. In this class the logic expressions may be lengthy but are restricted in the number of input variables comprising each p-term. A theoretical analysis of the area efficiency of the new design is supplemented by CAD design examples which verify its superiority. Implementation of the multi-decoder design using three dimensional micro-circuit topography to attain even greater savings in area and speed is considered in the conclusion of this report.
A NEW MULTI-DECODER PLA DESIGN

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Abstract: A multi-decoder design for PLA devices is introduced and found to be superior to both two decoder ROM and single decoder PLA devices in implementing a special class of Boolean expressions. In this class the logic expressions may be lengthy but are restricted in the number of input variables comprising each p-term. A theoretical analysis of the area efficiency of the new design is supplemented by CAD design examples which verify its superiority. Implementation of the multi-decoder design using three dimensional microcircuit topography attain even greater savings in area and speed is considered in the conclusion of this paper.

I. INTRODUCTION

A ROM device with two decoders, n inputs and l outputs requires an area proportional to the number of cells or crosspoints which total 2n(2n/2) - l2. For simplicity we assume the two decoders are identical. The useful space for data storage is of size 2n(2n/2) cells. If a ROM is implemented in a one decoder design equivalent to a single decoder PLA capable of accommodating the maximum number of p-terms (2^n) given n total inputs, it would be of size (2n - 1)2^n with an unacceptable decoder area of 2n2^n. In addition to requiring less area, a two decoder design has a propagation delay proportional to \sqrt{2^n} while a single decoder ROM has a delay proportional to 2^n as an order of magnitude estimate for both cases. Since PLA devices are usually designed with a single decoder, the transition to a two decoder PLA design is justifiable only if a sufficiently large number of p-terms are required for the output expression(s). Normally the decomposition to a two decoder architecture requires a preconditioning of the given Boolean expressions that is likely to result in the decision to utilize a two decoder ROM architecture.

In Section II we consider a particular class of expressions in which the n inputs are partitioned into s subsets of r inputs each and in which each subset can contribute at the most y variables to each p-term. Each p-term in the final output expression may then contain up to s x y input variables. It is found that there are combinations of values of q, n and s for which a two decoder PLA, capable of implementing any expression in the above class, is quite superior to both a one decoder PLA and to a regular two decoder ROM. The new multi-decoder PLA designs are ROM-like in the sense that the AND arrays (the decoders) are preprogrammed, and are PLA-like in the sense that they implement only a restricted class of expressions. Potential applications where such large but restricted expressions might arise include pattern recognition, knowledge based systems and artificial intelligence. The proposed multi-decoder PLA devices need not be restricted to the aforementioned cases with preprogrammed decoders. This is done in Section II only to establish the need and utility of such devices which then could be designed without preprogramming the decoders to supply greater flexibility and potential use.

The multi-decoder PLA design is compared to a ROM design by using both the simplified theoretical analysis in Section II as well as the more precise area assessment made in Section III based on actual CAD layout design examples. The ROM design in Section III is based on an interesting approach utilizing a dual decoder architecture which can be viewed as a cascade of two one decoder ROMs. This design consequently lends itself for iterative cascading of single decoder ROMs to produce multi-decoder ROMs and PLAs. Also, in the case of a ROM, the exact allocation of inputs to each decoder is decided upon by minimizing a desired cost function such as total silicon area as explained in Section III. The possibility of a multi-decoder ROM implemented with three-dimensional microcircuit topography having substantially reduced propagation delay is among the topics recommended for further research in the conclusion. Section IV.

II. A MULTI-DECODER DESIGN FOR A CLASS OF PLA DEVICES

In this section we consider the performance of a new class of multi-decoder PLA devices that implement a class of Boolean expressions with restricted p-terms as mentioned above. These new devices are found to be more area efficient than a ROM or single decoder PLA implementation of such expressions. The following definitions are used

n = number of inputs
l = number of outputs
s = number of subsets of inputs, each of size r
y = maximum contribution from each of the input subsets to each p-term
W1 = width of decoder for one decoder PLA design
W2 = width of each decoder for a multi-decoder PLA design
W3 = width of decoder for a two decoder ROM design
D1 = area of decoder in a one decoder PLA design
D2 = total decoder area in a multi-decoder PLA design
\[ D_3 = \text{total decoder area in a two decoder ROM} \]
\[ A_1, A_2 \text{ and } A_3 = \text{total chip area for a one & two decoder PLA, and two decoder ROM, respectively} \]
\[ M_1, M_2 \text{ and } M_3 = \text{total data storage area for above three cases} \]

where all areas are measured in terms of number of cells or crosspoints.

We consider first the case of a one decoder PLA design. The maximum width of the decoder, which corresponds to generation of the maximum number of p-terms given the above restriction of having q entries from each of the s input subsets, is

\[ W_1 = \left( \frac{r^s}{q!(r-q)!} \right)^{2^n} \]  \hspace{1cm} (2.1)

and its size is

\[ D_1 = 2nW_1 \]  \hspace{1cm} (2.2)

The data storage space is of

\[ M_1 = lW_1 \]  \hspace{1cm} (2.3)

locations and the total device size is

\[ A_1 = D_1 + M_1 = (2n + l)W_1 \]  \hspace{1cm} (2.4)

For an s decoder PLA design, with each decoder having one of the s input subsets as its input, we get

\[ W_s = \left( \frac{r^s}{q!(r-q)!} \right)^{2^n} \]  \hspace{1cm} (2.5)

The total size of the s decoders is

\[ D_s = s(2nW_1) = 2nW_s = 2nW_1^{1/s} \]  \hspace{1cm} (2.6)

and the data storage space is of size

\[ M_s = lW_1 = M_1 \]  \hspace{1cm} (2.7)

The chip size is then

\[ A_s = D_s + M_s = 2nW_1 + lW_s \]  \hspace{1cm} (2.8)

The memory space in both the one and multi-decoder PLA's are of identical size, but the size of the decoders is reduced dramatically in the multi-decoder design, as is apparent from the ratio,

\[ \frac{D_s}{D_1} = \frac{1}{W_s^{s-1}} \]  \hspace{1cm} (2.9)

from which we get

\[ \frac{A_s}{A_1} = \frac{2nW_1^{s-1} + l}{2n + l} \]  \hspace{1cm} (2.10)

The approximate expression above likewise applies to the ratio of the areas of the one and two decoder ROM's as mentioned in the introduction, which illustrates that the new multi-decoder PLA design achieves the same advantages in comparison to a one decoder PLA for implementing the class of Boolean expressions defined above.

In addition to demonstrating the superiority of the multi-decoder PLA in comparison to a one-decoder PLA design, we need to consider the conditions under which it compares favorably with a two-decoder ROM for which we have:

\[ W_2 = 2^{n/2} \]  \hspace{1cm} (2.11)
\[ D_2 = 2n(2^{n/2}) \]  \hspace{1cm} (2.12)
\[ M_2 = 2^n \]  \hspace{1cm} (2.13)
\[ A_2 = D_2 + M_2 = (2n + 2^n/2)2^{n/2} \]  \hspace{1cm} (2.14)

From (2.5), the following sufficient condition for \( A_2 < A_3 \) is easy to deduce

\[ q \leq \frac{n}{2^l + \log n} \]

and for \( s = 2 \) we get

\[ q \leq \frac{n}{2\log n} \]  \hspace{1cm} (2.15)

which gets closer to an equality as \( n \) increases and \( q \) becomes small. As \( n \) increases, the ratio \( A_2/A_3 \) decreases rapidly. The main source of the inefficiency of the ROM implementation for this range of values of \( n \) is that it contains much more memory space than is needed for the restricted class of expressions of interest. For example, for \( s = 2 \) and a given \( l \) and \( q \), \( A_2 \) increases as \( O(n^{2q^2}) \) while \( A_3 \) increases as \( O(2^n) \). So the area of a ROM increases exponentially in \( n \) versus the polynomial increase in the PLA implementation.

To illustrate the performance of the proposed multi-decoder PLAs we consider the following examples:

**Example 1:** For \( n = 18, s = 2, q = 2 \) and \( l = 1 \), we derive

\[ W_2 = 2^{11.44}, A_2 = 2.59 \times 10^4 \]

while

\[ W_3 = 5.2 \text{ and } A_3 = 2.81 \times 10^5 \]

and

\[ A_2/A_3 = 0.092 \]

A one decoder PLA will require

\[ W_1 = 2.07 \times 10^4 \text{ and } A_1 = 7.57 \times 10^5 \]

and

\[ A_2/A_1 = 0.033 \]

Clearly the two decoder PLA is superior to both the ROM implementation, which has more area and capability than is needed for the task at hand, and to the one decoder PLA, which is too long for practical implementation.

**Example 2:** Same as in Example 1 but with \( l = 0 \) outputs.

In this case we get

\[ A_2 = 2.13 \times 10^5 \]

\[ A_2/A_3 = 0.081 \]

and

\[ A_2/A_1 = 0.22 \]

where the ROM becomes more inefficient while the performance of the one decoder PLA improves slightly as predicted by Eq. (2.10) but still remains inferior to the two decoder design.

**Example 3:** Here we let \( n = 21, s = 2, q = 3 \) and \( l = 1 \).

In this case we get

\[ A_2 = 3.16 \times 10^6 \]

and

\[ A_2/A_3 = 0.87 \text{ and } A_2/A_1 = 0.02 \]
design rules. Fig. 2a depicts a two decoder PLA having the functional capability of a ROM, with 16 total inputs and one output. The decoder are fully decoded, each having 8 inputs and 256 8-bit p-terms. Fig. 2b depicts a two decoder PLA also having 16 total inputs and one output but with restricted input partitioning (q = 2) which results in 1:12 2-bit per terms per decoder. Both designs are capable of implementing the class of expressions of interest, however the ROM design has more capability than is needed for the task at hand. These designs form the basis for the following comparative analysis between a two decoder ROM and two decoder PLA.

Given the two designs illustrated in Fig. 2, we can determine precisely the silicon area $A_P$ required to implement a two decoder PLA ($s = 2$) with restricted input partitioning as defined in Section 1. $A_P$ is then compared to the total silicon area $A_R$ required to implement a two decoder PLA with unrestricted ROM capability.

Adhering to the scalable MOSIS design rules and the particular design shown in Fig. 2, a set of equations were empirically developed to determine absolute layout dimensions for any size two decoder PLA. The length $L_P$ and width $W_P$ of the layout are given by

$$L_P = C_1 \frac{n/2^s}{(n/2-1)!} q^2 + C_2 (t+1 \ MOD \ 2) + C_3$$

$$W_P = K_1 n + K_2 t \frac{n/2^s}{(n/2-1)!} q^2 + K_3$$

where

- $n =$ total number of inputs
- $q =$ number of variables each decoder contributes to a p-term
- $t =$ total number of outputs

representing the relevant parameters affecting device area and $C_1, C_2, C_3, K_1, K_2$ and $K_3$ are all design and technology dependent constants. These constants represent the contribution of device substructures (e.g. latches, pullups, various metallizations, OR and AND cells) to total device proportions Eqs. (3.1) and (3.2) apply only to the particular design implemented in Fig. 2 and may vary somewhat in form with even slight architectural alterations. Normalizing Eqs. (3.1) and (3.2) to the feature size $\lambda$ and inserting values for constants we obtain

$$L_P = 23.5 \frac{n/2^s}{(n/2-1)!} q^2 + \lambda (t+1 \ MOD \ 2) + 6.8 \ \lambda$$

$$W_P = 5.1 n + 31 \frac{n/2^s}{(n/2-1)!} q^2 + 288 \ \lambda$$

A 'C' program was written to automatically layout the two decoder PLA design described above. The physical layout of the design is based on the scalable V090.
where $\lambda$ may equal 75, 100 or 150 microns, corresponding to 1.25, 2.0 or 3.0 micrometer geometries as designated by the MOSIS scalable design rules. The modulus operator (MOD) present in Eqs. (3.1) and (3.3) simply reflects the architectural imposition that an even number of output lines must be present in the layout regardless of actual number of outputs, to maintain structural symmetry in the output OR array. Total silicon area for the two decoder PLA architecture, $A_P$, is then simply the product of Eqs. (3.3) and (3.4) given by

$$A_P = L_p \, W_p \, \lambda^2 \quad (3.5)$$

where area is expressed in terms of $\lambda^2$. It should be noted that the design chosen here to implement the PLA architecture is highly compact, leaving very little unused real estate within layout boundaries.

We next employ an approach similar to that above to determine $A_R$. The length $L_R$ and width $W_R$ of the silicon layout are given by

$$L_R = C_1 2^m + C_2 (l + 1 \, \text{MOD} \, 2) + C_4 2^{n-m} + C_4 \quad (3.6)$$

$$W_R = K_1 m + K_2 l 2^{n-m} + K_3 \quad (3.7)$$

where

- $m = \text{number of inputs entering upper decoder (PLA)}$
- $n = \text{total number of inputs}$
- $l = \text{total number of outputs}$

It should be noted that the variable $q$ is not considered here since there are no restrictions placed on the length of any $p$-term, each of which may contain up to $n$ variables in the final output expression. Once again normalizing to $\lambda$ and inserting precise values for constants we obtain

$$L_R = 10 \cdot 5 (2^m) + 11 (l + 1 \, \text{MOD} \, 2) + 13 (2^n - m) + 648 \, \lambda \quad (3.8)$$

$$W_R = 22 m + 51 (2^n - m) + 288 \, \lambda \quad (3.9)$$

Total silicon area for this structure is then

$$A_R = L_R \, W_R \, \lambda^2 \quad (3.10)$$

A particular value for $m$ can be determined, $m$, which minimizes $A_R$ given a particular $n$ and $l$. For this design $m$ is always greater than $n/2$, resulting in a fully minimized $A_R$ but having an unacceptably long rectangular silicon layout. A chosen $m$, in the range $n/2 < m < n$, will, for most selected values of $n$ and $l$, result in a more squarish and practical silicon layout at the expense of a slight increase in $A_R$ provided $n$ is not too large.

Area efficiency comparisons can be made between the dual decoder ROM and PLA layouts described above by examining the ratio $A_p / A_R$. Table 3.1 lists several values for $A_p / A_R$ given sample values for $n$, $l$ and $q$. Also listed are absolute values for $A_R$ given in terms of $\lambda^2$. For $n > 16$, $A_p$ was calculated using $m = n/2$ for comparative purposes only, since practical implementation is impossible.

It can be deduced from Table 3.1 that the ratio $A_p / A_R$ based on the particular design given above, coincides closely with the ratio $A_p / A_R$ derived by theoretical analysis in Section II. It can also be noted that for $q > 2$, either $A_p$ becomes too large for practical implementation or the ratio $A_p / A_R$ favors usage of the two decoder ROM. However, for $q < 2$, it can be concluded that the two decoder PLA design implemented above provides for a practical implementation of a particular class of logic expressions whereas a two decoder ROM implementation is either impractical or less area efficient.

IV. CONCLUSION

In this paper we have established the need for a new class of multi-decoder PLA devices that are superior to both ROM and single decoder PLA implementations of certain logic expressions that contain many $p$-terms but satisfy certain restrictions. Such devices could have wider applicability beyond this class of expressions. For example, the proposed multi-decoder design could be used for ROM implementations employing more than two decoders based on the design techniques exemplified in Section III. A particular ROM design using three decoders would most likely result in some savings in total decoder area, but more importantly, would result in even greater savings if implemented in three dimensional microcircuit topography. In this case the propagation delays would be approximately proportional to $l/2^{2m/3}$. This is an important topic for further research that can combine the proposed techniques presented in this work with new advances and current research in three dimensional microcircuit devices.

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Figure 1. Schematic of multi-decoder PLA

Figure 2. Two decoder ROM implementation (A) and Two decoder PLA implementation (B)
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