

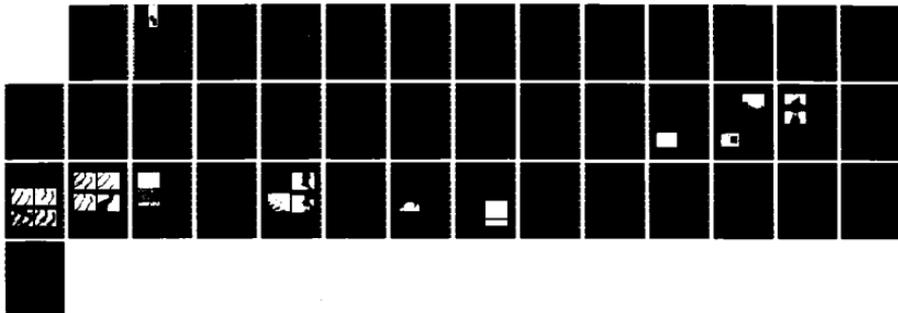
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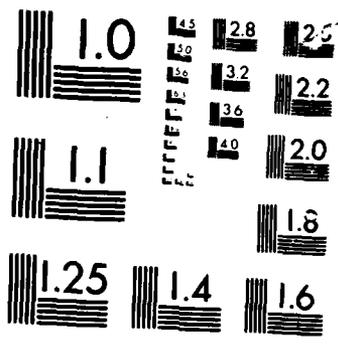
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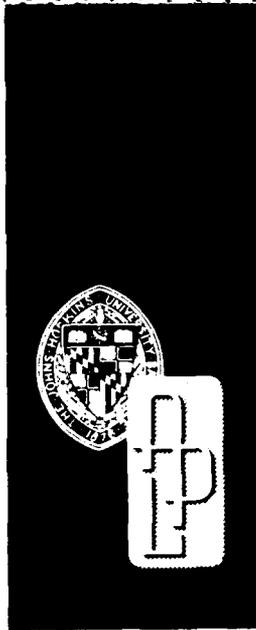


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Technical Memorandum

1984 IR&D ADVANCED PACKAGING STUDY

G. V. CLATTERBAUGH
H. C. CHARLES, JR.

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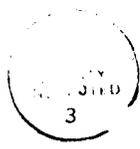
G. V. CLATTERBAUGH
H. C. CHARLES, JR.

THE JOHNS HOPKINS UNIVERSITY ■ APPLIED PHYSICS LABORATORY
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ABSTRACT

An advanced multiyear electronics packaging project has been started under the auspices of The Johns Hopkins University Applied Physics Laboratory's Independent Research and Development. The project is a comprehensive interactive one involving theory, modeling, structure fabrication, and reliability testing. Highlights of the first year's activities are presented in this report. Important results include: the creation of integrated thermal and thermomechanical models, the prediction of lifetimes under environmental and operational stress conditions, model verification and validation by carefully controlled experimentation, development of assembly techniques, and the invention of a new method for preparing controlled solder joint height and geometry.



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1.0 INTRODUCTION

The trend in microelectronics since its inception has been to extend the applications of electronic devices into areas where stringent requirements on size, density, speed, and complexity have forced the need to develop innovative concepts in microminiaturization. With the advent of very-large-scale integrated (VLSI) circuits and very-high-speed integrated circuits (VHSIC), electronics packaging engineers are faced with the task of designing packages that can accommodate increased power dissipation, number of pinouts, and circuit densities while at the same time reducing weight, package dimensions, and production costs. Thick film multilayer ceramic substrates and surface-mounted components such as ceramic chip resistors, capacitors, and leadless ceramic chip carrier (LCCC) packages have all been responsible for reducing density, weight, package dimensions, and production costs while increasing circuit densities. Large chip carriers that can accommodate the high input/output requirements of VLSI devices (with as many as 84 to 232 leads) are presently commercially available. The thermal management and determination of thermal-stress-related effects, the choice of interconnection materials and attachment techniques, and the assessment of overall system reliability for the surface-mounted circuit assembly remain as problems for the electronics packaging engineer to solve.

The problems most often encountered by the electronics packaging designer when faced with integrating all of the aspects of a complex circuit using VLSI custom-integrated circuits into a final design are

1. Control of complex circuit parameters such as capacitance and inductance for package and substrate leads,
2. Prediction of thermal profiles at critical locations where out-of-specification temperatures may result in reduced reliability for sensitive devices,
3. Estimation of thermal stress effects that may lead to accelerated failures at critical device interconnections,
4. Prevention of excess intermetallic formation at interconnections caused by thermally enhanced diffusion processes,
5. Proper material selection for optimum thermal, mechanical, and electrical performance,
6. Determination of overall system reliability in a known operating environment,
7. Process control during fabrication to ensure

consistent quality from one circuit assembly to another,

8. Determination of the applicability of various accelerated testing procedures to aid in making accurate reliability assessments.

In many applications, commercially available packaging and standard electronics assembly processing techniques may satisfy all the criteria for a reliable system. However, for those situations where nontypical operational and environmental conditions may require modifications to preexisting packaging concepts or where an innovative approach to hybrid design and fabrication may be required, the electronics packaging engineer must be able to model and test new design and fabrication concepts to ensure that all dimensional, operational, and reliability requirements are satisfied. To avoid numerous and costly redesigns, all of the necessary system performance and reliability assessments should be determined early in the design stage. Unfortunately, because of rapid advances in integrated circuit technology, complete information concerning the reliability of recent packaging processes, new materials and processing techniques, and state-of-the-art design rules for the economical use of advanced VLSI devices are often not available.

The methods and tools to assist the electronics packaging engineer in designing and evaluating system performance should include computer-aided design and performance simulation capabilities from thermal, mechanical, and electrical standpoints, as well as the experimental capability to monitor electrical performance and temperature and the mechanical capability to test for reliability and materials characterization. So essential are these tools, test methodologies, and characterization techniques to the successful integration of VLSI/VHSIC devices and packages into current and future prototype electronic systems produced at APL, that a multiyear IR&D effort in Advanced Packaging has been started. The results of the first year's activity (1984) are summarized in this report. The topics addressed include

1. Thermal analysis of VLSI packages and hybrid microcircuit assemblies,
2. Thermomechanical stress and low cycle fatigue in soft-soldered interconnections,
3. Accelerated testing of soft-soldered interconnections for surface-mounted components,
4. Special techniques for surface-mounting soldering applications,

5. Theoretical and experimental reliability assessments of LCCC in temperature-cycled and power-cycled environments,
6. Critical assessment of the finite-element method (FEM) for thermal and thermomechanical analysis of miniaturized electronic assemblies.

2.0 THERMAL ANALYSIS OF SURFACE-MOUNTED COMPONENTS AND ELECTRONIC ASSEMBLIES

2.1 OVERVIEW

The area of thermal design and analysis of circuit assemblies is one of the most dynamic in investigative activity in the electronics industry. Thermal design represents a critical preproduction step necessary to ensure adequate thermal management prior to actual fabrication. In situations that involve conductive and radiative cooling, numerical techniques are available to obtain approximate solutions to both transient and steady-state heat-transfer problems. Situations involving more complex heat-transfer mechanisms such as forced convection cooling can often be simulated numerically by experimentally obtained heat-transfer correlations that are available in the literature.^{1,2} In some cases, experimental simulation of forced and natural convective environments may be required for correlating dimensionless heat-transfer relations for geometrical and material parameters specific to the actual electronic circuit package.

The FEM technique was chosen for the thermal analysis done in this study primarily because it is relatively easy to implement and both a preprocessor and a postprocessor are available for the construction, automatic data generation, and subsequent analysis of complex thermal models. The MSC NASTRAN finite element code³ was chosen because of its on-site availability and its proven ability to obtain reliable approximate solutions both to thermal and to thermal-stress problems.

The thermal analysis of a complex microcircuit assembly using the FEM technique is most economically done by dividing the overall problem into several smaller ones. An attempt to construct a model that incorporates an entire complex microcircuit consisting of many components would require the use of vast amounts of computer memory. Accurate models of individual components alone can result in reasonably priced computer simulations. On the other hand, attempts to oversimplify the model can result in an unacceptable compromise in accuracy. Reducing surface-mounted components and packages into equivalent lumped heat-transfer elements through individual, detailed FEM models is a useful approach to transform large complex circuit boards into relatively simple thermal networks.

The first step in the procedure requires the numerical estimation of the lumped thermal circuit parameters (i.e., thermal resistances and heat capacitances) for individual circuit board components. This is accomplished by dividing the component or package into finite elements and specifying the boundary conditions (i.e., the temperature and heat gradients). Passive elements (such as capacitors) can often be assigned thermal heat capacitance values (i.e., mass \times heat capacity), and hand-calculated thermal resistance estimates are usually sufficient. Components or packages that involve internal heat dissipation or active device heat generation usually require sufficient detail in the thermal model to reflect the large thermal gradients present. In the past, detailed temperature models were required only for die packages, since temperature estimates at the device junctions were of primary concern. However, for surface-mounted applications where significant thermal stress at soldered joints may occur, more complete temperature information will be required to accurately assess interconnection reli-

¹W. M. Rosenow, J. P. Hartnett, and E. N. Ganic, *Handbook of Heat Transfer Fundamentals*, McGraw-Hill, New York (1985).

²Y. Jaluria, *Natural Convection: Heat and Mass Transfer*, Pergamon Press, New York (1980).

³W. J. Anderson, *Finite Elements in Mechanical and Structural Design*, Macneal-Schwendler Corp., Los Angeles (1984).

ability for all soldered components. All linearized conductive and convective heat-transfer mechanisms can be included at the component level of the analysis. The resulting estimates for the component thermal resistance to be used in the lumped element formulation during the final stage of the analysis will reflect the influence of heat-transfer mechanisms used previously to estimate lumped circuit parameters.

After the individual components and packages have been replaced by a lumped thermal circuit element, the substrate can then be divided into finite elements, each bounded by node points to which the previously estimated lumped component and package elements are thermally connected. The philosophy behind a thermal analysis of a typical hybrid circuit such as a surface-mounted thick film microcircuit with surface mounted components is shown schematically in Fig. 1. In this particular situation, the temperature of interest is that of the junction of the active device, as shown in the figure. The total thermal resistance from chip to ambient consists of the sum of the thermal resistance values for each separate resistor element along the heat path between the source and the sink. Each of these values can be estimated using FEM techniques. They can be dependent on complex loss mechanisms such as convection (natural or forced air convection) and radiation. Radiative and convective effects tend to be nonlinear by nature and thus require iterative solution techniques that tend to dramatically affect computer costs. In many practical instances, some or all of these effects may be small enough to be neglected and thus reduce unnecessarily high computer expenditures.

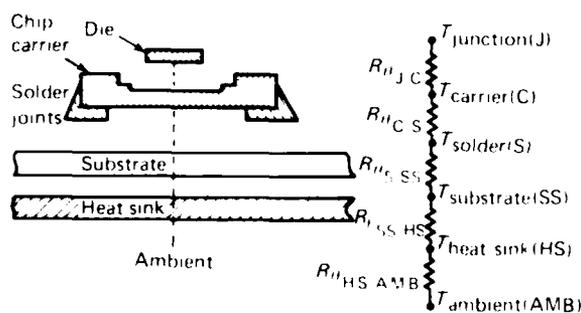


Figure 1. Typical thermal resistance (R_{th}) path from junction to temperature ambient for surface-mounted hybrid assembly.

2.2 FEM REPRESENTATION—LEADLESS CHIP CARRIER

The analysis of a particular component of interest begins with the geometrical construction of a model by dividing the component into a 1-, 2-, or 3-dimensional mesh containing grid points or nodes. The grid points serve as the demarcation for the finite element that occupies the space bounded by a particular subset of grid points. An example of an FEM model of a 68-pin leadless chip carrier is shown in Fig. 2. In this figure, only 1/8 of the actual part is divided into finite elements. It is assumed that the die is square and resides symmetrically in the center of the carrier; thus eightfold symmetry in the chip carrier plane can be exploited. Three-dimensional rectangular and wedge shaped solid elements are used in the model. Most FEM codes also provide 2-dimensional surface elements (not shown here) to account for surface heat conduction and radiative effects at the external boundaries of the component. The substrate is included in this calculation to allow for radiation and convective cooling from the bottom of the substrate.

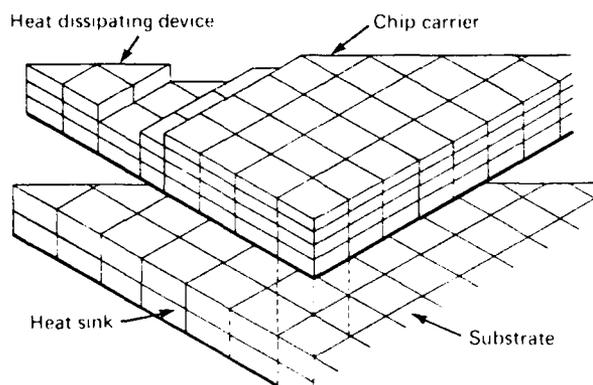


Figure 2. Finite-element thermal analysis model for LCCC.

Another important reason for including the substrate in the thermal resistance calculation in the vicinity of the chip carrier is illustrated by Fig. 3a. In this figure, we have a situation where the chip carrier footprint does not correspond to the symmetrical grid pattern that was chosen to represent the substrate. In order to treat the chip carrier as a lumped element, a precise method for thermally connecting the component to the substrate (i.e., to a grid point or set of grid points on the substrate) must be determined. Distributing the thermal load via a thermal resistor requires a knowledge of the thermal resistance between

the device and a particular location (i.e., the grid point location[s]) on the substrate. The connection of a chip carrier to the underlying substrate via thermal resistors is shown in Fig. 3b. Most finite-element codes with a thermal analysis capability contain thermal elements that are the electrical analogy of a resistor. With these elements and the estimation of the thermal resistance from chip to specific substrate grid point locations, the final lumped element model is complete. The model may include the entire circuit board or only a portion of it depending on the size and complexity of the entire circuit. Attached heat sinks may also be included

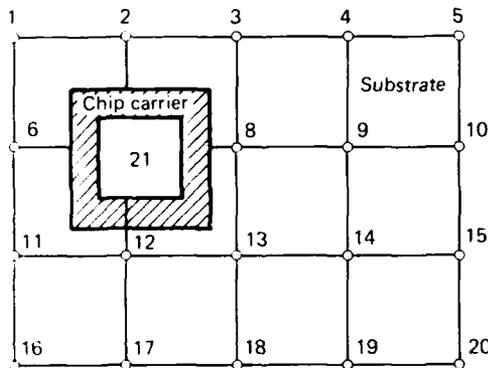


Fig. 3a Asymmetric chip carrier position with respect to arbitrarily chosen grid pattern for underlying substrate.

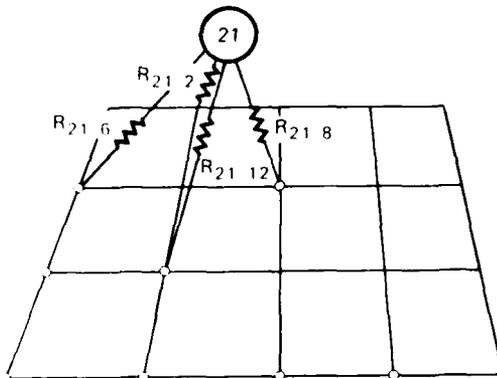


Fig. 3b Junction temperature for die mounted in chip carrier package reduced to a simple grid point through the use of thermal resistors. Grid point 21 serves as a point source for power dissipation while resistors distribute power to various grid point locations.

Figure 3. Schematic representation of the procedure for distributing power from a component generating heat to the underlying substrate via thermal resistors.

at this point in the analysis, as shown in Fig. 4. If the heat sink is in thermal equilibrium with the environment (i.e., the temperature of the heat sink is approximately equal for power-on and power-off conditions), the analysis is complete. If this is not the case, the analysis is extended in a completely analogous fashion to the electronic circuit housing or perhaps to a larger heat sink. In the case of a satellite, for example, this ultimate heat sink would be the surrounding space environment.

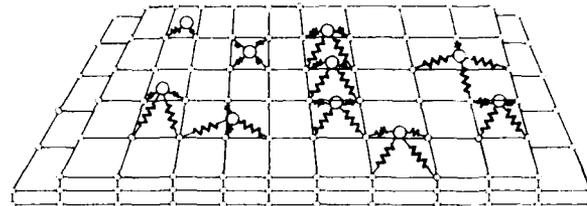


Figure 4. Thermal analysis model for a 10-component surface-mounted hybrid assembly with heat sink.

The procedure discussed in this section for performing thermal analysis on surface-mounted hybrid assemblies can be facilitated in future analyses by retaining FEM models of commonly used components and the information obtained in previous studies. The lumped thermal resistance and capacitance values for many of the standard packages and components will often remain relatively constant for similar applications. The availability of these data can reduce significantly the number of computations required to perform subsequent thermal analysis calculations.

2.3 THERMAL ANALYSIS—CHIP CARRIER SOLDER JOINTS

An example of a thermal analysis using FEM is the investigation of the effect of solder joint geometry and solder material on the thermal resistance of leadless chip carrier interconnections. The analysis was performed to

1. Determine whether solder joint geometry had any significant effect on the net thermal resistance,
2. Estimate the impact of a thermal resistance increase on the differential thermal expansion between chip carrier and substrate,
3. Determine whether higher thermal conductivity solders would significantly reduce net package thermal resistance.

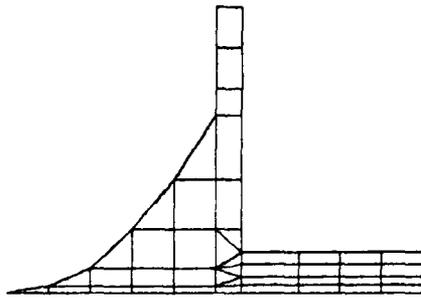


Figure 5. Finite-element model to estimate thermal resistance of a chip carrier solder joint.

A finite-element model for a solder joint is shown in Fig. 5. Thermal conductivities for eutectic tin-lead solder (63% Sn, 37% Pb by weight) and Sn62 solder (62% Sn, 36% Pb, 2% Ag by weight) were used in the analysis. Finite-element models and thermal resistance estimates for the four solder joint geometries considered in this study are given in Fig. 6.

Results of the analysis were used in a subsequent thermal analysis of a 68-pin chip carrier. The results showed that, for the solder joint geometry with the highest estimated net thermal resistance (9.41°C/W per joint for a 10-mil standoff height and Sn62 alloy), the portion of the total thermal resistance of the chip carrier due to the solder joints was less than 2% of the total. This indicates that the effect of solder geometry, standoff, and solder alloy are relatively insignificant for most chip carrier applications. As the number of pinouts decreases, however, the effect of the solder bond becomes a more significant contribution to the total thermal resistance. Thermal stress analyses indicate that the effect of increasing the standoff height for a 52-pin chip carrier from 10 mils to 20 mils would result in an increase in the differential thermal expansion of the chip carrier by approximately 6%. However, because of the increase in standoff height, the shear strain reduction for this case would be a net improvement of 200% (assuming idealized cylindrical joints). Thus, the small increase in differential thermal expansion should be more than offset by

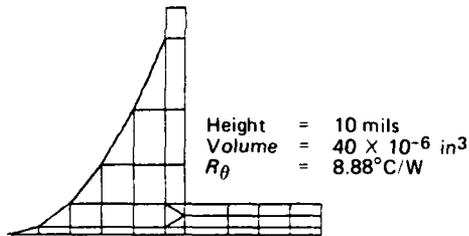
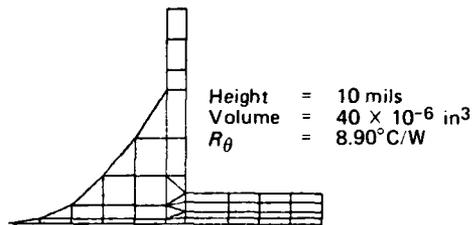
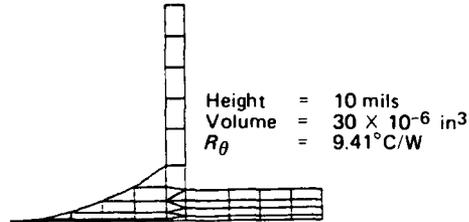
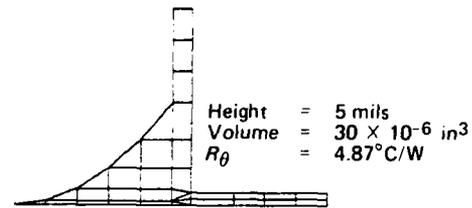


Figure 6. Results from FEM thermal analysis to estimate thermal resistance (R_{θ}) for several LCCC solder joint geometries.

the reductions in the solder joint shear strain. The end result of this study indicates that material selection and solder joint design considerations should be based primarily on their mechanical and fatigue properties and not on their heat-transfer characteristics.

3.0 THERMOMECHANICAL BEHAVIOR – SOFT-SOLDERED INTERCONNECTIONS

3.1 OVERVIEW

The surface mount approach to hybrid circuit design and manufacturing has been shown to be of primary importance owing to the relative ease of implementation, the rework capability, the component versatility, and the efficient use of valuable substrate real estate. Surface mounting in conjunction with multilayer thick-film technology can result in significant increases in circuit densities. Substrate materials commonly used for thick-film multilayer circuit applications, such as alumina and beryllia, possess enhanced heat-transfer characteristics required for future VLSI applications. In addition, the turnaround time and the ability to rework circuits quickly and inexpensively provide further incentives for adopting this technology. Although surface-mounting technology is not new, the reliability problems associated with the use of soft solders for component and package interconnections are not fully understood. To answer some of the most frequently asked questions concerning the reliability of these interconnections, much of the remainder of this report will focus on some of the thermal and mechanical problems associated with the use of soft solders with leadless chip carrier packages and the methods available to the electronics packaging engineer to predict the useful service life of such solder.

3.2 THEORY—HIGH-TEMPERATURE LOW-CYCLE FATIGUE IN SOFT-SOLDERED JOINTS

Most soft solders are low work-hardening materials that exhibit nonlinear viscoelastic behavior at typical operating temperatures. They are usually quite ductile, display a tendency to creep at very low strain rates, and exhibit minor amounts of work-hardening at higher strain rates. Mechanical properties vary widely with respect to temperature,⁴ strain rate,⁵ and grain size.⁶ Because they have relatively low melting tem-

peratures compared to many typical alloys, soft solders exhibit fatigue and fracture properties similar to many systems operating at elevated temperatures. For example, the mechanical properties of tin-lead solders at very low temperatures are similar to the room temperature properties for common, higher melting temperature alloys such as steel, nickel, etc. It is for this reason that many of the empirical results for high-temperature-low-cycle fatigue can be applied to soft solder alloys operating near room temperature.

Low-cycle fatigue in surface-mounted soldered interconnections has been observed primarily during temperature or power cycle testing when there is a large temperature coefficient of expansion (TCE) mismatch between the chip carrier and the substrate. More recently, the effect of strains induced by differential thermal expansion resulting from power cycling for matched TCE chip carrier and substrate materials has led to speculation concerning the reliability of solder interconnections.⁷ To date, however, there has been little evidence from either actual or simulated operational environmental power cycle testing⁸⁻¹¹ to support such concerns. However, solder joints subject to sufficiently large mechanical strains resulting from either temperature or power cycled environments will ultimately fail due to high-temperature-low-cycle fatigue. These failures can occur in the solder itself or in or near the usually brittle intermetallic bond interface region. The mechanical strains may result from the transient and steady-state thermal gradients that exist between an LCCC and the substrate, as in the case of power cycling, or from the large differential

⁷W. Engelmaier, "Functional Cycles and Surface Mounting Attachment Reliability," *Surface Mount Technology*, International Society for Hybrid Microelectronics (1984).

⁸I. M. Montante and D. R. Kling, "High Reliability Attachment of Multilayer Chip Carriers to Ceramic Substrates for the Class S Environment," *IEEE Proc. 1984 Electronics Components Conference*, pp. 129-137 (1984).

⁹D. L. Hallowell and D. W. Kellerman, "Analysis of a Stacked Thick Film Package," *Proc. 1984 Microelectronics Symposium of the International Society of Hybrid Microelectronics*, pp. 281-292 (1984).

¹⁰H. Danielsson, "Chip Carrier on Ceramic Thick Film Multilayer Boards in High Reliability Applications," *Proc. 1984 Microelectronics Symposium of the International Society of Hybrid Microelectronics*, pp. 56-60.

¹¹D. E. Reimer and C. W. Saulsberry, "Power Cycling of Ceramic Chip Carriers on Ceramic Substrates," *Proc. 1984 Microelectronics Symposium of the International Society of Hybrid Microelectronics*, pp. 480-485.

⁴*Development of Highly Reliable Soldered Joints for Printed Circuit Boards*, Westinghouse Report No. N69-25697 (1968).

⁵K. R. Stone et. al., "Mechanical Properties of Solders and Soldered Joints," *Brazing and Soldering* 4, Spring (1983).

⁶J. W. Aldrich and D. H. Avery, "Alternating Strain Behavior of a Super Plastic Metal," *Ultrafine Grain Metals, Proc. 16th Sagamore Army Materials Research Conference, Aug. 1969*, Syracuse University Press, pp. 397-416 (1970).

thermal expansion experienced during temperature cycling between the ceramic chip carrier and substrate and the high TCE solder.

During temperature and power cycling dwell periods, creep and other temperature-dependent relaxation phenomena can occur, decreasing the amount of recoverable strain per cycle depending on both the dwell time and temperature. Simultaneously, cyclic softening can occur,^{12,13} resulting in a lowering of the stress required on each succeeding cycle to produce a given amount of strain or, equivalently, causing a progressive decrease in the elastic strain.

In addition to these processes, temperature and stress-induced diffusion and intermetallic formation occur at the bond interface. In situations where bonding pads contain sufficient quantities of gold, tin diffusion into the pad metallization can result in the formation of a weak Au-Sn intermetallic interface that produces a bond that may be incapable of withstanding additional thermal cycling. Even in cases where stronger solder-to-metal interfaces are formed, tin migration can leave a lead-rich solder with reduced fatigue and creep properties.^{9,14} Oxygen embrittlement,¹⁵ observed in many fatigue specimens at elevated temperature, can greatly enhance crack propagation by oxidizing cracks and grain boundaries while in tension and preventing partial rewelding while in compression. One experimenter investigating the low-cycle fatigue properties of high-lead-content solders used for die attach¹⁶ reported that crack initiation was rapid (300 cycles) for samples cycled in air and retarded (no cracking after 3000 cycles) for identical samples cycled in vacuum.

High-temperature-low-cycle fatigue includes all of these effects: pure fatigue, creep, stress relaxation, recovery, thermally aided diffusion processes, and corrosion. The ultimate number of cycles that the soldered interconnection can endure will be a function of all of these competing mechanisms in varying degrees. The complex interaction between these competing failure mechanisms in soft-soldered interconnections is

¹²R. W. Rhode and J. C. Swearingen, "Deformation Modeling Applied To Stress Relaxation of Four Solder Alloys," *J. Eng. Mater. Technol.* **102**, pp. 207-214 (1980).

¹³C. A. Nuegebauer et. al., "The Measurement of Fatigue Suppression in Electronic Solder Joints," *8th Annual Soldering Technology Seminar*, Naval Weapons Center, China Lake, CA (Feb. 1984).

¹⁴E. Baker, "Stress Relaxation in Tin-Lead Solders," *Mater. Sci. Eng.* **38**, 241-247 (1979).

¹⁵M. Gell and G. R. Leverant, "Mechanisms of High Temperature Fatigue," *Fatigue at Elevated Temperatures*, ASTM STP 520, American Society for Testing and Materials, pp. 37-69 (1973).

¹⁶C. A. Nuegebauer, private communications.

not clearly understood. However, in order to predict useful service life, it will be necessary to identify which mechanisms predominate under given sets of operating or test conditions.

3.3 PREDICTING FATIGUE LIFE— THE COFFIN-MANSON EQUATION

When metals experience low-cycle fatigue due to reversed plastic flow, the number of cycles to failure (N_f) is often found to follow the empirical relationship¹⁷

$$\Delta\epsilon_p = CN_f^\beta, \quad (1)$$

where

$\Delta\epsilon_p$ = plastic strain range,
 N = number of cycles to failure,
 C, β = constants to be determined from nonlinear regression of experimental data.

For situations where elastic effects are important ($N_f > 1000$), N_f is related to the total strain through the empirical relation

$$\Delta\epsilon_T = CN_f^\beta + \frac{AC^n}{E} N_f^{\beta n'}, \quad (2)$$

where

$\Delta\epsilon_T$ = total strain range,
 E = Young's modulus,
 n', C, β, A = experimental constants.

The first term in this equation is simply the Coffin-Manson equation while the second relation, accounting for elastic fatigue damage, is known as the Basquin equation.¹⁷ The coefficient C in this equation is sometimes referred to as the fatigue ductility coefficient; at low temperature for most metals, $C = D^{0.6}$ where D is the true fracture strain. β is referred to as the fatigue ductility exponent and is usually found in the range of 0.4 to 0.8 for most metals. At low temperatures, the fatigue ductility exponent usually assumes the value of $\beta = 0.6$. The constant A at low temperatures can often be expressed by the relation $A = 3.5(\sigma_u)/D^{0.12}$ where σ_u is the ultimate tensile

¹⁷L. F. Coffin, "Fatigue At High Temperature," *Fatigue at Elevated Temperatures*, ASTM STP 520, American Society for Testing and Materials, pp. 5-34 (1973).

strength. The constant n' , the cyclic hardening exponent, decreases rapidly with increasing temperature as does the constant A .

3.3.1 Transition Fatigue Life

The transition fatigue life¹⁷ can be defined as the point where N_f for plastic effects is equal to N_f for elastic effects. This can be obtained from Eq. 2 by equating the first and second terms.

$$N_t = \left(\frac{ACn'-1}{E} \right)^{1/\beta(1-n')} \quad (3)$$

The transition fatigue life can be useful in determining the type of test or analysis that should be prescribed to estimate the service life. For example, if the design life is much less than N_t , low-cycle fatigue test procedures are required for material evaluation. If the design life is approximately equal to N_t , elastoplastic solutions are required. If the design life is much greater than N_t , elastic analysis will suffice.

3.3.2 Modified Coffin-Manson Equations

High-temperature effects such as creep and corrosion can be accounted for by modifying Eq. 1 to include frequency effects;¹⁷ this is given by

$$\Delta\epsilon_p = C(N_f\nu^{k-1})^\beta, \quad (4)$$

where

- ν = cycle frequency,
- k = experimental constant.

Williams¹⁸ developed a similar relationship based on a creep model for wedge crack growth at triple points where the controlling mechanism is grain boundary sliding. Grain boundary sliding is believed to be the dominant rate controlling mechanism in solders at temperatures in the approximate range of 0°C to 50°C.⁶ The functional relationship between N_f and plastic strain for this creep model possesses the same form as Eq. 4. This model assumed positive symmetrical stress cycles with no hold period, and, thus, frequency is dependent only on the time for stress loading and unloading. The model used for the derivation of this equation will permit the inclusion of dwell periods and nonsymmetric load and unload cycles, given that such effects as stress relaxation and

loading rates can be made quantitative. This equation can also be modified somewhat by the inclusion of an Arrhenius factor that expresses the effect of temperature on the rate of grain boundary sliding. This result is

$$N_f^\beta \nu^\alpha \epsilon_c \exp(-Eact/kT) = \text{constant}, \quad (5)$$

where

- ϵ_c = creep strain per cycle,
- k = Boltzman constant,
- T = temperature,
- $\beta, \alpha, C, Eact$ = experimental constants.

Norris and Landzberg¹⁹ used Eq. 5 to estimate the reliability of Pb95-Sn5-soldered interconnections undergoing thermal fatigue. They considered the frequency exponent to be an empirical factor that accounts for such time-dependent effects as strain rate, relaxation, etc. Later modifications have included an Arrhenius degradation factor to account for intangibles such as additional intermetallic formation and corrosion. This result is given by

$$N_f = C\nu^\alpha \Delta\gamma^{-2.0} \exp\left(\frac{-Eact}{kT}\right), \quad (6)$$

where

- $\Delta\gamma$ = shear strain range.

Engelmaier²⁰ derived a thermal fatigue model for eutectic tin-lead solder joints based on the frequency independent Coffin-Manson equation of the form

$$N_f = \frac{1}{2} \left[\frac{F\Delta\gamma}{2\epsilon'_f} \right]^{1/\beta}, \quad (7)$$

where

- ϵ'_f = fatigue ductility coefficient,
- β = fatigue ductility exponent,
- F = empirical factor.

He concluded from solder fatigue data from

¹⁸J. A. Williams, "Derivation of a Failure Law for Creep Under Cyclic Stress," *Fatigue at Elevated Temperatures*, ASTM STP 520, American Society for Testing and Materials, pp. 149-156 (1973).

¹⁹K. C. Norris and A. H. Landzberg, "Reliability of Controlled Collapse Interconnections," *IBM J. Res. Dev.*, 13.

²⁰W. Engelmaier, "Effects of Power Cycling on Leadless Chip Carrier Mounting Reliability and Technology," *Electronic Packaging Prod.*, pp.58-63 (April 1983).

Wild²¹ that a reasonable correlation of his model to these data could be found if the fatigue ductility exponent could be represented by the equation

$$\beta = -0.442 - 6 \times 10^{-4} T_c + 1.74 \times 10^{-2} \ln(1 + \nu), \quad (8)$$

where

T_c = mean cyclic solder joint temperature in °C,

ν = cyclic frequency, cycles/day,

and the fatigue ductility coefficient was given by

$$2\epsilon_f \approx 0.65.$$

The formulation assumes that there are cylindrical solder joints with no stress concentrations in the solder or at the bond interface and that the applied stress is primarily shear stress. It also excludes any second-order effects that may result in significant tensile or compressive strains. Included in the formulation is an empirical factor that takes into account variations in the physical and processing parameters that may affect joint reliability.

Clearly in cases where failure results from thermally enhanced diffusion processes, equations based on experimentally obtained isothermal fatigue data for solder would result in gross inaccuracies in reliability estimates of service life. In cases where diffusion kinetics represent the dominant rate controlling mechanisms for solder joint failures, solder fatigue relations should probably be abandoned in favor of the rate equations of the Arrhenius type. The Coffin-Manson formulation used a model representing crack propagation along slip planes. When modified for high temperature, the equation was found to be identical in form to a creep relation based on a triple point cracking model. In situations where the modified Coffin-Manson relations are valid, experimental determination of actual shear strains may be impractical if not impossible for most realistic situations. Simple flat plate (average temperature) models used in the literature to represent a powered LCCC can be shown to grossly overestimate actual shear strains. In addition, how does one determine, a priori, how significant stress concentration factors are in influencing the ultimate duty life? One approach to this problem is to

formulate numerical computer solutions that can provide some of the data not readily accessible by experimental methods. The versatility of the FEM for solving complex thermomechanical stress problems of the type encountered in soldered interconnections provides an alternative approach for obtaining critical strain data, in addition to providing a wealth of qualitative information.

3.4 FEM ANALYSIS OF CHIP CARRIER AND CERAMIC SUBSTRATE ASSEMBLIES

3.4.1 FEM Analysis of Differential Thermal Expansion for Power-Cycled LCCCs on Ceramic Substrates

Several authors^{7,19,22} have proposed solder joint fatigue models that require a knowledge of the differential thermal expansions between the substrate and the soldered components. In the case of temperature cycling, this differential expansion difference can be estimated quite simply by the relation

$$\Delta L = L/\sqrt{2} \times \Delta\alpha \times \Delta T, \quad (9)$$

where

L = length of the chip carrier,

$\Delta\alpha$ = differential coefficient of thermal expansion,

ΔT = temperature excursion.

In the case of power cycling, no such analytical result exists for typical chip carrier geometries. Finite-element thermal analysis of chip carrier assemblies indicates that, for most of the larger carriers, sizable thermal gradients can exist between the operating device and the cooler, heavier frame surrounding the die cavity. This cool heavy frame acts to constrain the thermal expansion, thereby reducing the stress at the solder joints at the cost of increasing the strain within the ceramic chip carrier itself. Estimates that call for the chip carrier displacement to be given by Eq. 9 can result in large discrepancies from the actual displacements. Thermomechanical analysis using finite-element techniques can provide an alternate, more practical method to estimate differential thermal displacements for power-cycled chip carrier assemblies. This analysis requires two steps:

1. A thermal analysis to determine temperatures

²¹R. N. Wild, *Some Fatigue Properties of Solders and Solder Joints*, IBM Technological Report 73Z00421 (1973).

²²J. R. Taylor and D. J. Pedder, "Joint Strength and Thermal Fatigue in Chip Carrier Assembly," *Int. J. Hybrid Microelectron.* 5 (1982).

over the entire domain of the problem (carrier and substrate),

2. The use of these values as temperature loads for a thermal stress analysis.

The FEM model used to estimate the differential thermal expansion for a power-cycled 68-pin chip carrier is similar to that shown in Fig. 2 and includes all of the features of the experimental set-up as discussed in Section 4.2 (see Fig. 18). A linear thermal analysis neglecting natural convection and radiation effects was used in this study. The validity of these approximations was verified through independent temperature measurements. Also, for the thermal analysis portion, individual solder joints were modeled as convective surface elements, conducting heat from their respective solder pads located on the carrier to the corresponding substrate bonding pads. Heat-transfer coefficients were derived from previously calculated thermal resistance values for various solder joint geometries. This approach is economical in reducing the number of solid elements required for the analysis and provides better estimates for cases where an insufficient number of solder elements are used.

The results from the analysis were then used to predict service life for experimental samples based on Engelmaier's modified version of the Coffin-Manson equation for predicting solder joint fatigue life. In a first estimate of the maximum shear strains that will occur, it is assumed that complete solder relaxation can occur during the dwell period of a power cycle. Also, it is assumed (as was the case in the experiments performed in this study) that the total strain does not decrease after the transient heat-up period due to the presence of an isothermal heatsink as depicted in Fig. 7. This last assumption guarantees that the temperature is a monotonically increasing function with time and that the maximum shear strain is reached during steady-state operating conditions. A more costly, step-wise quasistatic incremental procedure for determin-

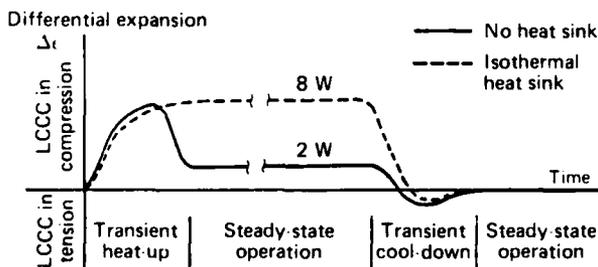


Figure 7. Effect of isothermal heat sink on the differential thermal expansion for power-cycled LCCC and ceramic substrate.

ing the peak transient shear strain would otherwise be required. The assumed values for Young's modulus, Poisson's ratio, and the TCE for both the ceramic chip carrier and the substrate were 4.1×10^{11} psi, 0.21, and 6.7×10^{-6} ppm, respectively.

Maximum displacements for a 68-pin chip carrier were calculated to be $2.8 \mu\text{m}$ for a 10 W power dissipation from a 0.76 cm^2 chip. Assuming cylindrical joint geometries and no stress concentrations, this would result in shear strains on the order of 5 to 6% for solder joints with standoff heights approximately 2 mils and about 1% or less for standoffs 10 mils or higher. Fatigue life for soft solders will generally surpass 1000 cycles if plastic strains are maintained under 1%. For 52-pin chip carriers dissipating the same 10 W of power, maximum displacements were found to be $2.0 \mu\text{m}$ for an identical size heat source. Estimated maximum chip temperatures for a heat sink at 28°C were 203°C and 182°C , for the 68- and 52-pin chip carrier models, respectively.

More detailed models analyzed included the rigidity introduced by the solder joints. Results from these studies indicated that, neglecting relaxation effects, actual in-plane shear strains are approximately half of those values obtained for the complete solder relaxation assumption. Figure 8 illustrates two solder joint models used in this calculation for the case of 10 W power cycling for both rectangular pillar style and extended fillet solder joint geometries (5 mil standoff). Stress contours with numbers ≤ 2 indicate regions

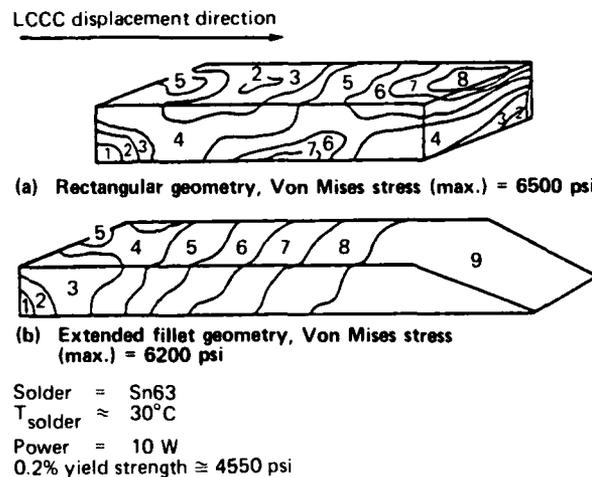


Figure 8. Stress contours for power-cycled solder joints (10-W power). Contours with numbers less than or equal to 2 indicate regions where the Von Mises stress is greater than 0.1% yield stress.

where the Von Mises stress is greater than the 0.2% yield strength. According to the Von Mises criterion, plastic flow should occur when the Von Mises stress exceeds the 0.2% yield strength of the material. For the case where the joint has no fillet, regions of high strain, although localized, can be estimated to occur in several locations. The presence of the solder fillet results in a significant reduction in these localized high strain density regions and should assist in extending the fatigue life of the interconnection.

The analysis also points out the fact that the numerically estimated magnitude of the differential thermal expansion does not differ by more than 1% for all pin locations. This differs from the thermal cycling case where the in-plane shear strains for the corner joints can be as much as 1.4 times that for the center pin location.

In Fig. 9, the effects of solder joint geometry on chip carrier displacement are illustrated. The displacements are exaggerated to show the effects of warpage due to joint type. The displacements were calculated assuming that the substrate was sufficiently stiff to resist bending. In most actual situations, this bending behavior will be shared between the chip carrier and the substrate. Warping can influence the direction of stress in critical locations, causing stress concentrations that can result in additional plastic flow.

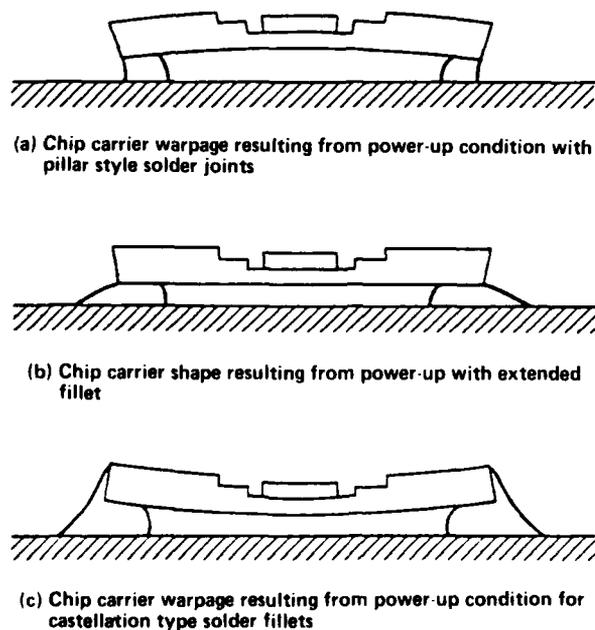


Figure 9. Effect of solder joint geometry on LCCC bending behavior during power cycling.

For example, additional tensile strains introduced through substrate warpage can increase the rate of crack propagation through the solder joints. In addition, such warping can exert significant stress on the device or on the device interconnection. Thermal analysis calculations performed in this study indicate that, for a two-dimensional chip carrier model, the thermal resistance is a minimum for a cavity thickness equal to the horizontal distance between the heat source and the chip carrier solder pads when the primary heat transfer is through the soldered leads. This condition would be approximately maintained for the 68-pin chip carrier with a 0.325-inch ceramic thickness from die cavity to bottom. This result indicates that, for larger chip carriers, increasing the cavity thickness to approximately $\frac{1}{4}$ to $\frac{1}{3}$ the chip carrier length will reduce the overall thermal resistance while providing an even more rigid structure to resist warpage.

Also, additional analysis indicated the effect of substrate and component stiffness on stress concentrations in solder joints. In Fig. 10, the areas of stress concentration for solder joints under various bending conditions are shown. Analysis indicates that the ratio of bending stiffness between soldered component and substrate can significantly influence stress concentration factors. Our studies also suggest the importance of tailoring the solder joint shape to reduce stress concentrations introduced by differences in the component and substrate rigidity. The results also indicate the importance of choosing representative substrates and components when simulating operating conditions for accelerated testing.

3.4.2 FEM Stress Analysis—Temperature-Cycled Solder Joints

Bond interfaces for temperature-cycled solder joints on ceramic substrates can experience large strains due to the large difference between the TCEs for solder and for ceramic. Large strains in chip carrier solder joints have been observed to cause thick film pad delamination²³ from the underlying dielectric material during extreme temperature cycling tests. This differential thermal expansion can also induce additional strains during power cycling environments in cases where power-on temperatures vary significantly from power-off temperatures. The analysis here attempts to evaluate the effect of solder joint design parameters on bond interface stresses occurring in temperature-cycled environments.

²³D. F. Reimer and J. D. Russell, "The Optimized Solder Bond For Ceramic Chip Carriers On Ceramic Boards," 1983 Proc. International Society for Hybrid Microelectronics, ISHM, pp. 217-222 (1983).

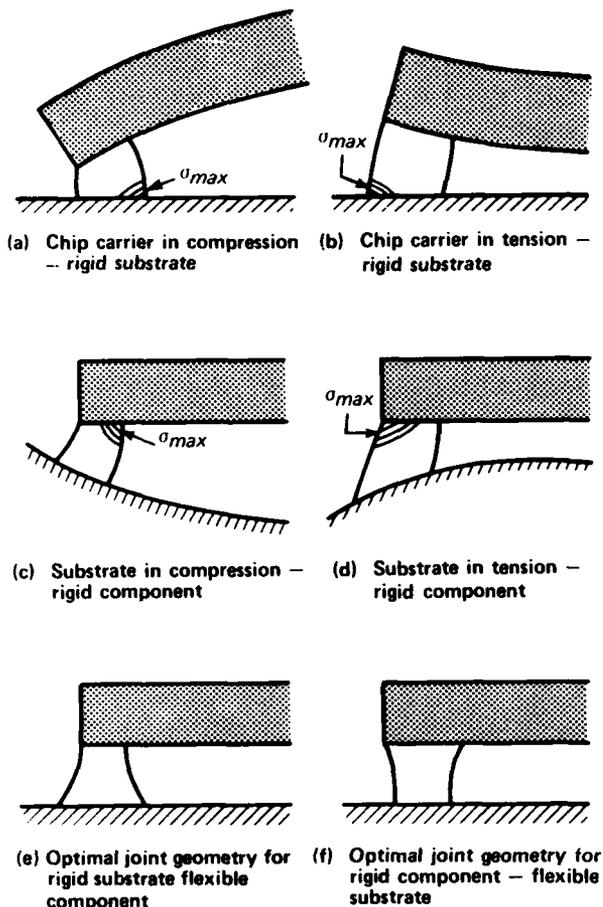


Figure 10. Effect of component and substrate bending stiffness on tensile stress concentrations in LCCC soldered interconnections.

An example of one of the geometrical models used for this analysis is shown in Fig. 11. In order to account for the difference in the TCE for the solder joint, it was necessary to include the constraining ceramic from the substrate and chip carrier in the model. Due to the size and complexity of the physical model, the following were assumed:

- A linear elastic analysis neglecting plastic flow and time-dependent phenomena
- A time-averaged value for Young's modulus over one-half the temperature cycle
- A Poisson ratio of 0.4

Calculated stresses would be significantly higher than those actually observed because of plastic flow and recrystallization mechanisms. However, valuable information concerning the influence of geometrical

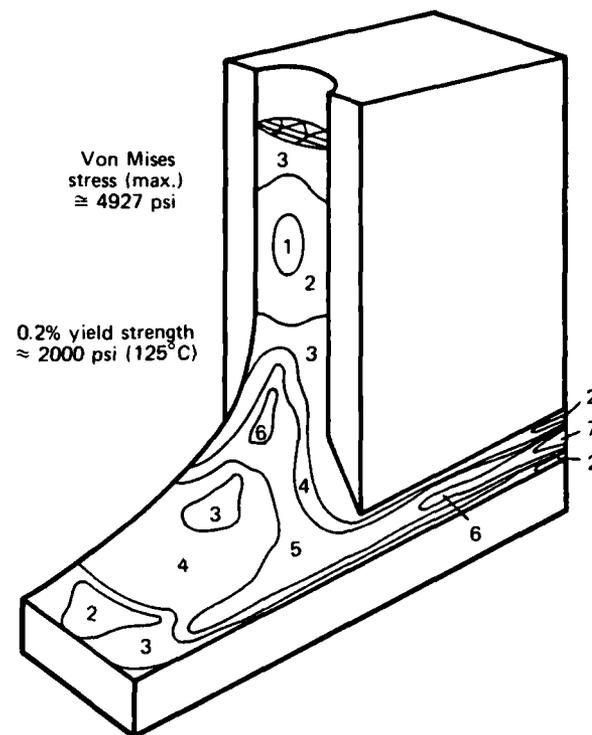


Figure 11. Finite-element model of LCCC solder joint for temperature-cycled stress calculation (23° to 125°C). Contours with numbers less than or equal to 2 indicate regions where Von Mises stress is greater than 0.2% yield strength.

parameters on stress concentration factors can be obtained. In Fig. 11, stress contours indicate the areas where localized plastic flow should occur. The largest stresses can be found in the region of the side castellation; stress fractures here because of temperature cycling are quite common. Other areas of high stress occur in the heel and toe portions of the joint.

Six solder joint models were constructed to estimate tensile stresses at the toe of the solder fillet when the joint was cooled from 125° to -55°C. These stresses, resulting from the contraction of the solder upon cooling, are believed to be responsible for thick film pad delamination. The vertical and horizontal stress components calculated are shown alongside the various models in Fig. 12. In Fig. 13, the tensile stress component acting on the pad metallization is plotted versus position for one of the solder joint models illustrated in the previous figure. The analysis points to the following conclusions regarding the effects of geometry on these stress components:

1. Increases in fillet angle (as shown in Fig. 12) result in increases in both the vertical and horizontal stress components.
2. Eliminating the side castellation will have little effect toward reducing both horizontal and vertical stress components at the toe of the solder joint.
3. Decreasing the pad length will reduce the horizontal stresses.
4. The effect of stress relief at the interface due to increases in the standoff height were found to be a maximum at 8 mils, i.e., the stresses were uniformly distributed throughout the heel of the

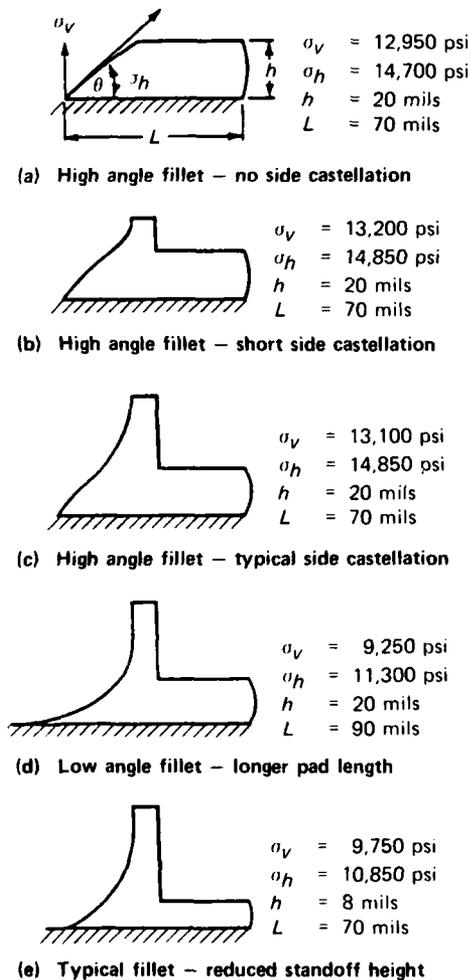


Figure 12. Results of FEM stress analysis to investigate optimal joint design for temperature-cycled LCCC solder joints.

joint. Below 8 mils, the stress began to increase while above 8 mils the shear stresses showed no further changes at the bond interface.

In addition to this analytical information, solder joint shear tests performed by Reimer²³ indicate that the ultimate fracture strength for shear with thick film materials is higher than that for tension by a factor of two. This would indicate that the best way to obtain a fatigue-resistant joint with respect to temperature cycling is to reduce the tensile stress component, which can be done simply by reducing the fillet angle and the standoff height. Unfortunately, reducing the standoff heights to values that yield low tensile stress components results in a joint design that makes post cleaning more difficult. The pillar-style joint shape, which does not contain a fillet, represents an alternative way to eliminate thick film bonding pad delamination.

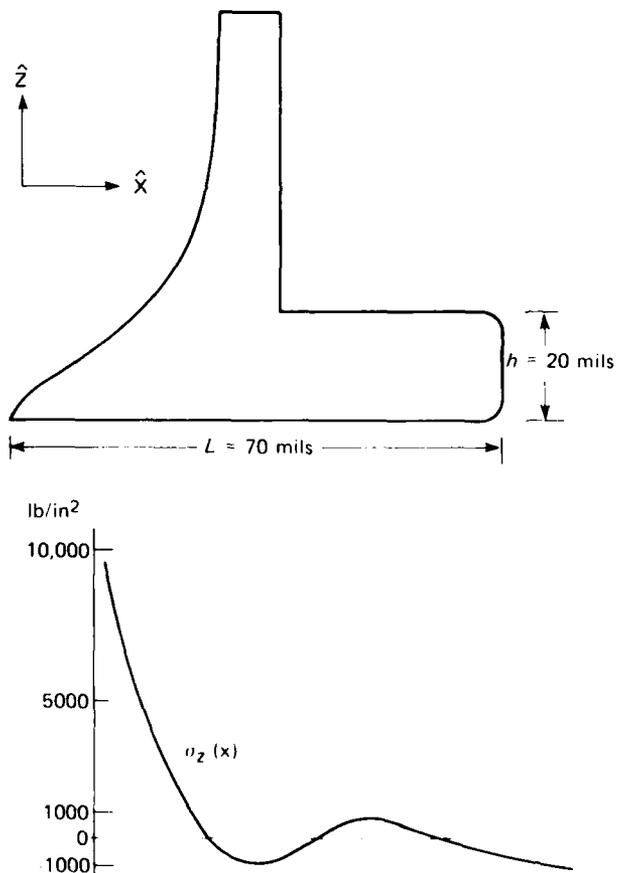
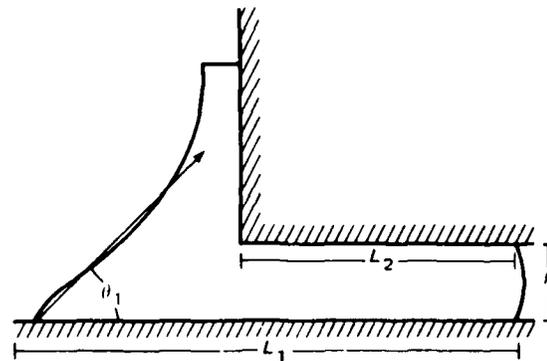


Figure 13. Tensile stress acting on pad metallization as a function of position along joint (see Fig. 12c).

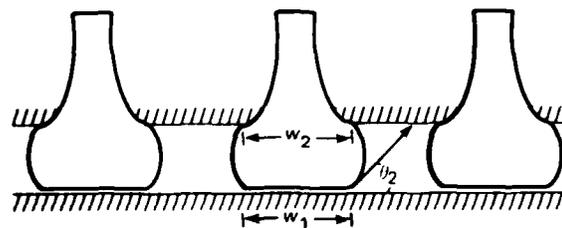
A finite-element analysis was performed on a rectangular pillar-style solder joint (Fig. 14) with estimated stress contours. The results indicate negligible tensile strains, as was expected. However, interface shear stresses and, consequently, the Von Mises stresses are quite large near the periphery of the bond interface because of the bulge that usually results from the solder joint. This bulge varies according to the amount of weight that the molten solder must support during the reflow operation. Stress concentration factors of about 2 to 3 due to this effect have been estimated by varying the curvature radius for the model illustrated in Fig. 14.

Figure 15 illustrates all of the solder joint design parameters that were evaluated in this study with regard to their effect on interfacial strains during temperature cycling or thermal shock testing. The most significant factor contributing to the tensile stresses at the solder joint/substrate interface is the angle θ_1 , the fillet angle, which is in turn influenced by the height of the solder joint. Thermal stress analysis indicates that a reduction in this angle will lead to significant reductions in the normal stress components at the solder/substrate interface.

The most significant factors influencing the interfacial shear stresses are the standoff height h and the angle θ_2 . Reductions in shear stresses can be achieved by increasing the height and reducing the contact angle θ_2 to 90° . It should also be noted that increasing the length of the pad to reduce the fillet angle will also increase the shear stress at the bond interface, partic-

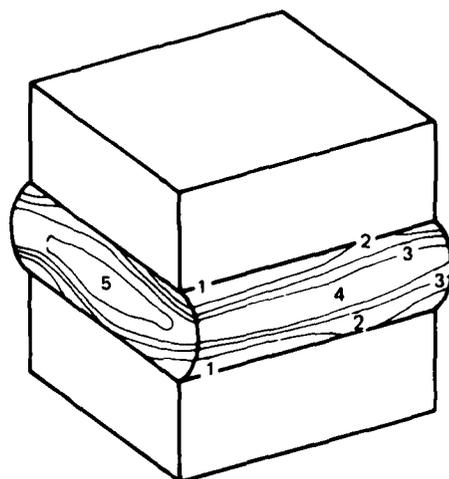


(a) Side view of leadless chip carrier solder joint.



(b) Front view of leadless chip carrier solder joints.

Figure 15. Geometrical design parameters for chip carrier solder joints.



Von Mises stress (psi)

- 9201 = 1
- 8355 = 2
- 7510 = 3
- 6665 = 4
- 5819 = 5

Figure 14. Stress contours for a rectangular pillar-style solder joint, temperature cycled from 125° to -55°C .

ularly in the fillet region. However, this increase was estimated to be relatively minor when compared to the net reduction in shear stress obtained by increasing the standoff height.

Choices concerning optimization of the solder joint design depend primarily on whether the bond is more likely to fail in shear or in tension. Reimer²³ has indicated that thick film solder bonds are significantly more tolerant of shear forces than of tensile forces. Thus, reductions in the tensile stresses at the expense of additional shear stresses would be preferable to prevent pad delaminations in thick film circuits.

For pillar-style geometry, it is possible to optimize the joint by choosing a large standoff (> 8 mils) and by increasing the contact angle to 90° . In practice, however, this is difficult to do with standard reflow techniques. The contact angle is highly influenced by pad geometry, component weight, solder volume, and the surface tension of the molten solder.

4.0 EXPERIMENTAL CONDITIONS AND METHODS

4.1 TEMPERATURE-CYCLING EXPERIMENTS

A temperature-cycling test was performed on 36 20-pin leadless chip carriers soldered to Pt-Au thick film bonding pads fired on 96% alumina (Al_2O_3). The test was performed to investigate the effect of temperature cycling on joints with differing standoff heights. The solder bond integrity prior to and after temperature cycling was measured using a torque shear testing device.

Three large 5 × 7-in. ceramic substrates were used for the test, each mounted to a copper-clad Invar heat sink and partially populated with 20-pin chip carriers. Each board had 12 specimens, four each of the three standoff heights of 50 μm , 125 μm , and 250 μm (2, 5, and 10 mils). The temperature cycling consisted of 200 cycles between -55° and 150°C with ½ hour dwell periods at the temperature extremes. An assembled test board is shown in Fig. 16.

The effect of temperature cycling on the solder bond shear strength was measured using a torque shear tester. Prior to temperature cycling, three chip carrier specimens (one each of the standoff heights) from each of the test boards were torque tested and their initial torque shear strength was recorded. After 200 temperature cycles, the remaining chip carriers were visually inspected for signs of cracking or adhesion loss and then torque tested. None of the chip carrier specimens exhibited any cracking or pad lifting. The results from the test (Table 1) indicate that the 125 μm (5 mil) standoff height suffered no loss in shear strength resulting

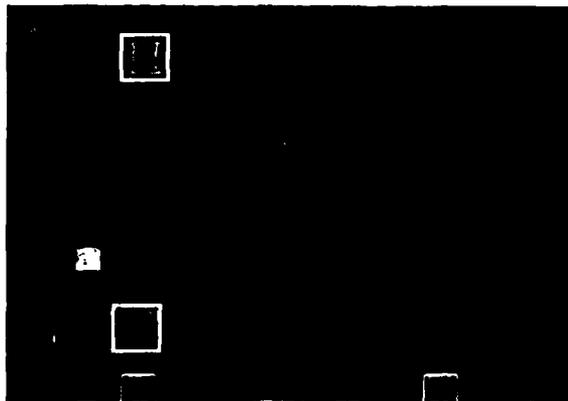


Figure 16. Test board after 200 temperature cycles with 20-pin chip carrier specimens.

Table 1
 Results of torque shear test for temperature-cycled LCCCs on thick film (Pt-Au) ceramic

| Solder Joint Height | Initial Torque Strength (N-m) | Final Torque Strength (N-m) | Percent Reduction in Torque Strength |
|-----------------------|-------------------------------|-----------------------------|--------------------------------------|
| 50 μm (2 mils) | 3.05 | 2.55 | -16 |
| 125 μm (5 mils) | 2.17 | 2.19 | 0 |
| 250 μm (10 mils) | 2.18 | 1.83 | -15 |

from the treatment while both the 50 μm and 250 μm specimens suffered roughly a 15% loss in shear strength. It should be noted, however, that the small standoff solder joints had a larger shear strength both initially and after the temperature cycling.

Initially, the primary location for the fractures from the torque test occurred at either the solder/conductor interface or the conductor pad/ceramic interface, with a small minority occurring at the chip carrier bonding pad interface. Examination of the bonding pads for the carriers that were torque tested after temperature cycling showed that separation occurred exclusively at the conductor/ceramic interface. This indicates that some reduction in the adhesion of the Pt-Au thick film bonding pad to the underlying ceramic had occurred as a result of the temperature cycling.

4.2 POWER-CYCLING EXPERIMENTS

4.2.1 Preliminary Power-Cycling Studies

Power-cycling experiments were designed to determine the sensitivity of joint design to the number of cycles to failure. In order to study the effects of joint height and geometry, solder processing techniques had to be devised to attain the desired joint height and fillet shape. The ability to control standoff height allows for both the fabrication of solder joints designed with optimum fatigue characteristics and the easy removal of residual flux during post-attachment cleaning. In order to achieve a wide range of heights and geometries for chip carrier soldered connections, it was necessary to bump chip carriers by placing premeasured

quantities of solder on the metallized bonding pads and reflowing them. This ensured that a sufficient and consistent amount of solder was available for any practical joint type. Additional details relating to the solder processing methods investigated in this study are discussed in greater detail in Section 4.4. For the experimental samples used in the following studies, standoff height was accomplished either by inverted reflow or by hot air techniques, also discussed in Section 4.4.

A preliminary phase of power-cycling tests was performed to determine what factors are significant in accelerating failures in chip carrier solder joints. Initially, nine chip carriers were chosen for this test (three 84-, three 68-, and three 52-pin), each mounted on a 2×2 -in., 25-mil ceramic substrate. Two power mosfet devices were used to dissipate power into the chip carrier die cavity. Substrate bonding pads were metallized with a copper thin film and then flash plated with gold to prevent oxidation prior to attachment. During the test, the solder temperature was controlled by a feedback circuit monitoring the voltage changes in a thermocouple soldered to one of the leads for each chip carrier specimen. An individual test sample is shown in Fig. 17; the entire group is shown in Fig. 18. Initially, the solder joints were power stored at 80°C (4.5 W continuous) for 1000 hr in air and then power cycled at a level of 5 W for a cycle frequency of 6 cycles/hr. Joint heights for the samples were approximately 10 to 15 mils. All of the joints survived 1500 power cycles. However, many of the mosfet devices began to fail shortly thereafter because of the effect of temperature cycling occurring at the soldered die interface. Weakening of this interface due to enhanced intermetallic formation and fatigue cracking resulted

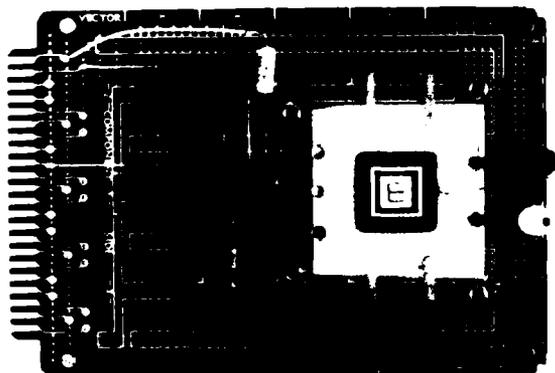


Figure 17. Experimental test setup for power storage and power-cycling test.

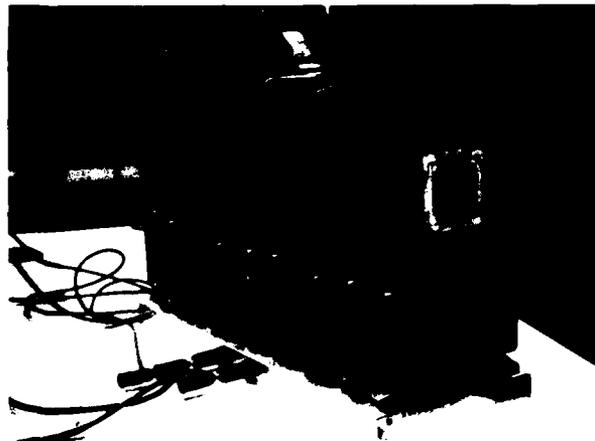


Figure 18. Individual test card for power-cycling experiment with 68-pin chip carrier.

in the eventual reduction of thermal conductivity across this bond interface. The remaining samples showed little effect from the treatment when examined by a scanning electron microscope (SEM), and further power cycling was discontinued. Solder joints from 68- and 84-pin chip carrier specimens are shown in Fig. 19 after the 1500 power cycles; the results from the test are presented in Table 2.

The steady-state strain differential across the solder joints was then estimated by an FEM analysis; the results indicated maximum shear strains on the order of 0.2% (assuming 15-mil cylindrical joints). Worst-case strain estimates can be made by assuming that the substrate is constrained from thermal expansion. These worst case values at a 5-W power level were less than 1% of the total strain amplitude. Estimates of service life for this strain amplitude using a modified Coffin-Manson relation (Eq. 7) indicated an $N_f \gg 1000$.

4.2.2 Joint Geometry Effect on Power-Cycling Fatigue Life

A second experiment was then undertaken to determine whether joint geometry was a significant factor with regard to solder joint reliability. The study involved eight chip carriers (four 68- and four 52-pin chip) using four basic solder joint designs, shown in Fig. 20. Two of the designs called for large standoffs (approximately 16 mils) while the other two used the more typical 2 to 3 mil standoff height that is obtained with more conventional reflow techniques. Power cycling was carried out with a 10-W chip resistor epoxied in the cavity with high-temperature (240°C)



Figure 19. Solder joints (Sn62) for 84-pin and 68-pin LCCC specimens after 1000-hr power storage at 80°C and 1500 power cycles at 5 W.

Table 2
 Summary of results from combined power storage and power-cycling test for LCCC solder joints (Sn62)

| Chip Carrier Type/Number | Standoff Height | Solder Power Storage | Failures After 1500 Power Cycles at 5 W* |
|--------------------------|------------------|----------------------|--|
| 52 pin/3 | 10 mils (250 μm) | 1000 hr at 80°C | None |
| 68 pin/3 | 10 mils (250 μm) | 1000 hr at 80°C | None |
| 84 pin/3 | 10 mils (250 μm) | 1000 hr at 80°C | None |

*Cycle frequency ≈ 144 cycles/day

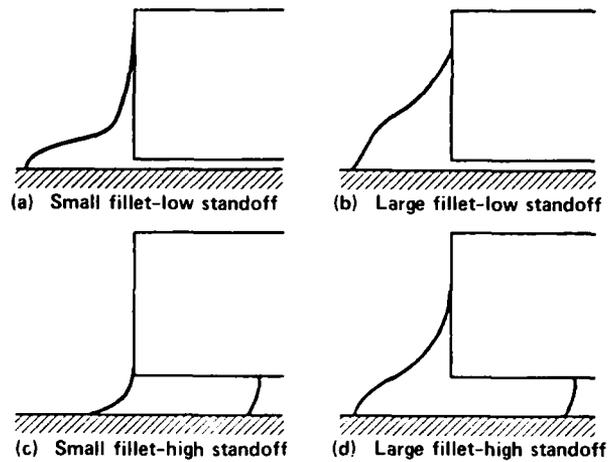


Figure 20. Four solder joint types for the power-cycling test to investigate the effects of joint geometry on reliability.

thermally conductive epoxy and two external power leads soldered to the resistors with Au80/Sn20 solder. The chip carrier specimens were mounted on 2 × 2-in. ceramic substrates and placed on a large aluminum heat sink. Thermocouples were epoxied to the chip resistor to detect significant thermal resistance changes from the substrate to the resistor surface. It had been observed previously that the occurrence of cracking just prior to failure brings about a significant increase in the thermal resistance. Thermal resistance changes can be shown to provide a much more sensitive measure of solder joint cracking than electrical resistance measurements. The steady-state temperature of the heat sink during the power cycling tests was 28°C. The experimental setup is shown in Fig. 21.

The mounting of the ceramic substrates to an isothermal heat sink served two functions in this experiment:

1. The heat sink allowed large power dissipations required to produce the strain levels needed for accelerated testing purposes.
2. It ensured that the maximum differential thermal expansion between the carrier and the substrate was a maximum during steady-state operation.

The effect of power cycling on the differential thermal expansion between carrier and substrate for testing with and without an isothermal heat sink is illustrated in Fig. 7. The use of a heat sink permitted the implementation of an inexpensive, steady-state finite-element model to provide numerical estimates of cycle life for comparison with experimental results.

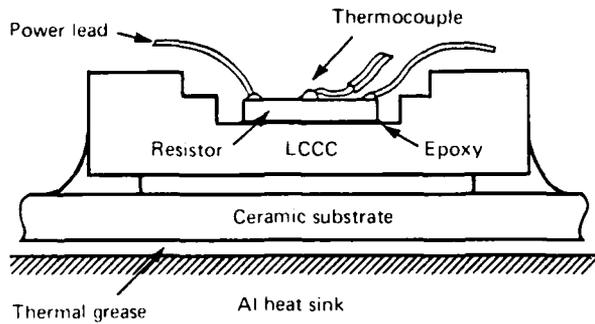


Figure 21. Test assembly used for power-cycling experiments to investigate the effect of solder joint geometry on fatigue life.

Of the four geometries shown in Fig. 20 for both 52- and 68-pin LCCCs, all of the samples showed little change in thermal resistance prior to the completion of the first 3000 power cycles. These power cycles were performed at a level of 10 W. The first significant change in thermal resistance occurred after the completion of 3200 cycles. The increase in thermal resistance was approximately 1.5°C/W and occurred over a range of 50 temperature cycles. Electrical continuity across the solder joints began to deteriorate rapidly after this point, and an open was noted after an additional 200 cycles. At this time, all of the remaining samples were microscopically inspected for visible signs of cracking, but no cracking or other forms of significant joint deterioration were noted.

To accelerate the failure in the remaining samples, the power dissipation was increased to 14 W. When this was done, one of the 68-pin specimens cracked from side to side with the fracture passing through the center of the cavity. The location of the fracture was a clear indication that the majority of the thermal stress during power cycling is accommodated by the ceramic carrier and not the solder joints. All of the remaining samples lasted an additional 1200 cycles at the increased power level, after which point the test was ended and each of the remaining specimens examined. The results, with estimated displacements and shear strains, are presented in Table 3. Also included in the table are service life predictions from Engelmaier's modified form of the Coffin-Manson equation.

Experimental results of chip carrier studies indicate that large fillet, low standoff joint shapes provided higher quality joints after extensive power cycling than did solder joints with high standoffs and small fillets. The relatively poorer quality high standoff specimens may indicate that differences in cyclic and time-dependent relaxation effects may be highly dependent on whether shear or tensile strain predominates, the number of cycles to failure (N_f) being greatly reduced for the latter case. Also, it was noted that the 52-pin chip carrier solder joints were significantly more degraded than were the 68-pin chip carrier specimens. This effect may be a result of either (a) a taper in these solder joints resulting from a substrate bonding pad larger than the corresponding chip carrier bonding pad

Table 3
 Summary of results for power-cycled LCCC solder joints (Sn62)

| Sample No. | LCCC Type | Geometry Type (see Fig. 20) | Maximum Estimated | | Predicted Life* (N_f) | Observed Life |
|------------|-----------|-----------------------------|-------------------------------|---------------------|---------------------------|---------------|
| | | | Differential Expansion (mils) | Joint Height (mils) | | |
| 1 | 52-pin | a | 0.08 | 2 | 830 | > 4410 |
| 2 | 52-pin | b | 0.07 | 2 | 1,185 | > 5630 |
| 3 | 68-pin | a | 0.08 | 2 | 830 | > 4410 |
| 4 | 68-pin | b | 0.09 | 2 | 575 | > 4410 |
| 5 | 52-pin | c | 0.09 | 16 | 129,000 | ≈ 3210 |
| 6 | 52-pin | d | 0.09 | 16 | 129,000 | > 4410 |
| 7 | 68-pin | d | 0.12 | 16 | 60,100 | > 4410 |
| 8 | 68-pin | d | 0.14 | 10 | 13,600 | > 3210 |

*Predictions for N_f from Eq. 7; $T_s \approx 35^\circ\text{C}$, $\nu = 144$ cycles/day, $F = 1$.

or (b) the thinner ceramic side wall on the 52-pin carrier, resulting in larger solder strains. The first reason is probably the more significant since the test substrates are significantly less rigid than the chip carrier and the joint taper is in the direction of increasing stress concentration at the carrier bond interface. Thus, based on stress concentration arguments, these samples should degrade more rapidly.

As a comparative analysis, solder joints from six of the power-cycled specimens are shown in Figs. 22 through 27. Solder joint appearance after power cycling was significantly better for low standoff solder joints, improving as the fillet volume increased. Joints

with large standoffs that contained an appreciable fillet also fared comparatively well. In addition, it was noted for the chip carrier specimen whose joints failed that solder joint cracking was not localized at the corner joints as is usually the case for such fractures in thermally cycled solder joints. Some of the poorer samples exhibited significant micropore formation with large voids in the castellation region. Significant intermetallic formation was also noted at the bond interfaces due mainly to the presence of gold in these regions. Since solder temperatures did not exceed 40°C throughout the entire test (< 1000 hr), stress-assisted diffusion appears to be the dominant factor for any



Figure 22. Low standoff-large fillet samples (68-pin LCCC) after 5600 power cycles.



Figure 24. High standoff-large fillet samples (52-pin LCCC) after 4400 power cycles.



Figure 23. Low standoff-small fillet samples (68-pin LCCC) after 4400 power cycles.



Figure 25. High standoff-small fillet samples (52-pin LCCC) showing fatigue failure after 3200 power cycles.



Figure 26. Low standoff-large fillet samples (52-pin LCCC) after 4400 power cycles.



Figure 28. Macrovoid formation inside castellation due to the large stresses and temperatures that occur there.



Figure 27. High standoff-large fillet samples (68-pin LCCC) after 4400 power cycles.

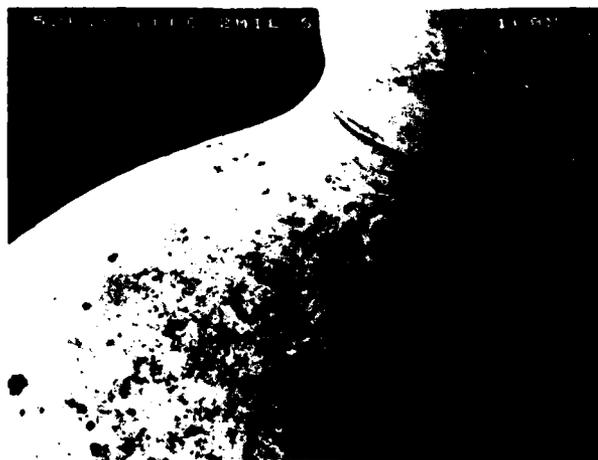


Figure 29. Fatigue striations resulting from LCCC bending for low standoff-small fillet sample (52-pin LCCC).

additional intermetallic growth. Also, at strain rates typical in power-cycling applications at and above room temperature, cyclic creep is probably the dominant contributor to void formation and grain recrystallization. As shown in Fig. 28, macrovoid formation can be seen to predominate in the castellation region of the solder joint resulting from the relatively high stresses that occur there. Fatigue striations for one of the samples are illustrated in Fig. 29. These striations correlate with FEM calculations that predict significant bending there due to the particular joint geometry for this specimen, as was illustrated previously in Fig. 9.

Cross sections of the low standoff, large fillet solder joints were made in order to verify that the integrity of the joint under the chip carrier, not visible during the initial SEM inspection, was of the same high quality as the fillet portion of the solder joint. SEM photomicrographs of the fillet and that portion underneath the carrier are shown in Figs. 30a and 30b. The figures indicate the high quality of this interconnection despite the extreme power levels.

These preliminary results also indicate that solder joint shape may be a primary rather than a secondary

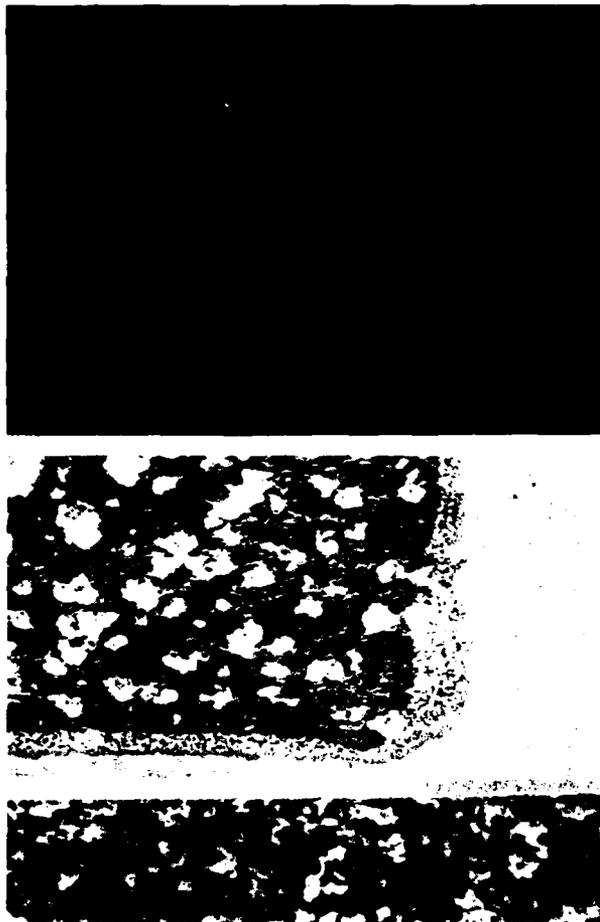


Figure 30. Cross-sectioned solder joint (low standoff-large fillet specimen) after 4000 power cycles.

factor in determining solder joint fatigue life in power-cycled environments. The effects of stress concentrations and stress relaxation can vary significantly with solder joint shape. Similarly, substrate and/or carrier warpage effects can be significantly influenced by solder joint geometry. These effects can result in large differences in the tensile strain component at the expense of, or in addition to, pure shear strain. If low cycle fatigue properties were independent of the strain direction, variations in strain components might result in minor miscalculations in the number of cycles to failure. However, large differences in the time-dependent behavior associated with compressive, tensile, and shear strains could account for the observed discrepancies between theory and experiment. For example, tensile relaxation tests conducted by Rhode and Swearingen¹² for several soft solder alloys showed that eu-

tectic SnPb solder relaxes to 50% applied stress at 25°C in less than 3 minutes.

Baker¹⁴ conducted a similar study to investigate compressive stress relaxation for tin-lead solder alloys. His results indicated that the relaxation rate for compressive specimens was independent of the applied stress and that the relaxation rate increased with increasing lead content for tin-lead alloy specimens. For eutectic SnPb solder, he observed a 50% stress relaxation that occurred in 138 hr at room temperature, in 28 hr at 43°C, and within 3 hr at 73°C. Comparison of these independent observations for the eutectic tin-lead solder indicates a 3 order-of-magnitude difference in relaxation rates for tensile versus compressive specimens. Making the reasonable assumptions that (a) low standoff joints with large solder fillets undergo more compressive straining than do higher standoff joints and (b) higher joints undergo more tensile straining than do shorter joints, then Coffin-Manson equations of the type used for solder reliability predictions would underestimate the low cycle fatigue life for the low standoff solder joint and overestimate it for the high standoff solder joint.

The important conclusion from these initial tests is that small standoff solder joints on ceramic substrate materials should provide a reliable interconnection for use in a power-cycled environment. This knowledge permits the fabrication of solder joints possessing a relatively small fillet angle (as was prescribed in Section 3.4 for eliminating pad delamination effects while power cycling), which in turn requires that the solder joint standoff height be relatively low. It should be noted that these results are applicable only for the joint geometries and for the package and substrate materials discussed in the analysis.

4.2.3 Effect of Solder Temperature and Power-Cycling Frequency

Additional studies have been undertaken to observe the effect of frequency, temperature, and FEM-estimated strain range on the number of cycles to failure. In this experiment, pillar-style solder joints were fabricated using pre-bumped 52- and 68-pin ceramic chip carriers and special hot air reflow techniques. The geometry for these solder joints is illustrated in Fig. 31. The standoff height for specimen solder joints was approximately 25 mils. The experimental test assembly was identical to that shown in Fig. 21 and as discussed in Section 4.2.2. Two temperature levels, 40°C and 65°C, and two frequency levels, 96 cycles/day and 288 cycles/day, were used. Strain levels varied somewhat between samples, and subsequent strain estimates were based on FEM-estimated differential thermal expan-

sion and independent temperature measurements for each of the test specimens. The results for this test, indicating FEM-estimated strain levels and both observed and estimated (Eq. 7) cycles to failure for all

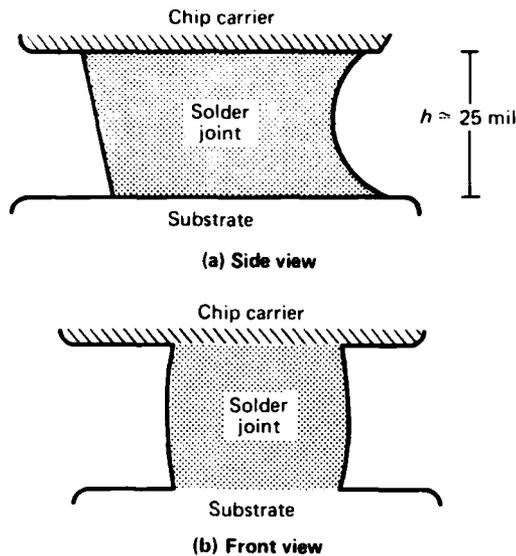


Figure 31. Pillar-style LCCC solder joints.

16 specimens, are presented in Table 4. N_f is plotted versus estimated strain range in Fig. 32. Observed failure modes in most cases indicated that the fracture predominates at the chip carrier bonding pad interface. Figures 33 and 34 are SEM photomicrographs of typical specimens exhibiting this failure mode.

Typically, the smallest solder cross section occurs at the chip carrier bonding pad interface. Several of the chip carrier specimens exhibited fatigue failure within the solder itself, not at the soldered interface. In these exceptional cases, the minimum cross-sectional area for the joint occurred toward the midsection. Figure 35 shows an example of a solder joint displaying this failure mode.

A primary observation from this experiment was the significant effect of frequency on the number of cycles to failure. Predictably, the effect of temperature at the higher cycle frequency (288 cycles/day) was less pronounced than that for the lower frequency (96 cycles/day). This would be due to the increased plastic strain resulting from creep and other time-dependent relaxation phenomena.

These results can be correlated with those expected for actual chip carrier packages mounted to non-isothermal substrates at reduced power levels by comparing Figs. 36a and 36b. Figure 36a illustrates the

Table 4
 Summary of results from power-cycling test: The effect of solder temperature and cycle frequency on fatigue life

| Sample No. | No. of Package Leads | No. of Soldered Leads | Solder Temperature (°C) | Cycle Frequency (cycles/day) | FEM-Estimated Shear Strain (%) | Predicted Fatigue Life* (cycles $\times 10^3$) | Observed Fatigue Life (cycles $\times 10^3$) |
|------------|----------------------|-----------------------|-------------------------|------------------------------|--------------------------------|---|---|
| 1 | 52 | 16 | 40 | 96 | 0.25 | 900 | 33.5 |
| 2 | 52 | 52 | 40 | 96 | 0.35 | 400 | 16.0 |
| 3 | 52 | 16 | 40 | 288 | 0.42 | 280 | 23.0 |
| 4 | 52 | 52 | 40 | 288 | 0.37 | 600 | 24.0 |
| 5 | 52 | 16 | 65 | 96 | 0.37 | 200 | 10.5 |
| 6 | 52 | 52 | 65 | 96 | 0.20 | 900 | 29.0 |
| 7 | 52 | 16 | 65 | 288 | 0.33 | 870 | 29.0 |
| 8 | 52 | 52 | 65 | 288 | 0.37 | 380 | 21.6 |
| 9 | 68 | 20 | 40 | 96 | 0.37 | 330 | 10.8 |
| 10 | 68 | 68 | 40 | 96 | 0.24 | 1000 | 21.0 |
| 11 | 68 | 20 | 40 | 288 | 0.26 | 950 | 54.0 |
| 12 | 68 | 68 | 40 | 288 | 0.37 | 620 | 40.0 |
| 13 | 68 | 20 | 65 | 96 | 0.40 | 160 | 10.0 |
| 14 | 68 | 68 | 65 | 96 | 0.45 | 140 | 2.5 |
| 15 | 68 | 20 | 65 | 288 | 0.38 | 240 | 32.0 |
| 16 | 68 | 68 | 65 | 288 | 0.40 | 310 | 20.7 |

*Predictions for N_f from Eq. 7; $F = 1$.

● $T = 40^{\circ}\text{C}$, $\nu = 96$ cycles/day ⊙ $T = 40^{\circ}\text{C}$, $\nu = 288$ cycles/day
 ◆ $T = 65^{\circ}\text{C}$, $\nu = 96$ cycles/day ■ $T = 65^{\circ}\text{C}$, $\nu = 288$ cycles/day

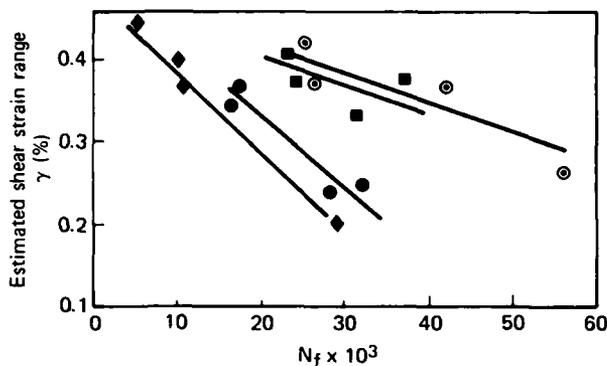


Figure 32. Number of cycles to failure versus estimated shear strain range for power-cycled leadless chip carrier solder joints.



Figure 33. Macrovoid formation at the chip carrier bond interface resulting from power-cycling stresses.

solder strain profile during heat-up, steady-state operation, and subsequent cool-down for a chip carrier package when mounted to an isothermal heat sink. In Fig. 36b the strain profile is illustrated for the more conventional situation. For this case, the shear strain range is composed of a high transient strain of limited time duration and a low steady-state strain. The high-frequency data collected in this study should correlate with that corresponding to the transient heat-up and cool-down for the real situation for applications involving device dissipations of a watt or more. The data provided at low frequency provide a lower



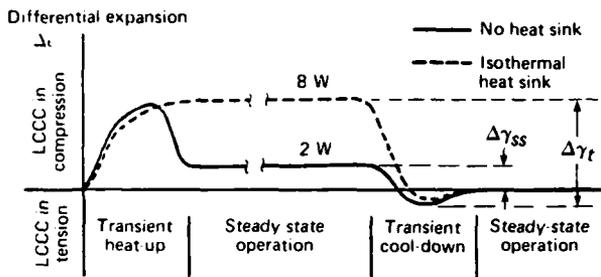
Figure 34. Power-cycling fatigue cracks at the chip carrier bond interface.



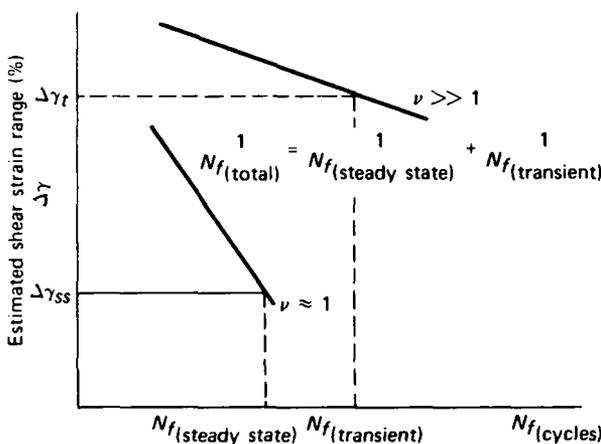
Figure 35. Solder fatigue cracking for a joint with an hourglass shape.

bound for the number of useful power cycles for applications involving more than 96 power cycles/day. Assuming that both the transient strain range and the steady-state strain range are known, the total number of cycles to failure can be estimated from the relation

$$\frac{1}{N_f} = \frac{1}{N_{ss}} + \frac{1}{N_t} \quad (10)$$



(a) High frequency-large transient strain range ($\Delta\gamma_t$) and low frequency-small steady state strain range ($\Delta\gamma_{ss}$) for typical power cycle.



(b) Predicting total number of cycles to failure from high frequency and low frequency isothermal power cycling data.

Figure 36. (a) High-frequency-large transient strain range ($\Delta\gamma_t$) and low-frequency-small steady-state strain range ($\Delta\gamma_{ss}$) for typical power cycle. (b) Predicting total number of cycles to failure from high-frequency and low-frequency isothermal power-cycling data.

The values of N_{ss} (steady state) and N_t (transient) can be estimated from the experimentally obtained data shown in Fig. 32. For applications involving a lower cycle frequency, further testing would be necessary.

As an example, consider a situation where the maximum transient strain produces the same number of cycles to failure as the steady-state strain level (i.e., $N_{ss} = N_t$). In this case, the combined number of cycles to failure would result in a useful life equal to $N_{ss}/2$. Thus, the transient effects can only reasonably be neglected for cases where $N_{ss} \gg N_t$.

4.3 THE SOLDER BALL SHEAR TESTING

Solder ball shear testing was investigated in order to characterize solder bond parameters and thick film solderability, and to evaluate temperature cycling and thermal shock effects as well as isothermal aging characteristics. The following procedure was developed for this study:

1. Placement of a premeasured quantity of solder on a special test substrate consisting of solder bonding pads of predetermined size and shape,
2. Reflow of the solder,
3. Experimentally treating each test substrate (i.e., thermal cycling or shock testing, high temperature storage, etc.),
4. Shear testing the solder balls with a conventional ball shear testing device.

A Dage-Precima Shear Testing Machine was used in the study, and the test procedure was similar to that used previously for ball bond shear testing.²⁴ We used this technique primarily because we needed a rapid, inexpensive method to test the compatibility of various solder/metallization systems. Also, it was desirable to have a method that could investigate (a) the effect of prolonged high-temperature storage on the adhesion of tin-lead solder alloys (Sn60, Sn63, and Sn62) to Pt-Au thick film bonding pads on multilayer thick film substrates and (b) the effect of temperature cycling and thermal shock on the degradation of the bonding pad interface.

For the purpose of determining whether or not solder balls could be used to simulate actual soldered interconnections, a thermal stress analysis was undertaken similar to that discussed in Section 3.4.2. In Fig. 37, one-quarter of a solder ball soldered to a thick film ceramic substrate (square bonding pad) is shown with the stress contours. The case illustrated here represents temperature cycling from 125° to -55°C. Stress levels at the interface were calculated to be on the order of those for a similar solder joint bonding pad interface area. Location and intensity of stresses will vary depending on the height, pad geometry, and curvature of the solder ball. Figure 38 shows a typical soldered ball on Pt-Au thick film bonding pads fired over dielectric on 96% alumina substrates.

²⁴H. K. Charles, Jr., G. V. Clatterbaugh, and J. A. Wiener, "The Ball Bond Shear Test," *Semiconductor Processing*, Dinesh C. Gupta, ed., ASTM STP 850, American Society for Testing and Materials (1984).

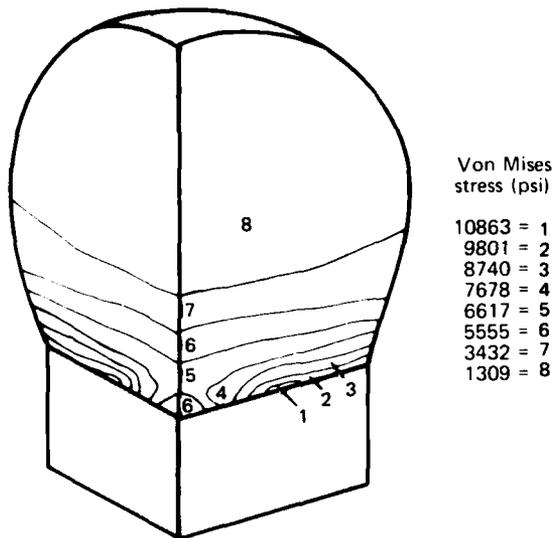


Figure 37. Stress contours for a solder ball on a ceramic substrate temperature-cycled from 125° to -55°C.



Figure 38. SEM photomicrograph of a solder ball shear testing sample.

4.3.1 Isothermal Aging Characteristics of the Thick Film/Solder Interface

The solder ball shear techniques discussed above were applied to the investigation of isothermal aging characteristics of three tin-lead alloys (Sn60, Sn62, and Sn63) soldered to Pt-Au thick film conductors. Four temperature levels (90, 110, 125, and 150°C) were chosen in order to possibly extract a thermal activation energy for the rate of change in shear strength. A square bonding pad geometry, 35 × 35 mils, was used. The bond interface area is similar to that for 50-mil pitch chip carrier bonding pads.

Solder ball shear test results for the isothermally aged solder balls off the Pt-Au thick film bonding pads indicated that no significant difference in aging characteristics was exhibited by any of the three alloys tested. Graphical shear test data for the eutectic Sn63 alloy is shown in Fig. 39. As indicated by the figure, the rate of change in the shear force required to remove the soldered specimens was large initially and then dropped rapidly toward zero as the aging time progressed. It is believed that the rejection of Pb at the interface and its subsequent buildup at the intermetallic interface slowed the growth rate for the formation of additional weak Au-Sn intermetallics. The rejection of Pb at the the intermetallic interface is probably a result of the low solid solubility of Pb in Au for the temperature range of interest.²⁵ A similar effect was noted previously for pull tested, isothermally aged tin-lead alloy cladding on copper leads soldered to thick film substrates.²⁶

Another unusual feature of the data was the steady-state behavior of the aged interconnections. We expected that the equilibrium condition would approach the same ultimate shear strength value for each of the temperature groups, differing only in the time it took to reach this condition. However, it appears that the diffusion barrier formation is relatively insensitive to

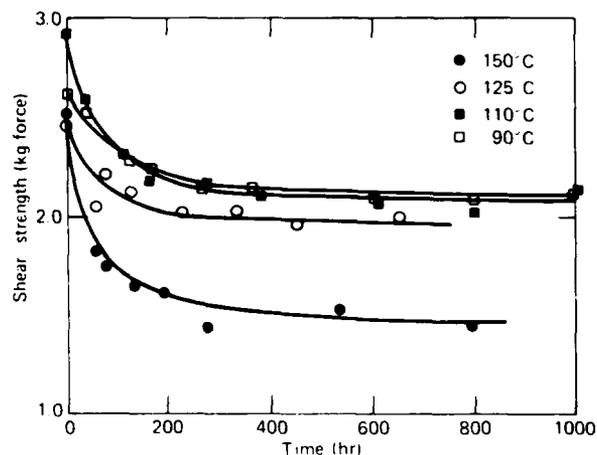


Figure 39. Isothermal aging results for shear-tested solder balls (Sn63) on Pt-Au thick film bonding pads (35 × 35 mils).

²⁵ M. Hansen, *Constitution of Binary Alloys*, McGraw Hill, New York, p. 223 (1958).

²⁶ T. F. Marinis and R. C. Reinert, "Isothermal Aging Characteristics of External Lead Solder Connections," *Proc. 1985 Electronics Components Conference*, pp. 73-80 (1985).

temperature and the percent reduction in strength depends solely on the aging temperature and not on the time-temperature product. This would suggest that excessive temperature storage or temperature-cycle testing of soldered joints could significantly reduce the fracture strength of the soldered interconnections.

4.4 SOLDER PROCESSING TECHNIQUES TO IMPROVE STANDOFF HEIGHT

In this section, we comment on the several techniques investigated in this study to increase standoff height for leadless chip carrier solder joints. The ability to control standoff height permits the hybrid engineer to fabricate solder joints that are designed for optimum fatigue characteristics and easy flux removal during post-attachment cleaning.

4.4.1 Pre-Bumping Chip Carriers With Solder Logs

In order to achieve a wide range of heights and joint geometries for chip carriers, it was found that bumping the carriers by placing premeasured quantities of solder on the metallized bonding pads and then reflowing them insured that sufficient solder was available for any practical solder joint geometry. The procedure consisted of fluxing the carrier pads with a resin (mildly activated) flux and then placing precut solder logs directly on the pads. The solder on the pads is then reflowed. We found that hot plate and infrared techniques were the only available methods that did not result in significant shifting of the manually positioned solder logs during the reflow operation. After the solder logs are reflowed, the solder-bumped chip carriers are cleaned of residual flux and stored in a nitrogen dry box to await attachment. We also tried the conventional technique of solder bumping by dipping in a solder pot, but this method does not produce large enough solder bumps to achieve a significant standoff.

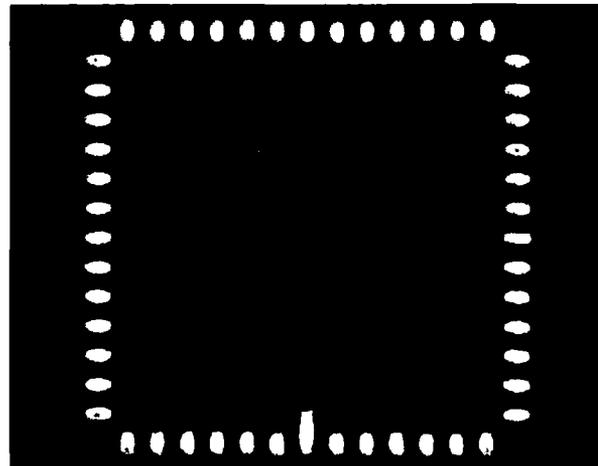
In the procedure described here, the solder was manually placed on the chip carrier leads. However, several automated alternative procedures are commercially available. One notable process, referred to as solid-state solder bumping,²⁷ consists of placing a mask directly over the bottom of the chip carrier with the pad footprint etched from the mask. Preformed solder spheres are dispersed over the chip carrier and mask assembly and settle into the etched portion of the mask resting on the chip carrier bonding pads. At

this point, a heated, nonsolderable material is pressed against the solder spheres with sufficient heat and force to weld the solder to the chip carrier pads. Once the solder is diffusion welded to the pads, the mask is removed and the solder is reflowed.

The process described here for bumping chip carriers resulted in bumps in excess of 25 mils for the largest solder logs used ($l = 0.06$ in., $d = 0.028$ in.). This also accounted for the volume of solder residing in the side castellations. Figures 40a and 40b are views of a 68-pin chip carrier bumped with Sn62 solder.

4.4.2 Inverted Substrate Reflow Method

Possibly the most obvious method for increasing joint height is the inverted substrate reflow method. This involves inverting the chip carrier assembly, thus permitting the gravitational force on the carrier to counter the surface tension of the molten solder during reflow. This technique requires at least one initial attachment however, either by a prior solder reflow or by preattachment using a solid-phase bonding process. Once the carriers have been soldered into place, a subsequent reflow in the inverted position will result in an increased standoff height. Significant increases



(a) Top view of ceramic chip carrier pre-bumped with solder



(b) Side view of chip carrier with solder bumps

Figure 40. 68-pin chip carrier pre-bumped with Sn62 solder logs.

²⁷R. H. Minetti, "Solid Phase Bonding For Use in the Assembly of Microelectronic Devices," *Proc. 1980 International Microelectronics Symposium*, pp. 126-129 (1980).

in the standoff height depend on (a) reducing the bonding pad length, (b) reducing the surface tension of the solder (e.g., using a resin flux during inverted reflow), (c) reducing the castellation length, and (d) increasing the solder volume. Reducing castellation and pad lengths reduces the net surface area of the initial solder joint, thereby lessening the effective surface tension of the system upon reflow.

The solder volume is ultimately the limiting parameter in most standoff designs. The obvious problems with the inverted substrate reflow method are that

1. It is not feasible in cases where the chip carriers are to be mounted on both sides.
2. There is difficulty in controlling solder joint geometries and final standoff heights.
3. Variations occur in standoff heights due to variations in carrier sizes.

These problems, however, may be minor when weighed against the possible benefits gained by increasing standoff height. Standoff values of up to 20 mils were achieved for both 68- and 84-pin chip carriers provided that sufficient solder was present initially. A simple calculation based on a rectangular (joint and fillet) and cylindrical (castellation) model for the volume of a solder joint can provide a sufficiently accurate method to determine how much solder is necessary initially to attain the desired height.

4.4.3 Solder Alloy Process

The solder alloy process requires the use of two solder alloys, a relatively low melting one and a higher melting one. The two alloys used in this study were Sn62 and Sn96. The chip carrier is bumped in the manner described previously with the higher melting Sn96 (96% Sn, 4% Ag by weight) alloy. The substrate is pretinned or screen printed with Sn62. The chip carrier is then properly positioned on the substrate and the assembly is reflowed, with the reflow time and temperature being closely controlled. Gradual introduction of lead into the Sn96 system lowers the melting point, and, if processed long enough, seating of the chip carrier may occur. The appearance of the joint after solidification is slightly mottled due to the variations in the melting temperatures of the various solder phases. Eight LCCC specimens attached to a thin film metallized ceramic substrate (Au plated on phased chrome-copper thin film) were placed in a thermal cycle chamber and underwent 200 thermal cycles in the temperature of 150° to -65°C. Dwell periods at both extremes were 15 min. The solder joints were seriously degraded by significant void formations as shown by SEM examination. Although voiding and grain enlargement were significant, no cracking was observed.

However, since such defects can act as crack nucleation sites during operational strain cycling, these joints would appear to be unsuitable for extending fatigue life.

4.4.4 Four-Post Solder Attachment Method

Another technique for controlling standoff height is the four-post attachment method, which consists of bumping the four center pads on each of the four carrier sides with a high temperature solder and bumping the rest with a lower temperature solder. The alloy system used was the Sn96 (221°C) and Sn62 (179°C) solders. The standoff height is controlled during substrate reflow by maintaining the reflow temperature several degrees below the melting point of the high temperature solder. Thus, the four higher temperature solder posts serve as a spacer to prevent seating during reflow. After this initial reflow, the four high temperature solder posts can be individually hand-soldered as a final processing step.

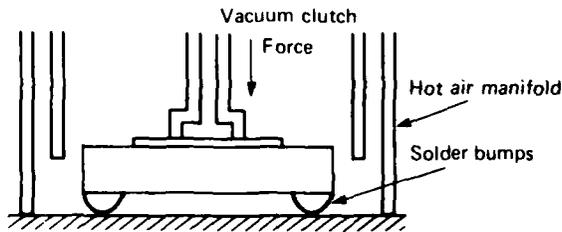
This process can also be used when hand-soldering operations are preferred or more sophisticated reflow techniques are not available. When hand soldering, the four solder posts need not involve the higher temperature alloy. Once the carrier is bumped with the four posts and positioned on the substrate, the four posts are individually hand soldered into place, the other three serving to maintain the desired post height. The rest of the interconnections are then made by hand soldering each of the remaining pads. The advantage to this process is the ability to control the standoff height while avoiding the necessity to combine several alloys in one joint. This system was employed to control the standoff height in the initial power-cycling tests conducted in this study.

4.4.5 The Hot Air Method For Controlled Interconnections

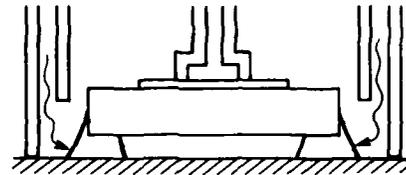
The hot air method is probably the most promising and reliable attachment scheme for high throughput production. The process is easily automated and can be adopted for use with many of the existing, commercially available rework stations for surface mounting applications. The method is illustrated in Fig. 41. The process involves a hot air solder reflow device similar to those used for chip carrier removal, with the addition of a mechanism on the vacuum chuck that allows the operator to adjust for the desired height. In the first step, the vacuum pick-up fixture positions the chip carrier on the substrate. Heated air then flows through a manifold that guides the heat to the chip carrier solder bumps and substrate pads, causing them to reflow. While the solder is still in a liquid state, the

vacuum fixture is raised or lowered to achieve the desired joint geometry. The technique can also produce an hourglass type of solder joint, which is use-

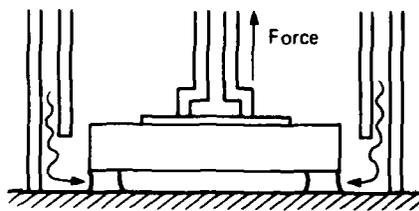
ful when it is desirable to shift the strain from the brittle bond interface to the more ductile solder portion.



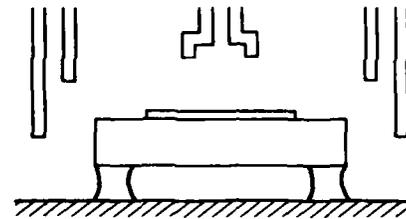
(a) Chip carrier is placed on substrate and hot air manifold surrounds the LCCC. A downward force is exerted on LCCC to provide intimate contact with substrate.



(b) Hot air is released, reflowing LCCC solder joints.



(c) While solder is still liquid, the LCCC is raised to permit standoffs to achieve desired height.



(d) The hot air is removed and the vacuum is disengaged leaving the carrier standoffs at the desired height.

Figure 41. Hot air reflow method for controlled standoff solder joints.

5.0 DISCUSSION

5.1 POWER-CYCLING EFFECTS ON LCCC SOLDER JOINTS

The results for both experimental power-cycling studies and FEM thermal stress analyses indicate that relatively large device power dissipation levels are required to produce sufficient strain on soldered chip carrier leads to induce failure when mounted to stiff, high thermal conductivity and TCE-compatible substrate materials. The reason for the relatively good power-cycling fatigue properties for the leadless chip carrier package used in this study is due to the rigid, cooler side walls of the JEDEC-type B leadless chip carriers. These rigid, cooler walls constrain the chip

carrier from expanding, thus concentrating most of the strain in the ceramic package rather than the solder joints. The large thermal gradient that exists between these side walls and the chip carrier cavity also limits the amount of power that can be dissipated by the active device. In thermal analyses using the chip carrier model illustrated in Fig. 2, a thermal resistance of approximately $16^{\circ}\text{C}/\text{W}$ was calculated for the 68-pin chip carrier, assuming heat conduction through the soldered leads only. This thermal resistance value increases when larger chip carrier packages are used despite the increased number of package leads. Thus, because of the increased width of the larger packages (to accommodate the additional leads) and the reduced

amounts of power that can be dissipated in the package, power-cycling effects for these larger chip carriers would be reduced.

The experiment investigating the effect of soldered lead geometry on the resistance to power-cycling fatigue indicates that increased life can be attained by fabricating solder joints with large fillets and small standoff heights. FEM studies indicate that large fillet geometries reduce chip carrier/substrate warpage and thus help to limit harmful tensile strains from reducing fatigue life. This large fillet geometry significantly reduces harmful stress concentrations while increasing the net cross-sectional area within the joint. Both of these factors tend to improve the fracture toughness of the joint.

Results from the power-cycling test for chip carrier solder joints dramatically demonstrate the effects of both temperature and frequency on the fatigue life of soldered interconnections. The dependence on frequency observed in these studies can be minimized by eliminating harmful tensile strain components. Reducing tensile strains is probably the most effective technique for reducing the effects of temperature and frequency in low cycle solder fatigue. Experimental studies on SnPb solder alloys indicate that harmful stress relaxation can occur much more rapidly during tensile strain holds than during compressive strain holds. In addition, oxygen embrittlement of grain boundaries predominating during tensile dwell periods can prevent partial rewelding during the compressive portion of the fatigue cycle. Thus, reducing the tensile strains can reduce the dependence of fatigue cracking on temperature and frequency while retarding crack propagation.

5.2 TEMPERATURE-CYCLING EFFECTS ON CHIP CARRIER PACKAGES

Results from torque shear tests performed on 20-pin chip carrier specimens soldered to Pt-Au thick film bonding pads indicated no effect on torque strength for 5-mil standoff samples, yet produced reductions of approximately 15% for both 2-mil and 10-mil standoff specimens. Microscopic examination of these samples indicated no signs of fatigue cracking; however, evidence of significant additional intermetallic formation at the thick film interface was observed. The fillet angle for these joints was slightly less than 45°, and the bonding pads were partially covered with a dielectric overlay that acted as a solder dam. Both of these techniques are valuable methods for preventing pad lifting. The results indicate that the 5-mil high joint produced no deterioration in interface shear strength

while providing a sufficiently high standoff to facilitate flux removal. FEM stress analysis also suggests that pillar-style solder joints with a truncated spherical geometry, such as those found in controlled collapse interconnections, tend to concentrate shear strains at the interface near the edges of the bond. Stress concentration factors of 2.5 to 3.0 were found for the pillar-shaped rectangular solder joint depicted in Fig. 14.

Analysis of standard chip carrier solder joint geometries suggests that long solder pads are preferable to shorter ones and that slightly elevated standoffs are preferred to lower ones. The longer bonding pad permits the fabrication of a solder joint with a low fillet angle while allowing a joint sufficiently high to facilitate flux removal after soldering. Also, as indicated in power-cycling experiments, increasing the fillet volume will increase the resistance of the joint to power-cycling fatigue.

5.3 TAPERING SOLDER JOINTS TO ELIMINATE STRESS CONCENTRATIONS

For cases where solder joints are attached to flexible or low-modulus substrate materials, solder joint tapering has been shown to improve the overall fatigue characteristics of the interconnection.²⁸ However, many of these low-modulus substrates have TCEs that are incompatible with assemblies using large leadless ceramic packages. In most of these cases, tapering will provide only a small increase in the fracture toughness of the joint through the elimination of stress concentrations. Further increases can be attained only through the increase of the cross-sectional area of the solder joint. In addition, the elimination of tensile strains introduced by substrate warpage will further extend the fatigue characteristics of the solder joint.

5.4 SOLDER BALL SHEAR TESTING

The results from both theoretical and experimental data on the use of the solder ball shear testing method were favorable. Both the ease of implementation and the consistency of test results were encouraging. Future applications will consist of

1. A test of solderability of thick film conductors from various vendors,

²⁸W. M. Sherry and J. S. Frich, "Analytical and Experimental Analysis of LCCC Solder Joint Fatigue Life," *Proc. 1985 Electronics Components Conference*, pp. 81-90 (1985).

2. A test of adhesion for qualifying solder processing control parameters,
3. A test to quantify the effect of thermal cycling and thermal shock on the integrity of the bond interface,
4. A test to compare FEM-estimated shear force on the solder/bonding pad interface resulting from temperature-cycling with solder ball shear forces after extended thermal shock or temperature-cycle testing.

5.5 FEM TECHNIQUE TO ESTIMATE FATIGUE LIFE

In previous sections, the use of finite-element analysis techniques in fatigue-resistant solder joint design and in the estimation of shear strains in power-cycled LCCC packages has been discussed. The method has been shown to qualitatively predict thermally induced stress concentrations for various geometrical solder joint configurations. However, insufficient data on the physical properties of the various material systems of interest for surface mount applications make accurate determination of fatigue and other processes dif-

ficult at this time. Empirical results for many metal systems indicate that low-cycle fatigue life depends on the amount of plastic flow per strain cycle. Accurate predictions of fatigue life require that time-dependent processes be completely defined. In addition, processes such as corrosion and diffusion can further complicate a reasonably accurate formulation of the problem. Before such time as the finite-element method can yield reasonably accurate quantitative solutions for interconnection reliability problems, a large effort must be undertaken to provide the physical constants and functional relationships necessary to characterize the thermal stress problem.

While the FEM technique cannot predict fatigue life, thermomechanical stress analysis can indicate the regions where failure is likely to occur. Also, estimation of differential thermal expansion can indicate whether worst-case strain levels (assuming complete stress relaxation) will exceed those recommended for reliable operation. This valuable information can assist the electronics packaging engineer in the development of packages, interconnections, and substrate assemblies that will further reduce or eliminate potentially harmful thermal stress concentrations.

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