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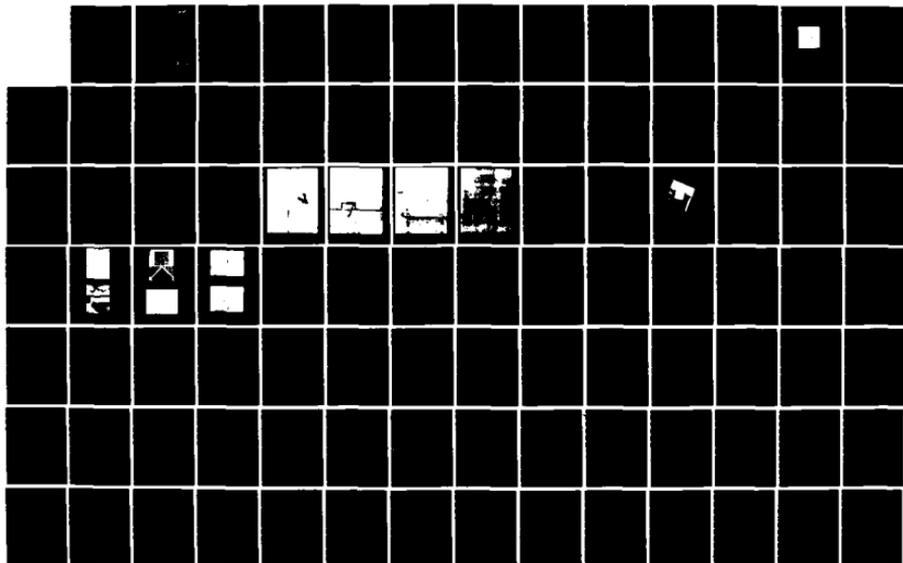
DEVELOPMENT OF SHORT GATE FET'S(U) HOWARD UNIV
WASHINGTON DC SOLID STATE LAB M G SPENCER ET AL.
JUL 84 AFOSR-TR-84-0033 AFOSR-81-0223

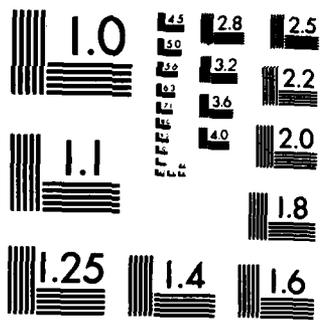
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**Development of Short Gate FET's
Final Report
Contract No. AFOSR-81-0223**

July 1984

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Summary

The goal of this work was to investigate the performance limitations of the "standard" GaAs FET structure. During the contract period we have constructed an AsCl₃ epitaxial system used to provide buffer layers for our FET structures, we have developed a submicron lithographic processes using deep U.V. techniques and, employing these techniques we have produced working .5 micron gate devices. In addition, we have investigated the "gettering" of substrates as a technique to improve the mobility of ion implantated layers. The result of this experiment showed was a correlation between improved hall mobilities and gettered substrates. Finally, a investigation of a self aligned source drain structure has commenced and several theoretical studies are reported.

Materials Development

In section A, we will report on the progress in development of a AsCl_3 system for the production of high quality buffer & active layers for our microwave devices. It is anticipated that the AsCl_3 material will provide thick buffer layers for isolating the substrate effects while growth technologies such as MBE will provide the thin critical active regions. Part B of this section concentrates on our gettering experiments on GaAs substrates for direct ion implantation applications while, part C reports on the status and capabilities of our recently acquired MBE system.

Introduction

We report here the status of our redesigned halide transport VPE reactor and results obtained to date. This effort parallels construction of a pyrolytic CVD reactor now completed.

As previously mentioned, GaAs FET performance shows a great dependence on submicron doping thickening products, background impurities and substrate properties. The system is designed to grow thick (greater than 10 micron) high-resistivity buffer layers which isolates our FET devices from substrate related problems.

The achievement of high resistivity buffer layers has been well demonstrated in the literature to require use of the well known "mole fraction effect" first described by Dilorenzo and Moore in 1971. A two bubbler systems similar to that of Cox and Dilorenzo (1971) is adapted, but with certain changes and simplifications.

VPE System Technology

A systematic outline of our system as originally designed is shown in figure (1). It was at first intended to demonstrate high-purity and reasonable process control with a simple reactor design. Systems improvements were later added as they proved necessary.

The original design was a teflon plumbing system using a continuous hydrogen purge to avoid adding reactor bypass valves as a possible source of contamination. The use of teflon is intended to minimize the presence of any metallic impurities, as well as decrease the "memory effect" of any system reagents. This teflon plumbing and buffer valves still seem to be a useful system feature and were retained in use.

The first growths utilized AsCl_3 obtained in pre-packaged plug-in bubblers from Apache Chemicals, Inc. These AsCl_3 bubblers were designed to plug into solid-state temperature controllers also manufactured by Apache chemicals, Inc. This was deemed to be a valuable feature which would minimize toxic hazards associated with loading the CVD system with AsCl_3 . We

Flow Schematic of GaAs Vapor Phase Epitaxial Reactor System

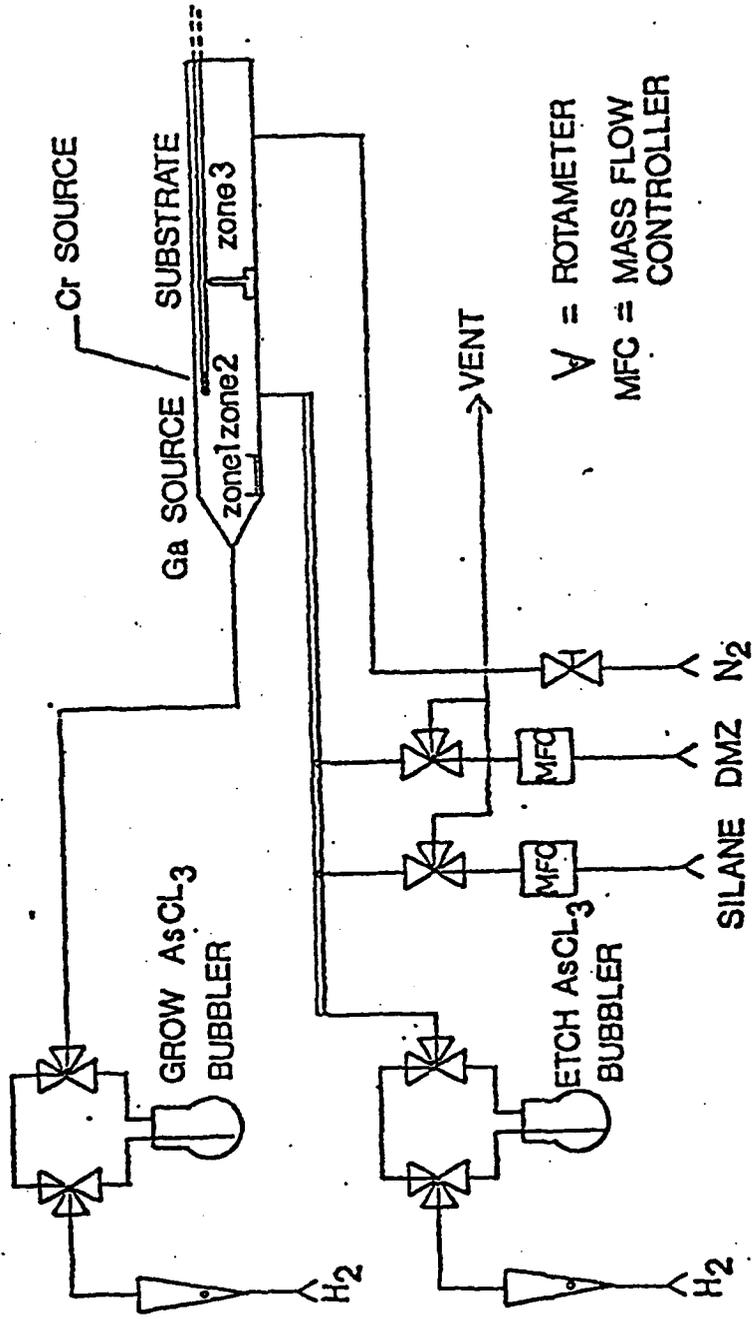


Figure 1

experienced many hardware problems with these temperature controllers. After being sent several updated versions, we have only this year obtained models which work as prescribed.

To check the reactor kinetics 45 grams of liquid Gallium as source material was loaded. We then attempted source saturation at 820°C and observed the saturation time and other characteristics. We found it necessary to add a source baffle to increase source saturation efficiency. Growth parameters of liquid source runs 3 thru 6 are shown in Table I.

The source boat was later loaded with approximately 40 grams of crushed GaAs as a solid phase source. Solid sources have been found to offer better thickness control, without the troublesome source saturation/etch cycle of liquid sources. Better surface morphology is also observed.

Initially we used as source material the upper "cone" portion of Bridgeman process semi-insulating GaAs crystals provided by Cominco, Inc. This solid source material was used in growths under a variety of reactor temperatures, carrier gas flows, and bubbler temperatures shown in Table I, runs 7 thru 21. Over certain parameter ranges good morphology and thickness control were obtained. Certain growth and hardware problems were encountered which we attacked with several design changes.

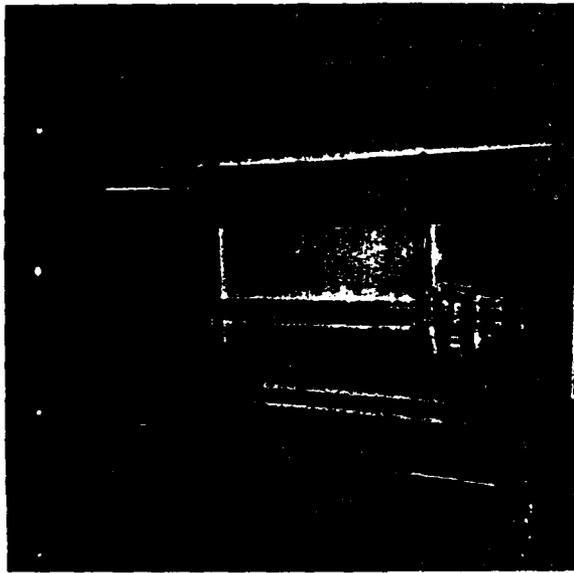


Figure 2

We decided to reduce the normal buildup of reaction by products at the exit end of the reactor tube by use of a hydrogen counterflow system. This build up could produce particle contamination. Several endcap designs were tried in which the substrate holder, dump tube and endcap were fused into one quartz containment assembly as shown in figure (2). The solid-source was changed to sealed-vessel synthesized GaAs dices supplied by Morgan Semiconductor for the runs remaining runs after run #20. This high purity source material gave only a superficial improvement in the electrical characteristics. Subsequently we were able to eliminate the solid source as a cause of the extrinsic compensation since no source, temperature or other growth parameter dependence was observed.

While at this point the faulty temperature controllers were still being used, it was suspected that the AsCl_3 itself was contaminated and causing the epilayers to become heavily compensated.

The AsCl_3 was returned in the plug-in bubblers to the manufacturer for analysis. Flame spectrochemical analysis revealed approximately 50ppm Fe, 20ppm Si and a few ppm traces of Mg and other elements. The source Fe levels are very consistent with the electrical characteristics observed in the epilayers.

Fe backgrounds generally in the 10^{-8} mole fraction range will yield high resistivity layers with mobilities of approximately 1000-2000 $\text{cm}^2 \text{V}^{-1} \text{Sec}^{-1}$. We tentatively concluded, therefore, that our low mobilities and high resistivities were caused by unintentional incorporation of bubbler Fe due to contaminated AsCl_3 .

System Modifications

To alleviate the above difficulties we have made changes in our source materials and process. The most important of these by far is the use of good quality AsCl_3 obtained from other domestic manufacturers.⁴ We will fill our plug-in bubblers with the pure AsCl_3 demonstrated in the field as having the requisite purity.⁵ This change alone is expected to solve most of the compensation problem.

The reactor tube itself has been modified extensively. At the inlet side a vacuum chamber thermally isolates the inlet tubes from the source region. This aids greatly in reducing any premature thermal decomposition of main or bypass injection line reagents. As already shown in figure (2), the substrate holder, dump tube and endcap were fused into one assembly for maximum leakage integrity. Not shown is the new flat O-ring joints which

Run No.	Sample No.	F_M (cc/M)	F_B (cc/M)	Pannel P (PSI)	Counter Flow F_C (cc/M)	Source	T_M ($^{\circ}C$)	T_B ($^{\circ}C$)	Prebake time (min)	Etch time (min) τ_e	Growth time (min) τ_G	Thickness d μm	Growth rate R_g $\mu m/min$	Source Temp T_S	Sub Tem T_p	Break down Voltage (Y) V_B	Mobility $\mu_{77^{\circ}K}$ M300	N300	
3	T1	330 15	100 15	Ga	max at 15		20	10	30	19	15	18	1.2	820	760	10	-	-	No morphology picture, thickness is questionable
4	T5	"	330 15	"	"	19.4	18.6	"	"	"	"	3	0.2	"	"	N/O	-	-	N/O = No breakdown observed
5	T6	"	"	"	"	19.3	10	"	17	"	"	"	"	"	"	400	-	-	Pyramid Growth Hall sample was not effected by the magnetic field
6	T7	"	"	"	"	19	10	"	19	"	"	N/O	-	"	"	N/O	-	-	fair morphology, slow growth rate
7	T8	"	"	solid	"	"	15	"	2	60	4	4	"	"	"	"	-	-	
8	T9	420	"	"	"	"	"	"	"	90	"	no growth	-	"	"	"	-	-	morphology bad, hall sample were not ohmic
9	T10	280	"	"	"	"	"	"	"	"	4	4	"	"	"	"	-	-	
10	T11	"	"	"	"	15	"	"	"	90	15	15	"	"	"	25	-	-	
11	T12	330	330	"	"	20	14	45	11	60	"	"	"	"	"	"	-	-	poor morphology
12	T15	"	400	"	"	20	15	"	"	"	"	14-20	"	830	745	50	-	-	hillocks growth, black non uniform growth
13	T16	"	"	"	"	"	"	"	5	"	14	14	"	830	740	100	-	-	fairly clean surface except for black spots which could be due to etch, uniform growth

Run No.	Sample No.	F_M (cc/M)	F_B (cc/M)	Source	Counter Flow F_C	Pannel P PSI	T_M °C	T_B °C	Prebake time (min)	Etch time (min) t_e	Growth time (min) t_G	Thickness d μm	Growth rate R_g $\mu m/min$	Source Temp T_S	Sub Temp T_D	Breakdown Voltage (Y) V_B	Mobility u77°K M300	N300	
14	T20	330	330	solid max at 15	one	20	15	60	10	5	60	7.5-10	830	710	70	-	-	-	poor morphology compared to T15 black spots got more non uniform growth
15	T23	"	"	"	both	"	"	"	5	"	"	12	"	725	100	"	"	"	fairly clean surface, some part looks peeling off uniform growth
16	T24	"	"	"	"	"	"	"	"	"	"	17.5	"	730	30	"	"	"	change of the solid source surface morphology improved, has black spots uniform growth
17	T25	330 15	400 15	GaAs max at 15 psi	"	"	"	"	"	"	55	12	"	"	"	32-110	"	"	poor morphology, blackspots uniform growth
18	T17	"	"	"	"	"	13	2	60	8	24-66	"	"	"	"	"	"	"	poor morphology worse than T25, high density of black spots. Uniform growth
19	T26	"	330	"	"	"	15	"	"	9	22-120	"	830	"	"	"	"	"	"
20	T21	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	layer is bad did not look at morphology & thickness
21	T28	"	"	"	"	"	"	"	"	"	12.5	"	"	"	24	"	"	"	good morphology, uniform growth double layer feature
22	T29	"	"	"	"	18	"	"	"	"	"	10	"	"	30-60	"	"	"	good surface, uniform growth no double layer feature
23	T30	"	"	"	"	16	"	"	"	"	"	11	"	"	20-120	"	"	"	part of the layer is foggy, dumptube were saturate with deposit around sub area uniform growth
24	T35	"	"	"	1888 20	16	"	"	"	"	"	10	"	"	5-12	"	"	"	partly foggy, uniform growth hillocks growth

Run No.	Sample No.	F _M	F _B (cc/M)	Source	Counter flow F _C	Pannel P PSI	T _M °C	T _B °C	Prebake time (min)	Etch time (min) τ _E	Growth time (min) τ _G	Thickness d v	Growth rate R _G v	Source Temp T _S	Sub Temp T _D	Breakdown Voltage (Y) V _B	Mobility μ 77°K M ₃₀₀	
24	T31	330 15	330	GaAs	2888 20	16	15	60	2	60	9	830	730	5-100				partly foggy, uniform growth, hillocks growth
25	T32	"	"	"	186 20	15	"	"	"	"	10	"	"	"	"	10-180		lower part is cleaner, back dots in the upper part good morphology, uniform growth
25	T33	"	"	"	"	"	"	"	"	"	10	"	"	"	"	60-190		" "
26	T34-2	"	"	"	1838 20	"	"	"	"	"	120	27.5	"	"	"	30-60		good morphology
27	C1-1	"	"	"	1848 20	"	"	"	"	"	"	19	"	"	"	26-65		hillocks growth, uniform growth 15 black spots
28	C2-2	"	"	"	185 20	12	"	"	"	90	14.5	"	"	"	"	42-100	1277, 1823	" "
29	M1-3	"	"	330 solid 15 GaAs	1858 20	10	"	"	"	"	12.5	"	"	"	"	4-10	N ₃₀₀ =1.2x10 ¹⁷	morphology is very good, no hillocks or pyramid uniform growth, bad crystal quality
30	T28-4	"	"	"	180 20	15	"	"	30	-	etch= all	"	"	"	"	-		poor morphology, all the layer etched
31	M1-5	"	"	"	"	"	10	"	20	-	etch 9	"	"	"	"	-		poor morphology 9.5 detach 10 at same part mostly the layer we attached

Run No.	Sample No.	F_M (cc/M)	F_B (cc/M)	Source	Counter flow F_C	Pannel P PSI	T_M °C	T_B °C	Prebake time (min)	Etch time (min)	Growth time (min)	Thickness d (μ m)	Growth rate R_g μ m/min	Source Temp T_S	Sub Temp T_D	Breakdown Voltage (Y) V_B	Mobility $\mu_{77^\circ K}$ M_{300}	N300
32	M1-6	320	290	solid GaAs	$\frac{185}{20}$		15	10	60	15	--	detch ~ 9.5	830	730	4-10			poor morphology, etch=9.5 μ m non uniform etch
33	T35-7	330	270	"	$\frac{183}{20}$		"	"	"	10	"	no uni- form etch	"	"	"	"		Morphology improved compare to M1-6 but not over all layer, non uniform etch
34	T29-8	"	250	"	$\frac{182}{20}$		"	"	"	30	"	$d_e > 9$	"	"	"	"		morphology improved more, non uni- form etch
35	T33-9	325	210	"	$\frac{181}{20}$		"	"	"	15	"	d_e ~ 8.5	"	"	"	"		good morphology, not uniform regrowth
36	T32-10	335	220	"	"		"	"	"	"	"	d_e ~ 6.5	"	"	20-70	"		good morphology, uniform etch, regrowth
37	M2-11	330	"	"	$\frac{180}{20}$		"	"	"	"	90	12.5	"	"	60	"		good morphology; uniform growth
38	M3-12	"	220	"	$\frac{182.5}{20}$	both	15	10	"	"	120	13	"	"	"	"	"	"
39	M4-13	"	220	"	$\frac{181}{20}$	"	"	"	"	"	"	no growth	"	"	"	"		increasing F_B after etch from 220 cc/M to 580cc/M, no growth, some etch
40	M5-14	"	"	"	$\frac{181}{20}$	"	"	"	"	"	90	2-4	"	"	"	"		F_B was increased to 480 cc/M right after etch, non uniform, at some part no growth
41	M7-1	"	"	"	$\frac{182}{20}$	"	0	10	"	"	120	"	"	"	"	"		"

will replace the taper joints used so far.

Up until now rotameters were used for main and bypass hydrogen gas metering in an initial attempt to keep costs low. These have been replaced by electronic mass flow controllers which will give superior accuracy.

The original plan to use Fe or Cr solid-phase doping for the high resistivity buffer layer has been scrapped in favor of more promising methods. Combinations of the mole fraction effect and addition of oxygen during growth have been observed to suppress incorporation of background impurities ^{6,7}. This oxygen gettering occurs without the memory effect caused by contamination of the tube when heavy metals are introduced as hi-resistivity dopants. There is also evidence of deep oxygen donors further serving to reduce the free carrier concentration. We will study other methods of introducing oxygen into the system, e.g., using CO₂ gas, without adversely affecting the mobility of the epitaxial active layers.

Summary

We conclude from the studies completed thus far that the more conventional designs for AsCl_3 , which our redesigned system more closely resembles, are best used for the growth of high purity GaAs buffer and active layers in conjunction with "clean" gettering techniques such as oxygen injection. Various oxygen compounds such as CO_2 and CO will allow better oxygen incorporation and at the same time introduce small quantities of deep carbon acceptors to more adequately compensate shallow Si donor and other acceptor levels. The mole fraction effect shows great promise in further dopant suppression when used in conjunction with the oxygen incorporation.

With this considerations taken into account we believe this modified approach is a much more fruitful method to reliably produce hi-quality epitaxial GaAs.

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7. I.S. Low et.al., op. cit.

B

Ion Implantation

Semi-insulating gallium arsenide grown by liquid encapsulated Czochralski (LEC) method has been plagued by a number of problems. For example, heating LEC substrates at typical annealing and growth temperatures (700-900°C) frequently produces a highly conductive thin layer near the surface. This phenomenon is usually accompanied by poor reproducibility of carrier concentrations, low mobilities, and photoluminescence changes. We have begun to study this and other problems related to GaAs substrates for direct ion implantation applications. A simple "gettering" technique that employs heat-treatments at 800° for 24 hours in flowing H₂ with an overpressure of As provided by InAs was used. An outline of our gettering experimental procedure is provided in table #2 on page 15 of this report.

Routine hall measurements were taken at room temperature and 77°K. The hall samples employed the standard Van der Pauw technique with clover-leaf shaped samples. Contacts to the specimen are made with tin beads alloyed to the leaves, which in turn provide edge contacts to the central part of the sample. For our purposes, the carrier concentration and the mobility are

Hall Mobility vs Substrate or Boule Number (300° K)

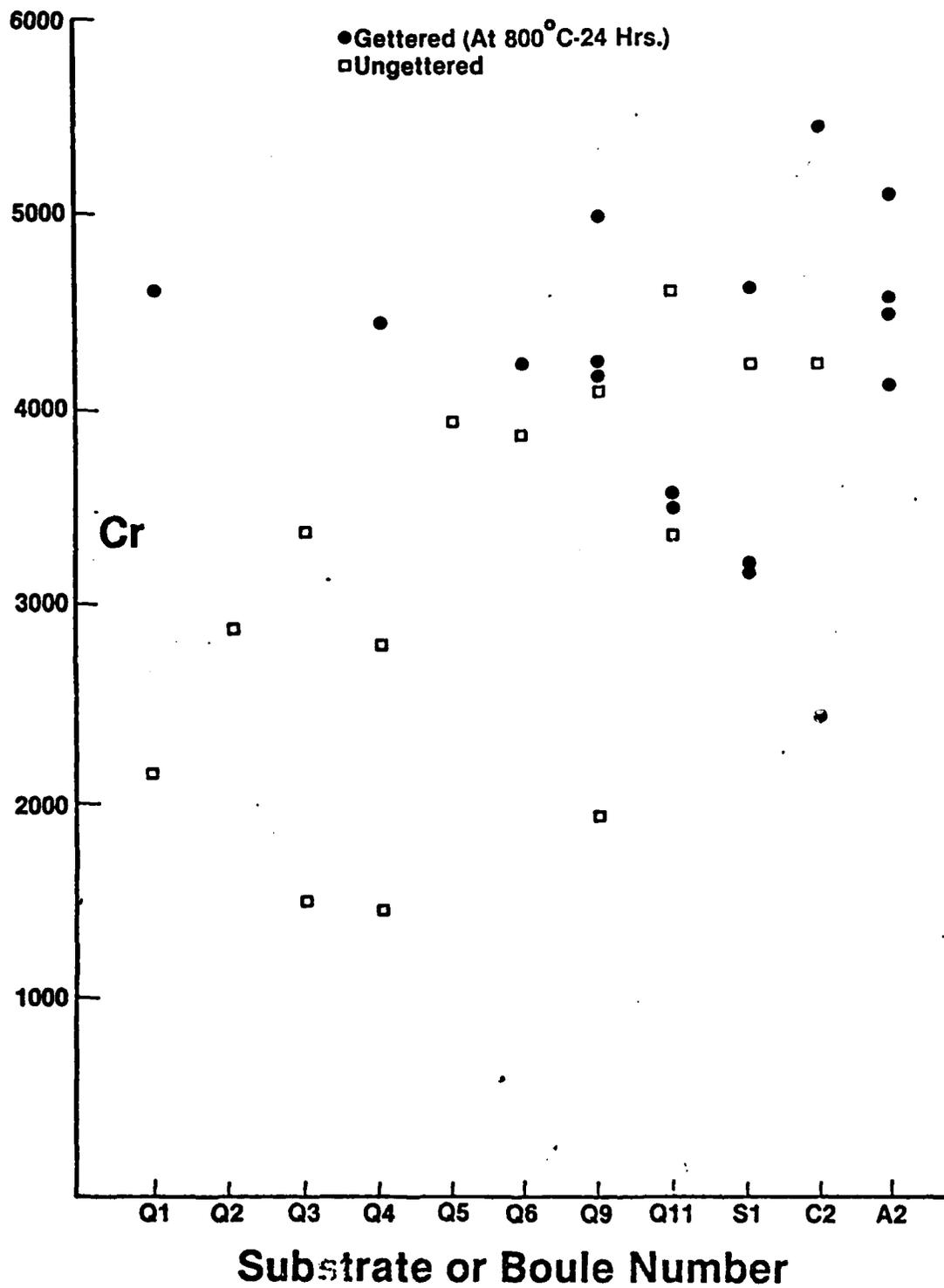


Figure 3a

Hall Mobility vs Substrate or Boule Number (77° K)

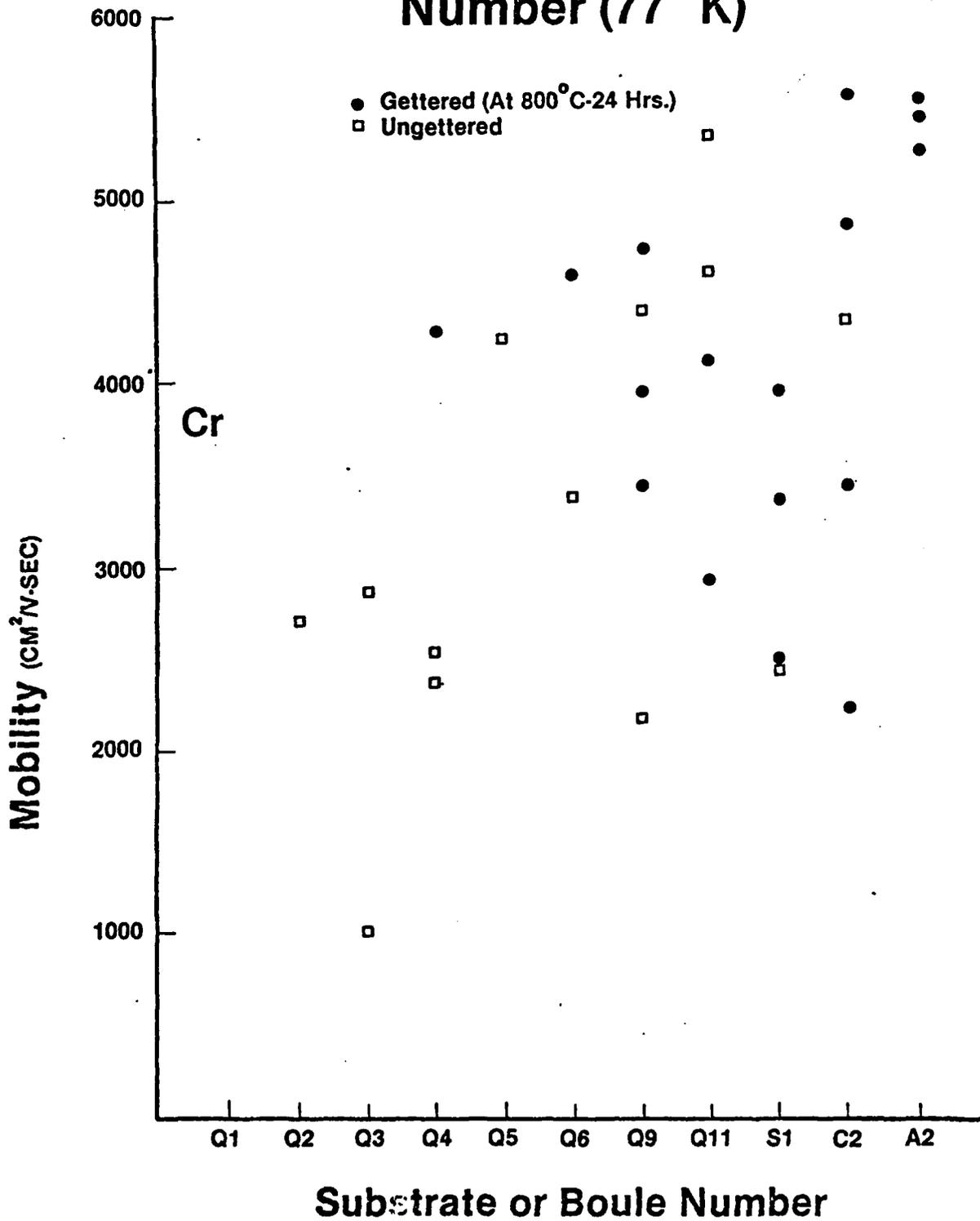


Figure 3b

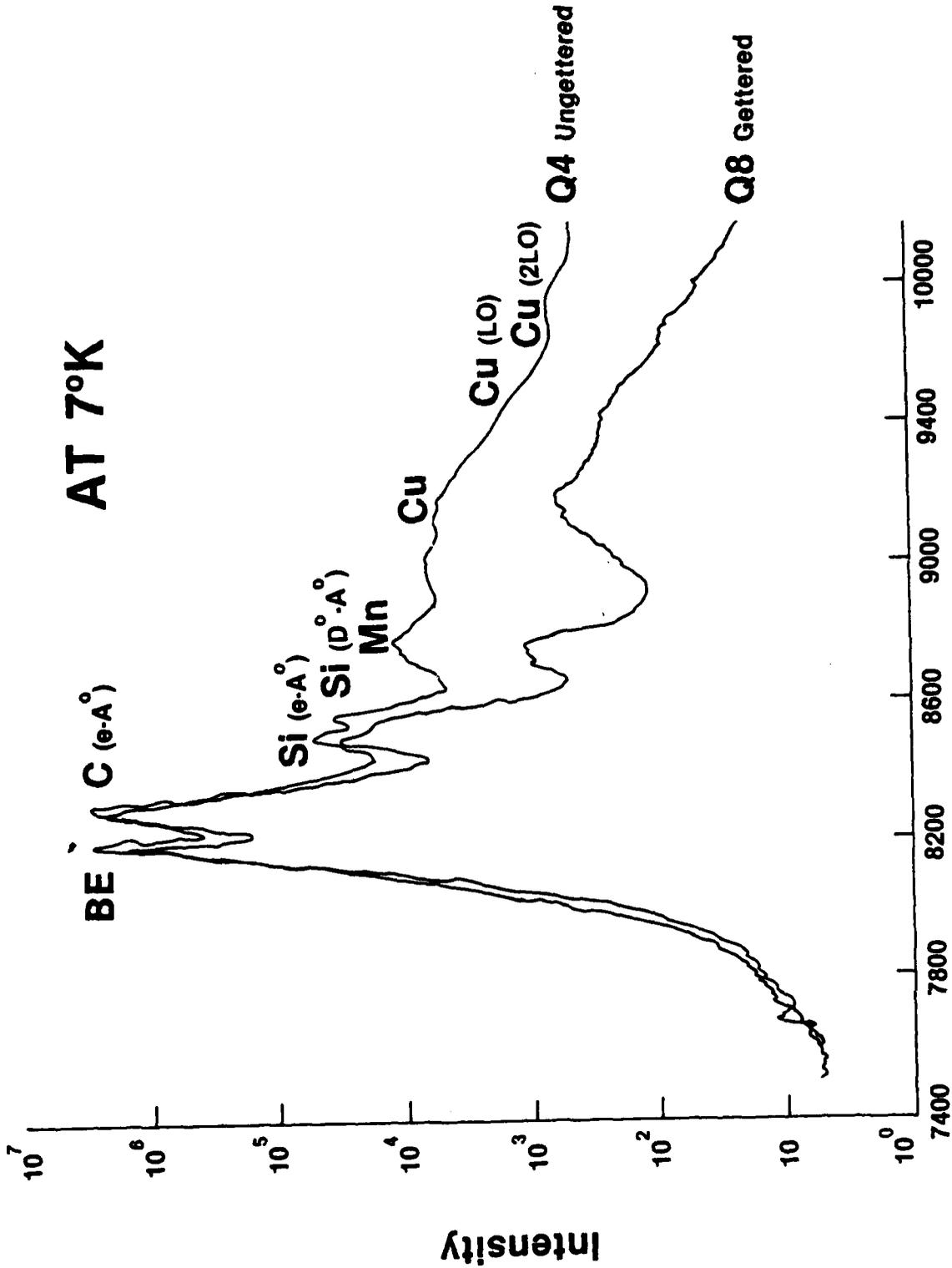
particular important values, and can be obtained from these measurements.

The heat treated or "gettered" implanted and annealed layers typically showed a higher room temperature and 77°K mobility. The improvement in mobility varies from wafer to wafer and is shown in the figures (3a) and (3b) of mobility vs substrate or boule number. For instance, Q9 showed at 35% improvement while Q11 showed no improvement. The wide range of data reveals the large differences in the substrate properties, residual impurities, and trap concentrations.

Standard photoluminescence spectra were also obtained for both the gettered and ungettered layers. The PL. was performed at 7°K using a Argon laser at a power level less than 100mw. The luminescence radiation was dispersed by a 3/4 meter grating monochromator and detected with a LN₂ cooled photomultiplier using phase-sensitive detection. The resulting PL spectra of the gettered samples exhibited a reduction in the Mn and Cu peak intensities. This result is illustrated in the PL spectrum of Q8 and Q4 (figure 4).

SIMS analysis experiments were performed on ungettered and gettered samples at Cornell University. The SIMS analysis

PL AT 7°K



Wavelength (\AA)

Figure 4

Depth Profile Q4 Ungettered

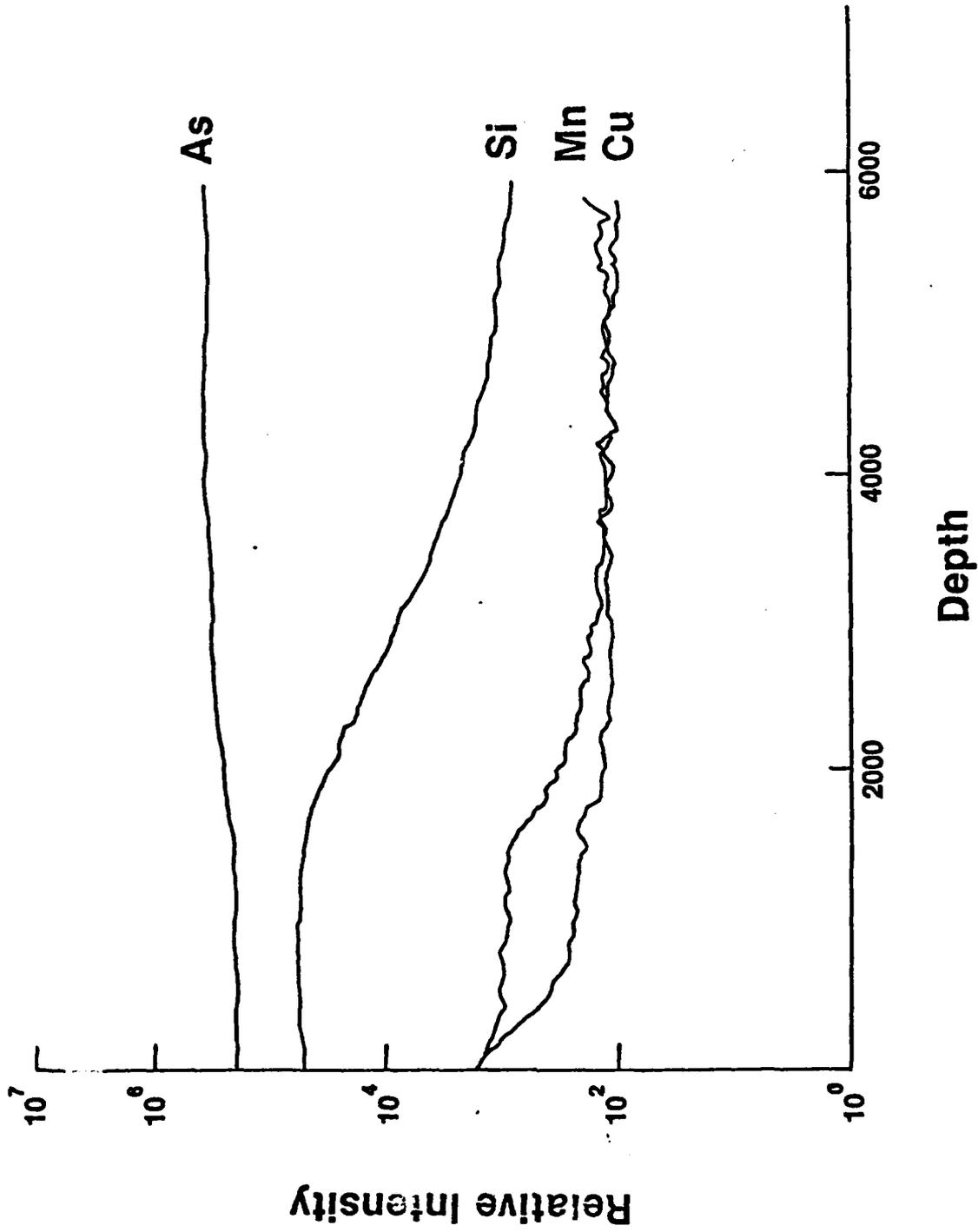


Figure 5

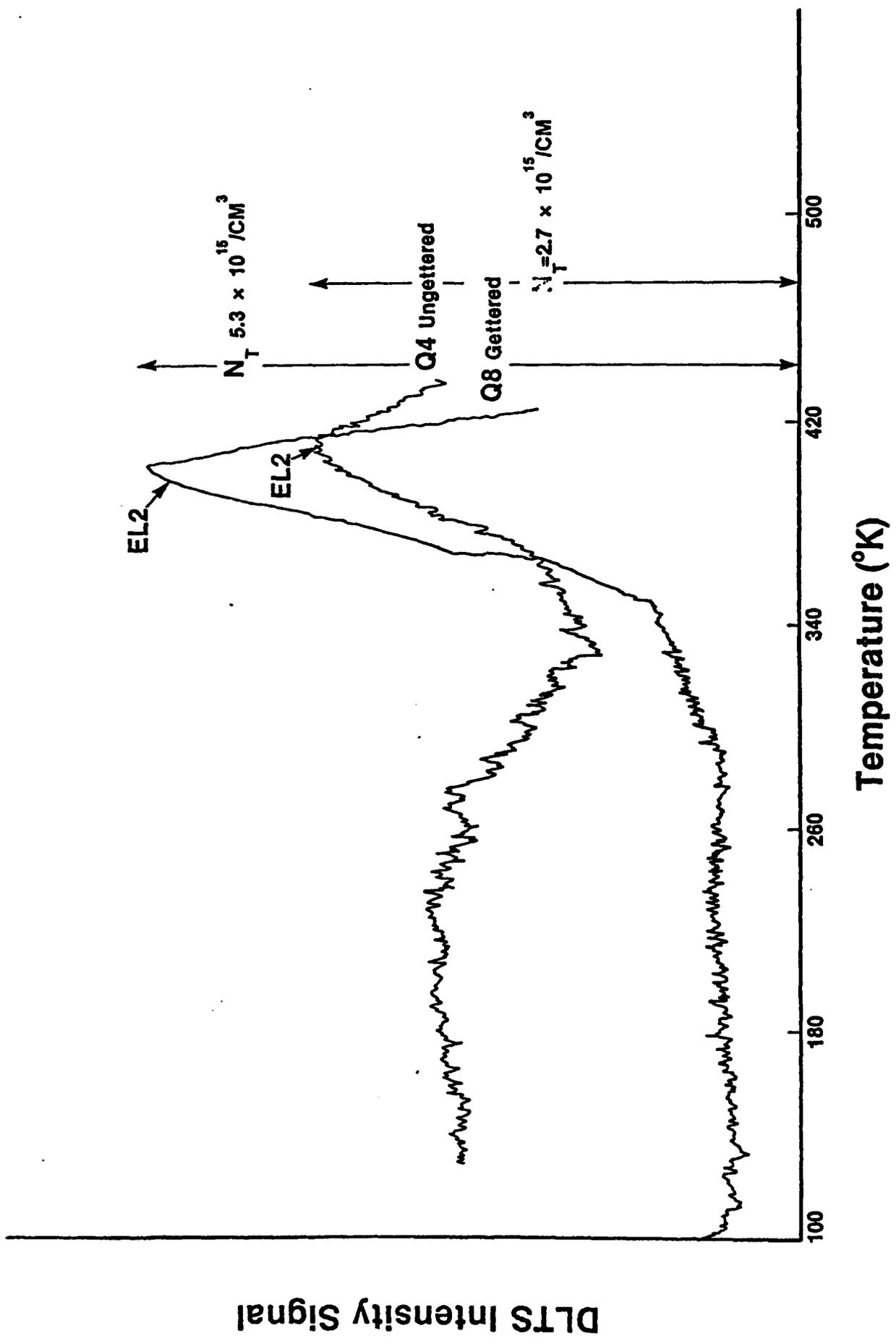


Figure 6

revealed the presence of several residual impurities. These impurities : Carbon, chromium, boron, manganese, copper and magnesium were clearly present in the 10^{14} - 10^{15} range. In addition, we observed outdiffusion for the substrate of copper, manganese, and magnesium. These results are shown in figure (5).

Electrically DLTS results figure (6) on schottky barriers diodes formed on the gettered and ungettered layers reveals an increase in the EL2 level and a reduction in the broad shallow peak. We believe that this broad peak is related to the presence of several residual impurities.

In summary, we have concluded from the studies completed that LEC substrates can be improved by heat treating. There are, however, a couple of precautions: 1) It is necessary to remove all of the gettered layer and, 2) provide an sufficient overpressure of As. This work was presented at the Electronic Materials Conference held at Santa Barbara.

GETTERING EXPERIMENTAL PROCEDURE

TABLE #2

POLISH SUBSTRATES

DIVIDE POLISHED SUBSTRATES INTO HALVES

BAKE ONE HALF OF THE SUBSTRATES AT
800° FOR 24 HOURS

POLISH BOTH SIDES OF THE GETTERED SUBSTRATES
(REMOVE 35 mm)

STANDARD CLEAN

IMPLANT

S_i^{29}	6.09×10^{11}	40 KV
	9.03×10^{11}	110 KV
	4.5×10^{12}	200 KV

ANNEAL AT 800°C FOR 30 MINUTES IN A CAPLESS ANNEALING SYSTEM WITH
FLOWING H_2

COMPARE ELECTRICAL PROPERTIES

C

Molecular Beam Epitaxy

We have a acquired and installed a MBE system. We anticipate that this system will be used to grow the critical layers for our FET structure. With MBE capabilities it will be possible to investigate normal GaAs FET's as well as the high electron mobility structures (HEMPT). We anticipate that we will be growing both single as well as multiple interface HEMPT devices. Our machine has the capability of growing on 2 inch substrates and we can load up to six wafers in a single pump down. We are presently baking out the furnaces in preparation for our first growth.



Figure 7
Calibration mark is one micron

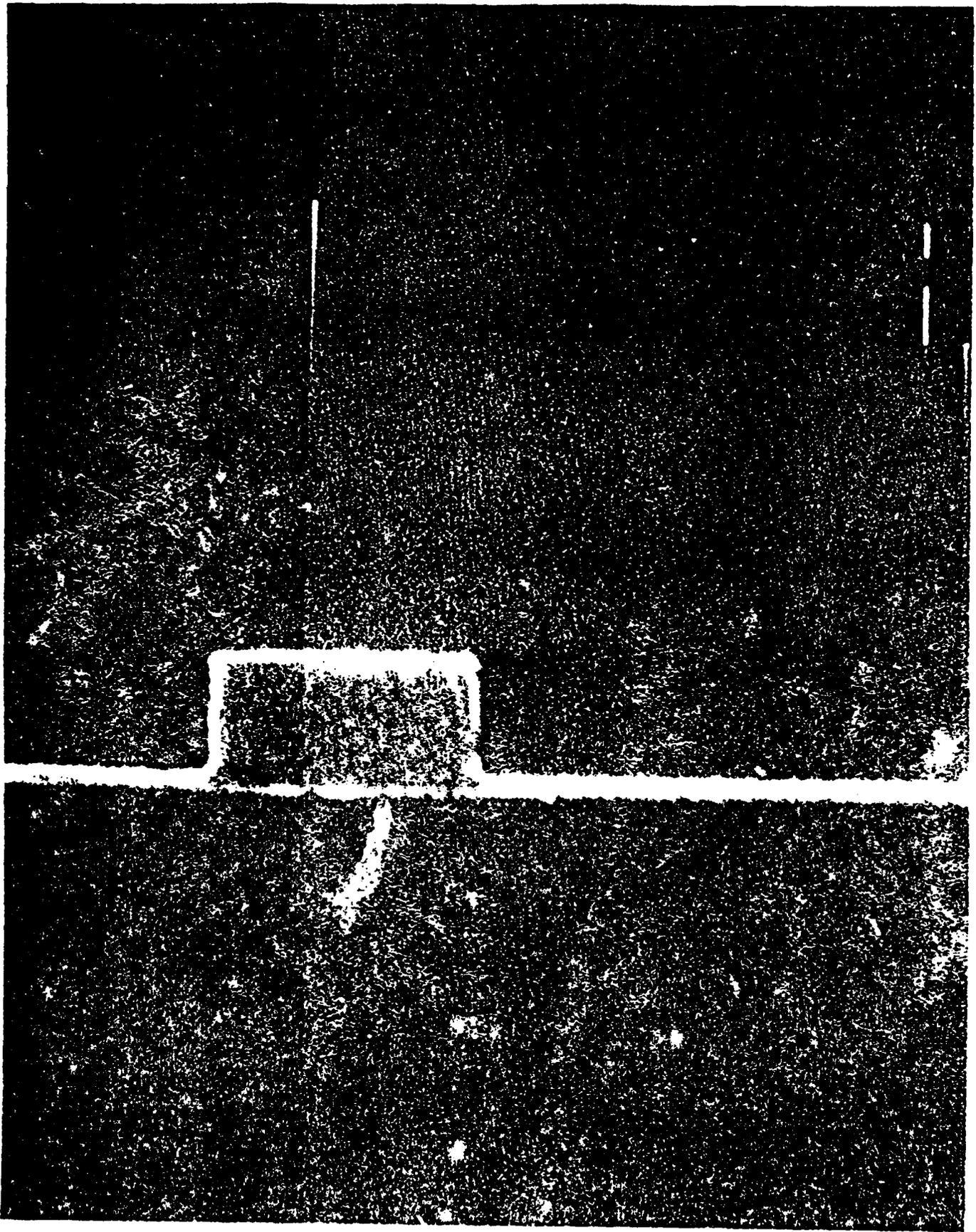


Figure 8
Calibration mark is one micron

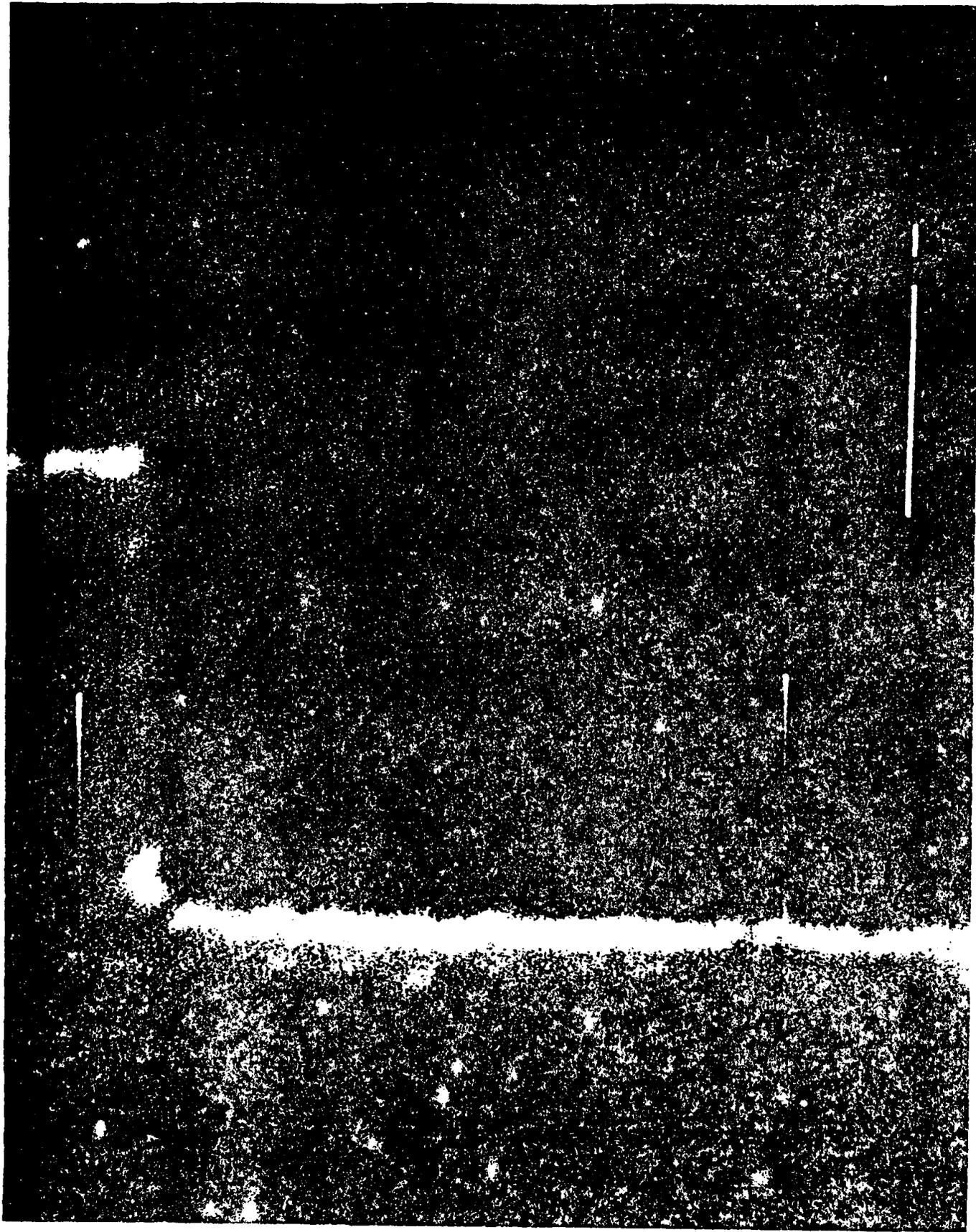


Figure 9
Calibration mark is one micron

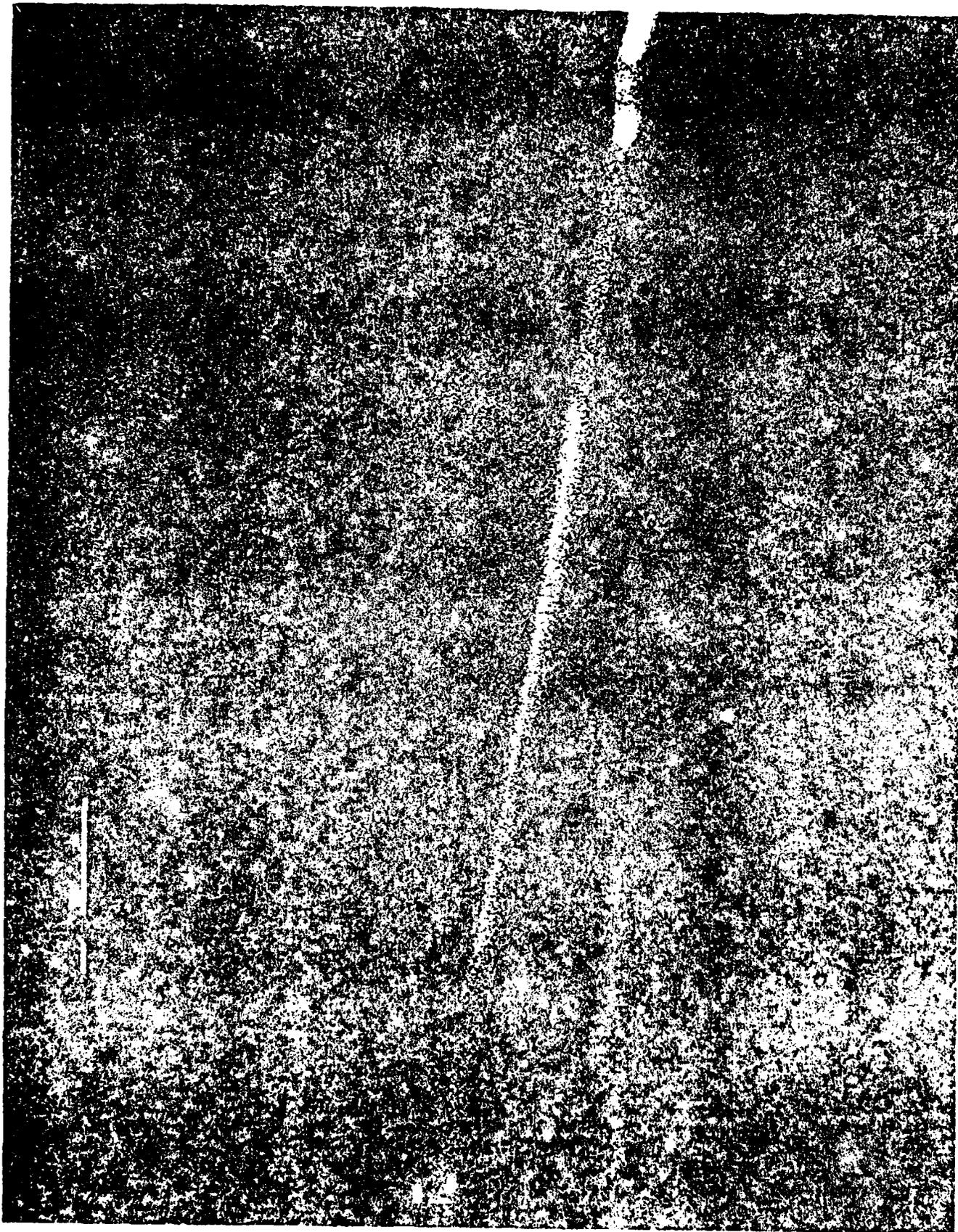


Figure 10
Calibration mark is one micron

Lithography

One of our principal problems during this work has been the development of our lithographic techniques. This section will summarize our efforts.

At the beginning of the contract a FET mask set and a test pattern were fabricated at the National Submicron Center located at Cornell University. The best results were obtained using a wet chemical etch. The smallest resolved features of the masks have linewidths of better than 0.25 microns. We then went through a period of considerable experimentation with the exposure and development parameters. Our final process consists of a two layer photoresist technique utilizing a co-polymer of PMMA and PMAA. The PMMA was used as the imaging resist and develops more slowly, the co-polymer was used to form a lift off lip similar to that shown in figure (7). Our final process is summarized in Table III. Examples of our better gate lift off are shown in figures (8),(9) and (10).

The key element that we found necessary to reproducibly form .5 micron lines was to obtain "good" conformal contact between the mask and the GaAs substrate. In order to ascertain

whether we are had contact a quartz plate was used. The substrate was observed through a quartz plate the same size as the mask. Figure (1) is representative of the type of contact we were able to obtain. On the areas where no fringes formed we observed a darken region which were the areas where we obtained good contact. We found excellent correlation between these contact areas and production of high quality lines. As indicated in Table III one of the process steps is dissolving the resist by using a O₂ plasma. For this process we have calibrated the etch rate in a barrel plasma reactor and this is illustrated in figure (12).

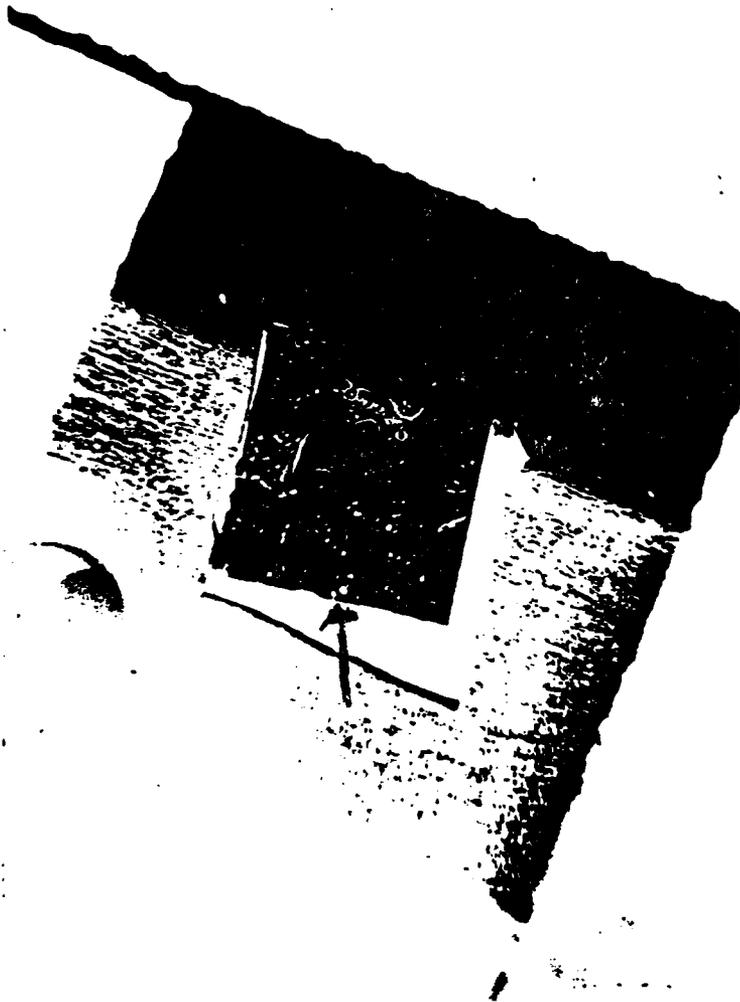


Figure 11

Arrow shows boundary between regions of different contact

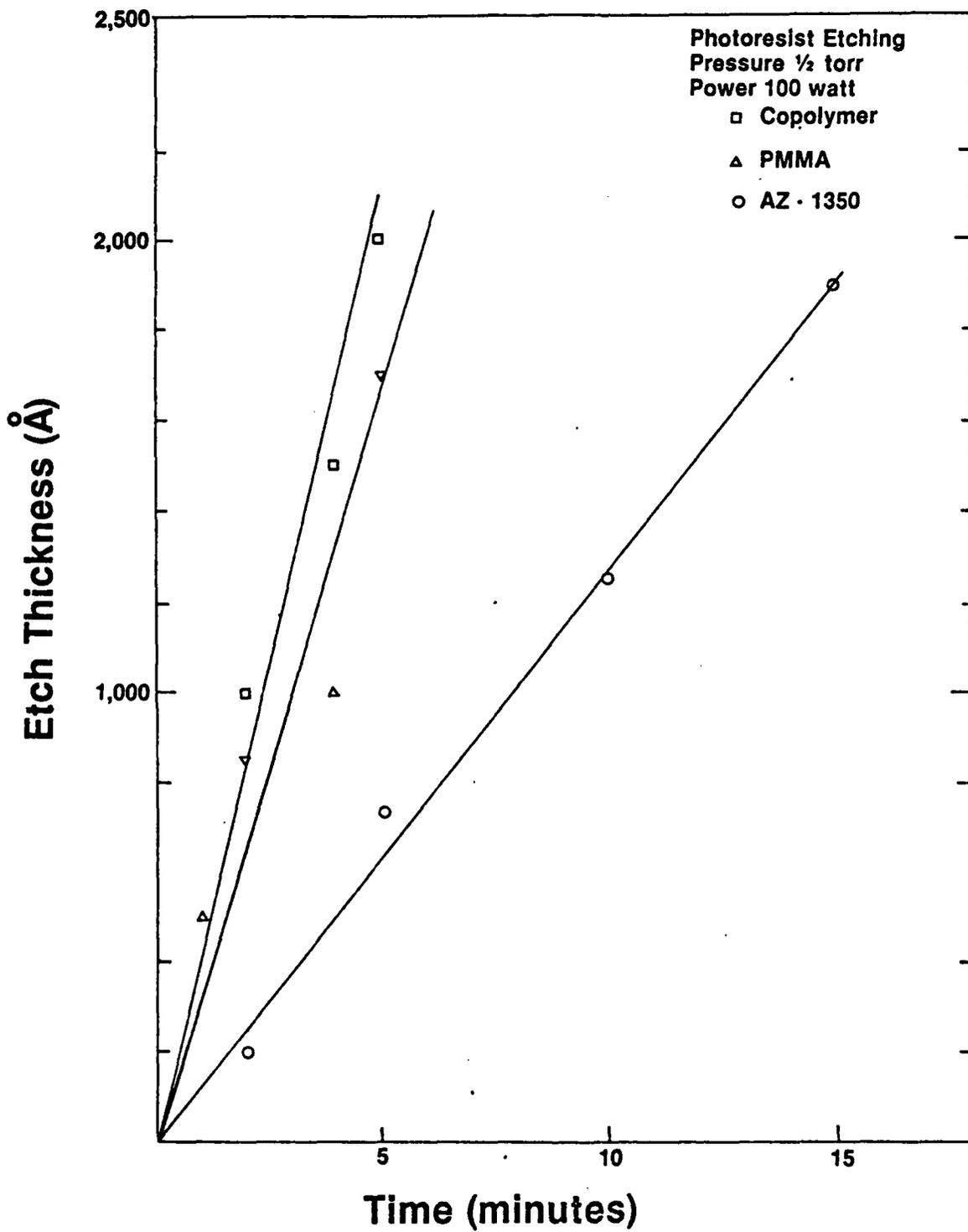


Figure 12

TABLE III

Process Summary for two layer photoresist

1. Cleaning and Degreasing
2. Bakeout in Air at 200°C for 30 min.
3. PMMA - PMMA Copolymer
is spun on at 5000Å thickness
4. Bakeout at 160°C for 45 min
5. 4% PMMA is spun at 3000Å thickness
6. Bakeout at 160°C for 60 min.
7. Wafer is placed under quartz plate to check confor
mal contact
8. Contact adjustment
9. Mask position checked and wafer exposed for 6 minutes at
a lamp intensity of 19.8mw/cm²

10. Sample is developed in solution of 2 parts Propanol 1
part Toluene

11. Oxygen Plasma Clean-up 1 minute at 100 watts a 1/2 torr
pressure

12. Sample is now ready for metallization

Device Structure and Results

In this section, we will summarize our device results. Since as mentioned in a previous section our vapor systems were not fully operational all of devices results are on ion implanted material. This material was baked out in order to attempt to getter residual impurities.

Our first submicron structure attempted to illustrate our lithography technology using a self aligned Ti/Al gate. In this structure the gate was deposited first and the source and drain were aligned around the gate. This structure was alloyed with the gate in place. We found it necessary to deposit a minimum of 2000 Å of Ti, to provide adequate protection during our source/drain alloying process. In the future, we intend to experiment with Pt as a barrier metal. Using this fabrication sequence we have fabricated working devices. Data and pictures for representative devices are shown in Table IV and figures (13), (14), and (15) respectively. We observed some problems with edge effects on the ohmic contact metalization layers. We believe these problems can be corrected by the addition of nickel to the metalization system.

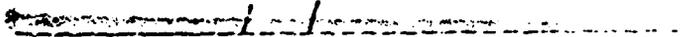
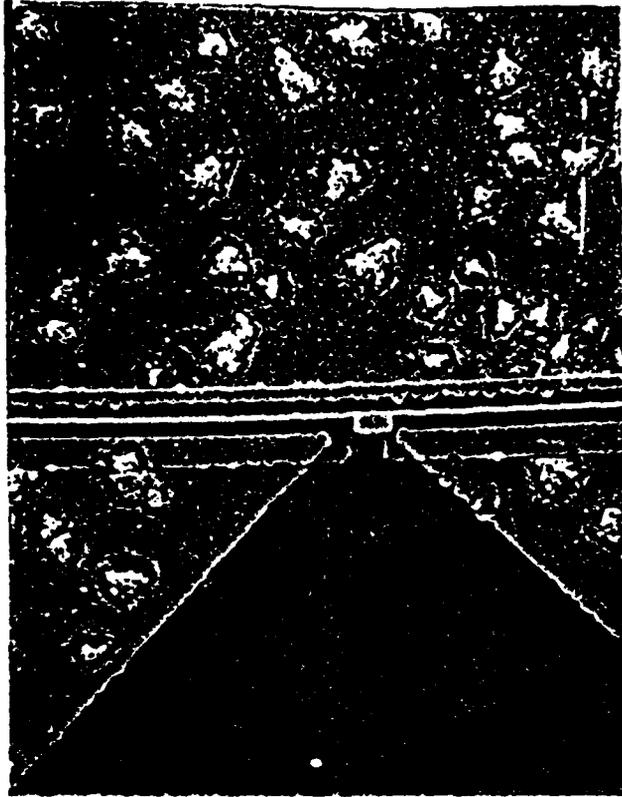


Figure 13

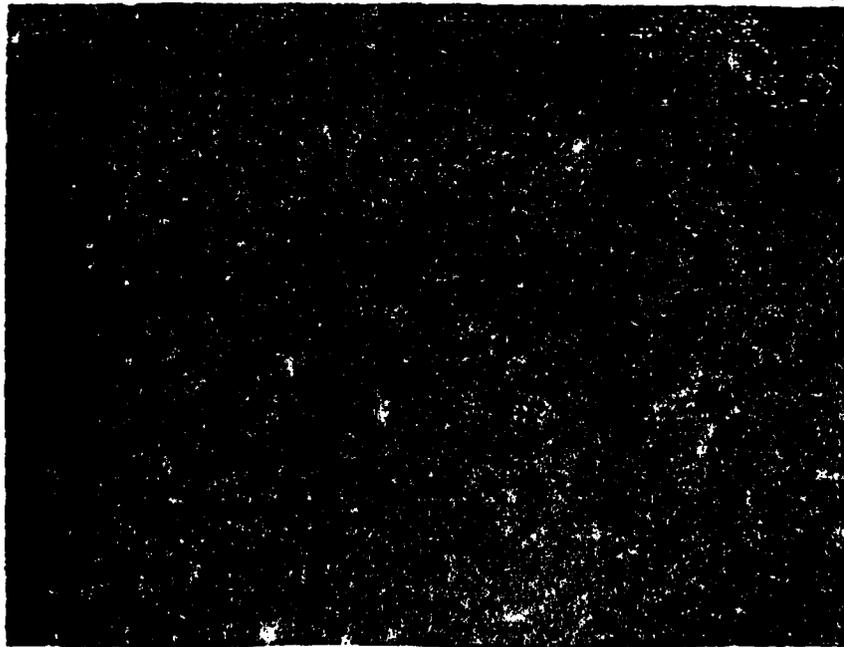
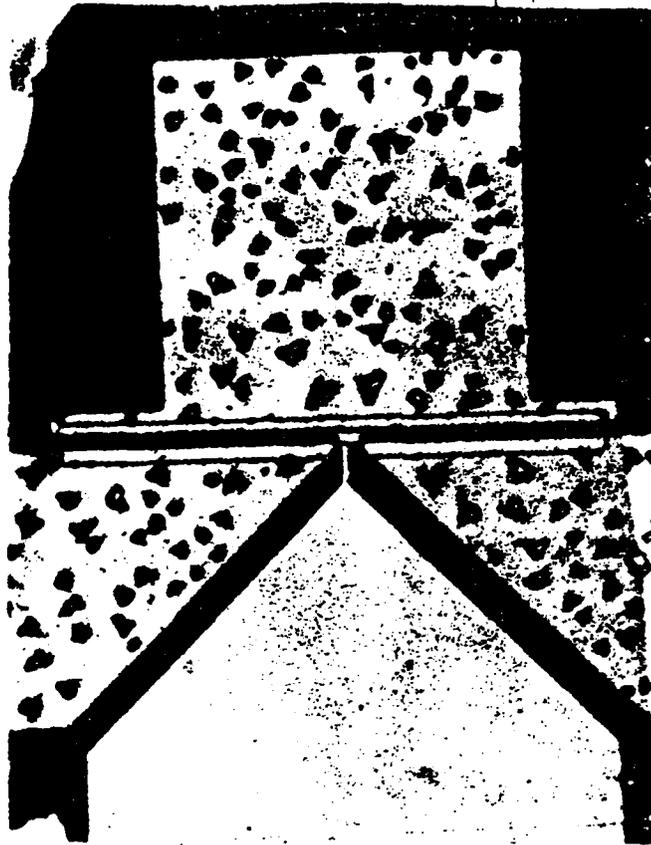


Figure 14

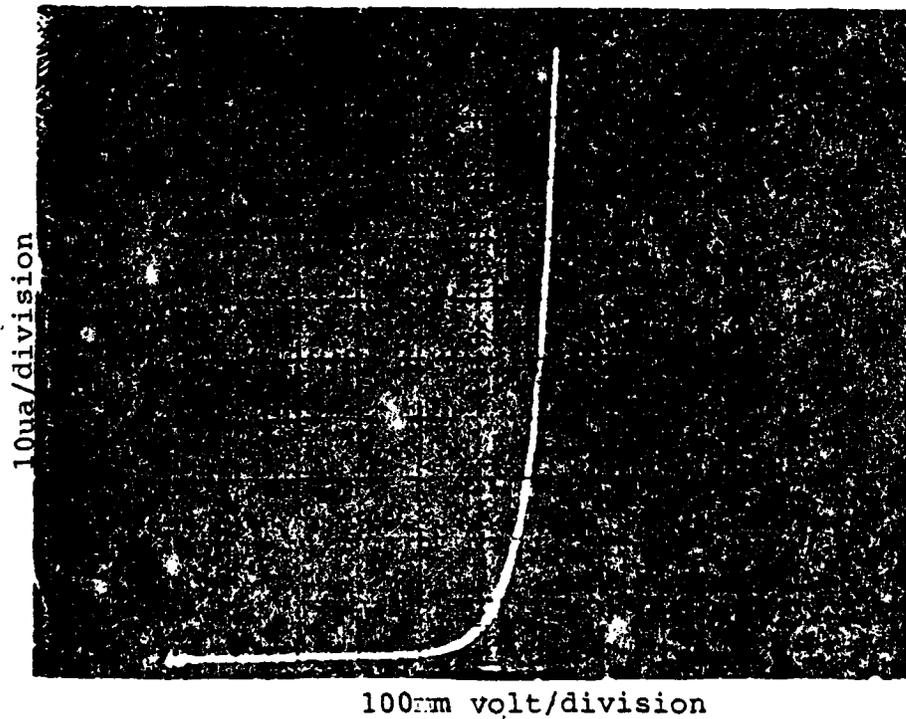
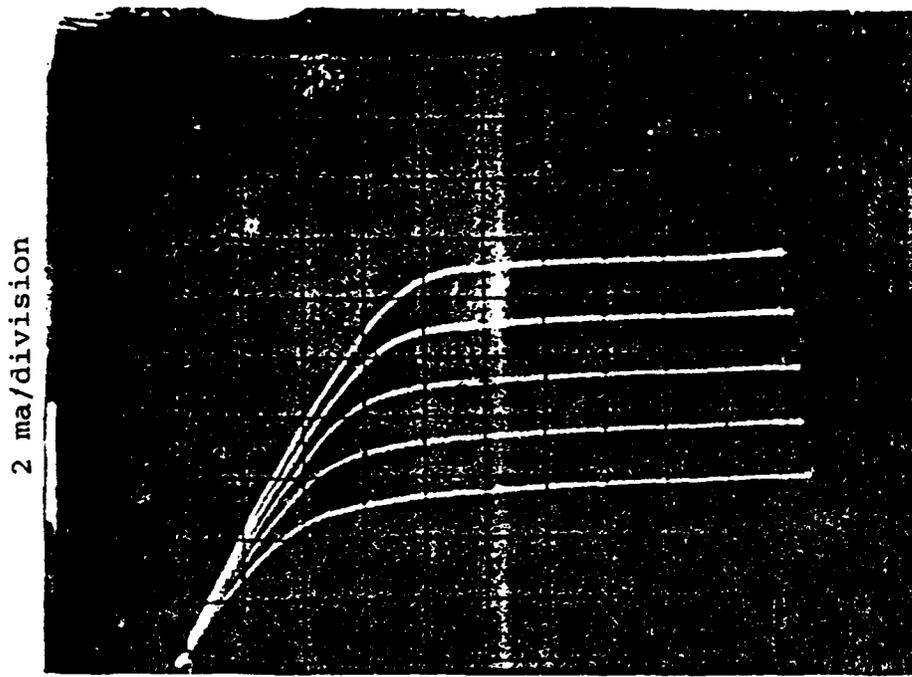


Figure 15
I-V characteristics of .5 micron FET (top)
I-V characteristics of gate of FET (bottom)

After demonstrating working devices we proceeded to develop a standard process for our short gate FET experiments. In this structure again the gate is deposited first then a "T" structure is formed by selectively etching the Ti in a CF_4 plasma. This is followed by a blanked evaporation of Au-Ge.

The source drain regions are then defined making this structure a self aligned gate as well as self aligned source drain structure. We anticipate that this structure should lower the parasitic resistance in the source region enough to enable isolation of the effects of gate length on device performance.

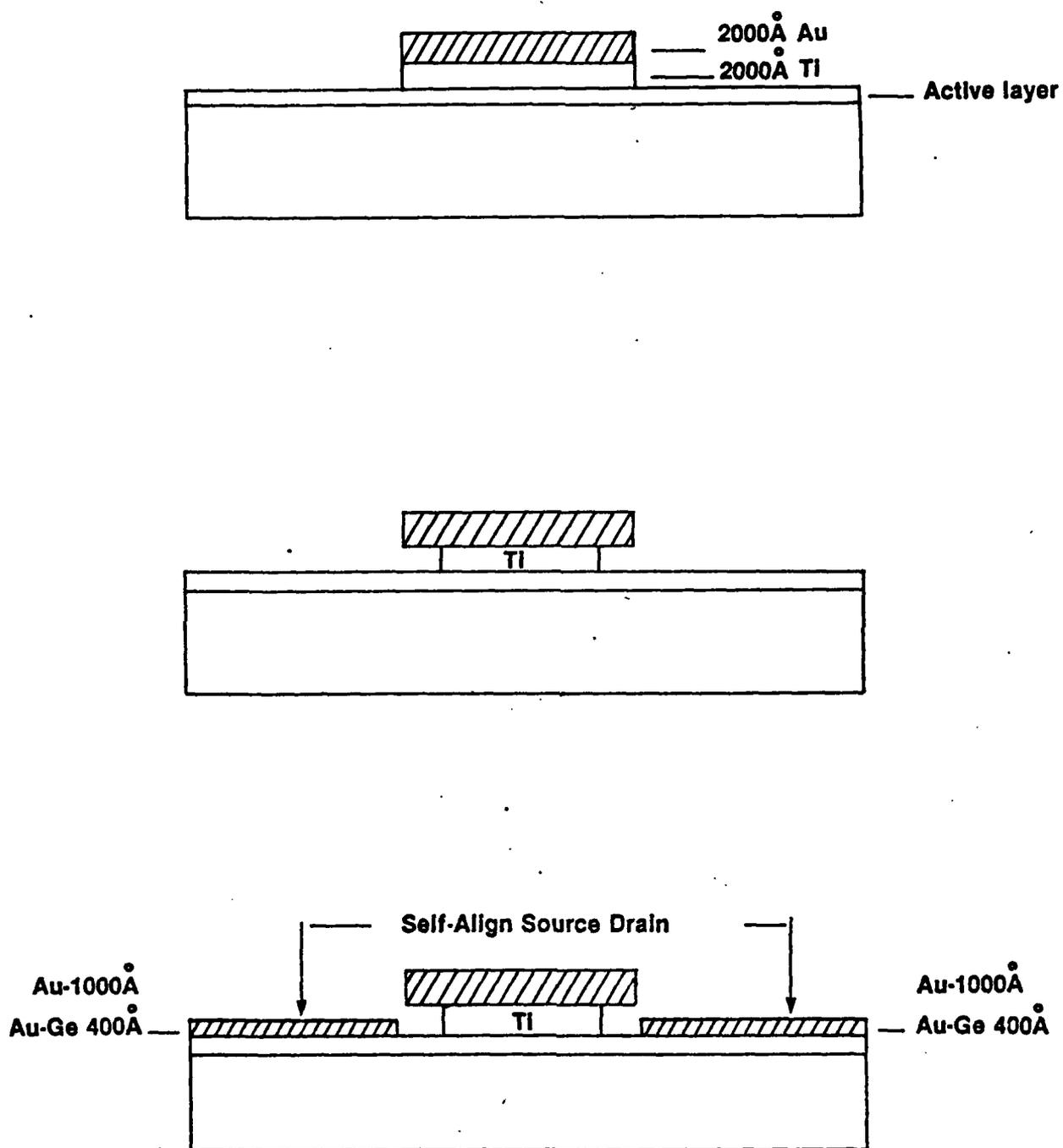


Figure 16

Table IV

D.C. Characteristics of representative .5 micron Fet's

Gate ideality factor	1.34
Built in gate barrier	.783ev
Source resistance	68 ohms
Drain resistance	42 ohms
Pinch off voltage	3.76 volts
Transconductance	73.2 mseeimens

Theoretical Studies

We have investigated several areas related to FET device performance. The details of these investigations appear in the following papers.

A CONTRIBUTION
" LEAKAGE EFFECTS IN n-GaAs
MESFET
WITH n-GaAs BUFFER LAYER "

BY

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Abstract

Whereas improvement of the interface between the active layer and the buffer layer has been demonstrated, the leakage effects can be important if the buffer layer resistivity is not sufficiently high and/or the buffer layer thickness is not sufficiently small. We find two buffer leakage currents exist from the channel under the gate to the source and from drain to the channel in addition to the buffer leakage resistance between drain and source. It is shown that for $1\ \mu$ gate-length n-GaAs MESFET if the buffer layer resistivity ρ is $12\ \Omega\text{-cm}$ and the buffer layer thickness h is $2\ \mu$, the performance of the device degrades drastically. We suggest that h should be below $2\ \mu$.

I. Introduction

The main advantage of using a buffer layer in n-GaAs MESFET is that the interface between the active layer and substrate can be improved. However, since the buffer layer placed between the active layer and the substrate has thickness of several microns and resistivity much higher than that of the active layer and lower than that of the substrate, leakage currents may flow from and to the active layer through the buffer layer due to its lower resistivity. The leakage effects on device parameters and in particular on device performance will be examined in this work.

In previous works dealing with leakage in a semi-infinite substrate (Liechti, 1976 and Reiser, 1973) the model of the leakage current was considered simply as a leakage resistance between the source and drain. Whereas this simple model is useful for explaining the effect of the leakage resistance on the I-V characteristics, a more detailed model is desirable. In this work we have considered the leakage problem of a finitely thick buffer layer and made detailed calculations which enable us to present a better model. In addition to the drain-to-source leakage resistance, the channel-to-source and drain-to-channel leakage currents are included in our model. Furthermore we have considered in our model, the varying channel potential which is of importance for short gate FET.

In order to simplify the calculation, we have neglected the possible effects of interface trapping and the space charge. Also we assume that the diffusion current from the active layer to the buffer layer is negligible and that the transverse field in the channel is much smaller than the longitudinal field so that the voltage along y-direction (transverse direction) can be considered to be the

same across the channel. This implies that the voltage on the channel-gate interface is the same as that on the channel-buffer layer interface under the gate. Thus a virtual gate electrode(see Fig. 1) can be assumed to exist along the interface between the active and buffer layer. In addition it is assumed that the gate-drain and gate-source spacing are negligibly small. Based upon these assumptions it is therefore possible to deal with merely a static field problem in the buffer layer. Along the interface between the buffer layer and S.I. substrate, no leakage is assumed to exist, i.e. the substrate is assumed to be a perfect insulator. Leakage occurs only in the buffer layer and its interface with the active layer.

By solving the field problem with the help of conformal mapping we can calculate the buffer leakage resistance r_{dsb} and the two leakage current sources I'_{GS} and I'_{DG} on using superposition principle for current on the three electrodes(Sec. II). With this model in mind we derive the equivalent circuit including the leakage effect from which the h-parameters for the device with and without buffer layer can be determined. The performance parameters such as gains and F_{MAX} can be obtained and compared for MESFET's with and without buffer layer(Sec. III). Numerical results and conclusions are presented in sections IV and V, respectively.

II. Analysis of Leakage Elements

We will derive the leakage elements, i.e., leakage resistance and the leakage current sources, by solving two-dimensional Laplace equation for potential distribution in the buffer layer with appropriate boundary conditions set on the interface between the active and buffer layers. In Fig.1, S' and D' are the virtual source and drain electrodes and G' is the virtual gate electrode on which the voltage varies along x-direction due to voltage variation in the channel. Since the field solution associated with Fig.1 with finite buffer layer thickness h is difficult, we will use conformal mapping three times to transform this original structure (A) to the parallel plate structure (c) as shown in Fig.2-c from which the field and potential can easily be obtained.

As shown in Fig.2-a (structure A) S', G' and D' are the virtual source, gate and drain, respectively where source and drain are extended into infinity along $\pm x$ and the buffer layer has a finite thickness h. Structure A can be conformally mapped into structure B' (Overmeyer, 1970) with the transformed dimensions given by

$$a_2 \approx b_2 = \frac{\pi}{2h} \tanh\left(\frac{\pi a_1}{2h}\right) \quad (1)$$

$$c_2 = \frac{\pi}{2h} \quad (2)$$

where a_1 is one half of the given gate length. A further transformation gives structure B with new dimensions as given by

$$\frac{c_2}{a_2} = \frac{1}{p} \quad (3)$$

or

$$p = \frac{a_2}{c_2} = \tanh\left(\frac{\pi a_1}{2h}\right) \quad (4)$$

From structure B the final parallel-plate structure (c) is obtained again by using conformal mapping (Okoro, 1980). From structure c we have

$$L=2K(p) \quad (\text{gate length}) \quad (5)$$

$$T=K'(p) \quad (\text{buffer layer thickness}) \quad (6)$$

where $K(p)$ and $K'(p)$ are the elliptical integral of the first kind and p is given in (4).

When bias voltages are applied to the gate and drain, the channel potential will vary along the longitudinal direction (from S' to D'). As a result of conformal mapping the field variation is preserved in the various structures. The virtual gate potential distribution in the original structure (structure A) can be approximated by two linear regions based on the model of Pucel, 1975 (see also Wang, 1979) as shown in Fig. 3 where $V_0(0)=0$, $V_0(\alpha)=V_p$ and $V_0(2a_1)=V_{DS}$ where V_p and V_{DS} are the pinch-off and drain to source potentials, respectively, α is the position of pinch-off point and $2a_1$ is the total given gate length. The virtual gate potential distribution on structure C can be transformed from Fig. 3 into Fig. 4 by requiring that the source, pinch-off and drain voltages remain invariant, i.e. $V_0(0)=0$, $V_0(\alpha')=V_p$ and $V_0(2K(p))=V_{DS}$ where $L=2K(p)$ is the length of the parallel-plate structure (C). In region I of Fig. 3 we have

$$V_0(x)=m_1x \quad 0 \leq x < \alpha \quad (7)$$

where $m_1=V_p/\alpha$ and in region I of Fig. 4 we have

$$V_0(x)=m_1'x \quad 0 \leq x < \alpha' \quad (8)$$

where $m_1'=V_p/\alpha'$. But

$$\frac{\alpha}{2a_1} = \frac{\alpha'}{2K(p)} \quad (9)$$

from which m_1' can be obtained and is given by

$$m_1' = \frac{V_p}{\frac{K(p)}{a_1} \alpha} \quad (10)$$

Similarly in region II of Fig.3 we obtaine

$$V_0(x) = m_2(x - \alpha) + V_p \quad \alpha \leq x \leq 2a_1 \quad (11)$$

where $m_2 = (V_{DS} - V_p) / (2a_1 - \alpha)$, and in region II of Fig.4 we obtain

$$V_0(x) = m_2'(x - \alpha') + V_p \quad \alpha' \leq x \leq 2K(p) \quad (12)$$

where

$$m_2' = m_2 \frac{2a_1 - \alpha}{2K(p) - \alpha'} \quad (13)$$

The parameters for the two linear-region approximation of gate potential distribution are summarized in table 1.

Here we will make use of superposition principle by which we will block one of the three electrodes, i.e., source, gate, or drain, at a time and calculate the leakage element so that the three leakage elements, i.e., r_{dsb} , I_{GS}' and I_{DG}' , can be determined from the final parallel-plate structure.

A. Leakage resistance r_{dsb}

Leakage resistance is defined as the resistance between source and drain when the gate electrode is blocked, i.e., there is no current flow on the gate or $(\partial V / \partial y)|_{y=T} = 0$ as shown Fig.5. Therefore, the structure reduces to a parallel-plate structure in which the leakage resistance between drain and source is given by

$$r_{dsb} = \rho \frac{2K(p)}{A} \quad (14)$$

where ρ is the resistivity of the buffer layer, $2K(p)$ is the distance between drain and source and A is the cross-sectional area which is given by

$$A = K'(p)z \quad (15)$$

where z is the width of the structure (in z direction). Thus the leakage resistance r_{dsb} in (14) becomes

$$r_{dsb} = \frac{\rho}{z} \frac{2K(p)}{K'(p)} \quad (16)$$

B. Leakage currents

Leakage between the gate and source, and between the drain and gate are modelled as two leakage sources I'_{GS} and I'_{DG} , instead of two resistors, because on the gate, the voltage varies along x -direction and therefore uniform leakage resistances can not be defined. On using the superposition principle I'_{GS} is obtained by calculating the voltage distribution in the structure C with the drain electrode being blocked, and I'_{DG} is obtained with source blocked.

(i). Source-to-gate leakage current I'_{GS}

The structure C when the drain is blocked is shown in Fig.6. Note that there is no leakage between the buffer and the S-I substrate. The general eigen solution of Laplace equation as applied to Fig.6 is given by

$$V_n(x,y) = \left[A_n \cosh(\alpha_n y) + B_n \sinh(\alpha_n y) \right] \left[C_n \cos(\alpha_n x) + D_n \sin(\alpha_n x) \right] \quad (17)$$

Using the boundary conditions shown in Fig.6, i.e.,

$$V_n(x,y) \Big|_{x=0} = 0 \quad (18)$$

$$\left. \frac{\partial V_n(x,y)}{\partial y} \right|_{y=0} = 0 \quad (19)$$

$$\left. \frac{\partial V_n(x,y)}{\partial x} \right|_{x=2K(p)} = 0 \quad (20)$$

$$V_n(x,y) \Big|_{y=K'(p)} = V_0(x) \quad (21)$$

where $V_0(x)$ is the channel and therefore the buffer layer potential. The potential distribution in the buffer layer can be obtained and is given by

$$V(x,y) = \frac{1}{K(p)} \sum_{n=\text{odd}} \frac{u_n}{\cosh\left[\frac{n\pi}{4} \frac{K'(p)}{K(p)}\right]} \sin \frac{n\pi x}{4K(p)} \cosh \frac{n\pi y}{4K(p)} \quad (22)$$

where

$$u_n = \int_0^{2K(p)} V_0(x) \sin \frac{n\pi x}{4K(p)} dx \quad (23)$$

or from Fig. 4

$$u_n = u_{nI} + u_{nII} = \int_0^{\alpha} V_0(x) \sin \frac{n\pi x}{4K(p)} dx + \int_{\alpha}^{2K(p)} V_0(x) \sin \frac{n\pi x}{4K(p)} dx \quad (24)$$

Substituting the appropriate values of $V_0(x)$ as shown in (8) and (12) into (24), we obtain

$$u_n = \left[\frac{4K(p)}{n\pi} \right]^2 m_2' \sin \frac{n\pi}{2} + \left[\frac{4K(p)}{n\pi} \right]^2 (m_1' - m_2') \sin \frac{n\pi \alpha'}{4K(p)} \quad (25)$$

The total leakage current I_{GS}' is given by

$$I_{GS}' = \frac{z}{\rho} \int_0^{K(p)} \left. \frac{\partial V(x,y)}{\partial x} \right|_{x=0} dy \quad (26)$$

where z is the width of the structure and ρ is the resistivity of the

buffer layer. On using (22), (25) and (26) the total leakage current from the gate to source can be obtained and is given by

$$I'_{GS} = \frac{z}{\mathcal{J}K(p)} \sum_{n=\text{odd}} u_n \tanh \left[\frac{n\pi}{4} \frac{K'(p)}{K(p)} \right] \quad (27)$$

(ii). Drain-to-gate leakage current I'_{DG} .

The structure C when source is blocked is shown in Fig.7. Fig.7-a shows the drain is biased at V_{DS} . This is equivalent to the situation as shown in Fig. 7-b from which a solution similar to that in the previous subsection can be obtained. Thus using boundary conditions as shown in Fig.7-b, we have

$$K(p) \cdot V(x,y) = \sum_{n=\text{odd}} \frac{u_n}{\cosh \left[\frac{n\pi}{4} \frac{K'(p)}{K(p)} \right]} \cos \frac{n\pi x}{4K(p)} \cos \frac{n\pi y}{4K(p)} \quad (28)$$

where u_n' is given by

$$u_n' = u_{nI}' + u_{nII}' = \int_0^{2K(p)} [V_0(x) - V_{DS}] \cos \frac{n\pi x}{4K(p)} dx \quad (29)$$

On using the appropriate values of $V_0(x)$ given in (8) and (12) in (29), we obtain

$$u_n' = \left[\frac{4K(p)}{n\pi} \right]^2 \left[(m_1' - m_2') \cos \frac{n\pi \alpha'}{4K(p)} - m_1' \right] \quad (30)$$

And the total drain to gate leakage current I'_{DG} is given by

$$I'_{DG} = \frac{z}{\mathcal{J}} \int_0^{K(p)} \left. - \frac{\partial V(x,y)}{\partial x} \right|_{x=2K(p)} dy \quad (31)$$

or

$$I'_{DG} = \frac{z}{K(p)} \sum_{n=\text{odd}} u_n' \sin \frac{n\pi}{2} \tanh \left[\frac{n\pi}{4} \frac{K'(p)}{K(p)} \right] \quad (32)$$

Note that the total leakage currents given by (27) and (32) are inversely proportional to the buffer layer resistivity which implies that higher buffer layer resistivity will give rise to a decrease in leakage currents resulting in better device performance. However, as will be shown later, the buffer layer thickness is critical to leakage resistance and currents.

It should also be noted that the gate-to-source and the drain-to-gate leakage currents are the same as the channel-to-source and drain-to-channel leakage currents, respectively.

III. Performance Parameters

The equivalent circuit of MESFET including the leakage elements obtained in Sec.II is shown in Fig.8. The performance parameters of the device can be obtained using h-parameters(Ohkawa, 1975). Using simple network theory, the h-parameters of Fig.8 can be obtained as follow

$$h_{11} = \left. \frac{V_1}{I_1} \right|_{V_2=0} = \frac{1+j\omega c_{gs}r_i}{j\omega c_{gs}+j\omega c_{dg}-\omega^2 c_{gs}r_i c_{dg}} \quad (33)$$

$$h_{12} = \left. \frac{V_1}{V_2} \right|_{I_1=0} = \frac{(c_{dg}/c_{gs})-B}{A+(c_{dg}/c_{gs})} \quad (34)$$

$$h_{21} = \left. \frac{I_2}{I_1} \right|_{V_2=0} = \frac{g_m-j\omega c_{dg}(1+j\omega c_{gs}r_i)}{j\omega c_{gs}+j\omega c_{dg}(1+j\omega c_{gs}r_i)} \quad (35)$$

$$h_{22} = \left. \frac{I_2}{V_2} \right|_{I_1=0} = \frac{(c_{dg}/c_{gs})-B)(Ag_m-j\omega c_{dg})}{A+(c_{dg}/c_{gs})} + \left(\frac{1}{z_{dbs}} + Bg_m + g_{dg} + j\omega c_{dg} \right) \quad (36)$$

Where

$$A = \frac{1}{r_i(j\omega c_{gs} + \frac{1}{r_i})} \quad (37)$$

$$B = \frac{g_{gs} - g_{dg}}{j\omega c_{gs} + \frac{1}{r_i}} \quad (38)$$

$$z_{dbs} = \frac{R_{ds} + r_{dsb}}{r_{dsb} + j\omega c_{ds} r_{dsb} R_{ds} + R_{ds}} \quad (39)$$

For the intrinsic device parameters see Table 2. The drain to gate leakage transconductance g_{dg} is given by

$$g_{dg} = \frac{I'_{DG}}{V_{DS}} \Big|_{V_{GS}=\text{constant}} \quad (40)$$

When no leakage exists in the buffer layer, I'_{DG} and I'_{GS} are equal to zero and $r_{dsb} \rightarrow \infty$, the resultant h-parameters approaches to the well-known intrinsic h-parameters (Ohkawa, 1975).

The performance parameters are:

A. Maximum stable gain GMS

$$GMS = \frac{|h_{21}|}{|h_{12}|} \quad (41)$$

B. Unilateral gain U

$$U = \frac{|h_{12} + h_{21}|^2}{4[\text{Re}(h_{11}) - \text{Re}(h_{22}) + \text{Im}(h_{12})\text{Im}(h_{21})]} \quad (42)$$

where Re denotes the real part and Im denotes the imaginary part.

G. Maximum frequency of oscillation F_{MAX}

$$F_{MAX} = \frac{F_T}{2\sqrt{r_1/R_{ds}}} \quad (43)$$

IV. Numerical Results

The MESFET numerically analyzed in this section has a gate length of 1μ and a width of 500μ with an active layer thickness of 0.2μ and a buffer layer resistivity of $12 \Omega\text{-cm}$. The typical intrinsic parameter values for the MESFET is shown in table 2 (Liechti, 1976). Unless otherwise stated, the buffer layer thickness is assumed to be 2μ .

The comparisons between the performance parameters of the MESFET with and without buffer layer are based on the intrinsic equivalent circuit in which the parasitic elements have been neglected (see Fig.8)

The leakage current sources are strongly dependent on the resistivity of the buffer layer as shown in (27) and (32). Therefore, by increasing the resistivity of buffer layer, the leakage currents will decrease which improves the device performance. In Fig.9 the leakage resistance and currents are given as functions of the buffer layer thickness. In order to reduce the leakage, the buffer layer thickness must be less than 2μ . If otherwise leakage will short-circuit the active layer current. It is noted that $I'_{DG} \gg I'_{GS}$. This can be accounted for by the existence of high field region between the drain and gate. The variation of the leakage currents with the normalized drain bias voltage V_{DSN} is shown in Fig.10, where the slopes of the curves give the leakage transconductances.

It is shown in Fig.11 that F_{MAX} for the buffered device degrades by a factor of 2 to 4 due to leakage effect. By increasing the buffer layer resistivity and/or decreasing the buffer layer thickness F_{MAX} will improve proportionally.

The unilateral and the maximum stable gains vs. frequency are found decreasing with frequency. But they are much lower for the buffered device due to leakage effect when compared with those of the intrinsic device, as shown in Figs. 12 and 13.

VI. Conclusions

The leakage effect in MESFET has been investigated. It has been shown that if the buffer layer resistivity is low and/or the buffer layer thickness is large, leakage effect will considerably degrade the device performance. We have shown that for the 1μ gate-length n-GaAs MESFET if the buffer layer resistivity ρ is 12^{-2} -cm and the buffer layer thickness h is 2μ , the gains of device decrease drastically from their intrinsic values. Since the leakage resistance is proportion to ρ and the leakage currents are inversely proportional to ρ thus leakage effects can be reduced by increasing ρ . However, both the leakage resistance and currents depend on h more strongly than ρ thus it is advantageous to decrease h for improving performance. We suggest that h should be lower than 2μ .

Table. 1

Parameters for two-linear region approximation of gate potential distribution

(known) Original structure	(calculated) Final structure
α	$\alpha' = \alpha \frac{K(p)}{a_1}$
m_1	$m_1' = \frac{V_p}{\alpha'}$
m_2	$m_2' = \frac{m_2(2a_1 - \alpha)}{2K(p) - \alpha'}$

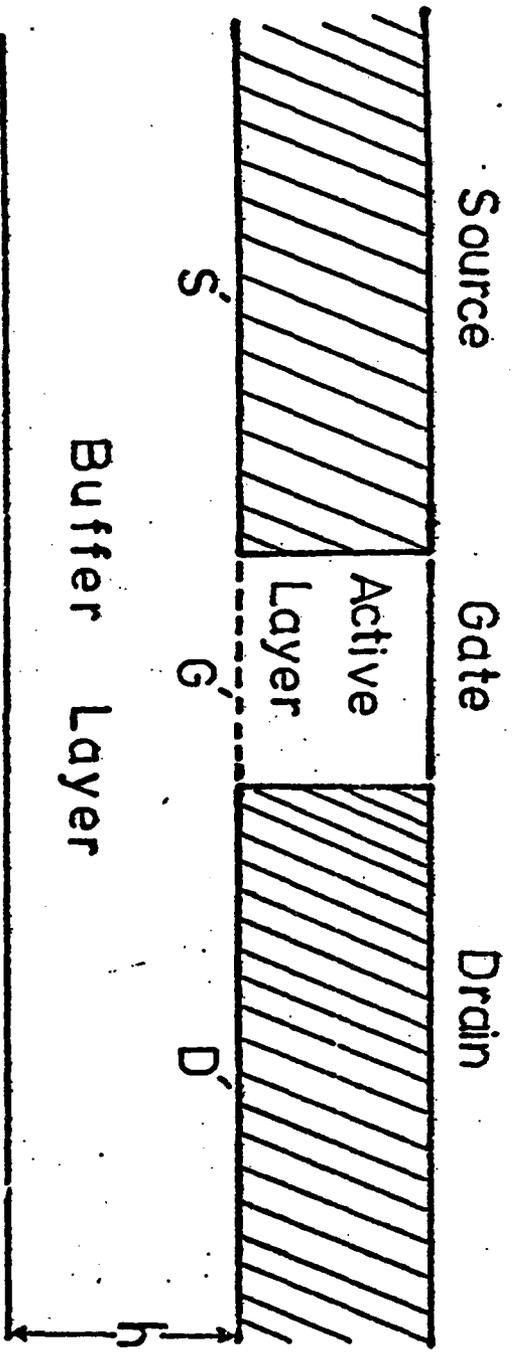
Table. 2

Typical intrinsic parameter values for the MESFET with the gate length of 1μ , width of 500μ , active layer thickness of 0.2μ with the doping density of 10^{17} cm^{-3}

c_{gs}	0.31 Pf
c_{dg}	0.038 Pf
r_i	8.0 Ω
g_m	22 mV
R_{ds}	350 Ω
c_{ds}	0.11 Pf

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S-I. Substrate

Fig. 1

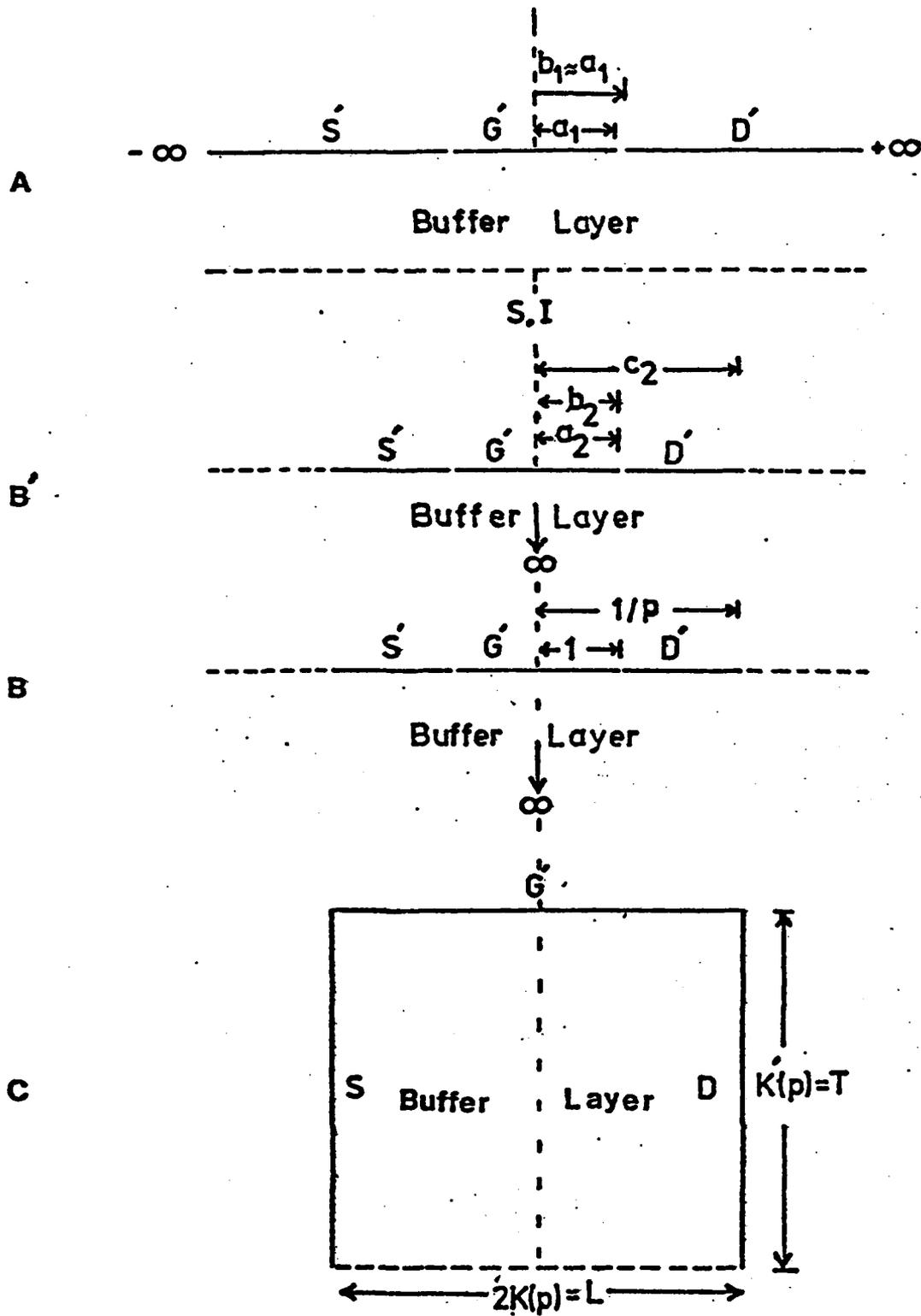


Fig. 2

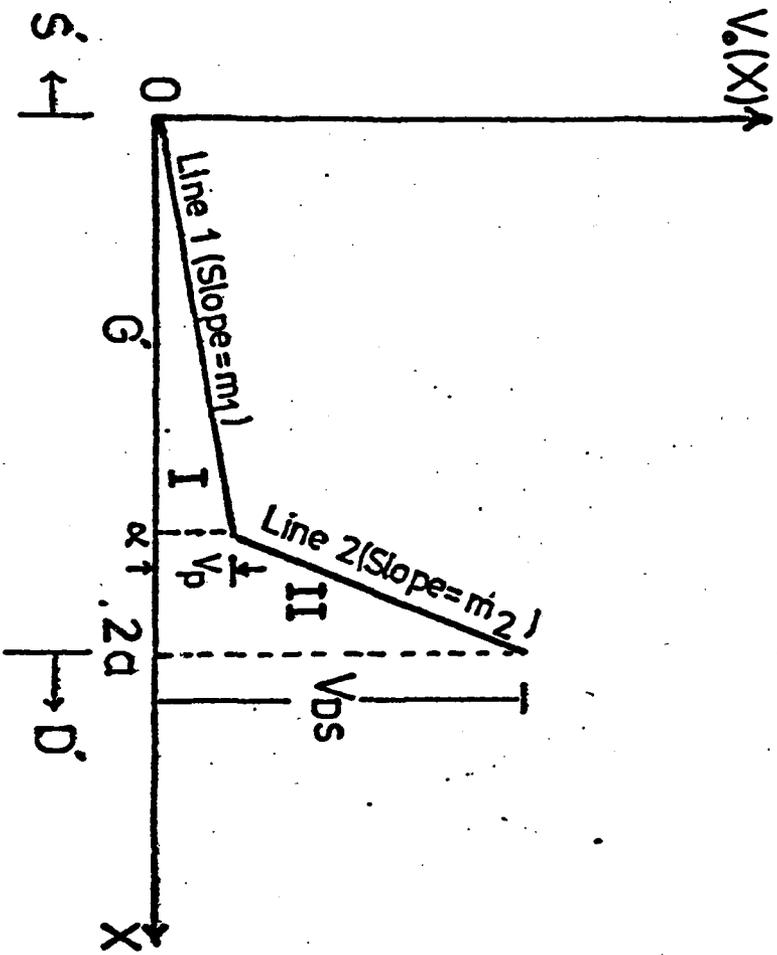


Fig. 3

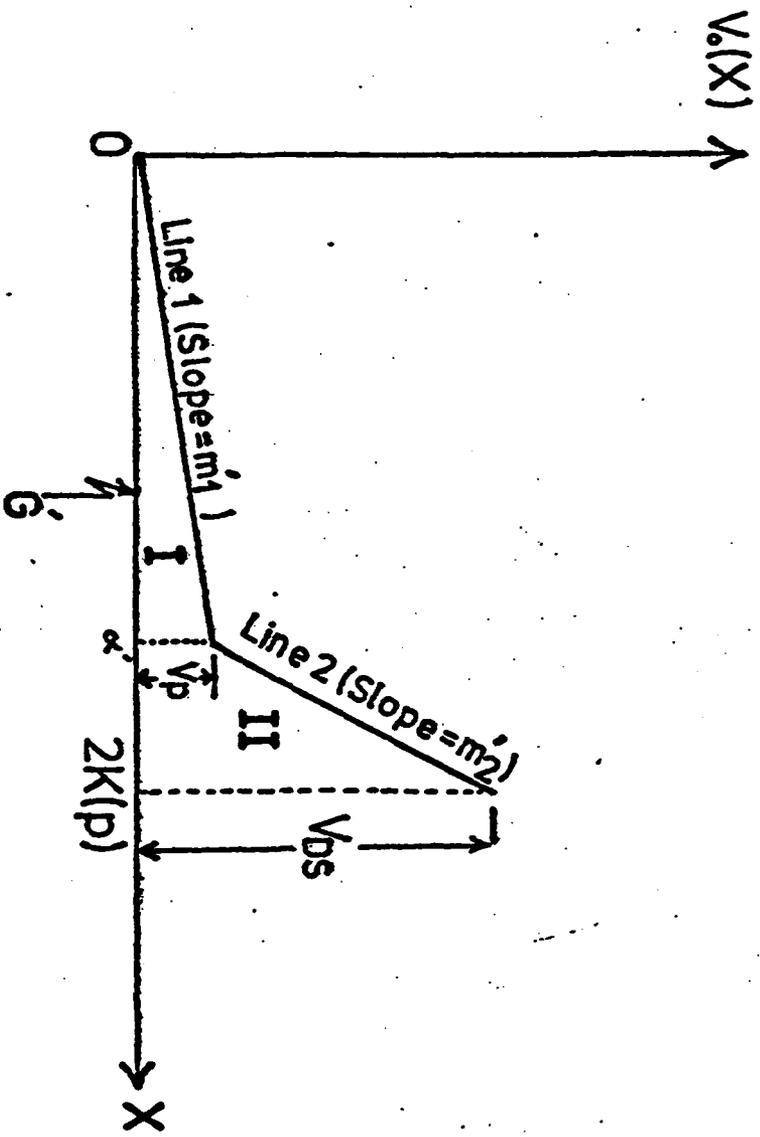


Fig. 4

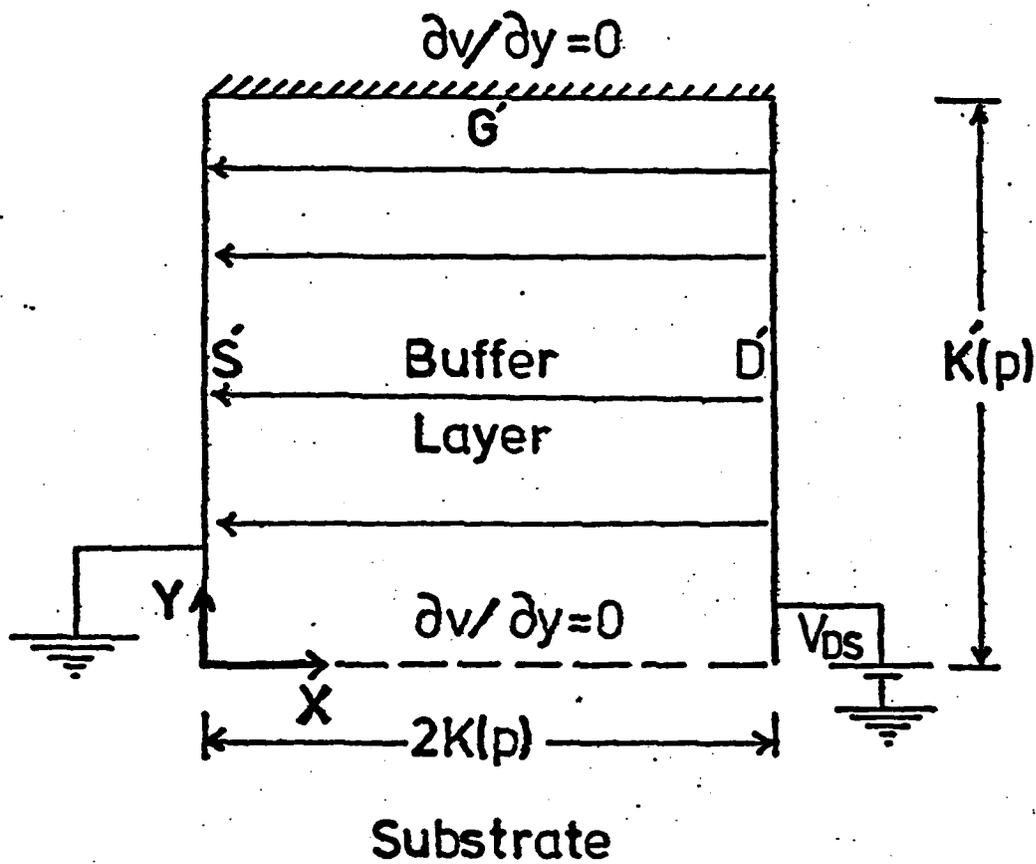


Fig. 5

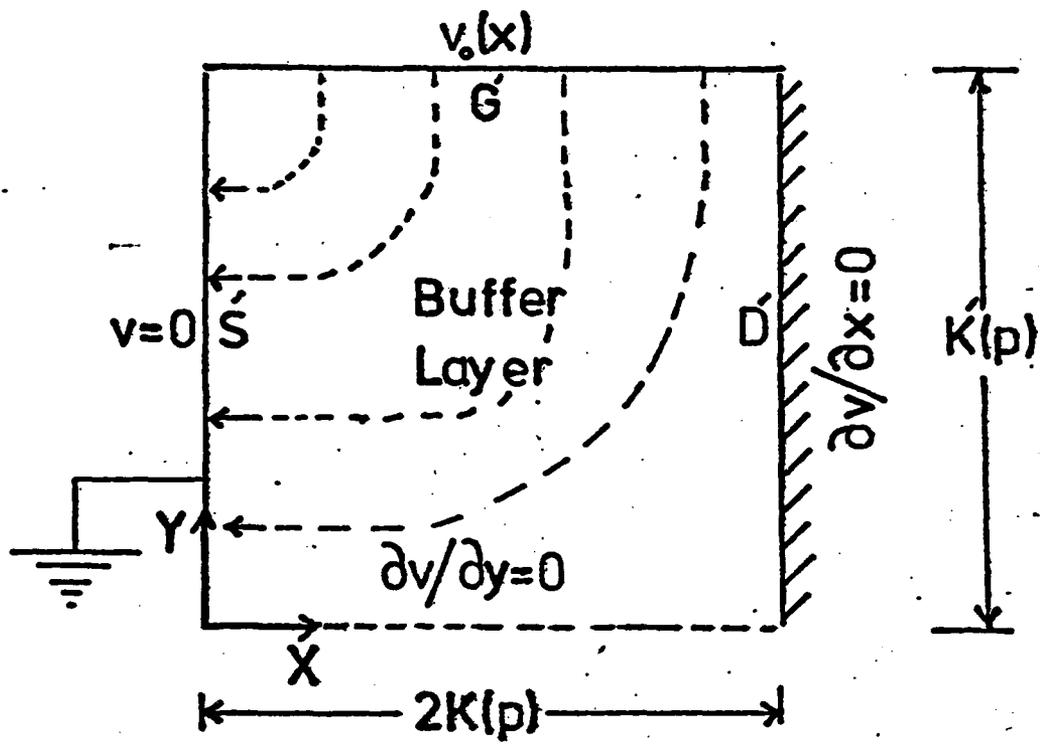
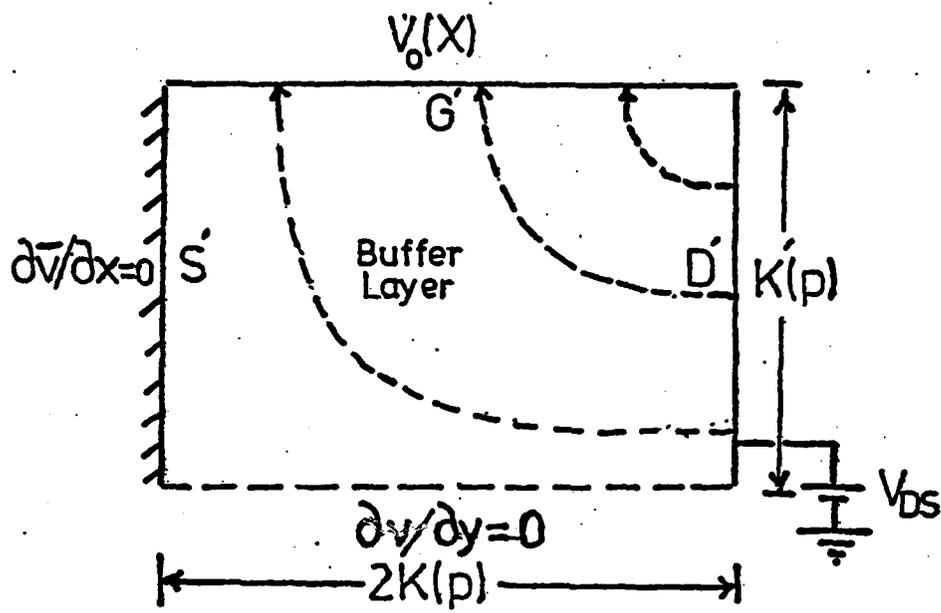
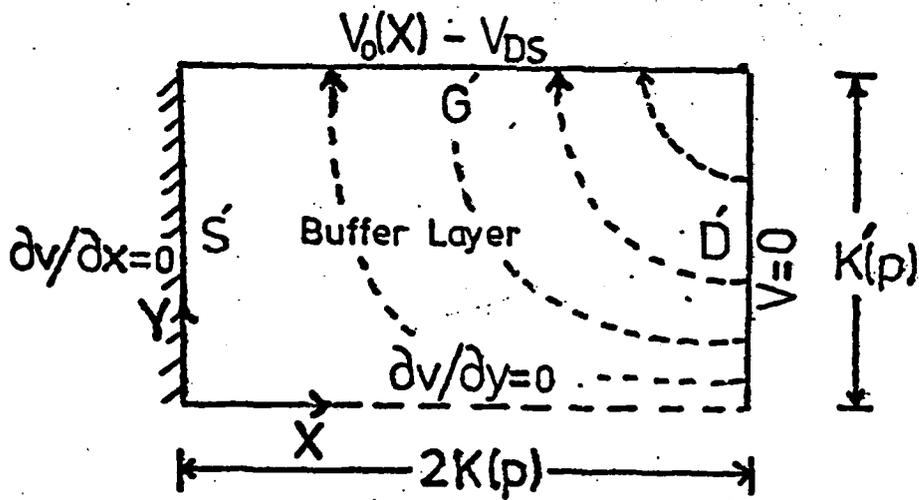


Fig. 6



(a)



(b)

Fig. 7

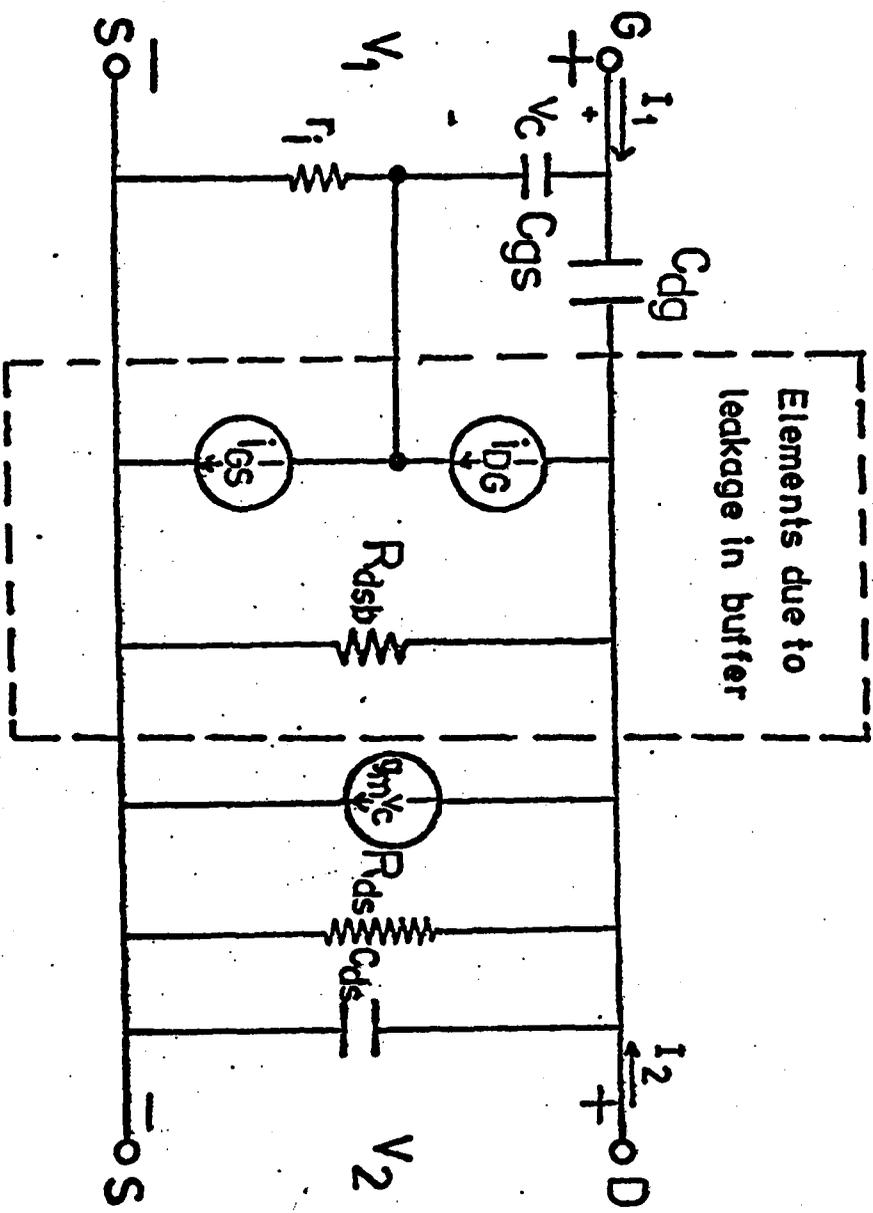


Fig. 8

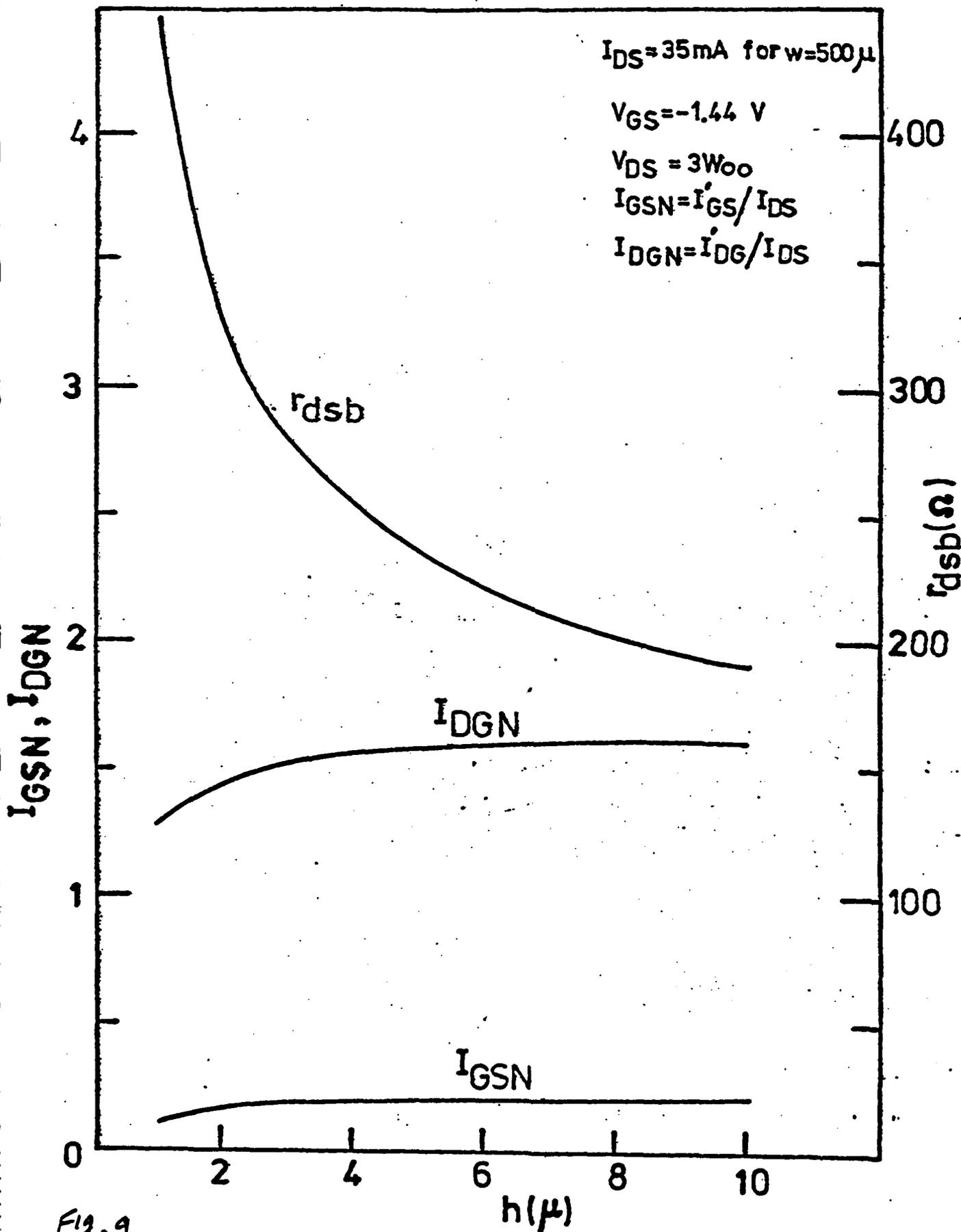


Fig. 9

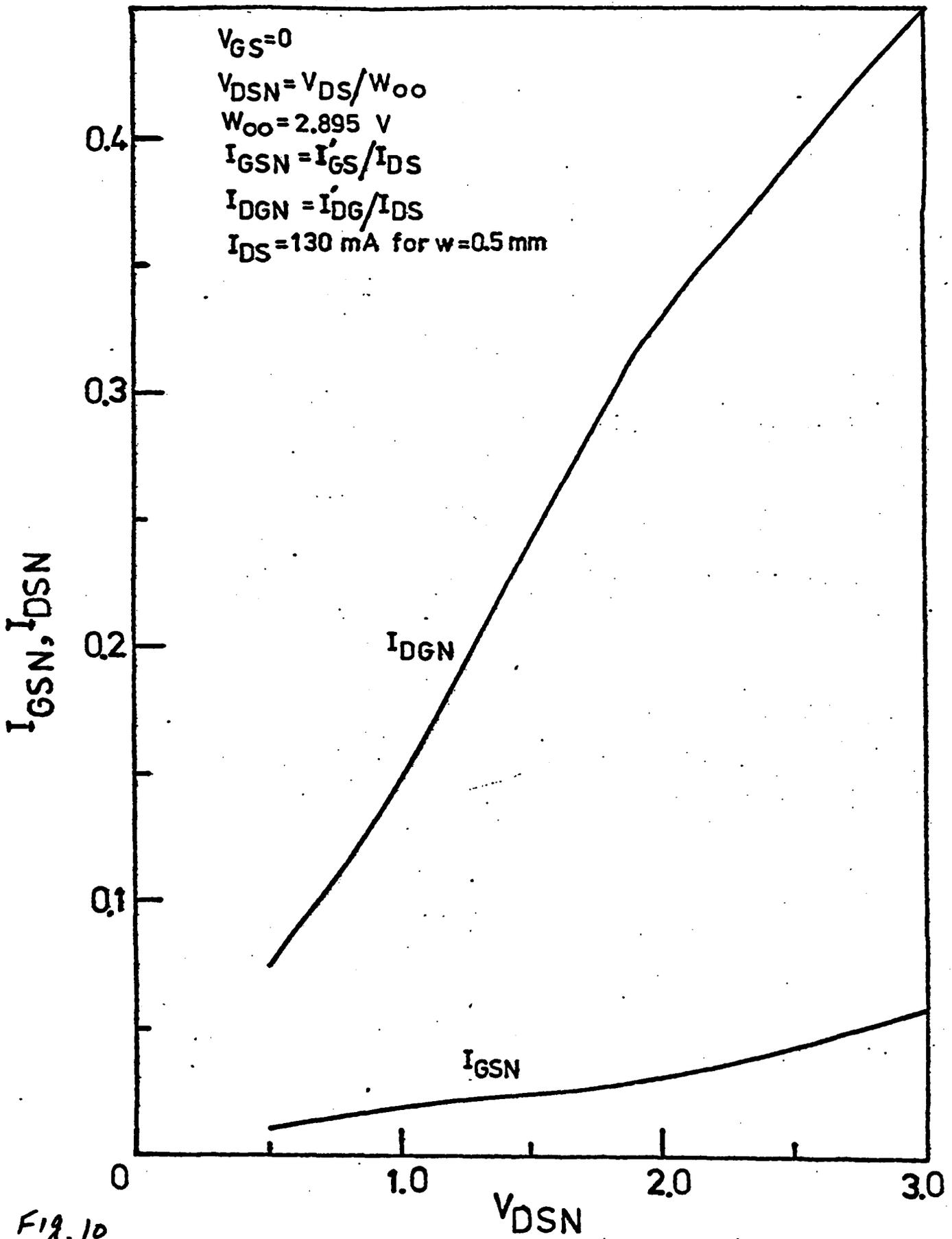


Fig. 10

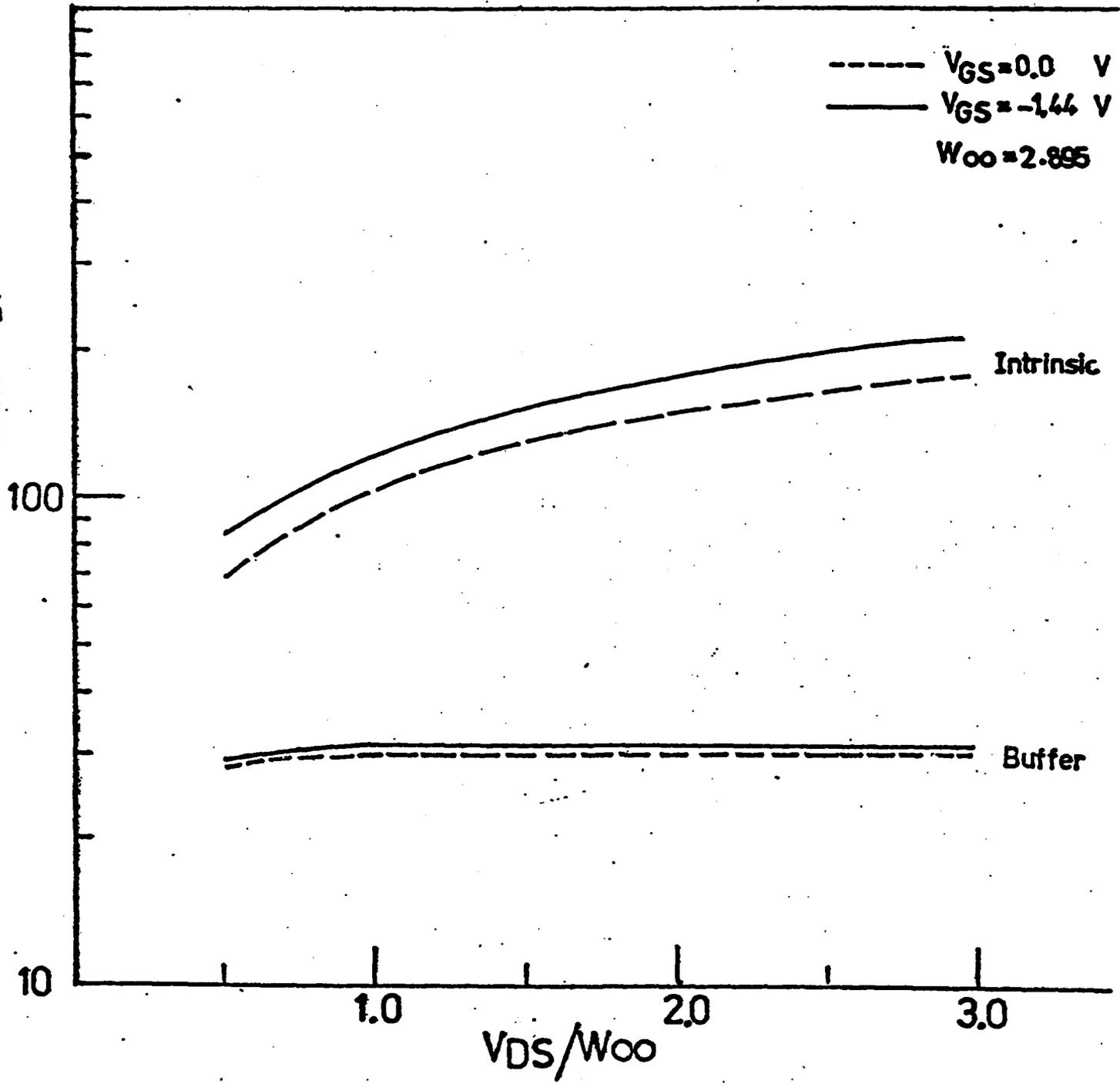


Fig. 11

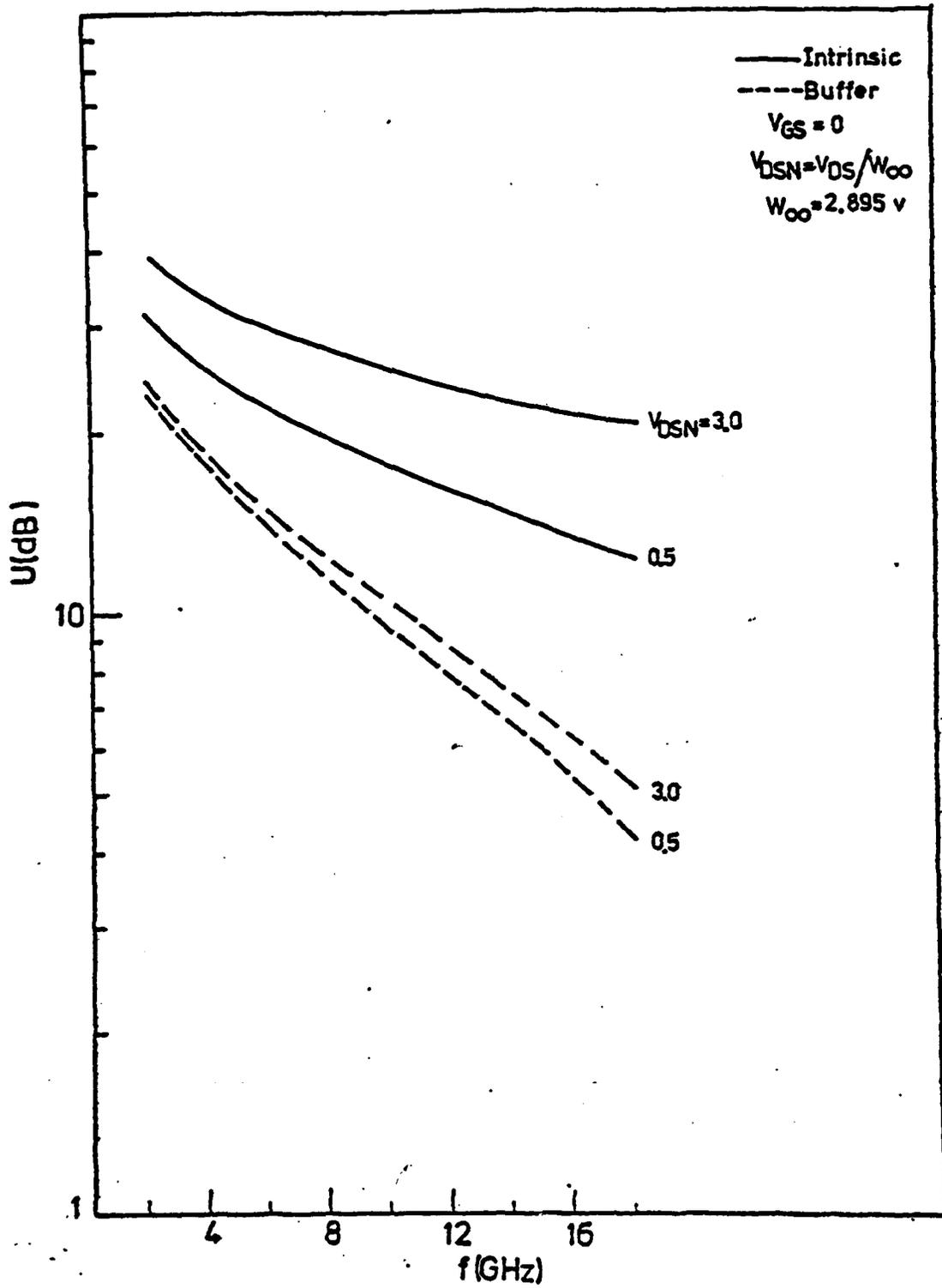


Fig. 12

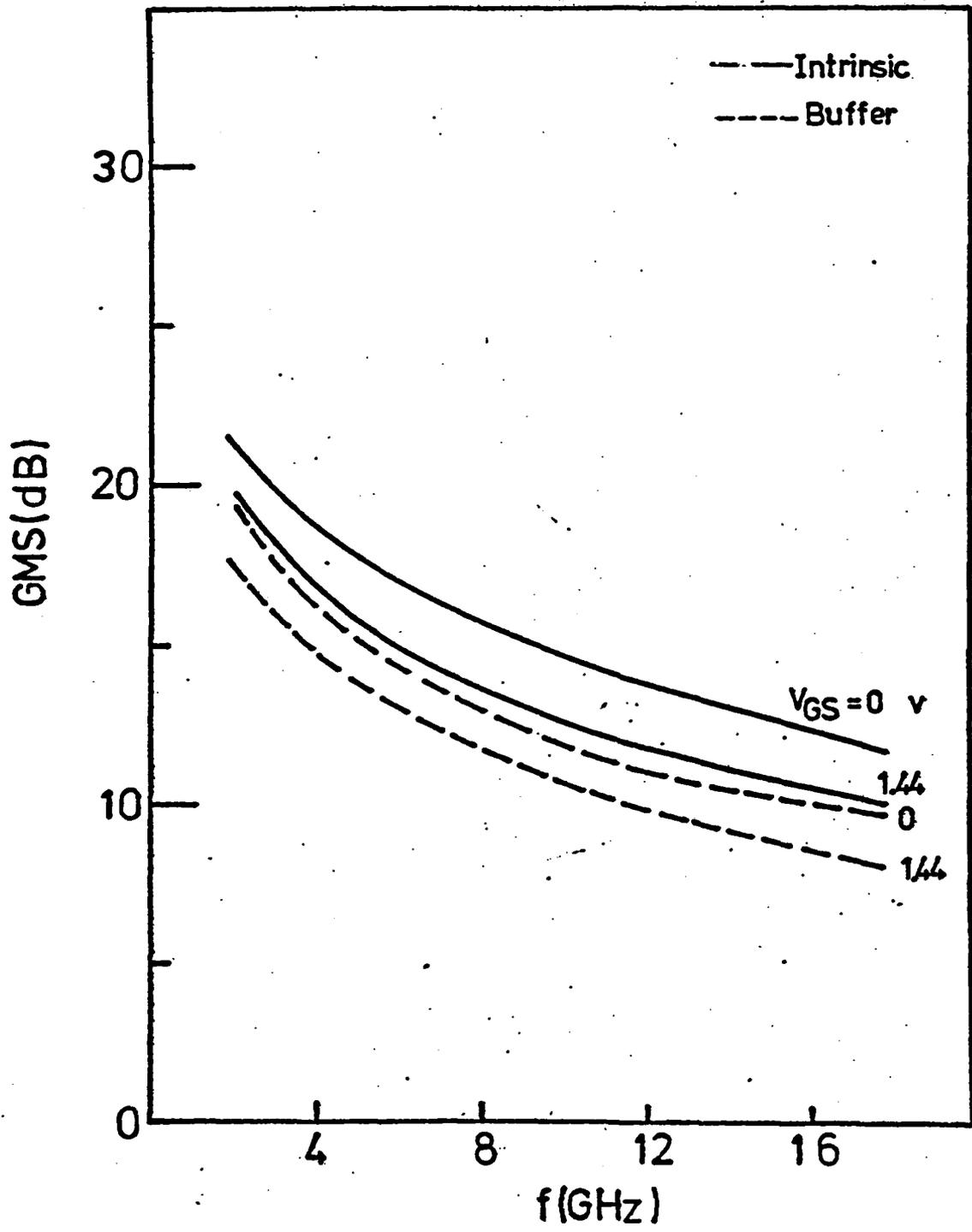


Fig. 13

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A CONTRIBUTION

"GaAs MESFET WITH
LATERAL NON-UNIFORM DOPING"

BY

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ABSTRACT

An analytical model of the GaAs MESFET with arbitrary non-uniform doping is presented. Numerical results for linear lateral doping profile are given as a special case. Theoretical considerations predict that better device linearity and improved F_T can be obtained by using linear lateral doping when doping density increases from source to drain.

I. INTRODUCTION

Improved linearity and noise figure in FET's with vertical non-uniform doping has been demonstrated by Williams and Shaw(1978), Roberts, Lynch, Tan and Gladstone(1978), Pucel(1978) and Santis(1979). In this paper we consider the non-uniform doping (along the electron motion) in the GaAs layer of the FET. Two advantages in this type of FET are anticipated. First if an appropriate profile is used, the depletion-channel interface can become more uniform along the lateral direction hence better linearity. Secondly, The cut-off frequency F_T increase can be realized for certain lateral doping profile.

A general mathematical analysis is presented in which the depletion region potential is solved from Poisson's equation as a boundary value problem. In the channel we adopt the saturation velocity model introduced by Williams and Shaw(1978) which is valid for short gate (Sze, 1981). The analysis takes into account two-dimensional general non-uniform doping profile. In obtaining numerical results however, a simple linear doping profile along the lateral direction is assumed. Device parameters such as g_m , C_{gs} and F_T are given in terms of the gate bias voltage for the FET with gate length of 0.6μ .

In Sec. II the two dimensional potential in the depletion region is analyzed. In Sec. III the depletion height h/a , reduced potential and channel current for linear lateral doping case are presented. Device parameters are obtained in Sec. IV. Conclusions are given in Sec. V.

II. TWO DIMENSIONAL ANALYSIS OF THE DEPLETION REGION POTENTIAL

A. General solution

The two dimensional Poisson's equation is given by

$$\nabla^2 W(x,y) = \frac{\partial^2 W(x,y)}{\partial x^2} + \frac{\partial^2 W(x,y)}{\partial y^2} = -f(x,y) \quad (1)$$

where $f(x,y) = qN(x,y)/\epsilon$, $N(x,y)$ is the x-and-y dependent doping density and $W(x,y)$ is the potential in the depletion region as shown in Fig. 1. This inhomogeneous second order partial differential equation can be solved by using Green's function method where equation (1) will be written as

$$\frac{\partial^2 G(x,y)}{\partial x^2} + \frac{\partial^2 G(x,y)}{\partial y^2} = -\delta(x-\xi)\delta(y-\eta) \quad (2)$$

where ξ and η are the dummy variables. The boundary conditions associated with (1) are given as follow

Schottky gate:
$$W(x,y) \Big|_{y=0} = 0 \quad (3)$$

Depletion-channel interface:
$$\frac{\partial W(x,y)}{\partial y} \Big|_{y=h} = 0 \quad (4)$$

Ohmic contact source:
$$\frac{\partial W(x,y)}{\partial x} \Big|_{x=0} = 0 \quad (5)$$

Ohmic contact drain:
$$\frac{\partial W(x,y)}{\partial x} \Big|_{x=l} = 0 \quad (6)$$

where h is the variable depletion layer height and l is the gate

length (see Fig. 1). It is the unique property of the operator (∇^2) which is the sum of the two commutative operators which enable us to find an explicit solution to (1). Equation (1) can be written as

$$\nabla^2 W(x,y) = K_1 W(x,y) + K_2 W(x,y) \quad (7)$$

where $K_1 = \partial^2 / \partial x^2$ and $K_2 = \partial^2 / \partial y^2$. Friedman (1956) shows that if K_1 and K_2 commute, K_2 (or K_1) can be treated as a constant so that the partial differential equation (1) becomes an ordinary differential equation given by

$$\frac{d^2 W(x,y)}{dx^2} + m^2 W(x,y) = -f(x,y) \quad (8)$$

where $m = \sqrt{K_2}$. Using the boundary conditions given in (5) and (6), the solution of (8) becomes

$$W(x,y) = \frac{1}{m} \int_0^x -f(\tau,y) \sin[m(x-\tau)] d\tau \quad (9)$$

where $f(\tau,y)$ is the spectral representation of K_2 . The eigenvalues of $m = \sqrt{K_2}$ will be purely imaginary i.e., $m = (jn\pi)/2h$, and consequently the sin term in (9) will become sinh. The eigenfunction of K_1 can be determined by considering the following homogeneous ordinary differential equation

$$\frac{d^2 W(x,y)}{dy^2} + \lambda^2 W(x,y) = 0 \quad (10)$$

where $\lambda = \sqrt{K_1}$. Using boundary conditions given in (3) and (4), the

eigenfunctions of W can be obtained and they would be of the form $\sin \lambda y$ where $\lambda = (n\pi y)/2h$ ($n=1,3,5,\dots$). Because of the fact that W is orthogonal and it can be normalized to unity, let

$$f(\zeta, y) = \sum_{n=\text{odd}} \left[\beta_n \sin \frac{n\pi y}{2h} \right] \quad (11)$$

where

$$\beta_n = \frac{2}{h} \int_0^h \sin\left(\frac{n\pi y}{2h}\right) f(\zeta, y) dy \quad (12)$$

where $2/h$ is the normalization factor. Substituting (12) into (11), the spectral representation of K_2 can be obtained and is given by

$$f(\zeta, y) = \frac{2}{h} \sum_{n=\text{odd}} \sin\left(\frac{n\pi y}{2h}\right) \int_0^h d\eta f(\zeta, \eta) \sin\left(\frac{n\pi \eta}{2h}\right) \quad (13)$$

Note that $f(\zeta, \eta)$ includes the general doping density in dummy variables ζ, η , i.e., $f(x, y) = qN(x, y)/\epsilon$. The depletion region potential $W(x, y)$ of the FET with general two dimensional doping density can be obtained by substituting (13) into (9) and it is given by

$$W(x, y) = -\frac{4q}{\epsilon} \sum_{n=\text{odd}} (1/n) \sin\left(\frac{n\pi y}{2h}\right) \left\{ \int_0^x d\zeta \int_0^h d\eta \cdot N(\zeta, \eta) \sin\left(\frac{n\pi \eta}{2h}\right) \sinh\left[\frac{n\pi}{2h}(x-\zeta)\right] \right\} \quad (14)$$

B. Uniform doping profile

Whereas equation (14) satisfies (1) and its boundary conditions as can be verified, it reduces to the solution for uniform doping (Pucel, 1975) by setting $N(\xi, \eta) = N_0$ in (14). Thus at the interface ($y=h$) equation (14) becomes

$$W(x, h) = -\frac{4qN_0}{\pi\epsilon} \sum_{n=\text{odd}} (1/n) \sin\left(\frac{n\pi}{2}\right) \int_0^x d\xi \int_0^h d\eta \sin\left(\frac{n\pi\eta}{2h}\right) \sinh\left[\frac{n\pi}{2h}(x-\xi)\right] \quad (15)$$

After integration and some algebra, equation (15) becomes

$$W(x, h) = \frac{16qh^2N_0}{\epsilon\pi^3} \sum_{n=\text{odd}} (1/n^3) \sin\left(\frac{n\pi}{2}\right) \quad (16)$$

The identity

$$\sum_{n=\text{odd}} (1/n^3) \sin\left(\frac{n\pi}{2}\right) = \frac{\pi^3}{32} \quad (17)$$

can be applied to (16) to give the depletion region potential in a uniformly doped FET, i.e.,

$$W(x, h) = W_{00} \left(\frac{h}{a}\right)^2 \quad (18)$$

which is identical to that obtained by Pucel (1975). W_{00} is the pinch-off potential of a uniformly doped FET.

$$W_{00} = \frac{qa^2N_0}{2\epsilon} \quad (19)$$

Note that there is no well-defined pinch-off potential for non-uniformly doped FET.

III. LINEAR LATERAL DOPING PROFILE

For the special case of lateral doping, $N(\xi, \eta) = N(\xi)$ in equation (14), where $N(\xi)$ is the lateral doping profile. Therefore, the depletion region potential for lateral doping becomes

$$W(x, y) = -\frac{4q}{\pi\epsilon} \sum_{n=\text{odd}} (1/n) \sin\left(\frac{n\pi y}{2h}\right) \int_0^x d\xi \int_0^h d\eta N(\xi) \sin\left(\frac{n\pi\eta}{2h}\right) \sinh\left[\frac{n\pi}{2h}(x-\xi)\right] \quad (20)$$

A. Depletion height and reduced potential distribution

For linear doping let

$$N(\xi) = N_0(1 + \alpha\xi) \quad (21)$$

where α is the rate of change of doping density which increases with ξ (or x) if $\alpha > 0$ and decreases if $\alpha < 0$. N_0 is assumed to be 10^{17} cm^{-3} . Substituting (21) into (20),

$$W(x, y) = -\frac{4qN_0}{\pi\epsilon} \sum_{n=\text{odd}} (1/n) \sin\left(\frac{n\pi y}{2h}\right) \int_0^x d\xi \int_0^h d\eta (1 + \alpha\xi) \sin\left(\frac{n\pi\eta}{2h}\right) \sinh\left[\frac{n\pi}{2h}(x-\xi)\right] \quad (22)$$

After integration with respect to η , (22) becomes

$$W(x, y) = -\frac{8qhN_0}{\pi^2\epsilon} \sum_{n=\text{odd}} (1/n^2) \sin\left(\frac{n\pi y}{2h}\right) (A_1 + A_2) \quad (23)$$

where

$$A_1 = \int_0^x d\xi \sinh\left[\frac{n\pi}{2h}(x-\xi)\right] \quad (24)$$

$$A_2 = \alpha \int_0^x d\xi \cdot \xi \sinh\left[\frac{n\pi}{2h}(x-\xi)\right] \quad (25)$$

Or

$$A_1 = -\frac{2h}{n\pi} \cosh\left[\frac{n\pi}{2h}(x-\xi)\right] \Big|_{\xi=x} \quad (26)$$

$$A_2 = \alpha \left\{ -\frac{2h}{n\pi} \int \cdot \cosh\left[\frac{n\pi}{2h}(x-\xi)\right] - \left(\frac{2h}{n\pi}\right)^2 \sinh\left[\frac{n\pi}{2h}(x-\xi)\right] \right\} \Big|_{\xi=x} \quad (27)$$

Thus

$$A_1 = -\frac{2h}{n\pi} \quad (28)$$

and

$$A_2 = -\frac{2h\alpha x}{n\pi} \quad (29)$$

Therefore equation (23) becomes

$$W(x,y) = -\frac{8qhN_0}{\pi^2\epsilon} \sum_{n=\text{odd}} (1/n^2) \sin\left(\frac{n\pi y}{2h}\right) \left(-\frac{2h}{n\pi} - \frac{2h\alpha x}{n\pi}\right) \quad (30)$$

or

$$W(x,y) = \frac{16qh^2N_0}{\pi^3\epsilon} \sum_{n=\text{odd}} (1/n^3) \sin\left(\frac{n\pi y}{2h}\right) (1+\alpha x) \quad (31)$$

At depletion-channel interface, i.e., $y=h$, the depletion region potential $W(x,y)$ becomes

$$W(x,h) = \frac{16qh^2N_0}{\pi^3\epsilon} (1+\alpha x) \sum_{n=\text{odd}} (1/n^3) \sin\left(\frac{n\pi}{2}\right) \quad (32)$$

Using the identity described in (17), equation (32) reduces to

$$W(x,h) = \frac{qh^2N_0}{2\epsilon} (1+\alpha x) \quad (33)$$

The reduced potential u which is the same as w of Pucel (1975) can be obtained as follows

$$u^2(x,h) = \frac{W(x,h)}{W_{00}} = \left[\frac{h(x)}{a}\right]^2 (1+\alpha x) \quad (34)$$

where W_{00} is given in (19). Because α plays an important role in our analysis, its range and limitation need to be considered. When

α is too small, the doping becomes almost uniform, however, α can not be too large for otherwise the semiconductor will become degenerate. We shall consider the two cases, i.e., small α ($|\alpha l| = 0.1$) and large α ($|\alpha l| = 0.9$) where the gate length is assumed to be 0.6μ .

(i). Small α ($|\alpha l| = 0.1$)

In this case the normalized depletion height h/a becomes almost uniform in the saturation velocity model (Sze, 1981), i.e., $u=s$ where $s=u(0,h)$. Therefore (34) becomes

$$h/a = \sqrt{\frac{s^2}{1+\alpha x}} \approx s \quad (35)$$

Where s is the reduced potential at the source and is given by (Pucel, 1975)

$$s = \sqrt{\frac{V_{gs} + \phi}{W_{00}}} \quad (36)$$

Where V_{gs} is the gate-source bias voltage and ϕ is the barrier potential.

(ii). Large α ($|\alpha l| = 0.9$)

In this case it is necessary to calculate the potential $V(x)$ in the channel. From Fig. 1 and equation (34),

$$V(x) = -(V_{gs} + \phi) + W(x,h) = W_{00} [u^2(x,h) - s^2] \quad (37)$$

Under the commonly used assumption of neutral channel, where the carrier and doping densities are the same, the Poisson's equation becomes

$$\frac{d^2 V(x)}{dx^2} = 0 \quad (38)$$

The assumption of neutral channel is reasonable for high doping density. It is obvious that the solution of (38) is $V(x) = Ax + B$,

Where A and B are constant to be determined. Using the conditions that $V(0)=0$ (source is grounded) and $V(\ell)=V_{ds}$ (drain-source bias potential), one obtains $B=0$, and $A=V_{ds}/\ell$. Therefore the channel potential $V(x)$ becomes

$$V(x) = (V_{ds}/\ell)x \quad (39)$$

From (37) and (39), the reduced potential $u(x,h)$ can be obtained and is given by

$$u(x,h) = \sqrt{\frac{w_{00}s^2 + (V_{ds}/\ell)x}{w_{00}}} \quad (40)$$

And from (34) the normalized depletion height h/a can be obtained and is given by

$$\frac{h(x)}{a} = \sqrt{\frac{s^2 + (V_{dsn}/\ell)x}{1 + \alpha x}} \quad (41)$$

Where $V_{dsn} = V_{ds}/w_{00}$. Equation (41) implies that as α increases, the height of the depletion region is no longer a constant and varies with α and x .

B. Channel Current

The total current consists of the conduction current and diffusion current. However, in the neutral channel the diffusion current can be neglected. Also neglected here is the small band-gap narrowing effect due to doping variation.

The conduction current is given by

$$I(x) = qn(x)v_s A \quad (42)$$

Where q is the electron charge, $n(x) = N_0(1 + \alpha x)$ is the carrier

(or doping) density, v_s is the saturation velocity and $A(x)=z[a-h(x)]$ is the cross-sectional area (z is the device width). Thus from (42) we have

$$I(x)=qN_0(1+\alpha x)\left[1-\frac{h(x)}{a}\right]azv_s \quad (43-a)$$

In equation (43-a) (which is equivalent to (6) of Pucel, 1975), the current is a function of $h(x)$ and $n(x)$. Therefore the total average current I (which is constant) is obtained by integrating (43-a) from $x=0$ to $x=l$

$$I = \frac{1}{l} \int_0^l I(x) dx \quad (43-b)$$

Thus for small α ($|\alpha l|=0.1$), $h(x)/a \approx s$ (see (35)), and the total average current becomes

$$I = qv_s z a N_0 (1-s) \left(1 + \frac{\alpha l}{2}\right) \quad (44)$$

And for large α ($|\alpha l|=0.9$), the total average current can be obtained from (43), and is given by

$$I = \frac{qv_s z a N_0}{l} \int_0^l (1+\alpha x) \left[1 - \frac{h(x)}{a}\right] dx \quad (45)$$

It is convenient that we perform the integration in u instead of x . From (40) we solve x in terms of u ,

$$x = \frac{l(u^2 - s^2)}{v_{dsn}} \quad (46)$$

Substituting (46) into (45) we get

$$I = \frac{2qzav_s N_0}{v_{dsn}} \int_s^d \left\{ u \left[1 + \frac{\alpha l}{v_{dsn}} (u^2 - s^2) - \sqrt{1 + \frac{\alpha l}{v_{dsn}} (u^2 - s^2)} \right] \cdot u \right\} du \quad (47)$$

Where d is the reduced potential at the drain, and is given by (Pucel, 1975)

$$d = \sqrt{\frac{V_{gs} + \phi + V_{ds}}{W_{00}}} \quad (48)$$

Equation (44) for small α and (47) for large α are dependent on the gate bias voltage, their transfer characteristics as functions of $(V_{gs} + \phi)/W_{00} = s^2$ are shown in Fig. 2. For the purpose of numerical calculation, it is specified that $\alpha = 1.67 \times 10^3 \text{ cm}^{-1}$ for small α and $\alpha = 1.5 \times 10^4 \text{ cm}^{-1}$ for large α . Thus for example, for $\alpha = -1.67 \times 10^3 \text{ cm}^{-1}$, $N(x)$ decreases from 10^{17} cm^{-3} (source) to $9 \times 10^{16} \text{ cm}^{-3}$ (drain), or for $\alpha = 1.5 \times 10^4 \text{ cm}^{-1}$, $N(x)$ increases from 10^{17} cm^{-3} (source) to $1.9 \times 10^{17} \text{ cm}^{-3}$ (drain). The gate length is assumed to be 0.6μ and the drain-source bias voltage is assumed to be high enough to ensure saturation, i.e., $V_{ds} = W_{00}$.

Fig. 2 shows significant improvement in linearity when α is large. However, when $\alpha < 0$, channel pinches off quickly at low gate-source bias voltage. The reason why it pinches off so fast is that both the channel opening and the carrier density are decreasing functions of x (see (38)). Therefore, the voltage swing is very much limited and devices with $\alpha < 0$ are of little use.

When α is small, there is no significant difference in the transfer characteristics when compared with uniform doping ($\alpha = 0$) as it should be.

IV. DEVICE PARAMETERS

The small-signal parameters for the case of linear doping is presented in this section. The parameters of a typical FET is assumed to be $z=500 \mu$, $a=0.2 \mu$, $l=0.6 \mu$, $N_0=10^{17} \text{ cm}^{-3}$, $E_s=4.44 \text{ KV/cm}$, $\epsilon_r=12.5$, $\mu_0=4500 \text{ cm}^2/\text{V-sec.}$, $\phi=0.8 \text{ V}$, and $v_s=\mu_0 E_s$. ($0.1 \leq \alpha l \leq 0.9$).

A. Transconductance g_m

The transconductance g_m is defined as

$$g_m = \left. \frac{\partial I}{\partial V_{gs}} \right|_{V_{ds}} = - \left(\frac{\partial I}{\partial s} \frac{\partial s}{\partial V_{gs}} + \frac{\partial I}{\partial d} \frac{\partial d}{\partial V_{gs}} \right) \bigg|_{V_{ds}} \quad (49)$$

When α is small, the transconductance can be obtained by using (44) and (49) and is given by

$$g_m \bigg|_{(h/a)=s} = \frac{qz v_s a N_0}{2W_{00} s} (1 + \alpha l/2) \quad (50)$$

When α is large, equation (47) can be numerically differentiated according to (49). The transconductance for small and large α are shown in Fig. 3. As expected, for small α , the variation of g_m with gate bias voltage approaches to that of the uniform doping. However, as $|\alpha l|$ approaches unity there is significant improvement in linearity of g_m .

B. Gate-to-source capacitance C_{gs}

According to Pucel (1975), the total charge on the gate electrode is given by

$$Q_g = \epsilon_r \epsilon_0 z \int_0^l E_y dx \quad (51)$$

Where E_y is the y-component of the electric field defined as

$$E_y = \left. \frac{\partial W(x,y)}{\partial y} \right|_{y=0} = \frac{2W_{00}}{a}(h/a)(1+\alpha x) \quad (52)$$

Differentiating (14) with respect to y , E_y hence Q_g can be evaluated.

C_{gs} is defined as (Pucel, 1975)

$$C_{gs} = \left. \frac{\partial Q_g}{\partial V_{gs}} \right|_{V_{ds}} = \left(\frac{\partial Q_g}{\partial s} \frac{\partial s}{\partial V_{gs}} \right) \Big|_{V_{ds}} \quad (53)$$

For small α , Q_g can be obtained from (51) and (52),

$$Q_g = \frac{2\epsilon_r \epsilon_0 W_{00} z s}{a} \left(l + \frac{\alpha}{2} l^2 \right) \quad (54)$$

And from (53), C_{gs} becomes,

$$C_{gs} \Big|_{h/a=s} = \frac{\epsilon_r \epsilon_0 z}{as} \left(l + \frac{\alpha}{2} l^2 \right) \quad (55)$$

For large α , Q_g becomes

$$Q_g = \frac{2\epsilon_r \epsilon_0 W_{00} z}{a} \int_0^l (1+\alpha x)(h/a) dx \quad (56)$$

Where h/a is given in (41). Substituting (56) into (53), C_{gs} for large α can numerically be evaluated. Fig. 4 shows that the rate of change of Q_g with $(V_{gs} + \phi)/W_{00}$ is larger for small α than that for large α . This implies that C_{gs} decreases as $|\alpha|$ increases, as shown in Fig. 4.

C. Cut-off frequency F_T

The unit gain cut-off frequency is given by

$$F_T = \frac{g_m}{2\pi C_{gs}} \quad (57)$$

It is shown in Fig. 5 that for $\alpha > 0$ F_T does not vary with V_{gs} and F_T for large α (where $\alpha l = 0.9$, as an example) is almost twice as large as F_T for small and vanishing α . This improvement in F_T can be accounted for by the increase in g_m and decrease in C_{gs} due to the non-uniformity of doping.

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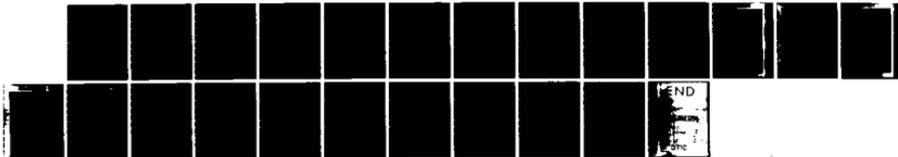
DEVELOPMENT OF SHORT GATE FET'S(U) HOWARD UNIV
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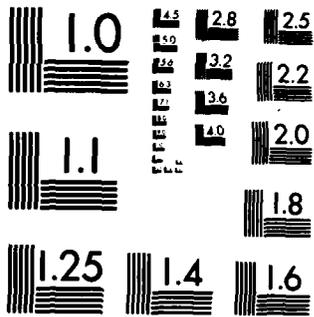
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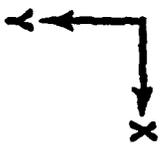
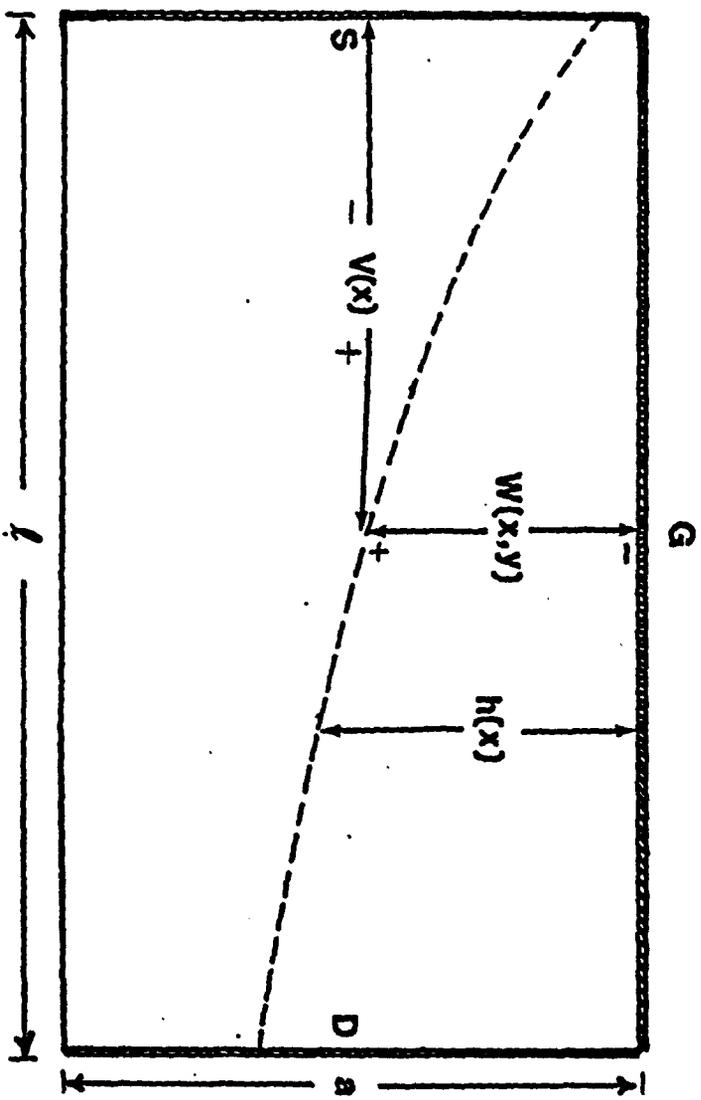


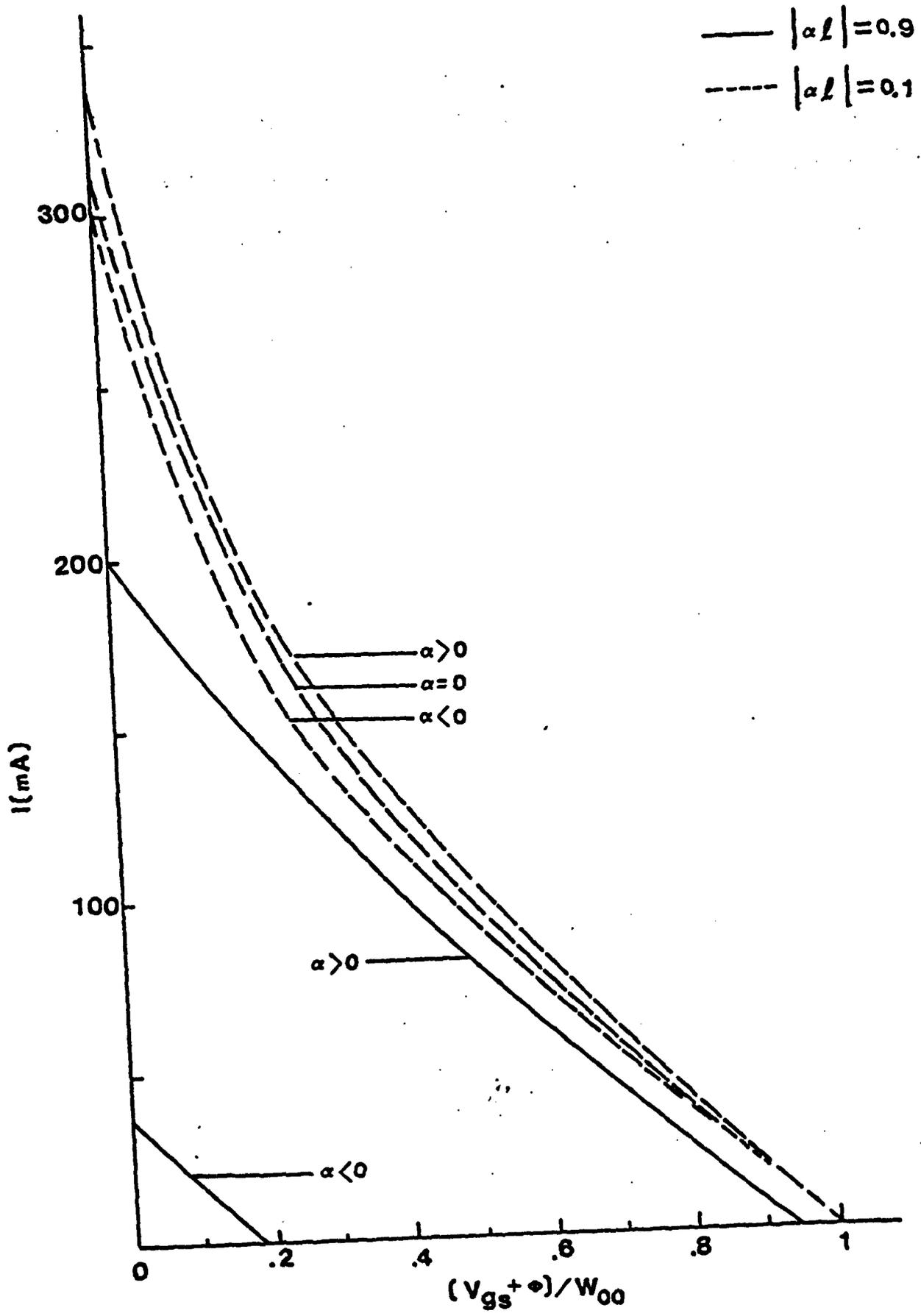
V. CONCLUSIONS

Analytical solution of potential in MESFET's with arbitrary doping profile have been presented. The linear doping profile has been treated as a special case, in detail. Numerical results on device parameters for linear lateral doping profile are presented and compared with those for uniform doping. It is shown that there is significant improvement in linearity as $|\alpha l|$ approaches toward unity. The transconductance of the FET is found to be larger for $\alpha l = 0.9$ than that for $\alpha l = 0.1$. This improvement in g_m can be accounted for by the increase in carrier density in the channel. Significant improvement in F_T can be realized for FET's with increasing doping density from source to drain (i.e., $\alpha > 0$). The analytical solution presented here is sufficiently general and it can be applied to other types of profiles such as exponential, power law and step for either vertical or lateral doping or their combinations. In future these topics will be investigated. Although experiments on vertical non-uniform doping have appeared, none has been available on lateral or general doping. Our theory predicts that the device performance depends on doping profile. Optimum lateral and vertical doping will be shown to be important for FET power amplifier.

LIST OF FIGURES

1. Cross-sectional diagram of MESFET showing geometrical dimensions ($a=0.2 \mu$, $l=0.6 \mu$, $z=500 \mu$).
2. Transfer characteristics for uniformly ($\alpha=0$) and non-uniformly ($\alpha \neq 0$) doped GaAs MESFET ($a=0.2 \mu$, $l=0.6 \mu$, $z=500 \mu$, $N_0=10^{17} \text{ cm}^{-3}$, $W_{00}=2.895 \text{ V}$, $V_{ds}=W_{00}$).
3. Transconductance vs. normalized gate voltage for uniformly ($\alpha=0$) and non-uniformly ($\alpha \neq 0$) doped GaAs MESFET ($a=0.2 \mu$, $l=0.6 \mu$, $z=500 \mu$, $N_0=10^{17} \text{ cm}^{-3}$, $V_{ds}=W_{00}=2.895 \text{ V}$).
4. C_{gs} and Q_g vs. normalized gate bias voltage for uniformly ($\alpha=0$) and non-uniformly ($\alpha \neq 0$) doped GaAs MESFET ($a=0.2 \mu$, $l=0.6 \mu$, $z=500 \mu$, $N_0=10^{17} \text{ cm}^{-3}$, $V_{ds}=W_{00}=2.895 \text{ V}$, $\epsilon_r=12.5$).
5. Cut-off frequency F_T vs. normalized gate bias voltage for uniformly ($\alpha=0$) and non-uniformly ($\alpha \neq 0$) doped GaAs MESFET ($a=0.2 \mu$, $l=0.6 \mu$, $z=500 \mu$, $V_{ds}=W_{00}=2.895 \text{ V}$).

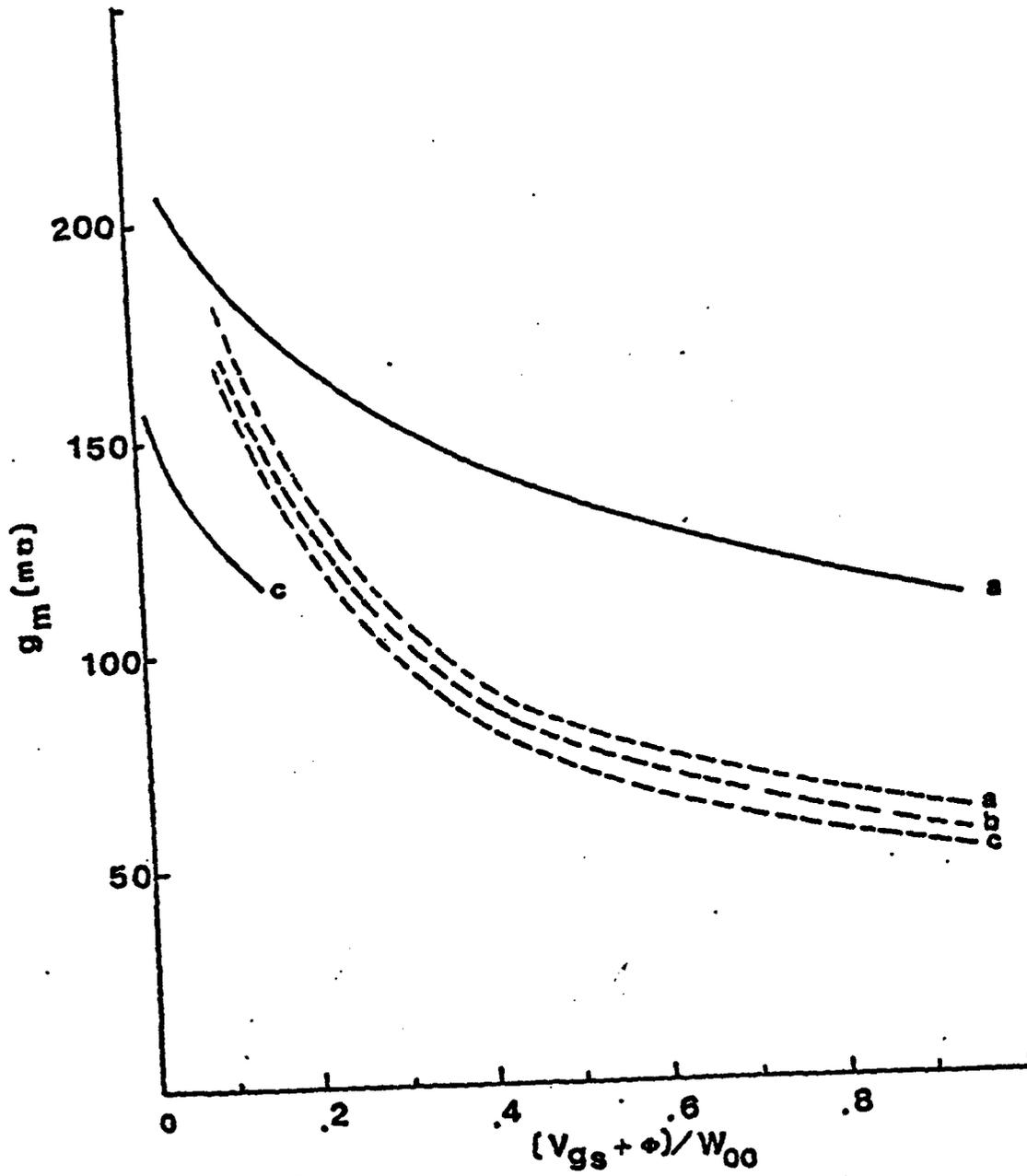




----- $|\alpha l| = 0.1$

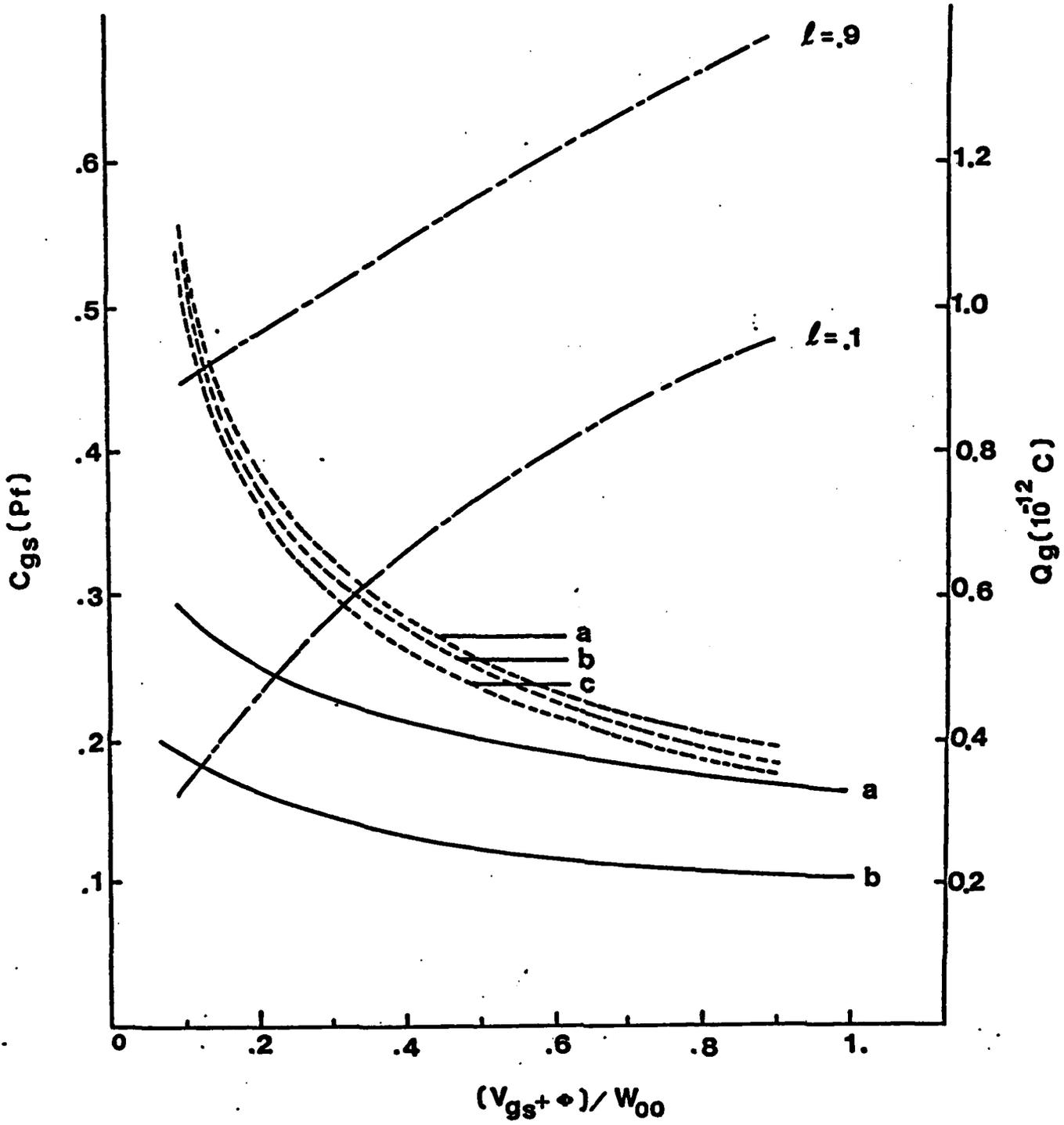
————— $|\alpha l| = 0.9$

a $\alpha > 0$
b $\alpha = 0$
c $\alpha < 0$

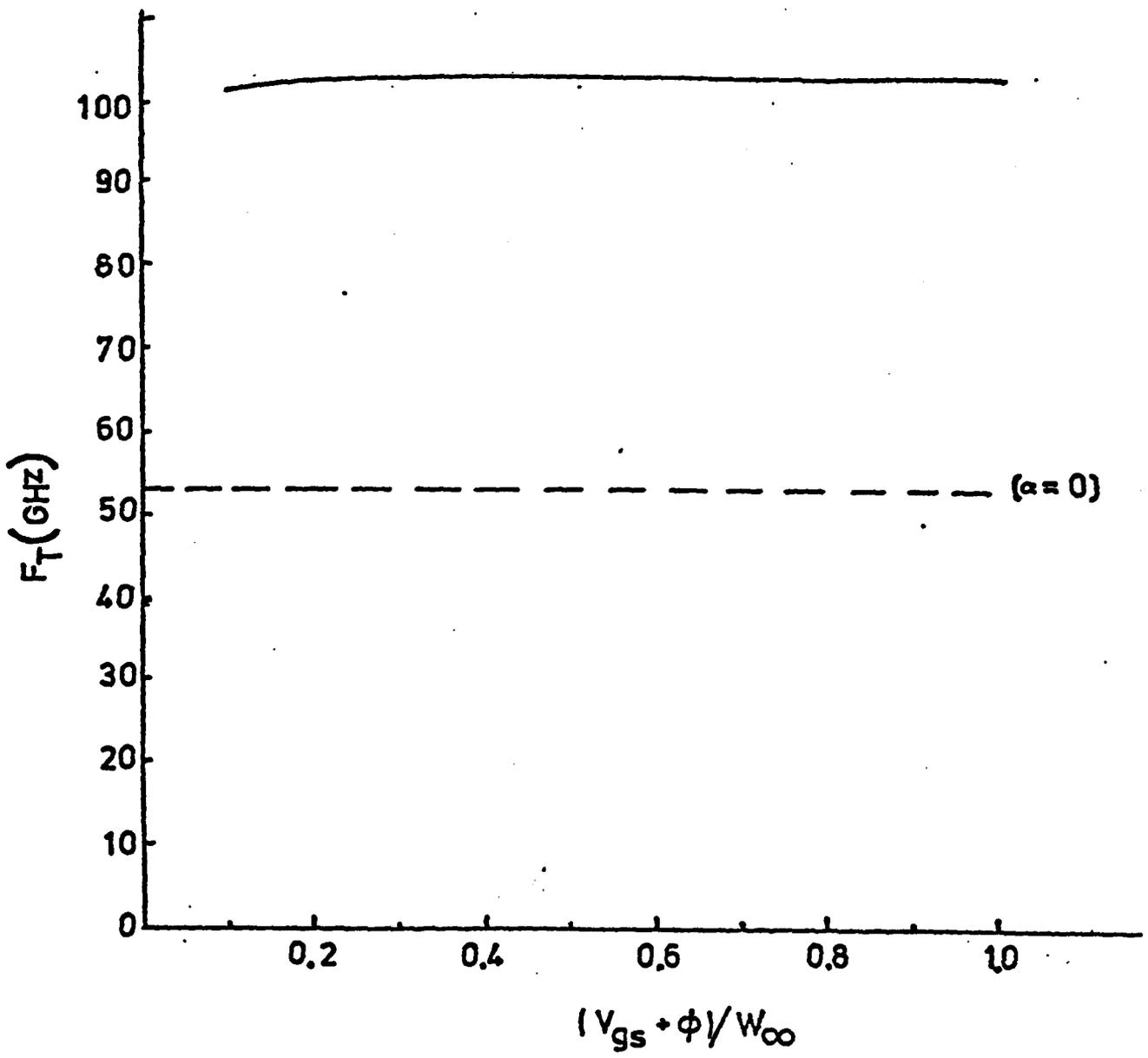


a $\alpha > 0$
 b $\alpha = 0$
 c $\alpha < 0$

— $|\rho l| = .9$
 - - - $|\rho l| = .1$
 - · - Q_g



----- $|\alpha| = 0.1$
----- $\alpha = 0.9$



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Velocity Overshoot of Electrons in GaAs with Space Charge and Non-Uniform Field

By

YEN-CHU WANG and ZHENG-AN QIU²⁾

Simple analytical transport model is used for self-consistently calculating velocity overshoot under constant current. It is shown that space charge and non-uniform field drastically reduce the overshooting velocity and greatly elongate its distance of effectiveness.

Ein einfaches analytisches Transportmodell wird für eine selbstkonsistente Berechnung des Geschwindigkeitsüberschusses bei konstantem Strom benutzt. Es wird gezeigt, daß Raumladung und ein ungleichförmiges Feld den Geschwindigkeitsüberschuß drastisch reduzieren und seine Wirkungsdistanz weit ausdehnen.

1. Introduction

In the recent development of high-speed GaAs logic and high-frequency analog devices, interests are focused in the possibility of overshooting the electron drift velocity in a sufficiently short submicron device. When space charge limited current is also considered, the so-called ballistic transport device has become popular among researchers. Previous papers dealing with uniform field and therefore neglecting the space charge effect obtained at room temperature rather high overshooting velocities (5 to 7.5×10^7 cm/s) within distances from 0.2 to $0.4 \mu\text{m}$ for a constant field ranging from 10 to 25 kV/cm [1 to 4]. Since in small devices, electron density varies significantly close to the cathode contact, space charge and non-uniform field have to be considered self-consistently. Also important is the fact that capacitive current in small device in transient state must be accounted for. Previous work [5] dealt with non-uniform field non-self-consistently and the obtained results are difficult to compare.

2. Analysis

We will use the simple analytical transport model [4] to describe the electron transient behaviour. In this monoenergetic model approximate energy-related momentum and energy relaxation times are assumed to be valid under the condition that the electron energy is initially (at $t = 0$) maintained at a level higher than the optical phonon energy $\hbar\omega_p$, in order to avoid the unphysical negative energy relaxation time [6]. This initial level is found to be $4\hbar\omega_p = 0.148$ eV, and at this level the energy loss rate per unit time gives at $t = 0$ the correct value of zero before excitation and correct values after excitation for higher energy. The normalized balance equations are given

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by

$$\frac{dv}{dt} = a_1 Q(\varepsilon) E - b_1 f(\varepsilon) v, \quad (1)$$

$$\frac{d\varepsilon}{dt} = a_2 v E - b_2 g(\varepsilon), \quad (2)$$

where v , ε , and E are, respectively, the average electron drift velocity of electrons, energy, and field. The detailed description of the energy functions has appeared elsewhere [4]. In these equations the (thermal) diffusion effects are assumed to be negligible because diffusion is a slow process in a transient problem such as the one treated here.

The space charge effect is governed by the Gauss equation

$$\frac{\partial E}{\partial x} = \frac{\rho}{\varepsilon_0}, \quad (3)$$

where ρ is the charge density and ε_0 the dielectric constant. Here we consider an undoped GaAs device. The total current is given by

$$J(t) = \varepsilon_0 \frac{\partial E}{\partial t} + \rho v. \quad (4)$$

Substituting (3) into (4) we get

$$\frac{dE}{dt} = \frac{J(t)}{\varepsilon_0}, \quad (5)$$

where the total derivative $d/dt = \partial/\partial t + v \partial/\partial x$.

Equations (1), (2), and (5) constitute the three governing equations provided $J(t)$ is prescribed. The initial conditions are as follows: $v(0) = E(0) = 0$ and $\varepsilon(0) = 0.148$. The current is assumed to be $J(t) = J_0(1 + \alpha \cos \omega t) \theta(t)$, where $\theta(t)$ is the unit-step function, J_0 the bias current, and α the ac amplitude. The velocity overshoot results will be given as a function of x or t with total current J_0 and α as parameters. The ac frequency of the excitation current is assumed to be $\omega = 2\pi f$ where $f = 100$ GHz. The temperature is assumed to be 300 K.

3. Numerical Results

Fig. 1 shows the velocity overshoot for given bias current J_0 versus length for $\alpha = 0$.

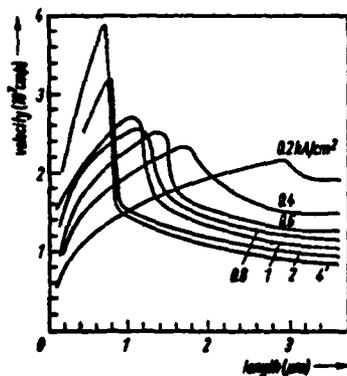
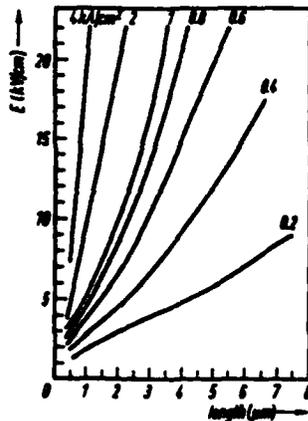


Fig. 1. Velocity overshoot vs. distance (length) for dc current excitation only ($\alpha = 0$). The bias dc current density J_0 is a parameter

Fig. 2. Field vs. distance for $\alpha = 0$ with J_0 as a parameter

When compared with the velocity overshooting curves for constant field [4] it is evident that the space charge field causes (i) lower peak velocities and that (ii) peaking occurs at much longer time and distance. Thus a submicron device will have much larger transit time than previously anticipated because the peaking velocity is reduced to $(2 \text{ to } 4) \times 10^7$ cm/s, if the space charge and capacitive current are properly accounted for, as is presented here. Collision will remain dominant even in submicron devices due to space charge and non-uniform field [7].

Fig. 2 shows the non-uniform field versus length with the total current as a parameter for $\alpha = 0$. Fig. 3 shows the $v-E$ curves for given device length for $\alpha = 0$. For long devices the $v-E$ behaviors are very close to the equilibrium curve, whereas for short devices they deviate from the steady state due to the effect that transit times for short length become comparable to energy relaxation time [8]. There is a striking difference between this and its counterpart with constant field [8], i.e., velocities decrease drastically beyond the peaks when a non-uniform field is considered as shown in Fig. 3, but they become almost saturated beyond the peaks for the constant field case.

In Fig. 4 the total current is plotted against the voltage for different device lengths for $\alpha = 0$. For a $0.2 \mu\text{m}$ device the current behaves like half-power function of voltage at low current, it increases fast at medium current levels and then its increase slows at high current level. For a $1 \mu\text{m}$ device the situation is quite different in that the current increases more slowly and tends to saturate at high current level. Fig. 5 presents the length versus transit time relationship.

Fig. 6 to 10 give the corresponding curves for $\alpha = 1.0$. In this case the ac current affects the velocity overshoot drastically as evident from comparison of Fig. 6 and 1.

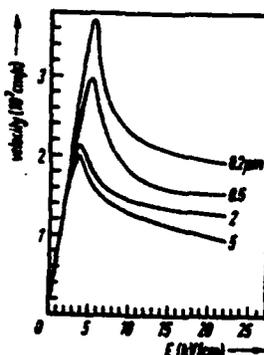


Fig. 3

Fig. 3. Velocity vs. field for variable device length and $\alpha = 0$

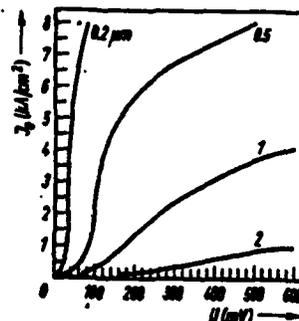


Fig. 4

Fig. 4. dc current density J_0 vs. voltage U for $\alpha = 0$ and different device length

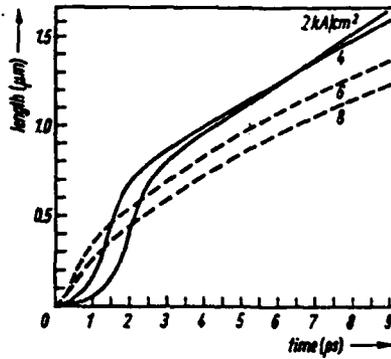


Fig. 5

Fig. 5. Device length vs. transit time for $\alpha = 0$

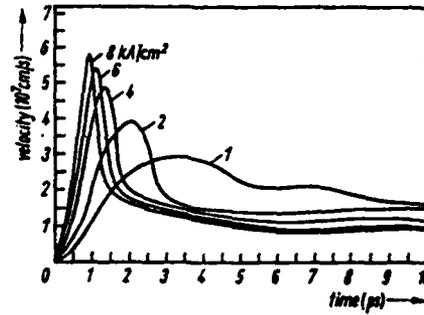


Fig. 6

Fig. 6. Velocity overshoot vs. transit time for both dc and ac current excitation ($\alpha = 1.0$) with J_0 as a parameter

Non-uniformity of field versus transit time as illustrated in Fig. 7 shows that non-uniformity of field is greatly reduced by the ac current excitation characterized by α and disappears at low bias current J_0 . Fig. 8 shows that ac current enhances the peak velocity for short devices. For a $0.4 \mu\text{m}$ device the peak velocity is about $4 \times 10^7 \text{ cm/s}$ at a threshold field of 10 kV/cm . These values are larger than those for the case of $\alpha = 0$ (Fig. 3). Fig. 9 shows the bias current J_0 as a function of voltage for different device lengths. When it is compared with Fig. 4 (for $\alpha = 0$), we see that there the voltage drop across the device corresponding to the same bias current is smaller due to the ac current contribution. In Fig. 10 length versus transit time is shown.

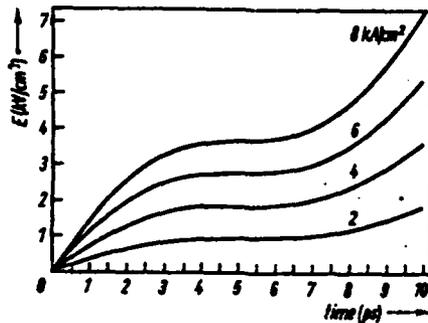


Fig. 7

Fig. 7. Field vs. transit time for $\alpha = 1.0$

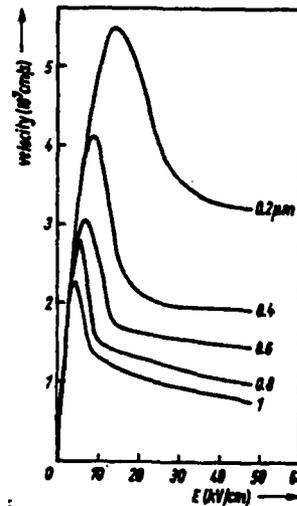


Fig. 8

Fig. 8. Velocity vs. field for $\alpha = 1.0$ and different length

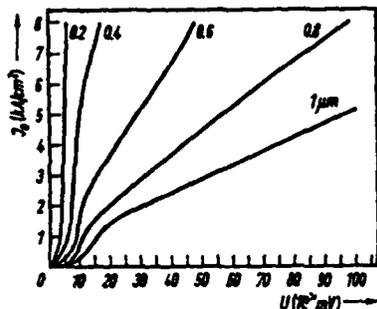


Fig. 9

Fig. 9. dc current density J_0 vs. voltage U for $\alpha = 1.0$

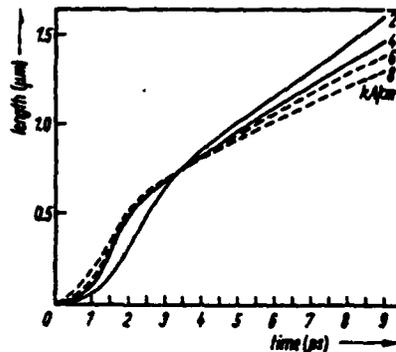


Fig. 10

Fig. 10. Length vs. transit time for $\alpha = 1.0$ and different J_0

4. Conclusions and Remarks

In conclusion we have found that for a realistic analysis of small devices for which both the space charge and non-uniform field effects are accounted, the average velocity of electrons overshoots only mildly at rather large distance when there is no ac current excitation ($\alpha = 0$), contrary to that for the constant field case. Thus collision remains important for submicron devices. In this case the $U-E$ characteristics also show different behavior in that though the velocity increases with decreasing length due to non-equilibrium, negative resistance regions exist. The J_0-U curves show a great deal more saturation tendency than predicted by the "ballistic" theory. In the case of dc plus ac current excitation ($\alpha = 1.0$), the ac current greatly modifies the field to such an extent that the field becomes more uniform for decreasing bias current.

It is beneficial, before this work is concluded, to remark on the special choice of 0.148 eV, instead of 0 eV, as the initial electron energy at $t = 0$. As is presented in [4], the energy loss rate is dominated by longitudinal polar optical mode. Unfortunately, relaxation times valid for all electron energies do not exist for polar optical modes due to partial inelasticity of scattering, although they are very useful in describing the transport properties [9]. For $\epsilon \gg \epsilon_p$ or $T, T_e \gg \theta_D$, where $\epsilon_p = \hbar\omega_p$ is the longitudinal polar optical phonon energy at $k = 0$, T_e the equivalent electron temperature, and θ_D the Debye temperature (418 K for GaAs), the scattering is elastic so that relaxation times are well defined. Our energy relaxation rate formula [4] obtained from solving Boltzmann's equation by use of a drift Maxwellian distribution, whereas valid for large energy, does not hold for $\epsilon < \epsilon_p$ (near $\epsilon = 0$) [9]. In this low-energy region the formula without correction factor would give $(\epsilon - \epsilon_L) \tau_e^{-1} \sim \ln(4\epsilon/\epsilon_p) \sqrt{\epsilon} \rightarrow -\infty$ so that $\tau_e^{-1} \rightarrow \infty$ as $\epsilon \rightarrow 0$, a result which so severely overestimates the contribution of the low-energy electrons to the energy loss rate as to cause infinite energy gain. In actuality electrons with $\epsilon \leq \epsilon_p$ cannot emit phonons, thus they should not contribute to spontaneous emission and cannot gain energy either. To circumvent the unphysical energy gain difficulty we postulate that the minimum energy of electrons in our simplified model should at least be ϵ_L , the thermal lattice energy, i.e., before entering from the cathode into the GaAs medium, an electron should have certain thermal energy although the field there is zero (e.g., n^+nn^+ structure). To satisfy the non-emission condition for low-energy electrons, we further assume that $\epsilon > \epsilon_p > \epsilon_L$ at 300 K and require that $(\epsilon - \epsilon_L) \tau_e^{-1}$ be zero at the cathode. This demands a

correction factor such that

$$(\epsilon - \epsilon_L) \tau_s^{-1} \sim \left(1 - \frac{r\epsilon_p}{\epsilon}\right)^n \frac{\ln(4\epsilon/\epsilon_p)}{\sqrt{\epsilon}}. \quad (6)$$

To fix the constants r and n we follow Ridley's arguments [6], i.e., they should be so chosen that when ϵ becomes large, correct energy loss rate is obtained. He suggested that $r = 4$ and $n = 2$. The initial energy is therefore taken to be $4\epsilon_p = 0.148$ eV instead of the commonly assumed 0 eV in typical Monte-Carlo calculations.

A possible physical explanation is as follows: Although initially the electron has no drift velocity, $v(0) = 0$ since $E(0) = 0$, and therefore no drift energy, continuity of current however requires the diffusion current to be present at the cathode where an electron temperature gradient exists; the cathode does not require the presence of infinitely large electron density as commonly assumed. This implies that a thermal spread of the cathode exists, inside of which the electron temperature must be higher than 300 K. As soon as the electron enters the medium, it picks up the drift energy at the high rate proportional to v^2 ; thus the further it moves away from the cathode, the more predominant the drift energy is, until it reaches the anode (which we do not consider here), where the velocity and field again vanish and the diffusion current takes over as the total particle current as before. It may be added that the diffusion current arises from the fact that an electron, shortly before entering the anode, has very high temperature gained from the field, thus a temperature gradient exists at the anode.

Once the initial energy is properly determined, the detailed diffusion process on the boundary, where electrons leave or enter, can be disregarded in our simplified model. It remains to be explained as to why diffusion can be neglected in the n-GaAs region. It is not difficult to include diffusion terms in the balance equations (1) and (2), but the transient analysis becomes tedious. Instead of doing this, one can include the diffusion current J_D in the phenomenologic current equation, which is somewhat easier in getting order-of-magnitude comparison. J_D is proportional to the gradient of density ρ governed by (3) and the field-dependent diffusion coefficient $D(E)$. To a first approximation, Fig. 2 for dc current excitation only shows that the field E is almost linear; thus $\partial\rho/\partial x$ is not large, justifying negligibility of J_D . Fig. 7 shows that for dc plus ac excitation ρ does indeed vary, but for the high-field region $D(E)$ decreases drastically and J_D still may be small enough to be negligible. It is noticed, however, that near the cathode, where E is small and therefore $D(E)$ large, diffusion current may generally become important. But even for this situation our special initial condition seems to work to our advantage giving small gradient of density thus favoring drift current.

Acknowledgement

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(Received September 23, 1982)

Coupling activities

As reported in the intern reports we have had several coupling activities with other government laboratories. With Harry Diamond Laboratories we have fabricated ohmic contacts on superlattice structures. With the Naval Research Laboratories we have been investigating the annealing and characterization of high energy implants. In addition, we have been investigating DLTS spectra of irradiated materials . One of these irradiation studies has been concluded and a paper is attached.

TRANSIENT CAPACITANCE MEASUREMENTS ON

NEUTRON IRRADIATED GALLIUM ARSENIDE*

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Abstract

Deep Level Transient Spectroscopy (DLTS) has been used to study the nature of the neutron-irradiation induced defects in GaAs. The measurements were made on a group of Schottky barrier samples on n-type ($1.2 \times 10^{17} \text{ cm}^{-3}$) LPE GaAs. The samples were exposed in a reactor to neutron fluences from $5 \times 10^{14} \text{ cm}^{-2}$ to $5 \times 10^{16} \text{ cm}^{-2}$. DLTS measurements on unirradiated samples revealed no electron traps with concentrations greater than $2 \times 10^{13} \text{ cm}^{-3}$. The samples irradiated to 5×10^{14} and $2 \times 10^{15} \text{ cm}^{-2}$ were studied as irradiated and after annealing to temperatures of 500C. The positions of the peaks studied here are sensitive to the electric field in the depletion layer. Evidence is also presented to demonstrate that the strength of the electric field enhanced emission effect decreases on annealing. The spectra for samples annealed to 500C contained three lines at .38, .56 and .78 eV below the conduction band. The line at .78 eV was the most prominent of these, and its line shape was found to within about 10% of that expected for a point defect.

Introduction

Following the observation by Electron Paramagnetic Resonance (EPR) that the As_{Ga} antisite in GaAs could be introduced by neutron irradiation (1) there were several attempts to determine whether the Deep Level Transient Spectroscopy (DLTS) line EL2 is also produced by neutron irradiation (2,3,4). G. M. Martin and S. Makram-Ebeid reported observing that neutron-irradiation produced a broad band and some of its changes on annealing (2,4). The general conclusion from these experiments was that the introduction rate for EL2 was much smaller than the introduction rate for the As_{Ga} antisite found by EPR. The main feature of the DLTS spectra was a broad line centered about -40C with some small shoulders. A broad line like this is assumed to be associated with complex defects (5) rather than a well defined point defect.

*Supported in part by the Office of Naval Research.

There are a number of reasons for making the in-depth DLTS study of the broad neutron-irradiation induced line which is reported here. One is the fact that the introduction rate (1) for this line is near to the rate found in the EPR experiments on the As_{Ga} antisite. This becomes even more compelling when it is understood that the nature of the electron wavefunction associated with the EPR signal implies that the EPR experiments are not very sensitive to whether the antisite is complexed with another defect or a donor. This broad line is also the dominant electron trapping feature observed in the upper half of the band gap in DLTS experiments.

Liquid Phase Epitaxial (LPE) samples were chosen for this experiment because it is possible to grow LPE GaAs which is essentially free of electron traps. This eliminates the need to subtract background signals from defects present in the starting material. The nature of the radiation induced defects may also be changed by interactions with defects already present in the starting material. Heavily doped (1.2×10^{17} Sn cm^{-3}) layers were chosen in order to use a range of fluences similar to those used in the EPR studies. At least 1×10^{15} neutrons cm^{-2} are needed to obtain a reasonable signal to noise ratio in EPR work, while fluences much higher than this are expected to compensate even heavily doped GaAs making conventional DLTS experiments difficult.

Experiment

The samples used in this experiment were 250 micrometer diameter gold Schottky diodes formed on a 10 micrometer thick n-type (1.2×10^{17} Sn cm^{-3}) LPE grown GaAs layer. Several GaAs chips were prepared each with about ten diodes. Each chip was irradiated in a reactor with a different neutron fluence to obtain a group of samples with fluences between 5×10^{14} and 5×10^{16} neutrons cm^{-2} . The neutron irradiations were carried out by E. Weber in a manner similar to that used by him to prepare samples for EPR experiments. The thermal annealing treatments were carried out in a hydrogen atmosphere after stripping off the gold Schottky metalization. Only those samples with fluences of 5×10^{14} and 2×10^{15} cm^{-2} are reported here as the others were rendered semi-insulating by the irradiation.

The DLTS measurements were carried out with a one MHz capacitance meter by applying a quiescent reverse bias and then periodically applying a voltage pulse to fill the electron traps. A computer controlled data acquisition system was used to set the temperature and to digitally record the capacitance transient after each filling pulse. The difference between the capacitance at times T_1 and T_2 was determined by a computer program to simulate a boxcar spectrum. The spectra generally were recorded from liquid nitrogen temperatures to about 420 K. C-V data were measured at several temperatures to obtain the capacitance at the quiescent reverse bias used during the DLTS measurements and to calculate the free carrier concentrations.

Results

The quality of the LPE layers was checked prior to the neutron irradiations by measuring DLTS and C-V data which indicated that the electron trap concentration was less than 2×10^{13} cm^{-3} . Layers with carrier concentrations of 1.2×10^{17} cm^{-3} were chosen in order to use neutron fluences near those used in EPR experiments on the As_{Ga} antisite.

Simulated boxcar spectra for samples irradiated to fluences of 5×10^{14} and 2×10^{15} neutrons cm^{-2} are illustrated in Figs. 1 and 2 respectively with $T_1=5ms$ and $T_2=50ms$. The DLTS spectra shown in Fig. 1a is typical of those often observed for neutron irradiated GaAs in that it is very broad.

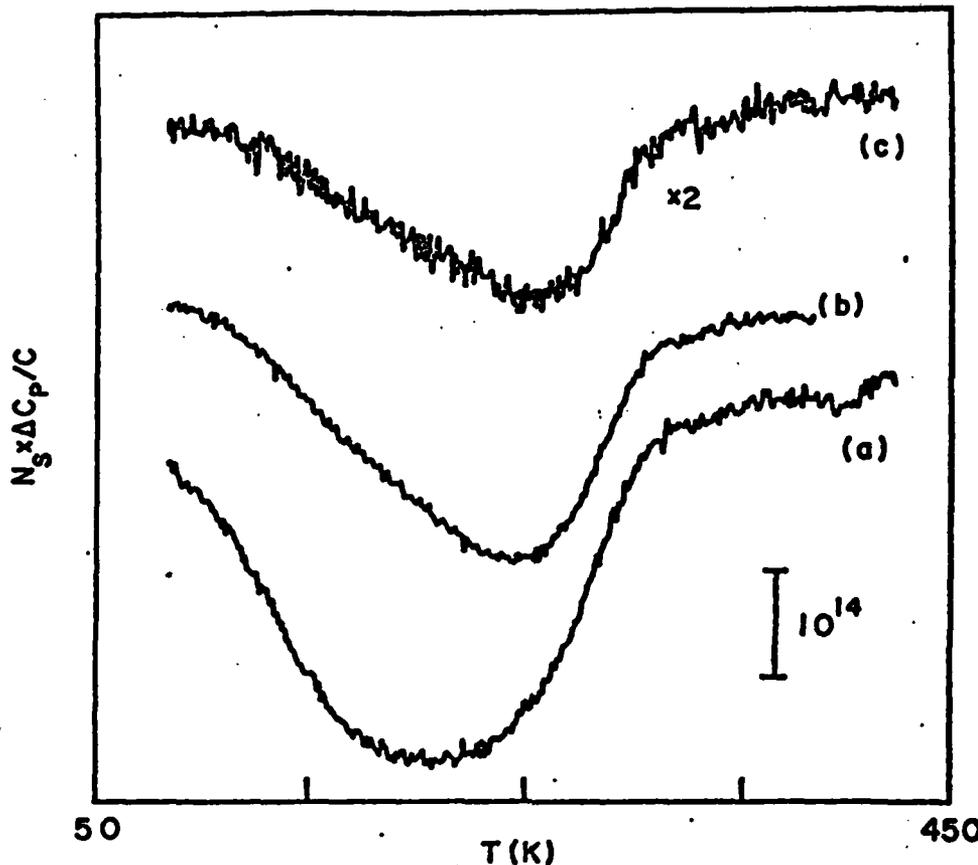


Fig. 1. The electric field dependence of a sample neutron irradiated to $5 \times 10^{14} \text{ cm}^{-2}$. a: bias = 3 volts, pulse to zero bias; b: bias 1 volt, pulse to zero bias; c: bias = 3 volt pulse height 1 volt.

The full width at half the peak amplitude for this line is about 150K which is four to five times broader than the lines observed for point defects. The width is a sign that a complex defect is involved in the trapping. These data were obtained with a 3 volt reverse bias and by pulsing to zero bias to fill the traps. As a further study of the sample the spectra in Fig. 1b was recorded with a one volt bias and a zero bias filling pulse. The peak in Fig. 1b is at a higher temperature than that in Fig. 1a, suggesting either a distribution of defects which varies with depth in the sample or that the emission rate in Fig. 1a was enhanced by the larger average electric field used in that measurement. To determine which effect is responsible for the peak shift, the data in figure 1c were measured with a 3 volt reverse bias and a one volt high filling pulse to obtain the same average electric field used in Fig. 1b, but over a different sample volume. Since almost identical spectra are found in Figs. 1b and 1c the conclusion is that the large average electric field used for the data in Fig. 1a enhanced the emission rate and caused the peak to shift to lower temperatures.

An estimate of the number of defects, N_t , can be made by using

$$N_t = F \Delta C_p N_s / C_0 \quad (1)$$

ΔC_p is the peak amplitude, C_0 the capacitance at the quiescent reverse bias, N_s is the free carrier concentration and F is a constant. Poisson's equation can be used to evaluate F for the case of a point defect with an exponential decay. In general F depends on the bias, pulse height, built in

potential, defect energy as well as T_1 and T_2 . For the various conditions used in these experiments the appropriate values of F ranged from 5 to 20. Using these assumptions results in a calculated defect concentration of $2 \times 10^{15} \text{ cm}^{-3}$ for Fig. 1 which corresponds to a defect introduction rate of 4.

This should be an underestimate of the actual value because the analysis ignores the fact that the line results from the distribution of defects. Since the entire capacitance transient was recorded, it is possible to measure C_T , the amplitude directly after the filling pulse, and to use it in place of ΔC_p in Equation 1 along with an appropriate value of F to find $N_t = 7 \times 10^{15} \text{ cm}^{-3}$. This gives an introduction rate of 14, which is probably a better estimate of the introduction rate as it represents an integration of all the transients under the peak.

Data on the annealing behavior of a sample irradiated to a fluence of $2 \times 10^{15} \text{ neutrons cm}^{-2}$ are presented in Fig. 2. The unannealed sample is shown in Fig. 2a along with the results of annealing it at 400C, 450C and 500C in Figs. 2b, 2c and 2d. While all these curves were recorded with the same bias and pulse height, measurements were also made with a number of other bias and pulse height combinations. The results of those tests indicated

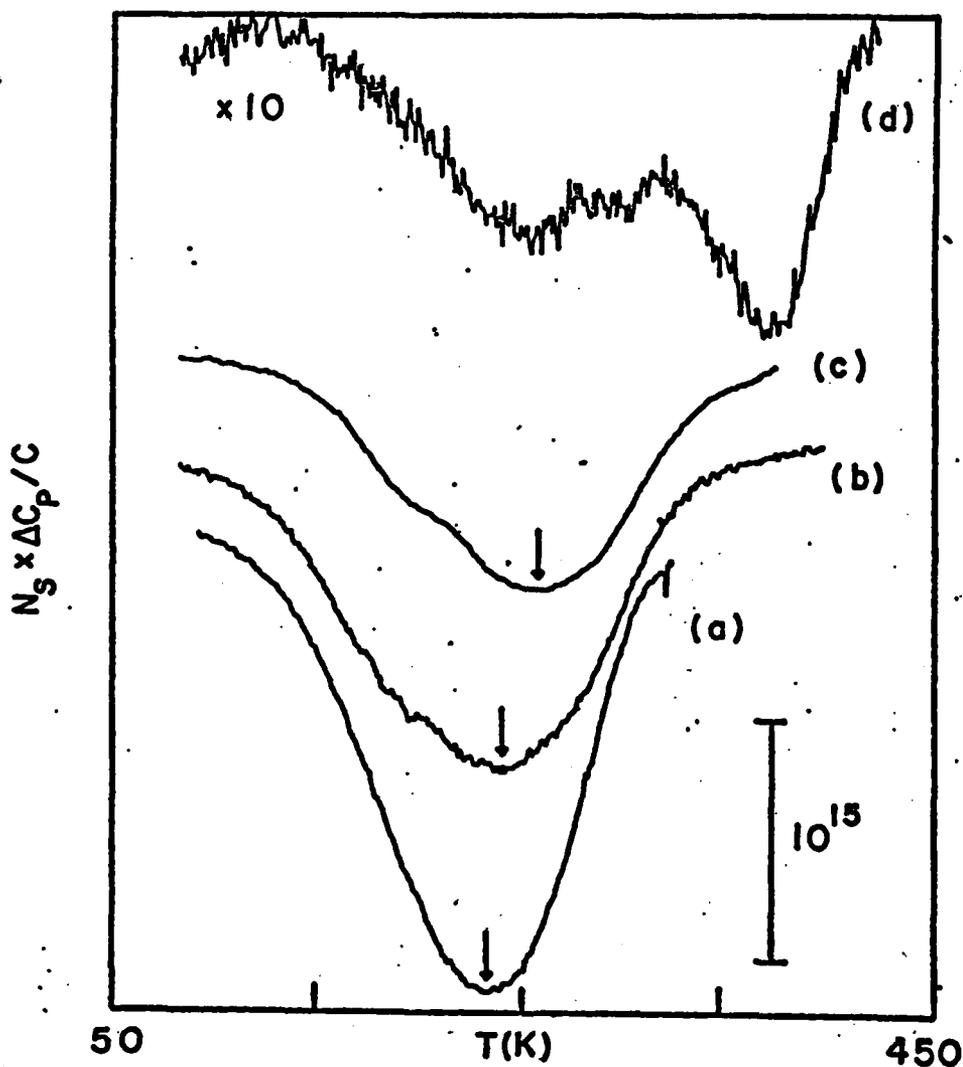


Fig. 2. Annealing data for a sample irradiated to $2 \times 10^{15} \text{ neutron cm}^{-2}$. a: unannealed; b: 400C; c: 450C; d: 500C.

that the emission rates were electric field enhanced for all but the sample annealed at 500C. The data shown in Fig. 2 are evidence for a weakening of the processes responsible for the electric field enhancement effects. The electric field applied during these experiments increased on annealing because the depletion layer width decreased due the free carrier concentration recovering from 3.6×10^{16} to $9.5 \times 10^{16} \text{ cm}^{-3}$. The arrow on each of the curves in Fig. 2 indicates the position of the peak of the spectra and they show that the peak is slowly moving to higher temperatures on annealing. This signifies a decrease in the emission rate at a given temperature.

A further examination of Fig. 2 indicates the growth of a shoulder on the low temperature side of the 400C and 450C data. A high temperature shoulder was also found on the 450C data though it cannot be seen in Fig. 2. The low temperature shoulder did not exhibit any evidence of electric field dependence. The high temperature shoulder was not distinct enough to determine if it was field dependent.

The most significant change in the spectra occurred after annealing at 500C. The intensity of the lines decreased significantly and a new line appeared at the high temperature end of the spectra. This was the first observation of a peak this high in temperature in these samples. The shape of the line agrees well with that predicted by a point defect model. A similar line is also observed in samples irradiated at higher fluences and annealed at 500C to restore their conductivity. The

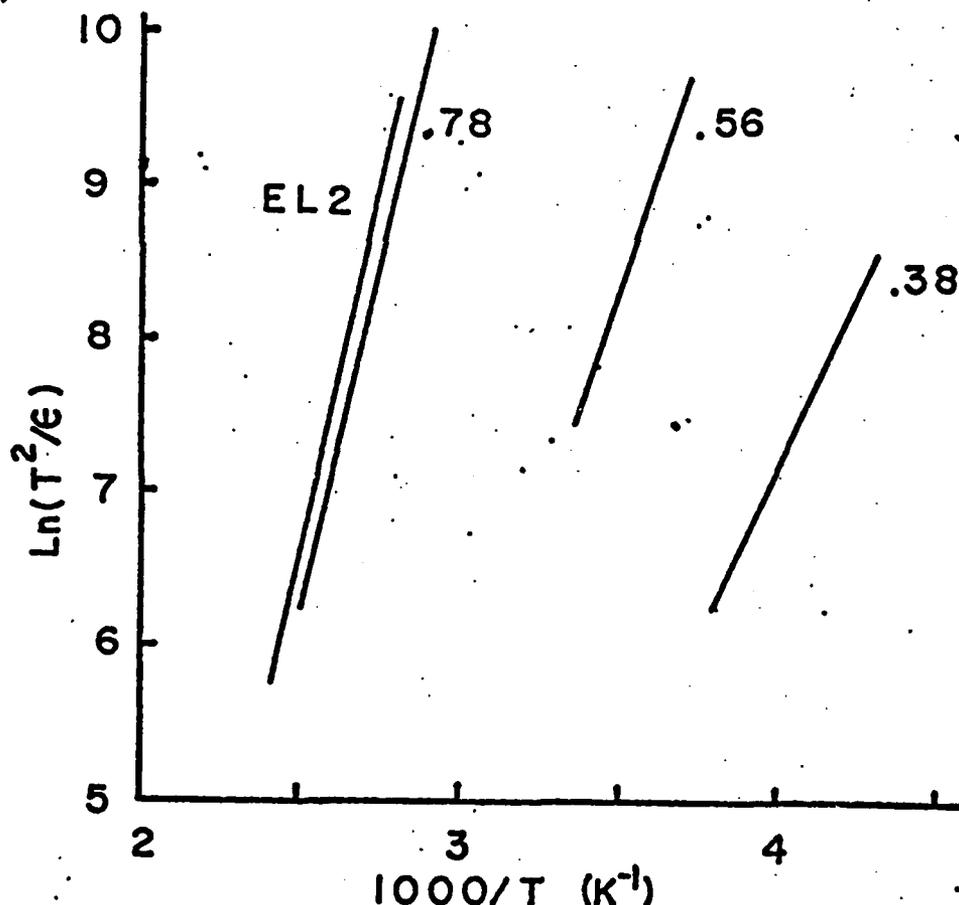


Fig. 3. Arrhenius plot for the spectra in Fig. 2c with $E_a = .38 \text{ eV}$, $A = 3.3 \times 10^4 \text{ sec}^{-1} \text{ K}^{-2}$; $E_a = .56 \text{ eV}$, $A = 1.4 \times 10^6 \text{ sec}^{-1} \text{ K}^{-2}$; $E_a = .78 \text{ eV}$, $A = 1.3 \times 10^7 \text{ sec}^{-1} \text{ K}^{-2}$, and with literature values of $E_a = .825$, $A = 2.9 \times 10^7 \text{ sec}^{-1} \text{ K}^{-2}$ for EL2 (6).

annealing process was checked on unirradiated samples to confirm that the new line was not introduced during the processing.

An Arrhenius plot for the lines in Fig. 2c is shown in Fig. 3 along with a line at the position expected for EL2. The data in this experiment were fit to

$$\epsilon = AT^2 \exp(-E_a/K_bT). \quad (2)$$

The high temperature line in Fig. 3 has $E_a = .78$ eV and $A = 1.3 \times 10^7$ which are near the values of $E_a = .825$ eV and $A = 2.9 \times 10^7$ often quoted for EL2 (6). The intensity of the .78 eV line corresponds to a defect concentration of $1.5 \times 10^{15} \text{ cm}^{-3}$. This needs to be compared with a defect concentration estimated to be between 1.5×10^{16} and $2.5 \times 10^{16} \text{ cm}^{-3}$ for the unannealed data in Fig. 2a.

Discussion

The results presented here give some new insight into the nature of the broad line observed in DLTS experiments on neutron irradiated GaAs. The first point to note is that the position of the peak for both samples presented here is very sensitive to the strength of the electric field in the junction. To estimate the position of the peak at zero field, the temperature of the peak for the sample shown in Fig. 1 was plotted for several emission rates against the applied field which ranged from 1.2×10^5 to 1.8×10^5 volts/cm. On extrapolating the data to zero electric field the lines fell in the temperature range where EL2 is found. While this suggests that the line may be a field shifted EL2 signal this is not likely because EL2 has not been observed to be sensitive to fields as low as 1.2×10^5 volts/cm (7). In addition when the line width is extrapolated to zero field it is too large for EL2.

The line width suggests that the line is associated with a complex defect with a distribution of energies. To obtain an estimate of the width of the defect distribution a program was developed to find the line shape that results when several point defects with varying energies and concentrations are added together. The energies and concentrations of the model lines were adjusted to obtain a good fit to a spectrum measured at low reverse bias for the sample in Fig. 2. A distribution extending from about .46 eV to .72 eV with a full width at half amplitude of .1 eV was found to give good fits to the line shapes measured for a variety of emission rates. The peak of the distribution was near the energy obtained in an Arrhenius plot of the DLTS line.

Another important feature of the data is the decrease in the strength of the field effect on annealing. This suggests that the strength of the mechanism is tied to the complexes which are being annealed. The data presented here indicate a considerable change takes place on annealing at 500C compared to the changes produced on annealing at 400C and 450C. Because of this rapid change between 450C and 500C it was not possible to track the development of the peak at .78 eV in the 500C data. This line may result from a weakening of the field effect or it may indicate the development of a point defect as the complexes break up. Since the DLTS data still show a broad peak at low temperatures and the free carrier concentration is not fully recovered at 500C, there are a number of reasons to expect that the .78 eV line may be due to the defect associated with EL2 complexed with another defect.

Several comparisons may be made between these results and those obtained by EPR measurements of the As_{Ga} antisite. The introduction rate found here is between 4 and 12 cm^{-1} which compares well with the rate of 10 cm^{-1} found for EPR data on the As_{Ga} antisite in semi-insulating samples irradiated at the same time (8). A review of the EPR data for the annealing behavior of As_{Ga} antisites found in as grown material and for antisites produced by either neutron irradiation or plastic deformation suggests that antisites exist in a variety of complexes with different thermal stabilities (9). The DLTS spectra presented here show neutron-irradiation induced defects which anneal out between 400 and 500c. A similar annealing stage has been observed by EPR for neutron irradiated GaAs (1).

In summary, the field dependence of the broad neutron irradiation induced DLTS line and the appearance on annealing of a line near the EL2 position suggest that the irradiation has produced the defect responsible for the EL2 line but complexed with other defects. These other defects result in a line which is very sensitive to the applied electric field. In addition, we conclude that these DLTS results have many of the same properties as the As_{Ga} antisite measured by EPR.

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