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ADVANCED ULTRA-VIOLET (UV) AIRCRAFT FIRE DETECTION SYSTEM

VOL III - GROUND SUPPORT EQUIPMENT (GSE) FOR SYSTEM CHECK-OUT

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The objective of this program was to utilize ultra-violet (UV) radiation technology to provide advanced means of detecting fire hazards more reliable, and more rapidly than current thermally activated continuous cable type system. This volume, Volume III of three volumes, provides detail information on the Ground Support Equipment (GSE) for automatic and manual checkout of the system.

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FOREWORD

The work reported herein was performed in accordance with Air Force Contract F33615-77-C-2029 under the direction of the Fire Protection Branch (AFWAL/POSH) of the Fuels and Lubrication Division, Aero Propulsion Laboratory, Air Force Wright Aeronautical Laboratories, Wright-Patterson Air Force Base, Ohio, under Project 2348, Task 01, Work Unit 02, with Mr G.T. Beery and Mr T.A. Hogan, AFWAL/POSH, as Project Engineers.

This report is the result of utilizing ultra-violet (UV) radiation technology in the development and flight testing of an advanced aircraft fire detection system.

The contractor was General Dynamics, Fort Worth Division, Fort Worth, Texas. Mr. R.J. Springer, Program Manager, directed the efforts of P.H. Lang, W.B. Kirk, B.B. Witte, D.C. Nelson, and J. Phillips. The overall effort was under the supervision of Mr. C.E. Porcher, Manager, Propulsion and Thermodynamics Section. Graviner Ltd./HTL Industries, General Dynamics subcontractor, accomplished the design, fabrication, environmental testing and support for the flight test phase of the program. Graviner/HTL's efforts were directed by Mr. S.P. Robinson who was supported by P.H. Sheath and D.J.V. Smith. Sacramento Air Logistics Command (SM-ALC) provided the F-111 aircraft and support for the flight test phase of the program. Mr B.W. Nichols, SM-ALC Engineering, coordinated the flight testing at McClellan Air Force Base.

This report describes the results of work conducted during the period of 15 December 1977 to 26 October 1981.

This is Volume III of three volumes. Volume I describes the overall work of the program which includes the results of the flight test phase. Volume II contains a description and details of the system circuit and software design. Volume III contains a description and details of the Ground Support Equipment (GSE) which is used as a fault diagnostic maintenance tool.

TABLE OF CONTENTS

SECTION	TITLE	PAGE
1.0	INTRODUCTION	1
2.0	SYSTEM DESCRIPTION	3
	2.1 CCU-G.S.E. Connection and Operation	3
	2.1.1 CCU on Aircraft	3
	2.1.2 CCU on Bench	5
	2.1.3 Ground Support Equipment	5
	2.2 Description of Tests	8
	2.2.1 Data Read	8
	2.2.2 Control Unit Test	9
	2.2.3 U.V.-Head (Sensor) Tests	9
	2.2.4 Parametric Test	9
	2.2.5 Functional Test	9
	2.2.6 Data Analysis	10
3.0	SYSTEM METHOD	11
	3.1 Hardware	11
	3.1.1 Microprocessor Card	12
	3.1.2 Printer	12
	3.1.3 Cableforms	12
	3.1.4 Power Supply Side 1 and 2	13
	3.1.4.1 Power Supply Specification	13
	3.1.4.2 Power Supply Description	13
	3.1.5 Power Supply to CCU	14
	3.1.6 Battery Support	14
	3.1.7 Input/Output Decode	16
	3.1.8 U.V. Head Simultion	16
	3.1.9 Head/Drive Control and Supply	20
	3.1.10 Voltage and Timing Monitoring	20
	3.1.11 25 Second Timer	22

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TABLE OF CONTENTS (CONT'D)

SECTION	TITLE	PAGE
3.2	Software	22
3.2.1	Over View	22
3.2.2	The Microprocessor Card Utilization	25
3.2.3	Note on the Start Up Condition	26
3.2.4	Tests Description	27
3.2.4.1	Simulate Heads and Emitter Response Time	27
3.2.4.2	To Determine Whether the G.S.E. can Communite with the CCU	28
3.2.4.3	Read DATA from CCU	30
3.2.4.4	The CCU Tests	32
3.2.4.5	Sensor Test	35
3.2.4.6	Parametric Test	39
3.2.4.7	Functional Test	42
3.2.4.8	Data Analysis Program	48
4.0	OPERATING INSTRUCTIONS	55
5.0	CONCLUSIONS	57
	REFERENCES	59
APPENDIX A-1	Microprocessor Card	61
APPENDIX A-2	Printer	71
APPENDIX A-3	U.V. Head and Emitter Simulation Flow Diagram	87
APPENDIX A-4	CCU-GSE Communication Flow Diagram	91
APPENDIX A-5	List of Error Codes	101
APPENDIX A-6	CCU Test Flow Diagram	109
APPENDIX A-7	Sample Assembler Listing for Tests	125
APPENDIX A-8	Sensor Test Flow Diagram	135
APPENDIX A-9	Parametric Test Flow Diagram	143
APPENDIX A-10	Functional Test Flow Diagram	153
APPENDIX A-11	Data Analysis Flow Diagram	169
APPENDIX B	Operating Instructions	181

LIST OF FIGURES

FIGURE	TITLE	PAGE
2-1	GSE Connections Sequence	4
2-2	GSE Connection, 28V Supply	6
2-3	Block Diagram of GSE	7
3-1	CCU Power Supply Control Diagram	15
3-2	Battery Supply Diagram	17
3-3	I/O Port Arrangement	18
3-4	U.V. Head Simultion	19
3-5	Head/Drive Control and Supply Circuit	21
3-6	Check Points Monitoring Diagram	23
3-7	25 Second Timer Diagram	23
3-8	GSE Software Flow Diagram	24
3-9	BCD Subroutine Diagram	40
3-10	Time Share Diagram of the CCU	43
3-11	Control Unit Data - Memory Map	49
3-12	Program Operation	51

ACRONYMS

GSE	Ground Support Equipment.
CCU	Computer Control Unit.
CWU	Crew Warning Unit.
LRU	Line Replaceable Unit.
RAM	Random Access Memory.
ROM	Read Only Memory.
USA	United States of America.
RUNP	Run Program from Location 0000.
UV	Ultra Violet.
PROM	Programmable Read Only Memory.
MRD	Memory Read Line.
CS 1	Chip Select 1.
CS 2	Chip Select 2.
I/O	Input/Output.
2K	2000

SUMMARY

The Ground Support Equipment (GSE) described herein is a portable automatic manual check-out unit for the Advanced Fire Detection System (AFDS).

It performs three basic functions. Firstly, it reads out the stored data from the AFDS gathered during a flight. Secondly, it checks the operational capability of the AFDS and finally it identifies faulty line replaceable units.

This report is divided into the following sections:

Section 1 is the Introduction.

Section 2 is a Systems Design Description and describes functionally the Hardware and Software.

Section 3 is the Systems Method and describes the Hardware and Software in detail.

Section 4 is the Operating Instructions.

Section 5 contains the Conclusion.

From the four major sections it can be seen that the GSE has been designed successfully. This is not to say that the GSE could not have been designed better.

Some circuitry duplication was necessary due to two independent sides of the Computer Control Unit, System A.

The microprocessor card was bought ready built. The major part of the interfacing circuitry was wire-wrapped on two dual size eurocards for ease of modifications and there were many.

Several problems were encountered with the software. One of the major problems was that there was no clear cut ending to the particular test devised. Problems were also encountered due to the lack of microprocessor equipment. Finally, some problems also arose when the GSE was operated in the U.S.A. during the CCU flight trials.

It was proposed that for production the specification of the GSE would change, which would result in the GSE being simplified. If the production quantity is small then the undesired functions are removed from the GSE software and if the production quantity is large then redesign the GSE.

1.0 INTRODUCTION

In order that the Advanced Fire Detection System (AFDS) can be checked out on a regular maintenance basis, it is necessary to provide some form of Ground Support Equipment (G.S.E.) for test.

The AFDS has its own built-in test system but cannot identify a single failure on System A without a G.S.E.

Furthermore, the G.S.E. enables post-flight data, stored during flight, to be read directly from the AFDS.

The G.S.E. is a portable automatic/manual check-out unit for the Advanced Fire Detection System. It performs three basic functions; it reads out the stored data gathered during the flight, it checks the operation of the system and it identifies which line replaceable unit (LRU) is faulty.

This report is a description of the detail implementation of the G.S.E. It is split into four major sections.

a) <u>System Design</u>

This section explains the functions of the G.S.E. for the following conditions:

Case 1 - When CCU is on aircraft.
Case 2 - When CCU is in laboratory.

A functional description of the G.S.E. hardware is given supported by a simplified block diagram. The software is discussed briefly, i.e. the object of each test performed on the CCU by the G.S.E. is given.

b) <u>System Method</u>

This section is split into two parts:

<u>Hardware</u>

The hardware is split into 17 functional parts and discussed.

<u>Software</u>

The overall design is discussed followed by a detailed description of each test.

c) Operating Instructions

d) Conclusions

2.0 SYSTEM DESCRIPTION

2.1 CCU - G.S.E. Connection and Operation

Cables 1 to 4 are custom-built to connect CCU to G.S.E.

The same cables are used to test both Systems A and B.

Normally the CCU is on the Aircraft, and cables 1, 2 and 3 are used, but the CCU can be tested under laboratory conditions, in which case cable 2 is replaced with cable 4. The main differences between cables 2 and 4 are:

Cable 2	Cable 4
1. Is an extension for the Aircraft cable form.	1. Is a Lab. support cable.
2. Powers G.S.E. from Aircraft Power supply.	2. Powers G.S.E. from bench power supplies.
3. Connects all sensors on Aircraft to G.S.E. input interface.	3. Has provision for connecting CWU and one dual or single U.V. sensor to G.S.E.

2.1.1 CCU on Aircraft

The sequence of connecting G.S.E. to CCU by cables 1 to 3 is shown in Figure 2-1. A complete set of operating instructions both in Manual Mode and Auto Mode is described in Appendix B.

Normally the G.S.E. is operated in Auto Manual in which case the operator ensures that:

a) G.S.E. IN/OUT switch is set to IN.
b) Auto/Manual key switch is set to Auto.
c) Set Power Switch to ON.
d) Press and Release "Start Button".

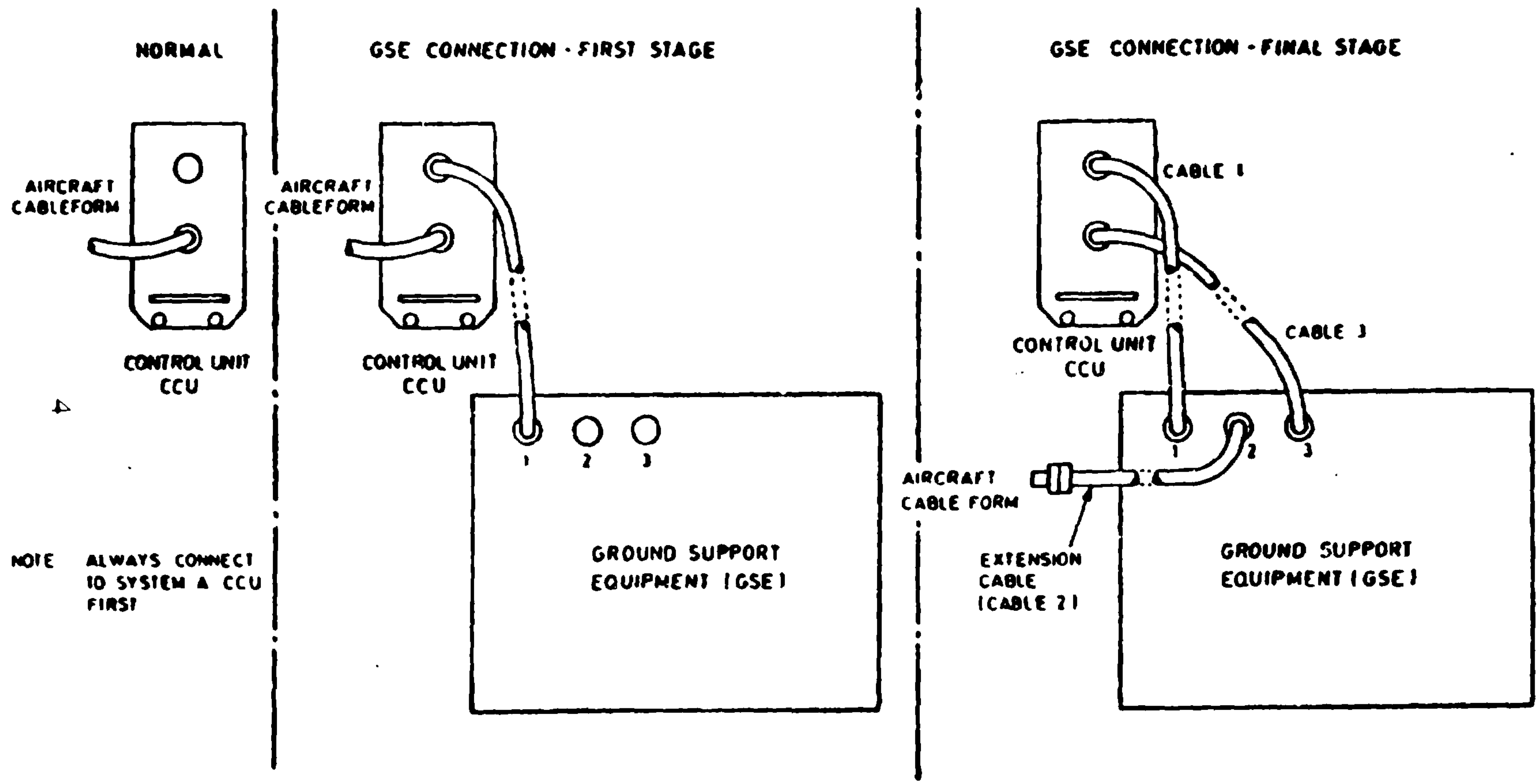


FIGURE 2-1 GSE CONNECTIONS SEQUENCE

Observe print out for results of the tests being performed. The print out will also show end of all tests when the paper is torn off.

When Manual Mode is selected, each test can be individually selected as long as certain rules are observed. The rules are described in Appendix B.

2.1.2 CCU on Bench

Figure 2-2 shows cable connections between G.S.E. and CCU. One of the main functions of cable 4 is to charge up the G.S.E. battery. It has additional connectors which enables it to be used for a bench checkout of system units. With this set-up the following tests cannot be conducted fully:

(a) Sensor Test

Because only one head can be connected.

(b) CCU Operating in Normal Mode

Although the CCU will be running in Normal Mode and respond to Fire and Fault Tests from the Crew Warning Unit, it can not detect real fire since simulated heads are connected to the CCU.

2.1.3 Ground Support Equipment

A simplified block diagram of the G.S.E. is shown in Figure 2-3. The G.S.E. contains a microprocessor system which controls all the interface circuitry to perform tests on the CCU. It also prints results of all tests on the printer.

Since the CCU (System A) consists of two microprocessor systems, the interface circuitry of the G.S.E. is duplicated to enable most tests to be performed in parallel. This results in a saving of approximately five minutes of CCU testing time. Since G.S.E. is common to both system A and system B, sufficient intelligence is built in to G.S.E. to recognize the system under test and perform tests accordingly.

The interface circuitry is divided into two equal sides which consist of:

(a) Complete control over CCU normal running and G.S.E. running mode.

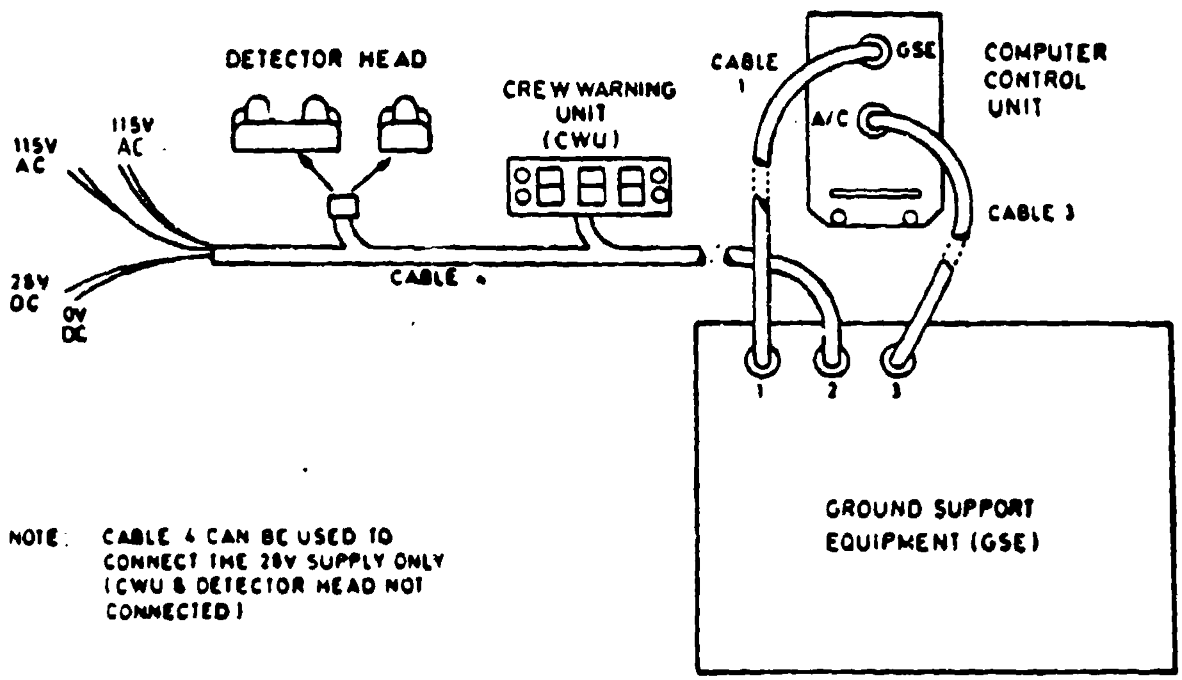


FIGURE 2-2 GSE CONNECTION, 28V SUPPLY

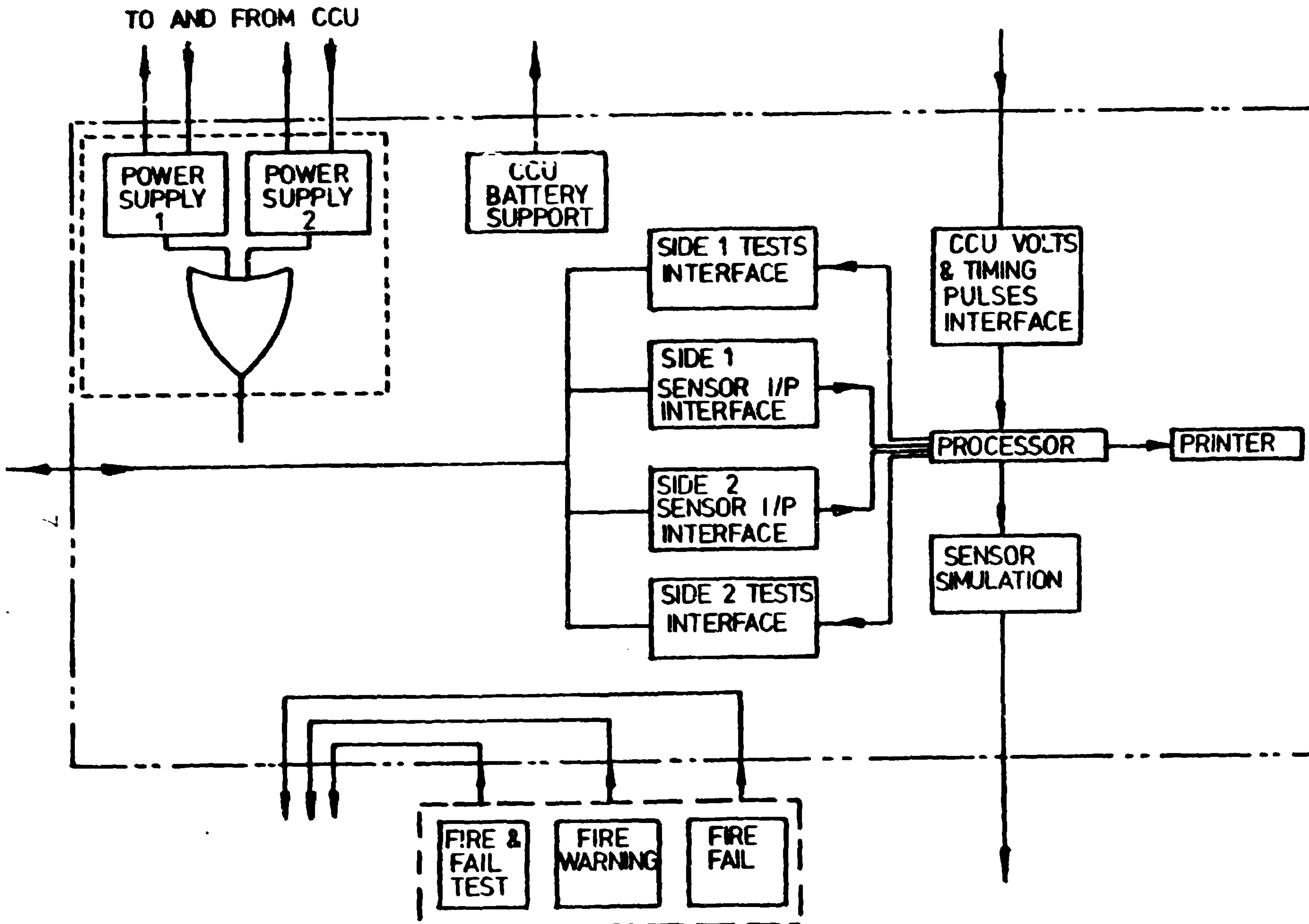


FIGURE 2-3 BLOCK DIAGRAM OF GSE

(b) Sensor input.

(c) CCU voltages and timing.

(d) Sensor simulation.

(e) CCU battery support.

(f) Power supply.

There are six tests performed by the G.S.E. and it may use one or more blocks of interface circuitry to perform each of the six tests. Five of these tests contain several sub-tests (e.g. for system A, 'Functional Test' contains 56 sub-tests).

The six tests are:

1 - Read data from CCU.
2 - Control Unit Tests.
3 - U.V. Head (Sensor) Tests.
4 - Parametric Tests.
5 - Functional Tests.
6 - Analyze data from CCU.

The G.S.E. can be operated in either Auto or Manual mode. In Auto mode the above tests are performed in the same sequence as they are listed above. However, in Manual mode the tests can be performed in any order, and any particular test can be repeated as many times as desired. Care should be taken to ensure Test 1 is always completed first, otherwise CCU data is lost. Consequently, data analysis test can not be performed. For this reason a key switch is used to set the G.S.E. in Auto mode when operated by non-skilled staff.

2.2 Description of Tests

A set of batteries housed in the G.S.E. support the RAM of CCU system A when the CCU is connected to the G.S.E. This is necessary because the battery support for system A is housed in system B.

2.2.1 Data Read

By putting the CCU into G.S.E. mode, the G.S.E. issues a command to perform a CCU housed test which dumps the RAM contents of CCU to G.S.E. This test takes approximately 25 seconds and initially it is performed on Side 1. If the CCU under test is System A, then the above is repeated for Side 2.

2.2.2 Control Unit Test

These are a set of four tests performed by CCU on itself but initiated by G.S.E.

The four tests are:

a) RAM - RETENTION A.

b) RAM - RETENTION B.

c) COMMON - LOGI.

d) RAM TEST AND SET.

The G.S.E. initiates these tests to be performed in the above sequence and monitors the results. If there is one or more failures then it is printed on the printer.

2.2.3 U.V. - Head (Sensor) Tests

This test determines the sensitivity of the U.V. heads. The U.V. emitters associated with each head are fired simultaneously for 10 seconds for Side 1. The pulses received from each head are counted and printed. With this information one of two conclusions can be drawn:

1) If the pulse count is less than 100 counts per 10 seconds then either the U.V. head has failed and must be replaced, or the emitter supply has failed.

2) If the pulse count is greater than 100 but less than 1000 then the U.V. heads need cleaning.

   If the CCU under test is system A, then the above is repeated for Side 2.

2.2.4 Parametric Test

The object of this test is to monitor the CCU supply i.e. 5v supply; 320v Emitter supply. Also the 15 second emitter test and Time Share (167ms) times are monitored. The results are printed.

2.2.5 Functional Test

The object of this test is to confirm integrity of CCU hardware to respond to Fire and Fault conditions simulated by the G.S.E.

2.2.6 Data Analysis

The data received from CCU during the first test (i.e. data read) and the data received during the third test, i.e. U.V. Head (Sensor) tests is analyzed by this program and the results printed.

3.0 SYSTEM METHOD

The system is described under the sub-headings of Hardware and Software as follows:

3.1 Hardware

A simplified block diagram of hardware is shown in Figure 2-3. For any detailed reference to hardware see circuit diagrams in Reference 3-1.

The hardware is divided into seventeen main blocks.

These are:

1. Microprocessor Card.
2. Printer.
3. Power Supply Side 1.
4. Power Supply Side 2.
5. Power Supply to CCU.
6. Battery support.
7. Input/Output Decode.
8. Set of Input Ports.
9. Set of Output Ports.
10. U.V. Head Simulation.
11. Head/Drive Supply Card Side 1.
12. Head/Drive Supply Card Side 2.
13. Head/Drive Control Side 1.
14. Head/Drive Control Side 2.
15. Voltages and Timing Monitoring.
16. Cableforms.
17. 25 second Timer.

3.1.1 Microprocessor Card

There were only two options available.

1) Custom built microprocessor card.

2) Buy a ready-made microprocessor card.

In both cases the processor card must be based on the RCA 1802 central processor unit so that it is compatible with the CCU.

To save time and money, it was decided to take Option 2. The microprocessor card selected is GRO430 low power single board computer supplied by "The Golden River Co.". The main features of the microprocessor card are:

10K PROM/ROM

2K RAM

PROM programmer on board

Total current typically 9mA.

For further details on the microprocessor card see Appendix A-1.

3.1.2 Printer

The printer selected is a Digitec Model 6410 with Option J, which provides 32 characters per line or 16 characters per line when selected.

The printer is manufactured by United Systems Corpn., U.S.A. For further details on the printer see Appendix A-2.

3.1.3 Cableforms

References 3-2, 3-3, 3-4 and 3-5 give all the details to manufacture cables 1 to 4. Installation system wiring is given in Reference 3-6.

The Amphenol connectors were selected to match those used on the CCU.

The Cannon connectors were selected due to easier delivery.

The cables were selected on the basis of being able to withstand worst operating conditions and yet produce a flexible cable form.

3.1.4 Power Supply Side 1 and 2

The G.S.E. is required to perform many similar functions to the CCU and thus employs the same power supply circuitry as the CCU. Also reference voltages of 8V and 5V are required to monitor the CCU voltages.

3.1.4.1 Power Supply Specification

Inputs

115V - 400 Hz - with a tolerance of +10% and -10%.
18 to 30V d.c.

Outputs

4.5V to 5.5V d.c.
310V to 340V d.c.

320V d.c. unregulated.

8V d.c.) Reference Voltages with tolerances
5V d.c.) of +5mV and -5mV.

3.1.4.2 Power Supply Description

A single transformer is employed to obtain the nominal 5.0V, 320V and 320V unregulated from 115V 400Hz.

Transient protection is provided at the input of the transformer by four transorbs and a series resistor capacitor arrangement.

The 5V and 320V are regulated by a series transistor method.

The 28V input is used to derive the 8V and 5V reference voltages. The former is derived by using a LM205 regulator and the latter is derived by using a LM340T 5V regulator.

The 5 volt supply is used to drive most of the G.S.E.'s electronics. The 320V supply drives the 16 UV photocells via the head/drive circuitry. The 320V unregulated supply drives the U.V. emitters associated with the photocells. The voltage monitoring circuitry uses 5 and 8V as its reference points. The 28v d.c. is further used to charge up the three Nickel Cadmium batteries that support the CCU RAM.

For Side 2, the 28v input and the 8 and 5V reference voltages are common to Side 1; but a separate input of 115v 400Hz and associated electronics are required.

The flexibility of the G.S.E. is increased by incorporating a 115V change-over arrangement for the printer, i.e. the printer is common to both sides and is initially supplied with 115V from Side 1 via a relay arrangement. The relay control is arranged such that if the 115V of Side 1 failed, then the printer will be supplied from Side 2.

3.1.5 Power Supply to CCU

The power supply to the CCU is routed via the G.S.E. This is necessary for a number of reasons:

1) The aircraft cableform carrying power to CCU is now connected to the G.S.E. This powers the G.S.E. to carry out tests on the U.V. heads.

2) In order to avoid corrupting the flight data it is necessary to hold the CCU in a power-off condition.

3) In order to perform certain tests it is necessary to have a complete control over the CCU.

Figure 3-1 shows a simplified diagram of the CCU power supply control. The power supply to the CCU is routed via a set of relay contacts. The operation of the relay is controlled by the microprocessor. Also the reset line of the CCU is controlled by another relay. The 28V is also routed via the G.S.E. but is not controlled. This arrangement gives the G.S.E. a complete control of the CCU.

3.1.6 Battery Support

If the CCU under test is system A then a 4 volt battery housed in the G.S.E. is required to support the CCU RAM when the G.S.E. is being connected to the CCU. The reason is that the battery support for system A is normally housed in system B, i.e. under the normal conditions system A is battery supported by system B via the Aircraft cableform. To make a complete CCU to G.S.E. connection it is necessary to connect the Aircraft cableform to the G.S.E., which results in the loss of battery support provided by the system B and consequently the flight data. For a correct G.S.E. to CCU connection, see Appendix B.

When the G.S.E. connection is complete, the result is that two sets of batteries are connected in parallel supporting the CCU RAM. The G.S.E. battery is routed to the CCU via a normally closed relay contact. This gives the G.S.E. the facility to disconnect the G.S.E battery support and test the CCU battery support sys....

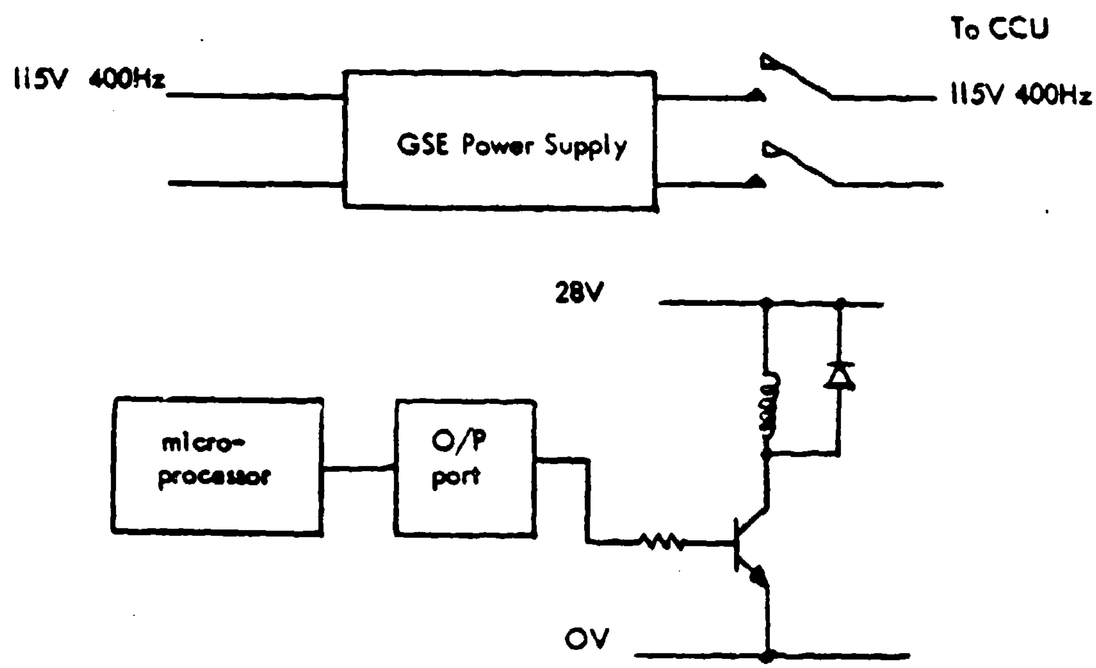


FIGURE 3-1 CCU POWER SUPPLY CONTROL DIAGRAM

Figure 3-2 shows a simplified diagram of the G.S.E. battery and its condition monitoring electronics.

The condition of the G.S.E. battery is monitored by a window detector. By pressing the TEST G.S.E. battery switch provided on the front panel, a Green Lamp adjacent to the G.S.E. switch illuminates if the G.S.E. battery condition is satisfactory. The window detector's limits are:

Lower Limit - 3.0V
Upper Limit - 7.0V

3.1.7 Input/Output Decode

The G.S.E. requires six input and five output ports.

To meet this requirement an RCA CDP 1853CD N-bit 1 of 8 decoder is employed along with 6 two input NAND gates. One input of the NAND gates is connected to the Memory Read Line (MRD) of the microprocessor.

The input port is enabled by providing a low pulse to its output disable pin, while the output port is enabled by providing a low pulse on chip-select one (CS1) and a high pulse on chip-select 2 (CS2) simultaneously. The state of the memory read line decides whether an input or output port is selected.

Figure 3-3 shows a simplified diagram of the I/O port arrangement.

3.1.8 U.V. Head Simulation

The G.S.E. is required to perform a functional test on the CCU's U.V. Head/Drive circuitry. In order to achieve this requirement the U.V. heads of the CCU are simulated. Unlike the real U.V. heads which are ON LINE all the time that the CCU is powered on, the simulated heads can be brought ON LINE or OFF LINE as required.

Figure 3-4 shows a simplified diagram of the U.V. head simulation.

Eight sets of simulated heads are individually controlled by the microprocessor via the output ports. For Side 2 the above circuitry is duplicated.

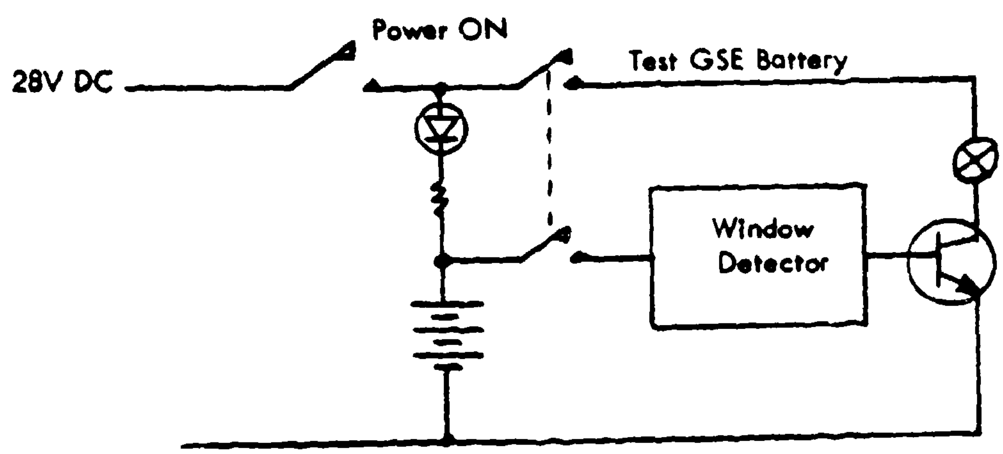


FIGURE 3-2 BATTERY SUPPLY DIAGRAM

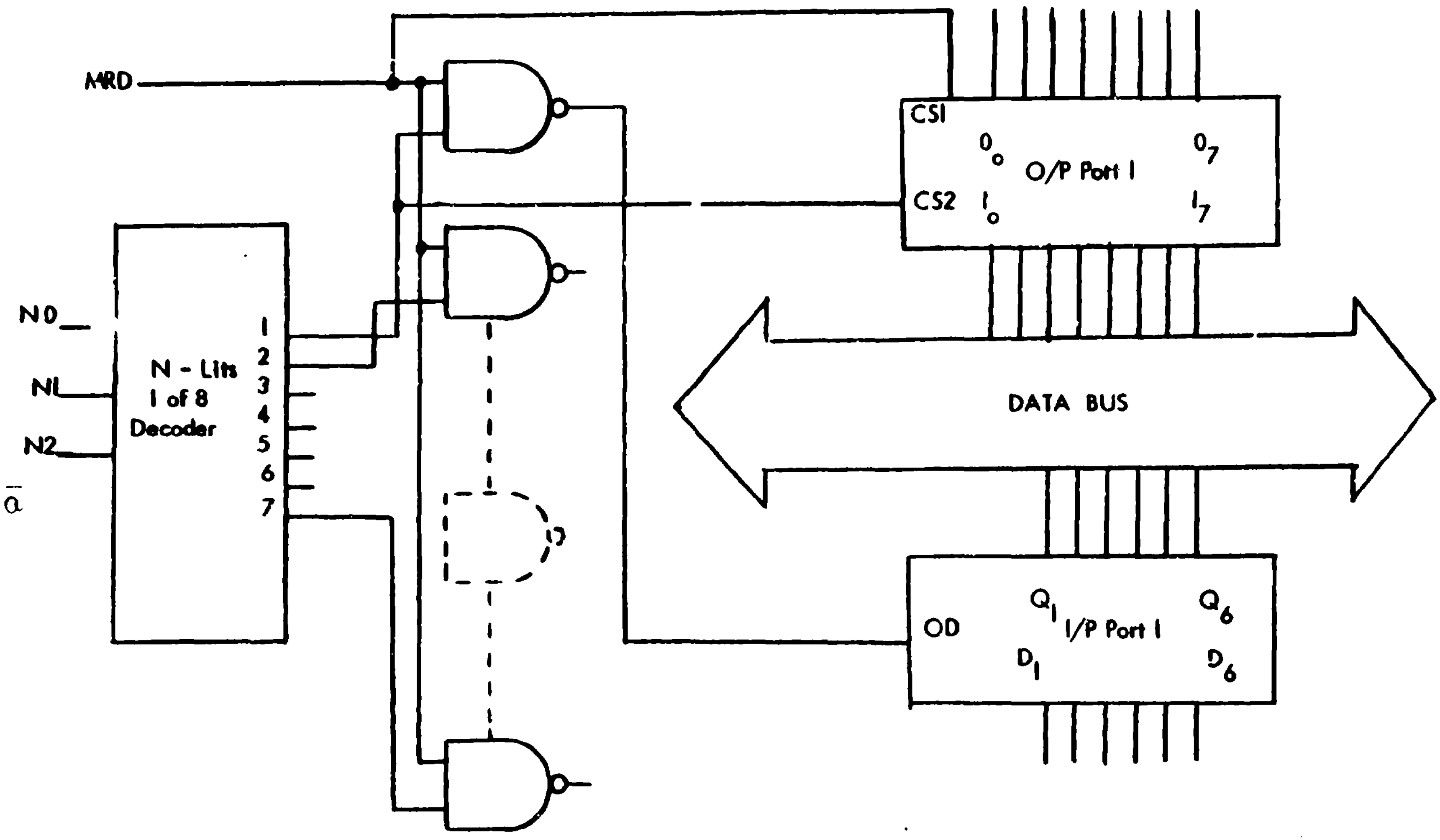


FIGURE 3-3 I/O PORT ARRANGEMENT

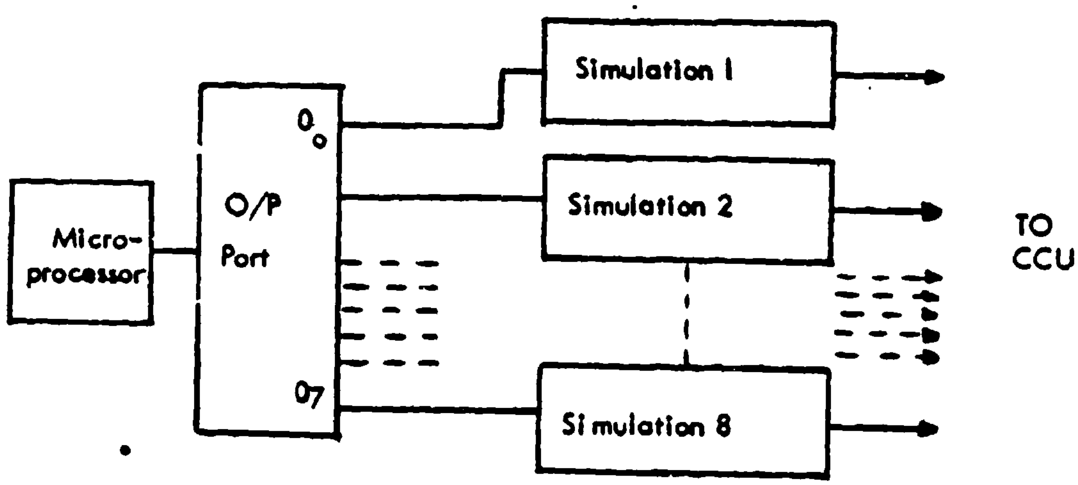


FIGURE 3-4 U.V. HEAD SIMULATION

3.1.9 Head/Drive Control and Supply

The CCU's Head/Drive control and circuitry is duplicated in the G.S.E. This is necessary in order to test the U.V. heads. Figure 3-5 shows a simplified diagram of the Head/Drive Control and supply circuit.

The control circuitry is driven by an oscillator of 250KHz. The 250KHz is divided down to give a train of pulses of period 896 us.

The train of pulses is used to interupt the microprocessor every 832 us during U.V. Head Test. The circuit operates as follows:

a) The U.V. Head Test is performed on one side at a time.

b) The control circuit and the Head/Drive circuit are repeated eight times for each side.

c) The Heads are brought on line.

d) The U.V. emitter is enabled.

e) The U.V. Head fires and generates a positive edge pulse.

f) The positive edge pulse enables the control logic which generate two separate pulses. One is of duration of 2ms and it is used to remove the 320V supply from the U.V. photocell; the other is of duration 1ms and it is enabled on to the DATA BUS.

g) The U.V. photocell is brought back ON LINE and the above (section e and f) keeps occurring until the U.V. Head and emitters are disabled.

For Side 2 sections (a) to (g) are repeated.

3.1.10 Voltage and Timing Monitoring

The following CCU voltage lines and timing pulses are monitored by the G.S.E.

Side 1	Side 2
320V DC	320V DC
5.6V DC	5.6V DC
Emitter Supply	Emitter Supply
15 second emitter test	15 second emitter test

COMMON TO BOTH SIDES.

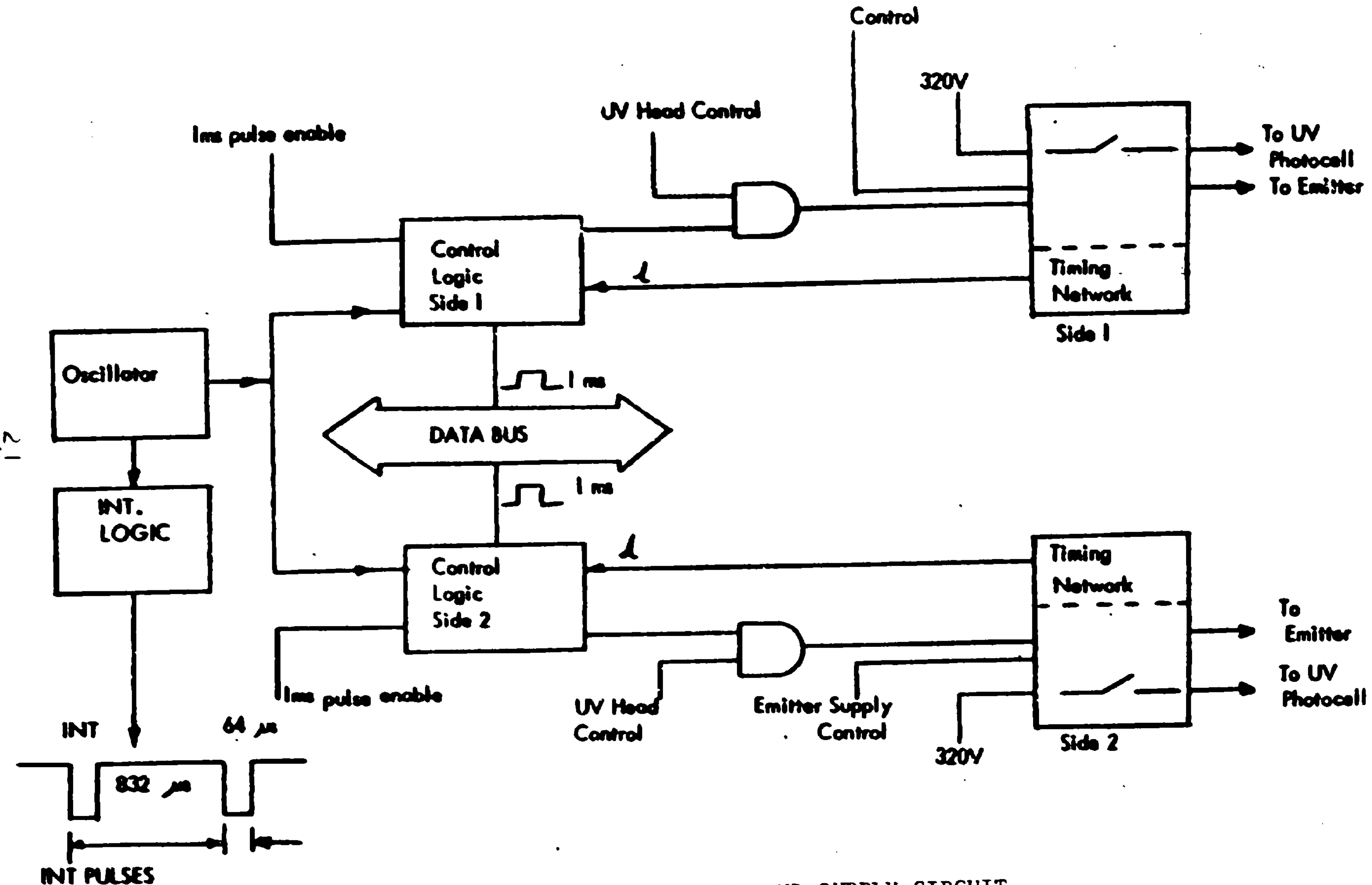


FIGURE 3-5 HEAD/DRIVE CONTROL AND SUPPLY CIRCUIT

Check Point 1 (CH1)

Check Point 2 (CH2)

Check Point 3 (CH3)

Check Point 4 (CH4)

System Configuration

The voltages are monitored for lower and upper limit by the use of window detectors, the outputs of which are connected to a set of input ports. The check points one to four lines are of 28V DC. Figure 3-6 shows a simplified diagram of check points monitoring.

The 28V is potted down to 5.6V and connected to 5V regulated supply via a diode. Also the 5.6V is connected to the input ports via Schmitt inverter buffers.

The G.S.E. uses the system configuration (5.6V) line to determine whether it is testing system A or system B. The system configuration line is O Red with 5.6V Side 2 and connected to an input port. The O Red arrangement is desired because for system A the system configuration line is HIGH and for system B it is open circuit. Further there is no 5.6V side 2 in system B. The G.S.E. detection of system configuration is configured such that any one or both lines HIGH constitutes system A and if none are HIGH then system B. This type of arrangement was necessary due to the independent power supplies of the CCU.

3.1.11 25 Second Timer

Figure 3-7 shows the simplified diagram of the 25 second timer.

The timer is built of a single 556 dual monostable integrated circuit plus timing capacitors and resistors. It is arranged such that, normally the output is held HIGH. When the control logic triggers the timer, a negative going pulse of duration 10 millisecond is produced. This negative going pulse is used to reset the microprocessor program to start from location 0000.

3.2 Software

3.2.1 Over View

Figure 3-8 shows a simplified flow diagram of the G.S.E. software. The flow diagram is designed to

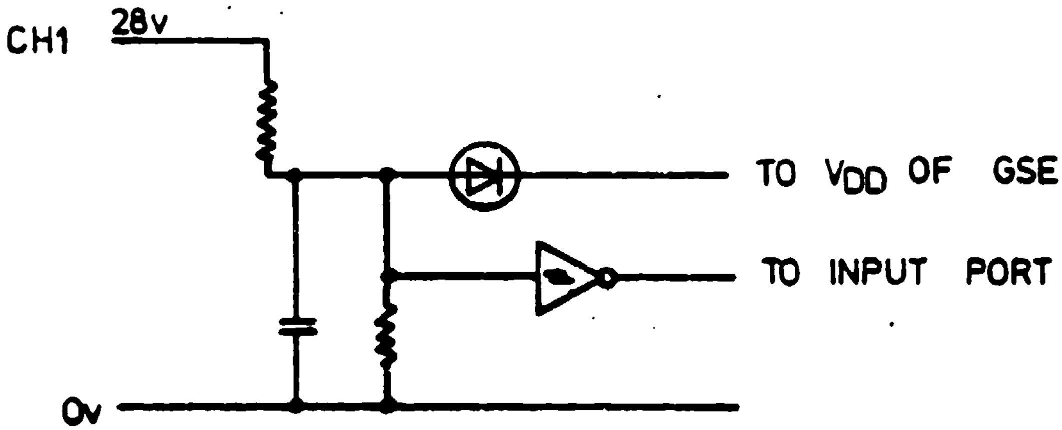


FIGURE 3-6 CHECK POINTS MONITORING DIAGRAM

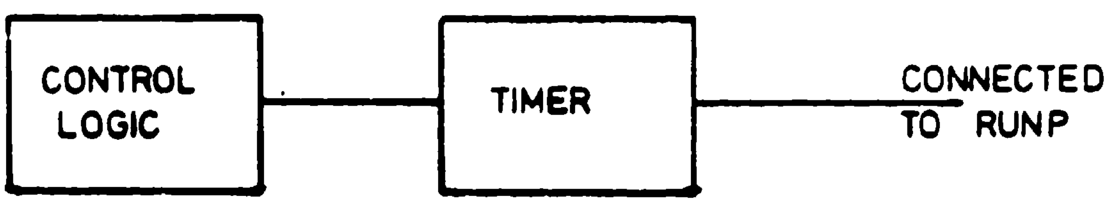


FIGURE 3-7 25 SECOND TIMER DIAGRAM

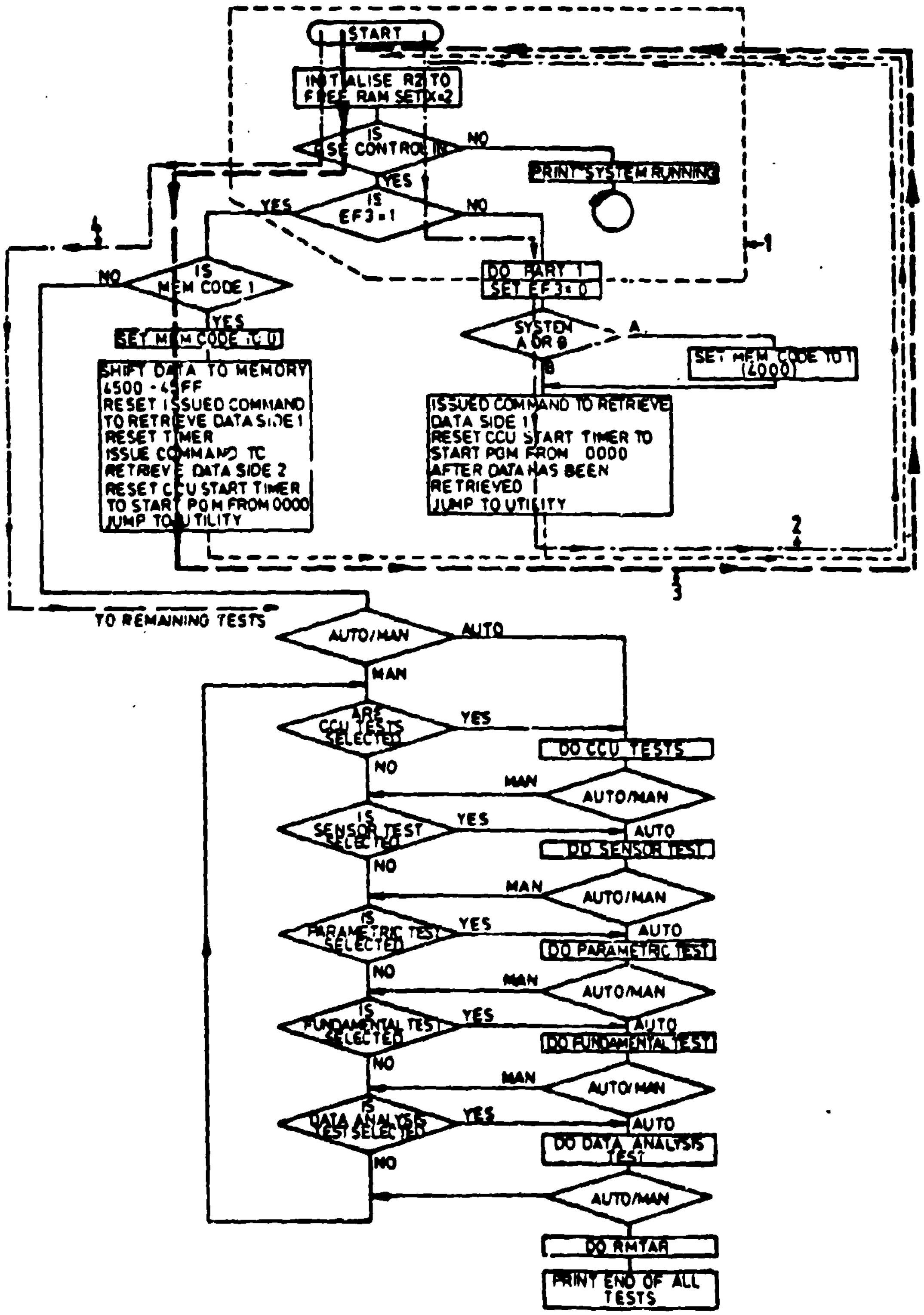


FIGURE 3-8 GSE SOFTWARE FLOW DIAGRAM

perform tests on the CCU in a pre-determined sequence. The sequence is:

a) Since most of the tests will corrupt the RAM of the CCU, it is necessary for the G.S.E. to perform the Read CCU test first. (i.e. Retrieve the flight data from the CCU RAM).

b) If there is a failure in the CCU during the CCU TESTS, SENSOR TESTS or PARAMETRIC TEST then the FUNCTIONAL TESTS and the DATA ANALYSIS TEST shall be aborted. Also any failure in the PARAMETRIC TEST aborts the whole range of tests. This leaves either the CCU TESTS or the SENSOR TESTS to be performed after the READ CCU tests.

c) Flight Data retrieved during the READ CCU test is useful only if there is no fault in the CCU. The FUNCTIONAL TEST, tests out the CCU's ability to respond to FIRE and FAULT conditions and thus needs to be performed before the DATA ANALYSIS.

There are two other tests:

1. To determine whether or not the G.S.E. can communicate with the CCU. This test is always performed before tests (a) to (f).

2. To simulate the Heads and Emitter Test during normal operation of CCU.

3. To simulate the Heads and Emitter responses to the FIRE TEST and FAULT TEST switches when CABLE 4 is used.

3.2.2 The Microprocessor Card Utilization

The microprocessor card is a self-contained low power single board computer with its own utility program. The G.S.E. program is housed in four 2K by 8 bit U.V. PROMS (2716). The G.S.E. program is located at 0000 to 2000.

The utility program is located at 8000 to 83FF. The microprocessor card also has 2K RAM located at 4000 to 8000.

The G.S.E. program utilizes some of the subroutines from the utility program (teletype input and print subroutines) and it also uses the microprocessor cards RAM as a rough working area, e.g. The FLIGHT DATA retrieved is stored at this RAM.

The microprocessor card can RUN programs in two main modes, i.e.

1. Utility Mode.
2. Program Mode.

To RUN in Utility Mode the RUN line must be taken to ground momentarily. This forces the microprocessor to start RUNNING from location 8000.

To RUN in the Program Mode the RUN line must be taken to ground momentarily. This forces the microprocessor to RUN from location 0000.

NOTE

When the microprocessor card is in the program mode, the program can be arranged to jump into the UTILITY mode but the reverse is not possible.

For further details on the microprocessor card, see Appendix A-1.

3.2.3 Note on the Start Up Condition

At POWER ON, the G.S.E. has the following conditions:

1. No power is applied to CCU.
2. CCU reset line held LOW.
3. The EF3 flag of the Central Processor Unit is held LOW.

The G.S.E. program starts by disabling the INTERRUPT line; sets up the various registers of the CPU; activates the appropriate hardware to apply power to CCU; and releases the CCU reset line. Next the program examines the position of the G.S.E. IN/OUT switch. If the G.S.E. IN/OUT switch is at position OUT, then the program branches to perform the simulation of Heads and Emitter Test. This simulation also responds to the FIRE TEST and FAULT TEST switches when CABLE 4 is used. If the G.S.E. IN/OUT switch is at position IN, then the program looks for the state of the EF3 flag. (i.e. HIGH or LOW). The state of the EF3 flag is monitored because it allows the program to decide whether or not it has retrieved the FLIGHT DATA SIDE 1 (Note: for System A, there are two independent sides). This Hardware/Software arrangement of the G.S.E. is necessary because:

1. The CCU transmits the data serially i.e. in the same format as a teletype.

2. In order to receive correctly the data transmitted by the CCU, the G.S.E. program jumps to the UTILITY program of the microprocessor card.

3. After all the data has been received by the G.S.E, the microprocessor card waits for further instructions which are not forthcoming. To escape from this UTILITY program condition, the RUNP line must be enabled, i.e. it must be taken to ground momentarily. This has the effect of starting the G.S.E. program from the beginning again. Hence, before DATA SIDE 1 is retrieved, the state of the EF3 flag is changed to HIGH. Consequently, when the program starts from the beginning, the second time, it is forced to branch to another part of the program. i.e. If it is System A, then retrieve DATA SIDE 2 or if it is System B then continue with the remaining tests. When DATA SIDE 2 has been retrieved, the program is forced to start from the beginning again and it proceeds to perform the remaining tests.

   The remaining tests can be performed in AUTO or MANUAL mode. However, trained personnel can perform the tests in a different sequence when the G.S.E. is operated in MANUAL mode.

3.2.4 Tests Description

3.2.4.1 Simulate Heads and Emitter Response Time

This routine detects the type of system under test (e.g. System A or System B). The operation of this routine is sychronized with the CCU, i.e. at power ON the CCU performs an Emitter Test by firing its emitters and looking at the response from the U.V. heads.

NOTE

If the CCU under test is System A then the Emitter Test is always performed on SIDE 2 first.

The architecture of this routine is:

1. It waits until the CCU's emitter line side 2 is HIGH.

2. It fires all heads on Side 2, i.e. simulating the Heads.

3. It waits until the CCU's emitter line side 2 is LOW.

4. It resets the simulated Heads.

5. It waits until the CCU's emitter line side 1 is HIGH.

6. It fires all Heads on Side 1, i.e. simulating the Heads.

7. It waits until the CCU's emitter line Side 1 is LOW.

8. It resets the simulated Heads.

9. It branches back to the beginning.

If system B is under test then it ships all operations regarding Side 2.

This routine is also used to test the CCU to respond to the FIRE test initiated by depressing the FIRE TEST switch on the Crew Warning Unit. When the FIRE TEST switch is pressed, the CCU fires all emitters. The routine detects this and fires all Heads simulating all Heads until the FIRE TEST switch is released. Consequently, the CCU resets its emitter line to LOW. The overall result is that the CCU responds with a FIRE CONDITION displayed on the CWU. In order to get out of this routine; it is necessary to set the G.S.E. IN/OUT switch to 'IN' and start the program again from location 0000, i.e. take the RUNP line to ground momentarily. For full details on this routine see Appendix A-3.

3.2.4.2 <u>To determine whether the G.S.E. can communicate with the CCU</u>

The flow diagram is shown in Appendix A-4 and it is referred to as a block labelled PART I in Figure 3-8.

The object of this part of the program is as follows:

3.2.4.2.1 <u>Initialize</u>

"POWER ON" condition of the CCU.

HOLD CCU in Reset Mode, etc.

3.2.4.2.2 <u>Print operating message</u>

"GD/GRAVINER DFDS AUTO ROUTINE".

3.2.4.2.3 Test position of G.S.E. IN/OUT switch.

3.2.4.2.4 If G.S.E. IN/OUT switch is at position 'OUT' then the CCU is in normal mode and the G.S.E. program must branch to perform the "simulate Heads and Emitter response test" routine (see Section 3.2.4.1).

3.2.4.2.5 If the G.S.E. IN/OUT switch is at position 'IN' then it must proceed to test the status of the EF3 flag.

3.2.4.2.6 If the status of EF3 is LOW then branch to Read data from CCU test otherwise proceed to determine whether or not the G.S.E. can communicate with the CCU.

The object of this part of the program is:

a) To determine whether the CABLE FORMS (one of three) are connected properly between CCU and the G.S.E., i.e. the G.S.E. can communicate with the CCU.

b) To determine and print SYSTEM CONFIGURATION, i.e. SYSTEM A or SYSTEM B.

c) For SYSTEM A a PASS status will allow the G.S.E. PGM to proceed to PART 2, i.e. the communication path is confirmed. A FAILURE status will print the following message:

   "NO G.S.E. - CCU PATH.
   CHECK CABLE 1 OR
   REPLACE CCU"

NOTE

During this condition, three faults are possible:

1. CCU Faulty.
2. Cableforms not connected properly.
3. Cableforms faulty.

It is recommended that in the event of the above failure, the Cableforms be checked (pin to pin connection). Reconnect the G.S.E. to CCU connections and repeat the test. If the failure condition still exists, and the cableforms were found to be correct then, the CCU must be assumed FAULTY. Hence the CCU must be sent to GRAVINER LIMITED for detailed analysis.

d) For SYSTEM A, four PASS/FAIL status conditions are possible:

   1. SIDE 1 & 2 PASS.
   2. SIDE 1 & 2 FAIL.
   3. SIDE 1 PASS, SIDE 2 FAIL.
   4. SIDE 1 FAIL, SIDE 2 PASS.

Occurrence of Condition '1' will allow the program to proceed to the remaining tests.

Occurrence of Condition '2' will not allow the program to proceed to the remaining tests.

It will also print the same failure message as in Section 3.2.4.2.6(c).

Occurrence of Condition '3 & 4' will not allow the program to proceed to the remaining tests if the G.S.E. is in AUTO mode, but it will allow the program to proceed to the remaining tests if the G.S.E. is in MANUAL mode. Also it will print the following messages:

SIDE 1 PASS)
SIDE 2 FAIL)

OR

SIDE 1 FAIL)
SIDE 2 PASS)

along with the failure message as in Section 3.2.4.2.6(c).

This part of the program is implemented by issuing conditions to the CCU to perform an IDLE ROUTINE.

The IDLE ROUTINE is housed in the CCU software and when enabled, it sets the G.S.E. 1 and G.S.E. 2 lines of the CCU to HIGH.

These G.S.E. lines are monitored by the G.S.E. program (for both sides if System A) and consequently the above decisions are made.

For full details on this part of the program see Appendix A-4.

3.2.4.3 Read DATA from CCU

The object of this part of the program is to retrieve the FLIGHT DATA stored in the CCU RAM. Refer to Figure 3-8 (the dotted path 1) of the program is already described in Section 3.2.4.1. and 3.2.4.2.

The hardware is arranged such that the program is forced to follow (the dotted path 2), i.e. to retrieve DATA SIDE 1. The data is retrieved by issuing the appropriate command to the CCU, to perform its 'SEND DATA OUT' routine. This is implemented in the following order:

1. Initialize the following:

a) Memory code to LOW, i.e. store 00 at location 4000.

b) Set EF3 flag to LOW.

2. Determine the type of system under test, i.e. System A or System B.

3. If the CCU is System A then set memory code to HIGH and proceed to 5.

4. If the CCU is System B then proceed to 5.

5.

a) Issue commands to the CCU Side 1 to perform its 'Send Data Out' routine.

b) Release the reset line of the CCU.

c) Start the 25 second timer. (See note below).

d) Jump to UTILITY program of the microprocessor card.

NOTE

As explained in Section 3.2.3., that in order to retrieve the data, the G.S.E. program must jump to the UTILITY program of the microprocessor card and in order to get out of the UTILITY, the RUNP line of the microprocessor card must be taken to ground momentarily. This is achieved by the 25 second timer, i.e. it takes approximately 23 seconds for the data transfer and 2 seconds later, the timer applies a short negative going pulse to the RUNP line of the microprocessor card.

6. Having retrieved data SIDE 1 the program starts from the beginning again and this time it follows (the dotted path 3).

7. If the CCU is type 'B' then the program proceeds to the remaining tests.

8. If the CCU is type A then the program performs the following:

a) Set memory code to LOW, i.e. store 00 at location 4000.

b) Shift DATA from Side 1 to locations 4500-45FF. (see note below).

c) Issue command to the CCU's Side 2 to perform its 'Send Data Out' routine.

d) Repeat as for Side 1 above.

9. Having retrieved the data from Side 2 the program starts from the beginning again and follows (the dotted path 4).

<u>NOTE</u>

The memory code is used to enable the program to determine:

(i) That it has retrieved data from Side 1 and the system under test is of Type B and thus proceed to the remaining tests.

(ii) That it has retrieved data from Side 1 and the system under test is of Type A and consequently it must retrieve data from Side 2.

(iii) That it has retrieved data from both sides and thus proceed to the remaining tests.

For full details on this program see Appendix A-4.

3.2.4.4 The CCU Tests

The CCU tests are a group of four tests housed in the CCU software. They are enabled one at a time. The tests are:

(i) RAM Retention A.

(ii) RAM Retention B.

(iii) Common Logic.

NOTE

For System A, both sides must see a FIRE condition before it is displayed on the CWU.

Hence, this condition is 'AND'ed in the Common Logic of the CCU and the results displayed.

(iv) RAM Test and Set.

The object of these tests is to confirm the integrity of the CCU RAM and the Common Logic part of the CCU.

The tests are performed in the numerical order above.

Further, if there is a future condition, it is recorded at a pre-determined area of the RAM (i.e. in this case at locations 4003 to 4013). After each condition is tested, the PASS/FAIL record register is incremented by one. Tests (i), (ii) and (iv) are performed simultaneously on both sides and test (iii) is performed on Side 1, and then on Side 2. At the end of these tests the PASS/FAIL status is printed in coded format, i.e. a row of zeros is printed if all tests were correct. If there were a failure then a 'one' will be printed in the corresponding position. Appendix A-5 gives a full list of messages corresponding to the failures in the CCU.

Further details of the four tests are now given.

(i) RAM Retention A

The G.S.E. program sets up the conditions for the CCU to perform this routine. The object of this routine is to load hexadecimal numbers in to the CCU RAM. The numbers start at 00 and finish at FF, since the size of the CCU RAM is 256 bytes. (FF hexadecimal = 256 memory bytes). The numbers are located in the incrementing manner.

When all the numbers have been loaded the CCU raises a G.S.E. flag. The G.S.E. program waits for four seconds to detect this flag and proceeds to the next program.

(ii) RAM Retention B

RAM retention A & B are essentially one program. The first one sets up a pattern of numbers and the second checks that pattern after the power supply to the CCU was switched 'OFF' for five seconds.

Hence the G.S.E. program disables the power supply of the CCU for five seconds. Also the conditions are set to perform the RAM Retention B. It then waits for four seconds to detect the RAM Retention B completion flag and then proceeds to the next program.

(iii) Common Logic

Before this test is performed, it is necessary to confirm that the CCU is able to respond to FIRE and FAULT conditions. This is necessary since the Common Logic routine assumes that a fire or fault condition will be transmitted. Thus the G.S.E. puts the CCU in Normal mode and simulates the U.V. Heads in firing mode. It waits for six seconds and then checks whether or not the CCU is in FIRE condition. If the CCU fails to respond with a FIRE condition then the G.S.E. aborts the Common Logic test. Otherwise it creates a FAULT condition by failing the CCU by not simulating the U.V. Heads in firing mode during the CCU's first emitter test. If the CCU fails to respond with a FAULT condition, then the G.S.E. determines whether the CCU under test is type A or B. If it is type B then the Common Logic test is skipped.

The G.S.E. sets up the conditions for the Common Logic routine to be performed on one side at a time. Side 1 is performed first. The programs wait for results for about six seconds and then proceed to the next routine.

(iv) RAM Test and Set

The object of this routine is to see whether all the CCU's RAM locations are functional. It does so by loading and checking two sets of patterns and in the end it sets all memory locations to zeros. Again the G.S.E. sets up the conditions for this routine to be executed; waits four seconds for the result then proceeds to the last part of 'The CCU Tests' program.

3.2.4.4.1 CCU Test Summary

The purpose of the RAM retention A and B is to confirm the CCU's Battery support, i.e. its ability to retain the FLIGHT DATA when the CCU is 'POWERED OFF'. Should a failure occur then a 'CCU BATTERY LOW' message is printed as well as a 'One' in the row of zeros displaying where the failure occurred.

During the Common Logic test, three possible faults occur.

1. Inhibit Fail.
2. Fault Fail.
3. Fire Fail.

Each of these faults refer to certain parts of the CCU hardware. A skilled person with sufficient knowledge of CCU hardware can pinpoint the position of the fault.

The RAM test and Set confirms the integrity of the CCU RAM and then sets it to zero.

At the end, the PASS/FAIL codes are printed. They are also scanned for any failure condition.

If the G.S.E. is in AUTO mode and a failure condition exists, then a flag is set up. If the G.S.E. is in MANUAL mode with a failure condition, no flag is set up. This flag is used just before the Functional Test to determine whether or not 'The Functional Test' and 'Analyze Data Test' should be performed.

For full details on these tests see Appendix A-5, A-6, and A-7.

3.2.4.5 Sensor Test

The object of this is to determine:

1. The sensitivity of the U.V. Head (i.e. the photocell).

2. That the U.V. Head and the connecting wires are correct and functional. This is achieved by duplicating the U.V. Head/Drive circuitry in the G.S.E. and by connecting the U.V. Heads to the G.S.E., i.e. the G.S.E. has complete control over the U.V. Head and Emitter supplies.

This routine switches the U.V. emitters 'ON' and counts the number of pulses received from the U.V. photocells for a period of ten seconds. For System A each U.V. Head consists of two photocells and two emitters. One photocell and one emitter refer to Side 1 of the CCU and the others to Side 2. Further, a maximum of 8 U.V. Heads can be connected to the CCU. However, the current CCU's are configured to use only five U.V. Heads. This means that sufficient intelligence must be built into the Sensor Test such that it only prints the results of the U.V. Heads that exist.

This is implemented as follows:

1. Initialize Registers, i.e. clear registers which will hold the pulse count; set up the address of the Interrupt subroutine.

2. Enable Interrupt, fire the Emitters Side 1 and jump to SELF LOOP.

3. The Hardware Interrupt occurs every 832 microseconds and the G.S.E. program jumps to the Interrupt subroutine. (See Section 3.2.4.5.1. for the Interrupt routine).

4. The program jumps out of the Interrupt subroutine and returns back to the SELF LOOP.

5. Procedures 3 & 4 are repeated for ten seconds whence the program jumps to Part 2 of the Sensor Test.

6. The emitters are switched 'OFF'.

7. A decision is made whether the counted pulses refer to SIDE 1 or SIDE 2.

8. It is determined whether the first head exists or not. If it exists then the counted pulses are converted to decimal numbers and printed. This operation is repeated for all the 8 U.V. Heads.

9. If the system under test is type A then re-initialize the registers. Fire emitters SIDE 2; enable the Interrupt and jump to SELF LOOP 2.

10. Operations 3 to 8 are repeated.

11. If the G.S.E. is in AUTO mode then proceed to the next test otherwise branch to the Manual Loop.

For details on this test see Appendix A-8.

3.2.4.5.1 BCD to Decimal Conversion

The object of this subroutine is to convert the number of pulses counted/10 seconds in Binary Decimal Code to Decimal Numbers. It is capable of converting a full 16 bit number, i.e. a max hex number of magnitude FFFF. This subroutine is implemented as follows:

1. Store the hex number to be converted in a 16 bit register (i.e. R3).

2. Clear and arbitrarily assign the decade order to 5 RAM locations where the converted number is to be held, as follows:

RAM location	Assigned decade value
4030	Ten Thousands
4031	Thousands
4032	Hundreds
4031	Tens
4030	Units

3. Read the least significant HEX digit, i.e. the least four bits.

4. Since the least HEX digit has a weighting of 'one'; test it for <, = & >10. If it is less than 10 add it to the UNIT decade, i.e. 10^0. If it is equal to 10 then add one to the TENS decade:

   (i.e. 10^1)

   If it is greater than 10 then add one to the TENS decade, subtract 10 from the tested value and add the remainder to the UNIT decade.

5. Read the second least HEX digit. This has a decimal weighting of 16.

6. Test it for zero.

6.1 If equal to zero then do Step 7.

6.2 If greater than zero then add 1 to the TENS decade and 6 to the unit decade.

6.2.1 Test both Unit and Tens decade for overflow i.e. Test Unit Decade for = or > 10. If it is equal to 10 then subtract 10 from the unit decade and add 1 to the Tens decade. If it is greater than 10 then subtract 10 from the Unit decade and add 1 to the Tens decade. Having tested the Unit decade, test the Tens decade applying the same analogy.

6.3 Decrement the read value and test it for zero.

6.4 Repeat Steps 6.1 to 6.4.

7. Read the third least HEX digit. This has a decimal weighting of 254.

8. Test it for zero.

8.1 If equal to zero then do Step 9.

8.2 If greater than zero then add 2 to the Hundreds decade; 5 to the Tens decade and 6 to the Unit decade.

8.2.1 Test the Units, Tens, Hundreds and Thousands decade for overflow. Same analogy as in Para. 6.2.1. is applied.

8.3 Decrement the read value.

8.4 Repeat Steps 7 to 8.4.

9. Read the most significant HEX digit. This has a decimal weighting of 4096.

10. Test it for zero.

10.1 If equal to zero then do Step 11.

10.2 If greater than zero then add 4 to the Thousands decade, 9 to the Tens decade and 6 to the Units decade.

10.2.1 Test the Units, Tens, Hundreds, Thousands and Ten Thousands decade for overflow.

10.3 Decrement the read value.

10.4 Repeat Steps 9 to 10.4.

11. Print the converted number.

Subroutines are written for the Units, Tens, Hundreds and Thousands decade overflow tests.

Figure 3-9 shows a flow diagram for the BCD subroutine. Appendix A-7 gives assembly listing as part of the Sensor test. This subroutine is also used by the Data Analysis Test.

3.2.4.5.2 The Interrupt Subroutine

The object of this routine is to count the number of pulses for 8 photocells in parallel for a period of 10 seconds. Further it must be able to distinguish that for a particular photocell; for the occurrence of two consecutive pulses only one is stored, i.e.:

Pulses arrived   101110) Photocell 1

Pulses stored   101010)

The above process is repeated for all 8 photocells. If the ten seconds are not up then, the exit from this routine is to either SELF LOOP 1 or SELF LOOP 2 otherwise the exit is to part 2 of the Sensor Test.

This routine is implemented as follows:

1. Initialize.

2. Read all 8 photocells (i.e. Have any one or all of them fired).

3. Determine if a pulse occurred immediately before the current read cycle and apply the above logic two consecutive pulses.

4. If a valid pulse exists for any of the 8 photocells then increment the corresponding photocell pulse counter.

5. If 10 seconds are up then branch to PART 2 of the Sensor Test otherwise branch to either SELF LOOP 1 or SELF LOOP 2.

For full details on this routine see Appendix A-8.

3.2.4.6 Parametric Test

The object of this test is to confirm that the integrity of the CCU's power supply rails, i.e. 320V, 5.6V and the emitter supply. Further it confirms the 15 second emitter test.

HEXA-DECIMAL TO BCD CONVERTION SUBROUTINE.

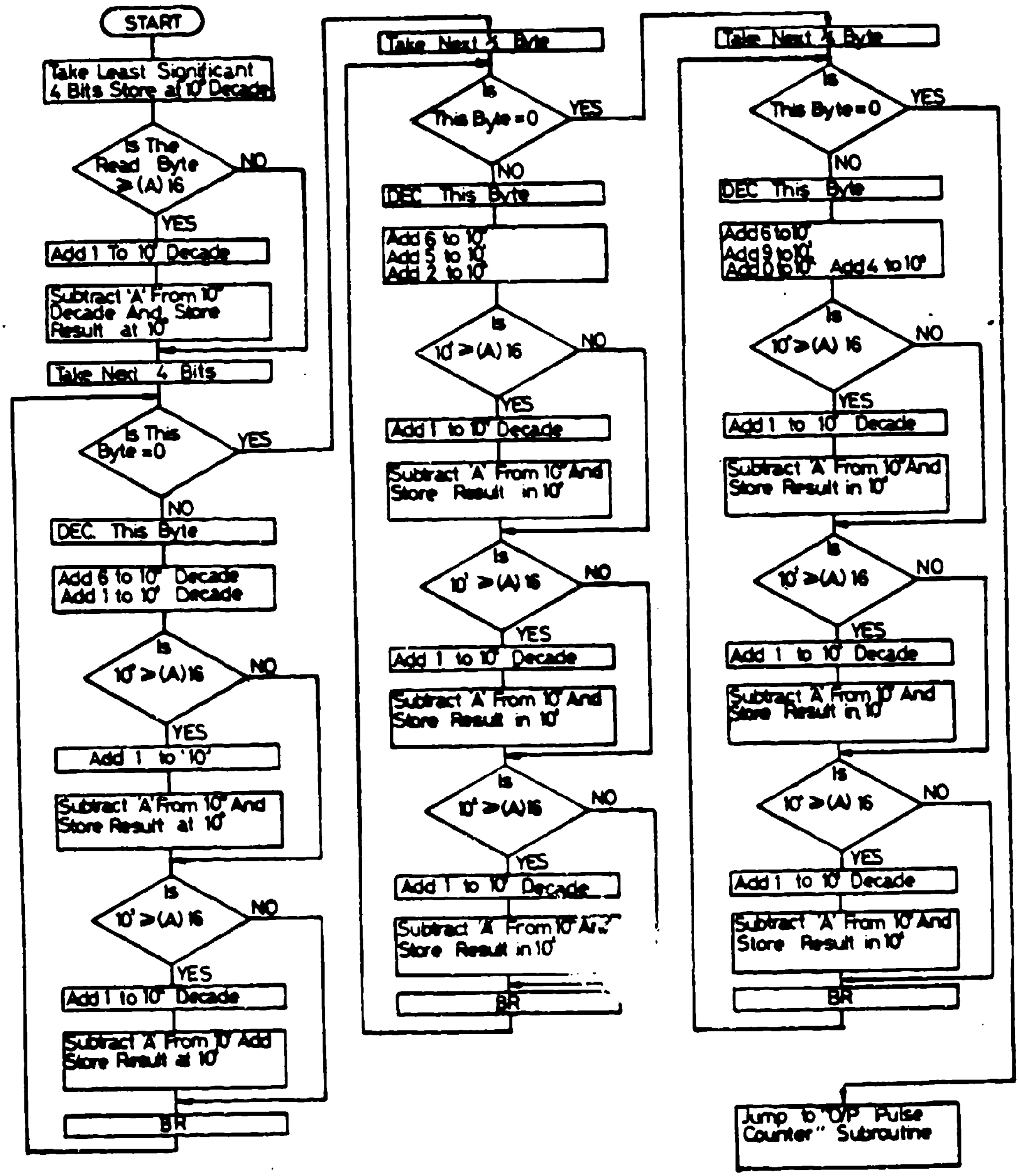


FIGURE 3-9 BCD SUBROUTINE DIAGRAM

The power supply monitoring is implemented by a set of window comparators. When the supply rails of the CCU go below or above their predetermined values (See Section 3.1.4) then a flag is raised. The Parametric Test detects this flag and prints the appropriate message. See Appendix A-5 for a whole list of messages.

As always, sufficient intelligence is built into this test so that both types of CCU's can be tested efficiently. If any failure is encountered during the power supply monitoring and if the G.S.E. is in AUTO mode then the remaining tests are aborted. However, if the G.S.E. is in the MANUAL mode then this test branches to the MANUAL loop.

The second part of this test is to confirm the integrity of the 15 second emitter test. The CCU energizes its emitters for one Time share period every 15 seconds and it looks for positive response from the U.V. Heads. If there is no response then the CCU reconfigures such that the offending U.V. Head is switched off line. If sufficient number of U.V. Heads fail then the CCU issues a FAULT condition.

The emitter test puts the CCU in Normal mode and observes for the emitter line to go HIGH. If it does not go HIGH within six seconds, then it issues an error message (See sample print out) otherwise it observes the Emitter Line to go LOW. If the Emitter Line does not go LOW within 180 ms then an error message is printed, otherwise it observes that the Emitter Line does not go HIGH for the next 14 seconds. At this stage it starts to observe the Emitter Line to go HIGH. If it does not go high within one second then an error message is printed.

This is repeated for Side 2 if applicable.

If the G.S.E. is in AUTO mode then occurrence of any failure aborts the remaining tests. If in MANUAL mode then branch to the Manual Loop. Below is a full list of error messages for the Parametric Test.

1. 5.6V SIDE 1 FAILED.
2. 5.6V SIDE 2 FAILED.
3. 320V SIDE 1 FAILED.
4. 320V SIDE 2 FAILED.
5. EMITTER FAILURE 01.
6. EMITTER FAILURE 02.
7. EMITTER FAILURE 03.
8. EMITTER FAILURE 04.
9. EMITTER FAILURE 05.
10. EMITTER FAILURE 06.
11. EMITTER FAILURE 07.
12. EMITTER FAILURE 08.

NOTE

Emitter failure codes 01, 02, 03 and 04 apply to SIDE 2 and 05, 06, 07 and 08 apply to SIDE 1. Further points marked 01 to 05 correspond to the type of Emitter Failure for SIDE 2. For SIDE 1 the points would go from 05 to 08. For full details on this routine see Appendix A-5 and A-9.

3.2.4.7 Functional Test

This test confirms the integrity of the CCU Head Drive/Supply circuitry. It is achieved by putting the CCU in normal mode and simulating the U.V. Heads in a predetermined sequence and observing the FIRE/FAULT response of the CCU. E.g. simulate a FIRE condition. If the CCU responds with a FIRE signal then the Head Drive/Supply circuitry corresponding to the simulated heads is functional. The Functional Test is divided into seven major tests. These tests are implemented in the following manner.

Initially the CCU RAM is cleared by performing the RAM Test and set routine. See Section 3.2.4.4. Put the CCU in Normal Mode and simulate the U.V. Heads during the CCU Emitter Test. If the CCU fails after the first Emitter Test then store a failure code (01) at location 4050 and increment the failure code Register, i.e. 4051.

NOTE

Locations 4050 to 4089 are used to store the PASS/FAIL status of the SUB-TESTS during the Functional Test. At the end of the Functional Test the PASS/FAIL statuses are printed (see sample print outs in Appendix B, Chapter 5). These codes are issued with the code decode list of messages to determine which part of the CCU's Head Drive/Supply circuit is faulty.

Let the CCU run for another five Time share periods and observe if a FIRE condition is generated. If a FIRE condition is generated then store a failure code at location 4051 and increment the failure code register, i.e. 4052. (Both sides of the CCU share the time to observe FIRE/FAULT condition, i.e. each one observes for 167 milliseconds in turn). See Figure 3-10.

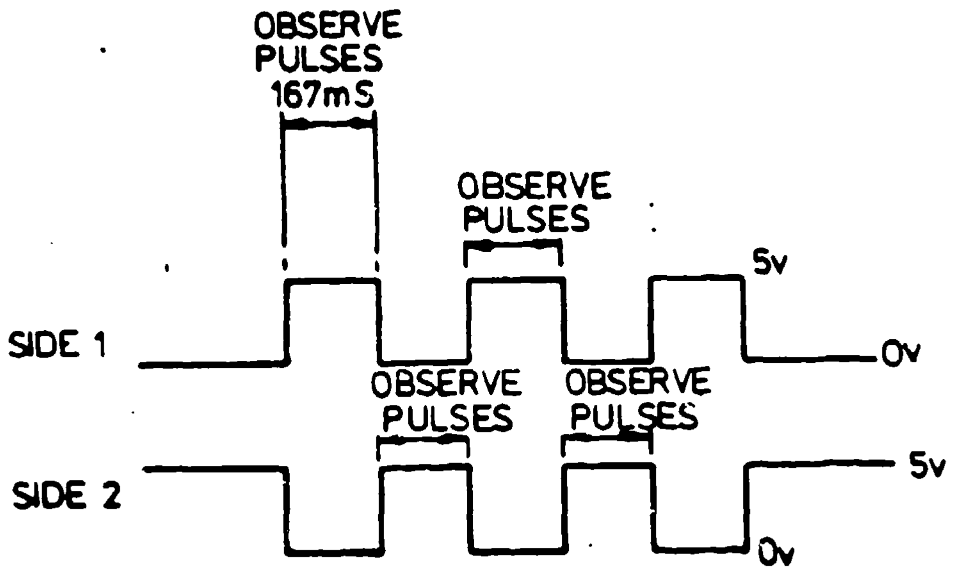


FIGURE 3-10 TIME SHARE DIAGRAM OF THE CCU

The above is a set of initial tests. The following are a further set of seven tests. If the CCU under test is of type A then all seven tests are performed and if the CCU is of type B then tests four, five and seven are performed. The method of storing PASS/FAIL status is the same as for the initial tests.

Test 1

(a) Fire all Heads on SIDE 1 (i.e. simulate Heads).

(b) Hold Heads in standby mode on SIDE 2.

(c) Wait for 6 Time Share periods and then observe a FIRE condition.

(d) If a FIRE condition exists then there is a permanent fault in the Head Drive/Supply (or logic) circuitry on SIDE 2. If no FIRE condition exists then branch to Test 2.

Test 2

Repeat Test 1 except change all references of SIDE 1 to SIDE 2 and vice-versa.

Test 3

(a) Fire all Heads on SIDE 1 (i.e. simulate heads).

(b) Fire Head one on SIDE 2.

(c) Wait for six Time Share periods and observe for a FIRE condition.

(d) If FIRE condition exists then the Head 1 Drive/Supply and Logic circuitry is functional otherwise it is faulty.

(e) Reset Head on SIDE 2.

(f) Wait for six Time Share periods and observe for NO FIRE condition.

(g) If FIRE condition exists then the Head 1 Drive/Supply and logic circuitry is faulty otherwise it is functional.

(h) Repeat Steps (b) to (g) for remaining seven Heads.

Test 4

Repeat Test 3 except change all references of SIDE 1 to SIDE 2 and vice-versa.

Test 5

If tests one to four are successful then all Head Drive/Supply and logic circuitry is functional. The remaining tests (i.e. 5, 6 and 7) are concerned with confirming the CCU's ability to respond to the adjacency sets.

NOTE

In order to reduce the probability of a false warning given by the CCU, the U.V. Heads are arranged in a set of pairs to look for FIRE in a predetermined area. This pairing of U.V. Heads is termed as the Adjacency Sets. For further details on adjacency sets see Appendix A-1, Volume II.

Adjacency sets are as follows:

The suffix refers to SIDE 1 or SIDE 2, i.e. Head 1^1 = Head 1, Side 1.

1. Head 1^1; Head 2^2
2. Head 2^1; Head 3^2
3. Head 2^1; Head 1^2
4. Head 3^1; Head 2^2
5. Head 4^1; Head 8^2
6. Head 8^1; Head 4^2

Hence for test five:

(a) Fire Head 1^1 and Head 2^2 (i.e. simulate Heads).

(b) Wait for six Time Shares and observe for a FIRE condition.

(c) If FIRE condition exists then the particular adjacency set response is corret, otherwise faulty CCU. NOTE: This time is not the Head drive/supply circuitry at fault. It could be the Logic card or the software at fault.

(d) Reset Heads 1^1 and 2^2.

(e) Wait for six Time Share periods and observe for the FIRE condition to reset.

(f) If FIRE condition exists then the CCU can not respond to the particular adjacency set correctly otherwise it's functional.

(g) Repeat the steps (a) to (f) for the remaining adjacency sets.

Test 6

In this test illegal adjacency sets are enabled to confirm that the CCU shall not respond with a FIRE condition unless the correct set of Heads see the FIRE. The illegal adjacency sets are:

1. Head 1^1; Head 3^2.
2. Head 4^1; Head 2^2.

Hence:

(a) Fire Heads 1^1 and 3^2 (i.e. simulate Heads).

(b) Wait for six Time Shares and observe for a FIRE condition.

(c) If FIRE condition exists then the CCU is faulty otherwise it is functional.

(d) Reset Heads 1^1 and 3^2.

(e) Wait for six Time Shares and observe for FIRE condition.

(f) If FIRE condition exists then the CCU is faulty otherwise it is functional.

(g) Repeat steps (a) to (f) for the remaining adjacency sets.

Test 7

The object of Test 7 is to disable some Heads such that the CCU fails after it has performed its first emitter Test.

Sets of Heads to be disabled are:

1. Heads 1^1, 2^1 and Heads 1^2, 2^2.
2. Heads 2^1, 3^1 and Heads 2^2, 3^2.
3. Heads 4^1, 8^1 and Heads 4^2, 8^2.

(a) Reset CCU RAM to zero.

(b) Fire all heads except Heads 1^1, 2^1, 1^1 and 2^2 (i.e. simulate heads).

(c) Wait six seconds and observe for a FAULT condition.

(d) If a FAULT condition exists then the CCU is functional otherwise it is faulty.

(e) Repeat steps (a) to (d) for the remaining sets of Heads.

When the G.S.E. has gone through the above tests it prints out the PASS/FAIL statuses. During test one to seven, if any failure is encountered then the Functional Test is aborted immediately and the PASS/FAIL status printed, i.e. 56 zeros will be printed except for a single "1" which corresponds to the position of the program at which the CCU failed.

e.g. 00000000001000 ......) a total of 56 digits
     00000   )

The above print out is used with the PASS/FAIL messages to determine which part of the CCU is faulty, i.e. the zeros are read as 1 to 56 starting from the beginning of the top line. The messages are listed from 1 to 56. In the above example the program failed during Test 3 while testing for Fire response when all Heads fired on Side 1 and Head 4 fired on Side 2. This statement is directly the result of determining where the "1" appeared, i.e. 11th place and then reading decode message 11 (see Appendix A-5).

The last action carried out by this program is to reset the CCU RAM to zero and proceed to 'Analyze Data' test if the G.S.E. is in AUTO mode otherwise branch to Manual Loop.

For a full list of Failure messages see Appendix A-5.
For full details on Functional Test see Appendix A-10.

3.2.4.8 Data Analysis Program

3.2.4.8.1 Summary

The purpose of the program is to analyze the data stored in the control unit as a result of a flight. This data breaks into two types, namely data that is analyzed and presented as information and data that is used to determine the status of the control unit. It is used to inform the operator of a course of action to take.

The program also accesses counts from the 10 second U.V. read test program for the analysis.

The philosophy used is that whenever one fault in the data is encountered, an action is indicated by utilizing the printer and the analysis is aborted. This is so because software to cope with multiple failures would be prohibitively long due to the many combinations involved.

3.2.4.8.2 Control Unit Data

Data included in the control unit is as follows, and it is summarized on the memory map Figure 3-11.

Ref. (a) A time marker which is stored when the pilot pushes the fire test button and is used as an event reference, such that the point in the flight where an event occurred can be determined, since the pilot would record in his flight log the time that the button was pressed.

Ref. (b) Which heads in the system are on line and which are faulty, along with a time marker denoting when the last head failed.

Ref. (c), The status of adjacency sets (which is directly related to (b) according to the configuration hard wired into the system) and the time that an adjacency set has failed.

Ref. (d) An indent. which indicated whether data has been stored by the system.

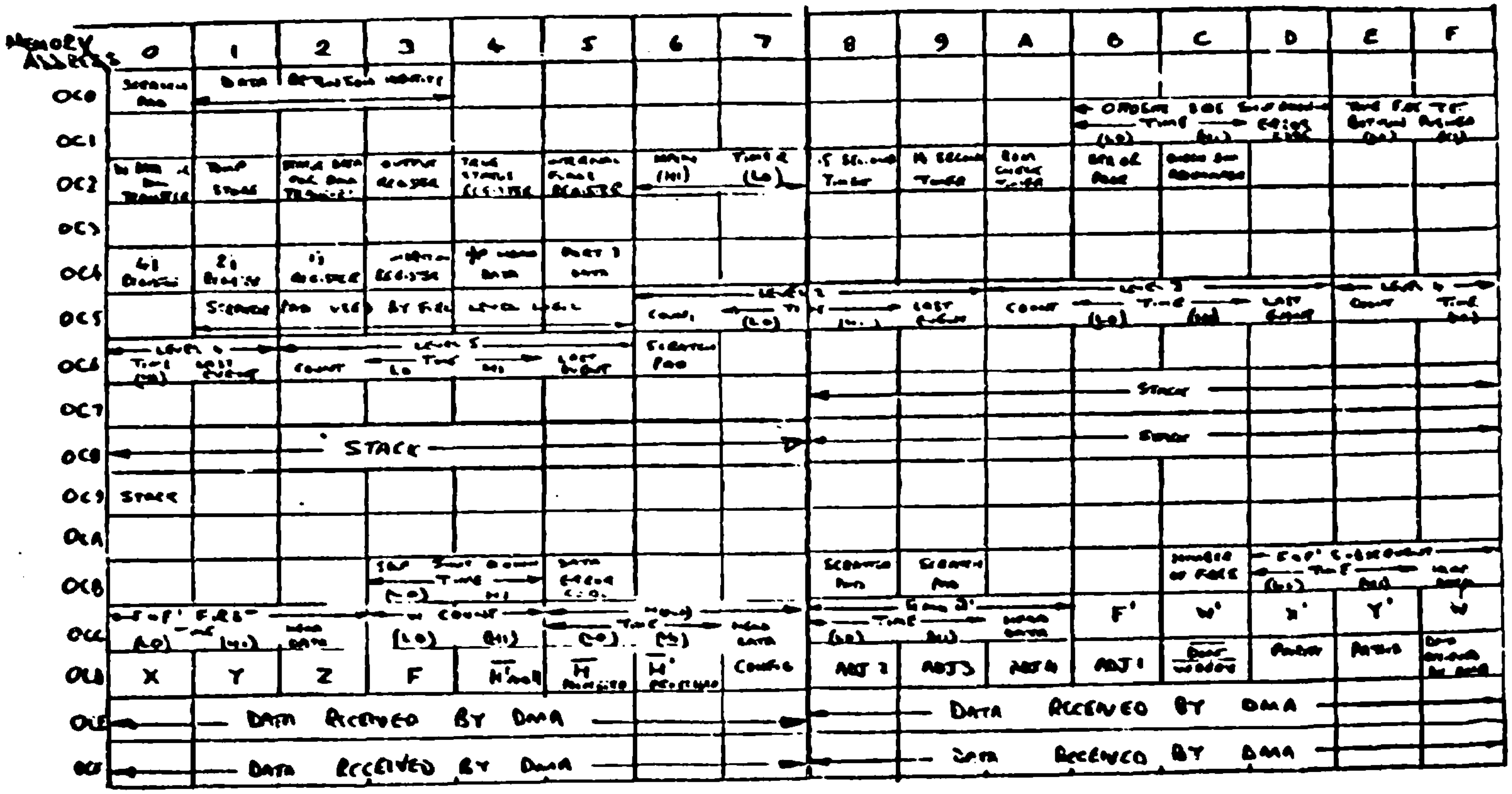


FIGURE 3-11 CONTROL UNIT DATA - MEMORY MAP

Ref. (e) A counter which is incremented on every occasion that the system recognizes that a head has caused a 'gate' to be filled (W count).

Ref. (f) Memory locations which store data indicating how near the system gets to a fire condition. These are constitued by levels 2 - 5 for a System A or levels 2 and 3 for System B. First level fire indication is indicated by (e) above. A single fire level indication consists of the latest time that this event occurred, the head or heads recording the "fire nearness" level and an accumulator storing the number of times that this level has been observed.

Ref. (g) An indication of which area indicates a fire when a first test event occurs.

Ref. (h) The time when the first fire starts to be observed by the system.

Ref. (j) An indication of which area indicates a subsequent fire event.

Ref. (k) The time when the first or subsequent fire extinguishes.

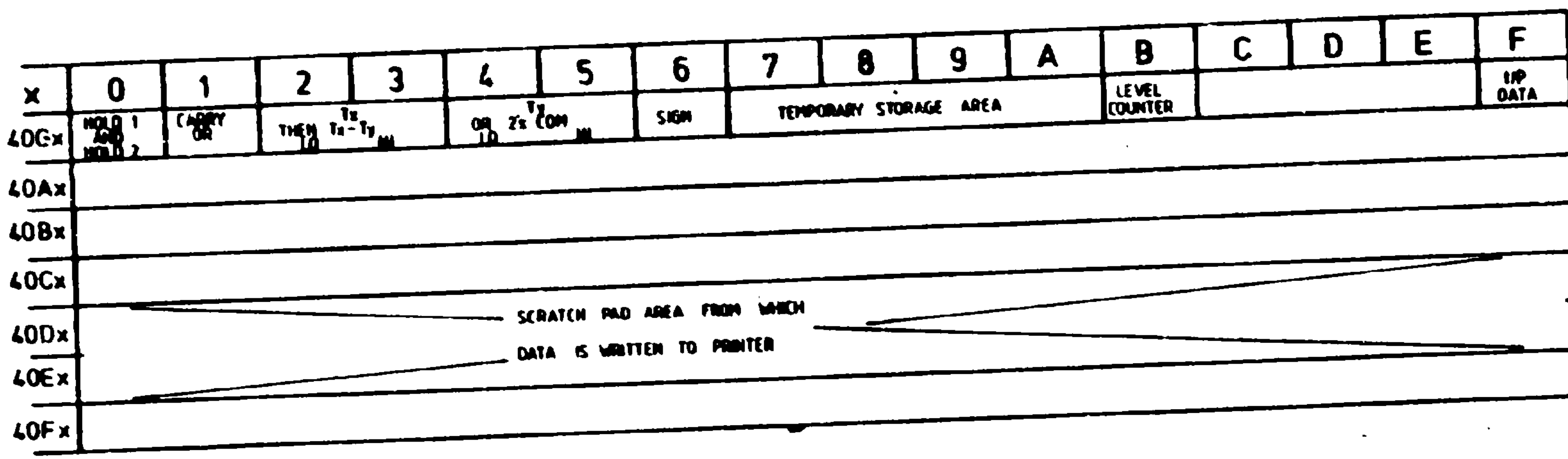
Ref. (l) The number of fires logged by the control unit.

Ref. (m) An error code and time marker recording a processor self shut down.

3.2.4.8.3 Program Operation

The following figures along with the program listings of Appendix A-11 describe the operation of the program.

Figure 3-12 lists the RAM memory of the G.S.E. computer board that it utilized by the data analysis program.



4400 to 44FF = STORED CONTROL UNIT SIDE 1 DATA

4500 to 45FF = STORED CONTROL UNIT SIDE 2 DATA

421D to 425C = HEAD COUNTS FROM 10 SECOND HEAD TEST PROGRAM

FIGURE 3-12 PROGRAM OPERATION

The program utilizes subroutines available in the GRUTIL software package, namely subroutine handling techniques, message printing and next to ASCII conversion routines. It also uses subroutines developed for the data analysis program.

Since many print outs require variables, the data is printed from a scratch pad area. When required during the program the scratch pad is wiped clean, which entails loading the pad with ASCII clear characters terminated with a character that the printer recognizes as returning the print size to small.

The data analysis program starts by performing various checks to determine whether data has been saved or whether the memory locations have been corrupted.

The check at PNT. 5 of Data Main Program 1 is a check carried out to determine whether hardware failures have occurred in the control units circuitry associated with the fire and fault switches. If this route fails to check out, the effect could appear in one of two areas, namely the circuit or the CCU and its associated circuit. The print out enables an appropriate decision to be made.

A check on system status is made, checking whether failures have occurred in flight, and checking print out failure mechanisms and times.

Adjacency set failures and head failures are looked for and if found, area of failures are printed along with the action required to rectify the problem.

Head pulse data (gathered during the 10 second head test program) is checked to determine whether emitter lines to all heads of one side are functional. This is done by observing that at least one head present for the given configuration has responded with a count of at least 128 pulses during the head test sequence. Failure to respond to this requirement is taken as an indication of failure of the emitter line and an action is printed.

Next to be analyzed is determined by the events that took place during the last flight. If a fire or fires have occurred, fire data is analyzed. If no fires are recorded, then the fire level data and background count is analyzed.

In the case of a fire, the number of fires is printed along with the area in which the first fire occurred and its start time relative to the time that the pilot depresses the CWU fire test button. The time at which the first (or subsequent) fire extinguishes along with the area in which the fire was last observed, is also computed and fed to the printer. All times are converted from increments representing head test periods, (14.8 seconds), to an approximate minute indication by dividing the computed results by 4 using the R4SHR routine. All times printed are first treated to blank out leading zeros to make reading easier.

If no fires occur, the program path analyzes background (W) counts and fire level (or nearness to fire) data.

This data is listed in tabular form with column headings of LEVEL, COUNT, TIME and HEAD.

The program accesses the appropriate level count, converts this into a BCD number, then to an ASCII format suitable for transmission to the printer. It also blanks off leading zeros. The result is then stored in the appropriate scratch pad locations, such that when the pad is written to the printer it appears in the appropriate column.

For second level up to fifth level data, the time of the event is also processed relative to the time that the pilot's fire test button is depressed. BCD conversion, zero blanking and conversion to ASCII format is again utilized along with program which allows the push button time polarity to be displayed. i.e. if the event occurs before the pilot depresses the CCU fire test button, then the event time is printed as a negative time. The head column displays heads which have been responsible for the fire event levels.

At the completion of either background analysis, or the fire analysis program, according to whether the unit is running in manual or automatic mode, the program operation will return to the manual loop until control is recovered by depressing the G.S.E. start button.

4.0 OPERATING INSTRUCTIONS

The operating instructions are shown in Appendix B.

<u>NOTE</u>

Appendix B is a copy of the G.S.E. operating manual.

5.0 CONCLUSIONS

As supported by the preceding sections and the appendices the G.S.E. design has been successful.

The hardware for the G.S.E. is shown to be duplicated sections of the CCU, such that any simulation carried out by the G.S.E. is identical to that of the CCU. The major part of the G.S.E. electronics was built on two dual size eurocards which were wire wrapped because of the very short time scales required to complete the G.S.E. design. The PCB's were designed such that it did not impose severe restrictions on modifications that would normally be expected during the design.

It was apparent during manufacture that the particular connectors used had long lead times from the suppliers and should be noted for the future.

The general design of the software presented a problem regarding data retrieval from the CCU. Because of the data transmission speed, the microprocessor had to use a utility program which gave rise to problems on start up, whereby the G.S.E. had to remember that data had been retrieved from sides A and B, otherwise the data was lost.

The first system was manufactured and pressed into service on the flight trials. It became apparent that minor design problems existed with the unit. The hardware and software problems were analyzed and solved.

REFERENCES

3-1 Graviner Ltd. Drawing; Circuit Diagram for GSE, No. 51659-062CD, Rev. D

3-2 Graviner Ltd. Drawing; Aircraft to G.S.E. Cable (No. 1), No. DSK 8601, Rev. B

3-3 Graviner Ltd. Drawing; Aircraft to G.S.E. Cable (No. 2), No. DSK 8602, Rev. B

3-4 Graviner Ltd. Drawing; Aircraft to G.S.E. Cable (No. 3), No. DSK 8603, Rev. B

3-5 Graviner Ltd. Drawing; Lab Support Cable (No. 4), No. DSK 8752, Rev. A

3-6 Graviner Ltd. Drawing; Advanced Fire Detection System Wiring, No. Z22004, Rev. D

APPENDIX A-1

MICROPROCESSOR CARD

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APPENDIX A-1

This Appendix gives functional details on the Golden River GR0430 low power single board computer.
Details down to circuit level can be obtained form

Golden River Company Limited,
Telford Road,
Bicester,
Oxfordshire OX6 OUL

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APPENDIX A-1

1. To operate the Golden River's GRO430 Low Power Microcomputer, the following minimum conditions should be established.

   (a) Zero volt power line to Pin 1 of Edge Connector (E.C)

   (b) 8.0 volt to 12.0 volt power line to Pin 3 of E.C.

   (c) Zero volt RS232 (Pin 7 of 25 pin "D") to pin 56 of E.C.

   (d) RS232 data from terminal (Pin 2 of 25 pin "D") to pin 58 of E.C.

   (e) RS232 data to terminal (Pin 3 of 25 pin "D") to pin 59 of E.C.

   (f) One side of normally open switch to pin 56 of E.C.

   (g) The Other side of switch to pin 57 of E.C.

2. Check terminal settings as follows:

   (a) 30 chars per sec (300 baud)

   (b) Even parity

   (c) 1 stop bit

   If an alternative data rate is require under 2(a), refer to drawings for link selection.

3. Connect terminal and power supply. Operate and release switch.

   The terminal should now print:

   "GRUTIL VERS X.X"

   If that happens, refer now to GRUTIL documentation.

4. Your terminal may require some or all of the following conditions:

   (a) Pin 5 of "D" Connector to +5V (Pin 2 of E.C.)

   (b) Pin 6 of "D" Connector to +5V (Pin 2 of E.C.)

   (c) Pin 8 of "D" Connector to +5V (Pin 2 of E.C.)

   (d) Pin 20 of "D" Connector to +5V (Pin 2 of E.C.)

APPENDIX A-1

1. The software is as per description for Ver 2.2 except for the following deletions:-

   @M Command no longer available

2. All subroutine addresses listed are still valid.

3. Version 4 will run in any hardware with the following requirements:

   (a) I/O Port at Unit 6, EF1, EF2 as ready lines

   (b) Program location # 8000 - #82EF

   (c) Program must be entered with X=P=O

   (d) Interrupts are disabled by Grutil upon entry.

   (e) Minimum #30 bytes RAM must be available somewhere in system. Grutil will select upper most #30 bytes in Memory Map, out of valid functional memory.

4. Version 4 takes a little longer to start because of RAM locating routine.

5. New command available:

   ?R Dump all CPU register values at the time of entry to GRUTIL, except R0 and R1. Addresses are given showing the position of the RAM that GRUTIL has located for storage of these values.

6. The bug which prevented program loading at 10cps has been corrected.

APPENDIX A-1

1. Place an erased 2716 or 2758 Prom into position O (nearest the UART) with the same orientation as GRUTIL PROM (at other end of row)

2. Check that the PROM is 'clean' by doing a CRC check, which should give FFFF, e.g.

   *MO 400 (2758 Prom)
   *MO 800 (2716 Prom)

3. Load the data to be programmed into the PROM into RAM (Locations *4000 - *47FF) and perform a CRC check on RAM.

4. Apply 25.5 Volts ± 0.5 Volts to the test point connector, TP1. Restart system with RUN-U (connect pin 57 of edge connector to ground)

5. Use copy command to copy RAM data into PROM e.g.

   *M4000 0 400 (2758) (will take ≃60 seconds to complete)
   *M4000 0 800 (2716) (will take ≃120 seconds to complete)

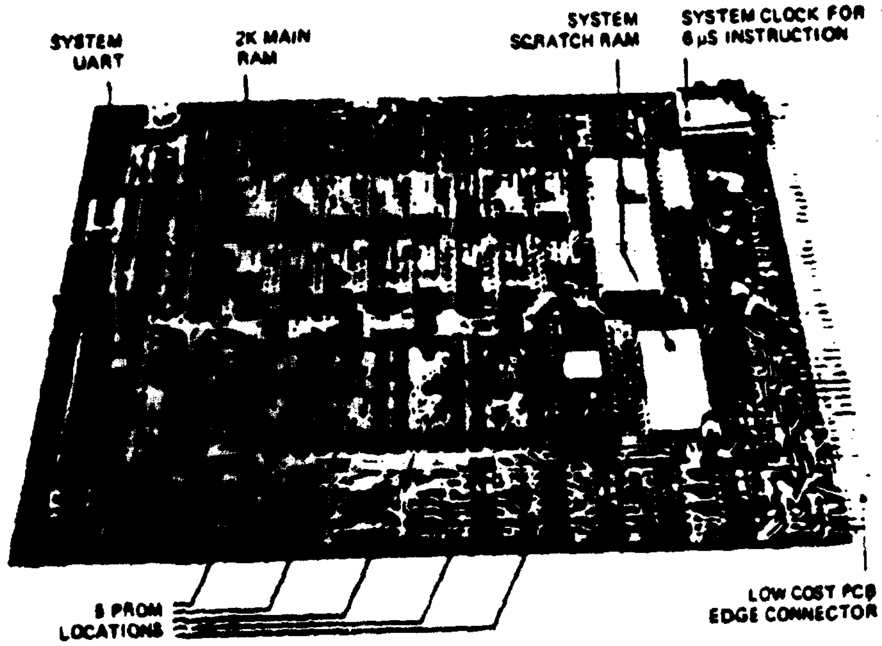
6. Remove 25V connection.

7. Restart system with RUN-U (Connect pin 57 of edge connector to ground).

8. Perform CRC of Prom to check contents, e.g. MO 800 for 2716.

GOLDEN RIVER

GR0430 Low Power Single Board Computer



MAIN FEATURES

- 1802 CMOS Central Processing Unit
- 2K Bytes Static Read/Write Memory
- Sockets for up to 10K bytes of erasable reprogrammable or mask programmed Read Only Memory
- Large I/O Capability for up to 256 [illegible]
- Complete with Utility PROM ready to start
- System UART Port on CPU Board
- On-Board PROM Programming
- Lower Power Design with total consumption typically 20mA.
- Easy to power, with only single 3V to 20VDC input, or regulated standard 5V ± 5%
- Minimum size and weight system at 15[illegible] x 203 x 25mm (6.20" x 8.00" x [illegible]), 225g (8 oz.)
- Unibus system for easy parallel bus
- Wide operating temperature range −30°C + 90°C

UNIQUE I/O PHILOSOPHY

All CPU and MEMORY functions are concentrated on the GR0430 Single Board Computer which leaves the O.E.M. free to design and implement the ideal I/O structure for his particular application. The C.P.U. Board can become a standard component for many systems with consequent reduced systems [illegible] I/O Ports are designed to interface with the 60 way bus of the GR0430 and can usually be implemented on a Single Sided P.C.B.

Standard I/O Boards are available as follows

(a) Fast Multiply Divide Board

(b) 64 Line input board

(c) Mixed I/O Board with 4 UARTS and 6 Parallel Ports

DESIGN THEMES FOR GR µP PRODUCTS

- Low Power and minimum power supply voltage constraints
- Concentration of CPU CONTROL, SYSTEM I/O and PROM/RAM on a main board, with user I/O on separate boards

GR 0430 General Description

The GR0430 Single Board contains 2K bytes of static read only memory using low power CMOS RAM chips which at most times consume only leakage current. Sockets are provided for user program PROM of up to 8K bytes (using Intel 2716 EPROM's) and the system monitor GRUTIL occupies a fifth position giving a total board capability of 10K bytes. When delivered the board contains a single Intel 2758 programmed with GRUTIL in the system PROM position.

The board has the facility to program the above 2 types of EPROM in one position on the board, without need for any special equipment other than a 26V ± 1V external power supply. The new or erased PROM is inserted into the PROM location zero, and after applying 26V the user can imagine that the first 1K or 2K (2758 or 2716 respectively) is Read/Write Memory. Single words or whole sections can be programmed at the rate of 50mS per location.

Also on board is a high speed asyncronous system port which may be connected to devices such as a Teletype ASR33, a Texas Instruments Silent 700 Terminal, or fast V.D.U. at up to 960 characters per second. This port is designed as a system entry point and can be used as a monitor or maintenance position in the final O.E.M. application.

The ... ower consumption of the GR0430 has been kept to an absolute minimum by use of low power C... technology, and by switching the NMOS EPROMs to "OFF" when not being accessed. As a result the absolute maximum power consumption of the board is around 40mA, by using certain software techniques and taking a low speed jumper link option on the board, the mean current requirement can be as low as 3mA typical. Also, since an on board regulator is used, a low cost alkaline cell such as a PP9 battery can provide the systems total electrical requirement.

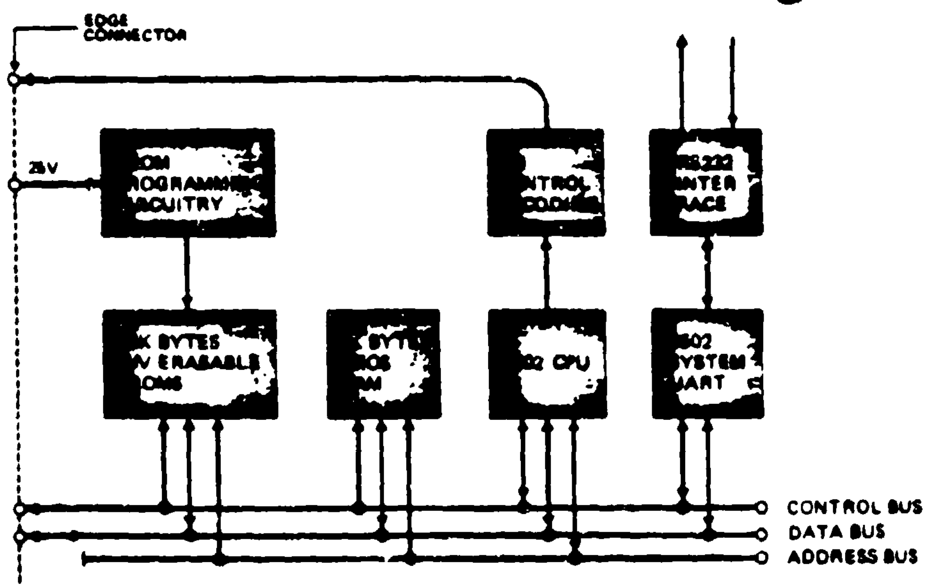
In order to maintain high reliability, a minimum of discrete components have been used as follows:

18 Resistors
6 Ceramic Capacitors
4 Tantalum Capacitors (rated 10V, run at 5V)
7 Silicon diodes
7 Transistor Packages
2 Crystals

In addition, apart from hardware and fittings, a total of 48 integrated circuits in dual in line packages, are soldered into the board. The five PROM sockets bring the total component count to 96 items. The number of inter connects is approximately 1200.

The board is normally flow soldered and hence has protective green epoxy screen to both sides.

Functional Block Diagram



1802 CPU

The CPU used on GR0430 is R.C.A.'s powerful CMOS 8 bit CDP1802, fabricated on a single LSI chip, and supplied in a 40 pin D.I.L. package. The 1802 contains 16 general purpose 16 bit registers which may be used as Program counters, data pointers and as scratch pad locations (data registers) for 2 bytes of data. An 8 bit accumulator, an overflow bit, an arithmetic pointer, and registers for interrupt control complete the C.P.U.'s principal features. The powerful but simple interrupt facilities make provision of a large number of interrupt lines unnecessary, hence maintaining a simple hardware exploitation.

APPLICATIONS

GR0430 has definite advantages in the following areas over other SBC/MBC approaches.

- **Specific I/O Requirement:** GR0430 allows user to define I/O structure and format.
- **Low Power:** e.g. data logging, petrochemical applications – typically 10mA consumption.
- **One-off:** On board PROM programmer makes GR0430 a good investment as PROM programmer.
- **Wide Temperature Range:** Most μP boards do not operate below 0°C. Due to use of CMOS Technology, this board operates from –30°C to +85°C.
- **Light Weight:** Minimum power supply removes need for bulky weighty transformers and low reliability electrolytic capacitors.

UTILITY PROGRAM GRUTIL SUMMARY

With GRUTIL, the single board GR0430 can be in use within minutes of unpacking provided a Terminal is available. Start operation by pressing reset and a solicit "—" will be issued.

[illegible]MXXXX	YYYY	Dump memory Y bytes from location X
[illegible]MXXXX	Y . . .	Load the string of hex characters into mem. starting at location X
[illegible]PXXX		Start Program operation at location X
[illegible]MXXXX	YYYY	Performs CRC check sum on Y bytes, starting at location X
1T		Prints repeatably a test alpha string
2T		Performs a check on memory RAM and reports operating locations
[illegible]M0020	20	Dumps CPU Registers at last GRUTIL entry point

Plus more functions e.g. 3P, *M, @M etc. I/O Routines are also available for use by the user program.

SOFTWARE DEVELOPMENT

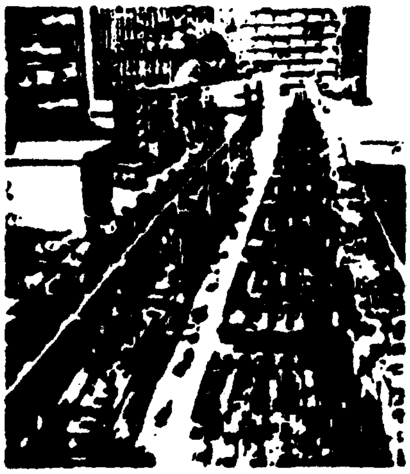
Software development is best done using the facilities of a full manufacturers development system. Resident assemblers, editors, and debugging tools greatly reduce the development time and result in efficient machine code. Using GR0430, the development engineer can easily write small programs in machine code, but for non trivial applications over say 100 bytes it is best to use development facilities, as mentioned above.

Golden River can supply software development expertise on a daily, weekly or monthly basis [illegible] for capital equipment and/or staff for all types of development requirements. The company has a full set of RCA development hardware and has been responsible for development of a number of large programs.

An assembler is available for GR0430 which allows full assemblies of programs up to [illegible] bytes long using only GR0430 and a Silent 700 [illegible] Tape Terminal. This facility is on general release.

GOLDEN RIVER – A COMPANY PROFILE

Golden River is an independant British Company operating from a modern manufacturing base at Bicester in Oxfordshire. The company has a strong background in the Traffic Data Collection Area and holds a dominant share of the market with local authorities and Central Government for traffic counting equipment.



During 1975, 76 and 77 considerable [illegible] allocated to the development of a [illegible] microprocessor systems suitable for [illegible] volume applications [illegible] GR0430 [illegible] the first product to be released [illegible] development.

Future [illegible] the same development [illegible] company [illegible] through the [illegible]

Specifications

Word Size:
Instruction 8 bits, 16 bits or 24 bits. Data 8 bits.

Instruction Set:
91 basic instructions. Control memory reference, Register Operations, Logic Operations, Arithmetic Operations, Branch instructions and I/O Control, 256 operation codes total.

Auxiliary I/O
2 single bit input lines EF3 and EF4. 1 testable output line Q.

Utility Program
1 2758 PROM ready programmed with GRUTIL-Golden River Utility Program Vers X.X.

On Board Programming Facilities
1 Position for 2716 or 2758 Programming. 50mS Programming time per location. 25V ± 1V supply @ 30mA for programming.

Cycle Time:
Basic Instruction Cycle 6.6 μS (Typically 95% of cycles will be 6.5 μS).

Cycling Time (μS)
Optional Jumper Link 104.ı μS (For very low power operation).

Memory Addressing:

PROM	0000-1FFF (2716 PROMS)
	0000-0FFF (2758 PROMS)
	0000-07FF (1832 PROMS)
PLUS	8000-87FF (2716 SYS PROM)
	8000-83FF (2758 SYS PROM)
RAM	2K BYTES 4000-47FF
PLUS	128 BYTES 8800-887F

Memory Capacity:
As above, off board memory not available.

I/O Addressing:
Each external I/O Unit has unique code of 8 bits which is strobed from data bus. Direct capacity of 256 input, 256 Output Ports.

System Port:
Designed as monitor port for the final OEM system. Asyncronous 7 bit ASCII Port 10cps to 960cps, odd/even parity.
Negative supply generated from incoming signal.

DMA Operations
Special DMA cycles to input or output. Maximum transfer rate 150,000 c.p.s. 2 lines provided for DMA in & DMA out.

Interrupts
Single vectored interrupt line provided. Maximum response time 6.5 μS.

Interfaces
All signals 5V CMOS compatible.

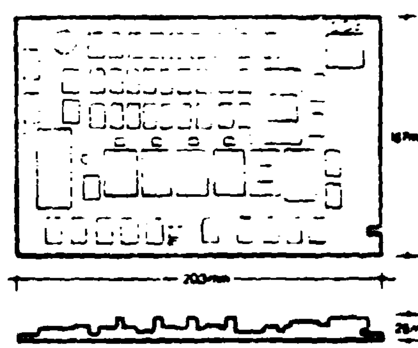
System Clock
2.457600 MHz or 153,600 Hz. Jumper Selectable.

Connectors
60 Way 0.1" P.C.B. connector with Keyway at Position 54. Single sided connections assigned.

Control Lines
Run-U causes Vectored restart to the Utility Program at location #8000. Run-P causes Vectored restart to the User Program at location #0000.

Compatible Racking Systems
Specify Vero 4μ System 4E for cards and Modules.

Physical Characteristics
Size: 157 x 203 x 25mm (6.20" x 8.00" x 1.00").
Weight: 225g (8 oz)



Temperature:
Storage −55°C −100°C. Operation −30°C + 85°C.

User Defined Jumper Links:
Slow Clock to reduce system power. 512, 1024, 2048 byte ROM chip select. System UART Baud Rate 10cps to 960cps C.P.U. voltage link for faster CPU capability.

Electrical Requirements:
Pin 3-9.0V to 20.0V @ 45mA maximum or
Pin 2-5.0V ± 5% @ 40mA maximum
If Pin 3 option is selected, 5.0V ± 5% is available at Pin 2, @ maximum 40mA.

OTHER RELATED PRODUCTS

MK4/1	Card Frame Unit 4μ x 19"
MK4/4	Power Supply & Rechargeable Cell Unit
MK4/5	Microprocessor Unit
MK4/6	2K Byte RAM Memory Unit
MK4/7	8K Byte PROM Memory Unit
MK4/11	Manual I/O Port
MK4/12	8 Bit Parallel I/O Port
MK4/13	RS232 I/O Port

LEADERS IN ELECTRONIC INSTRUMENTATION

GOLDEN RIVER
COMPANY LTD
Telford Road Bicester Oxfordshire England
Telephone Bicester 44561 Telex 837446

APPENDIX A-2

PRINTER

APPENDIX A-2

This Appendix gives full details on the printer DIGITEC 6400 series.

WARNING

This instrument is designed to prevent accidental shock to operator when properly used. However no engineering design can render safe an instrument which is used carelessly. Therefore, this manual must be read carefully and completely prior to making any measurements. Failure to do so can result in a serious or fatal accident.

SHOCK HAZARD (As defined in Underwriters Laboratories [illegible] and [illegible] Standards for Safety Twelfth Edition, dated June 23, 1969.)

"Shock hazard shall be considered to exist at any part involving a potential of between 42.4 volts peak and 40 kilovolts peak in the following cases.

A. If the current through a load of not less than 500 ohms exceeds 300 milliamperes after 0.0003 second.

B. If the current through a load of not less than 500 ohms exceeds 5 milliamperes after 0.2 second.

C. [illegible] current through a load of not less than 500 ohms to decrease to 5 milliamperes is between 0.1 and 0.2 second, and the total quantity of electricity passed through the load up to that time exceeds 4 millicoulombs.

D. If the time required for the current through a load of not less than 500 ohms to decrease to 5 milliamperes is between 0.03 and 0.1 second, and the total quantity of electricity passed through the load up to that time exceeds 75T-350T² millicoulombs, where T is the time in seconds.

E. If the potential is more than 5 kilovolts peak and if the total capacitance of the circuit is more than 3000 micromicrofarads.

NOTE: Additional factors might apply when potentials more than 40 kilovolts peak are present.

United Systems Corporation claims proprietary rights in the material disclosed hereon. This manual is issued in confidence for [illegible] and may not be reproduced or used to manufacture [illegible] without [illegible] written [illegible] USC [illegible].

SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE

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APPENDIX A-2

WELCOME

Welcome — from United Systems Corporation. Thank you for choosing the DigiTec 6400 Series alphanumeric printer. Your continued satisfaction with DigiTec products is important to us; so this manual has been prepared to promote a clear understanding of the instrument, its capabilities and its proper use. Please follow these instructions to ensure optimum performance from, and your continued satisfaction with, your 6400 Series printer.

UNPACKING AND INSPECTION

Examine the shipping carton and the printer for any evidence of damage to the instrument. If there is any indication of damage, file a complaint immediately with the carrier.

Save the shipping carton and packing materials for future storing or shipping of the instrument.

Should there be no sign of damage, proceed with the instructions in this manual. Read the Shock Hazard warning on the inside of the front cover to avoid injury due to electrical shock.

If the instrument must be returned, contact the factory for prior approval. Give a full explanation of the reason and, if a malfunction is involved, the mode of operation in which it occurred. Upon receipt of approval, ship in the original carton (or otherwise sufficiently packaged to prevent damage in shipment) PREPAID to your nearest authorized service center.

CONTENTS

Section 1

INTRODUCTION
.1 General Description 3
.2 Features 3
.3 Options 3
.4 Technical Assistance 4
.5 Specifications 4

Section 2

PANEL FUNCTIONS 5

Section 3

STARTUP
.1 Power 6
.2 Paper Loading 7

Section 4

MODEL 6410 INTERFACING
.1 Input Connections 8
.2 Interface Selection 11
.3 Input Formats 12
.4 Data Transmission Timing 12
.1 Asynchronous Operation 12
.2 Baud Rate Selection 13
.5 ASCII in the 6400 Series Printers 13

Section 5

MODEL 6420 INTERFACING 14
.1 Input Connections 16
.2 Data Transmission Timing 17
.1 Asynchronous Operation 17
.2 Synchronous Operation 17
.3 ASCII in the 6400 Series Printers 17

Section 6

SERVICE INFORMATION 18

1. INTRODUCTION

1.1 General Description

The DigiTec 6400 Series alphanumeric printers are small, desk-top printers that print first-line-up like a person normally reads. They combine the benefits of microprocessor technology with United Systems' experience as a leading manufacturer of digital printers.

Model 6410 interfaces to your system through a serial format and Model 6420 has an 8-bit, parallel bus interface. Both models print 64 different letters, numbers and symbols in a 5x7 [illegible] matrix controlled by the standard ASCII code. The electr[illegible] [illegible]itive printing technique provides quiet, reliable oper[illegible] and a high-contrast printout that is easy to read.

The 6400 Series designer-styled cases make an attractive addition to any system. In addition, special colors and your own identification are available in OEM quantities.

1.2 Features

These outstanding features highlight the DigiTec 6400 Series printers:

- Serial (RS-232-C and isolated 20 mA current loop) or 8-bit, parallel bus interface
- Data rates of 110 or 300 baud serial, or 3500 characters/second parallel
- 21 characters/line standard
  32 characters/line optional
- Input buffer for one line
- Dot matrix, electric printing
- Bold-face characters for special emphasis

1.3 Options

Option "J". Option "J" provides 32 characters/line capacity in place of the standard 21 columns.

1.4 Technical Assistance

United Systems Corporation offers assistance, if necessary, in solving application problems. We also encourage inquiries concerning special applications and custom-designed systems.

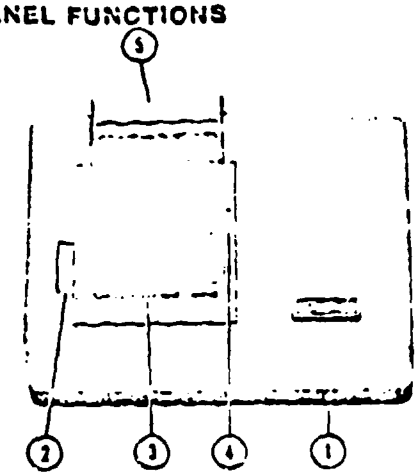
1.5 Specifications

GENERAL SPECIFICATIONS

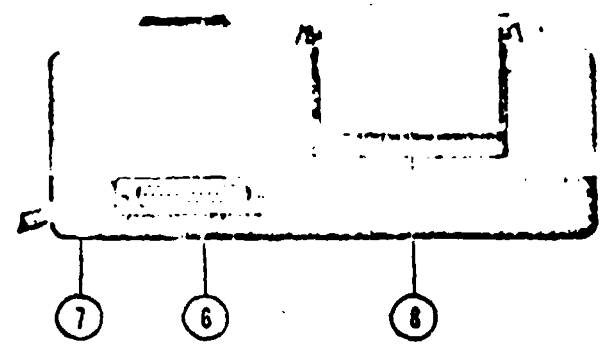
ELECTRICAL		
Model 6410 Inputs/ Outputs	RS-232-C	Mark: logic 1, -15 V to 0 V (open circuit) Space: logic 0, 3 V to 15 V
	20 mA Current Loop	Mark: logic 1, current ON Space: logic 0, current OFF (open circuit)
Model 6420 Inputs/ Outputs	Busy Out	Low: 0.45 V max, 1.6 mA typical High: 2.4 V min, 50 µA typical
	$\overline{\text{Strobe}}$ Data Inputs and Test Input	Low: -0.2 V min., 0.5 V max., ± 10 µA High: 3.0 V min., 5.0 V max., ± 10 µA
	Test Input Pulse Width	100 µs min
Isolated 20 mA Current Loop		Optically coupled
Input Buffer		Holds one line
Power		115 or 230 Vac @ 15 VA, 50-400 Hz
Operating Ambient		0° to 50° C

PHYSICAL	
Printer Life	Printhead: 3 million lines Stylus: 500,000 lines, 20 characters each
Printhead	5 x 7 dot matrix, Electrosensitive type
Characters	Height: 2.3 mm 21 per line (32 per line optional)
Print Speed	2 lines/second
Paper	Electrosensitive, 100 ft (approx. 6500 lines)
Dimensions	7.5 in. x 2.875 in. x 5.375 in.
Weight	3.5 lbs.
Interface Connector	EIA Standard (Cannon #DB-25P)

2. PANEL FUNCTIONS



FRONT PANEL



REAR PANEL

① Power ON indicator

② Paper Advance: thumbwheel, turn towards rear to advance paper.

③ Tear Bar/Window

④ Paper Feeder Release: lifts stylus, releases paper feeder mechanism so paper can be pulled out of printhead.

⑤ Paper Spindle

⑥ Input Connector

⑦ Power Cord (115/230 Vac selector and fuse are located inside the case)

⑧ Paper roll on spindle

3. STARTUP

This section explains how to apply power to your DigiTec 6400 Series printer and how to load paper in the printhead. Your printer will then be ready for operation.

CAUTION

The printer should be operated ONLY with paper installed to prevent possible damage to the printhead.

3.1 Power

The Model 6400 Series printer can be operated on either a 115 Vac or a 230 Vac power line.

It is normally shipped for 115 Vac unless specified for 230 Vac. If 230 volt operation is needed, you must follow this procedure.

① Remove the four screws, one in each corner, on the bottom of the printer case.

② Lift the front of the case top and let it pivot backwards to rest on the table.

③ The fuse is located in the lower right-hand corner, looking from the front. 115 Vac operation requires a 1/4 amp, 125 volt fuse. 230 Vac operation requires a 1/8 amp, 250 volt fuse.

④ Lift the black power cord and notice the zero-ohm-resistor jumpers underneath. The position of these jumpers selects either 115 Vac or 230 Vac operation (insulated wire may be used instead of the resistors). The positions are as follows:

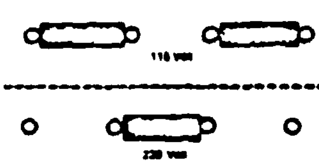
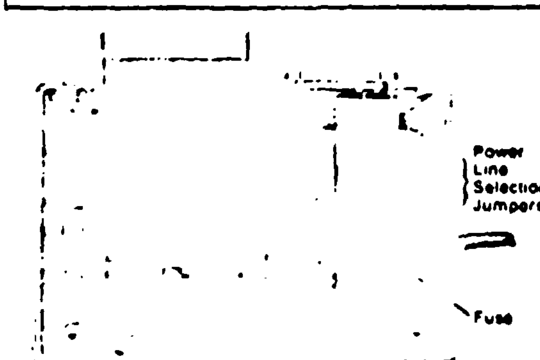


Figure 1. 115/230 Volt Selection

IMPORTANT

Be sure the proper rated fuse is installed for the power line rating selected. 115 Vac requires a 1/4 amp, 125 volt fuse. 230 Vac operation requires a 1/8 amp, 250 volt fuse.



3.2 Paper Loading

The 6400 Series alphanumeric printers are shipped without paper installed to prevent damage to the printhead during shipment. To load a roll of paper into the printer, follow this procedure:

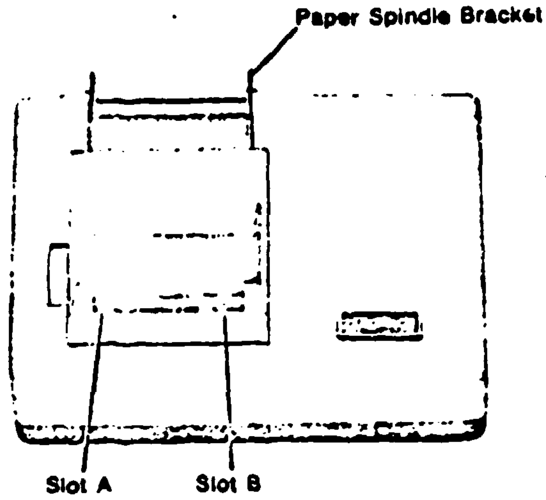
> **CAUTION**
>
> The paper is electrically conductive. It should not be allowed to contact the printer's circuits when the unit is plugged in.

1. Turn the printer ON.
2. Place a roll of paper on the Paper Spindle. Both the spindle and a roll of paper are contained in a plastic bag shipped with the printer.
3. Place the loaded spindle into the slots in the Paper Spindle Bracket. The loose end of paper should come off the bottom of the roll and up towards you.
4. Make sure all paper from a previous roll is removed from the printhead. To remove leftover paper, turn the Paper Advance dial.
5. Pass the end of paper down into Slot A in the top of the printhead.

▶ NOTE: *NEVER put new paper into the printhead until ALL paper from the previous roll is removed.*

6. Feed the paper into Slot A while turning the Paper Advance dial towards the rear of the printer. The paper automatically cycles through the printhead and out the Slot B

▶ NOTE: *The printer does not detect when the paper supply runs out. Red stripes on the paper indicate that the supply is low.*



4. MODEL 6410 INTERFACING

Your Model 6410 alphanumeric printer provides a choice of two basic types of interfaces for data communications in the serial character/serial bit mode. 1) RS-232-C and 2) 20 mA current loop. The design of your data transmitting device determines which interface your printer requires.

Through the framework of these two basic interfaces, operation of your 6400 Series printer is controlled by eleven-bit, serial binary words. These binary words include control characters coded as defined by the widely-accepted American Standard Code for Information Interchange (ASCII). The Model 6410 printer accepts a single, fixed word format.

We normally ship the Model 6410 printer set up for the RS-232-C interface at a data rate of 110 baud. But you may easily change this setup in the field to satisfy your own requirements. This section contains the information necessary to adapt your printer's input to your specific application and to make the proper interface connections to input connector J4.

4.1 Input Connections

The connections to input connector J4 of your 6410 printer are defined by Table 1 below.

Examples that illustrate the connections for each type of interface follow the table. Keep in mind that the 20 mA current loop mode may be wired for either teletype or solid-state transmitters.

RS-232-C transmitting should not exceed 70 feet in length.

In 20 mA current loop applications, a number of printers may be connected in series across the transmitter. When this is done, you must add up the total voltage drops of each printer in the series (1.8V nominal each) to determine the voltage required from your transmitter to maintain a proper current level of 20 mA in the loop.

PIN NO.	ASSIGNMENT	
8	Received Line Signal Detect (logic 1 indicates Receiver ON)	RS-232-C
7	Signal Ground	RS-232-C
2	Received Data	RS-232-C
1	Protective Ground	RS-232-C
12	External Transmitter Current Source	20 mA Current Loop
13	External Receiver Current Source	20 mA Current Loop
9	Transmit Loop Input	20 mA Current Loop
21	Transmit Loop Return	20 mA Current Loop
10*	Test Pin. Logic 0 (Ground) on this pin generates an internal test of the printer and a printed test message.	
11	Auxiliary I/O Line (specials only)	

Table 1. Connector J4

*For this function to operate, the Received Data line must be in the Marking condition

Figure 2 illustrates portions of the printer circuits that associate with each pin of connector J4.

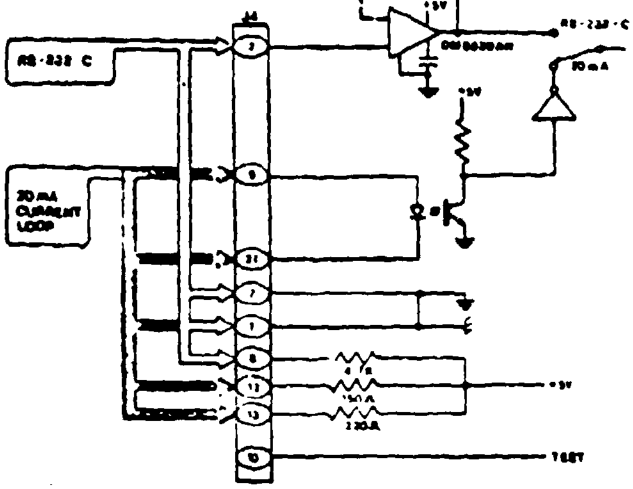
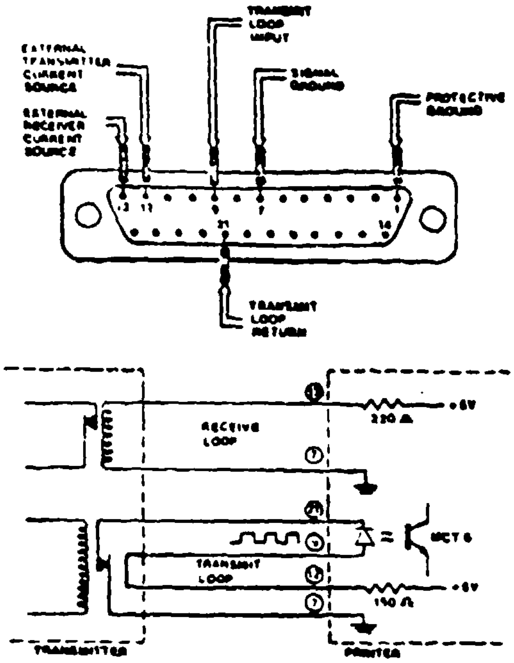
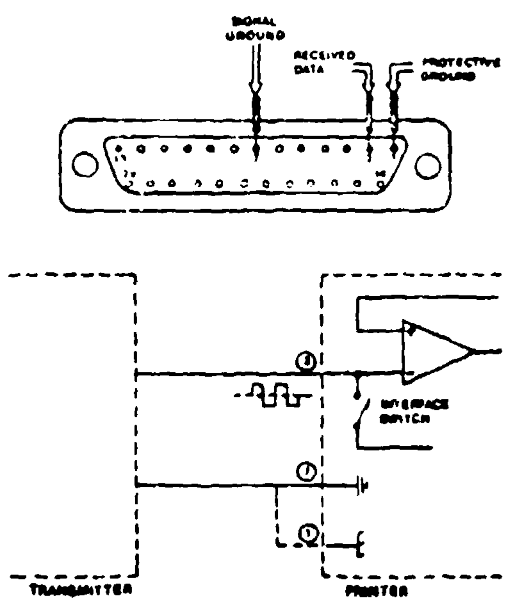


Figure 2. Model 6410 Interface

■ EXAMPLE: 20 mA current loop interface to type 33ASR Teletype only.



■ EXAMPLE: RS-232C Interface

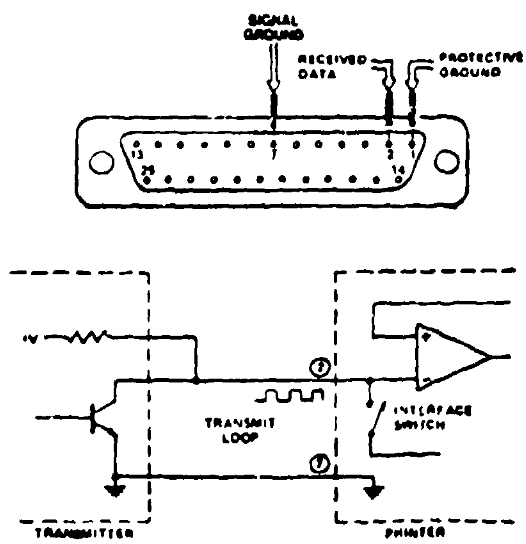


■ EXAMPLE: Solid-state transmitter interface

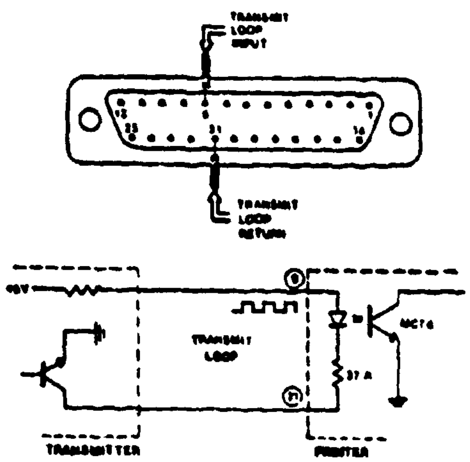
▶ NOTE: *Signal level specifications for this application are:*

	MAX.	MIN.
HIGH =	*15V*	*2.8V*
LOW =	*0.5V*	*-15V*

(LOW TO MARK)



■ EXAMPLE: 20 mA current loop, isolated input interface



4.2 Interface Selection

A plug-in jumper is provided on the printer's circuit board for selecting either RS-232-C or 20 mA current loop interface. This jumper location is shown in Figure 3.

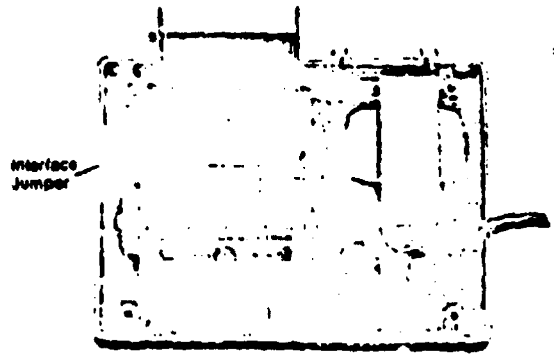
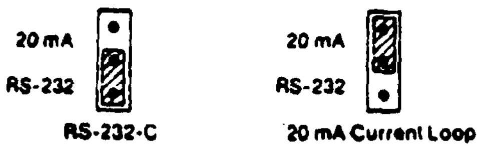


Figure 3. Interface Jumper Location

The jumper positions are as follows:



4.3 Input Formats

The Model 6410 alphanumeric printer has a fixed, 11-bit word format as follows:

- One START bit
- Seven ASCII data bits
- One PARITY bit (not checked)
- Two STOP bits

4.4 Data Transmission Timing

The timing relationship between the transmitted data rate and the ability of your Model 6410 printer to receive and print the data is determined by two factors: 1) the speed in bits/second (baud rate) of the serially transmitted data, and 2) the speed with which the printer can print one line of data. You must ensure that the transmitter does not send data faster than the printer can print it.

Your Model 6410 printer operates in the ASYNCHRONOUS mode at either of two baud rates: 110 baud or 300 baud. This section contains instructions on how to operate your printer in the asynchronous mode and how to select the baud rate that suits your application.

4.4.1 Asynchronous Operation

The maximum number of data characters transmitted between print commands must not exceed the number of characters per line that the printer records, or some of the data may be lost. The baud rate of the transmitted data and the duration of a print cycle determine this relationship. Your 6400 Series printer operates at a rate of 2 lines per second, which means that 500 ms is required to print one line of data (the print cycle duration). The baud rate depends on your transmitter.

▶ NOTE: *Print commands (ASCII 0A) may not be transmitted faster than once every 500 ms.*

In asynchronous operation, you must supply the proper timing to ensure that the transmitted rate of each line of data maintains a correct timing relationship with your printer.

If the time required to transmit one line of data is equal to or greater than the time required to complete one print cycle (500 ms), no special consideration need be given to the timing of your printing system.

■ EXAMPLE: At a rate of 110 baud, one eleven-bit data character requires 100 ms of time; so one complete line of 21 characters allows ample time for one print cycle to be completed. The transmitted stream of data may flow without interruption.

If the time required to transmit one line of data is less than the time required for the printer to print one line (500 ms), you need to give special consideration to the timing of your printing system or some of the data may be lost. This can be accomplished by inserting the proper number of Stop bits between data characters to occupy the full in transmission.

■ EXAMPLE: At a rate of 300 baud, one eleven-bit data character requires 37 ms of time. If one line of data contains only ten characters (370 ms), the complete line will have been transmitted before the print cycle is finished.

4.4.2 Baud Rate Selection

A plug-in jumper is provided on the printer's circuit board for selecting either 110 baud or 300 baud data transmission rates. This jumper location is shown in Figure 4.

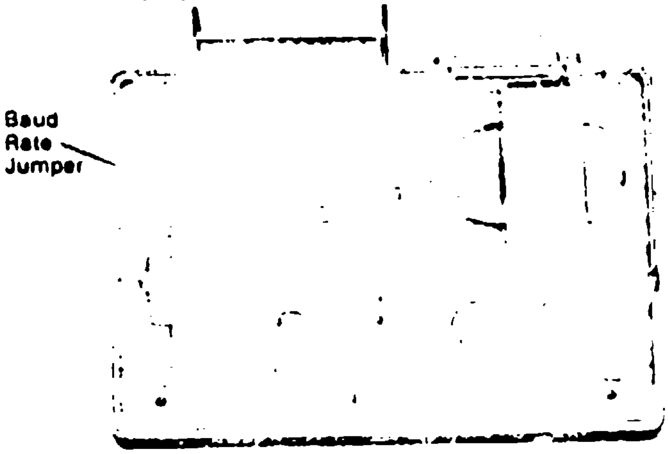
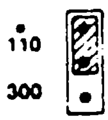
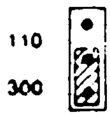


Figure 4. Baud Rate Jumper Location

The jumper positions are as follows.



110 baud



300 baud

4.5 ASCII in the 6400 Series Printers

Table 2 defines the printed characters and control functions that are produced by the partial ASCII code in the 6400 Series alphanumeric printers. The hexadecimal numbers given in the table are easier to handle than the longer binary ASCII numbers that the printer uses and are easily converted to binary when required.

Control Function	Hex	Char	Hex	Char	Hex	Char	Hex	Char	Hex
PRINT DATA*	0A	Space	20	0	30	@	40	P	50
		!	21	1	31	A	41	Q	51
		"	22	2	32	B	42	R	52
BOLD "FACE ON"	0E	#	23	3	33	C	43	S	53
		$	24	4	34	D	44	T	54
		%	25	5	35	E	45	U	55
		&	26	6	36	F	46	V	56
BOLD FACE "OFF"	0F	'	27	7	37	G	47	W	57
		(	28	8	38	H	48	X	58
		)	29	9	39	I	49	Y	59
		*	2A		3A	J	4A	Z	5A
		+	2B	;	3B	K	4B		
			2C	<	3C	L	4C		
		-	2D	=	3D	M	4D		
			2E	>	3E	N	4E		
		/	2F	?	3F	O	4F		

*Will also print without an 0A command whenever a total of 32 characters are received. With Option "J", 32 characters per line, do not send a line feed (0AH) after 31 characters. Otherwise, the automatic line feed and the one last transmitted will cause your printer to line feed twice. After 31 characters, you may send a "SPACE" character to make 32 characters to get an automatic line feed.

Table 2. ASCII Table

5. MODEL 6420 INTERFACING

Your Model 6420 alphanumeric printer provides an eight-bit, parallel interface for data communications in the serial character/parallel bit mode.

Through the framework of this interface, operation of your 6400 Series printer is controlled by eight-bit parallel binary words. These binary words include control characters coded as defined by the widely-accepted American Standard Code for Information Interchange (ASCII).

This section contains information necessary to make the proper connections to the printer's input connector J4 and an explanation of the ASCII code as it applies to your DigiTec 6400 Series printer.

5.1 Input Connections

The connections to input connector J4 of your Model 6420 printer are defined by Table 3 below. Keep in mind that you can operate your printer in either of two formats: 1) asynchronous or 2) synchronous. These two operating formats are explained in greater detail in Subsection 5.2. Examples that illustrate connections to your printer follow the table.

Pin No.	Assignment	Pin No.	Assignment	
1	Protective Ground	14	Bit 0	DATA INPUTS
2	STROBE (STR)	15	Bit 1	
4	Busy Out (word input and print)	16	Bit 2	
		17	Bit 3	
7	Signal Ground	18	Bit 4	
10	Test Pin, Logic 0 (Ground) on this pin generates an internal test of the printer and a printed test message	19	Bit 5	
		20	Bit 6	
		21	Bit 7	
11	Auxiliary I/O Line (specials only)			

Table 3. Connector J4

- Eight-line data input, TTL positive true
- $\overline{STR}$ is TTL negative true (logic 0)
- $\overline{STR}$ pulse width: 15 us min
- Busy Out: positive true (logic 1)

Figure 5 illustrates portions of the printer circuits that associate with each pin of connector J4

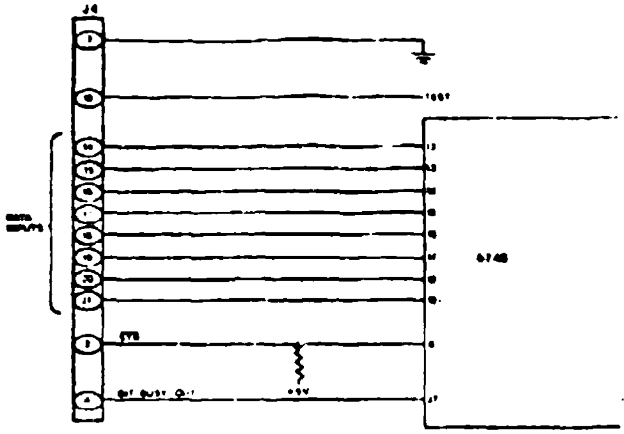
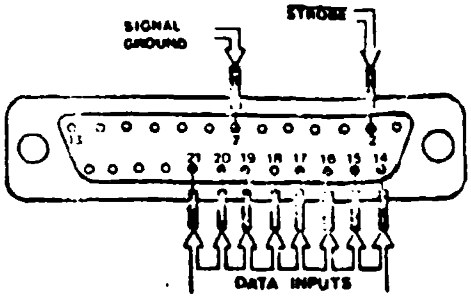
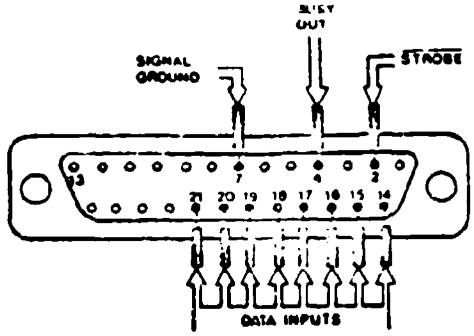


Figure 5. Model 6420 Interface

■ EXAMPLE 1 Connections for asynchronous operation



■ EXAMPLE 2 Connections for synchronous op.



5.2 Data Transmission Timing

You can choose either asynchronous or synchronous operation for your Model 6420 printing system. In asynchronous operation the transmitted data rate is not directly controlled by the printer. In synchronous operation the transmitted data rate is directly controlled by the printer. Figure 6 is a timing diagram of your Model 6420 printer.

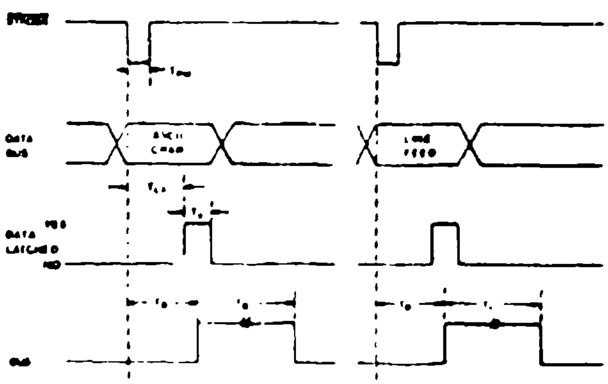


Figure 6. Timing Diagram

Symbol	Application	Limits	
		Min	Max
T_{LA}	Delay time, $\overline{STR}$ Data must be valid from 15 μs to 40 μs AFTER $\overline{STR}$ goes low.	40 μs	
T_D	Delay time, input to BUSY		50 μs
T_B	Busy time per bit		200 μs
T_L	Busy time per line	500 ms	530 ms
T_V	Data valid time	1 μs	20 μs
T_{PW}	Pulse width time, $\overline{STR}$	15 μs	

When $\overline{STROBE}$ goes True, two things happen

1) Data will be latched into printer between 15 μs and 40 μs later

2) Busy will become valid 50 μs later (maximum).

5.2.1 Asynchronous Operation

You can operate your printing system in the asynchronous mode if you observe two basic rules:

A. Characters (8-bit, [illegible] bytes) must be transmitted no faster than 3500 [illegible] characters/second with each pulse period no less than [illegible] µs.

B. Print cycle command pulses must be no less than 500 ms duration.

5.2.2 Synchronous Operation

You can operate your printing system in the full synchronous mode by using pin 4 (BUSY OUT). BUSY OUT supplies a logic 1 pulse (POSITIVE logic) every time an 8-bit data word is received by the Model 6420. This is a 230 µs pulse to interrupt the transmitter from sending any more data until the printer is ready to receive it. A longer (500 ms) pulse is also sent out from this pin every time a PRINT command is received by the printer.

5.3 ASCII in the 6400 Series Printers

Table 4 defines the printed characters and control functions that are produced by the partial ASCII code in the 6400 Series alphanumeric printers. The hexadecimal numbers given in the table are easier to handle than the longer binary ASCII numbers that the printer uses and are easily converted to binary when required.

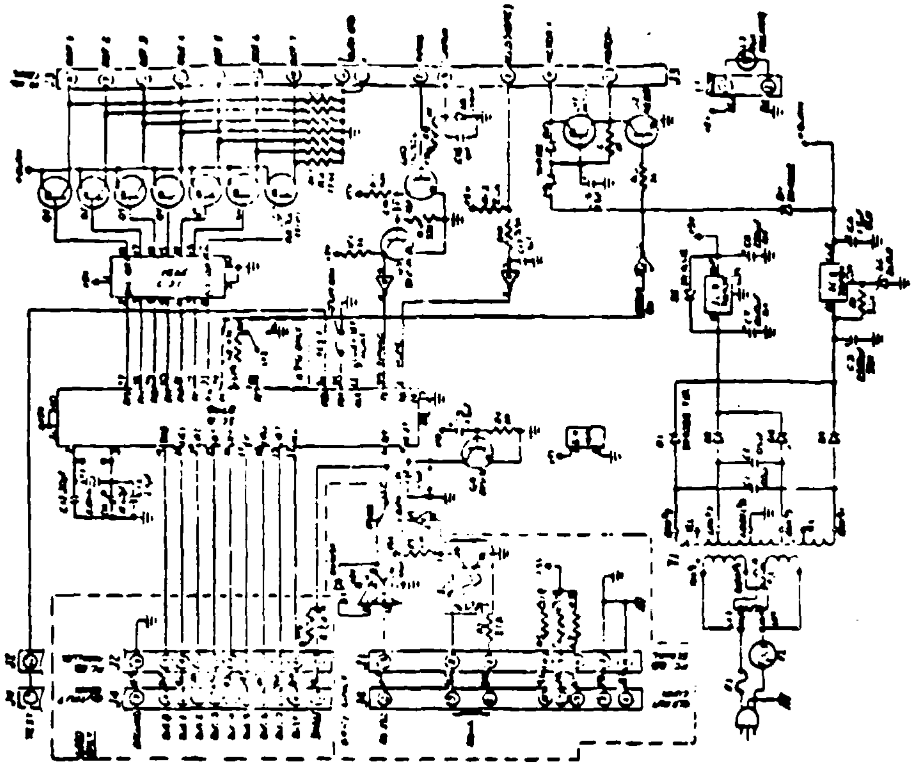
Control Function	Hex	Char	Hex	Char	Hex	Char	Hex	Char	Hex
PRINT	0A	SPACE	20	0	30	@	40	P	50
DATA*		!	21	1	31	A	41	Q	51
		"	22	2	32	B	42	R	52
BOLD	0E	#	23	3	33	C	43	S	53
FACE		$	24	4	34	D	44	T	54
"ON"		%	25	5	35	E	45	U	55
		&	26	6	36	F	46	V	56
BOLD	0F	'	27	7	37	G	47	W	57
FACE		(	28	8	38	H	48	X	58
"OFF"		)	29	9	39	I	49	Y	59
		*	2A	:	3A	J	4A	Z	5A
		+	2B	;	3B	K	4B		
		,	2C	<	3C	L	4C		
		-	2D	=	3D	M	4D		
		.	2E	>	3E	N	4E		
		/	2F	?	3F	O	4F		

*Will also print without an 0A command whenever a total of 32 characters are received. With Option "J", 32 characters per line, do not send a line feed (0AH) after 31 characters. Otherwise, the automatic line feed and the one last transmitted will cause your printer to line feed twice. After 31 characters, you may send a "SPACE" character to make 32 characters to get an automatic line feed.

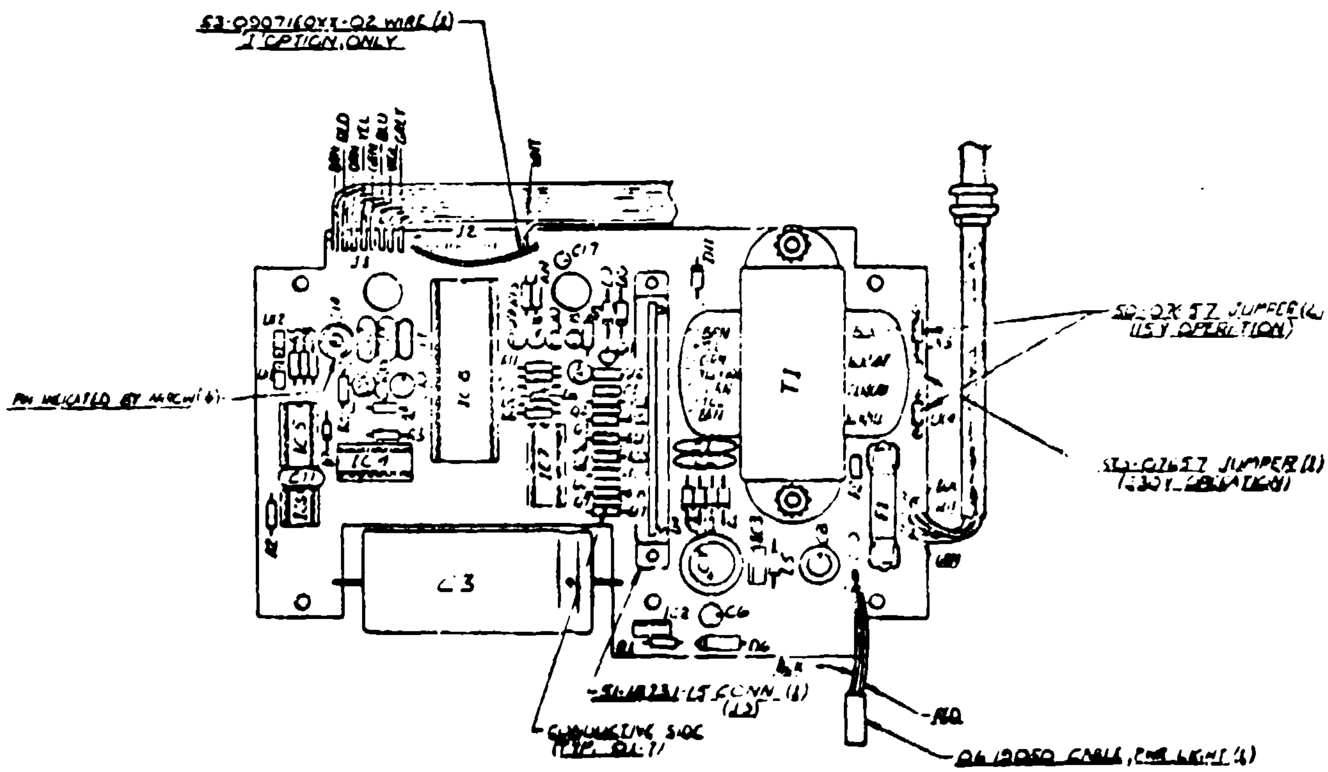
Table 4. ASCII Table

6. SERVICE INFORMATION

This section contains schematics, parts location pictorials and a parts list to assist those who are technically qualified to use this information.

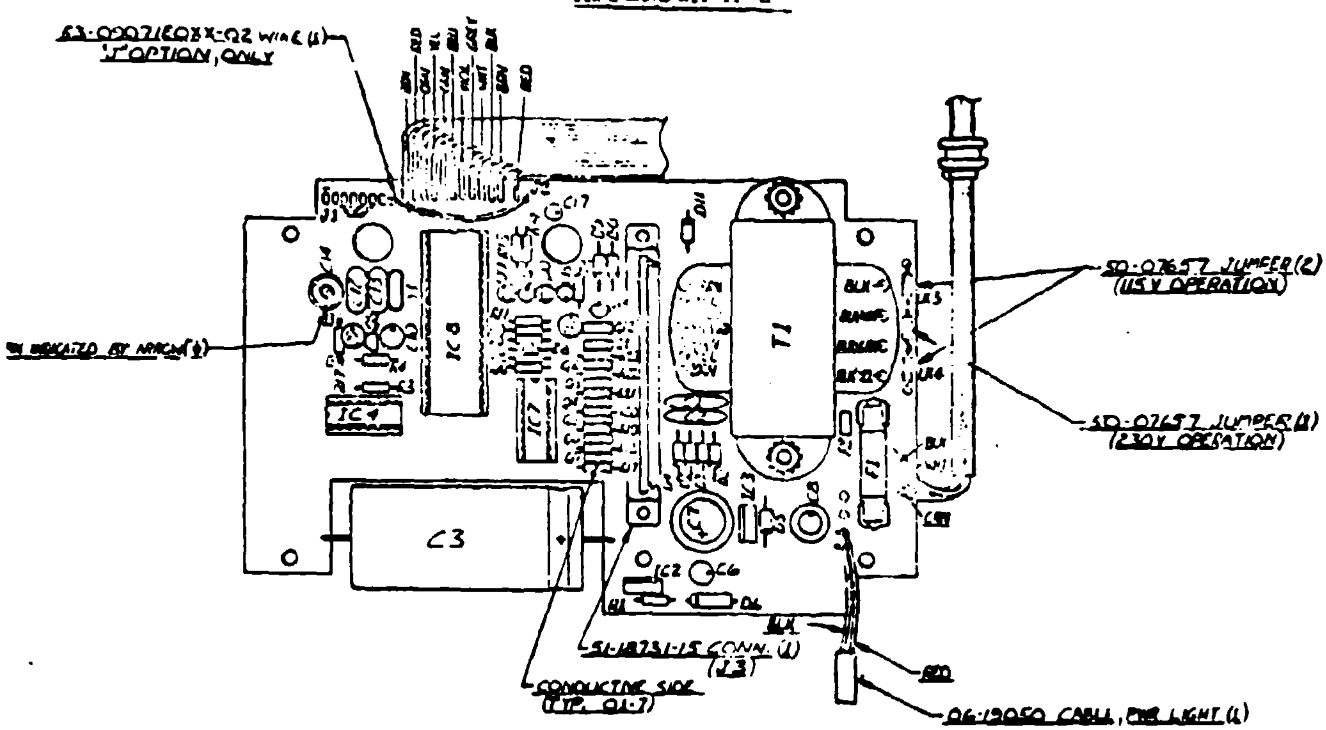


Schematic, Models 6410/6420



Pictorial, Model 6410

APPENDIX A-2



Pictorial, Model 6420

PARTS LIST

The following parts list contains the electrical (and some mechanical) components of each subassembly of the Model 6400 Series alphanumeric printers.

Under DESCRIPTION, the *type* of each capacitor and resistor is given by these codes:

CAPACITORS
- A = Aluminum
- C = Ceramic
- E = Electrolytic
- M = Mica
- P1 = Polyester
- P2 = Polystyrene
- P3 = Metalized Polycarbonate
- T = Tantalum

RESISTORS
- C = Carbon
- F = Film
- V = Variable
- W = Wire-wound

MODEL 6410

MAIN BOARD

Reference	Description	USC Number	Vendor
Complete Assembly		06-18730-01	USC
C1, 2	C, 0.05 mF, 100 V	56-10215S503KP1	Centralab, UC Series
C3	AE, 2500 mf, 50 V	56-15604MN258N50	Sprague, Type TVA
C4-6, 9, 10, 18	T, 1.5 mf, 50 V	56-12731D155N50	Siemens, B45154
C7	E, 1000 mf, 16 V	56-10203-108N16	Sprague, Type 503D
C8	E, 220 mf, 16 V	56-10203-227N16	Sprague, Type 503D
C11	M, 100 pf, 500 V	56-10210A101HL5	Elmenco, DM Series
C12	M, 30 pf, 300 V	56-10210A300JL3	Elmenco, DM Series
C13	M, 24 pf, 500 V	56-10210A240JM5	Elmenco, DM Series
C14	15-60 pf	56-18868-09	
C15, 17	T, 0.1 mf, 35 V	56-12731A104N35	Siemens, B45134
C16	T, 0.47 mf, 35 V	56-12731A474N35	Siemens, B45134

MAIN BOARD (continued)

Reference	Description	USC Number	Vendor
D1-5, 9, 10	Power diode, 100 PIV	40-07707-01	Fairchild, 1N4000 Series
D6	Zener diode, 6.5 V	40-09219-06	Schauer, SZ-6.5A
D7, 8	Signal diode	40-09297	Motorola, 1N4154
F1	Fuse, 1/4 A, Slow-Blow	52-09309-02	Buss, MDL-1/4 A
F2	Fuse, thermal	52-16830-096	Micro Devices, 60961
IC1, 2	Voltage regulator	40-16079	Fairchild, 78M24UC
IC3	Voltage regulator	40-16501	Fairchild, 78M05C
IC4	Hex inverter	40-15956	Motorola, MC14049BCP
IC5		40-17170	National Semi, DM8820AN
IC6	Opto-isolator	40-14875	Monsanto, MCT6
IC7	8-segment display driver	40-18722	Motorola, MC3491
IC8	Microprocessor	07-18750 (40-17923-02)	Intel, P8748-8
Q1-7	Power transistor	40-15168	Motorola, MJE701
Q8	Signal transistor	40-11353	GE, 2N5172
Q9, 10	Signal transistor	40-04233-05	GE, X16A565-5
Q11	Signal transistor	40-09952	Fairchild, 2N4250
Q12	Power transistor	40-14164	Motorola, MJE800
R1	C, 5.6 kΩ, 1/4 W, 5%	55-10101HK005R6	IRC, GBT-1/4
R2	C, 27 Ω, 1/4 W, 5%	55-10101HA027	IRC, GBT-1/4
R3, 8	C, 47kΩ, 1/4 W, 5%	55-10101HK047	IRC, GBT-1/4
R4, 9, 12, 15, 16	C, 1kΩ, 1/4 W, 5%	55-10101HK001	IRC, GBT-1/4
R5	C, 150 Ω, 1/4 W, 5%	55-10101HA150	IRC, GBT-1/4
R6	C, 220 Ω, 1/4 W, 5%	55-10101HA220	IRC, GBT-1/4
R7	C, 4.7 kΩ, 1/4 W, 5%	55-10101HK004R7	IRC, GBT-1/4
R10, 14	C, 33 kΩ, 1/4 W, 5%	55-10101HK033	IRC, GBT-1/4
R11, 17-23	C, 10 kΩ, 1/4 W, 5%	55-10101HK010	IRC, GBT-1/4
R13	C, 22 kΩ, 1/4 W, 5%	55-10101HK022	IRC, CBT-1/4
S1	Switch, illuminated rocker	43-18724	C & K, CK5101
T1	Transformer, power	42-17665	USC
Y1	Crystal, 2.8 MHz	40-17929	Valtec, VM6-HC18

MISCELLANEOUS

Reference	Description	USC Number	Vendor
Paper		19-17210	USC
Paper Spindle		22-17971	USC
Connector, 25-pin male		51-09174-01	Canon, DB-25P
Power Cord		53-18738	Belden, 17226
Printhead		47-18726	Pansonic, EUY-10E012LU
Case, top		30-18705	USC
Case, bottom		30-18706	USC
Jumpers, zero-ohm		50-07657	Erie, 333
Jumpers, plug-in		51-18194	Berg, 65474-002
J3	Printhead connector	51-18731-15	Cinch, 252-15-30 240
Lamp for power switch		52-09346	Wagner Elec., 335
J4	25-pin female connector	51-09174-02	Canon, DB-25S

MODEL 6420

All other parts are the same as on the Model 6410 printer

MAIN BOARD

Complete Assembly		05-18730-02	USC
No C11			
No D7			
No IC5, 6			
IC8	Microprocessor	07-18869 (40-17923-02)	Intel, P8748-8
No R2 5 8			
R17	C, 47 kΩ, 1/4 W, 5%	55-10101HK047	IRC, GBT-1/4

APPENDIX A-3

U. V. HEAD & EMITTER SIMULATION FLOW DIAGRAM

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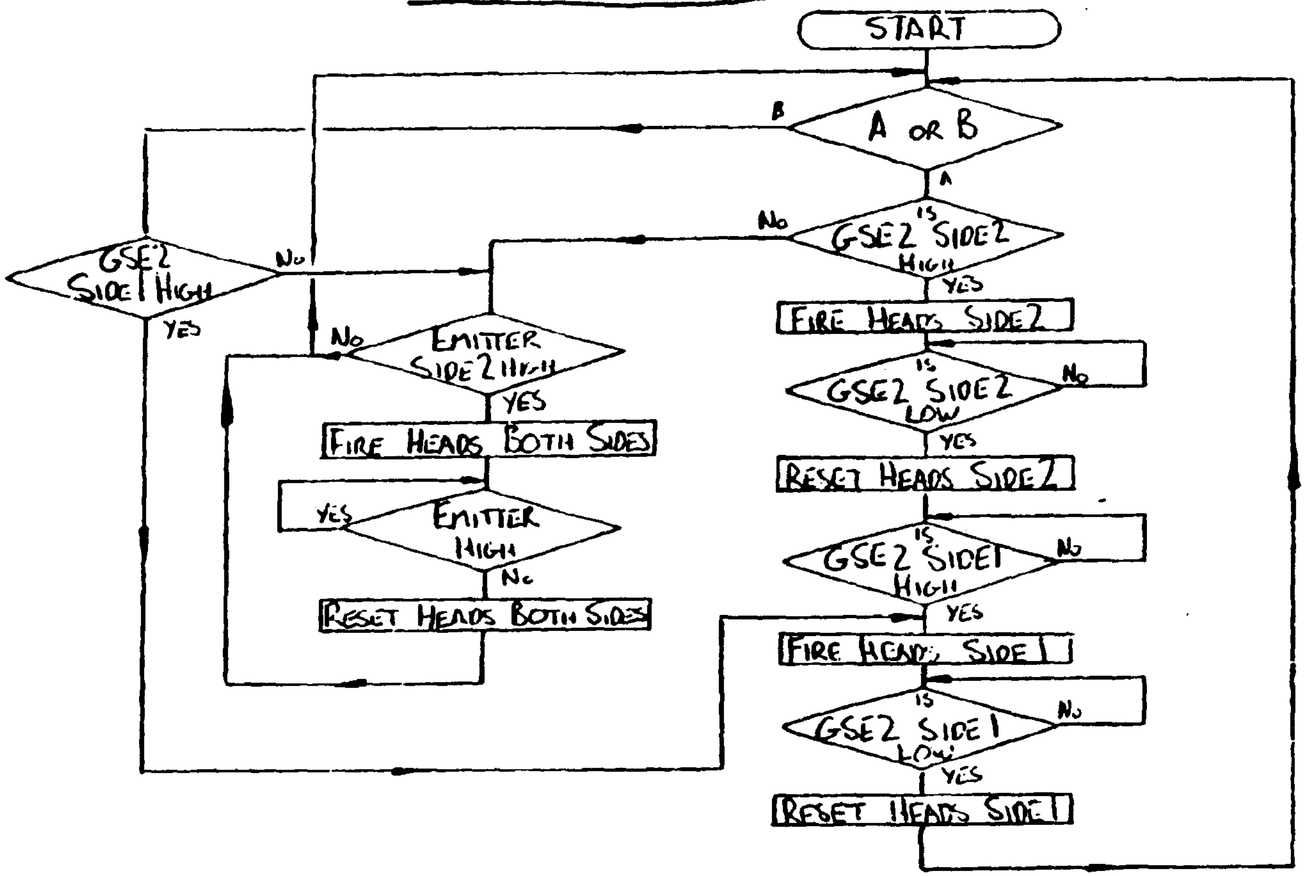
APPENDIX A-3

Head & Emitter Simulation



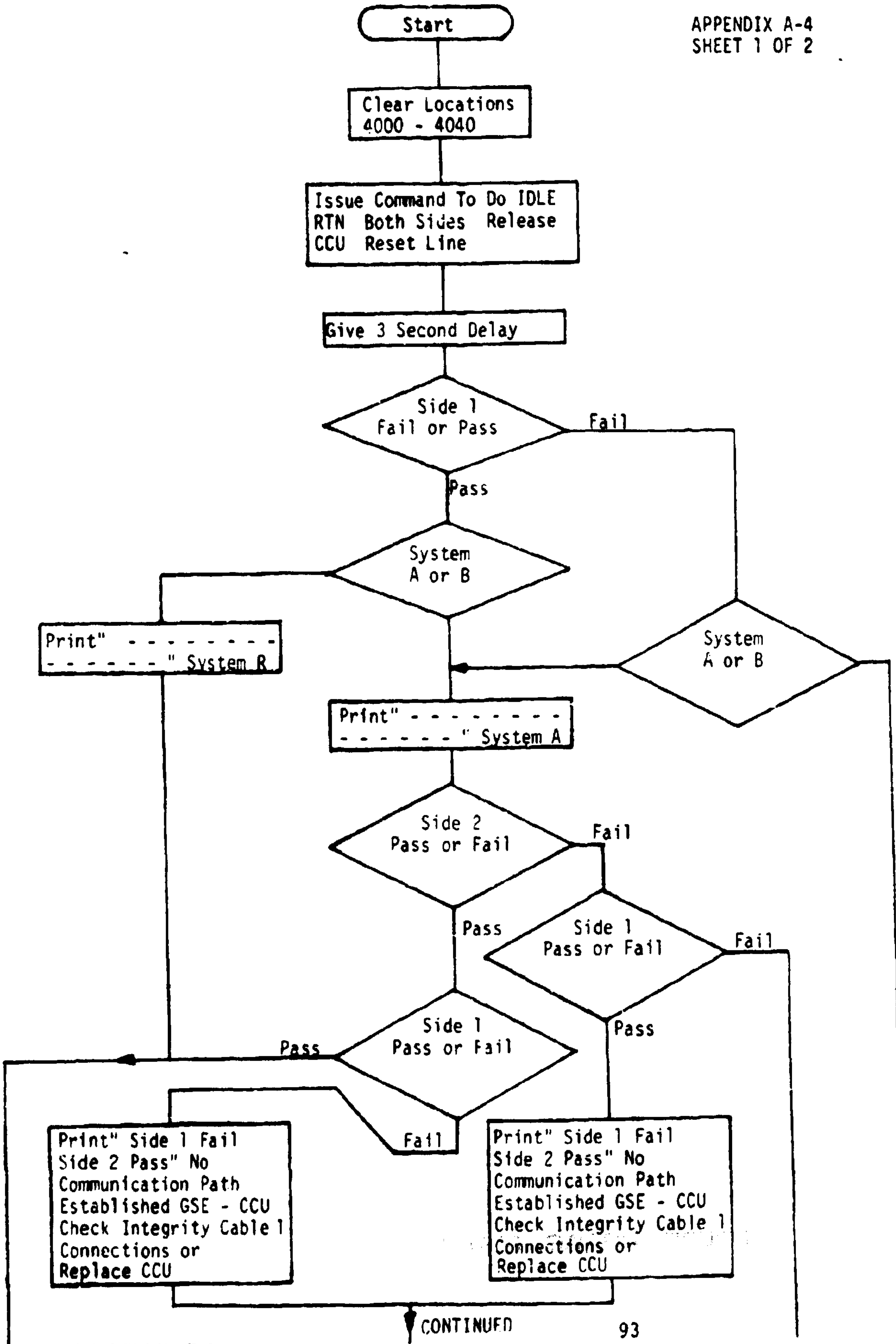
THIS ROUTINE SIMULATES HEADS & EMITTER TESTS.

(i) WHEN CCU RUNS NORMALLY

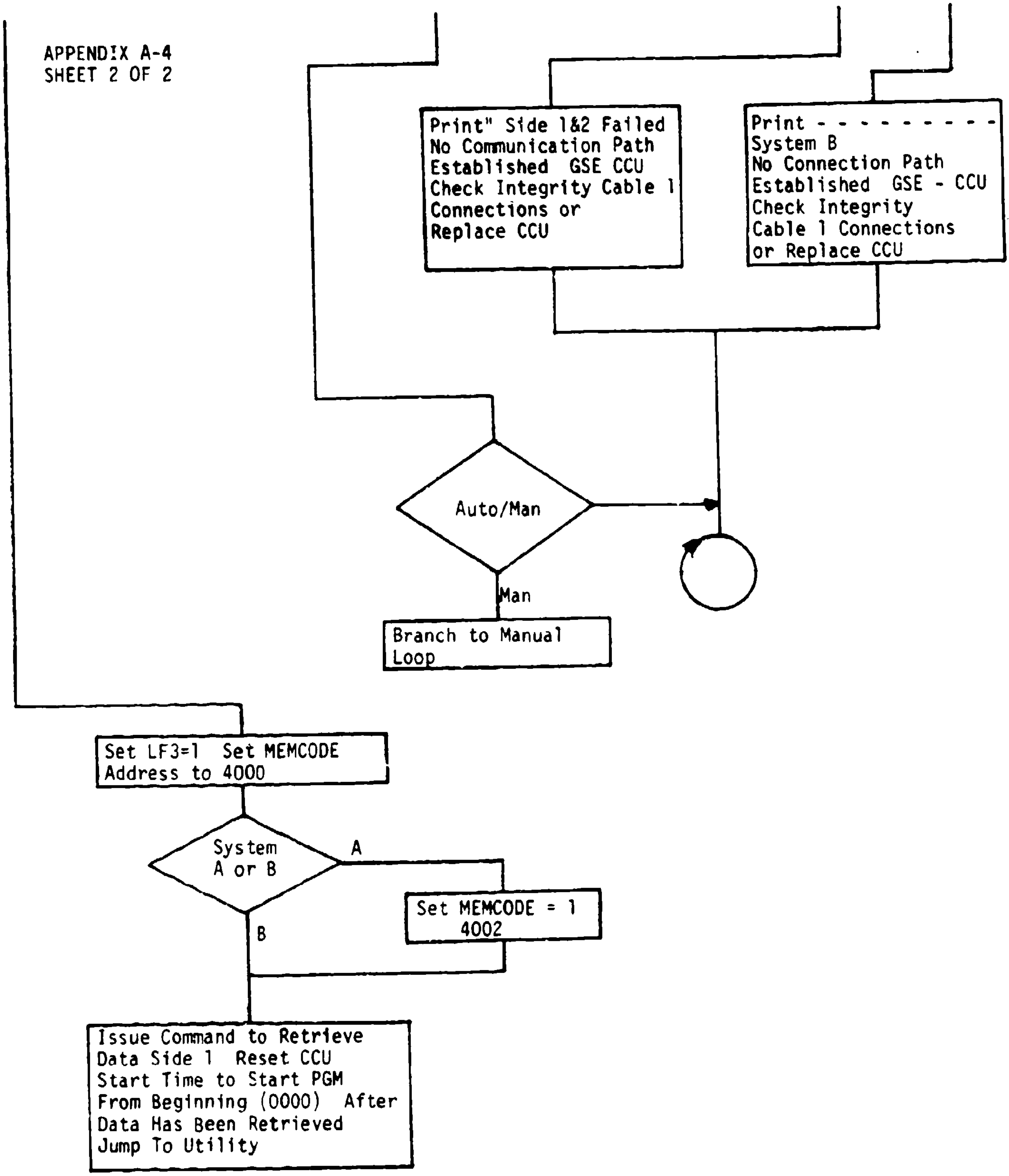
(ii) " " " " WITH LAE SUPPORT CABLE.

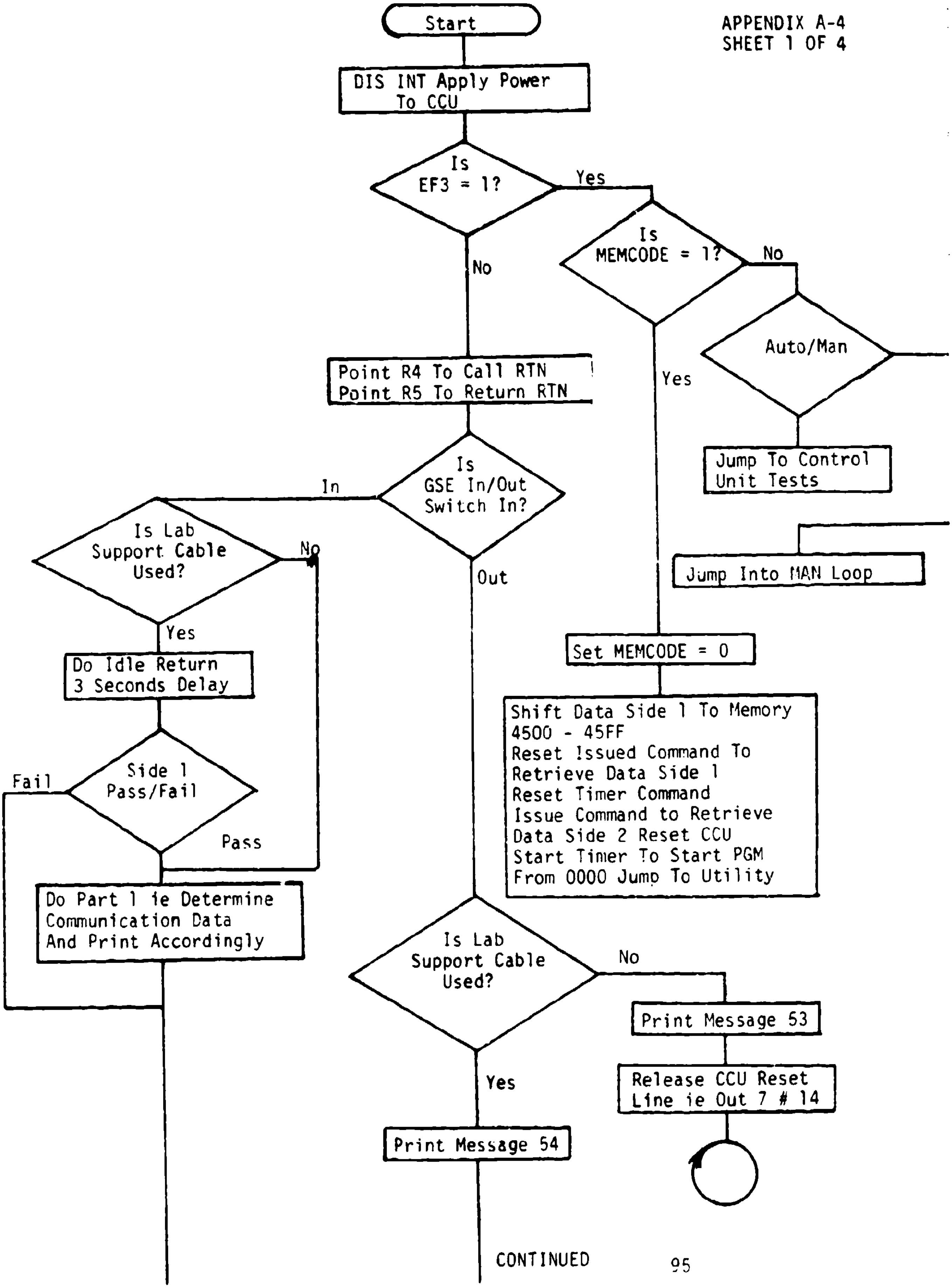
APPENDIX A-4

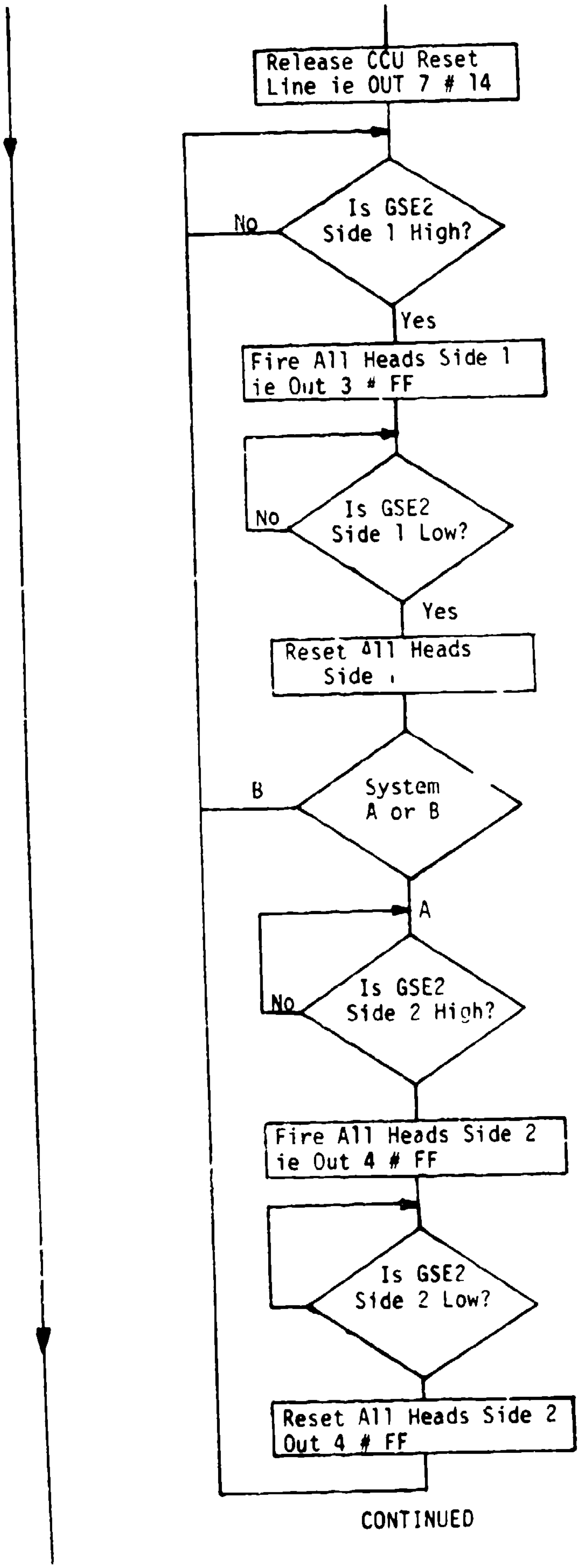
CCU-GSE COMMUNICATION FLOW DIAGRAM


Start
Clear Locations 4000 - 4040
Issue Command To Do IDLE RTN Both Sides Release CCU Reset Line
Give 3 Second Delay
Side 1 Fail or Pass
Fail
Pass
System A or B
Print" - - - - - - - - - - - - - - - " System B
System A or B
Print" - - - - - - - - - - - - - - - " System A
Side 2 Pass or Fail
Fail
Pass
Side 1 Pass or Fail
Fail
Pass
Side 1 Pass or Fail
Pass
Fail
Print" Side 1 Fail Side 2 Pass" No Communication Path Established GSE - CCU Check Integrity Cable 1 Connections or Replace CCU
Print" Side 1 Fail Side 2 Pass" No Communication Path Established GSE - CCU Check Integrity Cable 1 Connections or Replace CCU
CONTINUED

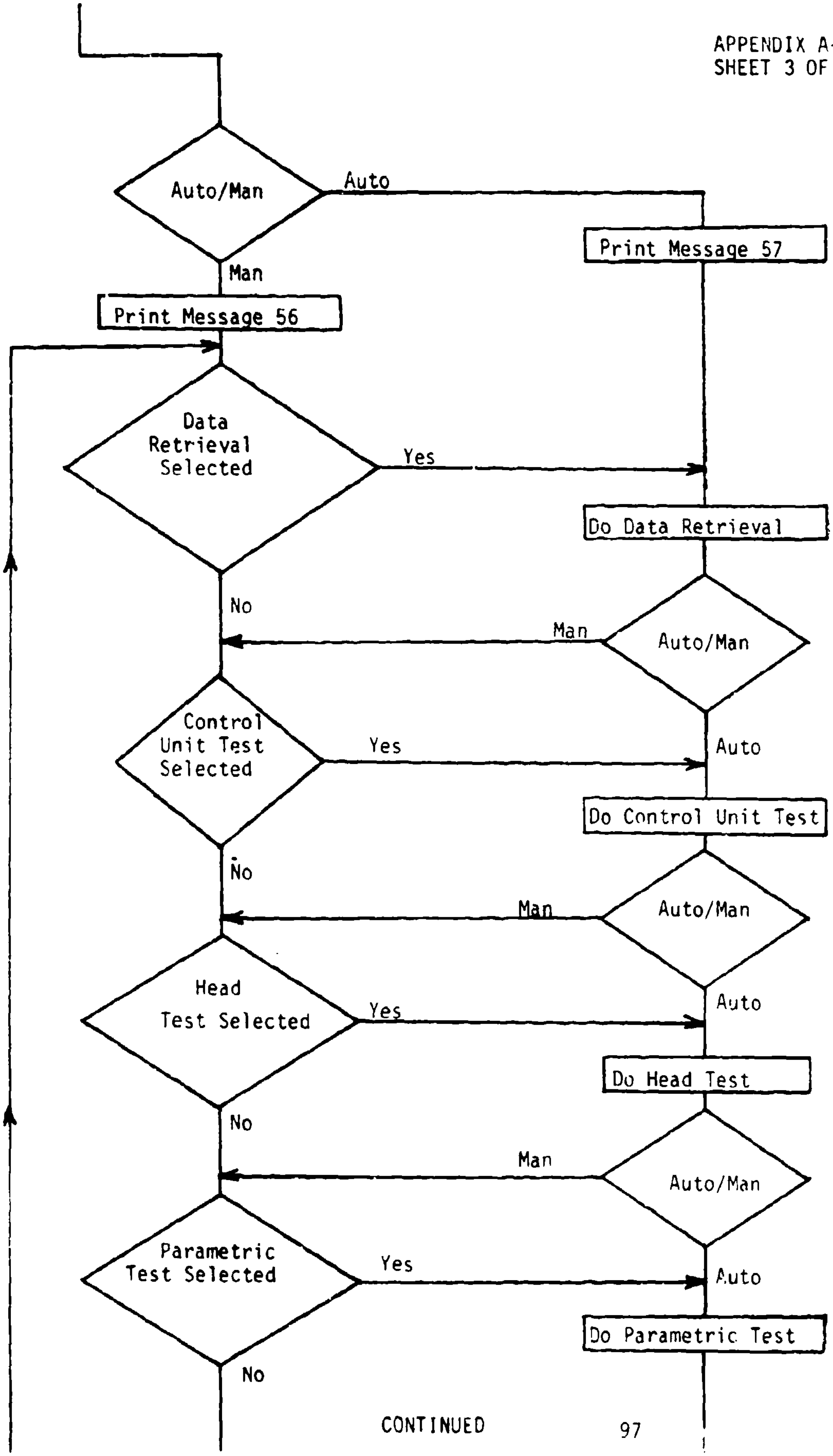
APPENDIX A-4
SHEET 2 OF 2



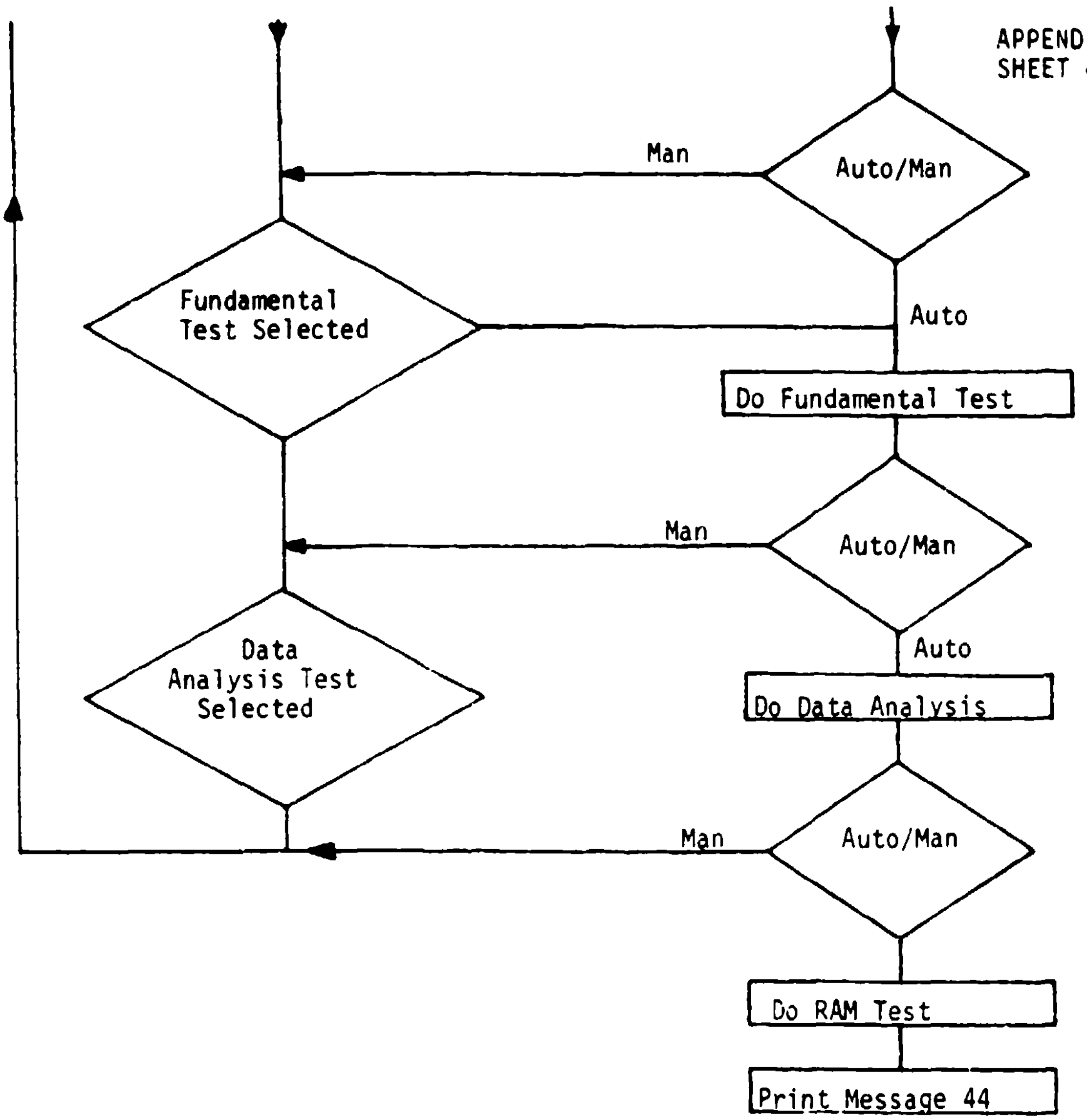

Start
DIS INT Apply Power To CCU
Is EF3 = 1?
Yes
No
Is MEMCODE = 1?
No
Yes
Auto/Man
Jump To Control Unit Tests
Jump Into MAN Loop
Point R4 To Call RTN
Point R5 To Return RTN
Is GSE In/Out Switch In?
In
Out
Is Lab Support Cable Used?
No
Yes
Do Idle Return 3 Seconds Delay
Side 1 Pass/Fail
Fail
Pass
Do Part 1 ie Determine Communication Data And Print Accordingly
Set MEMCODE = 0
Shift Data Side 1 To Memory 4500 - 45FF
Reset Issued Command To Retrieve Data Side 1
Reset Timer Command
Issue Command to Retrieve Data Side 2 Reset CCU
Start Timer To Start PGM From 0000 Jump To Utility
Is Lab Support Cable Used?
No
Yes
Print Message 53
Release CCU Reset Line ie Out 7 # 14
Print Message 54
CONTINUED

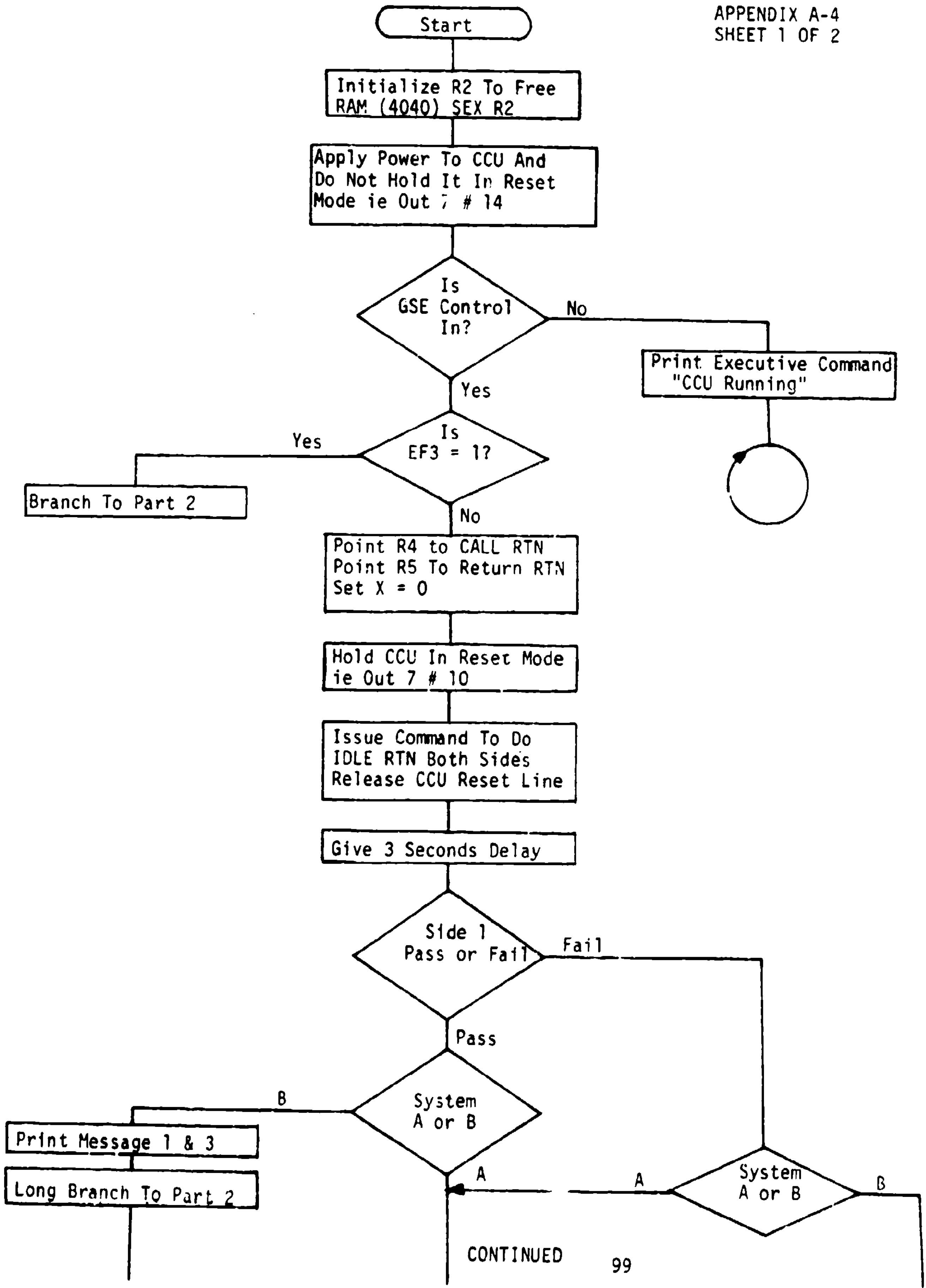

Release CCU Reset Line ie OUT 7 # 14
Is GSE2 Side 1 High?
No
Yes
Fire All Heads Side 1 ie Out 3 # FF
Is GSE2 Side 1 Low?
No
Yes
Reset All Heads Side
System A or B
B
A
Is GSE2 Side 2 High?
No
Fire All Heads Side 2 ie Out 4 # FF
Is GSE2 Side 2 Low?
Reset All Heads Side 2 Out 4 # FF

CONTINUED

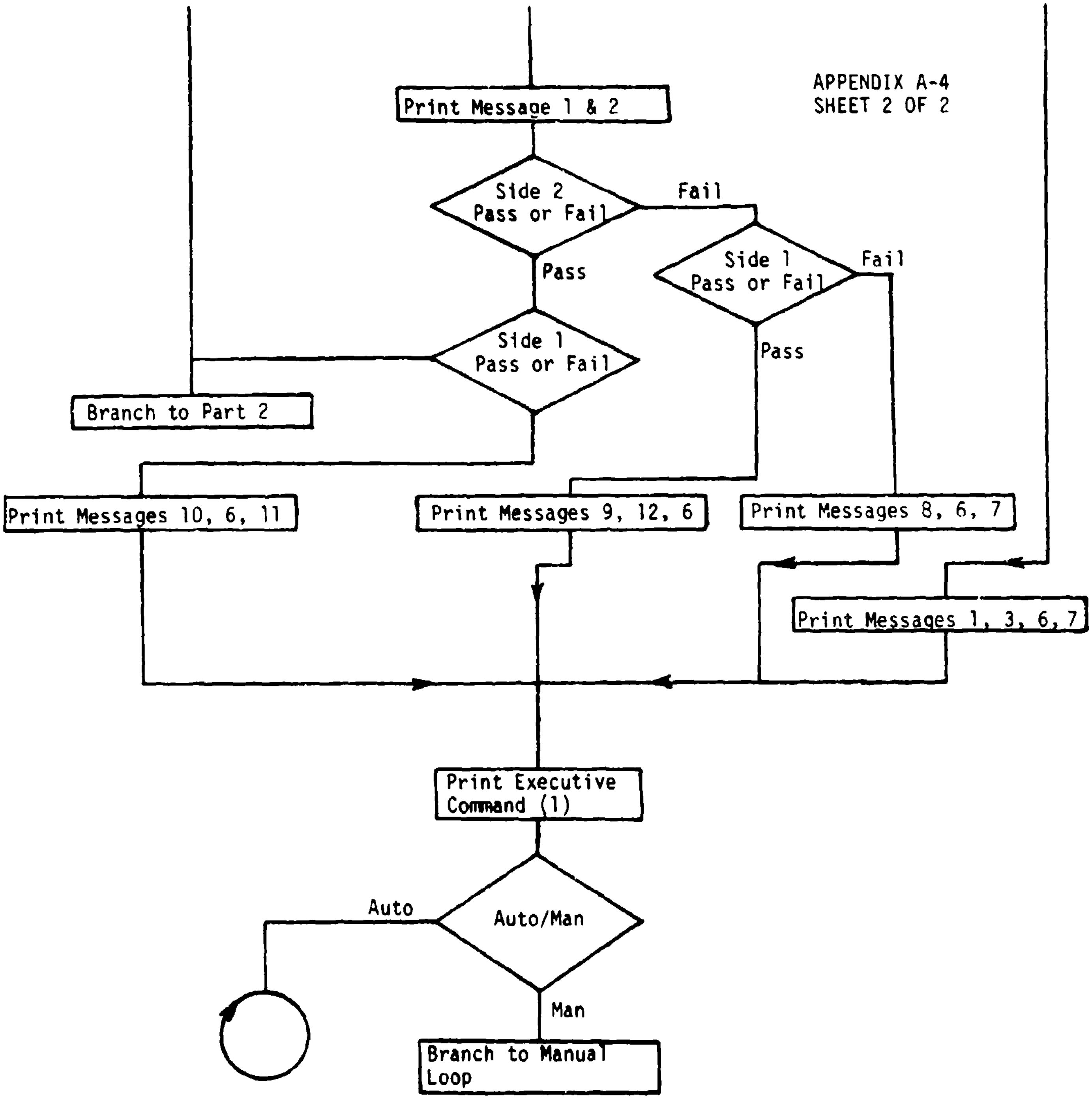

Auto/Man
Auto
Man
Print Message 57
Print Message 56
Data Retrieval Selected
Yes
Do Data Retrieval
No
Man
Auto/Man
Control Unit Test Selected
Yes
Auto
Do Control Unit Test
No
Man
Auto/Man
Head Test Selected
Yes
Auto
Do Head Test
No
Man
Auto/Man
Parametric Test Selected
Yes
Auto
Do Parametric Test
No

CONTINUED


Man
Auto/Man
Fundamental Test Selected
Auto
Do Fundamental Test
Man
Auto/Man
Auto
Data Analysis Test Selected
Do Data Analysis
Man
Auto/Man
Do RAM Test
Print Message 44


Start
Initialize R2 To Free RAM (4040) SEX R2
Apply Power To CCU And Do Not Hold It In Reset Mode ie Out 7 # 14
Is GSE Control In?
No
Print Executive Command "CCU Running"
Yes
Is EF3 = 1?
Yes
Branch To Part 2
No
Point R4 to CALL RTN
Point R5 To Return RTN
Set X = 0
Hold CCU In Reset Mode ie Out 7 # 10
Issue Command To Do IDLE RTN Both Sides
Release CCU Reset Line
Give 3 Seconds Delay
Side 1 Pass or Fail
Fail
Pass
System A or B
B
Print Message 1 & 3
Long Branch To Part 2
A
A
System A or B
B
CONTINUED

APPENDIX A-4
SHEET 2 OF 2



APPENDIX A-5

LIST OF ERROR CODES

APPENDIX A-5

This appendix consists of two parts. Both parts list a set of error messages. These messages are used to decode any failure conditions during the 'CCU Test'and' the 'Functional Test'. The first digit in the PASS/FAIL coded print out corresponds to the first error message.

PART 1 refers to the CCU Test

PART 2 refers to the Functional Test.

PART 1

Message Number	RAM Location	Error Message
1	4000	Indicates System A for Data Retrieved
2	4001	Adjacency Fail
3	4002	A/P Ident Not Available
4	4003	SIDE 1 RAMRETN - A FAIL
5	4004	SIDE 2 RAMRETN - A FAIL
6	4005	SIDE 1 RAMRETN - B FAIL
7	4006	SIDE 2 RAMRETN - B FAIL
8	4007	SIDE 1 COM-LOGIC PART 1 ABORT
9	4008	SIDE 1 INHIBIT FAIL
10.	4009	SIDE 1 COM-LOGIC PART 2 ABORT
11	400A	SIDE 1 FAULT FAIL
12	400B	SIDE 1 FIRE FAIL
13	400C	SIDE 2 COM-LOGIC PART 1 ABORT
14	400D	SIDE 2 INHIBIT FAIL
15	400E	SIDE 2 COM-LOGIC PART 2 ABORT
16	400F	SIDE 2 FAULT FAIL
17	4010	SIDE 2 FIRE FAIL
18	4011	SIDE 1 RAMTEST FAIL
19	4012	SIDE 2 RAMTEST FAIL

PART 2

Message Number	RAM Location	Error Message
1	4050	First Emitter Test Failed
2	4051	Fire Occured Immediately After Emitter Test
3	4052	Test 1 Failed
4	4053	Test 2 Failed
5	4054	Test 3 Head 1 (Lit 7) Side 2 Operate Failed
6	4055	Test 3 Head 1 Lit 7 Side 2 Reset Failed
7	4056	Test 3 Head 2 Lit 6 Side 2 Operate Failed
8	4057	Test 3 Head 2 Lit 6 Side 2 Reset Failed
9	4058	Test 3 Head 3 Lit 5 Side 2 Operate Failed
10	4054	Test 3 Head 3 Lit 5 Side 2 Reset Failed
11	405A	Test 3 Head 4 Lit 4 Side 2 Operate Failed
12	405B	Test 3 Head 4 Lit 4 Side 2 Reset Failed
13	405C	Test 3 Head 5 Lit 3 Side 2 Operate Failed
14	405D	Test 3 Head 5 Lit 3 Side 2 Reset Failed
15	405E	Test 3 Head 6 Lit 2 Side 2 Operate Failed
16	405F	Test 3 Head 6 Lit 2 Side 2 Reset Failed
17	4060	Test 3 Head 7 Lit 1 Side 2 Operate Failed
18	4061	Test 3 Head 7 Lit 1 Side 2 Reset Failed
19	4062	Test 3 Head 8 Lit 0 Side 2 Operate Failed
20	4063	Test 3 Head 8 Lit 0 Side 2 Reset Failed
21	4064	Test 4 Head 1 Lit 7 Side 1 Operate Fail
22	4065	Test 4 Head 1 Lit 7 Side 1 Reset Fail
23	4066	Test 4 Head 2 Lit 6 Side 1 Operate Fail
24	4067	Test 4 Head 2 Lit 6 Side 1 Reset Fail
25	4068	Test 4 Head 3 Lit 5 Side 1 Operate Fail
26	4069	Test 4 Head 3 Lit 5 Side 1 Reset Fail
27	406A	Test 4 Head 4 Lit 4 Side 1 Operate Fail
28	406B	Test 4 Head 4 Lit 4 Side 1 Reset Fail
29	406C	Test 4 Head 5 Lit 3 Side 1 Operate Fail
30	406 D	Test 4 Head 5 Lit 3 Side 1 Reset Fail
31	406E	Test 4 Head 6 Lit 2 Side 1 Operate Fail
32	406F	Test 4 Head 6 Lit 2 Side 1 Reset Fail
33	4070	Test 4 Head 7 Lit 1 Side 1 Operate Fail
34	4071	Test 4 Head 7 Lit 1 Side 1 Reset Fail
35	4072	Test 4 Head 8 Lit 0 Side 1 Operate Fail
36	4073	Test 4 Head 8 Lit 0 Side 1 Reset Fail
37	4074	Test 5 Adjacency 1, 2_2 Operate Fail
38	4075	Test 5 Adjacency 1, 2_2 Reset Fail
39	4076	Test 5 Adjacency 2, 3_2 Operate Fail
40	4077	Test 5 Adjacency 2, 3_2 Reset Fail
41	4078	Test 5 Adjacency 2, 1_2 Operate Fail

Contd....

Message Number	RAM Location	Error Message		
42	4079	Test 5 Adjacency 2, 1_2	Reset	Fail
43	407A	Test 5 Adjacency 3, 2_2	Operate	Fail
44	407B	Test 5 Adjacency 3, 2_2	Reset	Fail
45	407C	Test 5 Adjacency 4, 3_2	Operate	Fail
46	407D	Test 5 Adjacency 4, 3_2	Reset	Fail
47	407E	Test 5 Adjacency 8, 4_2	Operate	Fail
48	408F	Test 5 Adjacency 8, 4_2	Reset	Fail
49	4080	Test 6 Adjacency 1, 3_2	Operate	Fail
50	4081	Test 6 Adjacency 1, 3_2	Reset	Fail
51	4082	Test 6 Adjacency 4, 2_2	Operate	Fail
52	4083	Test 6 Adjacency 4, 2_2	Reset	Fail
53	4084	Test 7 Adjacency 1_1, 2_1, ~~4~~ 1_2, 2_2	Operate	Fail
54	4085	Test 7 Adjacency 1_1, 2_1, ~~4~~ 1_2, 2_2	Reset	Fail
55	4086	Test 7 Adjacency 2_1, 3_1, ~~4~~ 2_2, 3_2	Operate	Fail
56	4087	Test 7 Adjacency 2_1, 3_1 ~~4~~ 2_2 3_2	Reset	Fail
57	4088	Test 7 Adjacency 4_1, 8_1 ~~4~~ 4_2 8_2	Operate	Fail
58	4089	Test 7 Adjacency 4_1, 8_1 ~~4~~ 4_2, 8_2	Reset	Fail

Message No.	Message
1	GD/GRAVINER DFDS AUTO TEST ROUT N
2	--
3	SYSTEM A
4	SYSTEM B
5	SIDE 1
6	SIDE 2
7	NO GSE - CCU PATH CHECK CABLE 1 OR REPLACE CCU
8	TEST ABORT
9	SIDE 1 & 2 FAILED
10	SIDE 1 PASS
11	SIDE 1 FAIL
12	SIDE 2 PASS
13	SIDE 2 FAIL
	Messages 14-29 are no longer used.
30	GRAVINER DF DS F-111 CONFIRMED
31	ADJACENCY FAIL
32	CONTROL UNIT TESTS COMPLETE
33	REPLACE CCU ***************
34	Message 34 not used
35	START CONTROL UNIT TESTS
36	START UV-HEAD TEST
37	START PARAMETRIC TEST
38	START FUNCTIONAL TEST
39	Message 39 Not Used
40	UV-HEAD TEST COMPLETE
41	PARAMETRIC TEST COMPLETE
42	FUNCTIONAL TEST COMPLETE
43	Message 43 Not used
44	Message 44 Not used
	Messages 45-52 are not used.

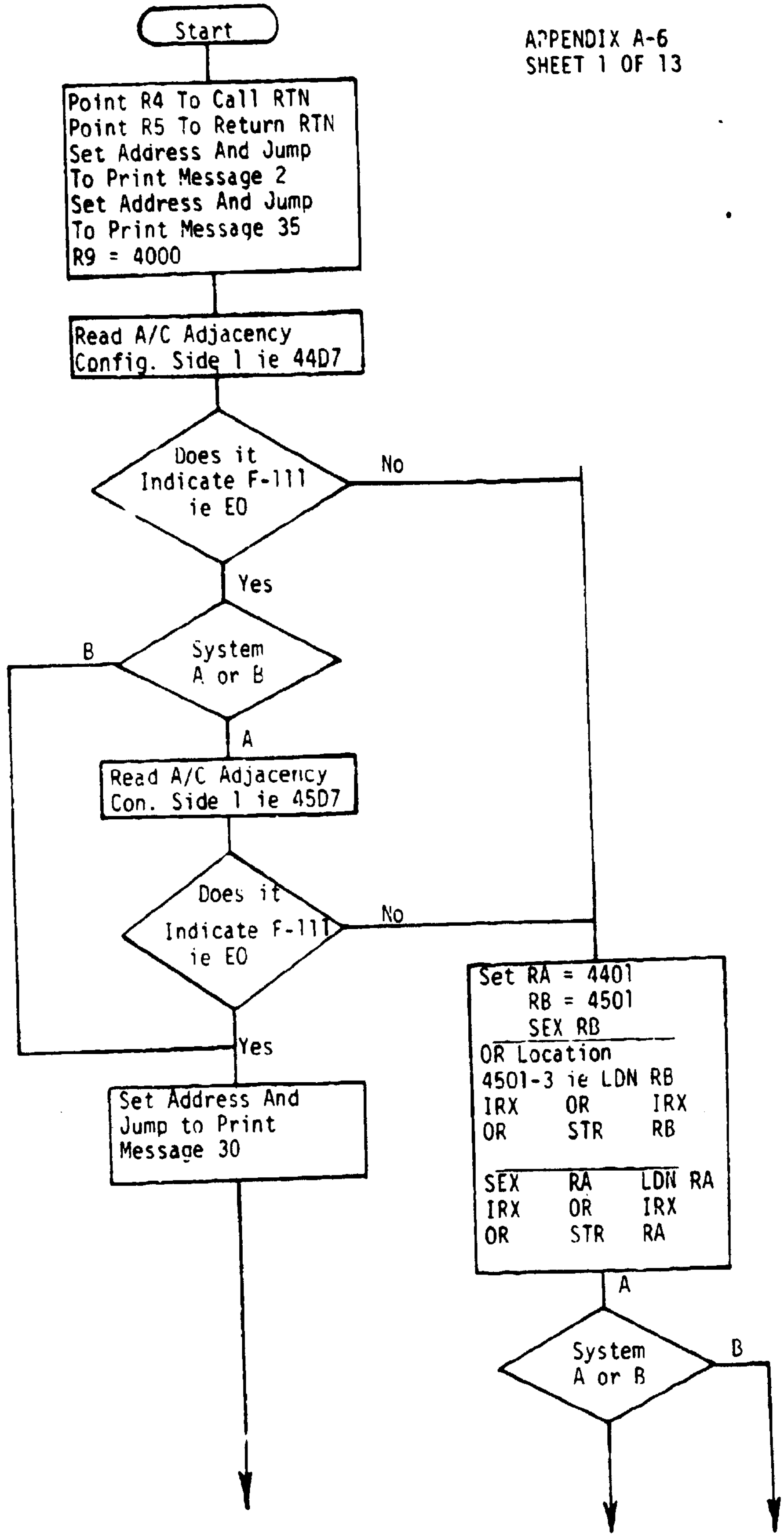
SAMPLE LISTING

Message No.	Message
53	CCU NORMAL MODE
54	Message 54 Not used
55	Message 55 Not used
56	MANUAL MODE SELECT TEST
57	AUTO MODE SELECTED
58	START READ CCU TEST
59	READ CUU TEST COMPLETE
60	AEROPLANE IDENT NOT AVAILABLE
61	COMMON LOGIC TEST ABORT
62	5.6V SIDE 1 FAILED
63	5.6V SIDE 2 FAILED
64	320V SIDE 1 FAILED
65	320V SIDE 2 FAILED
66	EMITTER FAILURE 01
67	EMITTER FAILURE 02
68	EMITTER FAILURE 03
69	EMITTER FAILURE 04
70	EMITTER FAILURE 05
71	EMITTER FAILURE 06
72	EMITTER FAILURE 07
73	EMITTER FAILURE 08

APPENDIX A-6

CCU TEST FLOW DIAGRAM

APPENDIX A-6
SHEET 1 OF 13



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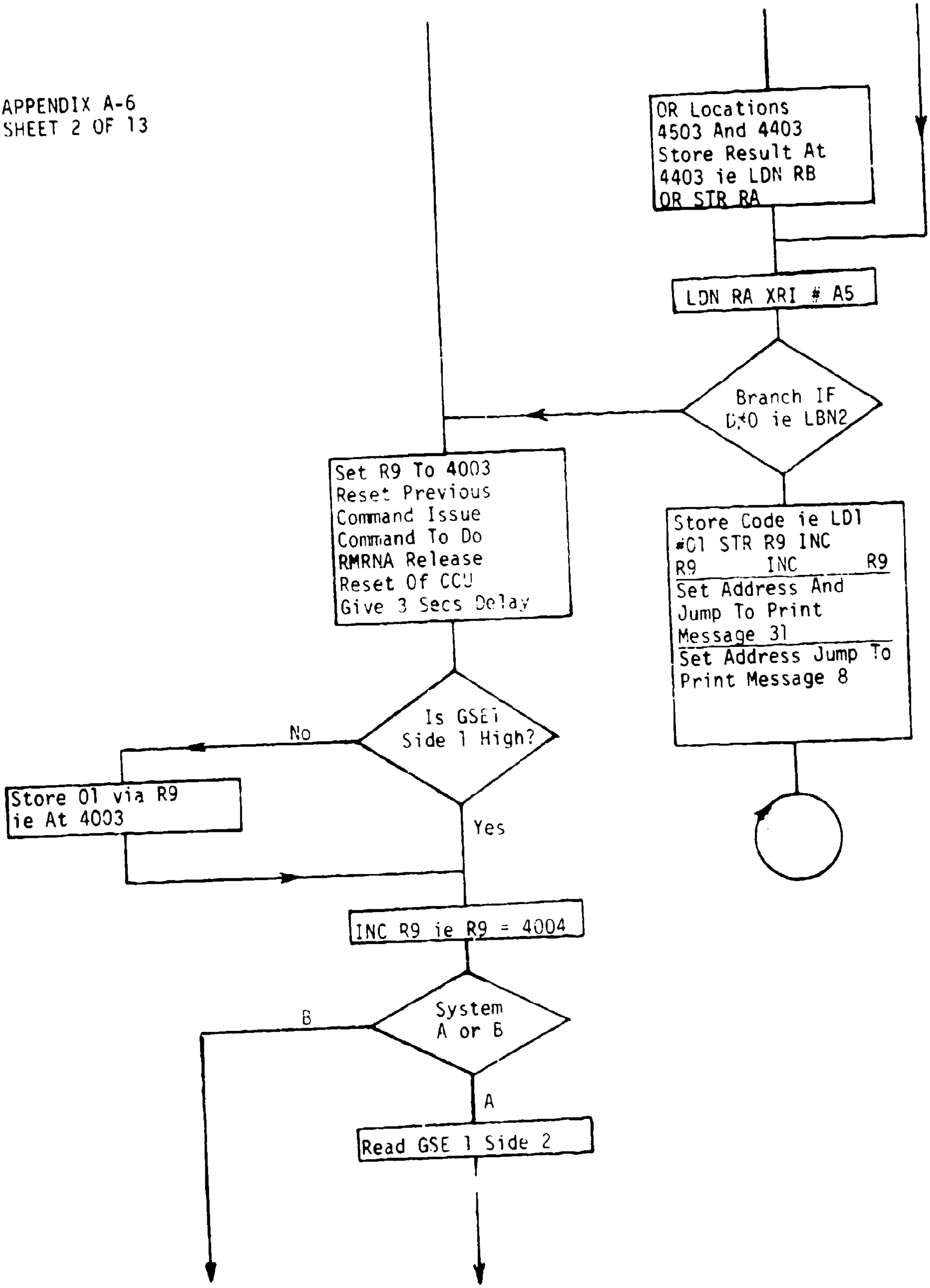
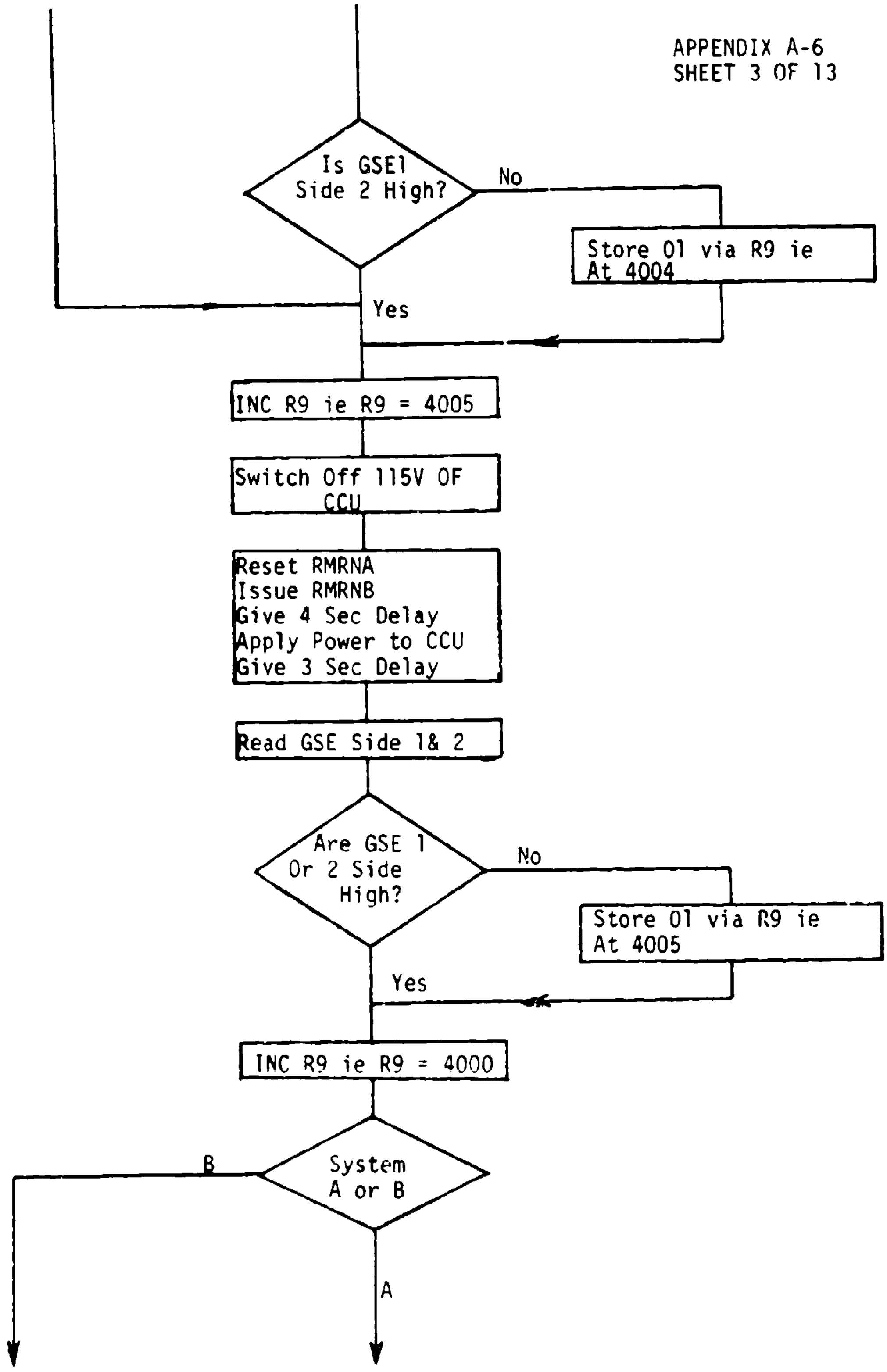
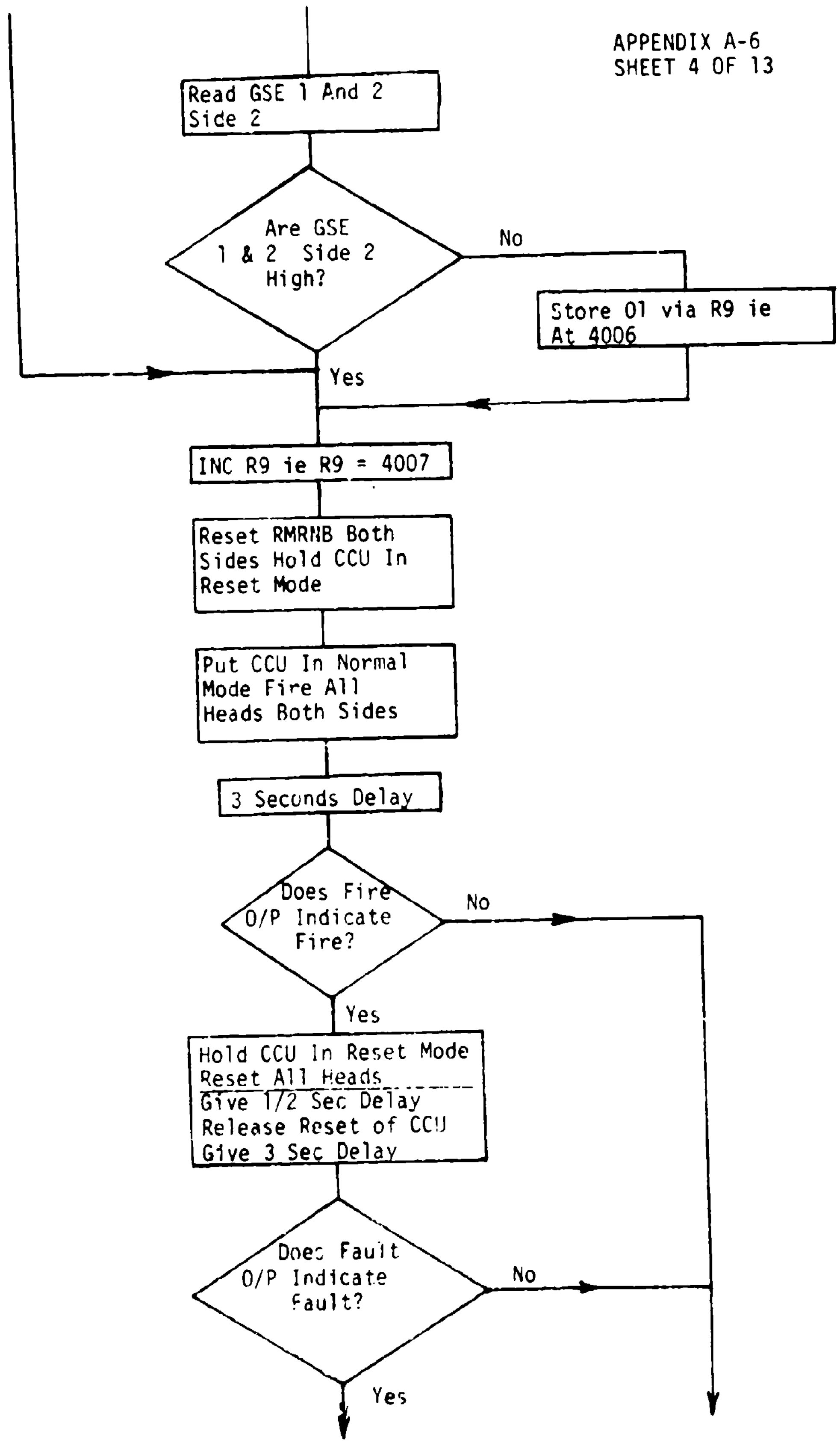
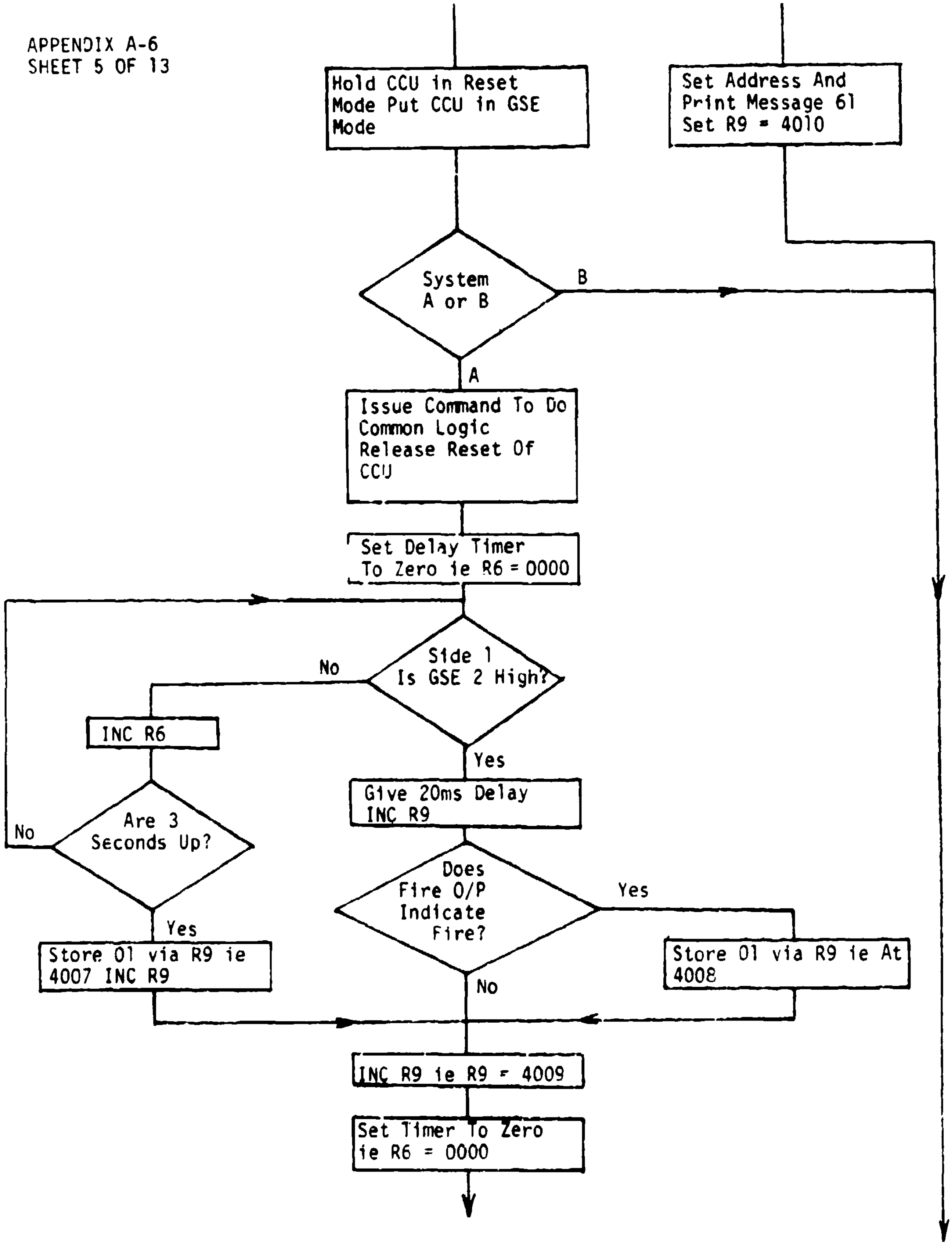
APPENDIX A-6
SHEET 2 OF 13

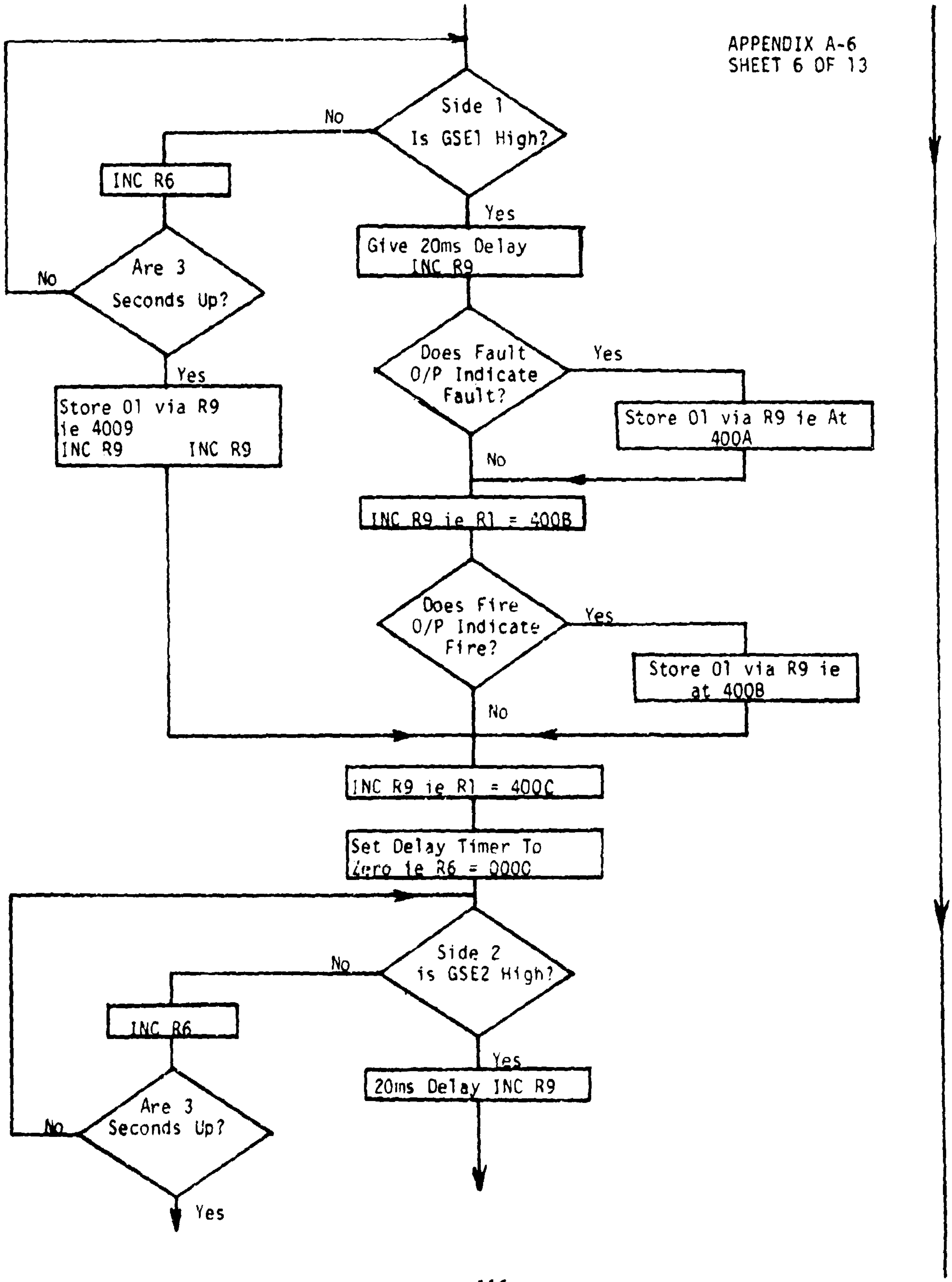


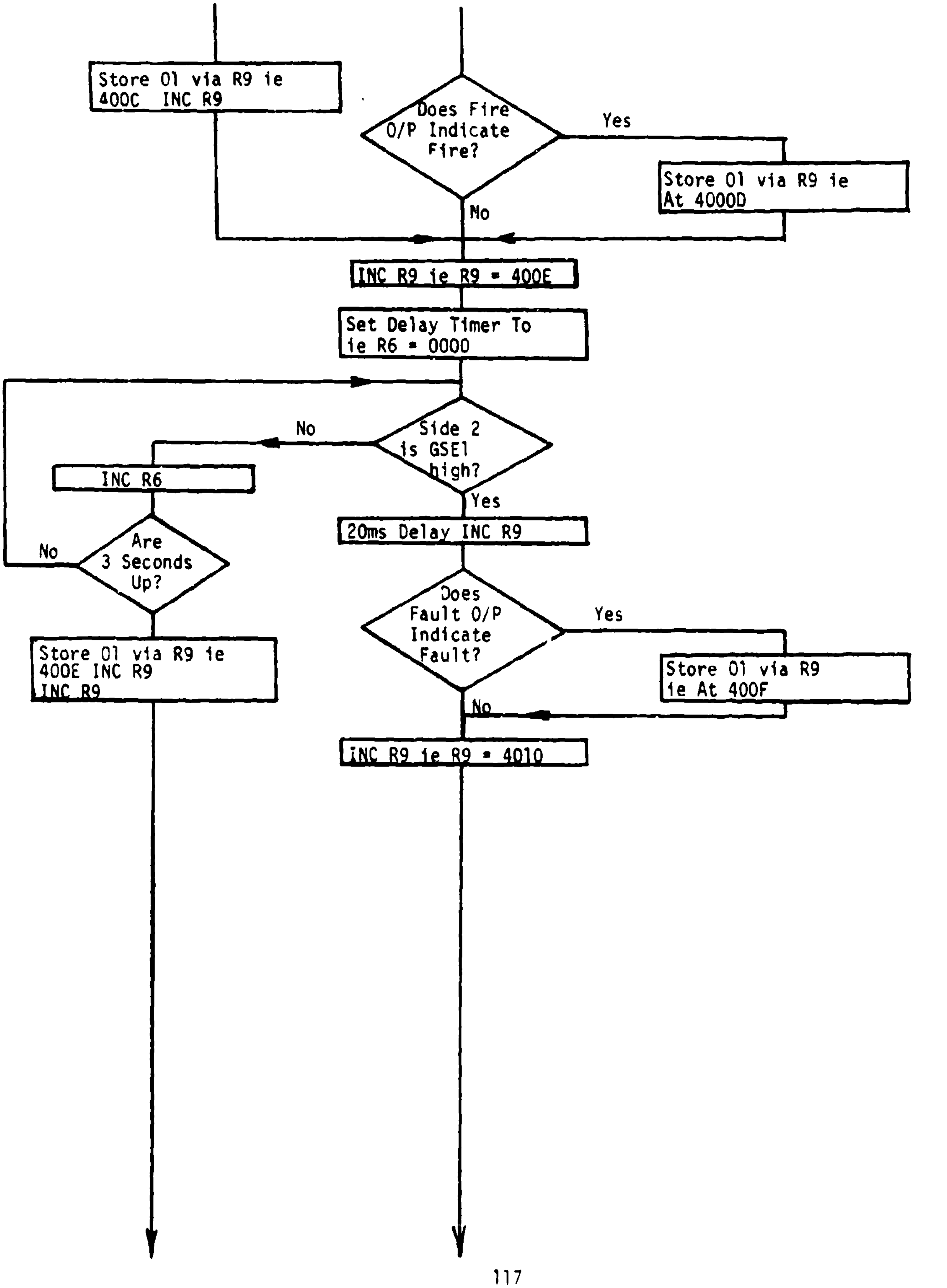

Is GSE1 Side 2 High?
No
Store 01 via R9 ie At 4004
Yes
INC R9 ie R9 = 4005
Switch Off 115V OF CCU
Reset RMRNA
Issue RMRNB
Give 4 Sec Delay
Apply Power to CCU
Give 3 Sec Delay
Read GSE Side 1& 2
Are GSE 1 Or 2 Side High?
No
Store 01 via R9 ie At 4005
Yes
INC R9 ie R9 = 4000
System A or B
B
A

APPENDIX A-6
SHEET 4 OF 13

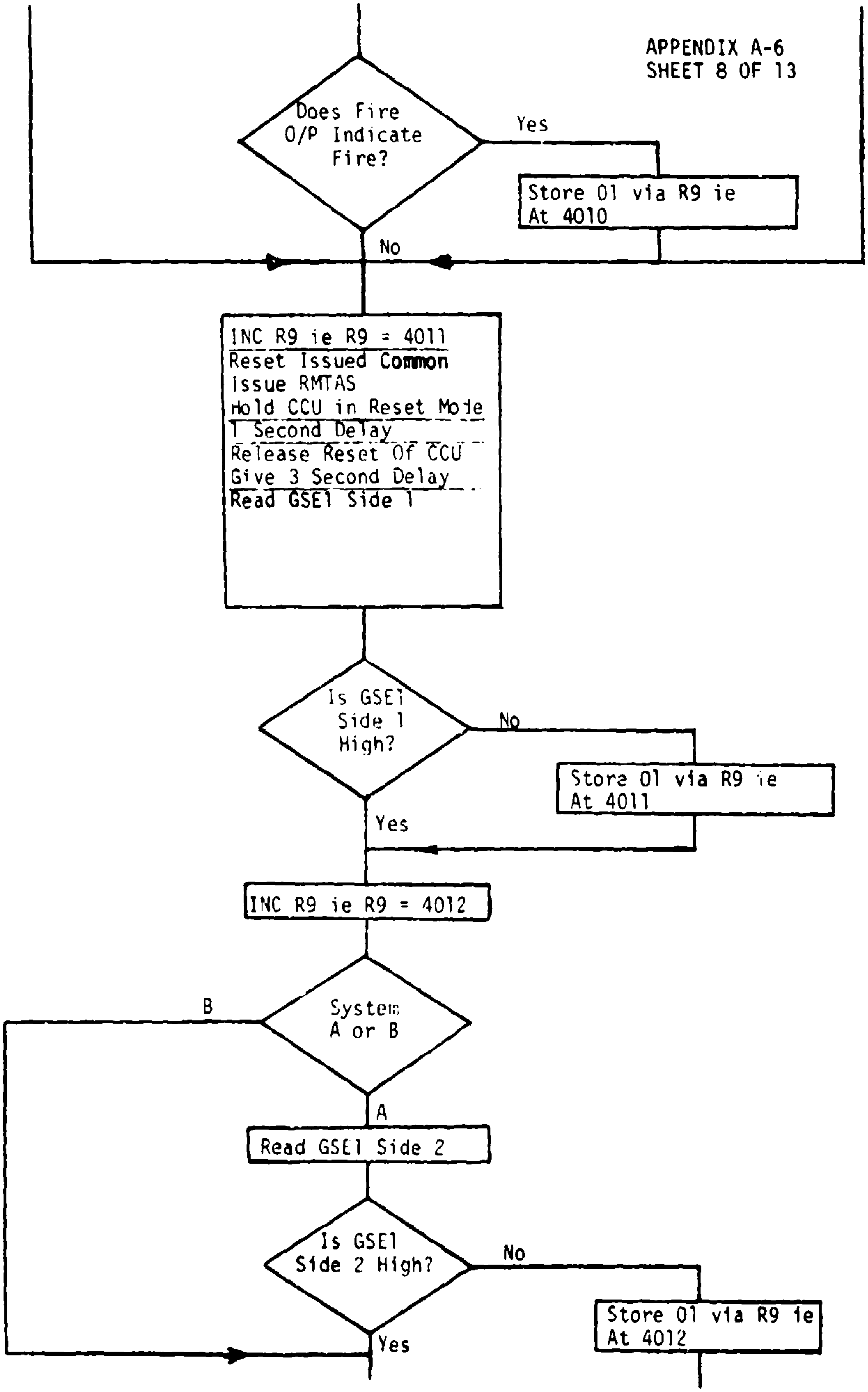


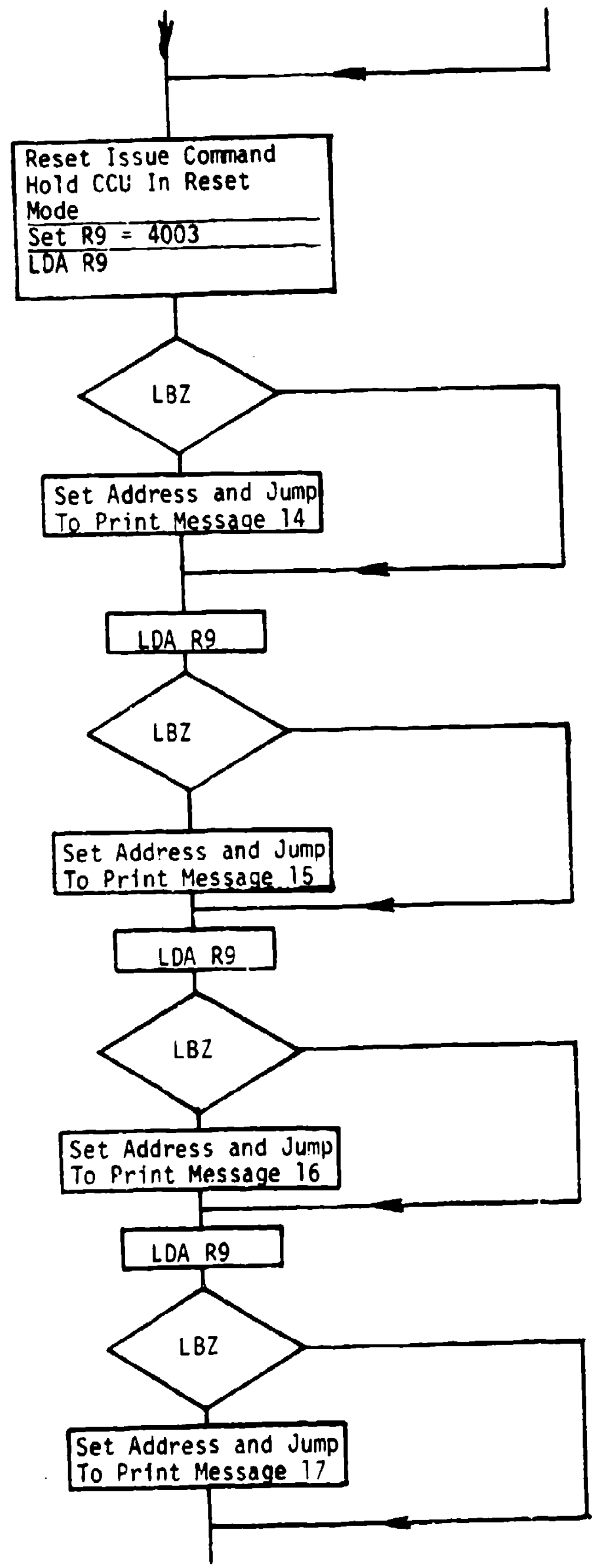

Hold CCU in Reset Mode Put CCU in GSE Mode
Set Address And Print Message 61 Set R9 = 4010
System A or B
B
A
Issue Command To Do Common Logic Release Reset Of CCU
Set Delay Timer To Zero ie R6 = 0000
Side 1 Is GSE 2 High?
No
INC R6
Yes
Give 20ms Delay INC R9
No
Are 3 Seconds Up?
Does Fire O/P Indicate Fire?
Yes
Yes
Store 01 via R9 ie 4007 INC R9
Store 01 via R9 ie At 4008
No
INC R9 ie R9 = 4009
Set Timer To Zero ie R6 = 0000

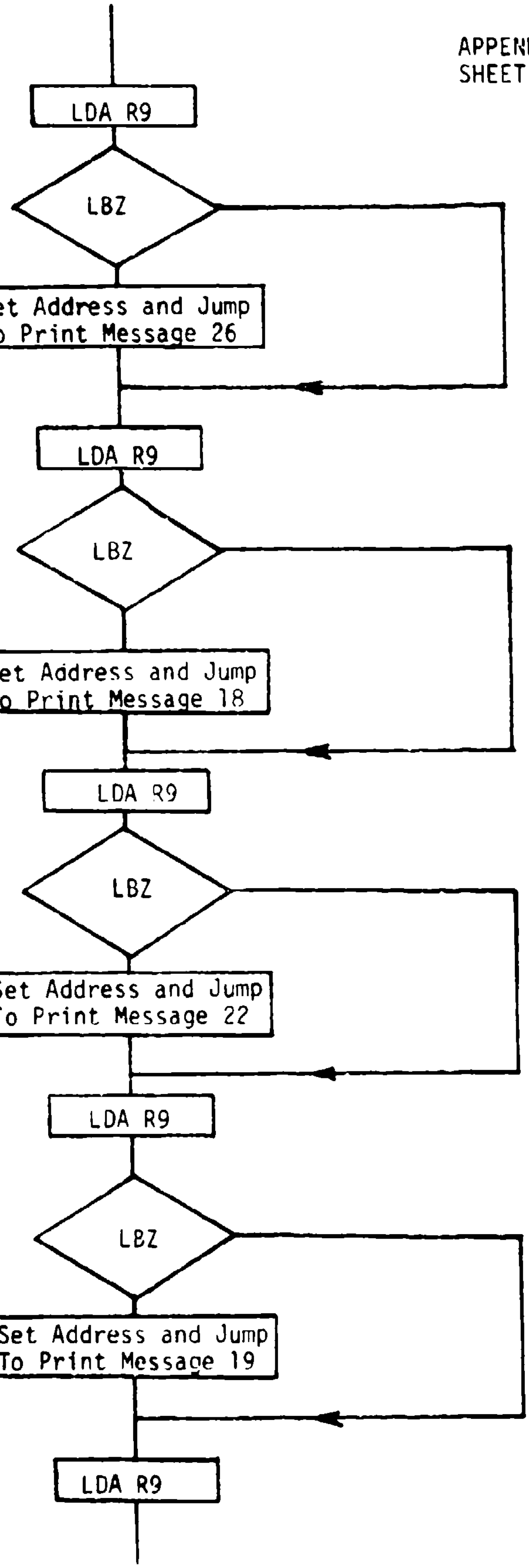

Side 1
Is GSE1 High?
No
Yes
INC R6
Give 20ms Delay INC R9
Are 3 Seconds Up?
No
Yes
Does Fault O/P Indicate Fault?
Yes
No
Store 01 via R9 ie 4009 INC R9 INC R9
Store 01 via R9 ie At 400A
INC R9 ie R1 = 400B
Does Fire O/P Indicate Fire?
Yes
No
Store 01 via R9 ie at 400B
INC R9 ie R1 = 400C
Set Delay Timer To Zero ie R6 = 000C
Side 2
is GSE2 High?
No
Yes
INC R6
20ms Delay INC R9
Are 3 Seconds Up?
No
Yes



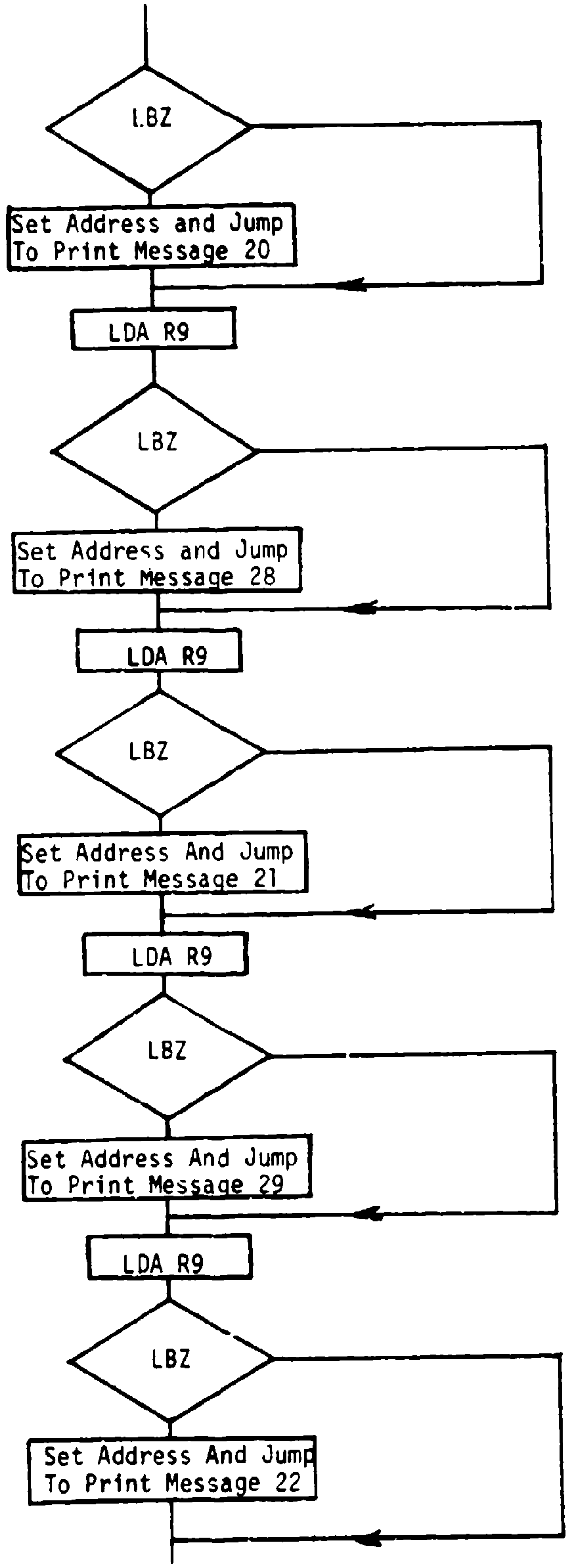
Store 01 via R9 ie
400C INC R9
Does Fire
O/P Indicate
Fire?
Yes
Store 01 via R9 ie
At 4000D
No
INC R9 ie R9 = 400E
Set Delay Timer To
ie R6 = 0000
No
Side 2
is GSE1
high?
INC R6
Yes
20ms Delay INC R9
No
Are
3 Seconds
Up?
Does
Fault O/P
Indicate
Fault?
Yes
Store 01 via R9 ie
400E INC R9
INC R9
Store 01 via R9
ie At 400F
No
INC R9 ie R9 = 4010

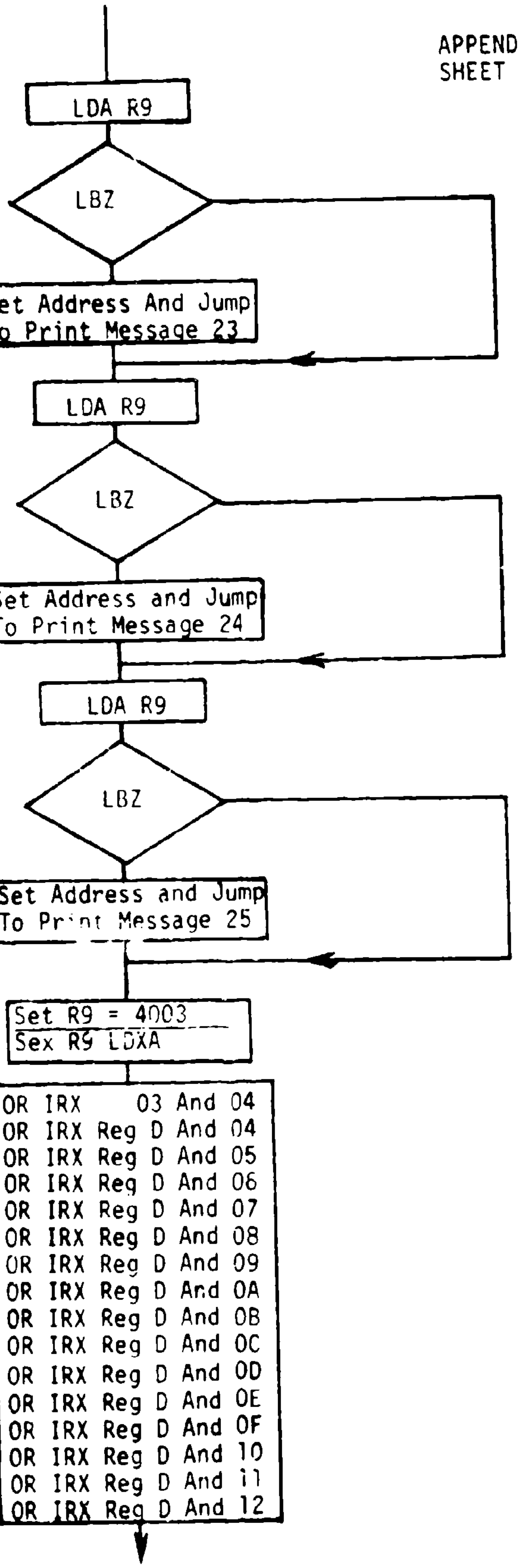

Does Fire O/P Indicate Fire?
Yes
Store 01 via R9 ie At 4010
No
INC R9 ie R9 = 4011
Reset Issued Common
Issue RMTAS
Hold CCU in Reset Mode
1 Second Delay
Release Reset Of CCU
Give 3 Second Delay
Read GSE1 Side 1
Is GSE1 Side 1 High?
No
Store 01 via R9 ie At 4011
Yes
INC R9 ie R9 = 4012
System A or B
B
A
Read GSE1 Side 2
Is GSE1 Side 2 High?
No
Store 01 via R9 ie At 4012
Yes

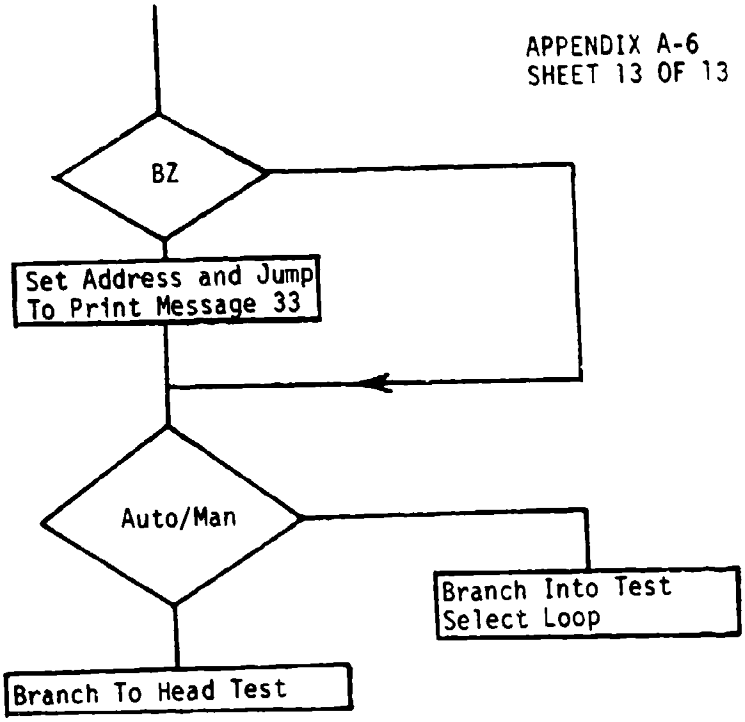

Reset Issue Command
Hold CCU In Reset
Mode
Set R9 = 4003
LDA R9
LBZ
Set Address and Jump
To Print Message 14
LDA R9
LBZ
Set Address and Jump
To Print Message 15
LDA R9
LBZ
Set Address and Jump
To Print Message 16
LDA R9
LBZ
Set Address and Jump
To Print Message 17


LDA R9
LBZ
Set Address and Jump To Print Message 26
LDA R9
LBZ
Set Address and Jump To Print Message 18
LDA R9
LBZ
Set Address and Jump To Print Message 22
LDA R9
LBZ
Set Address and Jump To Print Message 19
LDA R9

APPENDIX A-6
SHEET 11 OF 13




LDA R9
LBZ
Set Address And Jump To Print Message 23
LDA R9
LBZ
Set Address and Jump To Print Message 24
LDA R9
LBZ
Set Address and Jump To Print Message 25
Set R9 = 4003
Sex R9 LDXA
OR IRX 03 And 04
OR IRX Reg D And 04
OR IRX Reg D And 05
OR IRX Reg D And 06
OR IRX Reg D And 07
OR IRX Reg D And 08
OR IRX Reg D And 09
OR IRX Reg D And 0A
OR IRX Reg D And 0B
OR IRX Reg D And 0C
OR IRX Reg D And 0D
OR IRX Reg D And 0E
OR IRX Reg D And 0F
OR IRX Reg D And 10
OR IRX Reg D And 11
OR IRX Reg D And 12


BZ
Set Address and Jump To Print Message 33
Auto/Man
Branch Into Test Select Loop
Branch To Head Test

APPENDIX A-7

SAMPLE ASSEMBLER LISTING FOR TESTS

APPENDIX A-7

SAMPLE ONLY

```
[illegible]
[illegible]
[illegible] E ITO1
[illegible] F ITO2
[illegible] HERE
[illegible] 1
02
[illegible] MAIN
[illegible] LOOP1
[illegible] NEXTE1
[illegible] LOOP2
[illegible] NEXTE2
[illegible] LOOP3
[illegible] OUTPUT
[illegible] HEADS
[illegible]
[illegible]
[illegible] TIME2
[illegible] SHIFT
[illegible] E ITO
[illegible] MAIN
[illegible]
08A1 1
02
[illegible] TEST1
[illegible] NEXT1
08C1 1
02
[illegible] TEST2
[illegible] NEXT2
[illegible] 1
02
[illegible] TEST3
[illegible] NEXT3
[illegible] EXITX
[illegible] RET
0914 PC1
0919 PC2
091E PC3
0923 PC4
0928 PC5
092D PC6
0932 PC7
[illegible] PC8
[illegible] SID2
094E TRANS
0000

[illegible]
IM
0000 1
0000 1
0000 71201
0002 E01
[illegible]
0005 [illegible]
0007 [illegible]
[illegible] 0010
[illegible]
0010 [illegible]
0014 FEF7A01
0017 [illegible]
[illegible]
[illegible]
[illegible] E21
[illegible]
[illegible]

0001          ..GD/[illegible] OPBS AUTOMATIC TEST ROUTINE
0002 ORG0000
0003 DIS [illegible]             ..DIS INT
0004 SEX R0
0005 [illegible]                 ..APPLY POWER TO CCU
0006 [illegible]
0007 [illegible]
0008 [illegible] ,0000 10
0009 [illegible] LDI003 PHI R4 PHI R5    ..POINT R4 TO CALL RTN
0010 LDI040 PHI R2 PLO R2
0011 LDI0?7 PLO R4
0012 LDI0FA PLO R5          ..POINT R5 TO RETURN RTN
0013 LDI002 PHI R3          ..GET ADDRESS AND JUMP TO
0014 LDI024 PLO R3          ..PRINT MESS 1
0015 SEP R3
0016 SEX R2
0017 INP 4               ..TEST POSITION OF GSE
0018 ANI[illegible]      ..IN OUT SWITCH
0019 BNZ [illegible]     ..BRCH IF GSE MODE
0020 LDI002 PHI R3       ..GET ADDRESS AND JUMP
0021 LDI0[illegible] PLO R3   ..TO PRINT MESS 34
0022 SEP R3 SEX R0
0023 OUT [illegible]     ..SELECT [illegible] LINE
0024      ..FIRE HEADS IN [illegible] WITH EMITTER TEST
[illegible]
```

SAMPLE ONLY

```
[illegible]
[illegible]
0043 [illegible]        [illegible] R0 OUT 3,[illegible]   ..FIRE [illegible] SIDE 2
004F [illegible]FA101   BACK2: SEX R2 INP 4 AM1010   ..READ GSE 2 SIDE 2
[illegible]             BZ BACK2
0049 [illegible]        SEX R0 OUT 3,#00   ..RESET HEAD SIDE 2
004A E2,FA001           BACK3: SEX R2 INP 4 AM1040   ..READ GSE 2 SIDE 1
004C 3A4A1              BNZ BACK3
004E E[illegible]39F1   FHEAD1: SEX R0 OUT 3,#0F   ..FIRE GSE HEADS SIDE 1
0051 E2[illegible]FA001 BACK4: SEX R2 INP 4 AM1040   ..READ GSE 2 SIDE 1
0055 [illegible]2511    BZ BACK4
0057 E[illegible]3001   SEX R0 OUT 3,#00   ..RESET HEADS SIDE 1
005A [illegible]11      BR [illegible]
005C E[illegible]FA001  FIRE: SEX R2 INP 5 AM1080   ..IF EMITTER LINE HIGH
0060 [illegible]311     BZ [illegible]   ..BRCH IF EMITTER LINE LOW
0062 E0[illegible]3F1   SEX R0 OUT 3,#0F   ..FIRE GSE HEADS
0065 [illegible]FF1     OUT [illegible]   ..BOTH SIDES
0067 E2[illegible]FA001 BACK5: SEX R2 INP 5 AM1080   ..IF EMITTER LOW
006B 3A671              BNZ BACK5   ..BRCH IF EMITTER HIGH
006D E0[illegible]3001  SEX R0 OUT 3,#00   ..RESET HEADS
0070 [illegible]100[illegible]   OUT [illegible]   ..BOTH SIDES
0072 30[illegible]11    BR [illegible]
0074 [illegible]FA401   BACK6: INP 4 AM1040   ..READ GSE 2 SIDE 1
0077 3A5C1              BNZ FIRE   ..BRCH IF GSE 2 SIDE 1 LOW
0079 304E1              BR FHEAD1   ..BRCH IF GSE 2 SIDE 1 HIGH
007B FA40B91            DRET1: LDI#40 PHI R9
007E FA00A91            LDI#00 PLO R9   ..R9=4000
0081 09FB011            LDN R9 XRI#01   ..TEST MEM CODE
0084 3A[illegible]1     BNZ JUMP   ..BRCH IF NO SIDE 2
0086 FA00591            LDI#00 STR R9   ..RESET MEMCODE TO 0
0089 A7A81              PLO R7 PLO R8
008B FA44B71            LDI#44 PHI R7   ..R7=4400
008E FA45B81            LDI#45 PHI R8   ..R8=4500
0091 07581              PORY1: LDN R7 STR R8   ..[illegible] MEM 4400
0093 17181              INC R7 INC R8   ..THROUGH 44FF [illegible]
0095 97FB451            GHI R7 XRI#45   ..4500 THROUGH 45FF
0098 3A911              BNZ PORY
009A E01                SEX R0
009B [illegible]2301    OUT [illegible]   ..[illegible] DATA SIDE 2 AND
009D 1                  [illegible]   ..RESET PREV COMM
009D 67911              OUT [illegible]   ..RESET CCU & START TIMER
009F 1
009F FA00B6A61          LDI#00 PHI R6 PLO R6   ..R6=0000
00A[illegible] 16961    DIL1: INC R6 GHI R6
00A5 FB[illegible]01    XRI#[illegible]   ..1 SEC DEL
00A7 3AA31              BNZ DIL1
00A9 67901              OUT 7,#90   ..RELEASE TIMER & CCU
00AB 1
00AB C000001            ..[illegible]
00AE 1                  ..JUMP TO UTILITY. AT THIS TIME GSE
00AE 1                  ..WAITS TO RECIEVE DATA FROM CCU. IT
00AE 1                  ..FINALLY DOES & TIMER STARTS PGM
00AE 1                  ..FROM 0000
00AE F03CA31            JUMP1: [illegible]
00B1 F802B3031          LDI#02 PHI R3 SEP R3   ..TO PRINT MESS 59
00B5 FA40B2A21          LDI#40 PHI R2 PLO R2   ..R2=4040
00B9 E0[illegible]      SEX R0 OUT 5,#00   ..SET FF3 = 0
00BC [illegible]        OUT [illegible]   ..HOLD CCU IN RESET MODE
00BE E21                SEX R2
00BF 6B1                INP 3   ..TEST FOR AUTO/MAN
00C0 FA041              ANI#04
00C2 CA01001            LBNZ RETURN   ..BRCH TO MAN LOOP
00C5 C001BE1            LBR CCUT   ..BRCH TO CONTROL UNIT TESTS
00C8 3FE31              GSEM1: BN4 SKIP
00CA E01                SEX R0
00CB [illegible]        OUT [illegible]   ..ISSUE COMM TO RO
00CD [illegible]        OUT [illegible]   ..IDLE ROUTINE & RELEASE [illegible] RESET LINE
00CF F800B6A61          LDI#00 PHI R6 PLO R6
00D[illegible] 16961    DIL2: INC R6 GHI R6
00D5 FBFFC4C4C41        XRI#FF NOP NOP NOP   ..1 SEC DEL
00DA 3AD31              BNZ DIL2
00DC E26C1              SEX R2 INP 4   ..READ GSE 1&2 SIDE1
00DE FAC01              ANI#C0
00E0 CA01701            LBNZ RESPONSE
00E3 F840B91            [illegible]: LDI#40 PHI R9
00E6 FA00A91            LDI#00 PLO R9   ..R9=4000
00E9 F830591            [illegible]: LDI#30 STR R9
00EC 89FB401            GLO R9 XRI#40   ..LOAD RAM 4000 - 4040
[illegible]             INC R9
[illegible]             BNZ [illegible]
[illegible]             LDI#00 PLO R9   ..RESET R9=4000
[illegible]
```

SAMPLE ONLY

```
[illegible]                 0109 OUT 7      ..MODE [illegible] FT MODE
[illegible]                 0110 [illegible] PHI R6 PLO R6    ..R6=0000
[illegible]                 0111 DILA1 INC R6 GHI R6
[illegible]                 0112 [illegible]      ..1 SEC DEL
[illegible]                 0113 LBNZ DIL4
[illegible]                 0114 OUT 2      ..DO LINE [illegible]
[illegible]                 0115 OUT 7      ..RELEASE [illegible] RESET LINE
[illegible]                 0116 [illegible] PHI R6 PLO R6    ..R6=0000
[illegible]                 0117 DIL5 INC R6 GHI R6
[illegible]                 0118 [illegible] NOP NOP NOP    ..1 SEC DEL
[illegible]                 0119 [illegible] DIL5
0114 [illegible]            0120 SEX R2 INP 4    ..READ GSE 1&2 SIDE1
0116 FA[illegible]01        0121 ANI #C0
0118 3A[illegible]          0122 BNZ FAIL1      ..BNCH IF SIDE 1 FAIL
011A 6C                     0123 INP 4          ..TEST A OR B
011B FA[illegible]          0124 ANI #08
011D [illegible]            0125 BZ PASS1       ..BNCH IF B
011F F844A3                 0126 SYSTA1 LDI#44 PLO R3        ..SET ADDRESS & JUMP TO
0122 D3                     0127 SEP R3                      ..PRINT MESS 2
0123 F855A3                 0128 LDI#55 PLO R3      ..SET ADDRESS & JUMP TO
0126 D3                     0129 SEP R3         ..PRINT MESS 3
0127 6C                     0130 INP 4        ..READ GSE 1&2 SIDE2
0128 FA30                   0131 ANI #30
012A 3A[illegible]          0132 BNZ FAIL2       ..BNCH IF SIDE 2 FAIL
012C 6C                     0133 INP 4        ..TEST SIDE 1 PASS-FAIL
012D FAC0                   0134 ANI #C0
012F 32[illegible]          0135 BZ NPHASE     ..BNCH IF SIDE1 PASS
0131 F85DA3                 0136 LDI#5D PLO R3    ..SET ADDRESS & JUMP TO
0134 D3                     0137 SEP R3           ..PRINT MESS 11
0135 F865A3                 0138 LDI#65 PLO R3  ..SET ADDRESS AND JUMP TO
0139 [illegible]            0139
013A D3                     0140 SEP R3         ..PRINT MESS 12
013B F86DA3                 0141 LDI#6D PLO R3    ..SET ADDRESS & JUMP TO
013E D3                     0142 SEP R3         ..PRINT MESS 7
0130 30[illegible]          0143 BR NPHASE
013F 6C                     0144 FAIL1: INP 4     ..TEST A OR B
0140 FA08                   0145 ANI #08
0142 3A[illegible]          0146 BNZ SYSTA    ..BNCH IF A
0144 F844A3                 0147 LDI#44 PLO R3    ..SET ADDRESS & JUMP TO
0147 D3                     0148 SEP R3            ..PRINT MESS 2
0148 F875A3                 0149 LDI#75 PLO R3  ..SET ADDRESS & JUMP TO
014B D3                     0150 SEP R3       ..PRINT MESS 4
014C F86DA3                 0151 LDI#6D PLO R3    ..SET ADDRESS & JUMP TO
014F D3                     0152 SEP R3        ..PRINT MESS 7
0150 F87DA3                 0153 LDI#7D PLO R3    ..SET ADDRESS & JUMP TO
0153 D3                     0154 SEP R3        ..PRINT MESS 8
0154 30[illegible]          0155 HERE1: BR HERE1    ..LOOP TO ITSELF
0156 F844A3                 0156 PASS1: LDI#44 PLO R3    ..SET ADDRESS & JUMP TO
0159 D3                     0157 SEP R3        ..PRINT MESS 2
015A F875A3                 0158 LDI#75 PLO R3      ..SET ADDRESS & JUMP TO
015D D3                     0159 SEP R3        ..PRINT MESS 4
015E 30[illegible]          0160 BR NPHASE
0160 6C                     0161 FAIL2: INP 4     ..TEST SIDE 1
0161 FAC0                   0162 ANI #C0
016[illegible]              0163 BNZ FAIL3     ..BNCH IF SIDE 1 FAIL
016[illegible] F8[illegible]A3   0164 LDI#[illegible] PLO R3     ..SET ADDRESS & JUMP
016[illegible] D3           0165 SEP R3              ..TO PRINT MESS 10
016[illegible]              0166 LDI#[illegible] PLO R3    ..SET ADDRESS & JUMP
016[illegible] D3           0167 SEP R3         ..TO PRINT MESS 13
016D F86DA3                 0168 LDI#6D PLO R3    ..SET ADDRESS & JUMP
0170 D3                     0169 SEP R3        ..TO PRINT MESS 7
017[illegible]              0170 BR NPHASE
017[illegible] F8[illegible]A3   0171 FAIL3: LDI#[illegible] PLO R3    ..SET ADDRESS & JUMP
017[illegible] D3           0172 SEP R3        ..TO PRINT MESS [illegible]
017[illegible] F86DA3       0173 LDI#6D PLO R3    ..SET ADDRESS & JUMP TO
017[illegible] D3           0174 SEP R3        ..PRINT MESS [illegible]
017B 30[illegible]          0175 HERE3: BR HERE3     ..LOOP TO ITSELF
017D E[illegible]           0176 [illegible]
[illegible]                 0177 [illegible] PHI R2 PLO R2    ..R2=4040
[illegible]                 0178 SEX R2 INP 3    ..READ I-P 3
[illegible]                 0179 ANI #04
[illegible]                 0180 BZ AUTO      ..BNCH IF AUTO
[illegible]                 0181 RETURN: LDI#[illegible] PLO R3     ..SET ADDRESS & JUMP
[illegible]                 0182 [illegible] PHI R3
[illegible]                 0183 SEP R3              ..TO PRINT MESS [illegible]
[illegible]                 0184 [illegible] LDI#40 PHI R2 PLO R2 SEX R2    R2=4040
[illegible]                 0185 INP 5      ..READ I-P 5
[illegible]                 0186 ANI #40
[illegible]                 0187 [illegible] DATA     ..BNCH TO DATA PGM
[illegible]                 [illegible]
[illegible]                 [illegible]     ..BNCH TO [illegible] UNIT TEST
[illegible]                 [illegible]
[illegible]                 [illegible]     ..BNCH TO [illegible] HEAD TEST
[illegible]                 [illegible]
[illegible]                 [illegible]     ..BNCH TO PARAMETRIC TEST
[illegible]                 [illegible]
[illegible]                 [illegible]     ..BNCH TO HEAD [illegible]
[illegible]                 [illegible]
[illegible]                 [illegible]     ..BNCH TO DATA ANALYST
```

SAMPLE ONLY

```
[illegible]               [illegible]
01A4 [illegible]          BNZ MEMO7         ..BRCH TO 10 SEC MEMO TEST
01A6 [illegible]          [illegible]
01A9 [illegible]          BNZ PARA          ..BRCH TO PARAMETRIC TEST
01AB [illegible]          [illegible]
01AE [illegible]          BNZ MEM IM        ..BRCH TO MEMO SIM
01B0 [illegible]          IMP [illegible]
01B3 [illegible]          BNZ ANAL          ..BRCH TO DATA ANALYSIS
01B5 [illegible]          [illegible]
01B7 [illegible]          [illegible] PLO R3   ..SET ADDRESS & JUMP
01BA D3                   SEP R3            ..TO PRINT MESS 57
01BB [illegible]          [illegible]       ..BRCH TO RETRIEVE DATA
01BE [illegible]          [illegible]
01C1 C00[illegible]       MEADTI [illegible]
01C4 [illegible]          PARAI [illegible] 0836
01C7 [illegible]          MEMSIM: [illegible] .3F7
01CA [illegible]          ANAL [illegible] C012C0
01CD E0                   RETAAL: SEX R0
01CE [illegible]          OUT [illegible]   ..GIVE RHATEST COMA
01D0 67101                OUT 7,#10         ..HOLD CCU IN RESET HOLD
01D2
01D2 F800B6A6             LDI#00 PHI R6 PLO R6   ..R6=0000
01D6 [illegible]          DIL6: INC R6 GHI R6
01D8
01D8 FBFF                 [illegible]       ..1 SEC DEL
01DA 3AD6                 BNZ DIL6
01DC 67141                OUT 7,#14         ..RELEASE CCU RESET LINE
01DE F800B6A6             LDI#00 PHI R6 PLO R6   ..R6=0000
01E2 16[illegible]        DIL7: INC R6 GHI R6
01E4 FBFFC4C4C4C4         [illegible] NOP NOP NOP NOP   ..3 SEC DEL
01EA 3AE2                 BNZ DIL7
01EC E0                   SEX R0
01ED 67001                OUT [illegible]   ..[illegible] TO CCU
01EF F8C0A3               LDI#C0 PLO R3     ..SET ADDRESS & JUMP
01F2 D3                   SEP R3            ..TO PRINT MESS 44
01F3                                        ..READ CCU (RETRIEVE DATA)
01F3
01F3 F844A3               DATA: LDI#44 PLO R3   ..SET ADDRESS & JUMP
01F6 D3                   SEP R3            ..TO PRINT MESS 2
01F7 F8B5A3               LDI#B5 PLO R3     ..SET ADDRESS & JUMP TO
01FA D3                   SEP R3            ..PRINT MESS 5[illegible]
01FB E0                   SEX R0
01FC 65011                OUT 5,#01         ..SET EF3 = 1
01FE F840B2A2             LDI#40 PHI R2 PLO R2   ..R2=4040
0202 E26C                 SEX R2 INP 4      ..TEST A OR B
0204 FA0[illegible]       ANI#0[illegible]
0206 [illegible]          [illegible] MEMO  ..BRCH IF A
0209 [illegible]          RETI: [illegible] R0
020B [illegible]          OUT [illegible]   ..[illegible] DATA SIDE 1
020D 67111                OUT 7,#11         ..START INT TIM
020F F800B6A6             LDI#00 PHI R6 PLO R6   ..R6=0000
0213 16[illegible]        DIL8: INC R6 GHI R6
0215 FB80                 XRI#80            ..1 SEC DEL
0217 3A13                 BNZ DIL8
0219 67141                OUT 7,#14         ..RESET INT TIM & RELEASE
021B                                        ..RESET OF CCU
021B C00000               LBR#0000
021E                      ..JUMP TO UTILITY[illegible] THIS TIME USE WAITS TO
021E                      ..RECIEVE DATA FROM [illegible] IT FINALLY DOES
021E                      ..[illegible] UTILITY IS INTERRUPTED BY TIMER
021E F80159               MEMO: LDI#01 STR R9   ..STORE 01 AT 4000
0221 3009                 BR RETI
0223
0223                                        ..PRINT MESS ROUTINES
0223
[illegible]                                 [illegible] GRAVINER IFDS AUTO TEST ROUTINE (1)
[illegible] [illegible]   E[illegible] [illegible] R0 SEP R4
[illegible] [illegible]   [illegible] FE[illegible]
[illegible] 30[illegible] BR EXIT
[illegible]
[illegible]               [illegible] MODE [illegible]
[illegible]               EXIT[illegible] [illegible] R0 SEP R4
[illegible] [illegible]   [illegible] EE[illegible]
[illegible]               BR EXIT
[illegible]
[illegible]               [illegible] ANAL MODE [illegible]
[illegible]               [illegible] R0 SEP R4
[illegible]               [illegible] 0876
[illegible]               BR EXIT
[illegible]
[illegible]               [illegible] COMPLETE [illegible]
[illegible]               [illegible] SEP R4
[illegible]               [illegible] 08[illegible]
[illegible]
[illegible]               [illegible] CHANGE [illegible]
[illegible]               [illegible] SEP R4
[illegible]               [illegible] 0992
[illegible]
```

This message not used any more

DATA ANALYSIS

SAMPLE ONLY

```
0000 ;                     0001
0000 ;                     0002   ..*****DATA MAIN PROGRAM 1*****
0000 ;                     0003 ORG#1800
1800 F818B3;               0004 LDI#18 PHI R3
1803 F807A3;               0005 LDI#07 PLO R3
1806 D3;                   0006 SEP R3
1807 ;                     0007
1807 F81FB9B0;             0008 LDI#1F PHI R9 PHI R0
180B F866A0;               0009 LDI#66 PLO R0  ..FOR DELAY RTN
180E F840B2;               0010 LDI#40 PHI R2
1811 A2;                   0011 PLO R2
1812 D0;                   0012 SEP R0  ..FREE RAM&DO DELAY
1813 ;                     0013
1813 D483EE181A302E;0014 SEP R4,#83EE,A(*+4) BR HOP1
181A 53544152542044;0015 ,T'START DATA ANALYSIS',#8A
1821 41544120414E41;0015
1828 4C59534953 8A;   0015
182E 6CFA08;               0016 HOP1; INP 4 ANI#08
1831 3A46;                 0017 BNZ PASS  ..NOT=0 IS SYS A
1833 F844BB;               0018 LDI#44 PHI RB  ..SET FOR DATA
1836 F845BA;               0019 LDI#45 PHI RA  ..TRANSFER,MOVE 4400>4500 ETC
1839 F800AAAB;             0020 LDI#00 PLO RA PLO RB
183D EB;                   0021 SEX RB
183E 72;                   0022 MORE; LDXA  ..GET DATA
183F 5A1A8A;               0023 STR RA INC RA GLO RA
1842 FB00;                 0024 XRI#00
1844 3A3E;                 0025 BNZ MORE  ..UNTIL ALL DATA XFERED
1846 F8D1A9;               0026 PASS;  LDI#D1 PLO R9
1849 D9;                   0027 SEP R9  ..DO WIPE
184A 2BF831;               0028 DEC RB LDI#31  ..ASCII '1'
184D 5B;                   0029 STR RB  ..ATM409E
184E F845BB;               0030 LDI#45 PHI RB
1851 F801AB;               0031 PNT1; LDI#01 PLO RB  ..POINT AT FIRST DATA
1854 72;                   0032 LDXA  ..SAVED INDICATOR
1855 FBA5;                 0033 XRI#A5
1857 3A63;                 0034 BNZ LOC1
1859 72FBA5;               0035 LDXA XRI#A5  ..CHECK FOR GOOD STORE
185C 3A63;                 0036 BNZ LOC1
185E F0FBA5;               0037 LDX XRI#A5
1861 32CE;                 0038 BZ PNT3
1863 ;                     0039
1863 D0D4;                 0040 LOC1;SEP R0 SEP R4
1865 83EE186B3080;         0041 ,#83EE,A(*+4) BR HOP2
186B 44415441204E4F;0042 ,T'DATA NOT SAVED SIDE ',#A0
1872 54205341564544;0042
1879 2053494445 20A0;0042
1880 D483EE40ED;           0043 HOP2; SEP R4,#83EE40ED  ..FROM WRITE PAD
1885 D0D483EE188D30;0044 PNT2; SEP R0 SEP R4,#83EE,A(*+4) BR HOP3
188C A8;                   0044
188D 44415441204 14E;0045 ,T'DATA ANALYSIS TEST ABORT',#0A0A8A
1894 414C5953495320;0045
189B 54455354204142;0045
18A2 4F52540A0A8A;         0045
18A8 6BFA04;               0046 HOP3; INP 3 ANI#04  ..TEST FOR AUTO/MAN
18AE CA18CE;               0047 LBNZ MAN
```

```
18AE D0D483EE18B630;0048 SEP R0 SEP R4,#83EE,A(*+4) BR DIZY
18B5 C8;                0048
18B6 0E454E44204140;0049 ,#0E,T'END ALL TESTS',#0F0A0A0A0A
18BD 4C20544553545 3;0049
18C4 0F0A0A0A0A;C0      0049
18C9 3009;              0050 DIZY: BR DIZY
18CB C01F95;            0051 MAN:   ,#C01F95
18CE F830AB;            0052 PNT3: LDI#30 PLO RB
18D1 8BFB40;            0053 LOC2: GLO RB XRI#40
18D4 C218DE;            0054 LBZ LOC3  ..END MC30-C3F FOR ALL 0'S
18D7 72FB00;            0055 LDXA XRI#00
18DA 3AED;              0056 BNZ LOC4
18DC ;                  0057
18DC 30D1;              0058 BR LOC2
18DE F8A0AB;            0059 LOC3: LDI#A0 PLO RB    ..TEST MCA0-CAF ALL 0'S
18E1 8BFBB0;            0060 LOC5: GLO RB XRI#B0
18E4 C21913;            0061 LBZ LOC7
18E7 ;                  0062
18E7 72FB00;            0063 LDXA XRI#00
18EA C218E1;            0064 LBZ LOC5
18ED ;                  0065     ....RETURN FOR MORE BYTES
18ED D0D483EE18F6C0;0066 LOC4: SEP R0 SEP R4,#83EE,A(*+5) LBR HOP4
18F4 190B;              0066
18F6 434F5252555054;0067 ,T'CORRUPT MEMORY SIDE ',#A0
18FD 204D454D4F5259;0067
1904 205349444520A0;0067
190B D483EE40ED;        0068 HOP4:  SEP R4 ,#83EE40ED  ..FROM WRITE PAD
1910 C01885;            0069 LBR PNT2
1913 9BFB45;            0070 LOC7: GHI RB XRI#45
1916 CA1930;            0071 LBNZ PNT5  ..1ST OR 2ND PASS
1919 E2;                0072 SEX R2  ..POINT FREE RAM
191A 6CFA08;            0073 INP 4 ANI#08
191D C21930;            0074 LBZ PNT5  ..TEST SYS A OR B 0 =B
1920 EB;                0075 SEX RB
1921 F840BAF8EEAA;      0076 LDI#40 PHI RA LDI#EE PLO RA
1927 F8325A;            0077 LDI#32 STR RA  ..ASCII 2 AT WRITE PAD
192A F844BB;            0078 LDI#44 PHI RB
192D C01851;            0079 LBR PNT1
1930 F845BB;            0080 PNT5: LDI#45 PHI RB
1933 F800AB0B;          0081 LDI#00 PLO RB LDN RB
1937 F9DEFBFF;          0082 ORI#DE XRI#FF  ..IF BIT 5 OR0=0
193B 3A4D;              0083 BNZ PNT6  ..RESULT IS NON ZERO
193D E2;                0084 SEX R2
193E 6CFA08;            0085 INP 4 ANI#08
1941 327A;              0086 BZ PNT7
1943 ;                  0087
1943 F844BB0B;          0088 LDI#44 PHI RB LDN RB  ..GET SIDE 2 0C00 BYTE
1947 F9DEFBFF;          0089 ORI#DE XRI#FF
194B 327A;              0090 BZ PNT7
194D D0D4;              0091 PNT6: SEP R0 SEP R4
194F 83EE19553077;      0092 ,#83EE,A(*+4) BR PNT8
1955 ;                  0093
1955 0E434845434B20;0094 ,#0E,T'CHECK CWU-IF OK',#0F0A
195C 435755 2D494620;0094
1963 4F4B0F0A;          0094
```

```
1967 0E5245504C4143:0095 ,#0E,T'REPLACE CCU',#0F0A0A8A
196E 45204343550F0A:0095
1975 0A8A;           0095
1977 ;               0096
1977 C01885;         0097 PNT8: LBR PNT2
197A C01970;         0098 PNT7: ,#C01970   ——— 1980
197D ;               0099
197D ;               0100
197D ;               0101   ..*****DELAY ROUTINE*****
197D ;               0102   ..FOR DELAY BETWEEN PRINT OUTS
197D ;               0103   ..USES R0 AS PGM COUNTER
197D ;               0104   ..RETURNS TO R3 CONTROL
197D ;               0105   ..USES RE AS COUNTER
197D ;               0106 ORG#1F65
1F65 D3;             0107 OUTOF: SEP R3
1F66 ;               0108 .....ENTER HERE>>>>>>>>
1F66 F8FFBEAE;       0109 LDI#FF PHI RE PLO RE
1F6A 2E9E3A6A;       0110 PLUS: DEC RE GHI RE BNZ PLUS
1F6E 3065;           0111 BR OUTOF
1F70 ;               0112
1F70 ;               0113
1F70 ;               0114       ..*****FIRST ENTRY TO ALL DATA ANALYSIS**
1F70 ;               0115       ..*****IF PROGRAMME IS RUN IN ISOLATION**
1F70 ;               0116 ORG#1EF8   ——— 1CF0
1EF8 67;             0117 OUT 7
1EF9 10;             0118 ,#10    ..ASSUMES SET UP TO X=P=0
1EFA F883B4B5;       0119 LDI#83 PHI R4 PHI R5
1EFE F8F7A4;         0120 LDI#F7 PLO R4
1F01 F8FAA5;         0121 LDI#FA PLO R5
1F04 C01800;         0122 ,#C01800
1F07 ;               0123 END
0000

? F,H,L,U=
```

APPENDIX A-8

SENSOR TEST FLOW DIAGRAM

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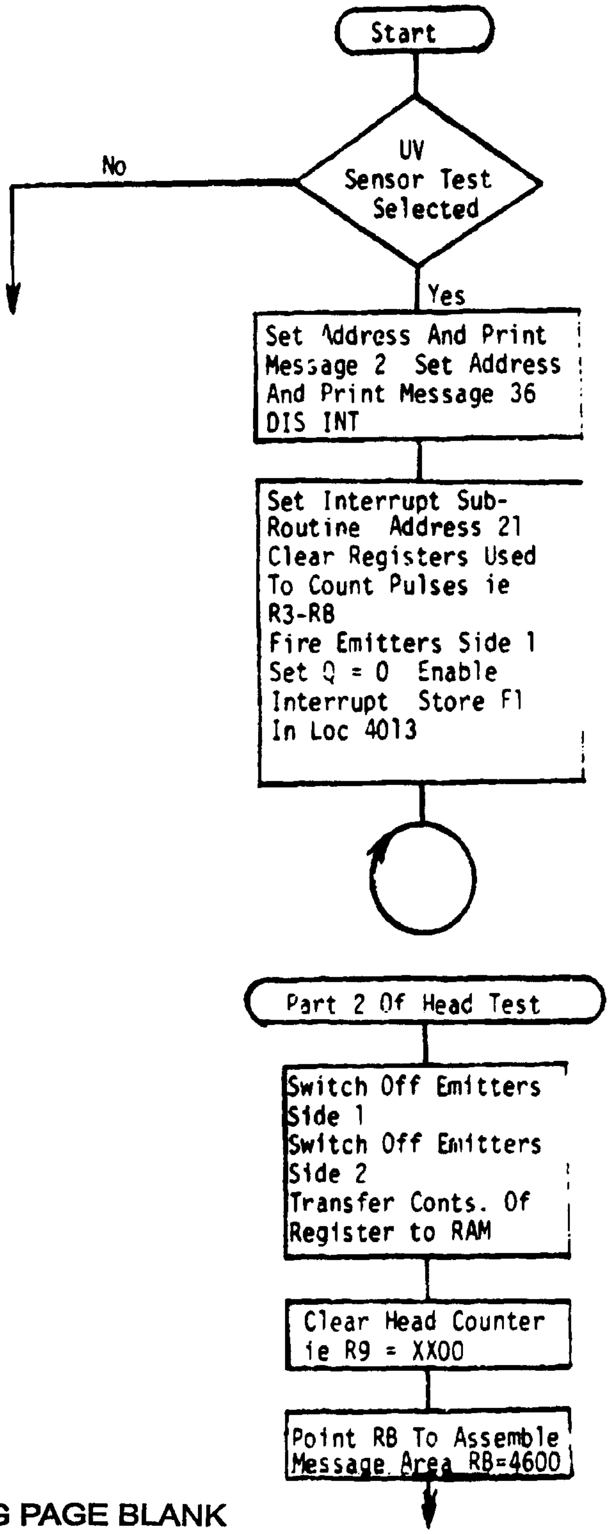
APPENDIX A-8
SHEET 1 OF 3
(SENSOR TEST)



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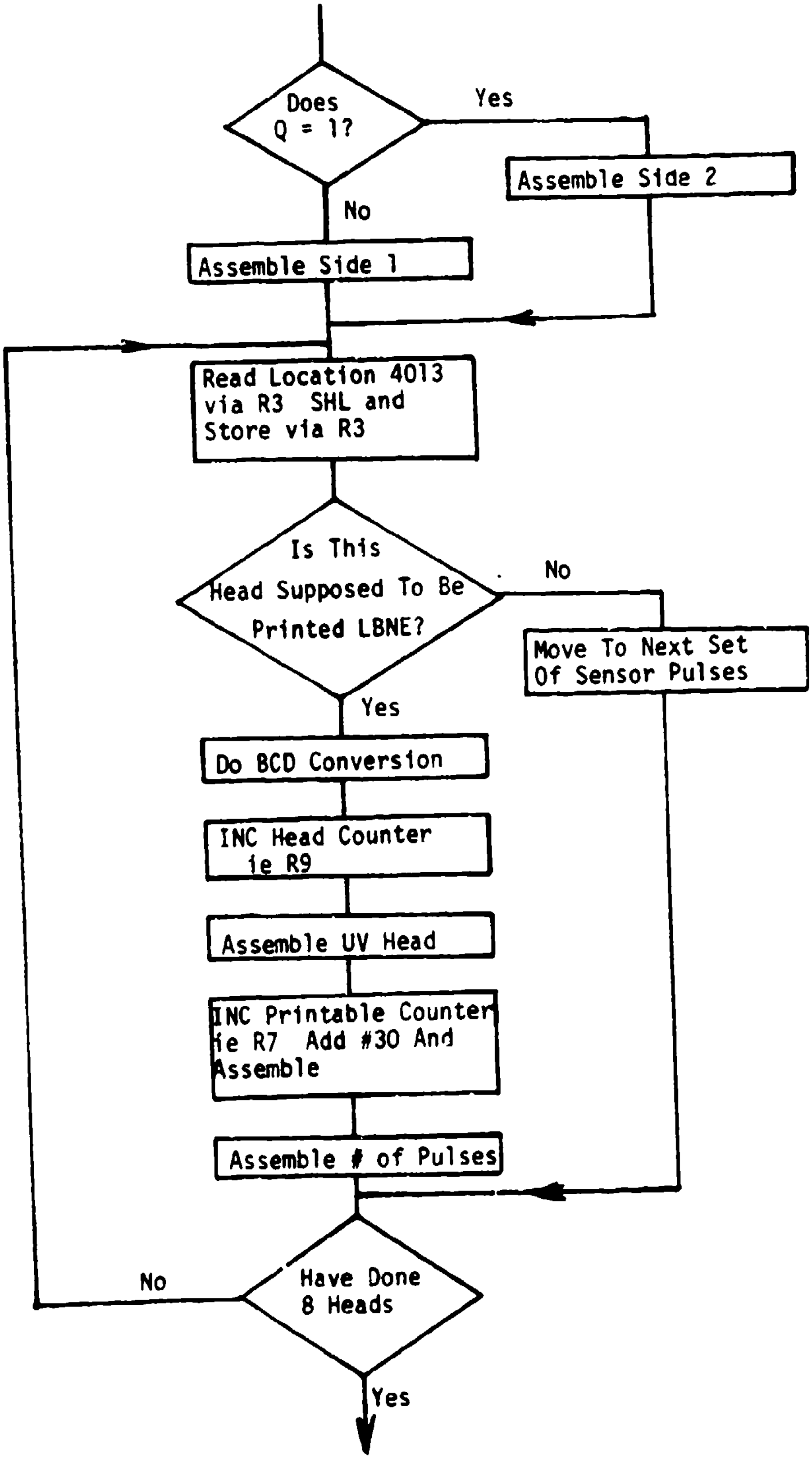
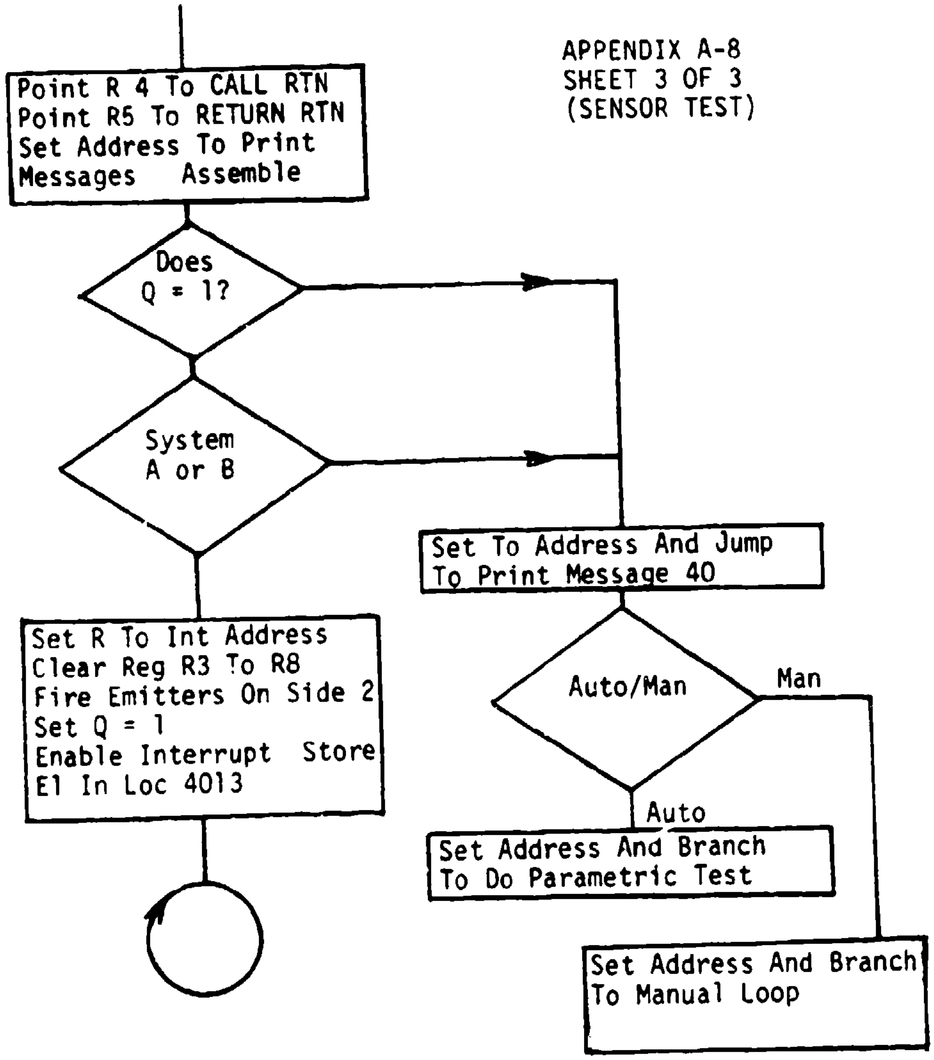
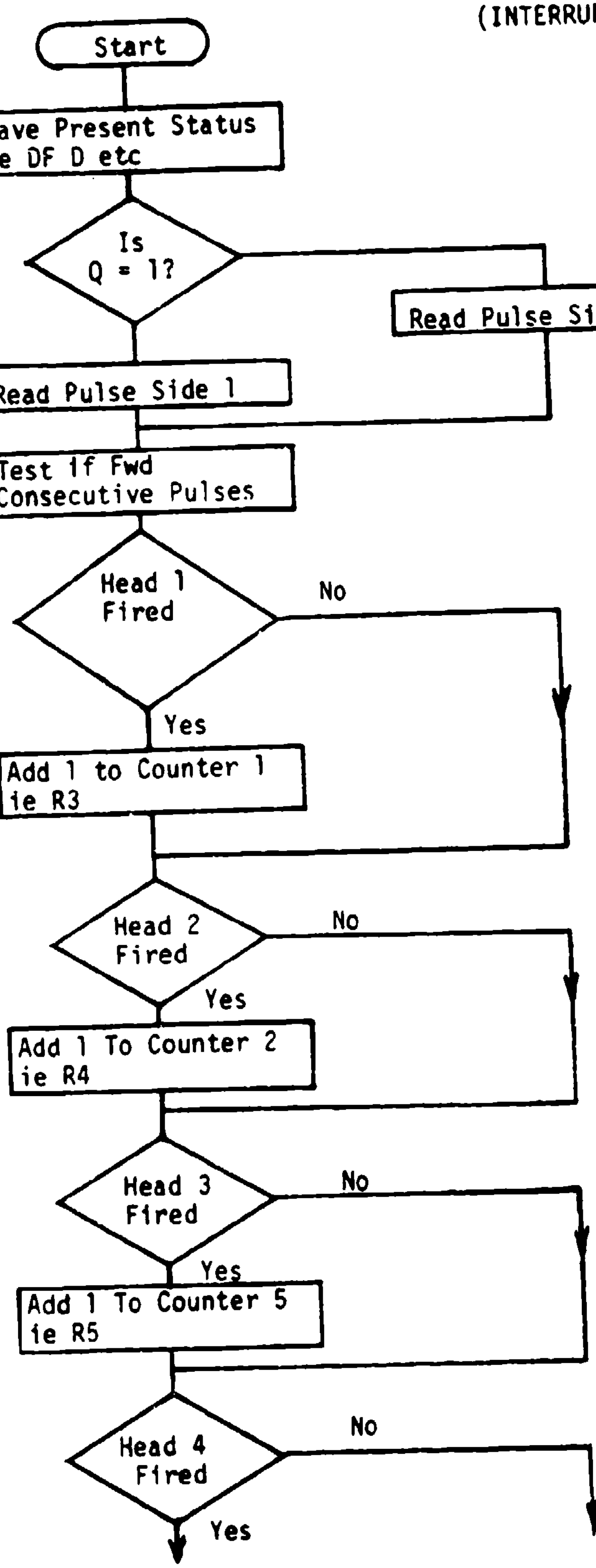
APPENDIX A-8
SHEET 2 OF 3
(SENSOR TEST)



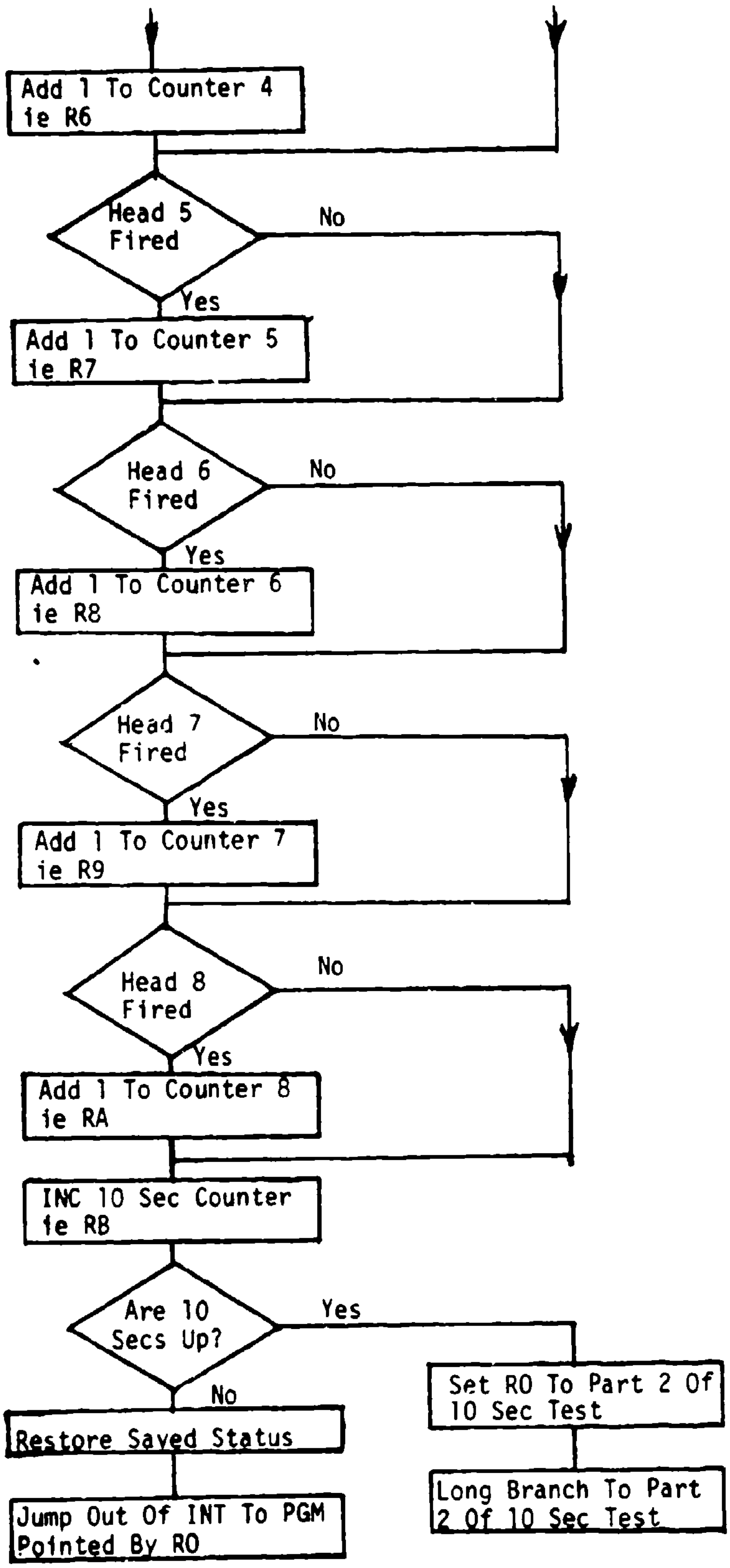
APPENDIX A-8
SHEET 3 OF 3
(SENSOR TEST)



APPENDIX A-8
SHEET 1 OF 2
(INTERRUPT SUBRTN)



APPENDIX A-8
SHEET 2 OF 2
(INTERRUPT SUBRTN)

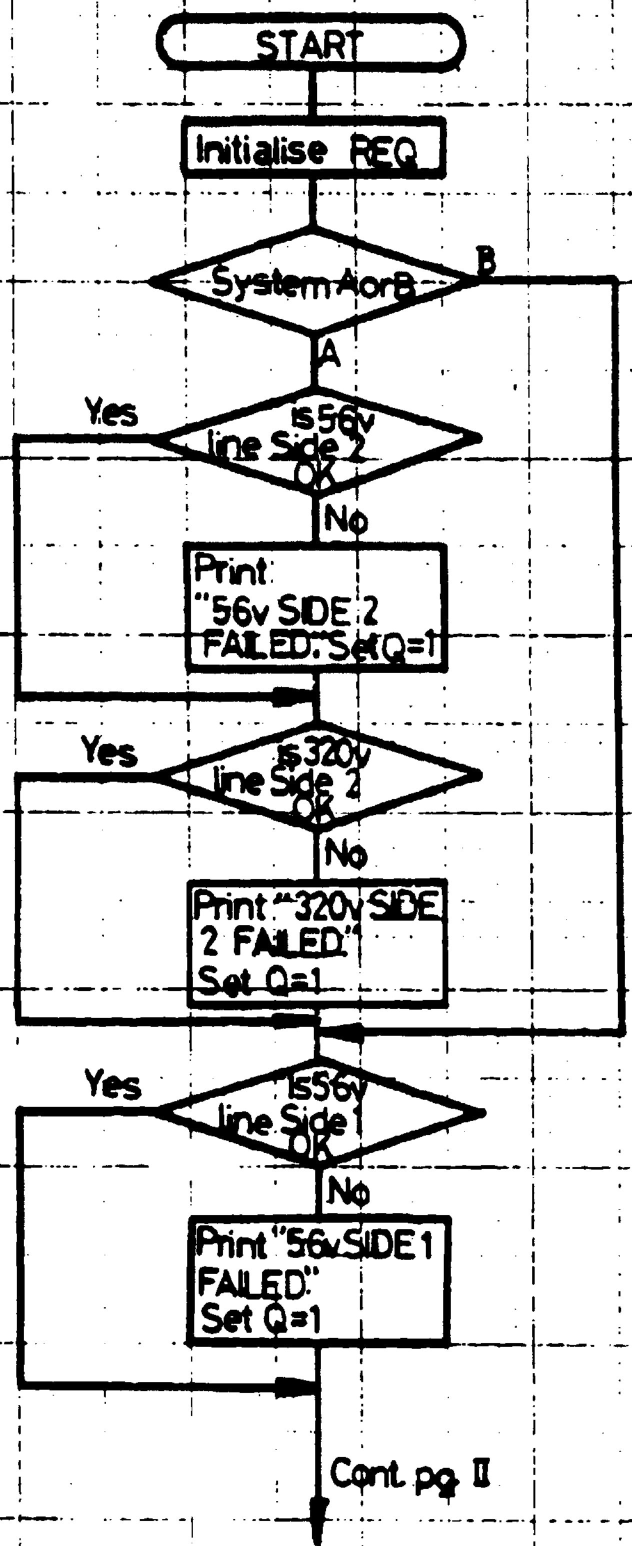


APPENDIX A-9

PARAMETRIC TEST FLOW DIAGRAM

APPENDIX A-9

PARAMETRIC TEST



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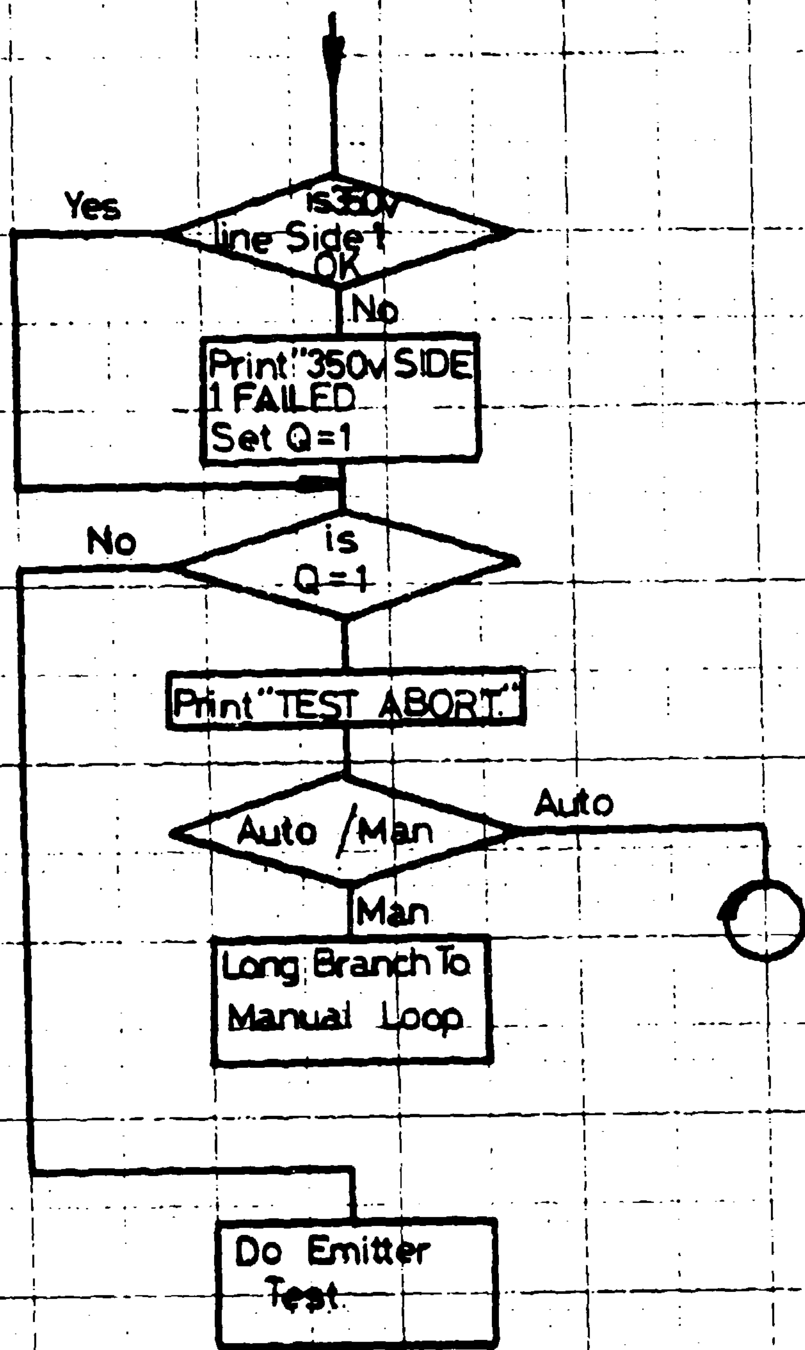
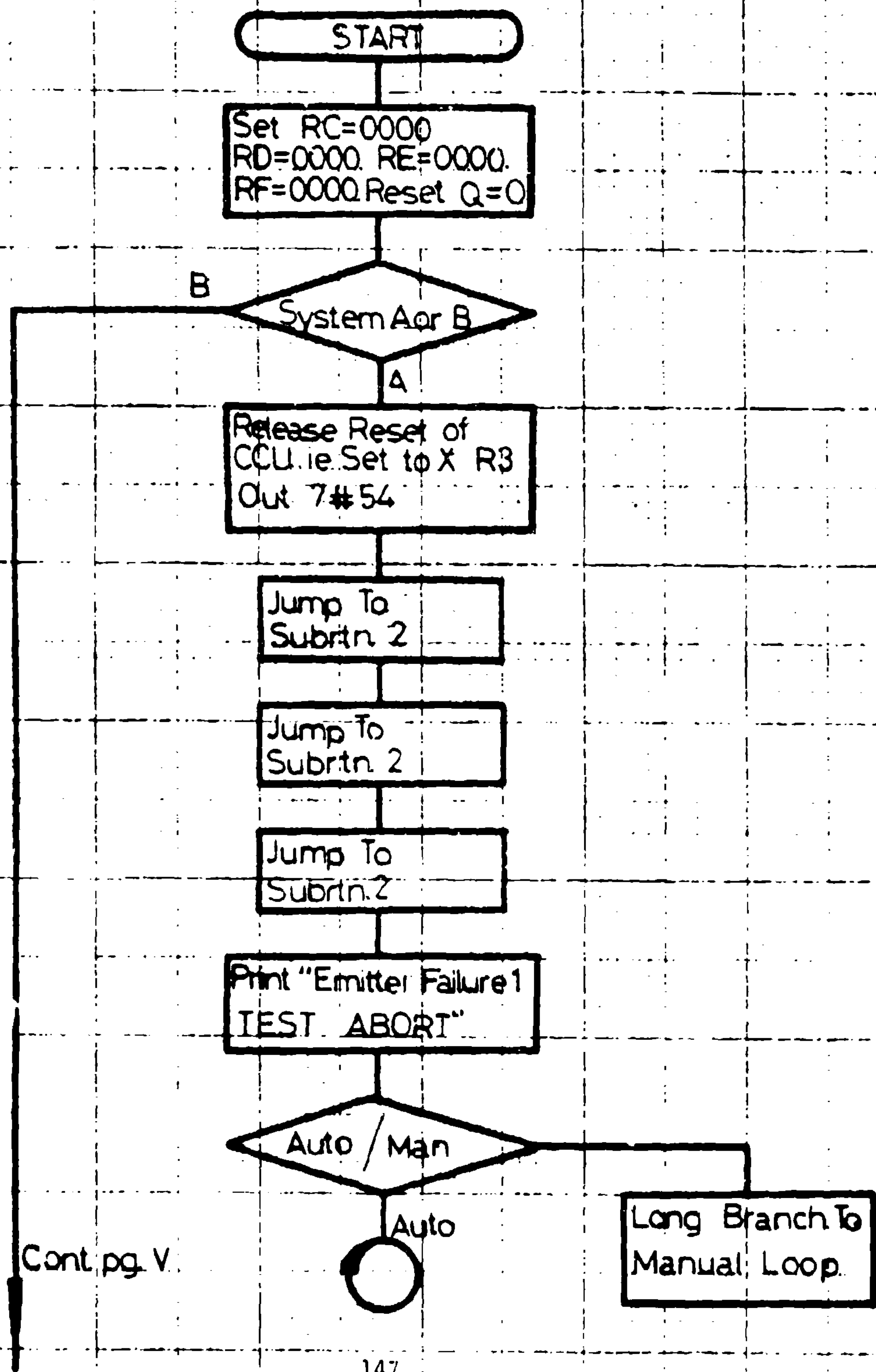
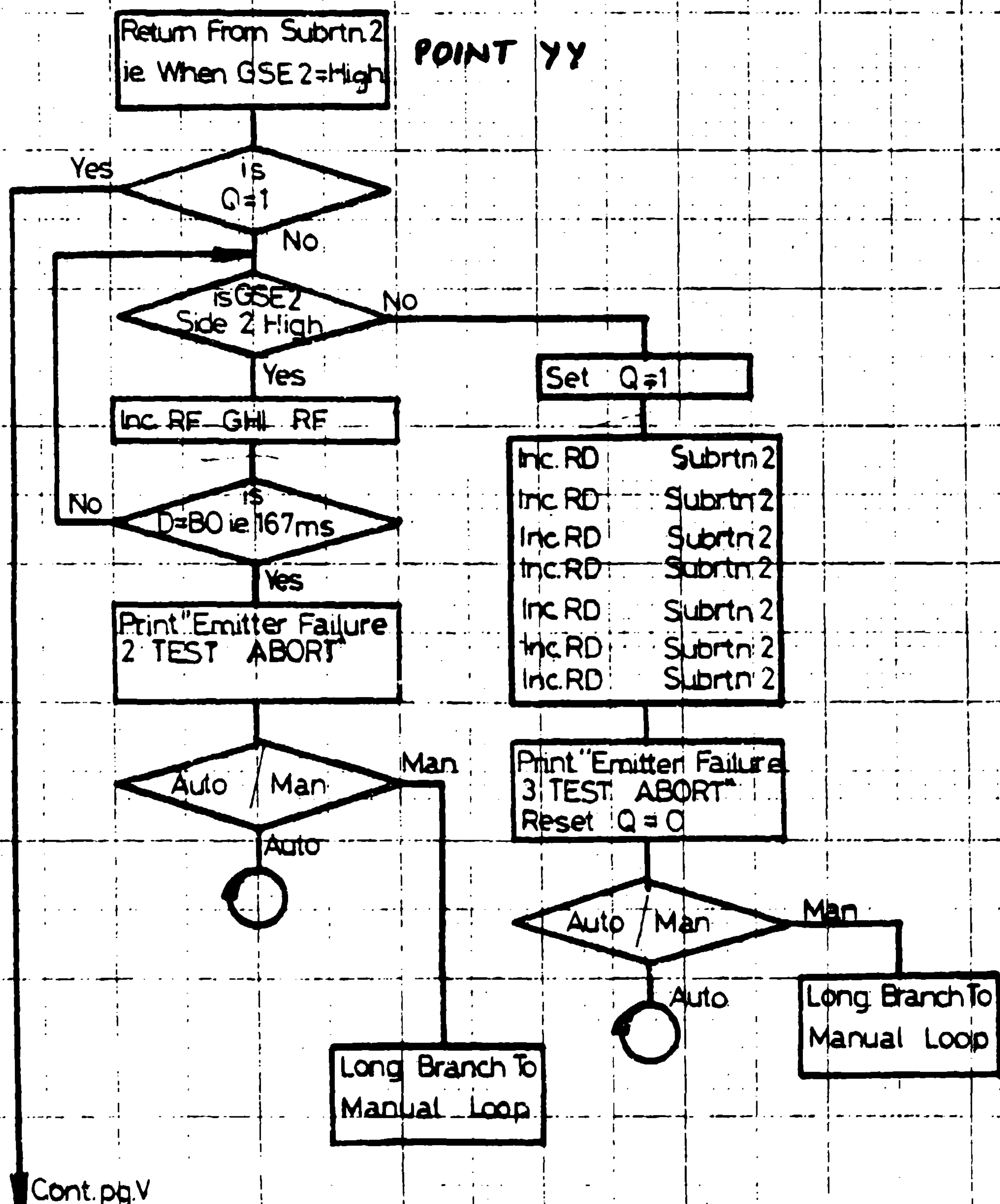

Yes
is 350v line Side 1 OK
No
Print "350v SIDE 1 FAILED
Set Q=1
No
is Q=1
Print "TEST ABORT."
Auto / Man
Auto
Man
Long Branch To Manual Loop
Do Emitter Test

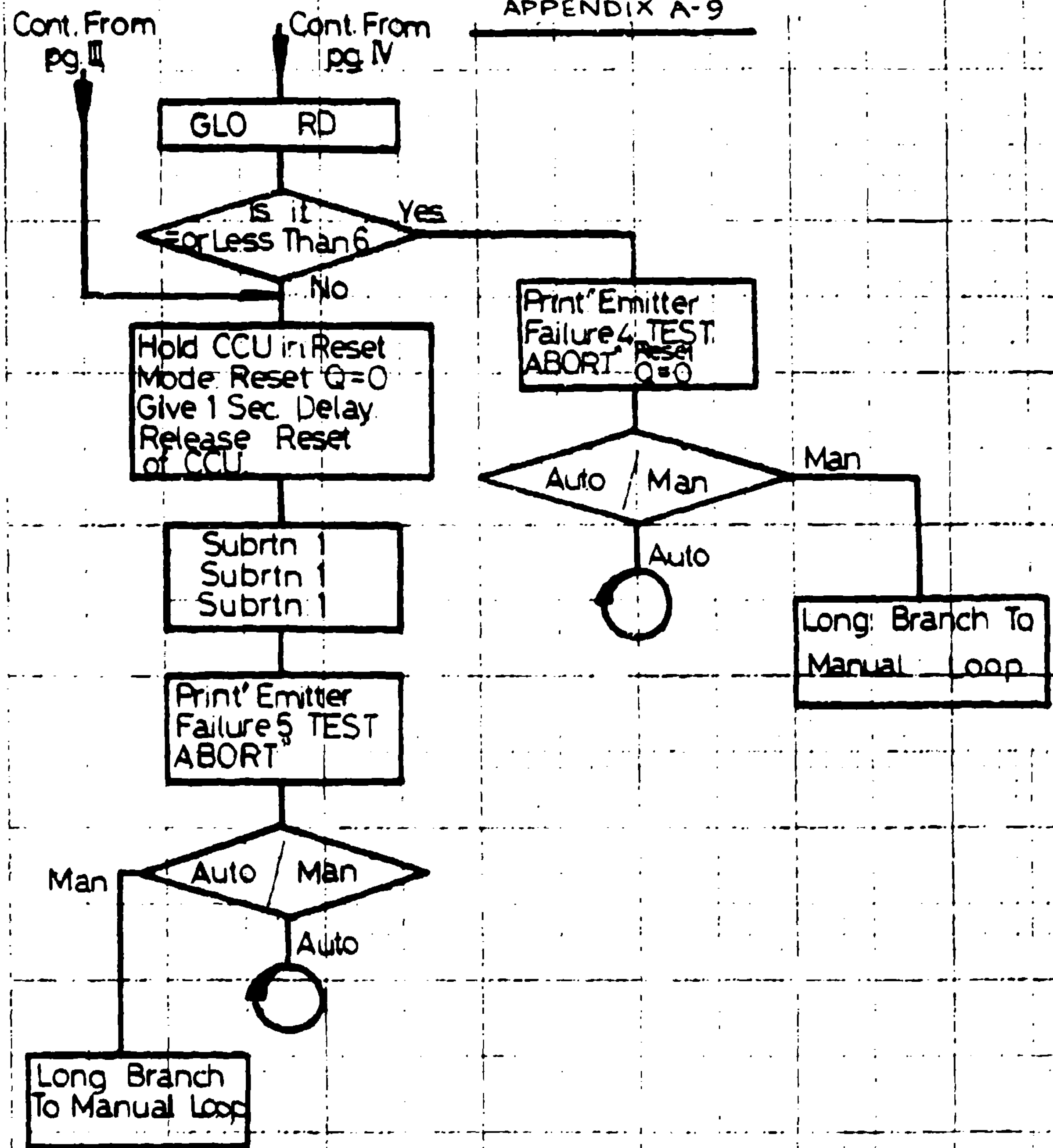
APPENDIX A-9

EMITTER TEST



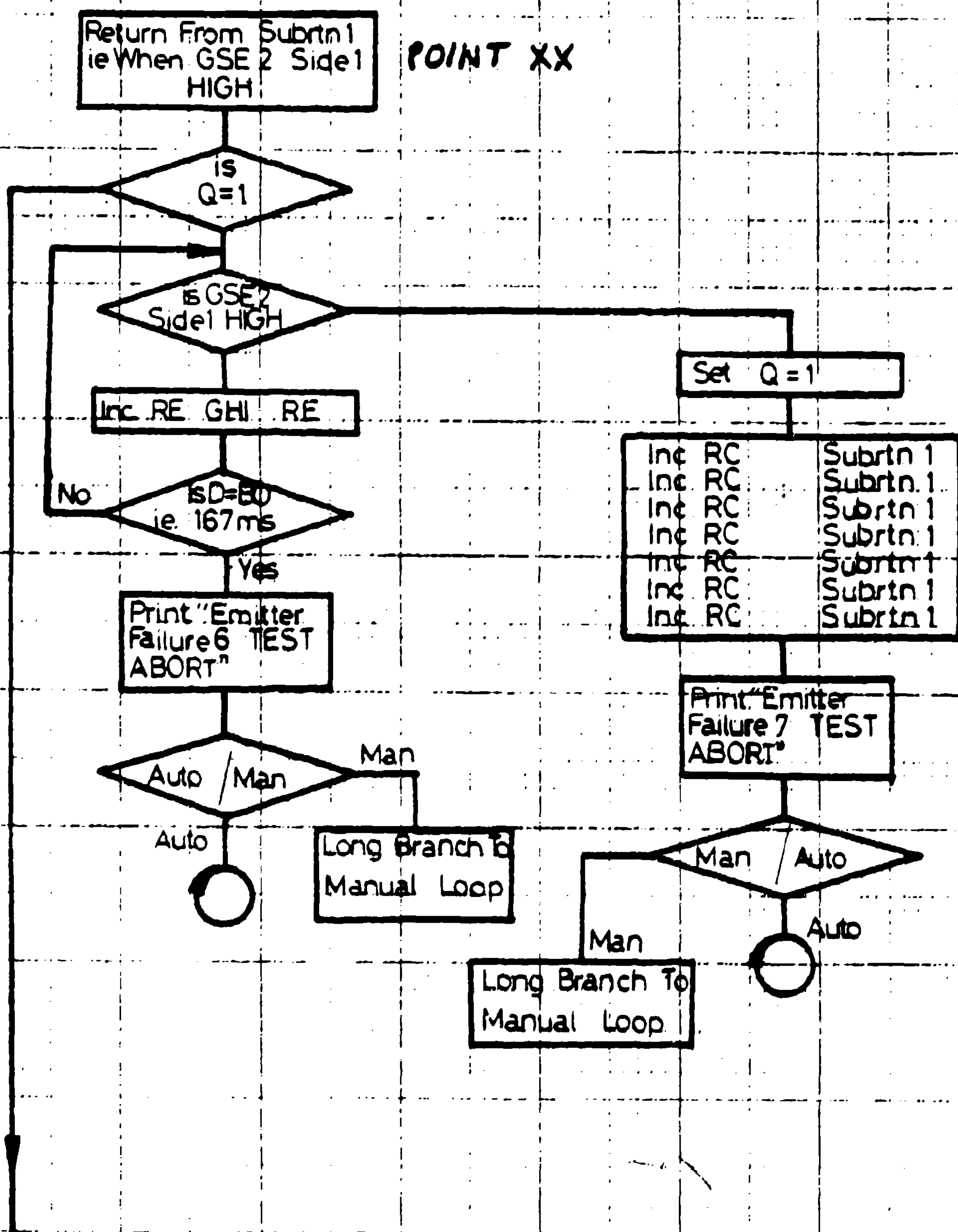

Return From Subrtn 2
ie When GSE 2=High
POINT YY
Yes
is Q=1
No
is GSE 2 Side 2 High
No
Yes
Set Q=1
Inc RF GHI RF
Inc.RD Subrtn 2
Inc.RD Subrtn 2
Inc.RD Subrtn 2
Inc.RD Subrtn 2
Inc.RD Subrtn 2
Inc.RD Subrtn 2
Inc.RD Subrtn 2
No
is D=B0 ie 167ms
Yes
Print "Emitter Failure 2 TEST ABORT"
Print "Emitter Failure 3 TEST ABORT" Reset Q=0
Auto / Man
Man
Auto
Auto / Man
Man
Auto
Long Branch To Manual Loop
Long Branch To Manual Loop
Cont. pg. V

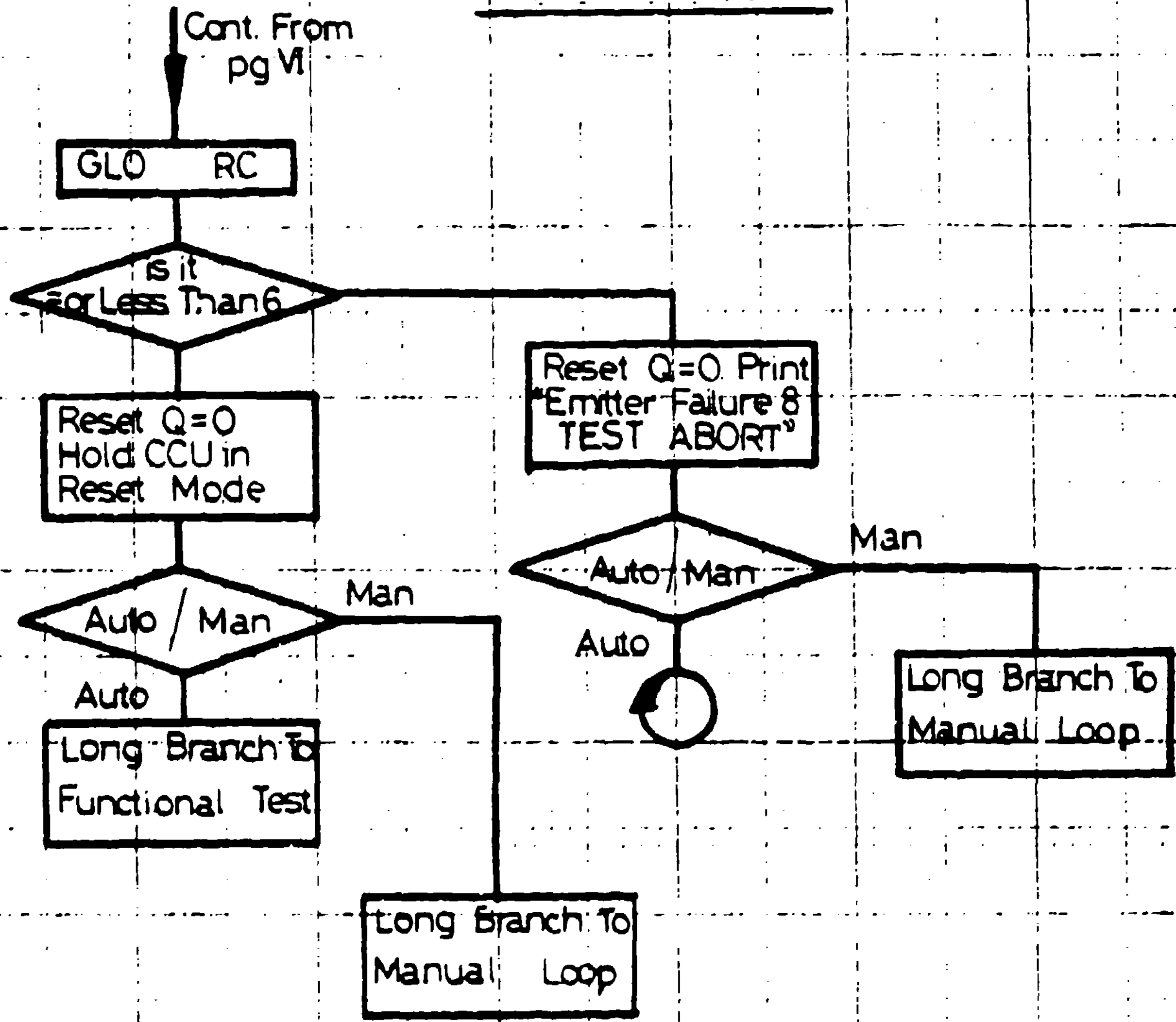
APPENDIX A-9



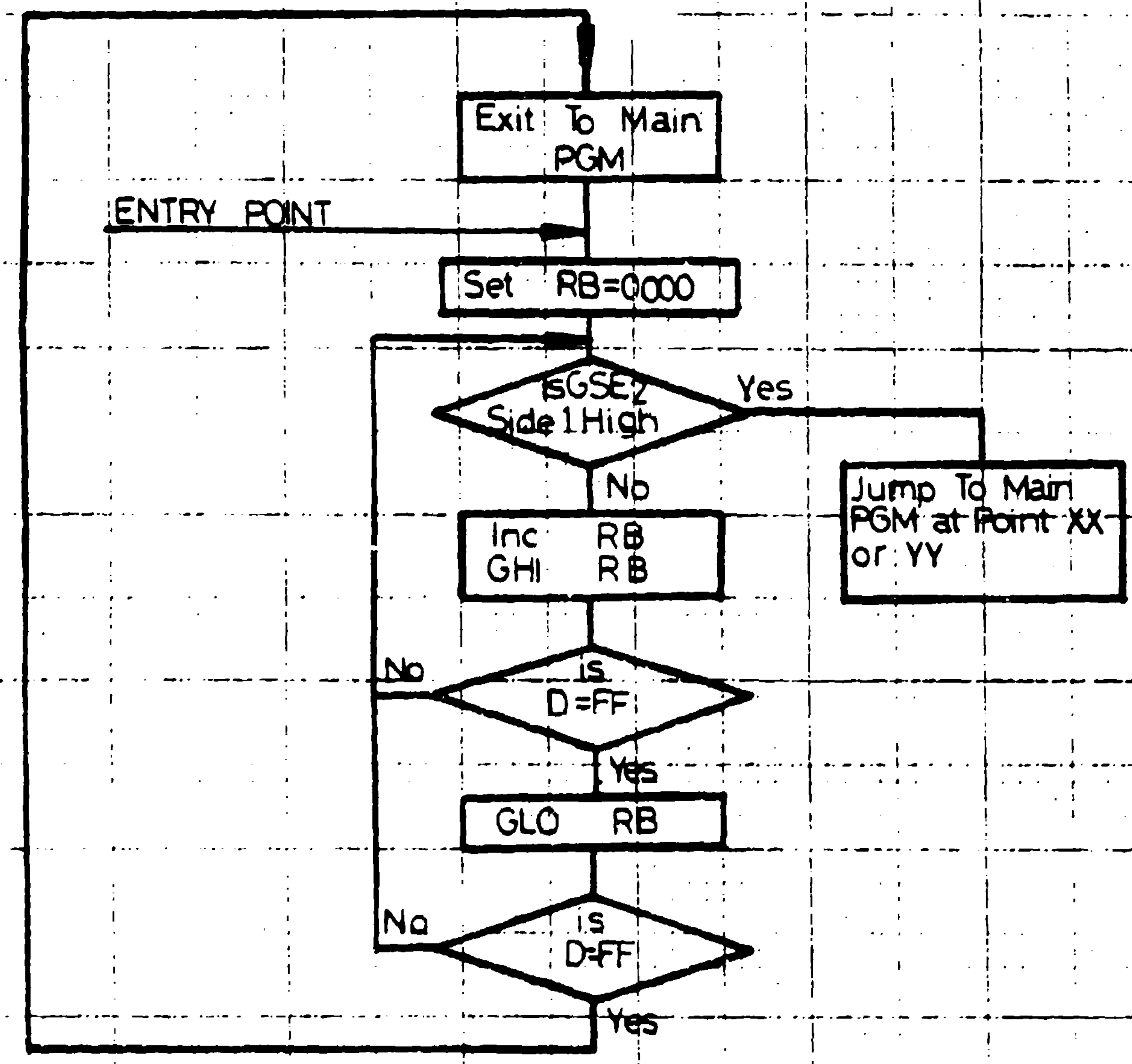
Cont. From pg. III
Cont. From pg. IV
GLO RD
Is it For Less Than 6
Yes
No
Hold CCU in Reset Mode Reset Q=0 Give 1 Sec. Delay Release Reset of CCU
Subrtn 1
Subrtn 1
Subrtn 1
Print' Emitter Failure 5 TEST ABORT"
Auto / Man
Man
Auto
Long Branch To Manual Loop
Print' Emitter Failure 4 TEST ABORT" Reset Q=0
Auto / Man
Man
Auto
Long Branch To Manual Loop

APPENDIX A-9


Return From Subrtn 1 ie When GSE 2 Side 1 HIGH
POINT XX
is Q=1
is GSE 2 Side 1 HIGH
Set Q = 1
Inc RE GHI RE
Inc RC Subrtn 1
Inc RC Subrtn 1
Inc RC Subrtn 1
Inc RC Subrtn 1
Inc RC Subrtn 1
Inc RC Subrtn 1
Inc RC Subrtn 1
No
is D=B0 ie. 167ms
Yes
Print "Emitter Failure 6 TEST ABORT"
Print "Emitter Failure 7 TEST ABORT"
Auto / Man
Man
Auto
Long Branch To Manual Loop
Man / Auto
Man
Auto
Long Branch To Manual Loop


Cont. From pg VI
GLO RC
Is it = or Less Than 6
Reset Q=0
Hold CCU in
Reset Mode
Auto / Man
Man
Auto
Long Branch To
Functional Test
Long Branch To
Manual Loop
Reset Q=0 Print
"Emitter Failure 8
TEST ABORT"
Auto / Man
Man
Auto
Long Branch To
Manual Loop

SUBRTN 1.

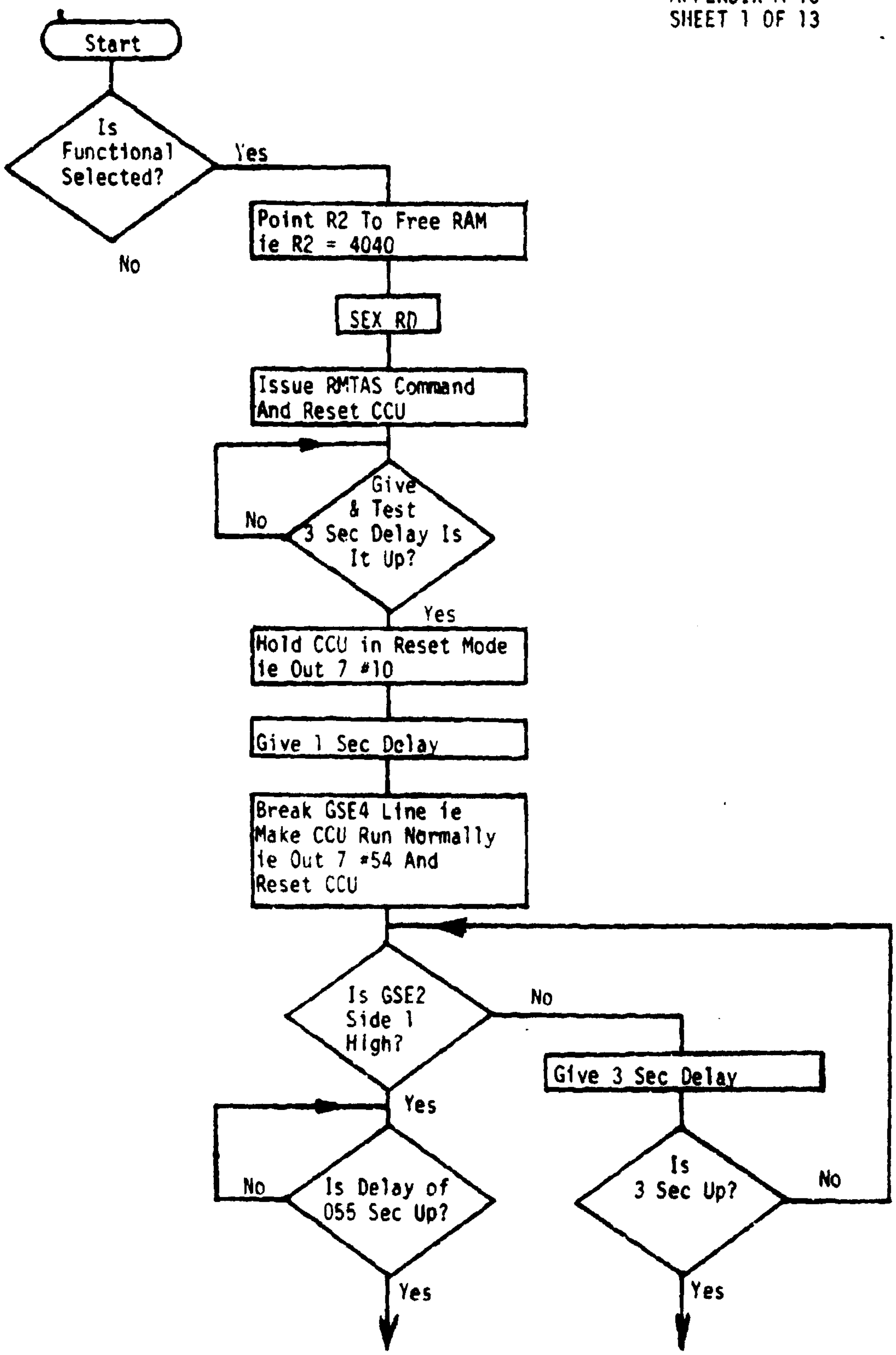


FOR SUBRTN 2, REPEAT ABOVE EXCEPT CHANGE ALL REFFERENCES ~~OF SIDE 1 TO SIDE 2~~. ALSO CHANGE POINT XX TO YY

FOR ASSEMBLY LISTING AND OBJECT CODE SEE APPENDIX A-7

APPENDIX A-10

FUNCTIONAL TEST FLOW DIAGRAM



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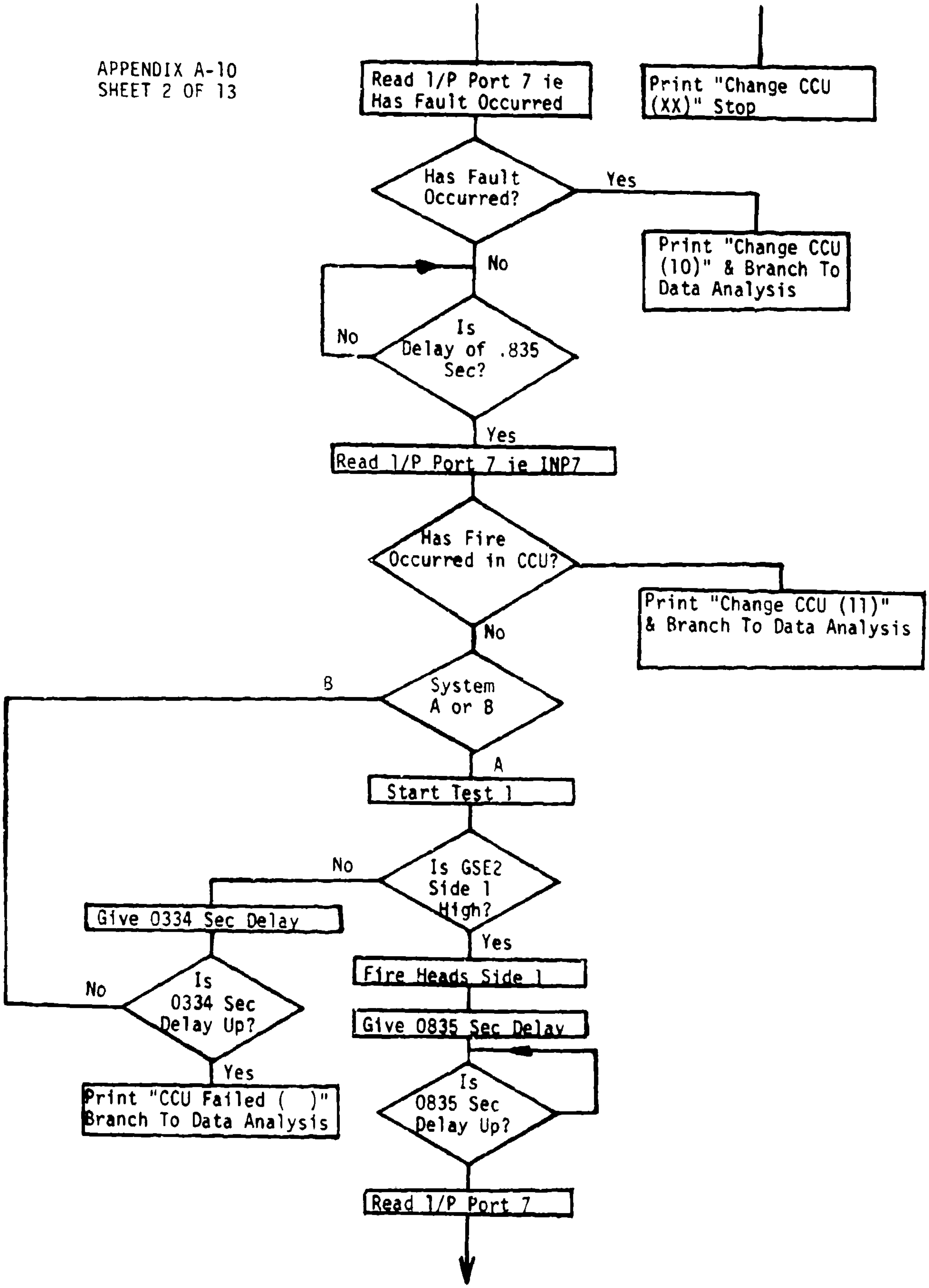
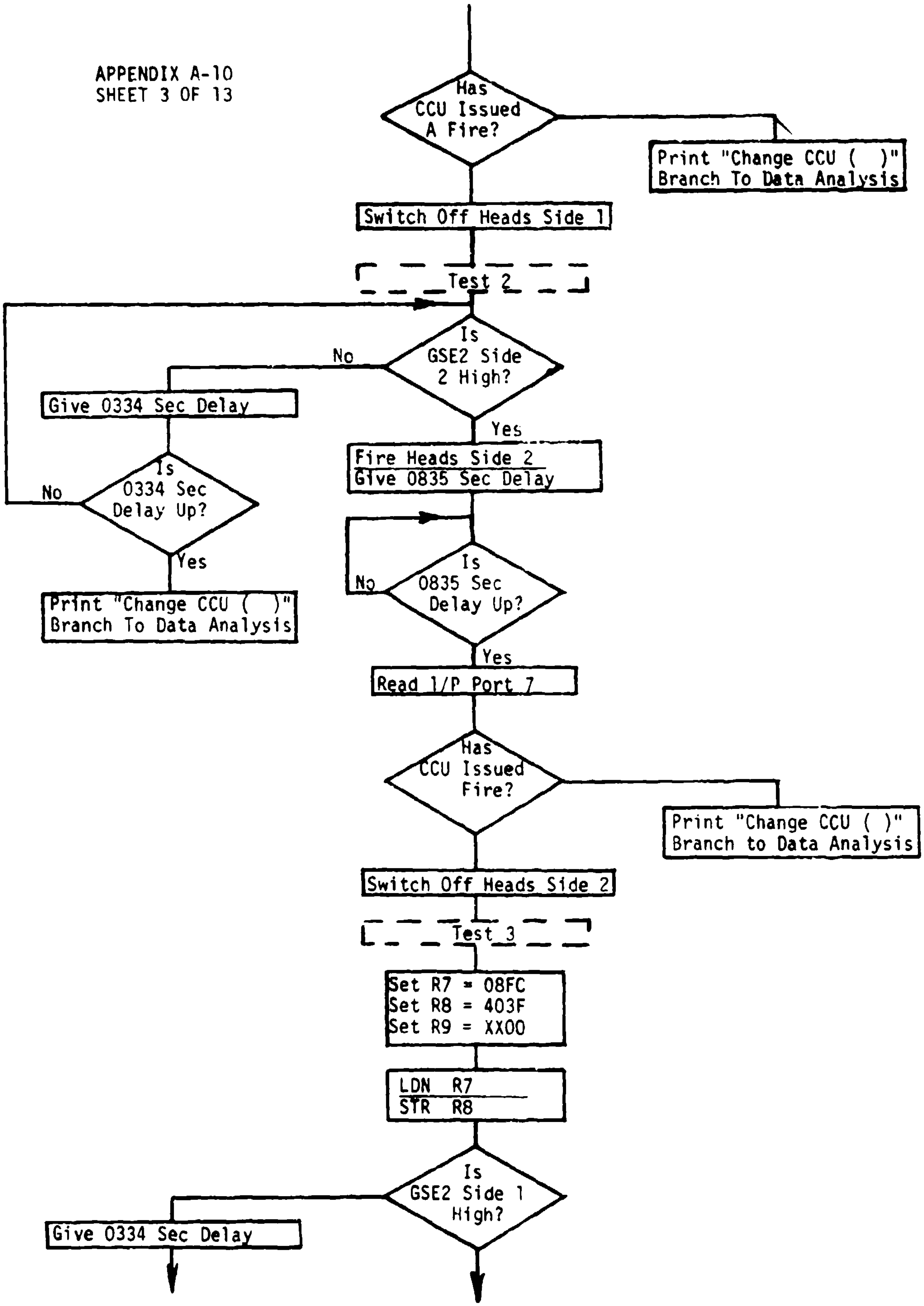
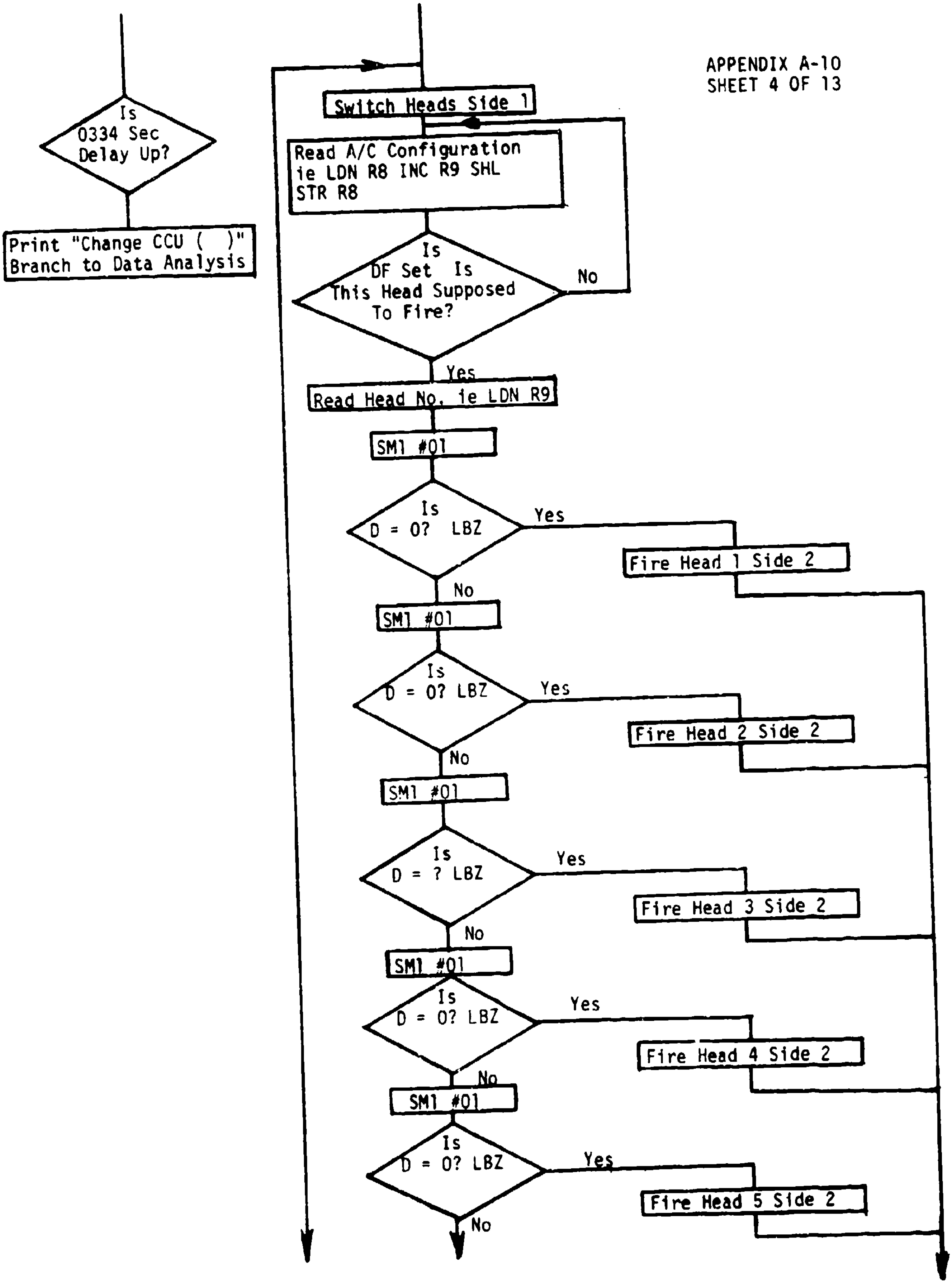
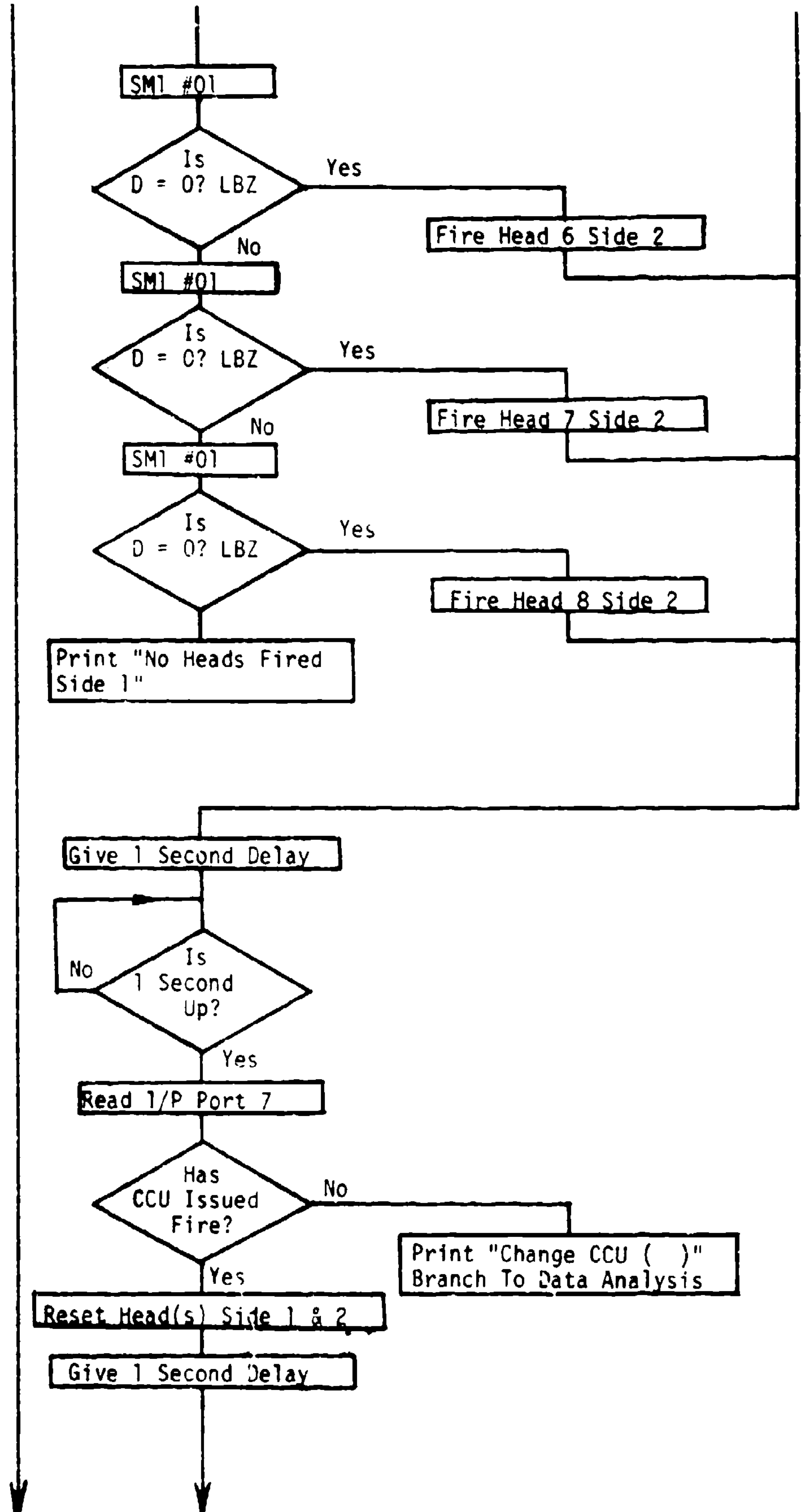
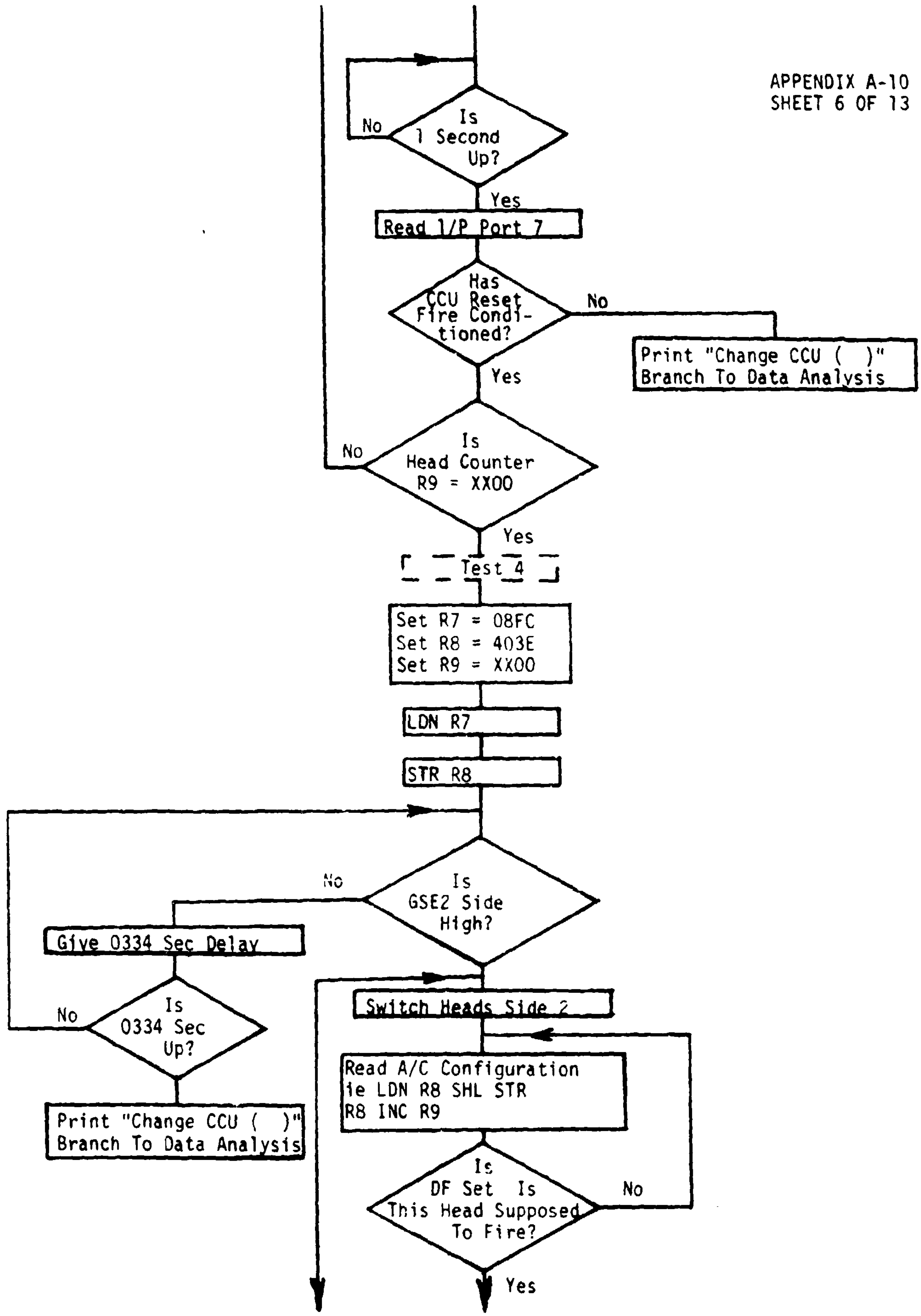

Read 1/P Port 7 ie Has Fault Occurred
Print "Change CCU (XX)" Stop
Has Fault Occurred?
Yes
Print "Change CCU (10)" & Branch To Data Analysis
No
Is Delay of .835 Sec?
No
Yes
Read 1/P Port 7 ie INP7
Has Fire Occurred in CCU?
Print "Change CCU (11)" & Branch To Data Analysis
No
System A or B
B
A
Start Test 1
Is GSE2 Side 1 High?
No
Give 0334 Sec Delay
Yes
Fire Heads Side 1
No
Is 0334 Sec Delay Up?
Give 0835 Sec Delay
Yes
Print "CCU Failed ( )" Branch To Data Analysis
Is 0835 Sec Delay Up?
Read 1/P Port 7

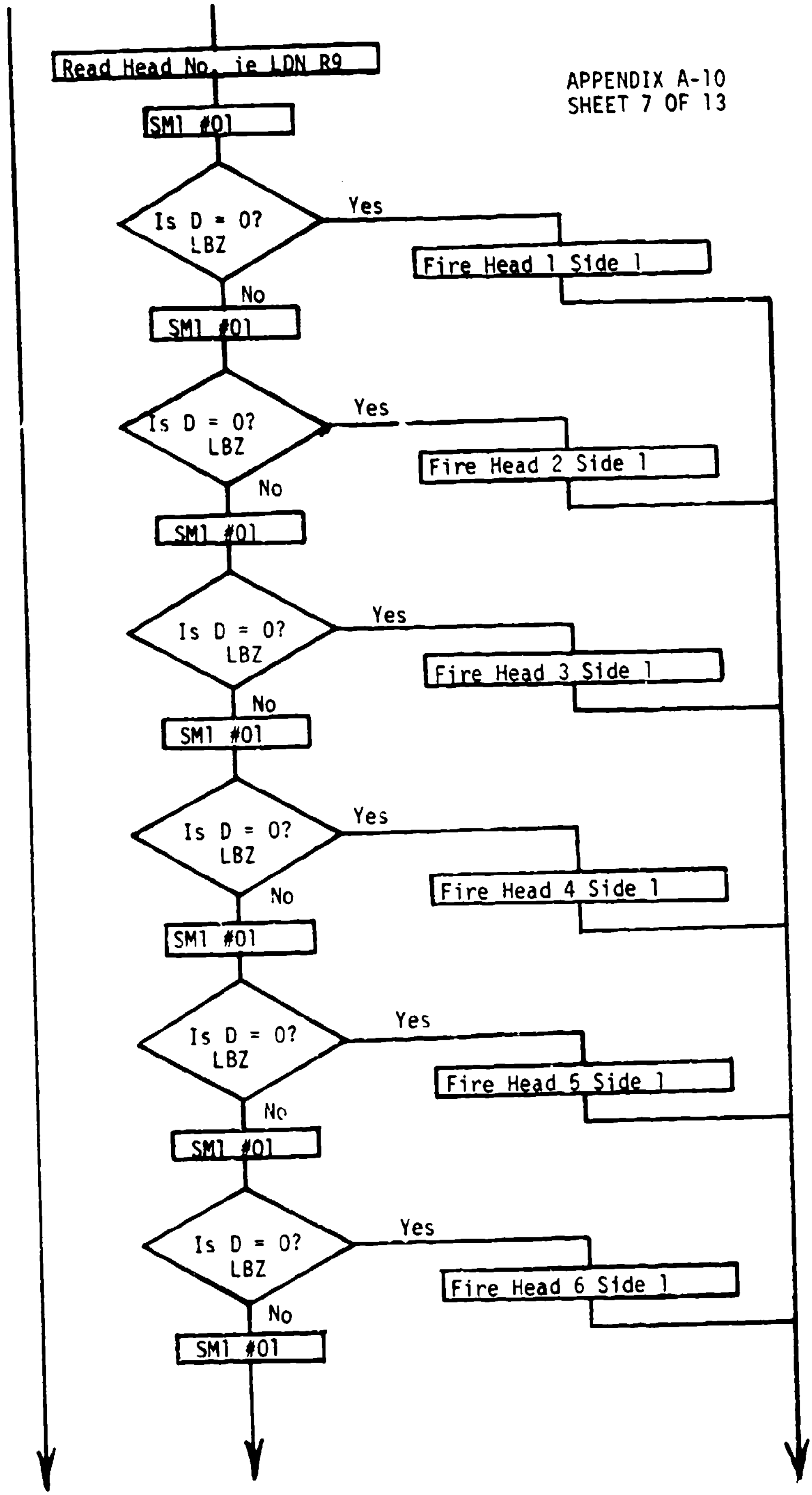
APPENDIX A-10
SHEET 3 OF 13



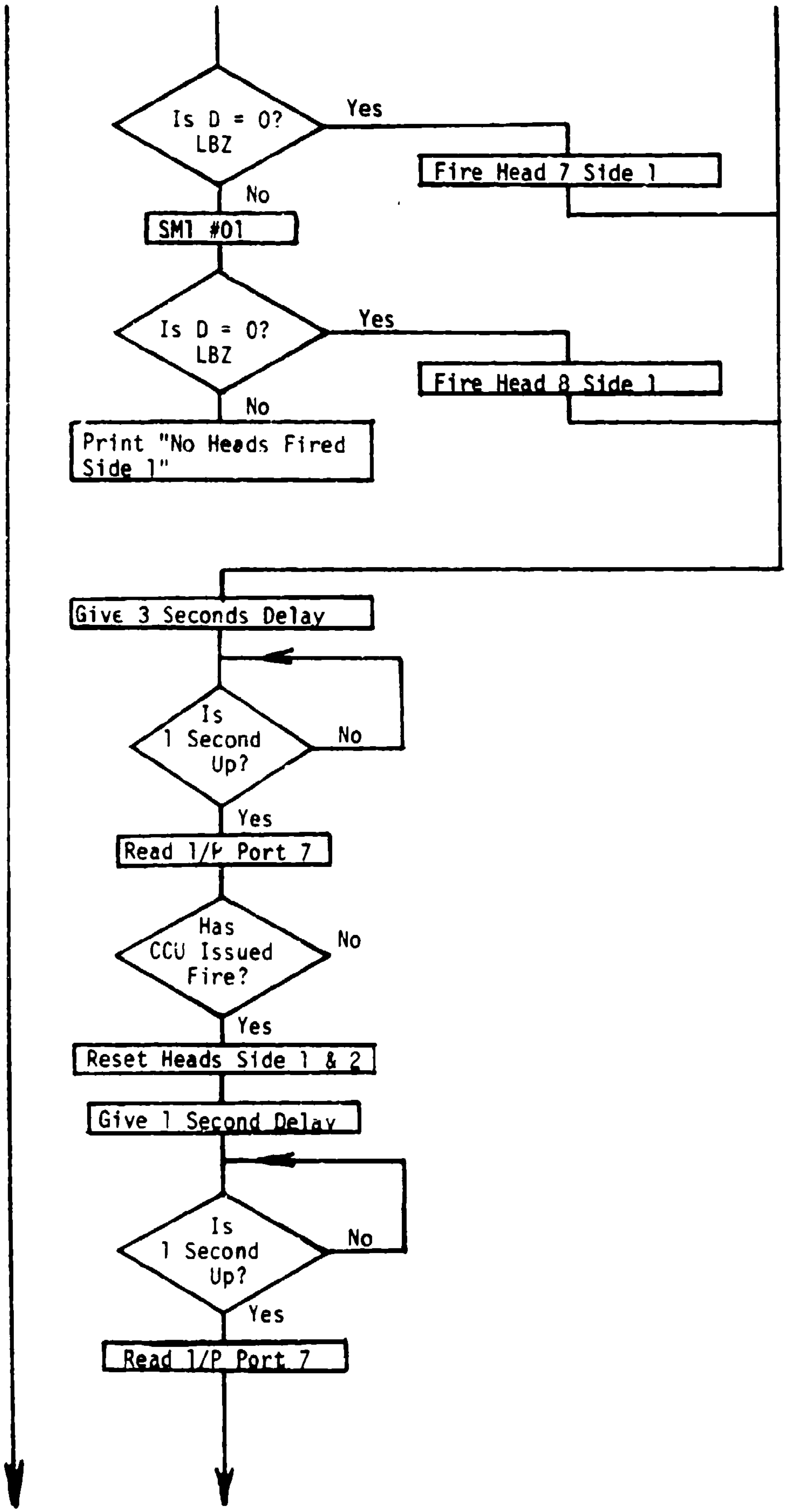

Is
0334 Sec
Delay Up?
Print "Change CCU ( )"
Branch to Data Analysis
Switch Heads Side 1
Read A/C Configuration
ie LDN R8 INC R9 SHL
STR R8
Is
DF Set Is
This Head Supposed
To Fire?
No
Yes
Read Head No. ie LDN R9
SM1 #01
Is
D = 0? LBZ
Yes
Fire Head 1 Side 2
No
SM1 #01
Is
D = 0? LBZ
Yes
Fire Head 2 Side 2
No
SM1 #01
Is
D = ? LBZ
Yes
Fire Head 3 Side 2
No
SM1 #01
Is
D = 0? LBZ
Yes
Fire Head 4 Side 2
No
SM1 #01
Is
D = 0? LBZ
Yes
Fire Head 5 Side 2
No


SM1 #01
Is D = 0? LBZ
Yes
Fire Head 6 Side 2
No
SM1 #01
Is D = 0? LBZ
Yes
Fire Head 7 Side 2
No
SM1 #01
Is D = 0? LBZ
Yes
Fire Head 8 Side 2
Print "No Heads Fired Side 1"
Give 1 Second Delay
No
Is 1 Second Up?
Yes
Read 1/P Port 7
Has CCU Issued Fire?
No
Print "Change CCU ( )" Branch To Data Analysis
Yes
Reset Head(s) Side 1 & 2
Give 1 Second Delay

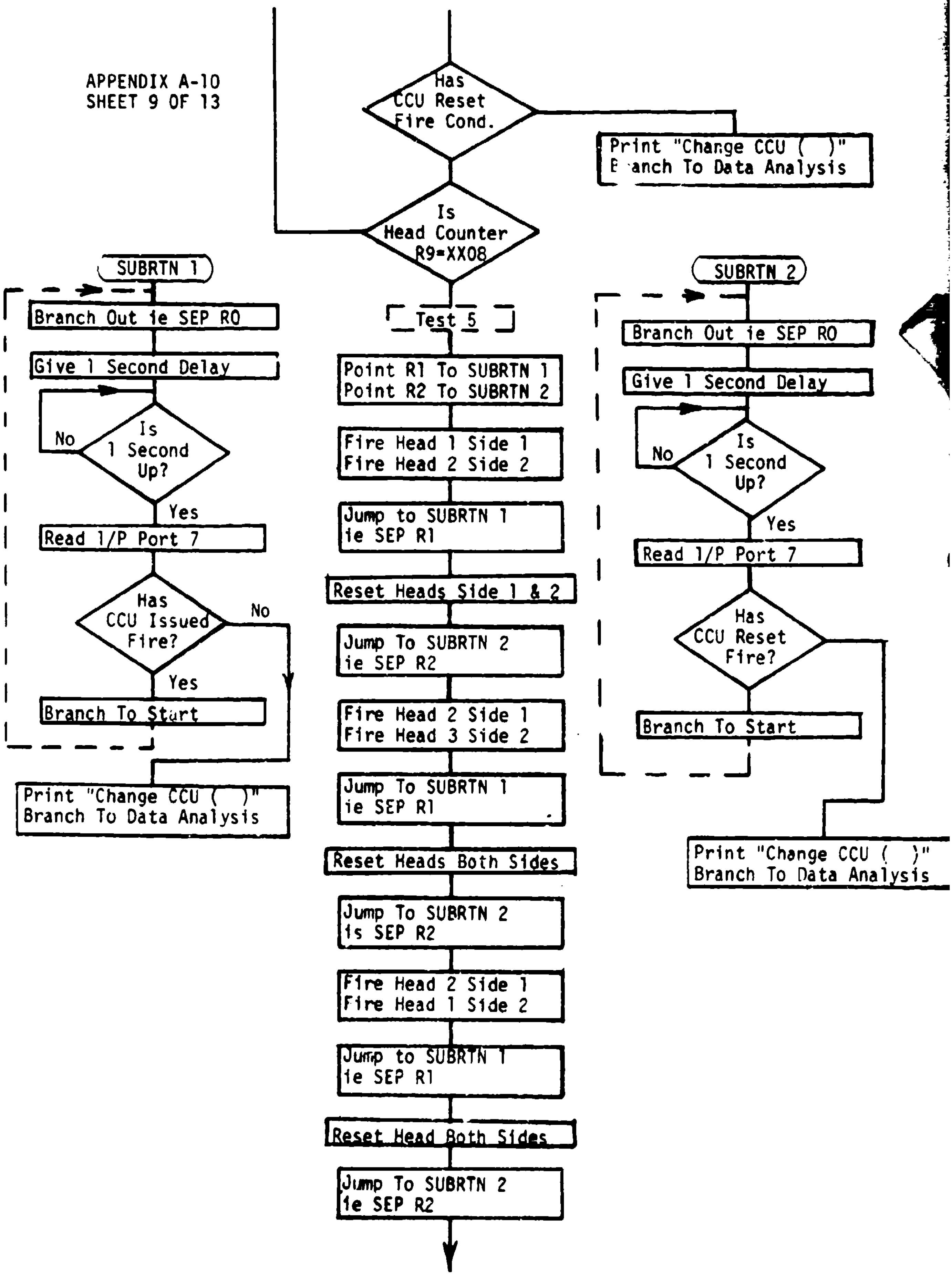

Is 1 Second Up?
No
Yes
Read 1/P Port 7
Has CCU Reset Fire Conditioned?
No
Print "Change CCU ( )" Branch To Data Analysis
Yes
Is Head Counter R9 = XX00
No
Yes
Test 4
Set R7 = 08FC
Set R8 = 403E
Set R9 = XX00
LDN R7
STR R8
Is GSE2 Side High?
No
Give 0334 Sec Delay
Is 0334 Sec Up?
No
Print "Change CCU ( )" Branch To Data Analysis
Switch Heads Side 2
Read A/C Configuration ie LDN R8 SHL STR R8 INC R9
Is DF Set Is This Head Supposed To Fire?
No
Yes

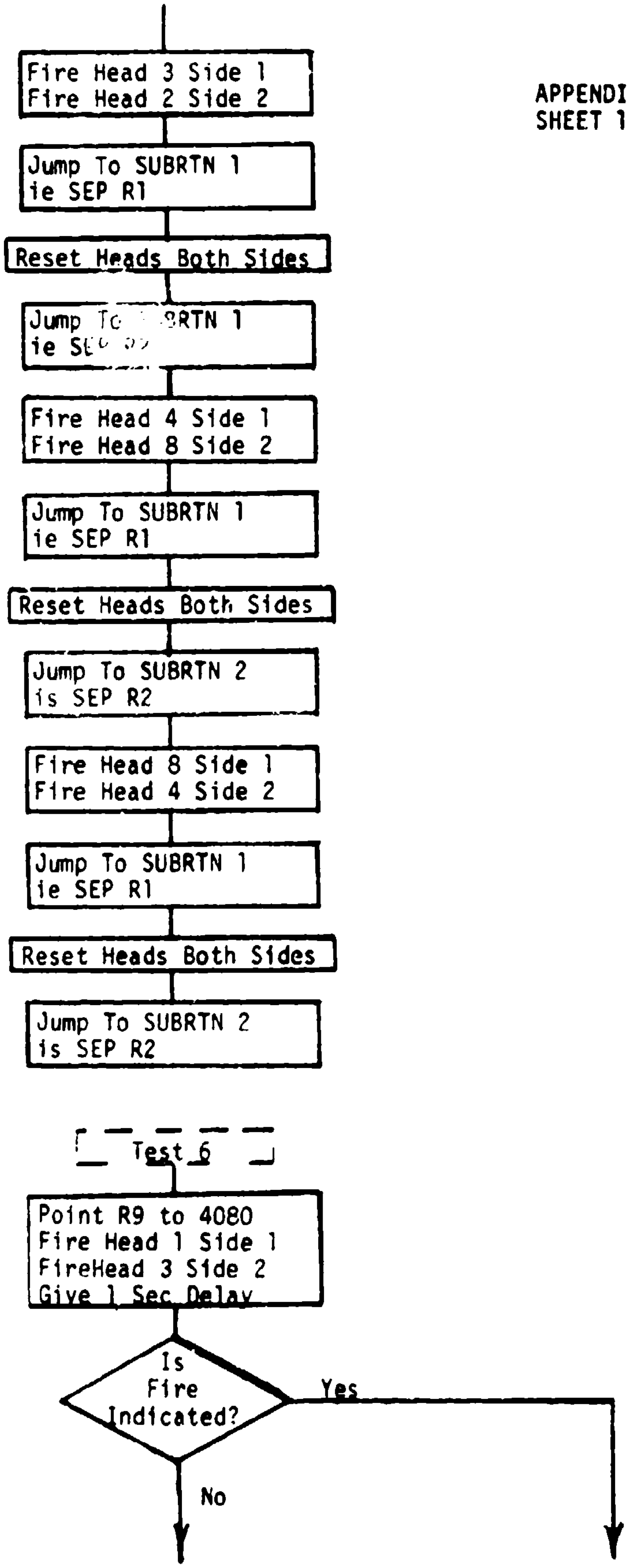

Read Head No. ie LDN R9
SM1 #01
Is D = 0?
LBZ
Yes
Fire Head 1 Side 1
No
SM1 #01
Is D = 0?
LBZ
Yes
Fire Head 2 Side 1
No
SM1 #01
Is D = 0?
LBZ
Yes
Fire Head 3 Side 1
No
SM1 #01
Is D = 0?
LBZ
Yes
Fire Head 4 Side 1
No
SM1 #01
Is D = 0?
LBZ
Yes
Fire Head 5 Side 1
No
SM1 #01
Is D = 0?
LBZ
Yes
Fire Head 6 Side 1
No
SM1 #01

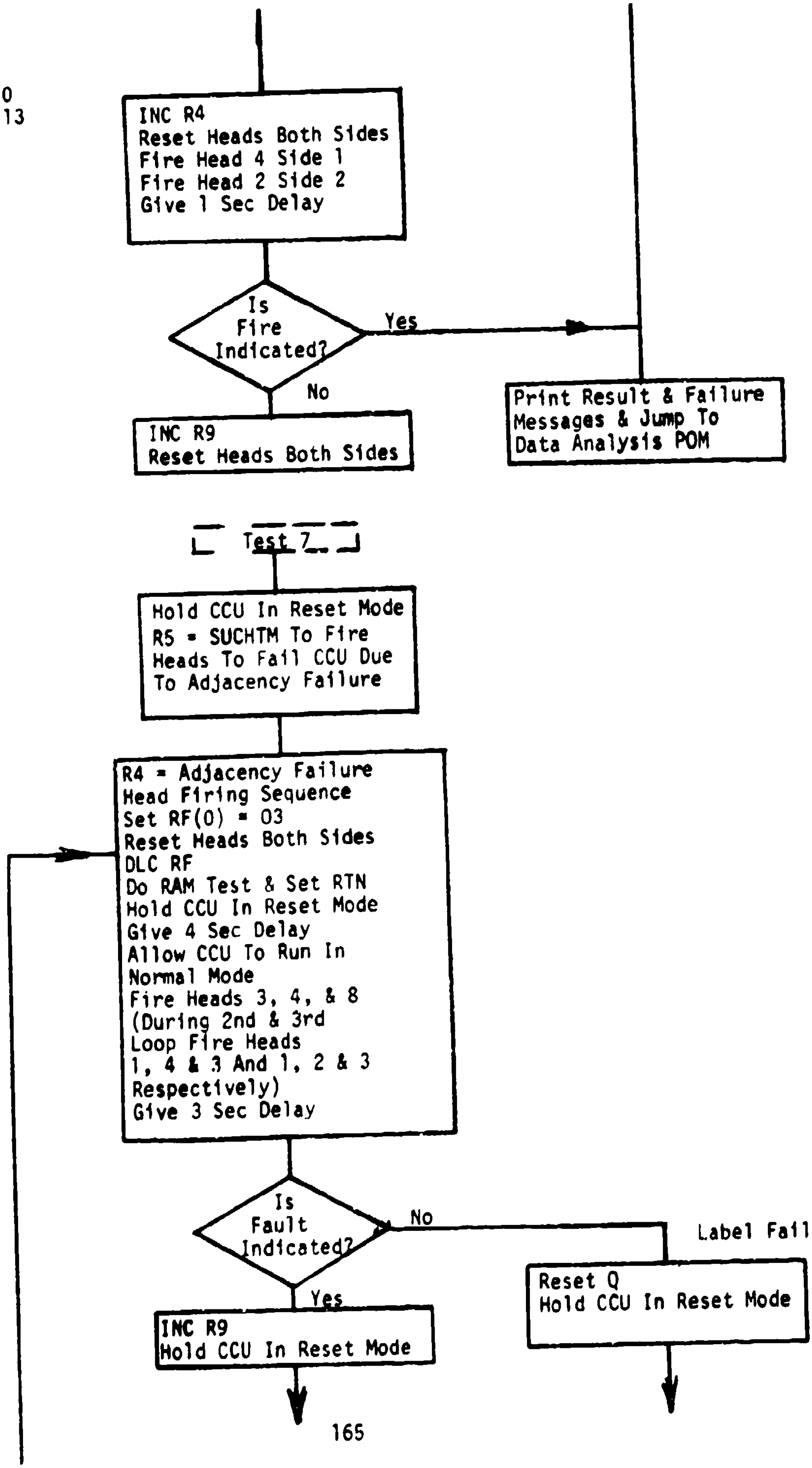
APPENDIX A-10
SHEET 8 OF 13



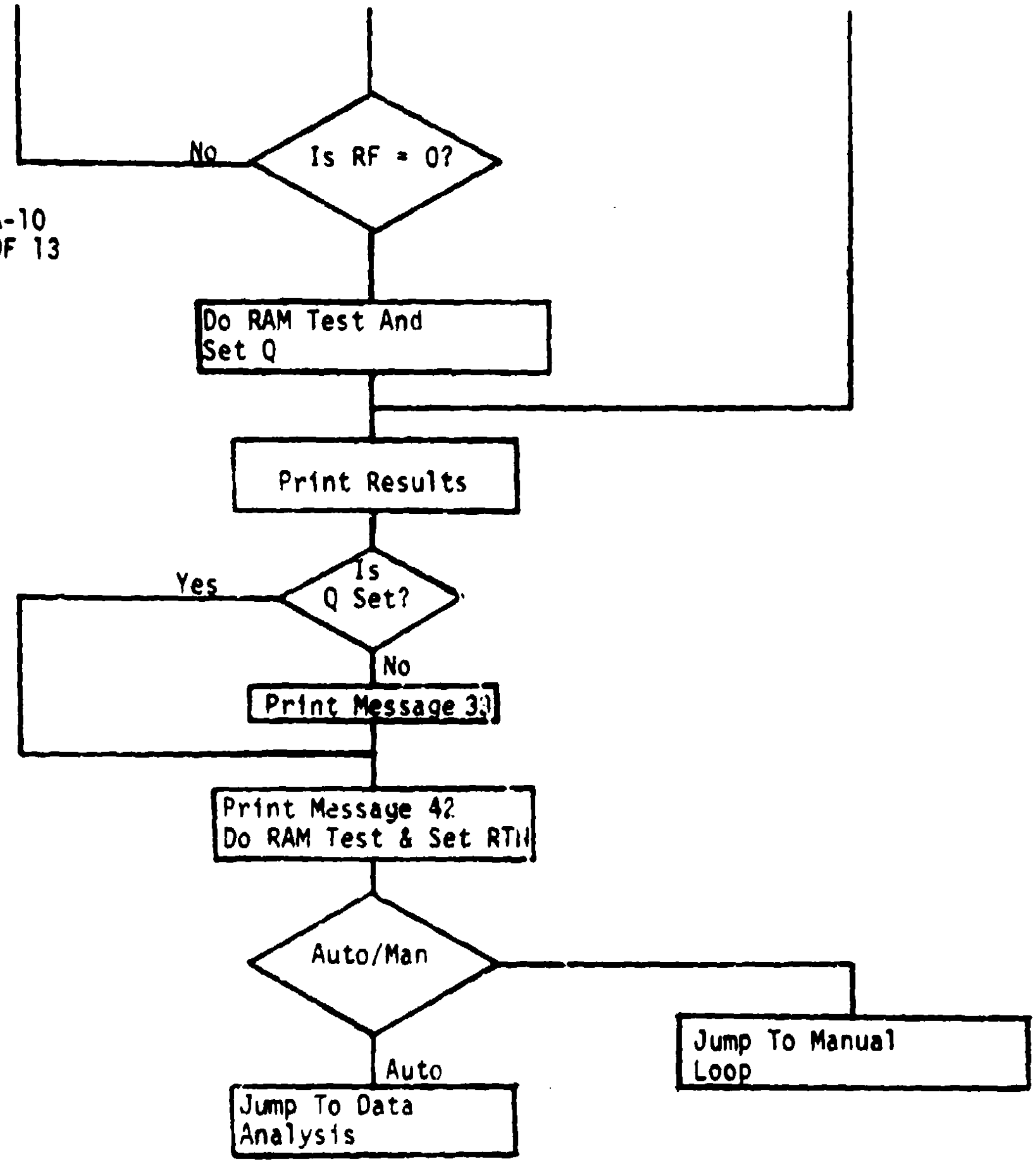
APPENDIX A-10
SHEET 9 OF 13

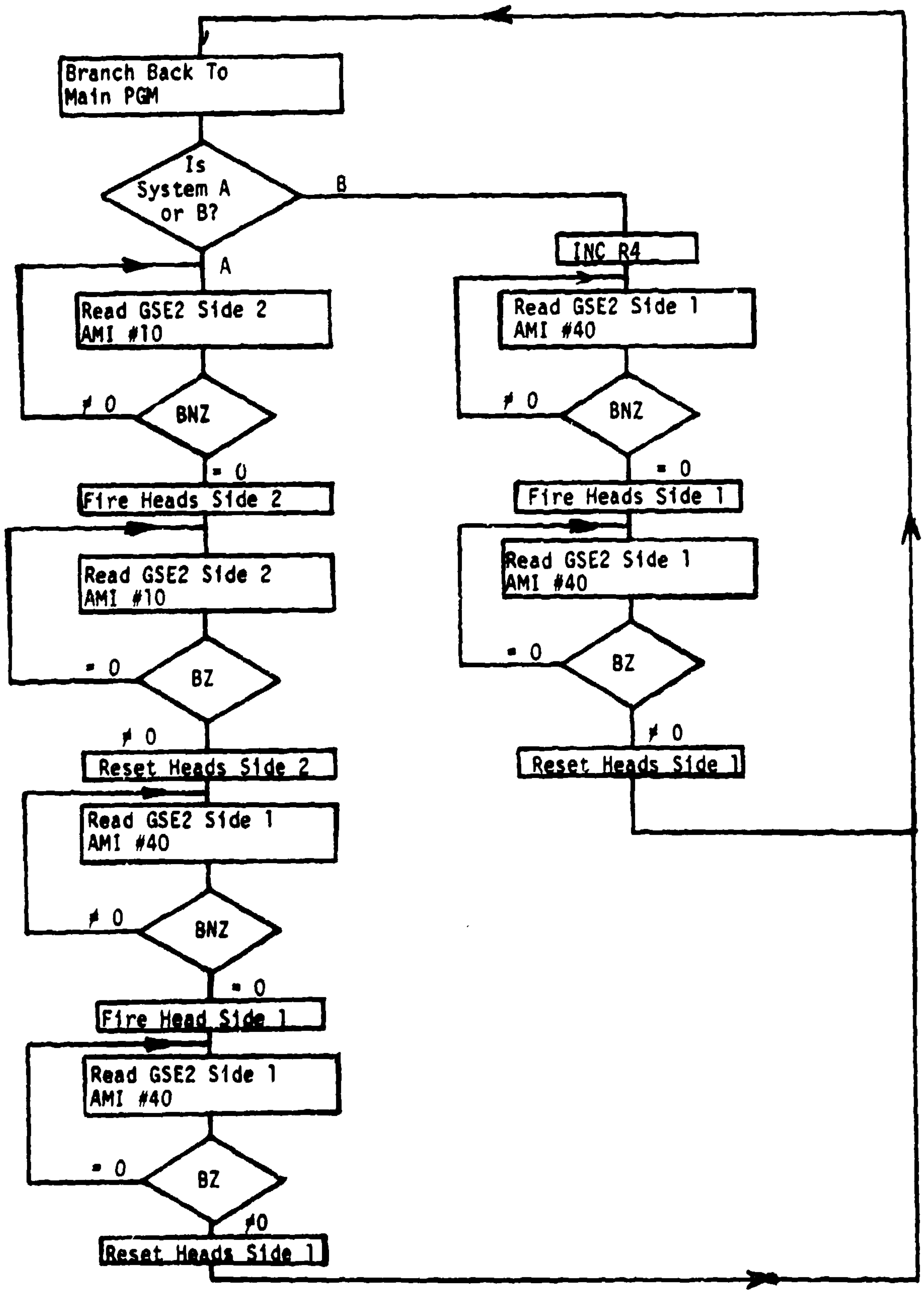



Fire Head 3 Side 1
Fire Head 2 Side 2
Jump To SUBRTN 1
ie SEP R1
Reset Heads Both Sides
Jump To
ie
Fire Head 4 Side 1
Fire Head 8 Side 2
Jump To SUBRTN 1
ie SEP R1
Reset Heads Both Sides
Jump To SUBRTN 2
is SEP R2
Fire Head 8 Side 1
Fire Head 4 Side 2
Jump To SUBRTN 1
ie SEP R1
Reset Heads Both Sides
Jump To SUBRTN 2
is SEP R2
Test 6
Point R9 to 4080
Fire Head 1 Side 1
FireHead 3 Side 2
Give 1 Sec Delay
Is Fire Indicated?
Yes
No


INC R4
Reset Heads Both Sides
Fire Head 4 Side 1
Fire Head 2 Side 2
Give 1 Sec Delay
Is Fire Indicated?
Yes
No
Print Result & Failure Messages & Jump To Data Analysis POM
INC R9
Reset Heads Both Sides
Test 7
Hold CCU In Reset Mode
R5 = SUCHTM To Fire Heads To Fail CCU Due To Adjacency Failure
R4 = Adjacency Failure Head Firing Sequence
Set RF(0) = 03
Reset Heads Both Sides
DLC RF
Do RAM Test & Set RTN
Hold CCU In Reset Mode
Give 4 Sec Delay
Allow CCU To Run In Normal Mode
Fire Heads 3, 4, & 8
(During 2nd & 3rd Loop Fire Heads 1, 4 & 3 And 1, 2 & 3 Respectively)
Give 3 Sec Delay
Is Fault Indicated?
No
Yes
Label Fail
Reset Q
Hold CCU In Reset Mode
INC R9
Hold CCU In Reset Mode

APPENDIX A-10
SHEET 12 OF 13

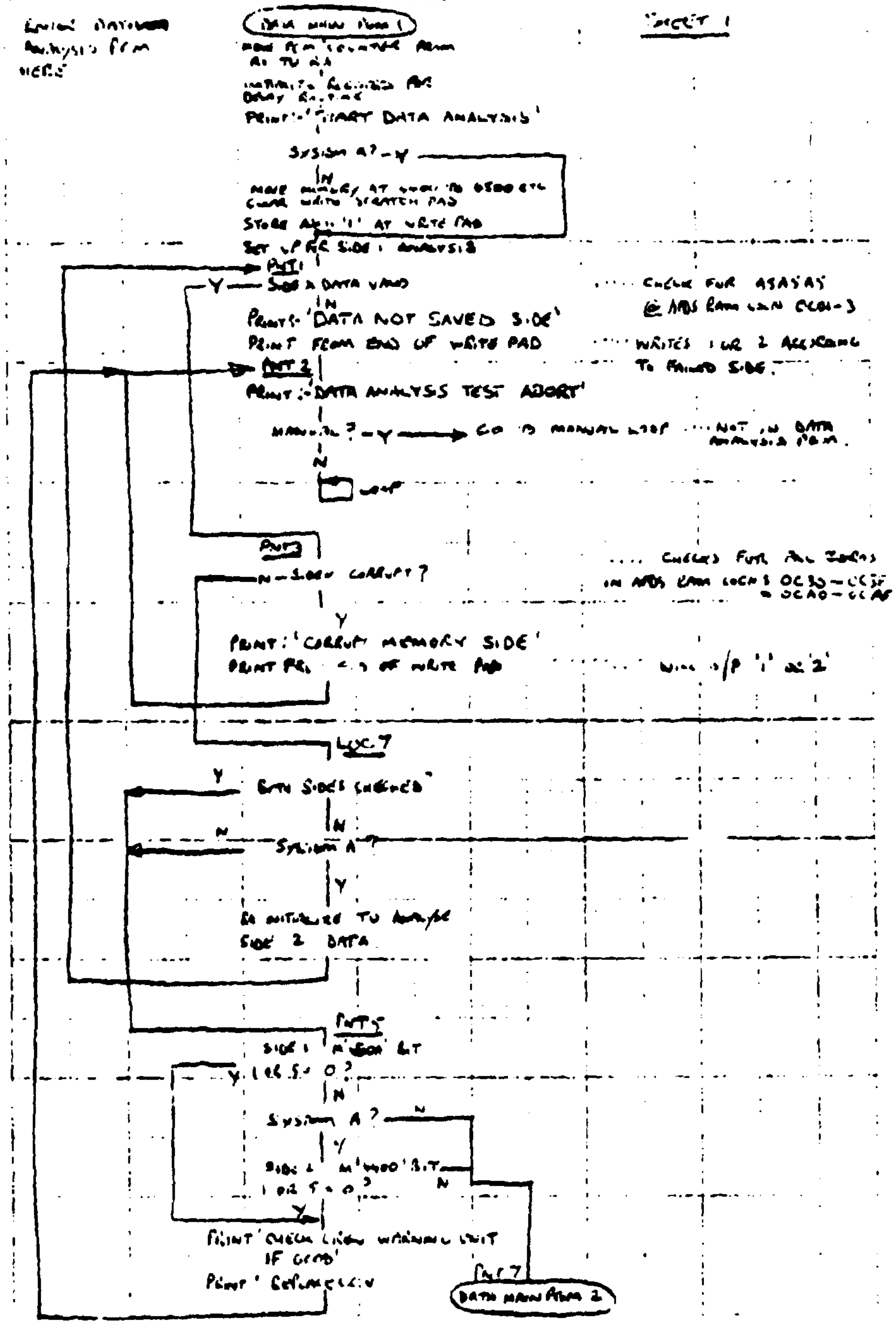



Branch Back To
Main PGM
Is
System A
or B?
B
A
INC R4
Read GSE2 Side 2
AMI #10
≠ 0
BNZ
= 0
Fire Heads Side 2
Read GSE2 Side 2
AMI #10
= 0
BZ
≠ 0
Reset Heads Side 2
Read GSE2 Side 1
AMI #40
≠ 0
BNZ
= 0
Fire Head Side 1
Read GSE2 Side 1
AMI #40
= 0
BZ
≠0
Reset Heads Side 1
Read GSE2 Side 1
AMI #40
≠ 0
BNZ
= 0
Fire Heads Side 1
Read GSE2 Side 1
AMI #40
= 0
BZ
≠ 0
Reset Heads Side 1

APPENDIX A-11

DATA ANALYSIS FLOW DIAGRAM

APPENDIX A-11



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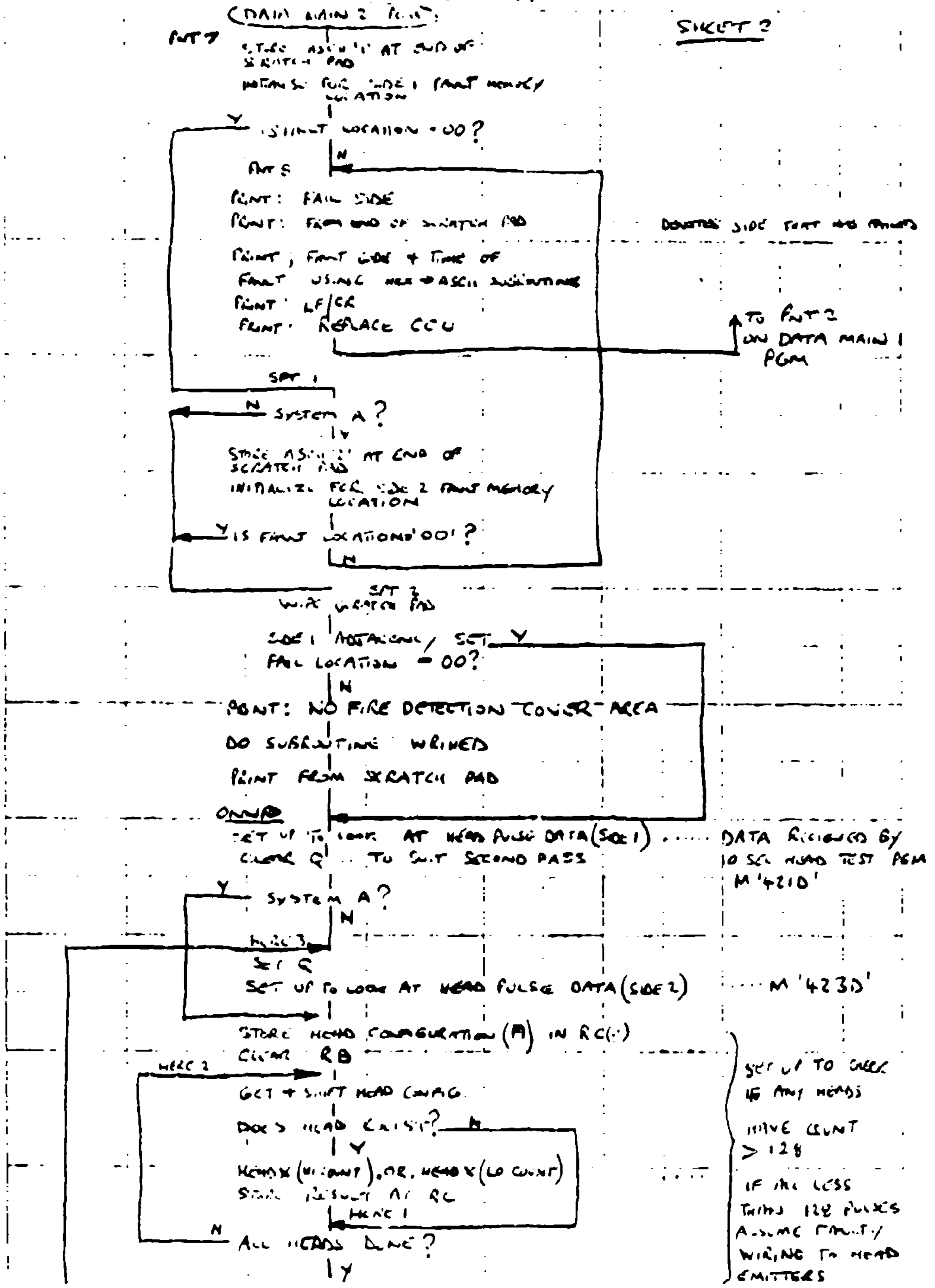
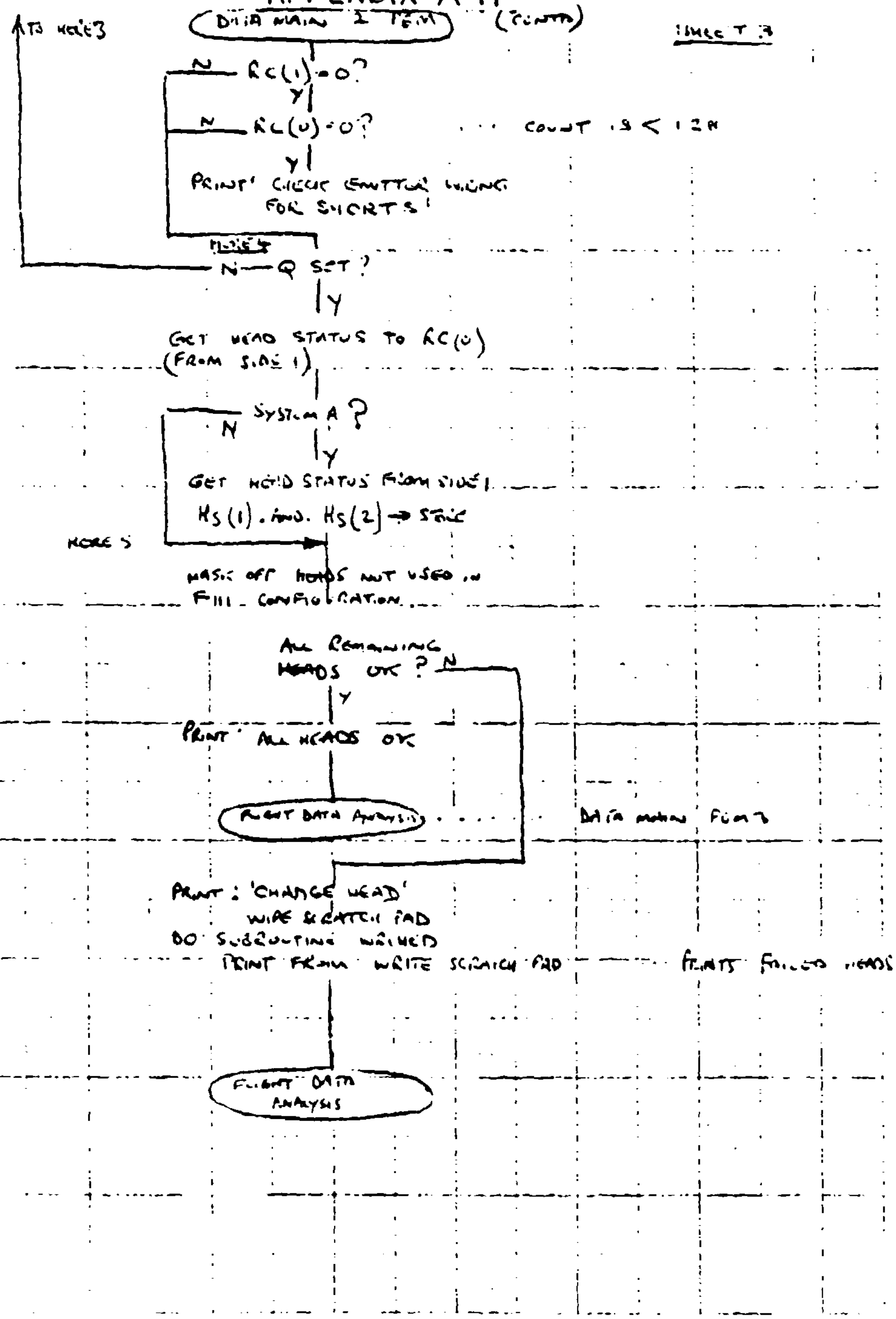
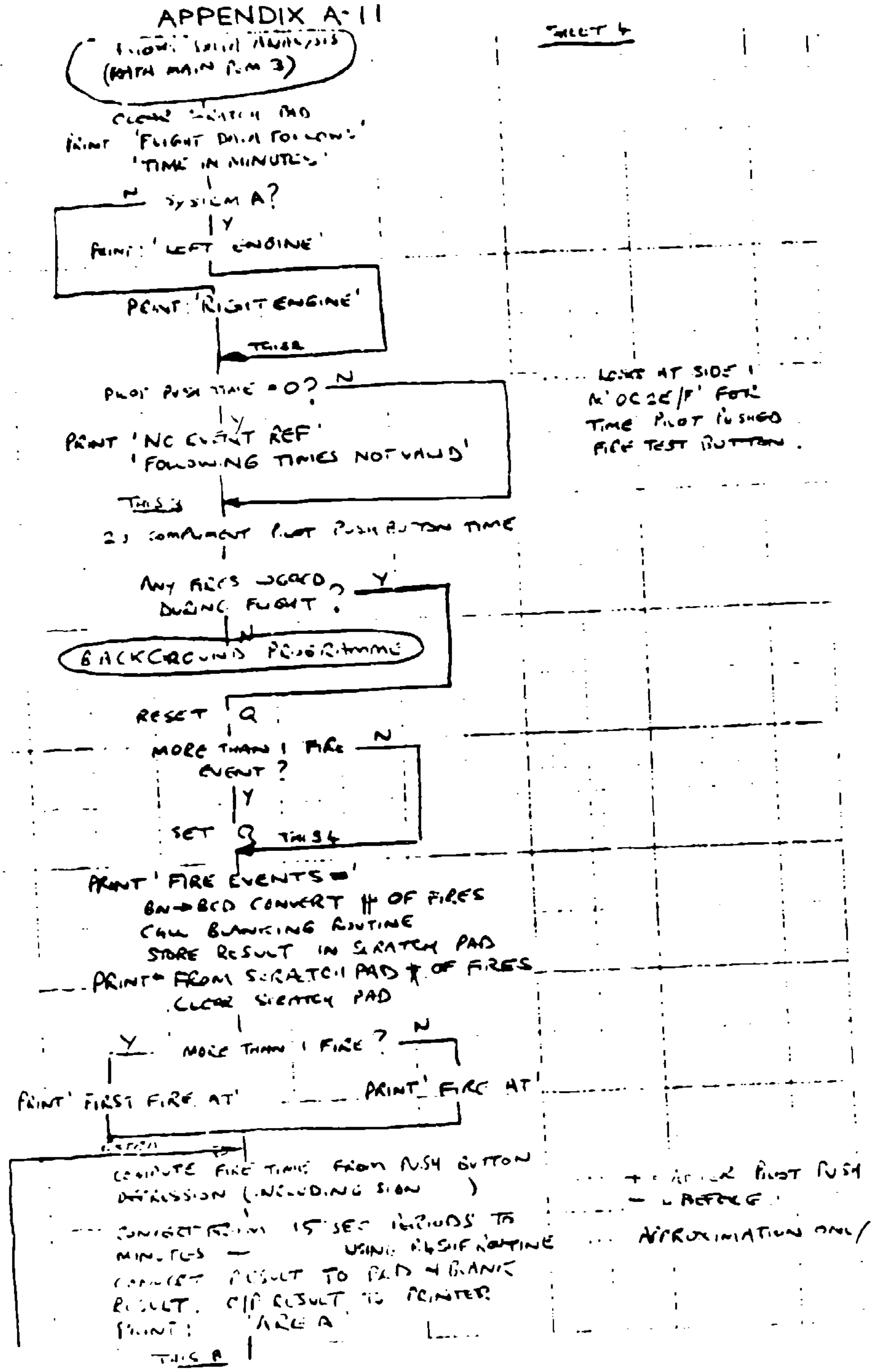
APPENDIX A-11



APPENDIX A-11

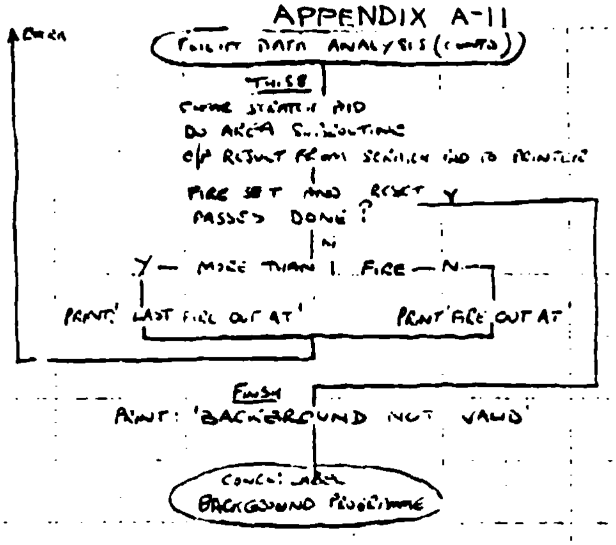


APPENDIX A-11

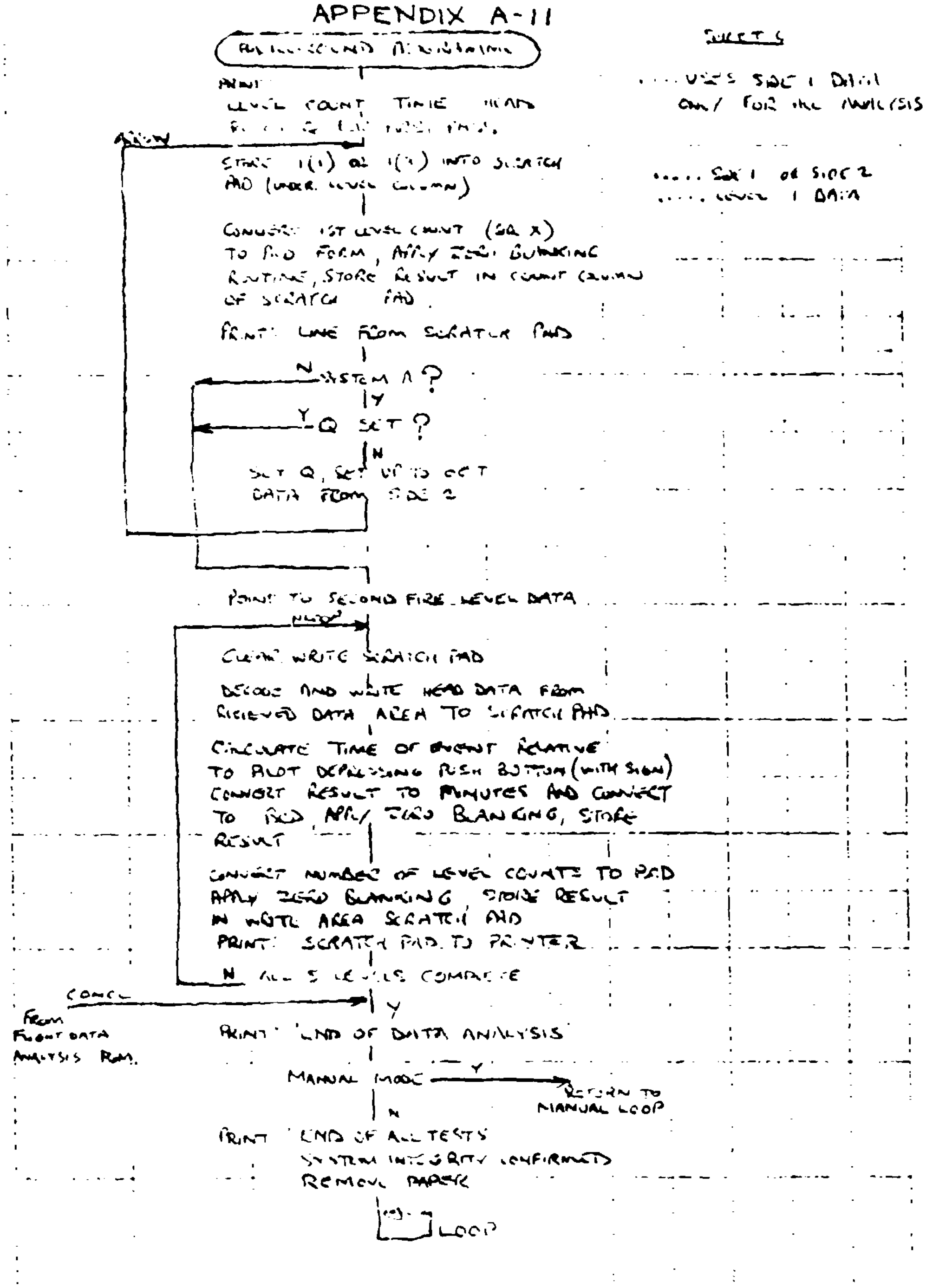


APPENDIX A-11

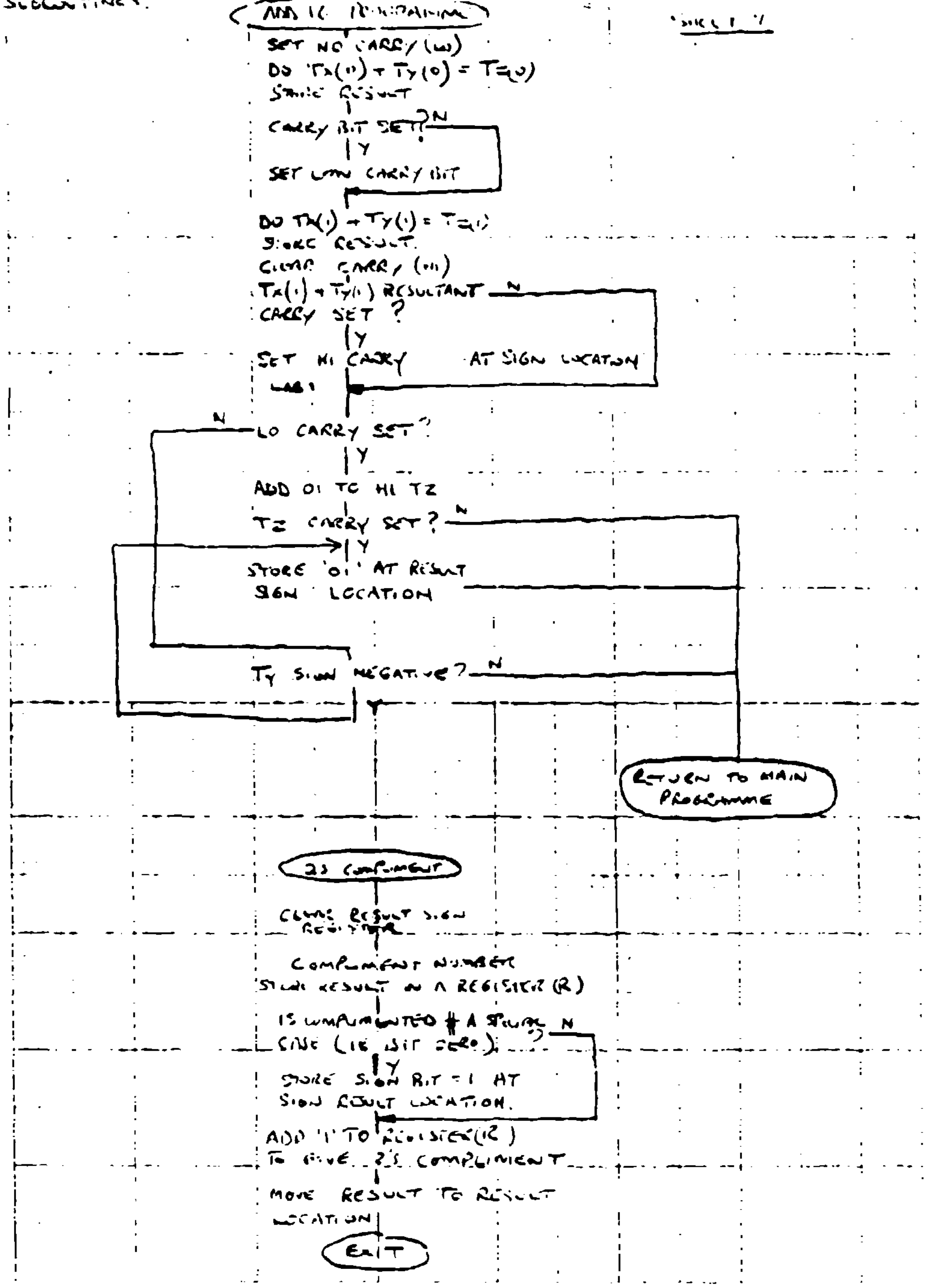
SHEET 5



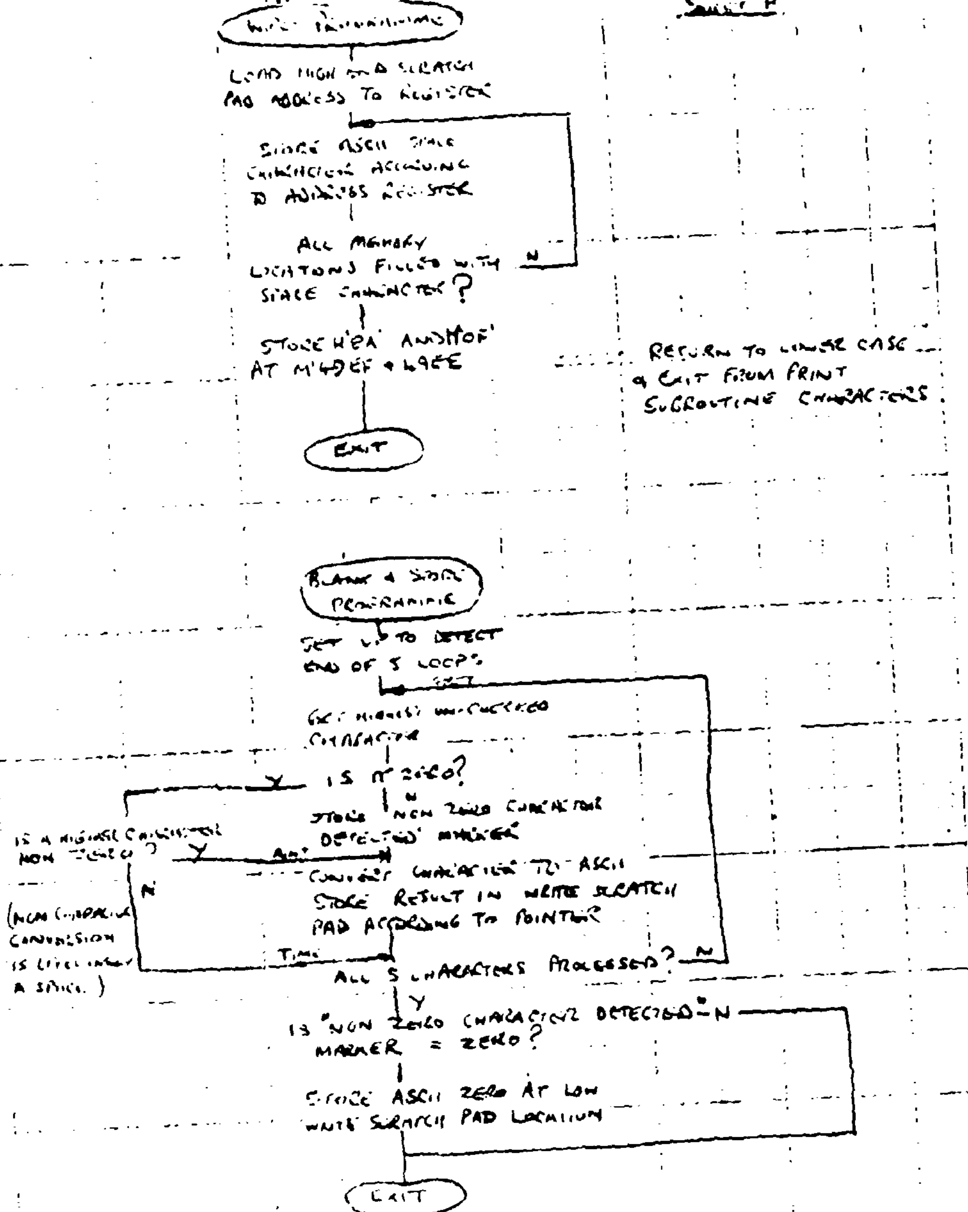
APPENDIX A-11



APPENDIX A-11

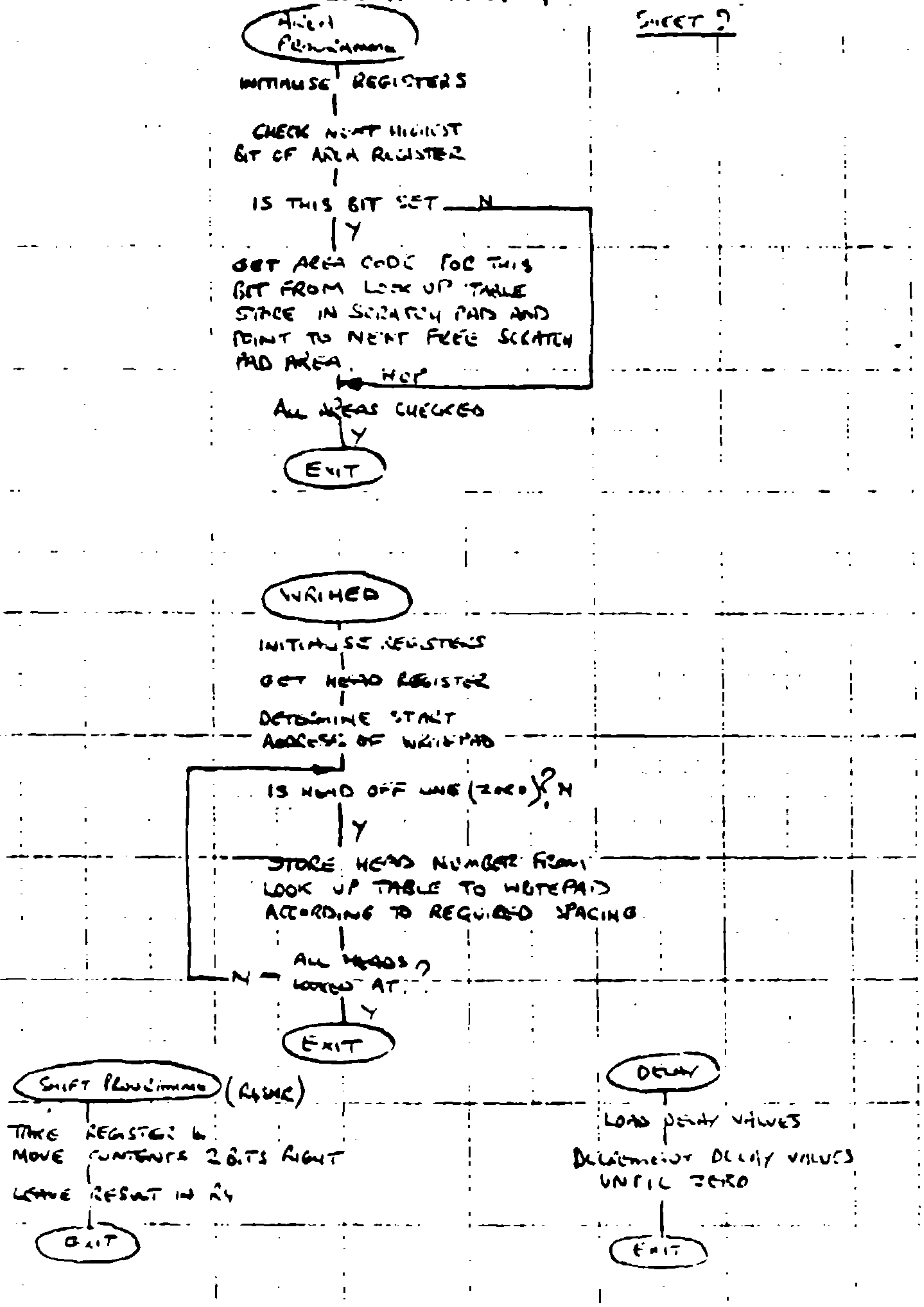


APPENDIX A-11



APPENDIX A-11

SHEET 2



APPENDIX B

OPERATING INSTRUCTIONS

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GRAVINER
ADVANCED FIRE DETECTION
SYSTEM

OPERATION and MAINTENANCE MANUAL
Number MM.055

June 1980 (Revised Oct. 81)

Graviner Limited, Poyle Road, Colnbrook, Slough, SL3 OHB, England
Telephone Colnbrook 3245 Telex 848124

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TABLE OF CONTENTS

1. INTRODUCTION

2. ABRIDGED SPECIFICATION

3. INSTALLATION CHECKS

4. GROUND SUPPORT EQUIPMENT

5. OPERATIONAL PROCEDURES

   Pre-Flight Checks
   Cockpit Check
   In-Flight Operation
   Post-Flight Checks

6. SYSTEM DESCRIPTION

7. MAINTENANCE PROCEDURES

ILLUSTRATIONS

Fig.

1-1 Frontispiece

4-1 Paper Threading
4-2 Main Features of RAM Print-Out
4-3 Cable 4 Connections

5-1 Ground S[illegible]uipment Connections
5-2 Typical [illegible]ts

6-1 Gra[illegible]re Detection System - F111
6-2 Simp[illegible]agram - System A
6-3 Approxima[illegible]ion of Sensors
6-4 Time Sharing
6-5 Front Panel Layout

CHAPTER 1

INTRODUCTION

The Graviner Advanced Fire Detection System uses micro-processor controlled ultra-violet sensors to provide a very high level of detection validity even against a background of bright sunlight.

The equipment is used to detect fires in aircraft engine nacelles, and two systems are provided. System A is mounted on the left side and has dual sensor heads and dual micro-processors to give a high level of 'cross-checking' under fire conditions, and to give continued valid operation even if one or more items in the system fail. System B is mounted on the right side and has single sensor heads and a single micro-processor.

Both systems comprise up to eight detector heads (five installed in F111), a Computer Control Unit (CCU), and share a common Crew Warning Unit (CWU). In addition, a Ground Support Equipment (GSE) is used for pre-flight and post-flight checks.

Features include continuous self-checking of the sensors and the processors plus both a FAULT and a FIRE indicator on the CWU. If self-checks indicate that a system will not be able to satisfactorily indicate a fire, the FAULT indicator illuminates, warning the operator. A FIRE indication will not be given if there is a fault in the system.

FIG. 1-1 UNITS OF EQUIPMENT

CHAPTER 2

ABRIDGED SPECIFICATION

Response	The system indicates a fire when a detector head is exposed to a fire for 1 second or more. Full sunlight falling on the sensor does not affect its sensitivity.
Sensor Failure	System A: Both sensors in a detector head have to fail before a fault warning is given, and if the sensors are part of an adjacent pair, then a fault warning will not be given until all four sensors have failed. System B: A fault warning is only given if the sensor that fails is the only one covering a fire area.
Detector Heads	Each detector is sealed against contamination and can withstand up to +260°C for an indefinite period. The connector has a life expectancy of 1000 hours at this temperature.
Computer Control Unit	Monitors up to eight detector heads continuously and actuates the Crew Warning Unit. Has the ability to bypass faulty sensor inputs and in type A systems to maintain processing using one channel if one of the dual processing systems fail.
Crew Warning Unit	Provides warning lamps and test buttons for use by the aircrew.
Ground Support Equipment	Portable unit to automatically access stored data from the aircraft and to check out the system.
Power Requirements	System A: 102-124V, 380-420Hz at 300mA Max. 16-29V d.c. at 230mA max. for CCU plus 15mA for CWU. System B: 102-124V, 380-420Hz at 150mA max. 16-29V d.c. at 250mA max. for CCU plus 15mA for CWU. GSE: Obtains supplies from aircraft, but 16-29V d.c. at 20mA required for bench recharging of internal battery.

Dimensions and Weight

CCU: 285mm deep, 198mm high, 115m wide nominal (11.1 x 7.8 x 4.5 in.). Weight system A = 3.72kg (8.2 lb), system B = 3.3 kg (6.04 lb).

Head, System A: 105mm wide, 60mm high, 75mm deep (4.2 x 2.4 x 3 in.). Weight = 0.19kg (0.42 lb) each.

Head, System B: 70mm wide, 60mm high, 75mm deep (2.76 x 2.4 x 3 in.). Weight = 0.11kg (0.24 lb) each.

CWU: 146mm wide, 47mm high, 119mm deep (5.75 x 1.85 x 4.7 in.). Weight = 0.65kg (1.37 lb). Unit is shared by both systems.

GSE: 385mm deep, 465mm wide, 377mm high (15.16 x 18.31 x 14.84 in.). Weight = 17.77kg (36 lb) including cables.

CHAPTER 3

INSTALLATION CHECKS

Before replacing the engines in the nacelles, proceed as follows:

(1) Check that the wiring has been carried out according to drawing No. Z22004. Clean each sensor bulb with metal polish. Avoid touching the bulbs after cleaning.

(2) Fit the Crew Warning Unit and the two Computer Control Units into the aircraft. The thicker cable from the aircraft cableform is connected to system A CCU (Part No. 53813-203).

(3) With the aircraft ground power on, switch on the 115V a.c. and 28V d.c. circuit breakers for the equipment. Check that the FAIL indicators on the CWU do not illuminate.

(4) View the detector heads in each engine nacelle and check that the emitters flash every 15 seconds. Check that when the FIRE DET TEST button is pressed on the CWU in the cockpit the emitter flashing rate increases (2 people needed).

(5) Carry out a full check using the Ground Support Equipment as described in 'Pre-Flight Checks' (5-1).

CHAPTER 4

GROUND SUPPORT EQUIPMENT

The GSE is a portable automatic check-out unit for the aircraft equipment. It performs 3 basic functions; it reads out the stored data gathered during the flight, and it checks the operation of the system and identifies which line replaceable unit (LRU) is faulty.

The flight data is stored in RAM's in the CCU and a battery back-up in system B CCU keeps the RAM data refreshed when the aircraft supplies are switched off. To ensure that the RAM data is not lost when the GSE is connected, a refresh battery is contained in the GSE and is connected to the CCU via cable 1. Note that the GSE must always be connected to system A CCU first and that cable 1 must be connected before the aircraft cableform is disconnected from the CCU. The cables are stored in the top cover.

To ensure that the RAM refresh battery in the GSE is fully charged, cable 4 is plugged into cable No. 2 socket and the 28V wires in the cable are connected to a bench 28V supply when the GSE is not in use. The battery should be charged for at least 3 hours prior to use. Before carrying out any tests, always verify that the battery is satisfactory by pressing the GSE BATTERY TEST button and checking that the adjacent indicator illuminates. If the lamp does not illuminate, reconnect the GSE to the 28V bench supply.

Always check the quantity of paper on the printer roll. Red lines on the printer show the roll diameter at which the roll should be changed. To load the paper, refer to fig. 4-1 and proceed as follows:

(1) Open the viewing window by turning the catches and then hinging the window to the right.

(2) Press the Paper Feed Release Button and remove the existing paper.

(3) Insert the paper spindle into a new roll of paper† (Electro-sensitive) and place the spindle into the slots in the Paper Spindle Bracket. The loose end of paper should come off the bottom of the roll and up towards the operator.

(4) Pass the end of the paper down into slot A in the top of the printhead.

(5) Feed the paper into slot A while turning the Paper Advance Thumbwheel towards the rear of the printer. The paper automatically cycles through the printhead and out of slot B.

(6) Hinge the viewing window to the left and latch into position by turning the two catches.

† Replacement part number 19-17210
(United Systems Corp. Dayton, OHIO)

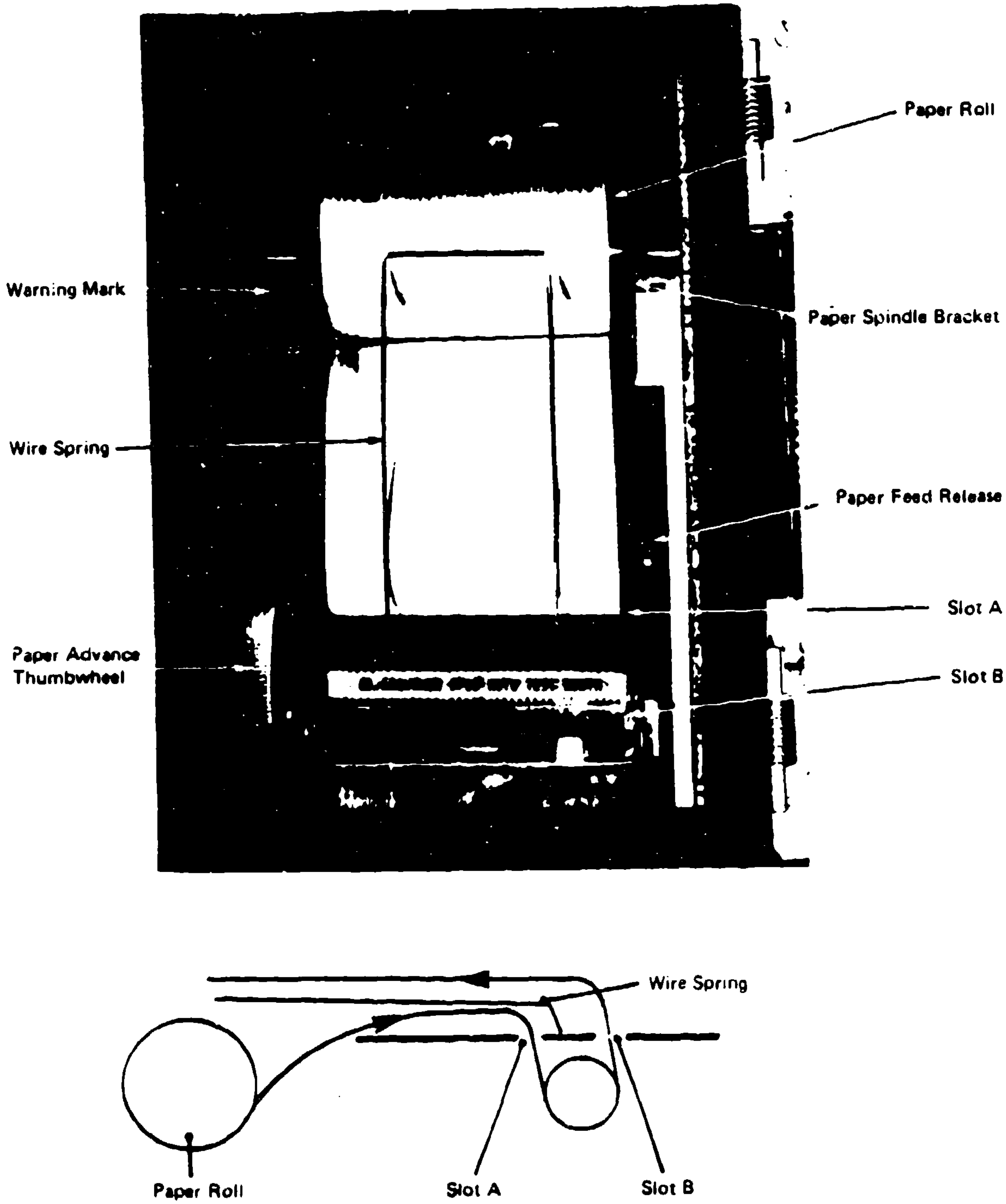


FIG. 4-1 PAPER THREADING

At any time the paper can be pulled through the printer by holding the Paper Feeder Release Button down.

The GSE will only operate fully when the GSE switch is set to IN. When the switch is set to OUT, the inputs and outputs are isolated from the GSE internal circuits. By reconnecting the aircraft cableform to the CCU, normal operation of the aircraft equipment can be obtained with the GSE still connected to the GSE connector on the CCU.

For standard flight testing, the GSE is operated in the AUTO mode. The MANUAL routine selection position of the keyswitch enables each test to be individually selected, as long as certain rules are observed, as follows:

(1) Turn key switch to Manual.

(2) Depress start button.

<u>NOTE</u>: Having printed the opening messages the printer will print:

MANUAL MODE-----------SELECT TEST?----------'X'

(3) Select DATA READ program.
Having read the data printer will print message 'X' again.

(4) Select Control Unit tests.
Having performed and printed results the printer will print message 'X' again.

(5) Select UV Head Tests.
Having performed and printed results the printer will print message 'X' again.

(6) Select Parametric Test.
Having performed and printed results the printer will print message 'X' again.

(7) Select Functional Test.
Having performed and printed results the printer will print message 'X' again.

(8) Select Data Analysis Test.
Having performed and printed results the printer will print message 'X' again.

(9) Power off and disconnect cables as for AUTO MODE if the above tests are not to be repeated.

The four indicators marked '1, 2, 3, 4' provide additional diagnostic information if a fault develops. They are used only when cable 1 of the GSE is connected (the aircraft cable form is connected straight to the CCU), and the GSE switch is set to IN.

INDICATOR	FUNCTION
1 2	Illuminate alternately at the time sharing rate (each on for 167ms) to show that the time sharing is operational.
3 4	Indicator 3 illuminates when side 1 emitter operates (every 15 seconds) and indicator 4 illuminates when side 2 emitter operates.

The main features of the RAM print-out are identified in fig. 4-2.

In addition to its use when recharging the GSE battery, cable 4 has additional connectors which enables it to be used for a bench check-out of system units. The connections are shown in fig. 4-3.

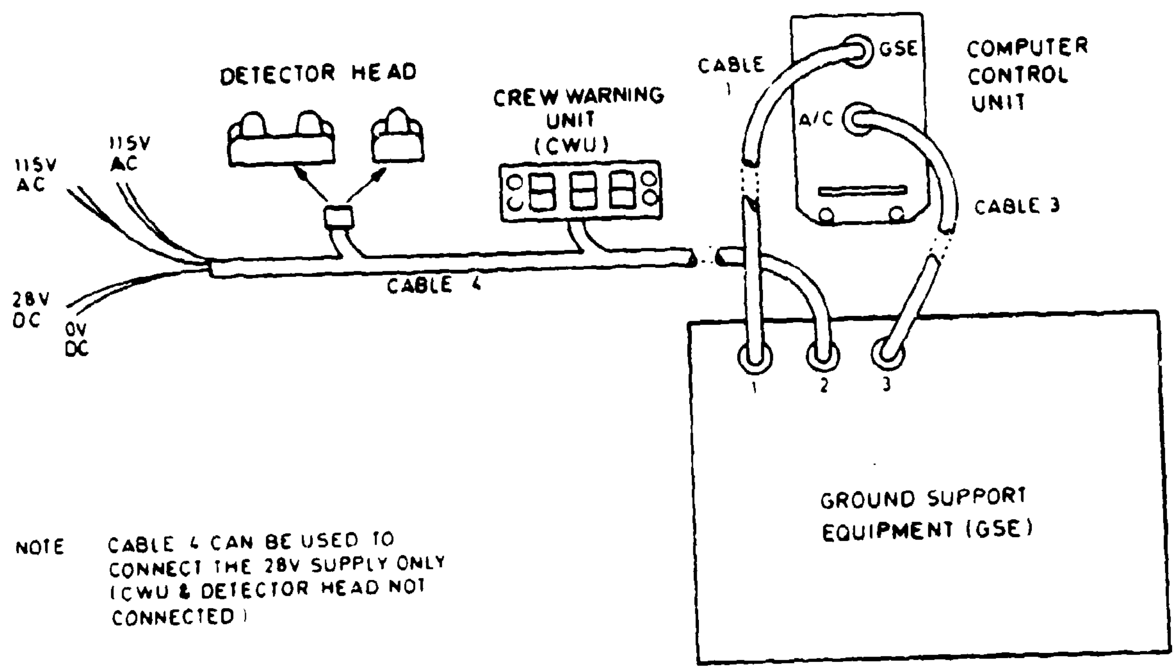


FIG. 4-3 CABLE 4 CONNECTIONS

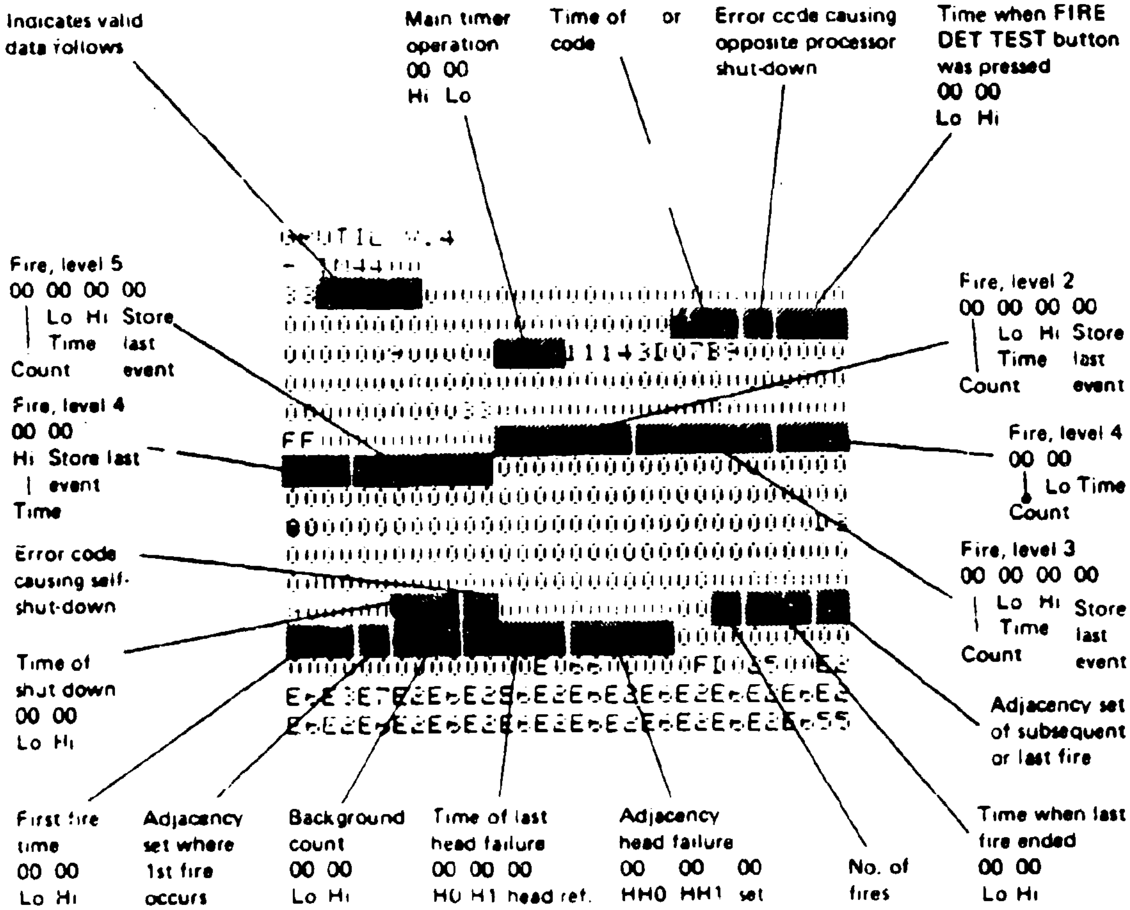


FIG. 4.. MAIN FEATURES OF RAM PRINT-OUT

CHAPTER 5

OPERATIONAL PROCEDURES

1. Pre-Flight Checks

These checks ensure that the equipment is fully functional before a flight test is started. Proceed as follows:

(1) Switch on the aircraft circuit breakers for the engine fire control system and run the equipment on ground power for 30 minutes; this ensures that the RAM refresh bat ries in system B CCU have sufficient charge to hold ed data.

(2) Ensure that the GSE has been on charge for at least 3 hours immediately prior to use. Press the GSE BATTERY TEST button and check that the adjacent indicator illuminates (GSE refresh battery is charged). Check that there is sufficient paper on the printer paper roll. If necessary, replace the roll (see Chapter 4).

(3) Connect the GSE to the CCU of system A (Part No. 53813-203), starting with cable 1 and then connecting as shown in fig. 5-1.

WARNING: WHEN THE AIRCRAFT PLUG IS REMOVED FROM THE CCU, AC POWER IS PRESENT ON THE EXPOSED CONNECTIONS OF THE AIRCRAFT PLUG.

(4) On the GSE set the POWER switch to ON and check that 115v side 1 and 115v side2 power rail indicators illuminate, noting that with system B only side 1 indicator will illuminate. Set the GSE switch to IN, ensure that the AUTO/MANUAL keyswitch is at AUTO and press the START PROGRAM button. The flight data print-out will be meaningless but will show how many good detector heads are available. Verify that there are no equipment faults indicated on the rest of the print-out.

(5) Reconnect the aircraft cableform to the CCU of system A and repeat the connections and checks of (3) and (4) above for the CCU of system B (Part No. 53813-204).

2. Cockpit Check

With the equipment power on, the following checks must be made prior to a test flight:

(1) Press the FAIL IND TEST button on the Crew Warning Unit (CWU) and check that the left and right FIRE DET FAIL indicators illuminate.

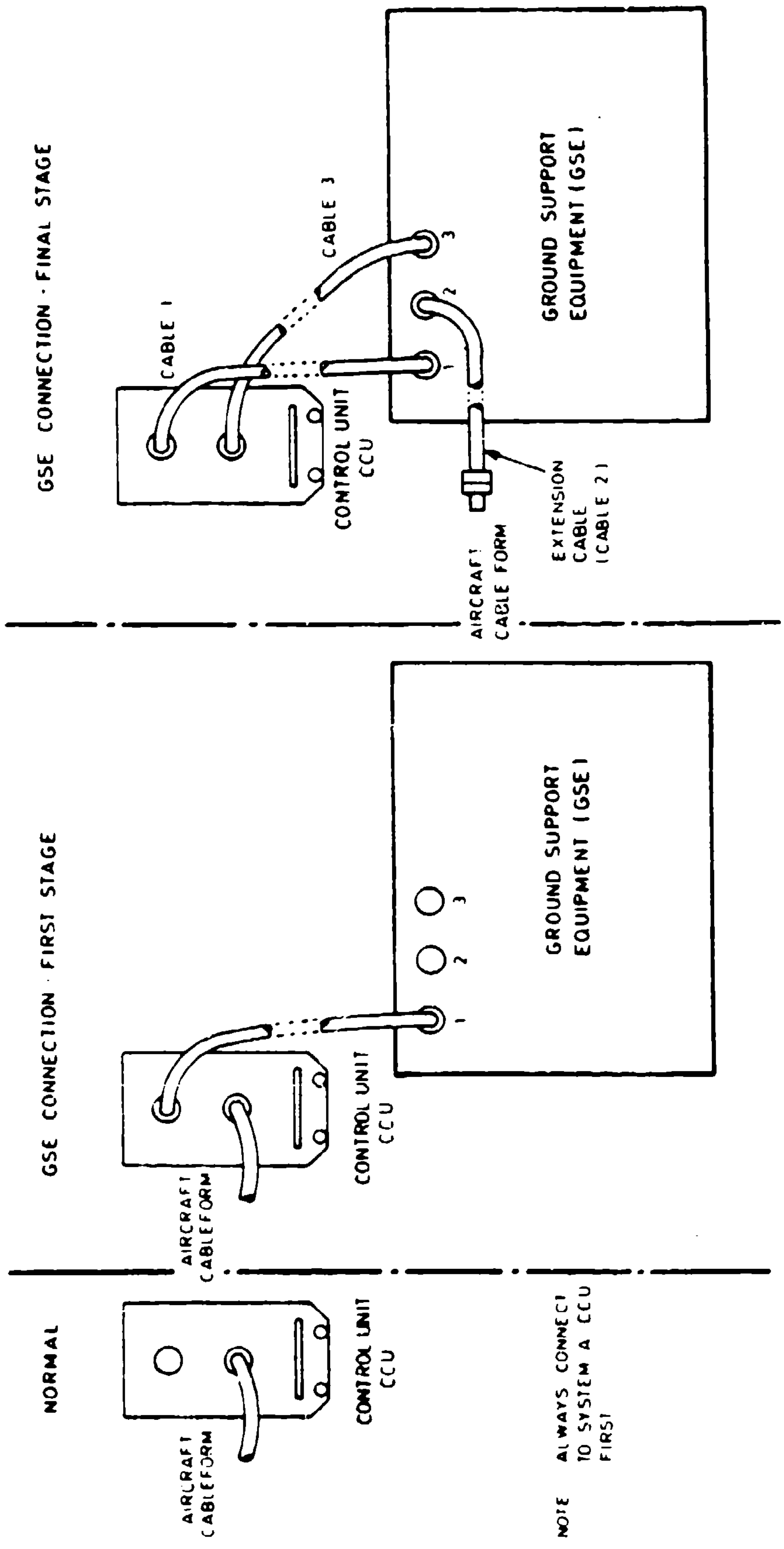


FIG. 5-1 GROUND SUPPORT EQUIPMENT CONNECTIONS

(2) Press the FIRE DET TEST button and record the time at which it was pressed. Check that the left and right FIRE indicators illuminate.

NOTE: The FIRE DET TEST button can be pressed at any time during a flight to check the circuit but the time at which the button is pressed must be recorded on every occasion. This provides the datum time for the stored flight data.

3. In-Flight Operation

If a fire occurs during the flight, the appropriate FIRE button will illuminate (LEFT or RIGHT).

For future analysis, the equipment records the time and sensor inputs for all fire or 'near-fire' events in relation to the time when the FIRE DET TEST button was last pressed.

4. Post-Flight Checks

CAUTION: THE FOLLOWING CHECKS MUST BE CARRIED OUT WITHIN A FEW HOURS OF THE AIRCRAFT LANDING. THE TIME IS DETERMINED BY THE CHARGE ON AN INTERNAL BATTERY; IF THE BATTERY DISCHARGES BEFORE THE CHECKS TAKE PLACE, ALL THE FLIGHT DATA WILL BE LOST. WITH A FULLY CHARGED BATTERY THE DATA WILL BE HELD FOR UP TO 8 HOURS BUT FOR SAFETY IT IS RECOMMENDED THAT THE CHECKS ARE MADE WITHIN 2 HOURS OF LANDING.

Proceed as follows:

(1) Remove power from Fire Detection System as follows:-
(a) Break CCU/CWU 28V DC Breaker
(b) Break AC system A or system B Breakers as appropriate
NOTE: System A has two AC Breakers

(2) Ensure that the GSE has been on charge for at least 3 hours immediately prior to use. Press the GSE BATTERY TEST button and check that the adjacent indicator illuminates (GSE refresh battery is charged). Check that there is sufficient paper on the printer paper roll. If necessary, replace the roll (see Chapter 4). Set the GSE switch to IN, ensure that the AUTO/MANUAL keyswitch is at AUTO, and that the POWER switch is OFF.

NOTE: There is an instruction label on the GSE giving connection and operating information.

(3) Connect cable 1 from GSE socket 1 to the GSE plug on the CCU of system A (Part No. 53813-203).

CAUTION: TO ENSURE THAT THE STORED DATA IS NOT LOST, SYSTEM 'A' CCU MUST ALWAYS BE CHECKED BEFORE SYSTEM 'B', AND CABLE 1 MUST ALWAYS BE CONNECTED BEFORE THE AIRCRAFT CABLEFORM IS DISCONNECTED FROM THE CCU.

(4) Complete the connections between the GSE and CCU as shown in fig. 5-1. Note that the aircraft cableform to system A CCU is thicker than that to system B CCU. Make AC Breakers followed by DC Circuit Breakers.

(5) On the GSE set the POWER switch to ON and check that the adjacent power rail indicators illuminate, noting that with system B only one 115V indicator will illuminate (not side 2). If the indicators do not illuminate check the aircraft circuit breakers.

(6) Press the START PROGRAM button. The GSE will start to print out the stored RAM data. There are two tables of data from system A and one from system B. After the RAM data the GSE will perform a series of tests. If the tests are satisfactory an appropriate print-out will result. If a fault is present, the print-out will indicate which LRU should be replaced. Typical print-outs are shown in fig. 5-2. Total test run time in automatic mode is typically 7½ minutes.

(7) On the CWU (cockpit) press the FIRE DET TEST and then the FAIL IND TEST buttons. Check that the appropriate indicators illuminate.

(8) When the checks on system A have been completed satisfactorily, disconnect the aircraft cableform from the GSE extension cable and reconnect it securely to the A/C PLUG on system A CCU. Disconnect the GSE PLUG cable (cable 1) from system A CCU.

(9) Repeat procedures (2) to (8) for system B (Part No. 53813-204).

(10) After checking and carefully reconnecting both units, carry out a cockpit check of the CWU to ensure that the connections are satisfactory.

Note. System B may be checked out in isolation by carrying out procedures (2) to (8) for system B only, however data retained in system A will be lost.

```
GD/GRAVINER DFDS AUTO TEST ROUTN

----------------
SYSTEM A
MANUAL MODE
SELECT TEST

---------------
GD/GRAVINER DFDS AUTO TEST ROUTN

----------------
SYSTEM A
MANUAL MODE
SELECT TEST
----------------
START READ CCU TEST

GRUTIL V. 4
->!M4400
33A5A5A5000000000000000000000000
00000000000000000000000000000000
8F0000950400000426293A0513000000
00000000000000000000000000000000
008F008E0E3E00000000000000000000
FF8F8F8F00000004008F7D04000F0301
008F00000000008F0000000000000000
00000000000000000000000000000000
00000000000000000000000000AE5D03
00000000000000000000000000000000
00000000000000000000000000000000
00000000000000004000000001040000
0200D071020:008F00000000000000F
0F8F8FFFD00000E066000000FD0250E2
E6E30055555555555555555555555555
55555555555555555555555555555555
```

```
->
GRUTIL V. 4
->!M4400
33A5A5A5000000000000000000000000
00000000000000000000000000000000
0000010504010004262A3A05CC000000
00000000000000000000000000000000
00000000FF1E00000000000000000000
FF8F000000007F04000F7C04000F0301
008F0000000000000000000000000000
00000000000000000000000000000000
000000000000000000000000000D0059
00000000000000000000000000000000
00000000000000000000000000000000
00000000000000008F02000001040000
020000140002000000000000F8F8F00
000000FF000D000E06600000FD0250E0
E4E1E5E0E4E0E4E0E4E0E4E0E4E0E4E1
E5E1E5E1E5E1E5E0E4E0E4E0E4E1E555

->READ CCU TEST COMP
MANUAL MODE
SELECT TEST
----------------
START CONTROL UNIT TESTS
GRAVNER DFDS
F-111 CONFIRMED
0101000001000000
REPLACE CCU
CONTROL UNIT TESTS COMPLETE
MANUAL MODE
SELECT TEST
----------------
```

```
START UV-HEAD TEST
SIDE 1
UV-HEAD 1 1346
UV-HEAD 2 1359
UV-HEAD 3 1134
UV-HEAD 4 0000
UV-HEAD 5 1325

SIDE 2
UV-HEAD 1 0000
UV-HEAD 2 0876
UV-HEAD 3 0000
UV-HEAD 4 0000
UV-HEAD 5 0869

UV-HEAD TEST COMP
MANUAL MODE
SELECT TEST
```

FIG. 5-2 TYPICAL GSE PRINT-OUTS

CHAPTER 6

SYSTEM DESCRIPTION

The units of the system are shown in fig. 6-1, and a simple block diagram in fig. 6-2.

1. Sensors

The sensors used are Graviner developed units which give a signal when exposed to ultra-violet (UV) radiation at frequencies below those in solar radiation; hence they discriminate against sunlight. Within the operating spectrum of the sensor there is still sufficient UV radiation from the flames.

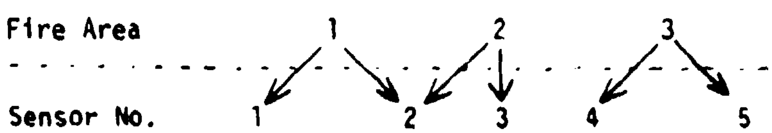
When the sensor operates, an avalanche action occurs and the increase in current is detected at the Computer Control Unit (CCU). The 320V sensor supply is then switched off to allow the sensor to recover, and then switched on again. If the UV sensor avalanches four times or more in three successive 167ms gating periods then a fire condition is computed.

In the dual system (system A), two sensors are mounted on each detector head and are controlled in a time-share arrangement. A fire condition will only be computed if both sensors avalanche four times or more in each of three successive gating periods per side.

In certain parts of the installation two detector heads view the same area. This is termed adjacency, and the processor checks that all sensors covering a particular area give a similar output under fire conditions. The heads which provide adjacency outputs are given in Table 6-1. The outputs of both sides of a detector head and adjacent heads are fed via an AND system to give the greatest certainty of a fire condition. If a fault condition exists in any sensor, the output will change to an OR system so that valid fire warnings will still be given even when up to three of the four sensors (two system A detector heads) covering an area fail. The approximate positions of the sensors in the engine nacelle is shown in fig. 6-3.

TABLE 6-1

ADJACENCY



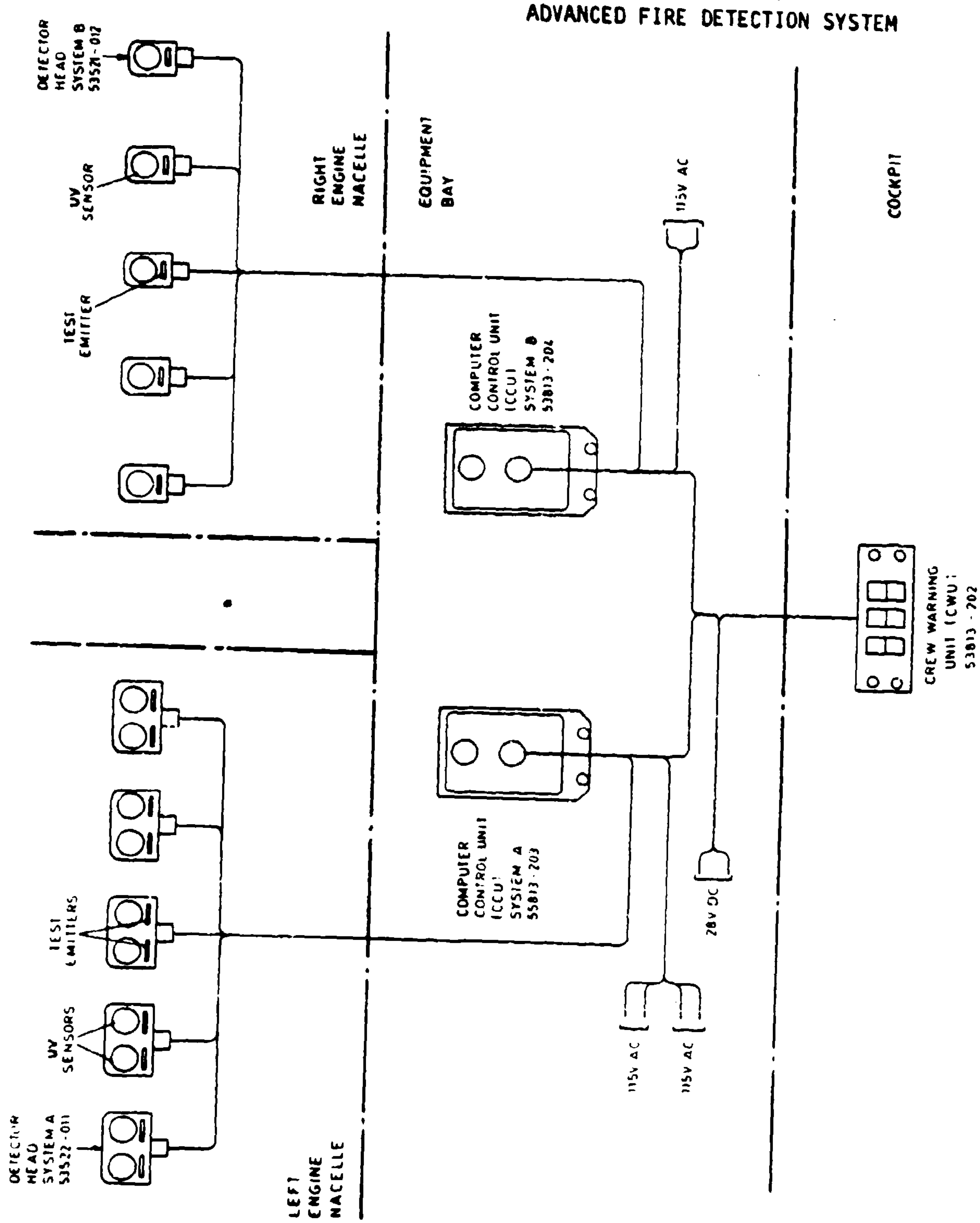


FIG. 6-1 GRAVINER ADVANCED FIRE DETECTION SYSTEM – F111

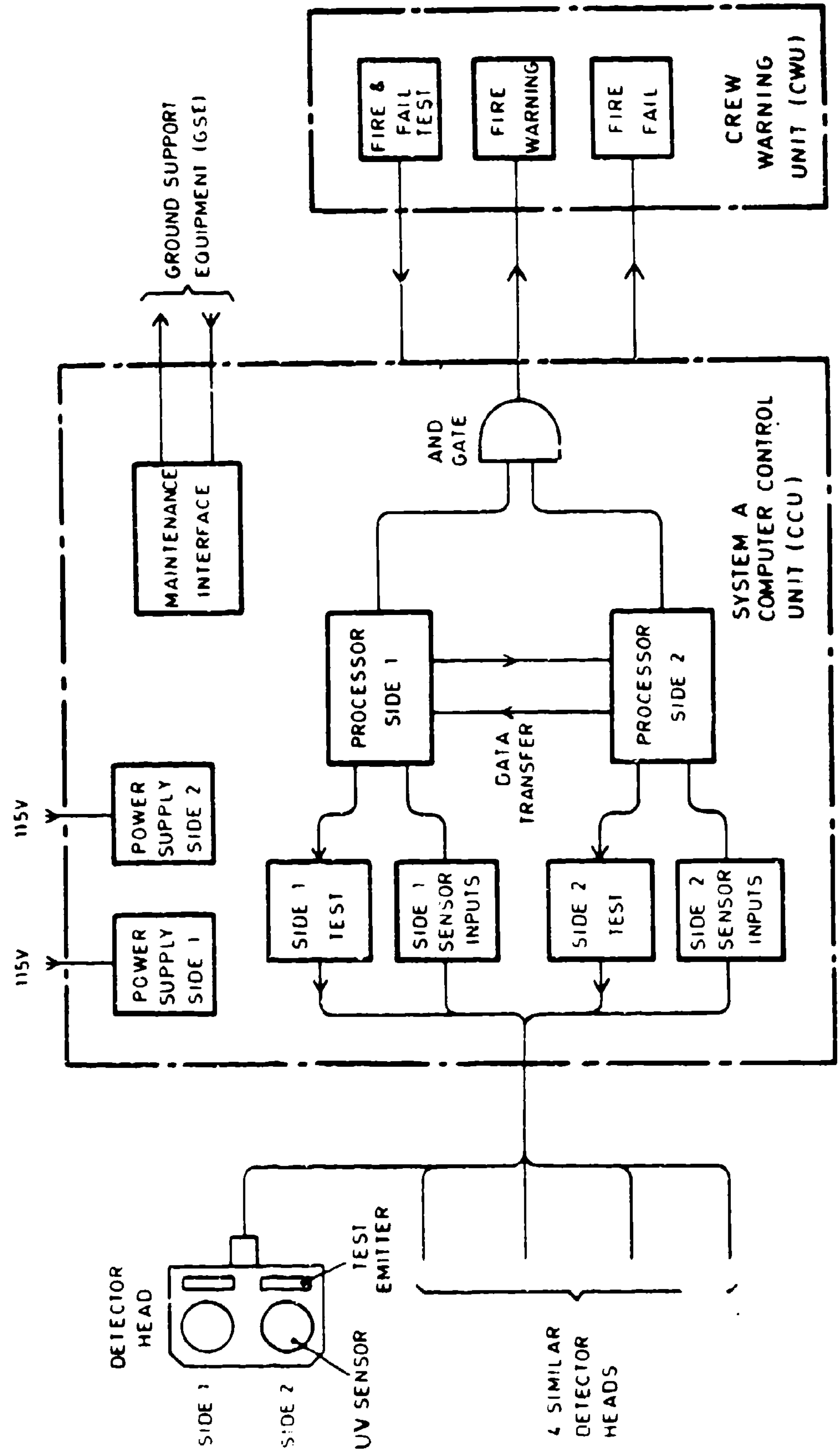


FIG. 6-2 SIMPLIFIED BLOCK DIAGRAM – SYSTEM A

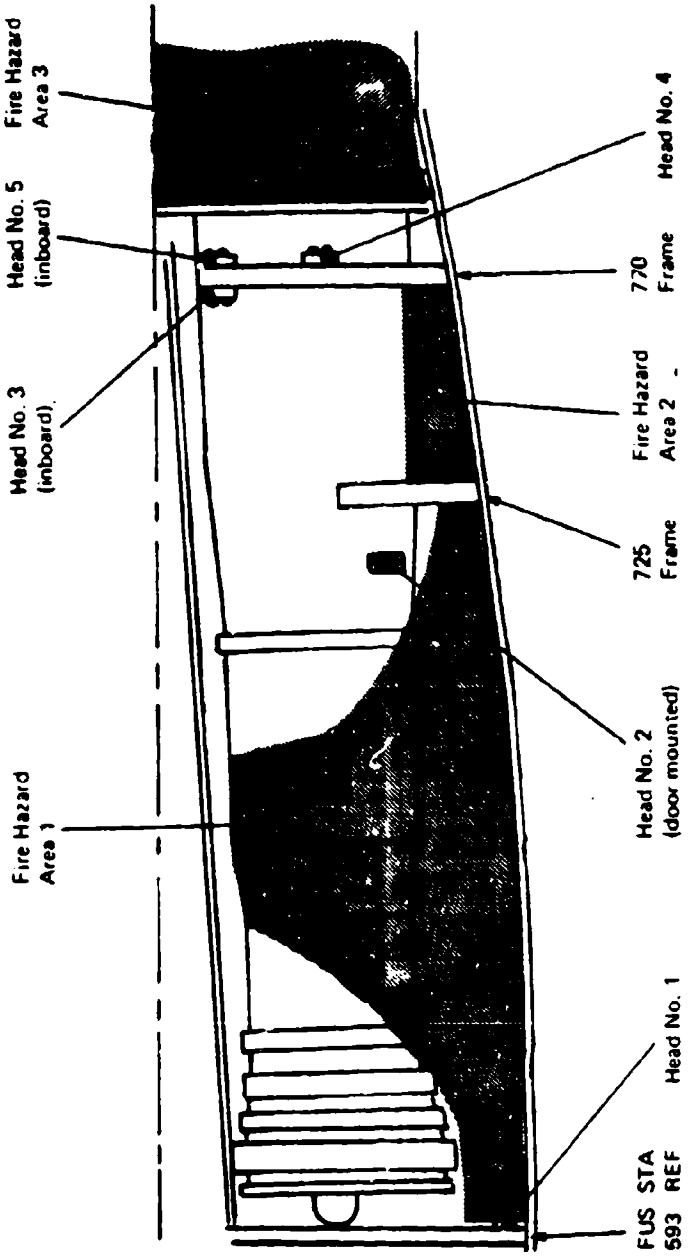


FIG. 6-3 APPROXIMATE POSITION OF SENSORS

To ensure that the sensors are operating correctly, each has an adjacent UV emitter which is activated every 15 secs while the equipment is operating. In system A, the side 1 emitters are energised simultaneously and the processor checks the output from every side 1 sensor. The side 2 emitters are then energised and the processor checks every side 2 sensor. If a sensor is found to be faulty, the processor arranges to disregard its output when computing a fire condition.

2. Computer Control Unit (System A)

The CCU contains two microprocessor systems each with their own power supplies. Each processor controls one sensor in every dual detector head but each is interconnected so that the fault status of the sensors, the processors themselves, and the associated electronics can be verified. The power supplies are completely separate so that if one fails half the system is still available to detect fires.

The CCU operates in a continuous series of 167ms periods, as indicated in fig. 6-4.

A random access memory (RAM) keeps a record of all sensor 'counts' (number of gate periods in which 4 or more avalanches took place), sensor and processor status, etc. To retain the information when the aircraft supplies are switched off, a rechargeable RAM refresh battery is contained in the CCU of system B which supplies the two RAM's in system A and the one in the system B CCU.

3. Computer Control Unit (System B)

The CCU contains a single microprocessor only. However, it will take note of adjacency conditions (table 6-1). The same self-checking facilities are incorporated as in system A.

4. Crew Warning Unit

The CWU has FIRE and FAULT indicators for two installations (system A, LEFT engine and system B, RIGHT engine). In addition, it has test buttons for both the FIRE and FAULT indicator circuits.

5. Ground Support Equipment

The GSE is connected into the aircraft system by cables. It provides an automatic print-out of the RAM contents so that the time of a fire, the number of fires, etc, can be quickly ascertained. The RAM also provides a mass of other data which will be used as an aid to future designs. The GSE is also used to give a comprehensive check-out of the aircraft equipment. These include a CCU test, a sensor test, a parametric test (power supplies, etc), a functional test, and finally a data analysis. The print-out indicates when tests are satisfactory and also identifies failures down to LRU level.

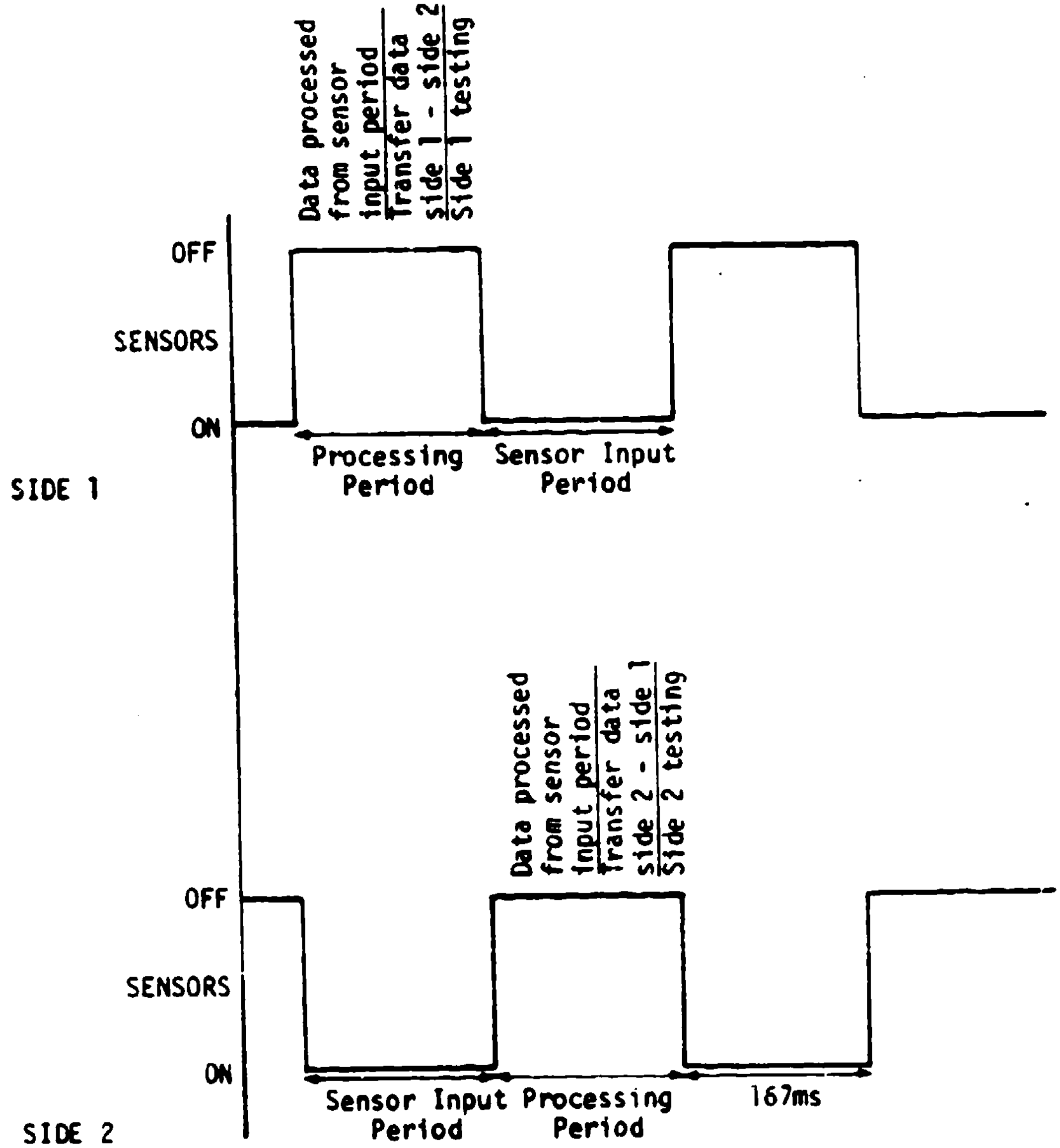


FIG. 6-4 TIME SHARING

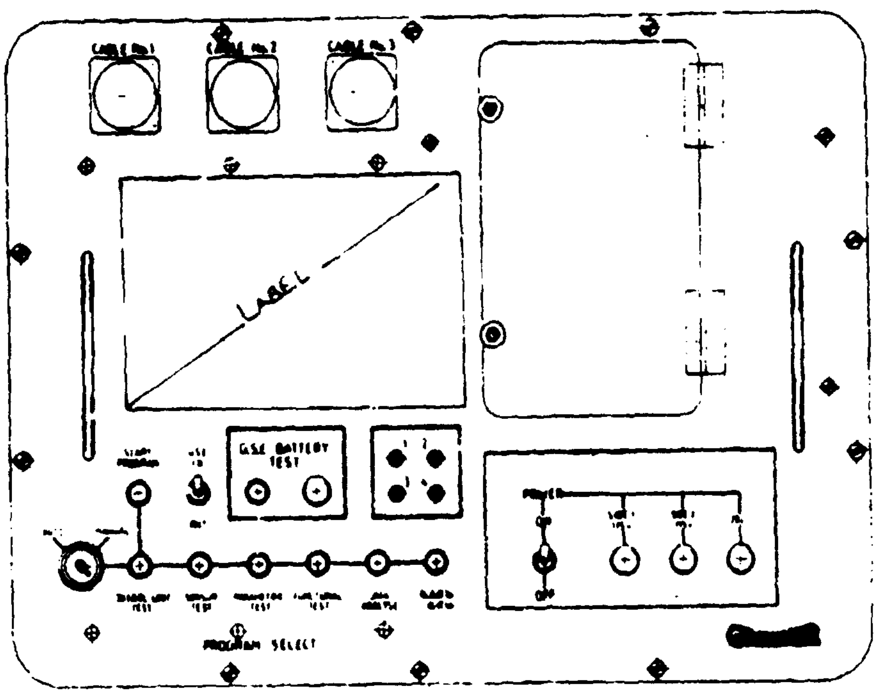


FIG.6-5 FRONT PANEL LAYOUT.

CHAPTER 7

MAINTENANCE

1. Detector Heads

Each time that an engine is removed from the aircraft, inspect and clean all the detector heads (both sensors and emitters) in that nacelle with metal polish.

If a sensor fault is indicated, before replacing the appropriate detector head, check for cleanliness. When a head has been either cleaned or replaced, repeat the GSE check to ensure that the sensor is operational and there is no wiring fault.

After 1000 flying hours, the detector heads should be replaced.

2. Crew Warning Unit

Replace the indicator lamps in the CWU periodically according to the aircraft maintenance schedule.

3. Ground Support Equipment

If the battery test indicator does not illuminate when the button is pressed and the GSE has just been on charge, check the battery indicator.

Periodically connect one end of cable 4 to cable No. 2 socket and the appropriate wires at the other end to 115V a.c. and 28V d.c. bench supplies. Set the POWER switch to ON and check that the appropriate indicators illuminate.

A partial indication that Ground Support Equipment is functional may be obtained by pressing and releasing the start program button on the GSE front panel.

The printer should respond with the message;

SYSTEM B
NO GSE - CCU PATH
CHECK CABLE 1 or REPLACE CCU
TEST ABORT.

END-7-83