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A SPICE2 MODEL FOR THE M732 ANALOG TIMER INTEGRATED CIRCUIT

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The development of a SPICE2 circuit model for the M732 analog timer integrated circuit (Motorola SC25362PH-7749) is described. Overall circuit operation, timer model usage and a comparison of model and hardware measured results are also presented.

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INTRODUCTION

The development of a computer model for the 11720574 analog timer integrated circuit is described in this report and is part of an overall project to model select components of the M732 proximity fuze.

The SPICE2 circuit analysis program is used in conjunction with the Gummel-Poon bipolar transistor model to simulate timer operation and offer a method of evaluating proposed circuit modifications. Semiconductor model parameter approximations, resistor value determinations, and SPICE2 program input are discussed. Overall circuit operation, timer model usage, and a comparison of model and hardware measured results are also presented.

M732 TIMER INTEGRATED CIRCUIT COMPONENT DETERMINATIONS

Transistor Model Parameter Approximations

The SPICE2 circuit analysis program provides for the use of a bipolar junction transistor model developed by H. K. Gummel and H. C. Poon (ref 1). It is an integral charge control model and includes high injection effects. A list of the parameters used by the model appears in table 1 (ref 2). The methods used to determine only those parameters for which there was available data from which to make calculations are described in this report. All other parameters are set to typical values suggested by the SPICE2 program.

Parameter determination begins with a mathematical description of model behavior in the forward active region. Equations 1 and 2 represent expressions for d.c. collector current and d.c. base current, respectively (ref 3).

$$I_c = \frac{I_s}{Q_B} \left\{ EXP \left(\frac{V_{be}}{V_T} \right) - 1 \right\} \tag{1}$$

$$I_B = \frac{I_s}{B_F} \left\{ EXP \left(\frac{V_{be}}{V_T} \right) - 1 \right\} + C_2 I_s \left\{ EXP \left(\frac{V_{be}}{N_e V_T} \right) - 1 \right\} \tag{2}$$

They are expressed in terms of the NPN transistor model parameters listed in table 1, base-to-emitter capacitor voltage (V_{be}), normalized base charge (Q_B), and thermal voltage (V_T). V_T is defined as

$$V_T = \frac{kT}{q}$$

where k is Boltzmann's constant, q is the charge of an electron, and T is the junction temperature in kelvins. Variable Q_B is defined by the following equations (ref 3):

1

$$Q_1 = 1 + \frac{V_{bc}}{V_a} + \frac{V_{be}}{V_B} \tag{3}$$

$$Q_2 = \frac{I_s}{I_k} \left\{ EXP \left(\frac{V_{be}}{V_T} \right) - 1 \right\} + \frac{I_s}{I_{KR}} \left\{ EXP \left(\frac{V_{bc}}{V_T} \right) - 1 \right\} \tag{4}$$

$$Q_B = \frac{Q_1}{2} \left\{ 1 + (1 + 4 Q_2)^{1/2} \right\} \tag{5}$$

Variable V_{bc} represents the transistor's base to collector capacitor voltage. Equations 1 and 2 are approximations to more general equations but can be assumed to be valid within the forward active region. The general model and its associated expressions appear in appendix A, but parameter approximations are based on equations 1 through 5, and the test data in tables 2 and 3. The data in tables 2 and 3 reflects transistor and resistor values typical of the manufacturing process used to fabricate the M732 timer integrated circuit.* The data should not be misconstrued as being the result of a probing of the M732 timer chip by the author.

By neglecting losses due to bulk resistance, a value for saturation current, I_s, can be determined from device data measured at a collector current of 50 µA. A value for Q_1 must first be calculated from equation 3 as follows:

$$Q_1 = 1 - \frac{4.353}{200} + \frac{0.647}{200}$$

$$Q_1 = 0.981$$

Solving for Q_2 from equation 4,

$$Q_2 = \frac{I_s}{0.01} \left\{ EXP \left(\frac{0.647}{0.02575} \right) - 1 \right\} + \frac{I_s}{0.1} \left\{ EXP \left(\frac{-4.353}{0.02575} \right) - 1 \right\}$$

$$Q_2 = (8.169 \times 10^{12}) \, I_s$$

An expression for Q_B can now be developed by using Q_1 and Q_2 to solve equation 5. Substitution yields the following:

$$Q_B = \frac{0.981}{2} \left\{ 1 + \left[1 + (4) (8.169 \times 10^{12}) \, I_s \right]^{1/2} \right\}$$

By substituting for Q_B in equation 1, and setting I_c equal to 50 µA, the following value for saturation current can be obtained:

---

* The data in tables 2 and 3 was obtained via telephone conversations with Paul Daniels and Tony Alvarez of Motorola Inc., Phoenix, AZ.

$$50 \times 10^{-6} = \frac{I_s \left\{ \text{EXP} \left(\frac{0.647}{0.02575} \right) - 1 \right\}}{\frac{0.981}{2} \left\{ 1 + (1 + (4)(8.169 \times 10^{12}) I_s)^{1/2} \right\}}$$

$$I_s = 6 \times 10^{-16} \text{ A}$$

Values for the forward nonideal base current coefficient, C_2, and the non-ideal base to emitter emission coefficient, N_e, are determined from equation 2 and the above calculated value for I_s. Solving for C_2

$$C_2 = \frac{I_B - \frac{I_s}{\beta_F} \left\{ \text{EXP} \left(\frac{V_{be}}{V_T} \right) - 1 \right\}}{I_s \left\{ \text{EXP} \left(\frac{V_{be}}{N_e V_T} \right) - 1 \right\}} \qquad (6)$$

In equation 6, base current, I_B, is calculated on the basis of the data in table 2 at a collector current of 50 μAas follows:

$$I_B = \frac{I_c}{\beta} = \frac{50 \times 10^{-6}}{75}$$

$$I_B = 0.667 \times 10^{-6} \text{ A}$$

Other values are obtained directly from the data in tables 1 and 2. Value substitution yields the following expression for C_2 in terms of N_e:

$$C_2 = \frac{0.667 \times 10^{-6} - \frac{6 \times 10^{-16}}{100} \left\{ \text{EXP} \left(\frac{0.647}{0.02575} \right) - 1 \right\}}{6 \times 10^{-16} \left\{ \text{EXP} \left(\frac{0.647}{V_T N_e} \right) - 1 \right\}}$$

$$C_2 = \frac{2.95 \times 10^8}{\text{EXP} \left(\frac{0.647}{V_T N_e} \right)} \qquad (7)$$

An approximate value for N_e can be obtained by substituting equation 7 for C_2 in equation 2 and solving for N_e at a base to emitter capacitor voltage of 0.731 V. Rewriting equation 2

$$\frac{I_B - \frac{I_s}{\beta_F} \left\{ \text{EXP} \left(\frac{V_{be}}{V_T} \right) 1 \right\}}{2.95 \times 10^8 I_s} = \frac{\text{EXP} \left(\frac{V_{be}}{V_T N_e} \right) - 1}{\text{EXP} \left(\frac{0.647}{V_T N_e} \right)} \qquad (8)$$

3

By assuming that EXP $(V_{be}/V_T N_e)$ and EXP (V_{be}/V_T) are both much greater than one, an expression for N_e can be obtained by taking the natural logarithm of both sides of equation 8 and solving for N_e as follows:

$$N_e = \frac{V_{be} - 0.647}{\ln \left[\frac{I_B - \frac{I_s}{\beta_F} \{ EXP (\frac{V_{be}}{V_T}) - 1 \}}{2.95 \times 10^8 \, I_s} \right] V_T} \qquad (9)$$

The value for I_B in equation 9 is determined by neglecting losses due to bulk resistance and dividing equation 1 by β, as follows:

$$I_B = \frac{I_c}{\beta} = \frac{I_s}{Q_B \, \beta} \{ EXP (\frac{V_{be}}{V_T}) - 1 \} \qquad (10)$$

But before a value for I_B can be calculated, the magnitude of Q_B must be determined at a base-to-emitter capacitor voltage (V_{be}) of 0.731 V. Solving for Q_B from equations 3 through 5

$$Q_1 = 1 - \frac{4.269}{200} + \frac{0.731}{200} = 0.982$$

$$Q_2 = (\frac{6 \times 10^{-16}}{1 \times 10^{-2}}) \, EXP (\frac{0.731}{0.02575}) = 0.128$$

yielding

$$Q_B = \frac{0.982}{2} \{ 1 + (1 + 0.512)^{1/2} \} = 1.096$$

A substitution for Q_B in equation 10 yields the following value for I_B:

$$I_B = \frac{6 \times 10^{-16}}{(1.096) \, (85)} \{ EXP (\frac{0.731}{0.02575}) - 1 \}$$

$$I_B = 13.74 \ \mu A$$

Value substitutions for I_S, C_2, I_B, and V_{be} in equation 9 yield the following value for N_e:

$$N_e = \frac{0.731 - 0.647}{\ln \left(\frac{13.74 \times 10^{-6} - \frac{6 \times 10^{-16}}{100} \{ EXP (\frac{0.731}{0.02575}) - 1 \}}{2.95 \times 10^8 \times 6 \times 10^{-16}} \right) \times 0.02575}$$

$$N_e = 1.95$$

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By substituting for N_e in equation 7, a value for C_2 can be calculated as follows:

$$C_2 = \frac{2.95 \times 10^8}{\text{EXP} \left\{ \frac{0.647}{(0.02575)(1.95)} \right\}}$$

$$C_2 \approx 750$$

Since the data in table 3 defines junction capacitance in terms of farads per unit area, a value for junction surface area must be obtained before capacitance can be calculated. Figure 1 represents an example of an integrated bipolar transistor. The surface area of one of its junctions is composed primarily of the deposited region's lower surface. Values of length and width needed for the calculation of this area are obtained from a microscopic photograph of the physical device's top view. Emitter junction length (L) and width (W) define the emitter deposited region's lower surface area as follows:

$$A_L = (L)(W)$$

$$A_L = (1.87 \times 10^{-5})^2 m^2$$

$$A_L = 3.5 \times 10^{-10} m^2$$

Surface area due to the depth of the diffusion is determined by

$$A_D = (2)(L)(D) + (2)(W)(D)$$

$$A_D = (4)(2.5 \times 10^{-6} m)(1.87 \times 10^{-5} m)$$

$$A_D = 1.87 \times 10^{-10} m^2$$

By summing these areas and multiplying by the capacitance per unit area, a value for base-to-emitter junction capacitance can be expressed as follows:

$$C = C_o (A_L + A_D)$$

$$C = 4.65 \times 10^8 \text{ pF/m}^2 \left\{ 3.5 \times 10^{-10} m^2 + 1.87 \times 10^{-10} m^2 \right\}$$

$$C = 0.25 \text{ pF}$$

Base to collector capacitance and collector substrate capacitance are also approximated at a value of 0.25 pF. Typical values were assumed for the other model parameters listed in table 1. PNP transistor data of the type used to calculate NPN behavior was unavailable. As a result, PNP transistor parameters were assumed equal to NPN parameters.

A comparison between device measured data and transistor model results appears in table 4. Differences in current gain and collector current are primarily the result of an underestimation of bulk resistance values. Such a difference, however, does not malign model accuracy since device-supplied data

was characterized as typical and subject to variations in gain much greater than those experienced with the model. The "used" column in table 1 reflects the final list of parameter values used to model the M732 timer's NPN and PNP bipolar transistors. A list of the SPICE2 input data used to generate the model results of table 4 appears in appendix B.

Diode Model Description and Resistor Value Determinations

Diode model parameters were specified with the same values as those calculated for a transistor. Other values were approximated by typical values. A list of diode parameters appears in table 5 (ref 2).

Zenar diodes were modeled by a voltage source and series connected diode. They were connected in such a way as to prevent a flow of current from the source. A value of 5.9 V was assigned to the voltage source making the voltage drop across the series combination equal to approximately 6.6 volts.

Resistor values were determined from the data in table 3, the Specification control drawing (SCD) schematic for the M732 timer circuit (fig. 2) (ref 4), and a microscopic photograph of the physical device. Resistive lengths were measured, divided by their widths, and multiplied by a factor expressed in ohms per square area. A factor of 125 Ω/square was used in determining the resistance values of those components indicated in figure 2 as not being ion-implanted. Ion-implanted components were calculated using a factor of 1 Ω/square. Components Cl, RT, RA, RB, and C4 (fig. 2) represent discrete components external to the M732 timer integrated circuit. All other parameters are part of the IC.

SPICE 2 PROGRAM INPUT

Circuit Layout

Two types of data comprise the input necessary for a SPICE2 simulation. The first type describes circuit layout and the second type specifies simulation control. Circuit layout is the more important and begins with a node and component labeled schematic of the circuit to be modeled. The M732 timer circuit (fig. 3) represents such a schematic and allows card input to be properly prepared for submission to the program. SPICE2 component input basically consists of a component name, a description of nodal connections, and a component descriptor or value.

In the case of a transistor, the component name must start with the letter Q and be no more than eight characters long. Nodal connections must be listed in the order of collector, base and emitter. The transistor's component descriptor is a name which points the program to a set of user defined parameters describing the transistor's characteristics. The characteristics are specified on a card known as a .MODEL card. The card is of a general format and is used to describe a number of different semiconductors. A transistor component card and its

corresponding .MODEL card appear as follows:

```
QXXX N1 N2 N3 MNAME AF
.MODEL MNAME TYPE (PNAME1=PVAL1 PNAME2=PVAL2 etc)
```

In the above example, MNAME acts as a link between the semiconductor character-istics listed on the .MODEL card and the circuit element QXXX. The parameter TYPE defines the model as one of the semiconductor types listed in table 6 (ref 2). Parameters listed within the parentheses are defined in table 1. An addi-tional parameter, specified on semiconductor component cards only, is the area factor (AF). It is obtained from an area measurement of the physical devices top view which is then normalized to the smallest measured circuit example of that device. For example, a transistor, Q2, which is twice the size of a transistor, Q1, is described with the same component descriptor as Q1, but with an area factor of 2. Area factor is important because it is used by the program to modify transistor parameters which are a function of area. Transistor parameters affected by area are labeled with an asterisk in table 1.

Diode component description follows the basic component format and requires that the diode component name start with the letter D. In addition, nodal connections must be listed in the order of anode to cathode. As in the case of the transistor, diode characteristics are described by a .MODEL card whose model name is identical to the component descriptor referenced by the diode component card. Area factor is also a part of diode component description and affects those parameters indicated in table 5.

Zenar diode description utilizes SPICE2's sub-circuit capability. It allows a particular connection of elements to be placed as a single component anywhere in the circuit. A sub-circuit call references and places a sub-circuit as follows:

```
XYYY N1 N2........NN SUBNAM
```

In the above card, variable XYYY is the unique name of the circuit component to be described by the sub-circuit. The name must begin with the letter X and be no more than eight characters long. N1 through NN represent the main circuit nodes to which the sub-circuit is to be connected. SUBNAM identifies the sub-circuit being referenced by matching exactly the name appearing on the first card of the sub-circuit description as follows:

```
.SUBCKT SUBNAM N1 N2........NN
```

While SUBNAM must correspond exactly to the SUBNAM on the sub-circuit call, nodes N1 through NN need not numerically match the nodes listed on the sub-circuit call. The nodes of the sub-circuit call list, however, will be assumed to be electrically equivalent to corresponding nodes in the .SUBCKT node list. A sub-circuit element list is terminated by an .ENDS card of the following form:

```
.ENDS SUBNAM
```

Resistor input begins with a component name of eight characters or less starting with the letter R. Node connections are then supplied and followed by a resistance value. The following demonstrates this format:

    R5 3 4 5K

Capacitors are described with the same format as resistors but must have component names which begin with the letter C.

Voltage sources used within the M732 timer model are of the D.C. or piecewise linear type. Both require a component name beginning with the letter V, a positive terminal node, a negative terminal node, and in the case of a D.C. source, one numerical voltage value. When the supply is described in a piecewise manner, the format is as follows:

    V N1 N2 PWL (T1 V1 T2 V2.....etc.)

In the above format, T1 is the independent variable and represents the time at which voltage V is V1. The characters, PWL, identify the source as being piecewise linear and must appear as depicted.

Simulation Controls

Simulation control input for the M732 Timer model consists of a few of the many control options available with SPICE2. The control options used include COMMENT cards, .OPTIONS cards, .TRAN cards, .PLOT cards, a TITLE card, and an .END card. These options are the only options discussed in this report. The control options available with SPICE2 are discussed in more detail in the SPICE2 User's Manual (ref 2).

Comment cards are used throughout the model listing to identify circuit modules and clarify model input. They can be placed anywhere in the input deck but must be preceded by an asterisk.

.OPTIONS cards act to define the option variables listed in table 7 (ref 2) The .OPTIONS card format is as follows:

    .OPTIONS OPT1 OPT2.....(or OPT1=X)

A .TRAN card is used to specify transient simulation controls and is written with the following format:

    .TRAN P1 P2 P3 P4

Variables P1, P2, P3, and P4 represent print interval, simulation stop time, simulation start time, and maximum step size, respectively.

A .PLOT control card is used to specify plotted output. Its general format is as follows:

.PLOT PTYPE OV1 OV2......OV8

In the above format, PTYPE represents the type of analysis which produced the output requested. In the case of the model described by this report, transient analysis was the only type of analysis performed. The word TRAN was, therefore, always used as the PTYPE variable. OV1 through OV8 represent from one to eight output variables to be plotted on the same axis.

Voltage outputs are one possible type of output variable and are requested with the following format:

V(N1,N2)

Variables N1 and N2 represent the assumed positive and negative nodes between which voltage is to be measured. If N2 is omitted, ground is assumed as the negative node.

Current output is obtained by referencing a voltage source through which the current flows. A current output request appears as follows:

I(VXXXX)

VXXXX may be a source of some value or a zero valued voltage source whose only function is to act as a reference for a current output request. The following .PLOT card example requests that the transient voltage between nodes one and two be plotted along with the current flowing through voltage source, V7:

.PLOT TRAN V(1,2) I(V7)

Surrounding the entire model are an initial TITLE card and a final .END card. The .END card is preceded by a period while the TITLE card is not. Their combined appearance is as follows:

TITLE
"MODEL DATA"
.END

The listing in figure B-2 (app B) references figure 3 and exemplifies the type of inputs just discussed. A more detailed description of SPICE2's program input format can be obtained from the SPICE2 User's Manual (ref 2).

TIMER MODEL USAGE

The primary purpose for the development of the M732 timer model is to provide a means by which Product Assurance engineers can determine the acceptability of engineering change proposals (ECP), requests for waiver (RFW), or requests for deviation (RFD). Such device modification requests, often

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submitted by manufacturers, must be evaluated to determine their acceptability with regard to device specifications outlined by specification control drawings (SCD). The most critical of the SCD requirements for the M732 timer IC are those involving the measurement of a parameter designated as "time out." Time out is the amount of time it takes for the voltage across capacitor Cl (fig. 3) to reach a threshold at which timer output is delivered to the M732 oscillator. Because of its importance, an example of time out determination is presented as a demonstration of timer model usage.

Timer Operation

Before describing time out determination, a general description of the timing process should be presented. A description of the timing process begins with the SPICE2 schematic (fig. 3). A multi-vibrator action is initiated as follows: When voltage is applied at node 1, capacitor C4 charges through resistors RA, RB, and R11 to a voltage which is approximately one half of node 2's regulated 14.7 volts. When C4 charges to a value large enough to turn transistor Q2 on, Q2 draws current out of Q9's base, turning it on. Transistor Q3A then becomes active and drives Q3 on. As a result, Q6 and Q101 turn on allowing capacitor Cl to charge through resistor RT and diode D8. At the same time, capacitor C4 is discharged through resistor RB and transistor Q6 causing transistor Q2 to turn off. When this happens, the charging of capacitor Cl is interrupted until C4 can again become charged to a value large enough to repeat the cycle. This type of astable behavior continues until the voltage at node 40 drops to a value approximately two diode drops below the threshold voltage of node 44. Transistors Q13 and Q28 are then forced on turning Q21 on. Transistor Q24 also becomes active turning Q27 on. In addition to supplying pin 13 with a high output signal, Q27's on condition also causes Q23 and Q230 to turn on. This in turn drives Q26 on and latches the output signal at the supply voltage. Transistor Q16 is turned on by the increase in Q230's collector voltage, causing the turning off of transistor Q11 and the shut down of the voltage regulator.

Time Out Determination

The increase in voltage across a capacitor, C, which is being charged to some d.c. value, V, through a resistor, R, is classically expressed as follows:

$$V_c = V_o + (V - V_o) \left(1 - EXP \left(\frac{-t}{RC}\right)\right) \tag{10}$$

Variable V_o represents the initial charge on the capacitor. Assuming $V_o = 0$ and rewriting equation 10 to solve for the time, t, at which some capacitor voltage V_c is reached.

$$t = - (R)(C) \ln \left\{ - \frac{(V_c - V)}{V} \right\}$$

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In the timer circuit being modeled, the charging of capacitor C1 through resistor R_T is not continuous. Values for t must, therefore, be adjusted as follows:

$$t_D = \frac{t}{D} = \left\{ - (R)\ (C)\ \ell n \left[- \frac{(V_c - V)}{V} \right] \right\}/D \tag{11}$$

D is referred to as the duty cycle and represents that part of the multivibrator's period during which C1 is being charged. The duty cycle is easily obtained by executing the SPICE2 program input data for the abbreviated M732 timer IC test circuit (app B). The data reflects the circuit of figure 4 and monitors the duty cycle at node 81. Figure 4 is an abbreviation of the timer test circuit (fig. 5) prescribed by the timer SCD and is used for the purpose of decreasing computer costs to a reasonable level. The abbreviated model disregards the effect of the timer's output circuit since the output circuit is turned off until after time out occurs. While the timer output circuit would not be used to determine the length of time out, its presence would be necessary to determine timer response at the moment of time out. Upon execution of the data from figure B-3 (app B), a duty cycle of 0.02785 can be seen to exist for the specification control drawing conditions of table 8, subgroup 3 when resistor R_A is equal to 100 kΩ. Values for V_c and V are made available by the program execution of figure B-2 (app B). The value of V_c is obtained by recording the voltage across capacitor C1 [V(2,40)] when transistor Q13 (fig. 3) turns on and C1 begins to discharge. Variable V is defined as the sum of the voltage across resistor R_T [V(40,35)] and the voltage across capacitor C1 [V(2,40)] at any instant while C1 is being charged. Substitution of these values and those of R_T and C1, (fig. 5), into equation 11 yields the following value for time out:

$$t_D = - \frac{(2.2 \times 10^6)\ (0.56 \times 10^{-6})}{0.02785} \ell n \left\{ \frac{(6.631 + 7.233) - 7.4}{(6.631 + 7.233)} \right\}$$

$$t_D = 33.75 \text{ sec}$$

It should be noted that the function of source V_{cap} in figures B-2 and B-3 is that of an initial condition on capacitor C1. Its introduction was prompted by a desire to decrease computer running time and to minimize computer costs.

TIMER MODEL VERSUS HARDWARE MEASURED RESULTS

Acceptable timer operation is defined by specification control drawing 11720574. The measurement procedures to be followed when determining proper operation are also outlined by this SCD. SPICE2 simulations of timer operation were made under SCD prescribed conditions and produced results within the requirements dictated by the SCD. SPICE2 results were also compared with hardware measured data, and in most cases, fell within the measured data's 3 σ level. SCD requirements are described in table 8 in addition to a comparison of model results versus hardware measured data taken from Motorola lot SC25362PH-77.49. The hardware data used in table 8 are statistical results from a sampling of only one device lot and should not be expected to match exactly the results from a different lot.

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Table 1. SPICE2 NPN transistor model parameters

Symbol	Description	Values		
		Default	Typical	Used
β_F	Ideal forword current gain	100	100	100
β_R	Ideal reverse current gain	1.0	0.1	0.1
I_S	Saturation current (amps)	1.0E-14	1.0E-14	6.0E-16
R_B*	Base ohmic resistance (ohms)	0	100	100
R_C*	Collector ohmic resistance (ohms)	0	10	10
R_E*	Emitter ohmic resistance (ohms)	0	1	1
V_A	Forward early voltage	Infinite	200	200
V_B	Reverse early voltage	Infinite	200	200
I_K*	Forward knee current (mA)	Infinite	10	10
C_2	Forward nonideal base current coefficient	0	1000	750
N_E	Nonideal B-E emission coefficient	2.0	1.5	1.95
I_{KR}*	Reverse knee current (mA)	Infinite	100.0	100.0
C_4	Reverse nonideal base current coefficient	0	1.0	1.0
N_C	Nonideal B-C emission coefficient	2.0	1.5	1.5
T_F	Forward transit time (ns)	0	0.1	0.1
T_R	Reverse transit time (ns)	0	10.0	10.0
C_{CS}*	Collector-substrate capacitance (pF)	0	2.0	0.25
C_{JE}*	Zero-bias B-E junction capacitance (pF)	0	2.0	0.25
P_E	B-E junction potential	1.0	0.7	0.7

* Parameters affected by area factor (AF).

Table 1. (cont)

Symbol	Description	Values		
		Default	Typical	Used
M_E	B-E junction grading coefficient	0.5	0.33	0.33
C_{JC}*	Zero bias B-C junction capacitance (pF)	0	1.0	0.25
P_C	B-C junction potential (V)	1.0	0.5	0.5
M_C	B-C grading coefficient	0.5	0.33	0.33
E_G	Energy gap	1.11	1.11 SI 0.67 GE	1.11
P_T	Saturation current temperature exponent	3.0	--	3.0
K_F	Flicker noise coefficient	0	--	0
A_F	Flicker noise exponent	1.0	--	1.0

* Parameters affected by area factor (AF).

Table 2. Hardware measured test data typical of the M732 timer
fabricating process for NPN transistors (I)

Collector current (I_c)	Current gain (β)	V_{ce}[1]	V_{be}[2]
		(V)	(V)
50 µA	75	5.0	0.647
1 mA	85	5.0	0.731

---

[1] V_{ce} – Collector-to-emitter terminal voltage.

[2] V_{be} – Base-to-emitter terminal voltage.

NOTE: Data was assumed to be taken at a junction temperature of 298.56 K (78°F) resulting in a thermal voltage (V_T) of 0.02575 V.

Table 3. Hardware measured test data typical of the M732 timer
fabricating process for NPN transistors (II)

Parameter		
Name	Description	Value
C_o	Base-to-emitter zero bias capacitance	$4.65 \times 10^8 \, pF/m^2$
R_{ION}	Ion implanted sheet resistance	1 Ω/square
R_D	Diffused sheet resistance	125 ohms/square
T	Junction temperature	25.56°C
D	Emitter junction depth	2.5×10^{-6} m
L	Emitter junction length	1.87×10^{-5} m
W	Emitter junction width	1.87×10^{-5} m
k	Boltzmann's constant *	1.38×10^{-23} joules/°C
q	Charge of an electron	1.6×10^{-19} coul

---

* Joules/°C is equivalent to joules/K.

Table 4. Transistor model versus hardware measured operating point data

V_{be} (V)	V_{ce} (V)	Hardware measured current gain	Model measured current gain	Hardware measured collector current	Model measured collector current
0.647	5.0	75	74.6	50 μA	49.95 μA
0.731	5.0	85	85.36	1 mA	1.085 mA

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Table 5. SPICE2 diode model parameters

Symbol	Description	Default	Typical	Used
I_S*	Saturation current (amp)	1.0E-14	1.0E-14	6.0E-16
R_S*	Ohmic resistance (ohms)	0	10	10
N	Emission coefficient	1.0	1.0	1.0
T_T	Transit time (ns)	0	0.1	0.1
C_{JO}*	Zero-bias junction capacitance (pF)	0	2	0.25
P_B	Junction potential (V)	1.0	0.6	0.7
M	Grading coefficient	0.5	0.5	0.5
E_G	Energy gap	1.11	1.11 SI 0.69 SBD 0.67 GE	1.11
P_T	Saturation current temperature exponent	3.0	3.0 UN 2.0 SBD	3.0
K_F	Flicker noise coefficient	0	--	0
A_F	Flicker noise exponent	1	--	1

* Parameters affected by area factor (AF)

Table 6. Semiconductor model types

Designator	Definition
NPN	NPN BJT model
PNP	PNP BJT model
D	Diode model
NJF	N-channel JFET model
PJF	P-channel JFET model
NMOS	N-channel MOSFET model
PMOS	P-channel MOSFET model

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Table 7. SPICE2 .OPTION card options

Option	Effect
ACCT	Causes the execution time for the various sections of the program, as well as other accounting information, to be printed.
LIST	Causes the summary listing of the input data to be printed.
NOMOD	Suppresses the printout of the model parameters.
NODE	Causes the node table to be printed.
OPTS	Causes the option values to be printed.
GMIN=X	Resets the value of GMIN, the minimum conductance allowed by the program. The default value is 1.0E-12.
RELTOL=X	Resets the relative error tolerance of the program. The default value is 0.001 (0.1 %).
ABSTOL=X	Resets the absolute error tolerance of the program. The default value is 1.0E-12.
TRTOL=X	Resets the transient error tolerance. The default value is 10.0. This parameter is an estimate of the factor by which SPICE over-estimates the actual truncation error.
CHGTOL=X	Resets the charge tolerance of the program. The default value is 1.0E-14.
NUMDGT=X	Resets the numbers of significant digits printed for output variable values. X must satisfy the relation $1 < X < 7$. The default value is 4. Note this option is independent of the error tolerance used by SPICE (i.e., if the values of options RELTOL, ABSTOL, etc, are not changed then one may be printing numerical "noise" for NUMDGT > 5).
TNOM=X	Resets the nominal temperature. The default value is 27°C (300 K).
ITL1=X	Resets the d.c. iteration limit. The default is 100.
ITL2=X	Resets the d.c. transfer curve iteration limit. The default is 20.
ITL3=X	Resets the lower transient analysis iteration limit. The default value is 4.
ITL4=X	Resets the transient analysis timepoint iteration limit. The default is 10.
ITL5=X	Resets the transient analysis total iteration limit. The default is 5000.

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Table 7. (cont)

Options	Effect
LIMTIM=X	Resets the amount of time reserved by SPICE2 for generating plots. The default value is 2 (seconds).
LIMPTS=X	Resets the total number of points that can be printed in a d.c., a.c., or transient analysis. The default value is 201.
LVLCOD=X	If X is 2, then machine code for the matrix solution will be generated. Otherwise, no machine code is generated. The default value is 2.
LVLTIM=X	If X is 1, the iteration timestep control is used. If X is 2, the truncation-error timestep is used. The default value is 1. If method=gear and MAXORD > 3 then LVLTIM is set to 2 by SPICE2.
METHOD	Sets the numerical integration method used by SPICE2. Possible values are gear or trapezoidal. The default is trapezoidal.
MAXORD	Sets the maximum order for the integration method if gear's variable-order method is used. Should range between 2 and 6. Default value is 2.

Table 8. SCD requirements versus hardware and model results

Examination or test	Specific conditions	Symbol	Limits Min	Max	Hardware test results Mean	3σ	Model results
Subgroup 2							
Temperature: 25 ± 5°C	(ref 4)						
Current drain during timing	Vcc = 36.0 V (Measure current into pin 1)	IBO	5.0 mA	20.0 mA	11.9637 mA	1.9508 mA	18.1 mA
Output leakage current during timing	Vcc = 36.0 V (Measure current from pin 13)	ILO	—	12.0 µA	999.992 pA	7.21888 pA	540.0 pA
(A) Regulator voltage during timing	Vcc = 36.0 V (Measure voltage at pin 2)	VR1	(record value)		14.5509 V	0.297849 V	14.6 V
(A) Regulator voltage during timing	Vcc = 23.0 V (Measure voltage at pin 2)	VR2	(record value)		14.5059 V	0.2939 V	14.6 V
Regulator voltage after timeout	Vcc = 31.5 V (Measure voltage at pin 2)	VBO	—	1.0 V	216.663 mV	232.251 mV	600 mV
Current drain after timeout	Vcc = 31.5 V Adjust RL to make IL=100 mA (Measure current into pin 1)	IBI	105 mA	120 mA	109.333 mA	2.0716 mA	108.5 mA
Input to output voltage drop after timeout	Vcc = 36.0 V (Measured voltage between pins 1 and 13)	VO	—	1.7 V	1.07618 V	0.202233 V	0.858 V

Table 8. (cont)

Examination or test	Specific conditions	Symbol	Limits Min	Max	Hardware test results Mean	3 σ	Model results
Subgroup 3							
Temperature: 25 ± 5°C	(ref 4)						
Room ambient timeout	Vcc = 31.5 V R$_A$ = 0 R$_A$ = 100 kΩ R$_A$ = 453.2 kΩ	TRO TR1 TR2	1.8 sec 29.0 sec (4.33) -1%	2.2 sec 37.0 sec (TR1) +1%	1.9373 sec 33.7766 sec 145.648 sec	0.0579 sec 1.32333 sec 5.7608 sec	1.9 sec 33.75 sec 145.64 sec
$\frac{dV}{dt}$ immunity, ambient	Vcc = 36.0 V (ref 4)	DVDTA	--	0.2 V	999.991 µV	9.488 µV	0.1519 µV
Subgroup 4							
Temperature: 63 ± 3°C	(ref 4)						
High temperature timeout	Vcc = 31.5 V R$_A$ = 100 kΩ	TH	TR1 sec -2%	TR1 sec +2%	34.0159 sec	1.54616 sec	33.97 sec
$\frac{dV}{dt}$ immunity, hot	Vcc = 36.0 V (ref 4)	DVDTH	--	0.2 V	999.994 µV	5.722 µV	20.5 µV
Output leakage current, hot	Vcc = 36.0 V	ILH	--	100 µA	999.994 µA	3.8586 pA	69 nA
Subgroup 5							
Temperature: -40 ± 2°C	(ref 4)						

Table 8. (cont)

Examination or test	Specific conditions	Symbol	Limits Min	Limits Max	Hardware test results Mean	Hardware test results 3 σ	Model results
Subgroup 5 (cont)							
Low temperature timeout	Vcc = 31.5 V R_A = 100 kΩ	TL	TR1 sec −2%	TR1 sec +2%	33.8436 sec	1.688 sec	34.229 sec
dV/dt immunity, cold	(ref 4) Vcc = 36.0 V	DVDTL	—	0.2 V	999.995 µV	4.95 µV	342.7 µV
Input to output voltage drop after timeout, cold	Vcc = 36.0 V (Measure voltage between pins 1 and 13)	VOL	—	1.7 V	967.353 mV	490.678 mV	926 mV
Subgroup 6							
(ref 4)							
Temperature: as indicated							
Tolerance to ratiometer variability low side	Vcc = 23 V R_A = 80 kΩ R_B = 2400 Ω Temp +63 ± 2°C	T6L	TR1 sec −3%	TR1 sec +3%	34.2959 sec	2.11093 sec	34.141 sec
Tolerance to ratiometer variability, high side	Vcc = 36 V R_A = 120 kΩ R_B = 3600 Ω Temp −40 ± 2°C	T6H	TR1 sec −3%	TR1 sec +3%	33.3778 sec	1.92015 sec	34.21 sec
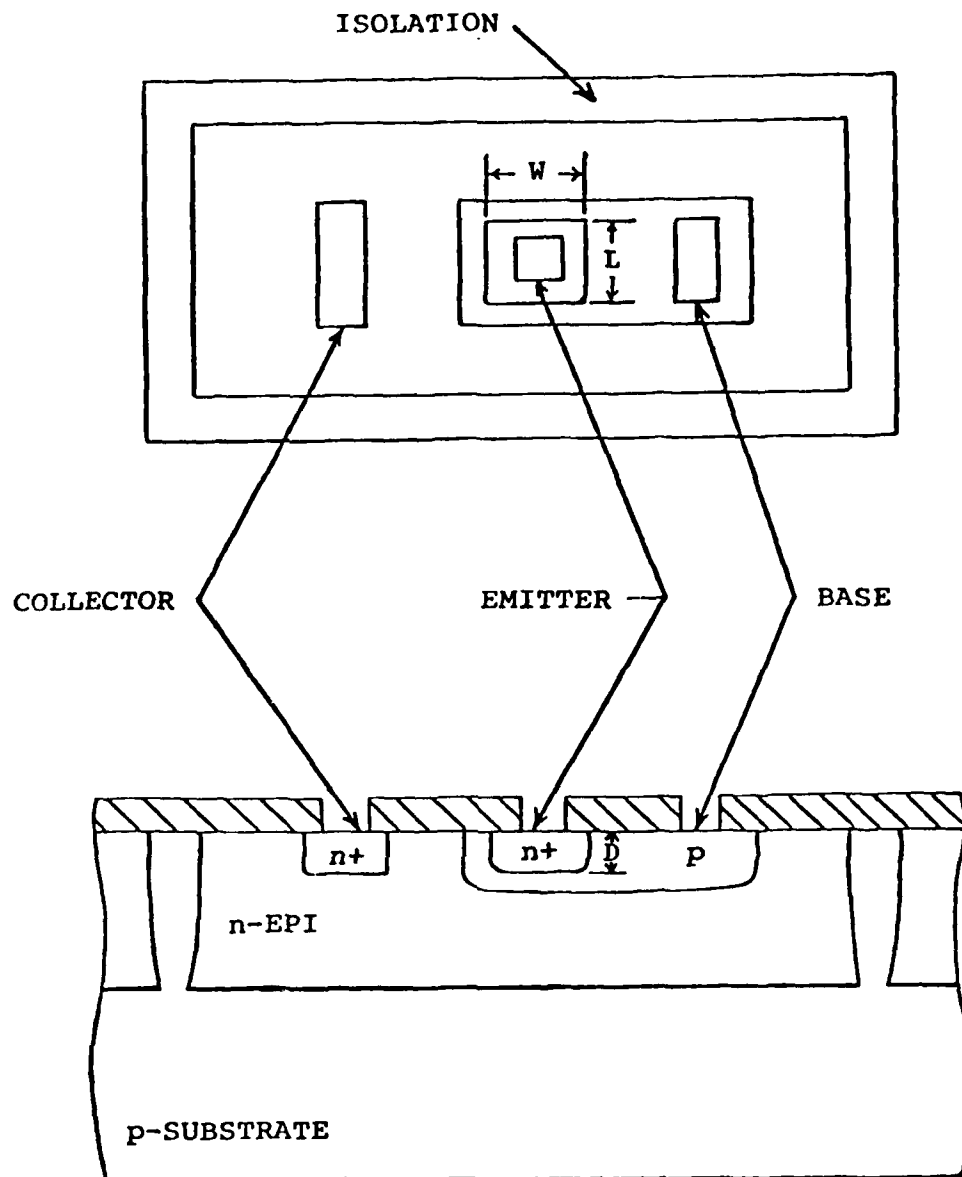
Figure 1. Typical integrated NPN bipolar transistor

Figure 2. Specification control drawing schematic for the M732 timer circuit
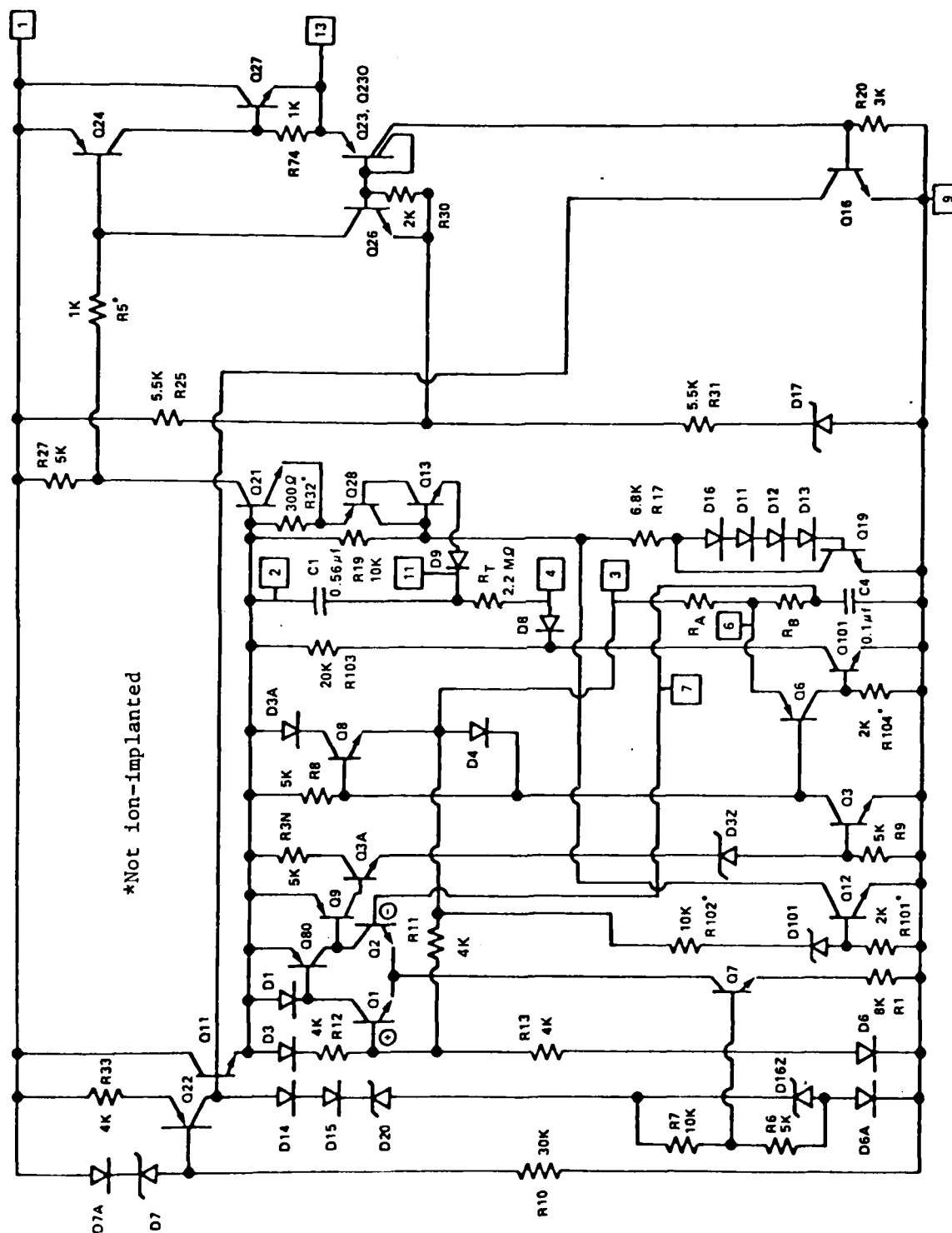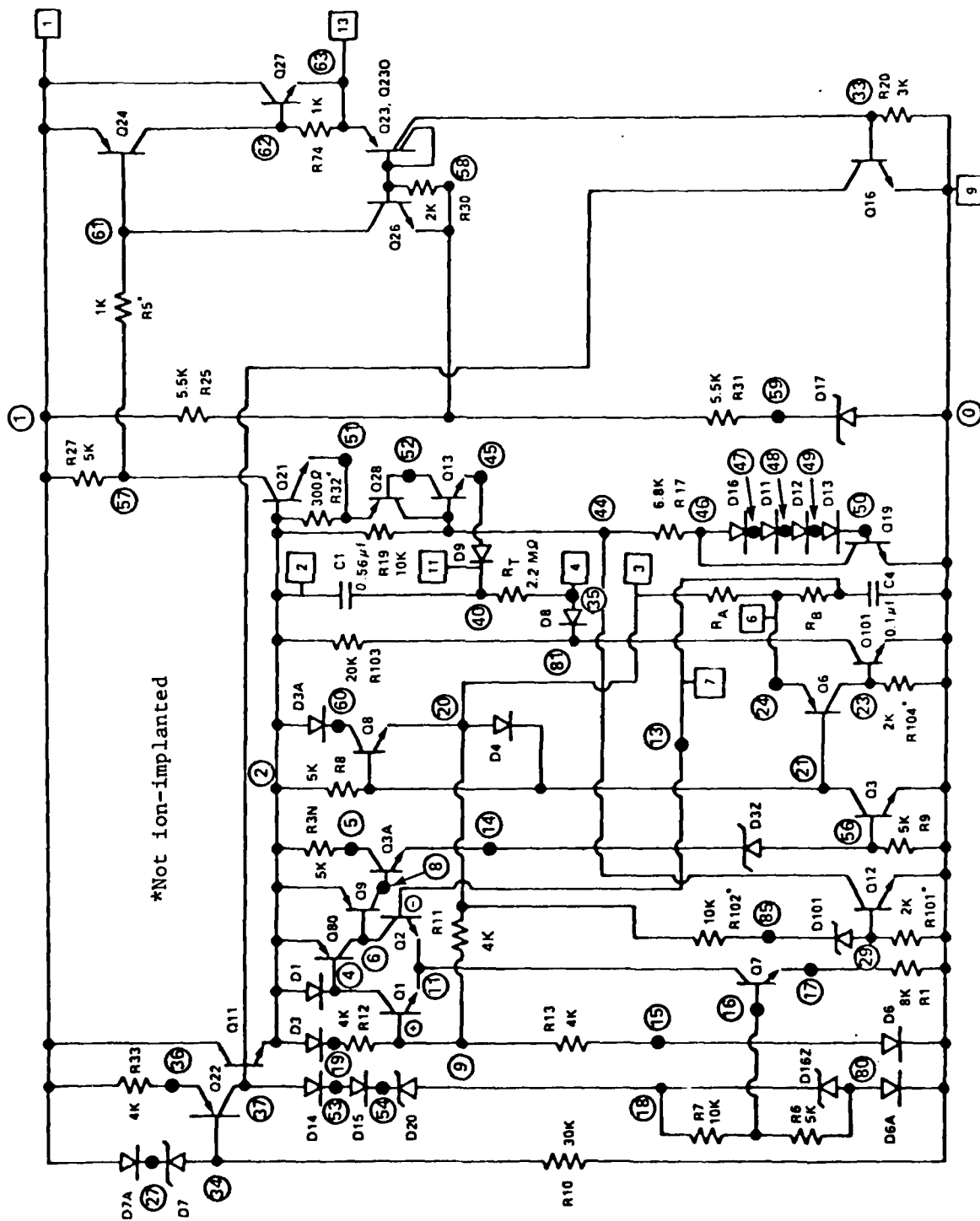
Figure 3. M732 timer circuit model schematic

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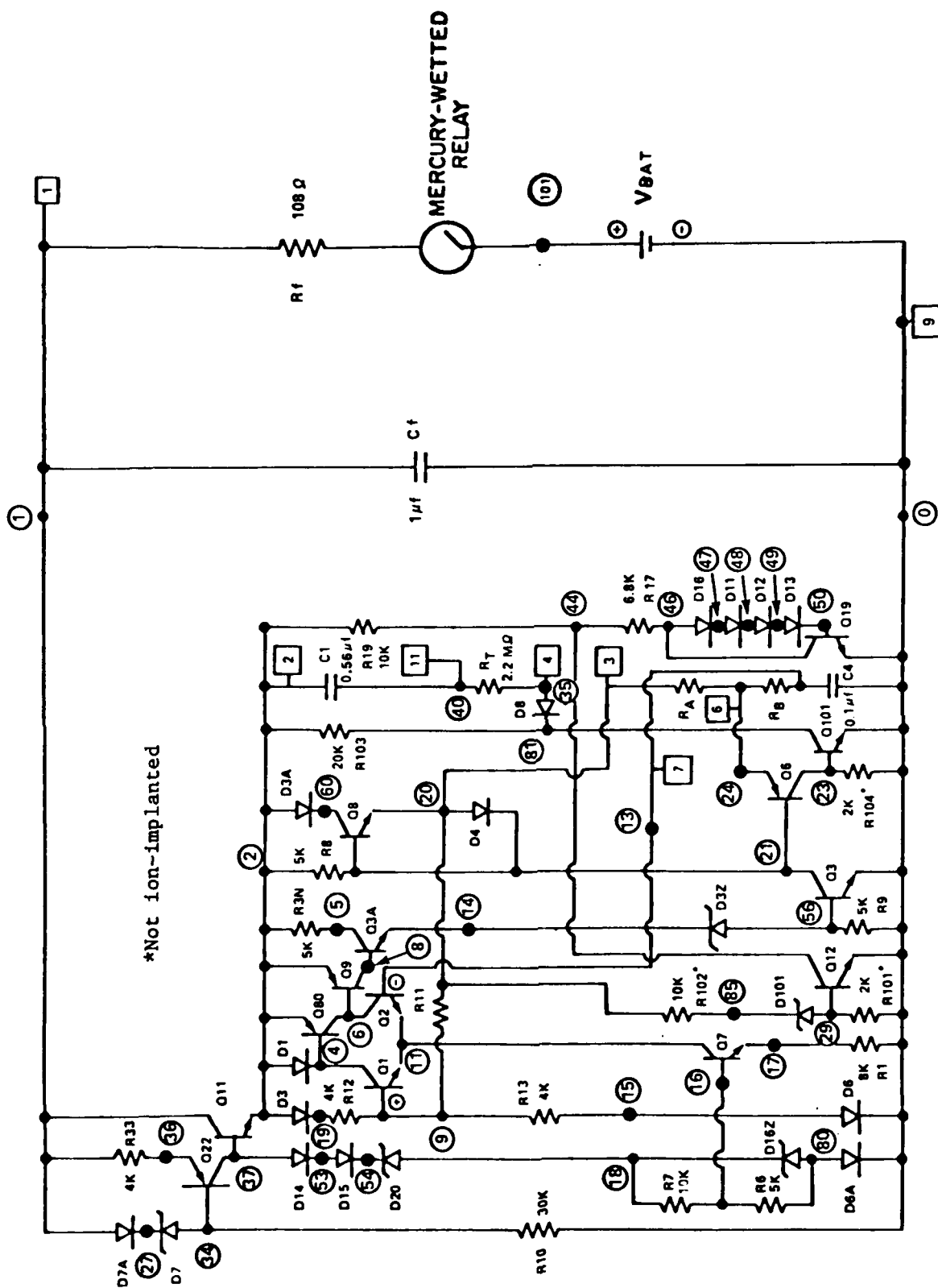
Figure 4. Abbreviated M732 timer test circuit

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RF = 1.8 ohms   CF = 1.0 uF

RA = varied   CO = 0.10 uF

RB = 3.0 K ohms   Cl = 0.56 uF

RT = 2.2 M ohms   CL = 0.002 uF

RL = 500 ohm potentiometer (adjust for IL = 100 mA)

Figure 5. SCD prescribed M732 timer test circuit
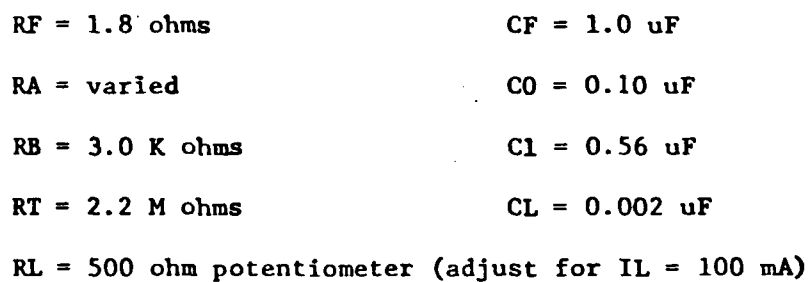
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APPENDIX A
GUMMEL-POON NPN TRANSISTOR MODEL AND DEFINING EQUATIONS

The following equations describe the behavior of the Gummel-Poon NPN transistor model of figure A-1.*

$$J_A = C_2 \, I_s \left\{ EXP \left(V_{be}/N_e \, V_T \right) - 1 \right\}$$

$$J_B = \left\{ I_s/\beta_F \right\} \left\{ EXP \left(V_{be}/V_T \right) - 1 \right\}$$

$$J_c = C_4 \, I_s \left\{ EXP \left(V_{bc}/N_c \, V_T \right) - 1 \right\}$$

$$J_D = \left\{ I_s/B_R \right\} \left\{ EXP \left(V_{bc}/V_T \right) - 1 \right\}$$

$$J_F = \beta_F \, J_B/Q_B \qquad\qquad J_R = \beta_R \, J_D/Q_B$$

$$Q_1 = 1 + \left(V_{bc}/V_A \right) + \left(V_{be}/V_B \right)$$

$$Q_2 = \left\{ I_s/I_K \right\} \left\{ EXP \left(V_{be}/V_T \right) - 1 \right\} + \left\{ I_s/I_{KR} \right\} \left\{ EXP \left(V_{bc}/V_T \right) - 1 \right\}$$

$$Q_B = \left\{ Q_1/2 \right\} \left\{ 1 + \left(1 + 4Q_2 \right)^{1/2} \right\}$$

$$C_E = \frac{C_{JE}}{\left\{ \left(1 - \dfrac{V_{be}}{P_E} \right) + 0.04 \right\}^{M_E}} + \frac{T_F}{V_T} \left\{ B_F \, J_B + I_s \right\}$$

$$C_c = \frac{C_{jc}}{\left\{ \left(1 - \dfrac{V_{cc}}{P_c} \right) + 0.04 \right\}^{M_c}} - \frac{T_R}{V_T} \left\{ B_R \, J_D + I_s \right\}$$

---

* J. C. Bowers, N. English, and H. A. Nienhaus, "Parameter Determination Techniques for the Gummel-Poon CAD Transistor Model," University of South Florida, Tampa, FL.

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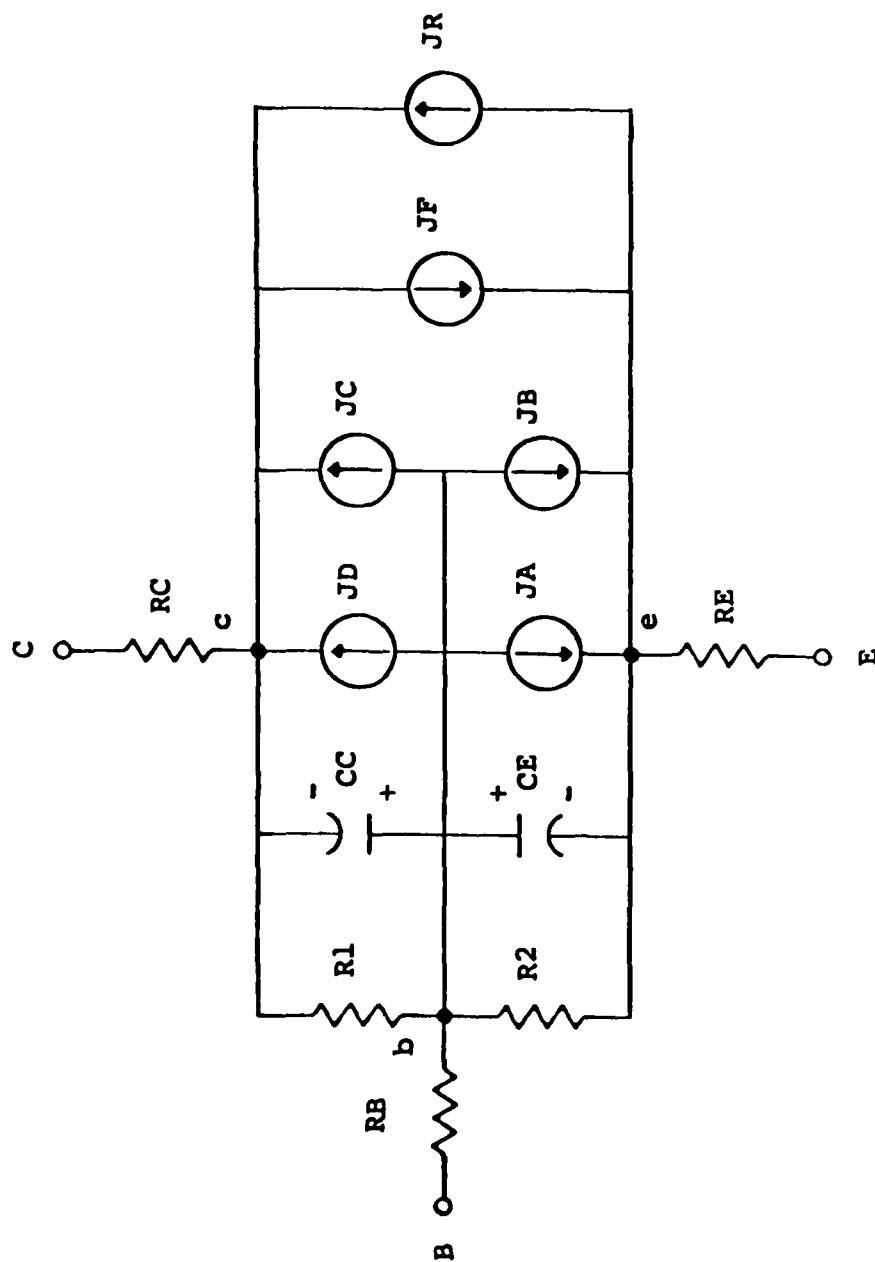
Figure A-1. Gummel-Poon NPN transistor model

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APPENDIX B
SPICE2 PROGRAM INPUT LISTINGS

NPN TRANSISTOR MODEL OPERATING POINT TEST

....

```
*    SIMULATION CONTROLS
*
.OPTIONS TNOM=25.555 METHOD=GEAR
.TRAN 1 5 0 1
*
*    CIRCUIT LAYOUT
*
VCE 4 0 5
Q 4 2 0 TRAN
VBE 2 0 0.731
*
*    NPN TRANSISTOR MODEL CHARACTERISTICS
*
.MODEL TRAN NPN(BR=0.1 RB=100 RC=10 RE=1 VA=200 VB=200
+IKR=100MA C4=1.0 NC=1.5 TF=0.1NS TR=10NS PE=0.7 ME=0.33
+CCS=0.25PF CJE=0.25PF CJC=0.25PF IK=10MA C2=750 NE=1.95
+EG=1.11 PT=3.0 KF=0 AF=1
+PC=0.5 MC=0.33 BF=100 IS=6E-16)
*
*    BASE CURRENT AND COLLECTOR CURRENT OUTPUTS
*
.PRINT TRAN I(VBE)
.PRINT TRAN I(VCE)
.END
```

Figure B-1.   SPICE2 program input of the NPN transistor model's
              operating point test circuit.

```
*****          ********  SPICE 2A.0 (15JUL75)  ********


M732 TIMER I.C. TEST CIRCUIT


*****************************************************************


*
*    SIMULATION CONTROLS
*
.OPTIONS ITL5=10000 NOMOD OPTS LIMTIM=20 METHOD=GEAR
+TRTOL=3 LIMPTS=5000
.TEMP 25
.TRAN 0.01E-3 2E-3 0 0.1E-3
*
*    CIRCUIT LAYOUT EXTERNAL TO TIMER I.C.
*
*      SUPPLY VOLTAGE
*
VBAT 101 0 PULSE(0 31.5)
*
*      INITIAL CONDITION VOLTAGE ON CAPACITOR C1
*
VCAP 2 401 PWL(0 0 1E-4 6.0 10E-4 9.0 20E-4 9.0)
*
C1 401 40 0.56E-6
C4 13 0 0.1E-6
CF 1 0 1.0U
CL 90 0 0.002U
RA 20 24 1K
RB 24 13 3K
RF 101 1 1.8
RL 90 0 340
RT 35 40 2.2MEG
*
*    CIRCUIT LAYOUT INTERNAL TO TIMER I.C.
*
*      RESISTOR LIST
*
R1 17 0 8K
R3N 2 5 5.5K
R5 57 61 1K
R6 16 80 5.2K
R7 16 18 9.5K
R8 2 21 4.7K
R9 14 0 5.2K
R10 0 34 27.5K
R11 9 20 4.2K
R12 19 9 4K
R13 9 15 4K
R17 44 46 5.678K
R19 2 44 7.978K
R20 33 0 3K
R25 1 58 5.5K
R27 1 57 5K
R30 60 58 2K
R31 58 59 5.5K
R32 2 51 300
```

Figure B-2.   SPICE2 program input of the SCD prescribed M732 timer
test circuit.

```
R33 1 36 4.2K
R74 62 63 1K
R101 29 0 2.2K
R102 85 20 11.7K
R103 81 2 22.4K
R104 23 0 2.2K
*
*      DIODE LIST
*
D1 2 4 DIODE1
D3 2 19 DIODE1 1.73
D3A 2 60 DIODE1 1.73
D4 20 21 DIODE1 1.73
D6 15 0 DIODE1 1.73
D6A 80 0 DIODE1 1.73
D7A 1 27 DIODE1
D8 35 81 DIODE1
D9 45 40 DIODE1
D11 47 48 DIODE1
D12 48 49 DIODE1
D13 49 50 DIODE1
D14 37 53 DIODE1 1.73
D15 53 54 DIODE1 1.73
D16 46 47 DIODE1
*
*      ZENAR LIST
*
XZD3Z 14 56 ZENAR
XZD7 27 34 ZENAR
XZD16Z 18 80 ZENAR
XZD17 59 0 ZENAR
XZD20 54 18 ZENAR
XZD101 85 29 ZENAR
*
*      TRANSISTOR LIST
*
Q1 4 9 11 TRAN3
Q2 6 13 11 TRAN3
Q3 21 56 0 TRAN3 4.7
Q3A 5 8 14 TRAN3
Q7 11 16 17 TRAN3
Q6 23 21 24 TRAN4 5.8
Q8 60 21 20 TRAN3 3.7
Q9 8 6 2 TRAN4
Q11 1 37 2 TRAN3
Q12 44 29 0 TRAN3
Q13 52 44 45 TRAN3
Q16 37 33 0 TRAN3
Q19 49 50 0 TRAN3
Q21 57 2 51 TRAN3
Q22 37 34 36 TRAN4 5.8
Q23 60 60 63 TRAN4 0.65
Q24 62 61 1 TRAN4 5.8
Q26 61 60 58 TRAN3
Q27 1 62 63 TRAN3 34.3
Q28 44 52 51 TRAN4
Q80 8 4 2 TRAN4
Q230 33 60 63 TRAN4 0.65
Q101 81 23 0 TRAN3 3.4
*
*    ZENAR DIODE SUB-CIRCUIT DESCRIPTION
```

Figure B-2.   Continued

```
*
.SUBCKT ZENAR 1 3
DZ 1 2 DIODE1
VZ 2 3 DC 5.9
.ENDS ZENAR
*
*   CURRENT VIEWING VOLTAGE SOURCES
*
VA1 63 90 DC 0.0
*
*   DIODE MODEL CHARACTERISTICS
*
.MODEL DIODE1 D(RS=10 TT=0.1NS CJO=0.25PF PB=0.7 IS=6E-16
+N=1.0 EG=1.11 M=0.5 PT=3.0 KF=0 AF=1)
*
*   TRANSISTOR MODEL CHARACTERISTICS
*
*      NPN TYPE
*
.MODEL TRAN3 NPN(BR=0.1 RB=100 RC=10 RE=1 VA=200 VB=200
+IKR=100MA C4=1.0 NC=1.5 TF=0.1NS TR=10NS PE=0.7 ME=0.33
+CCS=0.25PF CJE=0.25PF CJC=0.25PF IK=10MA C2=750 NE=1.95
+EG=1.11 PT=3.0 KF=0 AF=1
+PC=0.5 MC=0.33 BF=100 IS=6E-16)
*
*      PNP TYPE
*
.MODEL TRAN4 PNP(BR=0.1 RB=100 RC=10 RE=1 VA=200 VB=200
+IKR=100MA C4=1.0 NC=1.5 TF=0.1NS TR=10NS PE=0.7 ME=0.33
+CCS=0.25PF CJE=0.25PF CJC=0.25PF IK=10MA C2=750 NE=1.95
+EG=1.11 PT=3.0 KF=0 AF=1
+PC=0.5 MC=0.33 BF=100 IS=6E-16)
*
*   OUTPUT REQUESTS
*
.PLOT TRAN V(2,40)
.PLOT TRAN V(40,35)
*
*   THE FOLLOWING IS A LIST OF THE CIRCUIT ELEMENTS TO BE ELIMINATED
*   WHEN CREATING THE ABBREVIATED M732 TIMER I.C. TEST CIRCUIT OF
*   FIGURE 4.
*
*
```

RESISTORS	TRANSISTORS	DIODES	CAPACITORS	CURRENT VIEWING VOLTAGE SOURCES
R5	Q13	D9	CL	VA1
R20	Q16	XZD17		
R25	Q21			
R27	Q23			
R30	Q24			
R31	Q26			
R32	Q27			
R74	Q28			
RL	Q230			

```
*
.END
```

$$$$ OPTION SETTINGS

Figure B-2. Continued

```
•••••          ••••••••  SPICE 2A.0  (15JUL75)  ••••••••


ABBREVIATED M732 TIMER I.C. TEST CIRCUIT


•••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••


•
•    SIMULATION CONTROLS
•
.OPTIONS ITL5=10000 NOMOD OPTS LIMTIM=20 METHOD=GEAR
+TRTOL=3 LIMPTS=5000
.TEMP 25
.TRAN 0.01E-3 25.4E-3 0 5E-3
•
•    CIRCUIT LAYOUT EXTERNAL TO TIMER I.C.
•
•      SUPPLY VOLTAGE
•
VBAT 101 0 PULSE(0 31.5)
•
•      INITIAL CONDITION VOLTAGE ON CAPACITOR C1
•
VCAP 2 401 PULSE(0 5.0)
•
C1 401 40 0.56E-6
C4 13 0 0.1E-6
CF 1 0 1.0U
RA 20 24 100K
RB 24 13 3K
RF 101 1 1.8
RT 35 40 2.2MEG
•
•    CIRCUIT LAYOUT INTERNAL TO TIMER I.C.
•
•      RESISTOR LIST
•
R1 17 0 8K
R3N 2 5 5.5K
R6 16 80 5.2K
R7 16 18 9.5K
R8 2 21 4.7K
R9 14 0 5.2K
R10 0 34 27.5K
R11 9 20 4.2K
R12 19 9 4K
R13 9 15 4K
R17 44 46 5.1K
R19 2 44 7.4K
R33 1 36 4.2K
R101 29 0 2.2K
R102 85 20 11.7K
R103 81 2 22.4K
R104 23 0 2.2K
•
•      DIODE LIST
•
D1 2 4 DIODE1
```

Figure B-3.   SPICE2 program input for
the abbreviated M732 Timer I.C. test
circuit.

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```
D3 2 19 DIODE1 1.73
D3A 2 60 DIODE1 1.73
D4 20 21 DIODE1 1.73
D6 15 0 DIODE1 1.73
D6A 80 0 DIODE1 1.73
D7A 1 27 DIODE1
D8 35 81 DIODE1
D11 47 48 DIODE1
D12 48 49 DIODE1
D13 49 50 DIODE1
D14 37 53 DIODE1 1.73
D15 53 54 DIODE1 1.73
D16 46 47 DIODE1
*
*     ZENAR LIST
*
XZD3Z 14 56 ZENAR
XZD7 27 34 ZENAR
XZD16Z 18 80 ZENAR
XZD20 54 18 ZENAR
XZD101 85 29 ZENAR
*
*     TRANSISTOR LIST
*
Q1 4 9 11 TRAN3
Q2 6 13 11 TRAN3
Q3 21 56 0 TRAN3 4.7
Q3A 5 8 14 TRAN3
Q6 23 21 24 TRAN4 5.8
Q7 11 16 17 TRAN3
Q8 60 21 20 TRAN3 3.7
Q9 8 6 2 TRAN4
Q11 1 37 2 TRAN3
Q12 44 29 0 TRAN3
Q19 49 50 0 TRAN3
Q22 37 34 36 TRAN4 5.8
Q80 6 4 2 TRAN4
Q101 81 23 0 TRAN3 3.4
*
*   ZENAR DIODE SUB-CIRCUIT DESCRIPTION
*
.SUBCKT ZENAR 1 3
DZ 1 2 DIODE1
VZ 2 3 DC 5.9
.ENDS ZENAR
*
*   DIODE MODEL CHARACTERISTICS
*
.MODEL DIODE1 D(RS=10 TT=0.1NS CJO=0.25PF PB=0.7 IS=6E-16
+N=1.0 EG=1.11 M=0.5 PT=3.0 KF=0 AF=1)
*
*   TRANSISTOR MODEL CHARACTERISTICS
*
*     NPN TYPE
*
.MODEL TRAN3 NPN(BR=0.1 RB=100 RC=10 RE=1 VA=200 VB=200
+IKR=100MA C4=1.0 NC=1.5 TF=0.1NS TR=10NS PE=0.7 ME=0.33
+CCS=0.25PF CJE=0.25PF CJC=0.25PF IK=10MA C2=750 NE=1.95
+EG=1.11 PT=3.0 KF=0 AF=1
+PC=0.5 MC=0.33 BF=100 IS=6E-16)
*
```

Figure B-3. Continued

```
*     PNP TYPE
*
.MODEL TRAN4 PNP(BR=0.1 RB=100 RC=10 RE=1 VA=200 VB=200
+IKR=100MA C4=1.0 NC=1.5 TF=0.1NS TR=10NS PE=0.7 ME=0.33
+CCS=0.25PF CJE=0.25PF CJC=0.25PF IK=10MA C2=750 NE=1.95
+EG=1.11 PT=3.0 KF=0 AF=1
+PC=0.5 MC=0.33 BF=100 IS=6E-16)
*
*    OUTPUT REQUESTS
*
.PLOT TRAN V(81)
.END
```

Figure B-3. Continued

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