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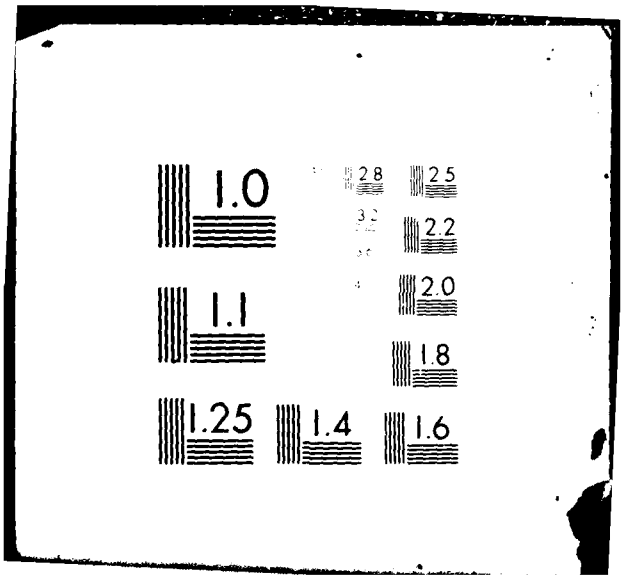
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RADC-TR-81-350
Final Technical Report
December 1981

ELECTRICAL CHARACTERIZATION OF THE 68000 MICROPROCESSOR

IBM Corporation

Jim D. Bailey

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ELECTRICAL CHARACTERIZATION OF THE 68000 MICROPROCESSOR

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This document discusses in detail the electrical characterization of the Motorola 68000, 16 bit microprocessor. Test results are presented on various mask sets and production lots. The test philosophy and test programs that were developed in this study are also presented in sufficient detail.

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EVALUATION

The objective of this effort was to electrically characterize the 68000, 16 bit microprocessor. From the resulting data, a MIL-M-38510 detail specification was to be prepared in a format compatible with DOD coordination standards.

The electrical characterization of the 68000 was successfully accomplished through a very complex and time consuming task. Over the course of this program, this state-of-the-art microprocessor was updated several times by the vendor to enhance performance and/or to improve yields. Each change required a thorough evaluation and comparison of the design or process enhancements versus potential reliability degradation. IBM produced a military detail specification M38510/540 to cover the latest update of the 68000. This specification defines three versions of the 68000 categorized by frequency and enclosed in three package types including two state-of-the-art leadless chip carrier packages.

This program demonstrates what can be accomplished when there exists a good working relationship between the user and the manufacturer of the part. IBM took a basic commercial part and provided the manufacturer the data he needed to militarize it. Motorola on the other hand cooperated in providing information, some proprietary, on key architectural and circuit designs, in addition to information on processing enhancements.

REGIS C. HILOW

Project Engineer

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1.0 INTRODUCTION

The MC68000 is one of the most technologically advanced and architecturally superior microprocessors available today. It follows that an acceptable electrical evaluation of this device would be a complex and time consuming task. This document will discuss in detail the MC68000 Electrical Characterization program and the results that were obtained as various mask sets and device lots were tested across an extended temperature range. For additional information on device description and system integration the reader should reference the Motorola Users Guide MC68000UM (AD2).

At the outset it must be noted that no MIL-883B type part was available for this test exercise from Motorola. Due to the recent announcement and frequent performance enhancements, a military device is now feasible. This program supports the accelerated development of that military product. Early functional failures at the MIL- temperature extremes are noted in this report and are to be expected since these devices were not screened to those corners. As the report tracks the maturity of the masks and process, the functionality at the temperature extremes improved greatly, yielding over 80% fully functional devices (of the test samples) to the military specification generated.

2.0 DEVICE DESCRIPTION

2.1 TECHNOLOGY

The MC68000 is a single chip 16-bit microprocessor fabricated using an N-channel, depletion load, silicon gate technology. The die, measuring approximately 40 μm^2 contains approximately 70,000 transistors. This level of density was achieved with the use of 3μm ground rules (HMOS I).

Further enhancements (HMOS II) and shrinkage is expected in 1982.

2.2 BLOCK DIAGRAM

A block diagram of the MC68000 is shown in Figure 1.0. The processor is composed of seventeen 16-bit registers, a program counter, status register, 16-bit ALU and control section. The flexible instruction set consisting of 56 instructions and 14 different addressing modes is implemented using an on-board microcode ROM. In addition the processor control section will support direct memory access, seven levels of processor peripheral interrupt and 6800 peripheral interface control. The 23 address lines that are supported by the processor allow direct access to over 16 M bytes of memory.

2.3 PIN DESCRIPTION

The MC68000 signal and pin assignment diagram is shown in Figure 2.0.

2.3.1 Address Bus

The address bus is composed of 23 tri-state bus outputs which provide addressing for all bus cycles except DMA operations and interrupts. The 23-bit address range of the processor allows addressing of over 8 MWords (16-MBytes) of memory.

2.3.2 Data Bus

The data bus is a 16-bit, bi-directional, tri-state path for data flowing to and from the processor. Data can be in byte or word length.

2.3.3 Address Strobe (AS)

The address strobe is an active low unidirectional tri-state signal. When AS is low it indicates that the address present on the address pins of the processor is valid.

2.3.4 READ/WRITE (R/W)

The READ/WRITE pin is a unidirectional tri-state signal that defines the processor operation and data bus direction. The signal is low (logic 0) during processor write operations and is high (logic 1) for all subsequent processor operations.

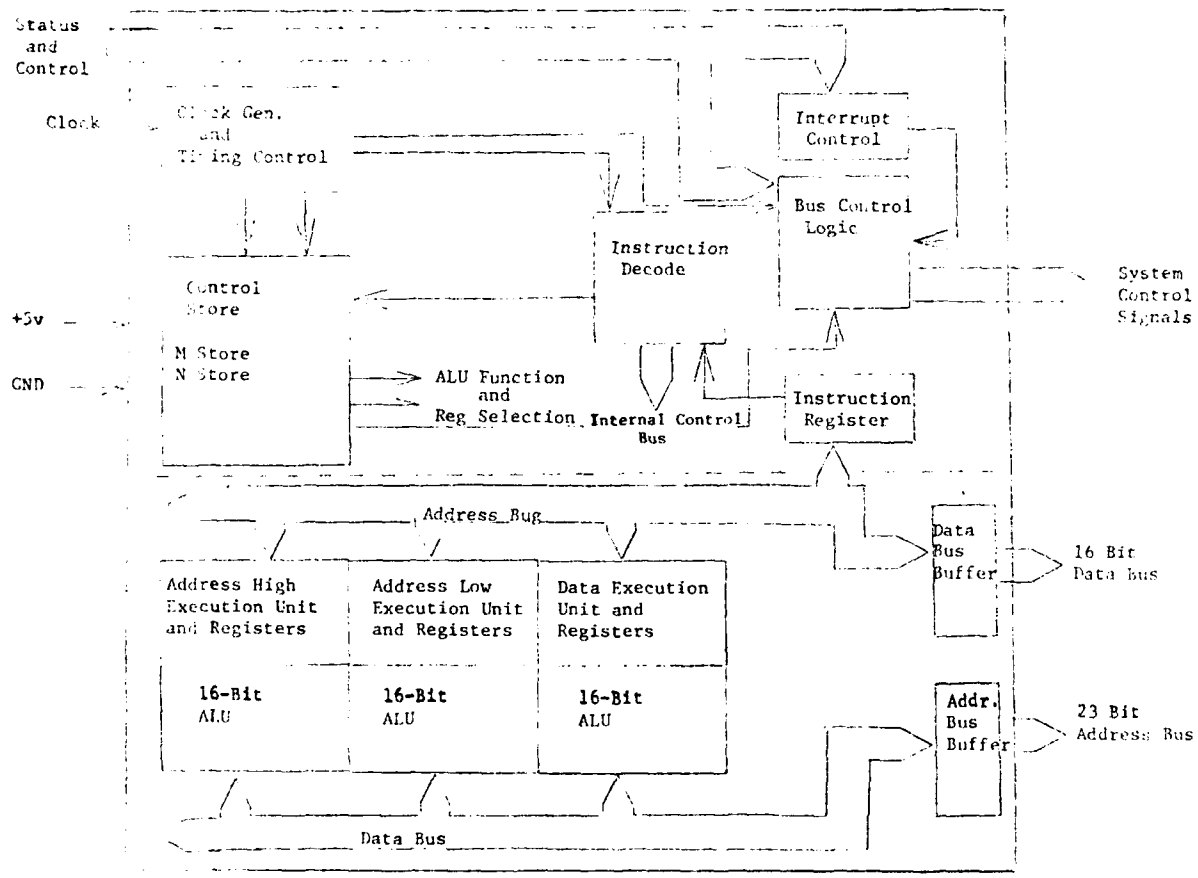


Figure 1.0 MC68000 Block Diagram

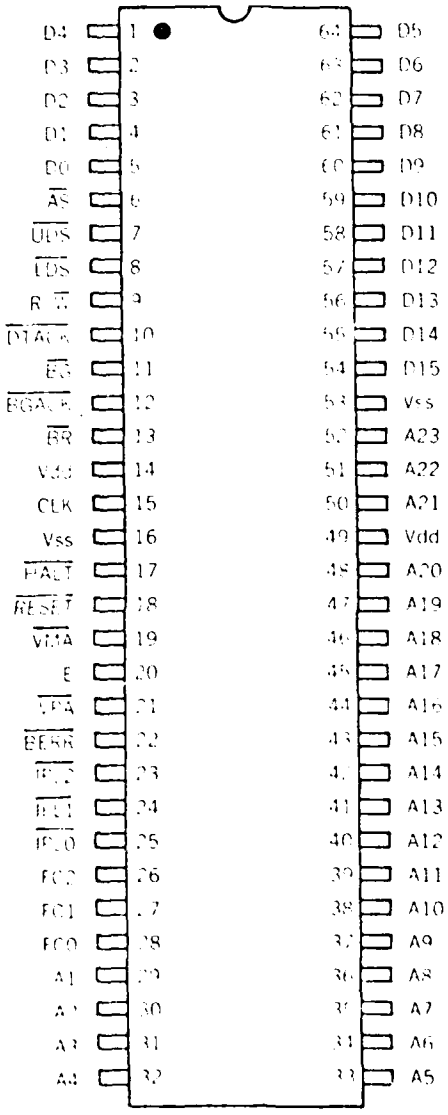


Figure 2.0 Terminal Connection and Pin Assignment

2.3.5 Upper and Lower Data Strobes (UDS-LDS)

The UDS and LDS are active low unidirectional control signals that indicate which half (upper 8 bits -UDS, lower 8 bit -LDS) are valid on the data bus during processor write operations. The UDS and LDS will always be active during processor read operations.

2.3.6 Data Transfer Acknowledge (DTACK)

The DTACK input is an active low asynchronous control line used to signal the CPU that a particular bus operation has been completed. The DTACK input is recognized by the processor on the falling edge of the input clock during CPU READ/WRITE operations. In early mask set devices (R9M, T6E) if DTACK was active by the fall of the input clock during bus cycle two (for READ/WRITE) the particular operation would be shortened by one CLK cycle. In later mask set devices (CC1) if DTACK is active at the fall of the input clock during bus cycle two it will have no effect on the overall bus operation.

2.3.7 Bus Request (BR)

This active low unidirectional input is used to signal the CPU that some other device wishes to take control of the system bus.

2.3.8 Bus Grant (BG)

The active low unidirectional output is used to signal other potential bus masters that the CPU will release the bus following completion of the current bus operation.

2.3.9 Bus Grant Acknowledge (BGACK)

This active low unidirectional input is used to signal the CPU that another device has control of the system bus.

2.3.10 Interrupt Control (IPL0, IPL1, IPL2)

These three active low unidirectional inputs are used by other devices that request a CPU interrupt. The three inputs allow seven levels of prioritized interrupts with level zero being the lowest priority.

2.3.11 Bus Error (BERR)

This active low unidirectional input is used to signal the CPU when a problem has occurred during a bus operations. It is used in conjunction with HALT to determine if the operation should be retried or the processor should initiate exception processing.

2.3.12 Reset

This bi-directional active low signal is used in conjunction with the HALT line to reset the CPU (system initialization sequence). In addition it is used to reset peripheral devices (see reset instruction).

2.3.13 HALT

The active low bi-directional signal is used to halt the processor at the end of a current bus cycle or to indicate the processor has halted due to a system failure.

2.3.14 Enable (E)

The unidirectional tri-state output is used to synchronously interface M6800 peripheral devices with the MC68000. The E output is a divide by ten of the input clock. The state of E output cannot be determined following a power on reset sequence.

2.3.15 Valid Peripheral Address (VPA)

This active low unidirection input indicates that the device being addressed and the subsequent data transfer should be synchronized to the MC68000 by the use of the E signal. If active low during an interrupt this signal indicates to the processor that auto vectoring should be used.

2.3.16 Valid Memory Address (VMA)

This active low unidirectional output indicates that the address on the bus is valid and that the device being addressed (M6800) is in sync with the processor.

2.3.17 Processor Status (FC0, FC1, FC2)

These three unidirectional tri-state output signals indicate the state of the present processor operation (user or supervisor) and the type cycle being executed.

2.3.18 CLOCK (CLK)

This unidirection input is the primary processor clock. The clock input waveform should be a signal having a 50% duty cycle and vary in frequency from 3 MHZ to 10 MHZ.

2.3.19 Signal Summary

All MC68000 signals are TTL compatible signals. The signal descriptions given in this section have been abbreviated and serve to familiarize the reader with the device and to point out some areas of interest that were discovered during characterization and are not mentioned in the vendors users guide. A more detailed description of the device pins and their function can be found in the Motorola Users Guide MC68000UM (AD2).

3.0 ELECTRICAL CHARACTERIZATION PROGRAM DEVELOPMENT

3.1 TEST EQUIPMENT

Due to the complexity of the MC68000 and the asynchronous bus structure of the device, an extensive amount of hardware was necessary in order to develop the function test vectors that would be used during the device characterization. The hardware included:

- In-house 16-bit Proto-typing System
- MDS-800 Development System
- HP 1615A Logic Analyzer
- IBM System S/370 (Editor)
- Macrodata MD-501 LSI Tester

The procedure for developing the software was to load a MC68000 test program into the proto-type system using the MDS-800 Development System. The program was then executed and the device outputs monitored using the H.P. 1615A Logic Analyzer. After determining the sequence in which the processor executed the program, the assembly code necessary to generate the Binary tester pattern for each clock cycle of execution was entered and properly coded with the aid of an IBM S/370 editor. The software was then downlinked to magtape and transferred to the Macrodata MD-501 LSI tester for final compilation and assembly into a Binary format. All device testing (functional, AC and DC) was performed using the MD-501. The Macrodata MD-501 is a 10 MHZ, 64 channel LSI tester. All 64 channels can be configured as either input, output or as a power supply. All power supplies are accurate to within 0.1% of their programmed value. All AC measurements are accurate to within ± 1ns.

3.2 Functional Testing

3.2.1 Logic Block Element Testing

Functional test software development was broken into two categories. The first category was Logic Block Element Testing (LBET). The objective was to stimulate the various logic sections of the device using a minimum number of instructions to insure that each of the relatively large functional blocks were operational, prior to instituting the very long and detailed instruction decode verification testing. The categories to be tested were:

- Reset
- Register, Array
- PC Test
- ALU
- Stack Test
- Interrupts

The reset test verifies the power-on reset sequence and the reset and halt instructions are operational.

The register array test ensures the integrity of each of the data and address registers. Pattern sensitive data is loaded into each register and checked for proper loading. In addition all other registers are tested for any possible adjacent register disturbance.

The objective of the ALU test is to insure functionality of the ALU. This is accomplished by executing all arithmetic and logical operations and testing the resulting output.

The PC and stack test verify operation of the program counter and supervisor stack pointer, by incrementing and where feasible decrementing each counter through overflow or underflow.

The interrupt test verifies the processor will respond to all levels of interrupt and that the proper interrupt vector location is executed for each level of interrupt.

3.2.2 Instruction Decode

The level of complexity of the MC68000 (56 instructions and 14 different addressing modes) makes testing of all instructions a very lengthy process. The approach to instruction testing was to break the instruction set into six categories. These categories were:

- Data movement
- Arithmetic operations
- Shift, rotates and logicals
- BCD operations
- Bit Test Operations
- Program/System Control

A detailed description of each program and the opcodes tested are given in Appendix A. When the functional test programs are converted to the conventional (Binary) format the result was over 13,000 lines of executable code. Due to the length of the Binary patterns they are not included within this document. However, they can be obtained from Rome Air Development Center (RADC) Reliability Branch. These patterns represent the forced and expected data by clock cycle for the automatic test equipment stimulation (MD-501) of the MC68000 device.

3.3 A.C. PERFORMANCE TEST DEVELOPMENT

The primary objective of the AC Test Development was to measure all of the most critical delays that are associated with the MC68000. The functional test patterns were used to precondition the device to a known state prior to performing the required measurement. The baseline used to determine which delays would be measured was the vendors data sheet. The delays shown in Table 1.0 are the actual delays that are measured using the MD-501. All measured times are accurate within $\pm$ 1ns. Due to the enable output (E) being in an undetermined state after power-on reset it was necessary to obtain the

AC PERFORMANCE SPECIFICATION MC68000

TEST	SYMBOL	FIG. NO.	REF. NO.	UNITS	NOTES	CONDITION
DIN TO CLK LOW (TSET)	TSICL	1	47	NS		VCC = +5.0 VOLTS
DIN TO CLK LOW (THOLD)	THDICL	1	47	NS		FREQ = [illegible] MIN
DTACK TO CLK LOW (TSET)	TSDTC	1	47	NS		[illegible]
BR TO CLK LOW (TSET)	TSBRCL	1	47	NS		FOR ALL TESTS
BR TO CLK LOW (THOLD)	THBRCL	1	47	NS		
BGACK TO CLK LOW (TSET)	TSBGCL	1	47	NS		
BGACK TO CLK LOW (THOLD)	THBGCL	1	47	NS		
VPA TO CLK LOW (TSET)	TSVPACL	1	47	NS		
VPA TO CLK LOW (THOLD)	THVPACL	1	47	NS		
BERR TO CLK LOW (TSET)	TSBERCL	1	47	NS		
BERR TO CLK LOW (THOLD)	THBERCL	1	47	NS		
CLK WIDTH LOW	TCL	1	2	NS		
CLK WIDTH HIGH	TCH	1	3	NS		
CLK HIGH TO FC VALID	TCLAV	1	6	NS		
CLK HIGH TO AS LOW	TCHSLX	1	9	NS		
CLK HIGH TO AS LOW	TCHSLN	1	10	NS	⊥	
CLK HIGH TO DS LOW	TCHSLX	1	9	NS		
CLK HIGH TO DS LOW	TCHSLN	1	10	NS	⊥	
CLK LOW TO AS HIGH	TCLSH	1	12	NS		
CLK LOW TO DS HIGH	TCLSH	1	12	NS		
CLK H TO R-W H	TCHRHX	1	18	NS		
CLK H TO R-W H	TCHRHN	1	19	NS	⊥	
CLK HIGH TO R-W LOW	TCHRL	1	20	NS		
CLK L TO DOUT VALID	TCLDO	1	23	NS		
CLK L TO ADDR. VALID	TCLAV	1	6	NS		
CLK HIGH TO BG LOW	TCHGL	1	33	NS		
CLK HIGH TO BG HIGH	TCHGH	1	34	NS		
CLK LOW TO VMA LOW	TCLVML	1	40	NS		
[illegible]	[illegible]	1	40	NS		
CLK LOW TO E LOW	TCLEL	1	41	NS		
CLK LOW TO E HIGH	TCLEH	1	41	NS		
CLK H TO ADDR. FC T.S.	TCHAZX	1	7	NS		OUTPUTS +-0.5V
CLK H TO ADDR. INVALID	TCHAZ	1	8	NS	⊥	OUTPUTS +-0.5V
CLK HIGH TO AS T.S.	TCHST	1	16	NS		OUTPUTS - 0.5V
CLK HIGH TO R-W T.S.	TCHRZ	1	24	NS		OUTPUTS - 0.5V
CLK HIGH TO DATA T.S.	TCHAZX	1	7	NS		OUTPUTS +-0.5V

Table 1.0

AC PERFORMANCE SPECIFICATION MC68000

TEST	SYMBOL	FIG. NO.	REF. NO.	UNITS	NOTES	CONDITIONS
ADDR VALID TO AS LOW	TAVSL	1	11	NS		DERIVED DELAYS
AS LOW TO ADDR INVALID	TSLAZ	1	13	NS		
AS LOW WIDTH LOW	TSL	1	14	NS		
AS LOW WIDTH HIGH	TSH	1	15	NS		
DS HIGH TO RW HIGH	TSHRH	1	17	NS		
ADDR VALID TO RW LOW	TAVRL	1	21	NS		
RW LOW TO DS LOW	TRLSL	1	22	NS		
DS HIGH TO DOUT INVALID	TSHDO	1	25	NS		
DS HIGH TO DIN INVALID	TSHDI	1	29	NS		
DS LOW TO EG LOW	TSLEGL	1	35	CLKS		
BG HIGH TO BG HIGH	TBHBGH	1	36	CLKS		
BGACK LOW TO EG HIGH	TGALGH	1	37	CLKS		
BG LOW TO BGACK LOW	TGLGL	1	38	CLKS		
BG WIDTH HIGH	TGH	1	39	CLKS		
VMA LOW TO E HIGH	TVMLEH	1	43	CLKS		
CS,AS HIGH TO VPA HIGH	TSHVPH	1	44	NS		
E LOW TO ADDR INVALID	TELAI	1	45	NS		
E CLOCK WIDTH	TECL	1	46	CLKS		
DTACK LOW TO DTACK LOW	TDELDAL	1	48	NS		
E WIDTH HIGH	TEH	1	50	NS		
E WIDTH LOW	TEL	1	51	NS		

Table 2.0

TEST	SYMBOL	CONDITIONS	UNITS	TEST TEMP. CODE	COMMENTS
ICC TEST	ICC	VCC = 5.5V	MA		VCC = 5.5VOLTS
VOL A23-1,FC0-2,B6,E	VOL	IOL = 3.2MA	VOLTS		VCC = 4.5VOLTS
VOL HALT	VOL	IOL = 1.6MA	VOLTS		"
VOL AS,R/W,DIS-0 UDS,LDS,VMA	VOL	IOL = 5.3MA	VOLTS		"
VOL RESET	VOL	IOL = 5.0MA	VOLTS		"
VOH (ALL OUTPUTS)	VOH	IOH = 400UA	VOLTS		
IIH (ALL INPUTS)	IIH	VIH = 2.4 VOLTS	UA		
IIL (ALL INPUTS)	IIL	VIL = 0.4 VOLTS	UA		
IOHZ (ALL OUTPUTS)	IOHZ	VOH = 2.4 VOLTS	UA		
IOLZ (ALL OUTPUTS)	IOLZ	VOL = 0.4 VOLTS	UA		
VIH (ALL INPUTS)	VIH	VGS TEST	VOLTS		VCC = 4.5
VIL (ALL INPUTS)	VIL		VOLTS		VCC = 4.5

Table 3.0

test mode for syncing the E output from Motorola. This information is considered proprietary and thus cannot be disclosed in this document. The delays shown in Table 2.0 are referred to as derived delays. These delays are output to output delays and are not directly measured by the MD-501 but are calculated based upon data obtained from the measured delays. Additional delays not specified by the vendor were measured and used to calculate these output to output delays.

The output loads used during AC testing were based upon the vendors recommended load circuit. The output load circuits are shown in Figure 3.0. A modification to the vendors load circuit was required to properly measure the tri-state delays. In Figure 3.0 the resistor Rx was added during tri-state measurements only. The resistor Rx when in parallel with R1 will make the pull-down resistance equal to the pull-up resistance (Rn). This will result in the outputs which are at a high level (logic 1) prior to tri-stating having the same tri-state fall transition as the rise time of the outputs which are at a low level (logic 0) prior to tri-stating. Without this loading change fall times exceed 2 to 3 clock cycles of decay (fall) time and are immeasurable by most modern ATE.

3.4 DC PARAMETRIC TEST DEVELOPMENT

The D.C. tests developed to evaluate the MC68000 are shown in Table 3.0. The baseline for test development was the vendors data sheet. Icc was measured dynamically (device running). In all tests Vcc was set to worse case. It was necessary to use the special tester configuration to sync Enable (E) and (VMA) outputs for D.C. measurements. All other test conditions were obtained from the vendors data sheet.

3.5 MAXIMUM OPERATING FREQUENCY (FMAX) TEST DEVELOPMENT

Due to the very high operating frequency (Fmax) of the MC68000 (8 MHZ - 10 MHZ) it was necessary to develop a method of determining the High Frequency limit of device operation. The exchange functional test pattern was used to implement an FMAX test. The FMAX test insures the MC68000 is operating correctly for the following frequencies:

- 4.0 MHZ
- 5.8 MHZ
- 7.14 MHZ
- 7.7 MHZ
- 8.3 MHZ

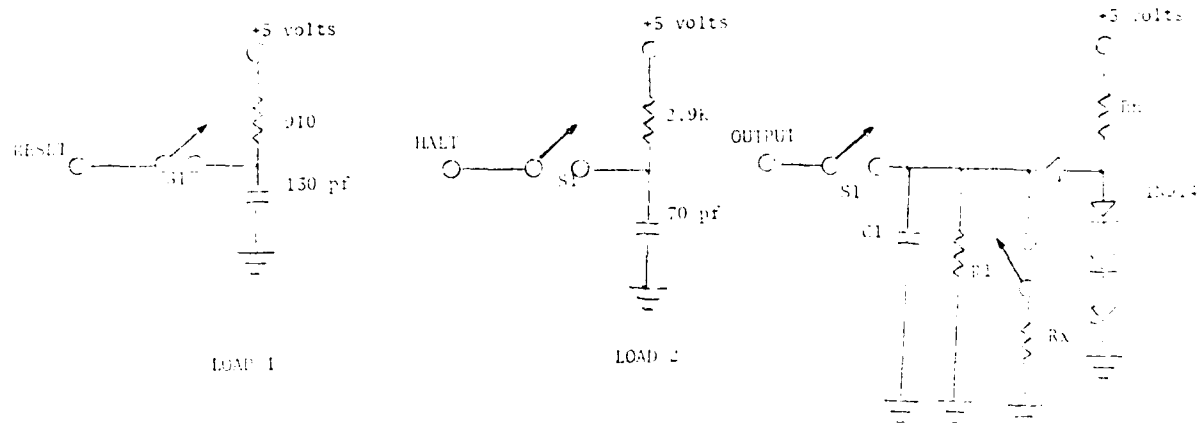
The upper limit is the maximum that could be achieved by the 10 MHZ MD-501.

3.6 CHARACTERIZATION PROGRAM SUMMARY

The finalized characterization program used to evaluate the MC68000 consisted of all the previously described tests except the LBET which is used for preliminary verification on development products only. Each test block

was varied by frequency, and/or Vcc variations as necessary to determine the MC68000 operability limitations. The test compendiums is repeated at -65°C, 25°C and +110°C case temp. A brief summary of the specified test variations follows.

All DC tests were measured at worse case supplies. All functional tests were executed at two frequencies (2.0 - 2.88 MHZ) with Vcc = 4.5v-5.5v. The FMAX test was performed at Vcc = 4.5v -5.5v. All AC performance measurements were made with Vcc = 5.0v and an operating frequency of 2 MHZ. Shown in Appendix B is a sample test run of the MC68000 characterization program.



LOAD 3 R1= 6.0K

Rx = 1.0K

LOAD 4 R1= 6.0K

Rx= 1.5K

Rn = 1.22K for AS, BG, E, FG1-2
= 740 for all other outputs

Figure 3.0 Output Load Circuit

T6E Device Functional Fail Summary

TEST	TEMP	Vcc @ 1MHz	Vcc @ 2.0MHz	Vcc @ 2.85MHz	COMMENTS
		4.5 4.75 5.0 5.25 5.5	4.5 4.75 5.0 5.25 5.5	4.5 4.75 5.0 5.25 5.5	
RESET	-55				
	+25				
	+100	X X	X	X	Reset Instruction
MEMORY CYCLE:	-55				
	25				
	+100				
PROGRAM	-55				
COUNTER:	25				
	+100	X X X	X X	X X	P. C. Fail
STACK	-55				
POINTER:	25				
	+100	X X X	X X X	X X	Stack Fail
REGISTER	-55				
ARRAY:	25				
	+100				
ALU:	-55				
	25				
	+100	X X	X		
PROCESSOR	-55				
INTERRUPT:	25				
	+100	X X X	X X	X X	Stack Fail

Device #: 2
Date: 7/22/80

TABLE 4.0

TEST	TEMP	Vcc @ 1MHz					Vcc @ 2.0MHz					Vcc @ 2.85MHz					COMMENTS
		4.5	4.75	5.0	5.25	5.5	4.5	4.75	5.0	5.25	5.5	4.5	4.75	5.0	5.25	5.5	
RESET	-55																
	+25																
	+100	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Reset Instruction
MEMORY CYCLE:	-55																
	25																
	100																
PROGRAM COUNTER:	-55																
	25																
	100	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	PC Increment
STACK POINTER:	-55																
	25																
	100	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	SP Addr. Pins Lbyte
REGISTER ARRAY:	-55																
	25																
	100																
ALU:	-55																
	25																
	100																
PROCESSOR INTERRUPT:	-55																
	25																
	100	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	XRTG = 36

Device #: [illegible]
Date: 7/22/[illegible]

Table 4.1

TEST	TEMP	Vcc @ 1MHz	Vcc @ 2.0MHz	Vcc @ 2.85MHz	COMMENTS
		4.5 4.75 5.0 5.25 5.5	4.5 4.75 5.0 5.25 5.5	4.5 4.75 5.0 5.25 5.5	
RESET	-55				
	25				
	100				
MEMORY CYCLE:	-55				
	25				
	100				
PROGRAM	-55				
COUNTER:	25				
	100	X			P.C. Increment
STACK	-55				
POINTER:	25				
	100	X			SP 1byte Write
REGISTER	-55				
ARRAY:	25				
	100				
ALU:	-55				
	25				
	100				
PROCESSOR	-55				
INTERRUPT:	25				
	100	X			SP 1byte Write

Device #: 5
Date: 7/27/[illegible]

Table 4.2

TEST	TEMP (°C)	Vcc @ 1MHz	Vcc @ 2.0MHz	Vcc @ 2.85MHz	COMMENTS
		4.5 4.75 5.0 5.25 5.5	4.5 4.75 5.0 5.25 5.5	4.5 4.75 5.0 5.25 5.5	
RESET	-55				
	25				
	100				
MEMORY CYCLE:	-55				
	25				
	100				
PROGRAM COUNTER:	-55				
	25				
	100	X			P.C. Increment
STACK POINTER:	-55				
	25				
	100	X			SP Lbyte Write
REGISTER ARRAY:	-55				
	25				
	100				
ALU:	-55				
	25				
	100				
PROCESSOR INTERRUPT:	-55				
	25				
	100				

Device #: [illegible]
Date: [illegible]

Table 4.3

TEST	TEMP	Vcc @ 1MHz	Vcc @ 2.0MHz	Vcc @ 2.85MHz	COMMENTS
		4.5 4.75 5.0 5.25 5.5	4.5 4.75 5.0 5.25 5.5	4.5 4.75 5.0 5.25 5.5	
RESET	-55				
	25				
	100				
MEMORY CYCLE:	-55				
	25				
	100				
PROGRAM	-55				
COUNTER:	25				
	100	X			P.C. Increment
STACK	-55				
POINTER:	25				
	100	X			SP Lbyte Write
REGISTER	-55				
ARRAY:	25				
	100				
ALU:	-55				
	25				
	100	X			Extended Div Time
PROCESSOR	-55				
INTERRUPT:	25				
	100	X			SP Lbyte Write

Device #: 7
Date: 7/22/80

Table 4.4

TEST	TEMP	Vcc @ 1MHz	Vcc @ 2.0MHz	Vcc @ 2.85MHz	COMMENT
		4.5 4.75 5.0 5.25 5.5	4.5 4.75 5.0 5.25 5.5	4.5 4.75 5.0 5.25 5.5	
RESET	-55				
	25				Processor Dead
	100	X			(no reset)
MEMORY CYCLE:	-55				
	25				
	100				
PROGRAM	-55				
COUNTER:	25				
	100	X X	X	X	P.C. Increment
STACK	-55				
POINTER:	25				
	100	X X	X	X	SP Hbyte Write
REGISTER	-55				
ARRAY:	25				
	100	X			XRTG = 197
ALU:	-55				
	25				
	100	X X	X	X	XRTG = 80
PROCESSOR	-55				
INTERRUPT:	25				
	100	X X	X	X	XRTG = 36

Device #: 3
Date: 7/22/80

Table 4.5

4.0 DEVICE EVALUATION

4.1 The data base used in evaluating the MC68000 was quite extensive. It involved three mask set iterations, devices with very noticeable process changes in addition to samples from one second source vendor (Hitachi).

The preliminary evaluation of the MC68000 was performed using the R9M mask set XC68000 device. This mask set of devices was the first set released by the vendor for user evaluation. It was not a fully functional device and therefore was shortly replaced with the T6E mask set. The R9M mask set was not evaluated using the characterization program due to the functional anomalies that were present.

The following mask set devices were evaluated using the existing characterization program.

- o T6E (10 pcs)
- o CC1 - 8 MHZ (10 pcs)(early)
- o CC1 - 10 MHZ (5 pcs)
- o CC1 - 8 MHZ (5 pcs)(late)
- o T6E - Hitachi (6 pcs)

4.2 T6E DEVICE EVALUATION

The T6E mask set devices were tested prior to completion of the instruction decode test and AC/DC performance test. Therefore early analysis of the device was performed using the Logic Block element test (LBET) software only. Week codes for these devices were 8013 and 8019.

Shown in Table 4.0-4.5 are the functional failures for the T6E devices. The 10 samples were tested with one device indicating no functionality at +25°C. This device was deleted from the remaining tests. The remaining 9 pcs of the XC68000 (T6E) were all functional at 25°C and -55°C TCASE. Problems with 6 of the devices occurred between 90°C and 100°C (TCASE) most notably with Vcc = 4.5 volts and FREQ = 1.0 MHZ. The nature of the failure centered on small geometry devices that were either leaking or failing to keep the internal bus precharged at slow frequencies and high temperature. When the device is operated at a slow frequency 1.0 - 3.0 MHZ and at an elevated temperature (<70°C) it is believed that the nodes were not maintaining (bleeding-off) the precharged level. This resulted in the address being lost prior to being latched into the output buffer logic. This anomaly was seen in the Program Counter Test, Stack Pointer Test and (on some devices), the Reset Test.

The software was modified to perform the functional tests at 2.0 MHZ and 2.88 MHZ in addition to the 1.0 MHZ test. The data in Table 4.0 - 4.5 indicates that functionality improved with increasing frequency due to the fact that the dynamic like nodes have less time to bleed-off prior to being latched into the output buffer. This problem was to be corrected on later devices and prompted an evaluation of the CC1 (8 MHZ) MC68000 mask set. Motorola,

however, changed the minimum operating frequency to 2.0 MHZ, and finally 3.0 MHZ in order to allow for the faster 8, and 10 MHZ drivers being developed

4.3 CCI (8 MHZ) DEVICE EVALUATION

4.3.1 Functional Testing

The first evaluation of the CCI mask set MC68000 was performed on 10 devices. The devices were week coded 8105.

The devices were initially screened across the mil-temp range of -55°C to +125°C (TCASE). The functional performance of the devices at the +125°C was degraded significantly from the +110°C (TCASE) performance. This resulted in the loss of a majority of the functional dependent AC-DC performance data. In evaluating the cause of the device failures it was discovered that at the elevated case temperature of +125°C, the θjc of the device (the temperature difference between junction temperature and case temperature) was approximately 10-15°C/watt. At the case temperature of 125°C, the junction temperature of a device dissipating 750 mw would be in excess of 135°C. At the date of manufacture the vendor was varying his process in order to optimize his yield and it is doubtful that the process would support functionality at this elevated temperature. The data taken at +110°C (TCASE) indicated acceptable device performance therefore functional testing was performed across a temp-range of -55°C to +110°C (TCASE).

Shown in Table 5.0-5.2 is a summary of the functional test results obtained during device testing. Due to the lengthy test time (approximately 25 min) required to test each device, the LBET portion of the functional test was bypassed. One device was found non-functional at room-temperature testing after delivery and was therefore deleted from the remaining temperature test runs.

At the -55°C (TCASE) test functional failures were noted on devices #1, #8. Device #8 exhibited high Vcc (5.5 volts) fails on select tests. The failure mechanism was found to be the status register in that during the op-code execution of CMP D5, D3, and Ext D3 (Byte) the EXTEND bit in the status register was being set. Device #1 exhibited similar failures at different Vcc levels. When tested at 25°C (TCASE) device #1 exhibited similar failures to those that were noted at the -55°C temp. test. All other devices were fully functional. The final temp. test was performed at +110°C (TCASE). Functional failures were noted on devices #7, #9. Device #7 would not process out of RESET vector Ø (power-on RESET) for any functional tests. Device #9 exhibited low Vcc (4.5 volt) fails on select tests. The failure mechanism centered on the inability of AS and DS to function properly during processor READ/WRITE operations. While this lot of devices showed significant improvement in functionality over previous T6E devices, IBM pursued testing of more mature CCL MASK product at 10 MHZ and a re-test of 8 MHZ devices to obtain full functionality at the mil temperature extremes.

INSTRUCTION DECODE FAILURE SUMMARY MC68000-LC1
(FAILURES BY DEVICE NUMBER)

SAMPLE LOT : 9 PCS CC1
WEEK CODE : 8105

FUNCTIONAL TEST DESCRIPTION	VCC	FREQ MHZ @ -55C 2.00	FREQ MHZ @ -55C 2.85	FREQ MHZ @ 0C 2.00	FREQ MHZ @ 0C 2.85	FREQ MHZ @ +25C 2.00	FREQ MHZ @ +25C 2.85	FREQ MHZ @ +110C 2.00	FREQ MHZ @ +110C 2.85	FREQ MHZ @ +125C 2.00	FREQ MHZ @ +125C 2.85	COMMENTS
EXG INST. TEST	4.5									2.9	2.9	DEVICE 6 FAILS ALL TESTS @ +125C
	5.0									2	2	
	5.5									2	2	DEVICE 7 FAILS ALL TEST @ 110/125C
LEA INST. TEST	4.5	1	1							2.9	2.9	
	5.0									2	2	
	5.5									2	2	
MOVE INST. TEST	4.5	1	1	1	1	1	1			2.9	2.9	
	5.0									2.9	2.9	
	5.5									2.9	2.9	
LINK, UNLINK INST. TEST	4.5									2.9	2.9	
	5.0	1	1	1	1	1	1	1	1	2	2.9	
	5.5									2	2.9	
MOVE INST. TEST	4.5									2.9	2.9	
	5.0									2	2	
	5.5									2	2	
MOVEM INST. TEST	4.5									2.9	2.9	
	5.0	1	1	1	1	1	1	1	1	2	2.9	
	5.5									2	2.9	
MOVEP INST. TEST	4.5									2	2.9	
	5.0									2	2.9	
	5.5									2	2.9	
MOVEA INST. TEST	4.5									2.9	2.9	
	5.0									2	2	
	5.5									2	2	
DBCC INST. TEST	4.5									2.9	2.9	
	5.0									2	2	
	5.5									2	2	

Table 5.0

[illegible] INST. TEST	4.5									2.9	2.9
	5.0									2	2
	5.5									2	2
ADD, ADDU INST. TEST	4.5									2.9	.9
	5.0									2.9	2.9
	5.5									2.9	2.9
ADDX INST. TEST	4.5									2.9	2.9
	5.0									2	2
	5.5									2	2
CLR INST. TEST	4.5	1	1	1	1	1	1	1		.99	.99
	5.0									2.9	2.9
	5.5				1					2.9	.9
CMP, CMPI, CMPM INST. TEST	4.5									[illegible]	[illegible]
	5.0									2.9	2.9
	5.5	6								2.9	2.9
DIV, DIVS INST. TEST	4.5							9	9	2.9	.9
	5.0									2	2
	5.5									2	2
EXT INST. TEST	4.5									2.9	.9
	5.0									2	2
	5.5	6								2	2
MULU, MULS INST. TEST	4.5							9	9	.99	.99
	5.0									2	2
	5.5									2	2
NEG, NEGX INST. TEST	4.5									2	2
	5.0									2.9	.9
	5.5									2.9	.9
SUB, SUBI, SUBQ, SUBX INST. TEST	4.5									[illegible]	[illegible]
	5.0									[illegible]	[illegible]
	5.5									[illegible]	[illegible]

Table 5.1

TAS, TST INST. TEST	4.5									249	249
	5.0									2.4	2.4
	5.5									2.4	2.4
AND, ANDI INST. TEST	4.5	1	1	1	1	1	1			249	249
	5.0									2.4	2.4
	5.5									2.4	2.4
OR, ORI, EOR INST. TEST	4.5									2459	2459
	5.0									245	245
	5.5									245	245
NOT, SHIFT, ROTATE INST. TEST	4.5	1	1	1	1	1	1	9		2459	2459
	5.0									245	245
	5.5									245	245
BIT (TST, SET, CLR, CHG) INST. TEST	4.5									259	259
	5.0									2	2
	5.5									2	2
BCD (ADD, SUB, NEG) INST. TEST	4.5							9		2459	2459
	5.0									2.4	2.4
	5.5									2.4	2.4
BRANCH, JUMP, RETURN INST. TEST	4.5							9		2459	2459
	5.0	1	1	1	1	1	1			2.4	2.4
	5.5									2.4	2.4
SDDA, SUBA, CMPA INST. TEST	4.5									2459	2459
	5.0									245	245
	5.5									245	245
MUSP, MSR, MCCR INST. TEST	4.5									259	259
	5.0									2.5	2.5
	5.5									2.5	2.5
TRAP, TRAPV INST. TEST	4.5									2459	2459
	5.0									245	245
	5.5									[illegible]	245

Table 5.2

4.3.2 DC Parametric Tests

The minimum and maximum data values obtained across the tested temperature range are shown in Table 5.3. It was noted that one device exhibited a slightly lower VOL (2.35 volts) than desired on the Enable output It was later learned that the enable output would be redesigned. Power dissipation was found to be 1.1 watts worse case (Vcc = 5.5 volts @ -55°C TCASE). This was within the vendors specification of 1.2 watts max. All remaining DC parameters were within the vendors specification.

4.3.3 FMAX Testing

FMAX testing indicated all devices to be operating at an FMAX of approximately 7.1 to 7.7 MHZ. The maximum frequency of operation occurs at the -55°C TCASE temperature. The 8 MHZ commercial temperature devices being tested were adequate to meet 6 MHZ military temperature operations. Therefore, the 6 MHZ commercial specifications for frequency and performance were used as pass/fail criteria for the devices in a military temperature environment.

4.3.4 AC Performance Testing

All devices were tested across the temp range of -55°C to +110°C TCASE. Shown in Table 5.4 - 5.5 are the min-max summary for all measured delays. All devices met the vendors 0°C - 70°C specification for a 6 MHZ device. It was noted during testing that the clock pulse width high delay (tcH) seemed to track with the frequency of the device. Through experimentation and later correlation it was found that the frequency of the device could be determined (± 0.5 MHZ) by the following equation.

$$FMAX = 1/[2(Tch) + trise + tfall]$$

Where: trise + tfall = 6ns

Using this method of determining FMAX it was found that worse case FMAX was:

$$\begin{aligned} FMAX &= 1/[2(61)ns + 6ns] \\ &= 1/128\ us \\ &= 7.8\ MHZ \end{aligned}$$

This clearly indicated the 8 MHZ 0°C - 70°C devices could meet an FMAX of 6.0 MHZ across the temperature range of -55° to +110°C (TCASE).

4.3.5 MC68000L8 Test Summary

Overall the AC, DC and FMAX performance was found to be acceptable when compared to a 6 MHZ device specification. However, functionally the devices exhibited some unusual anomalies at the lower (-55°C) test temp. It should be noted that the devices which exhibited the cold-temperature failures were the devices having the highest FMAX. This tends to point out a parameter of the process (threshold, or ion implantation) that results in increased performance but does not support functionality at the -55°C TCASE temperature.

REPORT TITLE -- MC68000 DC PARAMETRIC TEST RADC CCL MASK SET PARTS 3 PCS SAMPLE [illegible]
DATE CODE [illegible]

TEST	SYMBOL	CONDITIONS	SPEC. MIN	SPEC. MAX	IBM TEST DATA MIN	IBM TEST DATA MAX	UNITS	COMMENTS
[illegible]		FREQ [illegible]MHZ VCC=5.5V		219	[illegible]	[illegible]	[illegible]	VCC = [illegible]
[illegible]		IOL = 3.2MA		0.5	[illegible]	[illegible]	VOLTS	VCC = [illegible]
[illegible]		IOL = 1.6MA		0.5	[illegible]	[illegible]	"	"
[illegible]		IOL = 5.0MA		0.5	[illegible]	[illegible]	"	"
[illegible]		IOL = 5.0MA		0.5	[illegible]	[illegible]	"	"
[illegible]		IOH = 400UA	2.4		[illegible]	[illegible]	"	[illegible]
[illegible]		VIH = 2.4 VOLTS		1.0	-	[illegible]	[illegible]	
[illegible]		VIL = 0.4 VOLTS		1.0	-	[illegible]	"	
[illegible]		VOH = 2.4 VOLTS		2.0	-	[illegible]	"	
[illegible]		VOL = 0.4 VOLTS		2.0	-	[illegible]	"	
[illegible]		[illegible]			[illegible]	[illegible]	[illegible]	VCC = [illegible]
[illegible]					[illegible]	[illegible]	"	VCC = [illegible]

Table 5.3

REPORT TITLE --- MOTOROLA MC68000 AC PERFORMANCE TESTS --- RADC CC1 MAG SCT PARTS [illegible]

TEST	SYMBOL	CONDITIONS	SPEC. MIN	SPEC. MAX	IBM TEST DATA MIN	IBM TEST DATA MAX	UNITS	COMMENTS
DIN TO CLK LOW (TSET)	TDICL		25	-	0	3	NS	TEMP [illegible]
DIN TO CLK LOW (THOLD)	THDICL		-	-	[illegible]	4	"	[illegible]
DTACK TO CLK LOW (TSET)	TSDTCL		25	-	-1	[illegible]	"	
BR TO CLK LOW (TSET)	TSBRCL		25	-	2	[illegible]	"	
BR TO CLK LOW (THOLD)	THBRCL		-	-	[illegible]	[illegible]	"	
BGACK TO CLK LOW (TSET)	TSBGCL		25	-	3	[illegible]	"	
BGACK TO CLK LOW (THOLD)	THBGCL		-	-	[illegible]	[illegible]	"	
VPA TO CLK LOW (TSET)	TSVPACL		25	-	[illegible]	[illegible]	"	REQUIRES SPECIAL TEST [illegible]
VPA TO CLK LOW (THOLD)	THVPACL		-	-	[illegible]	[illegible]	"	
BERR TO CLK LOW (TSET)	TSBERCL		25	-	2	[illegible]	"	
BERR TO CLK LOW (THOLD)	THBERCL		-	-	[illegible]	[illegible]	"	
CLK WIDTH LOW	TCL		75	250	[illegible]	39	"	
CLK WIDTH HIGH	TCH		75	250	33	61	"	
CLK HIGH TO FC VALID	TCLAV		-	80	23	65	"	
CLK HIGH TO AS LOW	TCHSLX		0	-	31	49	"	(MIN)
CLK HIGH TO AS LOW	TCHSLN		-	70	34	61	"	(MAX)
CLK HIGH TO DS LOW	TCHSLX		0	-	[illegible]	47	"	(MIN)
CLK HIGH TO DS LOW	TCHSLN		-	70	29	55	"	(MAX)
CLK LOW TO AS HIGH	TCLSH		-	80	37	75	"	
CLK LOW TO DS HIGH	TCLSH		-	80	31	63	"	
CLK H TO R-W H	TCHRHX		0	-	13	24	"	[illegible]
CLK H TO R-W H	TCHRHX		-	80	22	33	"	(MAX)
CLK HIGH TO R-W LOW	TCHRL		-	80	11	31	"	
CLK L TO DOUT VALID	TCLDO		-	80	[illegible]	[illegible]	"	
CLK L TO ADDR. VALID	TCLAV		-	80	28	70	"	
CLK HIGH TO BG LOW	TCHGL		-	80	13	32	"	
CLK HIGH TO BG HIGH	TCHGH		-	80	16	33	"	

Table 5.4

CLK LOW TO VMA LOW	TCLVML		-	80	21	42	"	REQUIRES SPECIAL TEST [illegible]
CLK HIGH TO VMA HIGH	TCHVMH		-	-	6	33	"	
CLK LOW TO E LOW	TCLEL		-	-	17	38	"	REQUIRES SPECIAL TEST [illegible]
CLK LOW TO E HIGH	TCLEH		-	-	17	3[illegible]	"	
CLK H TO ADDR. F. T.S.	TCHAZX	OUTPUTS [illegible]	[illegible]	100	[illegible]	[illegible]	"	
CLK H TO ADDR. INVALID	TSHAZ	"	0	-	40	75	"	
CLK HIGH TO AS,DS T.S.	TCHSZ	OUTPUTS - 0.5V	-	100	31	56	"	
CLK HIGH TO R/W T.S.	TCHRZ	"	-	100	[illegible]	[illegible]	"	
CLK HIGH TO DATA T.S.	TCHAZX	OUTPUTS [illegible]	[illegible]	100	[illegible]	[illegible]	"	
ADDR VALID TO AS,DS L	TAVSL		35	-	45	[illegible]	"	[illegible]
AS,DS H TO ADDR INVLD	TSHAZ		40	-	[illegible]	[illegible]	"	[illegible]
AS,DS WIDTH LOW	TSL		170	-	[illegible]	[illegible]	"	
AS,DS WIDTH HIGH	TSH		180	-	[illegible]	[illegible]	"	
DS HIGH TO R/W HIGH	TSHRH		0	-	[illegible]	[illegible]	"	
ADDR VALID TO R/W LOW	TAVRL		25	-	[illegible]	[illegible]	"	
R/W LOW TO DS LOW	TRLSL		140	-	[illegible]	[illegible]	"	
DS HIGH TO DOUT INVLD	TSHDO		40	-	[illegible]	[illegible]	"	
DS H TO DI INVLD THOLD	TSHDI		0	-	[illegible]	[illegible]	"	
BR LOW TO BG LOW	TBRLGL		-	(1)	[illegible]	[illegible]	"	[illegible]
BR HIGH TO BG HIGH	TBRHGH		-	(1)	[illegible]	[illegible]	"	
BGACK LOW TO BG HIGH	TGALGH		-	(1)	[illegible]	[illegible]	"	
BG LOW TO BUS T.S.	TGLZ		-	(2)	[illegible]	[illegible]	"	[illegible]
BG WIDTH HIGH	TGH		-	(3)	[illegible]	[illegible]	"	[illegible]
VMA LOW TO E HIGH	TVMLEH		24[illegible]	-	[illegible]	[illegible]	"	
DS,AS HIGH TO VPA HIGH	TSHVPH		-	(4)	[illegible]	[illegible]	"	[illegible]
E LOW TO ADDR INVALID	TELAI		35	-	[illegible]	[illegible]	"	
BGACK WIDTH	TBGL		-	(5)	[illegible]	[illegible]	"	[illegible]
BERR LOW TO DTACK LOW	TBELDAL		50	-	[illegible]	[illegible]	"	
E WIDTH HIGH	TEH		600	-	[illegible]	[illegible]	"	
E WIDTH LOW	TEL		900	-	981	[illegible]	"	

Table 5.5

It may also indicate a race condition or design problem with the device that precludes 1-2 MHZ testing on the faster devices. At the higher test temp. (+100°C) the functional failures seem to be frequency related and supports the position that the lower frequency limit of 2 MHZ must be changed to a minimum of 3 MHZ, based on data obtained.

4.4 MC68000L10 DEVICE TESTING

Device testing was performed on 5 pcs of the MC68000L10 devices. Week codes for these devices were 8116 and 8119. These devices were loaned out by the vendor for characterization purposes only and were off-the-shelf, 0°C - 70°C, 10 MHZ devices.

4.4.1 Functional testing

Functional tests results for the five devices tested are shown in Table 6.0 - 6.2. One device (#2) indicated functional failures at -55°C and +25°C TCASE temperature. All remaining devices were found to be functional. Generally, the failures were found to be related to low Vcc (4.5 volts), low frequency (2.0 MHZ). The failure mechanism was failure to process out of Power-on reset and loss of address during RD/write operations. When tested at +110°C TCASE device #2 and #5 indicated functional failures. Device #5 failures occurred at Vcc = 4.5 volts with Freq = 2.0 MHZ only. At the frequency of 2.85 MHZ device #5 was functional. Device #2 exhibited across the board failures at Vcc = 4.5 volts.

4.4.2 DC Testing

DC parametric testing was performed across the temperature range -55°C to +110°C TCASE. Shown in Table 6.3 is the summarized D.C. parametric data. All devices tested within the vendors specification. It was noted that the two devices (#2, #5) exhibited higher supply current values (Icc) than the remaining 3 devices. This was especially evident on device #2 which exhibited an Icc (171 MA) 5% - 10% higher than the other devices (<165 MA). It was later shown that a screen of ICC <165 MA or a functional test at 3.0 MHZ at 110°C would eliminate any potential functional fail devices.

4.4.3 FMAX Testing

All devices passed at the maximum tested FMAX of 8.33 MHZ across the temperature range of -55°C to +110°C TCASE. Calculated FMAX (see sec. 4.3.4) indicates all devices operating with FMAX = 9.2 MHZ worst case (Tc = +110°C).

4.4.4 AC Performance Testing

All 10 MHZ, 0 to 70°C commercial devices tested within the vendors' 8 MHZ specification in full mil operation, Table 6.4 shows performance measurements obtained during device testing.

[illegible] TEST INSTRUCTION DECODE FAILURE SUMMARY MC68000L10-CC1

	VCC	FREQ MHZ @ -55C 2.00	FREQ MHZ @ -55C 2.85	FREQ MHZ @ 25C 2.00	FREQ MHZ @ 25C 2.85	FREQ MHZ @ +125C 2.00	FREQ MHZ @ +125C 2.85	COMMENTS
[illegible] INST. TEST	4.5					2.5	2	
	5.0							
	5.5							
[illegible] INST. TEST	4.5					2.5	2	
	5.0							
	5.5							
P.E.A. INST. TEST	4.5					2	2	
	5.0							
	5.5							
LINK, UNLINK INST. TEST	4.5					2.5	2	
	5.0							
	5.5							
MOVE INST. TEST	4.5					2.5		
	5.0							
	5.5							
MOVEM INST. TEST	4.5					2.5		
	5.0							
	5.5							
MOVEP INST. TEST	4.5					[illegible]	2	
	5.0							
	[illegible]							
MOVEQ INST. TEST	4.5					2.5	2	
	5.0							
	5.5							

Table 6.0

[illegible] INST. TEST	4.5				2.5	2	
	5.0						
	5.5						
[illegible] INST. TEST	4.5				[illegible]	[illegible]	
	5.0						
	5.5						
[illegible] INST. TEST	4.5				2.5	2	
	5.0						
	5.5						
[illegible] INST. TEST	4.5				2.5	2	
	5.0						
	5.5						
[illegible] INST. TEST	4.5	2			2.5	2	
	5.0						
	5.5						
CMP, CMPI, CMPM INST. TEST	4.5			2	2.5	[illegible]	
	5.0						
	5.5						
DIV, DIVS INST. TEST	4.5				2.5	2	
	5.0						
	5.5						
EXT INST. TEST	4.5	[illegible]			2.5	[illegible]	
	5.0						
	5.5						
MULU, MULS INST. TEST	[illegible]				2.5	2	
	5.0						
	5.5						

Table 6.1

[illegible] - [illegible] PARAMETRIC TEST [illegible] MASK SET PARTS DEVICE [illegible]
DEVICE TYPE [illegible]

TEST	CONDITIONS	SPEC. MIN	SPEC. MAX	IBM TEST DATA * [illegible]	[illegible]	[illegible]	UNITS	COMMENTS
[illegible]	[illegible]		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]		[illegible]	[illegible]	[illegible]	[illegible]	"	"
[illegible]	[illegible]		[illegible]	[illegible]	[illegible]	[illegible]	"	"
[illegible]	[illegible]		[illegible]	[illegible]	[illegible]	[illegible]	"	"
[illegible]	[illegible]		[illegible]	[illegible]	[illegible]	[illegible]	"	
[illegible]	[illegible]		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
[illegible]	[illegible]		[illegible]	[illegible]	[illegible]	[illegible]	"	
[illegible]	[illegible]		[illegible]	[illegible]	[illegible]	[illegible]	"	
[illegible]	[illegible]		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
[illegible]	[illegible]			[illegible]	[illegible]	[illegible]	"	

Table 6.3

[illegible] INST. TEST	4.5				2.5	2	
	5.0						
	5.5						
[illegible] SUBA, SUBX INST. TEST	4.5				[illegible]	[illegible]	
	5.0						
	5.5						
[illegible] INST. TEST	4.5				[illegible]	[illegible]	
	5.0						
	5.5						
[illegible] INST. TEST	4.5				[illegible]	[illegible]	
	5.0						
	5.5						
[illegible] INST. TEST	4.5				[illegible]	[illegible]	
	5.0						
	5.5						
[illegible] INST. TEST	4.5				[illegible]	[illegible]	
	5.0						
	5.5						
[illegible] INST. TEST	4.5				[illegible]	[illegible]	
	5.0						
	5.5						
[illegible] INST. TEST	4.5				[illegible]	[illegible]	
	5.0						
	5.5						
[illegible] INST. TEST	4.5				[illegible]	[illegible]	
	5.0						
	5.5						
[illegible] INST. TEST	4.5				[illegible]	[illegible]	
	5.0						
	5.5						
[illegible] INST. TEST	4.5				[illegible]	[illegible]	
	5.0						
	5.5						
[illegible] INST. TEST	4.5				[illegible]	[illegible]	
	5.0						
	5.5						

Table 6.2

REPORT TITLE --- MOTOROLA MC68000 AC PERFORMANCE TESTS --- CEE MASK SET PARTS DEVICE : #1-5
DEVICE TYPE : C30 DATE CODE ____

TEST	SYMBOL	CONDITIONS	SPECS MIN	SPECS MAX	IDM TEST DATA* -55	IDM TEST DATA* +25	IDM TEST DATA* +110	UNITS	COMMENTS
DIN TO CLK LOW (TSET)	TDTCL		25	-	2	3	0	NS	TEMP : -55C TO +110C (CASE)
DIN TO CLK LOW (THOLD)	THDTCL		-	-	0	4	4	"	VCC = 5.0 VOLTS
DTACK TO CLK LOW (TSET)	TSDTCL		25	-	3	0	0	"	FREQ : 2.0 MHZ
BR TO CLK LOW (TSET)	TSBRCL		25	-	3	0	0	"	
BR TO CLK LOW (THOLD)	THBRCL		-	-	2	2	2	"	
BGACK TO CLK LOW (TSET)	TSBGCL		25	-	-3	-3	-3	"	
BGACK TO CLK LOW (THOLD)	THBGCL		-	-	0	-1	-1	"	
VMA TO CLK LOW (TSET)	TSVPACL		25	-	-3	-4	-5	"	
VMA TO CLK LOW (THOLD)	THVPACL		-	-	4	-1	-2	"	REQUIRES SPECIAL TEST MODE
BERR TO CLK LOW (TSET)	TSBERCL		25	-	3	2	3	"	
BERR TO CLK LOW (THOLD)	THBERCL		-	-	4	3	3	"	
CLK WIDTH LOW	TCL		75	250	26	33	31	"	
CLK WIDTH HIGH	TCH		75	250	33	43	52	"	
CLK HIGH TO FC VALID	TCLAV		-	60	30	35	55	"	
CLK HIGH TO AS LOW	TCHSLX		0		24	31	41	"	(MIN)
CLK HIGH TO AS LOW	TCHSLN		-	70	31	40	50	"	(MAX)
CLK HIGH TO DS LOW	TCHSLX		0	-	19	28	29	"	(MIN)
CLK HIGH TO DS LOW	TCHSLN			70	29	39	47	"	(MAX)
CLK LOW TO AS HIGH	TCLSH		-	60	34	40	50	"	
CLK LOW TO DS HIGH	TCLSH		-	60	31	45	53	"	
CLK HIGH TO R-W HIGH	TCHRHX		0	-	16	24	29	"	(MIN)
CLK HIGH TO R-W HIGH	TCHRHX		-	62	11	14	16	"	(MAX)
CLK HIGH TO R-W LOW	TCHRL		-	60	10	15	25	"	
CLK LOW TO DOUT VALID	TCLDO			60	30	38	50	"	
CLK LOW TO ADDR. VALID	TCLAV		-	70	43	50	50	"	
CLK HIGH TO FC LOW	TCHFL			60	12	16	26	"	
CLK HIGH TO FC HIGH	TCHFH		-	60	17	18	24	"	
CLK LOW TO VMA LOW	TCLVML		-	50	20	29	36	"	
CLK HIGH TO VMA HIGH	TCHVMH		-	-	11	16	28	"	REQUIRES SPECIAL TEST MODE
CLK LOW TO E LOW	TCLEL				15	21	31	"	
CLK LOW TO E HIGH	TCLEH		-	-	16	20	27	"	REQUIRES SPECIAL TEST MODE
CLK HIGH TO ADDR. INVALID	THCHAX	VOUT = 1.5V		15	10	21	27	"	
CLK HIGH TO ADDR. INVALID	THAZ	"	0	-	25	41	45	"	
CLK HIGH TO ADDR. VALID	THCHAX	VOUT = 0.5V	-	15	40	47	51	"	
CLK HIGH TO ADDR. VALID	THAZ	"	-	100	12	20	25	"	
CLK HIGH TO DATA VALID	THCHDX	VOUT = 1.5V	-	100	50	54	54	"	

* CASE TEMPERATURE

Table 6.4

4.4.5 MC68000L10 Summary

The DC, AC and FMAX data obtained on the MC68000L10 devices indicates that the devices performed extremely well across the Mil-temp range when compared to the vendors 8 MHZ 0-70°C specification. The functional failures on device #5 would not have been noted if the minimum FMAX specification was 3 MHZ. The functional problems noted with device #2 are attributed to the vendors process and can be detected with a 4.5 volt functional screen across temp. The graph shown in Figure 4.0 (ICC vs TEMP) clearly illustrates that the processing parameters of devices #2 and #5 are somewhat different from the remaining three devices. All five parts were hand-screened 8 MHZ devices for 0 to 70°C operations. It is quite obvious from the test data that the vendors process had improved significantly during the time between early 8 MHZ and these 10 MHZ device evaluations and consequently the most recent 8 MHZ should show a much improved performance.

4.5 MC68000L8 (Later Vintage) Device Testing

Based upon the data taken on the MC68000L10 devices, 5 pcs of the most recent vintage MC68000L8 were loaned by the vendor for evaluation.

4.5.1 Functional Testing

Functional testing of the most recent 8 MHZ devices indicates similar results as were obtained during 10 MHZ device testing. Shown in Table 7.0 - 7.2 is a summary of the functional test results. One device (#3) was non-functional at the -55°C test temperature. The failure mode centered on loss of address during process of RD/WRITE cycles and failure to process out of reset vector Ø (Power-on Reset) at low Vcc (4.5v). All devices were functional at +25°C. Devices #3 and #1 exhibited functional failures at the +110°C test temperature. Device #1 exhibited low Vcc/Low Freq (4.5 volts/2.0 MHZ) failures. These failures were not detected as the frequency increased (2.85 MHZ). Device #3 continued to exhibit low Vcc (4.5 volts) failures. The failure mode was similar to those noted at the -55°C test temperature.

4.5.2 D.C. Parametric Testing

All devices tested within the vendors 8 MHZ 0°-70°C specification. Shown in Table 7.3 are the D.C. test results obtained for all devices tested. Worst case supply current was measured to be 217.8 MA at Vcc = 5.5 volts @ -55°C TCASE. This translates into 1.2 watts maximum power dissipation.

4.5.3 FMAX Testing

Maximum frequency of operation for all devices tested was measured to be 7.1 MHZ (MAX). Based upon clock pulse width high calculations, the slowest device across the tested temperature was calculated to have an FMAX = 7.9 MHZ worst case.

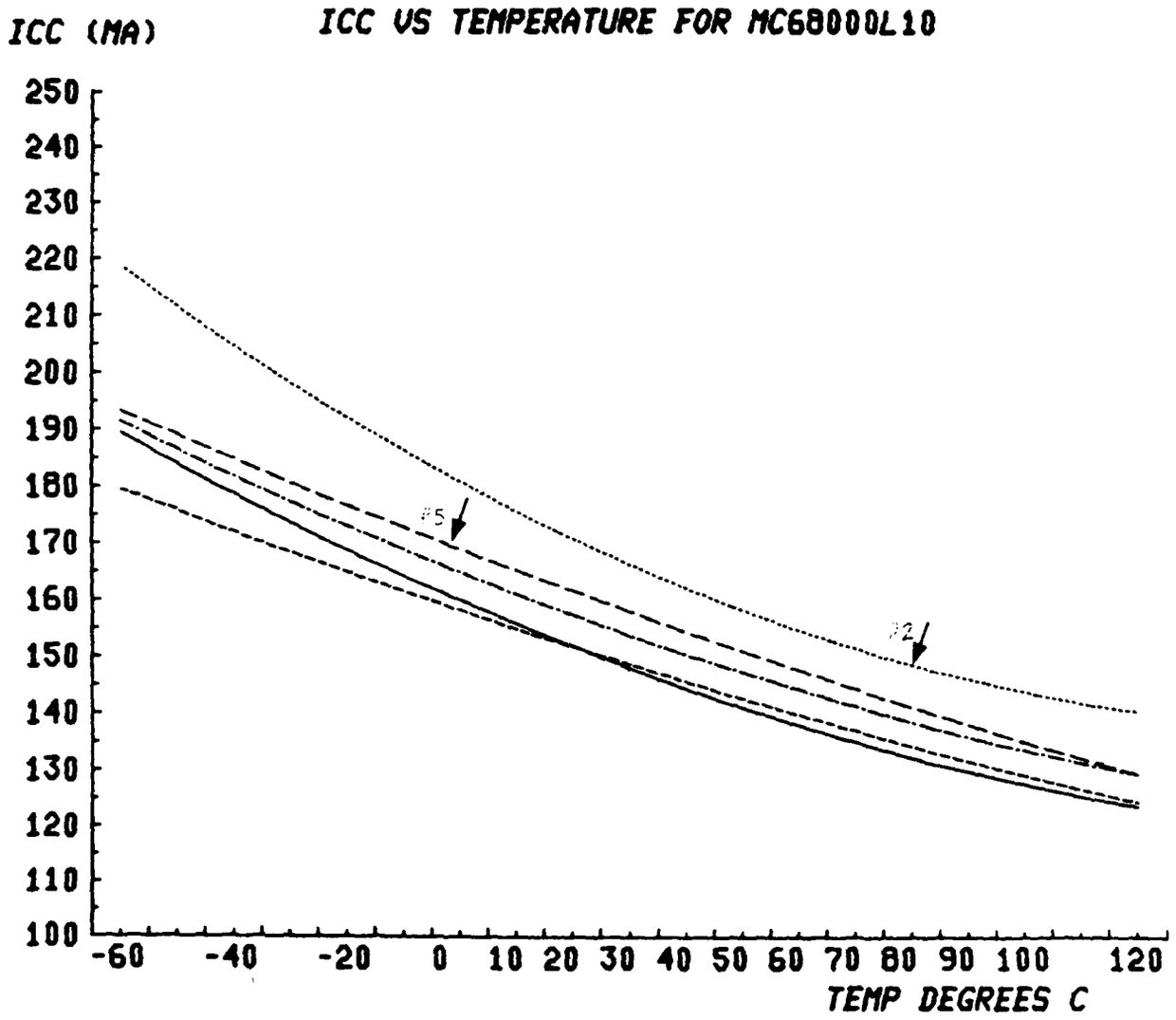

ICC (MA)
ICC VS TEMPERATURE FOR MC68000L10
250
240
230
220
210
200
190
180
170
160
150
140
130
120
110
100
#5
#2
-60
-40
-20
0
10
20
30
40
50
60
70
80
90
100
120
TEMP DEGREES C

Figure 4.0

REPORT TITLE INSTRUCTION DECODE FAILURE SUMMARY MC68000-LC1
(FAILURES BY DEVICE NUMBER)

	VCC	FREQ MHZ @ -55C 2.00	FREQ MHZ @ -55C 2.65	FREQ MHZ @ 25C 2.00	FREQ MHZ @ 25C 2.65	FREQ MHZ @ +125C 2.00	FREQ MHZ @ +125C 2.65	COMMENTS
EXG INSTR TEST	4.5	3	3					
	5.0	3	3					
	5.5	3	3					
CA INSTR TEST	4.5	3	3			3		
	5.0	3	3					
	5.5	3	3					
PEA INSTR TEST	4.5	3	3			3		
	5.0	3	3					
	5.5	3	3					
LINK UNLINK INSTR TEST	4.5	3	3			3		
	5.0	3	3					
	5.5	3	3					
MOVE INSTR TEST	4.5	3	3					
	5.0	3	3					
	5.5	3	3					
MOVEM INSTR TEST	4.5	3	3					
	5.0	3	3					
	5.5	3	3					
MOVEP INSTR TEST	4.5	3	3			3		
	5.0	3	3					
	5.5	3	3					
MOVEA INSTR TEST	4.5	3	3			3		
	5.0	3	3					
	5.5	3	3					

Table 7.0

Available Copy

MOVEQ INST. TEST	4.5	3	3			3	
	5.0	3	3				
	5.5	3	3				
ADD INST. TEST	4.5	3	3			3	
	5.0	3	3				
	5.5	3	3				
ADD, ADDQ INST. TEST	4.5	3	3			3	
	5.0	3	3				
	5.5	3	3				
MUL INST. TEST	4.5	3	3			3	
	5.0	3	3				
	5.5	3	3				
CMP INST. TEST	4.5	3	3			3	
	5.0	3	3				
	5.5	3	3				
CMP, CMPI, CMPM INST. TEST	4.5	3	3				
	5.0	3	3				
	5.5	3	3				
DIV, DIVS INST. TEST	4.5	3	3			13.5	3
	5.0	3	3				
	5.5	3	3				
EXT INST. TEST	4.5	3	3				
	5.0	3	3				
	5.5	3	3				
MOVE, MOVS INST. TEST	4.5	3	3			4.5	3
	5.0	3	3				
	5.5	3	3				

Table 7.1

[illegible], NEGX INST. TEST	4.5	3	3			3		
	5.0	3	3					
	5.5	3	3					
[illegible], SUBT, SUBQ, SUBX INST. TEST	4.5	3	3			3		
	5.0	3	3					
	5.5	3	3					
AS, TST INST. TEST	4.5	3	3			3		
	5.0	3	3					
	5.5	3	3					
AND, ANDI INST. TEST	4.5	3	3			3		
	5.0	3	3					
	5.5	3	3					
CR, ORI, EOR INST. TEST	4.5	3	3					
	5.0	3	3					
	5.5	3	3					
NOT, SHIFT, ROTATE INST. TEST	4.5	3	3			5	5	5 FAILS NOT DO FOFO - OFOF NEG BIT SET IN STATUS REG
	5.0	3	3			5	5	
	5.5	3	3			5	5	
BIT (TST, SET, CLR, CHG) INST. TEST	4.5	3	3			3		
	5.0	3	3					
	5.5	3	3					
ECD (ADD, SUB, NEG) INST. TEST	4.5	3	3			3		
	5.0	3	3					
	5.5	3	3					
BRANCH, JUMP, RETURN INST. TEST	4.5	3	3			3		
	5.0	3	3					
	5.5	3	3					
ADDA, SUBA, CMPA INST. TEST	4.5	3	3					
	5.0	3	3					
	5.5	3	3					
MOSP, MSR, MCCR INST. TEST	4.5	3	3					
	5.0	3	3					
	5.5	3	3					
TRAP, TRAPV INST. TEST	4.5	3	3			3		
	5.0	3	3					
	5.5	3	3					

Table 7.2

REPORT TITLE -- MC68000 DC PARAMETRIC TEST CCI MASK SET PARTS DEVICE : # 1-5
DEVICE TYPE: CP DATE CODE : 81.4

TEST	CONDITIONS	SPEC. MIN	SPEC. MAX	IBM TEST DATA * -55	+25	+115	UNITS	COMMENTS
ICC TEST	FREQ=6MHZ VCC=5.5V		2[illegible]	17.8	171.9	139.[illegible]	MA	VCC = 5.5VOLTS
VOL A23-1,FC0-2,BG,E	IOL = 3.2MA		0.5	0.20	0.25	0.29	VOLTS	VCC = 4.5VOLT
VOL HALT	IOL = 1.6MA		0.5	0.15	0.21	0.[illegible]	"	"
VOL A5,R/W,D15-0 D0,S,LDS,VMA	IOL = 5.3MA		0.5	0.25	0.21	0.28	"	"
VOL RESET	IOL = 5.0MA		0.5	0.15	0.21	0.29	"	"
VOH (ALL OUTPUTS)	IOH = 400UA	2.4		3.16	3.[illegible]	3.[illegible]	"	
IIH (ALL INPUTS)	VIH = 2.4 VOLTS		1.0	.004	.004	.033	UA	
IIL (ALL INPUTS)	VIL = 0.4 VOLTS		1.0	.004	.004	.0[illegible]	"	
IOHZ (ALL OUTPUTS)	VOH = 2.4 VOLTS		2.0	.001	.001	.001	"	
IOLZ (ALL OUTPUTS)	VOL = 0.4 VOLTS		2.0	.001	.001	.001	"	
VIH (ALL INPUTS)	VGS TEST			1.70	1.55	1.55	VOLTS	VCC = 4.5 V
VIL (ALL INPUTS)				1.05	1.05	1.10	"	VCC = 4.5 V

* CASE TEMPERATURE

NOTE: [illegible]
TEST MODE CONFIGURATION

Table 7.3

REPORT TITLE - - MOTOROLA MC68000 AC PERFORMANCE TESTS - CCI MASK SET PARTS DEVICE : # 1 [illegible]
DEVICE TYPE : [illegible] DATE CODE : [illegible]

TEST	SYMBOL	CONDITIONS	SPEC. MIN	SPEC. MAX	SUM TEST DATA * -55	+25	+110	UNIT	COMMENTS
DIN TO CLK LOW (TSET)	TDICL		25	-	3	3	2	NS	TEMP : [illegible] VCC [illegible] VOLTS
DIN TO CLK LOW (THOLD)	THDICL		-	-	4	4	1	"	FREQ : [illegible] MHZ
DTACK TO CLK LOW(TSET)	TSDTCL		25	-	0	0	0	"	
BR TO CLK LOW (TSET)	TSBRCL		25	-	2	2	2	"	
BR TO CLK LOW (THOLD)	THBRCL		-	-	3	2	2	"	
BGACK TO CLK LOW(TSET)	TSBGCL		25	-	-1	-1	-1	"	
BGACK TO CLK LOW(THOLD)	THBGCL		-	-	0	0	0	"	
VPA TO CLK LOW (TSET)	TSVPACL		25	-	-4	[illegible]	[illegible]	"	REQUIRES SPECIAL TEST MODE
VPA TO CLK LOW (THOLD)	THVPACL		-	-	-1	-2	-4	"	
BERR TO CLK LOW (TSET)	TSBERCL		25	-	3	3	4	"	
BERR TO CLK LOW(THOLD)	THBERCL		-	-	4	4	4	"	
CLK WIDTH LOW	TCL		75	250	22	23	32	"	
CLK WIDTH HIGH	TCH		75	250	39	48	59	"	
CLK HIGH TO FC VALID	TCLAV		-	80	35	45	65	"	
CLK HIGH TO AS LOW	TCHSLX		0	-	28	39	49	"	(MIN)
CLK HIGH TO AS LOW	TCHSLN		-	70	37	47	59	"	(MAX)
CLK HIGH TO DS LOW	TCHSLX		0	-	23	36	46	"	(MIN)
CLK HIGH TO DS LOW	TCHSLN		-	70	33	42	56	"	(MAX)
CLK LOW TO AS HIGH	TCLSH		-	80	37	46	63	"	
CLK LOW TO DS HIGH	TCLSH		-	80	34	53	72	"	
CLK H TO R-W H	TCHRHX		0	-	23	29	34	"	(MIN)
CLK H TO R-W H	TCHRHX		-	80	14	18	22	"	(MAX)
CLK HIGH TO R-W LOW	TCHRL		-	80	13	25	28	"	
CLK L TO DOUT VALID	TCLDO		-	80	33	45	57	"	
CLK L TO ADDR. VALID	TCLAV		-	80	48	58	73	"	
CLK HIGH TO BG LOW	TCHGL		-	80	14	26	30	"	
CLK HIGH TO BG HIGH	TCHGH		-	80	18	23	31	"	
CLK LOW TO VMA LOW	TCLVML		-	80	24	33	42	"	REQUIRES SPECIAL TEST MODE
CLK HIGH TO VMA HIGH	TCHVMH		-	-	15	27	32	"	
CLK LOW TO E LOW	TCLEL		-	-	16	29	39	"	REQUIRES SPECIAL TEST MODE
CLK LOW TO E HIGH	TCLEH		-	-	18	24	34	"	
CLK H TO ADDR.-FC T.S.	TCHAZX	VOUT +-0.5V	-	100	68	69	79	"	
CLK H TO ADDR. INVALID	TSHAZ	"	0	-	65	66	77	"	
CLK HIGH TO AS,DS T.S.	TCHSZ	VOUT +-0.5V	-	100	48	51	56	"	
CLK HIGH TO R-W T.S.	TCHRZ	"	-	100	31	25	-	"	
CLK HIGH TO DATA T.S.	TCHAZX	VOUT +-0.5V	-	100	57	71	101	"	

* CASE TEMPERATURE

Table 7.4

4.5.4 AC Performance

All devices tested within the vendors 0°-70°C 6 MHZ specification. Shown in Table 7.4 are the summarized results of the data obtained during device testing.

4.5.5 MC68000L8 (Latest Vintage) Summary

It is obvious that the performance of this set of 8 MHZ devices has improved significantly from the performance of the earlier 8 MHZ devices. Shown graphically in Figures 5.0-5.1 are two trends that illustrate the performance of the later vintage 8 MHZ devices. It is obvious that at the time of manufacture the vendor was making process changes to optimize yield and performance. This resulted in somewhat different NMOS trends in the earlier devices (L8). The later vintage (L8X) device trends are nearly those of the L10 devices as evidenced by the graphs of Figures 5.0-5.1. The later vintage MC68000L8 improved functionality and performance as a direct result of the vendors matured and stabilized process.

4.6 HD68000 DEVICE TESTING

Device Testing was performed on 6 pcs of Hitachi's HD68000. Hitachi is manufacturing the device under a Mask Exchange Agreement with Motorola and are manufacturing the device using the T6E mask set. Devices were marked as HD68000 with a 1D3 lot code identifier.

4.6.1 Functional Testing

Shown in Table 8.0 - 8.2 is the functional test summary for the HD68000 devices. Device testing at -55°C (TCASE) indicated functional failures on 3 devices (#2, #5, #6). These failures were very similar to the failures noted on late T6E/early CC1 Mask Set device MC68000's with the faster devices exhibiting high Vcc (5.5 volt) fails at the -55°C test temp. The failure mechanism was the loss of address and improper conditions on AS, DS during processor RD/WRITE operations. Device #2 exhibited gross functional failures at the $+25^{o}$C test temperature. The failure mechanism was the loss of address during processor RD/WRITE operations. All devices were functional at the $+110^{o}$C (TCASE) test temperature.

4.6.2 D.C. Parametric Testing

All device parameters were within the vendors 0°-70°C specification with the exception of supply current (Icc). Shown in Table 8.3 is the data summary obtained during device testing. Icc was measured to be 209 MA typically ($+25^{o}$C). This was approximately 25% higher than typical Icc measured on the MC68000 devices. This resulted in a 1.7 watt part worst case (Vcc = 5.5 Volts, @ -55°C) and exceeded the vendors original specification of 1.2 watts maximum.

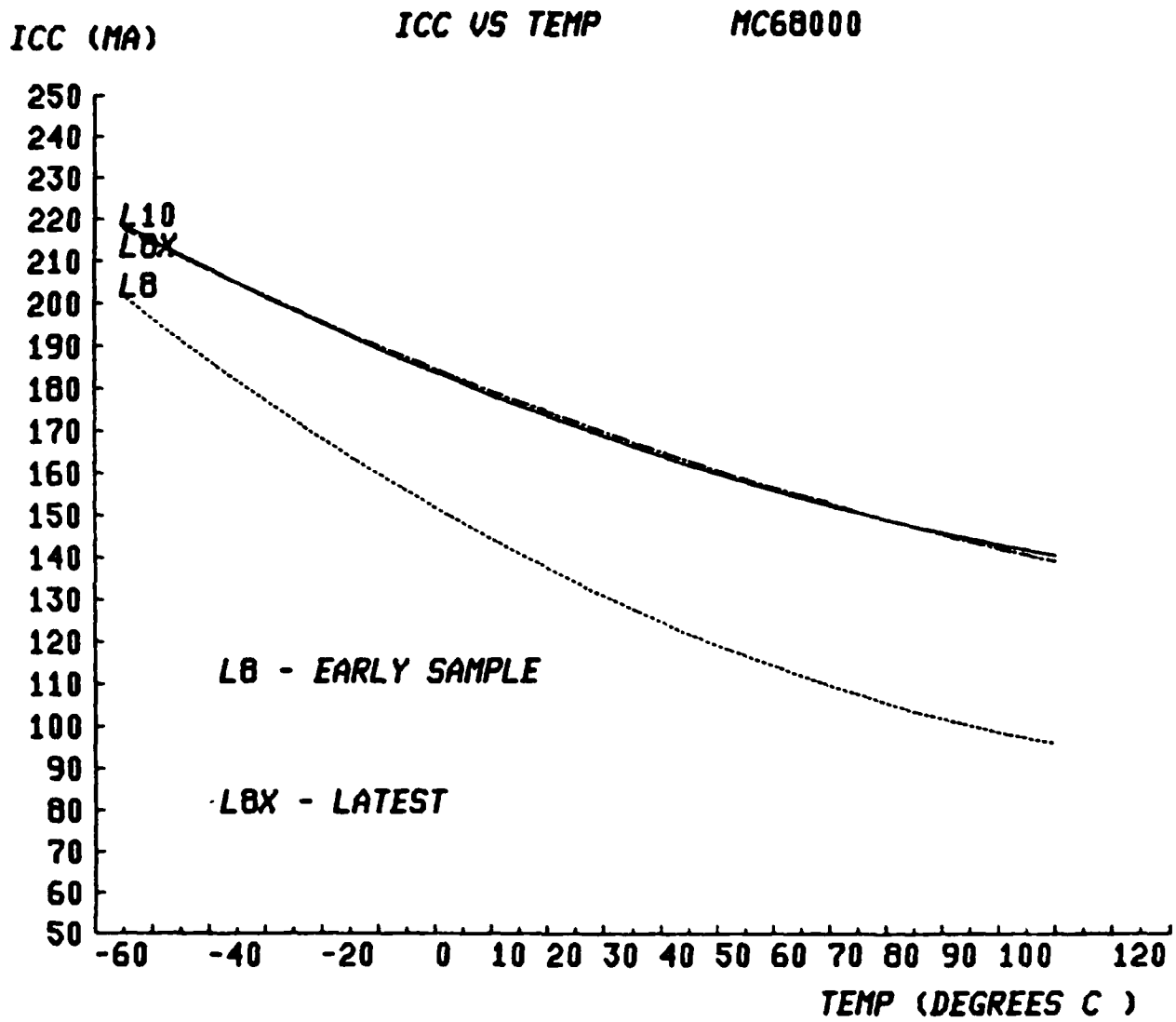

ICC (MA)
ICC VS TEMP
MC68000
250
240
230
220
210
200
190
180
170
160
150
140
130
120
110
100
90
80
70
60
50
L10
L8X
L8
L8 - EARLY SAMPLE
L8X - LATEST
-60
-40
-20
0
10
20
30
40
50
60
70
80
90
100
120
TEMP (DEGREES C)

Figure 5.0

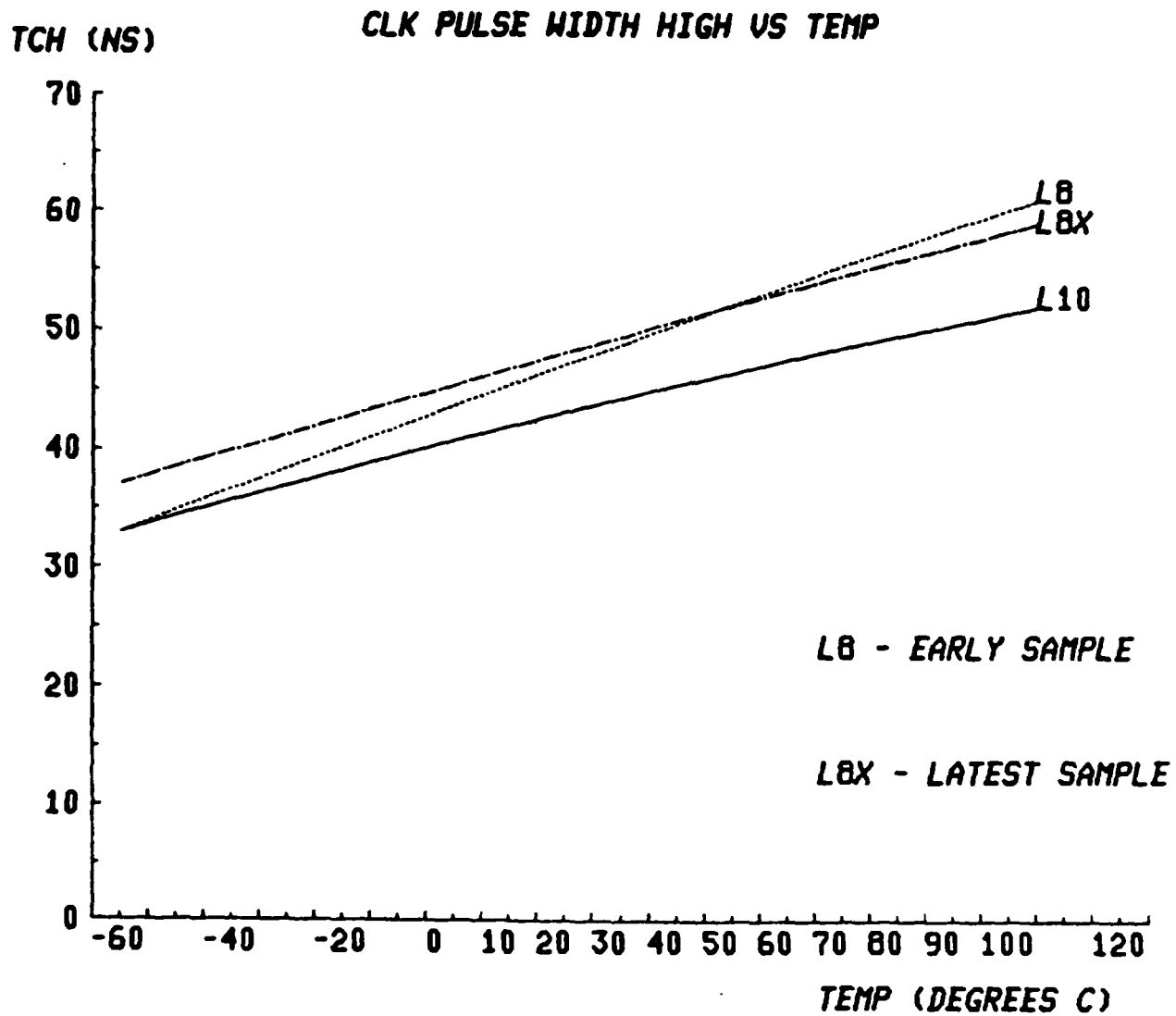

CLK PULSE WIDTH HIGH VS TEMP
TCH (NS)
70
60
50
40
30
20
10
0
-60
-40
-20
0
10
20
30
40
50
60
70
80
90
100
120
TEMP (DEGREES C)
L8
L8X
L10
L8 - EARLY SAMPLE
L8X - LATEST SAMPLE

Figure 5.1

REPORT TITLE INSTRUCTION DECODE FAILURE SUMMARY M68000 - T6

	VCC	FREQ MHZ @ -55C 2.00	FREQ MHZ @ -55C 2.85	FREQ MHZ @ 25C 2.00	FREQ MHZ @ 25C 2.85	FREQ MHZ @ +110C 2.00	FREQ MHZ @ +110C 2.85	COMMENTS
EXG INST. TEST	4.5			2	2			NO FUNCTIONAL FAILURES NOTED AT +110C
	5.0			2	2			
	5.5		5	2	2			
LEA INST. TEST	4.5			2	2			
	5.0			2	2			
	5.5		5.6	2	2			
PEA INST. TEST	4.5			2	2			
	5.0				2			
	5.5		2	2				
LINK, UNLINK INST. TEST	4.5			2	2			
	5.0			2	2			
	5.5			2	2			
MOVE INST. TEST	4.5							
	5.0			2	2			
	5.5	2		2	2			
MOVEM INST. TEST	4.5			2	2			
	5.0			2	2			
	5.5		5.6	2	2			
MOVEP INST. TEST	4.5			2	2			
	5.0			2	2			
	5.5		5.6	2	2			
MOVEA INST. TEST	4.5			2	2			
	5.0			2	2			
	5.5		2	2	2			

Table 6.0

MOVEQ INST. TEST	4.5				2		2		
	5.0				2		2		
	5.5	2			2		2		
[illegible] INST. TEST	4.5				2		2		
	5.0				2		2		
	5.5				2		2		
ADD, ADDQ INST. TEST	4.5				2		2		
	5.0				2		2		
	5.5				2		2		
ADDX INST. TEST	4.5				2		2		
	5.0				2		2		
	5.5			5.6	2		2		
CLR INST. TEST	4.5				2		2		
	5.0				2		2		
	5.5				2		2		
CMP, CMPI, CMPM INST. TEST	4.5				2		2		
	5.0				2		2		
	5.5			5.6	2		2		
DIV, DIVS INST. TEST	4.5				2		2		
	5.0				2		2		
	5.5			5	2		2		
EXT INST. TEST	4.5								
	5.0				2		2		
	5.5			2.5	2		2		
MULU, MULS INST. TEST	4.5				2		2		
	5.0				2		2		
	5.5				2		2		

Table 8.1 Fail Test Summary (Con't)

[illegible] INST. TEST	4.5			2	2		
	5.0			2	2		
	5.5	2		2	2		
SUB, SUBI, SUBQ, SUBX INST. TEST	4.5			2	2		
	5.0			2	2		
	5.5			2	2		
TAS, TST INST. TEST	4.5						
	5.0						
	5.5						
AND, ANDI INST. TEST	4.5			2	2		
	5.0			2	2		
	5.5			2	2		
OR, ORI, EOR INST. TEST	4.5			2	2		
	5.0			2	2		
	5.5	2	6	2	2		
NOT, SHIFT, ROTATE INST. TEST	4.5			2	2		
	5.0			2	2		
	5.5			2	2		
BIT (TST, SET, CLR, CHG) INST. TEST	4.5			2	2		
	5.0			2	2		
	5.5			2	2		
BCD (ABCD, SBCD, NEG) INST. TEST	4.5			2	2		
	5.0			2	2		
	5.5			2	2		
BRANCH, JUMP, RETURN INST. TEST	4.5			2	2		
	5.0	2	2	2	2		
	5.5	2	2	2	2		
[illegible] ADDA, SUBA, CMPA INST. TEST	4.5			2	2		
	5.0			2	2		
	5.5			2	2		
[illegible] INST. TEST	4.5			2	2		
	5.0				2		
	5.5						
EXAM, EXAMV INST. TEST	4.5			2	2		
	5.0			2	2		
	5.5			2	2		

Table 8.2

[illegible] HD68000 DC PARAMETRIC TEST [illegible] MASK SET PARTS DEVICE : # [illegible]
DEVICE TYPE: [illegible] DATE CODE/ID : [illegible]

TEST	CONDITIONS	SPEC. MIN	SPEC. MAX	IBM TEST DATA * [illegible]	[illegible]	[illegible]	UNITS	COMMENT
[illegible]	[illegible] VCC=5.5V		[illegible]	[illegible]	[illegible]	[illegible]	MA	VCC [illegible]
[illegible]	[illegible] = 3.2MA		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	VCC [illegible]
[illegible]	[illegible] = [illegible]MA		0.5	0.17	[illegible]	[illegible]	"	"
[illegible]	[illegible] = 5.3MA		[illegible]	0.47	[illegible]	[illegible]	"	"
[illegible]	[illegible] 5.[illegible]MA		[illegible]	0.17	[illegible]	[illegible]	"	"
[illegible]	[illegible]	[illegible]		[illegible]	[illegible]	[illegible]	"	
[illegible]	[illegible]		1.0	[illegible]	[illegible]	[illegible]	[illegible]	
[illegible]	[illegible]		[illegible]	[illegible]	[illegible]	[illegible]	"	
[illegible]	[illegible]		[illegible]	[illegible]	[illegible]	[illegible]	"	
[illegible]	[illegible]		[illegible]	[illegible]	[illegible]	[illegible]	"	
[illegible]	[illegible]			[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]				[illegible]	[illegible]	[illegible]	"	[illegible]

* [illegible]

NOTE: [illegible]

Table 8.3

[illegible]

TEST	SYMBOL	CONDITIONS	SPECS MIN	SPECS MAX	DIM TEST DATA * 50	125	210	N/A	COMMENTS
DS [illegible] CLK [illegible] (ENABLED)	TDSTCL		25	-	8	10	12	"	TEMP : [illegible] DEGREES CASE
HIN [illegible] CLK LOW (ENABLED)	TDHTCL		-	-	9	11	13	"	VCC : 5.0 VOLTS FREQ : 2.0 MHZ
CLACK TO CLK [illegible] (ENABLED)	TDSTCL		25	-	N/A	N/A	N/A	"	
DS TO CLK LOW (DISABLED)	TDSNCL		25	-	7	9	11	"	
DS TO CLK LOW (ENABLED)	TDHNCL		-	-	8	10	12	"	
DSACK TO CLK LOW (ENABLED)	TDSACL		25	-	3	5	7	"	
DSACK TO CLK LOW (DISABLED)	TDHACL		-	-	5	7	10	"	
VPA TO CLK [illegible] (ENABLED)	TDVPACL		25	-	3	1	2	"	
VPA TO CLK [illegible] (DISABLED)	TDHVPACL		-	-	4	5	5	"	REQUIRES SPECIAL TEST MODE
BERR TO CLK LOW (ENABLED)	TDSBRCL		25	-	8	10	12	"	
BERR TO CLK LOW (DISABLED)	TDHBRCL		-	-	10	12	14	"	
CLK WIDTH LOW	TCL		75	250	43	37	36	"	
CLK WIDTH HIGH	TCH		75	250	17	24	33	"	
CLK HIGH TO FC VALID	TCLAV		-	80	N/A	N/A	N/A	"	
CLK HIGH TO AS LOW	TCHSLX		0	-	30	43	55	"	(MIN)
CLK HIGH TO AS LOW	TCHSLN		-	70	39	49	64	"	(MAX)
CLK HIGH TO DS LOW	TCHSLX		0	-	26	40	52	"	(MIN)
CLK HIGH TO DS LOW	TCHSLN		-	70	36	46	64	"	(MAX)
CLK LOW TO AS HIGH	TCLSH		-	80	40	49	56	"	
CLK LOW TO DS HIGH	TCLSH		-	80	36	42	52	"	
CLK H TO R-W H	TCHRHX		0	-	28	36	45	"	(MIN)
CLK H TO R-W H	TCHRHX		-	80	18	24	31	"	(MAX)
CLK HIGH TO R-W LOW	TCHRL		-	80	25	31	39	"	
CLK L TO DOUT VALID	TCLDO		-	60	37	50	64	"	
CLK L TO ADDR. VALID	TCLAV		-	80	0	66	81	"	
CLK HIGH TO BG LOW	TCHGL		-	80	23	32	40	"	
CLK HIGH TO BG HIGH	TCHGH		-	80	22	31	41	"	
CLK LOW TO VMA LOW	TCLVML		-	80	22	37	46	"	
CLK HIGH TO VMA HIGH	TCHVMH		-	-	21	32	40	"	REQUIRES SPECIAL TEST MODE
CLK LOW TO E LOW	TCLEL		-	-	30	45	59	"	
CLK LOW TO E HIGH	TCLEH		-	-	29	32	46	"	REQUIRES SPECIAL TEST MODE
CLK H TO ADDR.+FC T.S.	TCHAZX	VOUT +-0.5V	-	100	-	93	106	"	
CLK H T ADDR. INVALID	TCHAZ	"	0	-	-	93	110	"	
CLK HIGH TO AS.DS T.S.	TCHSZ	VOUT +-0.5V	-	100	47	53	61	"	
CLK HIGH TO R-W T.S.	TCHRZ	"	-	100	37	41	37	"	
CLK HIGH TO DATA T.S.	TCHAZX	VOUT +-0.5V	-	100	56	68	74	"	

* CASE TEMPERATURE

Table 8.4

4.6.3 Maximum Frequency of Operation (FMAX) testing

All devices passed the maximum tested FMAX of 8.33 MHZ at the temperature range of -55°C to +110°C (TCASE). Calculated using pulse width high, the FMAX was found to be approximately 13.8 MHZ worst case (+110°C), however more samples need to be tested to guarantee this method of calculation holds true with the second vendor's process.

4.6.4 AC Testing

All device tested to within the vendors specification for a 6 MHz device shown in Table 8.4 are the AC performance results obtained during testing.

4.6.5 HD68000 Test Summary

The HD68000 device exhibited an unusually high FMAX (13.8 MHZ worst case). This is directly related to the vendors process. This is further illustrated by the supply current (Icc) data which resulted in an unusually high power dissipation. Having noted these two process parameters the functional performance was as expected. The fastest parts exhibiting the low temp (-55°C), High Vcc (5.5 volt) failures. However, it should be noted that not all the devices exhibited failures at the low temperature and that in general the devices have a higher than anticipated maximum frequency of operation. It can be expected as the vendor homes in on the corners of his process that the device failures noted during functional testing will go away resulting in a much improved MIL-temp device. In addition, the second source vendor's will be receiving next generation masks (vintage CC1) for processing. This mask set allows more margining due to critical path enchancements.

5.0 CONCLUSION

The evaluation of the MC68000 microprocessor was a complex and time consuming task. It involved the evaluation of many different mask set devices and devices with varying performance characteristics. However, the data presented within this report clearly shows that the device from its infant stage of development (R9M MASK SET) to the present day device has matured into one of the most technologically advanced 16-bit microprocessors available. Its performance across the MIL-temp range clearly indicates its applicability to a military environment. The vendors commitment to develop and provide this device for use within a Hi-Rel market combined with the general acceptance of the device by the design community should serve to provide a valuable tool to the electronic industry.

The existance of 5 potential sources through mask exchange with Motorola will provide a highly competitive and reliable part to military users. Of the five vendors, Motorola, Hitachi, Mostek and Rockwell have samples, while Signetics plans availability in 1982.

Motorola also plans enhancements to the performance of the MC68000 up to 16 MHZ in 1982. By 1Q82, a 12 MHZ device should be available, which by past experience should yield a 10 MHZ mil-temp device.

The performance growth and large compendium of peripheral circuits planned make this processor not only an excellent present design choice, but one that will offer future growth in all military applications.

APPENDIX A

```
NOP
MOVE        AAAA, D1
MOVE        5555, D7
MOVE        FF00, A1
MOVE        00FF, A6
MOVE        D1, (A7)
MOVE        D7, (A7)
MOVE        A1, (A7)
MOVE        A6, (A7)
EXG         D1, D7
MOVE        D1, (A7)
MOVE        D7, (A7)
EXG         A1, A6
MOVE    A1, (A7)
MOVE    A6, (A7)
EXG     D7, A1
MOVE    D7, (A7)
MOVE    A1, (A7)
EXG     A6, D1
MOVE    D1, (A7)
MOVE    A6, (A7)
NOP
STOP
```

```
NOP
MOVE        0000, A0
MOVE        0000, A1
MOVE        0000, A2
MOVE        0000, A3
MOVE        0000, A4
MOVE        0000, A5
MOVE        0000, A6
MOVE        A0, (A7)
MOVE        A1, (A7)
MOVE        A2, (A7)
MOVE        A3, (A7)
MOVE        A4, (A7)
MOVE        A5, (A7)
MOVE        A6, (A7)
LEA       xxx.W, A0
LEA       xxx.W, A1
LEA       xxx.W, A2
LEA       xxx.W, A3
LEA       xxx.W, A4
LEA       xxx.W, A5
LEA       xxx.W, A6
MOVE        A0, (A7)
MOVE        A1, (A7)
MOVE        A2, (A7)
MOVE        A3, (A7)
MOVE        A4, (A7)
MOVE        A5, (A7)
MOVE        A6, (A7)
NOP
STOP
```

LINK

```
NOP
MOVE        1000, A1
NOP
LINK        A1, 0100
NOP
NOP
UNLINK      A1
NOP
STOP
```

PEA

```
NOP
MOVE        00001200, A4
PEA         A4
NOP
STOP
```

```
NOP
MOVE        5555, D0
            AAAA, D7
            D0, (A7)
            D7, (A7)
            AAAA, D2
            5555, D6
            FOFO, A1
            OFOF, A6
            D2, (A7)
            D6, (A7)
            A1, (A7)
            A6, (A7)
            AAAAAAAA, D3
            55555555, D5
            FOFOFOFO, A2
            OFOFOFOF, A5
            D3, (A7)
            D5, (A7)
            A2, (A7)
            A5, (A7)
            A5, A2
            D5, D3
            A2, (A7)
            D3, (A7)
            0000 OFOF, D0
            0050, D1
             D0, (A7) L. WORD
             D0, (A7) + D L. WORD
             D0, (A7) + INDX + D L. WORD
             D0, (A7) - L. WORD
MOVE         D0, (A7) + L. WORD
            (PC+DISP), D1
            (PC+DISP+INDX), D1
NOP
STOP
```

```
NOP
MOVE        1200, A6
            D0, (A7)
            D1, (A7)
            D2, (A7)
            D3, (A7)
            D4, (A7)
            D5, (A7)
            D6, (A7)
            D7, (A7)
            A0, (A7)
            A1, (A7)
            A2, (A7)
            A3, (A7)
            A4, (A7)
            A5, (A7)
            1250, A6
MOVEM       (A6), REG LIST
MOVE        D0, (A7)
            D1, (A7)
            D2, (A7)
            D3, (A7)
            D4, (A7)
            D5, (A7)
            D6, (A7)
            D7, (A7)
            A0, (A7)
            A1, (A7)
            A2, (A7)
            A3, (A7)
            A4, (A7)
MOVE        A5, (A7)
            1300, A6
MOVEM       REG LIST, (A6)
MOVE        1300, A6
MOVEM       REG LIST (A6)
NOP
STOP
```

```
NOP
MOVE        A000, A0
MOVEP       55FFAAFF, D0
MOVE        D0, (A7)
MOVEP       D1
MOVE        D1, (A7)
MOVE        A001, A0
MOVEP       FF55FFAA, D2
MOVE        D2, (A7)
MOVEP       D3
MOVE        D3, (A7)
MOVEP       D3, (A0)
MOVEP       D2, (A0)
MOVE        A000, A0
MOVEP       D1, (A0)
MOVEP       D0, (A0)
NOP
STOP
```

MOVEQ

```
NOP
MOVE        0000, D1
MOVE        0000, D3
MOVE        0000, D6
MOVE        D1, (A7)
MOVE        D3, (A7)
MOVE        D6, (A7)
MOVEQ        55, D1
MOVEQ       0A, D3
MOVEQ       0F, D6
MOVE        D1, (A7)
MOVE        D3, (A7)
MOVE        D6, (A7)
NOP
STOP
```

MOVE A

```
NOP
MOVE        0000, A0
MOVE        0000, A3
MOVE        0000, A6
MOVE        A0, (A7)
MOVE        A3, (A7)
MOVE        A6, (A7)
MOVEA       5555AAAA, A0
MOVE        A0, (A7)
MOVEA       A0, A3
MOVE        A3, (A7)
MOVEA       A0, A6
MOVE        A6, (A7)
NOP
STOP
```

```
NOP
MOVEQ     00, D0
          00, D1
          00, D2
          00, D3
          00, D4
          00, D5
          00, D6
          00, D7
MOVE      D0, (A7)
          D1, (A7)
          D2, (A7)
          D3, (A7)
          D4, (A7)
          D5, (A7)
          D6, (A7)
          D7, (A7)
MOVEQ     0A, D0
          55, D1
          0A, D2
          55, D3
          0A, D4
          55, D5
          0A, D6
          55, D7
SWAP      D0
          D1
          D2
          D3
          D4
          D5
SWAP      D6
          D7
MOVE      D0, (A7)
          D1, (A7)
          D2, (A7)
          D3, (A7)
          D4, (A7)
          D5, (A7)
          D6, (A7)
          D7, (A7)
NOP
STOP
```

```
NOP
MOVE    5555, D1
MOVE    AAAA, D3
MOVE    0F0F, A1
MOVE    F0F0, A3
MOVE    D1, (A7)
MOVE    D3, (A7)
MOVE    A1, (A7)
MOVE    A3, (A7)
ADD     AAAA, D1
MOVE    SR, (A7)
MOVE    D1, (A7)
ADD     5555, D3
MOVE    SR, (A7)
MOVE    D3, (A7)
MOVE    F0F0, D1
ADD     D1, D0
MOVE    SR, (A7)
MOVE    D1, (A7)
MOVE    00F0, D3
MOVE    0050, D1
ADD     D3, D1
MOVE    SR, (A7)
MOVE    D1, (A7)
MOVE    0000, D0
MOVE    5555, A0
MOVE    1300, A6
MOVE    AAAA, (A6)
ADDQ    5, D0
MOVE    SR, (A7)
MOVE    D0, (A7)
ADDQ    5, A0
MOVE    SR, (A7)
MOVE    A0, (A7)
ADDQ    5, (A6)
MOVE    SR, (A7)
MOVE    (A6), (A7)
NOP
STOP
```

```
NOP
MOVE        0000, D2
MOVE        5555, D4
MOVE        12FE, A2
MOVE        1300, A6
MOVE        0505, A5
MOVE        D2, (A7)
MOVE        D4, (A7)
MOVE        A2, (A7)
MOVE        A4, (A7)
MOVE        2700, SR
ADDX        D2, D4
MOVE        SR, (A7)
MOVE        D4, (A2)
MOVE        5555, D2
MOVE        0000, D4
MOVE        2710, SR
ADDX        D4, D2
MOVE        SR, (A7)
MOVE        D2, (A7)
NOP
STOP
```

```
NOP
MOVE        FFFF, D0
MOVE        FFFF, D1
MOVE        FFFF, D2
MOVE        FFFF, D3
MOVE        D0, (A7)
MOVE        D1, (A7)
MOVE        D2, (A7)
MOVE        D3, (A7)
CLR         D0
MOVE        SR, (A7)
CLR         D1
MOVE        SR, (A7)
CLR         D2
MOVE        SR, (A7)
CLR         D3
MOVE        SR, (A7)
MOVE        D0, (A7)
MOVE        D1, (A7)
MOVE        D2, (A7)
MOVE        D3, (A7)
MOVE        1374, A6
MOVE        1350, A5
MOVE        1324, A4
CLR         (A6)
CLR         (A5)
CLR         (A4)
NOP
STOP
```

```
NOP
MOVE    00AA, D3
MOVE    0055, D5
MOVE    1350, A6
MOVE    D3, (A7)
MOVE    D5, (55)
CMP     D5, D3
MOVE    SR, (A7)
MOVE    D3, (A7)
MOVE    00AA, D3
MOVE    0055, D5
CMP     D3, D5
MOVE    SR, (A7)
MOVE    D5, (A7)
MOVE    0055, D3
MOVE    0055, D5
CMP     D5, D3
MOVE    SR, (A7)
MOVE    D3, (A7)
MOVE    00AA, (A6)
MOVE    00AA, D5
CMP     (A6), D5
MOVE    SR, (A7)
MOVE    D5, (A7)
MOVE    AAAA, D0
MOVE    1300, A6
MOVE    AAAA, (A6)
MOVE    2700, SR
CMPI    AAAA, D0
MOVE    SR, (A7)
MOVE    D0, (A7)
CMPI    5555, (A6)
MOVE    SR, (A7)
MOVE    (A6), (A7)
MOVE    1300, A6
MOVE    1376, A4
MOVE    00AA, (A6)
MOVE    AAAA, (A4)
MOVE    2700, SR
CMPM    (A6), (A4)
MOVE    SR, (A7)
NOP
STOP
```

```
MOVE        0004, D0
MOVE        0084, D3
MOVE        D0, (A7)
MOVE        D3, (A7)
EXT         D0
MOVE        SR, (A7)
MOVE        D0, (A7)
EXT         D3
MOVE        SR, (A7)
MOVE        D0, (A7)
MOVE        7FFF, D0
MOVE        800F, D3
MOVE        D0, (A7)
MOVE        D3, (A7)
EXT         D0
MOVE        SR, (A7)
MOVE        D0, (A7)
EXT         D3
MOVE        SR, (A2)
MOVE        D3, (A2)
NOP
STOP
```

```
NOP
MOVE        5555, D0
MOVE        0002, D1
MOVE        2700, SR
MOVE        D0, (A7)
MOVE        D1, (A7)
MULS        D1, D0
MOVE        SR, (A7)
MOVE        D0, (A7)
MOVE        00FF, D0
MOVE        0000, D1
MOVE        2700, SR
MULS        D1, D0
MOVE        SR, (A2)
MOVE        D0, (A7)
MOVE        5555, D0
MOVE        FFFC, D1
MULS        D1, D2
MOVE        SR, (A7)
MOVE        D0, (A7)
NOP
STOP
```

```
NOP
MOVE    0000, D0
MOVE    0000, D3
MOVE    0000, D5
MOVE    D0, (A7)
MOVE    D3, (A7)
MOVE    D5, (A7)
MOVE    5555, D3
MOVE    AAAA, D5
NEG     D0
MOVE    SR, (A7)
MOVE    D0, (A7)
NEG     D3
MOVE    SR, (A7)
MOVE    D3, (A7)
NEG     D5
MOVE    SR, (A7)
MOVE    D5, (A7)
NOP
MOVE    1300, A6
MOVE    5555, (A6)
MOVE    0001, D0
MOVE    00AA, D3
MOVE    55555555, D5
MOVE    2700, SR
NEGX    D0
MOVE    SR, (A7)
MOVE    D3, (A7)
MOVE    2700, SR
NEGX    D5
MOVE    SR, (A7)
MOVE    D5, (A7)
MOVE    00FF, D0
MOVE    00AA, D3
MOVE    00000055, D5
MOVE    2710, SR
NEG     D0
MOVE    SR, (A7)
MOVE    D0, (A7)
MOVE    2710, SR
NEGX    D5
MOVE    SR, (A7)
MOVE    D5, (A7)
MOVE    2710, SR
NEGX    (A6)
MOVE    SR, (A7)
MOVE    (A6), (A7)
MOVE    2700, SR
NEGX    (A6)
MOVE    SR, (A7)
MOVE    (A6), (A7)
NOP
STOP
```

```
NOP
MOVE    AAAA, D0
MOVE    5555, D2
MOVE    FFFF, D4
MOVE    D0, (A7)
MOVE    D2, (A7)
MOVE    D4, (A7)
SUBI    5555, D0
MOVE    SR, (A7)
MOVE    D0, (A7)
SUBI    AAAA, D2
MOVE    SR, (A7)
MOVE    D0, (A7)
SUBI    0FFF, D4
MOVE    SR, (A7)
MOVE    D4, (A7)
MOVE    AAAAAAAA, D0
MOVE    55555555, D2
SUBI    55555555, D0
MOVE    SR, (A7)
MOVE    D0, (A7)
SUBI    AAAAAAAA, D2
MOVE    SR, (A7)
MOVE    D2, (A7)
MOVE    AAAA, D0
MOVE    5555, A0
MOVE    0000, D2
SUBQ    5, D0
MOVE    SR, (A7)
MOVE    D0, (A7)
SUBQ    5, A0
MOVE    SR, (A7)
MOVE    A0, (A7)
SUBQ    7, D2
MOVE    SR, (A7)
MOVE    D2, (A7)
MOVE    5555, D1
MOVE    AAAA, D0
MOVE    2700, SR
SUBX    D1, D0
MOVE    SR, (A7)
MOVE    D0, (A7)
MOVE    5555, D1
MOVE    AAAA, D0
MOVE    2710, SR
SUBX    D1, D0
MOVE    SR, (A7)
MOVE    D0, (A7)
NOP
STOP
```

```
NOP
MOVE        AAAA, D0
MOVE        5555, D1
MOVE        FFFF, A0
MOVE        0000, D2
MOVE        1300, A6
MOVE        F0F0, (A6)
AND         D0, D1
MOVE        SR, (A7)
MOVE        D0, (A7)
MOVE        D1, (A7)
AND         (A6), D2
MOVE        SR, (A7)
MOVE        D2, (A7)
MOVE        5555, D0
MOVE        AAAA, A0
MOVE        1300, A6
MOVE        F0F0, (A6)
ANDI        0050, D0
MOVE        SR, (A7)
MOVE        D0, (A7)
ANDI        0050, (A6)
MOVE        SR, (A7)
NOP
STOP
```

```
NOP
MOVE        1300, A6
MOVE        F0F0, (A6)
MOVE        AAAA, D0
MOVE        2700, SR
OR          D0, (A6)
MOVE        SR, (A7)
MOVE        D0, (A7)
MOVE        5500, D0
MOVE        0F00, D1
OR          D0, D1
MOVE        SR, (A7)
MOVE        D1, (A7)
MOVE        0F0F, D0
MOVE        0505, D1
MOVE        A0A0, (A6)
ORI         0500, D0
MOVE        SR, (A7)
MOVE        D0, (A7)
ORI         0F, D1
MOVE        SR, (A7)
MOVE        D1, (A7)
ORI         F0, (A6)
MOVE        SR, (A7)
NOP
STOP
```

```
NOP
MOVE        F0F0, D0
MOVE        1300, A6
MOVE        A0A0, (A6)
NOT         D0
MOVE        SR, (A7)
MOVE        D0, (A7)
NOT         (A6)
MOVE        SR, (A7)
NOP
MOVE        0001, D0
MOVE        0008, D1
MOVE        8000, D2
ASL         7, D0
MOVE        SR, (A7)
MOVE        D0, (A7)
MOVE        0001, D0
ASL         D1, 0
MOVE        SR, (A7)
MOVE        D0, (A7)
ASR         D2, 7
MOVE        SR, (A7)
MOVE        D2, (A7)
MOVE        8000, D2
ASR         D2, D1
MOVE        SR, (A7)
MOVE        D2, (A7)
NOP
MOVE        0001, D2
MOVE        8000, D4
MOVE        0008, D6
```

```
LSL     7, D2
MOVE    SR, (A7)
MOVE    D2, (A7)
MOVE    0001, D2
LSL     D6, D2
MOVE    SR, (A7)
MOVE    D2, (A7)
LSR     D4, 7
MOVE    SR, (A7)
MOVE    D4, (A7)
MOVE    8000, D4
LSR     D4, D6
MOVE    SR, (A7)
MOVE    D4, (A7)
NOP
MOVE    0001, D0
MOVE    8000, D1
MOVE    0008, D2
MOVE    2710, SR
ROL     7, D0
MOVE    SR, (A7)
MOVE    D0, (A7)
MOVE    2710, SR
MOVE    0001, D0
ROL     D2, D0
MOVE    SR, (A7)
MOVE    D0, (A7)
MOVE    2700, SR
ROR     7, D1
MOVE    SR, (A7)
MOVE    D1, (A7)
MOVE    2710, SR
MOVE    8000, D1
ROR     D2, D1
MOVE    SR, (A7)
MOVE    D1, (A7)
MOVE    0000, D0
MOVE    2710, SR
ROXL    7, D0
MOVE    SR, (A7)
MOVE    D0, (A7)
MOVE    0000, D0
MOVE    2700, SR
ROXL    D2, D0
MOVE    SR, (A7)
MOVE    D0, (A7)
MOVE    0000, D1
MOVE    2710, SR
ROXR    7, D1
MOVE    SR, (A7)
MOVE    D1, (A7)
MOVE    0000, D1
MOVE    2700, SR
ROXR    D2, D1
MOVE    SR, (A7)
MOVE    D1, (A7)
NOP
STOP
```

```
NOP
MOVE    0880, D0
MOVE    2700, SR
MOVE    0800, D1
BTST    D0, 0007
MOVE    SR, (A7)
BTST    D0, 0001
MOVE    SR, (A7)
BTST    D0, D1
MOVE    SR, (A7)
NOP
MOVE    0007, D0
MOVE    0000, D2
MOVE    0006, D4
MOVE    2700, SR
BSET    D4, D2
MOVE    SR, (A7)
MOVE    D2, (A7)
BSET    D1, D2
MOVE    SR, (A7)
MOVE    D2, (A7)
BSET    0001, D2
MOVE    SR, (A7)
MOVE    D2, (A7)
MOVE    00F0, D0
MOVE    0008, D1
MOVE    0004, D2
BCLR    D1, D0
MOVE    SR, (A7)
MOVE    D0, (A7)
BCLR    D2, D0
MOVE    SR, (A7)
MOVE    D0, (A7)
BCLR    0002, D0
MOVE    SR, (A7)
MOVE    D0, (A7)
MOVE    0008, D0
MOVE    0000, D1
MOVE    0004, D2
MOVE    2700, SR
BCHG    D0, D1
MOVE    SR, (A7)
MOVE    D1, (A7)
BCHG    D2, D1
MOVE    SR, (A7)
MOVE    D1, (A7)
BCHG    0002, D2
MOVE    SR, (A7)
MOVE    D2, (A7)
NOP
STOP
```

```
NOP
MOVE    0000, D1
MOVE    0012, D2
MOVE    0022, D3
MOVE    2700, SR
MOVE    1300, A6
MOVE    0012, (A6)
MOVE    1350, A5
MOVE    0012, (A5)
ABCD    D2, D1
MOVE    SR, (A7)
MOVE    D1, (A7)
MOVE    2710, SR
ABCD    D3, D2
MOVE    SR, (A7)
MOVE    D2, (A7)
MOVE    2700, SR
MOVE    1302, A6
MOVE    1352, A5
ABCD    (A5), (A6)
MOVE    SR, (A7)
MOVE    0000, D1
MOVE    0012, D2
MOVE    0022, D3
MOVE    2700, SR
MOVE    1300, A6
MOVE    0012, (A6)
MOVE    1350, A5
MOVE    0012, (A5)
SBCD    D2, D1
MOVE    SR, (A7)
MOVE    D1, (A7)
MOVE    2710, SR
SBCD    D3, D2
MOVE    SR, (A7)
MOVE    D2, (A7)
MOVE    2700, SR
MOVE    1302, A6
MOVE    1352, A5
SBCD    (A5), (A6)
MOVE    SR, A7
MOVE    0000, D1
MOVE    FFFF, SR
MOVE    2700, SR
NBCD    D2
MOVE    SR, (A7)
MOVE    D2, (A7)
MOVE    2710, (A7)
NBCD    D1
MOVE    SR, (A7)
MOVE    D1, (A7)
NOP
STOP
```

```
100E    NOP
        MOVE    000F, D0
        MOVE    00F0, D1
        MOVE    000F, D2
        CMP     D1, D0
        BRAcc   ≠, 1050
1050    NOP
        MOVE    000F, D1
        CMP     D1, D0
        DBcc    =, 1200
1200    NOP
        MOVE    D2, (A7)
        MOVE    0000, D1
        SETcc   ≠, D2
        MOVE    D2, (A7)
        BRA     1250
1250    NOP
        BSR     1300
        NOP
        BSR     1350
1300    NOP
        MOVE    1450, A6
        RTS
1350    NOP
        MOVE    SR, (A7)
        RTR
        NOP
        STOP
```

```
NOP
MOVE        00000000, A1
MOVE        000000F0, A2
MOVE        1300, A6
MOVE        0000000F, (A6)
MOVE        2700, SR
ADDA        A2, A1
MOVE        SR, (A7)
MOVE        A1, (A7)
MOVE        00000A0A, A1
ADDA        (A6), A1
MOVE        SR, (A7)
MOVE        A1, (A7)
MOVE        00000000, A1
MOVE        00000FF0, A2
MOVE        00000FF0, A3
MOVE        2700, SR
CMPA        A1, A2
MOVE        SR, (A7)
MOVE        A2, (A7)
CMP         A3, A2
MOVE        SR, (A7)
MOVE        A2, (A7)
MOVE        00000A0A, A1
MOVE        00000A00, A2
MOVE        1300, A6
MOVE        0000000A, (A6)
SUBA        A2, A1
MOVE        SR, (A7)
MOVE        A1, (A7)
SUBA        (A6), A1
MOVE        SR, (A7)
MOVE        A1, (A7)
NOP
STOP
```

SYSTEM CONTROL

```
NOP
MOVE        00000A0A, A1
            2700, SR
            USP A1T
            SR, (A7)
            00000000, A1
            USP A1E
            SR, (A7)
            A1, (A7)
            2700, SR
            SR, (A7)
            2701, SR
            SR, (A7)
            2702, (A7)
            SR, (A7)
            2704, SR
            SR, (A7)
            2708, SR
            SR, (A7)
            270A, SR
            SR, (A7)
            0000, CCR
            SR, (A7)
            0001, CCR
            SR, (A7)
            0002, CCR
            SR, (A7)
            0004, CCR
            SR, (A7)
            0008, CCR
            SR, (A7)
MOVE        0010, CCR
            SR, (A7)
NOP
NOP
NOP
MOVE        SR, (A7)
STOP
```

CHK

```
NOP
MOVE        1000, D3
MOVE        0500, D1
MOVE        2000, D2
MOVE        2700, SR
CHK         D1, D3
NOP
NOP
MOVE        2700, SR
NOP
CHK         D2, D3
NOP
STOP
```

DIVS

```
NOP
MOVE        AAAA, D1
MOVE        0002, D2
MOVE        2700, SR
DIV         D0, D1
MOVE        AAAA, D1
MOVE        FFFFFFFE, D0
MOVE        2700, SR
DIV         D0, D1
NOP
STOP
```

```
NOP
MOVE    1300, A6
MOVE    0000, D0
MOVE    00F0, D2
MOVE    2700, SR
TAS     D0
MOVE    SR, (A7)
MOVE    D0, (A7)
MOVE    2700, (A7)
TAS     D2
MOVE    SR, (A7)
MOVE    D2, (A7)
MOVE    AAAA, (A6)
MOVE    2700, SR
TAS     (A6)
MOVE    SR, (A7)
MOVE    (A6), (A7)
MOVE    0000, D0
MOVE    F000, D2
MOVE    2700, SR
TST     D0
MOVE    SR, (A7)
MOVE    2700, SR
TST     D2
MOVE    SR, (A7)
NOP
STOP
```

APPENDIX B

DEVICE NUMBER: 1 AT 25 DEG. CENT.

***** MC68000 DC PARAMETRICS *****

1: ICC TEST (FREQ = 6MHZ) VCC = 5.5 VOLT	CHAN 0	=	161.719	MA
2: VOL : A23-1,FCP (0.5V @ 3.2MA):	CHAN 5	=	.169501	V
	CHAN 9	=	.18	V
	CHAN 10	=	.187501	V
	CHAN 11	=	.187501	V
	CHAN 12	=	.194001	V
	CHAN 13	=	.1935	V
	CHAN 14	=	.1965	V
	CHAN 15	=	.196	V
	CHAN 16	=	.202501	V
	CHAN 17	=	.202501	V
	CHAN 18	=	.211501	V
	CHAN 19	=	.210501	V
	CHAN 20	=	.2145	V
	CHAN 21	=	.220001	V
	CHAN 22	=	.223501	V
	CHAN 23	=	.229	V
	CHAN 24	=	.224501	V
	CHAN 25	=	.233501	V
	CHAN 26	=	.2345	V
	CHAN 27	=	.239	V
	CHAN 28	=	.239	V
	CHAN 29	=	.242501	V
	CHAN 30	=	.2375	V
	CHAN 31	=	.2375	V
3: VOL : FC1 (0.5V @ 3.2MA):	CHAN 7	=	.169501	V
4: VOL : AS,DS,R-W (0.5V @ 5.3MA):	CHAN 60	=	.285501	V
	CHAN 61	=	.283301	V
	CHAN 62	=	.2135	V
	CHAN 63	=	.279001	V
5: VOL : DATA0 : (0.5V @ 5.3 MA):	CHAN 2	=	.257501	V
6: VOL : DATA1 : (0.5V @ 5.3 MA):	CHAN 2	=	.267	V
7: VOL : DATA2 : (0.5V @ 5.3 MA):	CHAN 2	=	.265501	V
8: VOL : DATA3 : (0.5V @ 5.3 MA):	CHAN 2	=	.2715	V
9: VOL : DATA4 : (0.5V @ 5.3 MA):	CHAN 2	=	.2725	V
10: VOL : DATA5 : (0.5V @ 5.3 MA):	CHAN 2	=	.2765	V
11: VOL : DATA6 : (0.5V @ 5.3 MA):	CHAN 2	=	.2785	V
12: VOL : DATA7 : (0.5V @ 5.3 MA):	CHAN 2	=	.282001	V
13: VOL : DATA8 : (0.5V @ 5.3 MA):	CHAN 2	=	.284	V
14: VOL : DATA9 : (0.5V @ 5.3 MA):	CHAN 2	=	.287001	V
15: VOL : DATA10 : (0.5V @ 5.3 MA):	CHAN 2	=	.2875	V

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16: VOL : DATA11 : (0.5V @ 5.3 MA ):      CHAN 2  = .292001      V

17: VOL : DATA12 : (0.5V @ 5.3 MA ):      CHAN 2  = .2895        V

18: VOL : DATA13 : (0.5V @ 5.3 MA ):      CHAN 2  = .299501      V

19: VOL : DATA14 : (0.5V @ 5.3 MA ):      CHAN 2  = .298501      V

20: VOL : DATA15 : (0.5V @ 5.3 MA ):      CHAN 2  = .307001      V

21: VOL : BG (0.5V @ 3.2MA):              CHAN 57 = .154001      V

22: VOL : E (0.5V @ 3.2MA):               CHAN 53 = .760001E-01  V

23: VOL : VMA (0.5V @ 5.3 MA):            CHAN 52 = .146         V

24: VOL : FC2 (0.5V @ 3.2MA):             CHAN 8  = .160501      V

25: VOL : RESET (0.5V @ 5MA):             CHAN 2  = .211001      V

26: VOL : HALT (0.5V @ 1.6MA):            CHAN 54 = .203         V

27: VOH : ADR,FC2&0,BG (2.4V @ 400UA):    CHAN 6  = 3.35501      V
                                          CHAN 8  = 3.34501      V
                                          CHAN 9  = 3.36501      V
                                          CHAN 10 = 3.35001      V
                                          CHAN 11 = 3.36501      V
                                          CHAN 12 = 3.35501      V
                                          CHAN 13 = 3.38001      V
                                          CHAN 14 = 3.36501      V
                                          CHAN 15 = 3.39001      V
                                          CHAN 16 = 3.38501      V
                                          CHAN 17 = 3.39001      V
                                          CHAN 18 = 3.39001      V
                                          CHAN 19 = 3.39501      V
                                          CHAN 20 = 3.40001      V
                                          CHAN 21 = 3.42501      V
                                          CHAN 22 = 3.41001      V
                                          CHAN 23 = 3.42501      V
                                          CHAN 24 = 3.40001      V
                                          CHAN 25 = 3.40501      V
                                          CHAN 26 = 3.37501      V
                                          CHAN 27 = 3.38501      V
                                          CHAN 28 = 3.40001      V
                                          CHAN 29 = 3.44001      V
                                          CHAN 30 = 3.43501      V
                                          CHAN 31 = 3.45501      V
                                          CHAN 57 = 3.36501      V

28: VOH : DATA0 : (2.4V @ 400 UA ):       CHAN 2  = 3.33001      V

29: VOH : DATA1 : (2.4V @ 400 UA ):       CHAN 2  = 3.33001      V

30: VOH : DATA2 : (2.4V @ 400 UA ):       CHAN 2  = 3.32501      V

31: VOH : DATA3 : (2.4V @ 400 UA ):       CHAN 2  = 3.33001      V

32: VOH : DATA4 : (2.4V @ 400 UA ):       CHAN 2  = 3.32501      V

33: VOH : DATA5 : (2.4V @ 400 UA ):       CHAN 2  = 3.32501      V

34: VOH : DATA6 : (2.4V @ 400 UA ):       CHAN 2  = 3.33501      V
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35: VOH : DATA7 : (2.4V @ 400 UA ):        CHAN 2  = 3.34501      V

36: VOH : DATA8 : (2.4V @ 400 UA ):        CHAN 2  = 3.35501      V

37: VOH : DATA9 : (2.4V @ 400 UA ):        CHAN 2  = 3.36001      V

38: VOH : DATA10 : (2.4V @ 400 UA ):       CHAN 2  = 3.37501      V

39: VOH : DATA11 : (2.4V @ 400 UA ):       CHAN 2  = 3.37501      V

40: VOH : DATA12 : (2.4V @ 400 UA ):       CHAN 2  = 3.40001      V

41: VOH : DATA13 : (2.4V @ 400 UA ):       CHAN 2  = 3.37501      V

42: VOH : DATA14 : (2.4V @ 400 UA ):       CHAN 2  = 3.39001      V

43: VOH : DATA15 : (2.4V @ 400 UA ):       CHAN 2  = 3.36501      V

44: VOH : AS,UDS,LDS,WR,FC1(2.4V @ 400UA):CHAN 7  = 3.35001      V
                                          CHAN 60 = 3.37001      V
                                          CHAN 61 = 3.36501      V
                                          CHAN 62 = 3.39501      V
                                          CHAN 63 = 3.38501      V

45: VOH : E,VMA (2.4V @ 400UA):            CHAN 52 = .250001E-01  V  FAIL
                                          CHAN 53 = 3.35501      V

46: IIH : ALL INPUTS (1.0UA @ 2.4 VOLTS): CHAN 4  = .1E-02       UA
                                          CHAN 5  = -.250001E-02 UA
                                          CHAN 32 = .200001E-02  UA
                                          CHAN 33 = -.15E-02     UA
                                          CHAN 34 = .200001E-02  UA
                                          CHAN 35 = -.250001E-02 UA
                                          CHAN 36 = -.500001E-03 UA
                                          CHAN 37 = .350001E-02  UA
                                          CHAN 38 = -.250001E-02 UA
                                          CHAN 39 = .300001E-02  UA
                                          CHAN 40 = .1E-02       UA
                                          CHAN 41 = -.350001E-02 UA
                                          CHAN 42 = .200001E-02  UA
                                          CHAN 43 = -.300001E-02 UA
                                          CHAN 44 = -.500001E-03 UA
                                          CHAN 45 = .200001E-02  UA
                                          CHAN 46 = -.350001E-02 UA
                                          CHAN 47 = .250001E-02  UA
                                          CHAN 48 = -.250001E-02 UA
                                          CHAN 49 = .15E-02      UA
                                          CHAN 50 = -.300001E-02 UA
                                          CHAN 51 = .15E-02      UA
                                          CHAN 54 = .500001E-03  UA
                                          CHAN 55 = -.350001E-02 UA
                                          CHAN 56 = .200001E-02  UA
                                          CHAN 58 = -.350001E-02 UA
                                          CHAN 59 = .200001E-02  UA

47: IIL : ALL INPUTS (1.0UA @ 0.4 VOLTS): CHAN 4  = .500001E-03  UA
                                          CHAN 5  = -.250001E-02 UA
                                          CHAN 32 = .250001E-02  UA
                                          CHAN 33 = -.300001E-02 UA
                                          CHAN 34 = .200001E-02  UA
                                          CHAN 35 = .500001E-03  UA
                                          CHAN 36 = -.450001E-02 UA
                                          CHAN 37 = .300001E-02  UA
```

```
                                                CHAN 38 = -.250001E-02 UA
                                                CHAN 39 = .250001E-02  UA
                                                CHAN 40 = [illegible]
                                                CHAN 41 = -.300001E-02 UA
                                                CHAN 42 = .15E-02      UA
                                                CHAN 43 = -.350001E-02 UA
                                                CHAN 44 = .300001E-02  UA
                                                CHAN 45 = -.250001E-02 UA
                                                CHAN 46 = .200001E-02  UA
                                                CHAN 47 = -.300001E-02 UA
                                                CHAN 48 = .200001E-02  UA
                                                CHAN 49 = -.350001E-02 UA
                                                CHAN 50 = .300001E-02  UA
                                                CHAN 51 = -.300001E-02 UA
                                                CHAN 54 = .250001E-02  UA
                                                CHAN 55 = .500001E-03  UA
                                                CHAN 56 = -.450001E-02 UA
                                                CHAN 58 = .200001E-02  UA
                                                CHAN 59 = -.15E-02     UA

48: IOHZ : ALL OUTPUTS (7 UA @ 2.4VOLTS):       CHAN 6  = -.100001E-02 UA
                                                CHAN 7  = -.100001E-02 UA
                                                CHAN 8  = -.950001E-03 UA
                                                CHAN 9  = -.900001E-03 UA
                                                CHAN 10 = -.100001E-02 UA
                                                CHAN 11 = -.11E-02     UA
                                                CHAN 12 = -.950001E-03 UA
                                                CHAN 13 = -.900001E-03 UA
                                                CHAN 14 = -.100001E-02 UA
                                                CHAN 15 = -.105E-02    UA
                                                CHAN 16 = -.105E-02    UA
                                                CHAN 17 = -.900001E-03 UA
                                                CHAN 18 = -.900001E-03 UA
                                                CHAN 19 = -.100001E-02 UA
                                                CHAN 20 = -.105E-02    UA
                                                CHAN 21 = -.105E-02    UA
                                                CHAN 22 = -.900001E-03 UA
                                                CHAN 23 = -.100001E-02 UA
                                                CHAN 24 = -.950001E-03 UA
                                                CHAN 25 = -.950001E-03 UA
                                                CHAN 26 = -.11E-02     UA
                                                CHAN 27 = -.900001E-03 UA
                                                CHAN 28 = -.900001E-03 UA
                                                CHAN 29 = -.100001E-02 UA
                                                CHAN 30 = -.900001E-03 UA
                                                CHAN 31 = -.100001E-02 UA
                                                CHAN 32 = -.100001E-02 UA
                                                CHAN 33 = -.900001E-03 UA
                                                CHAN 34 = -.900001E-03 UA
                                                CHAN 35 = -.950001E-03 UA
                                                CHAN 36 = -.105E-02    UA
                                                CHAN 37 = -.950001E-03 UA
                                                CHAN 38 = -.950001E-03 UA
                                                CHAN 39 = -.100001E-02 UA
                                                CHAN 40 = -.11E-02     UA
                                                CHAN 41 = -.105E-02    UA
                                                CHAN 42 = -.950001E-03 UA
                                                CHAN 43 = -.900001E-03 UA
                                                CHAN 44 = -.100001E-02 UA
                                                CHAN 45 = -.100001E-02 UA
                                                CHAN 46 = -.900001E-03 UA
                                                CHAN 47 = -.100001E-02 UA
                                                CHAN 57 = -.900001E-03 UA
```

	CHAN 11 = 53	NS
	CHAN 12 = 58	NS
	CHAN 13 = 50	NS
	CHAN 14 = 65	NS
	CHAN 15 = 64	NS
	CHAN 16 = 54	NS
	CHAN 17 = 49	NS
	CHAN 18 = 60	NS
	CHAN 19 = 59	NS
	CHAN 20 = 56	NS
	CHAN 21 = 56	NS
	CHAN 22 = 62	NS
	CHAN 23 = 61	NS
	CHAN 24 = 54	NS
	CHAN 25 = 51	NS
	CHAN 26 = 54	NS
	CHAN 27 = 65	NS
	CHAN 28 = 60	NS
	CHAN 29 = 62	NS
	CHAN 30 = 63	NS
	CHAN 31 = 59	NS
273:CLK H TO ADDR. INVALID: (VOH & VOL)=2.5V:	CHAN 9 = 59	NS
	CHAN 10 = 58	NS
	CHAN 11 = 57	NS
	CHAN 12 = 53	NS
	CHAN 13 = 51	NS
	CHAN 14 = 55	NS
	CHAN 15 = 64	NS
	CHAN 16 = 54	NS
	CHAN 17 = 49	NS
	CHAN 18 = 60	NS
	CHAN 19 = 59	NS
	CHAN 20 = 57	NS
	CHAN 21 = 58	NS
	CHAN 22 = 60	NS
	CHAN 23 = 61	NS
	CHAN 24 = 54	NS
	CHAN 25 = 51	NS
	CHAN 26 = 64	NS
	CHAN 27 = 65	NS
	CHAN 28 = 60	NS
	CHAN 29 = 62	NS
	CHAN 30 = 63	NS
	CHAN 31 = 58	NS
274:CLK HIGH TO AS,DS T.S. (VOH = 2.5V):	CHAN 60 = 47	NS
	CHAN 61 = 35	NS
	CHAN 63 = 49	NS
275:CLK HIGH TO R-W T.S. (VOH=0.5V) :	CHAN 62 = 22	NS
276:CLK HIGH TO DATA T.S.:TCHAZX (100NS MAX):	CHAN 32 = 58	NS
	CHAN 33 = 52	NS
	CHAN 34 = 51	NS
	CHAN 35 = 48	NS
	CHAN 36 = 46	NS
	CHAN 37 = 47	NS
	CHAN 38 = 53	NS
	CHAN 39 = 55	NS
	CHAN 40 = 55	NS
	CHAN 41 = 44	NS
	CHAN 42 = 49	NS
	CHAN 43 = 51	NS
	CHAN 44 = 46	NS
	CHAN 45 = 51	NS
	CHAN 46 = 60	NS
	CHAN 47 = 53	NS

```
                                        CHAN 50 = -.100001E-02 UA
                                        CHAN 51 = -.105E-02    UA
                                        CHAN 52 = -.100001E-02 UA
                                        CHAN 53 = -.100001E-02 UA

49: IOLZ : ALL OUTPUTS (7 UA @ 0.4 VOLTS):CHAN 5  = -.100001E-02 UA
                                        CHAN 7  = -.950001E-03 UA
                                        CHAN 8  = -.900001E-03 UA
                                        CHAN 9  = -.100001E-02 UA
                                        CHAN 10 = -.950001E-03 UA
                                        CHAN 11 = -.100001E-02 UA
                                        CHAN 12 = -.900001E-03 UA
                                        CHAN 13 = -.950001E-03 UA
                                        CHAN 14 = -.100001E-02 UA
                                        CHAN 15 = -.105E-02    UA
                                        CHAN 16 = -.100001E-02 UA
                                        CHAN 17 = -.100001E-02 UA
                                        CHAN 18 = -.100001E-02 UA
                                        CHAN 19 = -.105E-02    UA
                                        CHAN 20 = -.100001E-02 UA
                                        CHAN 21 = -.850001E-03 UA
                                        CHAN 22 = -.900001E-03 UA
                                        CHAN 23 = -.100001E-02 UA
                                        CHAN 24 = -.100001E-02 UA
                                        CHAN 25 = -.950001E-03 UA
                                        CHAN 26 = -.105E-02    UA
                                        CHAN 27 = -.950001E-03 UA
                                        CHAN 28 = -.950001E-03 UA
                                        CHAN 29 = -.105E-02    UA
                                        CHAN 30 = -.100001E-02 UA
                                        CHAN 31 = -.100001E-02 UA
                                        CHAN 32 = -.900001E-03 UA
                                        CHAN 33 = -.100001E-02 UA
                                        CHAN 34 = -.100001E-02 UA
                                        CHAN 35 = -.900001E-03 UA
                                        CHAN 36 = -.950001E-03 UA
                                        CHAN 37 = -.100001E-02 UA
                                        CHAN 38 = -.105E-02    UA
                                        CHAN 39 = -.900001E-03 UA
                                        CHAN 40 = -.100001E-02 UA
                                        CHAN 41 = -.850001E-03 UA
                                        CHAN 42 = -.900001E-03 UA
                                        CHAN 43 = -.11E-02     UA
                                        CHAN 44 = -.100001E-02 UA
                                        CHAN 45 = -.950001E-03 UA
                                        CHAN 46 = -.900001E-03 UA
                                        CHAN 47 = -.100001E-02 UA
                                        CHAN 57 = -.11E-02     UA
                                        CHAN 50 = -.100001E-02 UA
                                        CHAN 51 = -.900001E-03 UA
                                        CHAN 52 = -.850001E-03 UA
                                        CHAN 53 = -.100001E-02 UA

50: INPUT LOW TEST (ALL INPUTS) : @VCC = 4.5       IIL MAX = 1 V

51: INPUT HIGH TEST (ALL INPUTS) : @VCC = 4.5      IIH MIN = 1.55024 V
```

```
81:                                  5.5      PASS

**** INTEGER ARITHMETIC INSTRUCTIONS ****
82: ADD,ADDQ INSTRUCTION TEST        4.5      PASS

83:                                  5        PASS

84:                                  5.5      PASS

85: ADDX INST. TEST                  4.5      PASS

86:                                  5        PASS

87:                                  5.5      PASS

88: CLR INST. TEST                   4.5      PASS

89:                                  5        PASS

90:                                  5.5      PASS

91: CMP,CMPI,CMPM INST. TEST         4.5      PASS

92:                                  5        PASS

93:                                  5.5      PASS

94: DIV,DIVS INST. TEST              4.5      PASS

95:                                  5        PASS

96:                                  5.5      PASS

97: EXT INST. TEST                   4.5      PASS

98:                                  5        PASS

99:                                  5.5      PASS

100: MULU AND MULS INST. TEST        4.5      PASS

101:                                 5        PASS

102:                                 5.5      PASS

103: NEG,NEGX INST. TEST             4.5      PASS

104:                                 5        PASS

105:                                 5.5      PASS

106: SUB,SUBI,SUBQ,SUBX INST. TEST4.5         PASS

107:                                 5        PASS

108:                                 5.5      PASS

109:
109: TAS,TST INST. TEST              4.5      PASS

110:                                 5        PASS
```

AD-A111 491 IBM FEDERAL SYSTEMS DIV MANASSAS VA F/G 9/2
ELECTRICAL CHARACTERIZATION OF THE 68000 MICROPROCESSOR.(U)
DEC 81 J D BAILEY F30602-80-C-0119
UNCLASSIFIED RADC-TR-81-350 NL

2 OF 2
AD A
111491

END
DATE
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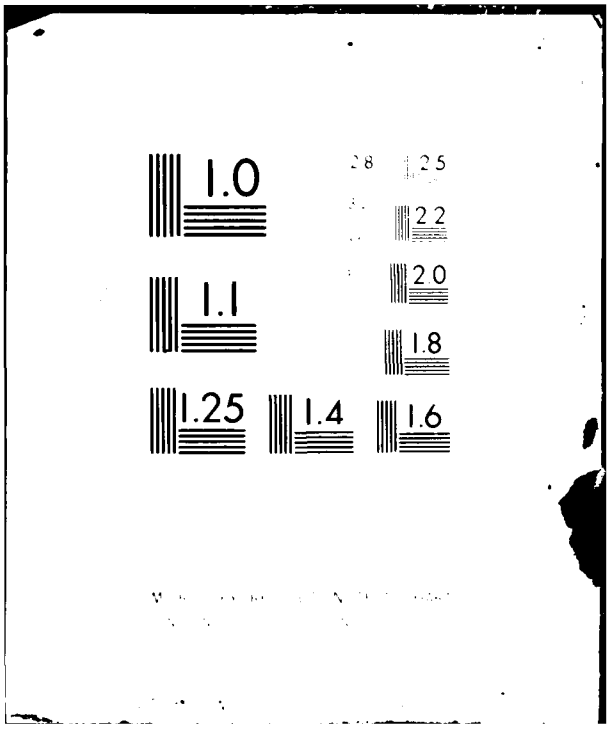
03-82
DTIC


1.0
2.8
2.5
2.2
2.0
1.1
1.8
1.25
1.4
1.6

```
111:                                5.5     PASS

**** SHIFT,ROTATE,AND LOGICAL INSTRUCTIONS ****
112: AND,ANDI INST. TEST            4.5     PASS

113:                                5       PASS

114:                                5.5     PASS

115: OR,ORI,EOR INST. TEST          4.5     PASS

116:                                5       PASS

117:                                5.5     PASS

118: NOT, SHIFT & ROTATE INST. TES4.5       PASS

119:                                5       PASS

120:                                5.5     PASS

**** BIT MANIPULATION INSTRUCTIONS ****
121: BIT(TST,SET,CLR,CHG) INST. TE4.5       PASS

122:                                5       PASS

123:                                5.5     PASS

**** BCD INSTRUCTIONS
124: BCD (ADD,SUB,NEG) INST. TEST 4.5       PASS

125:                                5       PASS

126:                                5.5     PASS

**** PROGRAM AND SYSTEM, CONTROL INSTRUCTIONS ****
127: BRANCH, JMP AND RET INST. TES4.5       PASS

128:                                5       PASS

129:                                5.5     PASS

130: ADDA, SUBA, CMPA INST. TEST    4.5     PASS

131:                                5       PASS

132:                                5.5     PASS

133: MUSP, MSR, MCCR INST. TEST     4.5     PASS

134:                                5       PASS

135:                                5.5     PASS

136: TRAP, TRAPV INST. TEST         4.5     PASS

137:                                5       PASS

138:                                5.5     PASS

139:  MC68000 INSTRUCTION DECODE VERIFICATION @ 2.85MHZ
**** DATA MOVE INSTRUCTIONS ****
140: EXG INST. TEST                 4.5     PASS
```

```
140:                                5       PASS
141:                                5.5     PASS
142: LEA INST. TEST                 4.5     PASS
143:                                5       PASS
144:                                5.5     PASS
145: PEA INST. TEST                 4.5     PASS
146:                                5       PASS
147:                                5.5     PASS
148: LINK,UNLINK INST. TEST         4.5     PASS
149:                                5       PASS
150:                                5.5     PASS
151: MOVE INST. TEST                4.5     PASS
152:                                5       PASS
153:                                5.5     PASS
154: MOVEM INST. TEST               4.5     PASS
155:                                5       PASS
156:                                5.5     PASS
157: MOVEP INST. TEST               4.5     PASS
158:                                5       PASS
159:                                5.5     PASS
160: MOVEA INST. TEST               4.5     PASS
161:                                5       PASS
162:                                5.5     PASS
163: MOVEQ INST. TEST               4.5     PASS
164:                                5       PASS
165:                                5.5     PASS
166: SWAP INST. TEST                4.5     PASS
167:                                5       PASS
168:                                5.5     PASS
**** INTEGER ARITHMETIC INSTRUCTIONS ****
169: ADD,ADDQ INSTRUCTION TEST      4.5     PASS
170:                                5       PASS
```

```
171:                                5.5     PASS
172: ADDX INST. TEST                4.5     PASS
173:                                5       PASS
174:                                5.5     PASS
175: CLR INST. TEST                 4.5     PASS
176:                                5       PASS
177:                                5.5     PASS
178: CMP,CMPI,CMPM INST. TEST       4.5     PASS
179:                                5       PASS
180:                                5.5     PASS
181: DIV,DIVS INST. TEST            4.5     PASS
182:                                5       PASS
183:                                5.5     PASS
184: EXT INST. TEST                 4.5     PASS
185:                                5       PASS
186:                                5.5     PASS
187: MULU AND MULS INST. TEST       4.5     PASS
188:                                5       PASS
189:                                5.5     PASS
190: NEG,NEGX INST. TEST            4.5     PASS
191:                                5       PASS
192:                                5.5     PASS
193: SUB,SUBI,SUBQ,SUBX INST. TEST4.5       PASS
194:                                5       PASS
195:                                5.5     PASS
196:
196: TAS,TST INST. TEST             4.5     PASS
197:                                5     * PASS
198:                                5.5     PASS
**** SHIFT,ROTATE,AND LOGICAL INSTRUCTIONS ****
199: AND,ANDI INST. TEST            4.5     PASS
200:                                5       PASS
```

```
201:                                5,5     PASS

202: OR,ORI,EOR INST. TEST          4,5     PASS

203:                                5       PASS

204:                                5,5     PASS

205: NOT, SHIFT & ROTATE INST. TES4,5       PASS

206:                                5       PASS

207:                                5,5     PASS

**** BIT MANIPULATION INSTRUCTIONS ****
208: BIT(TST,SET,CLR,CHG) INST. TE4,5       PASS

209:                                5       PASS

210:                                5,5     PASS

**** BCD INSTRUCTIONS
211: BCD (ADD,SUB,NEG) INST. TEST 4,5       PASS

212:                                5       PASS

213:                                5,5     PASS

**** PROGRAM AND SYSTEM, CONTROL INSTRUCTIONS ****
214: BRANCH, JMP AND RET INST. TES4,5       PASS

215:                                5       PASS

216:                                5,5     PASS

217: ADDA, SUBA, CMPA INST. TEST  4,5       PASS

218:                                5       PASS

219:                                5,5     PASS

220: MUSP, MSR, MCCR INST. TEST   4,5       PASS

221:                                5       PASS

222:                                5,5     PASS

223: TRAP, TRAPV INST. TEST       4,5       PASS

224:                                5       PASS

225:                                5,5     PASS
```

DEVICE NUMBER: 1 AT 25 DEG. CENT.

**** FMAX TEST ***

226:	FMAX TEST @ 4MHZ	4.5	PASS
227:		5	PASS
228:		5.5	PASS
229:	FMAX TEST @ 5.88MHZ	4.5	PASS
230:		5	PASS
231:		5.5	PASS
232:	FMAX TEST @ 7.14MHZ	4.5	PASS
233:		5	PASS
234:		5.5	PASS
235:	FMAX TEST @ 7.7MHZ	4.5	PASS
236:		5	PASS
237:		5.5	PASS
238:	FMAX TEST @ 8.3MHZ	4.5	PASS
239:		5	PASS
240:		5.5	PASS

DEVICE NUMBER: 1 AT 25 DEG. CENT.

***** MC68000 AC PERFORMANCE TESTS *****

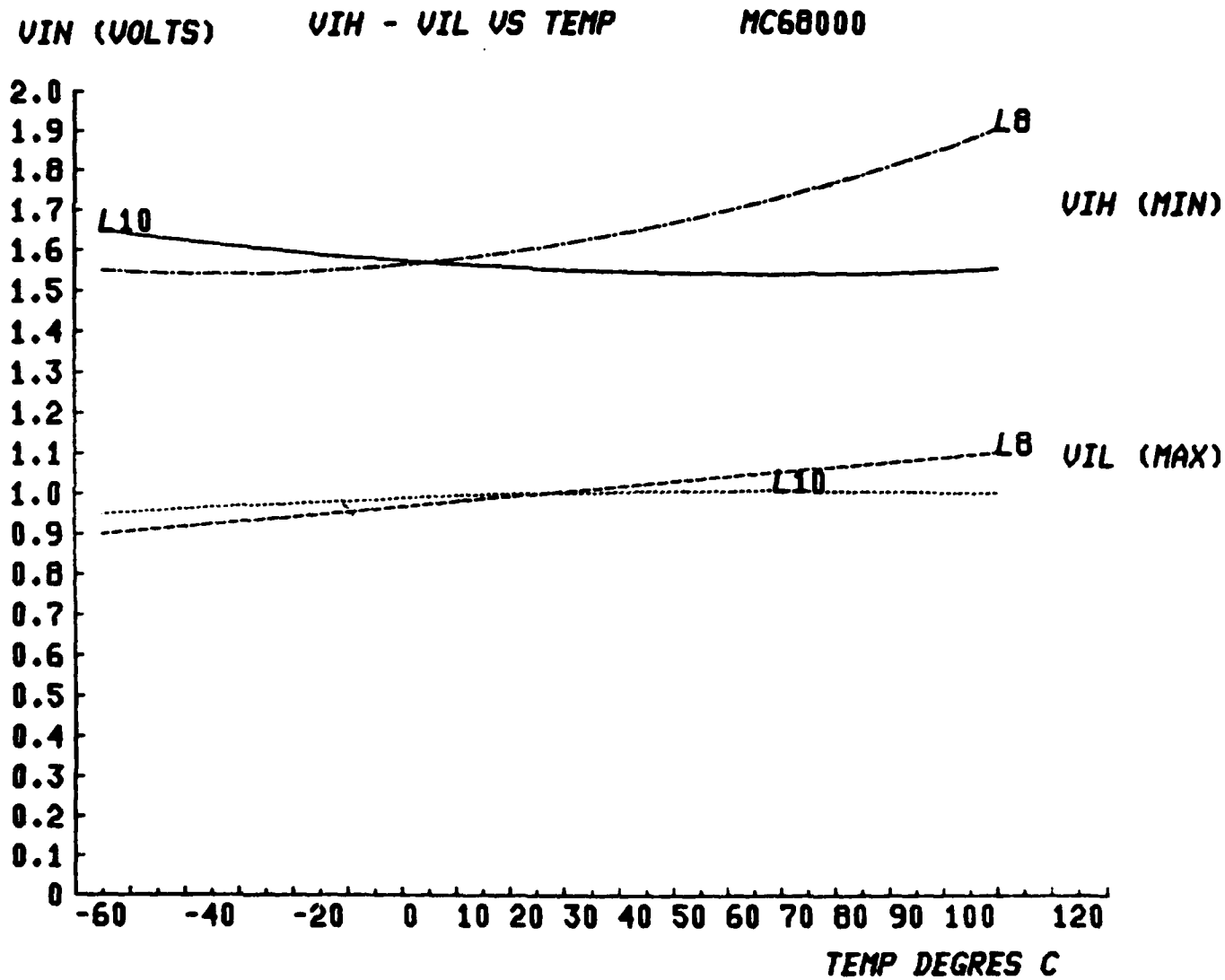
ALL SPECIFICATIONS REFLECT A 6 MHZ DEVICE

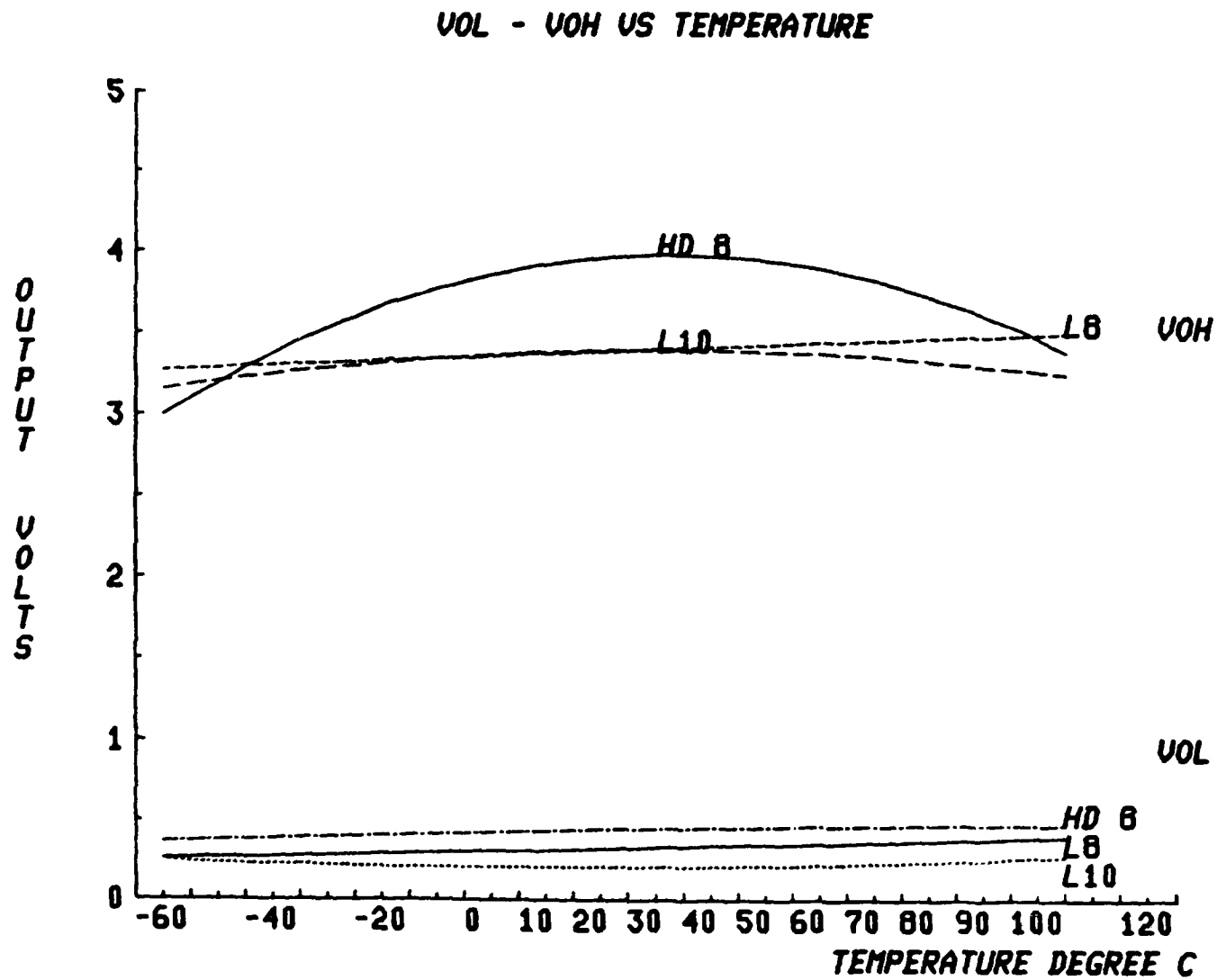
241: DIN TO CLK LOW (TSET): TDICL (25NS MIN):	CHAN 62 = 2	NS
242: DIN TO CLK LOW (THOLD): THDICL :	CHAN 62 = 0	NS
243: DTACK TO CLK LOW (TSET): TSDTCL (25NS MIN):	CHAN 62 = 0	NS
244: BR TO CLK LOW (TSET): TSBRCL :	CHAN 57 = 2	NS
245: BR TO CLK LOW (THOLD): THBRCL :	CHAN 57 = 2	NS
246: BGACK TO CLK LOW (TSET): TSBGCL :	CHAN 57 = -1	NS
247: BGACK TO CLK LOW	CHAN 57 = 0	NS
248: VPA TO CLK LOW (TSET): TSVPACL :	CHAN 52 = -5	NS
249: VPA TO CLK LOW (THOLD): THVPACL :	CHAN 52 = -3	NS
250: BERR TO CLK LOW (TSET): TSBERCL :	CHAN 62 = 3	NS
251: BERR TO CLK LOW (THOLD): THBERCL :	CHAN 62 = 4	NS
252: CLK WIDTH LOW : TCL (75NS MIN):	CHAN 32 = -22	NS
	CHAN 33 = -22	NS
	CHAN 34 = -22	NS
	CHAN 35 = -22	NS
253: CLK WIDTH HIGH : TCH (75NS MIN):	CHAN 32 = 42	NS
	CHAN 33 = 41	NS
	CHAN 34 = 41	NS
	CHAN 35 = 41	NS
254: CLK HIGH TO FC VALID : TCLAV (80NS MAX):	CHAN 6 = 39	NS
	CHAN 7 = 34	NS
255: CLK HIGH TO AS LOW (MIN): TCHSLX (20NS MIN)	CHAN 63 = 33	NS
256: CLK HIGH TO AS LOW (MAX): TCHSLN (70NS MAX):	CHAN 63 = 40	NS
257: CLK HIGH TO DS LOW (MIN): TCHSLX (20NS MIN)	CHAN 60 = 31	NS
	CHAN 61 = 29	NS
258: CLK HIGH TO DS LOW (MAX): TCHSLN (70NS MAX):	CHAN 60 = 37	NS
	CHAN 61 = 34	NS
259: CLK LOW TO AS HIGH: TCLSH (80NS MAX):	CHAN 63 = 41	NS
260: CLK LOW TO DS HIGH: TCLSH (80NS MAX):	CHAN 60 = 40	NS
	CHAN 61 = 49	NS
261: CLK H TO R-W H (MAX): TCHRHX (80NS MAX):	CHAN 62 = 25	NS

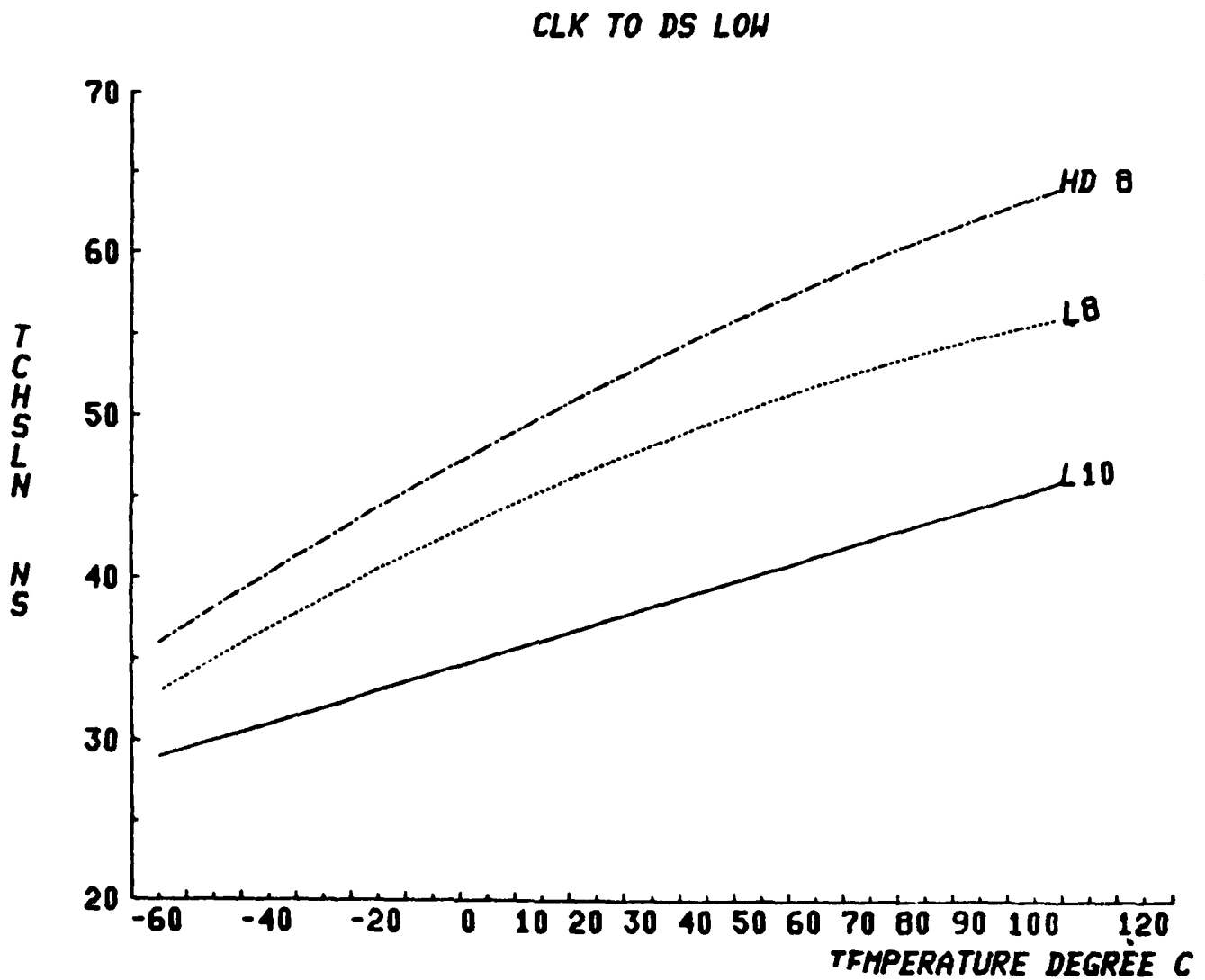
262: CLK H TO R-W H (MIN): TCHRHX (20NS MIN):	CHAN 62 = 15	NS
263: CLK HIGH TO R-W LOW: TCHRL (80NS MAX):	CHAN 62 = 19	NS
264: CLK LOW TO DOUT VALID: TCLDO (80NS MAX):	CHAN 32 = 35	NS
	CHAN 33 = 34	NS
	CHAN 34 = 36	NS
	CHAN 35 = 37	NS
	CHAN 36 = 36	NS
	CHAN 37 = 34	NS
	CHAN 38 = 33	NS
	CHAN 39 = 36	NS
	CHAN 40 = 36	NS
	CHAN 41 = 33	NS
	CHAN 42 = 36	NS
	CHAN 43 = 34	NS
	CHAN 44 = 33	NS
	CHAN 45 = 35	NS
	CHAN 46 = 0	NS
	CHAN 47 = 30	NS
265: CLK L TO ADDR. VALID: TCLAV (80NS MAX):	CHAN 9 = 41	NS
	CHAN 10 = 38	NS
	CHAN 11 = 47	NS
	CHAN 12 = 39	NS
	CHAN 13 = 47	NS
	CHAN 14 = 49	NS
	CHAN 15 = 50	NS
	CHAN 16 = 46	NS
	CHAN 17 = 29	NS
	CHAN 18 = 49	NS
	CHAN 19 = 53	NS
	CHAN 20 = 35	NS
	CHAN 21 = 44	NS
	CHAN 22 = 32	NS
	CHAN 23 = 0	NS
	CHAN 24 = 46	NS
	CHAN 25 = 46	NS
	CHAN 26 = 45	NS
	CHAN 27 = 49	NS
	CHAN 28 = 49	NS
	CHAN 29 = 50	NS
	CHAN 30 = 45	NS
	CHAN 31 = 45	NS
266: CLK HIGH TO BG LOW : TCHGL (80NS MAX):	CHAN 57 = 19	NS
267: CLK HIGH TO BG HIGH : TCHGH (80NS MAX):	CHAN 57 = 20	NS
268: CLK LOW TO VMA LOW : TCLVML (80NS MAX):	CHAN 52 = 29	NS
269: CLK HIGH TO VMA HIGH : TCHVMH :	CHAN 52 = 22	NS
270: CLK LOW TO E LOW : TCLEL :	CHAN 53 = 23	NS
271: CLK LOW TO E HIGH : TCLEH :	CHAN 53 = 21	NS
272:CLK H TO ADDR.-FC T.S. (VOH & VOL)-0.5V:	CHAN 6 = 57	NS
	CHAN 7 = 56	NS
	CHAN 8 = 58	NS
	CHAN 9 = 60	NS
	CHAN 10 = 63	NS

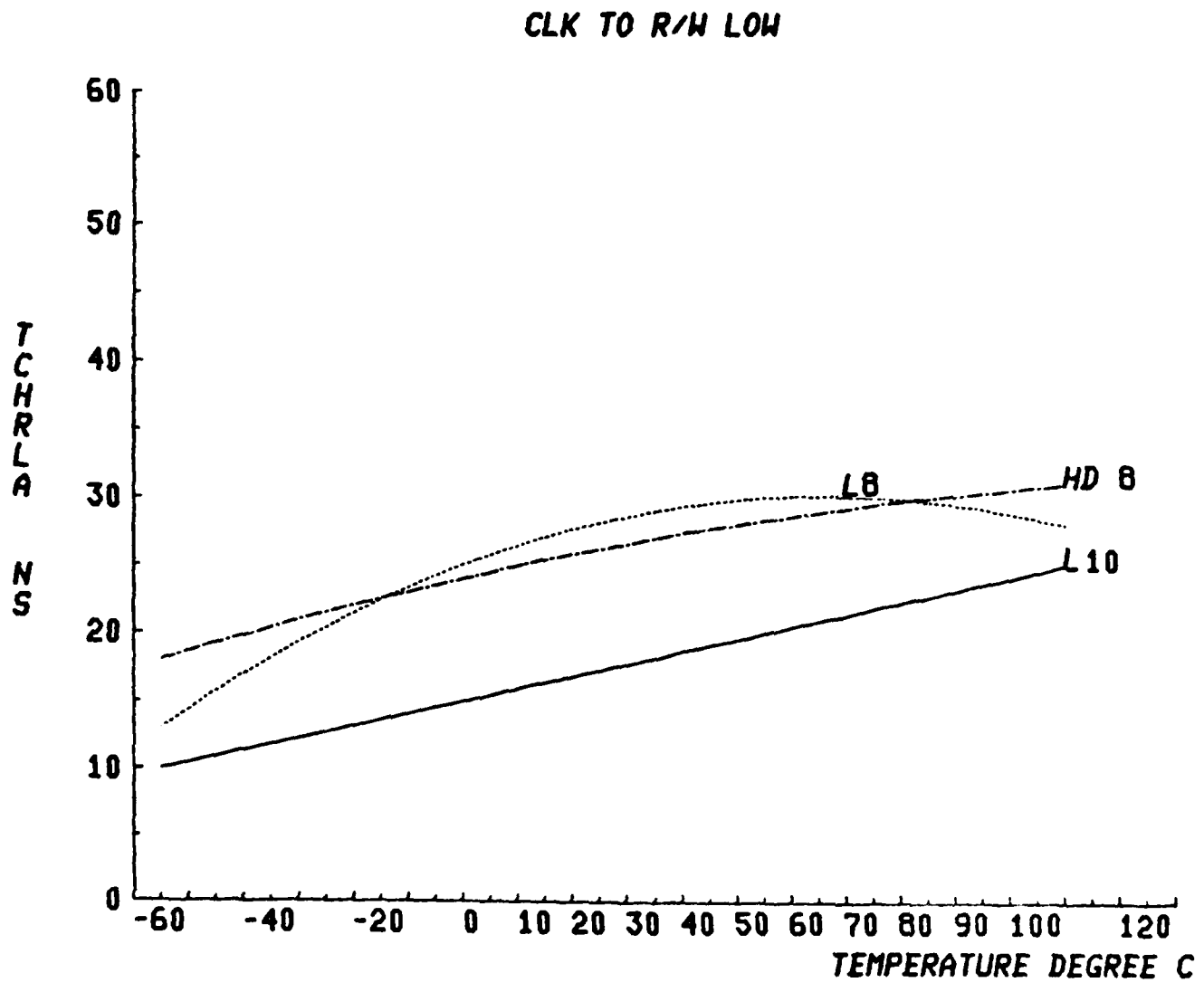
APPENDIX C

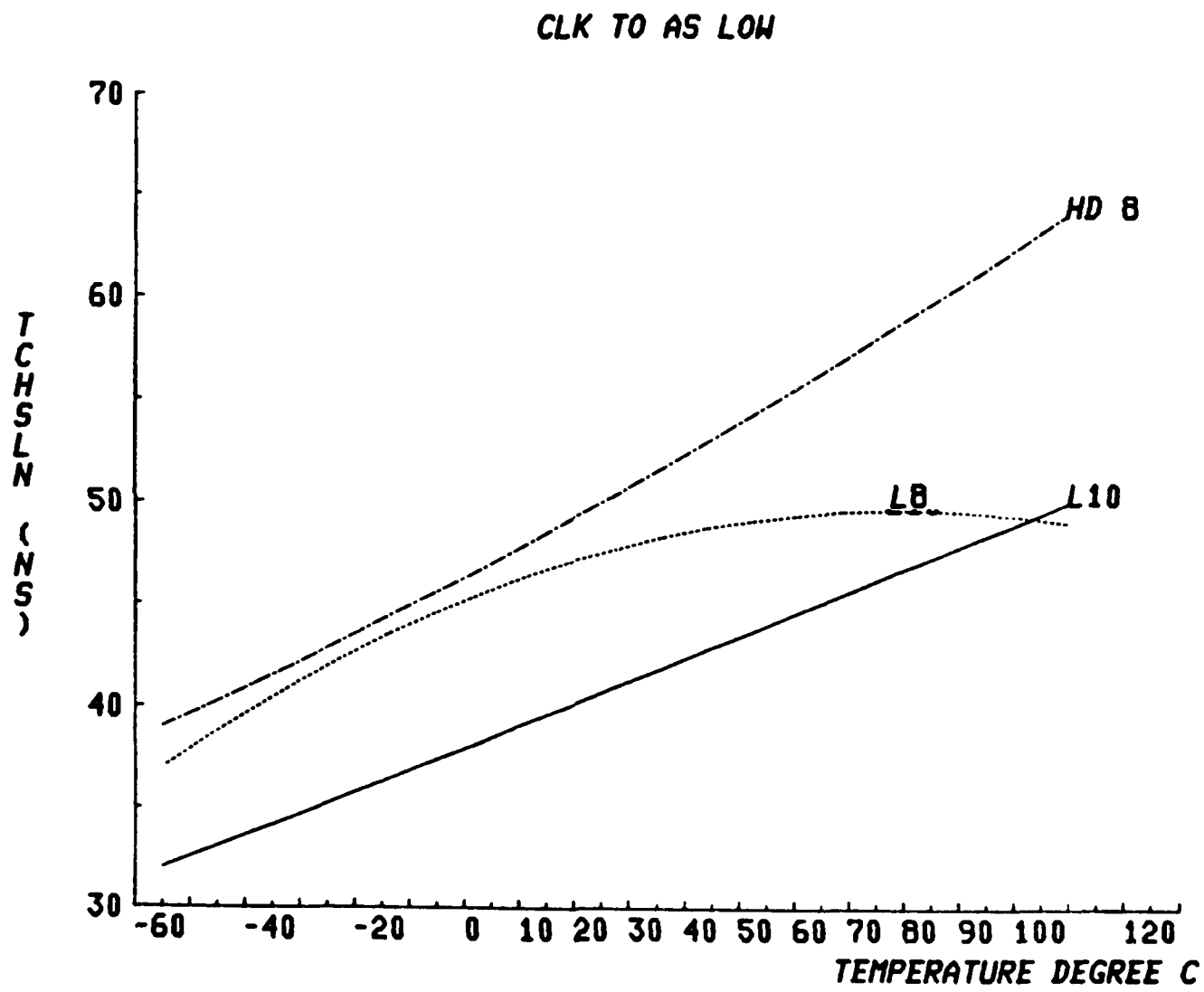
THE FOLLOWING GRAPHS ARE SELECT PARAMETERS OBTAINED FROM THE MOST RECENT MC68000L8, MC68000L10 AND HITACHI HD68000 DEVICES. THE DATA IS REPRESENTATIVE OF THE WORSE CASE DATA OBTAINED ACROSS THE TEMPERATURE RANGE OF -55°C TO +110°C T_{CASE}.

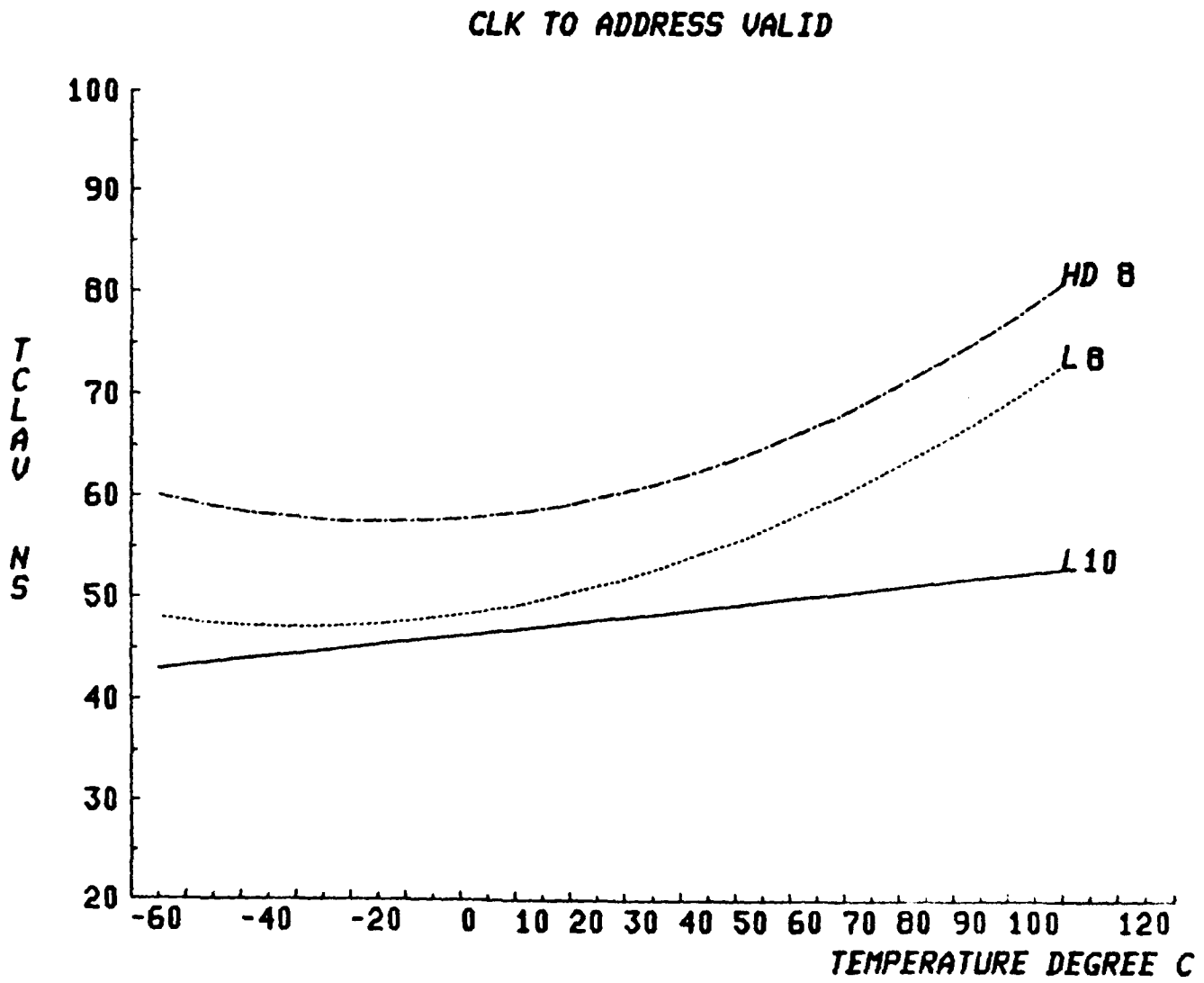

VIN (VOLTS)
VIH - VIL VS TEMP
MC68000
2.0
1.9
1.8
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
-60
-40
-20
0
10
20
30
40
50
60
70
80
90
100
120
TEMP DEGRES C
L8
L10
VIH (MIN)
L8
L10
VIL (MAX)


VOL - VOH VS TEMPERATURE
OUTPUT VOLTS
5
4
3
2
1
0
HD 8
L10
L8
VOH
VOL
HD 8
L8
L10
-60
-40
-20
0
10
20
30
40
50
60
70
80
90
100
120
TEMPERATURE DEGREE C


CLK TO DS LOW
TCHSLN NS
70
60
50
40
30
20
HD 8
L8
L10
-60 -40 -20 0 10 20 30 40 50 60 70 80 90 100 120
TEMPERATURE DEGREE C


CLK TO R/W LOW
TCHRLA NS
60
50
40
30
20
10
0
-60
-40
-20
0
10
20
30
40
50
60
70
80
90
100
120
TEMPERATURE DEGREE C
LB
HD 8
L10


CLK TO AS LOW
TCHSLN (NS)
70
60
50
40
30
-60
-40
-20
0
10
20
30
40
50
60
70
80
90
100
120
TEMPERATURE DEGREE C
HD 8
LB
L10


CLK TO ADDRESS VALID
TCLAV NS
100
90
80
70
60
50
40
30
20
-60
-40
-20
0
10
20
30
40
50
60
70
80
90
100
120
TEMPERATURE DEGREE C
HD 8
L 6
L 10

REFERENCES

1. Motorola Users Guide MC68000UM (AD)-(AD2)
2. Motorola Data Sheet AD1-814R2

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