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JUN 79 J B WILLIS, E R LORDING, L J ROBERTS
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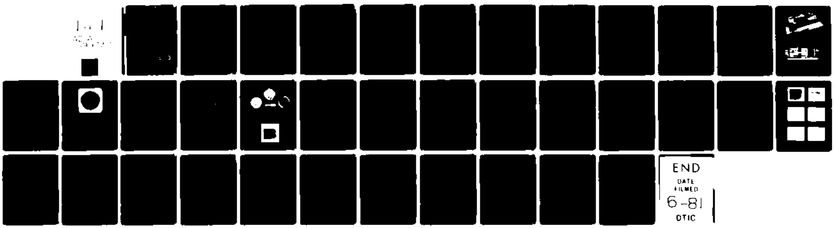

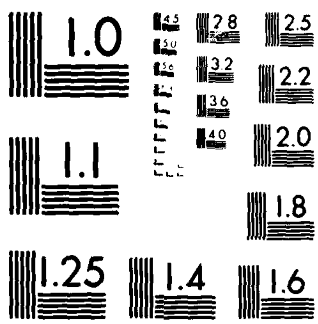

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AERODYNAMICS NOTE 394

SOLID STATE ELECTRONICS FOR AN AUTOMATIC SELF-BALANCING CAPSULE MANOMETER

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J. B. WILLIS, E. R. LORDING and L. J. ROBERTS

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SUMMARY

Modern solid state electronics for use with Midwood and Hayward (Ref. 1) automatic manometers are described. Essentially the motor transmitter unit is replaced with CMOS shift registers which generate the waveforms needed to drive the repeater motors and also provide the necessary memory. By powering the shift registers from dry cells when power is off, a memory of about a year is provided since the current drawn is so small. The rest of the circuitry uses an amplifier, phase detector, voltage controlled oscillator and power stage.

In addition, a system which eliminates the digitizer and/or replaces the indicator with a digital display is described. This system uses CMOS presettable up-down counters giving a direct BCD output with "memory", or a binary output if preferred.

Circuit details of both stages are included.

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16. *ABSTRACT*

Modern solid state electronics for use with Midwood and Hayward automatic manometers are described. Essentially the motor transmitter unit is replaced with CMOS shift registers which generate the waveforms needed to drive the repeater motors and also provide the necessary memory. By powering the shift registers from dry cells when power is off, a memory of about a year is provided since the current drawn is so small. The rest of the circuitry uses an amplifier, phase detector, voltage controlled oscillator and power stage.

In addition, a system which eliminates the digitizer and/or replaces the indicator with a digital display is described. This system uses CMOS presettable up-down counters giving a direct BCD output with "memory", or a binary output if preferred.

Circuit details of both stages are included.

CONTENTS

1. INTRODUCTION

The A.R.L. transonic wind tunnel has used automatic self-balancing capsule type manometers, designed by Midwood and Hayward (Ref. 1) of R.A.E., for over twenty years. They are normally used for the measurement of test section static and total pressure and model base pressure. From the static and total pressure the test section Mach number is computed and displayed. For these measurements of absolute pressure, they have performed very satisfactorily for a very long time. However, transmitter brushes and commutators do wear and need servicing, and the valve type electronics raises problems of maintenance and replacement. It was therefore decided to investigate replacing all the electronics, as an interim measure while more modern techniques of absolute pressure measurement were being investigated. Consequently, the replacement electronics were required to be simple and inexpensive, to maintain the same accuracy, and if possible to be more reliable.

The first stage of the work described consisted of modernizing the electronics and eliminating valves and motor generators. Later, it became apparent that it would be a simple matter to obtain a digital output by purely electronic means. It was then possible to eliminate electro-mechanical digitizers and their associated decoders, and to provide for digital display and recording much more readily. The second stage therefore is described as an addition to the main part of the work, and it may well be that a better, integrated arrangement is possible. This has not been investigated as the first stage had been installed and put into operation before the second stage had been completed, and a complete rebuild was not warranted.

The first stage of the work described here was carried out early in 1978, the second stage in 1979.

2. THE ORIGINAL MANOMETERS

The automatic manometers consist of two bellows, one evacuated and the other connected to the pressure to be measured, a repeater motor driving a balancing weight along a lead screw, a balance point detector and a dashpot, with the whole arrangement mounted as a balance on spring centres as shown in Figures 1 and 2 from Reference 1. In operation, a change in pressure causes the beam to deflect, which produces an output from the electromagnetic detector. This output increases in amplitude with distance of the beam from balance, and undergoes a phase shift of 180° as the beam passes through the balance point. It is used to drive the repeater motor in the right sense to move the weight and rebalance the system.

Similar repeater motors are simultaneously and identically stepped and these motors drive indicators and/or digitizers as required, and so indicate the absolute pressure being applied. The indicators read in inches of mercury (see Fig. 2(*b*)) so that one small division = 0·01 and this is the stated accuracy of the system. However, one step of the repeater motor is one half of one small division and this is the resolution of the system.

The original electronics are shown schematically in Figure 3, and the actual circuit in Figure 4.

It will be seen that the transmitter is motor driven, and so it is stationary when power is turned off, and knows where it is when power is again turned on—i.e. it "remembers".

The actual transmitter is shown in Figure 5, and the brushes connect +24v and ground through the various segments to produce the train of pulses needed to drive the repeater motors. It will also be seen from Figure 5, that the transmitter has four small square segments. These are to prevent the brush short circuiting the supply to ground and are electrically isolated or "OFF". Waveforms for the three output lines to the repeater motors, measured on one of the original units, are shown in Figure 6 which is a photograph of the actual oscilloscope traces obtained using a storage oscilloscope.

3. DESIGN OF NEW CIRCUITRY

One of the requirements of the new electronics was the elimination of the transmitters and the need to service their brushes. Thus a new way of producing the necessary pulse train had to be found, and it still had to have a memory. Obviously a shift register could be used to produce the pulse train, and driven by a voltage controlled oscillator (VCO) would give the necessary change of speed with change of input signal amplitude. The availability of CMOS integrated circuits with their very low current drain made indefinite operation from dry cells possible, and the 40194 integrated circuit selected has a freeze capability, so that when the main power supply goes low the shift register cannot move. The whole design then became relatively straightforward, and is shown schematically in Figure 7.

Preliminary work showed that the repeater motors could be driven as conventional 3 phase stepper motors, but this gave only half the accuracy—i.e. 1 small division per step instead of 2 steps per small division. It was desired to retain the maximum accuracy possible, and this mode of operation was discarded. With no data available on the repeater motors, it was therefore decided to reproduce the original drive wave forms. Half step operation in the conventional stepper motor meaning may be possible, but has not been investigated because of the uncertainty about the motor characteristics.

In Figure 8 is shown the amplifier, multiplier, and rectifier. No quadrature capacitor at the weighbeam is used, since this appeared to reduce the amplitude of the output, and have no other effect. The A.C. amplifier is conventional, and the multiplier is set up following the manufacturer's recommendations. (Ref. 2). The D.C. output from the multiplier follows the amplitude of the transducer signal and increases as the beam moves away from the null position. The sign of the multiplier output is determined by the phase of the transducer signal, and since there is a 180° phase shift as the beam passes through the null position, the sign of the multiplier output is determined by which side of the null position the beam is at any time. Multiplier ripple is filtered out, and the remaining D.C. signal level adjusted to give a signal going from 0 volt to +5 volts to control the direction of the shift registers. The D.C. signal is also rectified to give a D.C. signal dependent only on amplitude and this is used to drive the VCO.

The magnitude of the D.C. signal from the multiplier output is about ±2·0 volts for about ±7 small divisions deflection on the indicator.

The VCO (Fig. 9) is preceded by a buffer giving D.C. offset adjustment, as well as some gain, and operates so that 0 volts in gives 0 volts out. (Ref. 3). The VCO is a standard one, (Ref. 3) and gives, for the values shown in Figure 9, about 50 Hz for $Vin = 0$ volts to about 3,700 Hz for $Vin = +10$ volts and 5,300 Hz for $Vin = +15$ volts. In practice, a frequency ratio of about 80 : 1 is achieved, and the final desired frequency range selected using the two counters (Fig. 9) for frequency dividing. It should be noted that this VCO never stops, and the indicator therefore oscillates with an amplitude of one half of one small division (or one step) with a frequency less than 1 Hz. This was a deliberate choice, as most tunnel operators prefer to know that the system is alive. Obviously, by looking at the rectified output with a comparator, plus some gating, the output from the counters could be frozen at the null point, and the indicators would then stop at balance, instead of oscillating very slowly as in the present arrangement. With the values shown and for a tickover frequency of less than 1 Hz, the system responds rapidly and gives a small overshoot when returning from large beam deflections. In normal use, there is no overshoot.

For setting up the VCO, the potentiometer is adjusted until the lowest frequency of oscillation is obtained with the beam, of course, in its balanced position. The potentiometer should then be wound back until a small increase in frequency is detected.

In Figure 10 is shown the shift register arrangement. It will be seen that when the +5 volt supply goes low, dry cells take over and keep all the CMOS components alive. When the +22 volt supply used for the power stage goes low, the operation of the shift registers is frozen. To understand the operation of the shift registers, it is perhaps easier to consider first a 6 bit shift register generating conventional 3 phase wave forms. The shift registers are loaded (either parallel or serial) with three high followed by three low inputs, and connected end to end in both directions. Generation of output waveforms is shown in Figure 11, where one half of the complete waveform is given. Figure 12 shows the waveforms generated by shifting right and left, and it will be clear that changing from shift right to shift left is equivalent to interchange of two phases or reversal of direction of the motor.

For the circuit actually used it is required to produce an "OFF" pulse one sixth the length of the high and low states. This requires a twelve bit shift register, this time loaded with six high and six low inputs, connected both ways end to end as before, driven by clock pulses from the VCO, and direction being provided by the multiplier output. The "OFF" pulses are generated by detecting when the level of the correct two successive bits of the shift register output are of opposite sign. In Figure 13 are shown the actual wave forms generated by the shift register with the NOT wave forms produced by straight inverters. The "OFF" pulses are derived from XOR gates, and the complete circuit diagram of this portion of the system is given in Figure 10.

The power stage is also shown in Figure 10. The Darlington pair configuration was used to reduce power dissipation as well as to provide gain. With the transistor used and about one ampere for three repeater motors in parallel, the voltage drop is about 0·6 volts per Darlington pair, giving about 3·6 watts for the printed circuit board. For the most part, both inputs for each drive stage go up and down together, so that the output voltage goes to +22 volts or ground as required. The exception is the "OFF" case, when the input to the 2N5192 goes low and that to the 2N5195 goes high, so that both transistors are "OFF". The waveforms at the inputs follow from Figure 13 and are shown in Figure 14. Also shown is the collector output to one of the three repeater motor wires, and it will be seen that this is very close to that produced by the original commutator in the original transmitters. Photographs of the actual waveforms are shown in Figure 15.

Power supplies used are conventional regulated supplies and are not shown here. However to ensure that the driver stage is only powered up after the comparators preceding it and all the other voltages have stabilized, the arrangement using a relay is shown in Figure 16. When power is turned off the same relay drops out and cuts power to the driver stage before any of the other voltages start to fall. This is a precaution to try and eliminate spurious pulses being produced during turn ON and OFF.

For setting up purposes, various devices are needed. The weighbeam motor may be switched off, and the VCO and hence the indicator and digitizer run independently of the multiplier, in either direction. A fine zero adjust is shown on the amplifier circuit, and gives a total range of about seven small divisions. A manual push button is provided to load the shift register code, although this is only required when the system is first powered up. Figure 17 shows the control panel for one channel and the wiring of the switches required.

A "Freeze" control is provided which simply inhibits the VCO output, and so completely stops operation of the indicators, weighbeams and digitizer. This is useful for injecting fake digitizer inputs for checking computer interfaces, programs etc. However, if the code load button is pressed with a channel frozen, in general the code will be destroyed, and so the code load must only be used with all channels operating.

Finally, since only four channels were needed, no attempt has been made to minimize components, as the cost of components is small. For larger installations, considerable reductions could be possible and worthwhile. In size, the amplifier, VCO, and driver stages each use a printed circuit board about 65 mm by 125 mm and the shift register PCB is about twice that size. Consequently, the volume occupied by one channel is quite small. Since multipliers tend to run warm, it is preferable not to overcrowd this board.

4. PERFORMANCE

In operation, there appears to be an initial drift for about fifteen minutes as the amplifiers and multipliers warm up and this drift is of the order of two small divisions. Subsequently, the drift appears to be about one click or one half of one small division per hour or two, and is probably within the accuracy of the whole system. Out of phase oscillations of one click tend to degrade the maximum possible accuracy, but again the obtainable accuracy is probably that of the whole system.

5. ELIMINATION OF DIGITIZERS

Digitizers are now expensive items, and still tend to be less reliable than most other modern electronic components. Further, the original digitizers provide an output in Petherick code, which has to be decoded. There seemed therefore, to be good reasons to consider eliminating digitizers. In essence, all that is required is to count the VCO clock pulses. B.C.D. counters will then give an output which may be displayed and/or fed directly into a computer, thus eliminating digitizers and decoders. (Fig. 18). As will be seen in the following description, other advantages arise, and some of these, from the tunnel operator's point of view, are most attractive.

The circuit actually used is shown in Figure 19. Clock pulses from the VCO are counted using CMOS presettable up-down counters. The I.C.s used are CD4029 which may be used as B.C.D. or binary counters depending on the state of pin 9. Here, the first counter is wired as a binary counter, and the others as B.C.D. counters whose outputs are buffered and then fed to the displays and to the computer interface. Direction comes from the amplifier card, just as for the shift registers, and when power goes off, the counter card is powered by the same batteries as the shift register card. To ensure both counters and shift registers stay synchronized, the freeze for the counters is taken from a 74CO4 gate on the shift register card, (Fig. 10) and is used to stop the VCO.

Each clock pulse corresponds to one half of one small division on the old indicators, and the weighbeam motors still operate to this accuracy, and oscillate about the balance point to this accuracy just as before. However, in the arrangement used here, the half division is not displayed quantitatively as the overall accuracy of the system does not seem to warrant it. Instead, it is used to make the decimal point on the display flash on and off and so indicate that that channel is alive and running.

This arrangement necessitates dividing the clock frequency by two, taking direction into account, before the B.C.D. counters. The circuit used is shown in Figure 20. Here Q1, Q2, Q4 all apply to the first counter, which is connected as a binary counter, with the load inputs all grounded. Direction from the amplifier card is first inverted and then fed to all the counters. It is then XOR'd with Q4, and the output from the XOR gate is high when both direction and Q4 are correct for counting up or down. The result is that a carry is produced by Q1 and fed to the first B.C.D. counter, unless the direction changes too soon. The other part of the circuit resets this counter after a count of two, and the main comment here is that the Q2 non-inverting gate is needed for timing purposes.

The modifications to the shift register circuit are shown dotted in Figure 10. The VCO circuit is also modified to that shown in Figure 21. The counters on the VCO card are now CMOS, the freeze line is now controlled from the counter card, and a soft start has been incorporated. The reason for the latter is that if a pressure change occurs with power off, the weighbeam deflects. When mains power is then turned on, there is a time delay before the shift registers, counters, etc., start operating, for reasons dealt with previously. During this delay, the VCO output will be frozen, but the actual oscillator may be running at full speed. Thus, when the power supply relay closes, the whole system may be required to start, instantly, at top speed. Since the weighbeam motor may not be able to accelerate so rapidly, it is preferable to ramp up to speed quite slowly. Normal operation is, of course, not affected in any way.

Since the counters are presettable, and no digitizers are used, one set of B.C.D. switches may be used to preset all counters. Then in operation, the absolute reference pressure is read, set on the switches, and the load button pressed, and all channels are set up ready for operation. With some additional circuitry, included in Figure 19 all channels and the shift registers are frozen. This stops the weigh beams running, and each channel may be loaded individually, thus permitting "fake" inputs, which are useful for checking out of wiring, computer programmes etc. There is no longer any need to set up the indicator and then adjust the digitizer output to match. It is therefore possible to remove the set-auto switch, the up-down switch, the speed control potentiometer, the weighbeam ON-OFF switch and the freeze button, resulting in a much simpler control system. The fine adjustment potentiometer has been retained to allow small adjustments if needed. A sketch of the control panel is shown in Figure 22.

The display wiring is shown in Figure 23, and is conventional.

It should be noted that if digitizers are eliminated, and digital displays replace the original indicators, the driver stage of Figure 10 now has to drive only one repeater motor instead of three or four. This reduces the maximum current to about 0·25 amp., and lower power dissipation and less heating are immediately achieved, and the driver stage could be simplified.

However, the biggest advantages arise in setting up, since display and output for all channels can be easily set by one operation, and the displayed reading is the same as that going to the computer interface. Previously, although digitizer outputs were set up to match the indicated output, and both set up to the correct value, for each individual channel, there was no means of being sure they stayed that way i.e. digitizer malfunction was not necessarily apparent. Whether digital displays are preferred to the original indicators is a matter of personal preference, and of course the original indicators may be retained. However, to set them up to their correct values requires retention of the setting up controls.

6. FURTHER DEVELOPMENT

It should be pointed out that with the circuits given, it is possible for the clock pulse to arrive at the shift register and at the CMOS counters at the same time as the direction control changes. Specifications require the direction to be held about one hundred nanoseconds before the clock pulse arrives. It is not known what happens if this "set up" time is not provided. In practice, it does not seem to occur and obviously the probability is very small indeed.

As drawn, the VCO is approximately linear, as is the amplifier and the transducer output. It would seem that there could be advantages in making the system non-linear, with a high gain at the balance point and reducing the slope away from balance. This has not been investigated, but a spare amplifier is available on the LM3900 which could be used for this or any other purpose.

It would also be preferable to operate all the CMOS components from a higher voltage than +5, as used here. This would provide a better noise margin.

CONCLUSIONS

Modern solid state electronics for use with Midwood and Hayward automatic absolute manometers have been described. Occupying small volume and with no moving parts and still with a memory, much higher reliability should be achieved with the same performance as the original valve electronics. Details of a method which eliminates digitizers and provides digital displays are included.

ACKNOWLEDGMENT

The authors wish to acknowledge the assistance of Mr R. G. Broadbent.

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2.	—	Semiconductor Data Library. Vol. 6. CMOS Series B. Motorola Semiconductors Products Inc.
3.	—	Linear Applications. National Semiconductor Corporation. Editor: M. K. Vanderkooi.

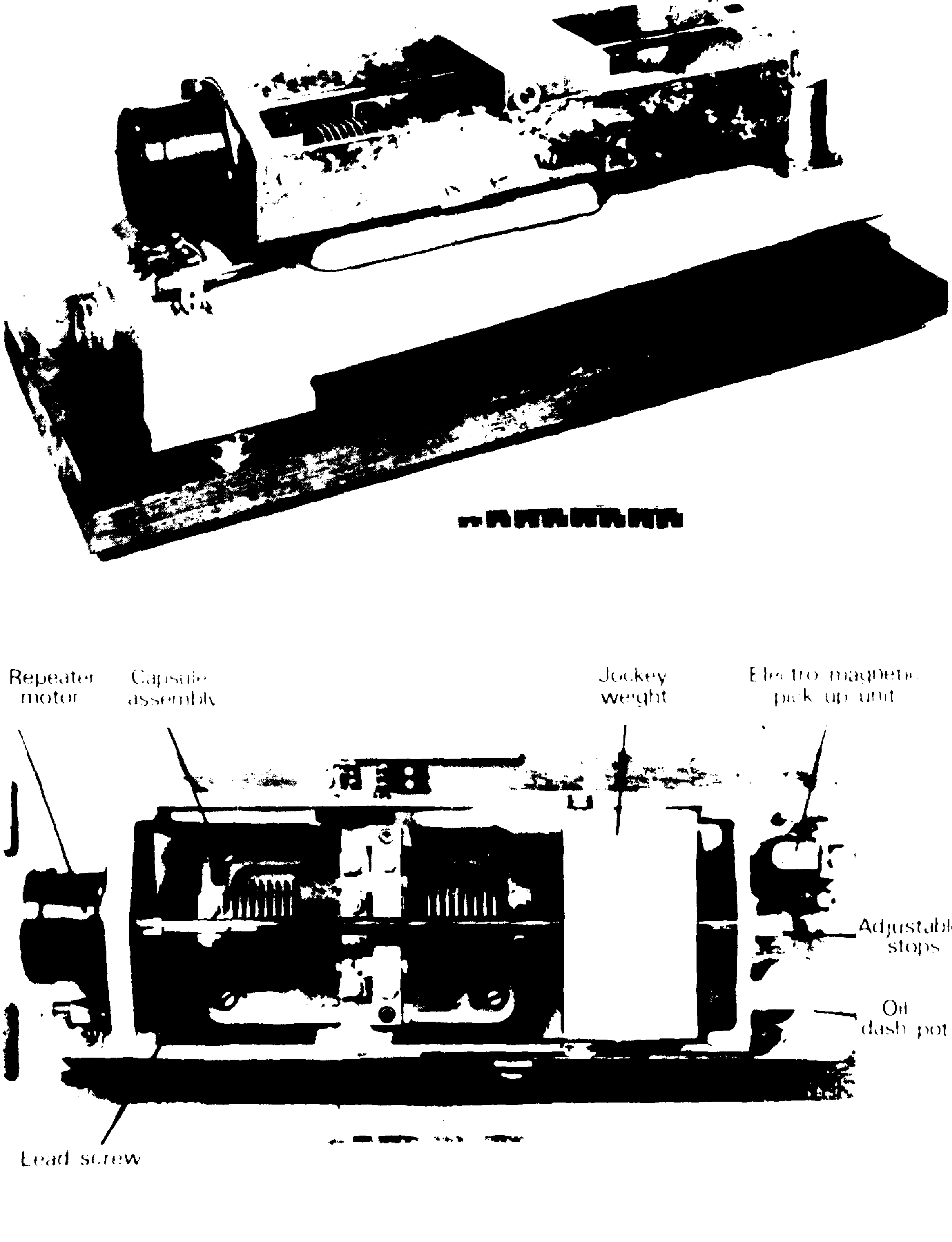


FIG. 1: AUTOMATIC MANOMETER (FROM REF. 1)

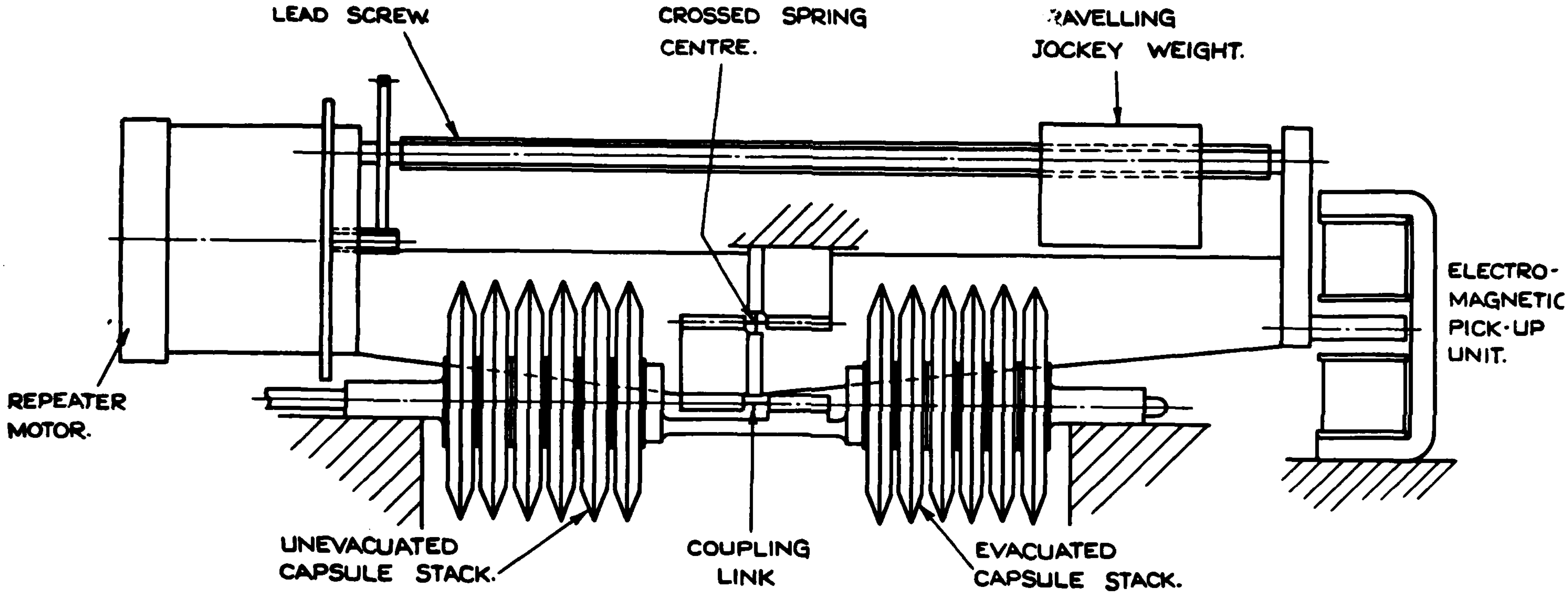


FIG. 2(a): DIAGRAMMATIC ARRANGEMENT—AUTOMATIC MANOMETER
(FROM REF. 1)

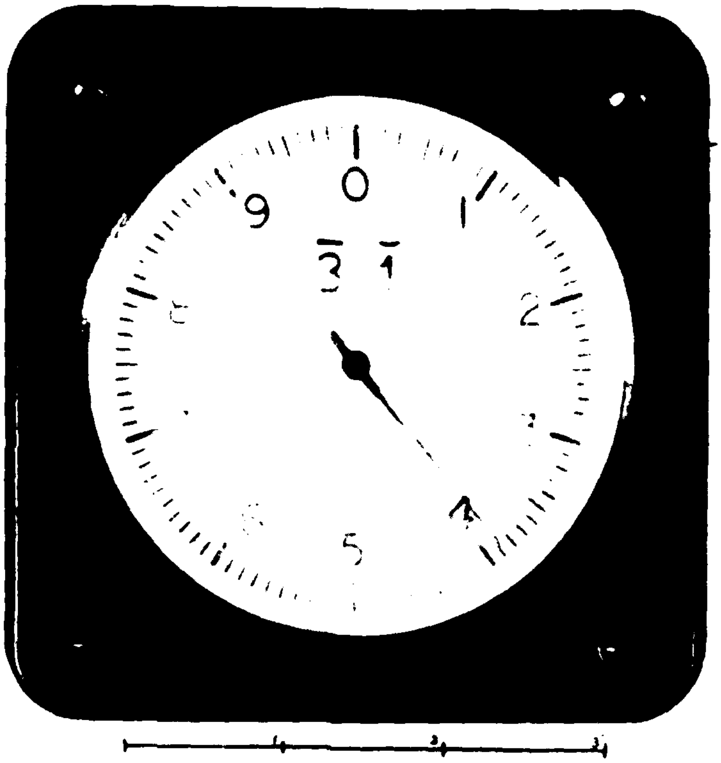


FIG. 2(b): INDICATOR

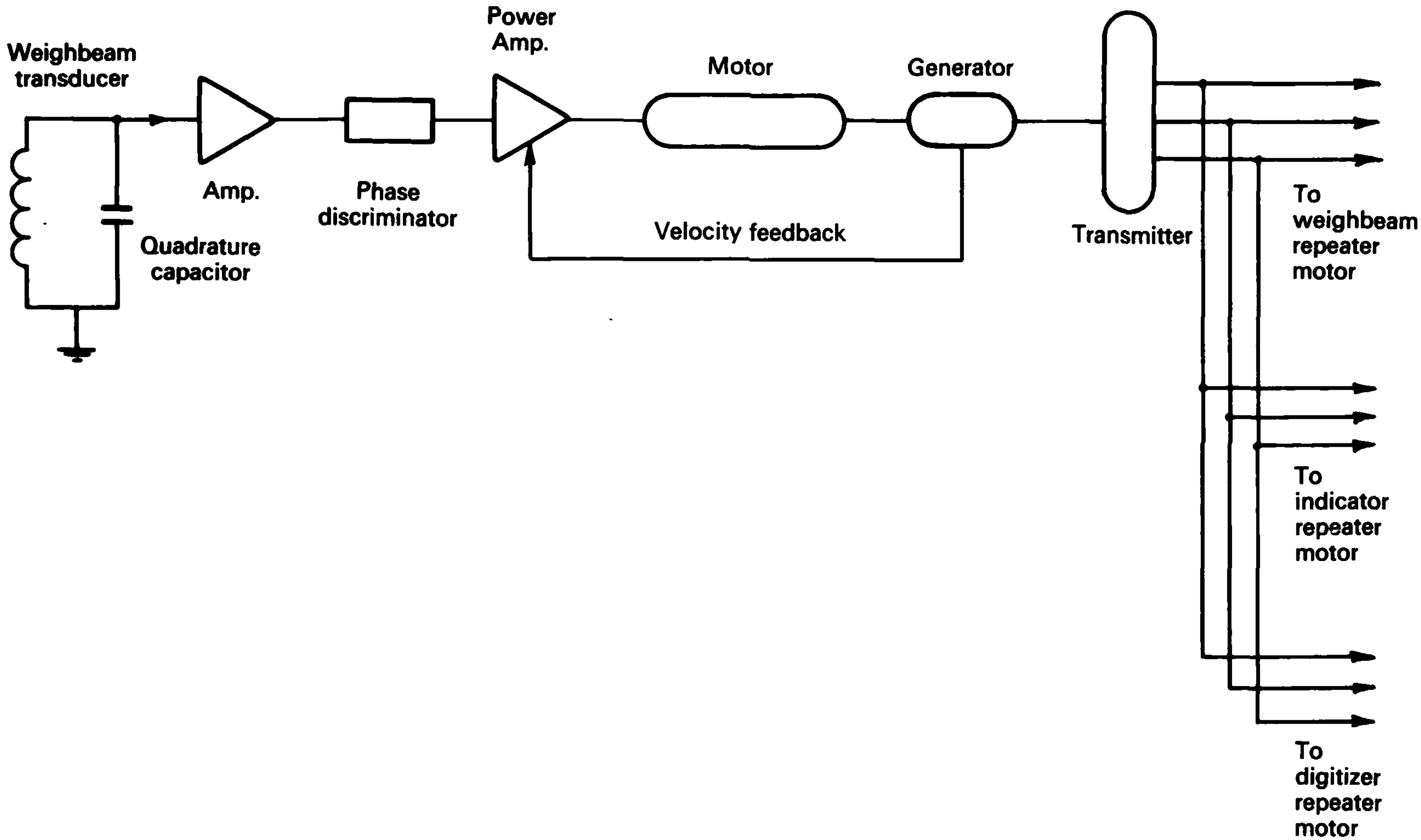


FIG. 3: SCHEMATIC DIAGRAM OF ORIGINAL ELECTRONICS

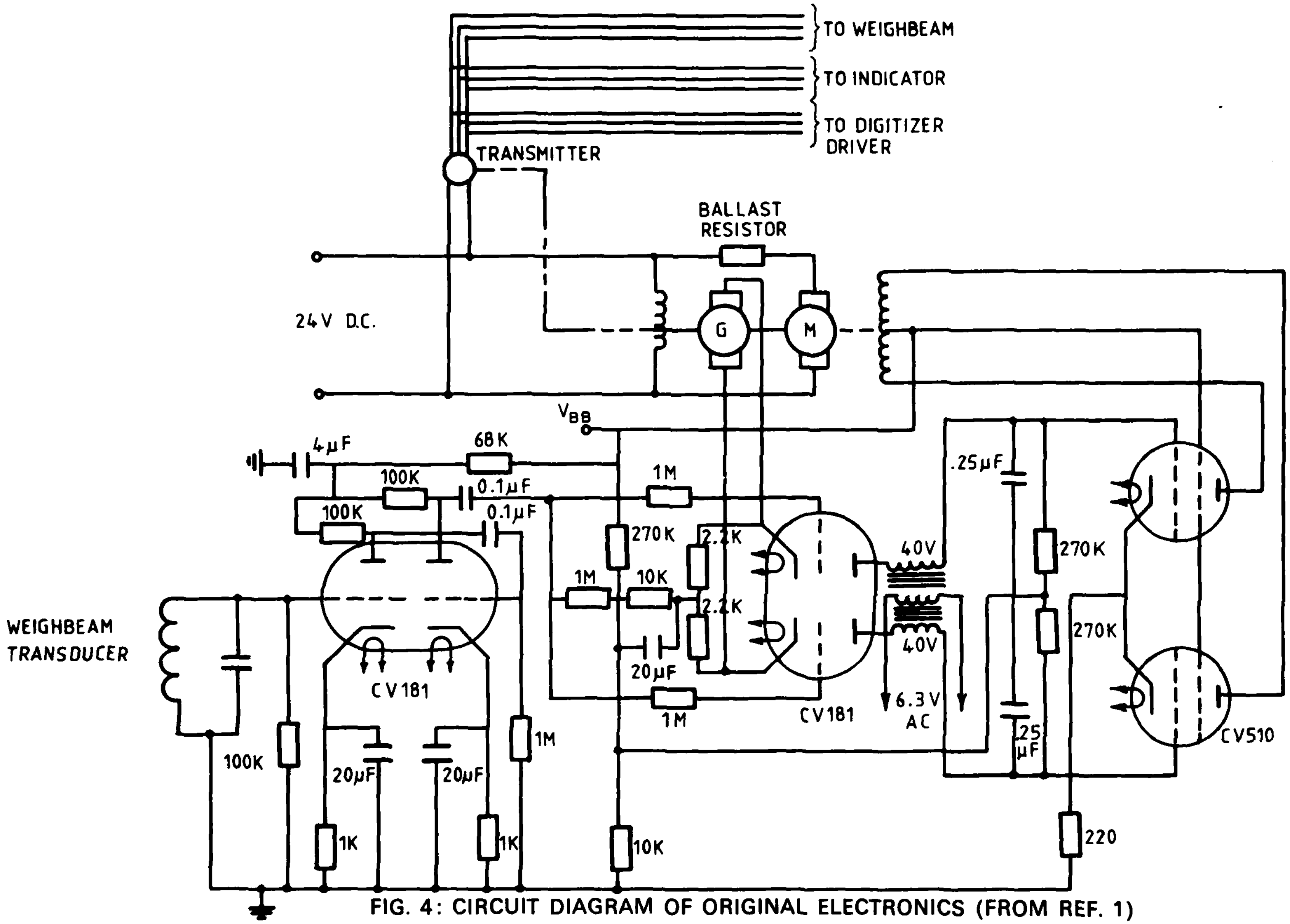


FIG. 4: CIRCUIT DIAGRAM OF ORIGINAL ELECTRONICS (FROM REF. 1)

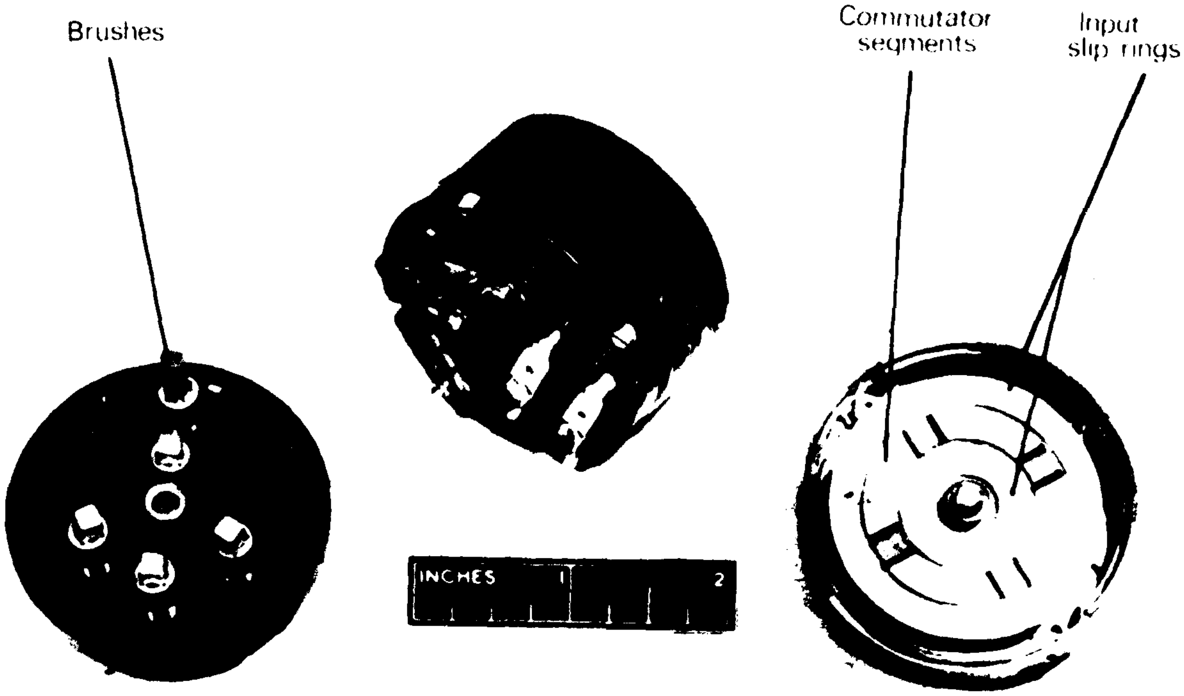


FIG. 5: COMMUTATOR TRANSMITTER (FROM REF. 1)

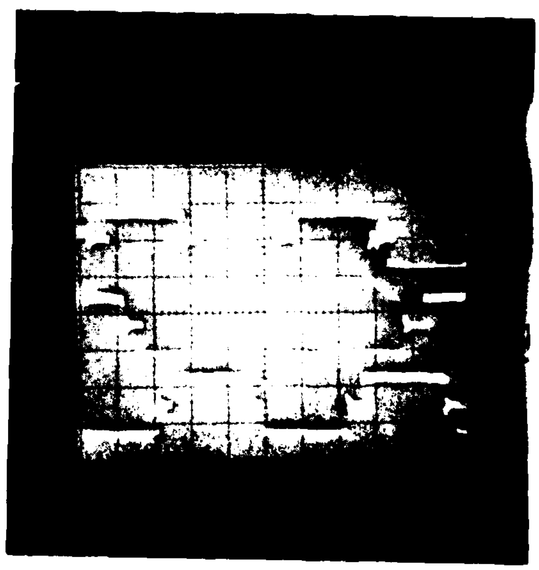


FIG. 6: ORIGINAL WAVEFORMS

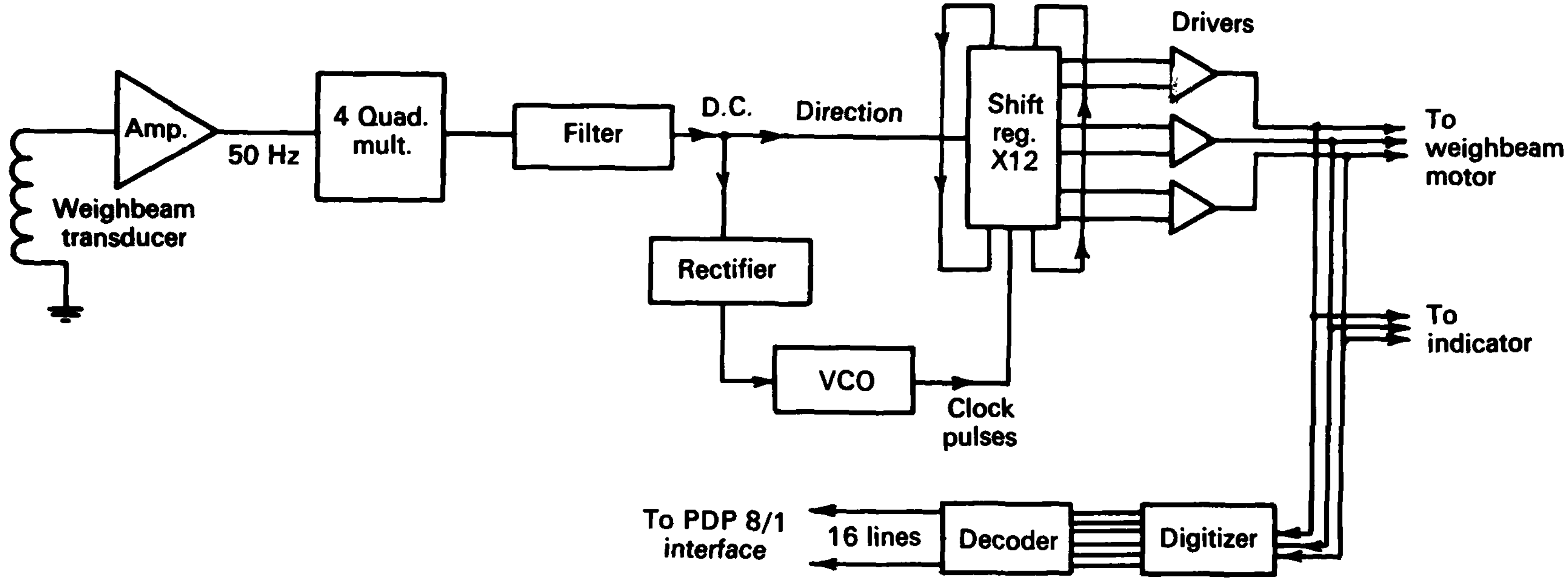
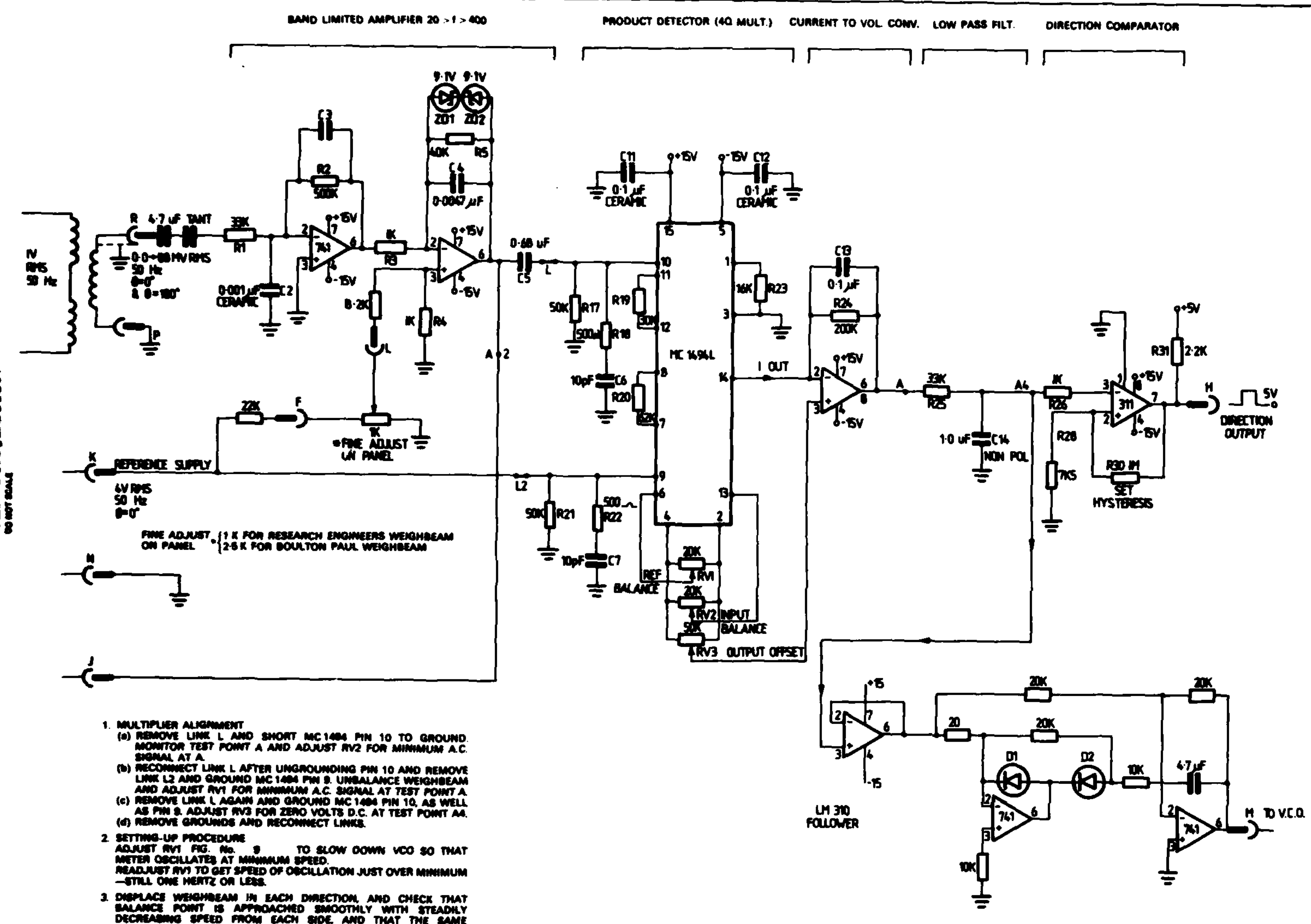
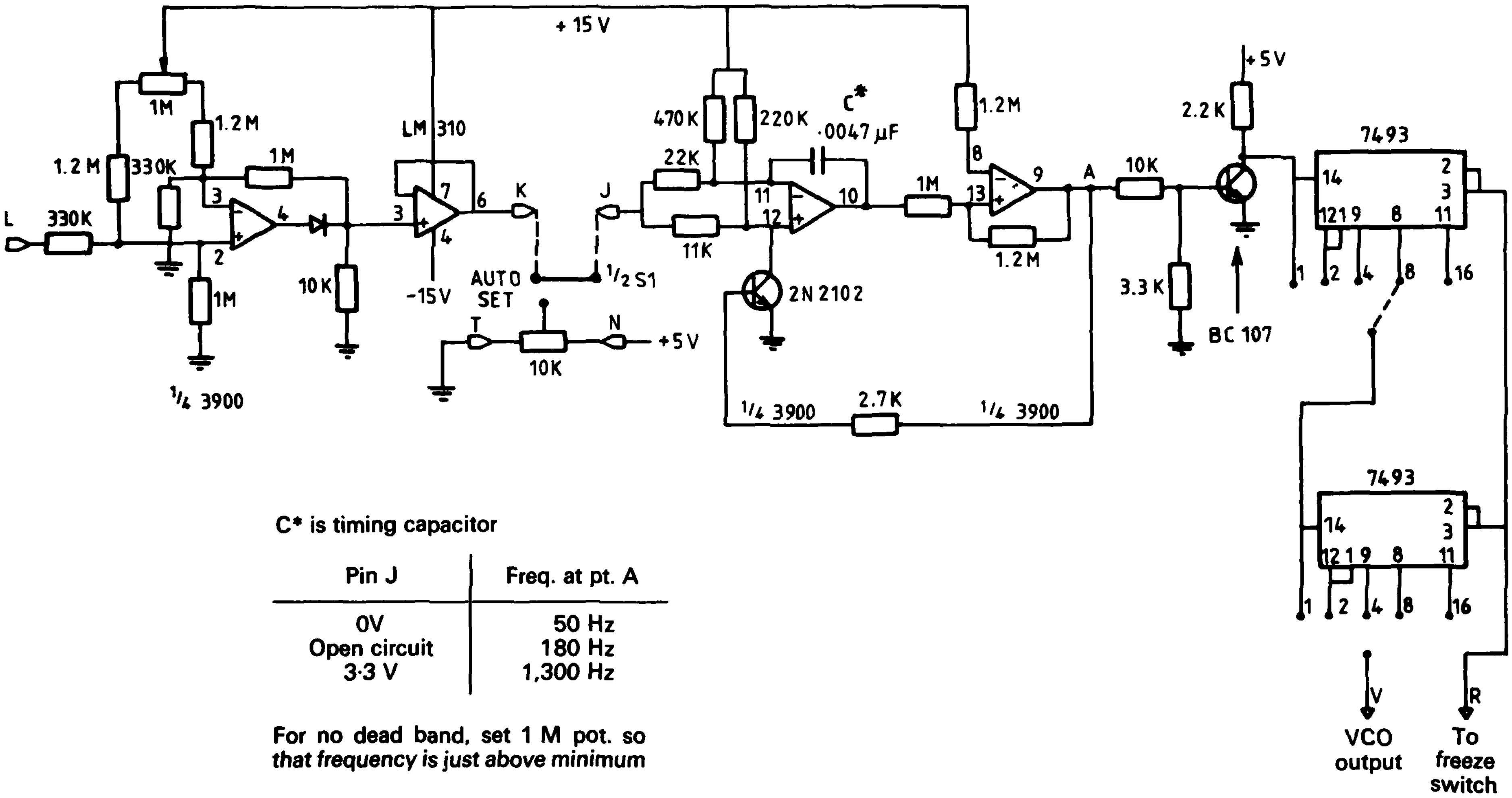


FIG. 7: SCHEMATIC DIAGRAM OF NEW ELECTRONICS



1. MULTIPLIER ALIGNMENT
   (a) REMOVE LINK L AND SHORT MC 1494 PIN 10 TO GROUND. MONITOR TEST POINT A AND ADJUST RV2 FOR MINIMUM A.C. SIGNAL AT A.
   (b) RECONNECT LINK L AFTER UNGROUNDING PIN 10 AND REMOVE LINK L2 AND GROUND MC 1494 PIN 9. UNBALANCE WEIGHBEAM AND ADJUST RV1 FOR MINIMUM A.C. SIGNAL AT TEST POINT A.
   (c) REMOVE LINK L AGAIN AND GROUND MC 1494 PIN 10, AS WELL AS PIN 9. ADJUST RV3 FOR ZERO VOLTS D.C. AT TEST POINT A4.
   (d) REMOVE GROUNDS AND RECONNECT LINKS.
2. SETTING-UP PROCEDURE
   ADJUST RV1 FIG. No. 9 TO SLOW DOWN VCO SO THAT METER OSCILLATES AT MINIMUM SPEED.
   READJUST RV1 TO GET SPEED OF OSCILLATION JUST OVER MINIMUM —STILL ONE HERTZ OR LESS.
3. DISPLACE WEIGHBEAM IN EACH DIRECTION, AND CHECK THAT BALANCE POINT IS APPROACHED SMOOTHLY WITH STEADILY DECREASING SPEED FROM EACH SIDE, AND THAT THE SAME BALANCE POINT IS REACHED. CHECK THAT INDICATOR DOES NOT SLOW AND THEN ACCELERATE TOWARDS THE BALANCE POINT. IF ASYMMETRICAL, RETURN TO STEP 1—MULTIPLIER ALIGNMENT.

FIG.8 AUTOMATIC MANOMETER REBUILD ANALOG SECTION



C* is timing capacitor

Pin J	Freq. at pt. A
0V	50 Hz
Open circuit	180 Hz
3·3 V	1,300 Hz

For no dead band, set 1 M pot. so *that frequency is just above minimum*

FIG. 9: VOLTAGE CONTROLLED OSCILLATOR

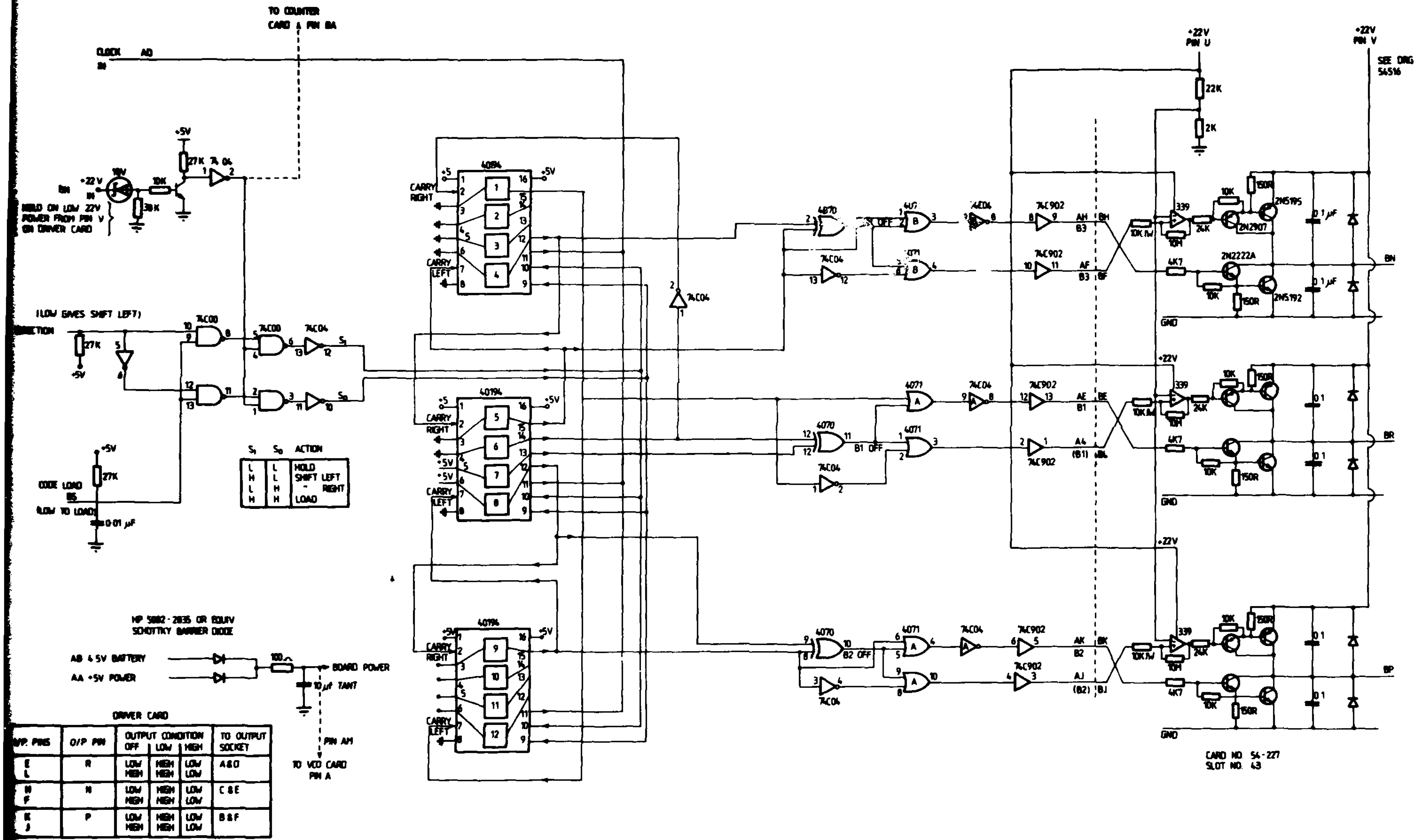


FIG. 10 AUTOMATIC MANOMETER REBUILD

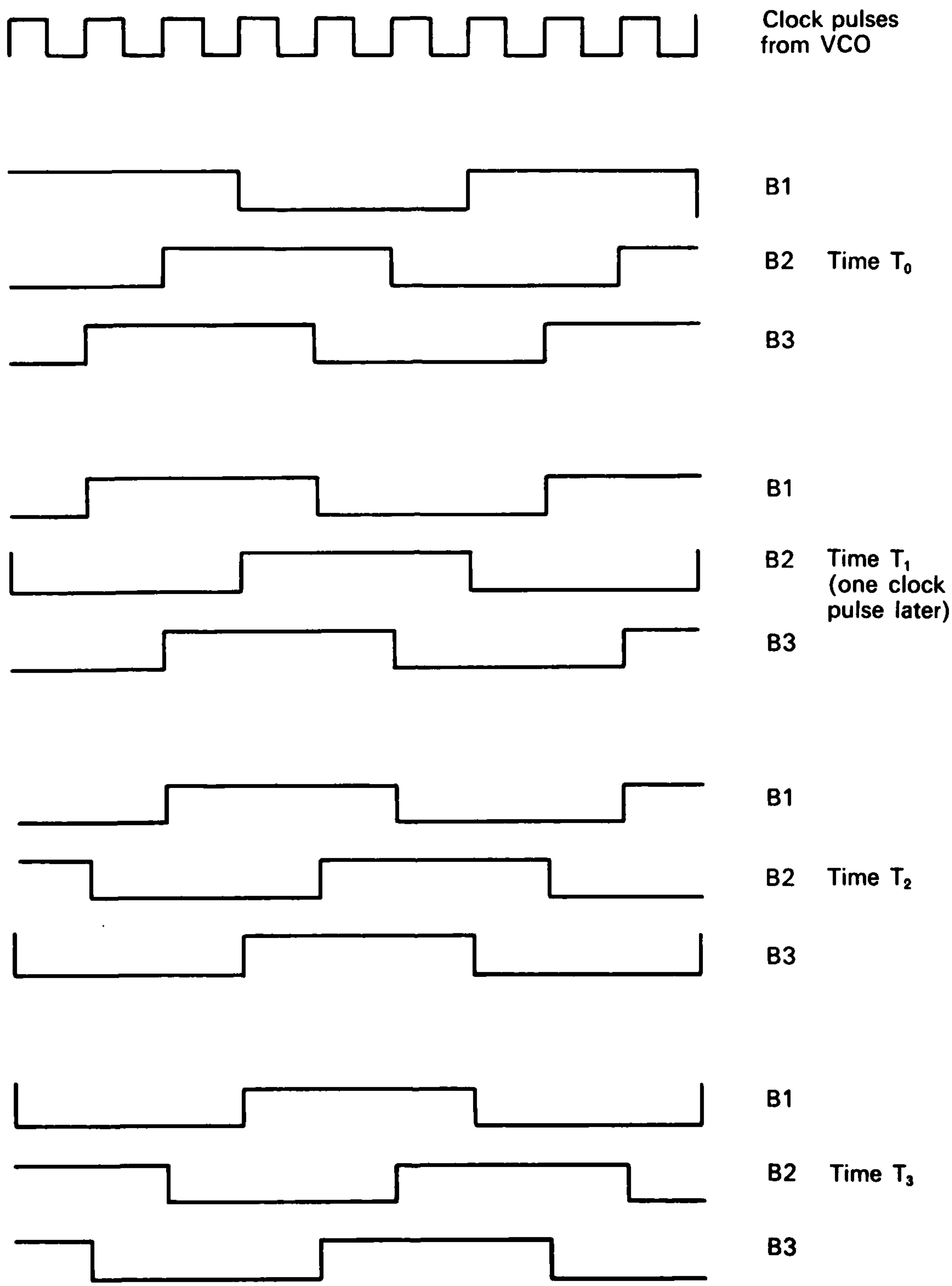


FIG. 11 : BASIC SHIFT RIGHT SEQUENCE (EXCLUDING OFF STATES)

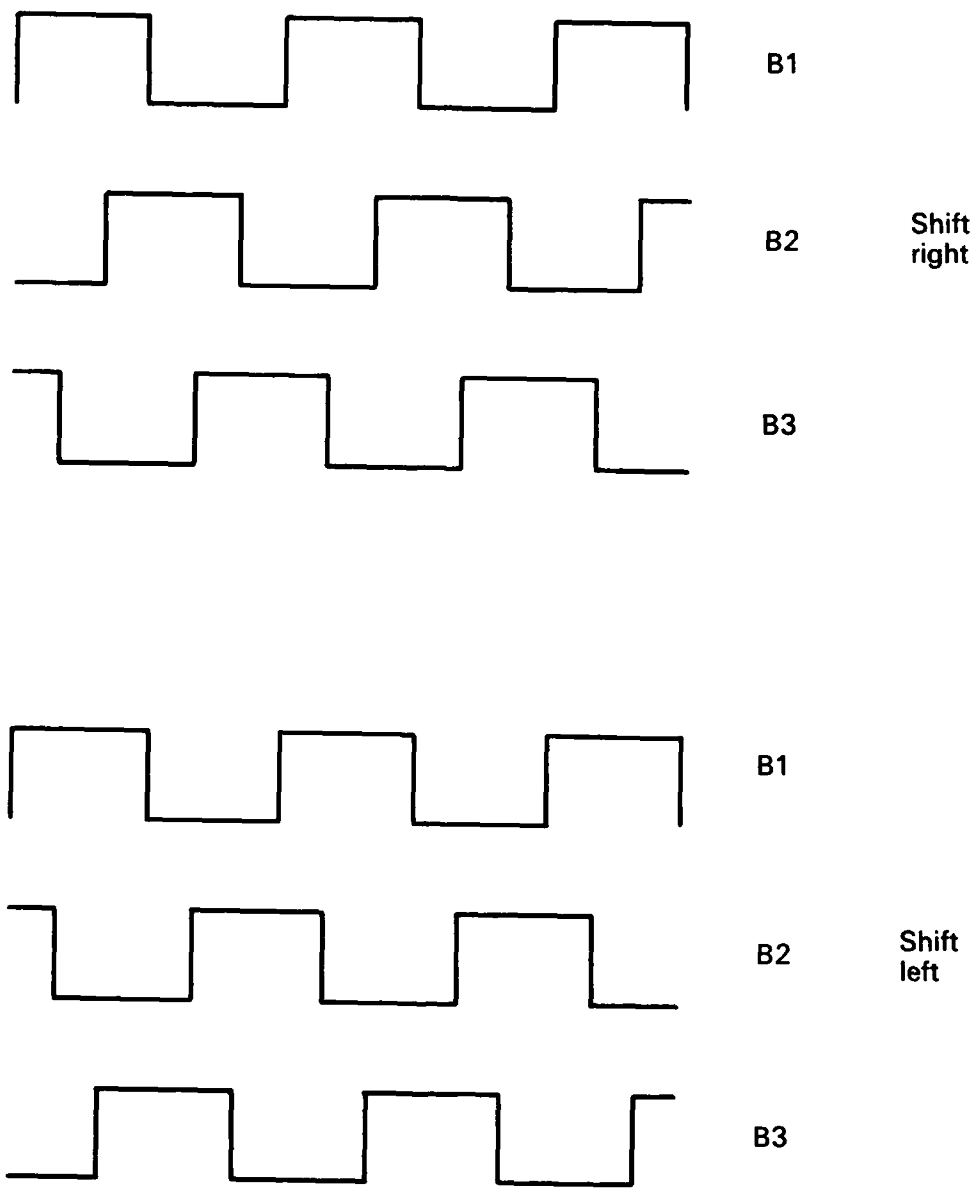
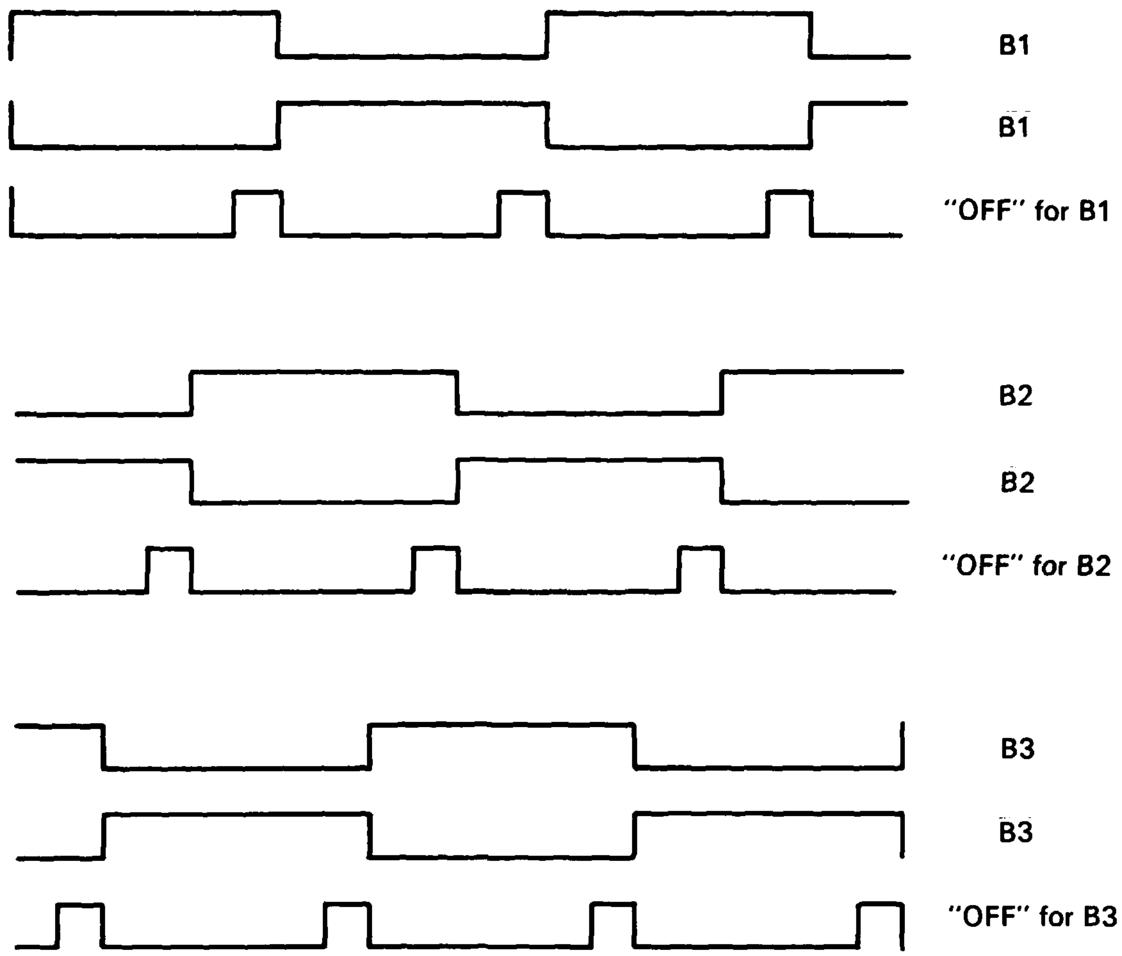


FIG. 12 BASIC SHIFT LEFT/ RIGHT SEQUENCE



B2 and B3 may be interchanged depending on direction

"OFF" pulses appear at beginning when running in opposite direction

FIG. 13: OFF PULSE TIMING

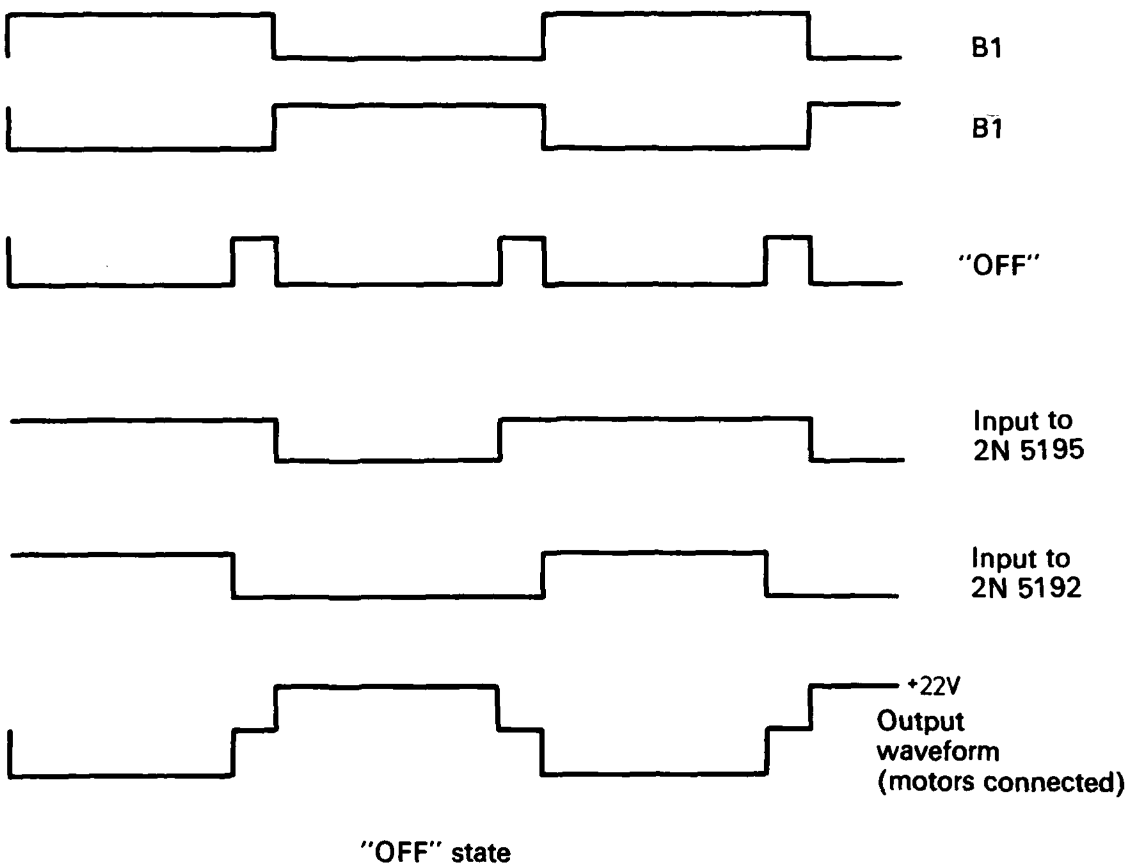
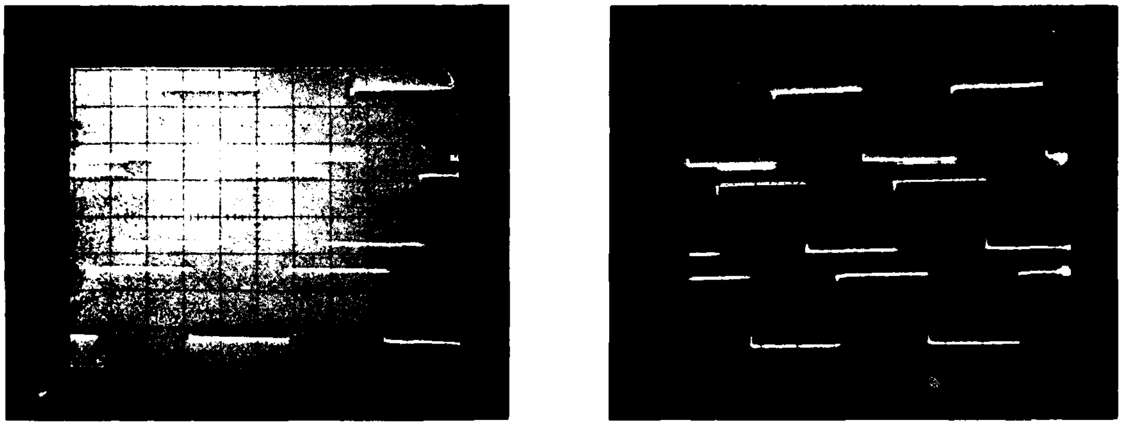
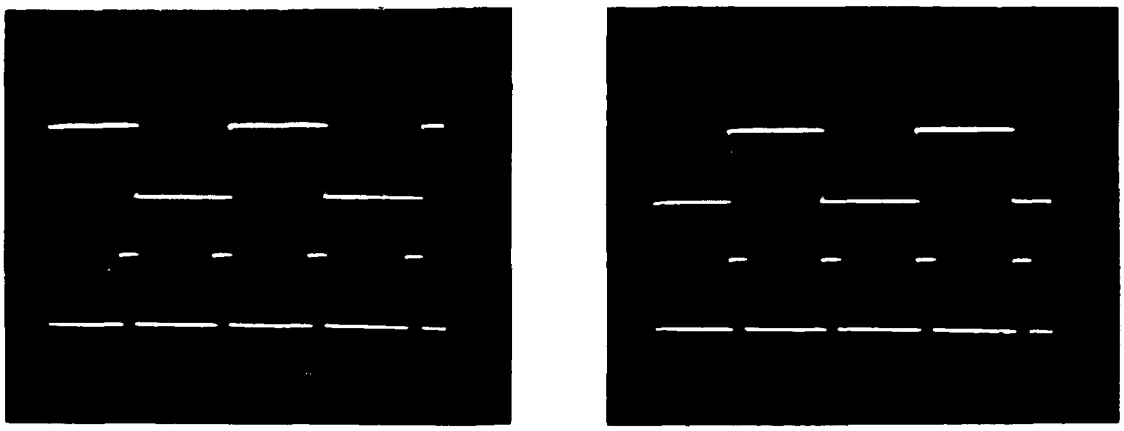


FIG. 14: POWER STAGE WAVEFORMS

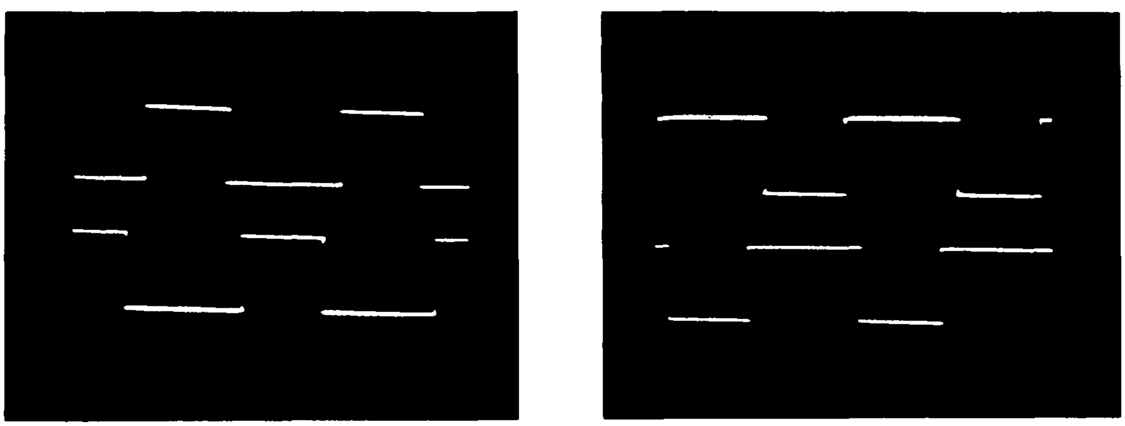
Clockwise rotation | Anticlockwise rotation



Basic waveforms for the three outputs from the 12-bit shift register



Timing of "OFF" pulses with respect to one of the three outputs



Waveforms at input to driver stage for one of the three outputs

FIG. 15: C.R.O. PHOTOGRAPHS OF ACTUAL WAVEFORMS

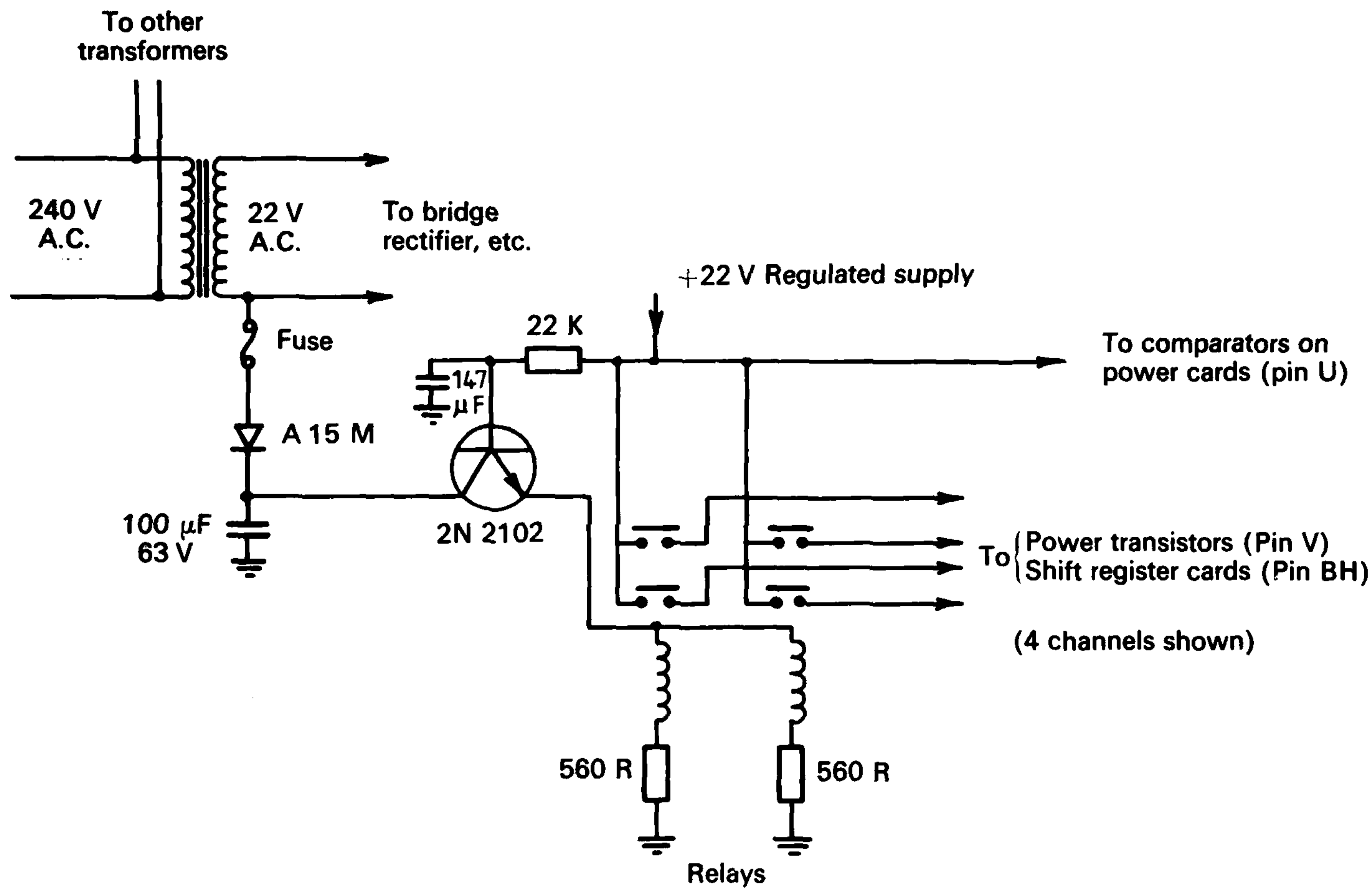
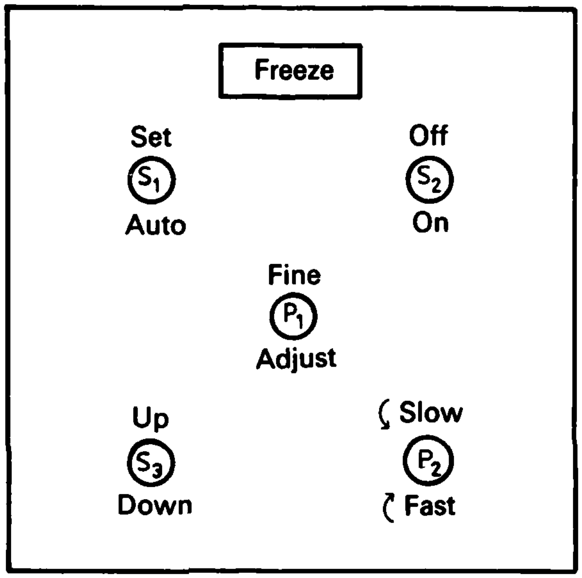
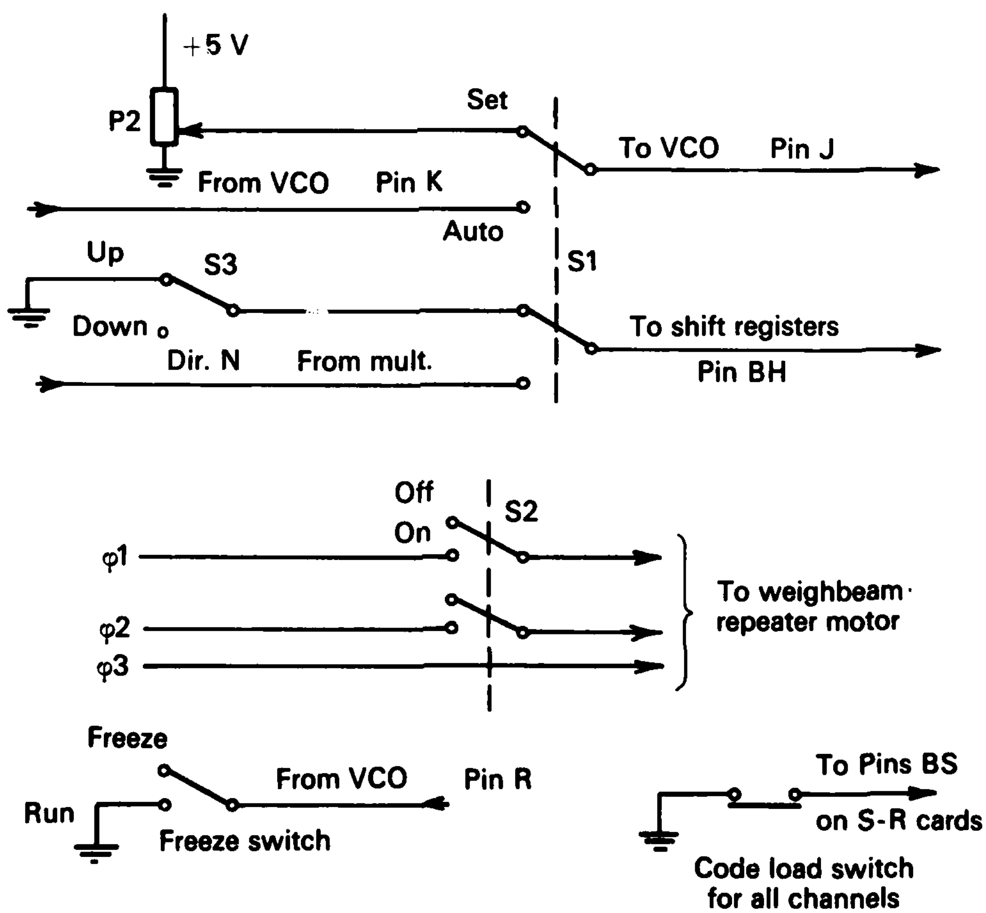


FIG. 16: FAST TURN-OFF, DELAYED TURN-ON POWER SUPPLY



Control panel for one channel



Fine adjust P1 see Fig. 8

FIG. 17: CONTROL PANEL AND SWITCHES

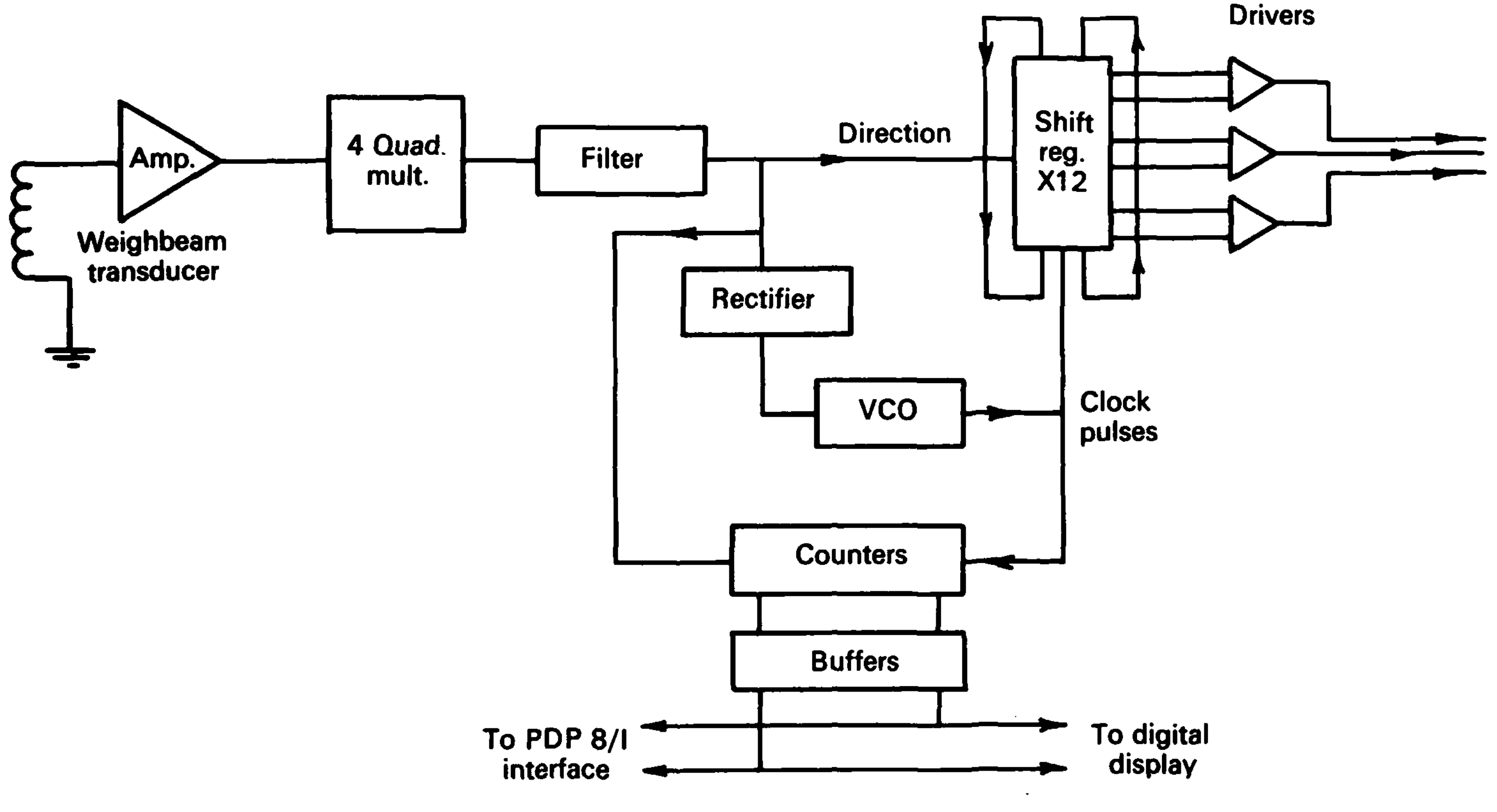


FIG. 18: SCHEMATIC DIAGRAM WITH DIGITAL DISPLAY AND NO DIGITIZER

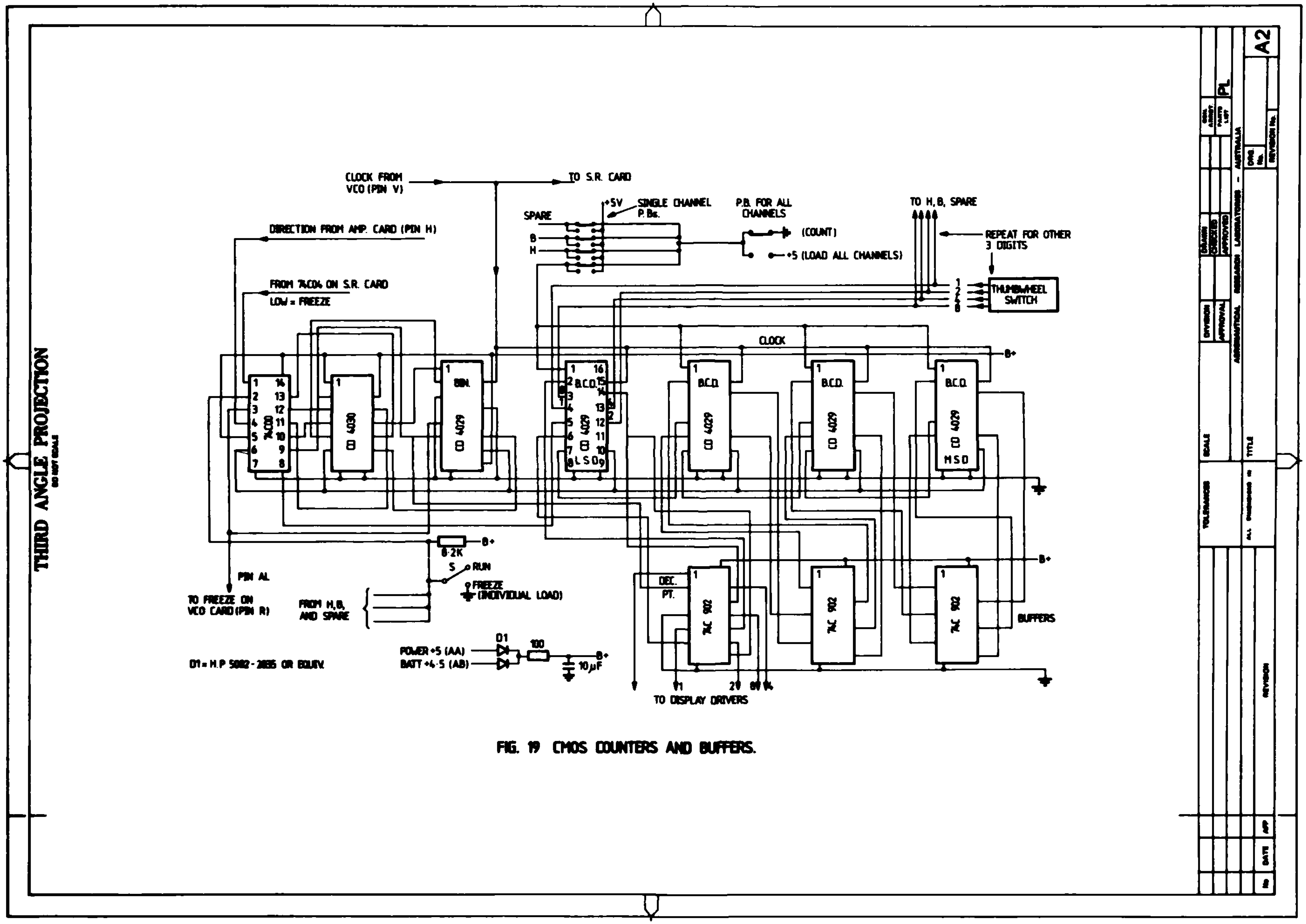
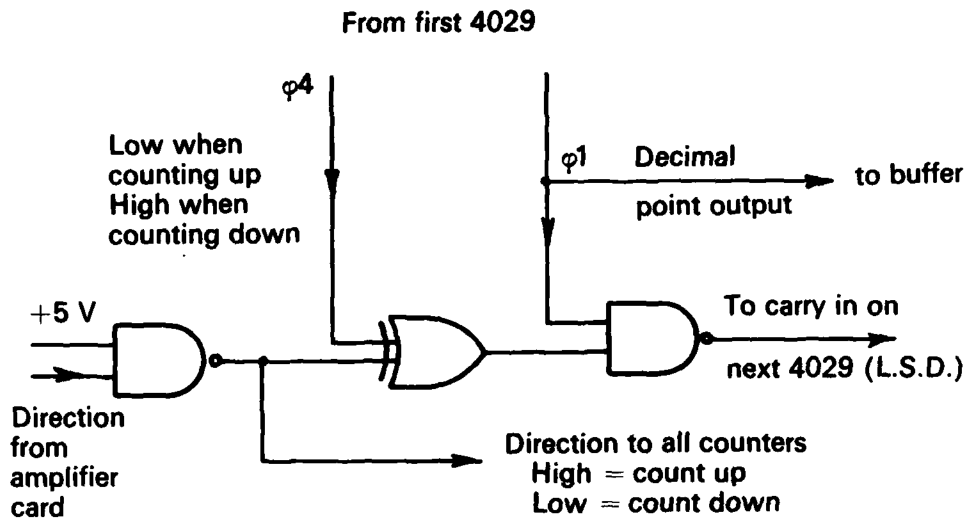


FIG. 19 CMOS COUNTERS AND BUFFERS.



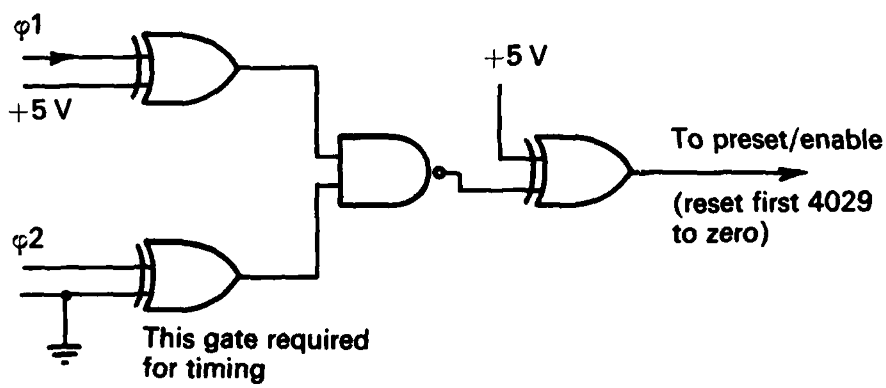


FIG. 20: DIVIDE BY TWO CIRCUITRY

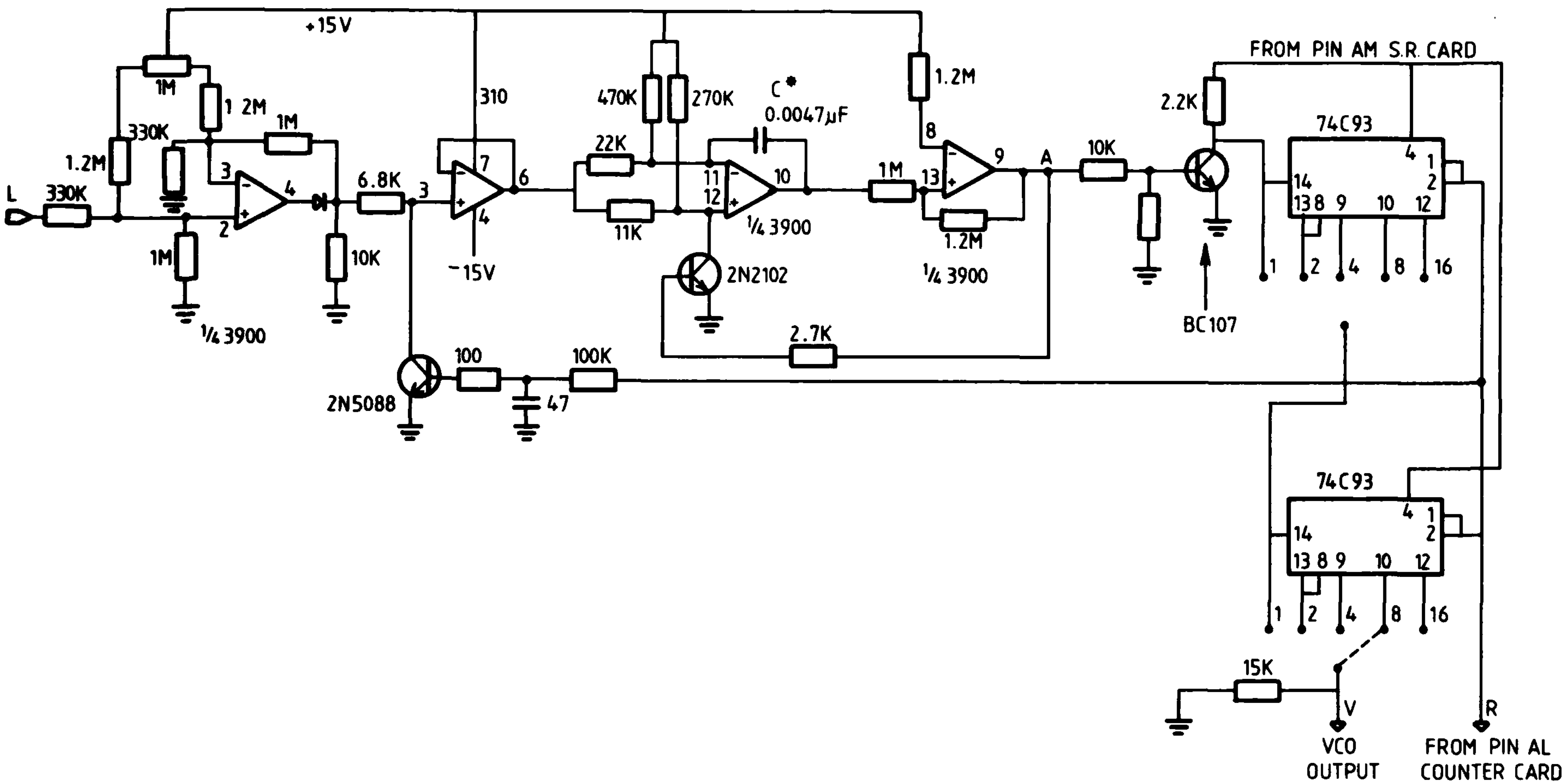


FIG. 21 MODIFIED VCO CIRCUIT

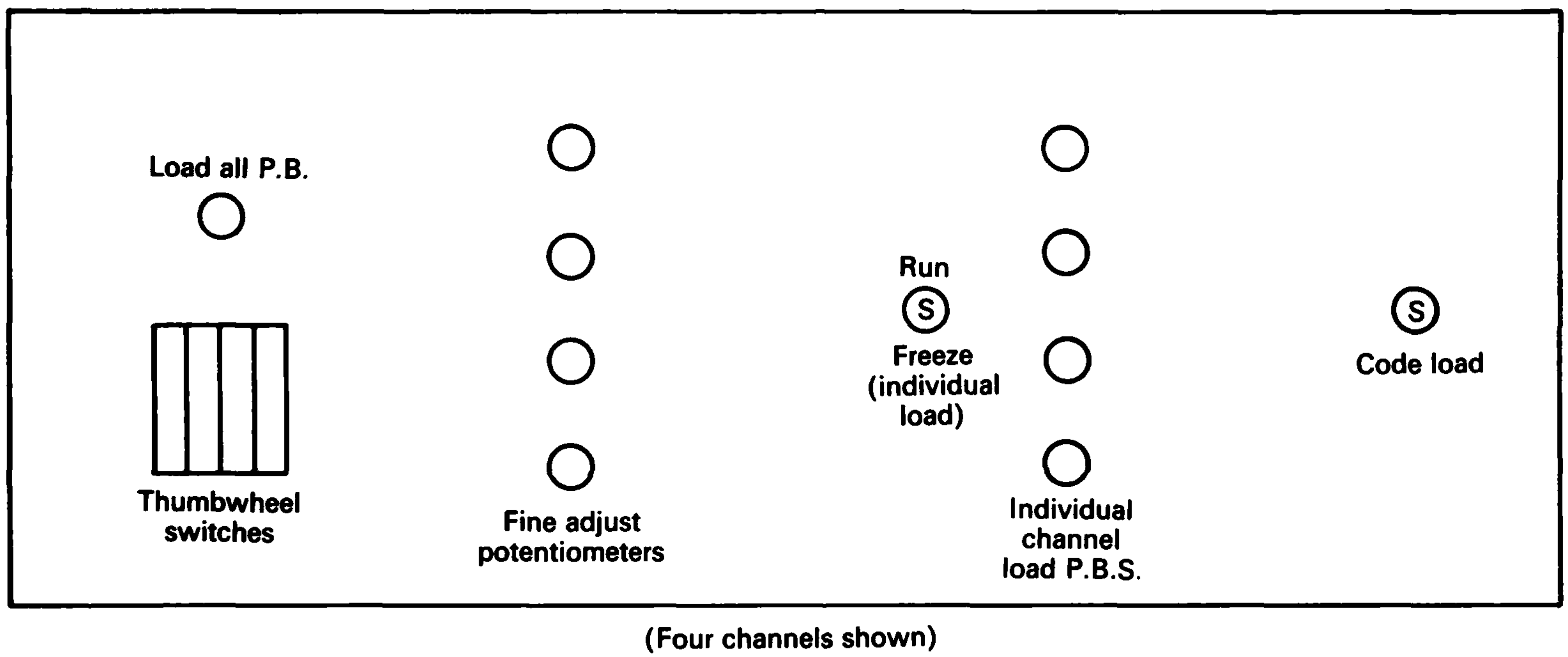


FIG. 22: CONTROL PANEL

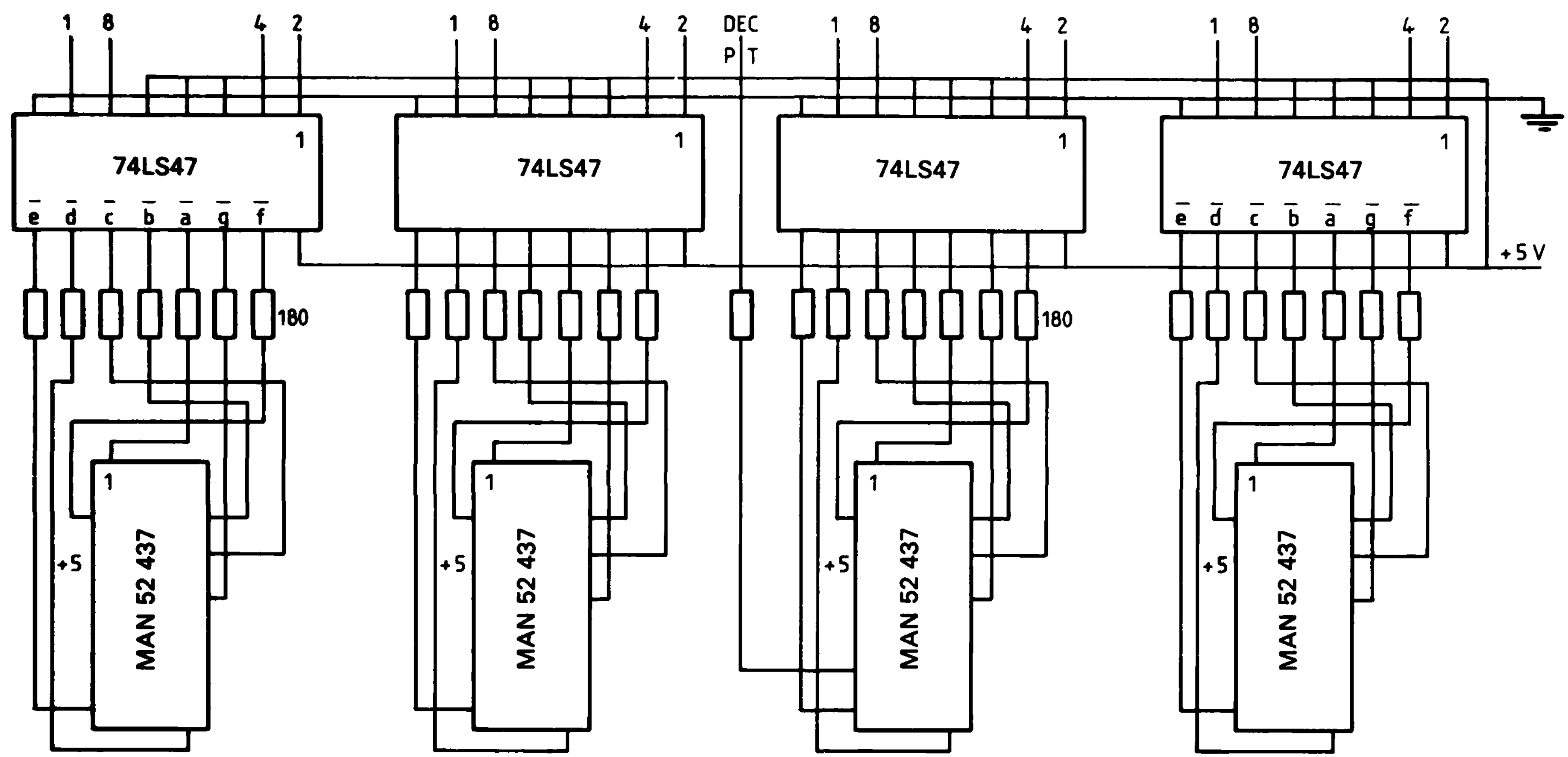


FIG. 23: DISPLAYS AND DRIVERS

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