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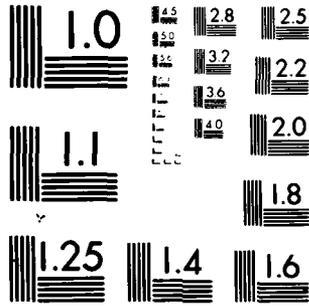
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With the information provided by previous ESCA studies that there is non-oxidized As in the oxide near the interface, detailed efforts have been undertaken to produce MOS structures without this deficiency. A two step insulator fabrication scheme was used to obtain improved capacitance-voltage characteristics. Other efforts concerned the deposition of different insulators on GaAs. The passivation of quaternary compound semiconductors was undertaken. Results on the experimental investigation regarding the mechanism of light emission from thin MOS structures are reported.			

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NEW PASSIVATION METHODS OF GaAs

FINAL TECHNICAL REPORT

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ABSTRACT

With the information from ESCA studies reported on native oxide MOS structures, efforts were undertaken to avoid the production of non-oxidized As atoms in the insulator, particularly near the interface. Therefore a two-step process of anodic oxidation was developed involving electrolytic oxidation of Al on a Ga-rich surface on GaAs. An attempt was made to formulate a simple electrical model of GaAs MOS diodes which fits reasonably well with experimental C-V and G-V characteristics (C-capacitance, G-conductance, V-voltage).

Results on d.c. emission of white light from thin GaAs MOS structures is reported. The spectral distribution of this emission seems to indicate that either a substantial contribution is obtained by the recombination of electrons and holes in the amorphous oxide (whose energy gap is larger than that of GaAs) or by direct recombination of hot charge carriers in the space charge layer.

Quarternary compound semiconductors are oxidized and analyzed. Efforts of anodic deposition of nitrides have not yet given any useful results. The deposition of SiO_2 by using emulsions is pursued and first results on the possibility of GaAs doping are presented.

CHAPTER I

INTRODUCTION

The period covered by this final report was again full of important developments. A great deal of effort of course had to be spent first in order to make the experimental facilities here in Darmstadt as good as those which the principal investigator was using with his collaborators previously in Newcastle upon Tyne, England. He is pleased to say that this first goal was achieved relatively quickly, particularly with the help of his new colleagues, Prof. A. Kessler, Dr. Mayer and his German secretary, Mrs. Tümmler. Equally important also was the contribution made by those of his coworkers who came with him from England, namely Dr. D. Pavlidis and Dr. S. Hannah. Several new appointments were made in Darmstadt: K. Röhkel, W. Schmolla and E. Huber. The provision of a research grant by the German Science foundation (Deutsche Forschungsgemeinschaft, together with the funds available from ERO, enabled us to invite Dr. Adachi from Tohoku University Sendai, Japan, to work for a year with this group on surface passivation for compound semiconductors.

With the realisation that many of the interface problems resulted from both non-oxidized arsenic atoms in the insulator near the interface and As vacancies in the semiconductor, both created due to the oxidation dynamics of native oxides, new possibilities were initiated and useful new results obtained. The research group

was therefore not only able to publish several new interesting results in the scientific literature, but some of us were involved with developments at other laboratories and with discussion meetings on surface passivation of compound semiconductor materials. Especially important to mention here is a period of work by H.L. Hartnagel at the Avionics Laboratories at Wright Patterson AFB, Dayton, Ohio, where he joined a strong group on GaAs surface passivation for MESFET structures. Results obtained both in Dayton and here in Darmstadt were then presented at the 7th Annual Conference on the Physics of Compound Semiconductor Interfaces in Estes Park, Colorado, January 29th to 31st 1980. Similarly Mr. K. Röhkel spent some periods at various British research laboratories where the questions of surface passivation were also systematically discussed. Further details on publications, conference meetings, etc. can be taken from attached copies of some of the papers and from the references in the Appendix of this report.

It should be mentioned here particularly that various joint projects were undertaken with the German Post-Office Laboratories here in Darmstadt. The closeness of this laboratory with the central research facility of the German Post-Office is understandably very beneficial for work of this type. Of course there are many other facilities both at the Technical University and in the neighbourhood of Darmstadt which were made use of in the course of the studies reported here.

Some of the investigations reported here were undertaken by student projects, some of which have not yet been completed. These efforts are also described in the following Chapters, which are organized by the particular investigator of surface passivation, whose name is in these cases also given.

CHAPTER 2

Characterisation and Performance of GaAs MOSFETS

(D. Pavlidis)

Low frequency and microwave tests were undertaken in order to characterise GaAs MOSFETs fabricated by us with anodically grown oxide gates. The devices were made on n-type, S doped VPE layers having a thickness between 0.7 and 1.5 μm , mobilities around $4400 \text{ cm}^{-2} \text{ V}^{-1} \text{ sec}^{-1}$ and carrier concentrations of the order of 10^{17} cm^{-3} . The epitaxial layers were grown on Cr-doped semi-insulating substrates with a resistivity larger than $10^7 \Omega\text{cm}$.

A glycol-tartaric acid based aqueous solution was used in order to anodically oxidise the gate notch after the source and drain ohmic contacts were formed. The device had 5 μm to 10 μm long, 300 μm wide gate strips. The gate to source (or drain) length was 10 μm and the channel depth underneath the oxide layer was of the order of 1000 \AA .

By measuring the drain resistance at the origin of the $I_d \rightarrow V_{ds}$ curve, displayed on a Tektronix curve tracer, it was found that $R_s = R_d = 40 \Omega$. The gate parasitic resistance R_g is a function of the gate geometry and metallisation technique employed and had in our case the value of 3 Ω .

The MOSFET transconductance g_{mo} was measured from the $I_d \rightarrow V_{ds}$ characteristic to be equal to 7.2 mmho's. The measurements demonstrated a reasonably high transconductance per unit gate length values in the range of 36 mmho's/mm. Finally, from the drain to source external conductance and the already evaluated R_s and g_{mo} values, it was found that the intrinsic output conductance G_{ds} is equal to 2.8 mmho's.

The equivalent circuit of Fig. 1 was used for modelling the tested devices. Some of its parameters, namely R_s , R_d , R_g , G_{ds} and g_{mo} were evaluated by low frequency measurements as described above. Others, however, such as C_{gs} , C_{dg} , R_{gs} and g_m^* were estimated by microwave measurements. A special microwave test fixture with 50 Ω microstrip lines on alumina substrates was fabricated and the transistors were mounted on an adjustable ground slab. Gold pressure contacts were used on the devices, which were all tested in the common source configuration. The driving point parameters S_{11} , S_{22} and the transfer terms S_{12} , S_{21} were measured with an HP 8410 A Network Analyser. A typical set of the measured S-parameters is given in Fig. 2. The elements C_{gs} , C_{dg} , R_{gs} were evaluated from the S-parameter data and are given in Table 1 together with other characteristics of the transistors.

- *) g_m - frequency-dependent transconductance of equivalent circuit
- g_{mo} - "low frequency" transconductance of MOSFET amplifier

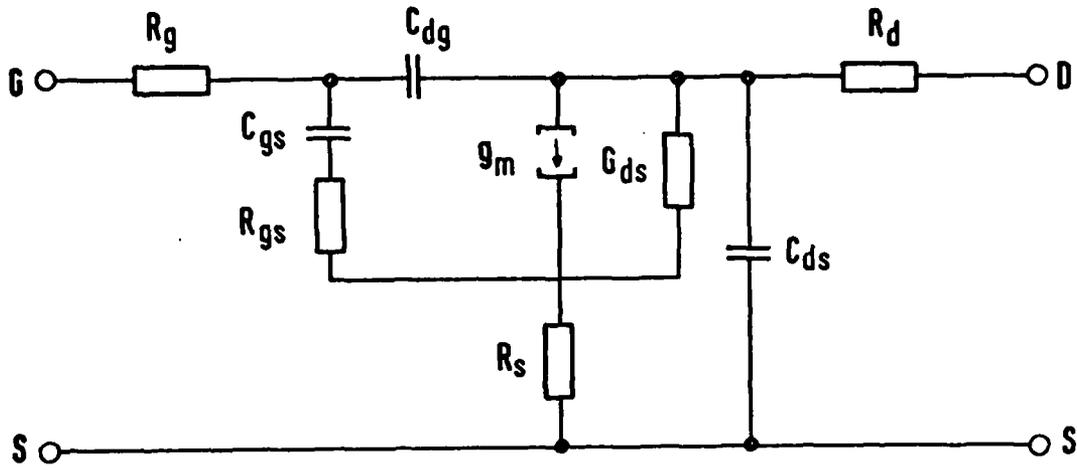


Fig. 1 MOSFET small-signal equivalent circuit

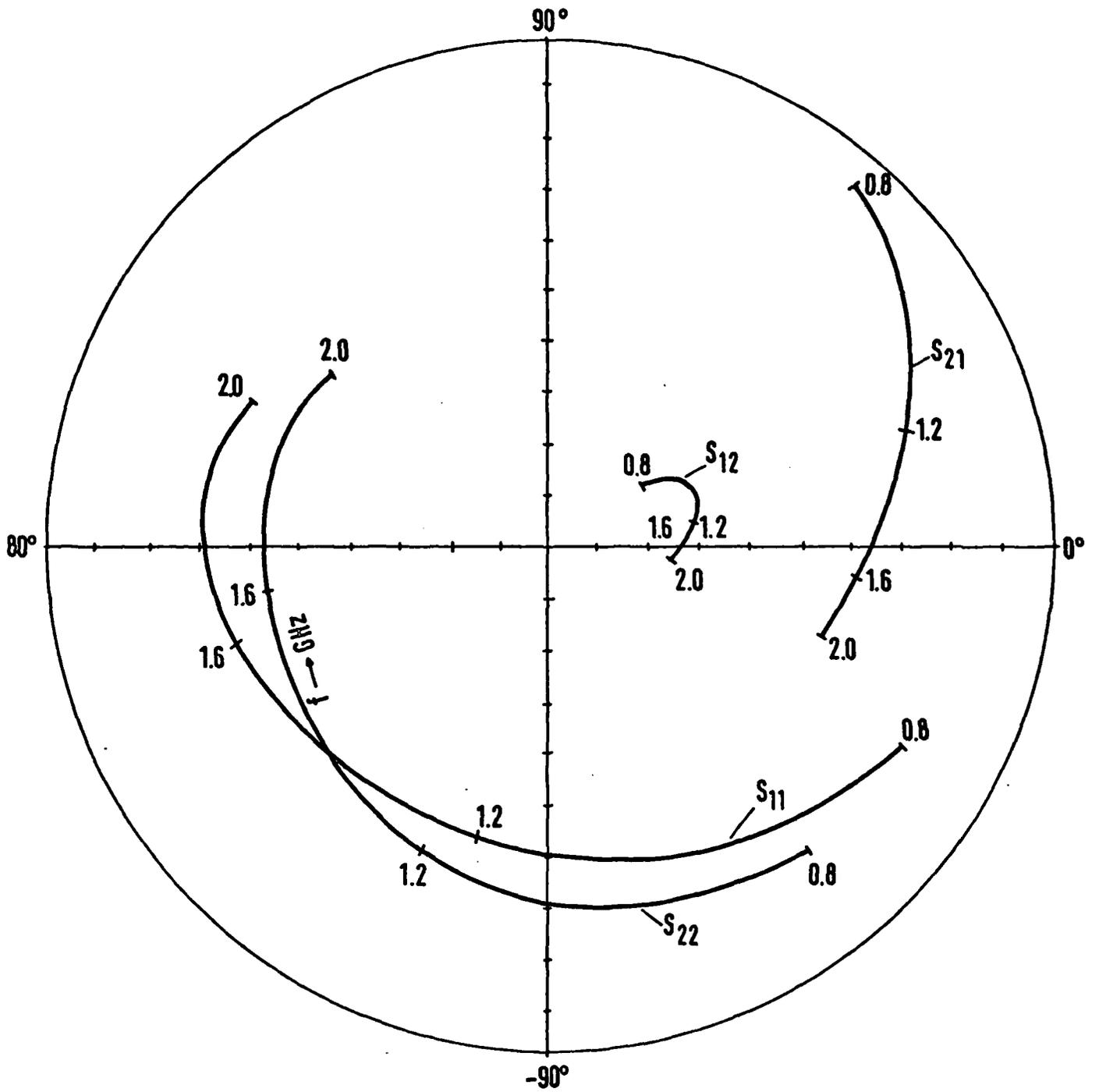


Fig. 2 Small-signal s-parameters of a MOSFET

Geometry

Gate length: $l = 5 - 10 \mu\text{m}$

Gate width : $w = 200 - 300 \mu\text{m}$

Gate to source/drain length: $l_s = l_d = 10 \mu\text{m}$

Channel depth (under gate notch): $= 1000 \text{ \AA}$

n - epi layer $= 0.8 - 1.0 \mu\text{m}$

Material parameters

Carrier density: $n = 1.0 \times 10^{17} \text{ cm}^{-3}$

Mobility: $\mu = 4400 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$

Substrate: Semi-insulating (S.I), Cr-doped
 $\rho > 10^7 \Omega\text{cm}$

Equivalent circuit parameters

Transconductance: $g_{mo} = 3.5 \text{ mmho}$

Output conductance: $G_{ds} = 2.8 \text{ mmho}$

Gate resistance: $R_{gs} = 2.0 \Omega$

Source/Drain resistance: $R_s = R_d = 40 \Omega$

Gate metal resistance: $R_g = 3 \Omega$

Gate to channel capacitance: $C_{dg} = 0.15 \text{ pF}$

$C_{gs} = 2.07 \text{ pF}$

Table 1 Typical parameters of an n-channel GaAs MOSFET

A maximum available gain (MAG) of 14 db was measured at 2 GHz, the maximum oscillation frequency being of the order of 4.8 GHz. The transconductance g_m was of the order of 11 mmho and remained relatively constant for operational frequencies as low as 800 Hz. Below this frequency the transconductance is seen to fall rapidly and is probably due to interactions with traps at the oxide-GaAs interface.

CHAPTER 3

Plasma Anodisation of GaAs

(D. Pavlidis)

GaAs was anodically oxidised in a high frequency (1 MHz) plasma produced by a 3 kW generator. A schematic diagram of the system used is given in Fig. 3. The vacuum chamber was made of fused quartz to withstand plasma temperatures. The chamber was first evacuated to a pressure of 10^{-6} Torr, and then filled with oxygen gas to a background pressure of 0.2 Torr. The GaAs samples were dc. biased at + 20 to + 40 Volts during the process. Finally the RF generator was inductively coupled to the chamber in the region of the cathode electrode.

The oxidation was done in the constant voltage mode with a series resistor of 100 Ω inserted in the circuit. It was found that for + 40 V bias, 0.2 Torr pressure and 17 cm electrode separation, the initial current through a 0.25 cm² sample is as high as 24 mA. This results in oxide breakdown 5 secs after the plasma generation, demonstrated by temporary (~ 2 secs) current increase through the sample. Further work on the optimisation of the plasma oxidation process is now being performed.

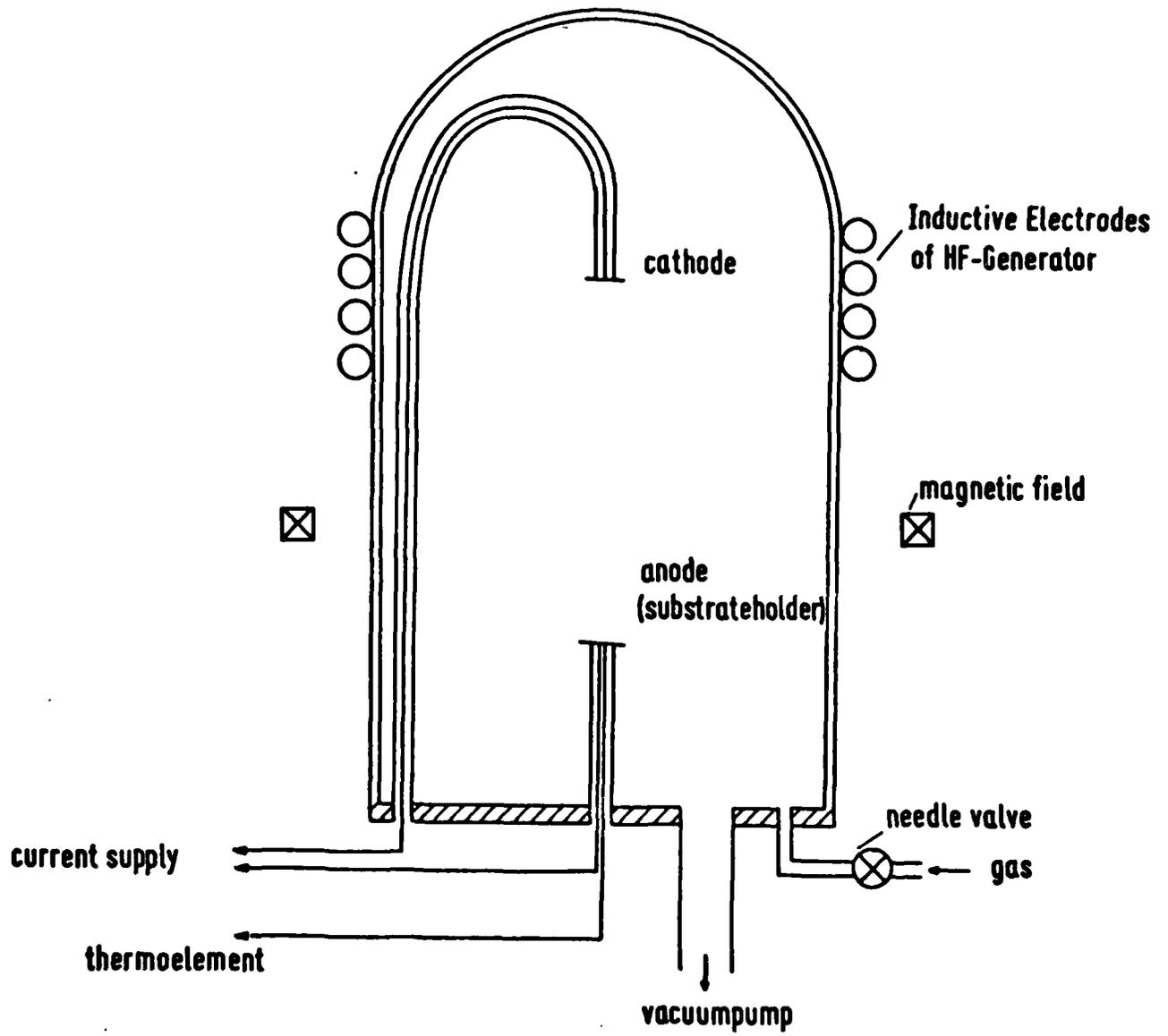


Fig. 3 Gas-Plasma Reactor for anodic oxidation

CHAPTER 4

Experimental Study of Thin-Oxide MOS Structures

(H. Adachi)

4.1 Light Emission from GaAs MIS Diodes

It was reported that the GaAs MIS diode with a very thin anodic oxide layer emits light under reverse voltage biasing condition^[1]. The diode shows good I-V characteristics like a Schottky barrier diode, although there is a very thin layer of anodic oxide. S. Ashok et al^[2] reported that a GaAs Schottky diode with very a thin anodic-plasma oxide layer also shows good I-V characteristics almost like an ideal Schottky diode, and its ideality factor (n-value) can still be as low as about 1.09 even if the oxide layer is 85 Å thick; but their MIS Schottky barrier diode does not emit any light. Our work was undertaken to look for the most suitable insulating layer for light emission and to find a physical explanation for it. It is not yet possible to give a conclusive statement on the emission mechanism but we report some interesting observations and suggest a first explanation of the experimental results obtained so far.

4.2 Effect of the chemical etching process

MIS Schottky barrier diodes were made on (100) oriented n-type GaAs wafers. The supplier information on the impurity concentration is $1.7 \times 10^{17} \text{ cm}^{-3}$. One surface of the wafer is mirror plane and the other surface is ground. The wafers are solvent cleaned and chemically etched just before the evaporation of an Au-Ge (12 %) ohmic contact and the mirror surface is covered with photo-resist during these evaporation processes to avoid making any scratches. The ohmic contact is heat treated in a N_2 gas flow at 350°C for 5 min. Samples are made with different fabrication details, as summarized in Table 2.

The sample (005) is carefully made, following the process reported by B. Bayraktaroglu^{1,3}. A thin anodic oxide layer is made by using the AGW* solution, and the resultant sample emits light. However, sample (006) also emits light; it was made at the same time with the same fabrication process as sample (005), except for the anodization process. Since the fabrication of sample (006) does not include any anodic-oxidation, it can be seen that an anodic oxide film is not essential for the emission of light, but that the normally present native oxide suffices whose thickness and other properties depend on the chemical and atmospheric treatment of the free GaAs surface.

*Acid-Glycol-Water

3 % aqueous solution of tataric acid : glycol
ratio: 1 : 2

The etching solution of the samples (005 and 006) is the so-called pre-evaporation etchant (mixture of 4 % H_2O_2 by volume and 2 % NaOH by weight), which includes a base. After etching the surface of a GaAs crystal with concentrated NH_4OH (25 %) and vacuum evaporating an Al electrode without any anodization of the surface, the resulting sample (009) emits also light. If the surface of the crystal is etched by using diluted HCl (25 % HCl is diluted with 5 portions of water) just before the evaporation of the Al electrodes, the resulting samples (007, 008, 018 and 020) do not emit light. These observations suggest that the etching solution, including the base added, makes important contributions to the light emitting phenomenon.

It can be concluded that etching with diluted HCl prevents light emission and etching with a solution, including alkali, improves it.

4.3 Reverse I-V characteristics

The reverse I-V characteristics are measured at room temperature and the results are shown in Figure 4 for several typical samples. All the non-light emitting diodes have a lower breakdown voltage and the fabrication process of every non-light emitting diode includes an etching process with diluted HCl.

The temperature dependence of the reverse I-V characteristics measured at 85° C is shown, together with the results obtained at room temperature, in Figure 5 for light emitting diodes and in Figure 6 for non-light emitting diodes. The temperature coefficients of the breakdown voltages are positive, independent of the breakdown voltage. The current for a biasing voltage below breakdown is increasing with increasing temperature for both cases. These facts are a characteristic feature of avalanche breakdown.

A possible explanation of the low breakdown voltage of the non-light emitting diodes is based on some fixed negative charges at the interface between semiconductor and oxide, namely in the transition layer. The band diagram of the Schottky diode without any interfacial charges is like that shown in Figure 7(a). The electric field in the transition layer is equal to that at the surface of the semiconductor. If there are some fixed negative charges at the interface, the potential at the interface is lifted up, and the band diagram is changed as shown in Figure 7(b). That is, the electric field strength in the transition layer is decreased and the electric field strength at the surface of the semiconductor is increased. Due to this increased field strength, the avalanche breakdown voltage is reduced. A low breakdown voltage is the common characteristic of the samples whose fabrication process includes the etching process with diluted HCl and does not include any anodization, so that it is most probable that the negative charge comes from the acidic etching solution, for example from etching Ga ions by HCl.

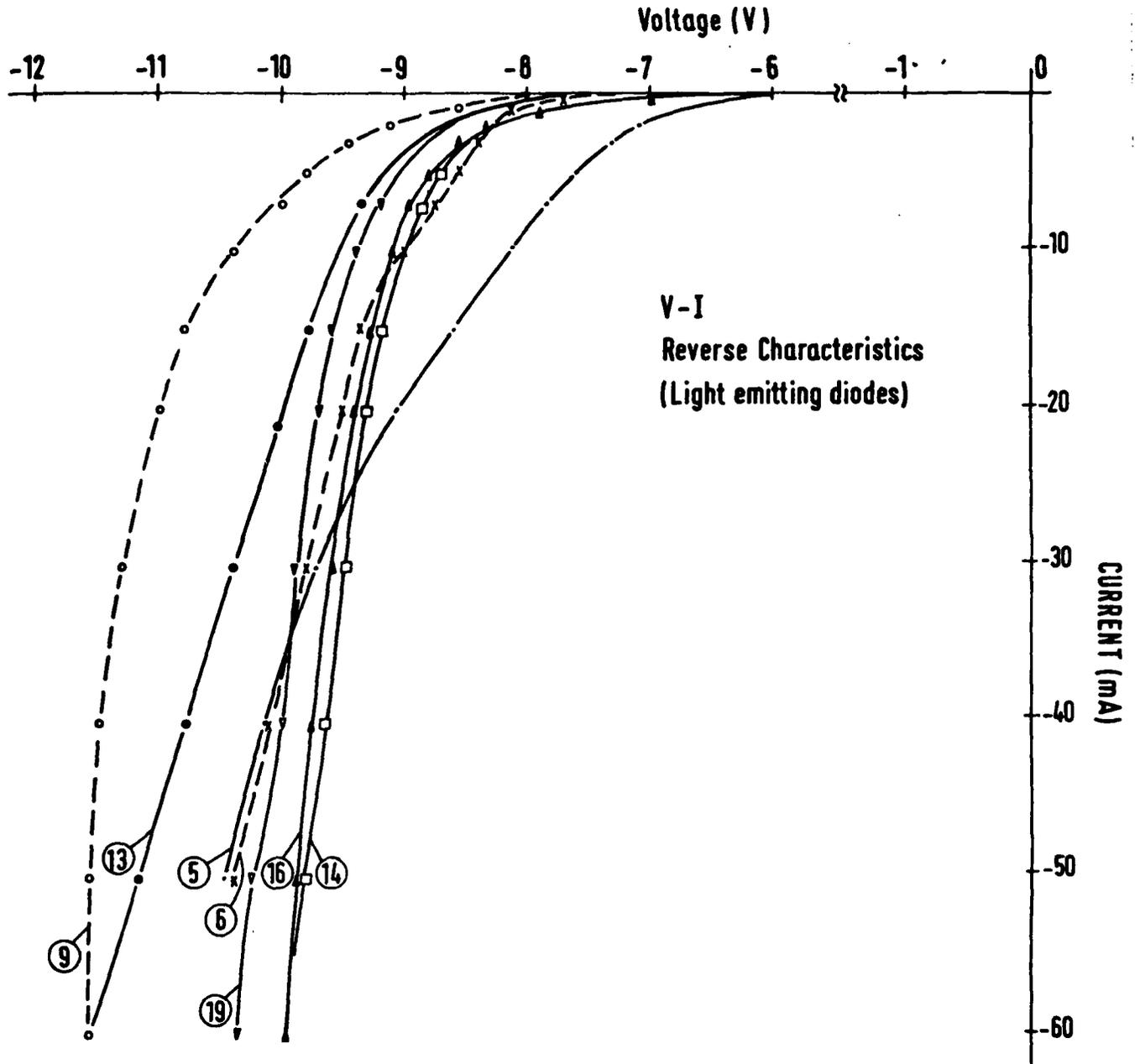


Fig. 4 (a)

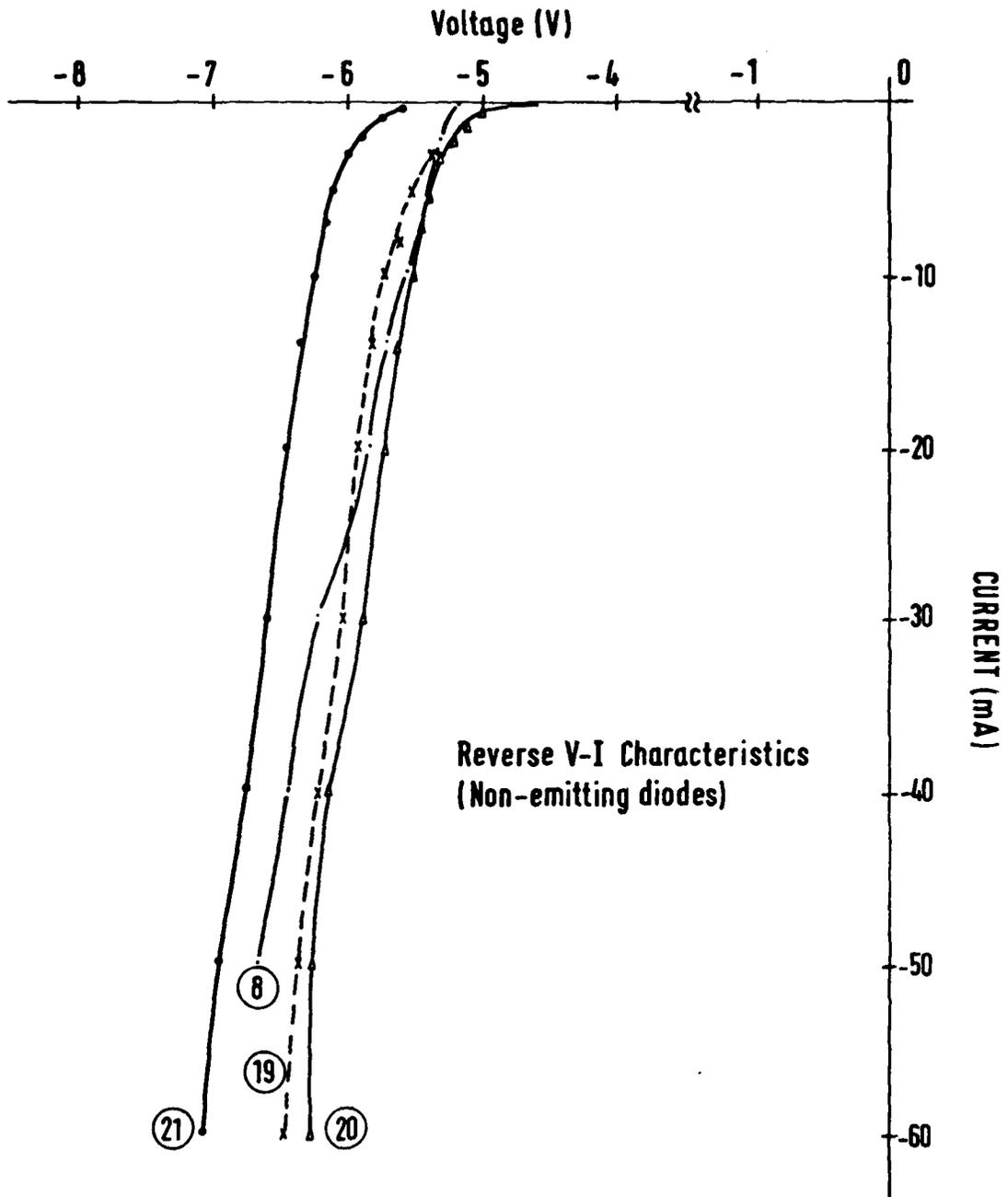


Fig. 4 (b)

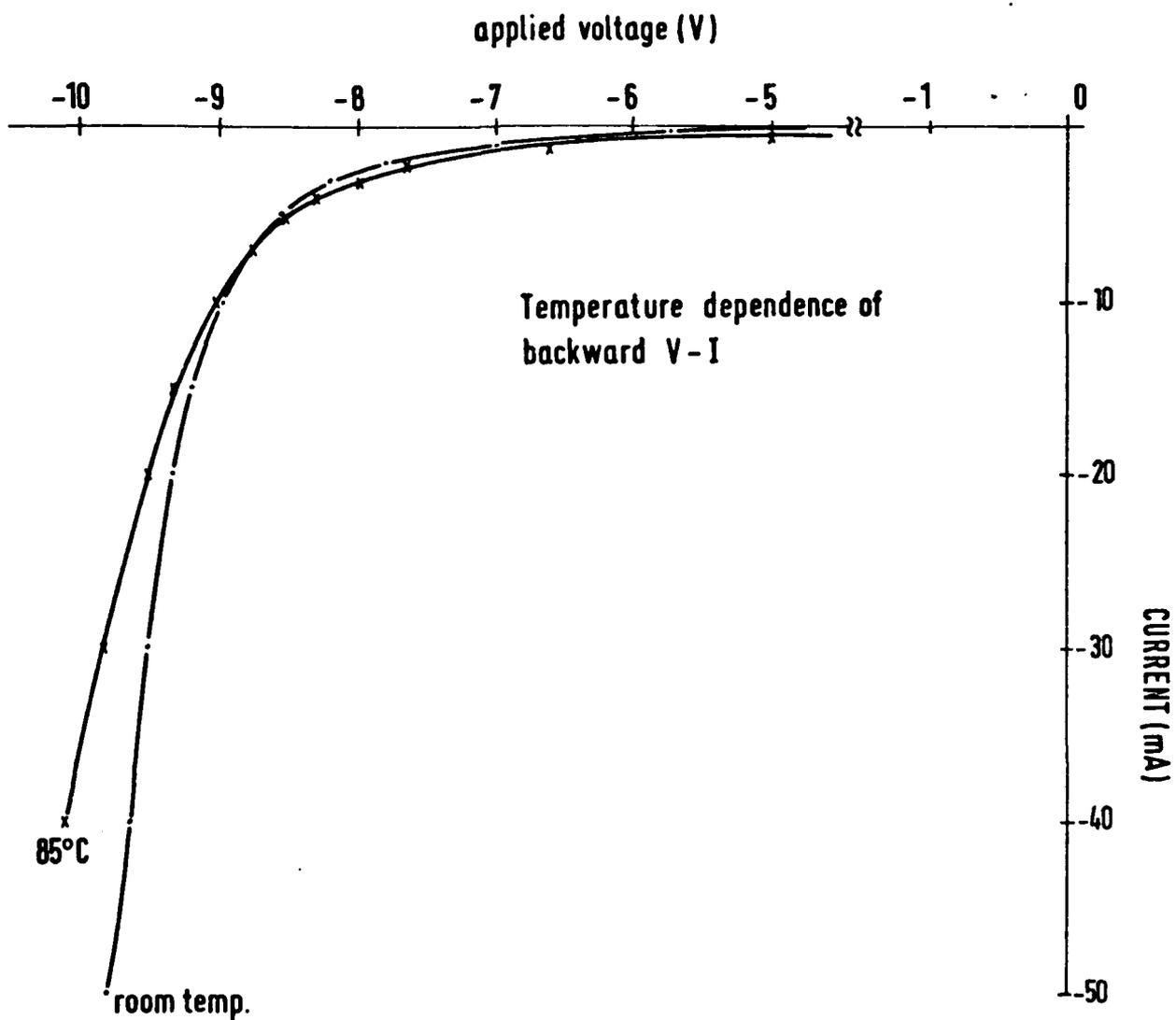


Fig. 5

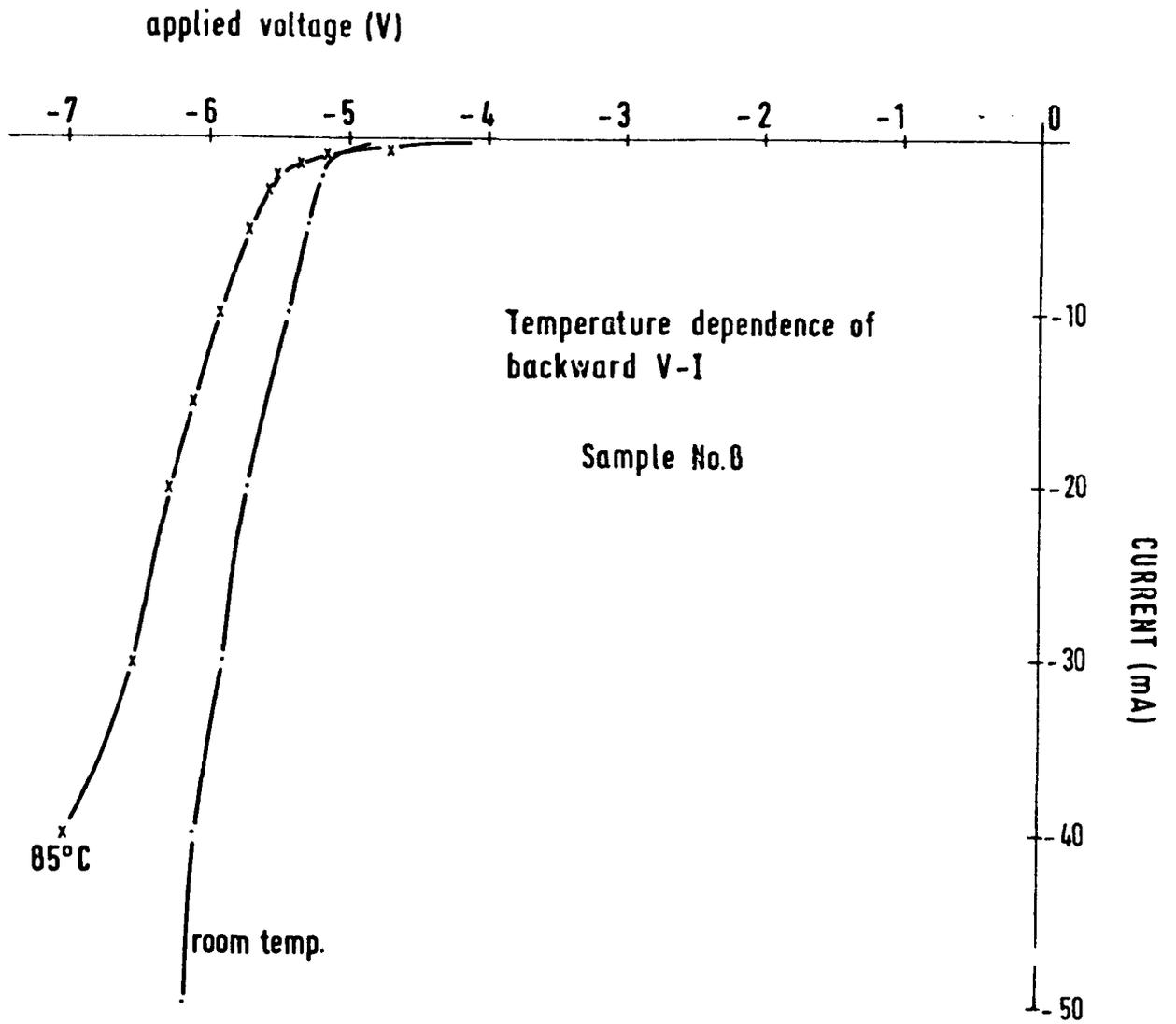


Fig. 6

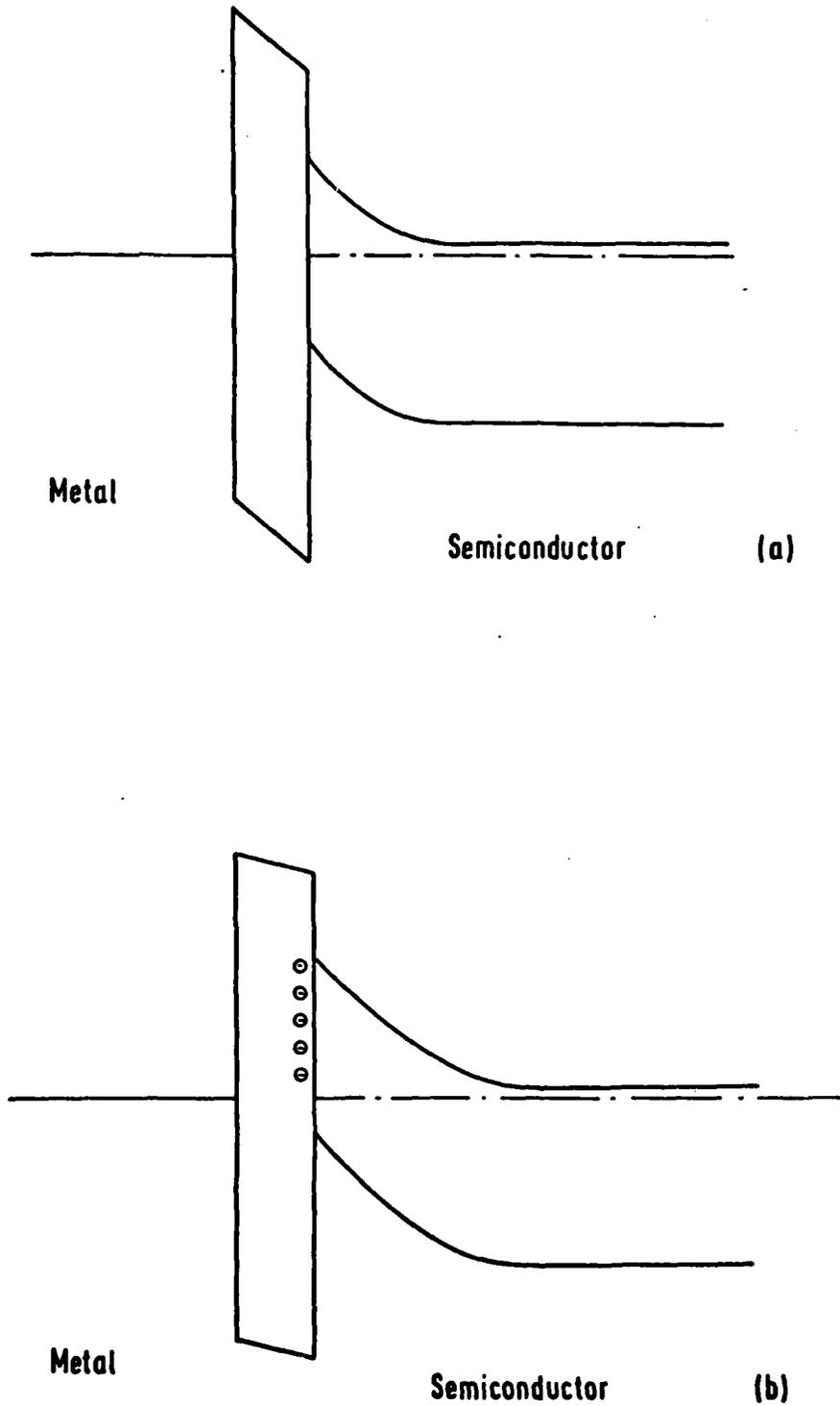


Fig. 7 Band diagram of the MIS Schottky barrier diode without interfacial charge (a) and with negative interfacial charge (b). The negative interfacial charge reduces the breakdown voltage of the reverse V-I characteristic.

The breakdown arises from the avalanche effect both in the light emitting and non-emitting diodes, so that it seems that the avalanche effect is not an exclusive condition for the light emission phenomenon. This is in contrast to the case of the reverse biased silicon p-n junction diodes, where the avalanche effect plays a primary role in the light emission. The reverse biased silicon p-n junction also emits light with a very wide spectrum, from the infrared region to blue, which is very similar to the light emitted from the GaAs MIS Schottky barrier diodes reported here.

So far it is only shown that the avalanche effect does not primarily govern the light emitting phenomena, but light emission is observed when the avalanche breakdown arises. The experiments are being continued to further clarify the surface preparation effects on the light emission phenomena.

Table 2 : A Summary of the light emission effects observed

Definition of Symbols employed:

- O The process was inclusive
- A 4 % H_2O_2 + 2 % NaOH
- B HCl (25 %) was diluted with 5 portions of water
- C NH_3 (25 %)

R1 The wax was removed with acetone, after the evaporation of Al electrodes

R2 After anodization with the AGW solution (50 μA , 3 V), the anodized oxide layer was etched out by using the solution B

R3 The sample was boiled in acetone. Three of ten devices with Al electrodes emit light.

R4 Light emission was observed just after fabrication, but the sample stopped emitting light after 3 weeks.

Continuation of Table 2

Sample	Sticking with wax	Etching solution	Anodization (AGW)	Boiling in acetone	Annealing before the evaporation of Al electrodes	Light emission
005	0	A	200 μ A, 2 V	0	350 C, 5 min.	yes
006	-	A	-	-	350 C, 5 min.	yes
008	0	B	-	R1	-	no
009	0	C	-	R1	-	yes
013	0	B	50 μ A, 2 V	0	350 C, 5 min.	yes
014	0	B	R2	0	350 C, 5 min.	yes
016	0	B	-	0	350 C, 5 min.	yes
017	-	A	-	-	350 C, 5 min.	yes
019	R3	B	-	R3	-	partly yes (R3)
020	-	B	-	-	-	no
021	-	B	-	0	-	no (R4)

CHAPTER 5

Light Modulation of GaAs-MOS Emitters

(E. Huber)

It can be expected that the GaAs-MOS light emitters exhibit a transient behaviour of switching on. Such transient delays would give further indications of the physical mechanism involved with the emission. It would however also show whether this light source can be employed for some optical communication applications. During the period of this grant a system was set up to measure the switching characteristics of light emitters.

In order to be able to compare the performance of MOS emitters with commercially available GaAs p-n junction emitters, this system was first employed to study such p-n devices. This work was undertaken in connection with a study project of several students.

At first, the rise- and faletimes of light emission were measured with several GaAs p-n junction LEDs. The electrical circuit used for this measurement is shown in Fig. 8. The LED is biased by a rectangularly shaped voltage from a function generator. The emitted light was detected by a PIN-Photodiode. Both the current through the LED and the current through the photodiode were simultaneously monitored with a two-channel oscilloscope. The risetimes of the generator and the photodiode are less than 50 ns.

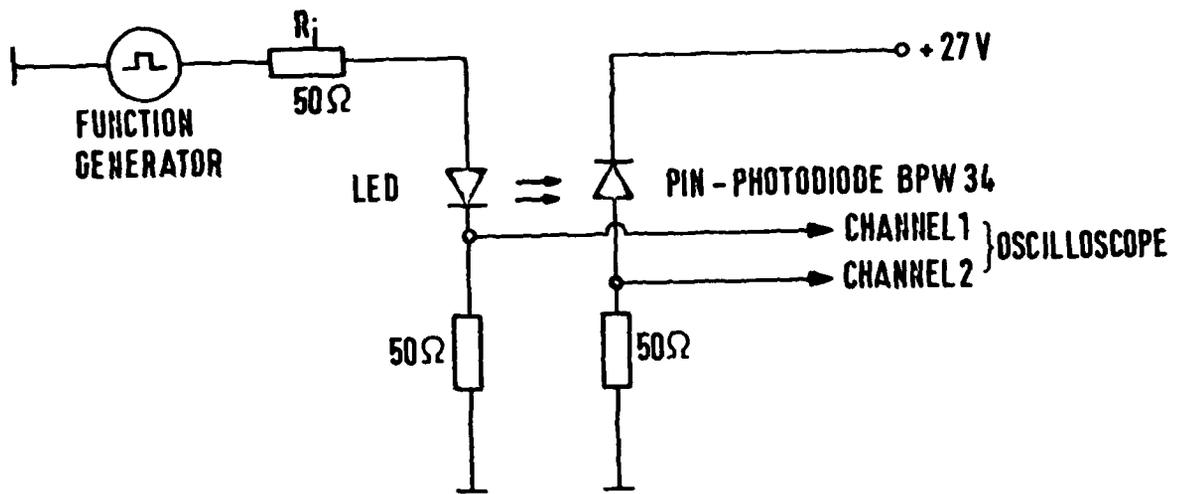


Figure 8 Circuit for measurement of rise- and falltimes of light emission

In Fig. 9 the measured risetimes are shown for 4 different LEDs as a function of peak biasing current. The risetimes for small current are determined by RC-time constants due to the junction capacitance and the current dependent resistance of the LED. For large current, the risetime becomes independent of current. In this region, the risetime is determined by the minority carrier lifetime in the LED. For the LEDs SU 22, LD 271, LD 242 the risetime is in the range of 1 μ s, which is expected for Si-doped GaAs LEDs while for the CQY 31 the risetime is about 100 ns, which is expected for Zn-doped GaAs LEDs. The measured falltimes of light emission showed generally the same behaviour.

For measurements with much faster emitters (one then has to use faster diodes, which are normally of lower sensitivity) and for measurements with emitters with smaller light output, the signal to noise ratio of the wide band measurement circuit becomes too large and it is therefore impossible to measure the risetime directly.

One can overcome this problem by measuring the frequency response of the LED and calculate the risetime from this data. The circuit for the frequency response measurement is shown in Fig. 10. The LED was modulated by a sinusoidal rf-voltage at an operating point adjusted by the DC-voltage source. The photodiode used in this measurement had a -3dB- cutoff frequency of about 500 MHz. The current through the photodiode was measured with a selective microvoltmeter with a bandwidth of 5 kHz.

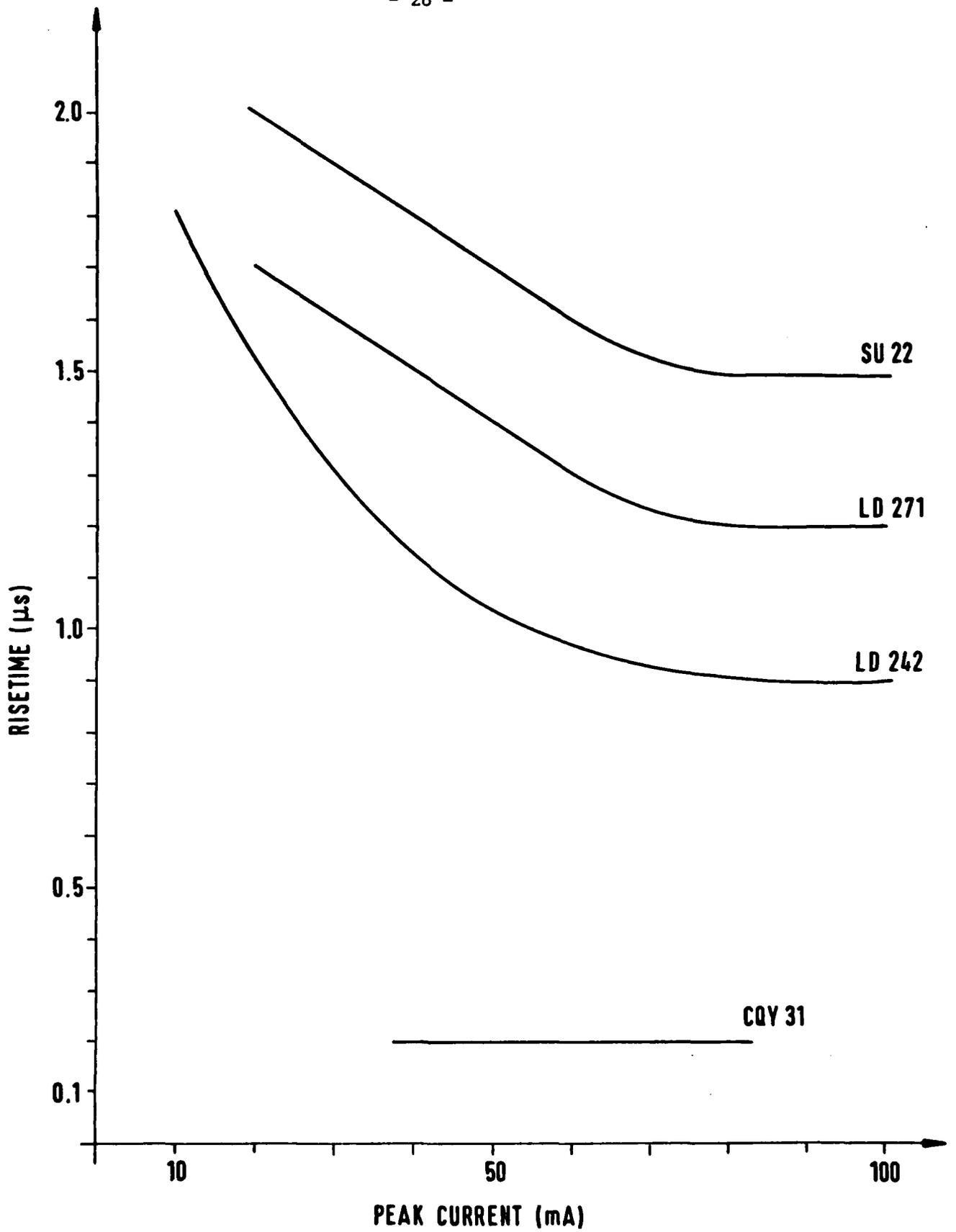


Figure 9 Risetime of different LEDs as a function of peak biasing current

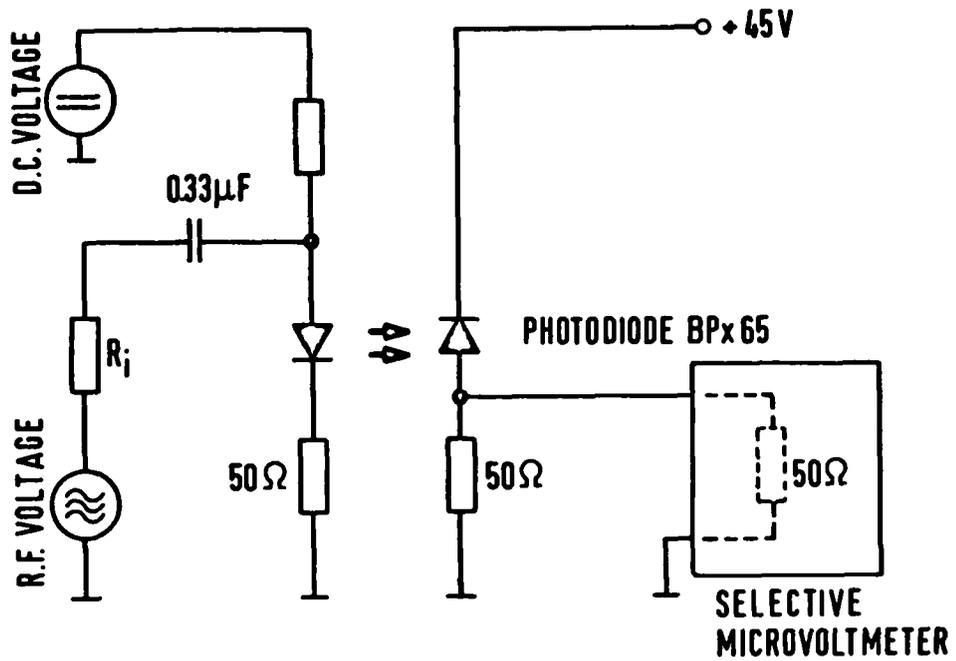


Figure 10 Circuit for frequency response measurement

The frequency response of the LEDs is shown in Figure 11.

Risetimes of the LEDs were calculated from the -3dB- cutoff frequencies of the frequency response characteristic by the relation

$$\tau_r \approx \frac{0,35}{f_r}$$

This relation holds for the risetime τ_r and the -3dB- cutoff frequency f_r of linear low pass filters^[4]. Table 3 gives a comparison of measured risetimes and risetimes calculated from the frequency response curves of the 4 LEDs. As one can see, the values coincide within a factor of two.

Corresponding work on GaAs MOS emitters is now in progress. First results seem to indicate that the rise- and fall times are somewhat larger, but results still have to be carefully verified to ensure that these speed limitations are not caused by the external circuit.

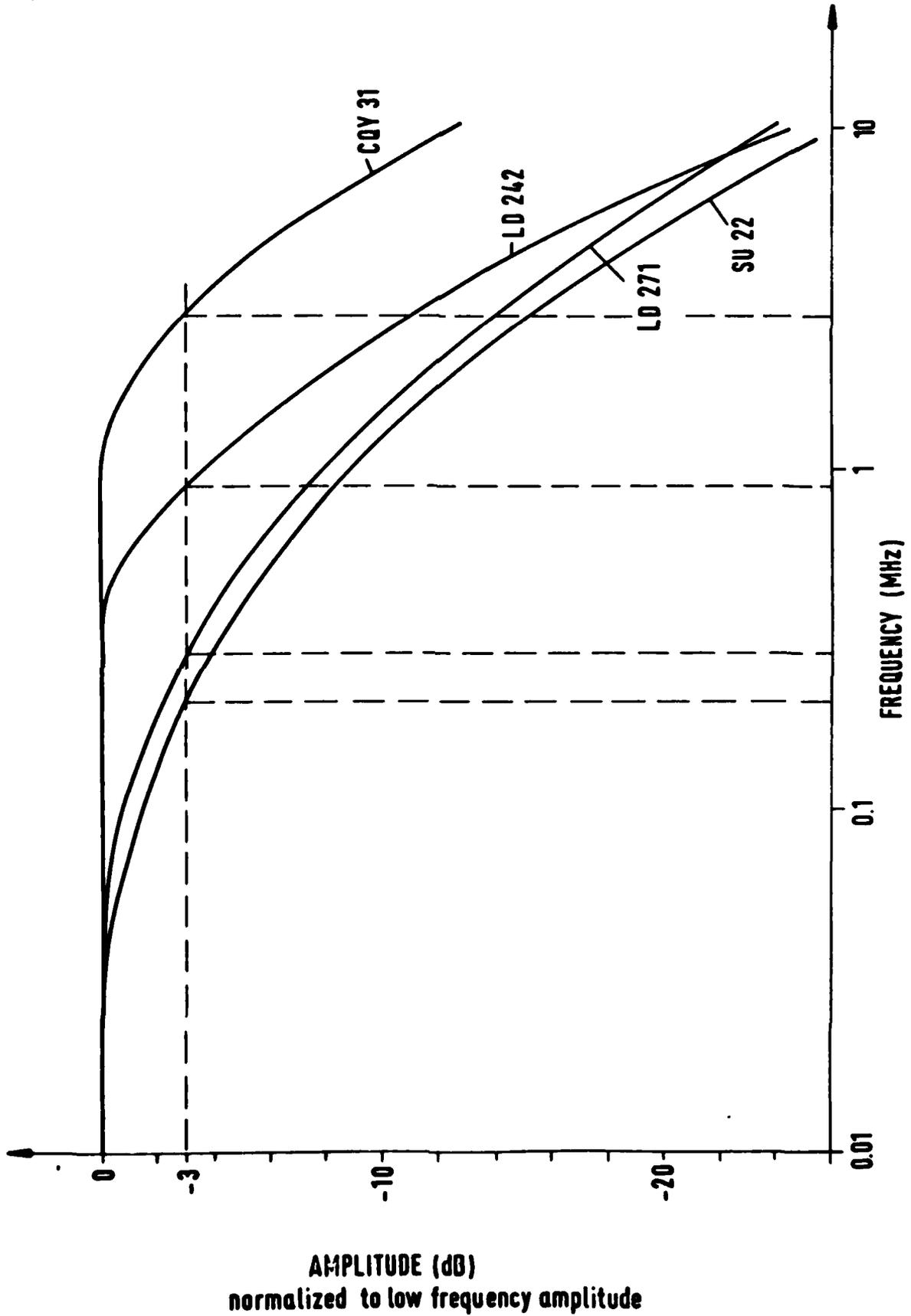


FIG. 11

Figure 11 Frequency response of several LEDs

Table 3

	CQY 31	LD 242	LD 271	SU 22
Risetime (measured) (μ s)	0,15	0,9	1,2	1,5
cut-off frequency (kHz)	2800	900	300	200
Risetime (μ s) calculated from cut-off frequency	0,13	0,4	1,0	2,0

CHAPTER 6

Fabrication of Thin Passivating Nitride Layers on GaAs

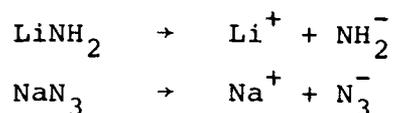
(W. Schmolla)

Some experimental observations seem to suggest that surface states might be particularly produced by oxygen covering the GaAs. There are indications that GaN, sputter - deposited onto clean GaAs surfaces, might result in a reduced surface state density. It is therefore important to consider whether oxide - free insulators might not be useful to passivate GaAs surfaces. Therefore the materials GaN and AlN are of interest since they show in their crystalline form a much larger band gap than GaAs. It is therefore useful to produce thin nitride layers in order to investigate the surface behaviour of GaAs thus covered.

Since a destruction of the GaAs single crystal occurs at the surface for processes above more than 600° C, low temperature processes are indeed of interest. It was therefore decided to fabricate GaN and AlN on Ga and Al respectively by a corresponding process similar to anodic oxidation. For this purpose, liquid ammonia at normal pressure and at temperatures between -33° C and -77° C were employed. Ammonia is a polar solution and exhibits a pH-range of 29*. One can use it with the following solutions as electrolyte: nitrides, azides, imides and amides. We selected sodium azide and

*Jochen Jander, Chemie in wasserfreiem flüssigem Ammoniak, Friedrich Vieweg & Sohn (1966)

lithium amide, as these chemicals can be handled in a safe manner and since they show a sufficient solubility in ammonia. The solutions separate into the following ionic species:



To obtain liquid ammonia, a special system was developed and dried ammonia gas was condensed in argon vapour. The cathode was for the subsequent anodic nitridization platinum.

The following observations could be made with this electrolytic work: At the cathode the known blue colouring effects occur due to dissolved sodium or lithium. These colours disappear after interrupting the voltage. They are caused by the creation of amide molecules at the aluminium anode. The evolution of gas was observed as well as a white porous layer after the evaporation of ammonia under argon. Since the layer could be removed easily by rubbing and since it showed an irregular and porous structure under the microscope, its composition was not further investigated. A similar result was obtained when a GaAs anode was used. In this case the layer had a grey colour. The additional over-potential during electrolytic growth between the electrodes never became larger than several tens of volts for a current of between one and hundred milliamps and showed irregular breakdown effects. All these effects could be explained on the basis of the different behaviour shown by nitrogen

ions in contrast to oxygen ions. Whereas oxygen ions can drift across an oxide layer once formed under the influence of an electric field, this seems to be impossible for nitrogen ions. It is possible that this is related to the different binding energies of oxides and nitrides. Reactions at higher temperatures than -33°C can not be investigated because of the low boiling temperature of ammonia. It would of course be possible to undertake electrolytic work with liquid $\text{NaNH}_2\text{-KNH}_2$ at about 100°C . However, both substances are very explosive in moist air. The conclusion of these initial investigations so far indicate that a nitride film formation for GaAs surface passivation with liquid ammonia requires further systematic efforts which are now under way.

CHAPTER 7

Passivation of InGaAsP

(W. Schmolla)

Quarterternary compound semiconductor materials are used at present to fabricate new light emitters for frequencies where lower attenuation values are available with optical wave guides. It is also of interest to investigate the electrical behaviour of oxide-covered compound semiconductor surfaces since previous work has produced a reasonably good understanding of the corresponding behaviour of the binary materials forming this new quarterternary composition. Investigations to measure the electrical behaviour of MOS structures in InGaAsP are therefore undertaken with the material manufactured at the German Post-Office Laboratories of the nearby Research Institute.

First experimental results indicate that the MOS structure is possibly less strongly affected by various trapping effects. It is of course not clear whether this observation is caused by a particular physical effect available with such quarterternary mixtures. For example it might be possible that the incorporation of non-oxidized As and P leads to conditions where some compensation of these trapping centers takes place. However, further work has to show what the reason for this observed behaviour is.

It has also been suggested that the reason for the strong interface state peak in the band gap of GaAs MOS structures is the presence of As vacancies created by the highly energetic dynamic processes of oxidation. Similarly it was proposed that the interface state densities in the lower half of the energy gap for InP MOS structures are created by In vacancies. It may be that such quaternary mixtures of both binary materials produce a compensation of both vacancy states. Further experimental efforts are underway to substantiate these initial findings.

CHAPTER 8

Emulsions on GaAs Surfaces

(K. Röhkel)

Experimental efforts are underway to explore the possibilities of passivating GaAs surfaces by the deposition of emulsions which turn into SiO_2 after suitable heat treatment. This is based on well-known products of the American Company Emulsitone and lately also of the German Degussa Company.

Recently, first results were published by a U.S. Laboratory¹⁵ where GaAs surface seem to have been passivated quite successfully with such SiO_2 deposition by spinning an emulsion and subsequent heat treatment.

An indication of good surface coverage and adhesion for these silica films out of deposited emulsions can be obtained if the well-known method of providing a doping source from these emulsions is found to produce uniformly doped layers into GaAs. This is in any case a useful technological facility. Therefore it was decided to explore these possibilities, in order to assess our method of depositing SiO_2 .

Since interest in such work also exists at the German Post-Office Laboratories (FTZ) here in Darmstadt, a joint project was undertaken to deposit such films on epitaxial GaAs surfaces. A student project was defined and the student, Mr. H.W. Wagner, undertook most of the experimental measurements under the supervision of Mr. K. Röhkel.

The best method for SiO_2 deposition on GaAs via emulsions was found to be as follows: The emulsion was deposited by spinning and subsequently a heat treatment was applied. A temperature between 200°C and 400°C for 15 minutes was first applied. A solid film occurred through polymerisation with the doping impurity Zn.

Onto (100)-orientated n-GaAs slices (doping concentration $\sim 10^{18} \text{ cm}^{-3}$ and thickness $\sim 1 \text{ mm}$) a SiO_2 layer of $\sim 4000 \text{ \AA}$ thickness was thus deposited and annealing was undertaken in an atmosphere of N_2 for 15 minutes. If the slices were heated up very slowly, the occurrence of little bubbles and cracks in the deposited silica film could be minimized. Such imperfections are magnified during the subsequent diffusion process (Figures 12, 13), which was undertaken at temperatures of around $800^\circ - 900^\circ \text{C}$ for about 20 - 60 minutes. The resulting p-n transition could be made visual by cleavage of the GaAs slices and suitable etching for about 20 sec. The scanning electron microscope details indicate that the junction is about $1 \mu\text{m}$ deep (Fig. 14). This result could be confirmed by the measurement with a microprobe (Fig. 16). After depositing suitable ohmic contacts, the current voltage behaviour shows that a suitable p-n junction is produced (Fig. 15).

Figure 12 : GaAs covered with a silica film after hardening at about 200° C, rapid heat rate



Figure 13 : GaAs surface after 40 minutes diffusion at 900° C (SiO₂ film removed) otherwise like Figure 12

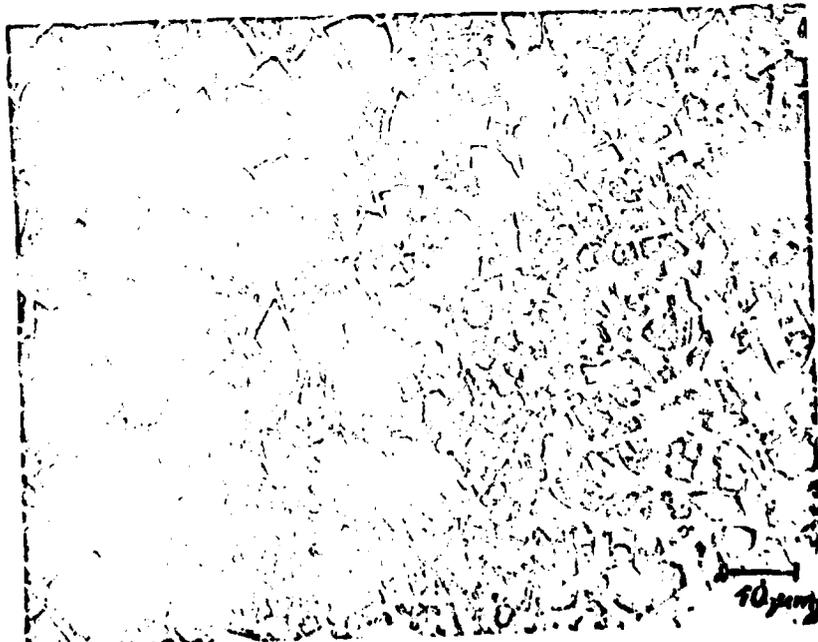


Figure 14 : SEM-result of the etched GaAs cleavage plane after diffusion (900° C, 40 min., p-n junction - 1,5 μ m)

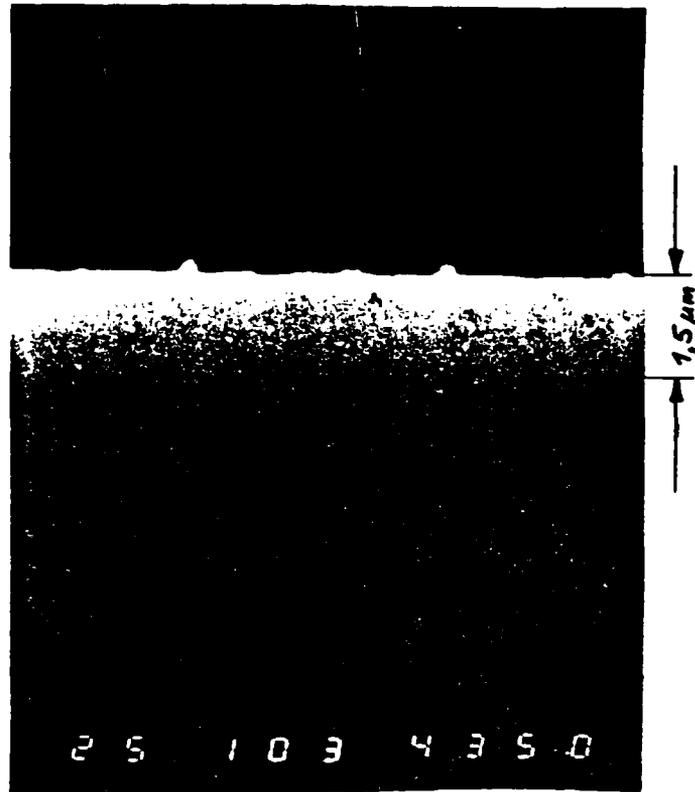


Figure 15: Current voltage characteristic of the p-n junction after ohmic contacts are applied

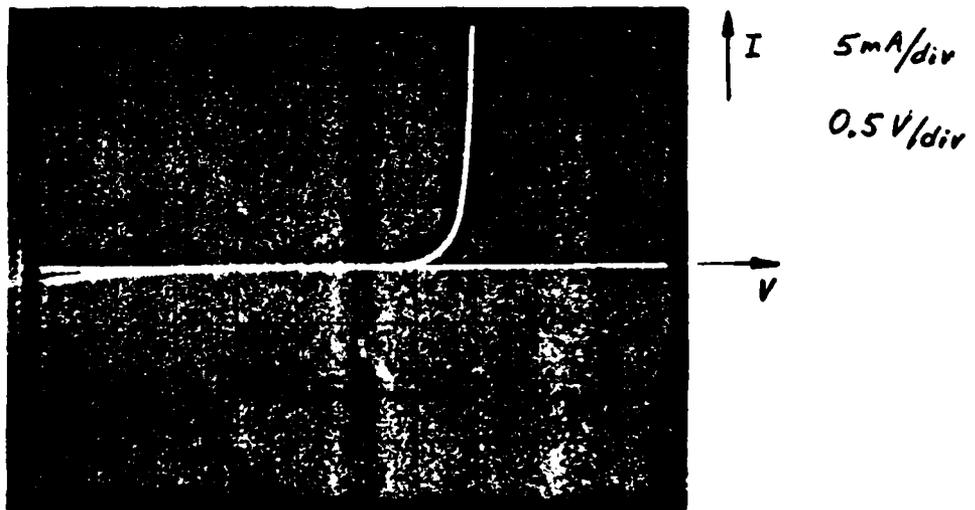
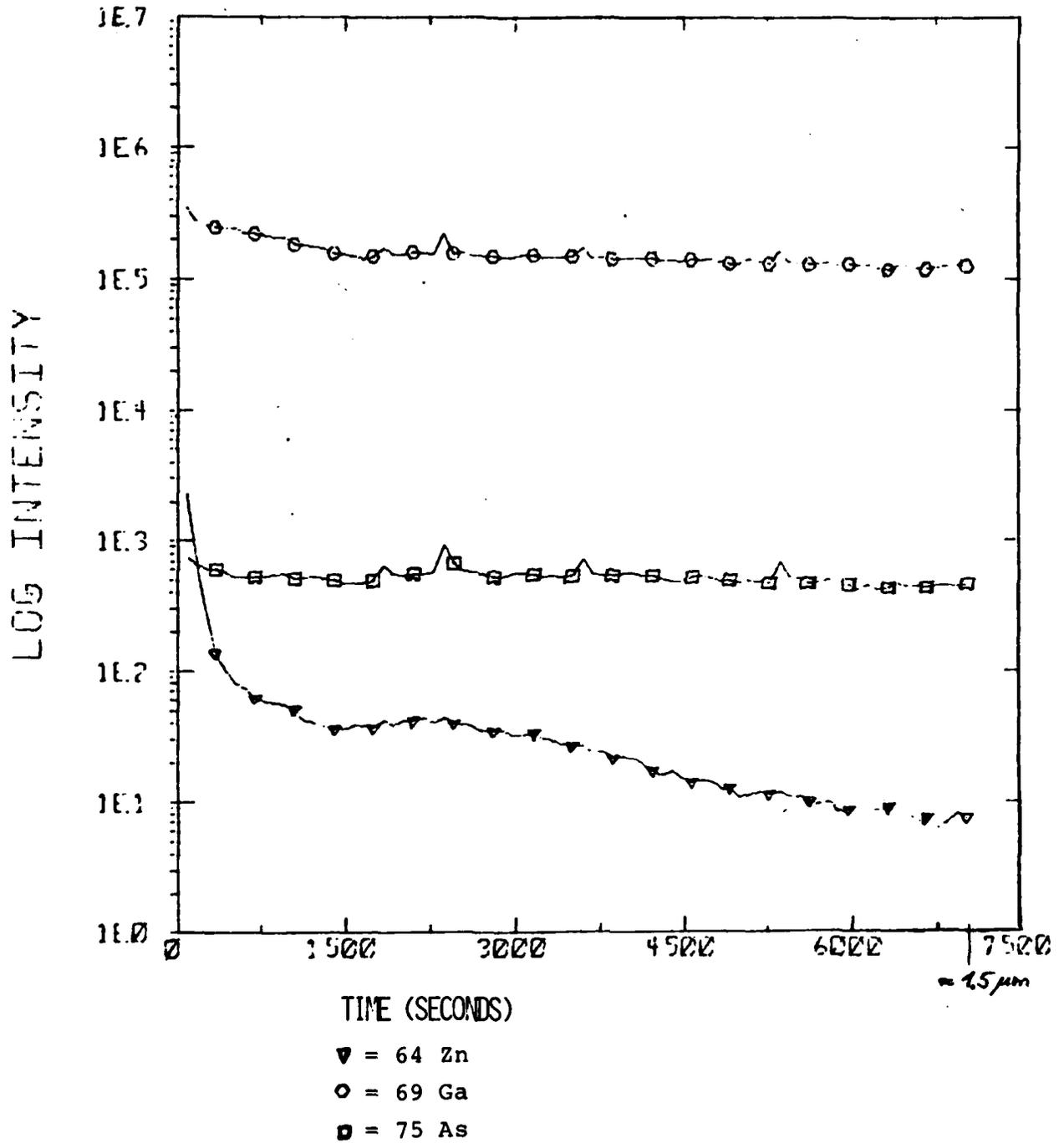


Figure 16 : Microprobe material profile versus etch time

GAAS (Zn)



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SECONDARY ION MASS SPECTROSCOPY

APPENDIX

Publications of the period of this report.

1. S. Hannah, B. Livingstone

Composite Al₂O₃ and Native Oxide on GaAs and InP, Incorporating
Enhanced G III Oxides for Surface Passivation; Paper presented at
MOS Conference in Durham, England, 1979

Institute of Physics Conference Series No 50, Ch. 4

2. H.L. Hartnagel

Non-Si MIS Structures

Invited Paper - International Autumn School on MIS Systems,
Dobogoko, Hungary, 12th - 22th Sept. 1979

3. H.L. Hartnagel, D. Pavlidis

Microwave Characterisation and Performance of GaAs MOSFETs
Conference Proceedings of the 9th European Solid State Device
Research Conference (ESSDERC 79), Munich, West Germany,
9th - 14th Sept. 1979

4. B. Bayraktaroglu, H.L. Hartnagel

Anodic Oxides on GaAs

IV: Thin Anodic Oxides on GaAs

Invited Paper, Int. J. Electronics 46 (1979), p. 1-11

5. P. Breeze, H.L. Hartnagel
An Assessment of the Quality of Anodic Native Oxides on GaAs
for MOS Devices
Thin Solid Films 56 (1979) p. 51-61

6. J.T. Grant, H.L. Hartnagel, F.L. Schuermeyer, B. Bayraktaroglu,
D. Mays
Multiple Insulator Layers on GaAs studied by Auger Analysis
Int. J. Electronics 46 (1979) p. 209-214

7. H.T. Mills, H.L. Hartnagel
Ohmic Contacts to InP
J. Electronics 46 (1979) p. 65-73

8. B.L. Weiss, H.L. Hartnagel
Crystallisation of Native Oxides on GaAs for Device Application
Thin Solid Films 56 (1979) p. 143-152

9. D.W. Langer, F.L. Schuermeyer, J. Johnson, H.L. Hartnagel,
H.P. Singh, C.W. Litton
Chemical Reactions of Oxide Layers on GaAs
7th Annual Conference on the Physics of Compound Semiconductor
Interfaces, Estes Park, Colorado, U.S.A., 29th - 31st Jan. 1980
to be published in Journal of Vacuum Science Technology

10. P.A. Breeze, H.L. Hartnagel
An Investigation of Anodically Grown Films on GaAs Using X-Ray Photoelectron
Spectroscopy
J. Electrochem. Soc.: Solid-State Science and Technology, Febr. 1980, Vo. 127, No2

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Appl. Phys. Lett. 34 (1979) 1

Composite Al₂O₃ and native oxide on GaAs and InP, incorporating enhanced group III oxides for surface passivation

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Abstract. Investigations into the MIS characteristics of anodic oxides on GaAs and InP have led to the development of a wet anodic method that enables good dielectric layers to be grown. The resulting MIS capacitance-voltage characteristics exhibit, for the first time, low-frequency-type behaviour, indicating that anodisation is feasible as a method of surface passivation of GaAs and InP. The results presented indicate that for the n-type semiconductors, the surface potential for GaAs may be varied between flat-band and strong inversion and for InP both strong inversion and accumulation are possible.

1. Introduction

GaAs and InP have become increasingly important as microwave device semiconductors because of their high electron mobility and high saturation velocity. Thus, together with the outstandingly successful Si MIS technology, has created the need for a good reliable surface passivation technique for these semiconductors. Until recently, all attempts to produce such a surface passivating layer have resulted in leaky dielectrics and/or surface-state-rich semiconductor surfaces. To date the best results for GaAs have been reported by Chang *et al* (1979) who formed a native dielectric layer in a plasma of O₂ in CF₄. For InP, the best dielectrics produced were described by Fritzsche (1978), who used chemical vapour deposition of SiO₂ onto InP surfaces.

In this paper, anodisation in an electrolyte as a technique for forming a dielectric is considered and three types of oxide layers have been investigated. Firstly, a native oxide formed by anodisation of the clean semiconductor surface was studied. Both the native oxides on GaAs and InP exhibit poor MIS characteristics; those of the GaAs are consistent with a large number of surface states and those on InP are primarily due to a leaky oxide. It is for these reasons that investigations of composite oxides on these semiconductors have been made. Two types of composites have been studied: the first involves anodisation of a deposited layer of Al on the clean semiconductor surface, the second, the chemical reduction of a thin native oxide before the Al deposition, with formation of the dielectric by the anodisation of the structure. It is the latter of these composites that exhibits promising characteristics.

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2. MIS diode preparation

A convenient method of assessing the quality of a surface passivating layer is to measure the capacitance-voltage characteristics of MIS diodes. The following section describes the procedures adopted to produce MIS diodes for each of the three types of passivating oxides.

All the oxides were grown under constant-current conditions at a temperature of approximately 5°C using an electrolyte first reported by Hasegawa and Hartnagel (1976) and consisting of a mixture of 3% tartaric acid solution and propylene glycol in the ratio 1:2:1. The growth of the oxides was monitored by measuring the overpotential across the growing oxide as a function of time.

As the initial step for all the oxides, the semiconductor substrates were cleaned in hot acetone, then in hot methanol and methanol in sequence, and then blown dry in a stream of nitrogen. For GaAs, the surface on which the oxides were to be grown was etched, for GaAs, with a mixture of 1:1 by weight of NiOH in water and 1:2 by volume of H_2O_2 in a ratio of 1:1, whereas for InP the etchant consisted of a mixture of HNO_3 , H_2O in the ratio 1:2:1. A typical etch time was 2 min, which removed approximately 500 Å of substrate. After etching the substrates were rinsed in deionised water and dried by wicking in nitrogen.

For growth of the native oxide, the etching of the semiconductor surface, the current density for GaAs native oxide was $100 \mu A cm^{-2}$ and that for InP was $200 \mu A cm^{-2}$. The growth constants and limitations of the oxide growth for GaAs and InP have been reported by Hasegawa and Hartnagel (1976) and by Colquhoun and Hartnagel (1977) respectively.

The first type of composite oxide (MAOS structures) was formed initially by deposition of a layer of Al, by thermal evaporation at a pressure of 10^{-6} Torr to a typical thickness of 500 Å, onto the etched semiconductor surface. Following the Al deposition the composite oxides were formed by anodisation. The effect of anodising such a structure on GaAs has been reported by Bayraktaroglu *et al.* (1977). The composite oxide thus formed depends on the current density used and the amount of GaAs consumed after the complete oxidation of the Al layer. Growth of such oxides on InP raised all attempts; the partially anodised Al film was seen to flake off the InP surface. This behaviour is assumed to be a function of the sticking qualities of the Al onto the etched InP surface.

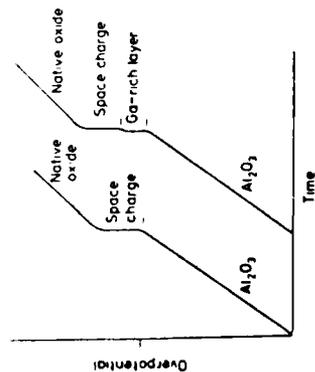


Figure 1. Schematic diagram for the overpotential-time curves for MAOS composite and new composite oxide on GaAs.

The second type of composite oxide is more complex than the above and great care had to be taken to ensure that the semiconductor surface remained clean during the process.

2.1. Step 1

After the initial etching of the semiconductor surface, a thin layer of native oxide 100 Å thick, was grown on the surfaces of both the GaAs and InP with current densities of $1 mA cm^{-2}$ and $200 \mu A cm^{-2}$ respectively, under strong light conditions. As these experiments were performed on n-type substrates, strong light was used to ensure a uniform oxide film.

The substrates were then removed from the electrolyte and cleaned in hot acetone, the samples were again blown dry and microscopically inspected for stains and particles.

2.2. Step 2

The oxides were then annealed in hydrogen at 1 atm for 10 min. The temperature for the GaAs substrate was 600°C, which was sufficiently high to reduce the oxides to their metallic elements and also to boil off the arsenic leaving behind a Ga-rich layer in intimate contact with the GaAs. The temperature for the InP substrate was 400°C, which produced the best device characteristics. The effect of a temperature of 600°C on the InP was to produce severe pitting of the surface.

2.3. Step 3

A layer of Al was deposited by evaporation at 10^{-6} Torr to a typical thickness of 500 Å.

2.4. Step 4

The structures were then anodised in dull light in the same manner as for the MAOS structures, at a current density of $100 \mu A cm^{-2}$ for the GaAs and $200 \mu A cm^{-2}$ for the InP. The growth curve for these oxides contained a new feature when compared with that of a similar composite oxide of the first type. A schematic diagram for the two structures, for comparison, is shown in figure 1. The initial linear region for both cases is characterised by a straight line and is due to the formation of Al_2O_3 . The new feature occurring with the second composite is believed to be due to the re-anodisation of, for GaAs, the Ga-rich layer and is characterised by a steep rise (approximately 4 V for an initial oxide layer of 100 Å) followed by an inflection. The second sharp rise corresponds to the sharp rise in the MAOS growth curve and is due to the formation of a space-charge layer in the GaAs surface (this space-charge voltage does not occur under strong light conditions). The final linear portion of the curve is due to the continued oxidation of the underlying substrate. This type of composite oxide was found to be readily and reproducibly grown on InP, unlike the attempts to grow MAOS type oxides and the overpotential-time characteristics show similar behaviour to those for GaAs.

2.5. Step 5

Ohmic contacts were then deposited onto the reverse surface of the substrates. For n-type GaAs, Au-Ce was used and for n-type InP, Au-Ge-Ni contacts were formed. The Ohmic contact metals had been omitted during the previous stages of this type of oxide growth to avoid any possible contamination and degradation during the initial

annealing cycle. The penultimate step for all the structures was to anneal the oxides (and Ohmic contacts) in nitrogen for 15 min, at a temperature of 350 °C for GaAs (the optimum annealing cycle for native oxides as determined by Weiss *et al* 1977), and at 300 °C for InP (the optimum temperature for native oxides as determined by Colquhoun and Hartnagel 1976). Finally Al field-plates were deposited by thermal evaporation through a metal screen. A typical field-plate was 1500 Å thick and 10^{-3} cm² in area, with typically 50 diodes per substrate.

3. Capacitance-voltage measurements

C-V characteristics were measured with a two-phase Brookdeal Lock-in Amplifier model 5502 in conjunction with a variable-frequency signal generator and a ramp voltage generator. A reference signal of 250 mV RMS was supplied to the lock-in amplifier and was capacitively divided to supply a measuring signal of 25 mV RMS to the diode under test. The calibration of the amplifier was achieved using air capacitors of known value. The C-V curve was monitored on a X-Y recorder. Low-temperature measurements were obtained by cooling the test rig with liquid nitrogen; the temperature was estimated by a thermocouple mounted near the substrate under test. Theoretical C-V curves were computed using the manufacturers quoted substrate background doping and by measuring the oxide capacitance at low frequencies and high accumulating bias.

Figure 2 shows C-V characteristics for native oxides on GaAs, for an n-type substrate with background doping of 2×10^{16} cm⁻³ and a diode area of 2×10^{-3} cm². Figure 2(a) shows the room-temperature behaviour plotted against frequency and figure 2(a) the effect of lowering the temperature. It can be seen that the essential feature at high frequencies and low temperatures is that the C-V curve becomes flat, indicating that the surface potential is virtually pinned. A comparison of experimental C-V curves with the theoretical results indicates that for n-type GaAs with background doping of 2×10^{16} cm⁻³, the surface potential is virtually pinned at -0.4 eV, which corresponds to depletion, and differs from the value obtained by Hasegawa and Hartnagel (1976) whose

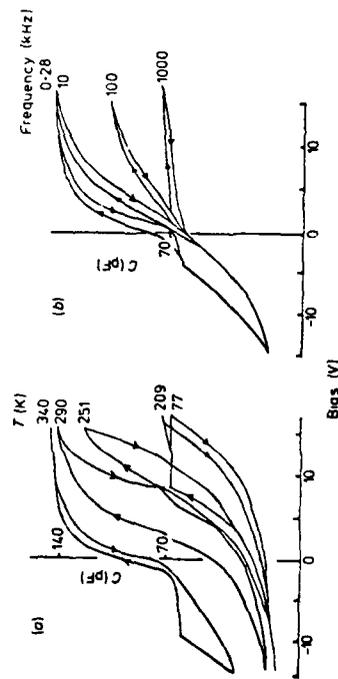


Figure 2. C-V characteristics of native oxide on GaAs. (a) Effect of temperature (data obtained at 1 kHz) and (b) effect of frequency (data obtained at 300 K). Sample B2; oxide layer 1000 Å thick; n-type GaAs; background doping 2×10^{16} cm⁻³.

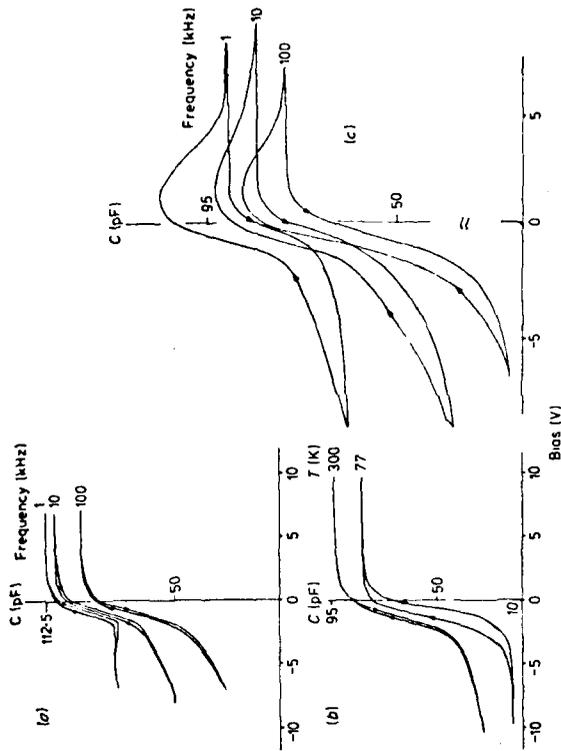


Figure 3. C-V characteristics of native oxides on InP. (a) Effect of frequency (data obtained at room temperature), (b) effect of temperature (data obtained at 100 kHz) and (c) effect of ageing (data obtained at room temperature). Sample e28, dull light, area = 0.717×10^{-2} cm².

results indicate pinning in weak inversion. Results for p-type GaAs indicate that for background doping of 10^{17} cm⁻³, the surface potential is virtually pinned at 0.5 eV. C-V characteristics for native oxides on InP are shown in figure 3 for an n-type substrate with background doping of 10^{15} cm⁻² and a diode area of 0.717×10^{-3} cm². Figure 3(a) shows the room-temperature behaviour plotted against frequency immediately after removal from the final annealing cycle. It can be seen that there is a large frequency dispersion in the oxide capacitance in accumulation, whereas in inversion the capacitance does not level off, indicating that there may be a leaky oxide. DC leakage measurements show that with an electric field of 2×10^6 V cm⁻¹ across the oxide, the leakage current density was 10^{-3} A cm⁻². The temperature variation of the C-V plots is shown in figure 3(b) and as can be seen, the curves become steeper when in inversion and the capacitance levels off almost exactly at the theoretical high-frequency capacitance. From a comparison of theoretical data and the experimental C-V curves it was found that there was no pinning of the surface potential. However, after leaving the test diode in air for a period of 1 week, the C-V characteristics changed to those shown in figure 3(c). These changes are produced as a result of the native oxide absorbing water from the surrounding atmosphere. A short annealing cycle of 150 °C for 30 min returns the C-V characteristics to those shown in figure 3(a).

Similar measurements on MAOS devices on GaAs indicate that the surface potential is again virtually pinned. Figure 4 shows the effect of temperature on the C-V character-

istic for a device with an Al_2O_3 1400 Å layer, overlying a layer of native oxide estimated to be between 50 and 100 Å thick. The value of the surface potential was found to be dependent on the amount of native oxide incorporated into the composite. For thin oxides, of the order of 50 Å thick, surface potentials were estimated to be -0.8 and 0.95 eV for n-type (10^{16} cm^{-3}) and p-type (10^{17} cm^{-3}) GaAs respectively. For oxide layers of thickness greater than 100 Å, the surface potential became pinned at -0.55 and 0.7 eV for n-type (10^{16} cm^{-3}) and p-type (10^{17} cm^{-3}) GaAs respectively.

The third type of oxide on GaAs displays C-V characteristics that are again dependent on the amount of GaAs consumed during the oxide growth. If the amount of GaAs consumed is limited to between 10 and 40 Å, as indicated in figure 5 (for a diode pro-

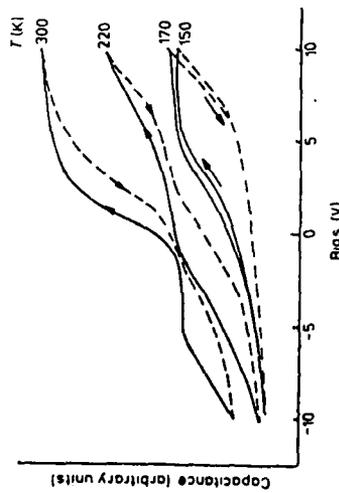


Figure 4. Effect of temperature on the C-V characteristics of a MAOS diode. Sample SJ/As, frequency 1 kHz, dull light.

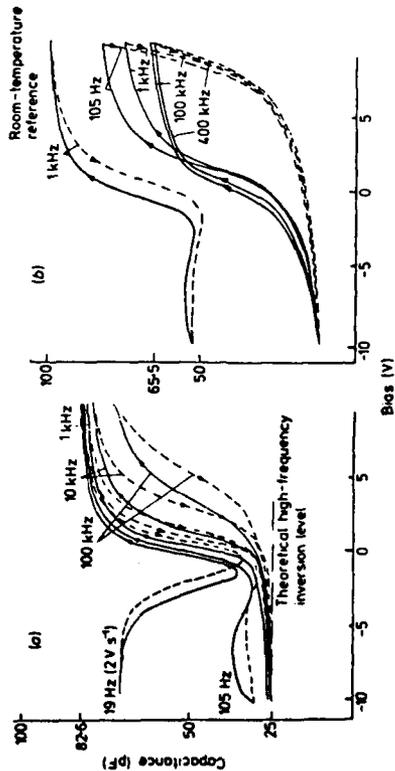


Figure 5. Effect of frequency at 300 K (a) and 77 K (b) on the C-V characteristics of new composite oxide on GaAs. (a) Sample 17/Ga, area $0.9 \times 10^{-3} \text{ cm}^2$, dull light; (b) sample 12/Ga, area $1 \times 10^{-1} \text{ cm}^2$, dull light.

duced on n-type GaAs, background doping $2 \times 10^{16} \text{ cm}^{-3}$, total oxide thickness 750 Å, diode area $9 \times 10^{-4} \text{ cm}^2$, the surface potential is no longer pinned. Figure 5(a) shows the characteristics as a function of frequency and it can be seen that for frequencies above 10 kHz, the inversion capacitance coincides with the theoretical high-frequency inversion capacitance; for low frequencies below 10 kHz, the inversion capacitance exhibits the expected low-frequency behaviour, characterised by a minimum in the curve. Deep depletion, which occurs for even relatively slow ramp speeds with the two previous types of oxides, is not observed with this oxide until a sweep rate of the order of 200 V s^{-1} is applied. Figure 5(b) shows the effect of frequency at low temperatures on a similar diode with a total oxide thickness of 700 Å and an area of 10^{-3} cm^2 . The accumulation capacitance is seen to vary, but the frequency dispersion saturates at 400 kHz and at this point the estimated surface potential is 0.05 eV, which corresponds to almost flat-band conditions.

If the amount of GaAs consumed is greater than 50 Å, then the C-V characteristics again deteriorate and eventually become the same as for MAOS devices incorporating thick native oxide layers. Surface potential pinning is exhibited for n-type GaAs (background doping 10^{16} cm^{-3}) at a value of -0.5 eV.

Similar results for n-type InP are shown in figures 6(a) and (b), where the background doping of the substrate is again 10^{15} cm^{-3} and the area and oxide thickness of the test diode are $0.813 \times 10^{-3} \text{ cm}^2$ and 750 Å. It can be seen from figure 6(a) that low-frequency-type behaviour starts at around 1 MHz and shows both strong inversion and accumulation. Deep depletion is not observed for ramp speeds up to 100 V s^{-1} .

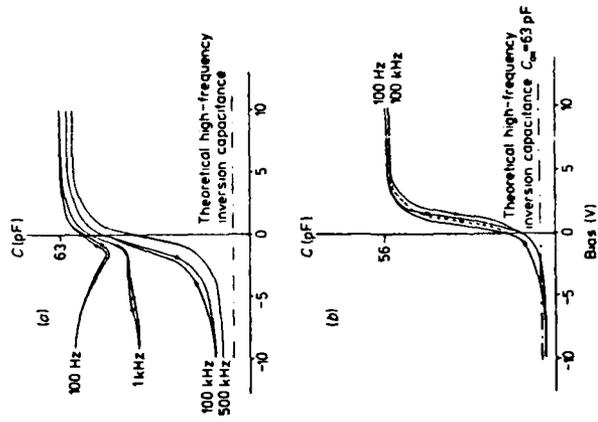


Figure 6. Effect of frequency at room temperature (a) and 77 K (b) on the C-V characteristics of composite oxides on InP. Sample e22, area $0.813 \times 10^{-3} \text{ cm}^2$, dull light.

There is again some frequency dispersion of the oxide capacitance, as with the native oxide structures, although it is reduced and saturates at approximately 500 kHz. The effect of temperature on the $C-V$ characteristics is shown in figure 6(b) and again both strong inversion and strong accumulation are observed, with the inversion capacitance approaching the theoretical high-frequency value. It is clear from these results that there is no pinning of the surface potentials, DC leakage measurements showed that with a field of $2 \times 10^6 \text{ V cm}^{-1}$ across the oxide, the leakage current was $\sim 10^{-3} \text{ A cm}^{-2}$.

Similar to GaAs, if the amount of InP consumed is greater than 50 Å, the $C-V$ characteristics again deteriorate, i.e. greater frequency dispersion and lower minority-carrier generation occur. The breakdown field of these composite oxides on both GaAs and InP was found to be $\sim 4 \times 10^6 \text{ V cm}^{-1}$.

4. Discussion

The surface potential pinning that occurs with both native oxide and MAOS structures on GaAs is associated with a large number of surface states at the oxide interface. With the MAOS structures the distribution of these traps is seen to be a function of the amount of GaAs consumed: recent work by Bayraktaroglu *et al.* (1979), who anodised Al on p-type GaAs in a solution of ammonium pentaborate, has shown that if the growth is terminated so that virtually no native oxide is formed, then no surface pinning occurs. The nature and cause of the surface traps are not fully understood, but work by Breeze *et al.* (1979) has shown that near a native oxide-GaAs interface, a region exists that contains an amount of non-oxidised or partially oxidized As.

It is believed that the improvements observed with the second type of composite oxide arise mainly from the reduction in the amount of As at the oxide interface, because of the formation of the Ga-rich layer by reduction in hydrogen. Experiments involving the annealing of a clean GaAs surface in hydrogen at 600 °C did not show the same improvements as those in which an oxide layer was grown on the surface before annealing. This is probably because the vapour pressure of As in the oxide is much greater than that of As in GaAs (Ishii and Jeppson 1977) at these temperatures.

The poor characteristics of InP native oxides have been associated with poor leakage characteristics of the oxide which do not allow the build-up of an inversion or accumulation charge. The attempts to grow MAOS-type oxides on the InP surface failed, probably because of poor sticking qualities. The new type of composite oxide, however, exhibits excellent capacitance-voltage characteristics which may be associated with the decreased conductivity of the insulator on the surface. However, similar oxides on an InP surface that was simply annealed in hydrogen, although they could be grown, did not show the same type of capacitance-voltage characteristics, indicating that the role of a reduced oxide in intimate contact with the InP is important in obtaining good MIS characteristics.

5. Conclusions

A method has been presented which shows for the first time that it may be possible to use wet anodisation as a technique for the surface passivation of GaAs and InP. The results have shown that for GaAs strong inversion and almost flat-band conditions have been achieved, whereas for InP both strong inversion and accumulation have been obtained.

To date, few attempts have been made to optimise the various steps involved in producing the devices and it is hoped that the MIS characteristics may still be improved and extended to p-type semiconductors.

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Non-Silicon MIS Structures

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1. Introduction

After the early non-Si components employed special effects of such semiconducting materials as GaAs, for example the electron-transfer effect, or efficient junction lasing, new developments produced microwave FET-amplifiers and their analog and digital integration. So far, these transistors are primarily of Schottky-gate type, but there is of course a great interest to have also MOSFET's. Extensive efforts are made therefore in many countries to obtain a passivation scheme on compound-semiconductor surfaces. So far, a variety of methods have been reported to form insulating films on GaAs and other compound semiconductors, including thermal-,

plasma- and anodic oxidation; evaporation, sputtering, chemical vapour deposition and others^[1]. None is fully satisfactory, although some are more useful already than others. They can be divided into two types of film formation, namely oxidation and deposition. The films obtained by oxidation are called "native oxide", if this is grown by consuming the semiconductor. The chemical composition of the oxide depends somewhat on the oxidation conditions. In general, a low temperature process such as plasma and electrolytic anodic oxidation produces oxides of both Ga and As. The composition ratio of Ga, As and O has been analyzed by various methods such as Auger electron spectroscopy, secondary ion mass spectroscopy and X-ray photoelectron spectroscopy.

A high temperature process such as thermal oxidation produces polycrystalline gallium oxide (Ga_2O_3). Oxides grown by a low temperature process change their composition to Ga_2O_3 when they are annealed at temperatures higher than 450°C . Polycrystalline Ga_2O_3 is rather conductive and not suitable for passivation of GaAs. Furthermore, thermal oxidation and high-energy plasma oxidation introduce a damaged layer on the GaAs surface.

To achieve a suitable passivation scheme, it is necessary to find an insulator satisfying a series of requirements. Firstly, the Interface semiconductor-Insulator must be such that the application of a bias to a metal-oxide-semiconductor sandwich enables one to bring the Fermi level freely to accumulation or to depletion or to inversion conditions. Secondly, the leakage current and charge trapping of the oxide must be very small. Then the chemical stability

of the insulator has to be high; particularly, the diffusion constants for important impurities of the semiconductor have to be sufficiently small in the insulator which has to act as a protective coating.

Some first achievements are now available with a few of the passivating films covering GaAs and other compound semiconductors. They are still tentative and require further confirmation. However, they already seem to give a coherent picture. The present review is written, to bring those entering this expanding field, into contact with the present-day understanding of passivation for compound semiconductors and to stimulate those working in this field to make further contributions. This review covers experimental information as established by many workers in this area.

2. Amorphous or Crystalline Oxides

Results are firstly reviewed here which show the change in the crystallographic structure, crystallinity and chemical composition as a function of growth rate (initial current density) and annealing parameters (annealing temperature, time and ambient atmosphere)^{|2|}. Then the electrical conditions after partial crystallization are described^{|3|}. It is therefore tentatively proposed here that partial crystallization does not only lead to the commonly accepted higher impurity diffusion along grain boundaries, but that the current is also increased in this way.

The material generally used for these experiments was (100) orientated bulk single crystal Si doped GaAs ($n = 2 \times 10^{18} \text{ cm}^{-3}$). It was cleaved into samples approximately 5 mm x 3 mm which was cleaned in an ultrasonic cleaner using acetone, trichloroethylene, methanol and chloroform.

Native anodic oxide layers were produced on the samples by anodisation in an electrolyte consisting of tartaric acid in glycol with the pH of the solution being adjusted to 6.3 by the addition of ammonium hydroxide^{|4|}. The oxide layers were grown using several values of the initial current density ranging from 0.1 to 2.0 mA/cm², with the current density being changed by varying the resistance in series with the electrolytic cell, and a constant voltage supply.

The samples were annealed in a quartz tube furnace in an atmosphere of high purity nitrogen (oxygen free) and the furnace temperature was accurately controlled using an electronic temperature controller so that the heat cycle used was reproducible. Before the samples were heated, the furnace tube was flushed out with nitrogen to remove all the oxygen present and it was prevented from entering the furnace tube via the gas outlet by using a bubbler partially filled with glycerine. The sample is heated up to the required temperature (T) as quickly as possible, held at this temperature for 10 mins and then cooled down at a rate of either 300° C per hour or 100° C per min.

The structure of the bulk oxide was determined by X-ray diffraction where the samples were mounted on aluminium rods which were mounted on the specimen holder of a Philips X-ray diffractometer. A plot of X-ray count as a function of 2θ was obtained, where θ is the angle of incidence of the X-ray beam with the sample. A cleaned unprocessed sample of the above GaAs was analysed and the (200) and (400) reflections of GaAs, which also occurred in all the spectra of the oxidised samples, served as a calibration for each spectrum by determining the 2θ scale of the instrument to find the instrumental peak broadening factor. The radiation used here was $\text{Fe } K_{\alpha}$ ($\lambda = 1.938 \text{ \AA}$).

The structure of the surface of the oxide layer was determined using an AEI E.D 2 electron diffraction camera. From the diffraction patterns obtained the structure and orientation of the surfaces of

the samples were obtained. An SEM fitted with a microprobe analyser was used to examine the surface topography and, roughly the chemical composition of the oxide layers respectively.

To determine the chemical resistance of the various oxide layers they were etched in a 10 % solution (by volume) of hydrochloric acid for 5 minutes after which the etching was terminated by washing the samples in de-ionised water.

Initially a thin anodic oxide layer (approximately 50 Å thick) was grown on a GaAs sample using an initial current density of about 0.25 mA/cm². An examination of this sample using reflection electron diffraction showed that the surface was almost amorphous, its diffraction pattern consisted of several diffuse bands which are characteristic of amorphous native oxide layers on GaAs^[5].

Another anodic oxide layer, of 2000 Å thickness, was grown with a current density of 1 mA/cm² and etched in HCl fumes to remove all but the last 50 Å (approximately) of oxide whose structure was determined by electron diffraction. The diffraction pattern consisted then of dots arranged in rings which indicates that the material immediately adjacent to the GaAs surface is now polycrystalline. This is either due to the crystallisation of the thin layer nearest to the GaAs when a reasonably thick oxide layer is grown, or due to the action of the HCl fumes on the remaining oxide layer. The former explanation could also be understood in connection with the observed excess Ga^[6] or non-oxidized^[7] As found in such a layer as described below in chapter 3.

Several samples were grown by using an initial current density of 1 mA/cm^2 and annealed in either As or high purity hydrogen at 500°C for 30 mins. After annealing the samples were chemically analysed and found to have a Ga : As ratio of about 2 : 1 as compared with a ratio of approximately 2 : 1.5 before annealing; this change was coincident with a change of oxide thickness from 2000 \AA (pink) to 1500 \AA (green). Taking into account the penetration depth of the microprobe analyser this corresponds to a considerable loss of the As component of the oxide. Since the presence of the As atmosphere would inhibit the loss of As from the oxide and no significant As loss is expected from the GaAs at this temperature^{|8|} it can be concluded that the observed As loss is due to the outdiffusion of arsenic oxide. Those samples annealed in the high purity hydrogen atmosphere behaved in a very similar manner. By raising the annealing temperature to 600°C and using a high purity hydrogen atmosphere, the amorphous oxides were reduced to metallic Ga in agreement with a basic chemical understanding of the elements involved^{|9|}.

For the anodised samples grown with an initial current density of 2 mA/cm^2 the only peak present in the spectrum of the anodised sample which was not present in the spectrum of the cleaned GaAs sample occurred at $2\theta = 40.6^\circ$, which corresponds to $d = 2.816 \text{ \AA}$. It was possible to determine the position of this peak accurately since the 2θ values of these peaks were very similar (40.45 and 40.60) and these two peaks were of a comparable magnitude, due to the low intensity (< 1 %) of the (200) GaAs reflection and the small

amount of anodic oxide present. The peak which occurs at $2\theta = 40.6^\circ$ for the anodised samples corresponds to the (200) reflection of $\beta - \text{Ga}_2\text{O}_3$, i.e. the $\beta - \text{Ga}_2\text{O}_3$ is (100) orientated. This is the most likely orientation of the $\beta - \text{Ga}_2\text{O}_3$ since its lattice constants in the (100) plane are very similar to those for the (100) plane of GaAs, as was also seen by the 'd' spacings of the (200) reflections of $\beta - \text{Ga}_2\text{O}_3$ which are 2.816 \AA and 2.832 \AA respectively. Information on the change in the volume and crystallite size with annealing temperature for the crystalline $\beta - \text{Ga}_2\text{O}_3$ is presented in Figure 1. This data can be derived from the intensity and the width at half intensity of the measured peak respectively. The results show that the unannealed samples contained an appreciable amount of crystalline $\beta - \text{Ga}_2\text{O}_3$ only for high-current density growth and that the total amount of crystalline material did not increase significantly until it was annealed above 450° C .

As the peak width is inversely proportional to the average size of the crystallites in the oxide, one can see that the crystallite size decreases initially with increasing annealing temperature until 450° C was reached above which it increases rapidly. It has to be noted of course that some of the observed variations in peak width, especially the decrease with increasing annealing temperature, may be due to other factors such as strain and variations in the chemical composition of the sample. On the other hand, a real decrease in average crystallite size over a limited temperature range can be considered as an indication for a considerable formation rate of new single-crystal nucleating sites. At higher temperatures it would

become more difficult to form sufficiently stable clusters of molecules to become single-crystal nucleating sites. There, only existing crystallites would grow and thus increase the average crystallite size. Such an interpretation would indicate that high annealing temperatures can be applied without considerable crystallisation by going as rapidly as possible over the temperature range from 350°C to 450°C , both when applying and when removing the heat. Experiments, described below, do indeed give some confirmation for this understanding.

A small but significant increase in the background of the spectra around $2\theta = 86^{\circ} \pm 3^{\circ}$ ($d = 1.4 \text{ \AA}$) was found which indicates that there may be an unmeasurably small amount of some other orientations of $\beta - \text{Ga}_2\text{O}_3$ present in the sample.

An important annealing parameter, which was found to be relevant to the occurrence of crystallisation in the oxide was the cooling rate used at the end of the annealing cycle. Several samples were grown using a current density of 0.1 mA/cm^2 and were annealed at 600°C as above except that the cooling rate used here was 100°C per min. instead of 300°C per hour as above. The quickly cooled samples showed no crystallisation. Thus, by using a high cooling rate, the material does not have enough time to arrange itself in a crystalline form and is "frozen" in an amorphous type of structure.

The effect of the annealing time was also studied on the samples which were found to be crystalline immediately after growth, i.e. those grown with a current density of 2 mA/m^2 . By varying the annealing time from 10 to 60 mins at a temperature of 600°C it was found that the average crystallite size increased with increasing the annealing time, see Fig. 2, with no significant change in the total volume of the crystalline $\beta - \text{Ga}_2\text{O}_3$. This can be considered to be due to the movement and coalescence of individual crystallites produced initially at lower temperatures.

All of the above results neglect the effects of the absorption of the X-rays in the amorphous oxide layers. An estimate of the average crystallite size of the $\beta - \text{Ga}_2\text{O}_3$, for a peak width at half height of 0.05° , gives a value of $\sim 150 \text{ \AA}$.

An analysis of the electron diffraction patterns produced by the samples grown with initial current densities of between 2.0 and 0.1 mA/cm^2 shows that the surfaces of all of the unannealed oxides are amorphous. However, after annealing in connection with the fabrication of Au Ge ohmic contacts on the back face of the sample, the surfaces of the oxides became slightly ordered and produced diffraction patterns which consisted of several very diffuse rings.

After annealing the samples grown using the above current densities and cooling the samples at a rate of 300°C per hour an analysis of the electron diffraction patterns showed that the

surface crystallised out into a polycrystalline β - Ga_2O_3 structure, with only the rings corresponding to the (h.o.l) reflections present. As the annealing temperature was raised the rings of the diffraction patterns became sharper, indicating an increase in the average crystallite size. Another effect which was observed at high annealing temperatures, especially for samples grown using a current density of 2 mA/cm^2 , was that the only rings corresponding to the (1.0.1) reflections were visible indicating that this structure had become more orientated. However, after annealing at 800°C it produced a pattern consisting of spots and rings showing that some crystals of β - Ga_2O_3 were produced. The crystallite size was found to be a function of the growth current density, the larger crystallite size being present in the samples grown with a higher current density, as was found by X-ray diffraction.

By using the annealing process with the fast cooling rate of 100°C per min even the sample annealed at 700°C for 10 mins. was found to remain almost amorphous in contrast to samples annealed at even as low as 500°C but cooled down at a very slow rate.

Thus the crystallisation at the surface of the oxide as studied by electron diffraction is much less pronounced than that at the interface. From a knowledge of the electron beam penetration and the approximate angle of incidence of the beam with the sample, the depth of the analysed material can in fact be estimated to be about 50 \AA . This surface crystallisation is of course grown in an

amorphous bed of oxide as opposed to any interfacial crystallisation, which is likely the crystallisation detected by X-ray diffraction.

The SEM shows all the sample surfaces to be extremely flat with the exception of a very occasional defect, which can be thought to be due to some contamination of the sample surface, except for samples, annealed at or above 800° C, when the micrograph of the surface shows the presence of quite large crystallites.

The variation of the overall As : Ga ratio can conveniently be assessed by microprobe analysis. The results as a function of annealing temperature show that there is a significant loss of the As component of the oxide between 400 and 500° C. This As loss coincides with a change in colour of the oxide for example from blue to purple which shows a change in the oxide thickness from 1000 \AA to about 850 \AA . Since no such As loss is known to occur in GaAs this change must come from the oxide and it is thought to be due to the loss of arsenic oxide, due to the high vapour-pressure of As_2O_3 at relatively low temperatures.

A comparison of the results of the X-ray and the electron diffraction experiments suggests that the predominant crystallisation process occurs at the GaAs-oxide interface with a secondary crystallisation process occurring at the oxide surface. This can be seen from the highly orientated nature of the interface oxide as compared to that on the surface as well as for the degree of order and the volume of the crystallisation, both of which are greater for

the interfacial process. The volume of the surface crystallisation is much less than that of the interfacial case since only the latter shows up on the X-ray spectra. These two crystallisation processes can be considered to be independent of each other since the orientation of the two crystallised layers is different.

It is useful to compare the structural results with the electrical behaviour of the oxide. For this purpose Al dots were evaporated onto the oxide after annealing. The capacitance against applied voltage and the DC conductivity were then measured. In special cases a wide range of RF and DC current measurements were taken to provide details for annealed samples under optimum conditions and figure 3 shows some typical results.

The C-V curves are given for $f = 1$ kHz. It should be mentioned that the curves were measured with an automatic C-V plotter. The dielectric constant of the oxide was found to be $\epsilon_r = 7.8$. The DC conductance was obtained by a Keithley 602 Electrometer. The I-V curves obtained had principally a transient characteristic (even for the high currents in the high-temperature-annealed samples). Thus hysteresis effects appear which of course in shape depend on the 'average ramp speed' corresponding to the hysteresis effects seen in the C-V curves. The I-V curves show average leakage currents, provided after the sample was kept for 30 min at its maximum stress bias but then measured point-by-point rather quickly. (On figure 3(c) the small hysteresis in C for the 300° C annealed samples and the

deep depletion should be noted.) Unfortunately, the DC conductivity has deteriorated slightly (compare figures 3b and 3d) and is in particular highest in the inversion region.

The DC conductivity increases exponentially with annealing temperature and reaches the μA ranges per cm^2 at 700°C for a gate bias of + 15 V, corresponding to an average field of $1.5 \times 10^6 \text{ V cm}^{-1}$ in the oxide. It seems that slowly cooled samples are less stable and show a higher current density. This might indicate how important it is for the oxides to remain fully amorphous.

To quantify this behaviour figure 4 shows a summary of the hysteresis amplitudes at a capacitance corresponding to the midpoint of the range between capacitance maximum around 60 pF (which looks like accumulation, is however likely to be more complex as shown below, at the end of Chapter 5) and the flat level around 30 pF (looking like inversion) and the DC current of one set of samples both as a function of annealing temperature. It can be concluded that the onset of some crystallization and the loss of As in the oxide seems to be associated with an increased DC conductivity.

3. Chemical Analysis

Using ESCA, it has been demonstrated^{|7|} that, by ion etching the oxide away from its top surface, one first finds the transition from As_2O_3 to non-oxidised As, and, only several etch minutes later, the transition from Ga_2O_3 to GaAs. This behaviour is not modified by any of the low-temperature annealing processes normally applied to GaAs MOS samples in order to achieve an improved capacitance-voltage behaviour. Laser annealing of GaAs MOS structures seem to have shown that the As_2O_3 - As transition can be made to go nearer to the oxide surface whereas the Ga_2O_3 - Ga interface moves simultaneously further into the GaAs. It would mean that the provision of sufficient energy causes a transfer of oxygen to take place from As_2O_3 to any non-oxidised Ga or to Ga in GaAs.

R.P.H. Chang reported^{|10|} for plasma oxidised GaAs that this non-oxidised As layer can be seen at the interface as a clear band when a thin slice transverse to the MOS surface is analysed by TEM. After the normal heat treatment of the MOS sample, this band seems to break up and forms elliptical islands. Aligning the electron-beam to obtain diffraction patterns can then be used to show that these islands are formed of crystalline As.

The conclusion of these results is surely, that the problem of GaAs passivation is caused primarily by the difference in oxidation rates for Ga and As.

Preliminary results^{|11|} show that a two step oxidation of the following procedure avoids the band of non-oxidised As and seems to give improved data : A thin layer of native oxide is first electrolytically grown into GaAs. This is then heated in hydrogen atmosphere to a sufficiently high temperature so that all As_2O_3 evaporates without, however, affecting the GaAs, and so that most of the Ga_2O_3 is transformed into Ga and H_2O (which evaporates)^{|9|}. A layer of Al is now evaporated on the remaining Ga + Ga_2O_3 film and electrolytically oxidised. This oxidation is pursued into the original Ga_2O_3 layer without, however, going into the GaAs. The resulting capacitance-voltage behaviour of such films is discussed at the end of Chapter 5.

Structural information on the composition of such thin films can be obtained by Auger electron spectroscopy (AES)^{|12|} and X-ray photoelectron spectroscopy^{|13|} (ESCA), when combined with a suitable etching technique. It seems that ESCA offers sometimes advantages over AES due to the possibility of stronger chemical shift data which is more easily obtained and also interpreted with the former^{|13|}. However, AES does have the advantage of speed and of being able to examine different parts of a single sample, so that a combination of both techniques where available offers the best solution.

GaAs samples were oxidised by using one of the following two electrolytes

(i) 3 % tartaric acid solution mixed in the volume ratio
1 : 2 with propan 1, 2 diol (AGW) | 4 |.

(ii) 0.02 M $(\text{NH}_4) \text{H}_2\text{PO}_4$ solution mixed in the volume ratio
1 : 2 with propan 1, 2 diol.

Anodisation was carried out under constant current conditions.

ESCA spectra thus obtained | 14 | were recorded on an A.E.I. E.S. 200 B spectrometer at typical chamber pressures of 2×10^{-8} Torr, utilising Mg $K_{\alpha 1}$ $K_{\alpha 2}$ radiation at 1253.6 e.V. They were recorded at 0.1 V sec^{-1} (Ga and As 3d peaks) and 0.05 V sec^{-1} (Al 2p and O1s regions). Both analogue and digital spectra were recorded simultaneously, the sampling rate for the latter being 50 times per minute.

Ar-ion milling was carried out using an ION-TECH saddle field ion source fitted with a scanning facility. The source has a beam of height 1 cm and this was scanned along the length of the sample, at a mean angle of 45° to the sample surface. Argon was 99.996 % purity (B.O.C.). The source was operated at either 8 kV 3 mA or 5 kV 2 mA. Approximate etch rates were 25 \AA per minute in the former and 6 \AA per minute in the latter case. These etch rates were estimated from depth profiles obtained from oxide films of known thickness.

Figure 5 - 8 show the profiles obtained from native oxide films grown on GaAs in the AGW electrolyte. The surface region is often As rich as compared to the bulk. (The first point in all these profiles is unrepresentative due to surface contamination and should be ignored.) The other features of these profiles are very similar to those already discussed. The bulk of the film is uniform with an As/Ga ratio of about 0.5. There is a slightly Ga_2O_3 rich region adjacent to the substrate and the As profile of the GaAs substrate indicates the probable presence of elemental As at the interface. The interface width obtained from the oxygen profile was 60 Å. (The sample was etched at 5 kV.)

4. Some Technological Recipes

In silicon technology, surface passivation is usually achieved by thermal oxidation. However, this method is not directly applicable to most compound semiconductors such as GaAs, due to the high vapour pressure of the volatile components (e.g. As). On the other hand anodic oxidation in both wet electrolytes as well as gas plasmas is a low temperature process and can be used as an alternative method to thermal oxidation. Wet anodic oxidation of GaAs is possible in a variety of electrolytes producing uniform and reproducible native oxides.

A simple cell used for the anodisation of the GaAs essentially consists of a GaAs anode and an Al or Pt cathode both immersed in a suitable electrolyte. A schematic drawing of a convenient cell is shown in Figure 9. A slow stirring of the electrolyte is achieved by a teflon encapsulated magnetic stirrer. The current is supplied to the cell by means of a high voltage supply (0 - 2100 V) with a very high resistor connected in series. The current supplied to the cell is measured with an ammeter connected in series, and the potential difference between the anode and the cathode is measured with a suitable calibrated x-t recorder connected in parallel with the cell.

The potential difference between the anode and the cathode consists of the following parts, namely potential drop between the cathode and the electrolyte, across the electrolyte, the oxide, and the GaAs anode. The first two of these potential drops are generally

very small (≈ 0.5 V) except when very high current densities are used. The voltage across the oxide is proportional to its thickness up to a limited value. This thickness limit is a property of the electrolyte used. Below this limit the potential developed across the oxide can be employed to estimate the thickness of the oxide grown. The potential drop at the anode itself consists of four parts,

- (a) the potential drop at the electrolyte - anode interface,
- (b) the potential drop across the space - charge layer in the GaAs,
- (c) the potential drop in the bulk of the GaAs due to its bulk resistivity which is a function of its doping concentration, and
- (d) the potential drop at the back ohmic contact.

All the abovementioned potential steps in the cell (except that one across the oxide) appear as an initial rise in the overpotential - time ($V - t$) curves. As the oxide grows under constant current conditions the $V - t$ curve increases linearly and by subtracting the initial rise from the final voltage, the potential across the oxide can be determined and used to estimate its thickness as suggested earlier.

The surface condition of the GaAs anode is of major importance in obtaining uniform and reproducible oxides by anodisation. A great deal of attention should be paid to the sample preparation and the techniques for maximum reproducibility.

The GaAs slices are usually in the form of 300 - 500 μm thick wafers, generally with one side polished. All wafers have to be solvent cleaned* and stored in dessicators containing silica gel.

Metallic ohmic contacts are produced on the unpolished side of the wafers by vapour deposition and subsequent annealing. For this purpose all wafers are stuck, polished side down, on a thin pre-cleaned glass substrate with Shipley 135 OH photoresist to reduce the risk of damage during handling. After removing about 1 μm of the surface of the wafers with a pre-evaporation etch**, the ohmic contact metals are deposited by evaporation on the etched surface from heated tungsten filaments at a residual pressure of at least 10^{-6} torr in a conventional evaporator. The ohmic contact metals are typically 2000 \AA 88 % Au - 12 % Ge alloy for n-type, and 200 \AA In + 2000 \AA Ag for p-type GaAs. Following the evaporation, the wafers are removed from the glass substrate by dissolving the photoresist in acetone. A second solvent cleaning removes all traces of photoresist.

**Pre-evaporation etchant:

A - 4 % H_2O_2 by volume, B - 2 % NaOH by weight, A : B = 1 : 1.

This etchant give an etch rate of $\sim 1000 \text{\AA}/\text{minute}$ at room temperature.

* Solvent Clean:

A 5 minute boil followed by a 5 minute of ultrasonic cleaning in the following solvents in turn:

- | | |
|----------------|------------------------|
| (i) Acetone | (ii) Trichloroethelene |
| (iii) Methanol | (iv) Chloroform |

The annealing of the ohmic contacts is done in a N_2 purged, closed-end, quartz furnace, The annealing temperature and time is chosen according to the type of GaAs. For n-type a 2 second annealing at $465^\circ C$ with $300^\circ C/min.$ heating and cooling rates, for p-type GaAs a 2 minute annealing at $600^\circ C$ with $100^\circ C/min.$ heating and cooling rates is usually found to produce the best results. It must also be mentioned that the use of an unpolished surface can be found to improve the ohmic contact properties.

5. MOS-Device Results

III - V compound semiconductors are to be employed wherever they are superior to Si or have facilities which are not available with Si. This means that a substantial interest exists in using them for optical applications. An interesting example was developed by workers at the Eastman Kodak Company^[15], where GaAsP photosensors are fabricated with anodically grown native oxides.

The other important applications area is microwave or giga-pulse rate devices because the electron saturation velocity and low-field mobility can be very high in many of these compound materials. GaAs Schottky-gate FETs are of course already very mature. Important requirements are, however, still a suitable passivation for the free GaAs surfaces between source, drain and gate, and the oxidation technology for achieving more easily submicron gate width with little alignment difficulties.

A major interest is the development of MOSFETs in GaAs. The gate of such a transistor can be forward biased without any danger of damage as would be the case with MESFETs. This feature is of advantage for large-signal operation with substantial input power applied to the gate. One would be able to operate FET amplifiers without any bias supply provided for the gate - a possible circuit advantage. The Fujitsu Laboratories in Japan have found^[16] that the MESFET of the same electrode geometry appears to have a larger parasitic capacitance C_{gs} between gate and source than the MOSFET. C_{gs} is dependent on the fringing edge capacitance of the gate strip and is

for MOSFETs, more like a plane-parallel capacitor without significant edge effects than it is for MESFETs. It is then argued^{| 16|} that the intrinsic current-gain cut-off frequency f_T can be potentially made considerably larger for MOSFETs than for Schottky-gate transistors, by reducing the gate length without being affected by the gate-fringing capacitance.

With these potential advantages in mind, several depletion and enhancement type GaAs MOSFETs have been fabricated by various laboratories. Perhaps the most advanced results have been reported from Japan^{| 16,17|}. 2μ long gates have shown unilateral power gain over the 2 - 8 GHz frequency range. An enhancement device exhibited a maximum frequency of oscillation at 13 GHz. A depletion device of 1.8μ gate length gave a maximum frequency of oscillation of 22 GHz. The intrinsic current-gain cut-off frequency for the depletion MOSFET is 4.5 GHz. This type of transistor produced 0.4 W output power at 6.5 GHz as a Class A amplifier.

By using a two-layer system on a semi-insulating substrate, namely a thin 0.25μ thick, $2 \times 10^{17} \text{ cm}^{-3}$ n-layer under a 1.5μ $5 \times 10^{14} \text{ cm}^{-3}$ n-layer covered by native oxide, an improved enhancement-mode FET was produced^{| 17|} showing good saturation characteristics and operating entirely in the enhancement mode. The S parameter measurements covering a frequency range of 2 - 12 GHz show that, although the gate length is only 1.5μ short, the unilateral gain U decreases with somewhat more than -6 db/Octave from about 11 db or 13 db power gain at 2 GHz - quite an impressive performance.

The difficulty with these otherwise very impressive devices is a strong charging effect both into traps at the interface and in the bulk of the oxide as described above. This manifests itself firstly as a drift in operating point of a transistor amplifier over the first seconds after switching on of the bias voltage. Then, a large frequency dispersion is observed, particularly with enhancement MOSFETs, at the lower frequency ranges between 10 and 100 kHz. Unfortunately, these effects are particularly serious for pulsed-signal operation as required for logic integration, where MOSFETs would in fact be particularly advantageous.

It seems that these problems can be avoided with InP by employing high-quality non-native oxides. The peculiarity of this semiconductor is the absence of any charge trapping effects at or near the interface with the oxide. Very noteworthy are here MISFETs produced by depositing organic insulators on InP^[18]. These insulating films are the Langmuir-Blodgett type of amphipathic molecules deposited first on a water surface and subsequently transferred to single crystal InP surface by dipping this and raising it through the air-water interface. A single monolayer is then transferred on to the InP substrate during each transversal of the water surface. The organic molecules used have a hydrophobic carbon tail and a hydrophilic polar head. Typical molecular size is 2.5 nm for stearic acid (C₁₇H₃₅ COOH) and 2.75 nm for arachidic acid (C₁₉H₃₅ COOH). The Langmuir-Blodgett films can be built up to a thickness of 1 μ. Cadmium arachidate shows improved adhesion properties. The gate metallisation used was Au + Cr or Al. Using the Nicollian-Goetzberger conductance method, a surface state density of $N_2 = 2.3 \times 10^{11} \text{ cm}^{-2} (\text{eV})^{-1}$ is found.

With a reduced interface trapping process for InP MIS structures, it can be expected that the microwave transistors produced with this material would exhibit better performance than GaAs devices at the lower frequency ranges as the traps would not be effective at microwave frequencies. This has indeed been found^{|19|}: both the output characteristics and the power gain of GaAs and InP FETs are similar at microwave frequencies. However, whereas the gain G_m of GaAs transistors is decreasing for the upper kHz frequency ranges, this is much less marked for InP devices.

The facility of fabricating multi-layer dielectric structures by anodic oxidation of suitably metallised GaAs surfaces, lead to long-term charge storage transistors^{|20|}. They operate in a similar manner as Si MNOSFETs where N is Si_3N_4 , except that it can be expected that trap charging occurs via Poole-Frenkel conduction across the native GaAs oxide which has a lower energy gap than the covering Al_2O_3 . Therefore native-oxide thicknesses above the tunnelling distance can be used when it was found that the discharging times for zero bias are substantially longer^{|21|} than with the corresponding Si N-O interface where the SiO_2 cannot be larger than 50 \AA . The increased charge retention facility of GaAs MAOSFETs was also found for transistors with a thin metallic film between the Al_2O_3 and the native GaAs oxide, so called MAMOSFETs.

Another area, where GaAs MOS structures have recently shown interesting behaviour, is the observation of light emission from diodes with oxide thicknesses up to around 200 \AA ^{|22|}. The devices

have to be biased then in the reverse direction, when minority carriers are formed in an inversion layer at the interface. They are injected into the oxide, at the same time when majority-type carriers are injected from the metal into the oxide towards the GaAs. The spectrum of the emitted light contains a substantial amount of energy close to and above the GaAs energy gap, indicating that radiative recombination processes occur at the interface in the GaAs. However, a large part of the emission spectrum is well above the GaAs forbidden-gap energy. The shape of this high-energy part of the spectrum does not change with increasing bias voltage, only the intensity of emission is growing. This seems to be an indication that light emission from the amorphous oxide occurs, although it is also possible that recombination radiation due to hot charge carriers in the GaAs occurs.

This emission effect deserves further studies. So far suitable devices have been found emitting light continuously with dc for many months without any apparent depreciation..

Pulsed-bias operated GaP MOS devices with wet anodic oxides^{|23|} have shown red-light emission due to recombination of the inversion charge due to avalanching with the returning majority charge, when each bias pulse is terminated.

6. Conclusions

Although interesting device results have been reported, it is particularly necessary to find ways of reducing the strong charge trapping at and near the interface between GaAs and the covering insulator and to avoid the interface layer of the non-oxidised component which oxidises less easily, such as As in GaAs. Present-day understanding suggests that the difficulty is primarily associated with this elemental non-oxidised component at the interface. Promising new observations indicate that a combination of a suitable non-native oxide with a thin intermediate Ga/Ga₂O₃ layer is a strong contender for improved GaAs passivation. Unfortunately, it is still too early to report on inversion-layer GaAs MOSFETs, which would be a clear indication that the passivation of GaAs has been solved, but a considerable amount of progress has already been made and it is hopeful that such good results can be achieved if the present-day effort is maintained or even enlarged.

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Figure Captions

Fig. 1 The variation of the X-ray intensity and peak width (x) at half height for the (200) reflection of β -Ga₂O₃ with annealing temperature for the samples grown with a current density of (a) 2.0 mA/cm², (b) 1.0 mA/cm² and (c) 0.1 mA/cm².

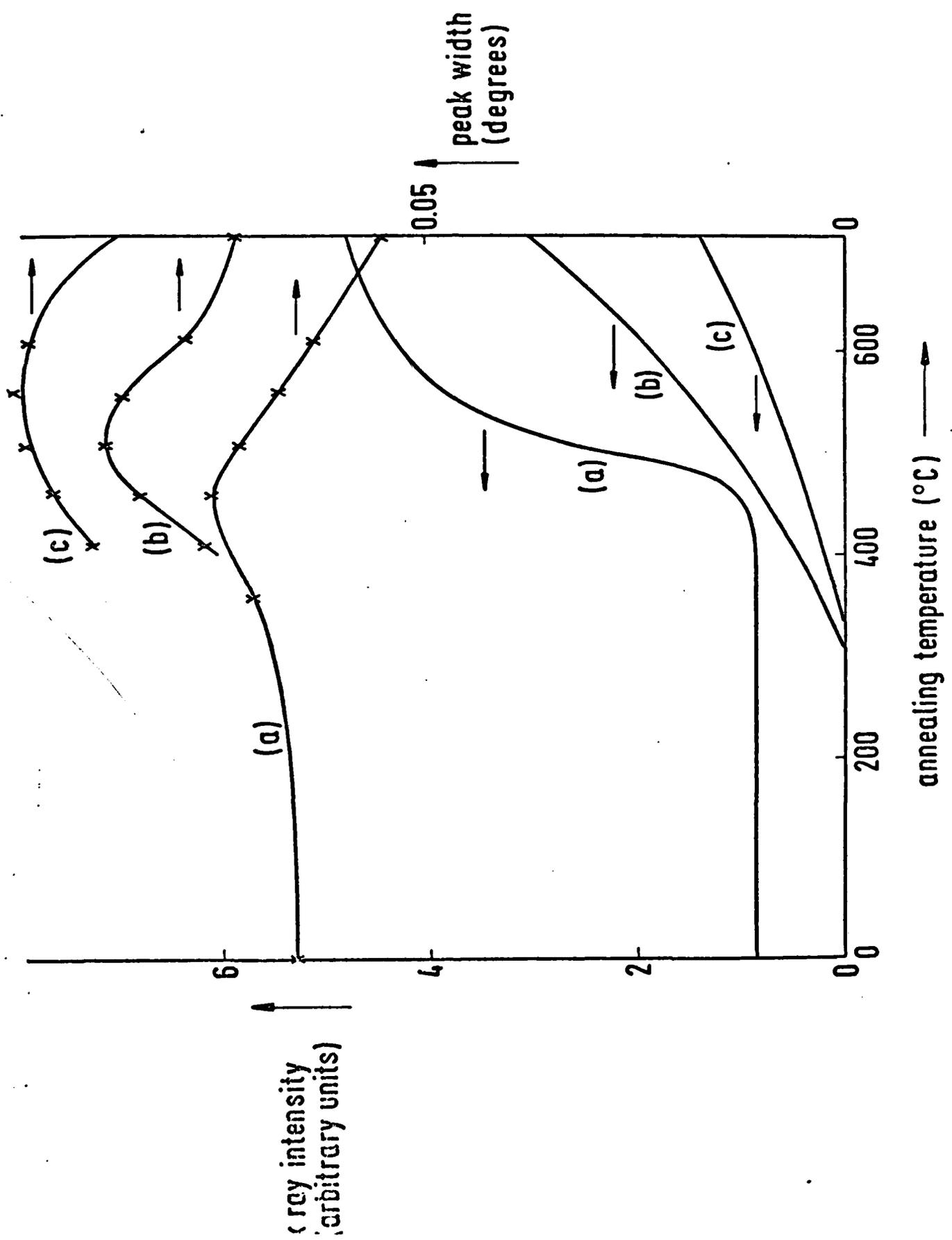
Fig. 2 The variation of the peak width at half height for the (200) reflection of β -Ga₂O₃ with annealing time at 600° C for sample grown with a current density of 2.0 mA/cm².

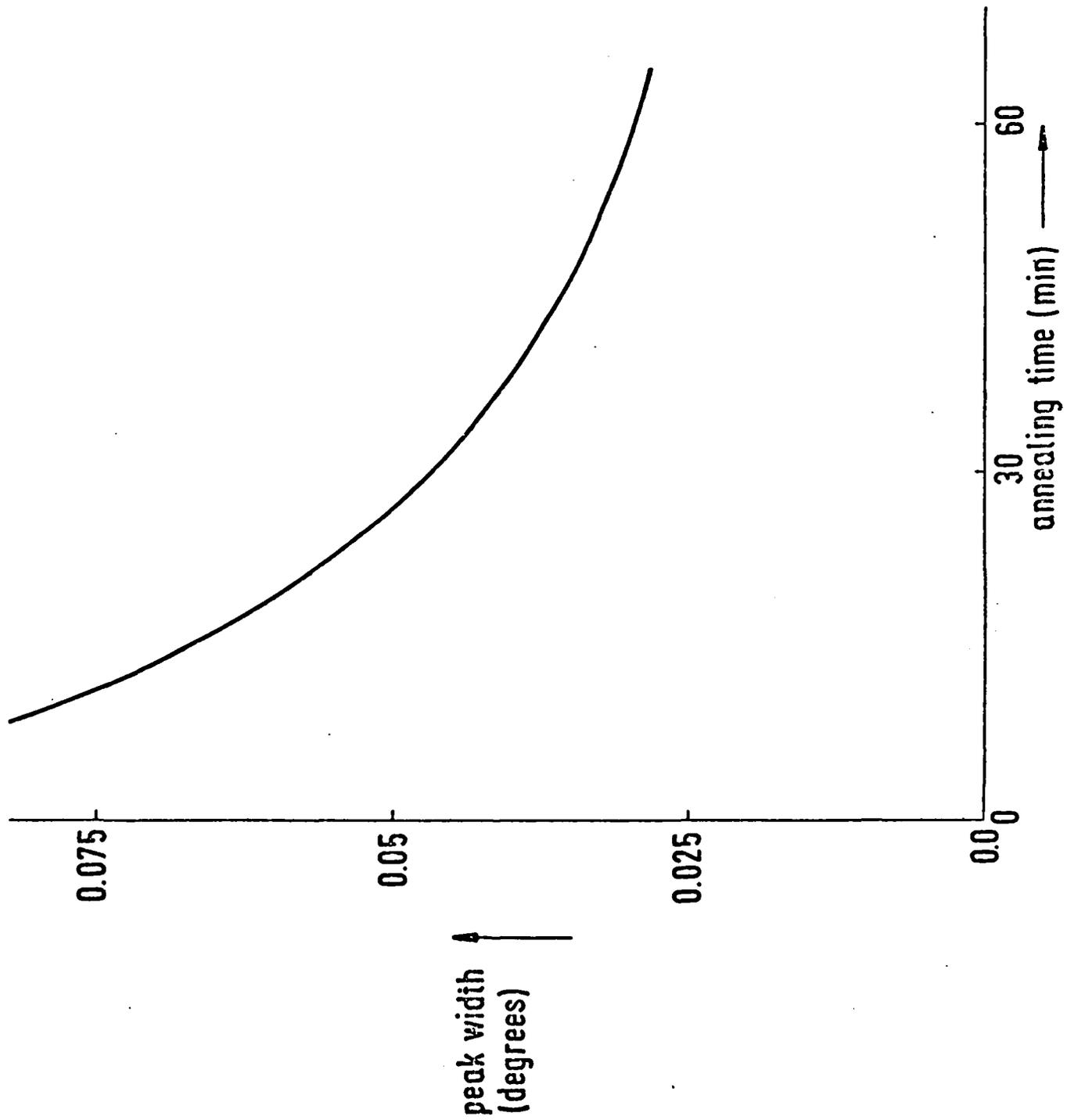
Fig. 3 Capacitance (C) and corresponding DC current (I) against voltage V_g applied to the Al electrode of MOS diodes for various annealing temperatures; (a), (b), unannealed; (c), (d) 300° C; (e), (f) 700° C. - and + refer to the polarity of V_g . Arrows indicate the direction of V_g change when a curve is plotted, oxide thickness = 1000 Å, area = 10⁻³ cm², ramp speed for C - V plot = 5 V s⁻¹.

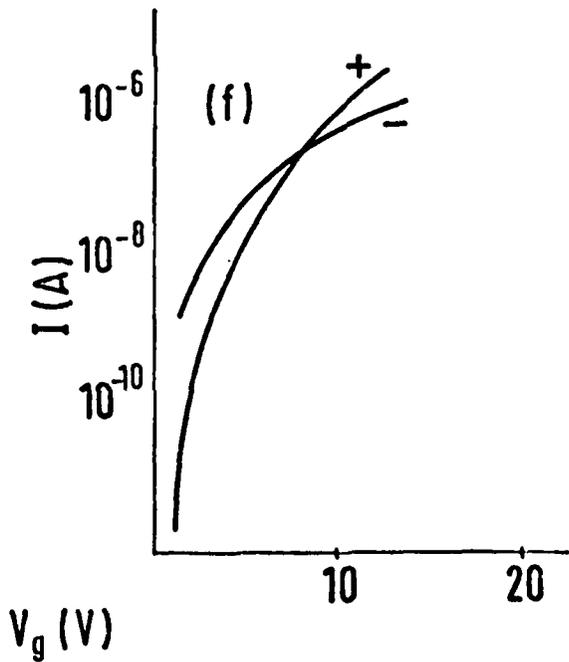
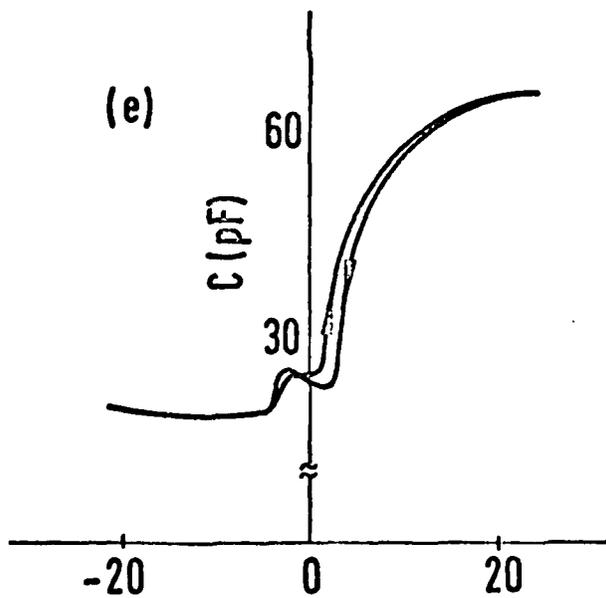
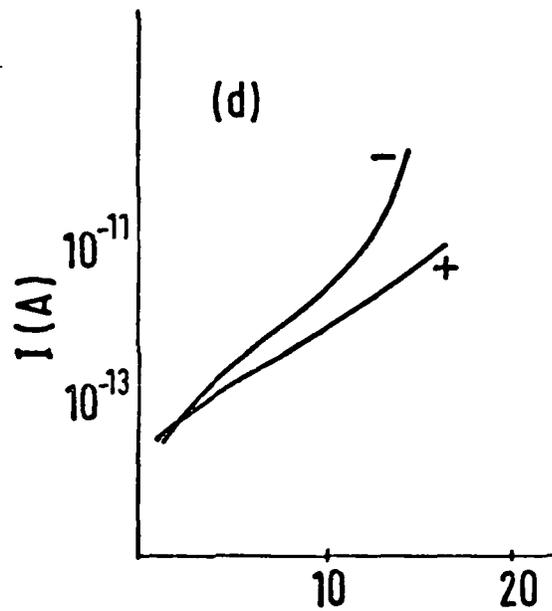
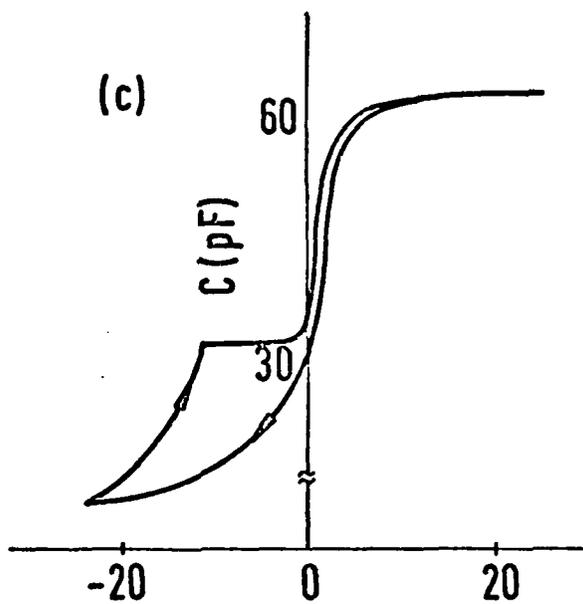
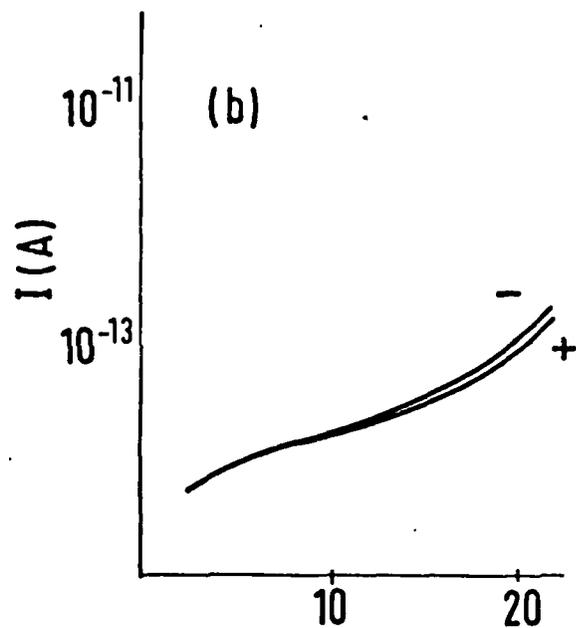
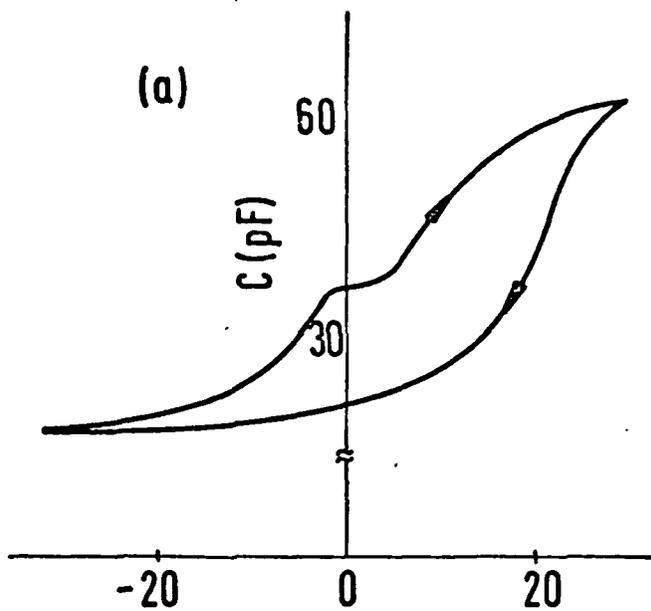
Fig. 4 The hysteresis of the C - V curves and the DC current I (see text) against annealing temperature used. $f = 1$ kHz, $V_{\text{stress}} = 20$ V, ramp speed = 15 V s⁻¹. • p-type; o n-type.

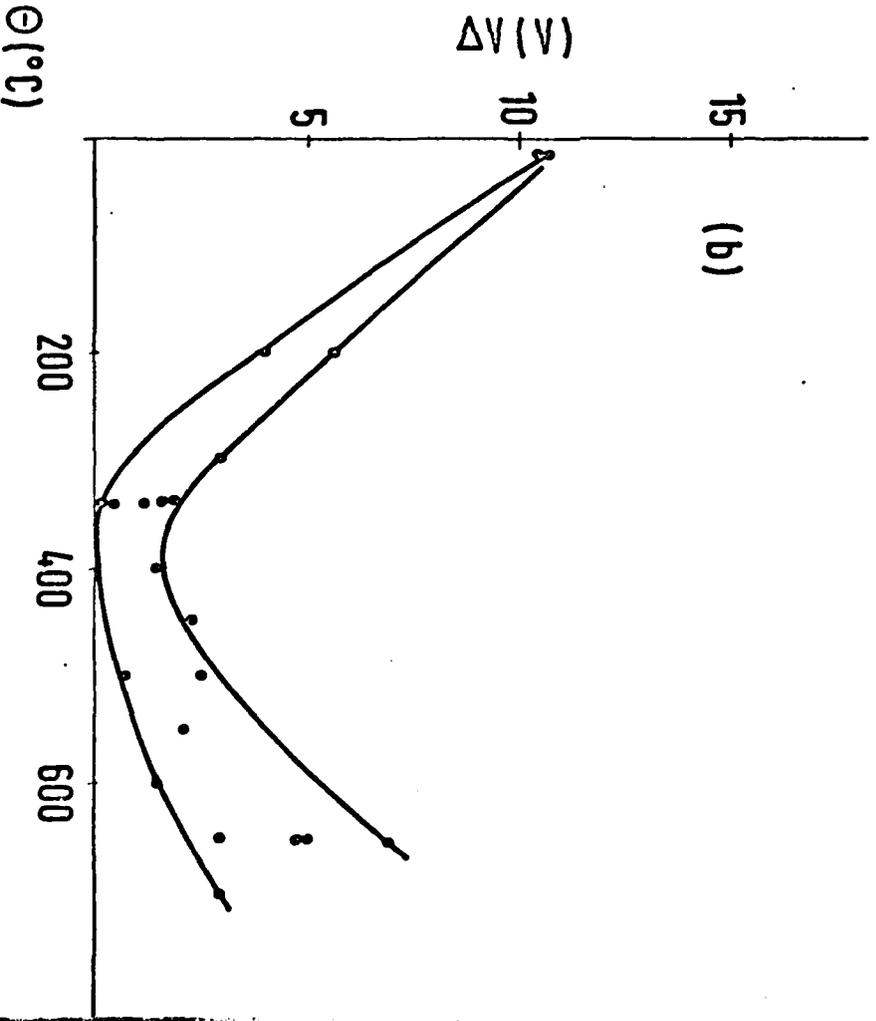
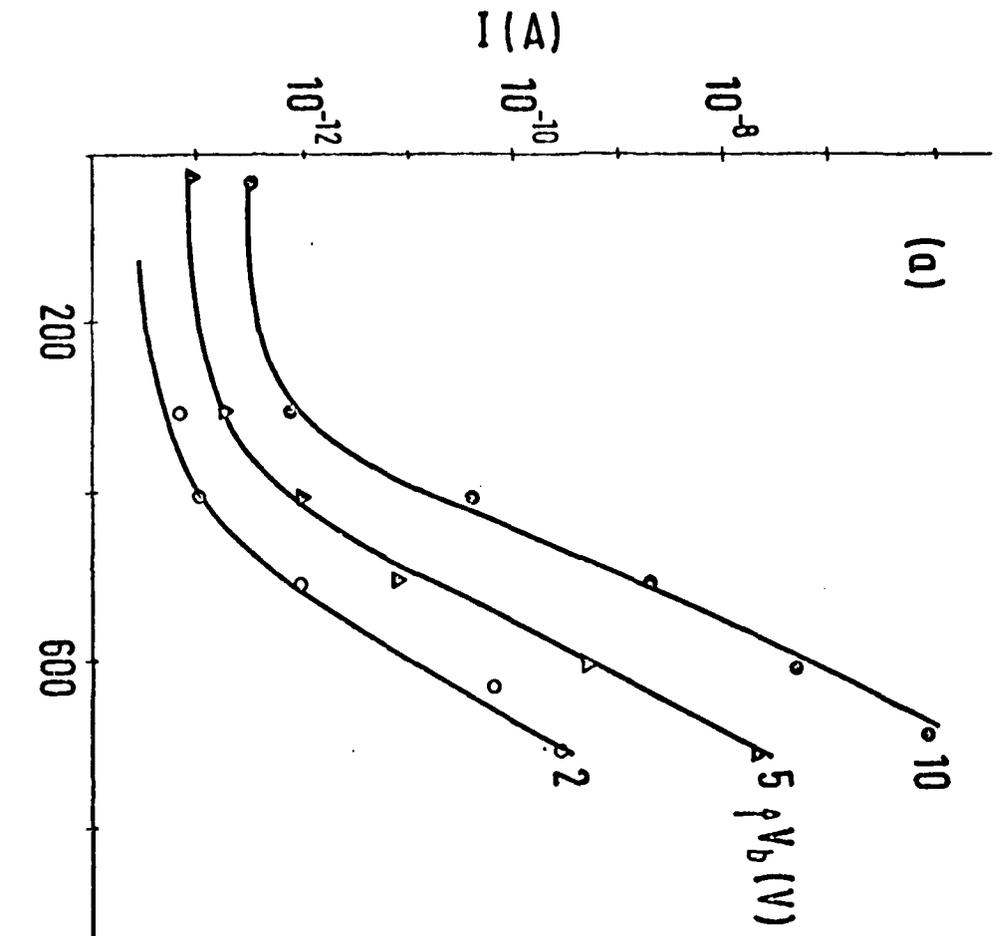
Fig. 5-8 Depth profiles of Ga and As 3d E.S.C.A. intensities

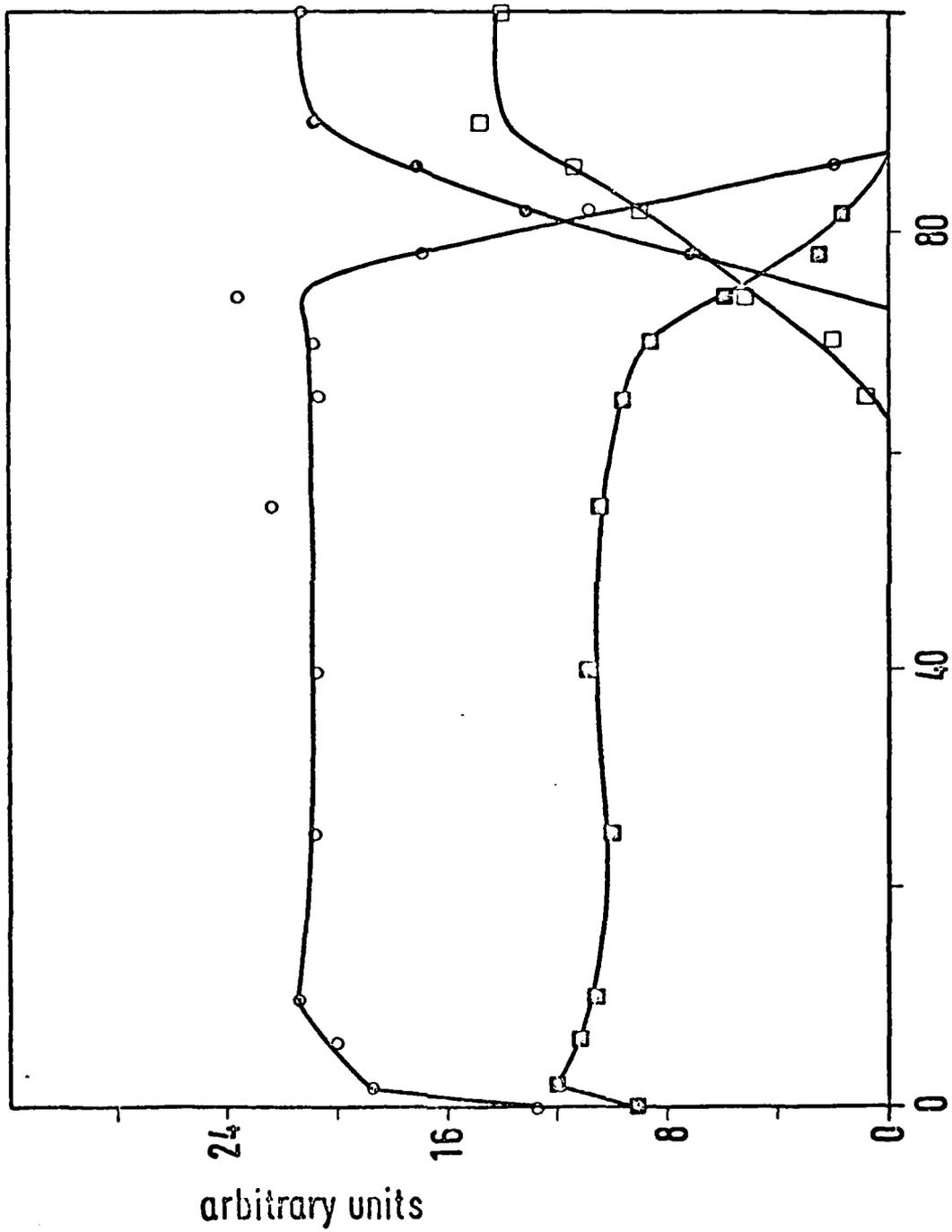
(in Fig. 7: o Ga in Ga₂O₃ o Ga in GaAs
 ▣ As in As₂O₃ ▣ As in GaAs)











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Microwave Characterisation and Performance of GaAs MOSFETs

D. Pavlidis

H.L. Hartnagel

Abstract

GaAs MOSFETs fabricated with anodically grown oxide gates in n-type epitaxial layer on semi-insulating substrates were tested at both low and high frequencies in order to evaluate their characteristics and prove their microwave capabilities. A maximum oscillation frequency of 4.8 GHz has been obtained with a 5 μm long gate structure. The device showed power gains (MAG) of the order of 14 db at 2 GHz and appreciable frequency dispersion of transconductance below 800 Hz.

I. Introduction

Although Si-MOS technology has already reached a mature stage, GaAs and related III - V compounds are well behind in this field due to the numerous difficulties involved with the passivation of their surfaces. Anodic^[1], Plasma^[2] and Nitride based^[3] passivation techniques have not yet resulted in satisfactory interface state characteristics and the formation of an inversion layer on the semiconductor surface has first to be confirmed before full advantage of the material properties in device applications can be taken.

The techniques developed until now for forming the insulator layers have primarily been applied in order to produce enhancement/depletion mode MOSFETs^[4,5] and thus show the advantage of using a gate insulator in order to protect a FET from positive voltage excursions, which in the case of Schottky gate transistors can be detrimental. Furthermore, due to the reduction of gate fringing capacitance in MOSFET's, a higher maximum oscillation frequency can be obtained than with similar MESFET structures^[6].

The results reported here concern the electrical properties of anodically made (AGW process^[1]) n-channel GaAs MOSFETs. Low frequency and microwave tests were undertaken in order to fully characterize the devices and prove their feasibility for microwave operation.

II. Device Structure

The devices were made on n-type, S doped VPE layers having thickness between 0.7 and 1.5 μm , mobilities around $4400 \text{ cm}^{-2} \text{ V}^{-1} \text{ sec}^{-1}$ and carrier concentrations of the order of 10^{17} cm^{-3} . The epitaxial layers were grown on Cr-doped semi-insulating substrates with a resistivity larger than $10^7 \Omega\text{cm}$.

A glycol-tartaric acid based aqueous solution was used in order to anodically oxidise the gate notch after the source and drain ohmic contacts were formed. The device was completed with conventional photolithographic and lift-off techniques^[4] and had 5 μm to 10 μm long, 300 μm wide gate strips. The gate to source (or drain) length was 10 μm and the channel depth underneath the oxide layer was of the order of 1000 \AA .

III. Low Frequency Electrical Characterisation

Low frequency tests were undertaken before mounting the devices in order to evaluate some of their characteristic parameters and assure proper operation. The output-drain characteristics were displayed on a Tektronix curve tracer and the drain saturation current (I_{dsat}) at zero gate voltage ($V_G = 0$) was measured to be of the order of 25 to 50 mA. A voltage of -3 to -4 Volts had to be applied to the gate of the tested devices in order to reduce the drain saturation current to at least 7 % of its maximum value, while pinch-off was sometimes impossible under weak illumination conditions.

The source and drain contact resistances R_S and R_D were estimated to be about 40 Ω each by measuring the drain resistance at the origin of the $I_D \rightarrow V_{\text{ds}}$ curve. Here, the assumption of $R_S = R_D$ was made due to the symmetrical device properties, allowing almost identical operation when the drain and source terminals were interchanged. The gate parasitic resistance R_g is a function of the gate geometry and metallisation technique employed. Evaporated aluminium was used in order to form the gate contacts of the tested devices and R_g was estimated to be of the order of 3 Ω .

The MOSFET transconductance g_{m0} was measured from the $I_D \rightarrow V_{\text{ds}}$ characteristic to be in the best case as high as 7.2 mS, while an increase of gate voltage by 2 V was found to reduce g_{m0} by at least 15 %. These data demonstrate reasonably high transconductance per unit gate length values in the range of 36 mS/mm.

Finally the magnitude of intrinsic output conductance G_{ds} was estimated by measuring the drain to source external conductance from the $I_D \rightarrow V_{\text{ds}}$ characteristics. By considering the already evaluated R_S and g_{m0} values, it was found that $G_{\text{ds}} = 2.8$ mS.

IV. Microwave Device Characteristics

The equivalent circuit of a GaAs MOSFET is shown in Fig. 1. Its derivation is based upon simple lumped modelling considerations for MOS Field-Effect-Transistors^[7] and is valid in a limited frequency range only. Some of its parameters, namely R_S , R_D , R_g , G_{ds} and g_{m0} can be evaluated by low frequency measurements as described in Section III. Others, however, such as C_{gs} , C_{dg} , R_{gs} and g_{m} need previous microwave characterisation of the device in order to be calculated.

A special test fixture with 50 Ω microstrip lines on alumina substrates was fabricated and the transistors were mounted on an adjustable ground stab as shown in Fig. 2. Pressure contacts to the device were achieved by gold springs for easy removal. The devices were all tested in the common source configuration.

First the MOSFET small signal S-parameters were measured with an HP 8410 A Network Analyser combined with an automatic S-parameter test-set (HP 8745 A). The latter instrument provides the facility for internal transistor biasing in the 0.1 to 2.0 GHz frequency range. The internal losses of the test circuit were taken into consideration by carefully calibrating it with a small GaAs slice inserted in the place where the transistor was subsequently mounted. The upper and lower surfaces of the calibration standard were both metallised with a Au/Ge alloy and contact to the upper face was made only with the gate and drain springs. The source spring was left to contact a bare section of the same semiconductor surface since its other end provided a dc return by connection to an adjustable-length short terminated line. A typical set of measured S-parameters is given in Fig. 3. The transfer parameter S_{12} describing the reverse power gain characteristics of the transistor was found to be by at least 8 db smaller than the forward parameter S_{21} . No error correction due to internal circuit reflections was made as a first simple approach to the microwave characterisation of the transistor. The measured driving point parameters S_{11} , S_{22} and the transfer terms S_{12} , S_{21} were used in order to evaluate the elements C_{gs} , C_{dg} and R_{gs} of the equivalent circuit of Fig. 1. This was achieved by expressing the S-parameters in terms of the lumped elements as outlined by Fischer^[7]. The obtained values are listed in Table 1 together with the remaining MOSFET parameters.

Gain measurements were made with the input and output of the devices simultaneously conjugately matched. The tuners available for our investigations were unfortunately of the conventional matching stub type and consequently dc-biasing networks had to be provided between the tuning elements and the device. These resulted in increased losses and complicated to analyse input/output transistor reflection characteristics. The Maximum Available Gain (MAG) of the tested transistors is plotted in Fig. 4 versus the operating frequency for $V_{DS} = 4$ V, $V_{GS} = -1$ V. The gate voltage was found to contribute marginally only to the power gain, its effect never exceeding 1 dB. The maximum oscillation frequency is seen to be of the order of 4.8 GHz with the transistor being unconditionally stable ($k > 1$) outside the measuring frequency range. A gain of 14 dB was measured at 2 GHz in spite of the estimated in Section III relatively large source resistance.

An investigation of the frequency dispersion of the transconductance was possible with the aid of a Rhode & Schwarz USVH Selective Microvoltmeter connected to the drain output of a simple test circuit. The magnitude of transconductance g_m is plotted in Fig. 5 over the frequency range of 20 Hz to 10 MHz. In contrast with other reported results^[6] on GaAs MOSFETs, the transistors showed a transconductance value g_m of the order of 11 mS which remains relatively constant for operational frequencies as low as 800 Hz. Below this frequency, the transconductance is seen to fall rapidly and is probably due to interactions with traps at the oxide-GaAs interface.

V. Conclusions

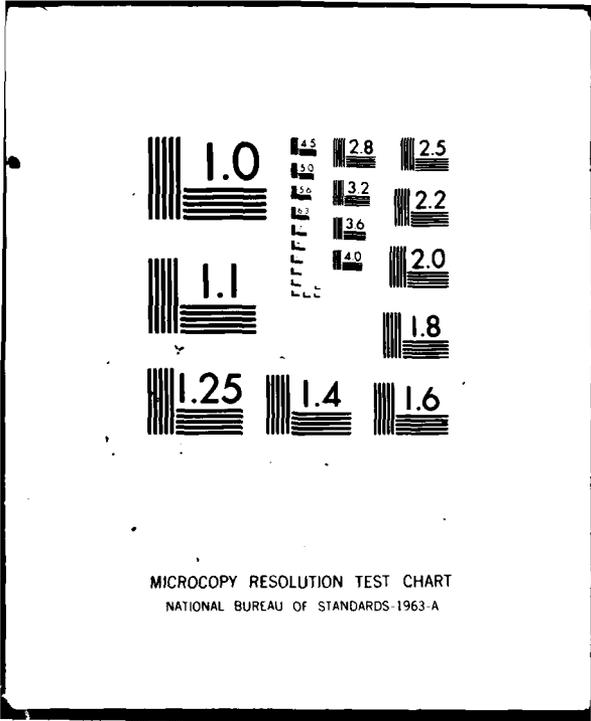
GaAs MOSFETs made on n-type epitaxial layers with the use of wet anodic oxidation techniques were tested at low and high frequencies in view of establishing a characterisation procedure suitable to evaluate the transistor performance. In spite of the fact that the tested devices were not optimised for microwave use, they demonstrated useful features such as satisfactory power gain, maximum oscillation frequency and transconductance figures. With these promising characteristics and the advantages of incorporating an insulator layer for gate protection and reducing gate edge parasitic effects, the future of GaAs MOSFETs looks promising under the condition of further improvements in the degree of sophistication and effectiveness of surface passivation techniques for III - V compounds.

Acknowledgement

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Invited paper

Anodic oxides on GaAs

IV. Thin anodic oxides on GaAs

B. BAYRAKTAROGLU† and H. L. HARTNAGEL†

As the anodic oxides produced on GaAs become thinner, the highly resistive nature of the oxides changes rapidly, allowing large leakage or tunnelling currents through the oxide without, however, permanently changing the original properties of the oxide layer. A considerable deviation from ideal insulator properties was observed with native oxides thinner than about 250 Å, and with anodic Al₂O₃, thinner than 100 Å. In the reverse bias conditions, MOS structures employing very thin oxides (<100 Å) can allow leakage currents of a few A cm⁻² with non-destructive white light emission. By limiting the minority carrier leakage currents, inversion charges can be made to accumulate near the GaAs surface and with such thin oxide GaAs MOS structures, light-enhanced currents were observed with large enhancement factors.

1. Introduction

One of the important basic parameters involved in the design of field-effect devices employing MOS structures is the thickness of the oxide layer used. For the purpose of enhancing the field effects in the semiconductor, the oxide thickness should be as thin as possible. For example, the transconductance of a MOSFET is an inverse function of the oxide thickness. However, as the oxide layer becomes thinner, leakage currents through the oxide increase rapidly, with detrimental effects on the space charge in the semiconductor by the creation of non-equilibrium conditions. The optimum oxide thickness that can be employed in a field-effect device depends on the physical properties of the oxide layer. It is therefore necessary, from a device application point of view, to know the electrical properties of very thin oxides as well as the thicker ones.

This paper reports an investigation of the electrical properties of thin (<300 Å) anodic oxides grown on GaAs, using *I-V* and *C-V* curves.

2. Initial considerations

The thin oxide layers described in this paper are anodically grown native or composite (a mixture of Al₂O₃ and native oxides) oxides on GaAs. The minimum thickness of oxide layer that can be produced on the GaAs surface is restricted by the initial growth phase of anodization in the case of native oxides (Bayraktaroglu and Hartnagel 1978 a) and by the uniformity of the evaporated Al films in the case of Al₂O₃ (Bayraktaroglu and Hartnagel 1978 b) or other composite oxides. It must be kept in mind that a thin layer of native natural oxide is usually present on GaAs exposed to an oxygen-containing atmosphere, and can thus be expected to occur between Al₂O₃

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and GaAs unless special precautions are taken. When native oxide layers are grown alone in electrolytes A and B (Bayraktaroglu and Hartnagel 1978 a, b), the minimum thickness of the oxides can be as low as 11 Å, provided the anodic current density is carefully controlled (Bayraktaroglu and Hartnagel 1978 a). The minimum thickness of Al₂O₃ that can be grown on GaAs, on the other hand, depends very much on the surface roughness of the GaAs substrate. Assuming that the surface is free from scratches and contamination, a minimum of 50 Å of evaporated Al film leads to the production of satisfactorily uniform 75–80 Å thick Al₂O₃ layers.

The uniformity of thin oxide films was judged by their electrical breakdown strengths. For this purpose, MOS structures were produced by evaporating Al field plates, 2000 Å thick, over the oxide layers grown on heavily doped GaAs ($N_D - N_A \cong 2 \times 10^{18} \text{ cm}^{-3}$) with typical field plate areas of 10^{-3} cm^2 , and the electrical breakdown strengths were tested under forward bias conditions. Oxide layers were considered uniform if their breakdown strengths were larger than $2 \times 10^6 \text{ V cm}^{-1}$ for native oxide and $5 \times 10^6 \text{ V cm}^{-1}$ for Al₂O₃ layers.

2.1. The growth of thin native oxides

The results of Breeze *et al.* (1978) and Chang *et al.* (1977) show conclusively that when GaAs is anodized for example in electrolyte B or conductivity-adjusted water, there sometimes exists near its surface a region of the oxide, 100–200 Å wide, with As deficiency, whereas there is always a non-oxidized As region in the oxide near the GaAs-oxide interface about 200 Å in width. If a very thin oxide layer is grown, say 200 Å thick, it is conceivable that these two regions overlap to produce nearly stoichiometric oxides.

The following procedure was employed to produce thin native oxides on GaAs. First, a thick layer of native oxide ($\sim 2000 \text{ Å}$) was grown and subsequently etched in NH₄OH. Then, by a second anodization, a 20–300 Å thick native oxide layer was regrown. A procedure similar to that described above was employed by Chang *et al.* (1977) to produce stoichiometric GaAs surfaces. They showed, with the aid of Auger electron spectroscopy, that on removing the regrown thin native oxide layer with ammonium hydroxide the ratio of As to Ga at the GaAs surface becomes unity.

The thicknesses of the native oxide layers were estimated from the overpotential rise of $V-t$ curves plotted continuously during anodization (Bayraktaroglu and Hartnagel 1978 a).

2.2. The growth of thin Al₂O₃ layers

Since the techniques for growing thin Al₂O₃ (and composite oxide) layers are similar to those for growing thicker layers (Bayraktaroglu and Hartnagel 1978 b), only a brief account of these techniques are given here.

Prior to the Al evaporation, at least 1 μm of GaAs was removed from its surface with the pre-evaporation etchant†. Al was evaporated in a conventional vacuum system at a residual pressure of 10^{-6} torr, or less at a rate of

† Pre-evaporation etchant: A, 4% H₂O₂ by volume; B, 2% NaOH by weight. A : B = 1 : 1.

100 \AA min^{-1} . All Al_2O_3 layers investigated here were produced using an anodic current density of $70\text{--}100 \mu\text{A cm}^{-2}$, which gives an Al_2O_3 growth rate of $20\text{--}30 \text{ \AA min}^{-1}$. At higher current densities the controllability of the Al_2O_3 thickness becomes reduced.

The oxide thicknesses can conveniently be estimated from the overpotential rise during anodization, provided the thickness-overpotential ratios of both Al_2O_3 and native oxides are known. Typical overpotential-time ($V-t$) curves plotted during the anodization of a thin layer of Al on lightly doped n -type GaAs is shown in Fig. 1. In the dark, after almost all Al is

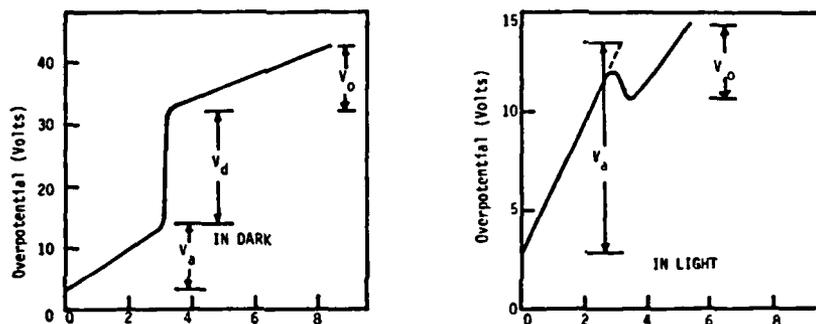


Figure 1. Overpotential-time ($V-t$) curves obtained during the anodization of thin Al layers on GaAs, both in the dark and in light. $N_D - N_A = 10^{16} \text{ cm}^{-3}$, Al thickness $\approx 100 \text{ \AA}$. V_a = Overpotential across Al_2O_3 . V_d = Voltage drop in the space-charge layer of GaAs. V_o = Overpotential across the native oxide.

converted into Al_2O_3 a change in the space-charge layer occurs in GaAs (Bayraktaroglu and Hartnagel 1978 b) which is detected as a sharp rise in the $V-t$ curves. Further anodization produces a native oxide layer whose thickness can again be estimated from the same $V-t$ curve as the overpotential rise after the sharp rise. In light, the anodization of Al is similar to that observed in the dark; however, as most of the Al layer is converted into Al_2O_3 , the highly reflective nature of Al becomes replaced by almost transparent Al_2O_3 and the small space-charge layer in GaAs due to the presence of Al disappears. During the period when native oxides form, photo-generated electrons in n -type materials drift into the GaAs bulk, whereas holes are used to prevent a space-charge layer from growing near the GaAs interface (Bayraktaroglu and Hartnagel 1978 a) and, therefore, unlike anodization in the dark, a large space-charge region does not form.

Due to the large number of holes in p -type GaAs, such space-charge effects are not observed on anodizing Al on p -type GaAs. The effect of light is therefore minimal, and the only way of determining when the native GaAs oxide starts to grow is by observing the change in the slope of the $V-t$ curves.

3. Non-equilibrium conditions

3.1. Thin native oxide MOS diodes

GaAs MOS diodes with very thin anodic native oxides ($20\text{--}300 \text{ \AA}$) show leakage currents that are sufficiently high for non-equilibrium conditions to

develop. When the oxide thickness is typically less than 100 Å, an MOS diode virtually acts as a Schottky diode with a forward threshold field of $\sim 2 \times 10^6 \text{ V cm}^{-1}$. Under reverse bias conditions the applied bias is absorbed almost entirely across the depletion layer formed in GaAs. This is demonstrated in Fig. 2 by the behaviour of the $I-V$ and $C-V$ curves of a typical MOS diode with 100 Å of native oxide.

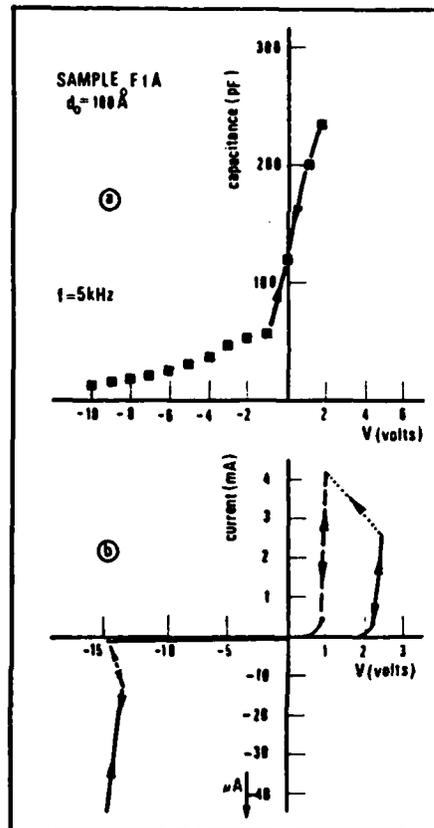


Figure 2. $C-V$ and $I-V$ characteristics of thin-film MOS diodes. The oxide thickness $\sim 100 \text{ \AA}$.

$C-V$ measurements were made in the steady-state condition, point-by-point with a capacitance bridge (Boonton Electronics, Model 75C); $I-V$ measurements were obtained with the aid of a curve tracer.

Figure 2 shows that under reverse bias conditions the capacitance of the diode decreases continuously, and virtually no inversion charges build up underneath the oxide layer. All inversion charges are therefore thought to leak through the oxide. Since almost all the bias applied goes to create a depletion layer in GaAs, the metal Fermi level becomes fixed with respect to the conduction band edge of GaAs with a minimal voltage drop across the

oxide. As the reverse bias is increased, the depletion layer widens to support the extra voltage, decreasing the diode capacitance.

The behaviour of the I - V curves can also be explained with the above-mentioned model. Under forward bias, the diode can sustain a field of $\sim 2 \times 10^6 \text{ V cm}^{-1}$, but at higher fields the leakage current rises very sharply and substantial noise is usually present in this region. Should the current level reach the A cm^{-2} range, the resistance of the oxide suddenly drops. When this happens the forward characteristics of the diode change permanently, reducing the forward bias threshold voltage to 0.5–0.6 V, regardless of the oxide thickness.

Under reverse bias conditions, the leakage current of diodes produced on n -type GaAs ($N_D - N_A = 10^{15} \text{ cm}^{-3}$) with Al field plates is less than $10^{-5} \text{ A cm}^{-2}$ (the sensitivity of the measuring system employed) up to about -15 V , and is independent of the oxide thickness in the range 20–100 Å. At this point a reproducible s -type negative resistance is observed and the current starts to increase rapidly in a linear fashion. This instability is also seen on reducing the voltage. The critical reverse bias which causes a sudden increase in the diode current depends not only on the GaAs doping, but also on the field plates used. Figure 3 shows the I - V characteristics of reverse-biased MOS structures with different GaAs doping and different field plates. Some measurements were also taken at 77 K.

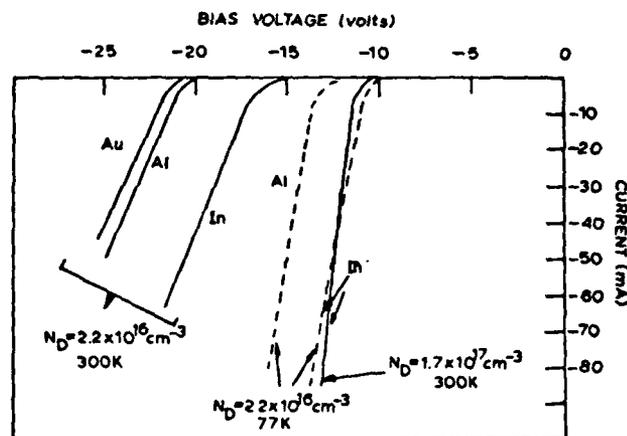


Figure 3. I - V characteristics of typical anodic oxide MOS structures produced on n -type GaAs with different top metal contacts at two test temperatures. The oxide thickness $\sim 50 \text{ \AA}$, estimated from V - t curves.

The temperature dependence of the reverse bias current is consistent with the avalanche multiplication process in GaAs. However, since the current is higher with field plates having low work functions than with those having high ones, at the same bias values, the whole current due to avalanche multiplication in the GaAs depletion layer is not likely to be the only source of current measured. MOS diodes produced on p -type GaAs, on the other hand,

show higher leakage currents with field plates having larger work functions. Non-destructive white light emission was also observed when the diode current is larger than about 1 A cm^{-2} . Details of this observation are reported elsewhere (Bayraktaroglu and Hartnagel 1978 c).

If the thickness of the native oxide is greater than 150 \AA , the above-mentioned properties of MOS diodes partially disappear. Typical $C-V$ and $I-V$ curves of GaAs MOS diodes with a native oxide layer about 300 \AA thick are shown in Fig. 4. In the reverse bias, at moderate fields ($\sim 10^6 \text{ V cm}^{-1}$)

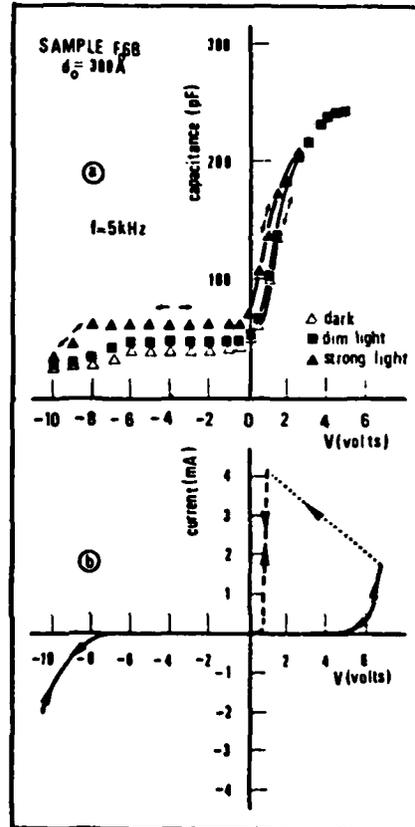


Figure 4. $C-V$ and $I-V$ characteristics of thin-film MOS diodes. The oxide thickness $\sim 300 \text{ \AA}$.

an inversion layer forms and the capacitance of the diode becomes fixed at C_{\min} . At higher fields, typically greater than $2 \times 10^6 \text{ V cm}^{-1}$, the capacitance decreases further and eventually joins the deep depletion curve. Increasing the light intensity has two effects on the capacitance.

- (1) C_{\min} increases due to the reduction in the depletion layer width. Since extra minority carriers are created by the incident light, a

- narrower depletion layer underneath the inversion region is required to create the same amount of inversion charges (Pierret and Sah 1970).
- (2) Departures from the quasi-equilibrium occur at higher voltages. This is again due to the creation of extra minority carriers which counterbalances some of the leakage currents, thereby sustaining the inversion layer at higher voltages.

Regardless of the light conditions and the test frequencies, the $C-V$ curves all join up with the deep depletion curve at high field values (typically at $4 \times 10^6 \text{ V cm}^{-1}$).

The $I-V$ curve shown in Fig. 4 is the same, in principle, as that shown in Fig. 2 under forward bias conditions. For fields larger than $2 \times 10^6 \text{ V cm}^{-1}$, a permanent change occurs in the oxide resistivity, as before. In the reverse direction the leakage current is less than $10^{-5} \text{ A cm}^{-2}$ for field values less than $2 \times 10^6 \text{ V cm}^{-1}$, but increases slightly at higher fields depending on the oxide thickness and the light conditions.

A comparison of the $C-V$ and $I-V$ curves shows clearly that when the reverse bias leakage current through the oxide begins to increase substantially, i.e. at about -6.0 V , a departure from the quasi-equilibrium conditions occurs and the capacitance of the diode begins to decrease below its C_{min} value.

So far we have considered either very thin oxides, i.e. $\leq 100 \text{ \AA}$, for which the leakage of the minority carriers is high, or relatively thick oxides, i.e. $\sim 300 \text{ \AA}$, for which an accumulation of the inversion charges take place. An interesting case arises if the thickness of the oxide is between these two values. For example, 150 \AA of oxide is normally thick enough to accumulate some inversion charges but is also thin enough to allow tunnelling to take place. Using oxides of these intermediate thicknesses, it was found that the reverse bias leakage current can be enhanced with the aid of light. A plot of the current versus the negative bias voltage is shown in Fig. 5 for an MIS

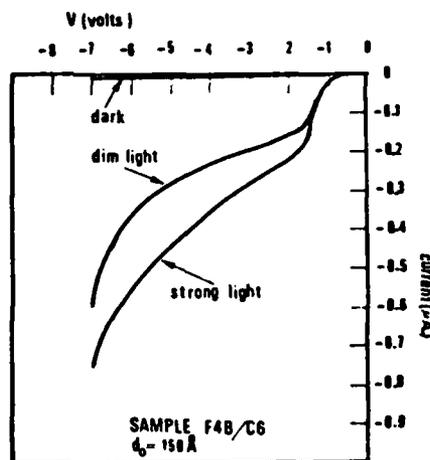


Figure 5. Reverse-bias $I-V$ characteristics of thin-film MOS diodes in light and dark conditions. The oxide thickness $\sim 150 \text{ \AA}$.

diode with a native oxide about 150 Å thick. These currents are much higher than expected from the extra electron-hole pair generation with light in the depletion layer of the GaAs, since currents of this magnitude are not observed, either with simple Schottky barrier diodes constructed in the same dimensions or with MIS diodes having thinner (<100 Å) oxide layers. It is also interesting to note that these currents do not start to increase until the reverse bias voltage reaches a threshold value. Similar currents were observed very strongly with thin Al_2O_3 , and the origin of these curves is discussed in detail in § 3.2.

3.2. Thin Al_2O_3 MIS diodes

Typical $C-V$ and $I-V$ curves of an MIS diode with a 75 Å thick Al_2O_3 layer are shown in Fig. 6. The effect of the light on the $C-V$ curve is similar to that observed with thin GaAs native oxide, i.e. C_{min} increases and the

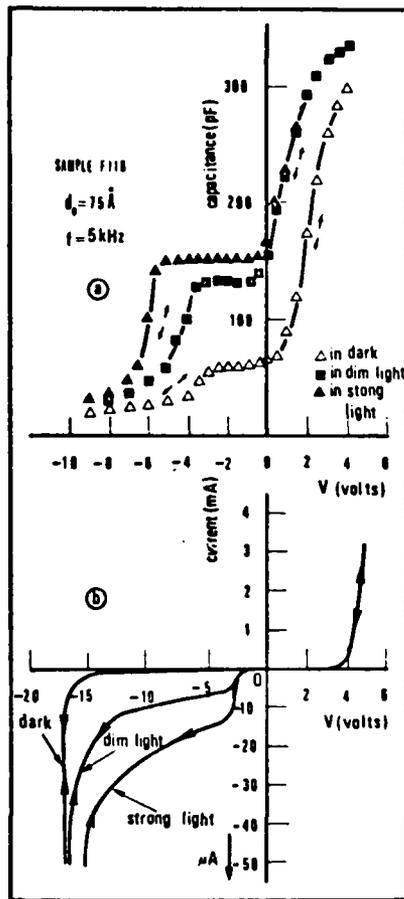


Figure 6. $C-V$ and $I-V$ characteristics of thin-film MIS diodes with ~ 75 Å Al_2O_3 on the insulator.

departures from the quasi-equilibrium occur at higher voltages under illumination. With the same light intensity the shift in the C_{min} values is higher in the present case than that observed with a 300 Å thick native oxide, as seen in Fig. 4. The I - V curves shown in Fig. 6 are rather interesting since they show very enhanced current levels in the reverse bias, with the same light intensities as used previously with 150 Å thick native oxide. Under forward bias conditions large leakage currents start to flow at field strengths of $> 5 \times 10^6$ V cm⁻¹. As long as this current level is kept within the A cm⁻² range, the electrical properties of the insulator are not changed, but at higher values the probability of permanent dielectric breakdown becomes higher.

Figure 6 also shows the effect of light on the reverse-bias currents. In the dark, the leakage current is less than 10⁻⁵ A cm⁻² up to about -15 V, where a sudden rise in the current is observed. In light, the current starts to rise at about -3 V and then tends to saturate. It is important to note that both the saturation current level and the voltage at which the saturation starts to occur increase with the light intensity. The current saturation level under similar illumination drops sharply as the Al₂O₃ layer is increased above 100 Å.

Clarke and Shewchun (1971) have reported similar light-enhanced currents with a 30 Å thick SiO₂ layer on Si. An explanation of this phenomenon given by Green and Shewchun (1974) was used as the basis for the analysis of the present situation.

In the dark, it is assumed that the leakage current is larger than the generation rate of the minority carriers, therefore no inversion layer charges can build up near the surface. Under these conditions the Fermi level of the metal is pinned with respect to the conduction band edge of the GaAs and most of the applied bias occurs across the depletion layer formed in the GaAs. However, if, with the aid of light, the generation rate of the minority carriers can be made larger than the leakage current, an inversion layer forms and the depletion layer width becomes fixed. Any further bias produces a voltage drop across the oxide, moving the Fermi level of the metal up with respect to the GaAs conduction band edge. A point will be reached at which the metal Fermi level is in line with the conduction band edge, and the probability of majority carrier tunnelling from the metal to the conduction band of the GaAs increases. The magnitude of this tunnelling current depends strongly on the voltage drop in the insulator, which is a function of the degree of inversion at the surface. However, as the degree of inversion depends on the balance between the minority carrier generation rate and the leakage current, it is possible under certain circumstances to induce majority carrier tunnelling currents by illumination. It is also reasonable to suggest that, for MOS structures produced on *n*-type GaAs, with the same oxide voltage, the position of the metal Fermi level will be higher when field plates with lower work functions are used. Figure 7 summarizes the mechanism of light-enhanced currents observed with GaAs MOS (or MAOS) diodes.

It was shown by Green and Shewchun (1974) and by Shewchun and Clarke (1973) that by choosing the right device parameters, the above-mentioned mechanism can increase the current by a factor of 1 to 10³ for the Si-SiO₂-metal system. A simple comparison of the I - V characteristics of an MIS diode such as the one shown in Fig. 6, and a Schottky diode produced in

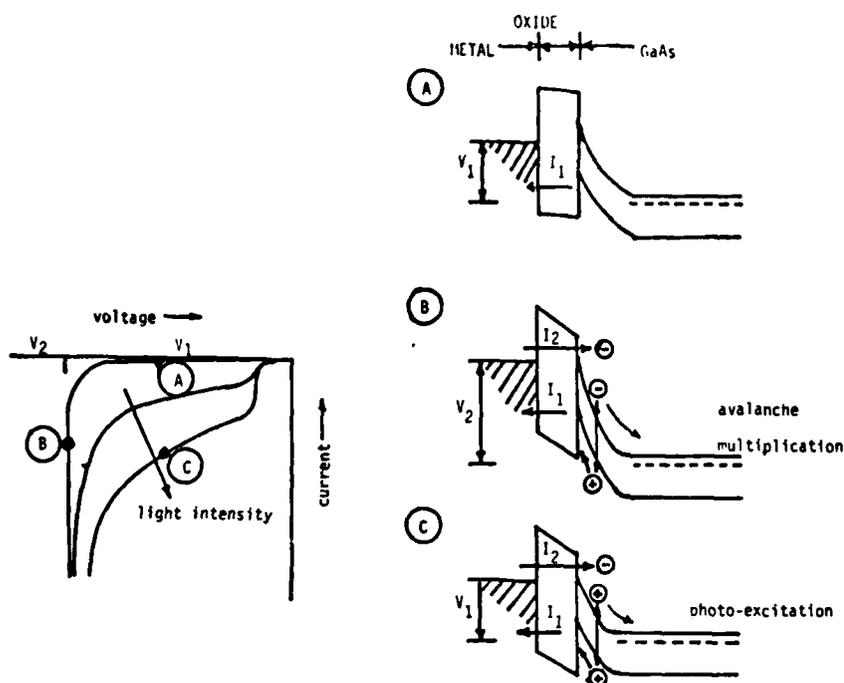


Figure 7. A proposed model for the current multiplication observed with thin-film MIS diodes on GaAs.

exactly the same way as the MOS structure but without the Al_2O_3 layer (which gives a leakage current of $< 10^{-5} \text{ A cm}^{-2}$ in bright light conditions), shows that with 75 \AA of Al_2O_3 a current enhancement of $> 10^3$ is possible. Similarly, from Fig. 5 an enhancement factor of 20 can be derived for the MIS diodes with 150 \AA of native oxides.

4. Device applications

It was demonstrated above that both the GaAs native oxide and the Al_2O_3 can be produced uniformly over the GaAs, even when they are less than 100 \AA thick. The electrical properties of these oxides are not very different from what is observed with thicker ones before the onset of non-equilibrium conditions. Thin native oxide and Al_2O_3 films were found to withstand fields up to 2×10^6 and $5 \times 10^6 \text{ V cm}^{-1}$ respectively. Also, with appropriate thicknesses a build-up of inversion charge near the surface was observed. In this respect one of the main uses of such thin oxides will be in manufacturing MOSFETs with high transconductances.

Since it is possible to obtain light-enhanced currents with thin oxide MOS structures (especially with thin Al_2O_3), such devices can be used as photo-sensors. The test devices employed in § 3 always had 2000 \AA of Al pads as the top contact which is, of course, highly reflecting. Incident light changed the MOS characteristics of these devices by creating electron-hole pairs only

around the edge region of the depletion layer. By using much thinner layers of metal, e.g. 50 Å of Au, which is practically transparent to the light, higher efficiencies may be possible.

If the minority carriers are supplied to the GaAs surface region of these reverse-biased thin oxide MOS diodes by means of, say, a second similar, but forward-biased, diode, transistor action is possible. The possibility of such a transistor, which is called the surface oxide transistor, was demonstrated by Shewchun and Clarke (1973) with 30 Å thick SiO₂ on Si.

5. Conclusions

In conclusion it can be said that, due to its lower leakage currents and higher electrical field strengths, a higher degree of inversion on the GaAs is possible with Al₂O₃ than with a native oxide of the same thickness. It is important to note that thin anodic oxides on GaAs (<100 Å) do not change their electrical properties until a leakage current density of several A cm⁻² is reached. Finally, a current enhancement process is possible with very thin Al₂O₃ layers on GaAs.

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AN ASSESSMENT OF THE QUALITY OF ANODIC NATIVE OXIDES OF GaAs FOR MOS DEVICES

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Our present understanding of the factors which affect the growth and properties of the anodic oxides of GaAs is reviewed. The various parameters which affect film composition are discussed and some new data from studies by electron spectroscopy for chemical analysis are given. An anodic growth mechanism is postulated which involves the interstitial ion drift of gallium and arsenic ions and a vacancy transport mechanism for oxygen. Experimental evidence in support of this is discussed. A brief review of the electrical properties of GaAs anodic native oxides is given. Areas in which further work is required are outlined.

1. INTRODUCTION

Since work was first started to find a suitable dielectric for the production of MIS devices on GaAs, a variety of materials and techniques have been investigated including the deposition of SiO_2 , Al_2O_3 and SiO_2N_x ¹⁻³, thermal oxidation^{4,5}, anodic oxidation⁶⁻⁹ and plasma oxidation¹⁰. Thermally grown native oxides on GaAs have been found to be composed almost entirely of Ga_2O_3 ¹ owing to the high volatility of As_2O_3 , although recent work on thermal oxidation under a controlled As_2O_3 vapour pressure has shown improved results¹¹.

The difficulties due to the loss of As_2O_3 and arsenic at elevated temperatures stimulated interest in finding a suitable low temperature technique. One technique which has shown promise is that of anodic oxidation. Initial results^{6,7} obtained using this method of oxidation were not very good, yielding non-uniform films with poor electrical characteristics. However, more recent results^{8,9} obtained after optimization of the growth parameters and of the electrolyte have shown that it is possible to grow uniform native oxide films with high resistivity and good dielectric breakdown strength. These results have been shown to be extremely reproducible, and the method allows easy control of the oxide thickness and is very simple to use.

More recently native oxide films have been produced using plasma oxidation in various forms: some of these methods are essentially anodic oxidation carried out in the gas phase. However, the films grown in this way appear to have somewhat higher d.c. leakage currents than films grown in solution.

In this paper we look at the properties of native oxides of GaAs formed anodically, assessing the results of the anodization technique used and indicating those areas in which further work is required.

2. ANODIC OXIDATION TECHNIQUE

The growth of a native oxide film on GaAs by anodic oxidation is carried out by polarizing the GaAs sample positively with respect to an inert electrode such as platinum in a suitable electrolyte. The important parameters which must be controlled are the current, the overvoltage and the electrolyte composition. The experimental apparatus used to carry out anodization has been described in detail by Hasegawa and Hartnagel⁹.

Growth may be carried out under either constant-current conditions or constant-voltage conditions (or a combination of the two)¹⁰. However, growth under constant-current conditions has the following advantages over the other regimes.

(i) The film growth occurs at a constant rate which may be controlled by varying the constant current employed.

(ii) The thickness of the growing film may be monitored by monitoring the voltage developed across the oxide. The thickness-overvoltage characteristics of anodic oxides are extremely reproducible, and once these have been determined any required thickness may easily be obtained. It should be noted, however, that the thickness-overvoltage characteristic varies with current density and so must be determined for the particular current density employed, once this has been optimized.

The composition of the electrolyte plays an important role in determining the reproducibility of anodic oxidation and also the properties of the oxide film. A great variety of electrolytes have been employed, but very reproducible results have been obtained⁹ with mixed aqueous glycol electrolytes. The role of the glycol seems to be to limit the diffusion rate of ions in the electrolyte. Many electrolytes etch the native oxide at a low rate which is dependent on such parameters as concentration, pH and temperature. The glycol seems to reduce the diffusion rate of the dissolution products away from the oxide surface and thus to make the anodic oxidation less sensitive to any pH or concentration changes; it also reduces the rate of dissolution. In addition the glycol will probably affect the transport of the oxidizing agent to the oxide surface but since this agent appears to be water¹² whose concentration is very high the effect is expected to be much less significant. We have measured an activation energy of 5 kcal mol^{-1} for the dissolution process in a mixed glycol-tartaric acid solution which is consistent with the proposal that it is diffusion controlled.

3. ANODIC FILM COMPOSITION

The composition of the electrolyte used also influences the properties of the anodic oxide film. The mechanism involved during GaAs anodization is not well understood at present but some general observations may be made.

It is well known that during the anodization of valve metals, particularly aluminium, some electrolytes give rise to barrier-type oxide films whereas other electrolytes produce porous films¹³. It is possible that the same situation exists with GaAs anodization, and if so it is important to avoid the formation of porous films since they can be expected to show poor electrical properties such as high, d.c. leakage currents. However, the dividing line between barrier and porous film

formation is not clear cut as some barrier-film-forming electrolytes seem to produce porous films when the anodization conditions are changed¹³. It has been observed¹⁴ in our laboratories that when the anodization of GaAs is carried out in an electrolyte consisting of 1 part of 0.02 M $(\text{NH}_4)\text{H}_2\text{PO}_4$ mixed with two parts of propan 1,2 diol the oxide film, which is initially of the barrier type, seems to become porous when the film thickness becomes large. This behaviour is characterized by a flattening off of the overvoltage-time curve for constant-current growth, and scanning electron microscopy photographs appear to show deep pores in such films. The onset of this behaviour appears to be sensitive to the growth current density, the critical thickness becoming smaller at low growth current densities. This phenomenon must be carefully monitored to avoid porous film formation, and its occurrence might account for some of the discrepancies in the reported properties of anodic oxides produced in different electrolytes.

Even when electrolytes are used under barrier-film-forming conditions, variations in oxide composition have been observed. The anodic oxide surface seems particularly sensitive in this respect. Chang *et al.*¹⁵ have used Auger depth profiling techniques to study GaAs native oxides produced by anodization in dilute aqueous solutions of H_3PO_4 . They observed a surface region which was arsenic deficient, the gallium-to-arsenic ratio at the surface being about 5. We have used X-ray photoelectron spectroscopy (electron spectroscopy for chemical analysis (ESCA)) combined with argon ion etching to carry out similar studies¹⁶. Samples of GaAs anodized in the $(\text{NH}_4)\text{H}_2\text{PO}_4$ -glycol electrolyte under barrier-film-forming conditions also exhibited a region close to the surface which was arsenic deficient. However, in this case, depending on the growth current density, no arsenic whatsoever was observed at the surface itself. The width of the region and the extent of the arsenic deficiency were observed to vary with the growth current density, the effect being more pronounced at high current densities (0.5 mA cm^{-2}). In contrast with this, samples grown in the AGW electrolyte⁹ (one part of 3 vol. % tartaric acid solution mixed with two parts of propan 1,2 diol) showed a gallium-to-arsenic ratio in the oxide surface region that was lower than that in the bulk of the oxide. Table I lists some gallium-to-arsenic ratios at the surface of native oxide films grown in different electrolytes.

The processes controlling the surface composition of anodic films have not been investigated. However, it seems most likely that surface absorption phenomena are involved, perhaps similar to those known to affect the anodic dissolution rate of some metals¹⁷. The equivalent dissolution rate of the anodic oxides of GaAs varies with different electrolytes. For example the rate is $35 \mu\text{A cm}^{-2}$ in the AGW electrolyte whereas in the $(\text{NH}_4)\text{H}_2\text{PO}_4$ -glycol electrolyte it is less than $1 \mu\text{A cm}^{-2}$. Since the dissolution process is also a surface phenomenon it may be possible to relate the surface composition to the equivalent dissolution rate.

However, regarding the surface composition, since the gate contact for a metal-oxide-semiconductor (MOS) device is placed on the oxide surface, it is important to establish whether or not it influences the device behaviour, and more work is required in this area.

The gallium-to-arsenic ratio in the bulk of the oxide film shows some variation with electrolyte composition (see Table I) and variations have also been noted¹⁸ from determinations made on similar oxides using different techniques. Chang *et*

TABLE I

THE GALLIUM-TO-ARSENIC RATIOS AT THE SURFACE AND IN THE BULK OF ANODIC OXIDES ON GALLIUM ARSINIDE GROWN UNDER DIFFERENT CONDITIONS

Gallium-to-arsenic ratio at or near the oxide surface	Gallium-to-arsenic ratio in the oxide bulk	Electrolyte, growth conditions	Reference
33	1.8	(NH ₄)H ₂ PO ₄ glycol, 500 μA cm ⁻²	16
14	1.8	(NH ₄)H ₂ PO ₄ glycol, 10 μA cm ⁻²	16
1.4	1.8	Tartaric acid glycol, 200 μA cm ⁻²	16
2.9	1.8	Aqueous H ₃ PO ₄ , constant voltage 150 V	15
1.4	0.77	Citric acid-glycol, constant current and constant voltage	19

al.¹⁵ have reported a gallium-to-arsenic ratio of 1.8 for the bulk of the oxide film. Verplanke and Tijburg¹⁹ have used radioactive tracer techniques to analyse films grown by anodization in a citric acid solution-glycol electrolyte. They have observed a gallium-to-arsenic ratio of about 0.7. In our own ESCA studies we have observed gallium-to-arsenic ratios in the range 1.7-1.8 for samples anodized in both AGW and (NH₄)H₂PO₄-glycol electrolytes. However, the extent to which the ESCA ratios are affected by the selective etching that occurs during the argon profiling has not been established so that at present these values are tentative. (A typical ESCA profile is illustrated in Fig. 1.) The reasons for the variations are not clear but Verplanke and Tijburg have suggested that it is due to the use of different electrolytes. However, their suggestion that the effect is due to the use of glycol in the electrolyte does not seem to account entirely for the difference in the light of our ESCA results unless selective etching affects the gallium-to-arsenic ratio here by a factor of 3, which is greater than the effect observed from the GaAs substrate (about 1.5) and therefore seems unlikely.

In view of these problems it is not clear what the optimum gallium-to-arsenic ratio should be. It might initially be anticipated that a ratio of unity is the most favourable. However, consideration of the densities of Ga₂O₃ and As₂O₃ indicates that, if equal volumes of each were mixed together, then the gallium-to-arsenic ratio observed would be 1.7, a value which is very close to some of those reported above. This leads to the possibility that the composition of the oxide film is controlled by some mechanism related to the mixing of the two oxides and that a ratio different from unity may lead to the most stable structure. However, more work is required to establish the range of compositions which can be achieved and the electrical properties associated with each composition. It should be pointed out in connection with this, however, that a recent paper²⁰ reported a gallium-to-arsenic ratio of unity for a plasma-grown anodic film formed beneath an aluminium oxide layer.

As with the surface region the composition at the GaAs-oxide interface also

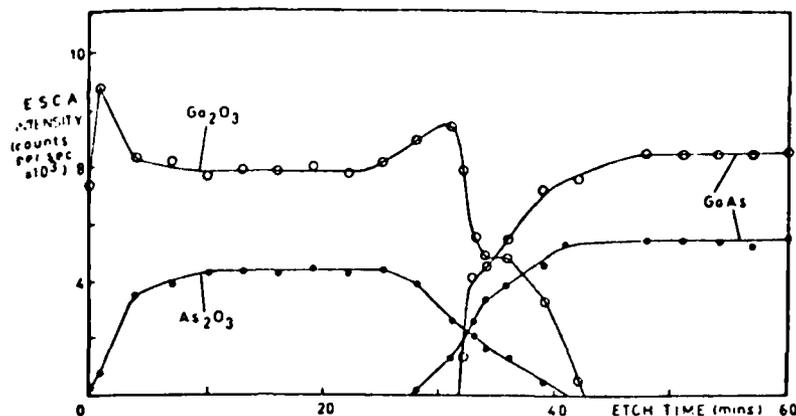


Fig. 1. A typical ESCA profile of an anodic oxide on GaAs: anodization in $(\text{NH}_4)_2\text{H}_2\text{PO}_4$ -glycol electrolyte at $10 \mu\text{A cm}^{-2}$; oxide thickness, 750 \AA ; ●, As; ○, Ga.

deviates from that in the bulk of the oxide. Chang *et al.*¹⁵ have reported an excess of arsenic at this interface. In our ESCA studies we have observed two important changes in composition close to the GaAs substrate (see Fig. 1). Firstly the As_2O_3 starts to disappear before the Ga_2O_3 so that the ratio of Ga_2O_3 to As_2O_3 increases in this region. Wilmson and Kce²¹ have made a similar observation. Secondly there is a region adjacent to the GaAs substrate in which arsenic appears but no gallium, although the ESCA chemical shift suggests that gallium is in a similar state to the arsenic in the GaAs¹⁶. Both these effects were observed in oxide films grown in either of the electrolytes which we studied. This seems to suggest that the composition in this region is controlled by the anodic growth mechanism involved and does not depend on the electrolyte.

The thickness-overvoltage characteristic of the anodic oxide varies with the growth current density. For example in the AGW electrolyte the observed⁹ values are 20 \AA V^{-1} at 1 mA cm^{-2} and 21.5 \AA V^{-1} at $100 \mu\text{A cm}^{-2}$. Crystallinity has been observed²² in oxides grown at current densities greater than 2 mA cm^{-2} . From these observations it appears that the structure of the anodic oxide is affected by the current density employed during growth. This may be related to the anodic growth mechanism since the variations occur with the same electrolyte.

The effect of annealing on the composition of anodic oxides has been studied by various workers^{15,19,22}. The results show that arsenic is lost from the film if annealing is carried out above 350 C owing to the high volatility of As_2O_3 . The effect becomes more pronounced the higher the temperature used, and polycrystalline Ga_2O_3 may start to appear²². These effects correlate with an increase in the d.c. leakage current through the oxide, and deterioration in the capacitance-voltage characteristics.

4. ANODIC GROWTH MECHANISM

Since the composition and hence the properties of anodically grown films on GaAs appear to be in part controlled by the growth mechanism, it is important to try

and understand this if the properties are to be completely controlled. Although very few studies have been reported on this aspect of GaAs anodization, there is a considerable amount of data available concerning the mechanism involved during the anodic passivation of various valve metals. Certain conclusions can be drawn from these data which may be of value in elucidating the mechanisms involved with GaAs. However, in the absence of clear experimental evidence the mechanisms which we propose must be of a speculative nature.

Davies *et al.*^{2,3} have used radioactive tracer techniques to study the migration of oxygen and metal atoms during the anodic oxidation of a series of metals. From these results they calculated a factor t_m which represents the fraction of the film growth due to the metal atom migration. These values are presented in Table II together with the ionic radii of the metal ions in the valency state appropriate for the oxide formed. From Table II it can be seen that the contribution from the metal ion decreases as the ionic radius increases, the contribution approaching zero for ions of radius greater than 0.8 Å. (The value for aluminium included in Table II is that obtained for anodization in a mixed glycol-sodium tetraborate electrolyte. Different results were reported for anodization in an aqueous citrate electrolyte, with a variation in t_m with current density. However, this may be due to porous film formation since this electrolyte has been reported¹¹ as being of a pore-forming nature whereas the former is not. Smaller variations of t_m with current density occurred with some of the other metals but these were not considered by the authors to be significant in comparison with the experimental errors; in these cases we have listed average values.)

TABLE II
THE CONTRIBUTIONS OF METAL ION DRIFT TO THE GROWTH OF ANODIC OXIDES ON VARIOUS METALS

Metal	Percentage contribution t_m of metal ions to film growth ^{2,3} (%)	Metal ion radius in oxide ^{2,4} (Å)
Zr	<5	0.79
Hf	<5	0.78
Nb	27	0.69
Ta	29	0.68
W	33	0.62
Al	58	0.51

The variation in t_m with ionic radius can be explained if the metal ions move interstitially through the oxide film during growth. If this is the case, then as the size of the ions increases, relative to the size of the interstitial sites, the activation energy for drift under the influence of the electric field is expected to increase, leading to the observed results. The situation is not quite as simple as this since we must consider the structures of the different oxides and the possible variations in the size of the interstitial sites. However, since anodic oxide films are generally amorphous and possess no long range order, it is possible that the structures are similar and are dominated by the relatively large oxygen anions.

If this interpretation is considered to be valid and applicable to GaAs anodization, then two conclusions may be drawn.

- (i) Since the ionic radii of gallium and arsenic are different (0.62 and 0.69 Å

respectively for the tripositive ions)* they are expected to drift at different velocities.
(ii) The size of the oxygen di-anion (1.40 Å) precludes the possibility that interstitial transport of oxygen makes a significant contribution to the growth.

Considering the transport of oxygen Pringle²⁵ has studied its migration during the anodic oxidation of tantalum. Firstly his results showed that oxygen atoms do migrate during anodic oxidation, secondly he demonstrated that during growth their order is preserved and thirdly he estimated that the average jump distance for an oxygen atom during migration is about 4 Å. (This is about the same order of magnitude as the distance expected between nearest neighbour oxygen atoms.) These results are entirely consistent with the assumption that oxygen migration takes place via a vacancy transport mechanism. In fact the preservation of order is exactly the opposite of what would be expected from an interstitial transport mechanism where the ions entering the film last would be expected to appear nearest to the opposite interface. Recent results from a similar study of GaAs anodization¹² showed that the order of oxygen atoms is also preserved in this case.

On the basis of these observations we propose a mechanism for GaAs anodic oxidation in which gallium and arsenic atoms are ionized at the GaAs-oxide interface by the high field present and that these ions then migrate interstitially from this interface towards the oxide surface under the influence of the field. We also suggest that oxygen transport from the surface towards the interface is by a vacancy transport mechanism. Because of their differing sizes the gallium and arsenic ions may drift at different rates. The vacancy transport mechanism for oxygen requires that positively charged vacancies are created at the oxide-semiconductor interface, possibly by the removal of gallium and arsenic lattice atoms as interstitial ions; these then drift towards the oxide surface under the influence of the electric field.

If the gallium and arsenic ions drift at different rates we might expect to observe this phenomenon as different concentration gradients of gallium and arsenic within the oxide film. There is no clear evidence that such a gradient exists but the actual concentration of interstitial ions present could be extremely small, depending on their absolute drift velocities. Accurate measurements of the overvoltage-thickness characteristic for anodic oxide films on GaAs²⁶ have shown a linear relationship for growth at 1 mA cm^{-2} . This suggests that there is no observable space charge effect within the film due to the migrating ionic species which in turn suggests that the concentration of ionic species present is low. The concentration should be greater at higher growth current densities and an effect may be observable under such conditions.

The build-up of arsenic observed at the oxide-semiconductor interface could be consistent with a higher activation energy for arsenic ion drift, but it would be an oversimplification to consider this to be the complete explanation. It has been suggested elsewhere¹⁵ that this arsenic build-up is due to the preferential formation of Ga_2O_3 . This was explained as due to the fact that Ga_2O_3 has a higher thermodynamic stability than As_2O_3 . However, the thermodynamic data refer to equilibrium conditions whereas here we are dealing with a kinetic situation where the height of the energy barriers is the most important consideration.

* Different sources give different values for the As^{3+} ionic radius. This value is calculated for sixfold coordination as is that for Ga^{3+} ; thus these are probably the best values for comparison purposes.

An alternative, although entirely speculative, explanation for the arsenic build-up is related to the way in which gallium and arsenic cations are formed and removed from this interface. If we consider a GaAs pair in the GaAs substrate at the interface, it is possible that under the influence of the high electric field the gallium atom may be removed as a positive ion, leaving the arsenic atom negatively charged and at the same time forming a positively charged vacancy. The positive vacancy and the arsenic anion could then become associated and trapped at the interface. The reverse situation where an arsenic cation is removed, leaving a negatively charged gallium species, is less likely owing to the more electropositive nature of gallium.

If the model is correct in predicting the formation of oxygen vacancies at the oxide-semiconductor interface, this is an unfavourable situation since it implies the likelihood of excessive defect concentrations in this region which might result in a higher interface state density. This situation is likely to be aggravated by the use of high growth current densities, especially if any space-charge-limiting effects are involved²⁷, and may explain some of the variations observed with current density. For this reason the use of low current densities (in the region of $100 \mu\text{A cm}^{-2}$) is likely to produce oxide films with better electrical properties.

Although the growth mechanism suggested here is largely speculative it does represent a starting point from which an interpretation of the available data becomes possible. This is important if we are eventually to gain a full understanding of the anodic growth process, and we hope that it will stimulate further consideration in these areas.

5. ELECTRICAL PROPERTIES OF ANODIC OXIDES ON GALLIUM ARSENIDE

The electrical properties of anodically grown native oxides on GaAs which have been discussed in detail elsewhere^{22,28-30} will be briefly mentioned here.

Kohn *et al.*^{28,30} have calculated the charge trapped in the oxide from d.c. leakage current measurements. Using this they have calculated the charge centroid, which was found to reach values of up to half the oxide thickness. The presence of the charge centroid was used to explain various instabilities observed in the anodic oxides. For example a non-destructive breakdown phenomenon was observed when the breakdown field strength ($(2-3) \times 10^6 \text{ V cm}^{-1}$) was just exceeded. Partial recovery took place if the device was stored for several days. It has been suggested that this breakdown occurs close to the interface owing to the high field associated with the trapped charge.

The capacitance-voltage characteristics of MOS diodes on GaAs exhibit several aspects of non-ideal behaviour including hysteresis, frequency dispersion and an accumulation capacitance which continues to increase with increased bias voltage. The last effect may also be explained by a charge centroid in the oxide which effectively reduces the capacitor thickness, thus causing an apparent increase in the accumulation capacitance.

Interpretation of these results in terms of the theory developed for the silicon-SiO₂ system seems to lead to the conclusion that the interface state density is very high and that prospects for device operation are not very good. However, it has recently been argued³⁰ that this theory is not applicable to the GaAs-native oxide

system because of the complicated oxide trapping and interface behaviour. Indeed, enhancement-depletion mode MOS field-effect transistors (MOSFETs)^{31, 32} which show promising characteristics have been fabricated using the GaAs anodic oxide technology, suggesting that the present understanding of their behaviour is far from complete

6. ANODICALLY GROWN DOUBLE OXIDE STRUCTURES

Recent work has examined the properties of dielectrics on GaAs incorporating aluminium oxide as well as the GaAs native oxide²⁹. These are fabricated by depositing a thin layer of aluminium on the GaAs substrate prior to anodization. Capacitance-voltage measurements made on diodes fabricated in this way show reduced hysteresis and an increase in the slope of the capacitance-voltage curve at high frequencies, indicating that the surface states are frozen out. The discrepancy between the predicted and observed capacitances is also reduced.

In addition, dielectrics fabricated in this manner have shown charge storage properties³³, and a memory transistor has been constructed using this technology³⁴. The performance of these devices compares extremely favourably with that of devices produced using silicon MNOS technology.

7. CONCLUSION

We believe that the anodic oxidation of GaAs represents the most promising technique available for the production of MOS devices on this semiconductor. However, the processes involved are extremely complicated and as yet not very well understood.

The effects of the electrolyte and of the growth current density on the properties of the anodic oxide need careful examination, and an attempt should be made to correlate any physical changes observed with the electrical characteristics of the films. It is also important to obtain a good working model for the growth mechanism involved during the anodic oxidation of GaAs and to try and understand how this influences the film structure and properties. Our suggestions in this respect are based primarily on results reported for other anodic systems, and our model is based on the interstitial transport of gallium and arsenic ions and a vacancy transport mechanism for oxygen ions. We believe that it represents a useful starting point for a critical examination of the mechanisms involved.

A detailed knowledge of the physical and chemical composition of the anodic oxide films is essential if a complete understanding of their behaviour is to be obtained. A significant amount of data is already available, much of it from Auger depth profiling studies. However, we have found that ESCA combined with argon ion etching provides extremely valuable complementary information. Its particular strength lies in the ability to distinguish between atoms of the same element in different chemical environments. This has allowed us to observe much more clearly the compositional changes that occur at the oxide-semiconductor interface. The use of a variety of different physical techniques will help to clarify certain areas of uncertainty, particularly the composition of the anodic oxide films. From this point of view the use of as many different techniques as possible will be highly advantageous.

With regard to the electrical properties of the GaAs anodic oxides, particularly their interfacial properties, it is clear that the currently available models are inadequate. In this area the availability of precise physical information will certainly assist in the development of more realistic models which predict the electrical characteristics much more reliably.

Finally, with the production of double oxide films on GaAs the flexibility of the anodic oxidation process has been demonstrated. This innovation has produced dielectrics with better electrical properties as well as introducing new possibilities for device applications. We feel that the value of this technology has now been proved.

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Multiple insulator layers on GaAs studied by Auger analysis

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Recently research was focused on the formation of multiple layer anodic insulators on GaAs to obtain superior passivation layers. In particular Al₂O₃ films in conjunction with native oxide films were evaluated. In this paper Auger analysis studies are reported on Al₂O₃-native oxide films on GaAs. The results indicate that oxygen migrates during anodization towards the interface while Ga and As migrate towards the surface.

1. Introduction

Passivation of GaAs surfaces requires a stable insulator with very small leakage currents apart from numerous other important features. Multiple-layer insulating films have therefore been grown anodically to achieve improved performance over the pure GaAs native oxides. In particular Al₂O₃ with its potentially wide energy gap of up to 8 eV has been considered a promising material. It is therefore useful to study the chemical compositional profiles of such structures by Auger spectroscopy. This work is also useful in the investigation of such properties as diffusion and high-field drift processes of material across an Al₂O₃ layer inserted into the native GaAs-oxide film.

Some preliminary results on plasma-discharge grown oxides on GaAs have been reported (Chang *et al.* 1977). In this paper we present further data on electrolytically grown oxides, based on the AGW electrolyte (Hasegawa and Hartnagel 1976). Earlier published findings are in fact confirmed here. However, several important further details are reported which are relevant for the correct selection of manufacturing parameters for device applications.

2. Experimental procedures

All oxide layers described in this work were grown in the AGW electrolyte (Hasegawa and Hartnagel 1976) under illuminated conditions. The pH value and the temperature of the electrolytic bath were kept at 2.5 and 5 °C respectively. Composite oxide structures were achieved by first depositing the desired thickness of the Al film on a chemically-polished, cleaned and chemically-etched surface of GaAs and anodizing the whole structure until all the Al was converted into Al₂O₃. Anodization was then continued, in order to grow GaAs native oxide layers. The thickness of each oxide layer was estimated by the overpotential rise during the growth of the corresponding layer (Bayraktaroglu and Hartnagel 1978). Annealing of some samples was carried out in N₂ ambient at 350 °C for 15 min with 100 °C min heat-up and cool-down cycles.

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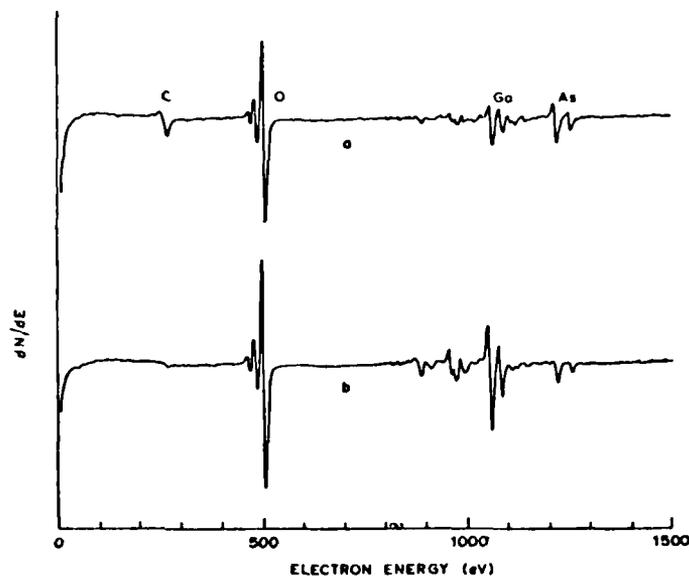


Figure 1. First derivative Auger spectra from anodized GaAs surface, illustrating electron beam effects. (a) using a $0.5 \mu\text{A}$ electron beam and (b) using a $5 \mu\text{A}$ electron beam. The data were taken using a sinusoidal modulation of 6eV peak-to-peak and a 0.3s time constant.

Auger measurements were performed with a scanning Auger microprobe (Physical Electronics Industries Model 545). Auger spectra were recorded in the usual first derivative form, dN/dE , and the intensities presented are the peak-to-peak heights (Joshi *et al.*, 1975). Serious changes in surface composition were noted when a 5keV , $5\mu\text{A}$ electron beam (rastered to produce 1.25mA/mm^2 current density) with a $25\mu\text{m}$ diameter was used. These changes could be eliminated by using a $0.5\mu\text{A}$ electron beam (rastered to produce a $5\mu\text{A/mm}^2$ current density). Figure 1 illustrates the changes in surface composition due to electron bombardment; the Auger spectra obtained for the $0.5\mu\text{A}$ and $5\mu\text{A}$ electron beam current are shown in Figs. 1 (a) and (b) respectively. The figure indicates a decrease in the As and C surface concentration for the $5\mu\text{A}$ beam. During profiling the beam current could be increased to $1\mu\text{A}$ without significant effect on the Auger measurements. The depth profiles were obtained by sputtering with 2keV Ar ions. The Ar ion beam width was approximately 1mm . Carbon was observed on all specimens; however, it decreased rapidly on sputtering, indicating a surface contamination.

Results and discussions

By first depositing a thin layer of Al on GaAs, anodic oxidation occurs initially of the total Al layer and subsequently of the underlying GaAs. This second oxidation has to involve transport of either oxygen to the interface (either interstitially or substitutionally as a vacancy) or Ga and As to the oxide surface or any combination of both. It is then possible, by studying the position of Al in the oxide by Auger analysis, to derive the ratio of the transport of Ga, As and oxygen species. However, the data must be considered on a qualitative basis; since the oxides are composites,

their ion etch rates are not known and therefore the ion etch time may not be proportional to the thickness of the film sputtered off.

Such measurements were undertaken with samples where the oxide was grown using different current densities and different Al and native oxide thicknesses. It was found for samples with 100 Å of Al and 1000 Å of native oxide that the Al peak position depends on the current density of growth (Fig. 2). With a current density of $100 \mu\text{A cm}^{-2}$, the ratio of the sputtering times below and above the Al peak is 1.5 whereas this number is 2.9 for a current density of $10 \mu\text{A cm}^{-2}$; the ratio of these numbers is 0.52, which was found to be independent of sample annealing. The above etch times were obtained from the Al and Ga signals at the halfpoints on the signal variations.

Unfortunately, it is not possible to use the amplitude of the Auger lines from the raw data as a measure of the elemental concentrations, as effects like Auger line shape changes, electron escape depth and preferential etching have not been taken into consideration. This problem was seen in the Ga Auger signals in going from the anodized GaAs to the GaAs, where the Ga signal indicates a dip. This dip is probably not due to a large decrease in Ga concentration but is mainly due to the fact that the Auger peaks from oxidized Ga and from Ga in GaAs appear at different energies. Techniques developed to overcome these problems in depth profiling (Grant *et al.* 1976) cannot be directly applied here owing to the small energy separation of the Ga and As lines. Such effects might also be responsible for the observation that the

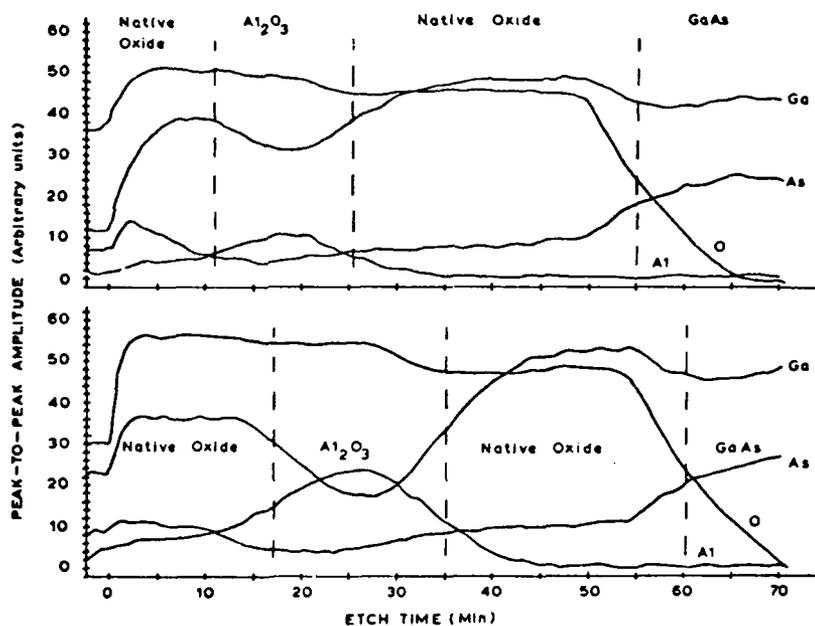


Figure 2. Depth profiles of GaAs with 100 Å of Al deposited following anodization. The anodization was continued until 1000 Å of native oxide was grown, as determined by the overpotential during film growth. Samples were anodized with current densities of $10 \mu\text{A cm}^{-2}$ (upper trace) and $100 \mu\text{A cm}^{-2}$ (lower trace). The oxygen Auger signal is shown attenuated by a factor of two. The data presented are raw data and the Al and oxygen noise levels can be seen in the GaAs region.

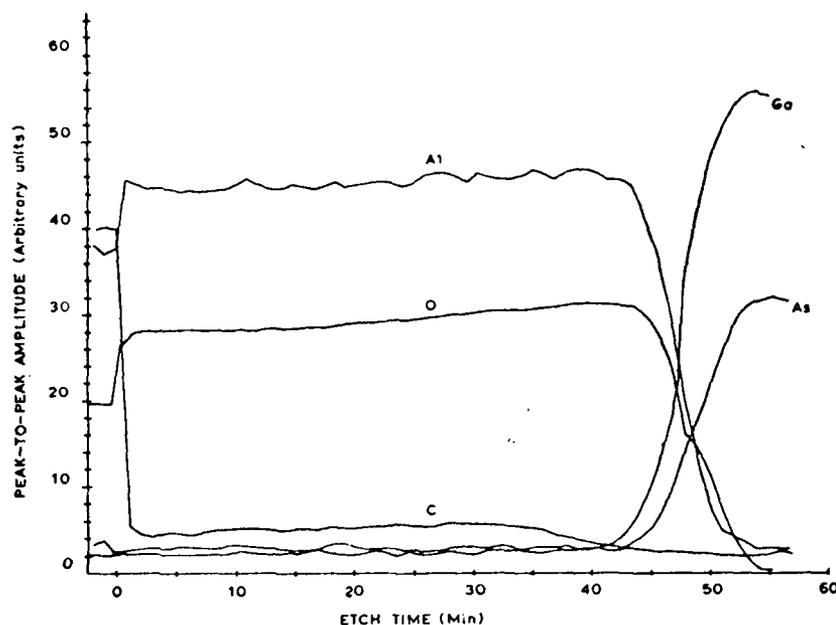


Figure 3. Depth profile of GaAs with 650 Å of Al deposited following anodization. Note the presence of approximately 2% carbon through the oxide. The oxygen signal was attenuated by a factor of five.

oxygen concentration underneath the Al peak appears to be about 15% lower than that above the Al peak (lower curves in Fig. 2). However, it is possible that there is a real phenomenon which would indicate whether the native oxide underneath the Al consists of either an oxide which is based on less oxygen atoms (say As_2O_3 rather than As_2O_5 , or Ga_2O_3 and As_2O_3 instead of GaAsO_4) or incompletely oxidized Ga and As. Further work in this area is planned.

It is also found that Al reaches through the oxide from its peak to the surface with reducing densities (Fig. 2), whereas the oxide underneath the Al peak does not exhibit any Al. This seems to indicate either that Al can be broken out of Al_2O_3 , ionized and drifted by the high growth field to the oxide surface, or that the oxygen transport from the oxide surface is so strong that any Ga and As ions drifting towards the surface are caught and ionized by these oxygen species before they reach the surface. This process could be associated with an ionized oxygen-vacancy drift towards the surface (Breeze *et al.* 1978). Another explanation for the surface composition could be that Ga and As diffuses along defects in the aluminium oxide and the aluminium surface is partially covered with Ga-oxide and As-oxide.

Within the Auger sensitivity, no C was found in the bulk of the oxide when the films were grown with current densities less than $100 \mu\text{A}$ while with higher current densities approximately 2 at. % residual carbon is observed in the oxide (Fig. 3). This indicates that the glycol-based electrolyte may incorporate carbon based anodic fragments into the oxide film during growth at very high densities.

With 1000 Å thick Al_2O_3 and a thick GaAs-oxide, we always find GaAs-oxide on top and below the Al_2O_3 , but the Al_2O_3 contains only minute amounts of Ga and As

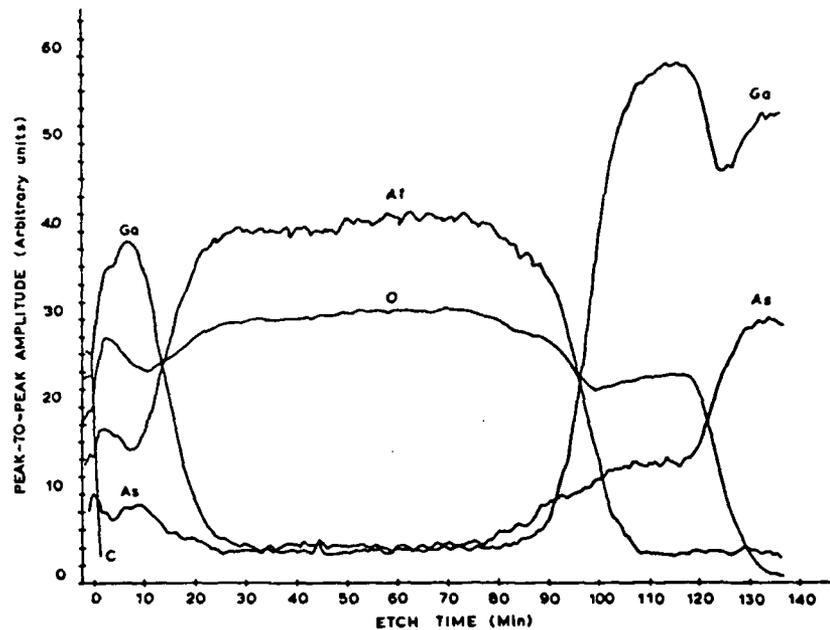


Figure 4. Depth profile of GaAs with 650 Å of Al deposited following anodization. The Al_2O_3 was approximately 1000 Å and the native oxide 700 Å as determined from the overpotentials. The oxygen signal was attenuated by a factor of five.

(Fig. 4). The etch time ratio for top and bottom GaAs-oxides does not seem to depend on anodization current density and does not depend on the GaAs-oxide thickness. However, for structures with thick Al_2O_3 (1000 Å) and thin GaAs-oxide (100 Å estimated from the anodization $V-t$ curves), no discrete native oxide layer was observed by Auger measurements for current densities of $100 \mu\text{A cm}^{-2}$ and above; for smaller current densities, native oxide was observed both on top and below the Al_2O_3 . Layered composite oxide formation is consistent with the memory effects observed previously (Bayraktaroglu *et al.* 1977). In all our measurements, the native oxides on top of the Al_2O_3 appear As deficient. If only thin native oxides are grown (100 Å) after establishing 150 Å of Al_2O_3 it was observed that no native oxide forms on top of the Al_2O_3 , although some Ga is always observed on the surface.

4. Conclusion

It is shown here that Auger spectroscopy of oxides on GaAs can give information on the transport mechanism during anodization of the elements forming the oxide. It is shown that GaAs-oxide usually forms both on top and below Al_2O_3 films. With thick Al_2O_3 films (1000 Å) only minute amounts of Ga or As can be observed by Auger spectroscopy in the Al_2O_3 .

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Ohmic contacts to InP

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The problems involved in making Sn-Ag ohmic contacts to InP have been investigated. The technique of thin film epitaxy has been adapted so that the problems have largely been overcome, resulting in high-quality ohmic contacts whose contact resistance is less than the measurement error and whose barrier height is too low to be detected. These ohmic contacts were used for the contacts of InP Gunn oscillators, and efficiencies somewhat less than 9% could be obtained, in agreement with theoretical predictions.

1. Introduction

Typical ohmic contacts on III-V compound semiconductors consist of vacuum deposition of suitable metals followed by an alloying cycle in an inert atmosphere. The temperature and time of this alloying cycle have to be limited to prevent disassociation of the semiconductor surface due to the greater evaporation rate of the group V element, unless special precautions are taken. The loss of this component is particularly serious for ohmic contacts because of the relatively thin layer of single-crystal regrowth underneath the metallization (Sebestyen *et al.* 1975). Therefore a process called T.F.E. (Thin Film Epitaxy) was developed for the fabrication of high-quality ohmic contacts onto GaAs. This new process includes a thin layer of Ga in the normal metallization and subsequent annealing in an atmosphere of As using a slow temperature cycle. Here similar results are presented for InP.

2. Sn-Ag ohmic contacts

A common technique for producing ohmic contacts onto InP is to vacuum-deposit Sn and Ag and then subsequently to anneal in an atmosphere of hydrogen at 450–500°C for 1 min. It was previously reported (Becker 1973) that such contacts have a non-uniform surface and non-linear I-V characteristics.

An investigation of the Sn-Ag ohmic contact metallization was conducted using epitaxial n on n^+ InP with $n \sim 10^{15} \text{ cm}^{-3}$ and $p \sim 1 \Omega \text{ cm}$, and the epitaxial layer being $16 \mu\text{m}$ thick with a crystal orientation of $\langle 100 \rangle$.

Prior to evaporation, the semiconductor slices were cleaned by boiling in trichloroethylene, acetone, methanol and chloroform. The surface was then etched in the pre-evaporation etch using HCl, HNO₃ and H₂O in the ratio 2 : 2 : 1. Although this has a rather fast etch rate of $\sim 2 \mu\text{m min}^{-1}$, a 10 s etch was found to leave the surface flat and undamaged when examined with an S.E.M. and X-ray analysis.

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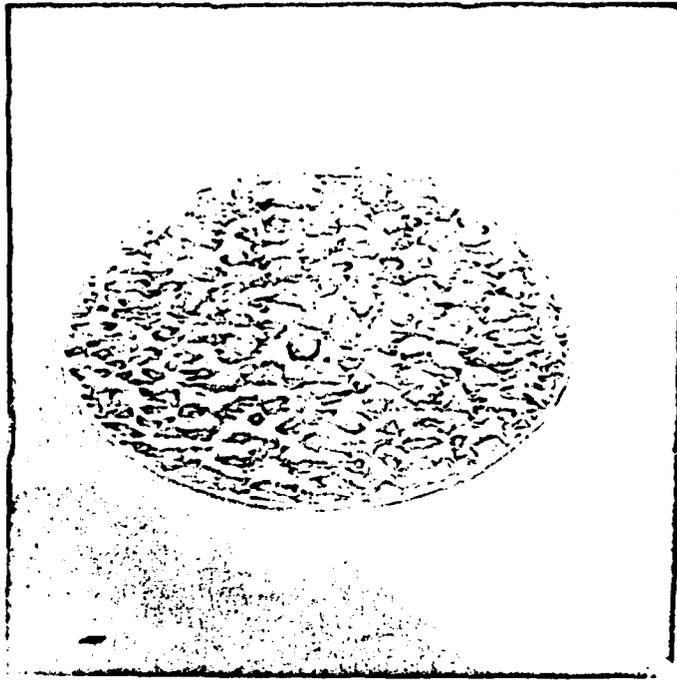


Figure 1. S.E.M. micrograph of a Sn-Ag ohmic contact alloyed for 1 min (magnification $\times 480$).

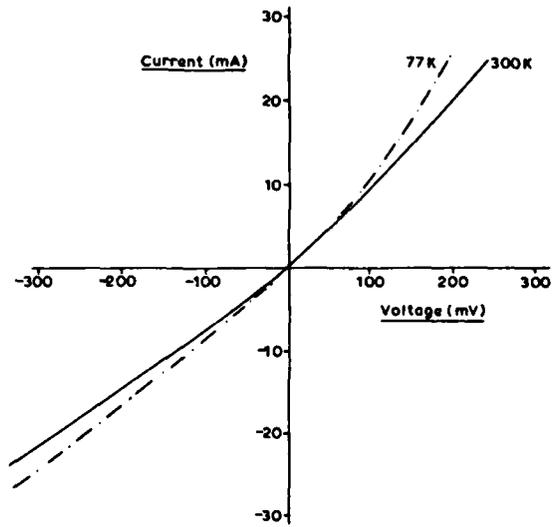


Figure 2. $I-V$ characteristics of Sn-Ag ohmic contacts.

The metallization used was 1200 Å Sn + 4000 Å Ag deposited by thermal evaporation in a vacuum of $<10^{-6}$ Torr. When subsequently annealed in an atmosphere of H_2 at $470^\circ C$ for 1 min, the resulting surface can be seen in Fig. 1 to be very non-uniform and the resulting I-V characteristics, shown in Fig. 2 at 300 K and 77 K are both non-linear. The specific contact resistance at 300 K is $4.6 \times 10^{-4} \Omega \text{ cm}^{-2}$ using Brooks and Mattes' (1971) equation to calculate the effect of spreading resistance.

E.D.A.X. (Energy Dispersive Analysis of X-rays) of the contact revealed that the 'hills' are composed mainly of Sn-Ag and the valleys of In-P, showing that the problem is de-wetting of the contact from the InP surface during the alloying cycle.

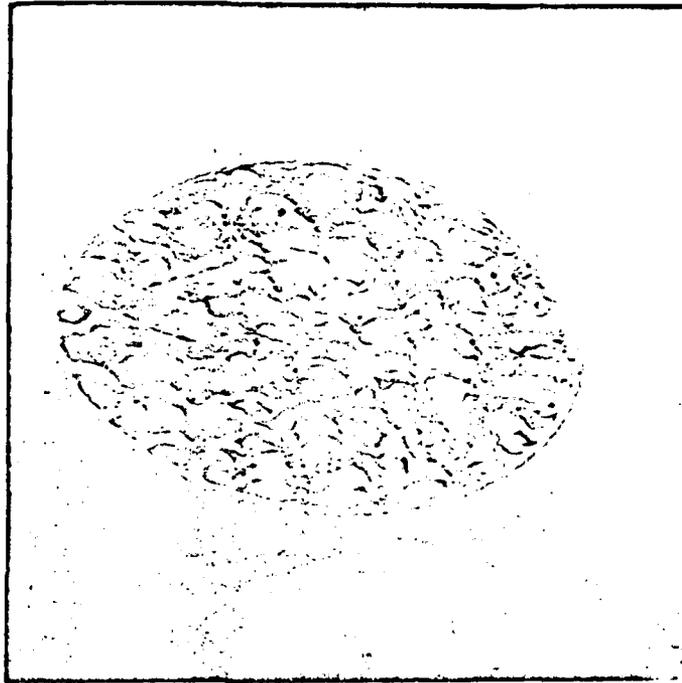


Figure 3. S.E.M. micrograph of a Sn-Ag ohmic contact alloyed for 5 min (magnification $\times 485$).

Increasing the alloying time resulted in the deterioration of the surface accompanied by an increase in the contact resistance. A typical contact, alloyed for 5 min, is shown in Fig. 3. The resulting specific contact resistance is $1.97 \times 10^{-3} \Omega \text{ cm}^{-2}$.

Higher alloying temperatures gave no improvement, and an extreme case for an alloying temperature of $600^\circ C$ is shown in Fig. 4, where some violent reaction can be seen to have taken place. E.D.A.X. spot analysis showed that, as before, the hill is composed of Sn-Ag but this time the 'valley' is mainly In and Ag with very little phosphorus present. In his investigation of the evaporation of InP, Farrow (1974) found that under Langmuir (free

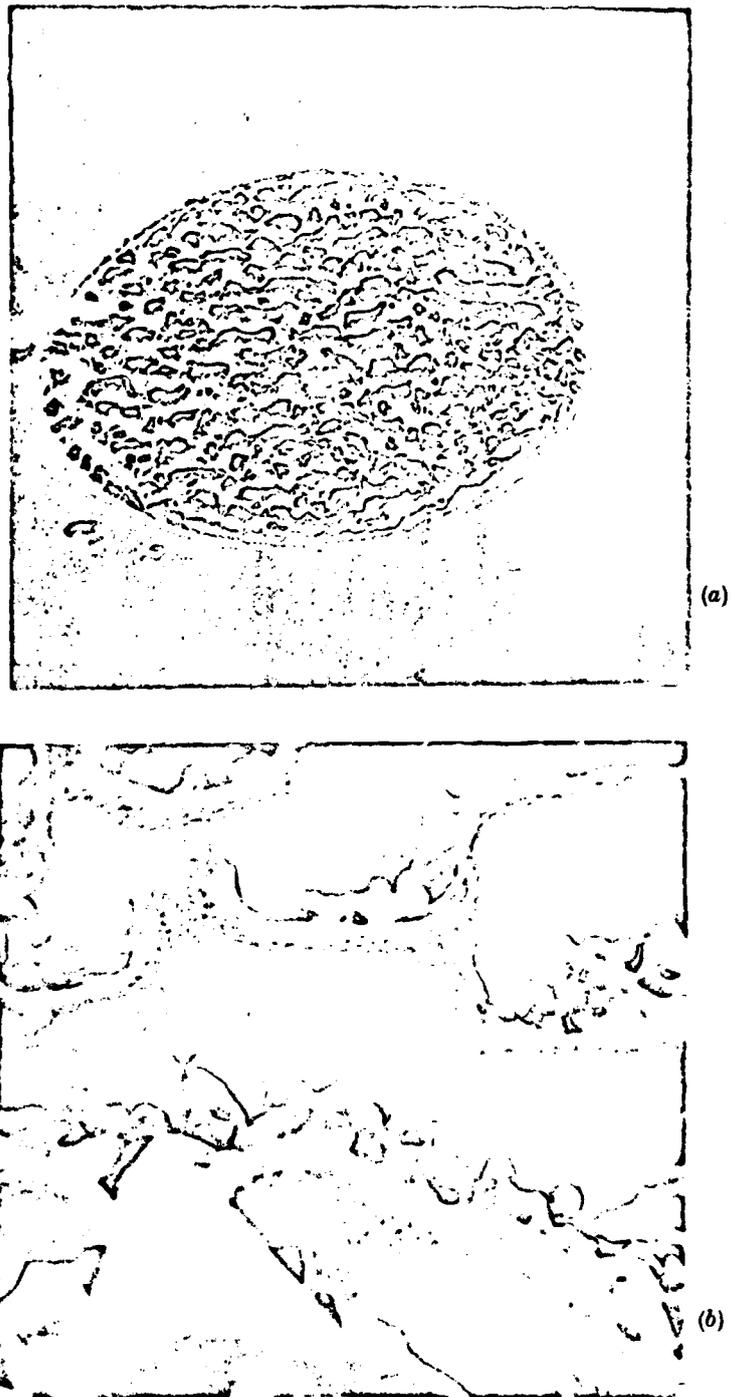


Figure 4. S.E.M. micrograph of a Sn-Ag ohmic contact alloys at 600°C (magnification (a) $\times 520$, (b) $\times 5200$).

evaporation conditions congruent evaporation occurs up to 356 °C, above which temperature the loss of phosphorus becomes greater than that of indium.

All these observations indicate the problems involved in making ohmic contacts to InP, i.e. 'balling up' or de-wetting of the contact metals and a loss of phosphorus during the alloying cycle.

3. T.F.E. grown ohmic contacts

The techniques developed for GaAs were adapted for InP where, of course, the arsenic vapour has to be replaced by a suitable phosphorus atmosphere and the equilibrium vapour pressure of P over InP is much greater than for As over GaAs, therefore limiting the maximum alloying temperature. The InP used here has the same specification as that described in the previous section.

To overcome the de-wetting of the contact metals, a thin layer of In was evaporated prior to the other metals to act as a 'wetting agent' during the alloying. In addition it will also act as the basis of the newly grown InP layer if phosphorus is provided during alloying.

The metallization used was



which was subsequently alloyed in an atmosphere of phosphorus using a furnace similar to that described by Sebestyen *et al.* (1975) with a slow temperature cycle, as shown in Fig. 5. Phosphorus was provided by including a small piece (of the red allotrope) inside the furnace ampoule along with the sample to be alloyed.

The resulting surface of the contact shown in the S.E.M. micrograph, Fig. 6 (a), can be seen to be extremely flat and quite featureless, and even at $\times 10\,000$ magnification, Fig. 6 (b), appears granular. A standard photolithographic float-off procedure was used to define the circular dots.

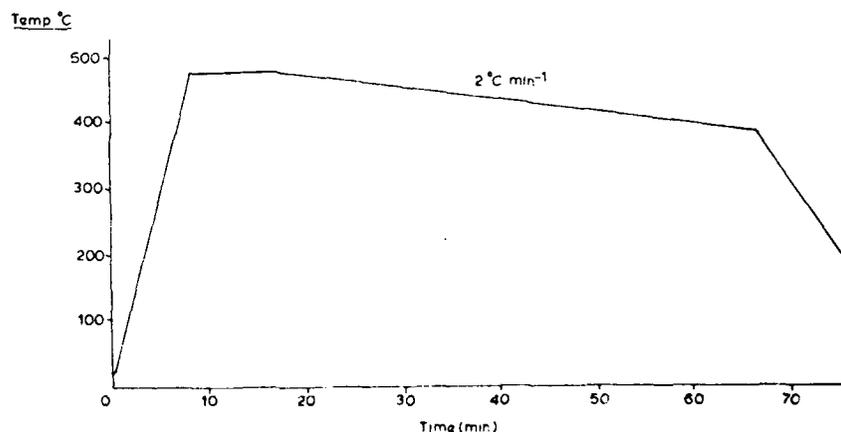


Figure 5. Alloying temperature cycle of T.F.E.-grown ohmic contacts.

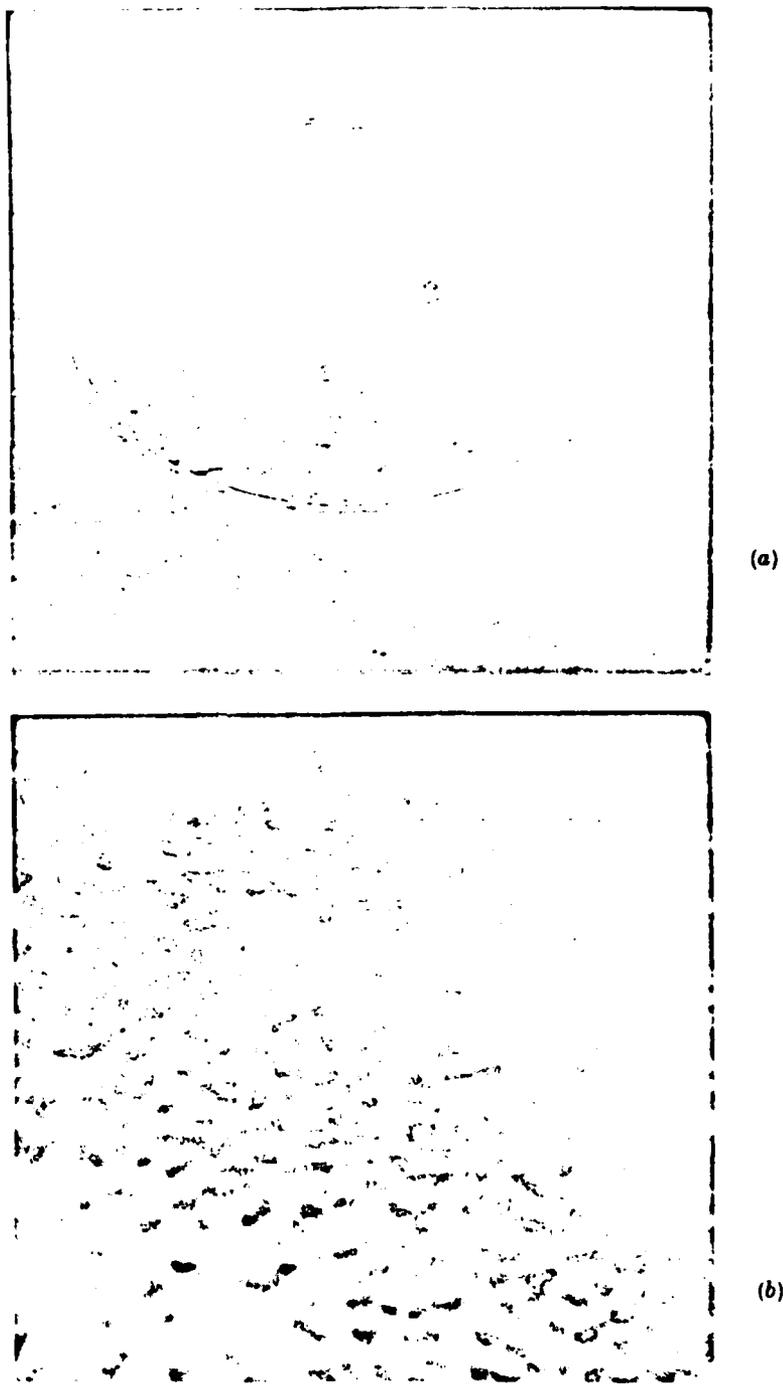


Figure 6. S.E.M. micrographs of the T.F.E.-grown ohmic contacts (magnification (a) $\times 510$, (b) $\times 10\,300$).

At 300 K the I - V characteristic (see Fig. 7) is linear, giving a specific contact resistance (Brooks and Mattes 1971) below the measurement error, i.e. $<10^{-4} \Omega \text{ cm}^{-2}$. Using the method of Tantraporn splitting (Tantraporn 1970), an attempt was made to measure the barrier height, but was unsuccessful because no splitting in the voltage-temperature characteristic could be detected, even down to 77 K, i.e. the I - V characteristic at 77 K is linear (see Fig. 7).

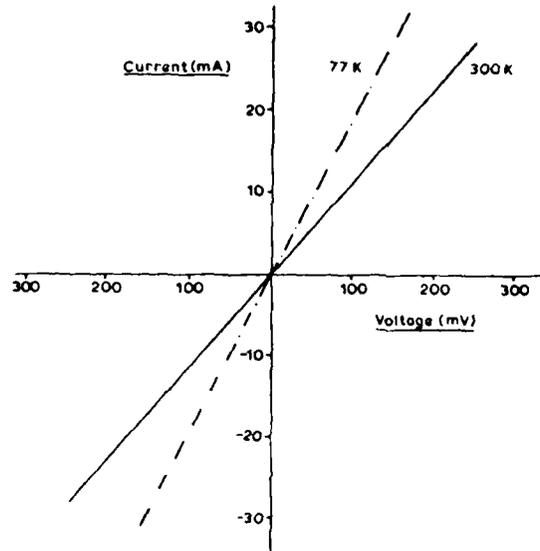


Figure 7 I - V characteristics of T.F.E.-grown ohmic contacts.

Another test commonly used on GaAs ohmic contacts is to compare the ratio of the conductivity at 77 K and 300 K with that predicted for the material. A similar test for InP presents difficulties due to the lack of relevant data, but the ratio of 1.76 obtained here for the T.F.E.-grown contacts seems to be in reasonable agreement with the limited information available (Tebbenham and Walsh 1975).

4. Gunn diodes

Gunn diodes with efficiencies as high as 22%, have previously been fabricated from InP (Colliver *et al.* 1974); this value is much greater than has been obtained from similar GaAs devices. The higher conversion efficiency was proposed to be due to two effects: the large peak-to-valley ratio of the electron velocity/field characteristic of InP, and the existence of a potential barrier at the cathode which permits the injection of hot electrons (Colliver *et al.* 1974).

Therefore a useful supplement to the ohmic contact work would be to fabricate some Gunn diodes using T.F.E. grown contacts and to test their characteristics.

4.1. Packaging

The T.F.E.-grown ohmic contact slices described in the previous section were cleared and mounted into S4 packages. Because the alloying temperature of these contacts was so low and InP so soft, it was essential that the use of Au-Ge solder and thermocompression bonding be avoided to prevent damage to the ohmic contact. The solder used had a melting point of 150°C, which is low enough to prevent any eutectic formation with the gold plating of the package. Although not very rugged, this method was adequate for the purpose required.

4.2. Pulsed $I-V$ characteristics

To prevent heating of the device, measurements were taken using a pulsed bias voltage of 25 ns duration with a repetition frequency of 75 Hz. The pulsed $I-V$ characteristic obtained is shown in Fig. 8, from which it can be seen that there is only a small 'current drop-back', and hence only a low conversion efficiency is to be expected.

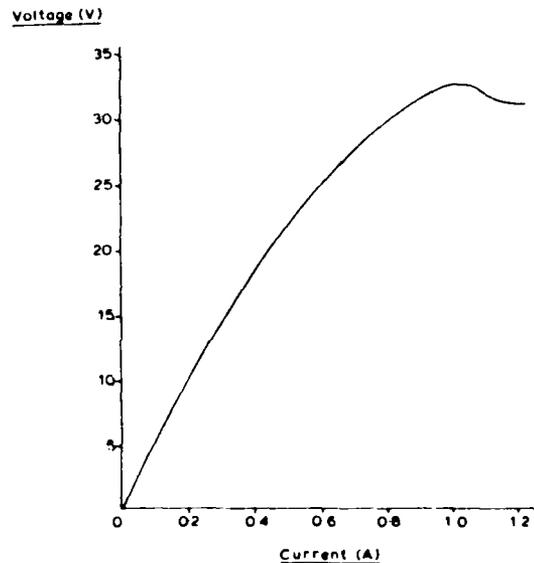


Figure 8 Pulsed $I-V$ characteristics of the InP Gunn diodes with T.F.E.-grown electrodes.

4.3. Microwave measurements

A coaxial cavity with a characteristic impedance of 50 Ω was used in conjunction with a HP181A sampling oscilloscope for all the microwave measurements. The diodes were biased with a pulsed supply as in the previous section. After optimizing all the variables, including bias voltage and cavity length, a maximum instantaneous efficiency of 3.1% was measured.

This is the overall efficiency and must therefore be corrected for the losses in the cavity. For a diode mounted in such a cavity, the overall Q is given by

$$\frac{1}{Q_t} = \frac{1}{Q_{ext}} + \frac{1}{Q_0} + \frac{1}{Q_d}$$

where the subscripts are t for total, 0 for unloaded cavity, ext for external circuit and d for the diode. These Q factors were determined by the impedance method (Ginzton 1957) and had the values

$$Q_{ext} = 128.9, \quad Q_0 = 69.1 \quad \text{and} \quad Q_d = 54$$

The previously determined efficiency can now be corrected for the losses in the cavity by the equation :

$$\eta_{corr} = \eta_{meas} \frac{1/Q_{ext} + 1/Q_0}{1/Q_{ext}}$$

to give a value of 8.9%.

This is low compared to the maximum value of 22% obtained by Colliver *et al.* (1974). Hence these high efficiencies obtained in InP Gunn diodes are due to a property of the cathode contact rather than of the material.

5. Conclusions

The difficulties involved in making an ohmic contact to InP comes from the de-wetting of the contact metals and a loss of phosphorus during the alloying cycle. T.F.E. has been applied to produce very high-quality ohmic contacts to InP with negligible specific contact resistance and a barrier height too low to be determined by Tantraporn splitting.

When this technique was used to form the contacts of Gunn diodes, low efficiencies were obtained confirming that efficiency is related to a property of the cathode contact.

ACKNOWLEDGMENTS

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CRYSTALLIZATION DYNAMICS OF NATIVE ANODIC OXIDES ON GaAs FOR DEVICE APPLICATIONS

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The structure of as-grown and annealed native oxide layers on (100) GaAs was studied using X-ray diffraction, reflection electron diffraction and microprobe analysis. The results show that crystalline β -Ga₂O₃ is present at the oxide-GaAs interface either when the oxide is grown using a current density larger than 2 mA cm⁻² or when it is annealed at temperatures above about 600 °C. The gallium excess with respect to arsenic is more pronounced for the oxides grown with a low current density than for the high current cases. Further, a loss of arsenic is found to occur during annealing.

1. INTRODUCTION

To date the anodic oxidation of GaAs using an electrolyte consisting of tartaric acid and glycol¹ has been found to produce oxide layers which have improved electrical and interface properties² and which are more suitable for device applications than oxide layers produced by other methods including thermal oxidation. The layers produced by anodization are very uniform and the process is highly reproducible. Such oxide layers have been used to realize depletion mode³ and inversion mode⁴ metal oxide semiconductor field-effect transistors (MOSFETs) on GaAs. Surface passivation and impurity diffusion barriers are two other device applications. The anodic oxidation technique has been used to determine the electrical properties of n-type GaAs⁵, for the analysis of multicomponent films on GaAs⁶, for the controlled removal of GaAs (as in the production of thin semiconductor samples for transmission electron microscopy (TEM) experiments⁷) and for the oxidation of InP⁸.

Many of these applications require the oxide to exhibit structural stability when it is subjected to various annealing processes. A preliminary study⁹ of the structural properties of these oxide layers has shown that β -Ga₂O₃ is present at the GaAs-oxide interface when oxide growth current densities of between 1 and 2 mA cm⁻² are used. The effects of annealing on the electrical properties of these oxide layers have shown them to be suitable for MOS applications¹⁰. Consequently to obtain a better knowledge of the thermal variation of the oxide properties a detailed

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study is required of the effects of annealing native oxide layers fabricated by using a variety of growth parameters.

Results are presented here which show the changes in crystallographic structure, crystallinity and chemical composition as functions of growth rate (initial current density) and annealing parameters (annealing temperature, time and ambient atmosphere). Finally the chemical resistance of the oxide to attack by HCl is assessed.

2. EXPERIMENTAL METHOD

The material used for these experiments was (100)-oriented bulk single-crystal silicon-doped GaAs ($n = 2 \times 10^{17} \text{ cm}^{-3}$) which was supplied by MRC with one face etch polished with bromine methanol. The GaAs was cleaved into samples approximately 5 mm \times 3 mm in area which were cleaned in an ultrasonic cleaner using acetone, trichloroethylene, methanol and chloroform.

Native anodic oxide layers were produced on the samples by anodization in an electrolyte consisting of tartaric acid in glycol, the pH of the solution being adjusted to 6.3 by the addition of NH_4OH . The oxide layers were grown using several values of the initial current density in the range 0.1–2.0 mA m^{-2} and a constant voltage supply. The current density was changed by varying the resistance in series with the electrolytic cell.

The samples were annealed in a quartz furnace tube in an atmosphere of high purity nitrogen (oxygen free) supplied by BOC and the furnace temperature was accurately controlled using an electronic temperature controller so that the heat cycle used was reproducible. Before the samples were heated the furnace tube was flushed out with nitrogen to remove all the oxygen present, and oxygen was prevented from entering the furnace tube via the gas outlet by using a bubbler partially filled with glycerine. The form of the heat cycle used for the annealing is shown in Fig. 1: the sample was heated to the required temperature T_A as quickly as possible, was held at this temperature for 10 min and was then cooled at a rate of either 300 $^\circ\text{C h}^{-1}$ or 100 $^\circ\text{C min}^{-1}$.

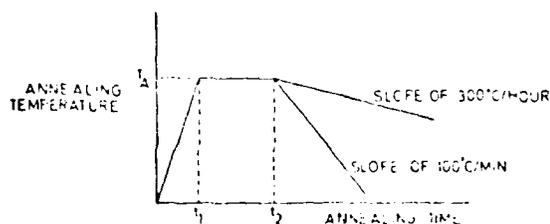


Fig. 1. The heating cycles used for the annealing processes.

The structure of the bulk oxide was determined by X-ray diffraction for which the samples were mounted on aluminium rods which were mounted in the specimen holder of a Philips X-ray diffractometer. A plot of X-ray count as a function of 2θ was obtained, where θ is the angle of incidence of the X-ray beam with the sample. A cleaned unprocessed sample of the GaAs was analysed and the (200) and (400)

reflections of GaAs, which also occurred in all the spectra of the oxidized samples, served as a calibration for each spectrum by determination of the 2θ scale of the instrument to find the instrumental peak-broadening factor. The radiation used here was $\text{Fe K}\alpha$ ($\lambda = 1.938 \text{ \AA}$).

The surface structure of the oxide layer was determined using an AEI ED2 electron diffraction camera. From the diffraction patterns obtained, the structure and orientation of the surfaces of the samples were determined. A scanning electron microscope fitted with a microprobe analyser was used to examine the surface topography and the chemical composition of the oxide layers.

For the determination of their chemical resistance the various oxide layers were etched in a 10 vol.% solution of HCl for 5 min, after which the etching was terminated by washing the samples in deionized water.

3. RESULTS

Initially a thin anodic oxide layer (approximately 50 Å thick) was grown on a GaAs sample using an initial current density of about 0.25 mA cm^{-2} . An examination of this sample using reflection electron diffraction showed that the surface was almost amorphous, its diffraction pattern consisting of several diffuse bands which are characteristic of amorphous native oxide layers on GaAs¹¹.

Another anodic oxide layer 2000 Å thick was grown with a current density of 1 mA cm^{-2} and was etched in HCl fumes to remove all but the last 50 Å (approximately) of oxide whose structure was determined by electron diffraction. The diffraction pattern consisted of dots arranged in rings which indicated that the material immediately adjacent to the GaAs surface was polycrystalline. The amorphous oxide was probably removed during the etching process to leave behind the crystalline oxide at the interface, unless crystallization was produced by the action of the HCl fumes on the remaining oxide layer.

Several samples were grown by using an initial current density of 1 mA cm^{-2} and were annealed in either arsenic or high purity hydrogen at 500 °C for 30 min. The samples annealed in an arsenic atmosphere were chemically analysed and were found to have a Ga:As ratio of 2:1, whereas the ratio was 2:1.5 before annealing; this change was coincident with a change in oxide thickness from 2000 Å (pink) to 1500 Å (green). When we take into account the penetration depth of the microprobe analyser this corresponds to a considerable loss of the arsenic component of the oxide. Since the presence of the arsenic atmosphere will inhibit the loss of arsenic from the oxide and since no significant arsenic loss is expected from the GaAs at this temperature¹² it can be concluded that the arsenic loss is due to the out-diffusion of arsenic oxide. A similar process has been reported recently¹³. The samples that were annealed in a high purity hydrogen atmosphere behaved in a very similar manner. However, on raising the annealing temperature to 600 °C and with the high purity hydrogen atmosphere the amorphous oxides were reduced to metallic gallium, as has been found previously¹⁴.

3.1. X-ray diffraction

For the anodized samples grown with an initial current density of 2 mA cm^{-2} the only peak present in the spectrum which was not also present in the spectrum of

the cleaned GaAs sample occurred at $2\theta = 40.6^\circ$ which corresponds to $d = 2.816 \text{ \AA}$. It was possible to determine the position of the peak accurately since the 2θ values of the peaks were very similar (39.45 and 40.00°) and since these two peaks were of a comparable magnitude (owing to the low intensity ($\approx 1\%$) of the (200) GaAs reflection and the small amount of anodic oxide present). The peak which occurs at $2\theta = 40.6^\circ$ for the anodized samples corresponds to the (200) reflection of $\beta\text{-Ga}_2\text{O}_3$, i.e. the $\beta\text{-Ga}_2\text{O}_3$ is (100) oriented. This is the most probable orientation of the $\beta\text{-Ga}_2\text{O}_3$ since its lattice constants in the (100) plane are very similar to those for the (100) plane of GaAs, and this was confirmed by the d spacings of the (200) reflections of $\beta\text{-Ga}_2\text{O}_3$ and GaAs which are 2.816 \AA and 2.832 \AA respectively. The change in the volume and the crystallite size with annealing temperature for the crystalline $\beta\text{-Ga}_2\text{O}_3$ are shown in Fig. 2, curves a; these results were derived from the intensity and the width at half intensity respectively of the peak. The results show that the unannealed samples contained an appreciable amount of crystalline $\beta\text{-Ga}_2\text{O}_3$ and that the total amount of crystalline material did not increase significantly until the samples were annealed above 450°C .

As the peak width is inversely proportional to the average size of the crystallites in the oxide, it can be seen that the crystallite size decreases initially with increasing annealing temperature up to 450°C , above which it increases rapidly. It should be noted of course that some of the observed variations in peak width, especially the decrease with increasing annealing temperature, may be due to other factors such as strain and variations in the chemical composition of the sample. In contrast, a real decrease in average crystallite size over a limited temperature range can be considered as an indication of a considerable formation rate of new single-crystal nucleation sites. At higher temperatures it will become more difficult to form clusters of molecules that are sufficiently stable to become single-crystal nucleation sites; thus only existing crystallites will grow and the average crystallite size will increase. Such an interpretation indicates that high annealing temperatures can be applied without considerable crystallization by going as rapidly as possible over the temperature range $350\text{--}450^\circ \text{C}$, both when heating and when cooling the samples. The experiments described below do indeed give some confirmation of this hypothesis.

A small but significant increase in the background of the spectra around $2\theta = 86^\circ \pm 3^\circ$ ($d \approx 1.4 \text{ \AA}$) was found which indicates that there may have been an immeasurably small amount of some other orientations of $\beta\text{-Ga}_2\text{O}_3$ present in the sample.

For the samples grown with an initial current density of 1 mA cm^{-2} the annealing process produced (100)-oriented crystalline $\beta\text{-Ga}_2\text{O}_3$, as found above. The variations of the amount and the crystallite size of the $\beta\text{-Ga}_2\text{O}_3$ with annealing temperature are presented in Fig. 2, curves b. The curves show that the unannealed samples contained no detectable amounts of $\beta\text{-Ga}_2\text{O}_3$, although after annealing at about 300°C some $\beta\text{-Ga}_2\text{O}_3$ was found. The average crystallite size of the $\beta\text{-Ga}_2\text{O}_3$ decreased up to an annealing temperature of about 500°C after which it increased, and this minimum in the average crystallite size coincides with a loss of the arsenic component of the oxide (see Section 3.3).

Finally, a series of samples was grown using a current density of 0.1 mA cm^{-2} and was annealed as described above. The results for these samples (Fig. 2, curves c)

are very similar to those obtained for the samples above except that a slightly higher temperature (about 450 °C) was required before the crystalline $\beta\text{-Ga}_2\text{O}_3$, which had a smaller average crystallite size, could be detected.

An important annealing parameter which was found to be relevant to the occurrence of crystallization at the oxide-GaAs interface was the cooling rate used at the end of the annealing cycle. Several samples were grown using a current density of 0.1 mA cm^{-2} and were annealed at 600 °C as described above except that the cooling rate used was 100 °C min^{-1} instead of 300 °C h^{-1} . The quickly cooled samples showed no crystallization at the interface between the oxide and the GaAs. Thus with a high cooling rate the material does not have enough time to arrange itself in a crystalline form and is "frozen" in an amorphous type of structure.

Although the cooling effect was only measured for an annealing temperature of 600 °C there is no reason why a similar effect should not take place at other annealing temperatures.

The effect of the annealing time was studied on the samples which were found to be the most crystalline, *i.e.* those grown with a current density of 2 mA cm^{-2} . By varying the annealing time from 10 to 60 min at a temperature of 600 °C it was found that the average crystallite size increased with increasing annealing time (Fig. 3) with no significant change in the total volume of the crystalline $\beta\text{-Ga}_2\text{O}_3$. This can be considered to be due to the movement and coalescence of the individual crystallites produced during the increased annealing time.

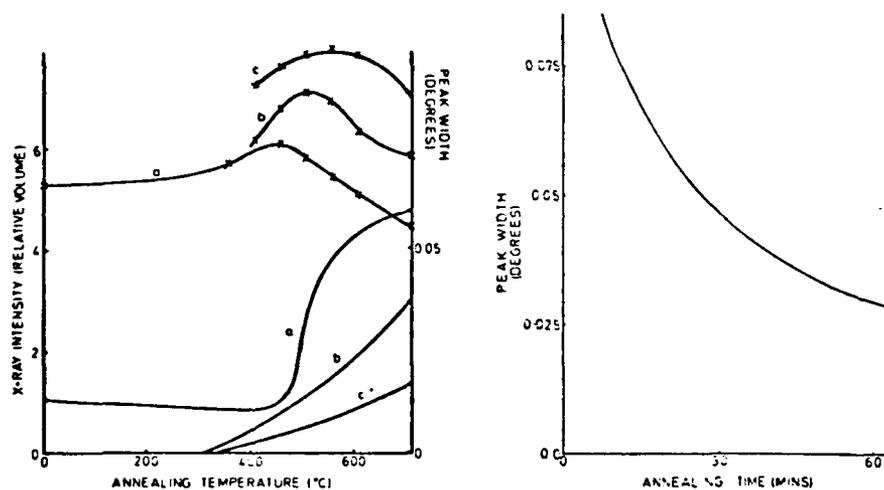


Fig. 2. The variation with annealing temperature of the X-ray intensity and of the peak width (\times) at half height for the (200) reflection of $\beta\text{-Ga}_2\text{O}_3$ for samples grown with current densities of 2.0 mA cm^{-2} (curves a), 1.0 mA cm^{-2} (curves b) and 0.1 mA cm^{-2} (curves c).

Fig. 3. The variation with annealing time at 600 °C of the peak width at half height for the (200) reflection of $\beta\text{-Ga}_2\text{O}_3$ for samples grown with a current density of 2.0 mA cm^{-2} .

The effects of the absorption of the X-rays in the amorphous oxide layers have been neglected in all of the above results. An estimate of the average crystallite size of the $\beta\text{-Ga}_2\text{O}_3$ for a peak width at half height of 0.05 gives a value of about 150 Å.

3.2. Reflection electron diffraction

An analysis of the electron diffraction patterns produced by the samples grown with initial current densities of between 2.0 and 0.1 mA cm⁻² shows that the surfaces of all of the unannealed oxides were amorphous. However, after annealing during the fabrication of Au-Ge ohmic contacts on the back faces of the samples, the surfaces of the oxides became slightly ordered and produced diffraction patterns which consisted of several very diffuse rings, as was found previously¹¹, which were due to amorphous native oxides present on the GaAs surface.

For samples that were grown using current densities of between 2.0 and 0.1 mA cm⁻², were annealed and then were cooled at a rate of 300 °C h⁻¹, an analysis of the electron diffraction patterns showed that the surface crystallized out into a polycrystalline β -Ga₂O₃ structure with only the rings corresponding to the $(h0l)$ reflections being present. As the annealing temperature was raised the rings of the diffraction patterns became sharper, indicating an increase in the average crystallite size. Another effect which was observed at high annealing temperatures, especially for the samples grown using a current density of 2 mA cm⁻², was that only rings corresponding to the $(10l)$ reflections were visible, indicating that this structure had become more oriented. However, annealing at 800 °C produced a pattern consisting of spots and rings that indicated the production of some crystals of β -Ga₂O₃. The crystallite size was found to be a function of the growth current density, the larger crystallite size being present in the samples grown with a higher current density, as was found by X-ray diffraction.

By using the annealing process with the fast cooling rate of 100 °C min⁻¹ even a sample annealed at 700 °C for 10 min was found to be almost amorphous. In Fig. 4 its diffraction pattern is compared with that of a sample that had been grown with 0.1 mA cm⁻², had been annealed at 500 °C and had been cooled at a rate of 300 °C h⁻¹.

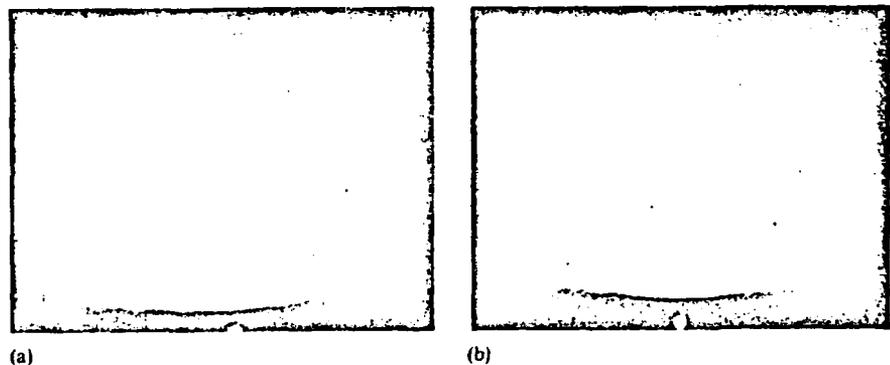


Fig. 4. Reflection electron diffraction patterns of samples grown with a current density of 0.1 mA cm⁻² and annealed (a) at 500 °C with slow cooling and (b) at 700 °C with fast cooling.

Thus the crystallization at the surface of the oxide is much less pronounced than that at the interface. From a knowledge of the electron beam penetration and the approximate angle of incidence of the beam with the sample, the depth of the analysed material can be estimated to be about 50 Å. This surface crystallization of

course occurs on an amorphous bed of oxide, unlike the interfacial crystallization detected by X-ray diffraction which takes place on a single-crystal GaAs substrate with a reasonable lattice match.

3.3. Scanning electron microscopy and microprobe analysis

Scanning electron microscopy (SEM) showed all the sample surfaces except that of the sample annealed at 800 °C to be extremely flat apart from very occasional defects which were thought to be due to some contamination of the sample surface. A micrograph of the surface of the sample annealed at 800 °C (Fig. 5) indicates the presence of crystallites. Consequently it is thought that this sample had completely crystallized, and this is confirmed by the electron diffraction patterns obtained for this sample.



Fig. 5. An SEM micrograph of a sample grown with a current density of 2.0 mA cm^{-2} and annealed at 800 °C. (Magnification, 7650 \times .)

For the microprobe analysis the $K\alpha$ X-ray lines were used in preference to the $L\alpha$ lines because of their greater peak separation (resolution). Allowances were also made for the relative yields for each of the peaks. Since the volume of emission could not be restricted to the oxide layer alone, some of the measured X-ray signal was produced in the GaAs structure.

The variation of the As:Ga ratio with temperature for the samples grown with a current density of 2 mA cm^{-2} (Fig. 6) shows that there was little change in the As:Ga ratio except in the sample annealed at 800 °C, which gave an As:Ga ratio of 0.34. However, annealing at this temperature also produces changes in the GaAs substrate¹² (a loss of arsenic) which will ultimately affect the annealing behaviour of the oxide layer since the GaAs-oxide interface may be destroyed. This dramatic decrease in the As:Ga ratio is due to the loss of arsenic from both the oxide layer and the GaAs substrate.

For the samples grown with a current density of 1.0 mA cm^{-2} the results for the variation of the As:Ga ratio with annealing temperature (Fig. 6) show that there is a significant loss of the arsenic component of the oxide between 400 and 500°C . This loss coincides with a change in the colour of the oxide from blue to purple which indicates a change in the oxide thickness from 1000 \AA to about 850 \AA . Since no such arsenic loss is known to occur in GaAs¹² this change must come from the oxide, as has been found previously for oxides grown using other electrolytes¹³, and it is thought to be due to the loss of As_2O_3 owing to the high vapour pressure of As_2O_3 at relatively low temperatures¹⁵.

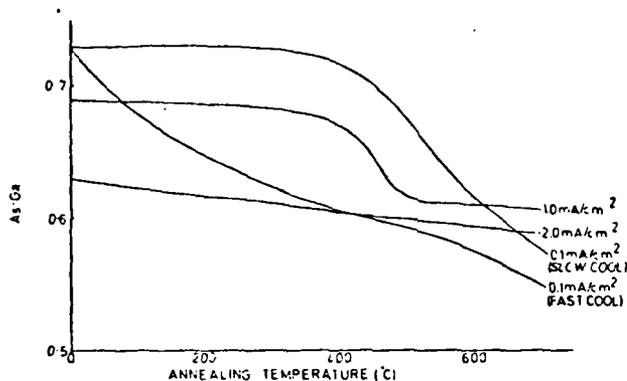


Fig. 6. The variation of the As:Ga ratio of samples grown with current densities of 2.0 , 1.0 and 0.1 mA cm^{-2} , annealed at various temperatures and then cooled at either $300^\circ \text{C h}^{-1}$ or $100^\circ \text{C min}^{-1}$.

Samples which had been grown with a current density of 0.1 mA cm^{-2} and which had been annealed using both the fast ($100^\circ \text{C min}^{-1}$) and the slow ($300^\circ \text{C h}^{-1}$) cooling rates were analysed (Fig. 6). The results indicate a difference in the arsenic content of the samples due to the two different cooling rates; this demonstrates the complex chemical nature of these oxide layers which can only be studied properly using a more sensitive analytical technique such as Auger spectroscopy.

An Auger analysis of some samples was undertaken. The analysis of some unannealed samples showed that the oxide contained more gallium and less arsenic than was found in the stoichiometric GaAs substrate¹⁶. Also the energy of the gallium peak was found to shift from 1067 eV in the oxide to 1072 eV in the GaAs; this indicates a change in the bonding environment of the gallium atoms which can be explained by all the gallium in the oxide being present as Ga_2O_3 .

3.4. Etching in HCl

The oxides grown using a current density of 2 mA cm^{-2} were found to be soluble in the HCl solution apart from those annealed at 600°C for 60 min , whose thickness was reduced from 1000 \AA to about 600 \AA , and those annealed at 800°C , which were completely insoluble in the etchant. However, the oxides grown to a thickness of 1000 \AA with a current density of 1 mA cm^{-2} behaved slightly differently: those annealed at 600°C for 10 min were found to be again only partly soluble

(leaving a layer about 400 Å thick) whereas those annealed at 600 °C for 60 min were completely insoluble; the samples annealed at 600 °C for 30 min had properties between these two. For the samples grown with a current density of 0.1 mA cm^{-2} and cooled using the two rates, only those annealed below 500 °C were found to be soluble in the etchant whereas those annealed above 500 °C were found to be insoluble.

Since amorphous Ga_2O_3 is soluble in the etchant¹⁴ whereas crystalline $\beta\text{-Ga}_2\text{O}_3$ is insoluble, the above-mentioned etching experiments provide further evidence for the presence of $\beta\text{-Ga}_2\text{O}_3$ at the GaAs-oxide interface and show that it increases with annealing temperature and time. At low annealing temperatures where the amount of crystalline $\beta\text{-Ga}_2\text{O}_3$ is small, any isolated crystallites are probably washed away with the surrounding amorphous material.

The residual etched surfaces were studied using SEM and with the exception of the sample annealed at 800 °C were all found to be flat. However, it should be noted here that the resolution of the scanning electron microscope used was 250 Å or greater so that small crystallites, which might have existed, could not be seen.

4. DISCUSSION

A comparison of the results of the X-ray diffraction and the electron diffraction experiments shows that the predominant crystallization process occurs at the GaAs-oxide interface with a secondary crystallization process occurring at the oxide surface. This can be seen from the highly oriented nature of the interfacial oxide compared with the surface oxide as well as from the degree of order and the volume of the crystallization, both of which are greater for the interfacial process. The volume of the surface crystallization is much less than that of the interfacial crystallization since only the latter shows up in the X-ray spectra. These two crystallization processes can be considered to be independent of each other since the orientations of the two crystallized layers are different. Consequently the bulk of the oxide which lies between the two crystallized layers is likely to exhibit an amorphous structure.

With current densities of 1 mA cm^{-2} and less the as-grown oxide layers are amorphous, whilst those grown using higher current densities are found to have a crystalline interfacial oxide layer. After annealing to sufficiently high temperatures and slow cooling, a crystalline interfacial layer is produced in the oxide, and the annealing temperature at which crystallization is detected is an inverse function of the growth current density used.

For the short annealing times used here (*i.e.* 10 min) slow cooling produces crystalline layers and rapid cooling produces non-crystalline layers. If longer annealing times are used, the material has time to rearrange itself into a crystalline structure so that the effect of the cooling rate will vanish. However, this assumes that the increased annealing time does not produce a change in the overall chemical composition of the layer.

At all times it is the gallium component of the oxide which determines the structure of the film whereas the arsenic component appears to be present in an amorphous form that is easily removed by annealing if the oxide is grown at a low current density.

5. CONCLUSIONS

The presence of crystallinity in the oxide layer at the GaAs oxide interface is generally considered to be detrimental to the electrical interface properties of any device using an MOS structure. In order to retain a suitable amorphous structure after annealing, the following conditions have been found to be important: (1) a current density of 0.1 mA cm^{-2} ; (2) annealing in nitrogen and a very fast cooling rate at the end of the heating cycle; (3) the lowest possible annealing temperature and the shortest possible annealing time.

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CHEMICAL REACTIONS OF OXIDE LAYERS ON GaAs

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The interface of GaAs and its native oxide exhibits a region of excess As. The amount of this excess is increased by laser annealing of the oxide layers; a corresponding change of the depletion layer capacitance is observed. The migration of As out of the surface of GaAs is clearly observed when Al is deposited on GaAs but not when Ga is deposited on GaAs. MOS structures are formed by a series of new processing steps that avoid the formation of excess As in the insulator region and As vacancies in the semiconductor region of the interface. The C-V characteristics of these structures show improvements over those produced by conventional oxidation methods.

1. INTRODUCTION

It is possible that oxide insulators will be attractive for GaAs surface passivation of various types of applications such as MESFET, optical devices and MOS structures. It is therefore important to study the relevant chemical reactions which occur during the formation of a native oxide. A series of experimental observations are reported here which are considered to be a useful contribution towards an understanding of the basic processes involved.

It seems that there are two important processes, firstly, the difference of oxidation heats of formation for Ga and As suggests that more Ga_2O_3 is formed than As_2O_3 (the two most commonly found compounds), and secondly the destruction of the GaAs surface through such processes as the heat of condensation which seems to favor the removal of As atoms from the atomic layers near the GaAs surface.

2. Laser-Annealed Native-Oxide/GaAs Structures

Various authors^{1,2} have established that non-oxidized As atoms extend from the GaAs interface a distance of around 10 nm further into the oxide than non-oxidized Ga. It is likely that this is caused by the difference in the heats of formation which are 156 kcal/mole for As_2O_3 ³ and 257 kcal/mole for Ga_2O_3 ; these are both probably the most common components of native oxides on GaAs. Our ESCA measurements confirmed this behavior for unannealed, AGW grown⁴ GaAs MOS structures using the Varian XPS system and an Ar ion etching at 2 kV.

In order to investigate the effect of localized heating on such interfaces, a pulsed ruby laser (pulse duration 25 nsec, laser energy .3 Joule/cm², 5mm diameter spot size) was used to irradiate an AGW native oxide-GaAs structure. Since the oxide is transparent, most of the

energy is absorbed at the oxide/semiconductor interface so that this region containing the non-oxidized As is locally heated. Provided that the local temperature is not raised to catastrophic melting or even evaporation values, interesting effects on the interface behavior result. ESCA studies show that the thickness of the region with non-oxidized As in the oxide near the interface has been increased 2 or 3 times. Profiles of the Gallium (and Arsenic) ratios of the oxidized to the non-oxidized concentrations are shown in Fig 1. Obviously, oxygen from As_2O_3 nearest to the non-oxidized As region is transferred to the Ga of the GaAs near the interface, thus increasing the non-oxidized As region at both ends.

This capability of changing the amount of non-oxidized As gives us the possibility of studying its effect on the electrical behavior of GaAs MOS structures. Firstly, using the method of photopulse analysis⁵, the capacitance C_0 of the oxide alone can be determined for equivalent measurement frequencies around 1 kHz. It is found that C_0 is increased by up to 100% for such laser-annealed samples with an increased non-oxidized As region. The apparent donor concentration has decreased from 1.8×10^{16} to about $4.7 \times 10^{15} \text{ cm}^{-3}$, as shown in Fig. 2. Obviously, these As atoms create states which can be easily filled and emptied from the semiconductor so that the oxide capacitor appears to be reduced correspondingly in effective thickness. The measurement of high-frequency capacitance-voltage characteristics seem to indicate a strongly enhanced trap density which is obviously another electrical manifestation of the interface containing elemental As. Normal thermal annealing at 350°C does not produce such widening of the atomic As region.

3. As-Vacancy Generation

The second interface state and trap generating mechanism seems to be the process of the energy provision by the first-layer oxidation, or the heat of condensation in connection with various deposited materials. This supplied energy creates vacancies of either Ga or As which form traps in the semiconductor near the interface.

Clear evidence of As-vacancy creation was obtained when Al was evaporated onto GaAs in an MBE system and the resulting surface was analyzed by Auger measurements. It was found then that the deposition of 30nm of Al causes the Ga signal to disappear almost entirely whereas the As signal remains very strong (see Fig. 3). Obviously, As was removed from the GaAs by Al deposition, and accumulated on the deposited Al surface. This effect is representative of numerous other deposited materials.

The heat of condensation for Ga on GaAs, on the other hand, seems to be lower³ than that of Al on GaAs. This material was therefore also evaporated onto GaAs. Indeed, the Auger method demonstrated that after about 30nm of Ga the As signal had practically disappeared (See Fig. 4). The condensation of Ga does therefore not release sufficient energy to knock out As from the GaAs lattice near the surface.

It seems to be valuable to undertake this deposition scheme with many further materials, particularly also the various insulators potentially useful for surface passivation. As is well known, the deposited Al can also be transformed by electrolytic oxidation into a good insulator which would cover then the GaAs surface. The As vacancies in the semiconductor underneath the interface would then prevent one from obtaining satisfactory C/V curves since the Fermi level gets pinned by such traps.

It is therefore understandable that the following scheme of surface passivation presents promising features.

4. Two-Step Oxidation

In line with the understanding that any processing involving low reaction energies does not perturb the GaAs composition, and that further any region of atomic As has to be avoided, the following processing steps were used⁵: A thin native oxide layer (less than 15nm was AGW⁴-produced onto GaAs, which was then annealed for about 30 minutes in H₂ at 650°C. The As₂O₃ of this film is then mostly evaporated (a low-energy process), and the Ga₂O₃ is to a large extent reduced to Ga by the formation of H₂O. Subsequently Al is deposited. The Al heat of condensation getters the remaining As out of the Ga-rich thin surface layer. This Al film is AGW anodized by carefully monitoring the overpotential-time curve which gives a clear indication when firstly all the Al, and when secondly all the Ga-film is oxidized. After the oxidation of the Ga layer, the anodic current is switched off (Fig. 5). The MOS devices fabricated by such a two-step anodic process give now very different capacitance/voltage characteristics (Fig. 6 for the "classical" anodic MOS diodes, and Fig. 7 for the new structures).

In order to investigate the chemical composition of the various steps, ESCA studies were undertaken. The following results were obtained: The H₂-annealed thin Ga-rich layer, before Al deposition, has indeed mostly metallic Ga, with small residual levels of Ga₂O₃ and metallic As. It was also discovered that the normal change-over from H₂ to N₂ gas in the furnace at a temperature of 300°C or higher produces a significant N-signal in the Auger spectra for the whole thickness of the Ga-rich

film. This effect does not appear for lower change-over temperatures. Is it possible that the reduced Ga atoms are still active and form GaN? This N in the Ga-rich film does, however, not seem to be essential for the improved C/V data of Fig. 7.

The annealing time has to be optimized in order to ensure that all the Ga_2O_3 is reduced to Ga. For example a 20 nm thick native oxide layer requires an annealing time of 45 min at 650°C to reduce all the Ga_2O_3 to Ga. From this data it can be estimated that the reaction rate for this reduction is probably limited by the diffusion of Ga_2O_3 towards the surface.

5. Conclusions

Experimental data is presented on the dynamics of forming a non-oxidized As layer in the insulator near the interface. This atomic As layer is found to cause a high density of short time constant traps which can be charged and emptied easily from the semiconductor. The creation of As vacancies in the GaAs near the surface by a strongly energetic insulator-deposition process is demonstrated with Al condensation, whereas the Ga condensation does not seem to produce such As vacancies.

The two-step anodic scheme seems to avoid both difficulties. The chemical analysis of the surface layer involved demonstrates that indeed a reduction of As and As_2O_3 takes place due to the low-energy process of thermal out-diffusion at 650°C .

The results presented here demonstrate that with the aid of systematic analytical work a better understanding of the processes of surface passivation can be obtained so that further progress can be made in this area.

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Fig. 1. Profiles of Gallium and Arsenide ratios of mixed oxides before and after laser annealing. Ratios are relative intensities of 3d photoelectron emission peaks corresponding to the oxidized state (Ga_2O_3 , As_2O_3) and the non-oxidized state (e.g. As or Ga in GaAs or in elemental form).

Fig. 2. Depletion layer capacitance (C_D) as function of photopulse for an oxide layer before and after laser annealing.

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Fig. 4. Principle peak Auger intensities of Gallium and Arsenic as a function of the thickness of Gallium layer deposited on GaAs.

Fig. 5. Anodic oxidation of an aluminum layer on a Gallium rich surface of GaAs. The cell potential is plotted as function of anodization time.

Fig. 6. Capacitance-Voltage characteristics of a GaAs MOS structure produced by anodic oxidation of GaAs.

Fig. 7. Capacitance-Voltage characteristics of a GaAs MOS structure produced by anodic oxidation of an aluminum film onto a Gallium rich surface of GaAs.

Ga and As Ratios

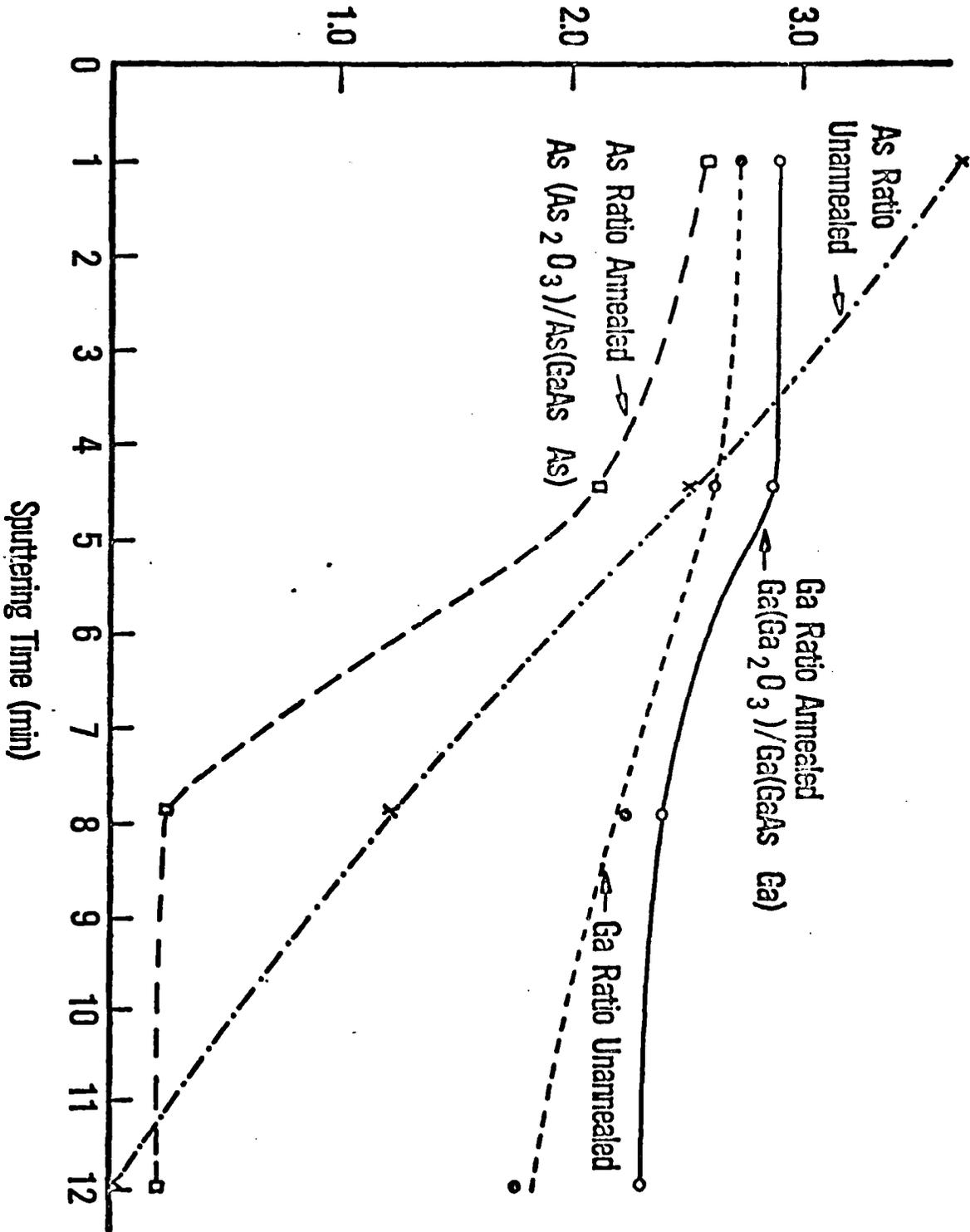


FIGURE 4

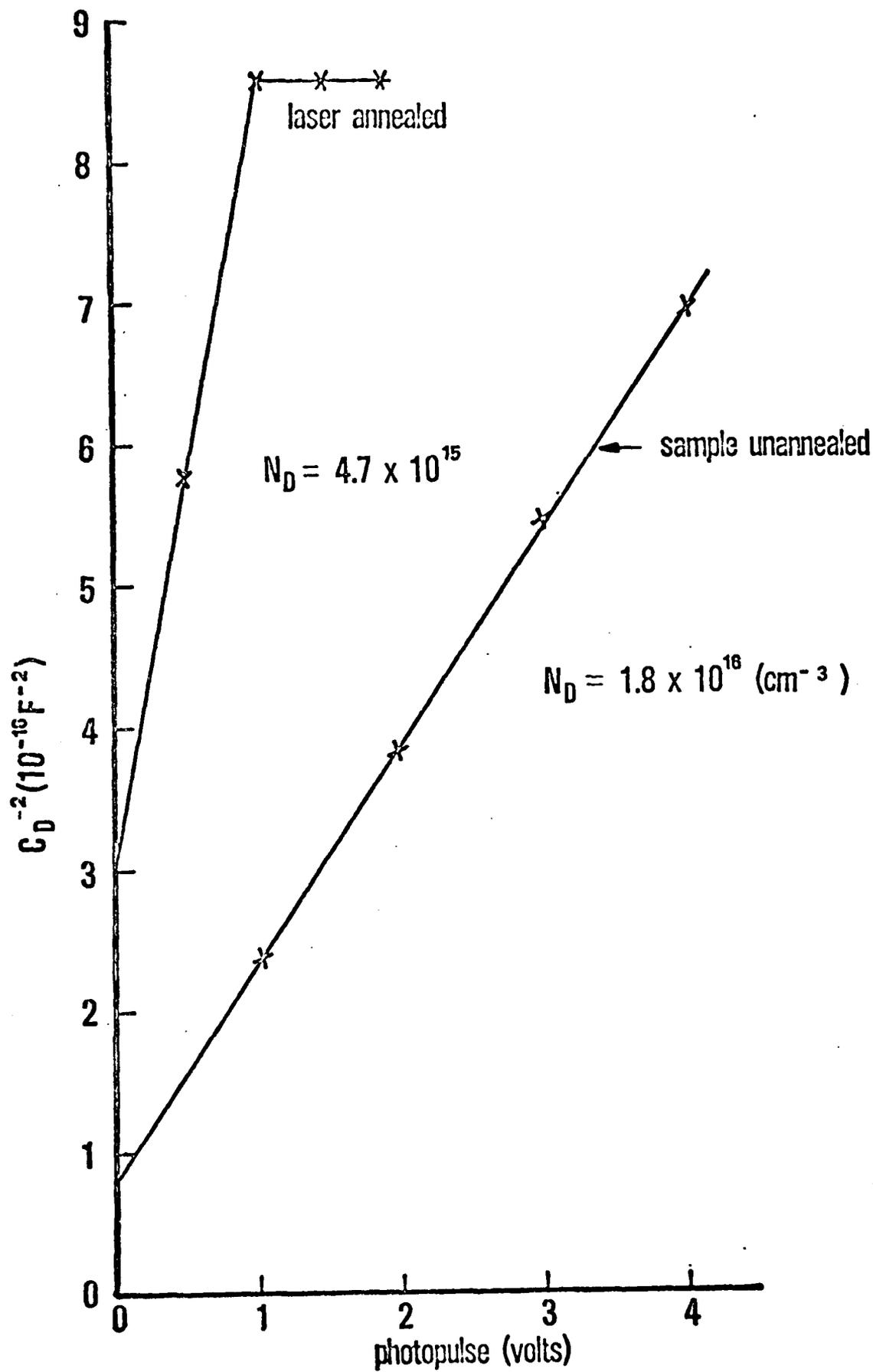
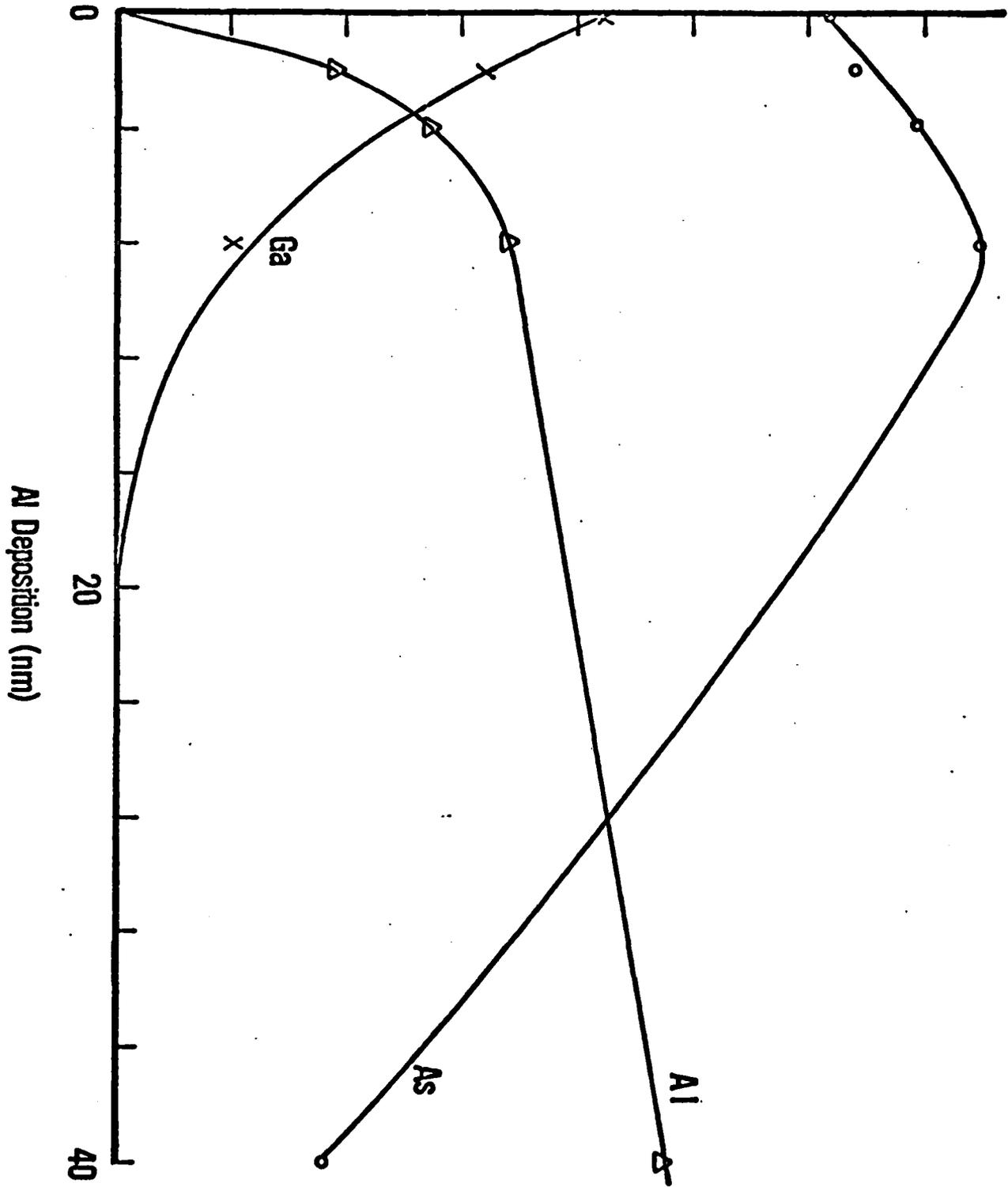


FIGURE 2

Al, Ga and As auger intensity (arbitrary units)



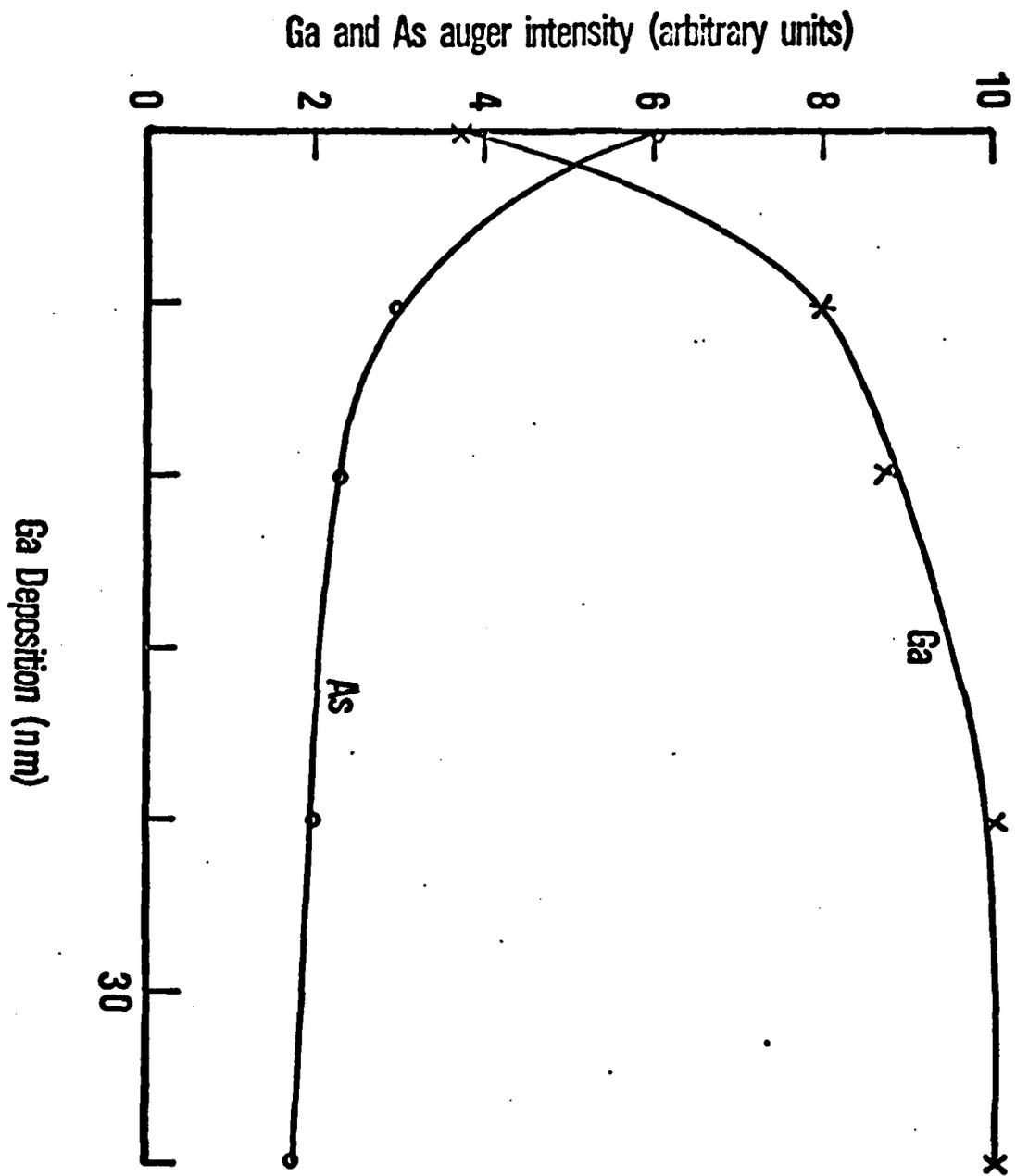


FIGURE 4.

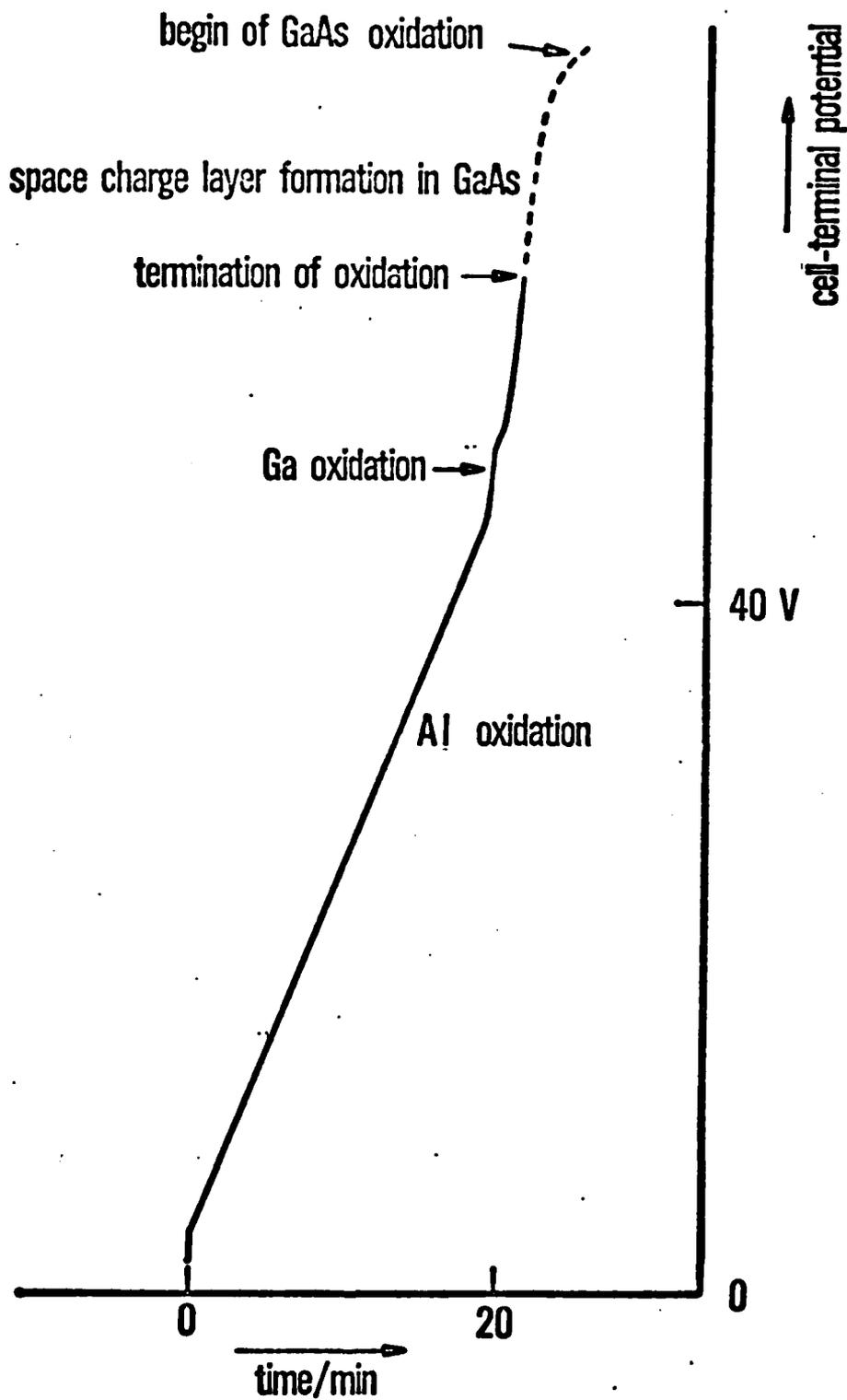
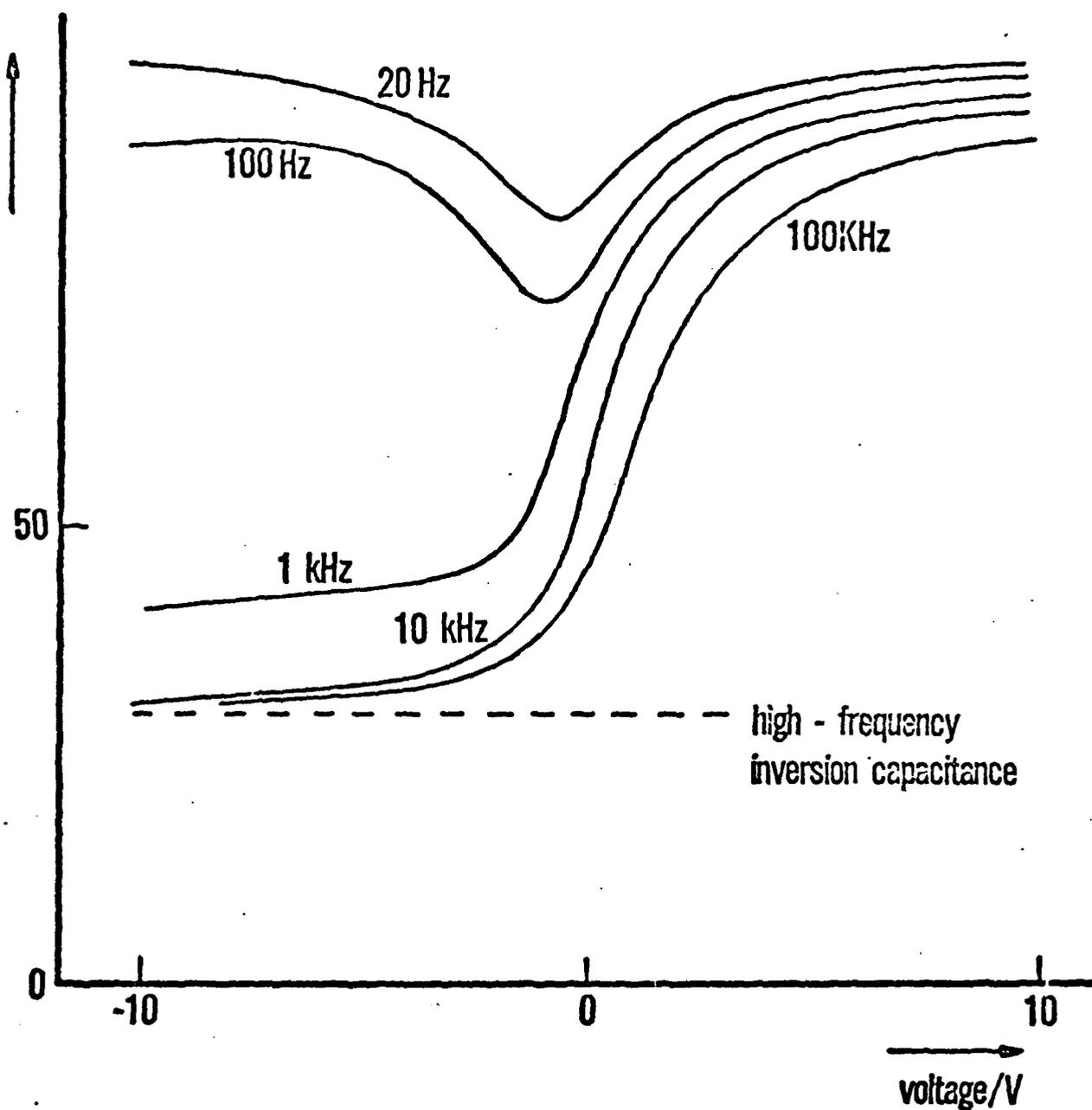


FIGURE 5



sweeping with triangular bias voltage sweep rate: 2V/sec
 except for 20 Hz: 0.2V/sec

only the data for sweeping from -10V to +10V are drawn.

$$N = 2 \cdot 10^{16} \text{ cm}^{-3}$$

$$d_{\text{Al}_2\text{O}_3} = 750 \text{ \AA}$$

$$d_{\text{Ga}} = 50 \text{ \AA}$$

FIGURE 7

An Investigation of Anodically Grown Films on GaAs Using X-Ray Photoelectron Spectroscopy

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ABSTRACT

Anodic oxides on GaAs have been examined using x-ray photoelectron spectroscopy (ESCA) combined with Ar-ion etching. The ESCA spectra were analyzed using both analog, and in some cases digital techniques. Results showed the films to be composed of As_2O_3 and Ga_2O_3 . The composition at the surface of the films was found to be electrolyte sensitive. At the oxide-semiconductor interface evidence was found suggesting a Ga_2O_3 rich oxide region and a layer adjacent to the semiconductor which appeared to contain elemental As. Anodically grown oxide films on GaAs incorporating Al were also studied and it appeared that the regions of GaAs native oxide above and below an Al_2O_3 region had differing compositions.

The anodic oxidation of GaAs (1) offers a very simple technique for producing barrier-type insulating films on this semiconductor. Such films are of great importance for the fabrication of MOS (metal-oxide-semiconductor) devices and success has already been achieved in producing transistors on GaAs (2, 3) using this technology. However, the oxide and interface

properties obtained still show room for improvement and work in our laboratories is concerned with optimization of the anodization conditions in order to improve device behavior. To do this effectively, detailed structural information is required and of the methods available to obtain this data Auger electron spectroscopy (AES) (4) and x-ray photoelectron spectroscopy (ESCA) (5, 6) are probably the most useful, when combined with a suitable etching technique.

In this paper we present chemical depth profiles of anodically grown films on GaAs, obtained using ESCA combined with Ar-ion etching. We feel that ESCA

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Key words: GaAs, anodic oxidation, ESCA, depth profiles.

offers advantages over AES due to the chemical shift data which is more easily obtained and interpreted with the former (6). However, AES does have the advantage of speed and of being able to examine different parts of a single sample, so that a combination of both techniques where available offers the best solution (5).

Experimental

GaAs samples (Monsanto n-type, carrier concentration 10^{18}) were cleaned in methanol and acetone and dried from acetone. Al (99.99% purity, M.R.C. Limited), where used, was deposited by evaporation under vacuum at about 10^{-6} Torr. GaAs samples were etched for 1 min in 1% HCl solution prior to anodization. Electrolytes were all made up from research grade reagents and deionized water. Two electrolytes were studied. These were: (i) 3% tartaric acid solution mixed in the volume ratio 1:2 with propan 1, 2 diol (AGW) (1) and (ii) 0.02M $(\text{NH}_4)_2\text{H}_2\text{PO}_4$ solution mixed in the volume ratio 1:2 with propan 1, 2 diol.

Anodization was carried out under constant current conditions using experimental apparatus and techniques described previously (1). After anodization the samples were rinsed in acetone. Typical sample size was $0.6 \text{ cm} \times 1.2 \text{ cm}$. The samples were attached to the copper spectrometer sample holder with ELEC-TRODAG 915 conducting paint (Acheson Colloids Company) to minimize sample charging. The sample holder itself was mounted on a UHV rotatable probe to ensure precise repositioning of the sample after rotation for etching.

ESCA spectra were recorded on an A.E.I. E.S. 200B spectrometer at typical chamber pressures of 2×10^{-8} Torr, utilizing Mg $K_{\alpha 1}$ $K_{\alpha 2}$ radiation at 1253.6 eV. They were recorded at 0.1 V sec^{-1} (Ga and As 3d peaks) and 0.05 V sec^{-1} (Al 2p and O 1s regions). Both analog and digital spectra were recorded simultaneously, the sampling rate for the latter being 50 times per minute.

Ar-ion milling was carried out using an ION-TECH saddle field ion source fitted with a scanning facility. The source has a beam of height 1 cm, and this was scanned along the length of the sample, at a mean angle of 45° to the sample surface. Argon was 99.996% purity (B.O.C.). The source was operated at either 8 kV 3 mA or 5 kV 2 mA. Approximate etch rates were 25Å/min in the former and 6Å/min in the latter case. These etch rates were estimated from depth profiles obtained from oxide films of known thickness. The anodic growth constants for oxidation of GaAs have been established previously (1). To obtain depth profiles the samples were etched in a stepwise fashion, spectra being recorded after each period of etching. Some idea of the reproducibility of the etching technique may be obtained from Fig. 6 where etching was continued into the substrate. As may be seen, in this region where constant composition is expected, fluctuations are less than $\pm 5\%$.

Data Processing

Most depth profiles were obtained from the ESCA peak areas of the Ga and As 3d peaks, the Al 2p peak and the O 1s peak in the analog spectra. To calculate these areas a triangular approximation was assumed so that

$$\text{peak area} = \text{peak height} \times \text{width at half height}$$

The intensity of photoelectrons of a given energy observed in a homogeneous material of path length x is given by (7)

$$I = \frac{F_0 D k}{\sigma} [1 - \exp(-\sigma x)] \quad (1)$$

if elastic scattering is neglected. I = intensity of photoelectrons emitted, F_0 = x-ray flux, σ = cross section for photoionization in a given energy level of a given atom for a given x-ray energy, D = density of the given atom in the material; k = a spectrometer con-

stant, $\sigma = 1/\lambda$, where λ is the mean escape depth of photoelectrons of given kinetic energy.

For two separate core energy levels A and B in the same sample measured under identical conditions (1) may be written

$$\frac{N_A}{N_B} = \frac{D_A}{D_B} = \frac{I_A \sigma_B}{I_B \sigma_A} \quad (2)$$

where N_A and N_B are the number of atoms per unit volume of A and B, if it is assumed that $\lambda_A \approx \lambda_B$. In our case this is true for the Ga and As 3d levels and the Al 2p level to within 3%, since $\lambda \propto \sqrt{\text{kinetic energy}}$ (8) and the above-mentioned levels are of very similar kinetic energies. We have used Eq. (2) to give depth profiles that show the relative numbers of atoms per unit volume. The results have been plotted relative

to the Ga 3d intensity I_{Ga} by plotting I_{Ga} , $I_{As} \frac{\sigma_{Ga}}{\sigma_{As}}$ and

$I_{Al} \frac{\sigma_{Ga}}{\sigma_{Al}}$ giving the relative number of atoms per unit

volume in arbitrary units of $\frac{N_A}{N_{Ga}} I_{Ga}$ for atom A.

The cross sections (σ) were taken from those calculated by Scofield (9). The O 1s region showed a strong oxide oxygen peak, the intensity of which was only used to obtain interface widths, so no corrections were applied.

Where the Ga 3d peaks due to Ga_2O_3 and GaAs were not clearly resolved the position of the composite peak center at half-height relative to the two extreme positions was used to estimate the amount of each component present, i.e., percentage of peak due to Ga_2O_3

$$\frac{\text{BE}(\text{Ga } 3d) - \text{BE}(\text{GaAs } 3d)}{\text{BE}(\text{Ga}_2\text{O}_3 \text{ } 3d) - \text{BE}(\text{GaAs } 3d)} \times 100\%$$

In the presence of As_2O_3 , elemental As was always observed after Ar-ion etching. On etching through the oxide film to the GaAs substrate the elemental As peak disappeared. An experiment using a sample of powdered As_2O_3 mounted on double-sided seltotape indicated that some of the oxide was reduced to elemental As by the ion beam. This is illustrated in Fig. 1. A similar experiment showed that Ga_2O_3 was stable towards reduction under the same conditions. It was therefore assumed that the origin of the elemental As peak in the anodic oxide film was from reduction of As_2O_3 . When constructing depth profiles the intensities of the As_2O_3 and elemental As 3d peaks were summed to give the total amount of As originally present as oxide. (Making the approximation that the cross sections and escape depths are the same for the two materials.) Where the elemental As 3d peak was obscured by that due to As in gallium arsenide its peak height was assumed to be one-third of that of the As_2O_3 peak for etching at 8 kV and one-quarter for ion etching at 5 kV. These were the ratios observed experimentally in the bulk of the oxide. Under these circumstances the assumed elemental As intensity of GaAs was also subtracted from the measured As 3d intensity of GaAs.

In order to assess the errors involved in the above approximations an attempt was made to analyze one complete set of digital spectra by employing a non-linear least squares fitting program which uses a Gaussian Lorentzian product function (10).

In order to obtain meaningful results it was necessary to fix the linewidths of the various 3d peaks of Ga and As in the interface region. The fixed values used were obtained from fits of spectra from the oxide, or from the GaAs substrate. The results are illustrated in Fig. 2, which also includes the profile obtained from the analog spectra. (The dips in the analog profiles after 13 min. etching are where the sample was left over night in the spectrometer after having etched for 10 min.)

As a further check of the validity of the approximation used to resolve the Ga 3d peaks of Ga_2O_3 and

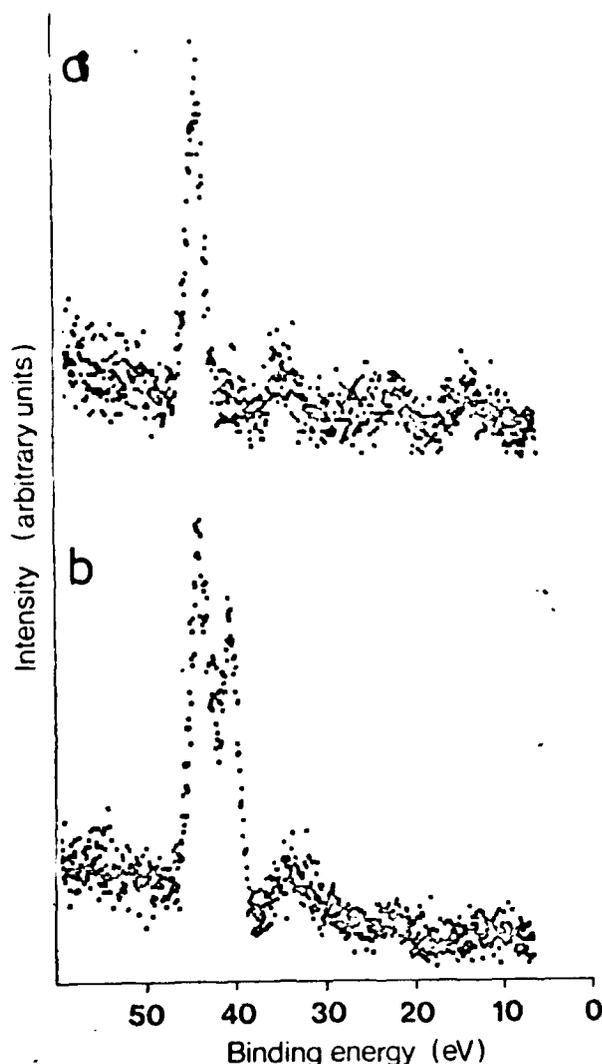


Fig. 1. ESCA spectra of the As 3d peaks for an As_2O_3 powder sample (a) before and (b) Ar-ion etching at 5 kV.

GaAs in the analog spectra the values of the expression

$$\frac{\text{BE}(\text{Ga } 3d) - \text{BE}(\text{GaAs } 3d)}{\text{BE}(\text{Ga}_2\text{O}_3 \text{ } 3d) - \text{BE}(\text{GaAs } 3d)}$$

were compared with values of the expression

$$\frac{I(\text{Ga}_2\text{O}_3)}{I(\text{Ga}_2\text{O}_3) + I(\text{GaAs})}$$

where $I(\text{Ga}_2\text{O}_3)$ is the intensity of the Ga 3d peak of Ga_2O_3 obtained from the digital analysis and similarly $I(\text{GaAs})$ represents the Ga 3d intensity of GaAs. Since both expressions represent the fraction of the Ga 3d peak due to Ga_2O_3 they should be identical. The values agree well ($\pm 5\%$) when the component peaks were of similar intensities but discrepancies appeared where the intensity ratio of the two components was estimated as greater than about 5:1 from the analog data. In these cases the weaker peak appeared relatively stronger from the digital analysis. However only in one case, point 14 in Fig. 2(b), did the difference exceed the $\pm 95\%$ confidence limits (equal to 2 standard deviations) of the digital analysis.

These differences probably arise for two main reasons. First, the approximation used to resolve the analog spectra is not entirely valid under the conditions where the discrepancies occur. Second, the 3d peak shapes are not perfectly fitted to a single peak

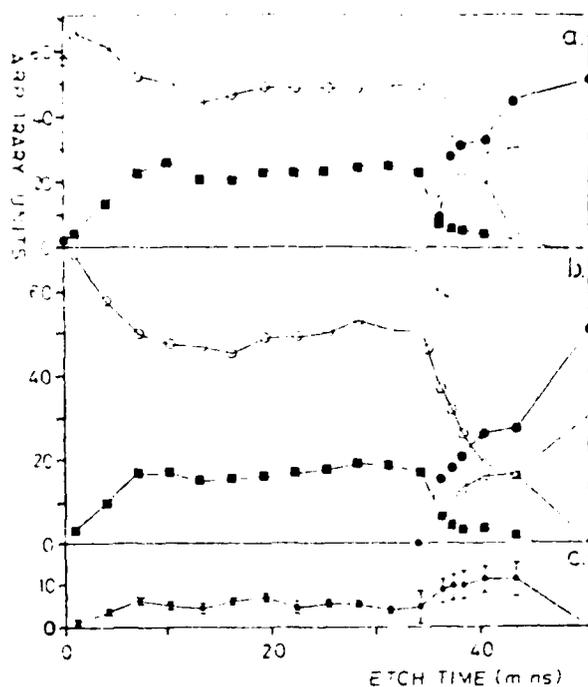


Fig. 2. Depth profiles of Ga and As 3d ESCA intensities from a 1000 Å oxide film grown on GaAs in $(\text{NH}_4)_2\text{H}_2\text{PO}_4/\text{glycol}$ electrolyte at $50 \mu\text{A cm}^{-2}$, Ar ion etching at 8 kV. (a) Profiles from analogue spectra, (b) profiles from digital spectra, and (c) profile of elemental As from digital spectra. For (a) and (b), \circ , Ga in Ga_2O_3 ; \bullet , Ga in GaAs; \blacksquare , As in As_2O_3 ; \square , As in GaAs.

(they are in fact closely overlapping doublets comprising the 3d 5/2 and 3d 3/2 peaks) and so the fitting program may obtain a better statistical fit by modifying the intensity of the weaker peak present. However the good agreement obtained in most cases is encouraging and indicates that the approximation used is a useful one in cases where no other method is available.

The region where the accuracy of the profile becomes most critical is at the interface because here the greatest compositional variations occur. In particular there is the question of whether or not there is any elemental As present at this interface.

In the case of the analog spectra, elemental As could not be resolved out in the presence of gallium arsenide As (i.e., at the interface); rather, a constant ratio of As_2O_3 :As was assured in these cases and only this amount subtracted from the overlapping peak of gallium arsenide (see above). Any additional elemental As over and above this amount will still be included with the gallium arsenide As. Hence, if there were excess elemental As present we might expect to see a profile such as that in Fig. 2(a) where the gallium arsenide As appears before, and is initially more intense than the Ga. (Note that within the substrate the As appears less intense than the Ga due to selective etching. This effect is discussed later.)

From the digital spectra, the computer analysis made it possible to resolve out the As 3d peaks due to As_2O_3 , As, and GaAs as shown in Fig. 3. The As_2O_3 and As intensities have not been summed in Fig. 2(b) but the elemental As plotted separately in Fig. 2(c). (The error bars in the latter figure represent the 95% confidence limits of the digital curve fitting analysis and do not include any other experimental errors.) As may be seen the amount of elemental As appears to increase at the interface even though the amount of As_2O_3 is decreasing. This also suggests the presence of excess elemental As at the interface. However in the digital profile of Fig. 2(b) the gallium arsenide Ga appears earlier than in Fig. 2(a), leading to some

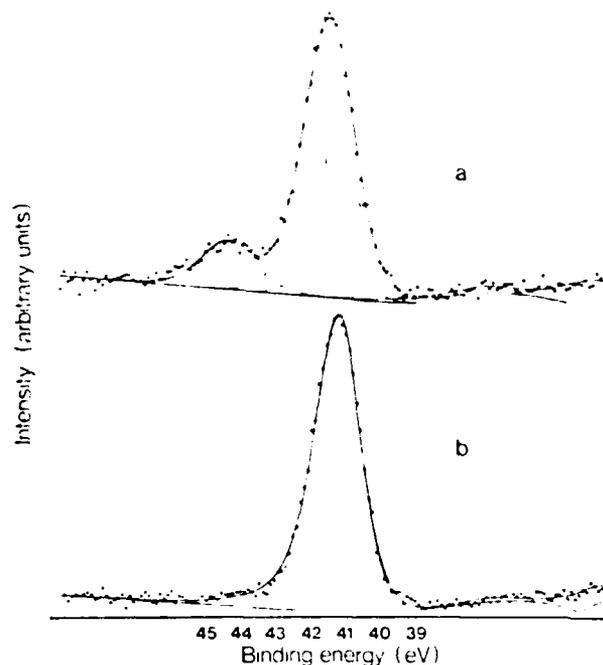


Fig. 3. Expanded spectrum of the As 3d region (a) at the interface showing the digital resolution of the 3d peaks due to As_2O_3 , As, and GaAs; (b) in the GaAs substrate.

uncertainty as to whether the feature in the analog profile can definitely be identified as being due to elemental As and is not merely an artifact of the method of data analysis. Two points should be mentioned in conjunction with this. First, although the Ga profiles do deviate in the interface region the difference between these in Fig. 2(a) and (b) only exceeds the 95% confidence limits of the digital analysis at point 14 (indicated on the figure). Second, the Ga profile of gallium arsenide is iterated to zero arbitrarily at the point shown in Fig. 2(b) since here none was observed. However the profile could be more abrupt than shown.

However better resolution was required in order to clarify this issue. This was achieved for the ESCA spectra by going to the narrowest slit width available. Figure 5 shows spectra at the interface of a sample grown at $10 \mu A cm^{-2}$ using this maximum resolution. The analog profile for the same sample is shown in Fig. 6. The spectra in Fig. 5 clearly show that significant changes occur in the As 3d spectrum before similar changes occur in the Ga 3d region and we believe that this is due to the presence of elemental As. Subsequently (for the profiles shown in Fig. 7 and 8) improved depth resolution was achieved by using lower Ar-ion etch rates.

With this improved resolution, and since reasonable overall agreement was obtained between the profiles obtained by analog and digital analysis of the same set of data the authors decided to rely exclusively on the analog treatment of the results.

Results

The binding energies of the various 3d peaks of Ga and As and of the Al 2p peak observed in these experiments are listed in Table I and compared with previously reported binding energies. The comparison indicates that the major peaks observed in the anodically grown films on GaAs correspond in position with those of Ga_2O_3 , As_2O_3 , and As within experimental error. In the film incorporating aluminum the Al 2p peak corresponds in position with that of Al_2O_3 . The CIS peak at 284.6 eV (which is the value obtained in this laboratory for a hydrocarbon contamination layer based in Au 4f_{7/2} at 84.0 eV) was generally used for

Table I. Peak positions

		Binding energy (eV)		
		This work (± 0.2 eV)	Previously reported (11, 12) ^a	F W H M (This work)
Ga 3d	GaAs	19.4 ^a	19.5	1.6 ^a
	Ga_2O_3	20.5 ^a	20.4	2.0 ^a
As 3d	GaAs	41.2 ^a	41.2	1.6 ^a
	As_2O_3	44.5 ^a	44.4	2.0 ^a
	As	41.8 ^{b,c}	41.8	1.8 ^a
Al 2p	Al_2O_3	74.5 ^b	74.5	1.9

- ^a Referred to CIS at 284.6 eV.
- ^b Referred to Ga 3d position of Ga_2O_3 at 20.5 eV.
- ^c Obtained from the best computer fitted spectra of the anodic oxide.
- ^d Referred to CIS at 285.0 eV.
- ^e Obtained from digital spectra.

calibration if possible but in many cases this did not prove reliable (This may be due to the presence of a carbon-containing species in the anodic films but more work is required to definitely establish this.) Under these circumstances internal calibration against the Ga 3d peak of Ga_2O_3 was used. In all experiments the internal calibration was consistent with the above assignment. Typical ESCA spectra of the Ga and As 3d region for an anodic oxide and the GaAs substrate are illustrated in Fig. 4.

In addition to the ESCA peaks discussed above, several other weaker peaks were also observed in the

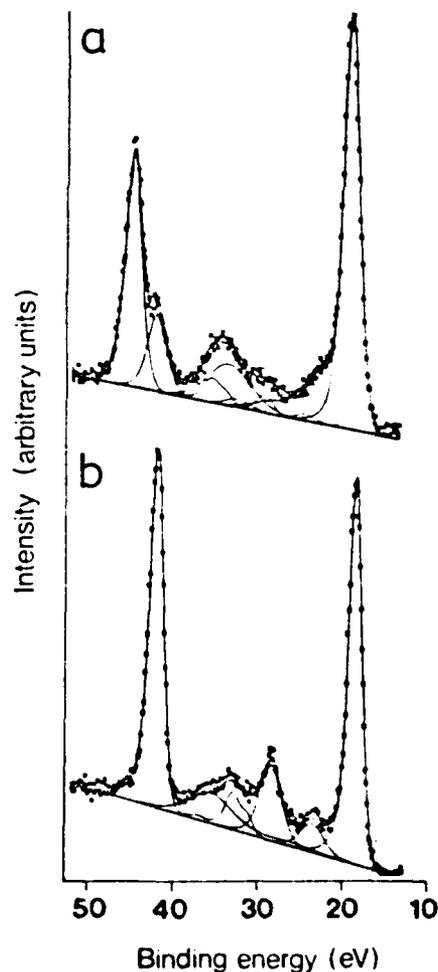


Fig. 4. ESCA spectra of the Ga and As 3d region with computer fit peaks of (a) GaAs native oxide and (b) GaAs substrate after removal of the native oxide by Ar-ion etching at 8 kV.

10-70 eV binding energy region (see Fig. 4). Two pairs of peaks occurred in the anodic oxide spectra between about 26 and 35 eV. These were assigned to the As L₂M₂M₂ Auger transitions (11), there being one pair associated with As₂O₃ and another with elemental As. When GaAs started appearing in this pair of Auger peaks were seen to slightly lower binding energies. Other peaks are the satellite peaks from the nonmonochromated x-radiation used in the spectrometer. Their position and intensity are well known and are taken from x-ray spectroscopy results (13). A broad peak was identified in the computer-analyzed spectra of the anodic oxide at about 39 eV. A similar peak was seen in the GaAs substrate at around 35 eV. The latter peak is a plasmon loss peak associated with GaAs (4, 14), and the lower peak probably has a similar origin. Finally, a new peak was seen at 27.5 (± 1) eV which disappeared on etching through to the substrate. This is probably the oxygen 2s peak (15), the assignment being supported by the fact that the peak correlates quite well with the oxygen 1s intensity which was monitored in most of these experiments.

Oxides grown in the (NH₄) H₂PO₄/glycol electrolyte.—The depth profiles shown in Fig. 2 were obtained from a 1000Å thick native oxide film on GaAs, grown in the (NH₄) H₂PO₄/glycol electrolyte at 50 $\mu\text{A cm}^{-2}$. As seen in the figure the surface of the oxide grown in this electrolyte is As deficient as compared to the bulk. For a similar sample grown at 500 $\mu\text{A cm}^{-2}$ the ESCA spectrum showed no As present at the surface. The bulk oxide region is fairly uniform and shows a constant As/Ga ratio of atoms per unit volume of between 0.5 and 0.6, this value appearing to be independent of growth current density over the range 10 μA –500 $\mu\text{A cm}^{-2}$. To what extent this ratio is affected by selective etching has not been established. However it is clear from the Ga and As profiles of gallium arsenide, where the As/Ga ratio is 0.6 instead of unity, that selective etching of As from the substrate definitely occurs.

At the oxide-semiconductor interface the As₂O₃ intensity generally starts to drop before that of Ga₂O₃. Indeed, in some cases the Ga₂O₃ intensity increases first before dropping off. This leads to a Ga₂O₃ rich oxide next to the substrate. The effect seems to be more pronounced at higher and lower growth current densities than it is at 50 $\mu\text{A cm}^{-2}$. See for example Fig. 6 for a sample grown at 10 $\mu\text{A cm}^{-2}$. Similar behavior has been observed for samples grown at 500 $\mu\text{A cm}^{-2}$.

From the profile in Fig. 2(c) it can be seen that the amount of elemental As observed increases at the oxide-semiconductor interface even though the As₂O₃ intensity is decreasing. This suggests that there is a region adjacent to the GaAs substrate where elemental As was present prior to Ar-ion etching. Alternatively it is possible that very thin films of As₂O₃ may be more readily reduced, leading to a smaller As₂O₃/As ratio than that observed in the bulk of the film. However, it has been suggested previously (4) that there is an As rich region adjacent to the substrate in anodic films on GaAs. In view of this it seems very probable that what we are seeing here is confirmation of the presence of elemental As at the oxide/semiconductor interface. Figure 5 shows spectra obtained on etching through the interface of a sample grown at 10 $\mu\text{A cm}^{-2}$. It can be seen that the changes in As 3d spectrum occur earlier than those in the Ga 3d region. The profile from the sample is shown in Fig. 6 and shows a similar region to Fig 2(c) although in this case the elemental As intensity is included in the As profile of gallium arsenide as discussed earlier. Similar results were also observed for samples grown at 500 $\mu\text{A cm}^{-2}$.

Interface widths, measured from these profiles, were defined as the distance over which the intensity of the component being measured changed from 20 to 80% of its steady-state value (6). Interface widths

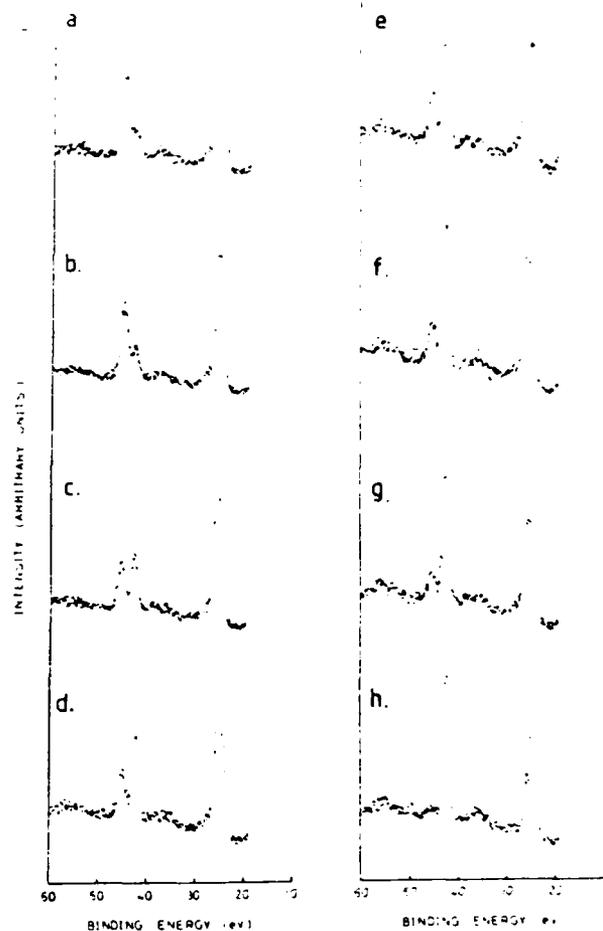


Fig. 5. ESCA spectra of As and Ga 3d region of sample grown at 10 $\mu\text{A cm}^{-2}$ after Ar-ion etching at 8 kV for (a) 25 min, (b) 28 min, (c) 31 min, (d) 32 min, (e) 33 min, (f) 34 min, (g) 36 min, (h) 39 min.

were measured on both Ga, As, and oxygen profiles. It was found that those measured from the oxygen

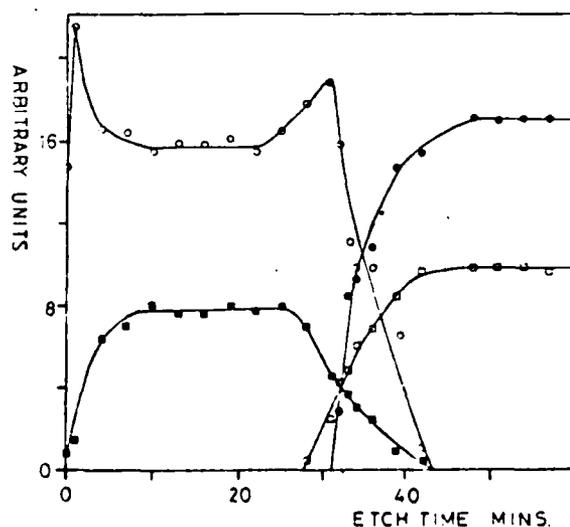


Fig. 6. Depth profiles of Ga and As 3d ESCA intensities from 800Å oxide film grown on GaAs in (NH₄)H₂PO₄/glycol electrolyte at 10 $\mu\text{A cm}^{-2}$. Ar ion etching at 8 kV. ○, Ga in Ga₂O₃; ●, Ga in GaAs; ■, As in As₂O₃; □, As in GaAs.

profiles gave the largest widths, as would be expected since they reflect the change in both As_2O_3 and Ga_2O_3 at the interface. The widths from the oxygen profiles are therefore used in discussing the interfaces.

Significantly smaller interface widths were observed when etching at 5 rather than 8 kV. For example the interface width measured for a 1000Å film grown at $500 \mu\text{A cm}^{-2}$ and etched at 8 kV was 210Å whereas the width measured for a similar film etched at 5 kV was about 90Å. This is due to knock-on effects occurring during ion etching which make the interface appear broader than it actually is. The effect is greater for higher energy bombarding ions. Another effect which has not been investigated in a systematic way here is uneven etching. This makes the observed interface width depend on what film thickness has previously been etched away, the broadening increasing for thicker films (6). Because of these effects the measured interface widths represent an upper limit and the actual widths may be expected to be significantly smaller than the measured values.

Oxides grown in the tartaric acid/glycol electrolyte.—Figure 7 shows the profiles obtained from a 500Å native oxide film grown on GaAs in the AGW electrolyte at $200 \mu\text{A cm}^{-2}$. In contrast to oxides grown in the previous electrolyte the surface region is As rich as compared to the bulk. (The first point in all these profiles is unrepresentative due to surface contamination and should be ignored.) The other features of these profiles are very similar to those already discussed. The bulk of the film is uniform with an As/Ga ratio of about 0.5. There is a slightly Ga_2O_3 rich region adjacent to the substrate and the As profile of the GaAs substrate indicates the probable presence of elemental As at the interface. The interface width obtained from the oxygen profile was 60Å. (The sample was etched at 5 kV.)

Using the data shown in Fig 7 an attempt was made to estimate the amount of elemental As present at the interface over and above that expected due to reduction of As_2O_3 by the ion beam. The gallium arsenide As peak intensities were all corrected for selective etching using the observed Ga/As ratio of the substrate which is 0.67 instead of unity, and assuming that the effect becomes operative as soon as the substrate appears. Using the corrected values the difference in areas beneath the Ga and As profiles of the gallium arsenide was obtained. From the known etch rate and the known density of As atoms in GaAs the area could be converted into a number of atoms per square centimeter, giving the value 2×10^{17} atoms cm^{-2} . It was not possible to assign a realistic value to the errors involved in this estimate.

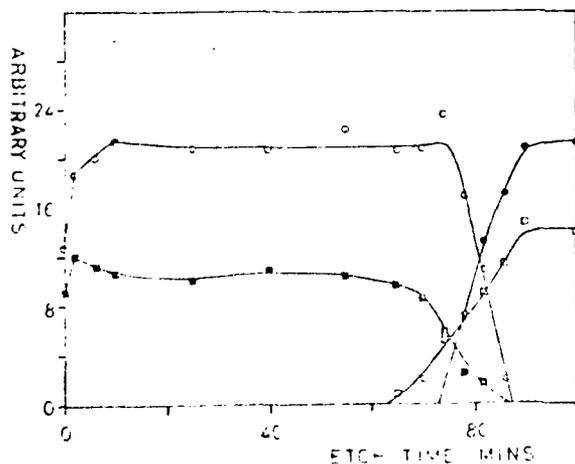


Fig 7. Depth profiles of Ga and As 3d ESCA intensities from a 500Å oxide film grown on GaAs in tartaric acid/glycol electrolyte at $200 \mu\text{A cm}^{-2}$. Ar-ion etching at 5 kV. ○, Ga in Ga_2O_3 ; ●, Ga in GaAs; ■, As in As_2O_3 ; □, As in GaAs.

Anodic films incorporating aluminum—Figure 8 shows the profile obtained from an anodic oxide film grown in the AGW electrolyte on a GaAs sample with 200Å of Al deposited onto its surface. ESCA spectra of the Ga and As 3d region taken at points A, B, and C in Fig 8 are shown in Fig 9. The total oxide film thickness here is approximately 900Å. As already noted, the Al 2p peak can be assigned to that of Al_2O_3 (see Table I). This peak was observed all the way through the oxide film and significant amounts were seen at the surface.

From Fig. 8(a) it can be seen that there are two GaAs native oxide regions, one above and one below the Al_2O_3 layer. The native oxide beneath the Al_2O_3 layer is similar in all respects to that observed on GaAs in the absence of Al [compare Fig. 4(a) and Fig. 9(c)] and at the oxide semiconductor interface the probable presence of elemental As is indicated. However the native oxide at the surface of the film [see Fig. 9(a)] shows marked differences when compared to the normal GaAs native oxides grown without Al. First the oxide is very As deficient as compared to the normal anodic oxide. The As/Ga ratio of atoms per unit volume here is about 0.3 rather than 0.5. Second the As_2O_3 :As ratio in this region is almost 1:1, not the 4:1 ratio expected from reduction of As_2O_3 by Ar ions at 5 kV. This situation persists right through the predominantly Al_2O_3 region until the oxide region underneath is reached when the normal ratio is again observed. This seems to suggest that there is some difference between the As_2O_3 in the two regions such that that nearer the surface is more readily reduced. An alternative possibility which cannot be ruled out from the data available here is that there was originally some unoxidized Al present in the film which reacted with As_2O_3 during Ar-ion etching to produce $\text{As} - \text{Al}_2\text{O}_3$, since Al_2O_3 is the thermodynamically more stable oxide.

Discussion

The foregoing results indicate that anodic native oxide films on GaAs may be divided into three regions;

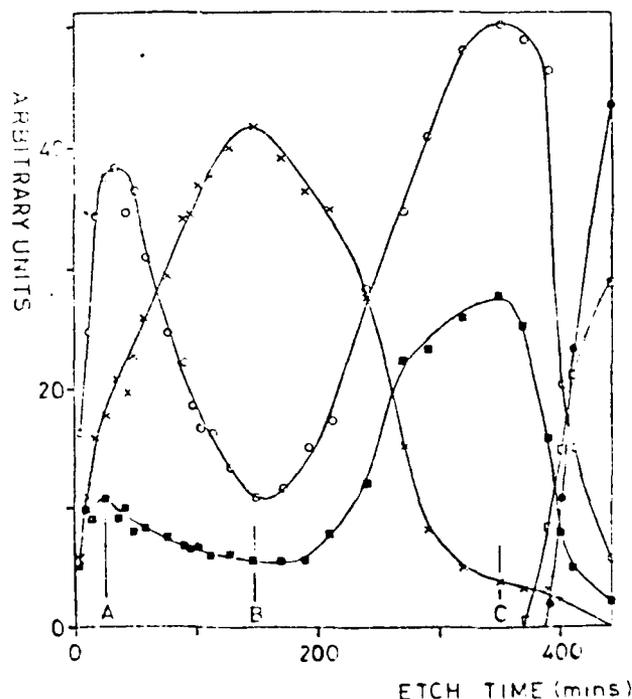


Fig 8. Depth profiles of Ga and As 3d and Al 2p ESCA intensities from an anodic oxide grown on GaAs - 200Å Al in tartaric acid/glycol electrolyte at 100 A cm^{-2} . Ar-ion etching at 5 kV. ○, Ga in Ga_2O_3 ; ●, Ga in GaAs; ■, As in As_2O_3 ; □, As in GaAs; ×, 1/2 of Al 2p intensity in Al_2O_3 .

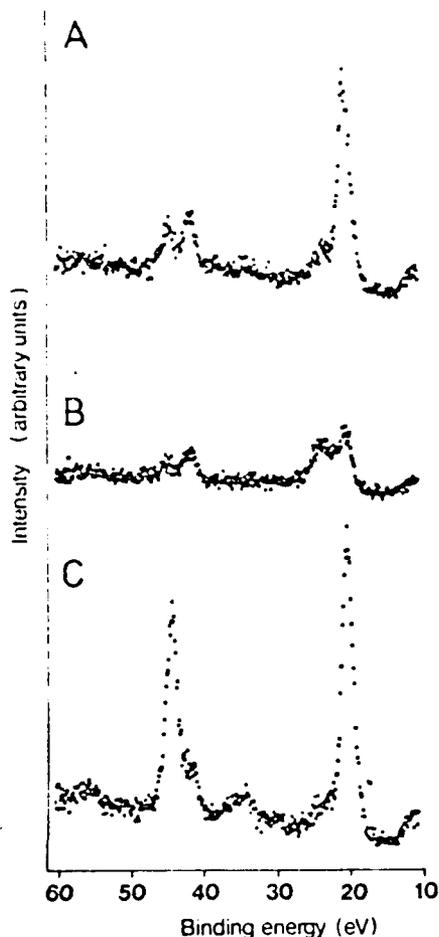


Fig. 9. ESCA spectra of the Ga and As 3d region recorded at points A, B, and C in Fig. 7.

the surface, the oxide bulk, and the oxide/GaAs interface region. In terms of chemical composition the surface region is extensively influenced by the electrolyte whereas the other two regions are not. The factors which control the surface composition are not known but the adsorption behavior of the electrolyte is probably important.

Due to the limited number of samples studied here no definite conclusions have been drawn concerning the influence of growth current density on film structure. However no overall systematic changes were observed over nearly two orders of magnitude ($10\text{--}500 \mu\text{A cm}^{-2}$). The most obvious variation seen was in the extent to which there was a Ga_2O_3 rich region in the oxide near the oxide/semiconductor interface. This seemed much less pronounced for samples grown at $50 \mu\text{A cm}^{-2}$ than for those grown at the extremes of the range studied. It is conceivable that the observed variation was simply an experimental artifact. However a previous report (16) of oriented $\beta\text{-Ga}_2\text{O}_3$ observed at this interface for samples grown at very high current densities ($>2 \text{ mA cm}^{-2}$) may also suggest a more Ga_2O_3 rich oxide at the interface, since As_2O_3 is a primary glass former and its absence could lead to polycrystalline Ga_2O_3 being formed. [Wilmsen and Kee also reported a Ga_2O_3 rich oxide near the interface in anodic oxides grown in both tartaric acid/glycol and H_3PO_4 solutions (5).] There was also some evidence that the surface depletion of As was less severe for samples grown at low current densities in the $(\text{NH}_4)_2\text{H}_2\text{PO}_4$ electrolyte. Similar results have been reported by Croset *et al.* (17) for samples grown in a $\text{Na}_2\text{PO}_4/\text{glycol}$ electrolyte.

As noted above it is possible that the as-grown anodic oxide films contain elemental As at the oxide/semiconductor interface. The origin of this elemental As is not known, but we have previously suggested (18) that the growth mechanism may be responsible. Whatever the reason for this accumulation, its presence must influence the interface properties and hence device behavior where this technology is employed. Because of this it would be advantageous to be able to control and hopefully eliminate this elemental As buildup. However, at present there is no obvious way in which this might be accomplished.

One further observation of relevance in connection with the oxide film growth mechanism is that in Fig. 8(a) Al_2O_3 is seen throughout the film. Its occurrence deep in the film, below the expected Al_2O_3 region, may be due to knock-on effects during ion etching. However, the spreading towards the oxide surface cannot be explained as an experimental artifact. It may mean that the previously suggested interstitial mechanism for metal ion drift (13) is an oversimplification and that "lattice" and "interstitial" ions can interchange within the film. Further experimental work is required here.

Finally, it is important to consider the effects of ion etching on the sample and how this influences the results. We have observed in these experiments that the Ar-ion beam reduces As_2O_3 . No similar effect was seen with Ga_2O_3 . We have also seen selective etching in the GaAs substrate where the observed Ga:As ratio was not unity. However, we have not yet been able to estimate the extent to which selective etching effects the observed Ga:As ratio in the oxide. Until the extent of this effect is known we cannot make any reliable quantitative measurements from results such as these. Also we have noted that the measured interface width is significantly influenced by the etching conditions, a factor which should be taken into account when using such measurements.

Conclusions

The results presented in this paper illustrate the application of ESCA to the study of anodic oxide films. Using this technique we have been able to obtain chemical depth profiles which provide considerable insight into the structure of such films. They indicate that the oxide/semiconductor interface region is very complex with variations in the $\text{Ga}_2\text{O}_3/\text{As}_2\text{O}_3$ ratio as well as the probable presence of elemental As. Some variation was noted between films grown in two different electrolytes.

Results from an anodic film grown on a GaAs substrate plus 200Å of aluminum also showed complex behavior. Two different native oxide regions were identified, one at the film surface which was relatively As_2O_3 deficient and one below the Al_2O_3 , adjacent to the substrate, which resembled the anodic native oxides seen in the absence of Al.

Much more work is still required, both on anodic native oxides of GaAs and also on multilayer anodic films. It is hoped that progress will be assisted by further applications of ESCA to take advantage of the insight which it allows.

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