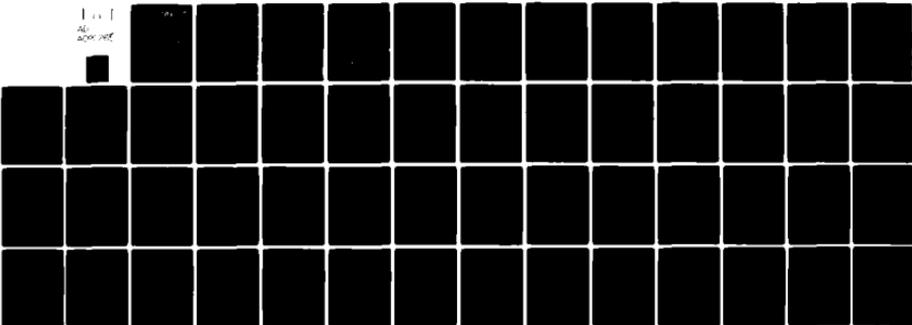


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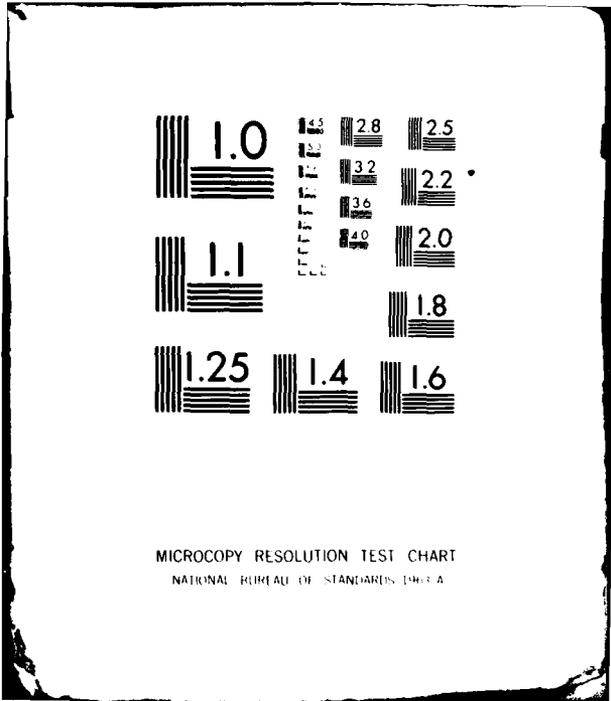
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DESIGN AND IMPLEMENTATION OF MULTI-INPUT ADAPTIVE SIGNAL EXTRAC--ETC(U)
JUL 80 W A GARDNER, M A SODERSTRAND F49620-79-C-0086
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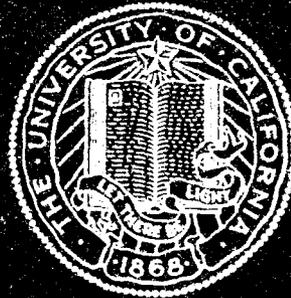


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tions and associated adaptive adjustment schemes. The methods of implementation considered are based on speed-cost efficient Residue Number System arithmetic, and include Read Only Memory table look-up, and microprocessors and minicomputers for hardware control and for software implementation.

The major goals of the research are improvements over prior art in signal extraction performance (as measured by signal distortion, signal-to-noise ratio and mean squared error) and in the cost of implementation and speed of operation. Results on both design and implementation of configurations and adjustment schemes are described.

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1.0 ABSTRACT

This is the Final Report on AFOSR contract F4920-79-C-0086 covering the period June 1, 1979 through May 31, 1980. It covers research on design and implementation of novel adaptive digital signal processors for signal extraction (i.e., reduction of noise, interference, and distortion). The signal extractor configurations and adaptive adjustment schemes considered are extensions and generalization of prior art (viz., the FIR digital filter and the LMS adjustment algorithm) that consist of various combinations and interconnections of conventional adaptive filtering and noise cancelling configurations and associated adaptive adjustment schemes. The methods of implementation considered are based on speed-cost efficient Residue Number System arithmetic, and include Read Only Memory table look-up, and microprocessors and minicomputers for hardware control and for software implementation.

The major goals of the research are improvements over prior art in signal extraction performance (as measured by signal distortion, signal-to-noise ratio and mean squared error) and in the cost of implementation and speed of operation. Results on both design and implementation of configurations and adjustment schemes are described.

DESIGN AND IMPLEMENTATION OF MULTI-INPUT
ADAPTIVE SIGNAL EXTRACTIONS

by

William A. Gardner and Michael A. Soderstrand

Report No. SIPL-80-11

July 1980

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2.0 RESEARCH OBJECTIVES

2.1 Research Objectives for Part 1

Part 1 of the research proposal presented several novel dual-filter configurations for adaptive signal extraction. The corresponding research objectives were loosely organized on the basis of associated modes of operation, as outlined below.

2.11 Two Modes: Primary Signal Absent/Primary Signal Present

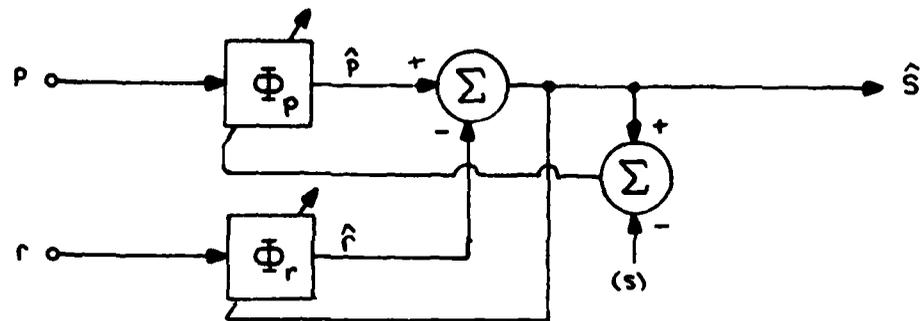
The objective here was to employ theoretical analysis and computer simulations to evaluate the performance of the two-stage adaptive signal extractor shown in Figure 2.11. The first stage in this configuration is adjusted only while the signal is absent, and it attempts to cancel noise or interference. The second stage is adjusted only while the signal is present, and it attempts to remove signal distortion introduced in the first stage due to leakage of the signal into the noise reference.

2.12 Two Modes: Reference Signal Present/Reference Signal Absent

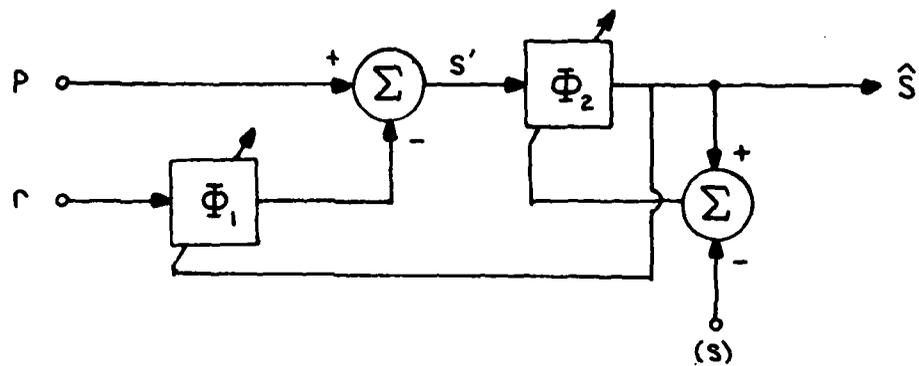
The objective here was to employ theoretical analysis and computer simulations to evaluate the performance of the three dual-filter adaptive signal extractors shown in Figure 2.12. These configurations employ hybrid adjustment schemes. Filter ϕ_2 (or ϕ_p) is periodically adjusted in an attempt to minimize the mean square error (MMSE) between the output signal and a reference signal which is periodically available. Filter ϕ_1 (or ϕ_r) is continually adjusted in an attempt to minimize the mean square output signal (MMSO). These adaptive signal extractors attempt to reduce both channel induced signal distortion and noise or interference.

2.13 One Mode: Decision Directed with Reference Noise Present

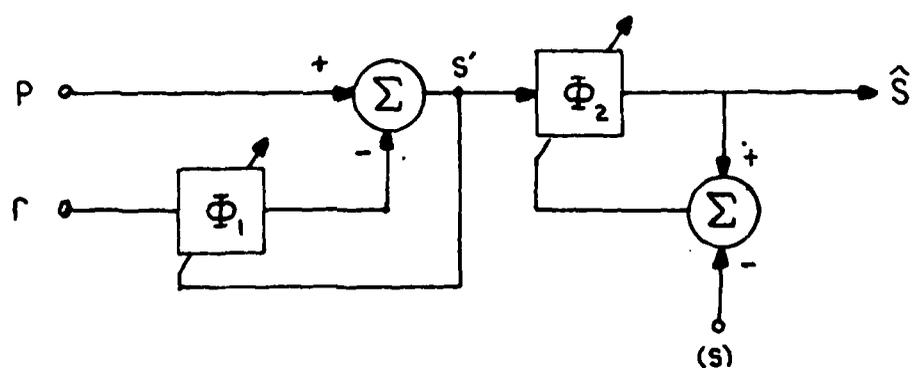
The objective here was to employ theoretical analysis and computer simulations to evaluate the performance of the dual-filter adaptive signal



(a)



(b)



(c)

FIGURE 2.12. The hybrid filters, (a) parallel configuration, (b) coupled-cascade configuration (c) uncoupled-cascade configuration

extractors for dual-channel data communication shown in Figure 2.13. The adjustment scheme for filter ϕ_p employs decision direction in order to seek MMSE. The filter ϕ_r (in Figure 2.13b) is adjusted to seek MMSO. The former filter attempts to reduce intersymbol interference, whereas the latter filter attempts to reduce interchannel interference.

2.14 Sequential Modes: Dual Primary and Dual Reference Signals

The objective here was to employ theoretical analysis and computer simulations to evaluate the performance of the coupled dual-filter signal extractors shown in Figure 2.14. Each dual-filter configuration attempts to provide a reference signal for adjustment of the other dual-filter.

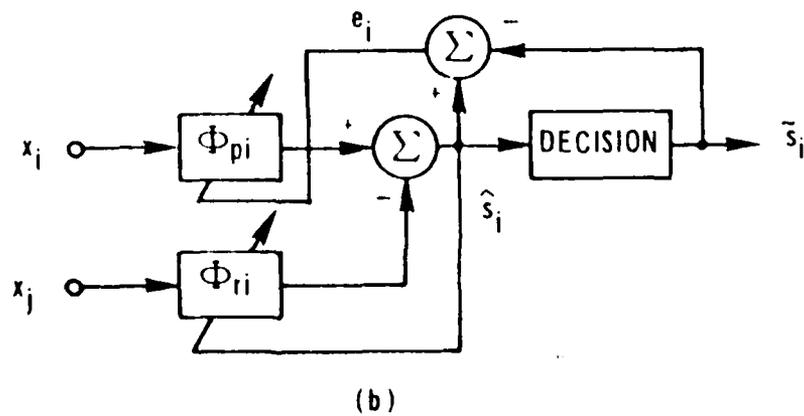
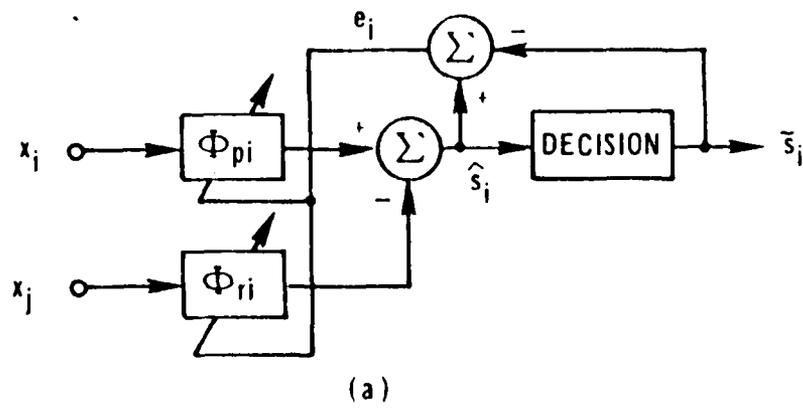


FIGURE 2.13. Dual-Filter Extractors for Dual-Channel Data Communications ($i = 1, 2$; $j = 1, 2$; $i \neq j$)

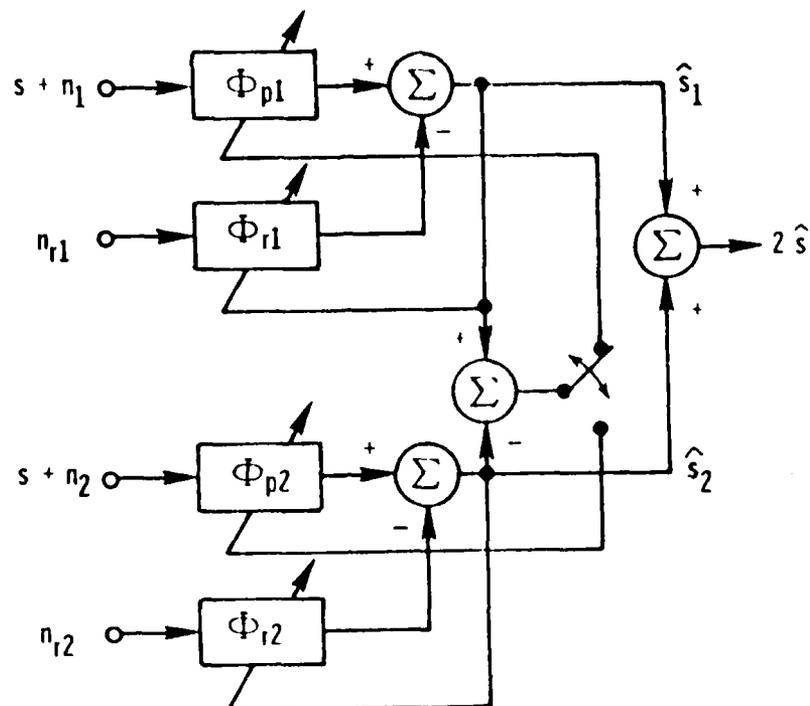


FIGURE 2.14. Coupled Extractors for Dual Primary and Reference Inputs

2.2 Research Objectives for Part 2

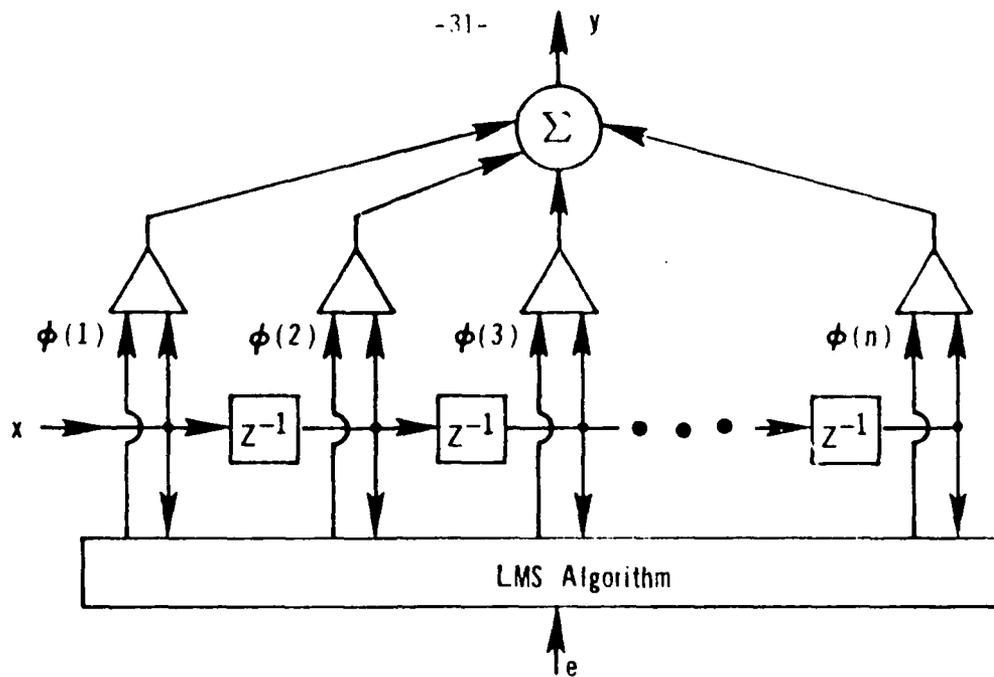
Part 2 of the research proposal presented five different techniques for implementation of both non-recursive and recursive adaptive filters in both hardware and software using Residue Number System (RNS) arithmetic.

2.21 ROM Table Look-Up FIR Filter

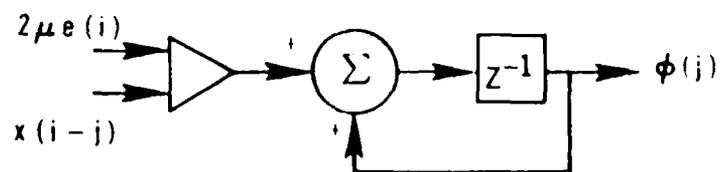
The objective here was to design high speed Residue Number System (RNS) arithmetic Read-Only-Memory (ROM) table-look-up hardware to implement the standard adaptive filter of Figure 2.21a and the LMS update algorithm of Figure 2.21b and 2.21c. Since RNS is integer arithmetic, the filter itself must be scaled such that all coefficients are adequately represented by integers. However, the LMS algorithm requires fractional multiplication. This fractional multiplication within the LMS algorithm was the primary difficulty to be resolved in this project.

2.22 Universal Adaptive FIR Filter for Use with a Microprocessor or Minicomputer

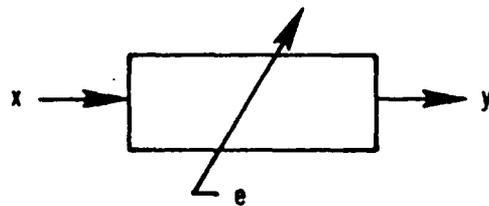
The objective here was to employ two pieces of special purpose hardware (one to perform the multiply/accumulate necessary for an FIR filter and the other to provide hardware assistance for the LMS algorithm) to assist a microprocessor or minicomputer in implementing an adaptive FIR filter at useful speeds. Figure 2.22a shows the basic filter structure. The hardware implements the functions in the box formed by the dotted lines and is based on RNS arithmetic. The LMS algorithm is shown in Figure 2.22b and this also is implemented in hardware. The microprocessor or minicomputer directs data flow such that the complete filter is implemented. The primary difficulties here are the specific design of the RNS hardware block for the FIR filter and the specifics of the implementation of the LMS update hardware.



a) Block Diagram of LMS Adaptive Filter

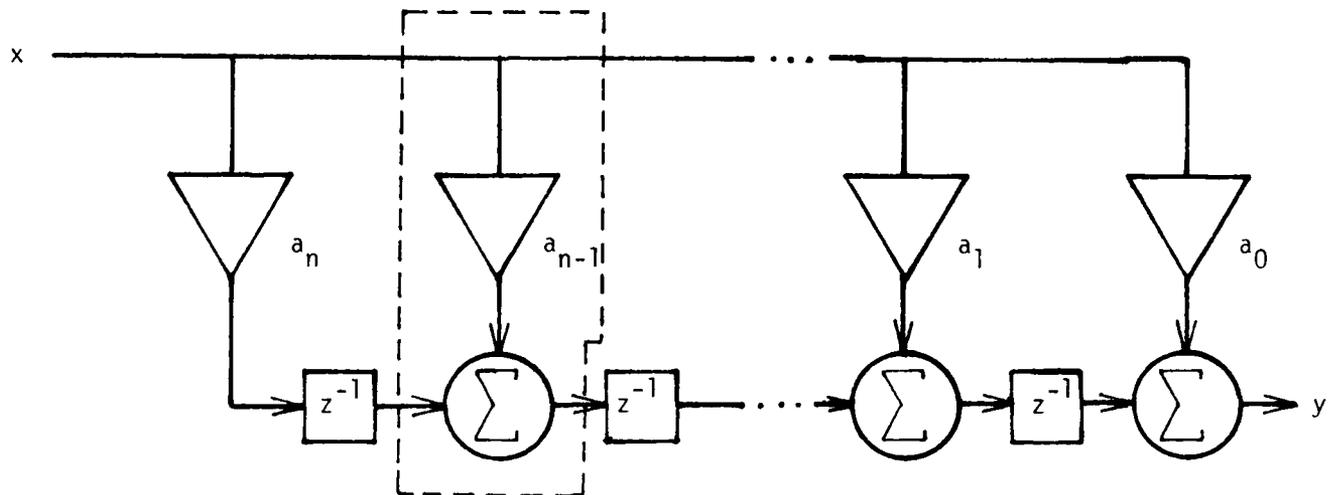


b) Block Diagram of LMS Algorithm

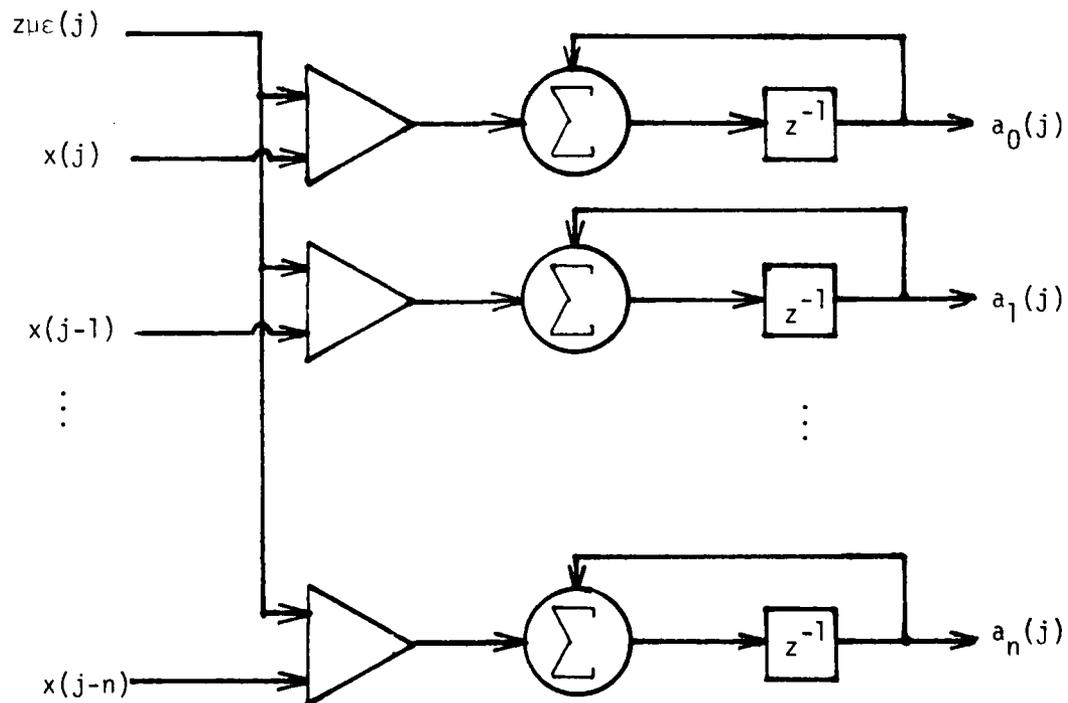


c) Symbolic Representation of LMS Adaptive Filter

FIGURE 2.21. LMS Adaptive Filter



a) Different Implementation of FIR Filter Suitable for Universal FIR Filter for Use with Microprocessor or Minicomputer



b) Complete LMS Update Algorithm

FIGURE 2.22 Universal FIR Filter for use with Microprocessor or Minicomputer

2.23 Software FIR Filter

The objective here was to develop a software LMS update algorithm compatible with the very-high-precision (150 bit) RNS software FIR filter previously developed.

2.24 Multiple Microprocessor Adaptive Signal Extractors

The objective here was to design an adaptive FIR filter using the LMS algorithm but implemented in hardware using multiple parallel microprocessors each processing one modulo of the total three (or more) modulo RNS. Figure 2.24a shows the basic configuration for the FIR filter. Each Modulo Processor (Mod 256, 255, and 253) is an eight-bit microprocessor with sufficient hardware support to implement the tapped delay line FIR filter in software. An RNS A/D and D/A converter interfaces with the signal and another eight-bit microprocessor serves as system controller. The details of this hardware implementation were the primary concerns of this project. One additional important concern was the LMS update hardware which was done in a separate microprocessor as shown in Figure 2.24b.

2.25 Adaptive IIR Filter Using Microprocessor Controlled LDI Ladder

The objective here was to develop a new recursive adaptive filter based on the LDI ladder. The LDI ladder was implemented using the microprocessor controlled section shown in Figure 2.25a. This basic hardware was designed using RNS hardware modulo 16, 15, 13 and 11. It was then used to construct the LDI ladder of Figure 2.25b. The final part of the project was to develop an algorithm for updating the ladder weights to implement an adaptive configuration.

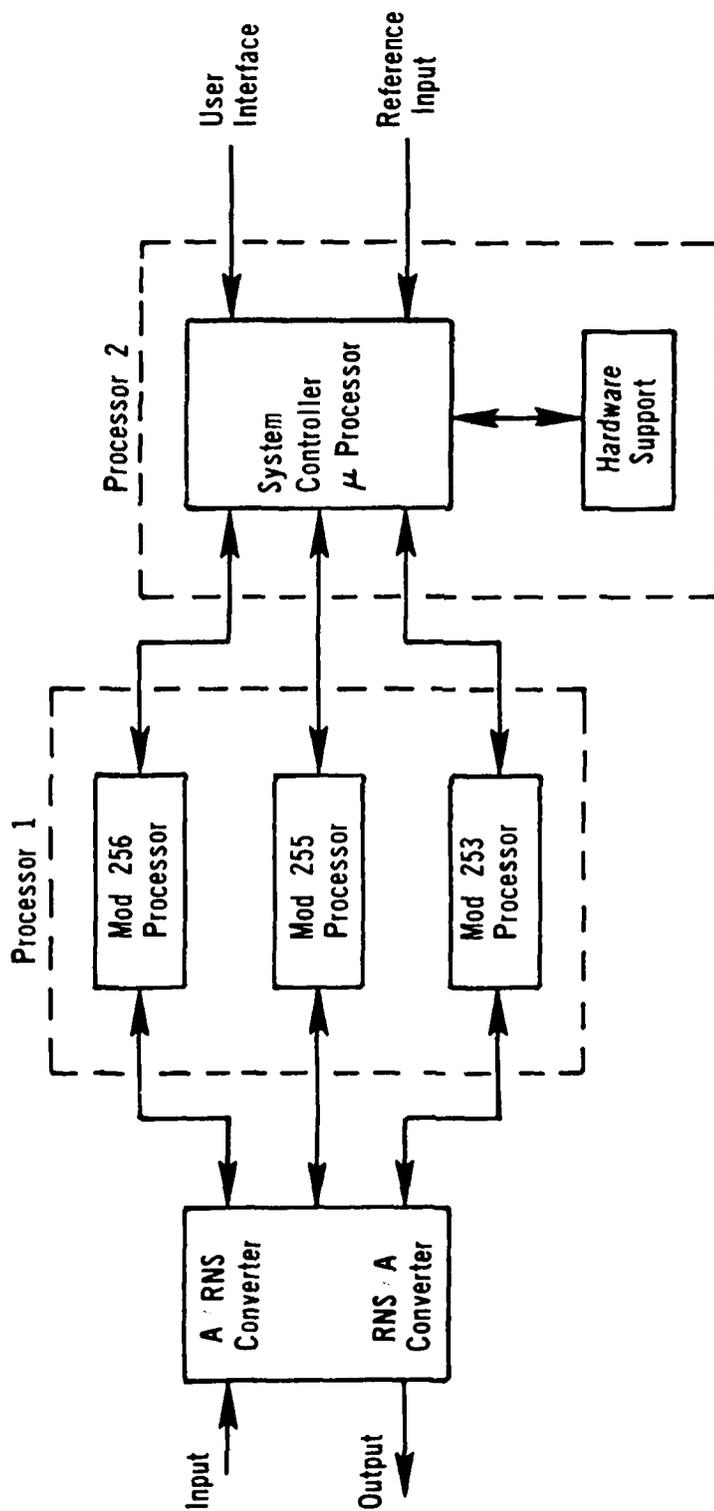


FIGURE 2.24 a) Multiple Microprocessor RNS Adaptive Filter

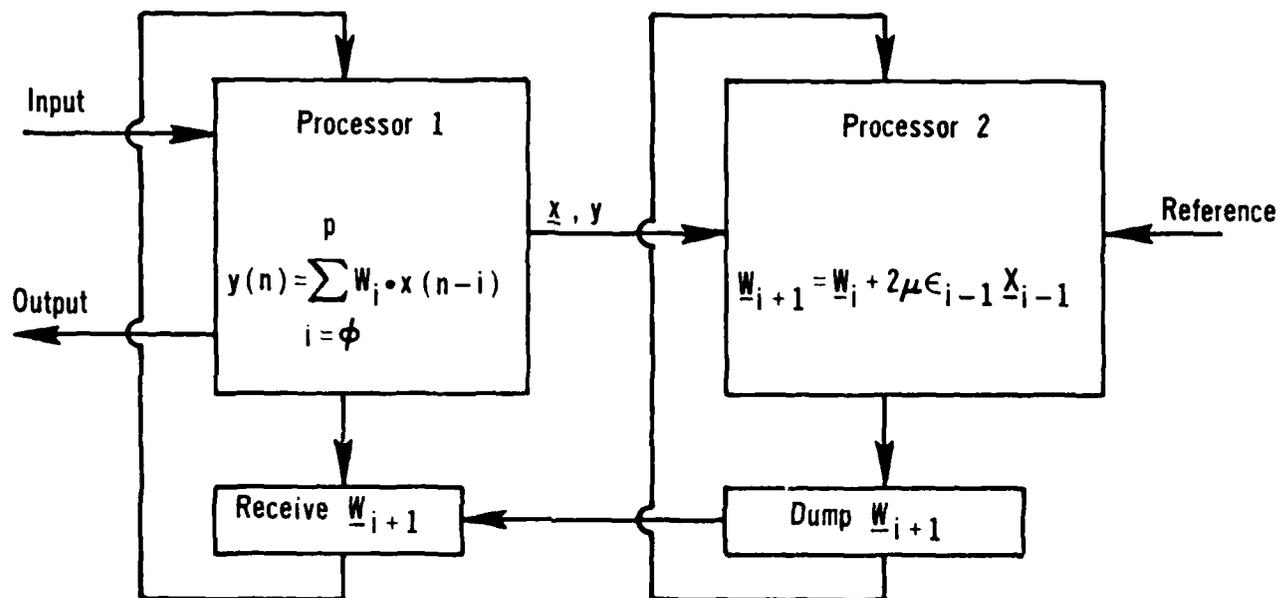
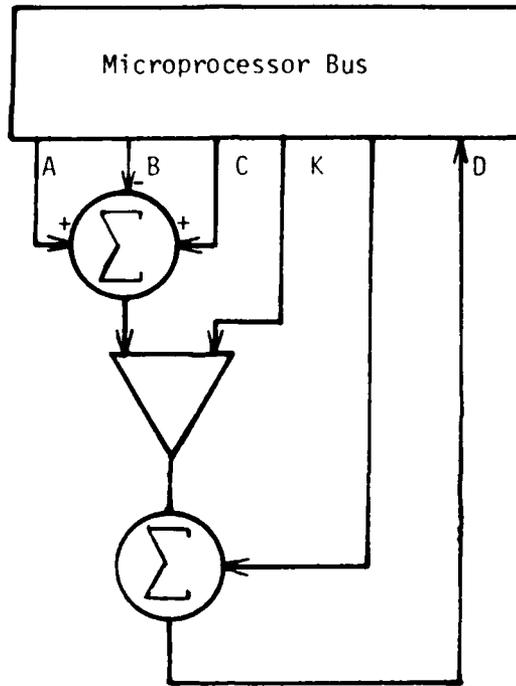
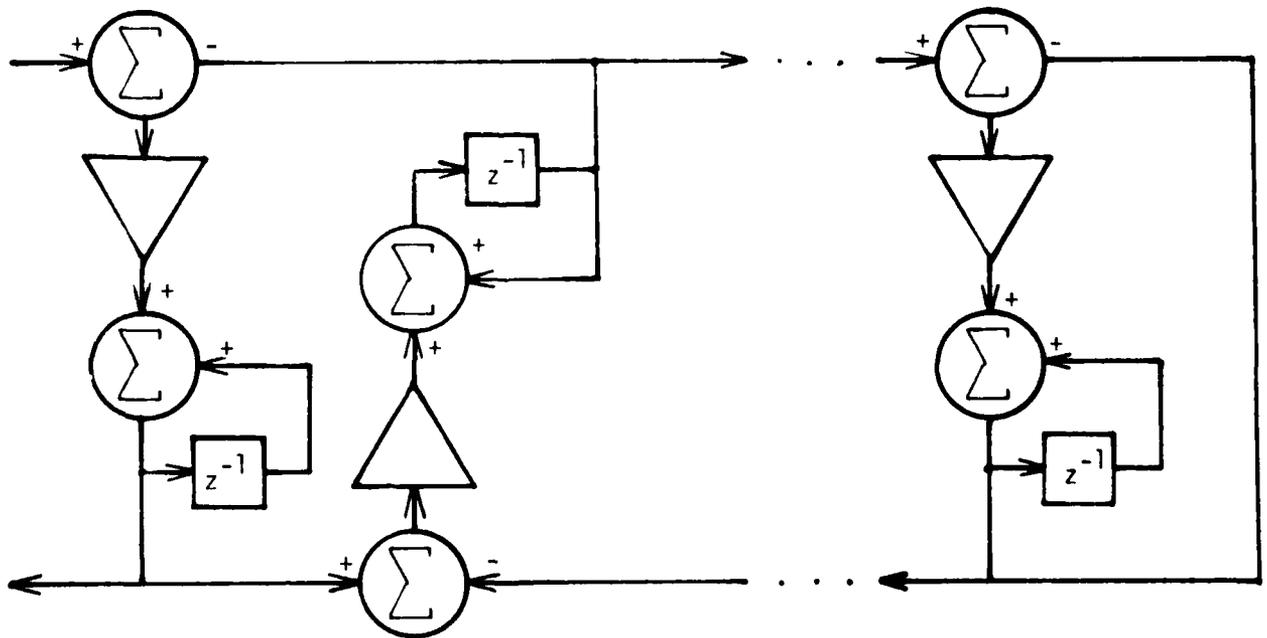


FIGURE 2.24 b) Hardware to Implement LMS Algorithm for Multiple Microprocessor RNS Filter



2.25 a) Universal Filter Hardware as Originally Proposed



b) Use of Modified Universal Filter Hardware to Produce LDI Ladders

FIGURE 2.25

3.0 RESULTS AND STATUS OF THE RESEARCH

3.1 Results for Part 1

3.11 Our comprehensive theoretical analysis [4.1-2] reveals that the novel two-stage adaptive signal extractor has excellent potential for noise cancellation with minimal signal distortion due to signal leakage into the noise reference. Although a fundamental trade-off between noise reduction and distortion control was discovered, this trade-off is quite favorable in that the distortion that would be introduced by a conventional single stage canceller can be significantly reduced with only a small loss in noise cancellation capability. In order to corroborate these theoretical predictions we have assembled a sophisticated multipurpose simulation package. Although the programs have all been written, debugged, and preliminary simulations carried out (See paragraph 3.15 below) a comprehensive set of simulations that will determine the capabilities as well as limitations of the two-stage device are still in the process of being carried out. The results will be reported in the Final Report for AFOSR Grant number 80-0189.

During our studies of the two-stage signal extractor shown in Figure 2.11, it was discovered that with a minor modification, it is applicable in situations where the signal is not detectably intermittent, but rather where the signal fluctuates slowly relative to noise fluctuations [4.1-8]. The modified two stage signal extractor is shown in Figure 3.11a. The differencing device Δ and its inverse serve to reduce the signal level relative to the noise level prior to noise cancellation, and then to restore the signal level prior to distortion reduction. This modified two-stage device is currently being tested with our multipurpose simulation package.

For applications where the signal is neither detectably intermittent nor slowly fluctuating relative to the noise, but where a pseudo random pilot

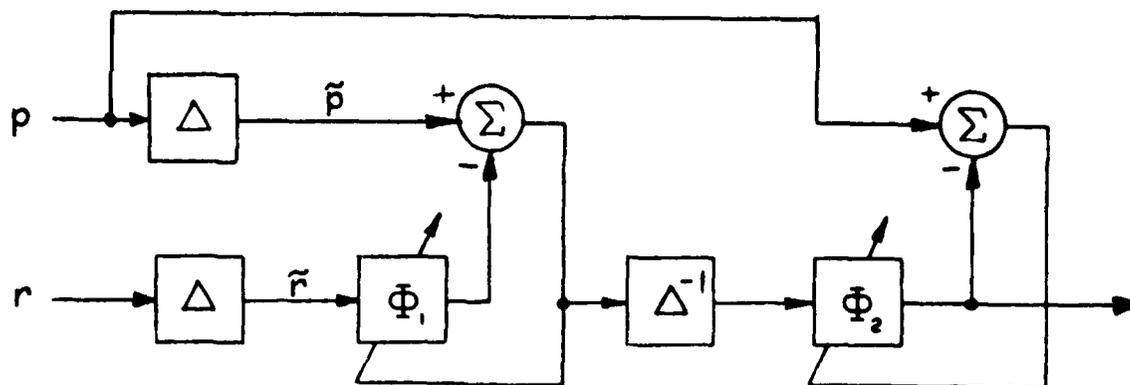


FIGURE 3.11a. Two-stage adaptive noise canceller for slowly fluctuating signals ($\Delta(z) = 1 - z^{-1}$)

signal can be superimposed on the original signal and transmitted simultaneously, we have discovered several multi-stage configurations that will remove distortion introduced in the process of noise cancellation. In the first such device [4.1-9], which is shown in Figure 3.11b, the first stage cancels noise and the second stage reduces distortion (and cancels the embedded pilot). In the other two devices [4.1-10], [4.1-11], which are shown in Figures 3.11c and d, the first stage cancels noise, the second stage cancels the embedded pilot signal, and the third stage removes signal distortion. Furthermore, as discussed in paragraph 3.13 following, these latter two three-stage devices can remove channel-induced distortion as well as distortion introduced in the noise cancellation stage. These three-stage signal extractors are currently being tested by simulation.

Another novel adaptive signal extractor that was discovered in our studies of the various approaches to distortion reduction after noise cancellation provides an alternative to Gitlin's recursive-like configuration for noise cancellation (without significant signal leakage into the noise reference) that avoids the possible instability of the inverse filter ϕ_p^{-1} shown in Figure 3.11e. This alternative [4.1-12] is shown in Figure 3.11f. The auxiliary adaptive filter ϕ_a attempts to match the inverse ϕ_p^{-1} but is guaranteed to be stable since it is non-recursive.

3.12 Our comprehensive analysis [4.1-13] reveals that our scheme for hybrid (MMSE/MMSO) adaptation of dual-filter signal extractors has excellent potential for outperforming the conventional dual-filter that is periodically adjusted MMSE in applications where the rate of nonstationarity of signals and noises exceeds the rate of periodic training. Although our idealized theoretical analysis reveals that the cascade structures shown in Figures 2.12b and c are superior to the parallel structure shown in Figure 2.12a, this

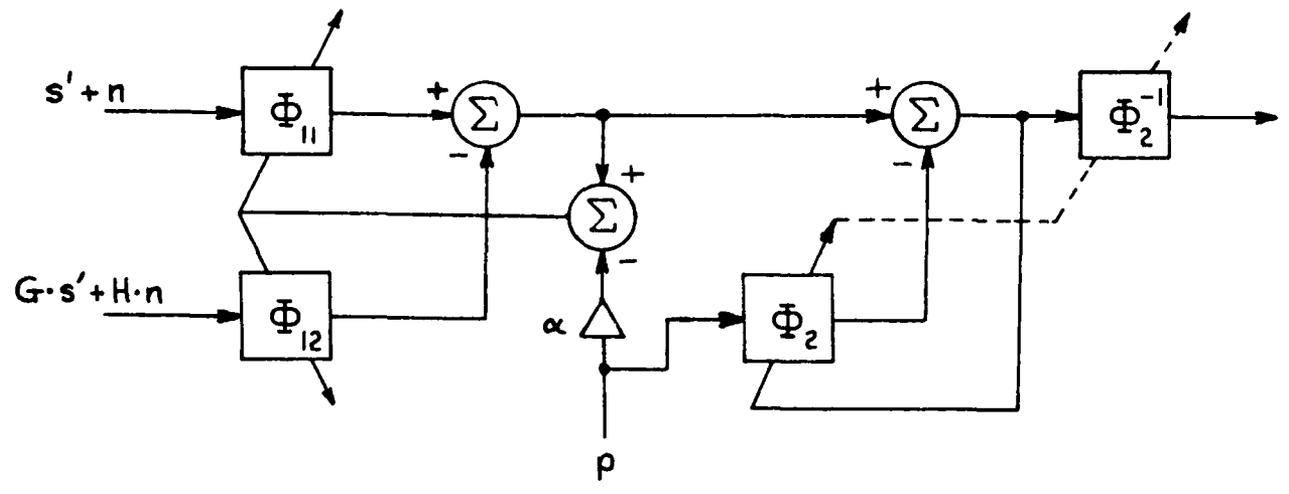


FIGURE 3.11c. Pilot aided three-stage adaptive noise canceller ($s' = s + p$)

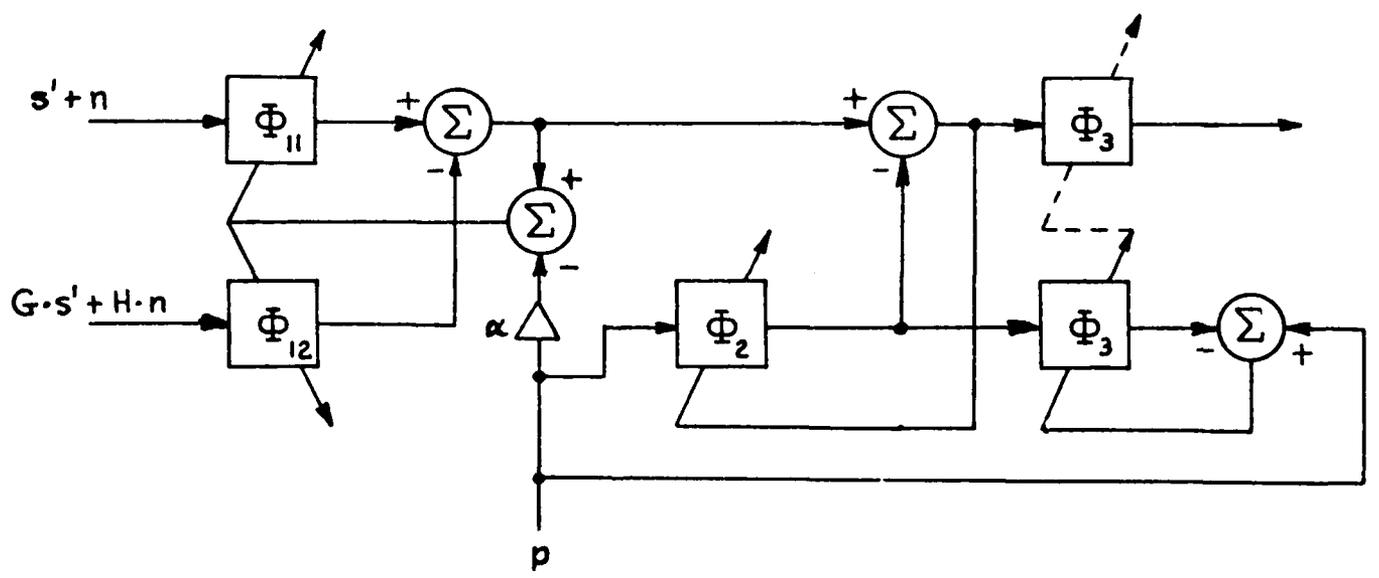


FIGURE 3.11d. Alternative pilot aided three-stage adaptive noise canceller ($s' = s + p$)

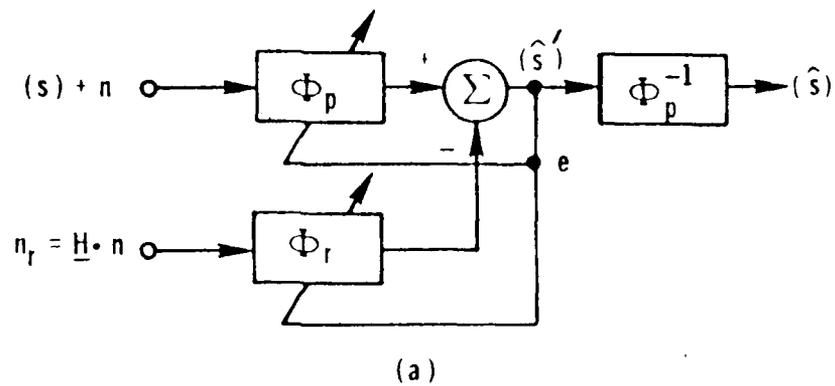


FIGURE 3.11e. Gitlin's Recursive-Like Canceller.

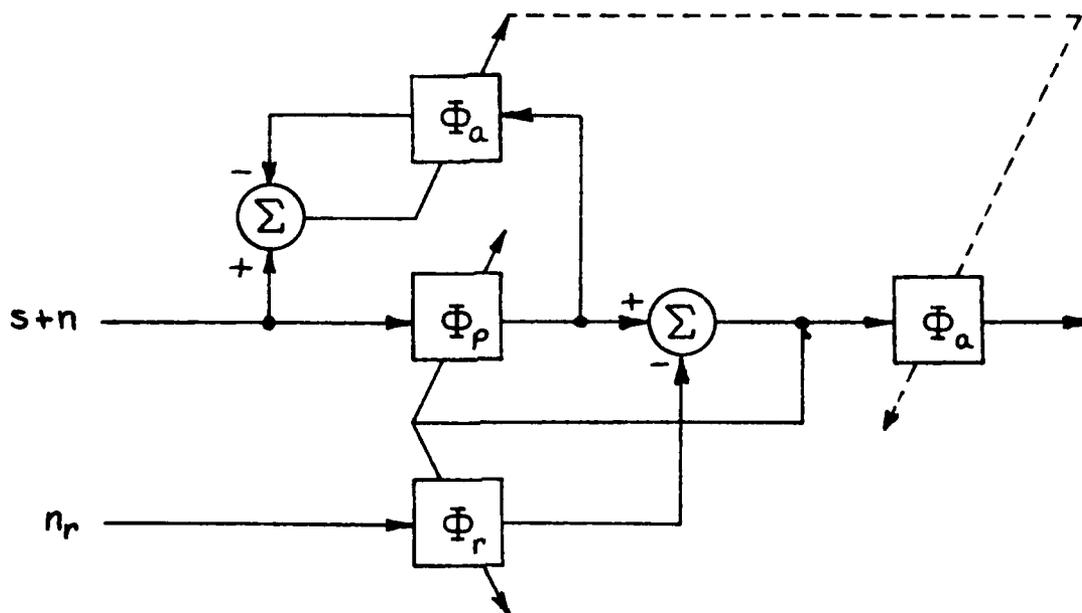


FIGURE 3.11f. Alternative recursive-like noise canceller that avoids potential instability of ϕ_p^{-1}

conclusion could conceivably break down in practice. Simulations to be carried out in the future will resolve this question, and will determine the actual capabilities and limitations of both dual-filter structures.

3.13 After preliminary study of the decision-directed dual-filter adaptive signal extractor for dual-channel digital data transmission, and assessment of the exceedingly large body of research, reported in the literature, on the decision-directed approach to adaptation, we decided to investigate an alternative approach based on the use of a source-embedded pilot signal for adaptation. Although this alternative has received some attention in the past it has not been exploited to nearly the extent that the decision-directed approach has. Furthermore, the embedded pilot approach appears to have much broader application as discussed in our report [4.1-11] which includes a comprehensive theoretical analysis of several multi-stage configurations including the three-stage devices shown in Figures 3.11c and d. The results of our theoretical analysis indicate that these new adaptive signal extraction configurations have excellent potential for simultaneous reduction of channel-induced distortion and cancellation of noise and interference. The actual capabilities and limitations of these devices are currently being determined by simulation, using our multipurpose simulation package. The results will be reported in the Final Report for AFOSR Grant number 80-0189.

3.14 Preliminary investigation of the coupled signal extractors described in research objective 2.14 revealed that the filters ϕ_{p1} and ϕ_{p2} will introduce signal distortion if a training signal or a pilot signal is not used. As a result, this objective was absorbed into the two studies, described under sections 3.12 and 3.13 above, on hybrid adaptation and adaptation with an embedded pilot.

3.15 Our completed simulation program is quite flexible in that it can be used to simulate various multi-stage configurations and it allows for specification of numerous parameters of the filters, adjustment algorithms, signal and noise models, and performance measures. Furthermore, the program provides graphs with theoretical predictions and simulation results superimposed for ease of comparison.

Our theoretical model and mathematical analysis presented in [4.1-3] yields a theoretical exponential learning curve (evolution of mean squared error) for uncorrelated data, and yields upper and lower bounding exponential learning curves for correlated data. These theoretical curves are shown together with curves from ensemble averages of 300 and 800 simulations in Figures 3.15a and b. Figure 3.15c shows a single sample path from such an ensemble to illustrate the difference between the evolution of squared error, and of mean squared error.

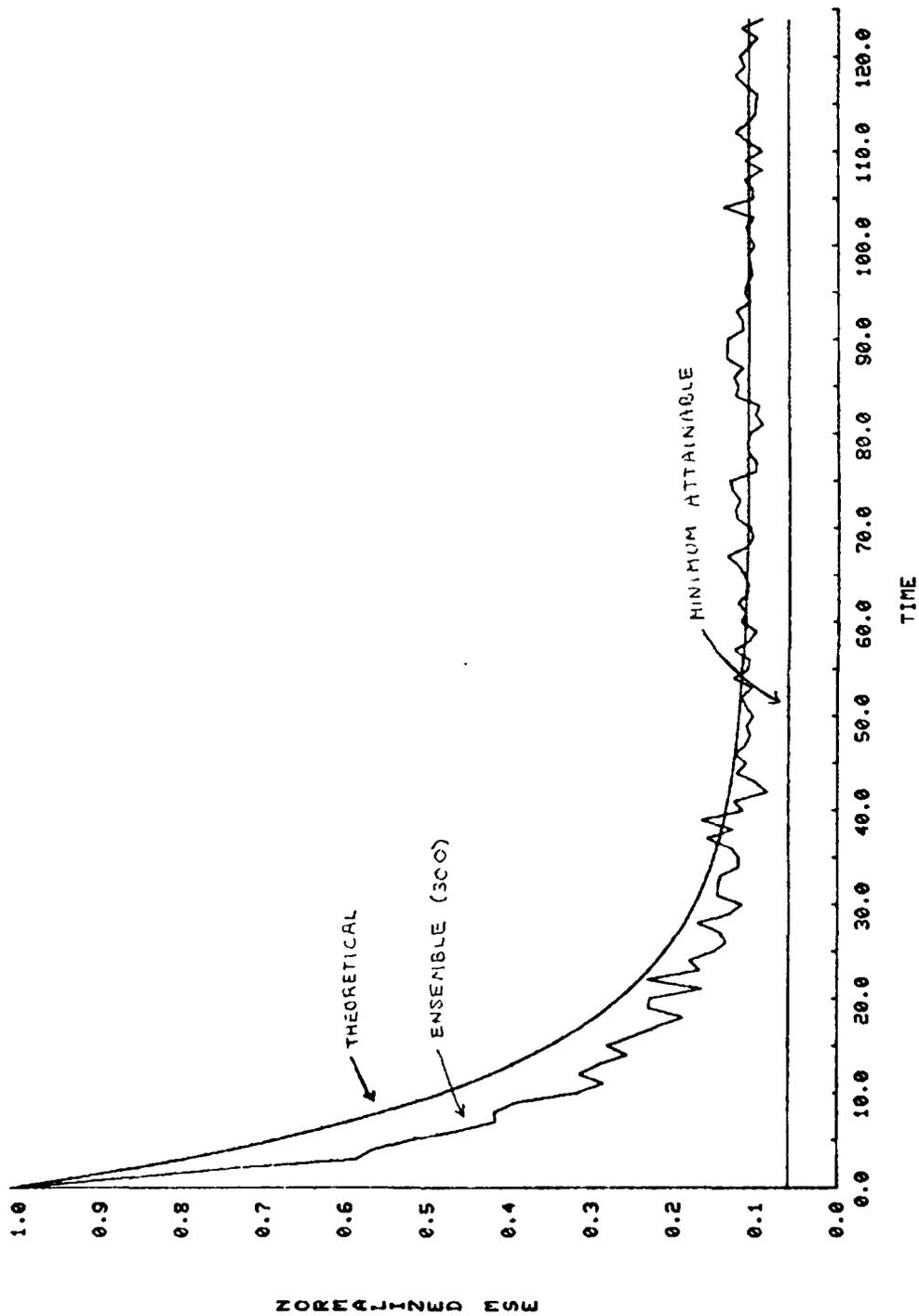


FIGURE 3.15 a. Learning curve for uncorrelated data

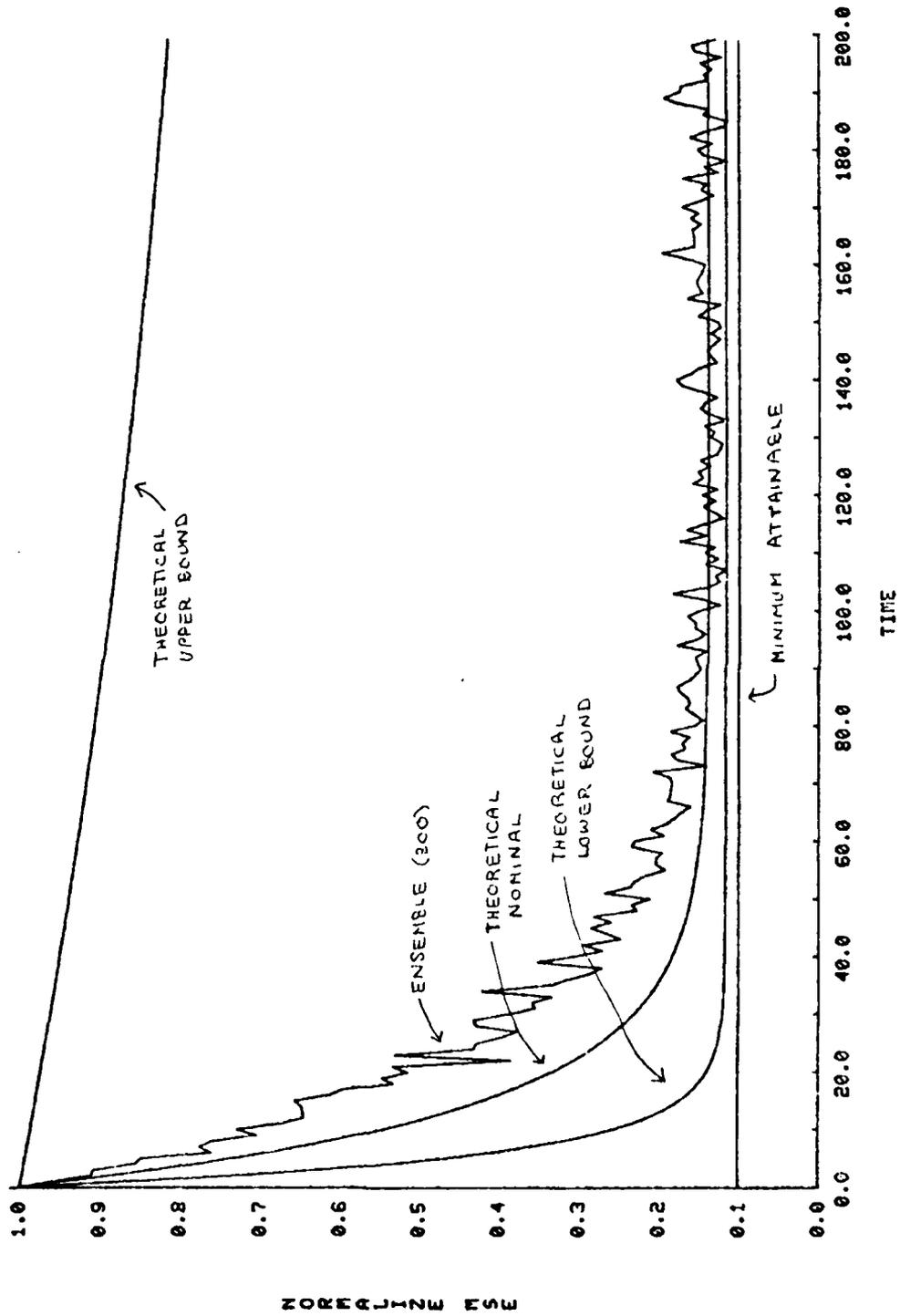


FIGURE 3.15 b. Learning curve for correlated data

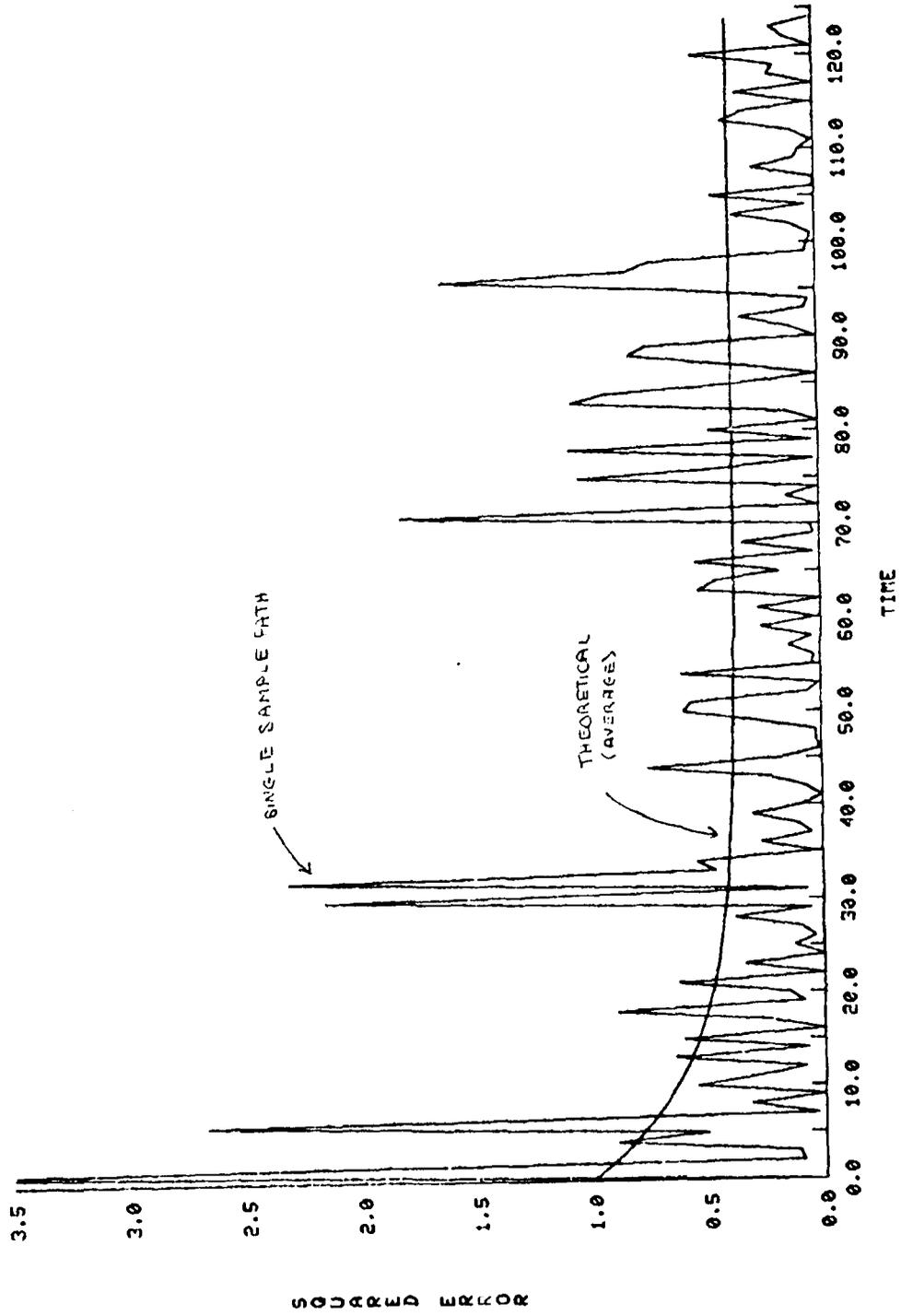


FIGURE 3.15 c. Single sample learning curve for uncorrelated data

3.2 Results for Part 1

3.21 ROM Table Look-Up Filter

The key to building high-speed adaptive digital filters using RNS arithmetic hardware is to develop a pipeline structure such that movement of samples through the pipeline is limited only by the time it takes to do one ROM table look-up. Since even inexpensive ROMs (under \$3.00) are available with look-up times in the 10-100 nanosecond range, 10-100 MHz throughput is readily attainable.

The pipeline structure chosen for this project is a modification of the FIR filter of Figure 2.22a. The modification consists of placing a delay (z^{-1}) after each multiplier in the figure and one additional delay after the summer which forms the output y . Once this is done, the structure has a delay after every single arithmetic operation (i.e.: after each multiplier and each adder). Thus data may be moved through the filter from delay to delay at a rate limited only by the time required to perform one arithmetic operation (one table look-up in RNS arithmetic).

As a result of pipelining the filter of Figure 2.22a, two units of delay are added to the filter modifying its difference equation to:

$$y(i) = \sum_{j=0}^n a_j x(i-2-j) .$$

The RNS chosen for the FIR pipeline is modulo 16, 15, 13, 11 equivalent to 15.7 bits in binary. Thus the pipelined version of Figure 2.22a is separately realized for arithmetic in each of the four moduli. As can be seen, these moduli are all representable in four bits, hence each arithmetic operation is accomplished by table look-up in a 256x4 ROM. For an adaptive filter with n weights this will require $2n-1$ ROMs and $2n$ delays per modulo

(each delay requires 4 "D" flip-flops or one four-bit register). This system would be well suited for operating on eight-bit input data since its nearly 16-bit dynamic range would allow for multiplication of the full eight-bit input word by an eight-bit coefficient. Higher dynamic range may be achieved by simply adding additional moduli.

The LMS update algorithm requires the computation of the gradient estimate $2\mu\epsilon(i)x(i-j)$ for coefficient j at time sample i where x is the input, $\epsilon(i) = y(i) - d(i)$, y is the output, and d is the desired output. The step size μ is a fractional quantity and as such multiplication by μ must be done in RNS using the scaling multiplier proposed by Soderstrand and Fields (Electronics Letters, Vol. 13, No. 6, pp. 164-166). This multiplier requires a fixed denominator for μ and this denominator must be the product of additional mutually prime moduli to be added to the existing moduli 16, 15, 13, 11. The new moduli chosen were 31, 29, and 23 resulting in a denominator of μ equal to the product of these moduli 20677. Thus μ itself is limited to the range of the original moduli (i.e.: $\pm 16 \cdot 15 \cdot 13 \cdot 11 / 2$ or -17160 to 17159) divided by 20677 resulting in $-.83 < \mu < .83$. The smallest non-zero magnitude of μ is $1/20677$ or 4.83×10^{-5} .

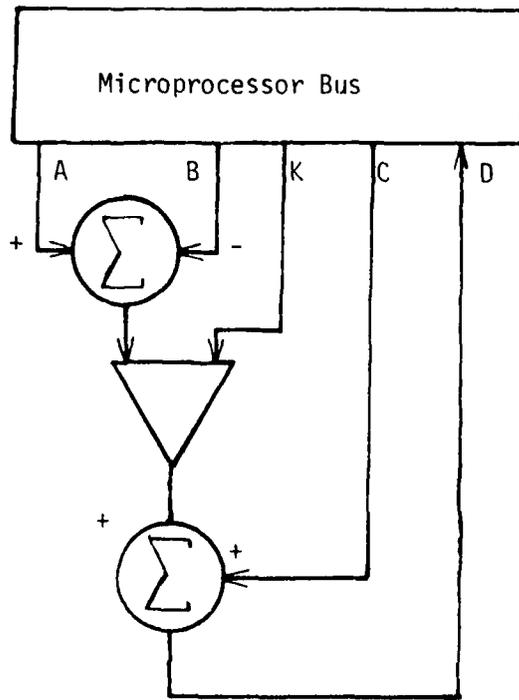
In order to add these new moduli we must have the representation of x , μ , y , and d in the new moduli as well as the old. Fortunately, we may assume that μ and d are provided in all moduli and the A/D and D/A conversion for x and y can provide the additional moduli for these quantities. In paper [4.2-1, 6.2-1] the RNS A/D and D/A operations are described. The input x will simply be converted to all needed moduli. The output y , however, must go through a base extension (see M. A. Soderstrand and E. L. Fields, "Multipliers for Residue-Number-Arithmetic Digital Filters," Electronics

Letters, Vol. 13, No. 6, pp. 164-166). This base extension is combined with the RNS D/A conversion as described in paper [4.2-1, 6.2-1] and [4.2-15] but does result in an additional delay of 4 (one for each original moduli) so the extended y is delayed by 6. The subtraction of d to form c , the multiplication by x , and the multiplication by the numerator of μ each take one additional delay for a total of $6 + 3 = 9$. Finally scaling by the denominator of μ takes 3 delays (one for each added moduli) and the adding of the negative gradient estimate to the coefficient takes an additional delay for a total of 13. Hence the entire LMS algorithm requires 13 delays, but may be pipelined so that the overall sampling rate and update rate remains one table look-up and the complete adaptive filter operates in the 10-100 MHz range.

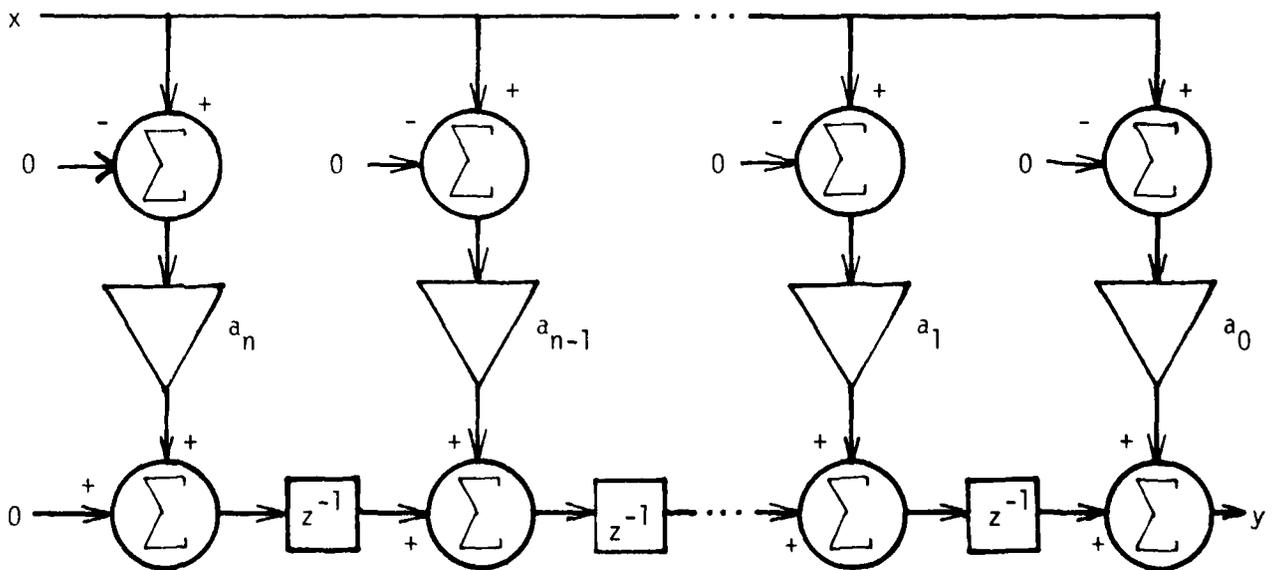
3.22 Universal Adaptive FIR Filter for Use with Microprocessors

This project has yielded the most results of all projects in the original proposal. One prime reason for this is a slight modification to the originally proposed hardware of Figure 2.24a to yield the hardware of Figure 3.22a. As a result the hardware can now be used in both FIR filter construction (Figure 3.22b) and LDI Ladder [see section 3.25] construction (Figure 3.25b). Furthermore, the flexibility of this microprocessor controlled hardware allows construction under software control of these and other structures.

The hardware of Figure 3.22b was built using ROM table look-up RNS techniques in modulo 16, 15, 13 and 11 [4.2-5, 4.2-16, 6.2-4, 6.2-5]. Also an LMS update board was constructed to assist in the LMS algorithm. These boards were then used to implement under software control on the IMSAI 8080 based microprocessor system both the FIR filter of Figure 3.22b and the dual delay line IIR filter of Figure 3.22c [4.2-16]. The resulting filters



a) Modified Universal Filter Hardware



b) Use of Modified Universal Filter Hardware to Produce FIR Filter

FIGURE 3.22

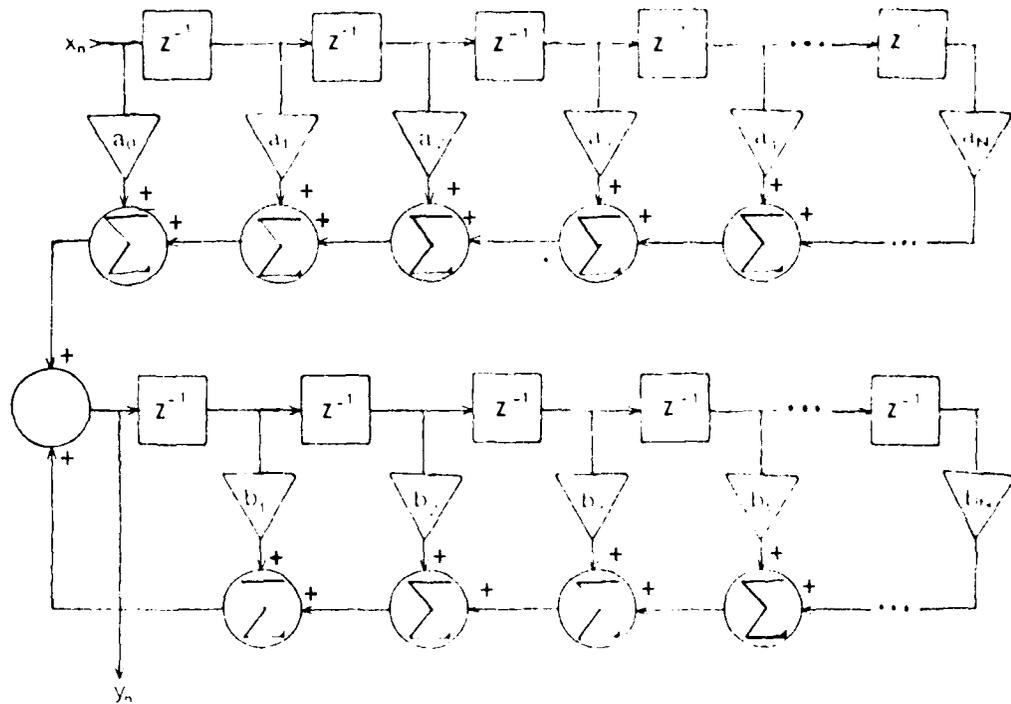


FIGURE 3.22 c Dual Delay Line Filter

have sampling rates which are dependent on the total number of weights in the digital filters. For filters with one through 8 weights, sampling rates vary from 2kHz to 500Hz.

This same hardware also can be used under software control to yield other configurations such as the LDI ladder (see section 3.25). However, the most promising concept may be the ability to use the microprocessor control to actually adapt structure as well as weights. This new concept for which the name "Totally Adaptive Filter" has been coined is described in detail in section 3.26.

3.23 Software FIR Filter

Due to the time spent on the other projects of this section and the discovery of a totally new project (section 3.26) no work was done on the 180-bit adaptive FIR filter during this contract period. All that remains to be done is the implementation and testing of an appropriate version of the LMS algorithm. This will be completed under AFOSR grant 80-0186.

3.24 Multiple Microprocessor Adaptive Signal Extraction

In this project the inherent parallel nature of the RNS is capitalized on by using a separate 8-bit 8080 microprocessor to process each of three moduli; 256, 255, and 253. Figure 2.24 shows the basic multiple microprocessor system and Figure 3.24a shows one of the three microprocessors (MOD 255) with its peripheral components. The MOD 255 multiplier and MOD 255 accumulator are hardware arithmetic units which themselves are RNS based [4.2-4, 4.2-6, 6.2-6]. This processor implements a complete FIR filter in modulo 255 arithmetic. It receives modulo 255 input from the RNS A/D converter and delivers modulo 255 output to the RNS D/A converter [4.2-1, 6.2-1]. Although each microprocessor operates completely independently and in parallel,

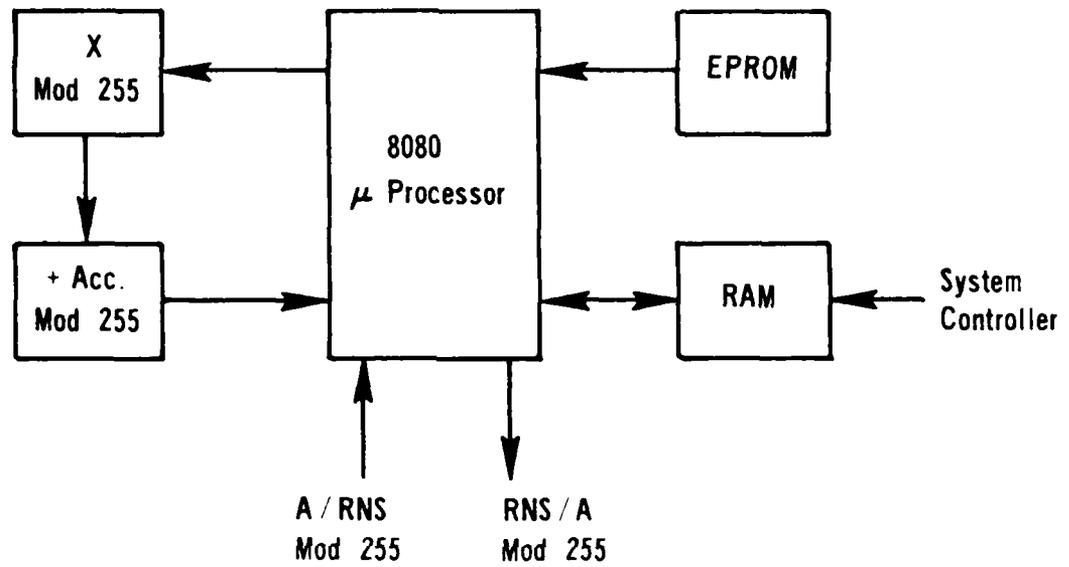


FIGURE 3.24 a

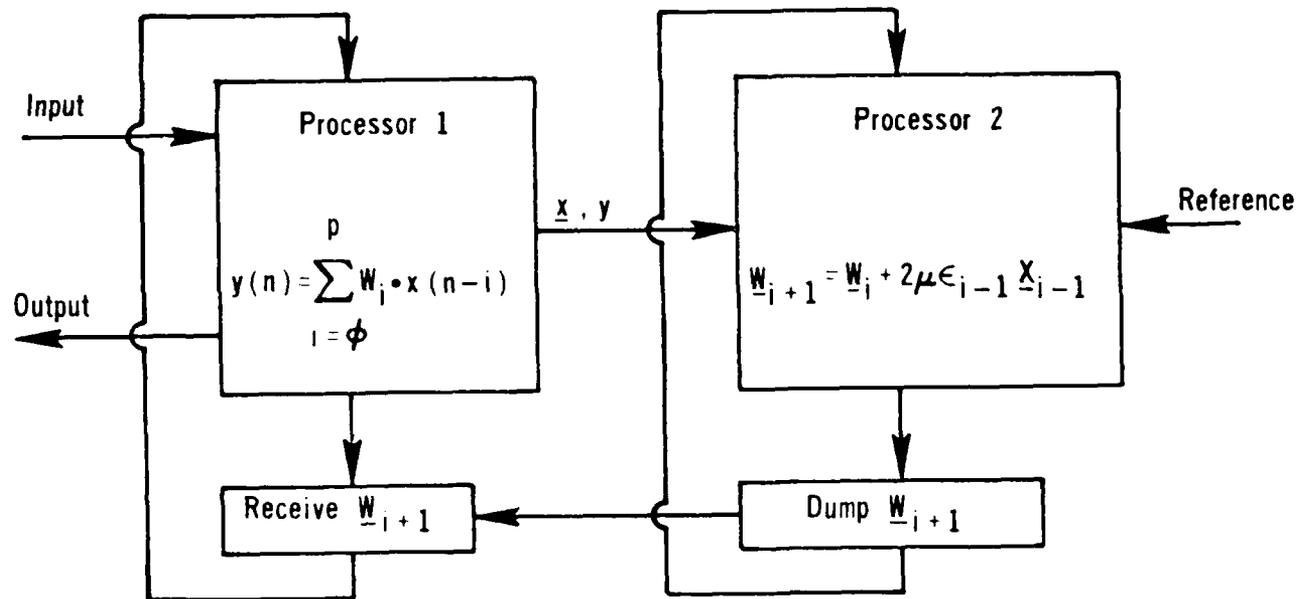


FIGURE 3.24 b

the overall result when interpreted in the RNS is an FIR filter with nearly 24 bits (256x255x253 range) of precision.

The LMS update algorithm is implemented in yet a separate microprocessor as indicated in Figure 3.24b. Furthermore there are five different update options (modifications of the LMS algorithm) available as follows:

1. Standard LMS algorithm
2. Same as option 1 except error used is average of last n error values
3. Standard LMS algorithm except update is done only every n samples (slowed down LMS)
4. Same as option 3 except error used is average of last n error values
5. Standard LMS algorithm except update is done only on one coefficient at a time, thus taking n samples to update n coefficients
6. Same as option 5 except error used is average of last n error values

The advantage of averaging error values as in options 2, 4, and 6 is that it tends to reject uncorrelated and leakage noise. The advantage of options 3 and 5 are hardware oriented. Each allows more time for the update hardware to do its processing thus allowing a less complex and less costly implementation with potentially higher speed.

The important components of the multiple microprocessor system are outlined in a series of papers [4.2-4, 4.2-5, 4.2-6, 4.2-12, 4.2-15] and oral presentations [6.2-4, 6.2-5]. The complete details of the entire system are documented in a University of California, Davis (UCD) Signal and Image Processing Laboratory (SIPL) Technical Report (UCD SIPL Technical Report) [4.2-10].

3.25 Adaptive IIR Filter Using LDI Ladder

As discussed in section 3.22, the Universal Filter hardware was modified to be capable of implementing the LDI ladder. A series of papers, reports,

and oral presentations [4.2-5, 4.2-8, 6.2-4] outline various components of the system and the complete details are in a UCD SIPL Technical Report [4.2-16]. Although the hardware for the LDI ladder and for the LMS update algorithm was completed, the required update algorithm for the LDI ladder was not addressed. This will be developed under AFOSR grant 80-0186.

3.26 Totally Adaptive Filters

As discussed in section 3.22, the flexibility of the universal filter hardware in constructing both non-recursive filters such as that of Figure 3.22c and recursive filters such as that of Figure 3.22e led to the idea of designing an algorithm that would adapt structure as well as weights. As part of the effort directed at recursive-like filters a new algorithm for updating true recursive filters was developed [4.2-2]. This algorithm uses Gitlin's recursive-like structure to update the dual-delay-line recursive structure of Figure 3.22e. A comparison of the LMS FIR algorithm, the Stearns-White IIR algorithm, the Feintuch IIR algorithm, and the new Soderstrand-Gitlin IIR algorithm showed considerable promise for the new technique [4.2-3]. However, the overall performance of the simple non-recursive LMS adaptive filter was hard to surpass [4.2-3]. Unless one knew "a-priori" which structure to choose, the non-recursive LMS structure was best.

However, with the flexibility of the universal filter hardware, the microprocessor could actually try different structures and choose the optimum structure without any "a-priori" knowledge of the system. This concept was first presented in an oral presentation at the digital signal processing workshop at the 1980 IEEE International Symposium on Circuits and Systems [6.2-4] and has since been written up in a series of papers

[4.2-11, 4.2-13, 4.2-14]. Simulation studies of the entire totally adaptive filter were carried out and reported in a UCD SIPL technical report [4.2-9].

The basic structure search algorithm is implemented in the microprocessor software. The flow-chart for this structure search is given in Figure 3.26a. As a test of the totally adaptive filter, six unknown filters were used in a system identification problem. The six unknowns were all lowpass filters. Three were non-recursive, three were recursive. Two had 5 weights, two had 7 weights, and two had 9 weights. Table 3.26-1 gives the pole and zero locations of these unknown systems. A seven weight totally adaptive filter was then used to identify each of these systems. Figure 3.26b shows the error generated during the structure search. Tables 3.26-2 and 3.26-3 compare the coefficients of the unknown system to the actual estimates made by the totally adaptive filter. Table 3.26-4 compares the performance in terms of final error of the totally adaptive filter to the LMS non-recursive algorithm and to six different recursive structures using the Stearns-White algorithm. The totally adaptive filter did as well or better than any of the structures on every test conducted. Work on this project will continue under AFOSR grant 80-0186.

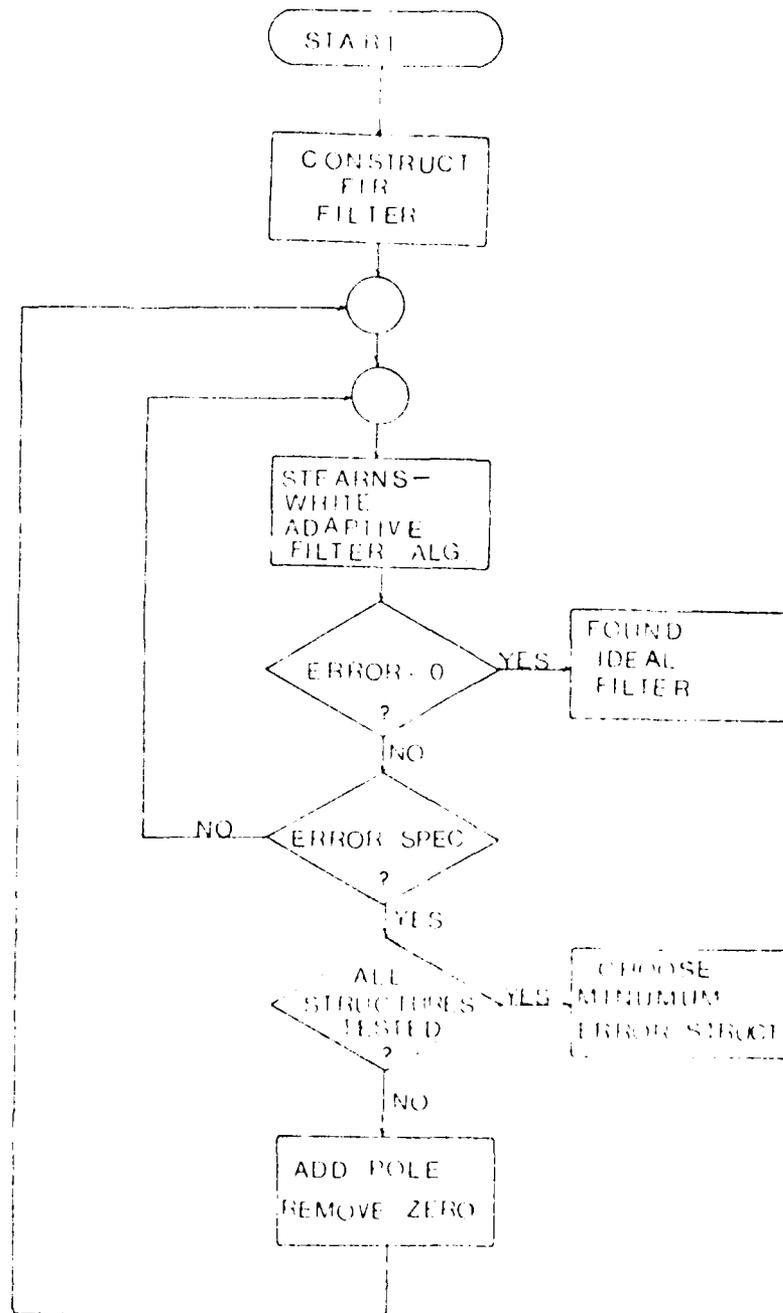


FIGURE 3.26 a. TOTALLY ADAPTIVE ALGORITHM

TABLE 3.26 - 1

UNKNOWN FILTER	ZEROS	POLES	r	θ
1	$Z_1 - Z_4$		1	180°
2	Z_1, Z_2	P_1, P_2	0.8	$\pm 175^\circ$
			0.4	$\pm 20^\circ$
3	$Z_1 - Z_6$		1	180°
4	Z_1, Z_2		0.8	$180^\circ \pm 5^\circ$
	Z_3		1	180°
		P_1, P_2, P_3	0.4	$-20^\circ, 0^\circ, 20^\circ$
5	$Z_1 - Z_8$		0.7	$180^\circ \pm 5^\circ, 180^\circ \pm 10^\circ,$ $180^\circ \pm 15^\circ, 180^\circ \pm 20^\circ$
6	Z_1, Z_2		0.7	$180^\circ \pm 20^\circ$
	Z_3, Z_4		0.7	$180^\circ \pm 25^\circ$
		P_1, P_2	0.4	$\pm 15^\circ$
		P_3, P_4	0.4	$\pm 20^\circ$

TABLE 3.26 - 2
COEFFICIENT VALUES OF UNKNOWN FILTERS

FILTER	a ₀	a ₁	a ₂	a ₃	a ₄	a ₅	a ₆	a ₇	a ₈	b ₁	b ₂	b ₃	b ₄
1	1	4	6	4	1								
2	1	1.59	0.64							.75	-.16		
3	1	6.	15	20	15	6	1						
4	1	2.59	2.23	0.64						1.15	-0.90	0.24	
5	1	5.44	13.06	18.05	15.74	8.85	3.136	0.64	0.576				
6	1	2.58	1.67	1.266	.2401					1.52	-.90	.2439	.0255

TABLE 3.26 - 3
ACTUAL COEFFICIENTS OF TOTALLY ADAPTIVE FILTER

FILTER	a ₀	a ₁	a ₂	a ₃	a ₄	a ₅	a ₆	a ₇	a ₈	b ₁	b ₂	b ₃	b ₄
1	1.0	3.999	5.999	3.999	1.0	2E-3	1E-3						
2	1.02	1.59	.740	.074						.718	-.159	.013	
3	1.0	5.999	14.999	19.999	14.99	5.999	1.0						
4	1.16	2.30	2.01	.564						1.22	-.982	.293	
5	1.01	5.41	12.94	17.87	15.58	8.85	3.14						
6	0.97	4.08	6.93	8.36	7.60	5.71	3.65						

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TABLE 3.26 - 4

UNKNOWN FILTER	NON-RECURSIVE	5 ZERO 1 POLE	4 ZERO 2 POLES	3 ZERO 3 POLE	2 ZERO 4 POLES	1 ZERO 5 POLES	0 ZERO 6 POLES	TOTALLY ADAPTIVE
1	5.1E-1	3.04E-3	7.88E-2	2.22E-1	7.2E-1	2.56	2.66	5.1E-4
2	2.28E-2	2.52E-2	1.22E-2	1.15E-2	1.31E-2	2.77E-1	1.16	1.15E-2
3	1.47E-3	5.29	6.36	6.63	6.66	6.68	6.69	1.47E-3
4	2.22E-1	3.30E-1	6.27E-1	1.06E-1	2.1E-1	2.55	2.64	1.06E-1
5	1.88E-1	4.96	5.40	6.43	6.45	6.47	6.47	1.88E-1
6	6.13E-1	2.34	2.30	3.41	3.30	3.48	3.49	6.13E-1

4.0 PUBLICATIONS

4.1 Publications for Part 1

4.11 Articles Published for Part 1

- *4.1-1. W. A. Gardner and B. G. Agee, "Two-stage adaptive signal extraction for intermittent-signal applications," IEEE International Symposium on Information Theory, June 1979.

4.12 Articles in Press for Part 1

- *4.1-2. W. A. Gardner and B. G. Agee, "Two-stage adaptive signal extraction for intermittent-signal applications," to appear in IEEE Transactions on Information Theory, Nov. 1980.

4.13 Articles Submitted for Publication for Part 1

- 4.1-3. W. A. Gardner, "Analysis of convergence of the estimated-gradient-descent algorithm for adaptive estimation, part I: stationary environment," submitted to Proceedings of the IEEE, as a regular paper, March 1980.
- 4.1-4. W. A. Gardner, "On 'Stationary and nonstationary learning characteristics of the LMS adaptive filter'," submitted to Proceedings of the IEEE as a regular paper, April 1980.
- 4.1-5. B. G. Agee and W. A. Gardner, "Embedded pilot signals for adaptive signal extraction in multi-channel environments," submitted to IEEE International Symposium on Information Theory, Feb. 1981.
- 4.1-6. J. Kazakoff and W. A. Gardner, "Simulations of two-stage adaptive signal extractors," submitted to IEEE International Symposium on Information Theory, Feb. 1981.
- 4.1-7. W. A. Gardner and M. Hajivandi, "Analysis of performance of the LMS algorithm for adaptive estimation in a nonstationary environment," submitted to IEEE International Symposium on Information Theory, Feb. 1981.

4.14 Articles in Preparation for Part 1

- 4.1-8. W. A. Gardner, "Two-stage adaptive noise cancellation for slowly fluctuating signals," in preparation for a letter in Proceedings of the IEEE.
- 4.1-9. W. A. Gardner, "Two-stage adaptive noise cancellation for arbitrary signals with an embedded pseudo random pilot signal," in preparation for a letter in Proceedings of the IEEE.
- 4.1-10. B. G. Agee and W. A. Gardner, "Three-stage adaptive signal extraction for reduction of channel distortion, noise, and interference, using an embedded pseudo random pilot signal," in preparation for a letter in Proceedings of the IEEE.
- 4.1-11. B. G. Agee and W. A. Gardner, "Partial supervision of adaptive multi-channel filters using embedded pseudo-random pilot signals," in preparation for a regular paper in IEEE Transactions on Acoustics, Speech, and Signal Processing.
- 4.1-12. W. A. Gardner, "A stable two-stage recursive-like noise canceller," in preparation for a letter in Proceedings of the IEEE.
- 4.1-13. B. G. Agee and W. A. Gardner, "Hybrid adaptation of filters for reduction of dual channel distortion and noise," in preparation for a regular paper in IEEE Transactions on Acoustics, Speech, and Signal Processing.

*Paper 4.1-2 is an expanded version of paper 4.1-1.

4.2 Publications for Part 2

4.21 Articles Published for Part 2

- 4.2-1. M. A. Soderstrand, "High speed data conversion using residue number arithmetic A/D and D/A converters," Proc. of 22nd Midwest Symposium on Circuits and Systems, Philadelphia, PA, June 1979, pp. 6-10.
- 4.2-2. M. A. Soderstrand, "Adaptive recursive filters," Proc. of 1979 International Colloquium on Circuits and Systems, Taiwan, China, July 1979.
- 4.2-3. M. A. Soderstrand, "Cost and performance comparisons of several implementations of adoptive recursive filters," Proc. of 13th Asilomar Conference on Circuits, Systems and Computers, Pacific Grove, CA, Nov. 1979, pp. 416-420.
- 4.2-4. M. A. Soderstrand and C. Vernia, "A high-speed low-cost modulo P_i multiplier with RNS arithmetic applications," Proc. of the IEEE, Vol. 68, No. 4, April 1980, pp. 529-532.
- 4.2-5. M. A. Soderstrand, C. Vernia, D. W. Paulson and M. C. Vigil, "Microprocessor controlled adoptive digital filters," Proc. of IEEE International Symposium on Circuits and Systems, Houston, TX, April 1980, Vol. 1, pp. 142-146.
- 4.2-6. M. A. Soderstrand and C. Vernia, "General modulo P_i multiplier with RNS arithmetic applications," Proc. of IEEE International Symposium on Circuits and Systems, Houston, TX, April 1980, Vol. 1, pp. 375-378.
- 4.2-7. E. L. Fields and M. A. Soderstrand, "Performance characteristics of digital ladder networks," Proc. of IEEE International Symposium on Circuits and Systems, Houston, TX, April 1980, Vol. 3, pp. 1121-1124.
- 4.2-8. D. W. Paulson, "IMSAI development system for PDP-11/34: user's manual," Report No. SIPL-80-4, ECE #146, Dept. of Electrical and Computer Engineering, University of California, Davis, January 1980.

- 4.2-9. M. C. Vigil, "A totally adaptive filter," Report No. SIPL-80-7, Department of Electrical and Computer Engineering, University of California, Davis, June 1980.
- 4.2-10. C. Vernia, "Multi-microprocessor non-recursive adaptive digital signal processing using residue number arithmetic," Report No. SIPL-80-8, Department of Electrical and Computer Engineering, University of California, Davis, June 1980.

4.22 Articles in Press for Part 2

- 4.2-11. M. A. Soderstrand and M. C. Vigil, "Simulation studies of a totally adaptive digital filter," Proc. of 23rd Midwest Symposium on Circuits and Systems, Toledo, OH, August 1980.
- 4.2-12. M. A. Soderstrand and C. Vernia, "Microprocessor controlled development system for adaptive filtering, using parallel processing and residue number arithmetic," MIMI '80, Montreal, Canada, September 1980.
- 4.2-13. M. A. Soderstrand and M. C. Vigil, "Microprocessor controlled totally adaptive digital filter," IEEE ICC '80, Rye town, New York, October 1980.

4.23 Articles Submitted for Publication for Part 2

- 4.2-14. M. A. Soderstrand, J. K. Kelley and J. J. Buteau, "A micro-processor based, RNS arithmetic, totally adaptive digital filter for system identification," submitted to 14th Asilomar Conference on Circuits, Systems and Computers, Pacific Grove, CA, November 1980.

4.24 Articles in Preparation for Part 2

- 4.2-15. M. A. Soderstrand and C. Vernia, "A new technique for number conversion from RNS to binary," in preparation for Electronic Letters.

- 4.2-16. D. W. Paulson, "Microprocessor controlled adaptive digital filtering using residue number system multiplier/accumulator and filter weight adjustment modules," Report No. SIPL-80-6, Department of Electrical and Computer Engineering, University of California, Davis.

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6.0 INTERACTIONS

6.1 Interactions for Part 1

The following oral presentation was also published in a printed proceedings and is thus listed in section 4.11 as well as here:

- 6.1-1 W. A. Gardner and B. G. Agee, "Two-stage adaptive signal extraction for intermittent-signal applications," IEEE Intern. Symp. on Information Theory, June 1979.

6.2 Interactions for Part 2

The following oral presentations that were also published in a printed proceedings are indicated by an asterisk. All such publications are also listed in section 4.21:

- *6.2-1 M. A. Soderstrand, "High speed data conversion using residue number arithmetic A/D and D/A converters," Proc. of 22nd Midwest Symposium on Circuits and Systems, Philadelphia, PA, June 1979, pp. 6-10.
- *6.2-2 M. A. Soderstrand, "Adaptive recursive filters," Proc. of 1979 International Colloquium on Circuits and Systems, Taiwan, China, July 1979.
- *6.2-3 M. A. Soderstrand, "Cost and performance comparisons of several implementations of adaptive recursive filters," Proc. of 13th Asilomar Conference on Circuits, Systems and Computers, Pacific Grove, CA, Nov. 1979, pp. 416-420.
- 6.2-4 M. A. Soderstrand, E. L. Fields, M. C. Vigil, and D. W. Paulson, "Concepts for adaptive digital filter structures," IEEE International Symposium on Circuits and Systems, Workshop on Theory and Applications of Finite Arithmetic Concepts in Digital Signal Processing, April 28-30, 1980, Houston, TX.

- *6.2-5 M. A. Soderstrand, C. Vernia, D. W. Paulson and M. C. Vigil,
"Microprocessor controlled adaptive digital filters," Proc. of IEEE
International Symposium on Circuits and Systems, Houston, TX,
April 1970, Vol. 1, pp. 142-146.
- *6.2-6 M. A. Soderstrand and C. Vernia, "General modulo P_i multiplier with
RNS arithmetic applications," Proc. of IEEE International Symposium
on Circuits and Systems, Houston, TX, April 1980, Vol. 1, pp. 375-378.
- *6.2-7 E. L. Fields and M. A. Soderstrand, "Performance characteristics of
digital ladder networks," Proc. of IEEE International Symposium on
Circuits and Systems, Houston, TX, April 1980, Vol. 3, pp. 1121-1124.

7.0 NEW DISCOVERIES/INVENTIONS

7.1 Discoveries and Inventions for Part 1

A number of new multi-stage adaptive signal extractor configurations have been invented during this research. They include those shown in Figures 3.11a, b, c, d, and f.

7.2 Discoveries and Inventions for Part 2

Important new discoveries associated with part 2 of the contract include:

1. Universal Filter Hardware (See Figure 3.22a)
2. New update algorithms including modifications to LMS (See section 3.24) and the Soderstrand-Gitlin algorithm (See section 3.26)
3. The totally adaptive filter (See section 3.26)

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