

AD-A091 90*

COLORADO UNIV AT BOULDER
HARDWARE REALIZATIONS FOR DIGITAL SIGNAL PROCESSING. (U)
OCT 80 R A ROBERTS

F/6 9/3

DAAG29-78-6-0188

UNCLASSIFIED

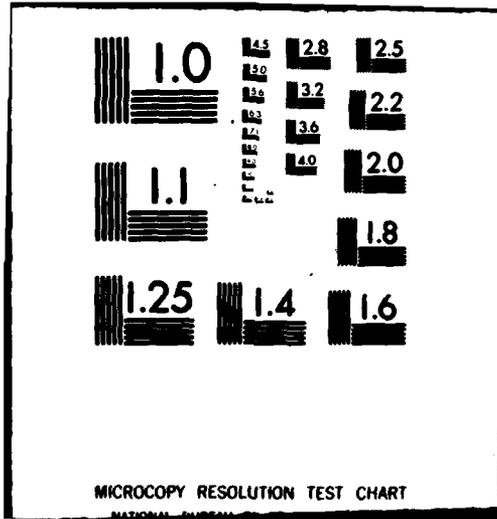
ARO-15974.1-EL

NL

1
2
3
4
5
6
7
8
9
10



END
DATE
FILMED
-BI
DTIC



UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

18

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

19

1. REPORT NUMBER 2. GOVT ACCESSION NO. 3. RECIPIENT'S CATALOG NUMBER

15974.1-EL AD-A091904 904

4. TITLE (and Subtitle) 5. TYPE OF REPORT & PERIOD COVERED

Hardware Realizations for Digital Signal Processing, Final Report 1 Sep 78 - 31 Aug 80

6. AUTHOR(s) 7. CONTRACT OR GRANT NUMBER(s)

Richard A. Roberts DAAG29-78-G-0188

8. PERFORMING ORGANIZATION NAME AND ADDRESS 9. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS

University of Colorado Boulder, CO 80309

10. CONTROLLING OFFICE NAME AND ADDRESS 11. REPORT DATE

U. S. Army Research Office Post Office Box 12211 Research Triangle Park, NC 27709 Oct 80

12. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office) 13. NUMBER OF PAGES

LEVEL 8

14. SECURITY CLASS (of this report) 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

Unclassified

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

NA

18. SUPPLEMENTARY NOTES

The view, opinions, and/or findings contained in this report are those of the author(s) and should not be construed as an official Department of the Army position, policy, or decision, unless so designated by other documentation.

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

digital signal processing digital filters
signal processing computers
speech processing
computer hardware

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Good digital filter realizations for hardware implementations, in narrowband filtering applications should have low roundoff noise, low coefficient sensitivity, and freedom from overflow oscillations. The hardware implementations presented here incorporate the above properties into a highly modular structure which can perform computations in pipeline fashion. That is, after an initial delay an output sample is obtained for each input sample. The realization and implementations discussed here contain more multipliers than direct form realizations. However, by using shorter word lengths because of their increased performance and distributed arithmetic,

AD A091904

BDC FILE COPY

DTIC NOV 18 1980

DD FORM 1 JAN 73 1473

EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

088400

8011 12 070

20. ABSTRACT CONTINUED

implementations (instead of multiplier structures) these implementations can have less total hardware complexity.

Accession For	
NTIS GRA&I	<input checked="" type="checkbox"/>
DTIC TAB	<input type="checkbox"/>
Unannounced	<input type="checkbox"/>
Justification	
By	
Distribution/	
Availability Codes	
Dist	Avail and/or Special
A	

FINAL REPORT

1. ARO Proposal Number: P-15974-EL
2. Period Covered by Report: September 1, 1978 to August 31, 1980
3. Title of Proposal: Hardware Realizations for Digital Signal Processing
4. Contract or Grant Number: DAAG29-78-G0188
5. Name of Institution: University of Colorado, Boulder, Colorado 80309
6. Author of Report: Richard A. Roberts
7. List of Manuscripts Submitted or Published During this Period: see attached
8. Scientific Personnel Supported by this Project and Degrees Awarded:
 - a. Masud Arjmand - Ph.D. student who will complete his studies in the spring of 1981. Supported 1/2 time in AY and full time summers.
 - b. David Kjosness - M.S. student supported 1/2 time for one semester. He graduated in June 1979.
 - c. C.T. Mullis supported for a total of four months full time in summers of 1979 and 1980
 - d. R.A. Roberts 1980
 - e. Larry Germann - M.S. student who is constructing a piece of hardware and has received support in the form of hardware supplies. He has received no salary.
 - f. Alberto Mordojovich - M.S. student who received a small amount of computer and typing support.

1. W.L. Mills, C.T. Mullis, R.A. Roberts, "An Iterative Estimation Technique for Power Spectra by an ARMA Model," Proceedings of the International Conference on Acoustics, Speech and Signal Processing, Denver, April 1980.

Abstract: Spectral pole-zero models are used as a method of reducing the number of parameters needed to represent certain classes of spectra, e.g., spectral envelopes having deep valleys. We present here an iterative algorithm for Autoregressive-Moving Average (ARMA) models that is based on a repeated use of Levinson's algorithm to obtain both poles and zeros. The procedure allows one to increase the number of poles and zeros iteratively, similar to linear prediction methods. Empirical results indicate that a slow growth of the orders of the denominator and numerator polynomials usually produces better ARMA models.

2. M. Arjmand, C.T. Mullis, R.A. Roberts, "A Modular Hardware Structure for Digital Filtering," Proceedings of the International Conference on Acoustics, Speech and Signal Processing, Denver, April 1980.

Abstract: Good digital filter realizations for hardware implementations, in narrowband filtering applications should have low roundoff noise, low coefficient sensitivity, and freedom from overflow oscillations. The hardware implementations presented here incorporate the above properties into a highly modular structure which can perform computations in pipeline fashion. That is, after an initial delay an output sample is obtained for each input sample. The realization and implementations discussed here contain more multipliers than direct form realizations. However, by using shorter word lengths because of their increased performance and distributed arithmetic implementations (instead of multiplier structures) these implementations can have less total hardware complexity.

3. M. Arjmand, R.A. Roberts, "Efficient Hardware Implementations for Fixed Point Digital Filters," Proceedings of the International Conference on Circuits and Systems, Houston, April 1980.

Abstract: The synthesis of a digital filter or digital signal processor is made up of several design decisions. From a given set of specifications one first obtains an external characterization of the filter, usually expressed in terms of a transfer function $H(z)$. Given the transfer function, the next step is to choose a realization for the filter which defines the internal structure of the filter. The choice of a realization is usually based on minimizing the effects of finite register length which include roundoff noise, coefficient truncation, overflow oscillations and zero-input limit cycles. After synthesizing a realization for $H(z)$ that optimizes one or more of the finite register effects, one is faced with a hardware implementation decision. Which hardware implementation is the most desirable?

A hardware implementation decision involves the consideration of several parameters such as data throughput, output signal quality, hardware complexity, total power consumed, etc. For a given output signal quality hardware structures are often compared on the basis of speed and hardware complexity. How should one measure hardware complexity? There have been several measures used in the literature including pin count, chip count, total chip cost in dollars, number of multipliers, etc. These measures are relatively crude.

We are using as a measure of hardware complexity the area needed to fabricate the device in NMOS process. This measure has the advantage of reducing all filter implementations to the common building blocks that make up the filter.

Examples are presented comparing the use of distributed arithmetic (Peled-Liu) implementations and more conventional multiplier implementations of fixed point digital filters.

4. C.T. Mullis, R.A. Roberts, "Normal Realizations of IIR Digital Filters," Proceedings of the International Conference on Acoustics, Speech and Signal Processing, Washington, D.C., 1979.

Abstract: Normal realizations of IIR Filters possess many desirable properties including freedom from overflow oscillations, low roundoff noise for many pole-zero locations, low coefficient sensitivity, and invariance of form under frequency transformations of the filter. Given a state variable model $\{A, b, c, d\}$ of a filter, we define a normal structure as a filter whose A matrix satisfies $AA^T = A^T A$. This paper develops design equations and formulas for roundoff noise of normal forms in terms of the poles and zeros of the filter transfer function. Comparisons of normal forms and minimal noise forms are given in geometric terms and give one an intuitive understanding of these structures.

5. M. Arjmand, R.A. Roberts, "Reduced Multiplier Low Roundoff Noise Digital Filters," Proceedings of the International Conference on Acoustics, Speech and Signal Processing, Washington, D.C., 1979.

Abstract: Minimal roundoff noise digital filter structures require $(n+1)^2$ multiplies per output sample for n^{th} order filters. This can be reduced to approximately $4n$ multiplies if these optimal forms are broken into second-order sections which are then connected in parallel or cascade. This compares to $3n$ multiplies for the usual cascade or parallel connection of second-order direct forms. This paper presents new reduced multiplier structures which have slightly increased roundoff noise over optimal forms but can be orders of magnitude better (in roundoff noise) than direct forms for narrowband filters. Results are given for second-order sections with seven and eight multiplies per section. (Direct forms require 6 multiplies per second-order section vis-a-vis 9 multiplies per second order section for optimal forms). Design equations are presented for these reduced multiplier structures in terms of the poles and zeros of the desired transfer functions.

6. M. Arjmand, R.A. Roberts, "On Distributed Arithmetic Structures for Digital Filtering," Proceedings of the Thirteenth Asilomar Conference on Circuits, Systems and Computers, Monterey, California 1979.

Abstract: Distributed arithmetic structures are an alternative hardware realization to the use of conventional multipliers in the implementation of digital filters. This paper compares the possible methods of partitioning the equations of a second-order digital filter for a distributed arithmetic

realization. These realizations are also compared to a conventional multiplier structure of the filter. The comparisons are based on two figures of merit that measure the product of the speed and the complexity of a given implementation.

7. M. Arjmand, R.A. Roberts, "Realizations of Low Roundoff Noise Digital Filters," Proceedings of the International Conference on Automatic Control, Denver 1979.

Abstract: Minimal roundoff noise IIR digital filters require $(n+1)^2$ multiplies per output sample for an n th order filter. By optimizing second-order sections which are then paralleled or cascaded, one can reduce the number of multiplies to approximately $4n$. These realizations are termed sectional optimal. They are a compromise between the minimal noise forms and direct forms which require approximately $3n$ multiplies. We present here explicit design equations and noise performance equations for low roundoff noise realizations for sectional optimal forms and other closely related low noise forms. These latter realizations possess slightly greater noise than sectional optimal forms but have one or two less multipliers per second-order section.

8. W.L. Mills, C.T. Mullis, R.A. Roberts, "Digital Filter Realizations Without Overflow Oscillations," IEEE Transactions on Acoustics, Speech and Signal Processing, Vol. ASSP-26, No. 4, pp. 334-338, 1978.

Abstract: Most of the literature dealing with overflow oscillation in fixed-point arithmetic digital filters has considered the direct form exclusively. It is possible to eliminate overflow oscillations, regardless of pole locations, by considering more general forms. A sufficient condition is given for a two's complement state variable realization of any order to be free of overflow oscillation. A simple characterization of the condition is given for second order filters. Among those second order forms which meet the condition are normal forms, and forms which minimize output roundoff noise.

9. C.T. Mullis, R.A. Roberts, "On Weak Equivalence of Linear Systems and Finite State Systems," SIAM Journal on Mathematical Analysis, Vol. 10, No. 3, pp. 498-511, 1979.

Abstract: It is shown that finite state machines exist which are weakly equivalent to linear systems, for some nontrivial definitions of weak equivalence. Two systems, one linear with state space R^n , the other with a finite state space, operate on the same stationary uncorrelated input sequence u . The two systems have real valued output sequences y and \hat{y} . Notions of weak equivalence are formulated which involve sets of mixed second moments of the input and two outputs. "Power spectrum equivalence" requires that $E(y_t y_{t+\tau}) = E(\hat{y}_t \hat{y}_{t+\tau})$ for all τ . "Cross-correlation equivalence" requires that $E(u_t y_{t+\tau}) = E(u_t \hat{y}_{t+\tau})$ for all τ . The interdependence of these and other notions of weak equivalence are studied. The existence of weakly equivalent finite state systems is constructively demonstrated for a standard class of linear systems.

10. W.L. Mills, C.T. Mullis, R.A. Roberts, "Low Roundoff Noise and Normal Realizations of Fixed Point Digital Filters," to appear in IEEE Transactions on Acoustics, Speech and Signal Processing.

Abstract: Explicit design and performance equations are given in terms of the parameters of the desired transfer function $H(z)$ for two classes of realizations. These realizations offer the digital circuit designer an alternative to the usual designs based on direct forms. In addition to low roundoff noise, these new realizations offer other desirable properties such as low coefficient sensitivities, and freedom from overflow oscillations. Numerical results are presented which detail the design process and verify the theory.

9. Research Findings:

This research has been concerned with the problem of developing efficient digital hardware structures for signal processing. Our point-of-view is somewhat different from that adopted by designers of these devices that are working in the industrial sector. They have taken the point-of-view that hardware must be versatile. It must perform more than one signal processing task. Thus many functions of the hardware must be controlled by software programs tailored for the particular class of problems. This kind of versatility can only be obtained by an increase in hardware complexity and a reduction in the data throughput of the device.

We have chosen to optimize digital processing structures for each particular task the processor is asked to perform. This not only simplifies the complexity of the structure but also greatly increases the data throughput of the device. We have concentrated on two signal processing tasks, digital filtering and spectral estimation.

The first problem we had to solve was how to meaningfully compare hardware structures. Complexity measures used in the literature are based on various parameters such as chip count or pin count of the IC components. These measures are difficult to incorporate into a theory. We are using what we consider a more fundamental measure -- namely the area needed to fabricate a given hardware design in an nMOS process. This kind of area calculation quantifies each hardware design in terms of its most fundamental elements and thus appears to be a good measure of hardware complexity.

Hardware complexity is, of course, only part of the story. Data throughput is another basic parameter of any signal processing device. Thus as a figure of merit for comparing various hardware designs we have used:

$$\text{Figure of merit} = (\text{nMOS chip area}) \times \left(\frac{1}{\text{word rate}} \right)$$

We have used this figure of merit in developing our theory of efficient hardware structures.

There are essentially four parameters that appear to be the basis for understanding and quantifying competing hardware designs. These parameters are:

(a) Concurrency of computation. This concept includes all forms of parallelism and pipelining used to increase data throughput.

(b) Good output signal quality. In any digital hardware device, finite register effects will affect the output quality of the processor adversely. These effects can be alleviated by increasing the word length of the digital device. However, increasing word lengths increases hardware complexity and reduces data throughput. Thus it is very important to reduce word lengths to as small a value as possible. This implies one must understand what realization or signal flow graph of a given input-output characterization is the best in the sense of minimizing finite register effects.

(c) Modularity and regularity of design. This idea is difficult to quantify but intuitively it is easy to see why it is important. Modularity of design refers to a structure which is made up of identical modules with simple and regular connections between the modules. This type of structure offers the designer many advantages including:

- (1) a simple design process for the input-output specification;
- (2) a simple implementation process for the actual construction of the device;
- (3) a systematic procedure for verifying and checking the logic and interconnections of the device. This can be a very important aspect in the design of devices with a large number of elementary components such as occurs in VLSI.

(d) Hardware complexity. We measure this parameter by calculating the

equivalent chip area needed to fabricate the device in nMOS. In studying hardware complexity we have found that distributed arithmetic (see Abstract 3 on Efficient Hardware Implementations) often results in lower complexity than the use of monolithic multipliers. We have spoken with many other hardware designers and they have reached similar conclusions on the desirability of using distributed arithmetic when it is feasible to do so.

We have incorporated these ideas in the search for good designs for linear filtering and spectral estimation. We believe we have found an excellent structure for linear filtering. This structure's attributes are summarized in Abstract #2 on "A Modular Hardware Structure".

We have also considered certain structures for spectral estimation that as are yet unpublished. We believe we are close to some good structures for this task also.

We have, in the course of this research, developed some side results not precisely in the main thrust of the proposal which will also prove to be of value. These include:

(a) The development of two new algorithms for ARMA spectral estimation (see Abstract #1).

(b) The development of a multitier lattice structure for use in both linear filtering and spectral estimation.

(c) An investigation of "block processing" in linear filtering which can be used to improve performance. Block processing is an old idea in which one processes data in blocks rather than one sample at a time. The results are also produced in blocks. This seemingly simple idea can lead to some dramatic improvements in processing performance. This work has not yet been submitted for publication.