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GaAs MONOLITHIC MICROWAVE SUBSYSTEM TECHNOLOGY BASE

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During the period covered by this report, a number of decisions on GaAs material growth and processing, improvements in device design, and changes in device and circuit fabrication were made. In addition, all of the required processing fabrication and measurement equipment has become fully operational. The above, in turn, have resulted in:

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1. increased yields of FET devices,
2. more uniform DC and RF characteristics,
3. improved FET performance as demonstrated by substantially higher output power per unit of gate width and higher power added efficiency, and
4. a faster program pace as manifested by more device and monolithic circuit processing runs per unit time.

The benefits of the Melbourn Liquid Encapsulated Czochralski facility are becoming evident as large diameter, low impurity GaAs boules grown in pyrolitic boron nitride crucibles are available and being used in this program. Measurements of mobilities have shown values close to the theoretical limit for the case of a zero background impurity level, i.e.; a mobility of 5500 for $n = 5 \times 10^{16}$.

16 to the 16th power

FET performance has improved to the point where the last four runs have yielded power outputs consistently between 0.52 and 0.64 W/mm. Narrow band (10 percent) monolithic amplifiers have demonstrated power outputs of nearly 400 mW and a two-stage, 1-watt, 5-10 GHz monolithic amplifer has been designed.

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SUMMARY

During the period covered by this report, a number of decisions on GaAs material growth and processing, improvements in device design, and changes in device and circuit fabrication were made. In addition, all of the required processing fabrication and measurement equipment has become fully operational. The above, in turn, have resulted in:

- increased yields of FET devices
- more uniform DC and RF characteristics
- improved FET performance as demonstrated by substantially higher output power per unit of gate width and higher power added efficiency.
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The benefits of the Melbourn Liquid Encapsulated Czochralski facility are becoming evident as large diameter, low impurity GaAs boules grown in pyrolitic boron nitride crucibles are available and being used in this program. Measurements of mobilities have shown values close to the theoretical limit for the case of a zero background impurity level, i.e.; a mobility of 5500 for $n = 5 \times 10^{16}$.

FET performance has improved to the point where the last four runs have yielded power outputs consistently between 0.52 and 0.64 W/mm. Narrow band (10 percent) monolithic amplifiers have demonstrated power outputs of nearly 400 mW and a two-stage, 1-watt, 5-10 GHz monolithic amplifier has been designed.

1. INTRODUCTION AND MANAGEMENT SUMMARY

During the period covered by this report, a number of decisions on GaAs material growth and processing, improvements in device design, and changes in device and circuit fabrication were made. In addition, all of the required processing, fabrication, and measurement equipment has become fully operational. The above, in turn, have resulted in:

- increased yields of field effect transistors (FET) devices
- more uniform dc and RF characteristics
- improved FET performance as demonstrated by substantially higher output power per unit of gate width and higher power added efficiency
- a faster program pace as manifested by more device and monolithic circuit processing runs per unit time.

At the beginning of this reporting period, a decision was made to fabricate all FET's by direct ion implantation into unbuffered semi-insulating GaAs substrates. The motivation for that decision was the elimination of the costly step of buffer layer growth and the subsequent requalification of the GaAs wafer. In addition to the improved wafer yield and cost benefits, unbuffered wafers also facilitate the achievement of high Q interdigital capacitors.

The direct ion implantation decision was a difficult one in that, when the decision had to be made, the typical mobilities then obtained were 10 to 20 percent lower than those achieved by implantation into buffer layers. The lower mobility resulted in predictably lower g_m, lower gain, lower power output, and lower efficiency. It was anticipated that the installation of the Melbourn Liquid Encapsulated Czochralski (LEC) crystal growth facility (figure 1) would result in the availability of large wafers (figure 2) of uniform lower impurity GaAs. The LEC crystal growth facility is now operational and large diameter, low impurity GaAs

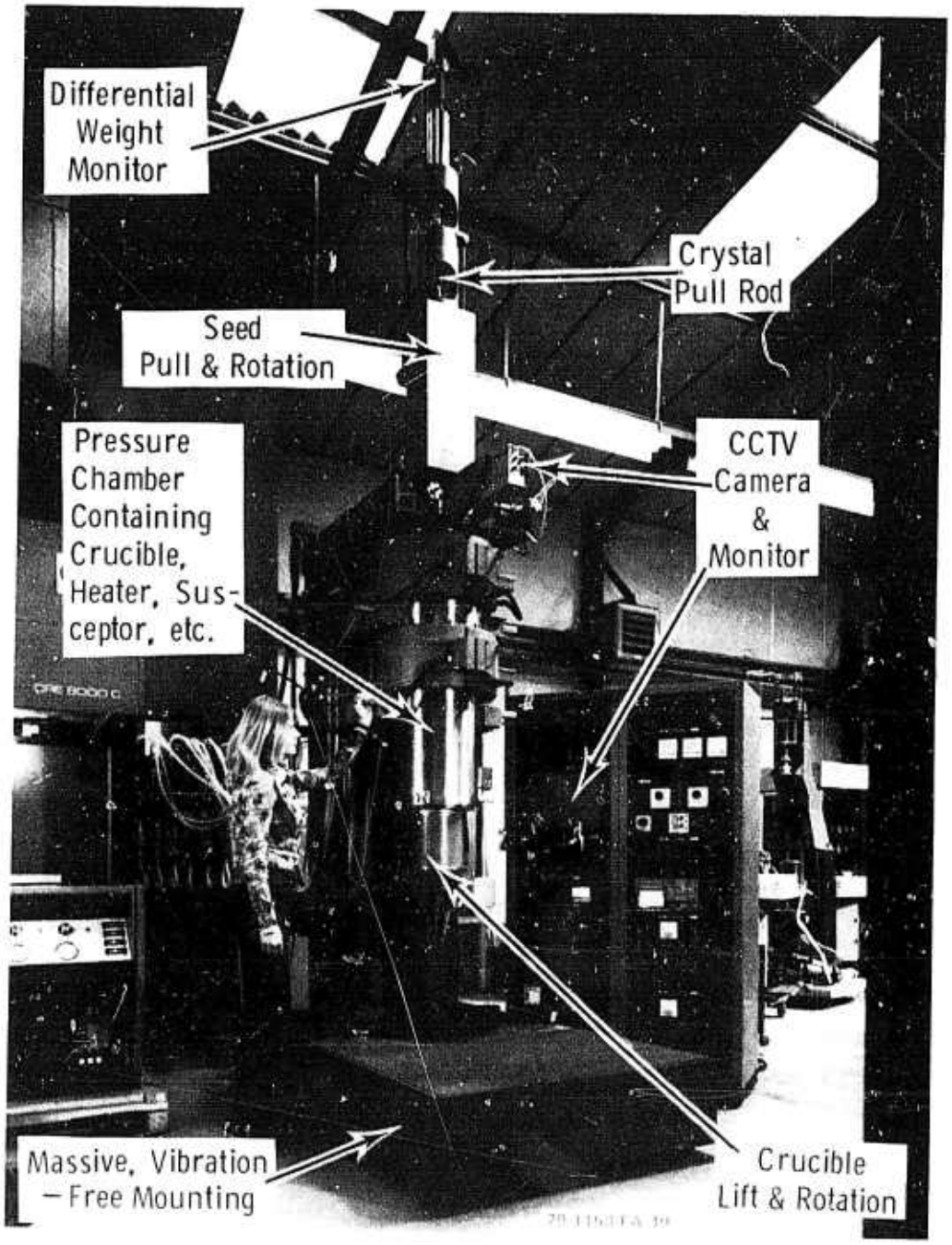

Figure 1. LEC Crystal Growth Facility

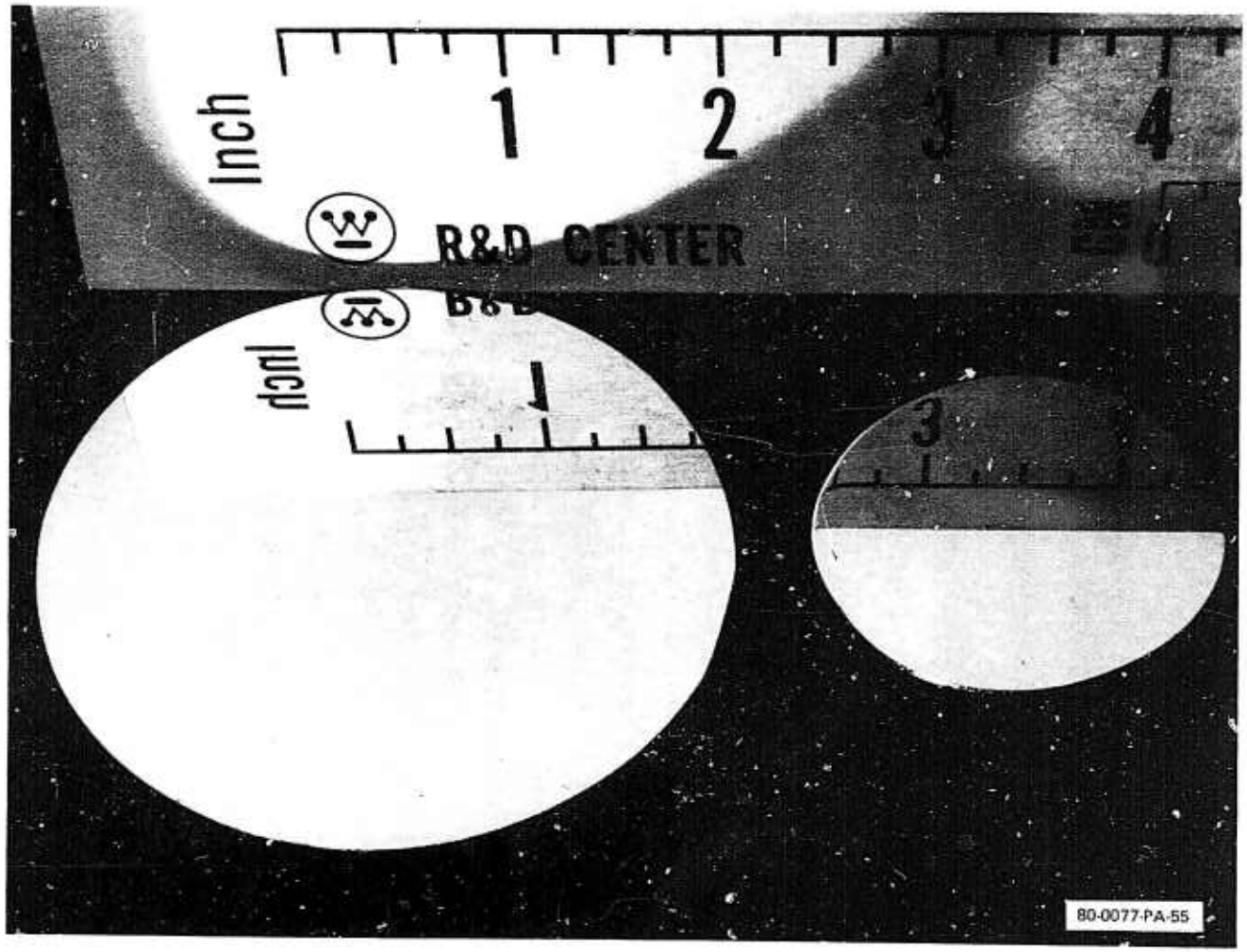

Figure 2. Two and Three-Inch GaAs Wafers From LEC-Grown Boules

boules grown in pyrolitic boron nitride crucibles are available and being used in this program. Measurements on this material have demonstrated that it has the lowest impurity content ever reported. Wafers of this material that have been capped, ion implanted, and annealed have been shown to have mobilities higher than previously achieved with buffer layers and close to the theoretical limit for the case of a zero background impurity level, i.e.; a mobility of 5500 for $n = 5 \times 10^{16}$ has been measured.

These uniform high mobility GaAs substrates are now available and being used for the fabrication of discrete FET's and monolithic circuits. Every step of the fabrication procedure from boule growth through RF testing of the completed device or circuit is now performed at Westinghouse. A photo of the LFE plasma nitride deposition system is shown in figure 3. This capping equipment had suffered from a number of defects and leaks which, after extensive rebuilding, have now been corrected. Uniform and satisfactory encapsulation of the ion-implanted wafers are now being achieved on most processing runs. The Varian/Extrion 400-kV ion implanter shown in figure 4 has been fully operational during this reporting period. Uniform and controlled profiles are consistently achieved when satisfactory capping has been achieved.

The excellent characteristics of the wafers prepared by direct implantation into unbuffered semi-insulating GaAs substrates has justified the earlier decision. If it had proven necessary, Westinghouse could have made use of its GaAs vapor phase epitaxy capability which is described in Appendix C. This vapor phase arsenic trichloride process is capable of large area, uniform growths with tightly controlled properties that can be varied.

A number of FET device geometry changes have been made. They include a recessed gate to provide gate control and more uniform g_m over the full gate-voltage range from pinch off through a fully conducting channel. The gate-to-drain spacing has been increased in order to inhibit the formation of Gunn domains and hence increase the breakdown voltage. In addition, the carrier concentration has been increased in order to increase the maximum channel current.

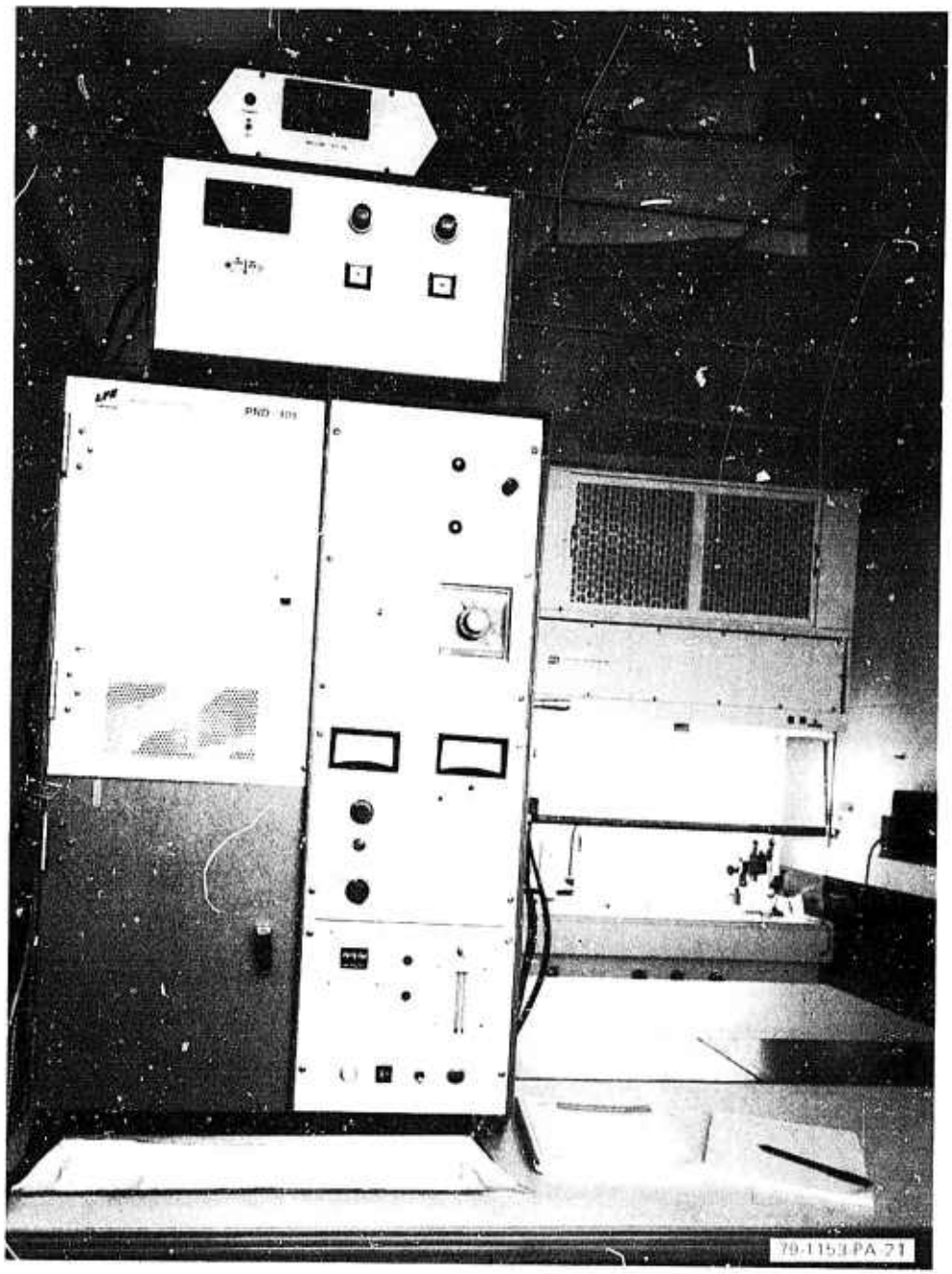

Figure 3. Plasma Nitride Deposition Equipment

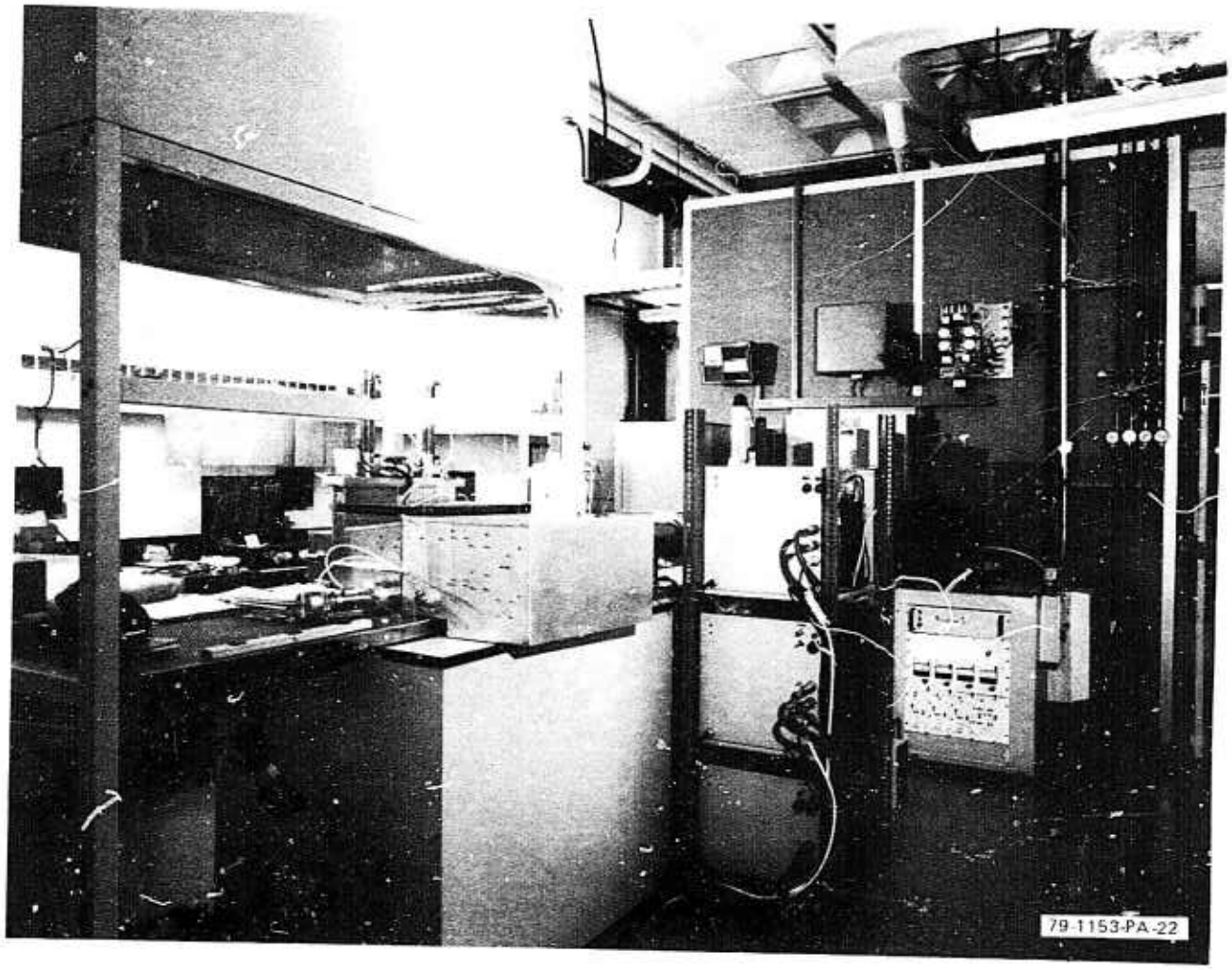

Figure 4. Varian/Extrion 400-kV Ion Implanter

The metallization system and processing procedures for the source and drain ohmic contacts have been changed. These changes have resulted in lower knee voltages and a higher channel current. The Schottky barrier gate metallization has also been changed to eliminate the use of chrome and its possible introduction of unknown quantities of chrome ions into the channel region under the gate.

All of these material and geometric and processing improvements are fully described in later sections of this report. They have resulted in substantial improvements of the yield, uniformity, and electrical performances of the FET's. The improved performance is illustrated by the chart of figure 5, showing the growth of power per unit of gate width achieved during the past 14 months (latest result -0.64W/mm). The last four runs illustrate both the higher power output and greater reproducibility which will result in improved monolithic amplifier yield and performance. The most recent run of single-stage monolithic amplifiers incorporating a 900-μm FET had an output power of nearly 400 mW. Allowing for output circuit losses, a power per unit gate width exceeding 0.5 W/mm was achieved. A two stage, 5-10 GHz monolithic amplifier, containing a 900 and a 2400-μm FET has been designed to have an output power of one watt.

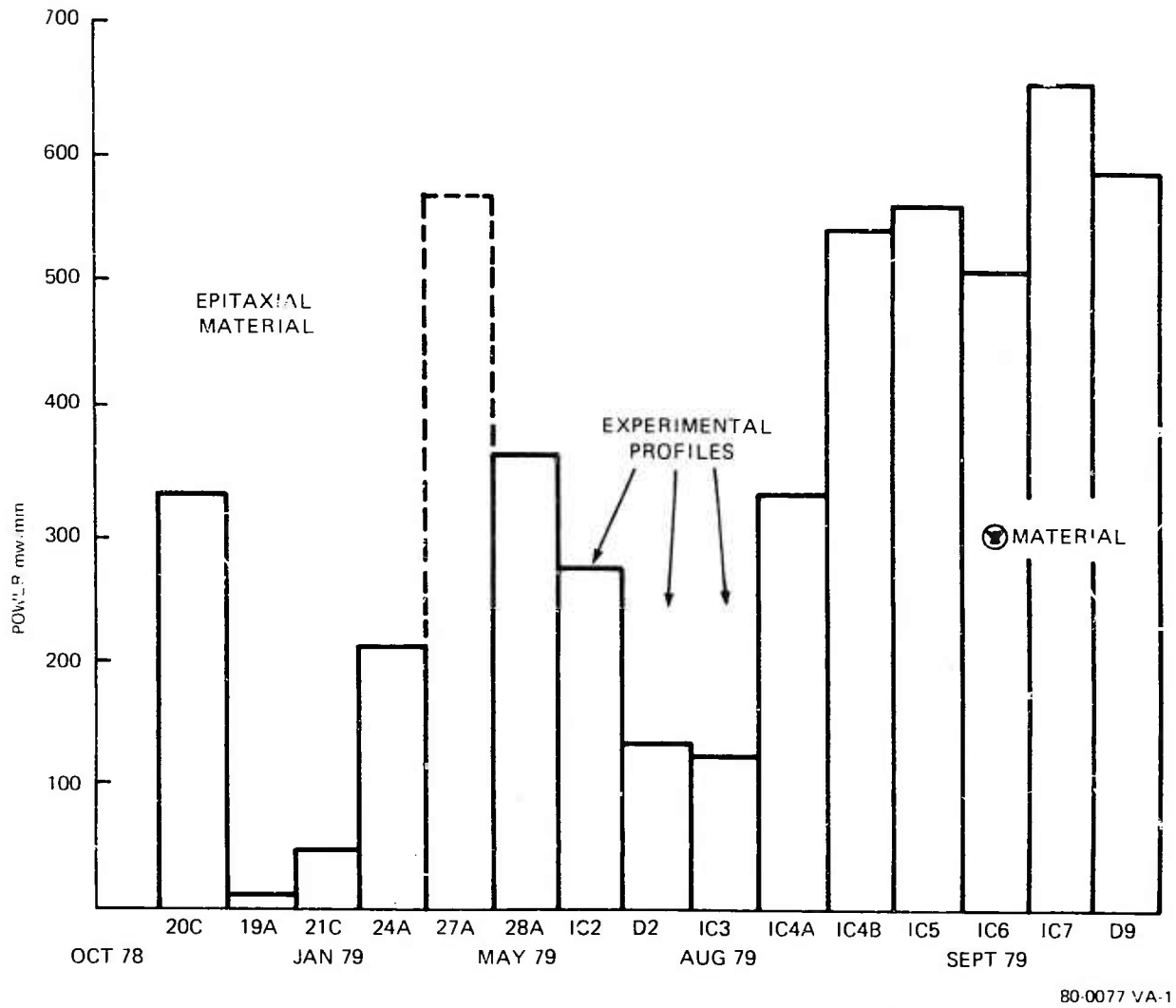

Figure 5. Power Output Per Unit Periphery for Westinghouse Ion-Implanted FET's

2. ION IMPLANTATION

All of the discrete device and integrated circuit objectives of this program depend upon a reliable source of wafers for fabrication. A consideration of the sponsor's ultimate cost and reliability objectives determined that selective, direct implantation into semi-insulating substrates would have to be the material preparation technique. In the course of Phase I, material preparation has progressed through:

1) Epitaxial layers
2) Buffer layer with uniform implants
3) Uniform direct implants
4) Selective direct implants
5) Multiple, selective direct implants

where stages 1 through 3 have now been terminated; the stage-4 technique is used routinely; and the stage-5 technique, which may be required for n^+ source-drain pads and/or on-chip phase shifter diodes, has been demonstrated but has not been incorporated in routine processing. Although ion implantation is critical to this program, it is a separate topic which is discussed in detail in Appendix E. A brief summary of the most significant aspects is discussed below.

The source of semi-insulating wafers for implantation has progressed from purchased, boat-grown GaAs-Cr ingots with their associated quality and delivery problems to 2 and 3-in. diameter, Cr-doped or undoped ingots. These ingots are grown, cut, and polished on site. The qualification process has been refined to eliminate unnecessary steps; other steps have become more elaborate since qualification is now directed more toward implantation to specification than rejection of unusable material. Plasma-enhanced deposition of Si_3N_4 from SiH_4 and N_2 has been established

as the encapsulation technology. The reproducibility of the refractive index ($n = 1.99 \pm 0.02$) and d, the thichness, (± 3 percent) is good; this is achieved on 2-in. diameter pieces and scale-up to 3-in. diameter appears to be feasible. Controlled Vapor Deposition (CVD)-grown phosphorus-silicon glass (PSG) was developed as a second level encapsulant. The PSG is employed in the photoresist, PSG, Si_3N_4 composite ion implantation mask for selective implants; the implants are performed through the Si_3N_4 and the patterns in the PSG are employed for registration.

The implantation technology development has been concentrated on the implantation of $^{29}Si^+$ for active channel layers. Silicon was initially chosen because Si implants can be activated effectively after ambient temperature implants in contrast to selenium, for example. In addition, Si can readily be implanted to the required depths, again in contrast to Se, and the Si profile integrity is good in contrast to sulfur. Ambient temperature implantation allows the use of photoresist in selective implantation and the use of high throughput, commercial ion implantation end stations. A Varian/Extrion 400-kV implanter with a 3-in. diameter cassette loading end station has been installed for this program. The 400-kV capability allows implantation of $^{29}Si^+$ through the Si_3N_4 to the depths required for power FET channels. Implantation through the Si_3N_4 improves reproducibility and does not affect encapsulant performance.

Si implantation at ambient temperature followed by $860^{\circ}/15$ min anneals using the encapsulant described above results in activation characterized by a linear relationship between implanted dose and activated center concentration with a threshold dose whose value depends on the deep level concentration in the starting material. The threshold is as low as $0.5 \times 10^{12}/cm^2$ in undoped GaAs and as high as $3 \times 10^{12}/cm^2$ in GaAs doped with chromium. Reproducibility of activation in boat-grown GaAs-Cr is poor, and this effort has been abandoned. Reproducibility of the active concentration/cm^2 in Westinghouse LEC GaAs-Cr is ± 5 percent

and the reproducibility in Westinghouse undoped LEC GaAs is better than ± 3 percent. The low field mobility in the Cr-doped material is 4100-4500 cm^2/volt-sec and 4740-4900 cm^2/volt-sec where both values are quoted at peak channel concentrations of 1.3-1.8 x $10^{17}/cm^3$. These values are believed to be state of the art.

$^{29}Si^+$ implantation into the undoped Westinghouse LEC material leads to gaussian profiles in good agreement with theoretical tabulations. Reproducibility of Capacitance Voltage (C-V) measured concentration profiles is better than two percent. Si^+ implantation into the companion Cr-doped material does not lead to gaussian profiles; the deep edge of these profiles is very abrupt. It is thought that the abruptness is related to the Cr concentration and Cr redistribution. This abruptness exhibits noticeable variation. It has not been decided whether this abruptness is sufficiently important to power FET performance to accept the resulting reductions in mobility and reproducibility, but the total process is under sufficient control to permit that determination.

The present processing yields a maximum concentration of 1.5 x $10^{18}/cm^3$ for Si implanted n^+ layers. Studies of the behavior of mobility with dose indicates that this maximum is determined by doping on both the Ga and As sublattices. An ambient temperature, selective coimplantation of Si and S has been developed to yield $\rho_s \leq 40\ \Omega/\square$ n^+ layers. This value is comparable to the present state of the art for thermal annealing and it is compatible with the existing selective channel technology.

3. DISCRETE FET'S

3.1 DESIGN

3.1.1 Introduction

The initial field effect transistors fabricated in this contract were self-aligned gate devices. The fabrication procedure of these devices required plating up of the source drain contacts to provide an overhang for the gate evaporation. This procedure places restraints on the subsequent fabrication procedure of the monolithic circuits and, hence, a more flexible "realigned" gate approach was instituted. The receipt of a Kasper 2001 HRZ Mask Aligner allowed Westinghouse, for the first time, to achieve 1μ line resolution with an ability to realign with submicron accuracy. An example of the results attained using this machine is shown in figure 6. A self-aligned gate device is also shown for comparison. Of particular interest is the small edge protrusion across the gate opening of the self-aligned device. Such defects seriously reduced the yield of this "high yield" process.

3.1.2 Device Dimensions

X-band operation requires that the gate length of the FET be 1μ and this, in its turn, means that the metallization (mainly gold) thickness must exceed 0.5μ in order that the gate resistance shall not be so high that it degrades the device performance. This relatively large thickness requirement places restrictions on the procedures that can be used to fabricate the gates as will be shown later.

The resistance appearing at the source end of the FET appears as a feedback element and, hence, affects the gain and the high-frequency operation of the device. In addition to the contact resistance between the metal and the semiconductor (which will be discussed later), the distance between the source and the gate

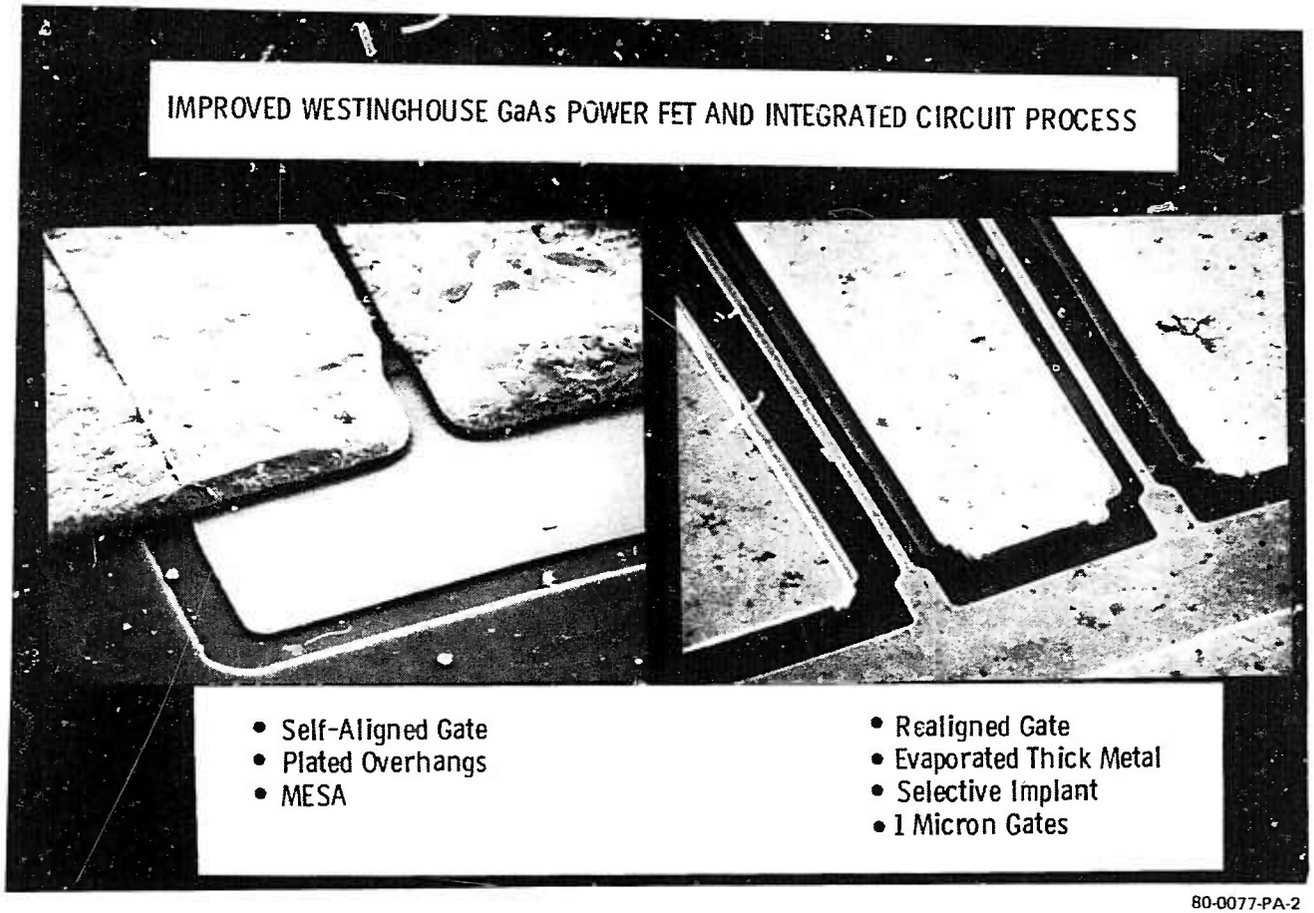

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Figure 6. Comparison of Self-Aligned and Realigned Gate Devices

of the device must be minimized to reduce the resistance due to the unmodulated portion of the semiconductor channel. We have chosen the value of 1 μ as being one consistent with the realignment capabilities of our fabrication technique.

The gate-to-drain spacing for this device needs to accommodate the formation of a static gunn domain that forms in the high field region adjacent to the gate and spreads towards the drain with increasing drain bias.[1] For the material we are using ($N_D = 1 - 1.5 \times 10^{17}/cm^3$), this distance must exceed 3 to 4 μ in order that the domain may not reach the drain metallization with a resultant castastrophic breakdown of the device.

In the case of the self-aligned gate devices, this gate-drain spacing was 1 to 2 μ and the devices were not able to operate at drain biases much above 10V without burning out. In the later devices, we are able to push the drain potential beyond 20V (maximum 35V) without destruction. This is illustrated in figure 7.

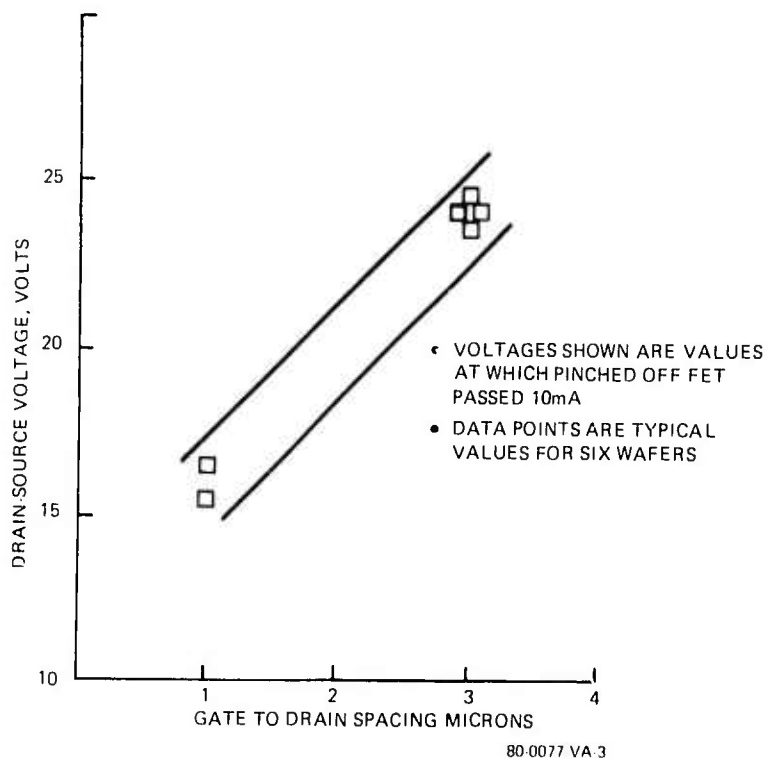


Figure 7. Improved Drain Voltage Capability Using Larger Gate-to-Drain Spacing

The voltage operation is limited, however, by gate leakage, which will be discussed later.

3.1.3 Gate Recess

Due to oxides forming charge states on the surface of gallium arsenide, the surface potential is 0.6 eV and of such a sign as to deplete the surface of electrons. For layers doped in the 1 to 1.5 x 10^{17}/cm range, the depth of depletion is 920Å to 750Å. The effect of this depletion can be appreciated by reference to figure 8.

In figure 8 (a) is shown a cross section of the FET with source, gate, and drain contracts. The depletion layer due to the surface potential and the gate at zero or slightly negative bias are also shown. The contact potential difference between the gate metal and the gallium arsenide is about 0.8 eV, resulting in a wider depletion layer at zero gate bias. This depletion layer is considerably reduced by the application of a positive bias as shown in figure 8(b). In device operation, the gate will be driven positively to 0.8V in order to derive the full channel current from the device. Note that in figure 8(b), the narrowest part of the channel does not appear under the gate and, hence, the gate has less ability to control the current.

In figures 8(c) and 8(d), the gate has been recessed to a depth equal to the surface depletion layer thickness. With this arrangement, the channel is always narrowest below the gate, even with positive bias, so the transconductance of the device is maintained.

3.1.4 Interconnection of Multiple Gate Devices

In the initial design of the FET's, the aim was to minimize the source inductance since that affects the device performance more seriously than the drain inductance. The device is shown in figure 9. The drains are wire bonded to the device header or the output stage of the amplifier circuit as shown in figure 9.

Later designs include the concept of the source "via" to connect the source of the device directly to the ground plane on the

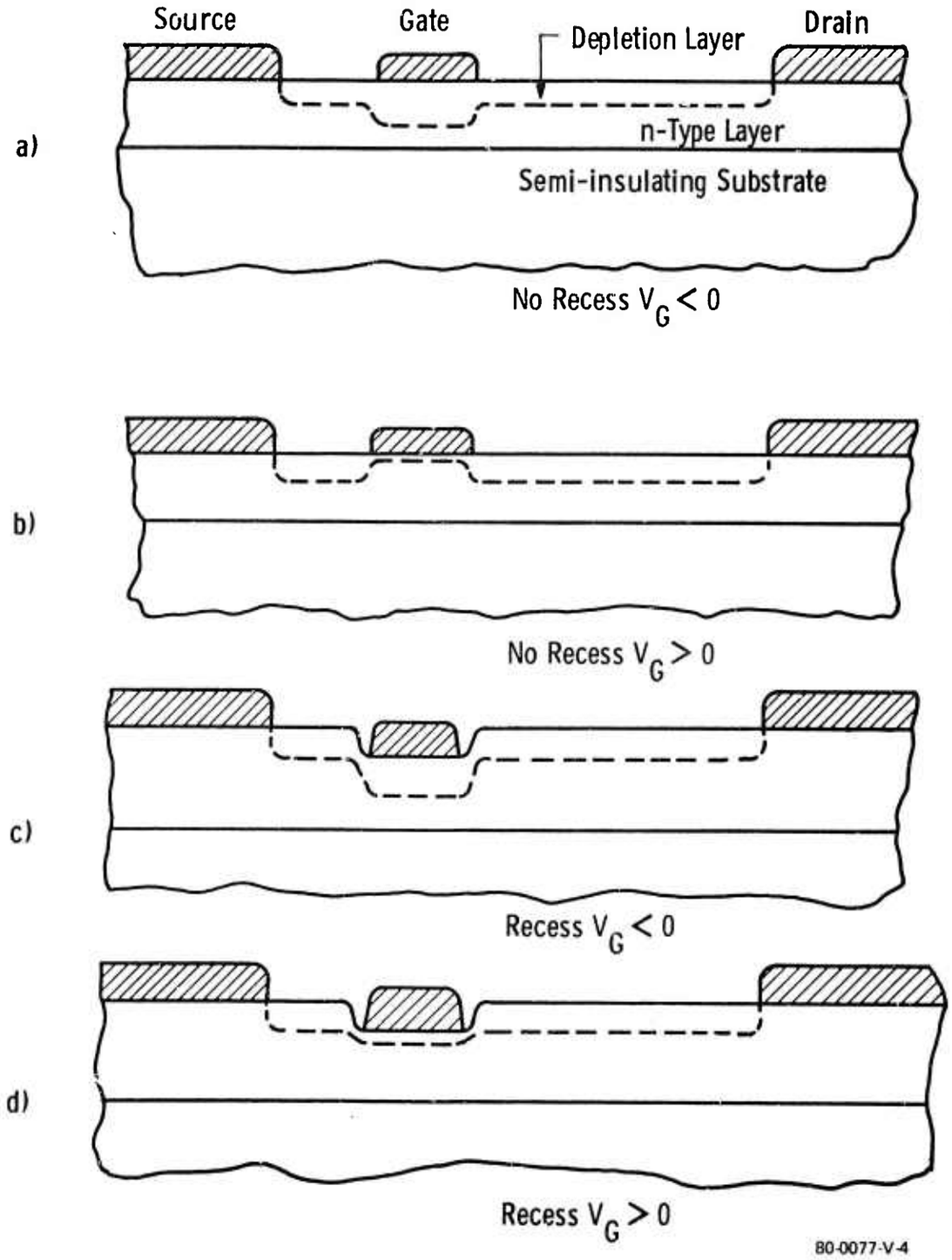


Figure 8. Effects of Gate Recess on Control of Drain Current

Figure 9. Sources Interconnected

back of the wafer through the substrate. A Scanning Electron Microscope (SEM) micrograph of the later design is shown in figure 10, albeit without the source "vias" present. The "vias" provide a low inductance connection to ground as well as a means of improving the heat sinking of the device.

3.1.5 Effect of Contact Resistance

We have calculated the contribution of the ohmic contact resistance in our power FET's to the total source resistance and to the knee voltage of the device. The equations used are from the analytic solution to the GaAs FET by M. Shur.[2] Essentially, the knee voltage consists of the voltage drop under the gate required to just form a domain between the gate and drain plus the voltage drop across all parasitic resistances between the source and drain. The parasitic resistances can be broken down into contact resistances at source and drain and the resistance of the GaAs active layer between source and gate and between gate and drain. The plan view of the device with dimensions is shown in figure 11.

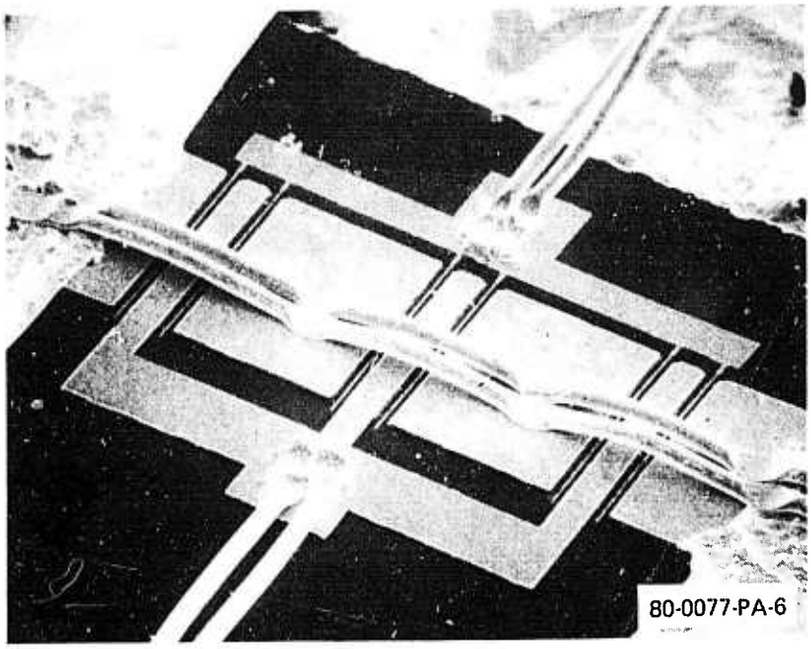
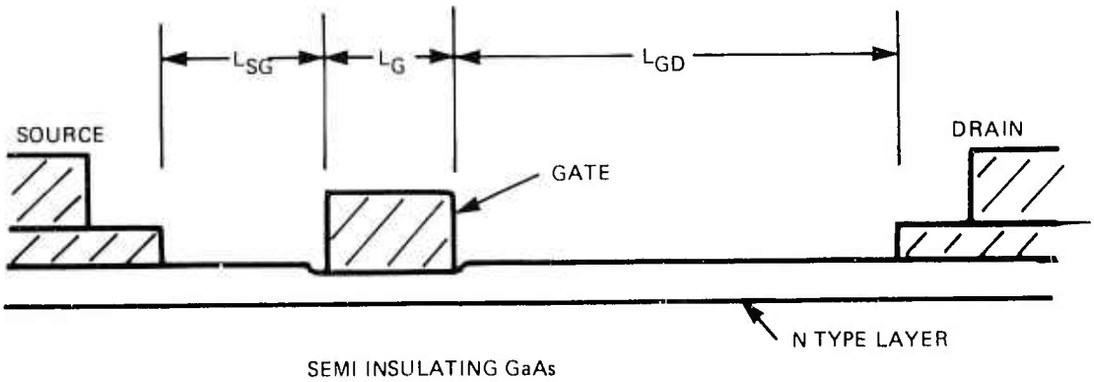


Figure 10. Drains Interconnected



L_{SG} = SOURCE TO GATE LENGTH = 1μm
L_G = GATE LENGTH = 1μm
L_{GD} = GATE TO DRAIN LENGTH = 3μm

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Figure 11. Plan View of GaAs Power FET for Calculation Purposes

The n-type active layer is assumed to be 700 ohms per square with a drift mobility of 3700 cm^2/v-s and a saturated drift velocity (or valley velocity) of 9×10^6 cm/sec. From the mobility and saturated velocity, we calculated the critical electric field required to form a domain as

$$E_{crit} = \frac{V_s}{\mu} = 2.4 \times 10^3 \text{ volts/cm.}$$

Next we calculate the resistance of the GaAs for a 1-mm periphery device (W) as

$$R_{sq} = \frac{700\Omega \times L_{sq}}{W} = 0.7\,\Omega$$

$$R_{GD} = \frac{700\,\Omega \times L_{GD}}{W} = 2.1\,\Omega$$

The voltage under the gate at saturation is

$$V_G = E_{crit} \times L_G = 0.24 \text{ volts.}$$

For a given specific contact resistance, R_C, we calculate the resistance at the source, R_{CS}, and drain, R_{CD}, using

$$R_{CS} = \frac{1}{W}\sqrt{700 \times R_C} = R_{CD}.$$

For example, with $R_C = 10^{-5}$ ohm-cm^2, we get $R_{CS} = R_{CD} = 0.84\,\Omega$.

If we take W = 1 mm and I_{DSS} of 0.30A/mm, we can now calculate the knee voltage

$$V_{KNEE} = V_G + I_{DSS}\,(R_{SG} + R_{GD} + R_{CS} + R_{DS})$$

and the source resistance

$$R_{SOURCE} = R_{SG} + R_{CS}.$$

The data for these calculations are shown in table 1 for the knee voltage as a function of contact resistance and in table 2 shows the dependence of the total source resistance on contact resistance.

The data of table 1 are plotted in figure 12.

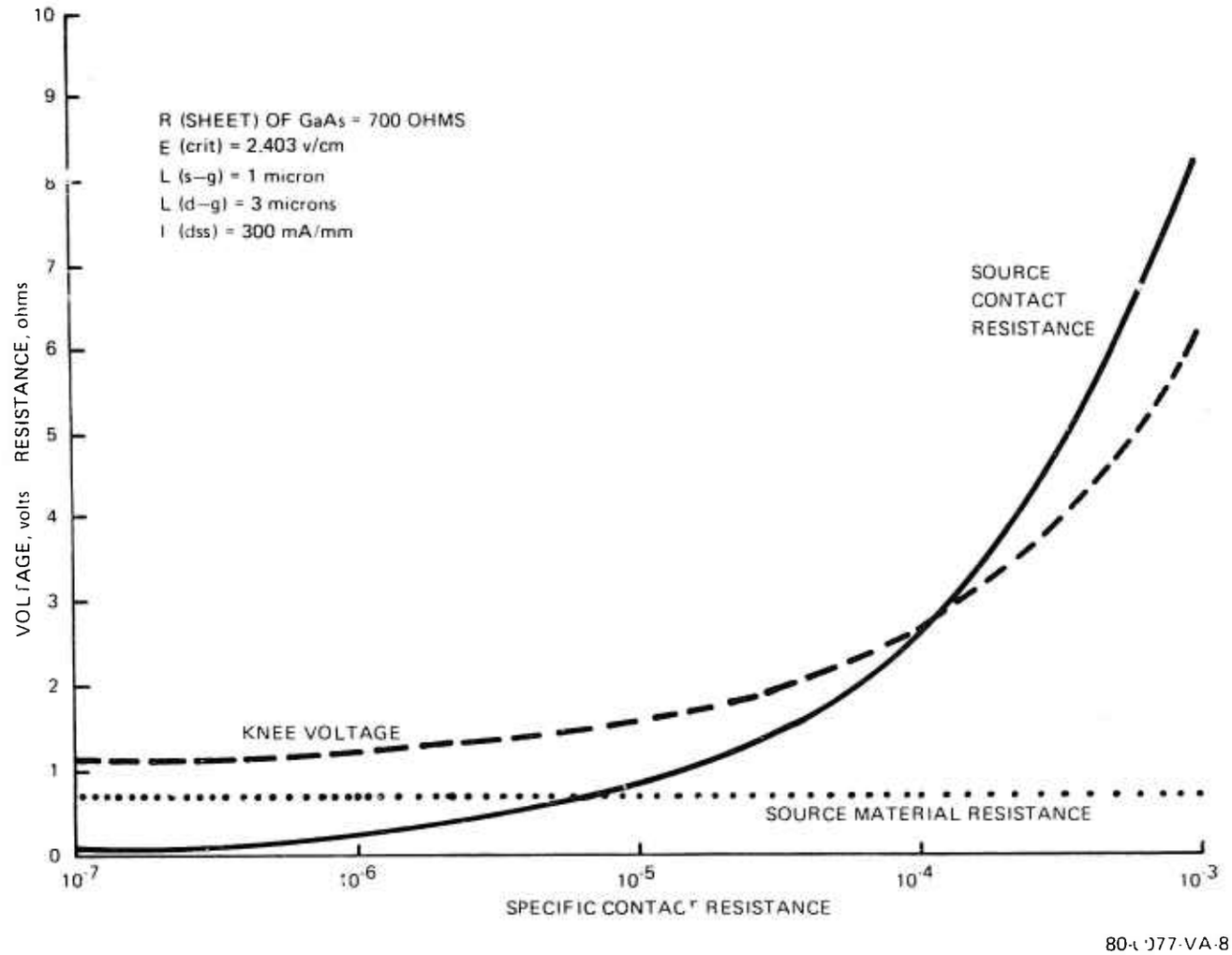


Figure 12. Effect of Specific Contact Resistance on Knee Voltage and Source Resistance of a Power FET

TABLE I

POWER FET KNEE VOLTAGE AS A FUNCTION OF CONTACT RESISTANCE FOR I_{DSS} = 0.30A/mm

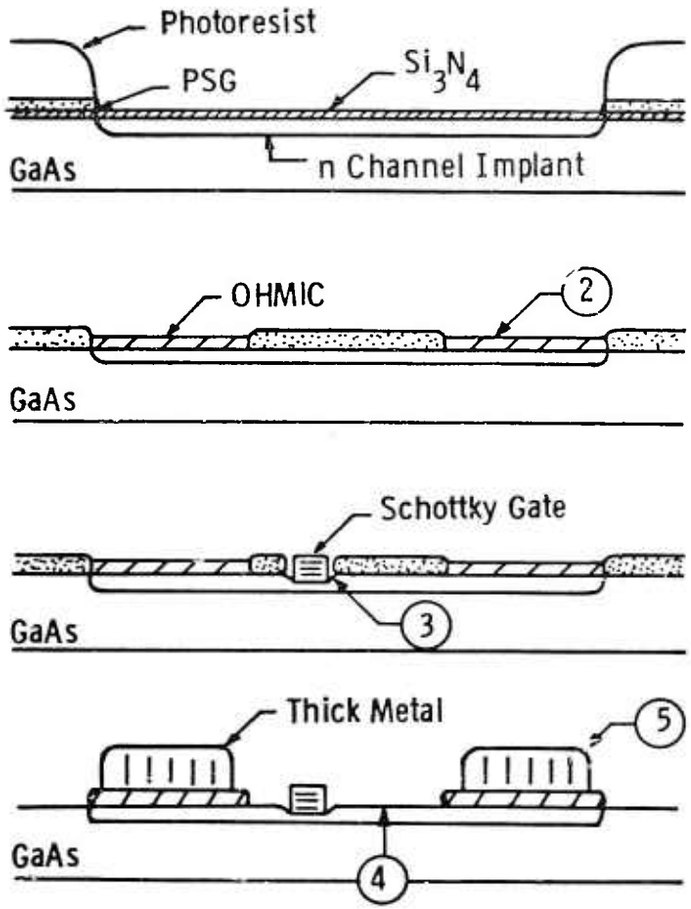
R_C (ohms-cm^2)	R_{CS} (ohms)	R_{CD} (ohms)	R_{SG} (ohms)	R_{DG} (ohms)	V_G (volts)	V_{KNEE} (volts)
10^{-3}	8.37	8.37	0.7	2.1	0.24	6.10
10^{-4}	2.65	2.65	0.7	2.1	0.24	2.67
10^{-5}	0.84	0.84	0.7	2.1	0.24	1.58
10^{-6}	0.26	0.26	0.7	2.1	0.24	1.24
10^{-7}	0.084	0.084	0.7	2.1	0.24	1.13

TABLE II

CONTRIBUTION OF CONTACT RESISTANCE TO TOTAL SOURCE RESISTANCE

R_C (ohm-cm^2)	R_{CS} (ohms)	R_{SG} (ohms)	R_{SOURCE} (ohms)	R_{CS}/R_{SOURCE} (percent)
10^{-3}	8.37	0.7	9.07	92
10^{-4}	2.65	0.7	3.35	79
10^{-5}	0.84	0.7	1.54	54
10^{-6}	0.26	0.7	0.96	27
10^{-7}	0.084	0.7	0.784	11

As a function of contact resistance, the knee voltage (dashed curve and left side vertical scale) drops below two volts from 3×10^{-5} ohm-cm^2 on down. Going from 10^{-5} to 10^{-7}, contact resistance improves V_{KNEE} by about a half volt. These values are lower than the observed knee voltage in our power FET's and the dependence on contact resistance at 10^{-5} ohm-cm^2 is greater. Also shown in figure 12 is the source contact resistance, R_{CS} by solid line and the source material resistance, R_{SG}, by the line with dots. Notice that, until the contract resistance is below 7×10^{-6} ohm-cm^2, over 50 percent of the source resistance



- Selective Ion Implantation
  - PSG + AZ1350J Implant Mask
  - Etch Alignment Marks in GaAs:Implant Si^+
  - CAP: PSG
  - Anneal: 860°C, 15 min.
- Ohmic Contact Formation
  - Deposit CVD SiO_2
  - Metallize
  - Dielectric Assisted Liftoff
  - Alloy
- Schottky Gate Definition
  - Align Gate Mask
  - Expose and Develop
  - Metallize
  - Dielectric Assisted Liftoff
- Thick Circuit + Ohmic Build-up
  - Strip SiO_2
  - Apply Photoresist & Expose
  - Soak in Chlorobenzene
  - Develop
  - Metallize
  - Liftoff

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Figure 13. Fabrication Sequence for a Direct Ion Implanted GaAs Monolithic Amplifiers and Discrete FET's

is caused by the ohmic contacts. At 10^{-6} ohm-cm^2, the contacts still contribute 27 percent of the total. These calculations argue the importance of getting the lowest possible contact resistance on power FET devices. We should point out that in small signal FET's with higher sheet resistivity active layers, R_{SG} rises in proportion to the resitivity while R_{CS} rises by the square root. Thus, the contribution of the contacts is a small fraction of the total source resistance although still quite important for low noise performance.

3.2 FET FABRICATION

3.2.1 Fabrication Sequence

The sequence of operations in the fabrication of the discrete FET's and the monolithic circuits is shown in figure 13. Selective ion implantation is made using "masks" of AZ1350J photoresist and phosphorus-doped SiO_2 (ion milled and chemically eteched using the same photoresist) through a 1000°A-thick layer of Si_3N_4. Implants have also been made into the "bare" gallium arsenide surface in which case the Si_3N_4 is added later.

The capping layer is an additional 2000°A-thick deposition of phosphorus silicon glass and the anneal cycle is 860°C for 15 min following the ramping sequence described in the ion implantation sections of this report.

The initial fabrication methods for these devices used a layer of low-temperature CVD SiO_2 (silox) to act as a spacing layer in the fabrication of the gate and in the deposition of the thick metal for the source and drain contacts and the metallization of the circuit for the amplifier. This can be seen in figure 13.

The ohmic contacts are deposited using the dielectric-assisted lift-off and are aligned to the implanted regions of the wafer using alignment marks ion milled into the surface of the gallium arsenide at the edge of the wafer. The various contact metallizations are described in more detail in Appendix B, but the present scheme is a triple-layer structure of gold-germanium (1100 Å), nickel (500 Å), and platinum (400 Å). After definition

of the metal, the contact is formed by alloying at 490°C in an atmosphere of nitrogen with 10 percent hydrogen. The gate is formed next in the sequence. After the photoresist is defined, the SiO_2 layer is chemically etched and then the gallium arsenide is eteched to form the gate recess. Without removing the photoresist, the gate metals, consisting of 500 Å titanium, 500 Å platium, and 4500 Å of gold are evaporated.

The final step in the fabrication process is the thick metal for the source and drain contacts for discrete devices and the addition of the passive elements for the circuits. This was also accomplished using dielectric-assisted liftoff. The metal system used in the buildup is chromium (800 Å), palladium (1000 Å), and gold (11,000 Å) to form a total metal thickness of just over a micron.

3.2.2 Use of Chlorobenzene

The dielectric-assisted lift-off was quite satisfactory for the discrete devices, although it meant leaving the oxide in place since the etch used to remove the oxide (Buffered HF) attacks the titanium of the gate and destroys the devices. A problem arose, however, in the fabrication of the monolithic circuits since it was necessary to overlap the thick metal forming the passive elements with the thin metal forming the ohmic contacts of the sources and drains of the FET's. Since the oxide had already been removed in these areas, it was not possible to reliably define the overlap. Accordingly, an alternative system was sought.

When photoresist is soaked in chlorobenzene after exposure, but before development, the surface becomes hardened and an overhang forms in the manner shown in figure 14. Figure 15 shows the thick metal on the source and drain contacts produced by this chlorobenzene process. The write feathered edges are due to distortion of the overhand during the evaporation of the platinum layer which requires great heat. This problem will be relieved by improved heat sinking of the wafer during evaporation.

Since removal of the oxide for circuit fabrication affects the gates, it was decided not to use the oxide at any stage during

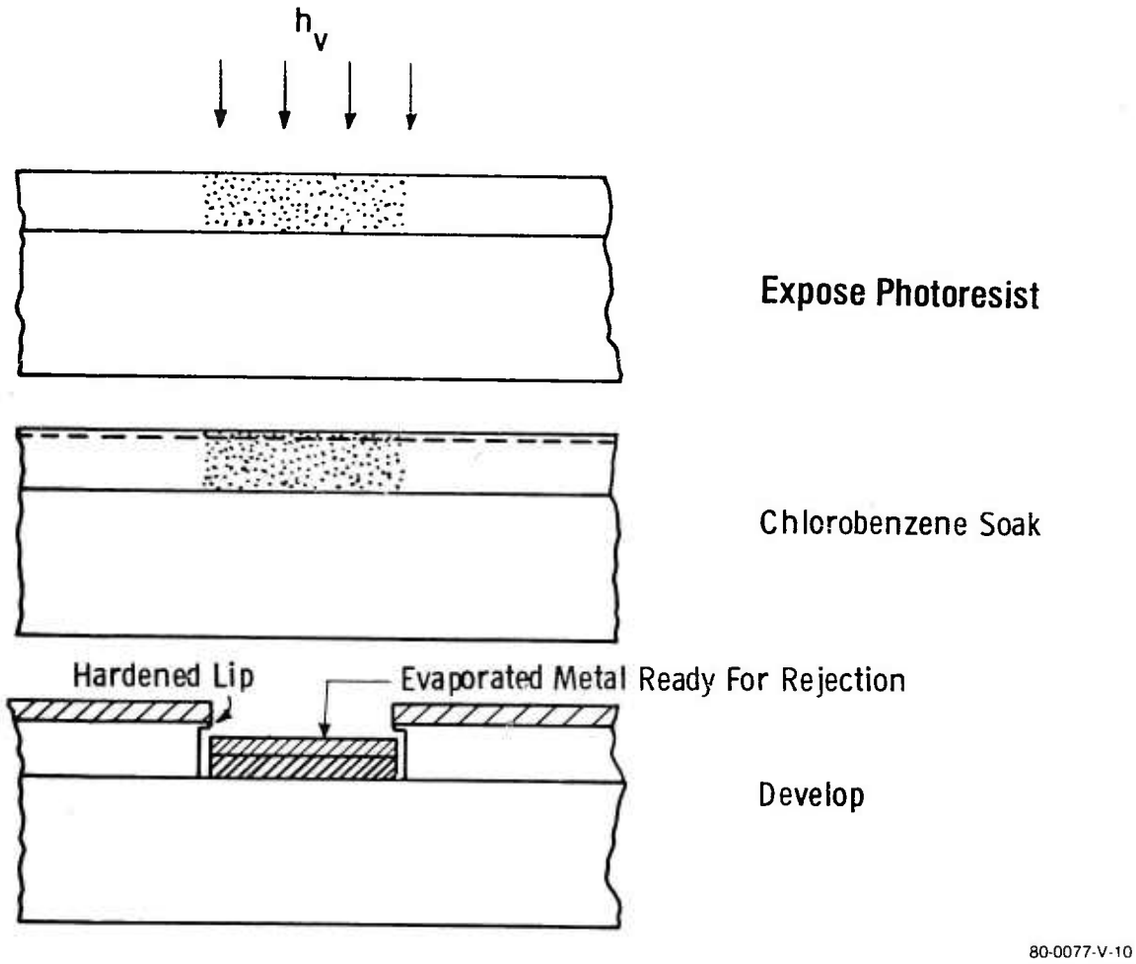

Figure 14. Schematic Diagram of the Chlorobenzene Photoresist Process

Figure 15. FET Fabricated Using the Chlorobenzene Process

the fabrication. Examples of 1μ gate openings made by the chlorobenzene process are shown in figure 16 (a) and (b). The gate shown in figure 15 was made in this way.

3.2.3 Ohmic Contacts

A full discussion of the ohmic contact formation is given in Appendix B. Briefly, the metallization scheme presently being used is gold-germanium alloy (11,00 Å), nickel (500 Å) and platinum (400 Å). This system has produced reproducible contacts whose contact resistance is 3×10^{-6} Ω-cm^2. The contacts are alloyed in a carbon boat at a temperature of 500°C in a 90 percent nitrogen, 10 percent hydrogen atmosphere flowing through a quartz tube.

An improved ohmic metallization scheme consisting of AuGe (450 Å), Ni (75 Å), Au (1100 Å), titanium-tungsten alloy (1200 Å) and Au has been investigated (see figure B-1 in Appendix B). This gave contact resistance values $< 10^{-6}$ Ω-cm^2, but has not yet been implemented into our device fabrication because the Ti-W layer must be RF sputtered onto the surface and this causes problems with our present fabrication procedure.

3.2.4 Gate Metallization

The present metallization scheme for the gates of the FET is titanium-platium-gold (500 Å - 500 Å - 4500 Å). This system is preferred over the previously employed chromium-palladium-gold gates from the point of view of reliability. Chromium is known to produce semi insulating gallium arsenide and recent work has shown that it diffuses quite freely, even at room temperature.

3.3 FET CHARACTERIZATION

3.3.1 dc Results

A typical characteristic taken on a Tektronix Curve Tracer is shown in figure 17. The point at which the drain current starts to increase, when the device is pinched off, is the point at which significant gate current starts to flow. This value ranges from 10 to 14 volts in our devices and this relatively low value, compared with other workers, is believed to be the main cause of the output power limitations of our transistors.

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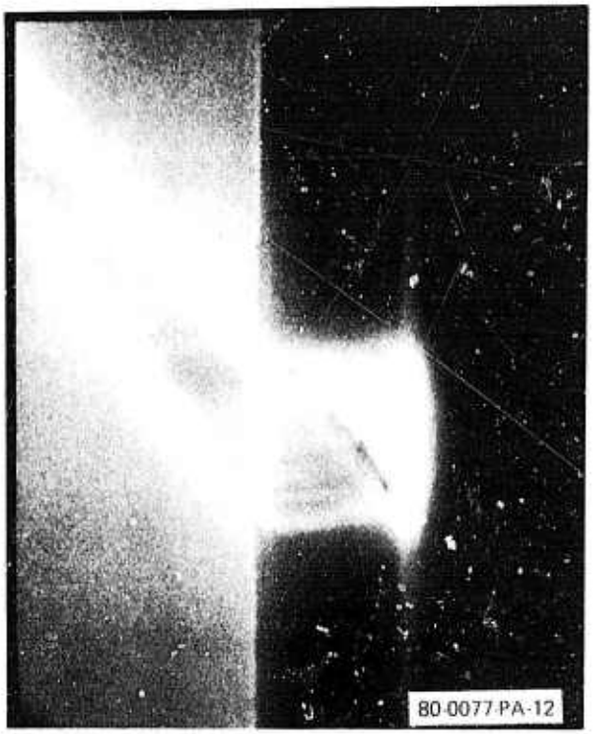

Figure 16a. 1-Micron Gate Opening in Photoresist

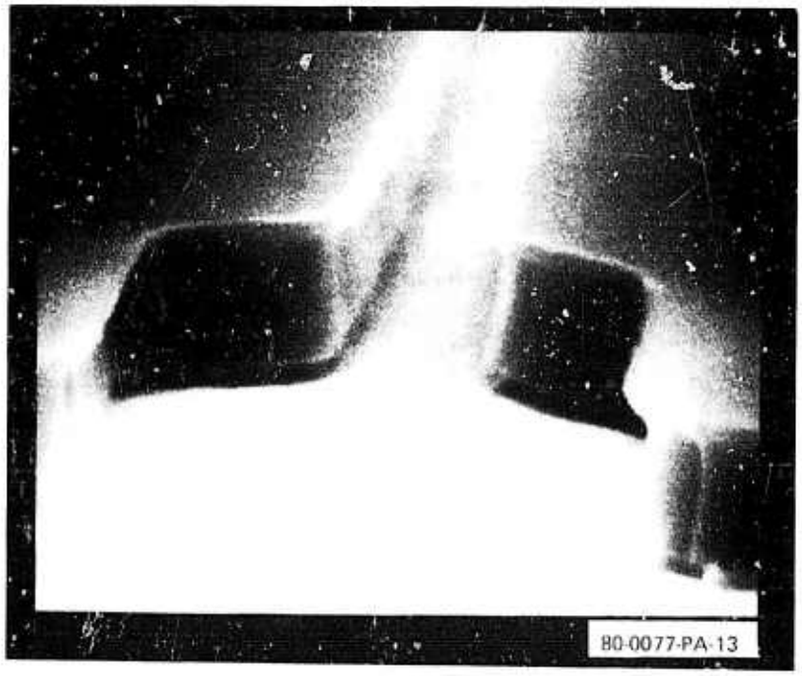

Figure 16b. 1 - Micron Gate Opening in Photoresist

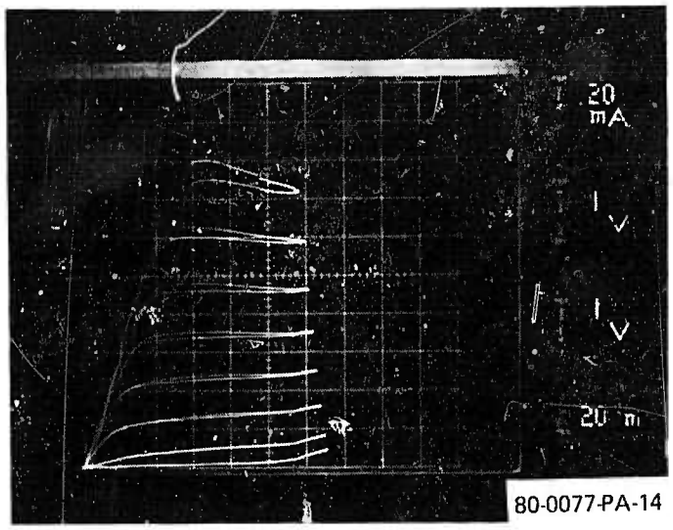

Figure 17. I - V Characteristics of 300 M Single Drain From Run D9E. Upper Trace is for Vg = +0.8 Volts

In table 3, the measured dc and RF parameters from a number of runs are compared. The most significant point in this table is the higher transconductance (and small-signal RF gain) that is obtained with the undoped runs. The lower breakdown voltage of the later D9E run is attributed to photoresist problems in depositing the gate (the edges are ragged) and not to any basic problem with the starting material.

3.3.2 Breakdown Voltage

The major factor limiting the power output of our device is the limitation on the gate-to-drain voltage that can be tolerated before the Schottky barrier gate draws appreciable current. Figure 18 shows the reverse gate-to-drain characteristics of a 900 μM, three-drain device from Run No. D9D. The characteristics are very soft and appreciable current begins to flow when the bias reaches 12 volts. The fact that current is flowing in the gate circuit limits the reverse voltage swing of the device to 12 volts. The forward voltage swing is limited to 0.8 volts,

TABLE 3

FET CHARACTERISTICS

RUN	28A	IC3E	IC48	I6C1	IC78	D9E
Material No.	CS4107	MR123	CS4107	WA4M	WA18M	W8N3
Type	Cr-doped	Cr-doped	Cr-doped	Cr-dpped	Undoped SiO_2 crucible	Undoped PBN crucible
V_{SAT}	1.8-2.2	2-2.5	2-2.5	1.8-2	1.8-2	2
V_{PO}	5-7	4-8	4-6	4-6	4-7	4-5
gm (300 μm) mzs	20-25	16-20	26	25	28	28
V_{BD}	20-25	20-28	>20	>20	>20	13
Small-signal (dB) gain at 8 GHz	6	7	7	7	11.5	10.2
Power out for 900μ at 4 dB gain (dBm)	24.6	21.0	26.6	26	27.2 (6 dB)	27.87
P_{OUT} (mW) avg over sev samples	288	100	457	398	524	572
Power-added efficienty	17%	10-12%	15%	18%	23%	19.25 Best 24%
Best value of mW/min					640	585
Best value of gain at 8 GHz						11.69

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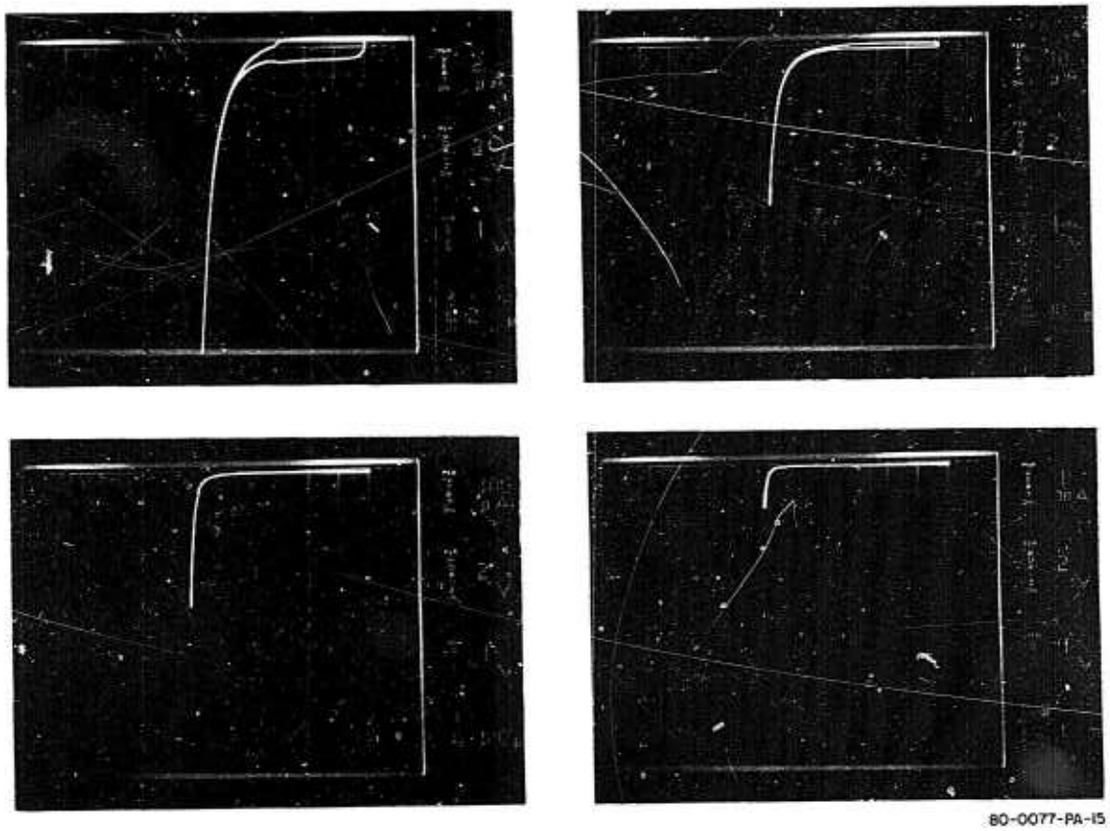

Figure 18. Gate-to-Drain Breakdown Characteristics for Derive No. D9D-7

at which point the Schottky diode of the gate is forward biased. Hence, the total voltage excursion possible on the gate with respect to the drain, in this case, is approximately 12.8 volts.

The problem is related to discrete breakdown points in the gate recess of the device shown by the appearance of white light in figure 19. The local appearance of the light suggests that it is not the basic geometry that is at fault, but rather small perturbations due to nonumiformities of gate metallization or gate recess etching.

In one particular instance, the onset of light output has been traced to a specific defect in the device fabrication. Figure 20 shows a device (No. IC6D-5) emitting light under gate-drain bias at two discrete points, only. Figures 21(a) and (b) are scanning electron micrographs of the same area from where the light is emitted. In this particular device, the gate metallization is offset in the gate recess (see figure 21(a)) allowing the gate metal to touch the side of the recess. Two points are clearly visible in figure 21(b) where the gate metal has "interacted" with the GaAs.

This interaction was thought to have occurred because of the heavy gold layer in the gate metallization and because gold is known to readily interact with GaAs. Accordingly, an experiment was performed where the gate was fabricated entirely of titanium without either the platinum or the gold overlayers. There is some improvement in the gate-breakdown voltage but the change is not significant.

There is a deterioration of the reverse characteristic as a function of time when drawing large (10μA/300μM) reverse currents. Experiments are presently in progress to investigate this phenomenon.

Light output occurs when the device is operating in the RF power mode. Figure 22 shows light emitted from a 900-μM periphery (three drain) device when delivering 366 mW of output power at 6 volts drain bias and 173 mA of drain current. This point is on the portion of the gain vs power output curve of this device

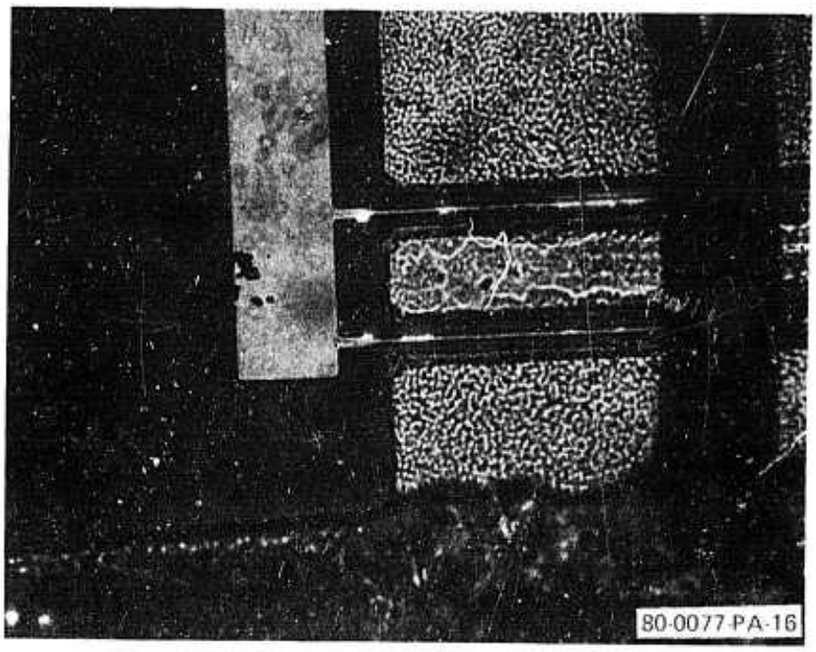

Figure 19. Light Output from Device No. D9D-7 Under Gate Drain Reverse Bias with the Source Floating

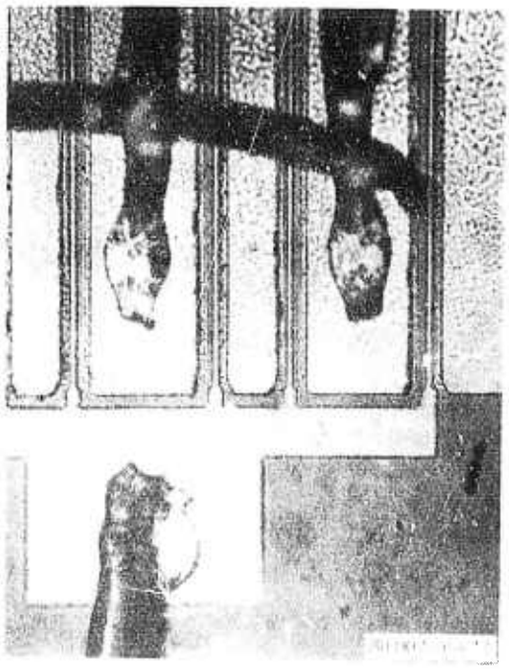

Figure 20. Light Emission From Device No. IC6 D-5 Under Gate-to-Drain Bias

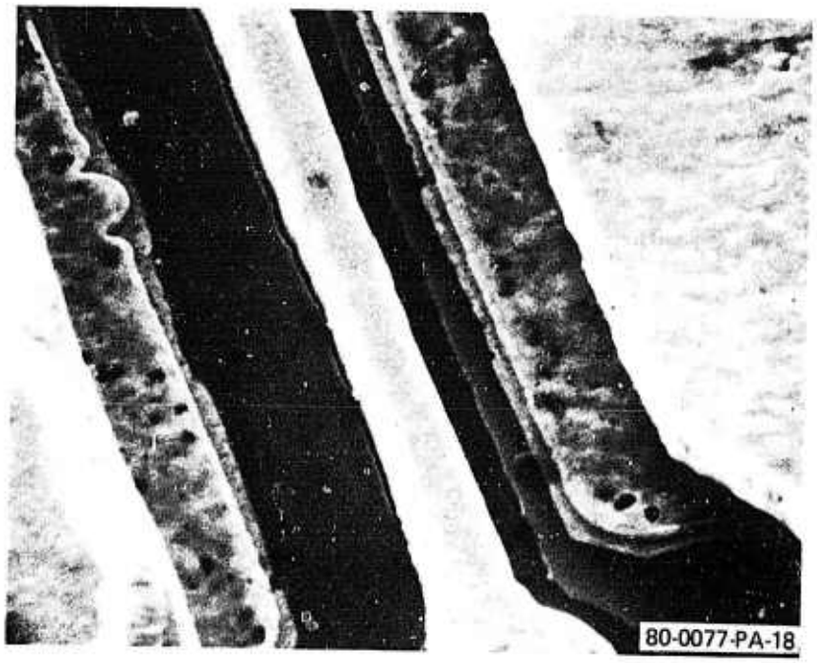

Figure 21(a). Scanning Electron Micrographs of Device No. IC6D-5 Showing Points at Which Light Is Emitted

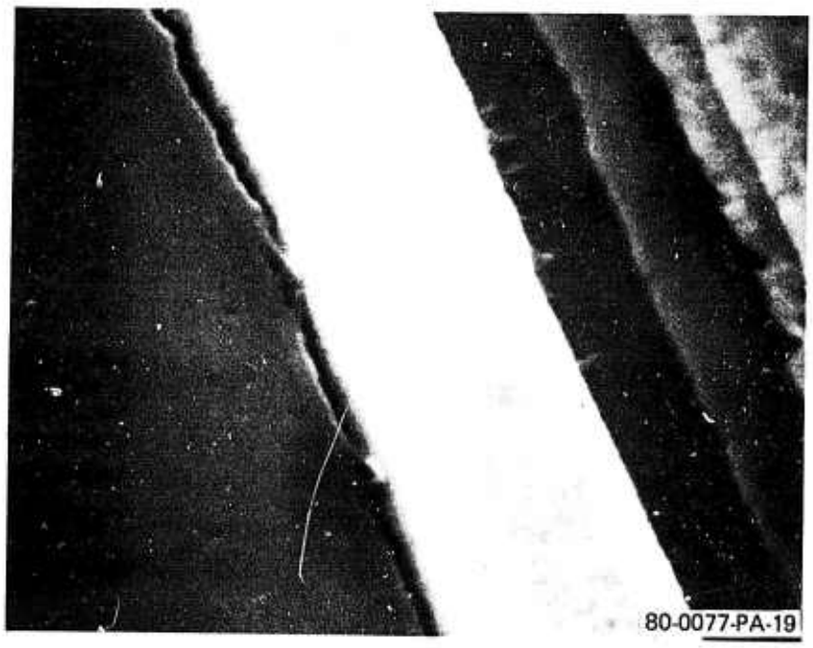

Figure 21(b) Scanning Electron Micrograph Enlargement

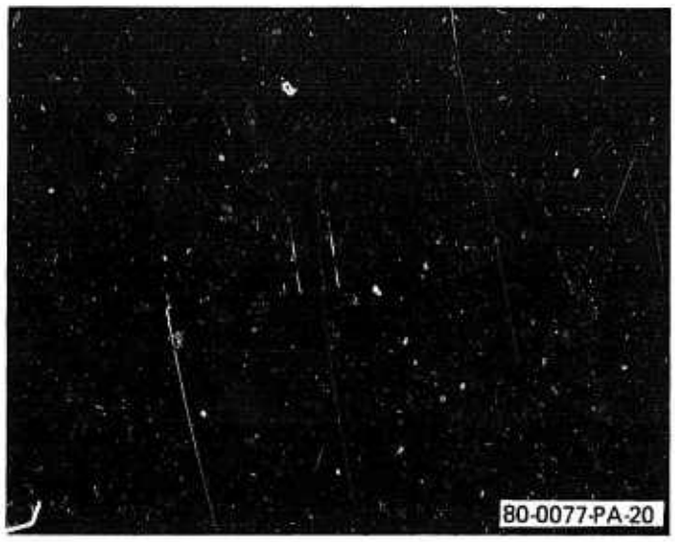

Figure 22. Light Emitted from Device No. IC7B-17 Delivering 25.64 dBm (366 mW) Output Power with V_D = 6.0 Volts, V_G = 1.4 Volts, ID = 173 mA and 5.03 dB RF Gain

where saturation of the gain is beginning to occur. If the light is caused by the same mechanism of gate breakdown as in the dc case it indicates that the same mechanism is responsible for the power saturation.

3.3.3 RF Performance

During the 12 months from October 1978 to September 1979, Westinghouse has made significant advances in the performance of their power GaAs FET utilizing direct ion implantation of the active layer in the substrate. In October 1978, the first run of realigned gate FET's (Run No. 20C) showed improved small-signal gain (6-8 dB at 8 GHz) and better output power per unit periphery (0.3 W/mm) than had been obtained from any previous self-aligned gate devices. Continuing improvements to the implant profile, carrier mobility, and device design, coupled with the recent introduction of undoped GaAs substrates grown at Westinghouse, have produced significantly better results. The small-signal gain is now 10-12 dB at 8 GHz and output powers over 1 watt

have been obtained. The best power per unit periphery is now 0.64 W/mm and the best power-added efficiency is 33 percent with typical devices producing 20 to 28 percent efficiency.

Both the small-signal tests and the power tests of our FET's have been automated using a desktop computer. We now have a storage system for our test data with 259 (146 different devices) small signal and 241 (51 different devices) power tests on file. This allows rapid comparison of device characteristics from run to run.

In this report section, we will cover our test methods and results. First is a description of our FET test fixture and the RF equipment used in the gain and power tests. Next we discuss the small-signal gain of the GaAs Fet's. This is followed by a model for the FET based on the small-signal data which is used for identification of problem areas. Finally, the power results and efficiencies obtained to date will be summarized.

3.3.3.1 Microwave Test Methods

The FET chips are soldered and wire bonded into a Au-plated copper header which is used for the small-signal and large-signal microwave tests. A photograph of the header and the assembly used to hold it is shown in figure 23. The header is 0.300 x 0.350 x 0.125 inches thick. It has a 0.025-in. high central ridge on which the FET chip is mounted and two microstrip 50-Ω lines to which the gate and drain are bonded. The microstrip is formed on 0.025-in. thick alumina pieces 0.110 in. long by 0.250 in. wide. Coupling to these microstrip lines is accomplished using Alford-type 9075-57 APC-7 to microstrip launchers sitting directly on the device header. A large water-cooled copper block is used to hold the header and two launchers together. The microwave properties of the header and launchers are illustrated by the reflection coefficient and loss curves plotted versus frequency from 2 to 12 GHz in figure 24. The upper curve shows the reflection coefficient looking at a header in which a gold ribbon has replaced the FET as a short at the end of the microstrip line. The reflection coefficient is better than 0.96 up to 12 GHz.

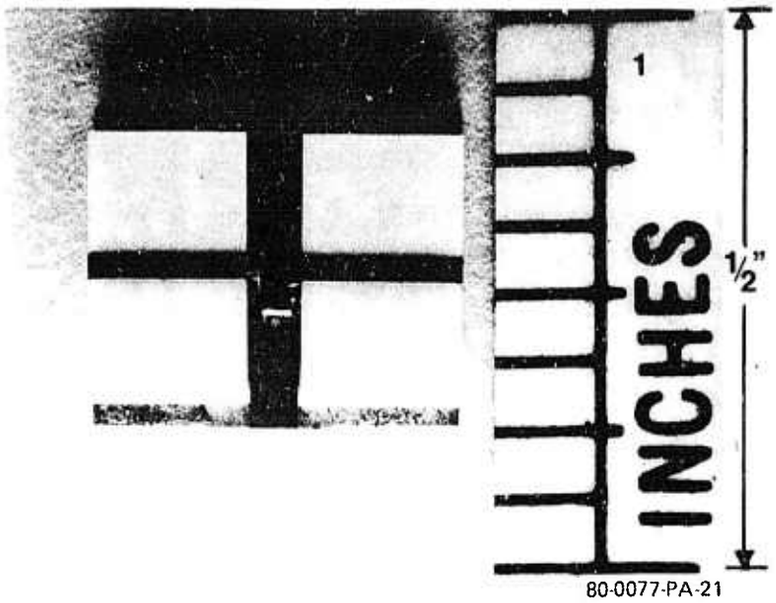

Figure 23(a) FET Mounted in Device Header

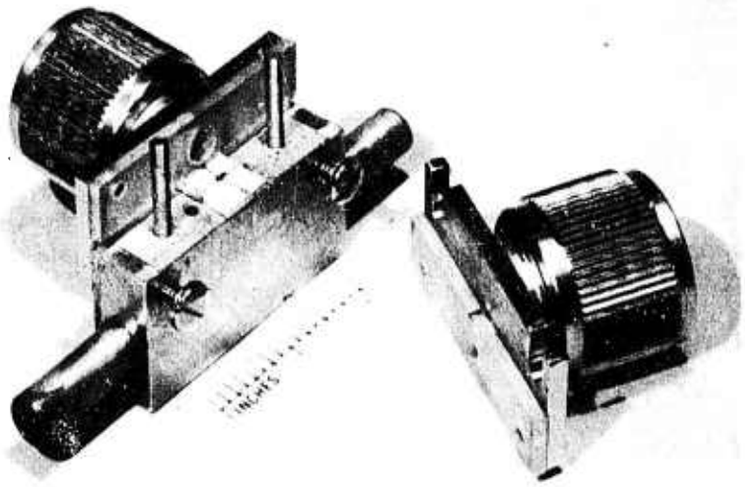

Figure 23(b). RF Test Fixture With Alford Launchers, Water-Cooled Copper Block and Device in Place

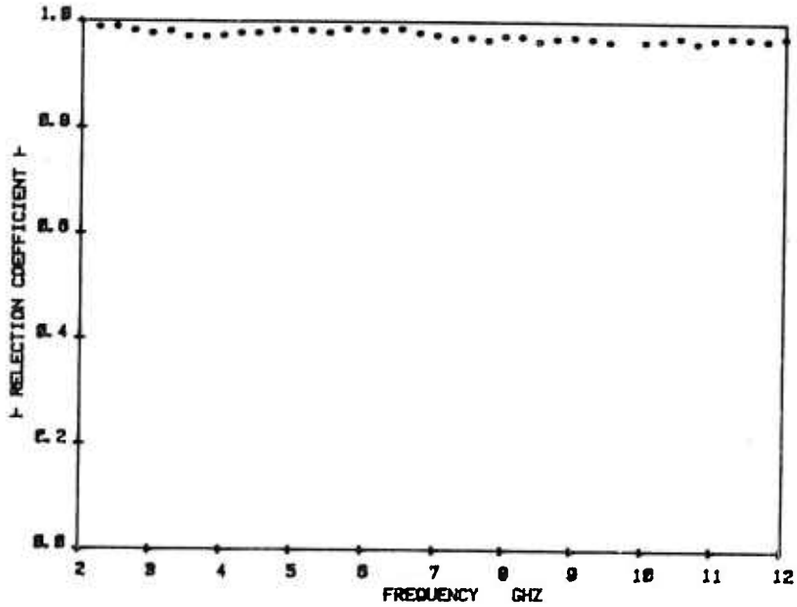

Figure 24(a). Reflection Coefficient vs Frequency with Shorted Header Assembly

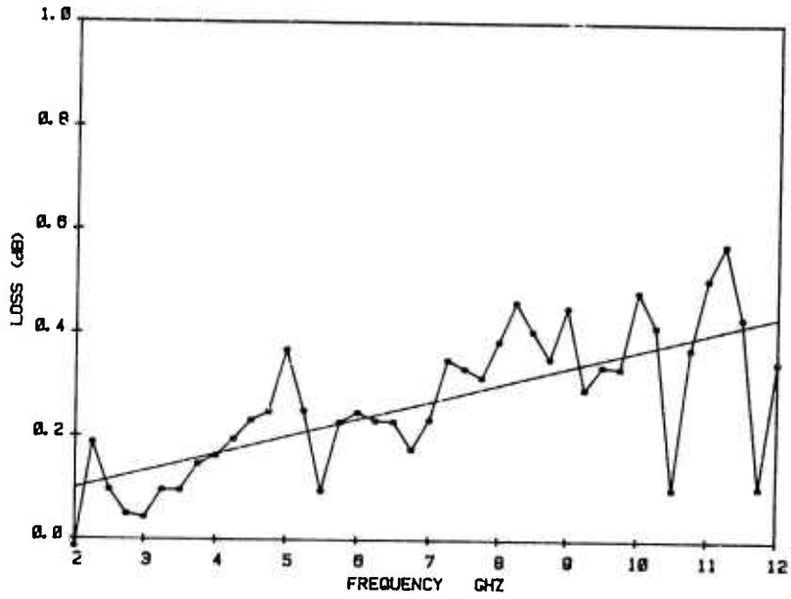

Figure 24(b). RF Fixture Loss vs Frequency With Through-Line Header Assembly

From the phase of the reflection coefficient, we deduce the electrical length of the header and launcher to be 3.525 cm. This value of electrical length issued to correct the phase of all measured S-parameter data taken on FET's in this header and fixture.

The lower curve in figure 24 shows the loss of the header and fixture when the header contains a 50-Ω microstrip through-line. The input reflection coefficient of this through-line was less than 0.2 up to 12 GHz. The straight line through the loss data from 2 GHz to 12 GHz represents the average loss and increases from 0.1 dB at 2 GHz to 0.45 dB at 12 GHz. These loss values were calculated by subtracting the reflection loss of S_{11} from the measured transmission loss of S_{21}. The variation of the measured data with frequency is due in part to the lack of full error correction on the S_{21} data measured on our network analyzer. Following these loss measurements, all the power test data for our FET's has been corrected by 0.2 dB loss at input and output when measured at 8 GHz.

The small-signal S parameters of our devices are measured on a Hewlett-Packard (HP) microwave network analyzer system. This equipment is controlled by an HP-9825A desktop computer with 24K bytes of memory and operates from 2 GHz to 18 GHz. In addition to taking data and performing the necessary error correction, the system can provide printouts or plots of the data or show it on a 17-in. diagonal graphics display screen. Program storage uses a floppy disc, while a permanent record of the measured S-parameters of most devices tested is kept on magnetic tape. Over 259 tests are currently on file using this system.

Our power testing of the GaAs FET's has also been automated using the HP-9825A computer. The advantages of this approach include enhanced accuracy, excellent reproducibility, long-term storage of tests results, and significantly reduced operator time for each power test. Most of all, the system provides the operator with a continuously updated display of the error-corrected device data during the test. This allows on-the-spot adjustment of tuners for optimizing the gain, output power, or power-added efficiency of the FET being tested.

The configuration of this system is shown by the block diagram of figure 25. The required instruments are connected to the HP-9825A computer using the Hewlett Packard Interface Bus (HPIB) or IEEE-488 general purpose interface bus. The low level RF source (upper left) is attenuated in 1-dB steps using HP-8494 and HP-8495 step attenuators controlled by a relay actuator operating from the HPIB line. This amplitude-controlled input signal is amplified by a travelling wave tube amplifier (TWTA) and then passes through an attenuator used for protection of the TWTA. A wideband directional coupler provides a sample of the incident power which is recorded by the computer using an HP-436A digital microwave power meter. The majority of the power passes through the directional coupler and through a circulator to the input of the device under test. The third port of the circulator is connected to an HP-432A microwave power meter which is used by the operator to monitor the reflected power at the input of the device under test. The output power of the device under test is attenuated, filtered, and monitored by the computer using another HP-436A power meter. Since the drain current of an FET can change as the power drive level is varied, an HP-3438A DVM is used by the computer to monitor the drain current throughout the test. Finally, since the power test bench is located at a right angle to the small-signal testing where the HP-9825A computer sits, an RS-232 serial communications link to a Hazeltine video terminal is used to put the power test data and instructions in front of the operator. A photograph of the power test bench is shown in figure 26. In the left foreground is the Hazeltine terminal. The left end of the bench has the RF source with a selection of three traveling wave tubes (TWT's) below. On the upper shelf are the two digital power meters, the analog power meter for reflected power observations and the power supplies and monitoring equipment. On the front of the test bench are the microwave components: step attenuator, directional coupler, circulator, bias tees, tuners, and the device under test.

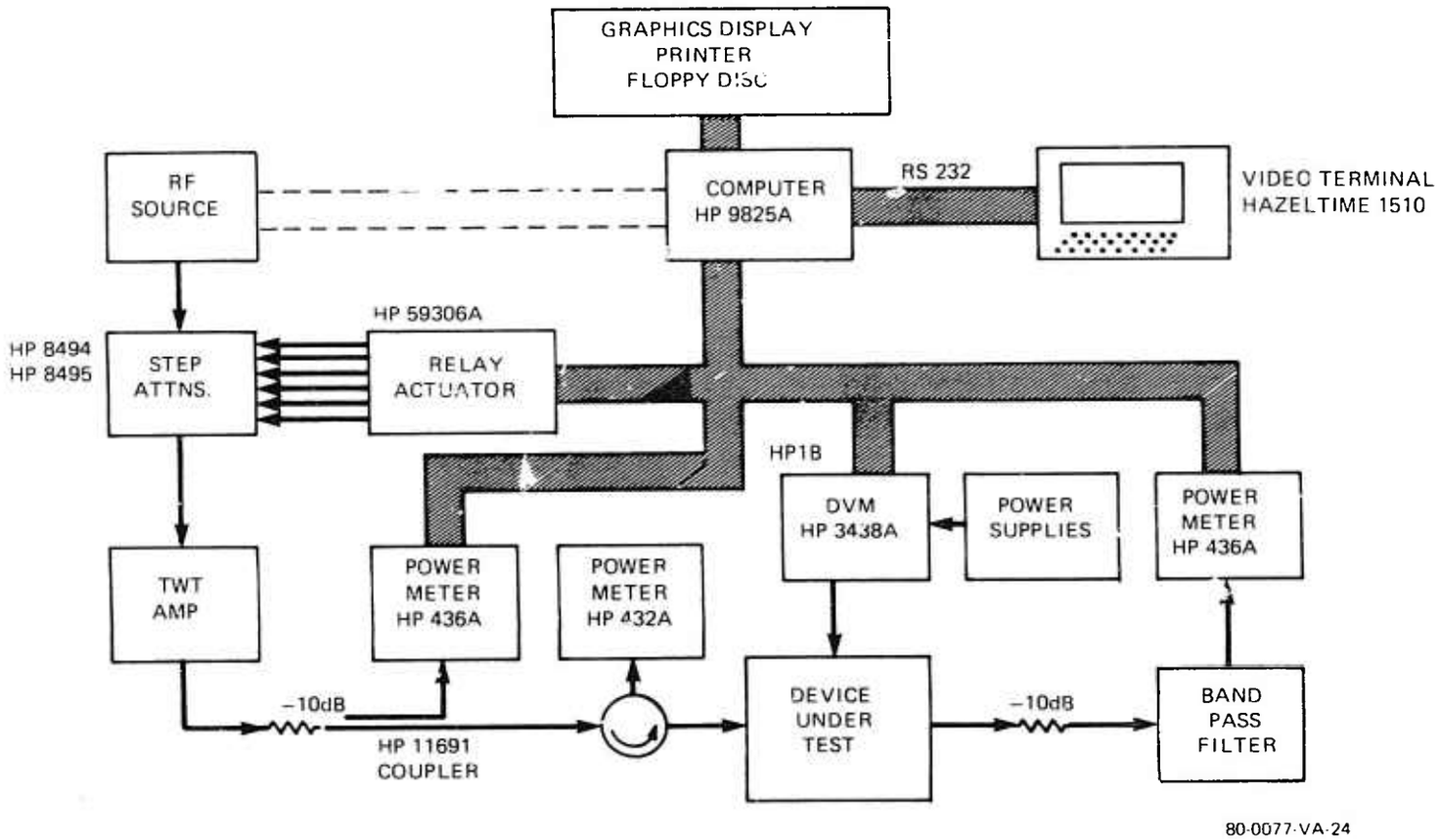

Figure 25. Block Diagram of Westinghouse Automated Microwave Power Measurement System for Characterizing GaAs Monolithic Power Integrated Circuits Developed Under DARPA Contract No. N00014-780-0268

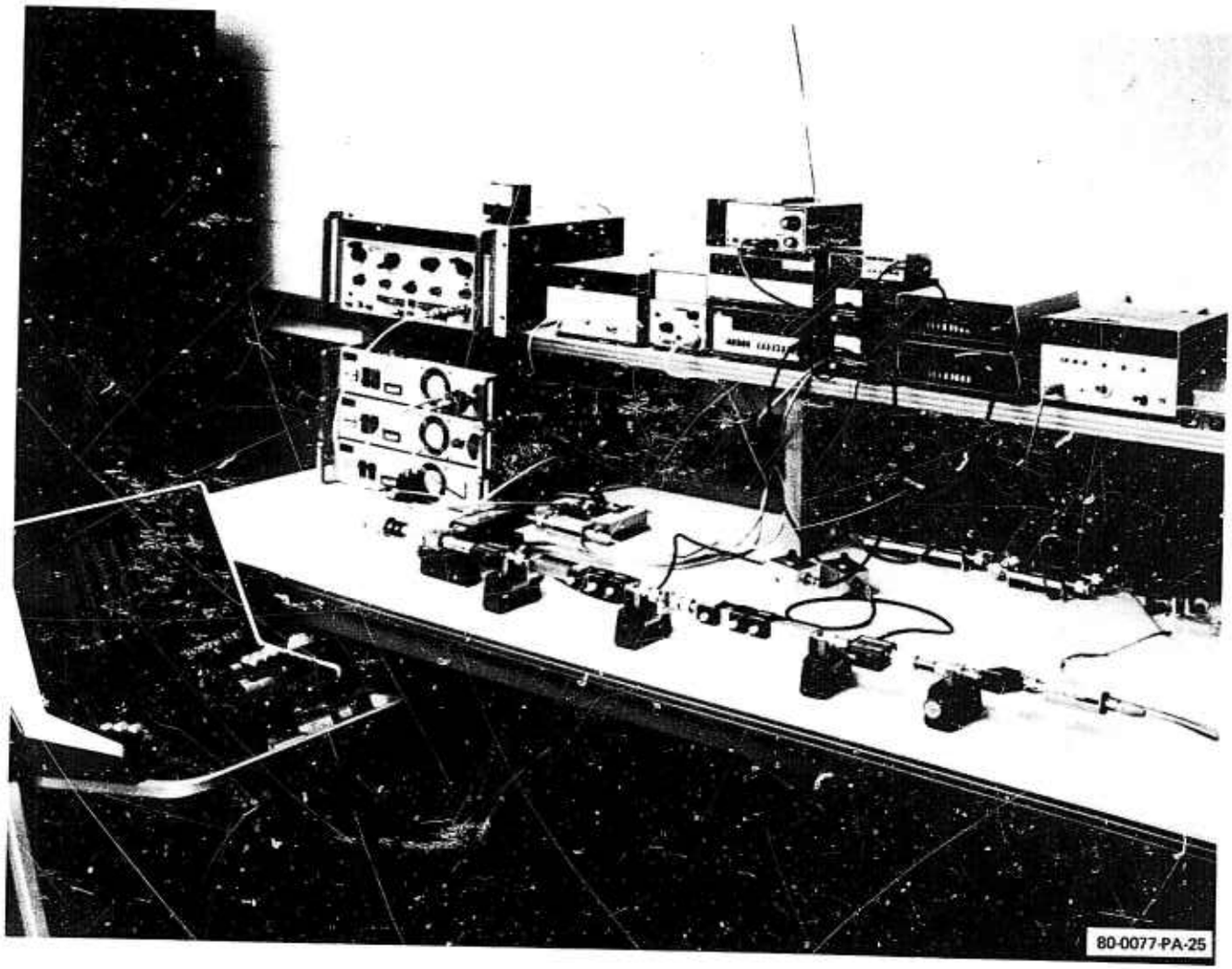

Figure 26. Power Test Bench

The system is calibrated with no device in place using the output power meter to establish the input power at the circulator output and then correcting the input power meter reading to this number. The output power meter is then connected to its normal location and, still with no device in place, the output reading is calibrated against the previously measured input power meter. The system now has two constants in memory which relate the true input and output power of the device under test to the input and output power meter readings, respectively.

When a device is tested, the system gives the operator a complete picture of the performance at all times. A printout of a power test on a 1200-micron periphery FET from run IC-7 at 8 GHz is shown in figure 27. The heading at the top identifies the device tested and the input power level at which the microwave tuning of the input and output of the FET was optimized for maximum output power. The next line shows the frequency, gate voltage, nominal drain voltage, resistance of the drain bias circuitry, and input and output loss of the tuners and the FET header. Then, we have the power test data. This shows corrected values of input and output power, gain, power-added efficiency, drain efficiency, drain current, and actual drain voltage at the device. This last term is the applied drain voltage minus the I-R drop in the bias resistance. These seven parameters are continuously measured, calculated, and displayed on the screen of the Hazeltine 1510 terminal during device tests to assist the operator in tuning the FET. In the case shown in figure 27, the FET produced 28.13 dBm output power at 8 GHz with 6 dB associated gain and 25 percent power-added efficiency. All of the power test data is stored on floppy disks for later reference and comparison.

3.3.3.2 Small-Signal Gain

All power FET's are tested for small-signal gain and their S-parameters are recorded for later modelling using the automated network analyzer. A typical set of S-parameters from 2 GHz to 12 GHz is plotted on a Smith chart in figure 28 for a 1200-micron periphery FET from run 1C-7 at V_D = 10 volts, V_G = -2 volts, and a

POWER TEST OF IC-7-B-#15-2-E TUNED FOR POWER @ 21 DBM

FREQ= 8.00 VG= -1.40 VD= 9.50 RD= 5.88 T1= 0.70 T2= 0.60

INPUT POWER dBm	OUTPUT POWER dBm	GAIN dB	POW-ADD EFF %	DRAIN EFF %	DRAIN CURRENT mA	DRAIN VOLTAGE V
-5.863	3.017	8.880	0.096	0.110	222.000	8.195
-4.933	3.977	8.910	0.120	0.137	222.000	8.195
-3.773	5.147	8.920	0.157	0.180	222.000	8.195
-2.853	6.097	8.950	0.195	0.224	222.000	8.195
-1.883	7.037	8.920	0.242	0.278	222.000	8.195
-0.903	8.017	8.920	0.304	0.348	222.000	8.195
0.127	9.057	8.930	0.387	0.444	221.000	8.201
1.137	10.047	8.910	0.486	0.558	221.000	8.201
2.177	11.097	8.920	0.619	0.710	221.000	8.201
3.177	12.097	8.920	0.780	0.894	221.000	8.201
4.157	13.087	8.930	0.980	1.123	221.000	8.201
5.137	14.057	8.920	1.224	1.404	221.000	8.201
6.327	15.237	8.910	1.606	1.843	221.000	8.201
7.277	16.197	8.920	2.004	2.299	221.000	8.201
8.207	17.127	8.920	2.473	2.837	222.000	8.195
9.187	18.117	8.930	3.107	3.563	222.000	8.195
9.857	18.797	8.940	3.635	4.167	222.000	8.195
10.867	19.817	8.950	4.582	5.251	223.000	8.189
11.897	20.857	8.960	5.780	6.621	225.000	8.177
12.897	21.877	8.980	7.288	8.343	226.000	8.171
13.907	22.917	9.010	9.201	10.523	228.000	8.159
14.907	23.957	9.050	11.579	13.225	231.000	8.142
16.067	25.127	9.060	14.897	17.009	236.000	8.112
17.077	26.047	8.970	18.042	20.661	241.000	8.083
18.057	26.767	8.710	20.820	24.058	245.000	8.059
19.097	27.337	8.240	23.087	27.160	248.000	8.042
20.067	27.687	7.620	24.509	29.635	246.000	8.054
21.117	27.947	6.830	25.273	31.890	242.000	8.077
22.137	28.137	6.000	25.294	33.778	238.000	8.101
23.147	28.257	5.110	24.187	34.968	236.000	8.112
24.207	28.307	4.100	21.688	35.498	235.000	8.118

Figure 27. Computer Printout for Power Test

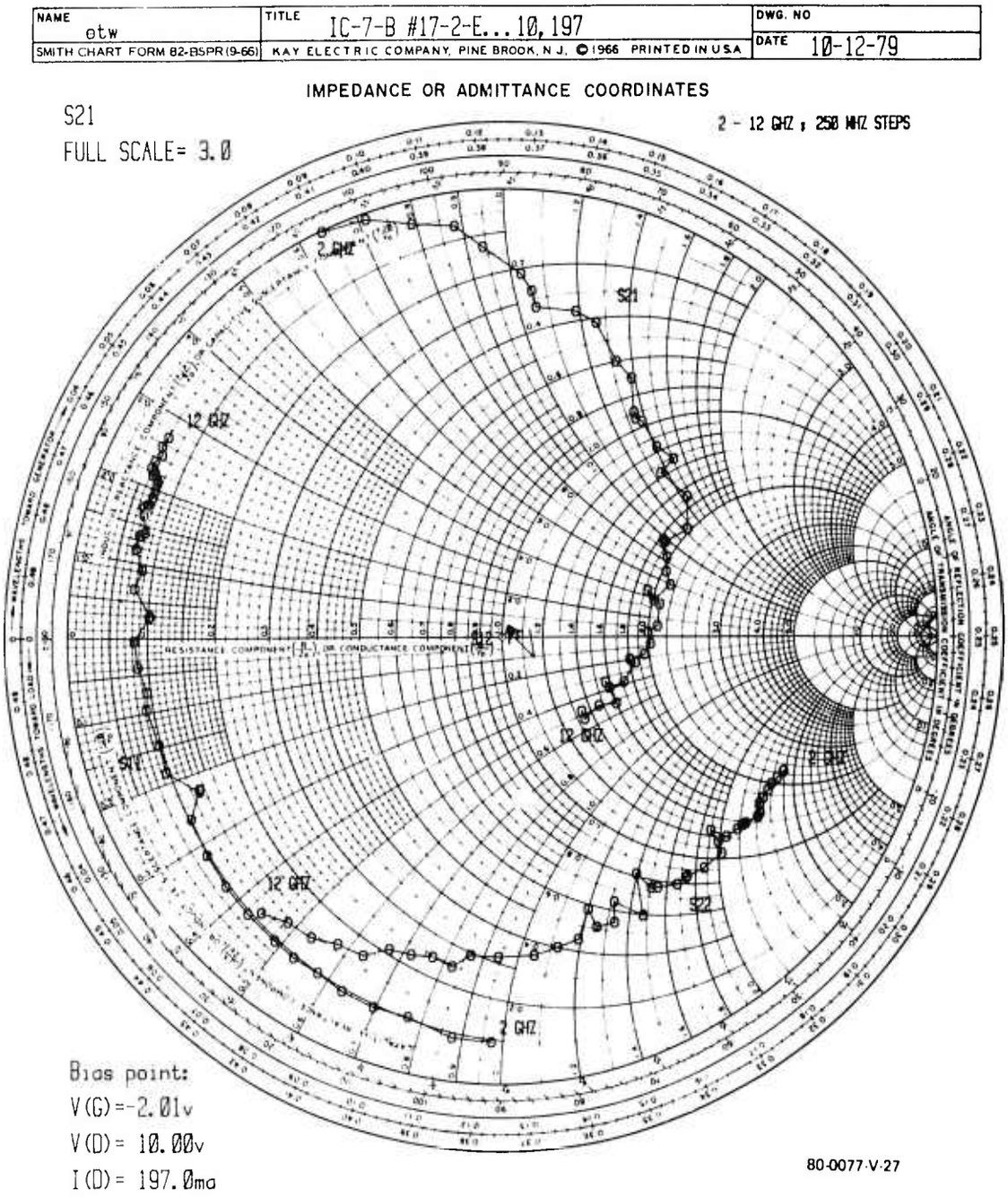

Figure 28. S Parameters for IC7 1200μ FET

drain current of 197 mA which is about half of I_{DSS}. S_{11} represents a well-behaved series R-L-C circuit with a real part of about 5 ohms. This is typical for a 1200-micron FET. S_{22} is more complex and needs both parallel and series elements to be modelled. The relatively large S_{22}, particularly at the low frequencies indicates a high value of R_{DS} and may lead to better power performance. The S_{12} is less than 0.1 and corresponds to very low reverse feedback through the FET on the header. Finally, S_{21} is large. The magnitude at the outside of the Smith Chart is 3.0 for the S_{21} curve. The magnitude of S_{21} drops below 1.0 above 9 GHz.

The maximum available gain of the FET's can be calculated from the S-paramters where the stability factor is above unity. In October, 1978, the gain of our early realigned gate GaAs FET's was 6-8 at 8 GHz, which was about 3 dB better than our previous self-aligned gate devices. The gains of several typical FET's from five wafers are plotted versus frequency in figure 29. Run 27A was fabricated on an eptiaxially-grown active layer, while run 28A was a direct implant of Si^+ into a commercial chromium-doped substrate. The gain of these two runs is nearly identical and shows about 8.5 dB at 8 GHz. The run labelled 1C-6-Cl is also a Si^+ implant, but uses a Westinghouse-grown chromium-doped substrate and has somewhat reduced gate length which produces better gain up to about 8 GHz. Two of the most recent power FET runs are also plotted, 1C-7-B and D-9-E. Both of these runs show small-signal gains between 11 dB and 12 dB at 8 GHz or a 3-4 dB gain improvement. Both these runs are Si^+ implants into undoped GaAs substrates grown at Westinghouse. 1C-7-B used a WA18M substrate grown in a quartz crucible while D-9-E used WBN3 grown in a pyrolytic boron nitride crucible. To date, all device runs using undoped-GaAs substrates have shown this improved gain.

3.3.3.3 Small-Signal Model

Small-signal models for devices from each run are created to further understand the relationships between FET performance and important device parameters. Run-to-run differences in the model

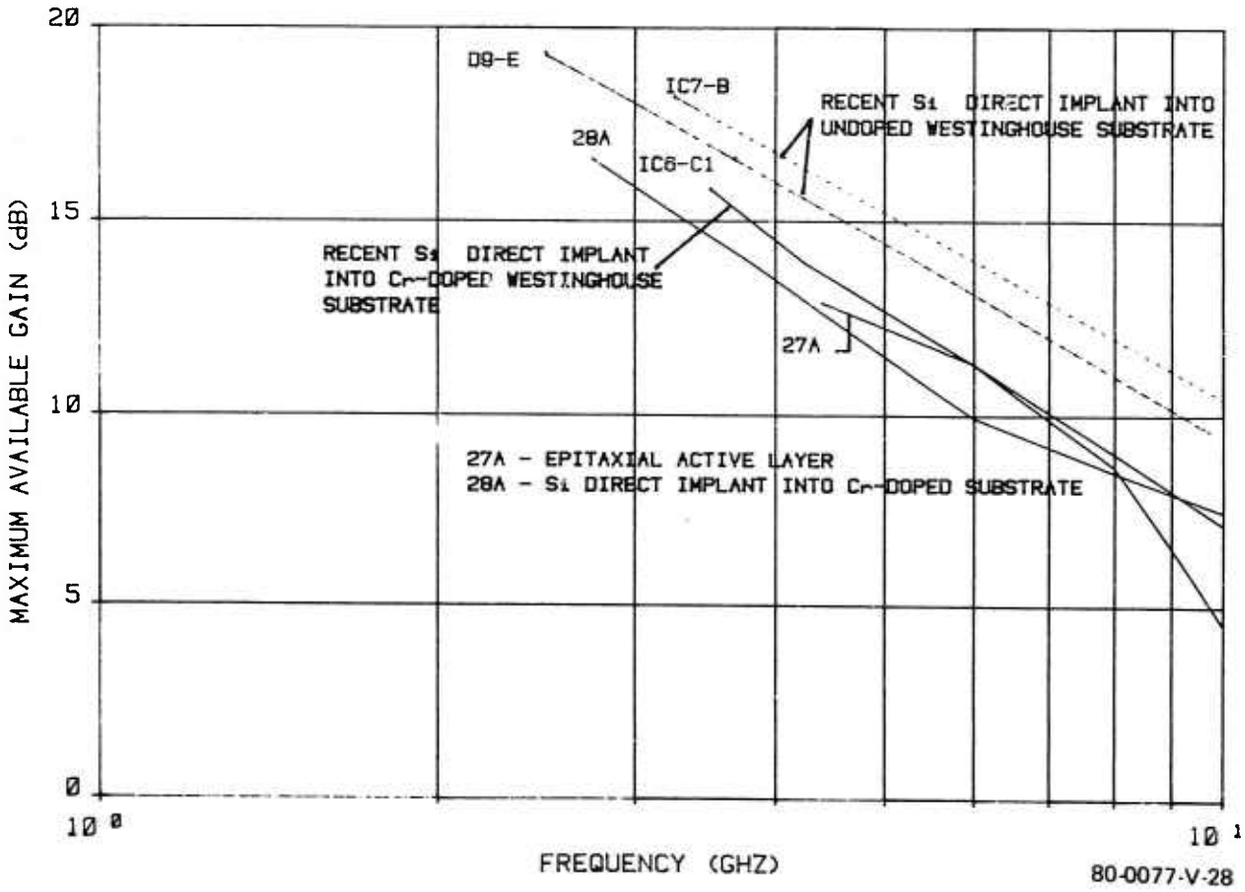

Figure 29. Maximum Available Gain for Typical FET's from Five Device Runs

values allow the identification and isolation of device problem areas to specific processes including fabrication, mounting and bonding, and materials. The behavior of the model parameters for successive runs confirm the methods used to achieve improved device performance. Scaled models can be used to predict the gain and S-parameters of different size devices, a technique particularly useful in integrated circuit (IC) amplifier design.

The circuit constructed to represent the device is shown in figure 30. Intrinsic device elements include R_G, R_D, G_M, C_{GS}, C_{GD}, C_{DS}, and . R_{DP}, R_{GP}, R_{SP}, L_{GP}, L_{DP}, and L_{SP} are the extrinsic elements. Values for each element are obtained by optimizing the model to measured 2 to 12 GHz S-parameter data, using microwave circuit analysis programs, such as COMPACT and similar Westinghouse programs.

Figure 31 shows a typical fit of the modelled S parameters to those of a measured device. The series RLC network used to represent the input of the FET consistently provides a good fit to the measured S_{11}, as shown in the figure. The transit time

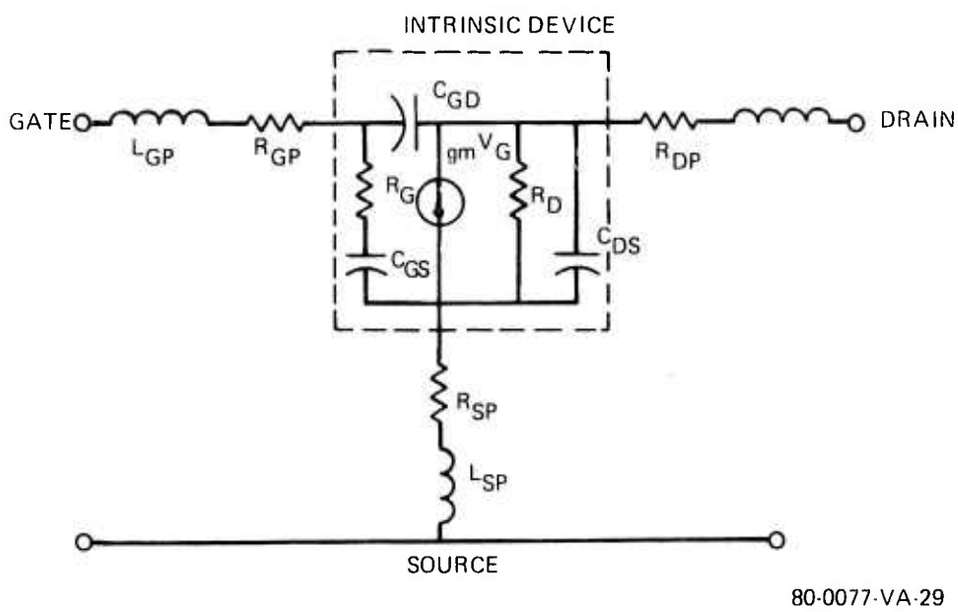

Figure 30. FET Model

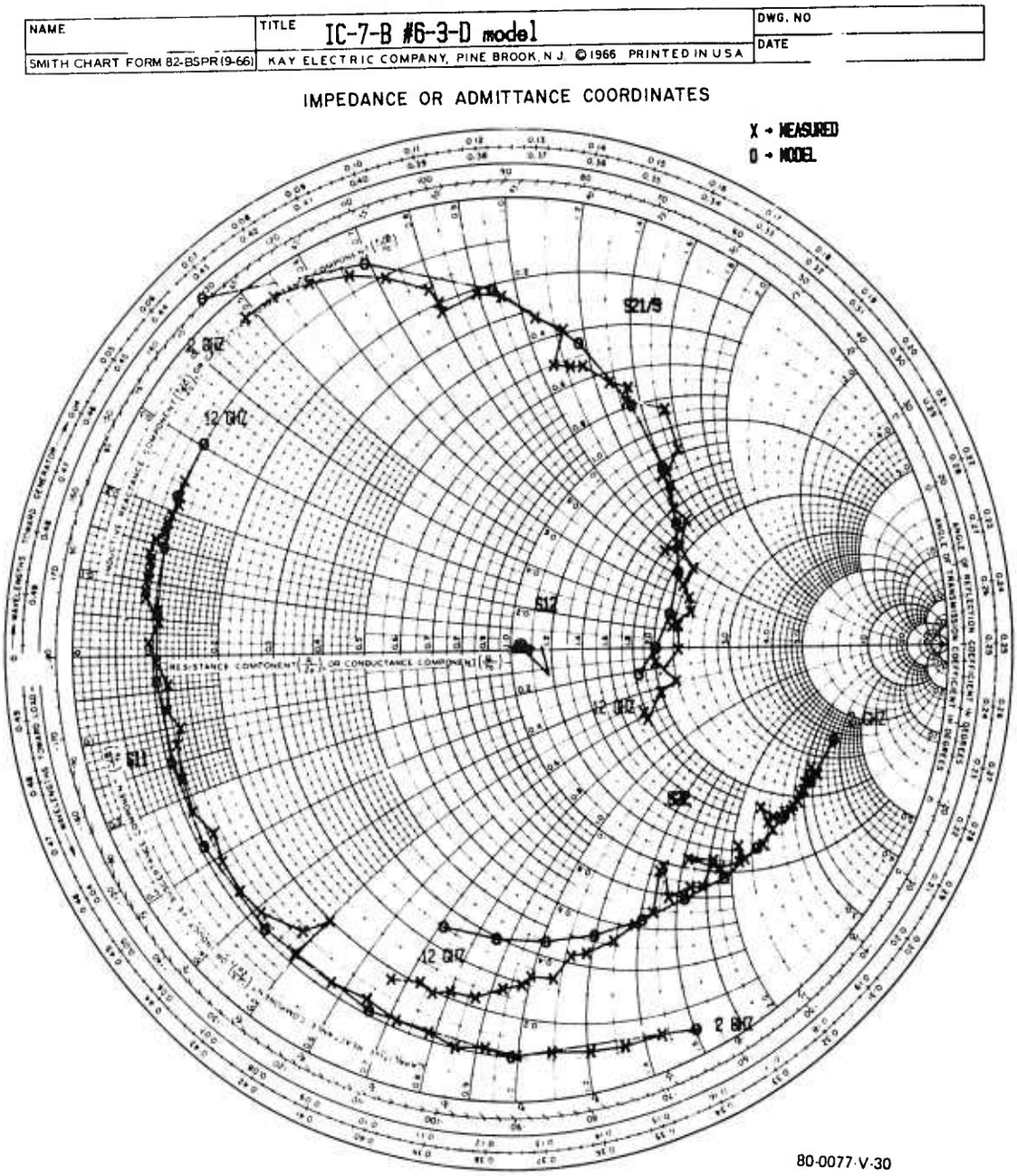

Figure 31. Comparison Between Measured S Parameters and Model

of the carriers under the gate of the FET, τ, was added to the FET model to provide consistently good fits for the modelled S_{21} to the measured data. The predicted S_{12} also matches the measured data over most of the frequency range. At the higher frequencies, where measurement problems associated with the test equipment result in irregular data, the fit is worse. Agreement between the model and measured data for S_{22} is difficult to obtain, particularly above 9 GHz. The inability of the model to accurately reproduce S_{22} over the whole frequency range may indicate that additional elements are needed in the model. Attempts to modify the model have not yet been successful. The maximum available gain and the K factor calculated from our model are in reasonable agreement with the measured values up to the frequencies where the deficiencies in the predicted values of S_{22} begin to have an effect.

Representative model values for some recent devices are given in table 4. Device periphery is 900 μm in each case. The series RLC input network has resistance values of about 4.5 ohms and

TABLE 4

SMALL SIGNAL MODEL PARAMETERS FOR RECENT DEVICE RUNS

900 μm

RUN	R_G+R_{GP} (Ω)	R_D (Ω)	R_{SP} (Ω)	R_{DP} (Ω)	G_M (m℧)	C_{GS} (pF)	C_{GD} (pF)	C_{DS} (pF)	L_{SP} (nH)	TAU (ps)
IC-6-C1	4.96	255	0.367	4.17	30.6	0.889	0.019	0.204	0.015	8.7
IC-7-B	4.2	381	0.793	4.2	42.2	0.918	0.017	0.019	0.021	8.49
D-9-E	4.5	395	0.82	4.1	46.9	1.02	0.013	0.206	0.025	11.1

80-0077-T-35

capacitance values ranging from 0.9 to 1 pF. Earlier devices have shown resistance values a few ohms higher and capacitance values have varied considerably, as the implant-doping profiles have been modified. The parasitic drain resistance, R_{DP}, is about 4 ohms in all three runs. Studies of the effect of R_{DP} on the predicted gain of the model show that this element is not very important. The values for C_{DS} and C_{GD} are similar for the three devices, 0.2 pF for C_{DS} and 0.013 to 0.019 pF for C_{GD}. Earlier runs showed feedback capacitance values three to four times higher than this. Parasitic source inductance, a problem associated with the mounting procedure, shows some variations; values ranging from 15 to 25 pH. The source areas on IC-6-C1 and IC-7-B were interconnected as part of the device fabrication, but the D-9-E source areas were interconnected by two 0.7-mil diameter gold wires stitch bonded between sources. In all cases, gold ribbons were used to connect the sources to ground. Despite the bonding differences, the source inductance for these runs was similar.

The elements which show the largest variation from run to run are R_{SP}, the source parasitic resistance; R_D, the shunt output resistance; and G_M, the tranconductance. We do not have a good explanation for the source resistance variations. The values of R_D and G_M have increased by factors of 1.5 to 2 over the modelled values for earlier runs. The values of R_D and G_M for runs IC-7-B and D-9-E are similar and contrast sharply with those of IC-6-C1. This difference may, in part, be atributed to the material properties. IC-6-C1 was fabricated from chromium-doped (WA4M) material, while IC-7-B was fabricated on undoped material (WA18M) pulled from a quartz crucible and D-9-E on undoped material pulled from a boron nitride crucible (WBN3). The resistivity of WA18M was low, $2x10^3$ Ω-cm, compared with $2x10^9$Ω-cm for WA4M and $5x10^7$Ω-cm for WBN3.

The lower value of output impedance for IC-6-C1, 255 Ω, compared with 381Ω for IC-7-B and 395Ω for D-9-E, may reflect conduction through the substrate due to the ionization of chromium centers proposed by Eastman[6].

The improved G_M for IC-7-B and D-9-E over that for IC-6-Cl is caused by the higher mobility values achieved when implanting into undoped substrates. The chromium-doped material produced 4100-4400 $cm^2/V\text{-}s$, while IC-7-B and D-9-E gave 4900 $cm^2/V\text{-}s$ and 4800 $cm^2/V\text{-}s$, respectively. The small-signal model predicts improved gain with better G_M and R_D values, which agrees with our material and processing improvements. The improved small-signal gain performance of recent runs is shown in figure 29. In addition, the RF G_M for recent runs has shown better agreement with the DC G_M measured at the same bias point.

3.3.3.4 Power Output

Improvements in substrate material and device processing techniques have allowed the output power per unit periphery of Westinghouse FET's to reach 0.648 W/mm for a 900-micron periphery FET and to equal or better 0.5 W/mm for FET's from the last five device runs. By combining two 900-micron or two 1200-micron FET's on a single chip, output powers of 0.916 W and 1.039 W at 8 GHz, respectively, have been achieved and better results from these larger devices is expected when source vias are added. Power-added efficiencies up to 33 percent have been observed with typical FET's giving 20-25 percent at 8 GHz.

Table 5 gives the best output power achieved for different device peripheries at 8 GHz. The best power per unit periphery, 0.648 W/mm, was achieved with a 900μm device, IC-7-B No. 22-2D. Output power at 8 GHz was 0.583 Watts. The details of the performance of this device will be discussed later. The 1200μm device, IC-7-B No. 12-2-E achieved 0.744, Watts at 4.8 dB gain, 20 percent power-added efficiency. Power/mm was 0.62 W/mm, which is comparable to the 900μm device. The linear gain was 7.8 dB and exhibited slight gain expansion to 8.1 dB just before output power saturation. I_{DSS} for this device was 390 mA. The device was tested at the bias point V_D = 10.6V, V_G=1.5V at 238 mA drain current. The best 1800μm device, D-9-E No. 5-3AB-6, consisted of two 900-μm devices bonded together. An output power of 0.916 Watts was achieved with 4.6 dB associated gain with 16.3 percent power-added

TABLE 5

OUTPUT POWER VS DEVICE PERIPHERY

8 GHz

Device Size (μm)	Device	V_D (V)	P (W)	P/mm
900	IC-7-B No. 22-2-D	10	0.583	0.648
1200	IC-7-B No.12-2-E	10.6	0.744	0.62
1800	D-9-E No.5-3-A8-6	10	0.916	0.51
2400	D-9-D No.2-6-AB-8	9.1	1.039	0.43

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efficiency. The power/mm, 0.502 W/mm, is lower than that of the previous devices, which may indicate problems in cell combining. The linear gain of this device was 8.2 dB. I_{DSS} was 600 mA, and V_D=10.0V, V_G = -2.5V at 265 mA drain current, the bias point.

A best-power output of 1 watt at 4.7 dB gain, 13 percent power-added efficiency was achieved with the 2400μm device, D-9-D No. 2-6-AB-8. The power per unit periphery was 0.43 W/mm. I_{DSS} for this device was 795 mA, and the bias point during the test, V_D=10.0V, V_G= -3.0V at 341 mA drain current. The output power vs gain characteristic is shown in figure 32. This device has a flat linear gain of 6.2 dB. The output power starts to saturate at 28 dBm, with 29.8 dBm of power at the 1-dB compression point. The power-added efficiency increases smoothly to a maximum of 13.5 percent but does not peak.

This device was mounted on the standard header and tested in the fixture described earlier, using the automated test system. Input and output tuning was accomplished using Alford

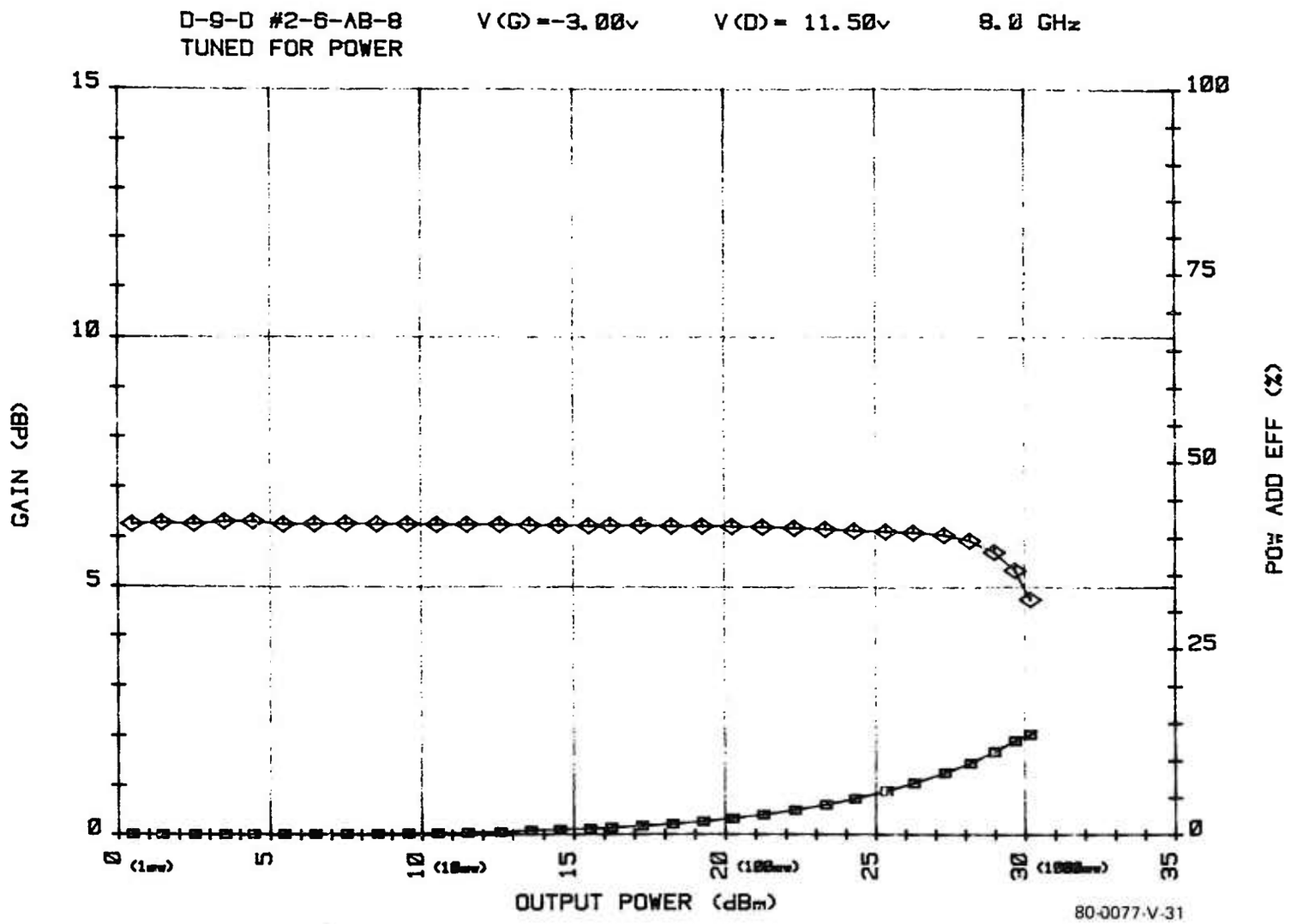

Figure 32. Gain vs Output Power for D-9 900μ FET

triple slug coaxial tuners. Due to difficulties encountered when tuning devices of this size and bias stability problems, the output power was not completely optimized for the bias point or drive levels used and superior results are expected from future devices.

At 8 GHz, the device which exhibited the best power per unit periphery, 0.648 W/mm, was IC-7-B No. 22-2-D. This device has an I_{DSS} of 330 mA. The maximum available gain calculated from the device S-parameter data was 11.6 dB at 8 GHz, which is in excellent agreement with the linear gain of 11.3 dB obtained when the device was tuned for gain at low input power levels in the power test system.

The output power vs gain characteristic is shown in Figure 33, for this device. The power test was taken with V_D=10V, V_G= -1.4V, and a drain current of 179 mA. The linear gain of the device was about 9.25 dB when tuned for optimum power. The output power begins saturating at about 26.3 dBm and, as the gain falls below 7 dB, little additional power is produced. The efficiency increases smoothly to a peak value of 23.78 percent with an output power of 27.43 dBm and 7.12 dB associated gain before rapidly dropping off.

This device was also tested for output power at different drain voltages. The gate voltage was held constant and the device tuned for optimum output power at each drain voltage. The linear gains achieved increased from 8.7 dB at the lowest drain bias to 9.6 at the highest. Figure 34 shows the effect of the drain bias voltage on power/mm and power-added efficiency. The associated gain for each data point is 5 dB. The output power/mm increases smoothly from about 0.5 W/mm at the lowest drain voltage to a high of 0.648 W/mm in the 9 to 10 V region and then decreases as the voltage is increased further. The power-added efficiency decreases steadily from a high value of 27.42 percent at the lower drain voltage to 19.69 percent at the higher drain voltage. This problem may be the result of gate-drain breakdown. The

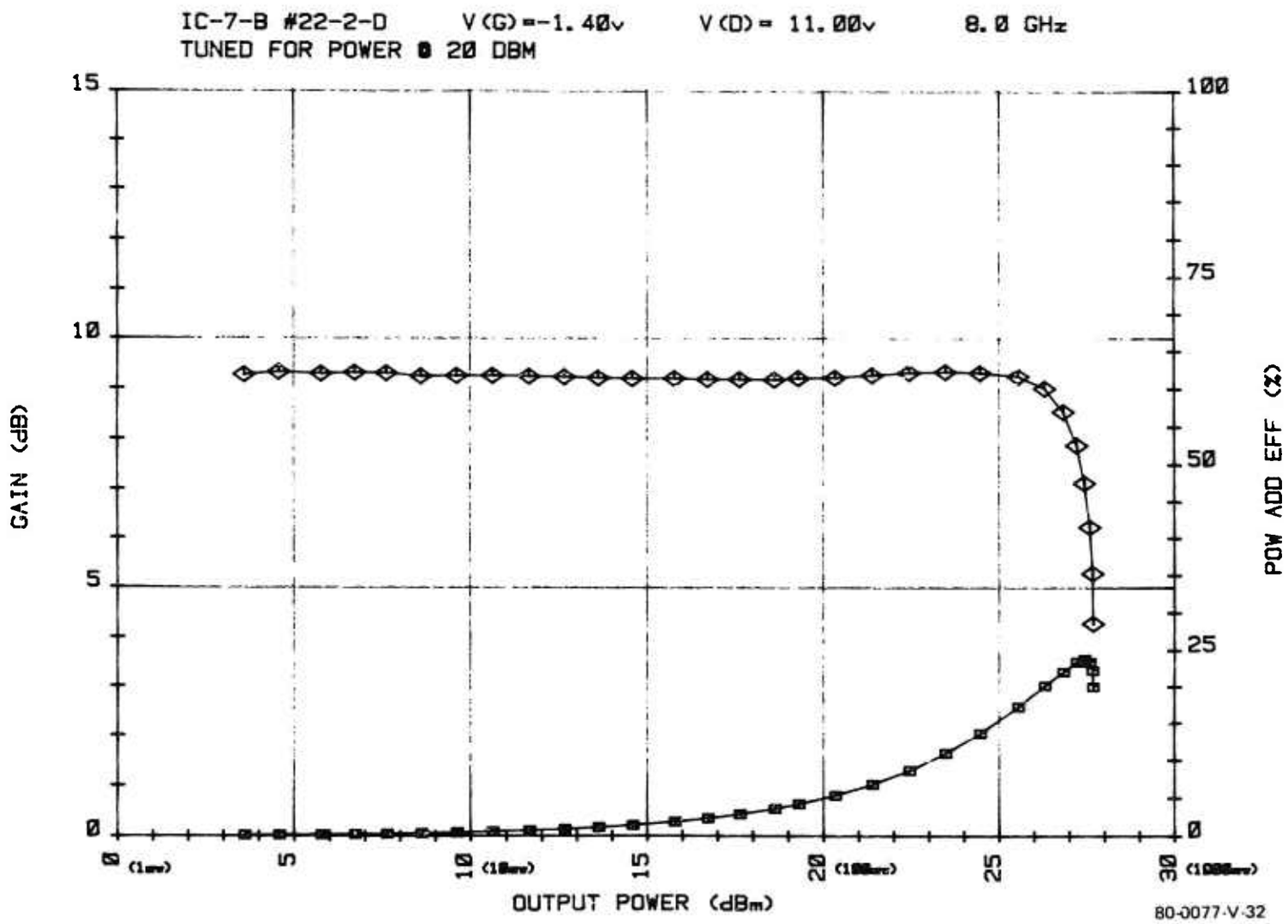

Figure 33. Gain vs Output Power for IC7 900μ FET

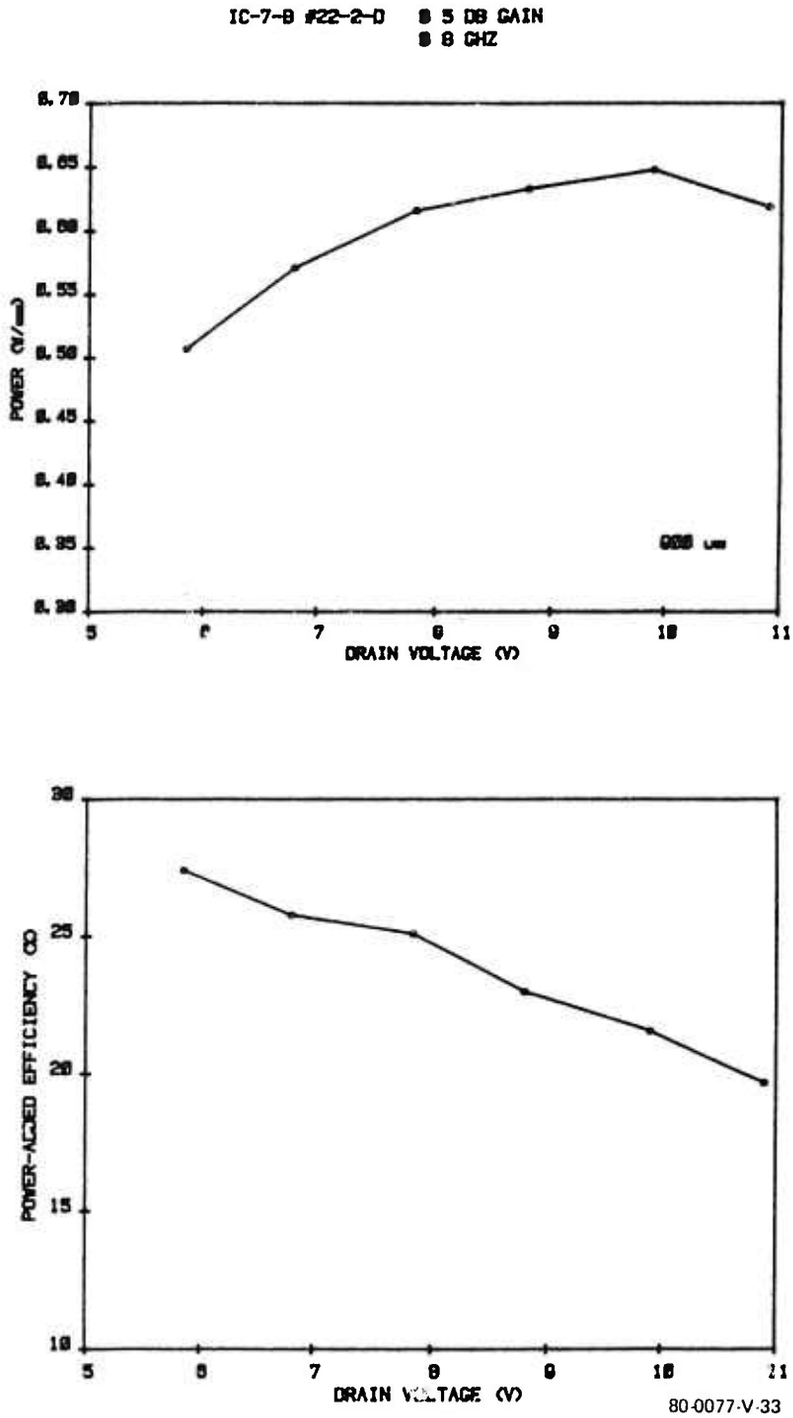

Figure 34. Effect of Drain Voltage on Power/Unit Periphery

tradeoffs apparent between and efficiency illustrate the need for consistency when discussing power performance.

Improvements in materials and fabrication techniques have allowed the performance of Westinghouse FET's to improve significantly. Figure 35 is a chronological listing of the performance of Westinghouse ion-implanted FET's since October 1978. This figure shows the steady improvement in the output power per unit periphery achieved by Westinghouse through September 1979. The last five runs have produced FET's which power/mm equal to or greater than 0.5 W/mm. Three of these runs have been with Westinghouse material. Output powers of 0.916 W and 1.039 W at 8 GHz with 1800-μm and 2400-μm devices have been achieved by combining FET's on a single chip and better results can be expected from these larger devices.

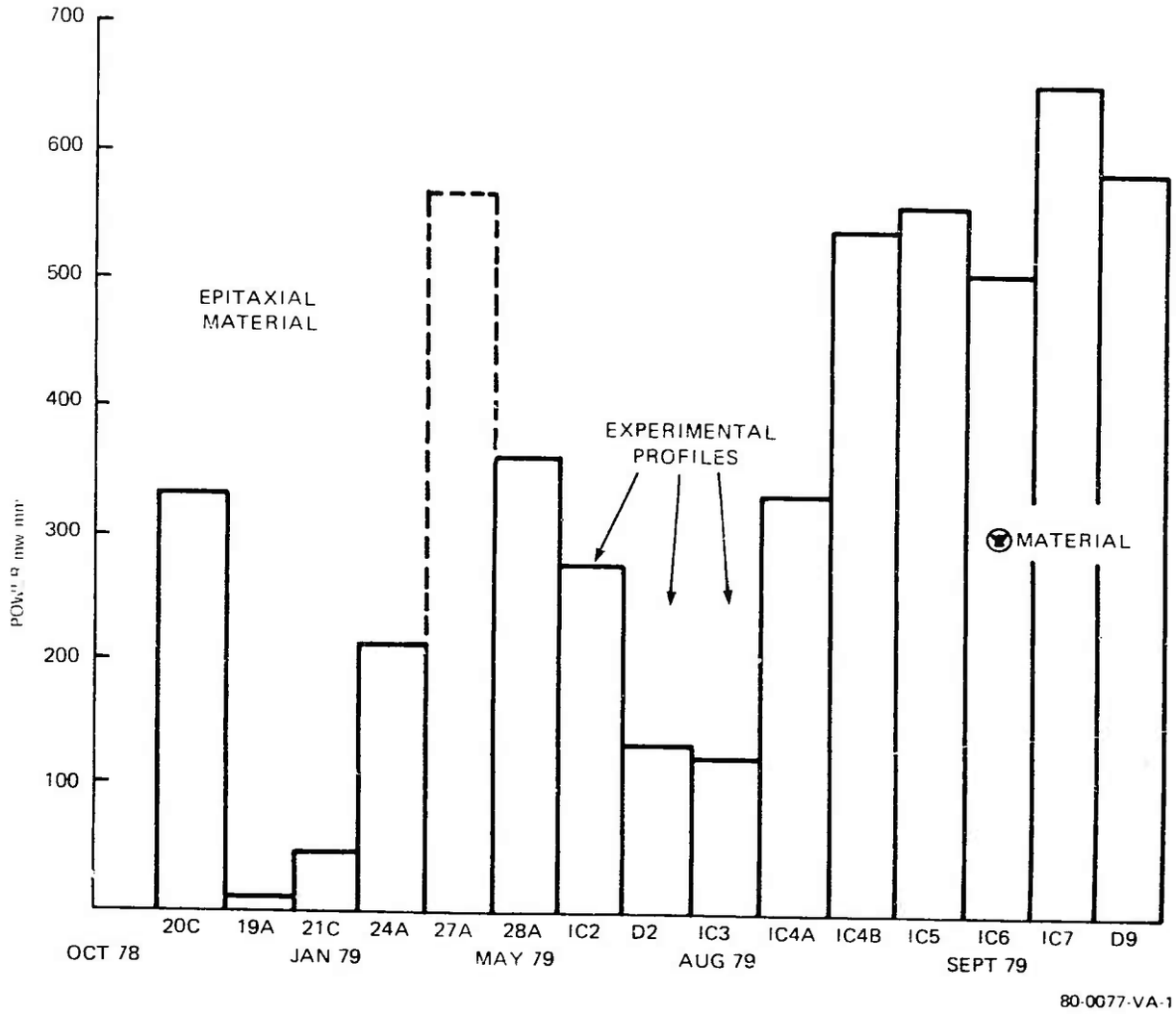

Figure 35. Power Output Per Unit Periphery for Westinghouse Ion Implanted FET's Since October 1978

4. MONOLITHIC AMPLIFIERS

4.1 CIRCUIT DESIGN TECHNIQUES

4.1.1 Introduction

Two fundamental monolithic amplifier types have been studied during the past year, the "coplanar" lumped-element type and the "microstrip" lumped-element type. The primary difference between the two types is, of course, the absence of a ground plane on the bottom of the coplanar amplifier chip. This difference creates unique advantages for each type, as outlined in table 6.

TABLE 6

COMPARISON OF COPLANAR AND MICROSTRIP MONOLITHIC AMPLIFIERS

Microstrip Advantages	Coplanar Advantages
1. Circuit elements are more easily calculated (well-defined ground)	1. Smaller, higher Q inductors
2. Reduces mutual coupling between inductors	2. Zo less dependent on GaAs wafer thickness.
3. Source vias and heat sinking are more easily realized.	3. Fringe capacitance to ground is lower.
4. No need for symmetry.	
5. Crossovers minimized.	
6. Topologically easier to arrange bias.	

During the early evolutionary stages of development of the directly-implanted FET's when output powers were low (<0.3 W/mm), the emphasis was on coplanar amplifiers since the lack of fringe capacitance to ground made lumped-element circuit design calculations straightforward. This allowed simple and rapid amplifier redesigns to accommodate the changing FET parameters from run to run.

However, as the implanted FET's have evolved and output powers >0.6 W/mm have become commonplace, the microstrip amplifier has the overwhelming advantage because of its much better heat-sinking capabilities. Hence, all current amplifier designs are microstrip. Examples of both types are shown in figure 36.

In order to keep chip size as small and as compact as possible, all amplifiers have utilized lumped-element (L's and C's) matching networks (versus distributed networks, which involve elements which are an appreciable fraction of a wavelength in size). The lumped-element design techniques for both amplifier types are similar except that the fringing capacitance to ground must be accounted for in the microstrip case to ensure accurate designs. Design procedures for lumped inductors and capacitors, as well as the associated microstrip transmission lines on GaAs, are discussed in the next three sections.

4.1.2 Lumped Element Design

4.1.2.1 Capacitors for Monolithic Circuits

Depending on the electrical application, there are two types of capacitors appropriate for monolithic microwave integrated circuits. The first of these is the thin-film overlay type, shown in figure 37, which is characterized by high capacitance/unit area (C/A) ratios for thin (0.1-0.3 micron) films, but low Q valves ($Q \approx 1$-10). Q valves can be made higher by using thicker films, but only at the expense of lowered C/A ratios.

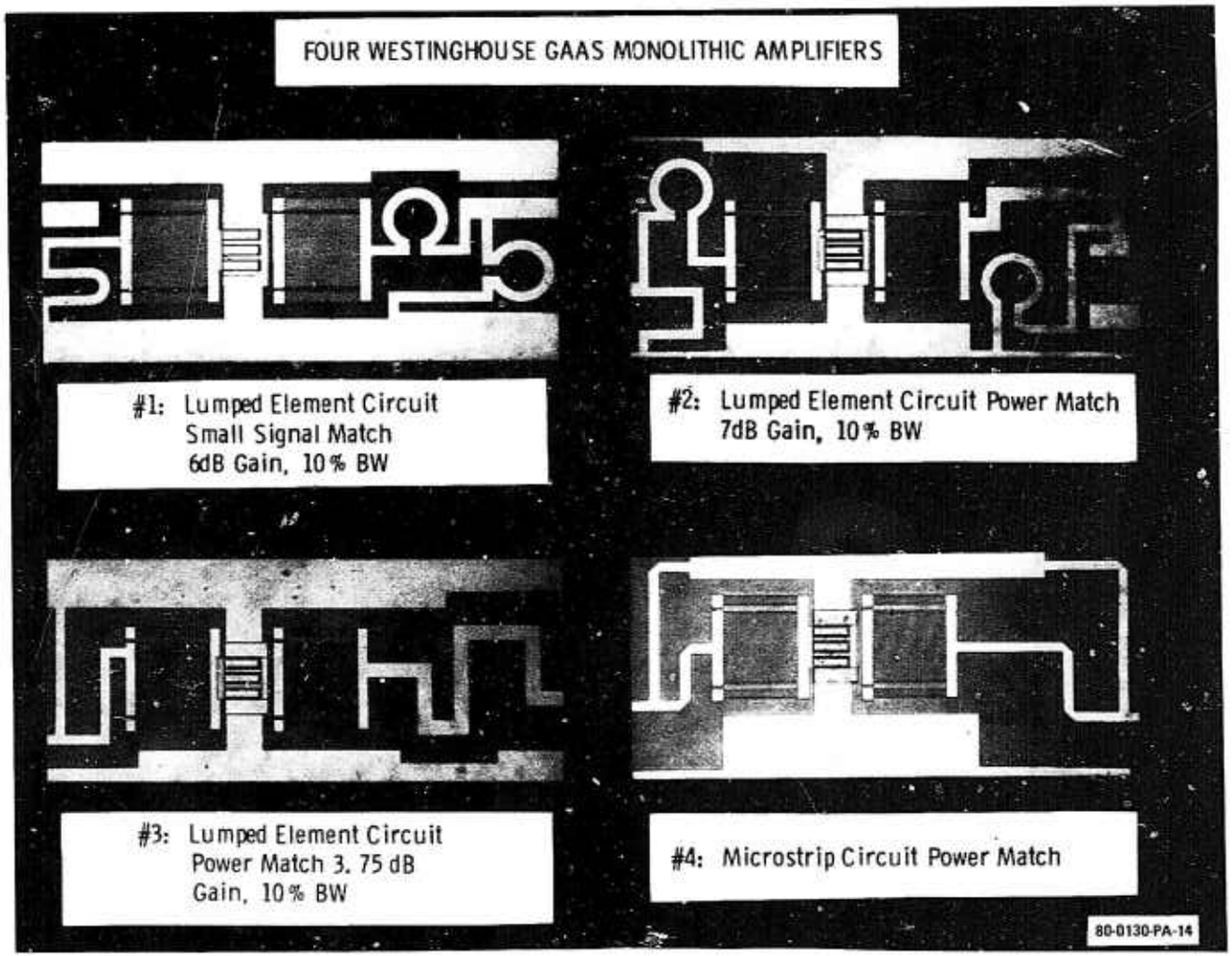

Figure 36. Westinghouse GaAs Monolithic Amplifiers

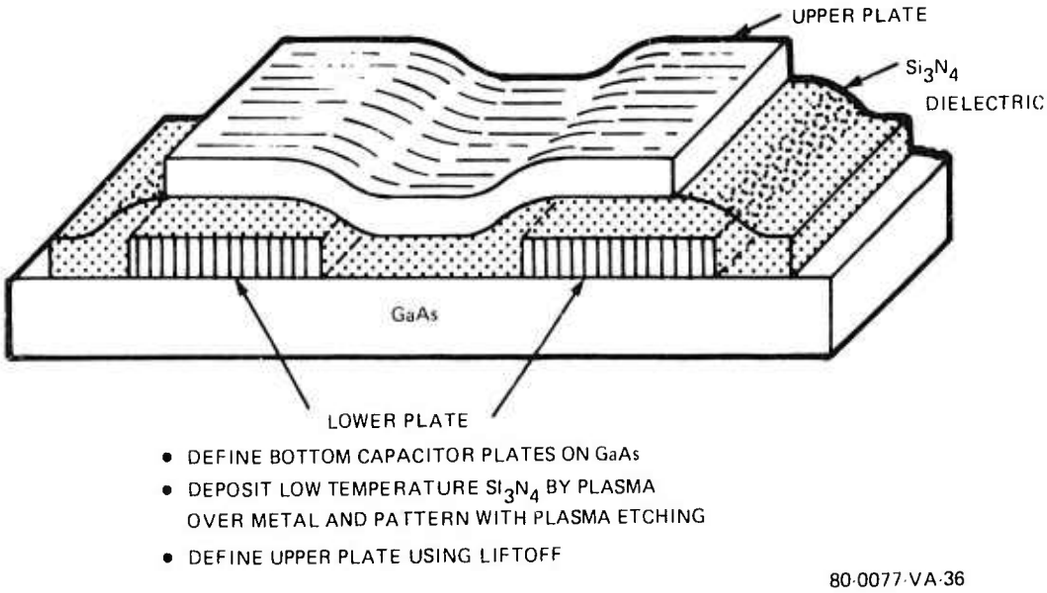

Figure 37. Overlay Capacitor Construction

These capacitors are appropriate for blocking and bypass applications. Several different dielectrics can be used in these capacitors, including:

- Sputtered SiO_2
- Pyrolitically-grown SiO_2
- Anodized Aluminum
- Anodized GaAs
- Tantalum Pentoxide
- Silicon Nitride
- "Organic" Oxides

However, from the standpoint of process compatibility, Silicon Nitride is the preferred dielectric since it is already used for capping and can withstand high temperatures. To date, due to the intensity of the discrete FET development effort during the past year, the time devoted to overlay capacitors has been minimal; hence, an overlay technology has not been developed. This has not proved a hindrance since bypassing can be accomplished temporarily by chip capacitors immediately adjacent to the amplifier chip.

The second type of monolithic capacitor is the interdigital capacitor which is appropriate for tuning elements. These capacitors are characterized by high Q's, typically 40-60 at 5 GHz, but small capacitance values, ranging from 0.05 up to 2 pF. During the first reporting period, attempts were made to fabricate interdigital capacitors using both ion-milling techniques and plating through thick photoesist. Both of these techniques suffered from various problems including low yield, poor line definition, edge buildup and low Q.

Because of these problems, a new technique was developed. This new technique, which is described more fully in section 4.4, involves the "chlorobenzene-assisted" lift-off of thick (1.5 microns) evaporated gold to form the interdigital fingers. It has proved to be a very successful and reproducible way to make high-quality interdigital capacitors (see section 4.4).

Two design techniques have been used for these interdigital capacitors; the first uses Alley's[7] analysis, while the second is a coupled-line analysis patterned after that developed by Paolino[8] for the "Lange" interdigitated coupler. Alley has modelled the interdigital capacitor as a pi network of capacitors with the shunt capacitance at each end being the sum of the terminal strip and finger capacitance to ground (figure 38). A coupled-line type of analysis was also carried out using the same model. Both methods yield essentially the same values for the series capacitance element C_2. The coupled-line analysis is advantageous in microstrip because it readily provides a value for the shunt capacitance of the fingers C_1. Both C_1 and C_2 are proportional to the number of fingers of the capacitor, as shown in figure 39.

In order to confirm the validity of the above design techniques, an experimental investigation was carried out using a typical matching circuit cut from a monolithic amplifier. For this investigation, the interdigital capacitor values are deduced from S-parameter measurements of the matching circuit. A model was first created corresponding to the circuit (figure 40), then the element

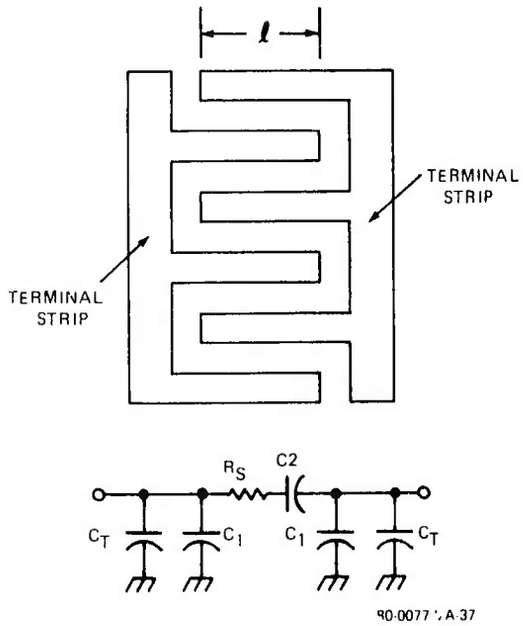

Figure 38. Interdigital Capacitor Layout and Schematic

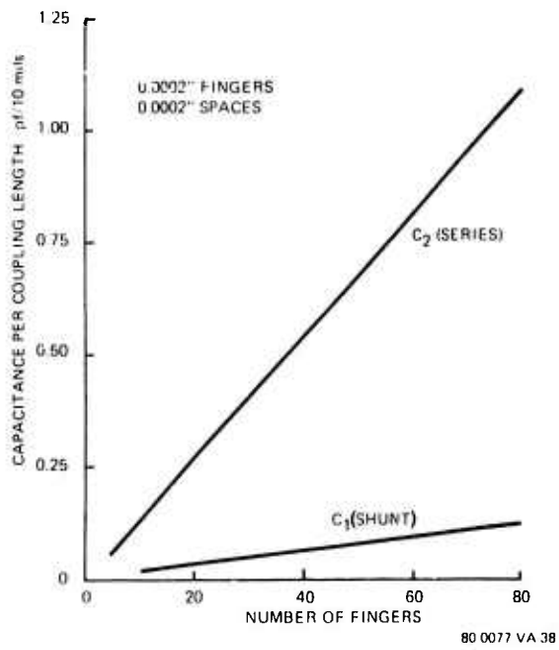

Figure 39. Capacitance vs Number of Fingers for Interdigital Capacitor

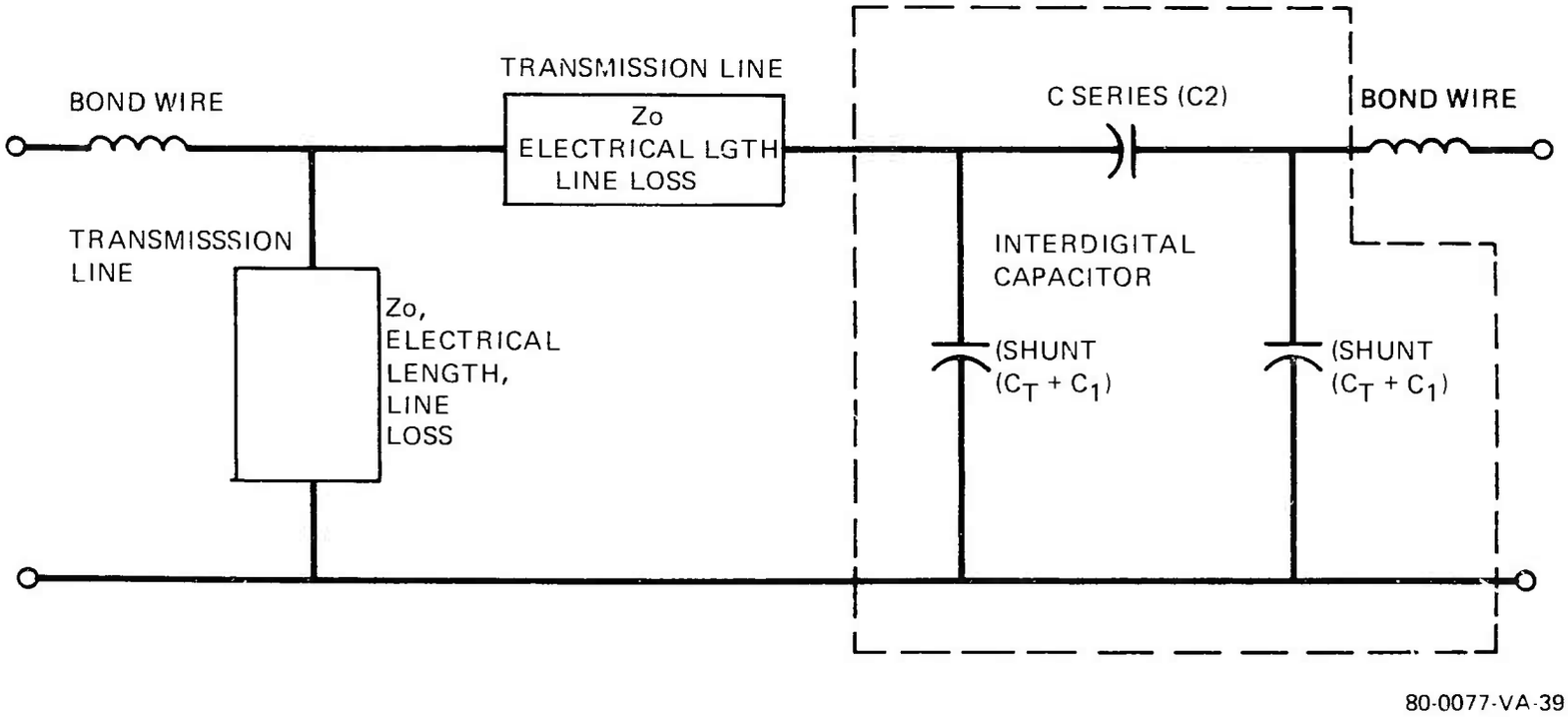

Figure 40. Monolithic Matching Circuit Model for Derivation of Integrated Capacitor Element Values

values of the model were optimized using COMPACT to fit the measured S parameter data. Excellent correlation was found between experiment and theory. For example, a 35-finger capacitor (finger width = 0.0017 in. (4 μ), gap width = 0.00023 in. (6 μ), finger length = 0.013 in.) was found to have a measured series capacitance, C_2, of 0.54 pF and a shunt capacitance, $C_T + C_1 = 0.18$ pF ($C_T = 0.1$ pF, $C_1 = 0.08$ pF). The Alley analysis predicted a series capacitance of 0.47 pF. The coupled-line analysis predicted a series capacitance of 0.54 pF and a shunt capacitance of 0.16 pF. An experiment was also carried out wherein ten trim fingers were bonded to the capacitor. The series capacitance increased to 0.68 pF and the shunt capacitance increased to 0.20 pF ($C_T = 0.1$ pF, $C_1 = 0.1$ pF), thus confirming the theory that both the series and shunt capacitance of the fingers are proportional to the number of fingers as illustrated in figure 39. The Q of the interdigital capacitors was measured using the test resonator shown in the previous report and was found to be 40-55 at 6 GHz. The corresponding calculated Q was 54 at 6 GHz.

4.1.2.1 Inductors for Monolithic Circuits

Compared to the monolithic capacitors described in the previous section which require sophisticated processing technologies, inductors for monolithic circuits are designed and fabricated in a very straightforward manner.

For tuning applications in coplanar circuits, simple one-turn inductors[9] can be used for inductance values up to 2 nH (see figure 41). Similarily, in microstrip circuits, short sections of high-impedance transmission lines serve as inductors and can be modeled exactly. The only precaution for either type is that the metal thickness be adequate, at least 1.5 and preferably 2.0-microns thick, in order to keep Q's high. Q values $\approx$ 80-120 are typical for single-turn inductors at a frequency = 7.5 GHz.

4.1.3 Microstrip Lines on GaAs

During this reporting period, microstrip lines on GaAs have been characterized both theoretically and experimentally. A substrate thickness of 0.004 in. has been used as the standard. This

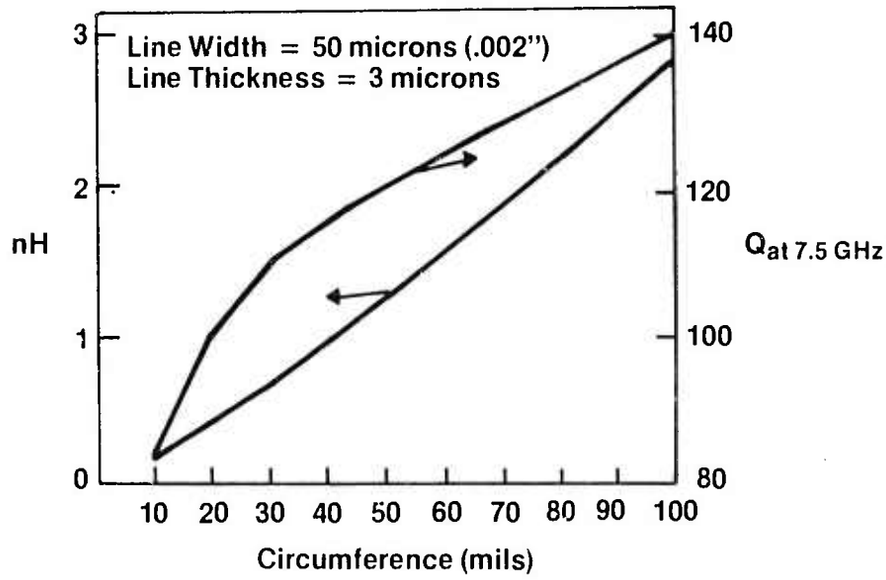

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Figure 41. Inductance and Q of Single Turn Circular Loop

represents a compromise between 1) an even thinner substrate which would be better for thermal impedance and 2) a thicker substrate which would be better for handling and would have lower microstrip line losses.

Figure 42 is a plot of conductor loss vs line width for microstrip transmission lines on 0.004 in thick GaAs. The gold metallization thickness assumed for this calculation is 2.0 microns. The dielectric loss tangent of semi-insulating gallium arsenide has been measured[10] to be ≈ 2 to 3×10^{-4} in the 2 to 12-GHz frequency range, which is nearly identical to that of alumina. Hence, dielectric losses are truly negligible ($\approx$0.01 dB/in) compared to the conductor losses.

In order to experimentally verify the calculated losses, both ring resonators and half-wavelength transmission line resonators have been fabricated on 0.004 in. GaAs and measured. The basic technique used is to lightly couple the resonators to a transmission line and measure the transmission Q (power vs f). Provided the

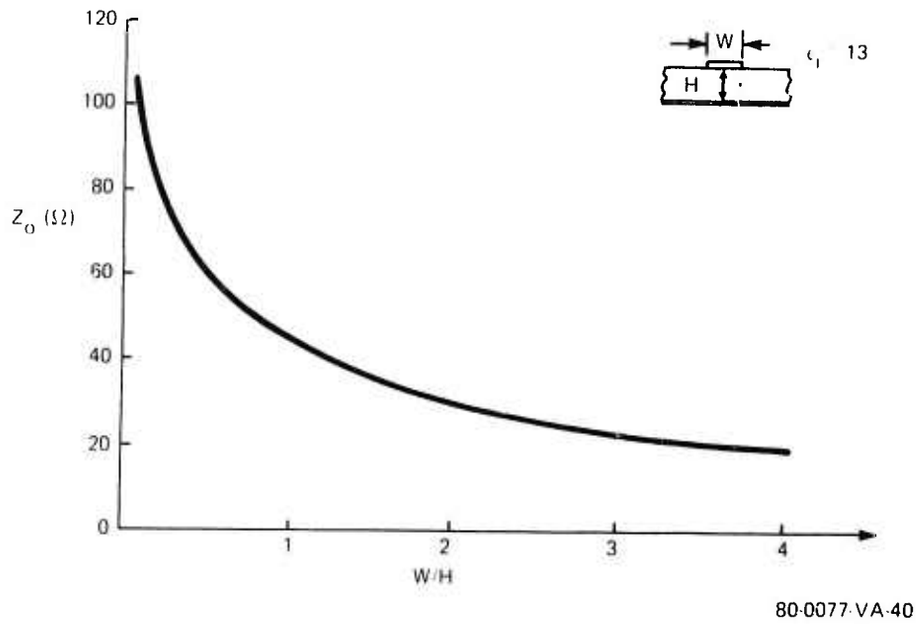

Figure 42. Microstrip Characteristic Impedance vs W/H for GaAs

coupling is very small, the transmission-line loss can be calculated from the familar equation $\alpha = \frac{27.3}{\lambda Q_u}$ dB/inch. Typical Q measurements for 50-Ωlines (0.003 in) at 10 GHz range from 62 for a half wavelength resonator to 78 for a ring resonator corresponding to a loss = 0.9-1.0 dB/in. This compares favorably with the theoretical value of 0.85 dB/in, as predicted from figure 43.

4.2 NARROW-BAND AMPLIFIER DESIGN

4.2.1 Introduction

During the past year, four different 10-percent bandwidth monolithic amplifiers, shown in figure 36, have been designed and tested. Three have been coplanar designs and the last and current design is a microstrip version.

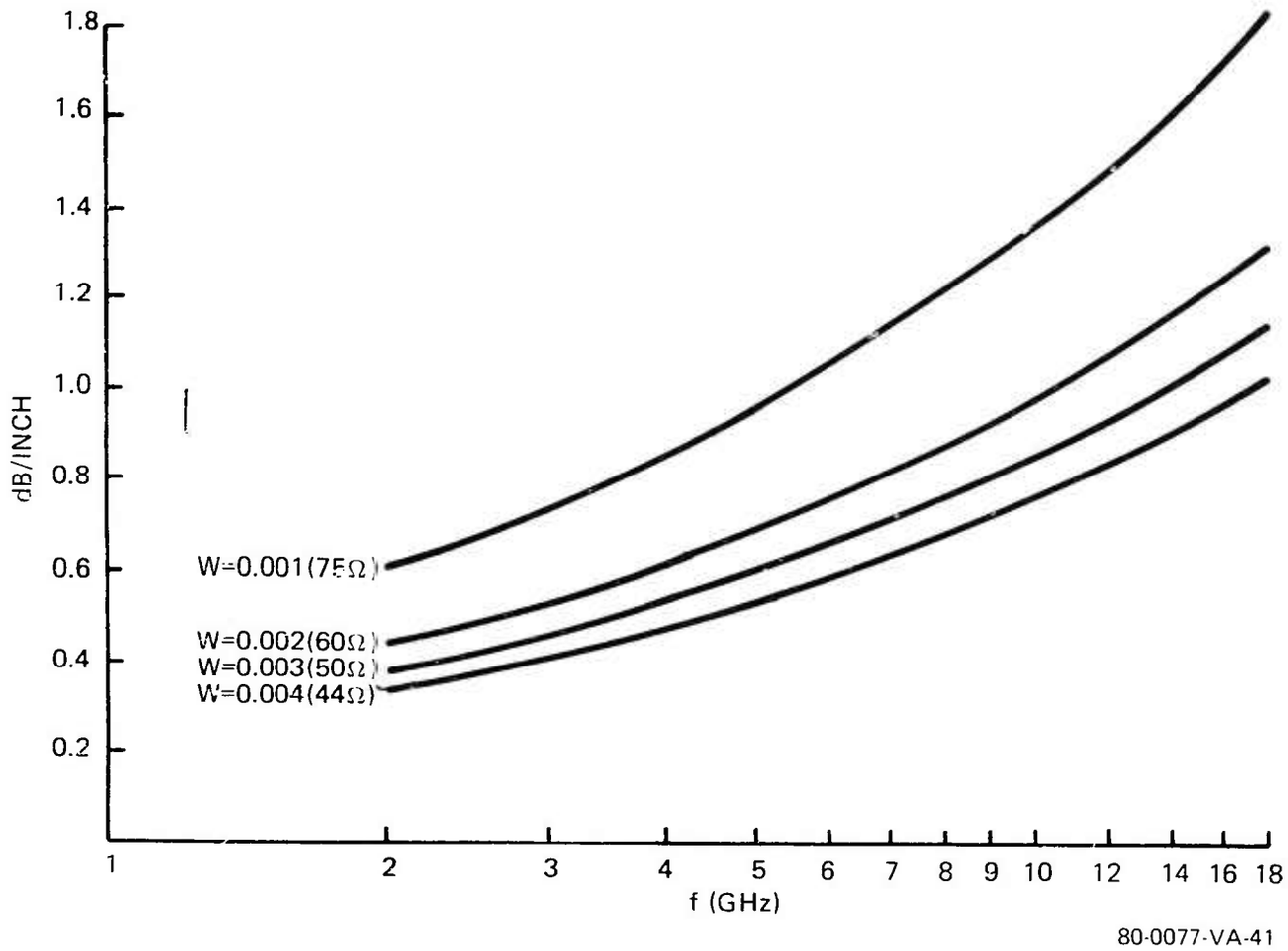

Figure 43. Conductor Loss for Microstrip Lines on 0.004-in. GaAs

The basic small-signal design procedures for these amplifiers is outlined below.

1. Measure device S parameters.

2. Using computer optimization routine, calculate FET model parameters.

3. Using AMPSYN, calculate input and output networks subject to any constraints and draw circuit masks.

4. Predict amplifier response using computer analysis routine.

For designing large-signal amplifiers, this procedure is modified to include actual measurements of optimum-load impedance for maximum power output. This information is then used to design the output-matching network.

In the next two sections, a typical amplifier design is illustrated and measured amplifier results are presented.

4.2.2. FET Characterization

Characterization of the discrete FET's includes both small-signal S parameter measurements plus power-saturation measurements as described earlier in section 3.3.3.4. Good examples of this design procedure are the amplifiers (both coplanar and microstrip) designed using Run 28A data. Run 28A is the first directly-implanted run which yielded significant output power.

Run 28A was characterized by a large number of good devices (from the standpoint of output power) and two very good devices. A typical P_{out} vs P_{in} curve for a 1200-μ FET is shown in figure 44. Note that the power output is +26 dBm at $\approx$ 3 dB associated gain (0.33 W/mm); however, the small-signal gain is low, only 4.6 dB. The best device from this run, 28A-D5-3D (900 μ) exhibited a power per unit periphery $>$ 0.46 W/mm with an associated gain = 3.7 dB at 418 mW out, as shown in figure 45. As mentioned earlier, measurements of gate length on this run yielded values between 1.5 and 1.75 microns due to a mask error as compared to the nominal design value of 1 micron. This increased gate length causes the input gate capacitance to be proportionately higher and the gain to be lower than anticipated.

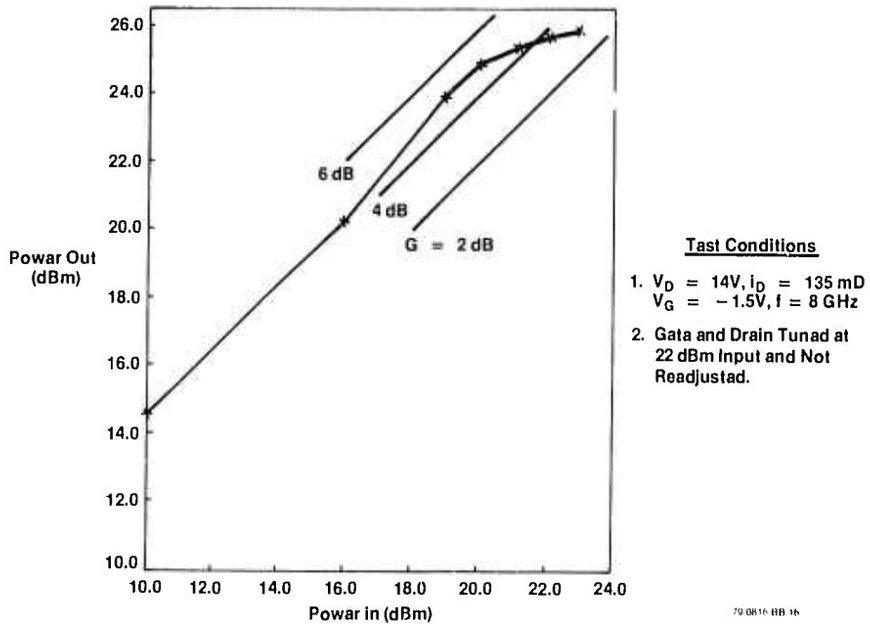

Figure 44. P_{out} vs P_{in} for Device 28A23-3E

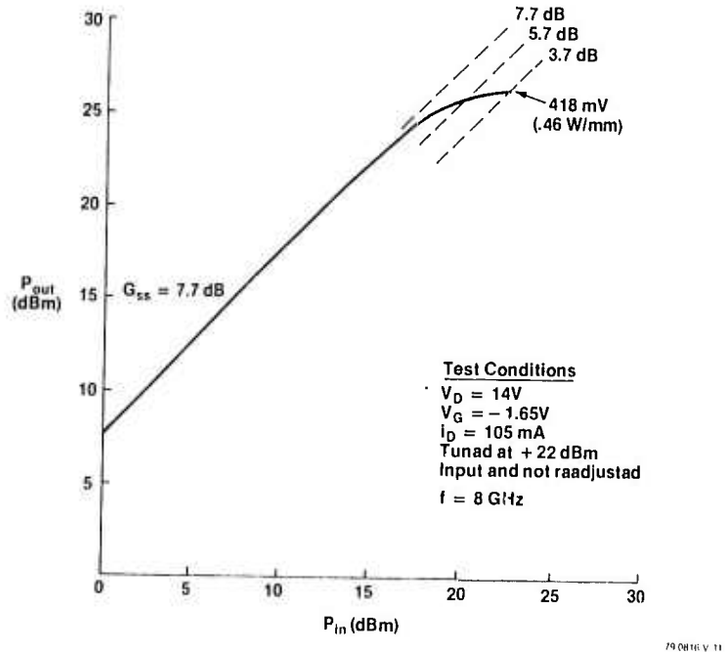

Figure 45. P_{out} vs P_{in} for Device 28A-D5-3D (900 μ)

Since Run 28 was the first directly-implanted run which yielded ≈10 discrete FET's with significant output power, it was decided to create two new designs based on Run 28 FET parameters. Four 900-μ FET's were measured on the network analyzer and the resultant S parameters were averaged to create a composite set of S parameters. The comparison between the individual and averaged value is shown in figure 46. The small-signal model corresponding to the average 28A S parameters is shown in figure 47. This model formed the basis for the two new amplifier designs discussed in the next section.

4.2.3 Coplanar Lumped-Element Amplifier

Using the average Run No. 28 FET parameters illustrated previously, a single-tuned lumped-element amplifier, centered at 7.5 GHz, was designed (figure 48). The output circuit was designed to transform from the 50-Ω load impedance to $\approx R_D/2$ (½ the drain resistance of the small-signal model). The calculated small-signal frequency response of the amplifier for various element Q's is shown in figure 49. Due to the fact that the amplifier was designed to operate in the large-signal region, the maximum available gain of 6.2 dB at 7.5 GHz is not obtained for the lossless case. Under large-signal conditions, the gain of the amplifier will drop ≈3 dB from that shown in figure 49. While this may seem low, it should be remembered that this is for the case where the gates are ≈1.5μ instead of 1 micron.

A twenty-trial Monte Carlo analysis was also performed for the amplifier. In this anlaysis, all lumped elements (Q's of 50 were assumed) are varied at random within a ±10 percent range. The small-signal gain at 7.5 GHz under worst-case conditions decreased from its nominal value by 0.6 dB.

4.2.4 Microstrip Lumped-Element Amplifier

A single-tuned microstrip amplifier was also designed using short sections of high-impedance transmission lines as inductors as shown in figure 50. This configuration is better from a heat dissipation standpoint due to the fact that the metal ground plane on the back of the chip can be soldered to the copper

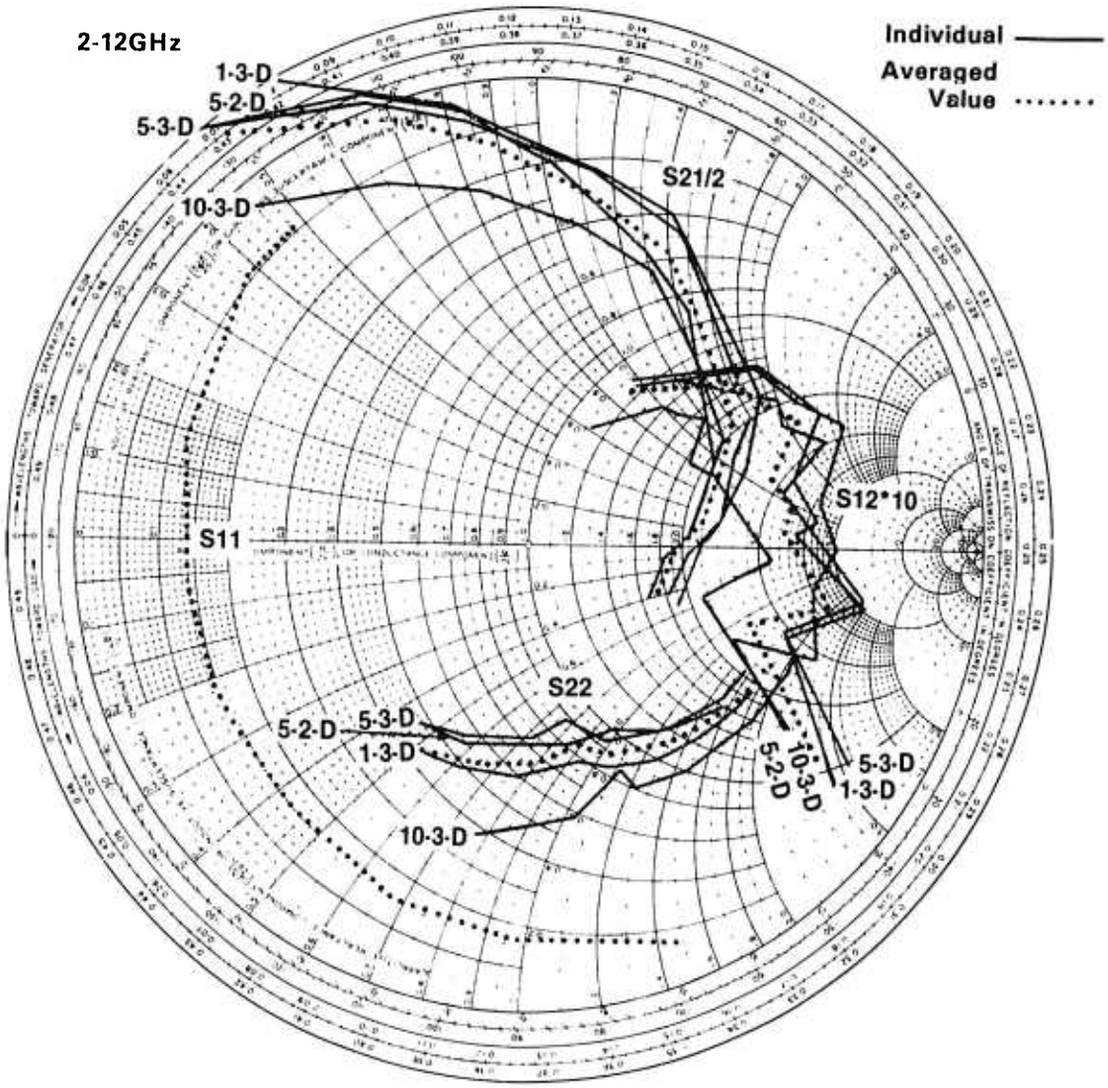

Figure 46. Individual and Averaged S Parameters for 900μ FET's

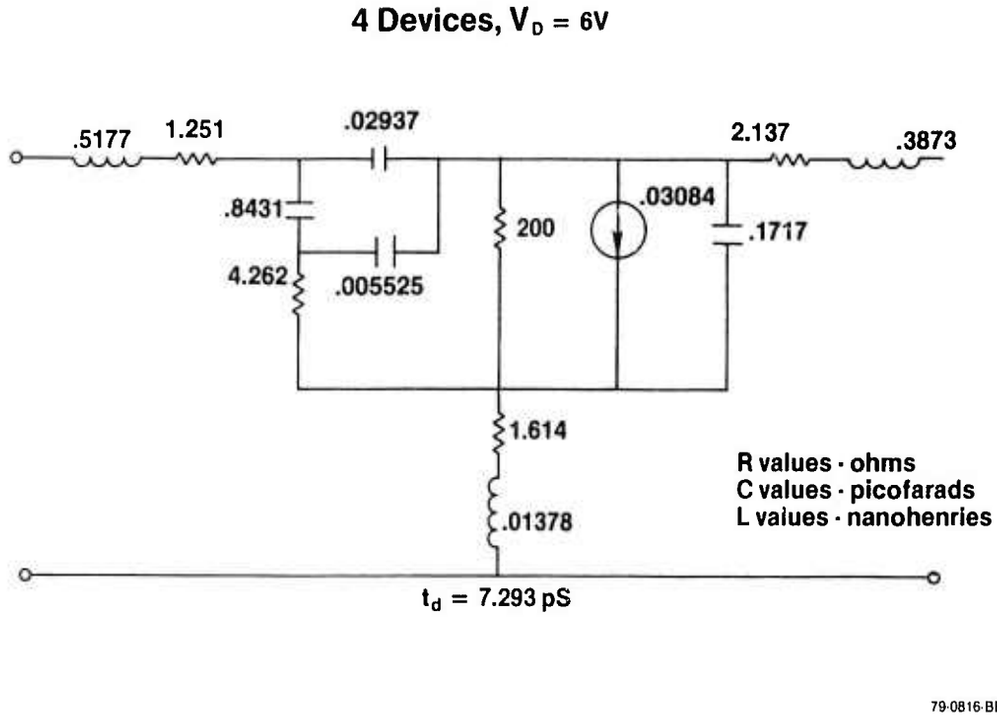

Figure 47. Average 900μ FET Model for Run 28A

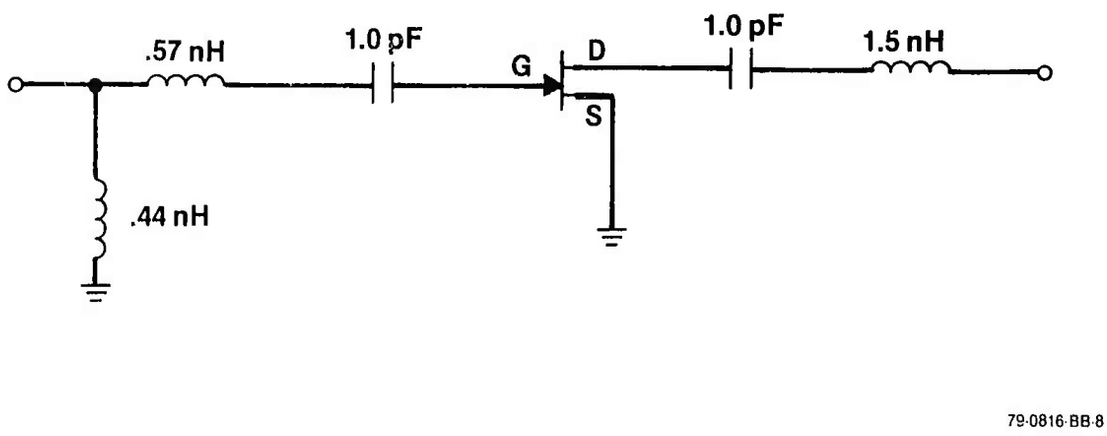

Figure 48. Schematic for Coplanar Amplifier Using Run 28A Average FET Values

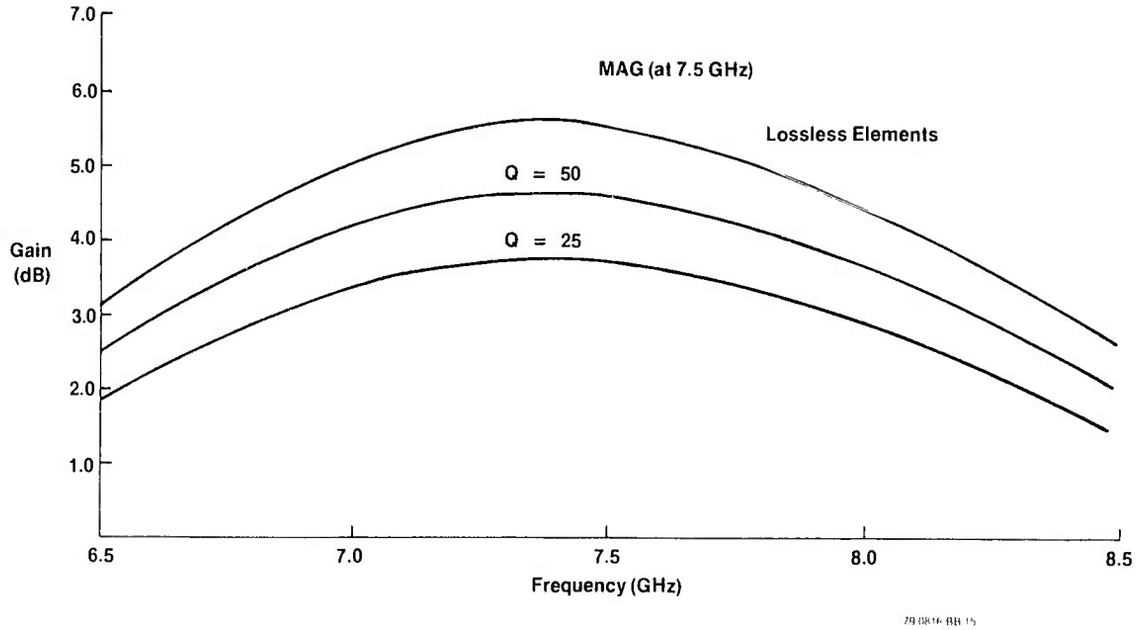

Figure 49. Calculated Small Signal Gain for Coplanar Amplifier

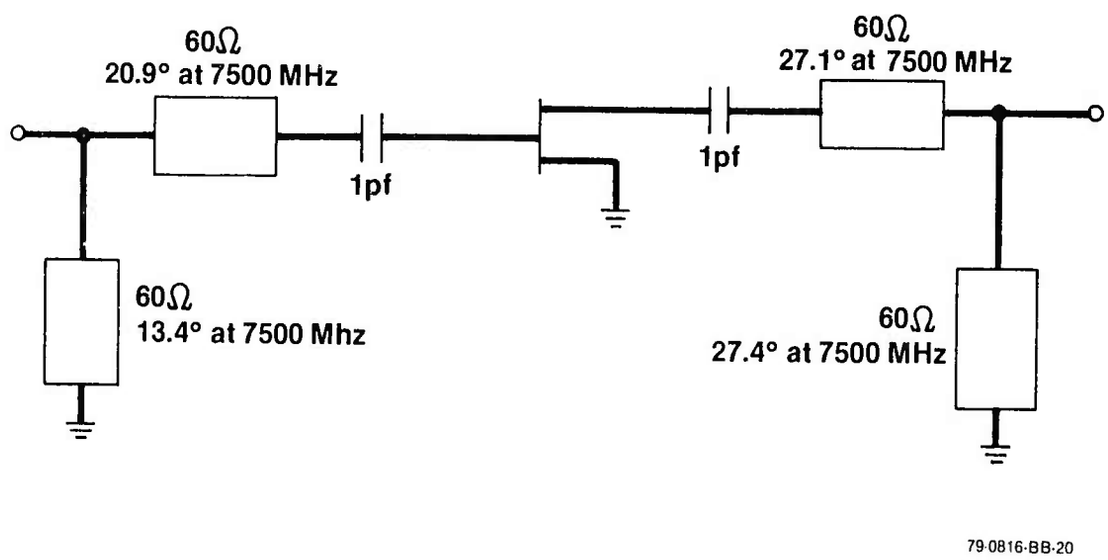

Figure 50. Microstrip Amplifier Schematic

heat sink and, in addition, facilitates the future use of vias for minimizing common-source impedance.

The calculated small-signal and large-signal gains are shown in figure 50. Figure 51 shows the maximum available gain of the FET under small-signal conditions along with the effects of adding the interdigital capacitors, Q=41, lossless transmission line, and lossy transmission line matching networks (α= 1 dB/in). Again, the maximum available gain of the FET including the interdigital capacitors is not obtained with the lossless case because the amplifier is tuned for power conditions. Because the amplifier chips are thinned to the final thickness of 0.004 in. by etching, some variation in the final thickness can be expected, which changes the microstrip geometry accordingly. To check the importance of this effect, the amplifier-gain response was calculated for substrate thickness of 0.0035 in. and 0.0045 in. and compared to the nominal response for 0.004 in. thickness. The responses are shown in figure 52. As can be seen, these substrate thickness variations have only a minor effect on gain response, shifting the center frequency by $\approx$200 MHz and causing a gain variation of $\pm$ 0.15 dB from nominal.

4.2.5 Measured Amplifier Results

As mentioned in section 6.2.1, four different amplifiers have been designed and evaluated during this reporting period. A major problem in the amplifier evaluation area has been the rapid evolution in the discrete FET's used in the amplifiers. This evolution frequently means that, from the inception of an amplifier design until it is actually fabricated and tested (typically 1-1 ½ months), the discrete FET characteristics will have changed to the extent that the circuit no longer is exact for the new FET charactetistics, resulting in input and output match characteristics which are shifted in frequency and/or have higher voltage standing wave ratio than designed. Nonetheless, many good amplifiers have been fabricated and evaluated. A summary of amplifier characteristics for seven different runs is shown in table 7. A short discussion of some of the more important runs follows.

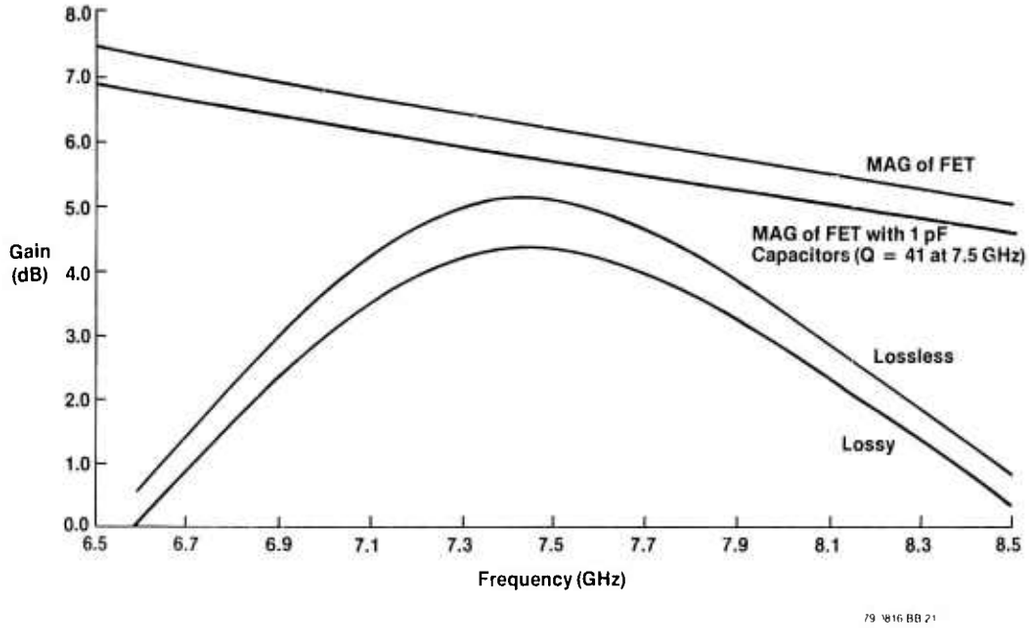

Figure 51. Loss Effects on Microstrip Amplifier Response

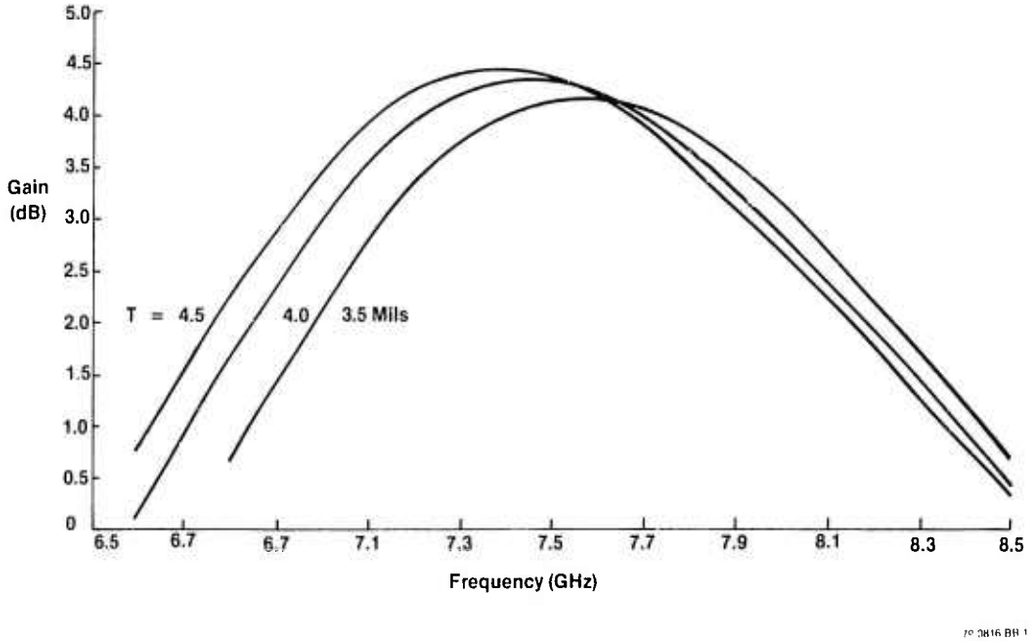

Figure 52. Effect of Substrate Thickness Variations on Predicted Response

TABLE 7

SUMMARY OF TEN-PERCENT BW AMPLIFIER PERFORMANCE

RUN NO.	AMPLIFIER DESIGN NO.	SMALL-SIGNAL GAIN	MAX POWER OUT	COMMENTS
21	1	-3 dB		High Contract-Resistance Thin-Circuit Metallization Gate Length = 1.5-2.0 micron
24	1	6 dB at 7.1 GHz	small-signal design	Confirmed Amplifier Design Techniques
27	1	– – –	– – –	High capacitor leakage due to incomplete etching of epi
28	1	3.5 dB at 6.0 GHz	100 mw saturated	First Directly-Implanted Run, Gate Length = 1.5-1.75 micron
IC2D	2	7 dB at 6.5 GHz	30-50 mw saturated	Experimental I^2 run with Deep Oxygen Implant
IC4A	3	6.9 dB at 7.15 GHz	266 mw with 3.5 dB gain	Output circuit tuned
IC7 ATL2	Microstrip	5.5 dB (MAG = 7.5 dB) F = 7.5 GHz	400 mw with 3.9 dB gain	

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Run 24 was the first run where good amplifier performance was obtained. The amplifiers initially exhibited high gain (10 dB), but were found to be working in an injection-locked oscillator mode. When the oscillations were quenched and the effective length of the bias lines was shortened, 6 dB gain at 7 GHz was realized as shown in figure 53. The 1-dB bandwidth for the amplifier was 80 MHz. Input and output VSWR match, as shown in figure 53, confirmed that the design of the matching circuits was basically correct except for a slight offset in center frequency. These amplifiers were designed using the device small-signal S parameters at bias conditions of V_{DS} = 8 V and I_{DS} = 125 mA and hence work best under small-signal conditions. In fact, under large-signal conditions, power output at the 1-dB compression point was only 13 dBm (saturated P_{out} = +17.5 dBm) due to improper match and inadequate heat sinking.

Run 27A fabricated on epitaxial GaAs produced very good discrete devices (see previous section 3), however, the amplifiers exhibited 3 to 8-dB loss. It was ascertained that the epi layer had not been removed completely in the area of the capacitors leading to very leaky and, hence, lossy capacitors.

Run 28A was the first directly-implanted run where the discrete FET's had significant output power. A typical amplifier gain response from Run 28A is shown in figure 54. Note that the small-signal gain is low, only 3.5 dB; however, considering that the typical discrete FET exhibited a small-signal gain of 4.5-5.5 dB and allowing for circuit and mismatch losses of 1.0-1.5 dB, this value is not unreasonable. Maximum power output of the amplifiers was typically only 50-100 mW due to the fact that the circuits were designed for small-signal gain rather that power match, plus the fact that the FET S parameters were different from the values assumed during the design, the design having been based on Run 21 measured S parameters. IC4A amplifiers were the first coplanar power-matched amplifiers which yielded significant ouput power. With output circuit tuning, 266 mW output power was obtained with 3.5 dB associated gain.

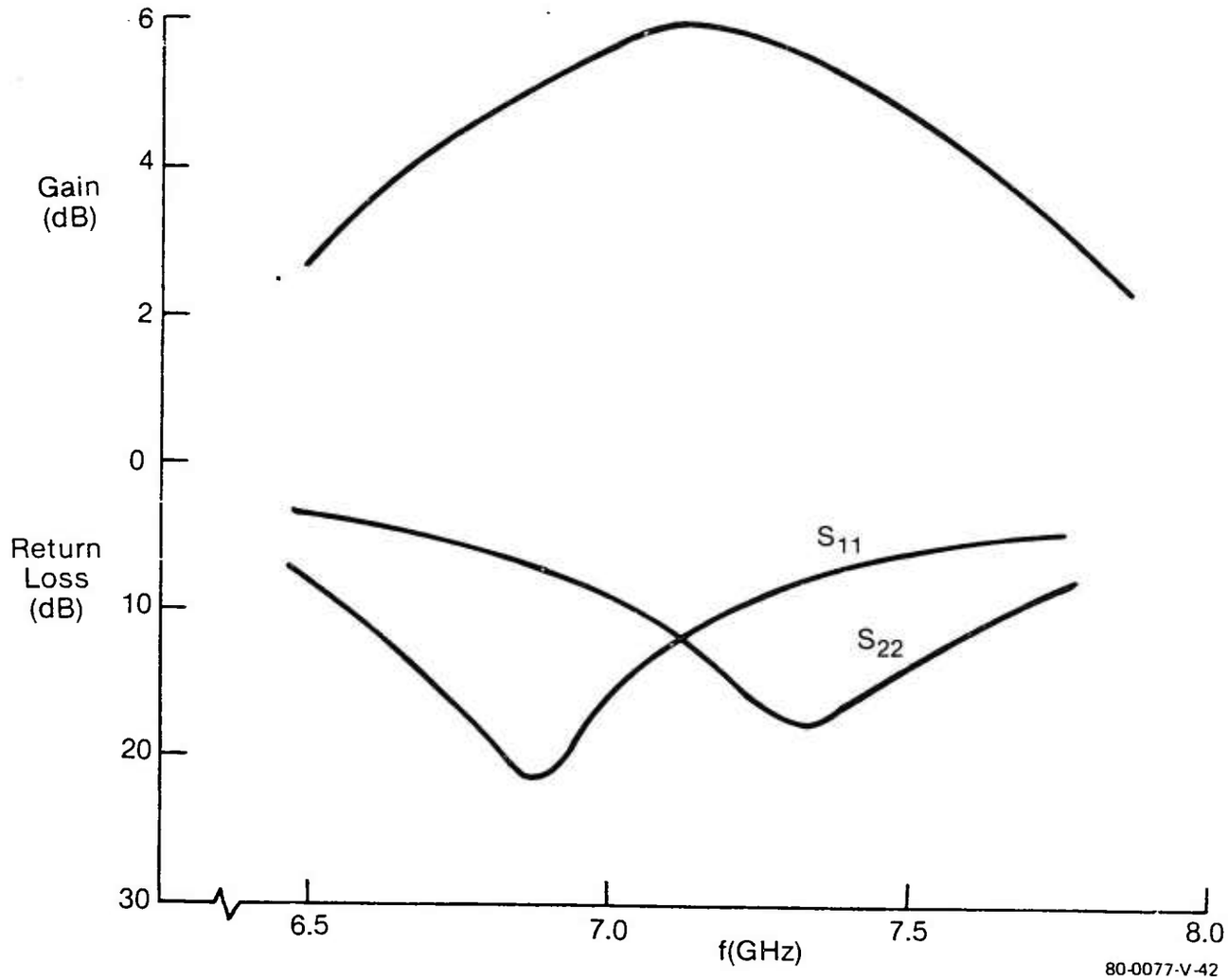


Figure 53. Gain and Match vs Frequency for Run 24 900μ FET

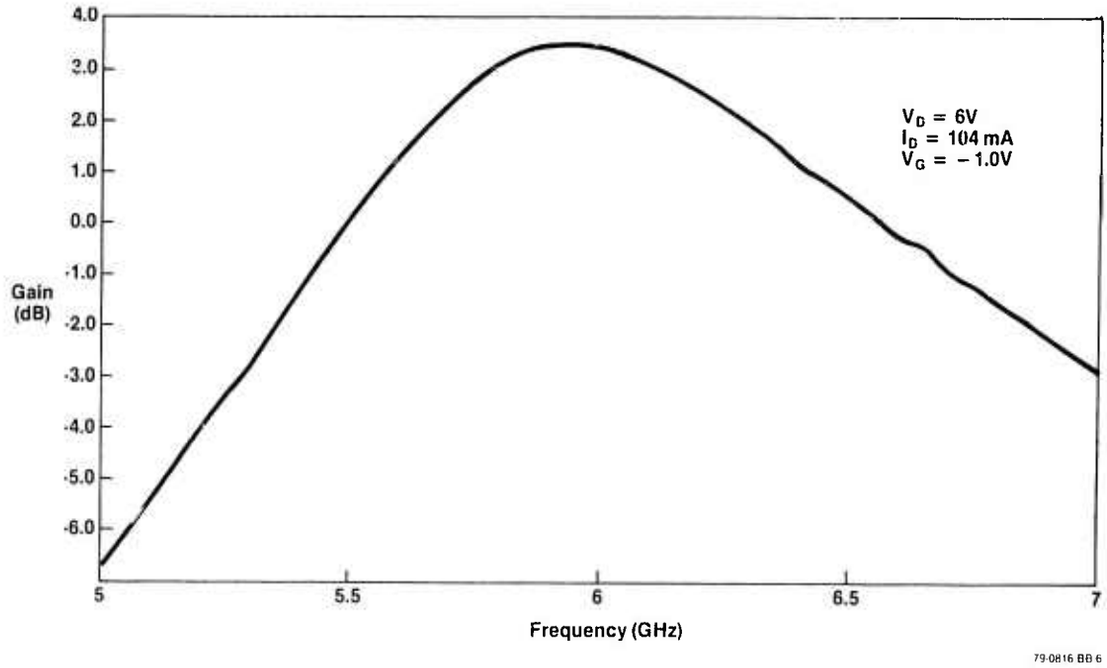


Figure 54. Gain vs Frequency

The microstrip design was evaluated with Run IC7. Output tuning was required, again as the result of the improved FET's which had different S parameters than those used in the original design. When tuned, 400 mW output power with 3.9 dB associated gain was obtained, as shown in figure 55. Allowing for 1-dB insertion loss in the output network, this means that the 900μ FET was delivering $\approx$500 mW (0.55 W/mm) which is consistent with measurements made on discrete FET's from this run.

With the completion of tests on narrow-band designs, work in the next reporting period will concentrate on octave-band designs, both single and multistage.

4.3 WIDE-BAND AMPLIFIER STUDIES

4.3.1 Introduction

In the early runs of both epitaxial and directly ion-implanted FET's, the S parameter measurements, and the resultant models created therefrom, exhibited low output drain resistance, R_D, and a corresponding low output power per unit periphery, typically 0.3 W/mm. As an example, the average Run 28A 900-μ FET model, as

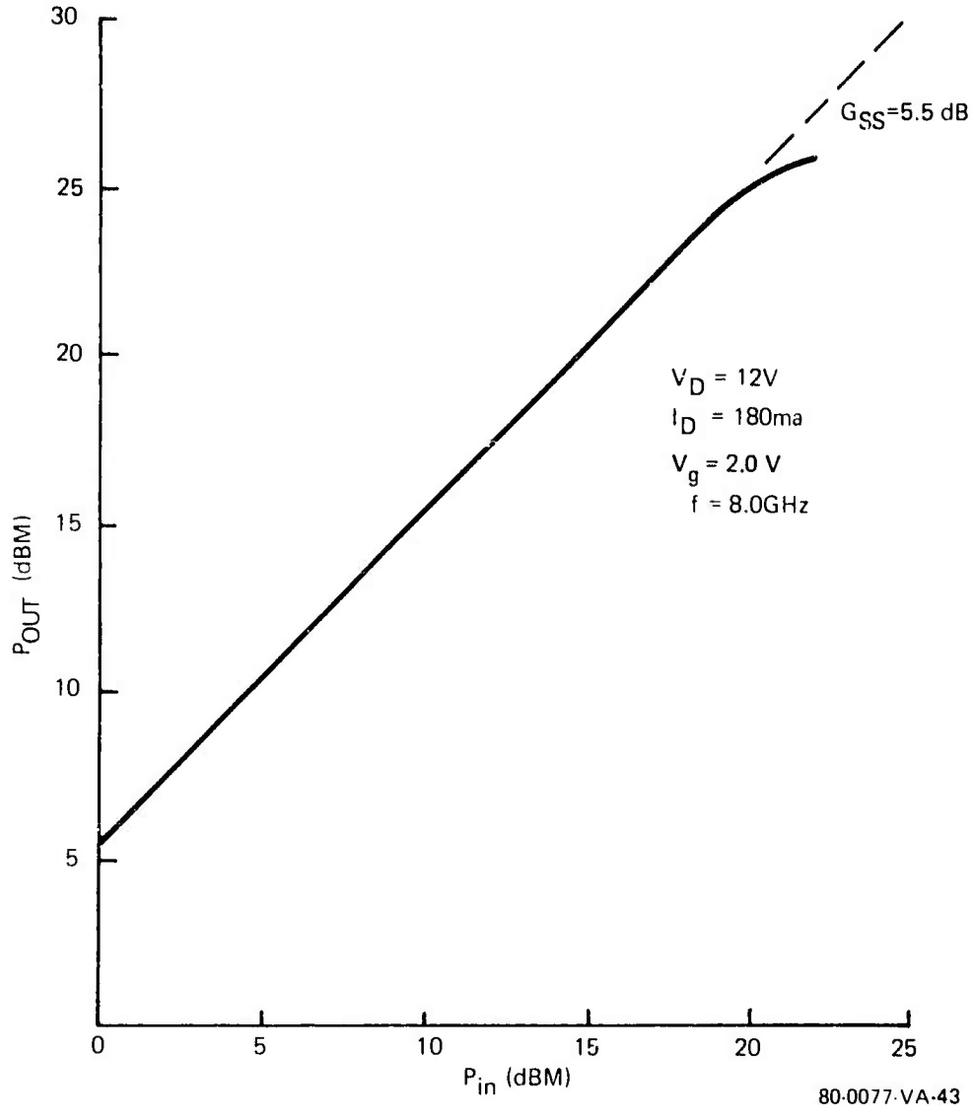


Figure 55. P_{out} vs P_{in} for IC7 Monolithic Amplifier

depicted earlier in section 4.2.2, figure 47, had a drain resistance of $\approx 200\,\Omega$, while a typical commercial FET exhibited $\approx 300\,\Omega$ drain resistance (scaled to the same periphery). This lower R_D and associated output power raised two important questions:

1) Was there a substrate conduction mechanism that was creating a second drain to source conductance path with a resultant lowering of R_D?

2) If power/unit periphery was limited to 0.3 W/mm, could a practical two-stage, octave bandwidth amplifier be designed?

Both of these questions were studied in some depth and the results are described in the following sections.

4.3.2 Substrate Conduction Studies

In postulating a substrate conduction mechanism for the lower R_D, it was noted that the FET's could be pinched off well; hence, if there were a substrate conduction mechanism, it must be ac coupled. There were, in fact, reports in the literature[6] of such a mechanism, hence it was decided to conduct an experiment to confirm or refute this idea.

Accordingly, the S parameters of a 1200-μ FET from Run 28A were measured at progressively lower frequency ranges all the way down to 0.5 MHz. For each frequency range, the FET model was created. The resulting models are shown in figure 56. As can be seen from this figure, the model parameters are essentially constant down to 0.5 MHz, thus refuting the idea of an ac-coupled substrate conduction mechanism.

In a related experiment, the FET model was studied as a funtion of drain voltage with drain current held constant.

The results of this experiment are shown in figure 57. It should be noted that, while the g_m of the FET is essentially constant over a drain voltage range from 3 up to 14 volts, the drain resistance varies by almost a factor of 3:1, from 99 Ω up to 291 Ω. This is in agreement with what one would expect from the slope of the I_D vs V_D characteristics and points up the importance of measuring the FET parameters at the drain voltage at which the FET will ultimately be used in order to be able to correctly design the output matching circuit.

FET Model for Device 28A-23-3E (1200μ) as Function of Frequency

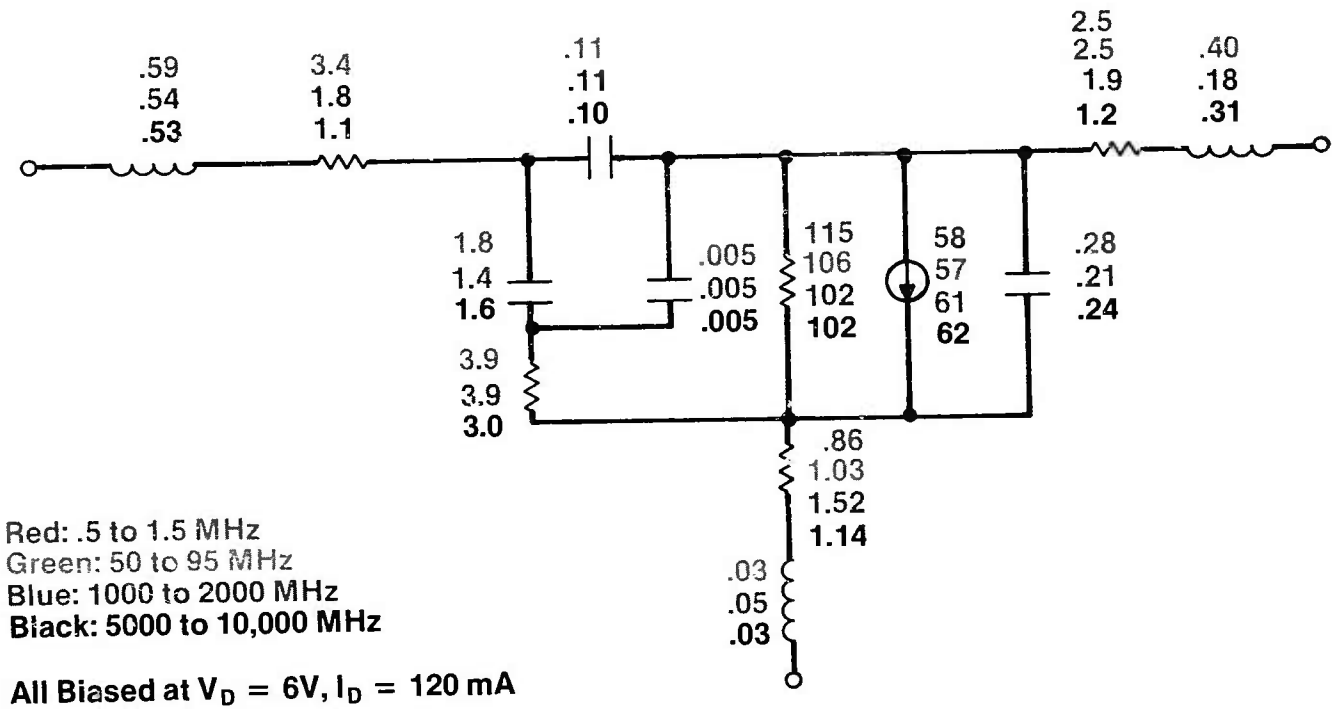


Figure 56. FET Model as a Function of Frequency

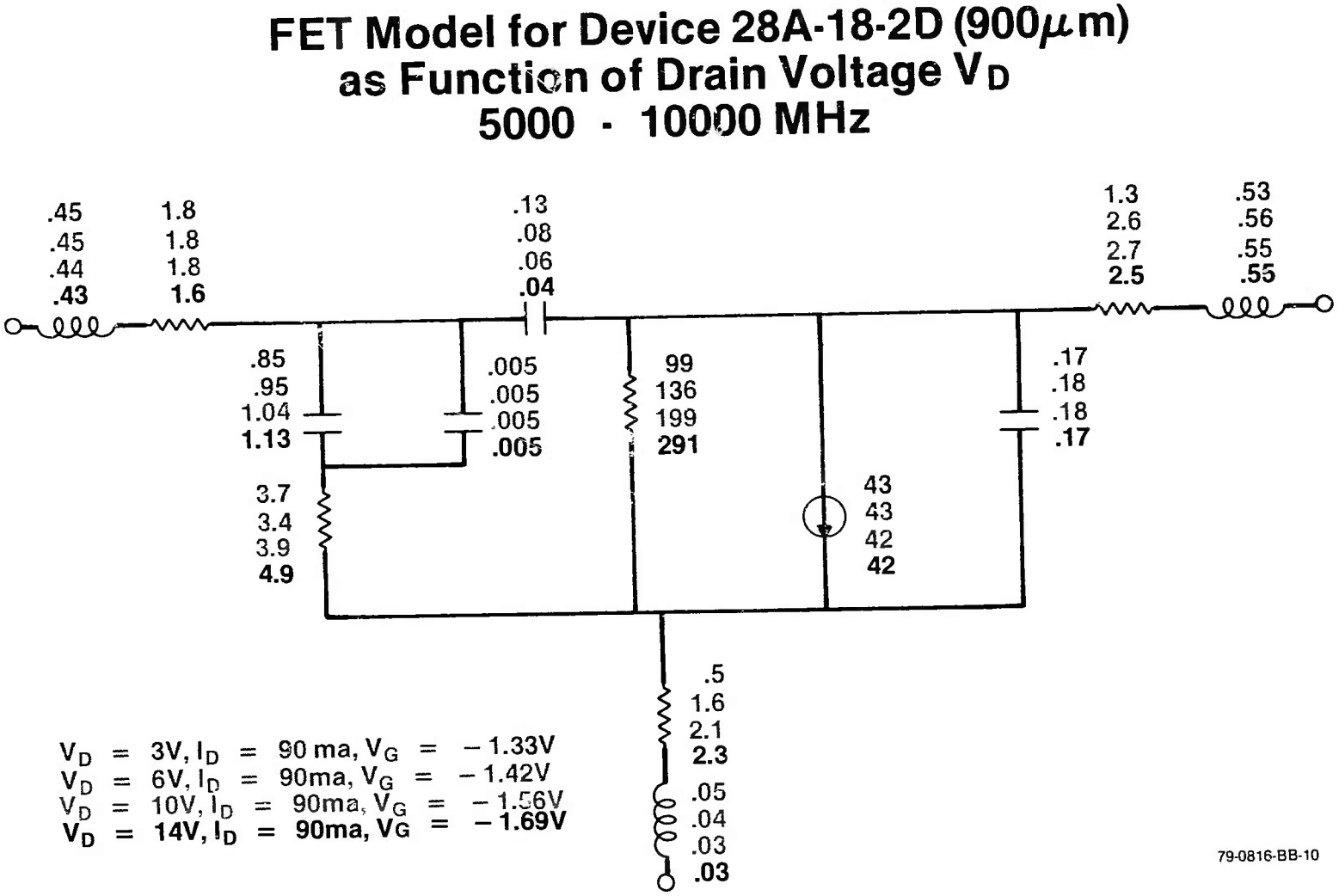


Figure 57. FET Model as a Function of Drain Voltage

4.3.3 Power/Unit Periphery Analysis of Two-Stage Amplifiers

In order to answer question No. 2 posed in the introduction i.e.; can a practical two-stage octave bandwidth amplifier be made with FET's with low W/mm output, three different FET output-power capabilities were considered; 0.3, 0.5, 0.7 W/mm, and two-stage amplifiers were designed for each case.

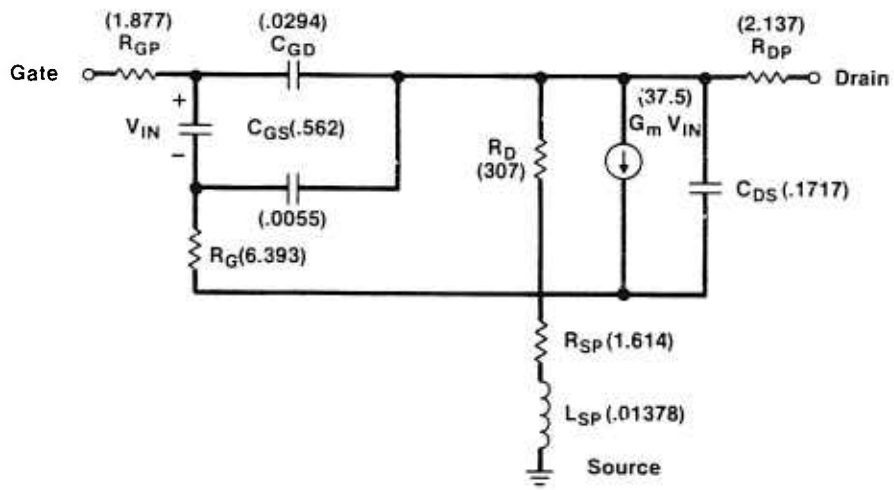
The models used are shown in figure 58. The basic model for all designs is the 900-μ run 28A model discussed earlier except that the input circuit parameters have been modified to correspond to a 1-micron gate length instead of the measured 1.5-micron gate length. Specifically, the input circuit resistance was increased by the factor $\frac{3}{2}$, while the input capacitances were decreased by a factor of $\frac{2}{3}$. In order to model the different output powers/mm the output resistance for the 0.5 W/mm and 0.7 W/mm cases were obtained by scaling R_D for the 0.3 W/mm case by factors of $\frac{5}{3}$ and $\frac{7}{3}$, respectively. Likewise, all parameters have been scaled for gate width.

Examining first the 0.5 W/mm case, as shown in figures 59 and 60, it can be seen that a very reasonable design results. All of the element values are realizable and a gain = 10 dB$\pm$0.8 dB is achieved over the 5 to 10-GHz band for matching element Q's = 50.

On the other hand, the 0.3-W/mm amplifier, as shown in figures 61 and 62 has serious problems. If one attempts to design the amplifier to operate over the full octave, then only 3 dB gain is obtained. If one compromises on bandwidth, then 5-6 dB gain can be obtained from 5 to $\approx$8.5 GHz. In addition, several inductor and capacitor values are large, i.e.; $>$2 pF or 2 nH, making the design difficult to implement.

The 0.7-W/mm design, as one would expect produces even better gain (12 $\pm$ 1 dB) as shown in figures 63 and 64. Several element values are large, making this design difficult; however, it is possible that another interstage topology might alleviate this problem.

This 0.5-W/mm design was also converted to a microstrip design as shown in figures 65 and 66. As can be seen, the design is realizable and has approximately the same response as the coplanar amplifier.



Values in Parentheses Apply to 0.5W/mm 900μm FET

	First Stage						Second Stage					
	Gate Periphery (μm)	C_{GS} (pf)	R_G (Ω)	G_m (m℧)	R_D (Ω)	C_{DS} (pF)	Gate Periphery (μm)	C_{GS} (pF)	R_G (Ω)	G_m (m℧)	R_D (Ω)	C_{DS} (pF)
.3W/mm	1500	0.937	3.836	51.3	120	.286	4000	2.5	1.439	136.8	45	0.763
.5W/mm	900	0.562	6.393	37.5	307	0.1717	2400	1.5	2.397	100	115	0.458
.7W/mm	600	0.375	9.59	25	644.7	0.114	1800	1.124	3.2	75	214.9	.3434

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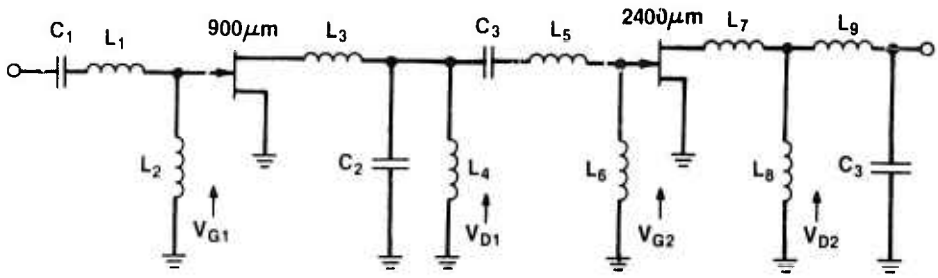
Figure 58. Models Used for Two-Stage One-Watt Amplifier Designs



Element Values for 10 dB Design

	nH		pF
L_1	0.84	C_1	0.36
L_2	0.50	C_2	1.42
L_3	1.42	C_3	0.65
L_4	0.77		
L_5	0.69		
L_6	0.47		
L_7	0.26		
L_8	1.41		
L_9	0.33		

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Figure 59. 0.5-W/mm Two-Stage Monolithic Coplanar FET Amplifier

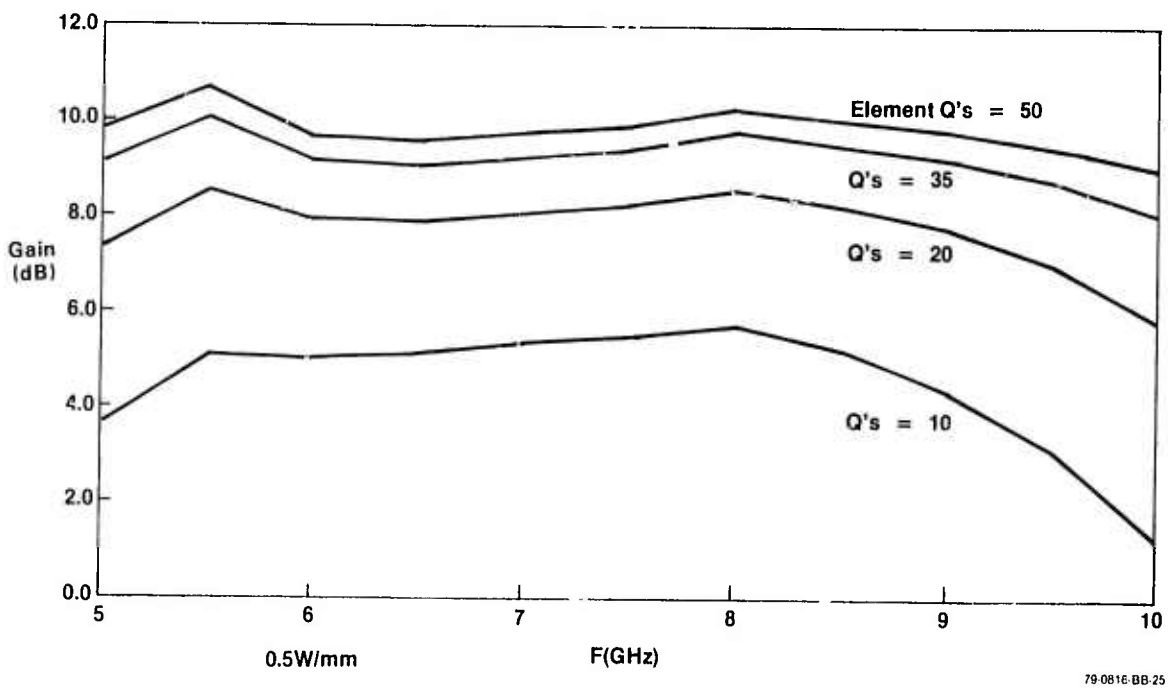
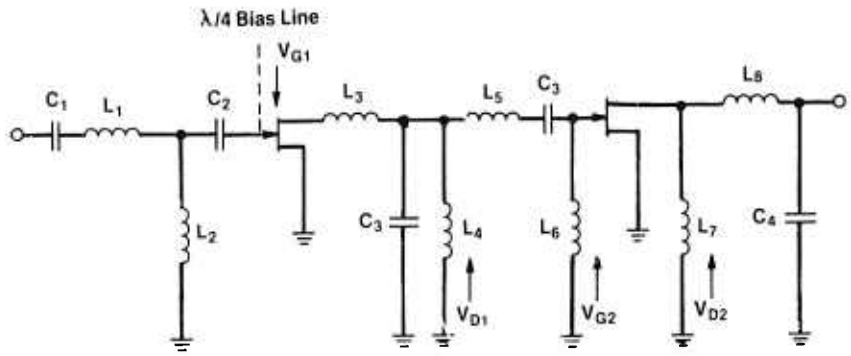


Figure 60. Calculated Gain for Two-Stage 0.5-W/mm Monolithic Coplanar Amplifier



6 dB Design	nH		pF	3 dB Design	nH		pF
L_1	1.91	C_1	0.40	L_1	1.26	C_1	0.38
L_2	0.69	C_2	2.07	L_2	0.47	C_2	2.02
L_3	0.72	C_3	1.13	L_3	0.88	C_3	1.20
L_4	2.28	C_4	0.59	L_4	2.40	C_4	0.52
L_5	0.68			L_5	0.72		
L_6	0.22			L_6	0.28		
L_7	0.57			L_7	0.61		
L_8	0.51			L_8	0.47		

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Figure 61. 0.3-W/mm Two-Stage Monolithic FET Coplanar Amplifier

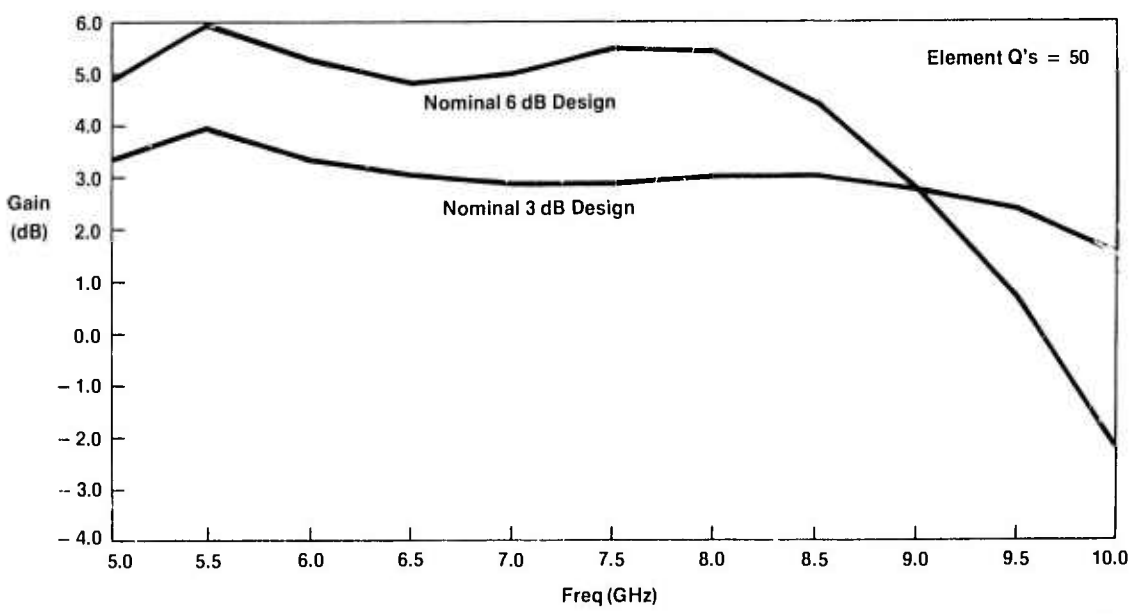

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Figure 62. 0.3-W/mm Two-Stage FET Amplifier Response

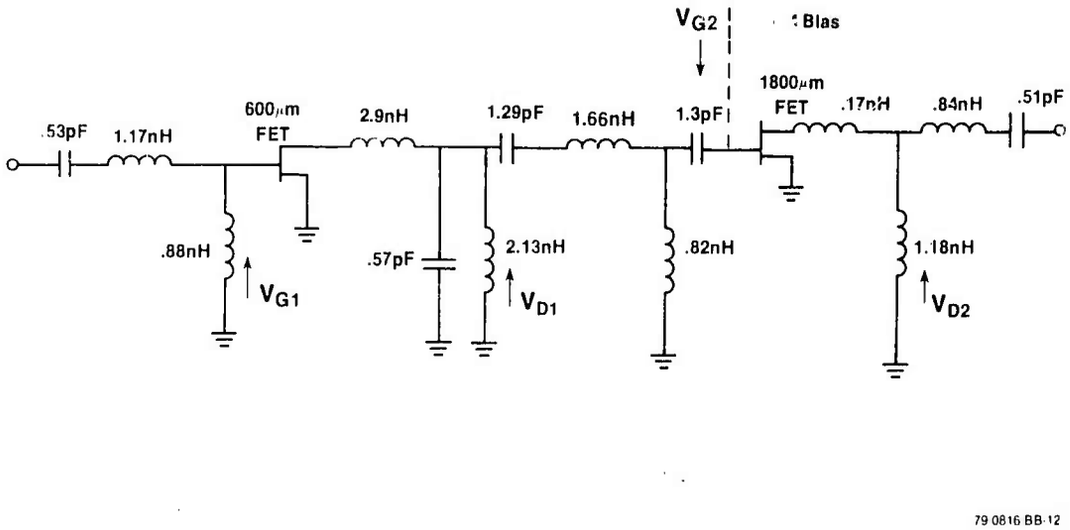

Figure 63. 0.7-W/mm Two-Stage FET Amplifier

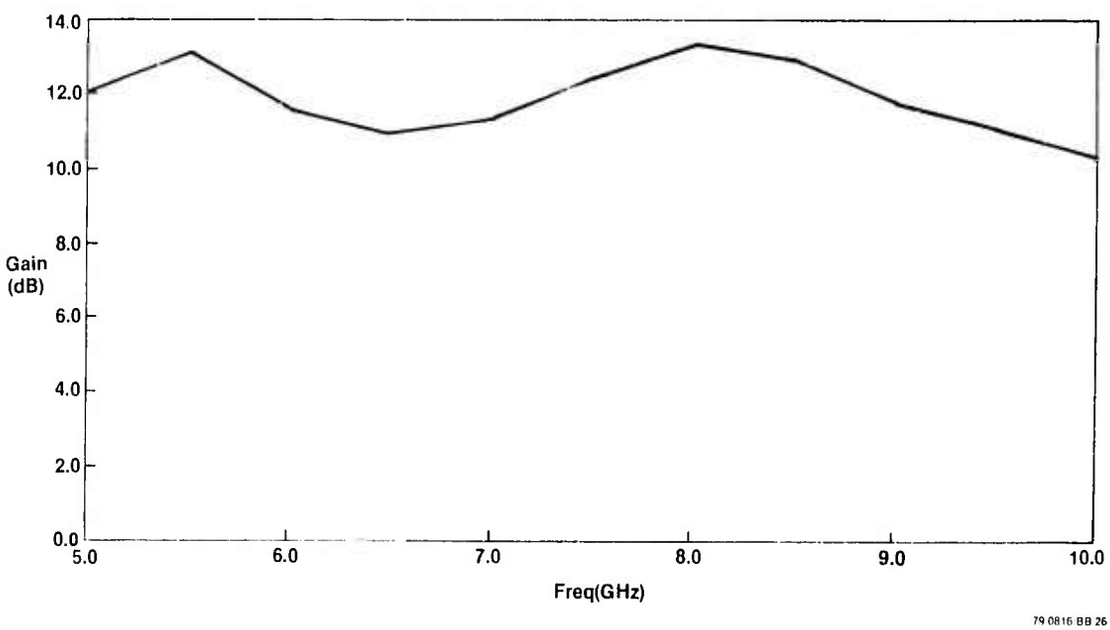

Figure 64. Calculated Gain for Two-Stage 0.7-W/mm Monolithic Coplanar Amplifier

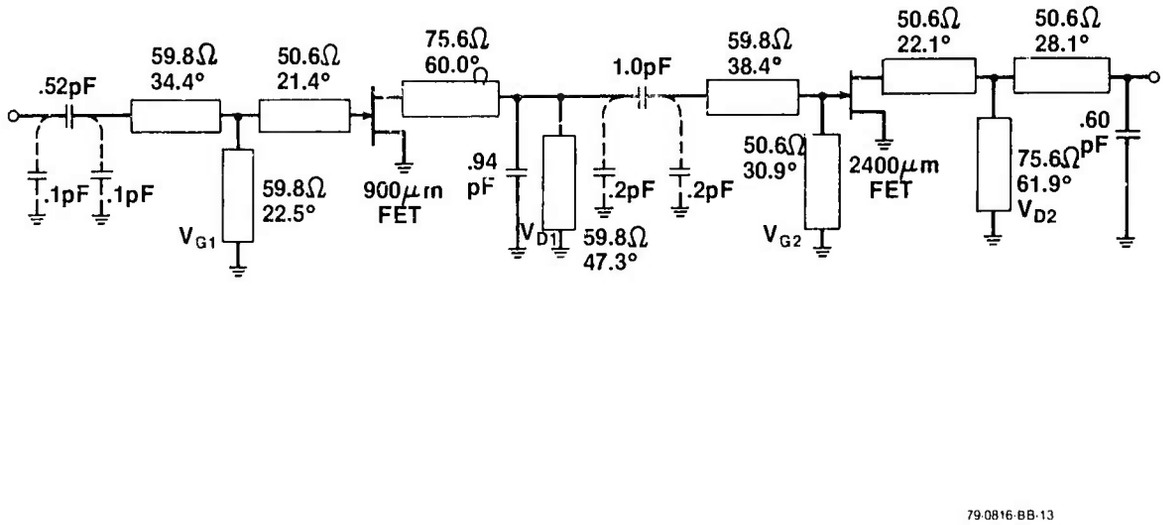

Figure 65. 0.5-W/mm Two-Stage FET Amplifier (Microstrip Version)

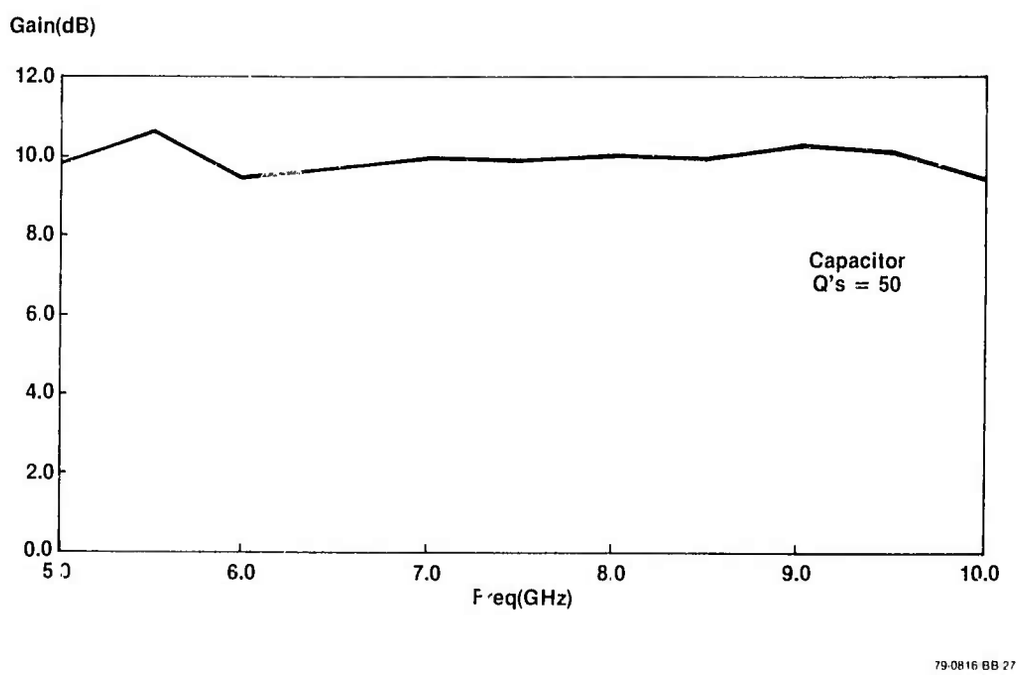

Figure 66. Calculated Gain for Two-Stage 0.5-W/mm Monolithic Microstrip Amplifier

4.3.4 Two-Stage Amplifier Layout

A circuit mask layout was created for the two-stage 0.5-W/mm coplanar design, as shown in figure 67. However, this layout was not committed to a mask since, during this time period, significant design changes were being made in the basic FET which would ultimately lead to a FET with much different model parameters than the 28A model used for the above designs. Specifically, the channel doping density was gradually increased to 1.2×10^{17} cm^{-3} in order to increase the channel current and, hence, the power output/unit periphery. This lead to a vastly improved FET with power output $\approx$0.52 - 0.62 W/mm, but with other important parameters, such as input capacitance and drain resistance, also greatly changed. This two-stage amplifier is presently being redesigned to reflect the parameters of the improved FET's.

4.4 CIRCUIT FABRICATION

4.4.1 Metallization

To keep RF losses to a minimum, the thickness of the metal forming the circuit should exceed the skin depth of the frequency of interest and preferably approach two or three skin depths thick. At 5 GHz, a skin depth is $\approx$1 micron, while at 10 GHz, it is $\approx$0.7-micron thick. Thus, a metal thickness of $\approx$2 microns is desirable. However, the thicker the metal, the more difficult it is to define. Hence, a compromise minimum thickness of 1.5 microns was selected.

With the original scheme of oxide rejection (see section 3.1), there was no problem with achieving this thickness, but, with the necessity of going to the chlorobenzene process, this step became more difficult. It is now necessary to put down 2 μm of photoresist in order to provide a sufficient margin for lift-off.

The results of such a lift-off can be seen in figures 68 and 69. Figure 68 shows the capacitor fingers at the input of a single-stage amplifier. The fingers are 5 μm wide with 5 μm gaps. Another view of these same fingers is given in figure 69 together with a view of an earlier interdigital capacitor fabricated by ion

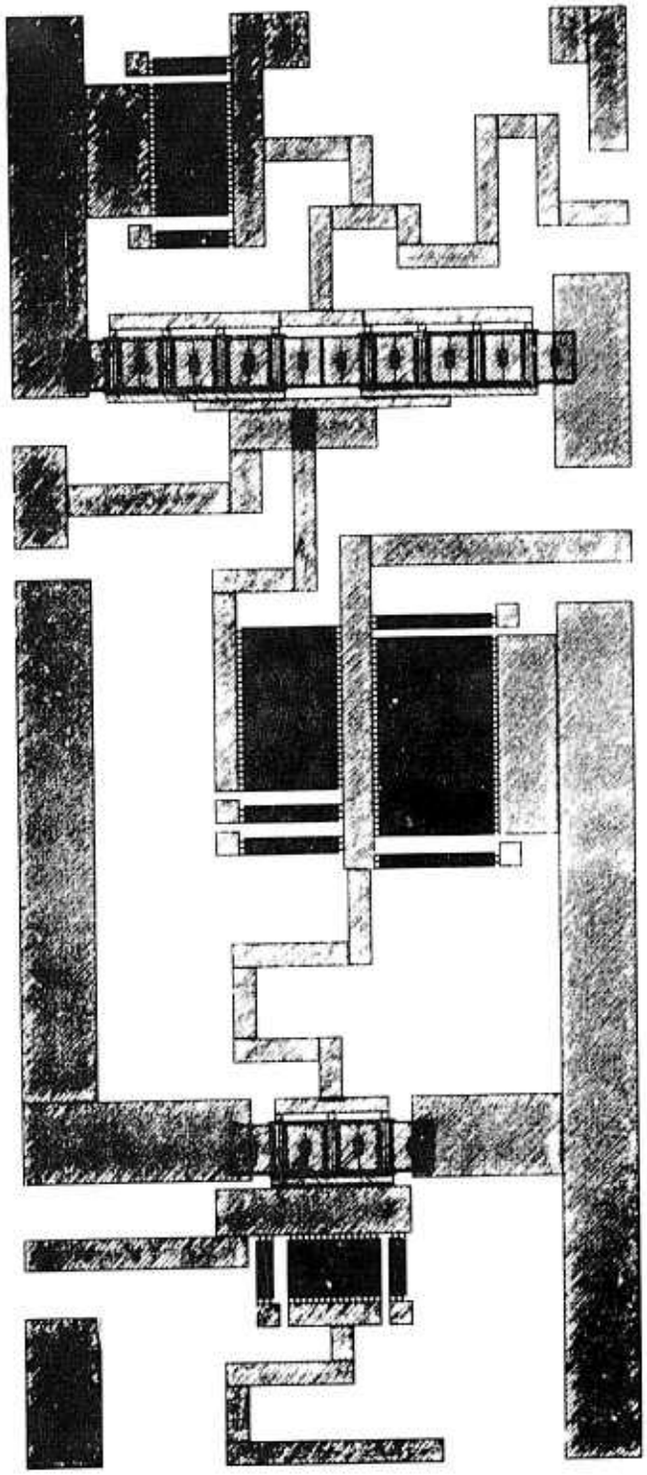

Figure 67. Two-Stage Amplifier Mask

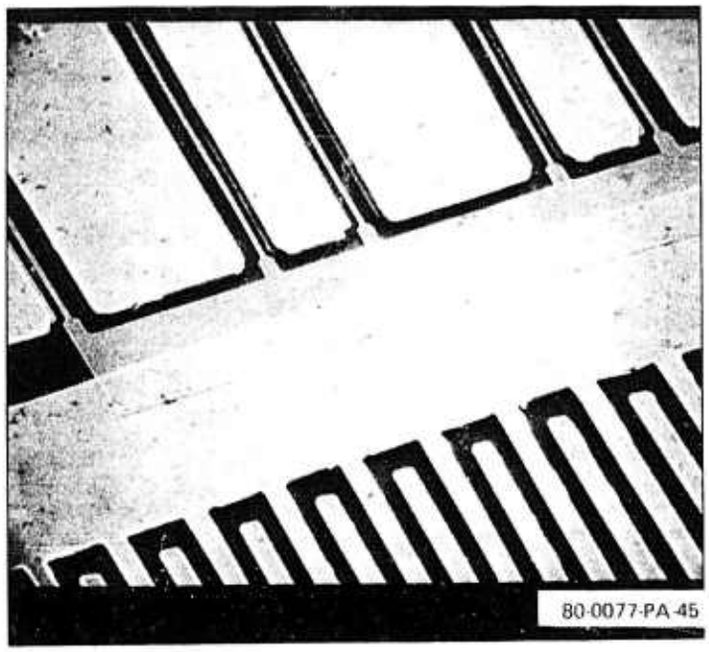

Figure 68. Capacitor Fingers at Input of Amplifier

milling. Notice the difference in the cross section of the fingers. Figure 70 shows the chlorobenzene-treated photoresist prior to metal evaporation for these same capacitor fingers.

Initially, the thick metallization for the circuit had been composed of the ohmic metallization (AuGe-Pd-Au) that was used at that time to form the source and drain contacts. This had the advantage that a photoresist step was eliminated from the fabrication process. The disadvantage was that the metallization forming the capacitor fingers now made "ohmic" contact to the semi-insulating substrates, which allowed space-charge-limited current to be injected into the substrate, and this made the capacitors leaky. The substitution of a Schottky metal formula (Cr-Pd-Au or Ti-Pt-Au) has eliminated this problem.

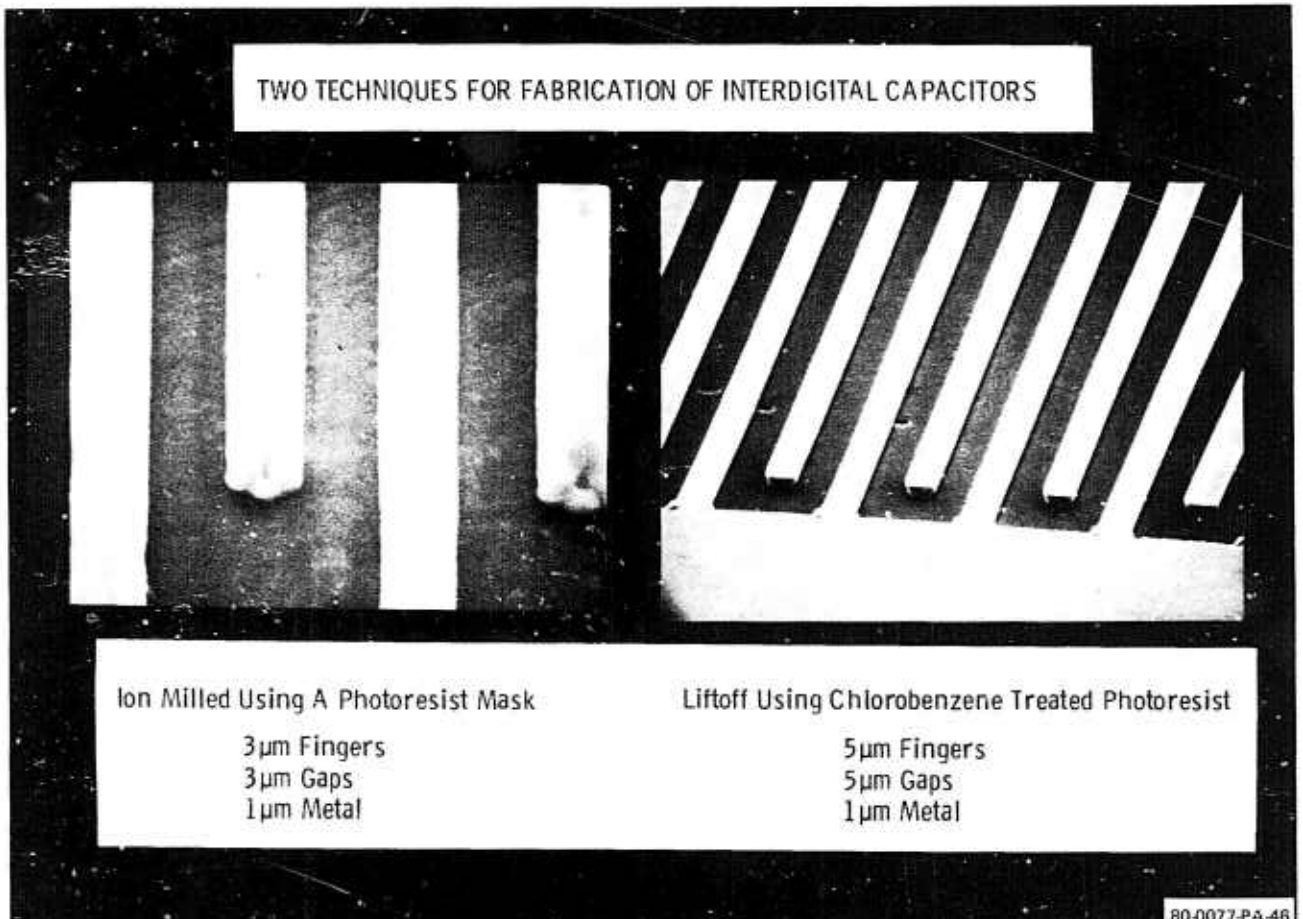

Figure 69. Two Techniques for Fabrication of Interdigital Capacitors

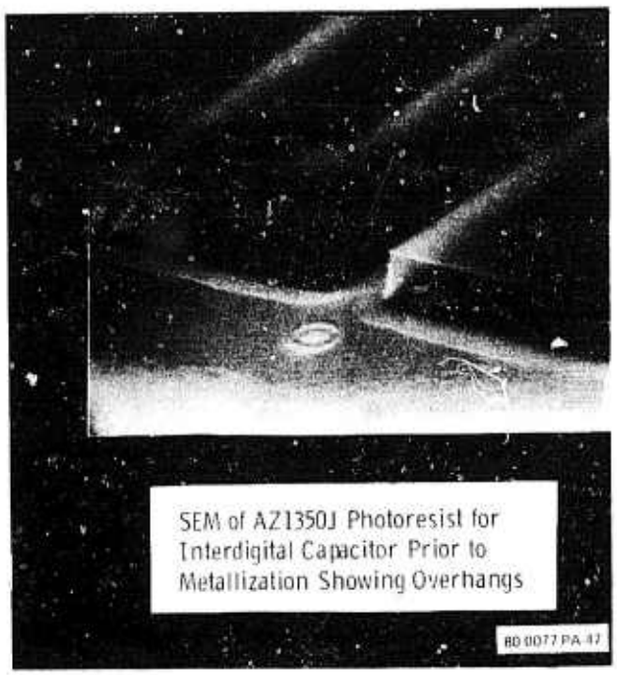

Figure 70. Use of Chlorobenzene-Treated Photoresist to Form Overhangs for Metal Rejection

4.4.2 Overlay Capacitors

In parallel with the interdigital capacitor development, a small effort was mounted to look at overlay capacitors. These devices have the advantage that they consume much less real estate than interdigital capacitors for the same capacitance value. Large values of capacitance are necessary for RF-bypass functions and overlay techniques represent the only practicable way these might be fabricated on chip.

Fabrication of dielectric overlay capacitors involves three basic steps: (1) deposition of the bottom electrode, (2) deposition and definition of the dielectric layer, (3) deposition of the top electrode. A suitable metallization formula for the bottom electrode is 600 Å Ti, 400 Å Pt, 8000 Å Au, and 500 Å Cr. Dielectrics which have shown promise are SiO_2 sputtered onto a 500°C substrate, densified CVD SiO_2, and plasma-deposited nitride. A suitable metallization formula for the top electrode is 800 Å Cr, 10,000 Å Au.

Figure 71 shows overlay capacitors that have been fabricated. Problems with excessive losses due to thin metallization have limited us to very low Q values (<3). This work is continuing.

4.4.3 Ground-Plane Fabrication

The performance of microstrip amplifiers requires a low resistivity ground plane on the back of the 100μm thick wafer. Since the chip is eventually soldered down on the chip carrier using a Au-Sn preform, it is important that not all the metallization be consumed by this solder, which has a relatively poor conductivity compared with pure gold. A barrier layer of nickel has therefore been introduced in the metallization scheme which now consists of Ti-Au-Ni-Au in the thicknesses 500-10,000-1000-1,000 Å, respectively.

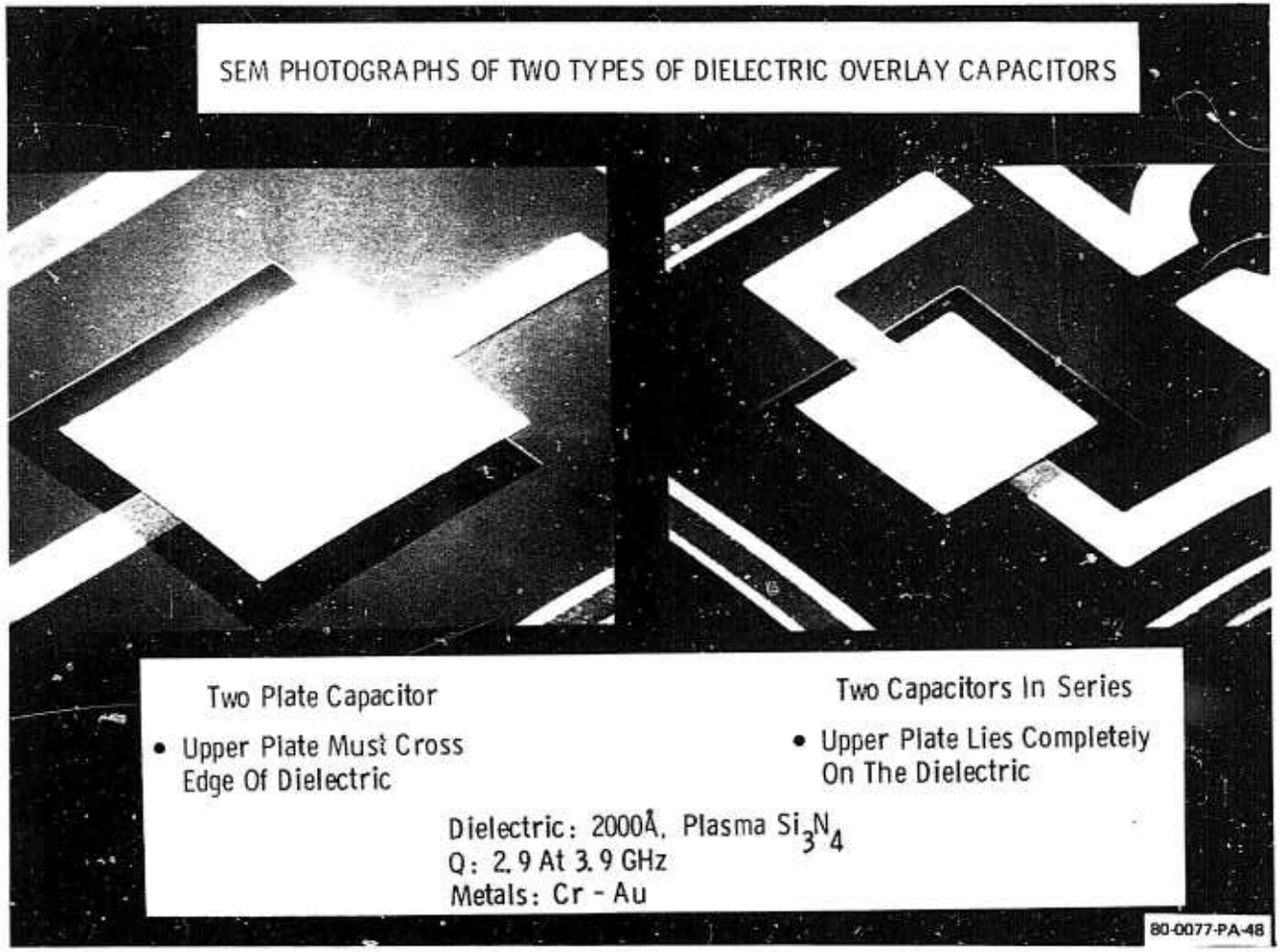

Figure 71. SEM Photographs of Two Types of Dielectric Overlay Capacitors

5. PHASE SHIFTER

The high pass - low pass phase shifter has been the preferred mechanization for the three-bit phase shifter for this program because of its compact size and potential for wide-band operation.

In order to investigate this concept, a one-bit (90°) high pass-low pass shifter was designed and built using lumped elements on a GaAs substrate, but with chip GaAs Schottky barrier diodes used as switching elements. The chip devices are being used to check out the circuit and design concepts, while the monolithic S-B technology is developing in parallel. Figure 72 shows the mask of the phase shifter; the chip size is 0.080 in. x 0.086 in. In operation, chip diodes mounted on the GaAs circuit are used to switch in either the low-pass filter, consisting of two series inductors and a shunt capacitor, or the highpass filter, consisting of two series capacitors and a shunt inductor. The circuit diagram is shown in figure 73. The difference in phase between the two states is relatively constant over a broad frequency range.

The phase shifter was tested without diodes by simply ribbon bonding between the elements to study the lumped-element circuits without the diode parasitics. The phase shifter was then mounted on a ½ x ½-inch sapphire coplanar substrate as shown in figure 74. Figures 75 and 76 show the insertion loss and differential phase shift obtained.

The phase shifters were then tested, one section at a time, with the diodes and bias lines connected. Poor results were obtained and testing revealed that the bias lines were too long. After correcting the bias line length, evaluation of the 90 degree bit phase shifter with chip GaAs S-B diodes was continued while awaiting the completion of the unit with monolithic diodes.

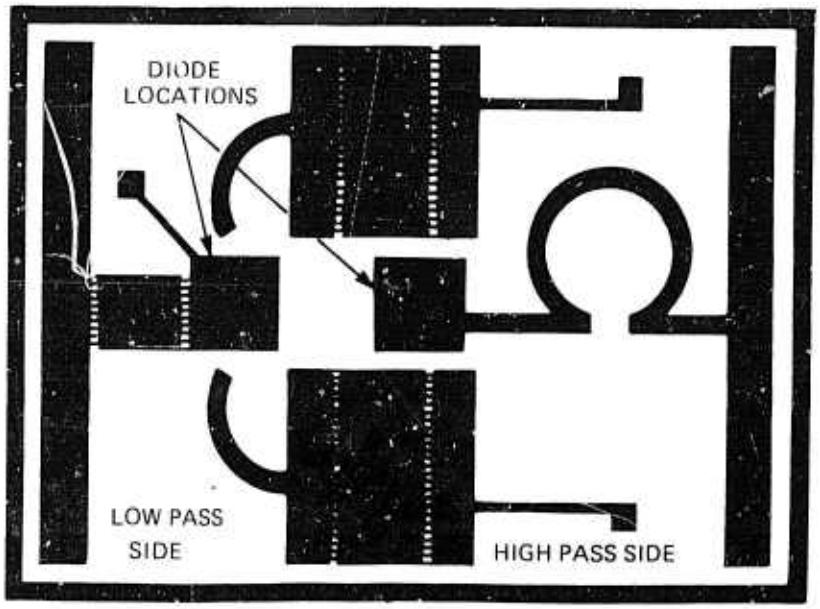

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Figure 72. Mask for 90-Degree Phase Shifter

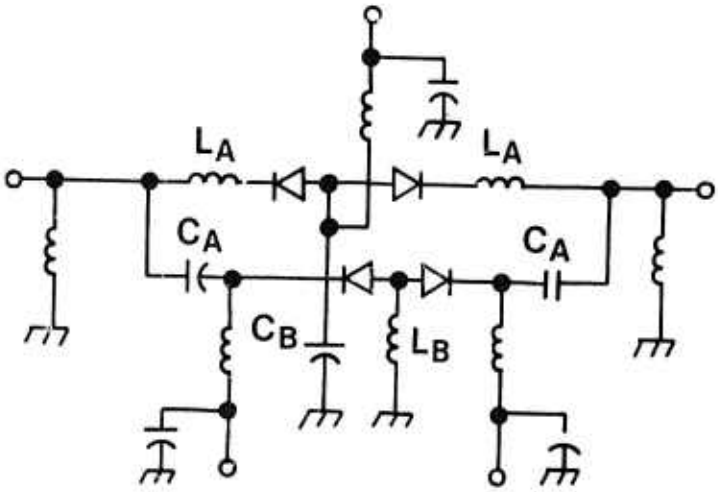

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Figure 73. Circuit Diagram of T-Section
Coplanar Line One-Bit Phase Shifter

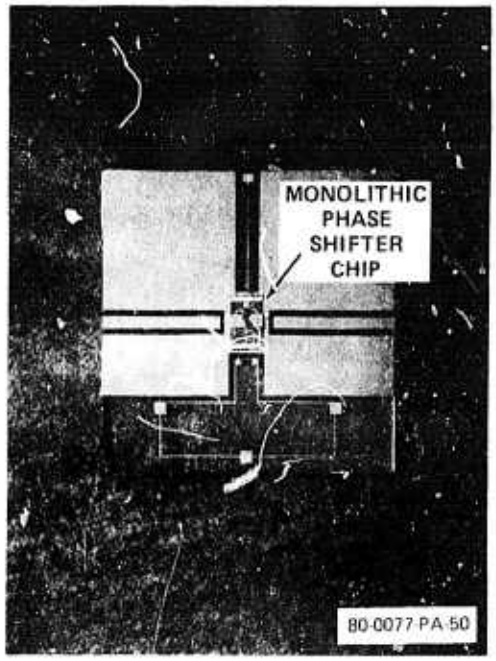


Figure 74. 90-Degree Phase Shifter Bit Mounted on Coplanar Test Substrate

Figure 77 shows the response of the phase shifter operating with four chip diodes. The high-pass response is skewed due to the added inductance of the diodes and some interaction with the reverse-biased low-pass circuitry. The low-pass state has a resonance due to interaction with the reverse-biased high-pass diodes. Disconnected from the high-pass circuit, the low-pass state alone showed a smooth well-behaved response. Calculations showed that a simple rearrangement of the switching diodes to the ends of the high and low-pass Tee's would eliminate this resonance; however, due to the intensity of the FET development effort, it has not been possible to try this redesigned phase shifter.

A totally monolithic 90-deg phase shifter was also fabricated on GaAs. Unfortunately, dc measurements of the monolithic diodes indicated extremely high reverse bias leakage and, hence, RF tests could not be performed. Again, due to the intensity of the FET and amplifier development, further work on this phase shifter was postponed.

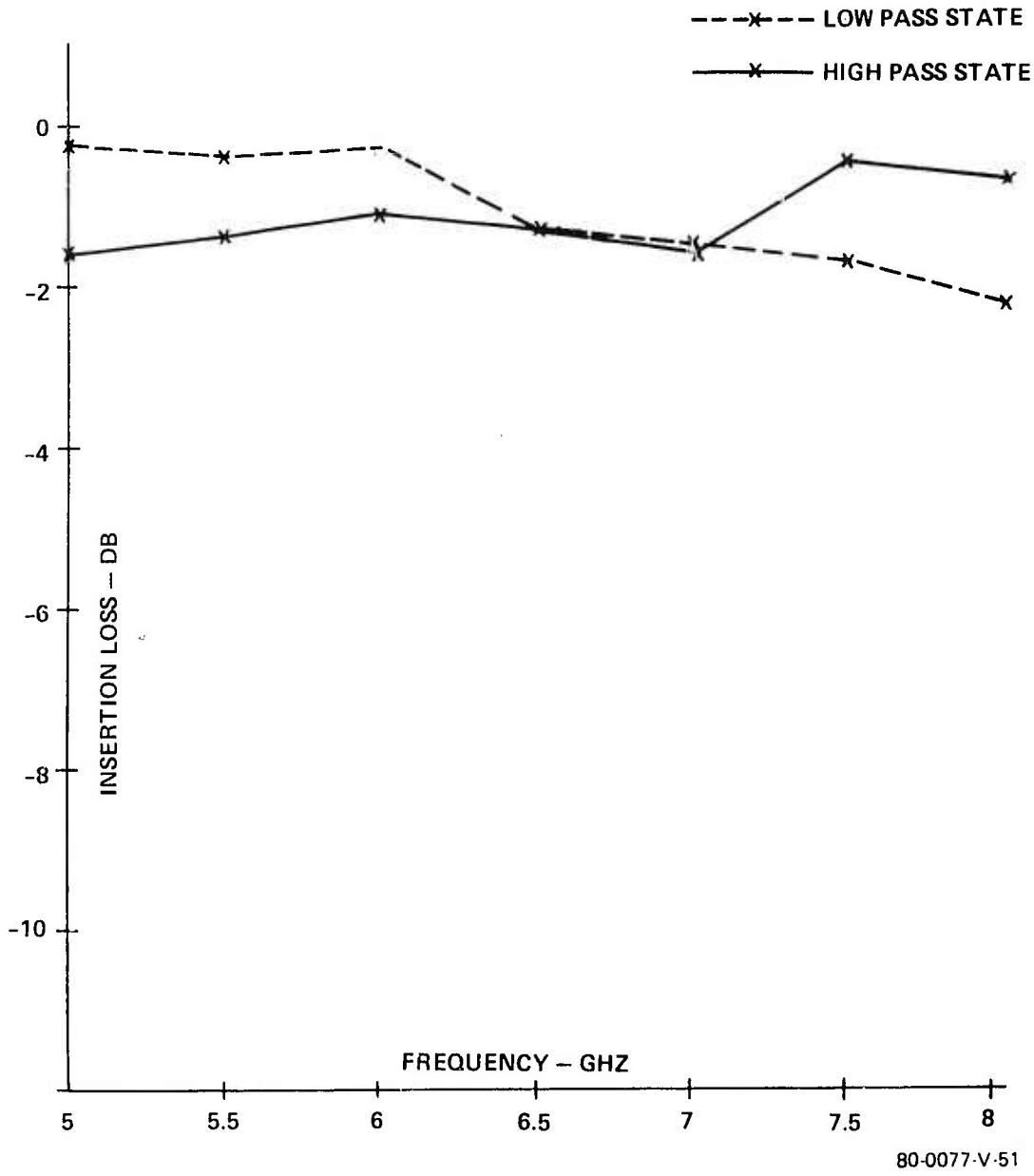


Figure 75. Insertion Loss vs Frequency

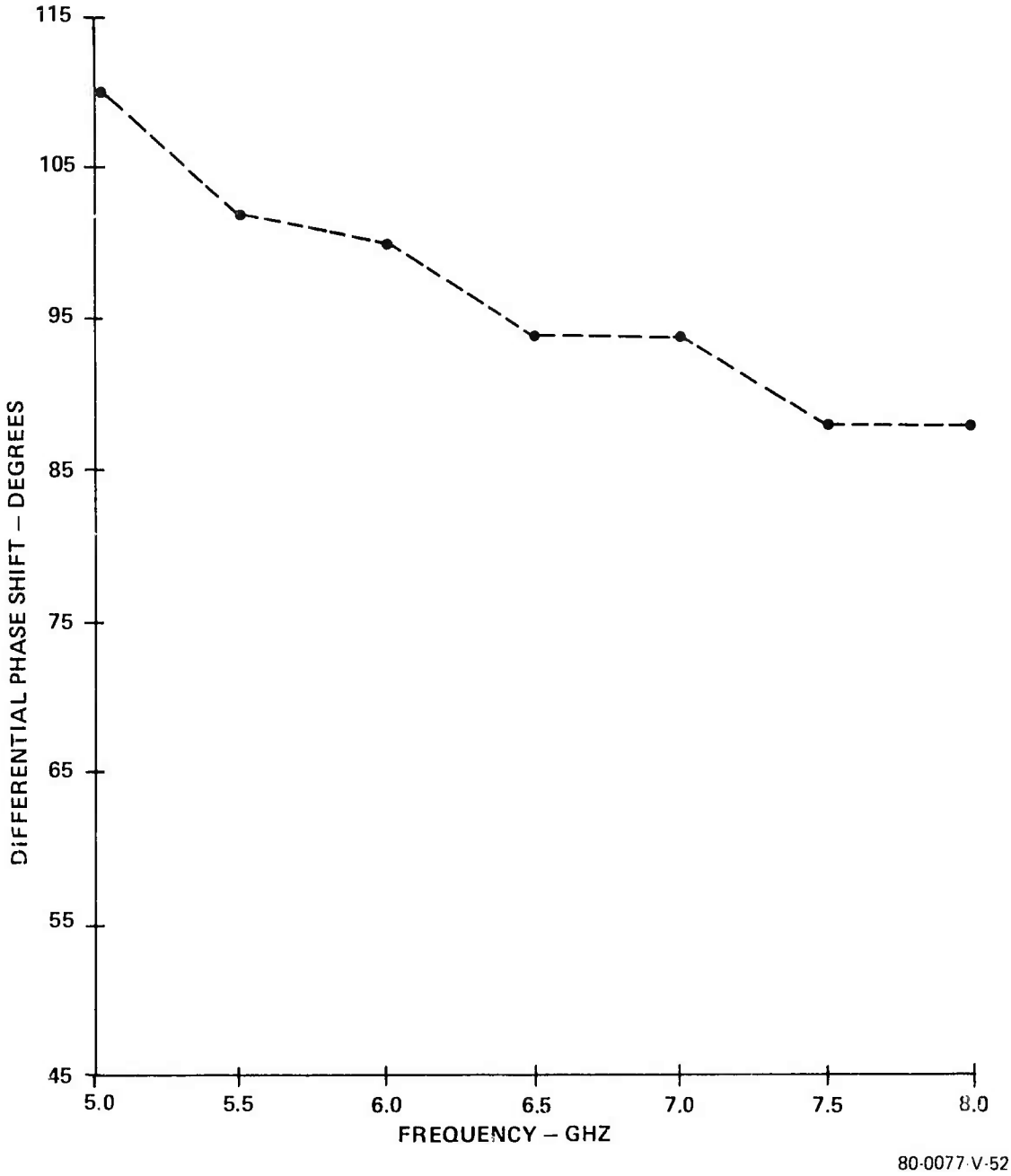


Figure 76. Differential Phase Shift vs Frequency

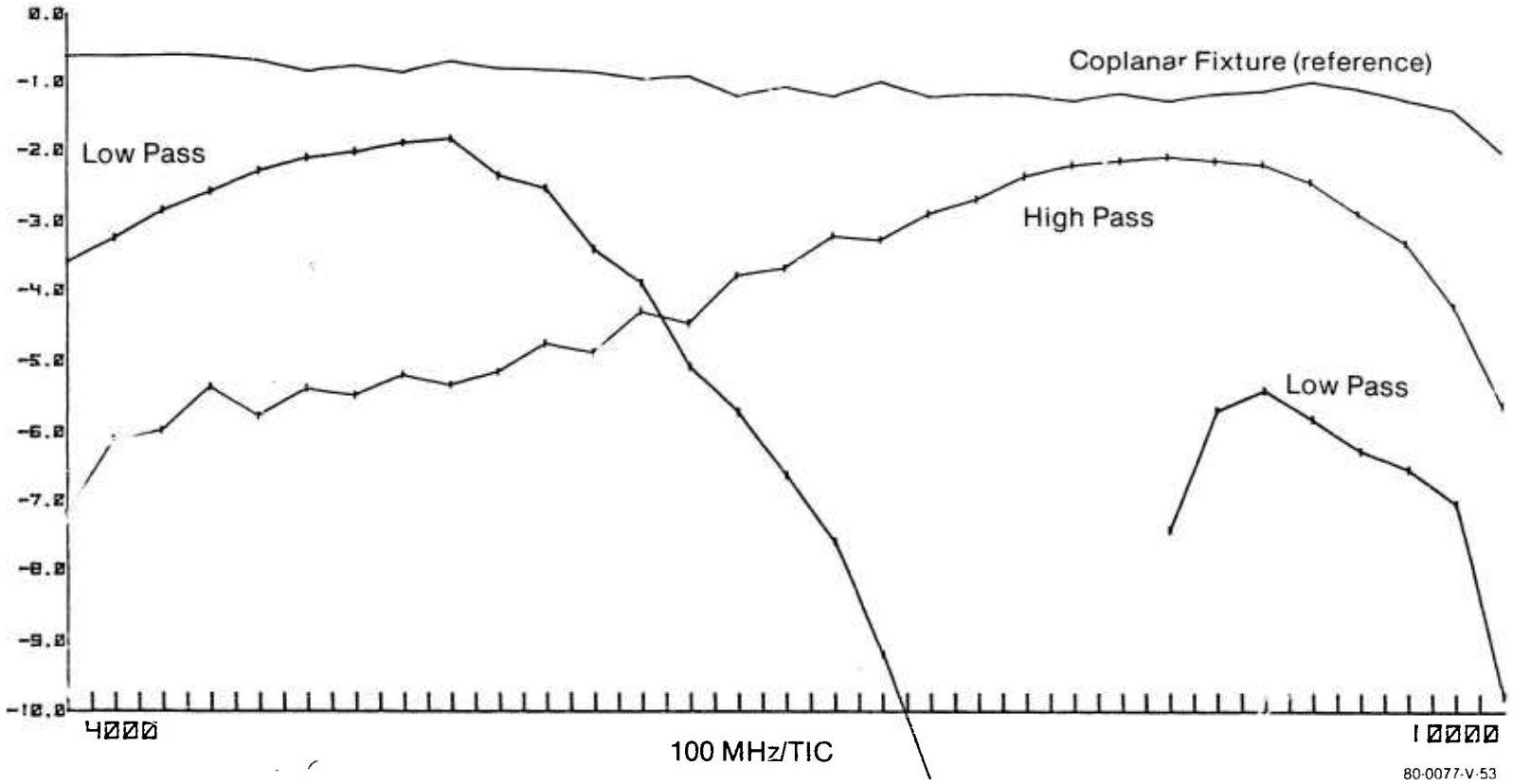
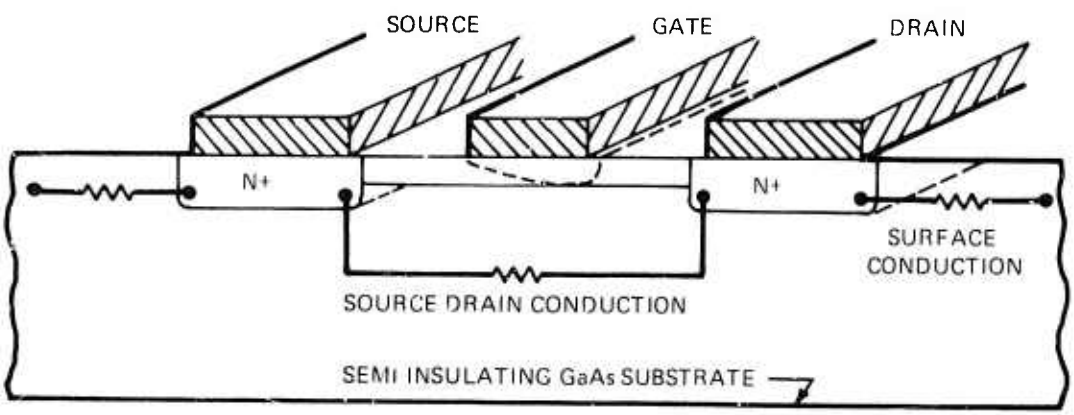


Figure 77. Measured Insertion Loss of the Monolithic 90-Degree Phase Shift Bit Using Chip GaAs S-B Diodes

6. GROWTH OF LARGE DIAMETER SEMI-INSULATING GaAs CRYSTALS BY LIQUID ENCAPSULATED CZOCHRALSKI (LEC)

The performance of GaAs microwave FET's and monolithic circuits is often adversely affected by the poor and upredictable quality of the semi-insulating substrates which are commercially available today. The effect of substrate quality on FET performance is illustrated in figure 78. The underlying high-resistivity GaAs substrate must retain its insulating properties throughout device fabrication in order to maintain high electrical isolation and low parasitic capacitances associated with the active device elements. Unfortunately, at the temperatures normally employed in FET processing, the thermal stability of the semi-insulating substrate has often been a severe problem in the past. A common manifestation of the problem is the formation of a conductive



- EXCESSIVE CONDUCTIVITY AFTER IMPLANTATION ANNEAL CAUSES DRAIN SOURCE PARASITIC CONDUCTION
- SURFACE CONVERSION SHORTS ADJACENT DEVICE ELECTRODES AND METAL INTERCONNECT PATTERNS
- HIGH SUBSTRATE TOTAL IMPURITY CONTENT REDUCES CARRIER MOBILITY AND DEGRADES FREQUENCY RESPONSE

80-0077 VA-54

Figure 78. Effects of GaAs Substrate Quality on FET Performance

surface layer following a thermal-annealing process. Excessive surface conduction can result in source-drain parasitic conduction and occasionally in surface shorts between adjacent device electrode and metal-interconnect patterns. This surface-conductive layer is generally thought to result from a redistribution of impurities in the substrate. In addition, commercially obtained semi-insulating substrates often contain a high total impurity content which reduces the electron mobility in FET channels and degrades the FET performance and frequency response.

Until quite recently, GaAs metal semiconductor field effect transistor (MESFET) fabrication technology has employed high-purity or Cr-doped homoepitaxial buffer layers to overcome the higher impurity content of semi-insulating GaAs substrates. When n-type active FET layers doped to 1×10^{17} cm^{-3} with silicon are formed by epitaxial growth on these buffer layers, near-theoretical electron mobilities of 5000 cm^2/V-sec have been achieved. For low-cost fabrication and reliability, however, the elimination of epitaxial growth processing through the use of direct implantation in semi-insulating substrates offers significant benefits. Recent results at our laboratories[11] and elsewhere[12] indicate that active FET layers with mobilities between 3800 and 4300 cm^2/V-sec (adequate for high performance FET fabrication) can be achieved by direct implantation, although lower mobilities are typically observed, in general, due to the poor and unpredictable quality of substrates available commercially. It is now well recognized throughout the industry that a reliable source of uniform, reproducible, and thermally stable GaAs material is urgently needed if direct ion implantation is to fulfill its promise in low-cost GaAs MESFET fabrication.

To provide a captive source of reliable, high-quality GaAs substrates, a new crystal growth and substrate preparation facility which utilizes a high capacity, Melbourn liquid-encapsulated Czochralski (LEC) puller has recently been established at the Westinghouse R&D Center in Pittsburgh. LEC growth was selected over other growth technologies because of its current

capability for producing two- and three-inch diameter <100>- and <111>- crystals of semi-insulating GaAs from which round, large-area substrates can be prepared (figure 79). In device processing, costs are approximately independent of wafer size, making large-area substrates very attractive for future low-cost manufacturing technology as illustrated graphically in figure 80. Perhaps of even more significance is the adapability of LEC growth to the use of silicon-free, pyrolytic boron nitride crucible techniques[13] offering the potential of semi-insulating GaAs crystals of significantly improved purity.

Since the completion of the crystal puller installation and associated facilities at Westinghouse in April 1979, significant progress in GaAs crystal growth, in terms of establishing a sound growth technology and in improving crystal purity using pyrolytic boron nitride crucibles, has been demonstrated. These improvements have already contributed directly to the higher implanted channel mobilities which are now being achieved and to the reproducible FET characteristics at the 0.6-Watt/mm power levels of our current devices. Our progress to date is highlighted by the following accomplishments which demonstrate:

- Reproducible growths of 2- and 3-inch diameter, <100>- 5 to 8 in. long GaAs crystals free of twin planes and inclusions.
- Growth of 3 in. diameter high-purity, semi-insulating <100> GaAs crystals from pyrolytic boron nitride crucibles.
- GaAs/PBN undoped crystals consistently yielding substrate resistivities approaching 10^8 ohm-cm which are thermally stable under implantation anneal.
- Secondary Ion Mass Spectometry (SIMS) analyses show GaAs/PBN crystals contain lowest total impurity content, especially Si and Cr impurities.
- Direct[29] Si implants into semi-insulating GaAs/PBN substrates yield uniform implant profiles and near theoretical mobilities (>5000 cm^2/V-sec).
- FET's fabricated on GaAs/PBN substrates exhibit excellent g_m, small-signal gains and RF output power.

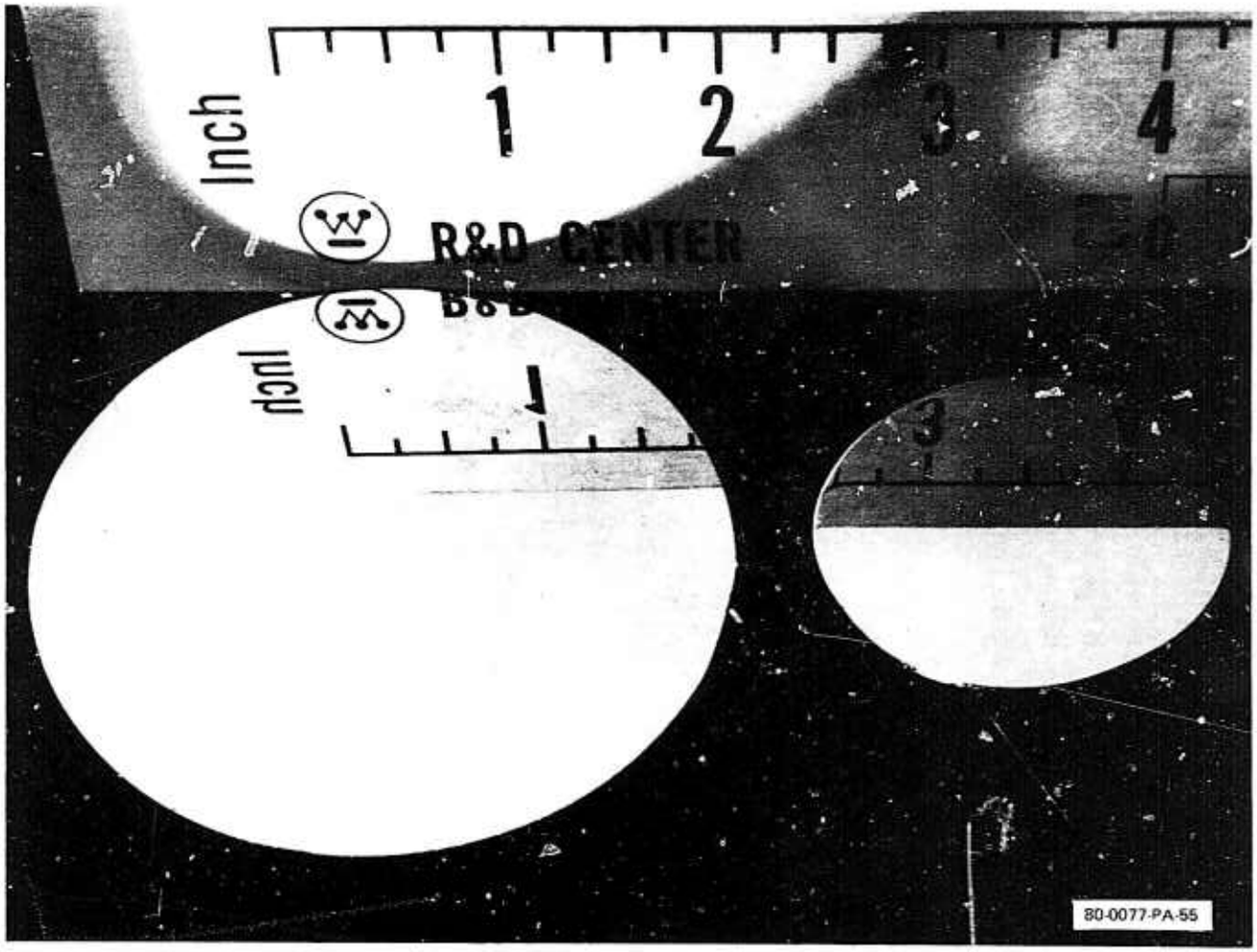
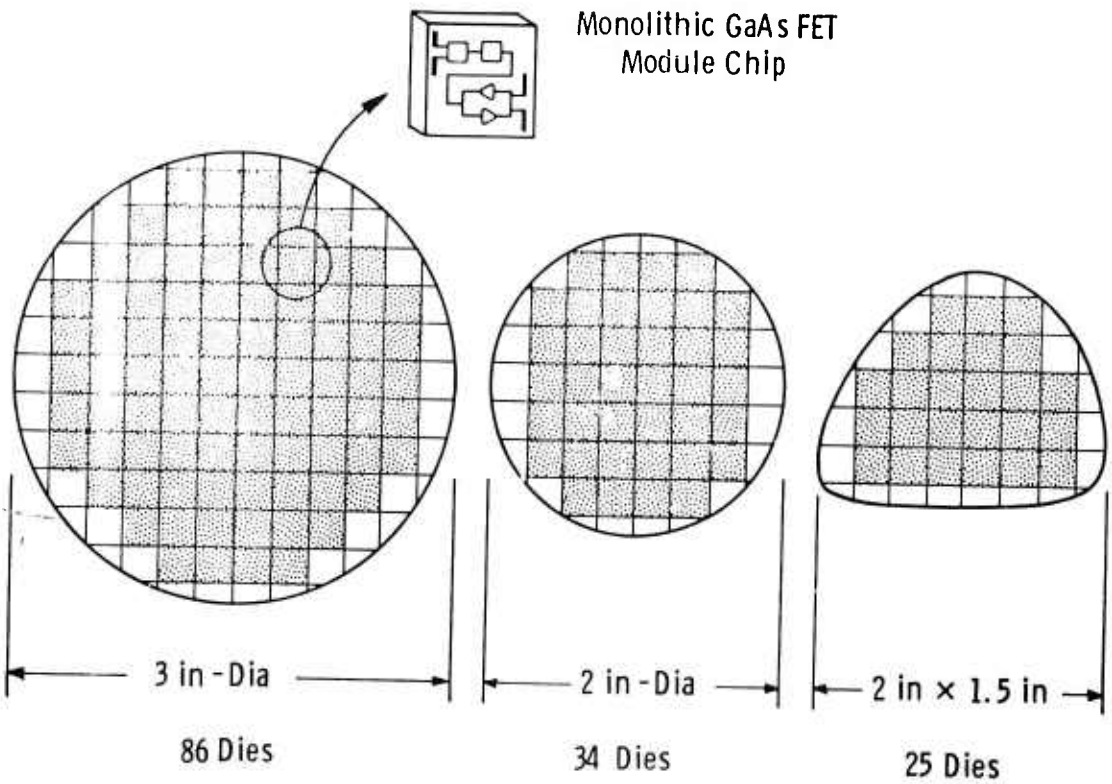


Figure 79. Two and Three-Inch Diameter GaAs Wafers Cut From <100> - Oriented Crystals Grown in the Westinghouse Melbourn Liquid Encapsulated Czochralski Puller



3 In-Dia, < 100 > - Round Wafers by Melbourn Technology Offers:

- Over 2 1/2 times as many dies/wafer as a 2 in diameter substrate
- Approximately same handling and processing costs as 2 in diameter substrate

80-0077-V-56

Figure 80. Effect of GaAs Wafer Diameter on Number of 250-mil^2 Module Chips Per Wafer

Studies of GaAs crystal growth fall outside the defined scope of this contract work. However, because of the importance of improved substrate quality to device performance and its future impact on the overall program goals, a brief outline of the GaAs growth facility established at Westinghouse the growth studies which have been performed to date, and the materials quality of substrates currently being utilized for FET and IC processing are described more fully in Appendix A.

7. FUTURE GOALS

7.1 ION IMPLANTATION

The inclusion of the N^+ contact in the fabrication sequence will improve the reliability and quality of the ohmic contacts. It may also improve the breakdown voltage of the FET, although indications are that the contacts are not the major problem at present.

The plasma-enhanced Si_3N_4 deposition system requires a great deal of attention in terms of calibration and cleaning. Consequently, we are currently investigating the use of reactively sputtered Si_3N_4 as a capping layer during the annealing of ion-implanted layers.

7.2 FET's

The fabrication of electrical and thermal connections (vias) between the source contact pads and the metal ground plane on the back of the 100-μm thick wafers is presently under study. The implementation of these vias in the device design will reduce the source inductance and remove some of the instabilities observed during device testing.

Coupled with the via technology is the development of air bridges for interconnection of FET contacts or as crossovers in the passive part of the circuit.

One of the major problems in obtaining good power output from our devices is the achievement of high reverse-voltage capability on the gateSchottky contacts. This problem appears to be related to detailed structure of the gate recess, but there is also some evidence that the carrier concentration (and perhaps the implant profile) may also be a factor. A study of this will proceed using light emission and its correlation with structures observed in the scanning electron microscope.

7.3 CIRCUITS

A two-stage amplifier design has been completed and devices are currently being fabricated. This amplifier is aimed towards octave bandwidth capability centered at 7.5 GHz with 1-watt output.

A three-stage amplifier will be designed when the results of the two stage have been evaluated.

7.4 PHASE SHIFTER

Emphasis will be on improvements in the phase shifter circuit to eliminate resonances.

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10. W.E. Courtney, "Complex Permittivity of GaAs and CdTe at Microwave Frequencies," IEEE SMTT Trans., vol. MTT-25, pp. 697-701, August, 1977.
11. Westinghouse Bi-Monthly Report, ONR Contract N00014-78-C-0268, "GaAs Monolithic Microwave Subsystem Technology Base," September 1978.
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APPENDIX A

GROWTH OF LARGE-DIAMETER SEMI-INSULATING GaAs CRYSTALS BY LIQUID-ENCAPSULATED CZOCHRALSKI (LEC)

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A.1 GaAs CRYSTAL GROWTH FACILITIES

A.1.1 Melbourn LEC Growth

For the growth of large diameter undoped and Cr-doped GaAs crystals, Westinghouse purchased a Melbourn high-pressure LEC puller from Metals Research Ltd. in England. This high capacity 60-kVA resistance-heated crystal-growth system utilizes a 6-in. diameter crucible and can operate at pressures up to 150 atmospheres. The maximum pull length is 24 in. and, although charges of 3 kg are used at present, charge weights up to 8 kg of GaAs are possible. The system features a closed-circuit TV for viewing the melt, a differential crystal weight monitor for control of growth, and a proprietary coracle technology for automatic diameter control. This technology involves the control of crystal dimensions by growth through an oriface formed by an inert silicon nitride disc floating on the melt. This technique, which has only been developed for <111> growth, is capable of controlling crystal diameter to within ±1 mm on a 55-mm diameter ingot. A plan view of the crystal growth laboratory is shown in figure A-1, which features a special reinforced concrete containment room for the Melbourn puller with a clean area surrounding the containment room for crucible loading and for the remote control console.

Figure A-2 is a photograph taken of the Melbourn LEC puller before installation in the containment room at Westinghouse. The high-pressure vessel of 60-liter capacity is divided into three chambers which are contained by the two large clamps shown in the photograph. These can be quickly disconnected and portions of the chamber can be lowered with a hydraulic ram system for easy access for cleaning and loading operations. Provisions are made for crucible rotation and lift (lower) and crystal rotation and

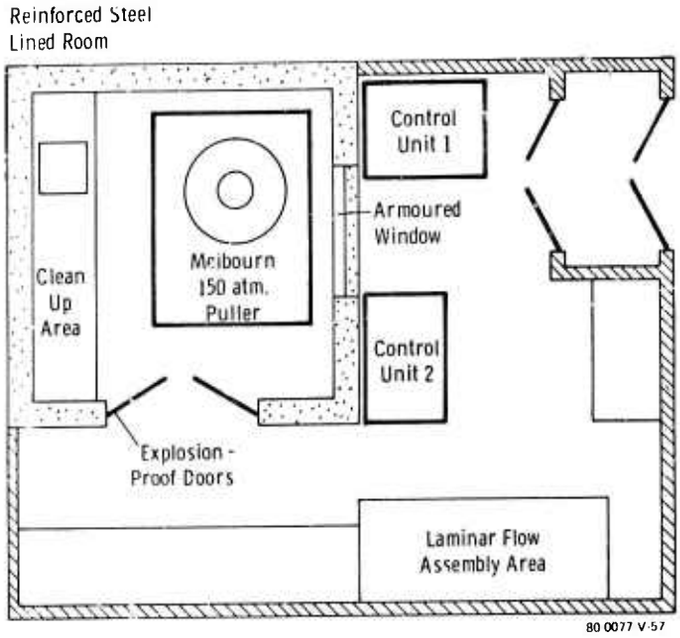

Figure A-1. Layout of GaAs 3-in. Diameter Crystal Growth Facility

lift (upper). The crystal is held by a load cell (top) within the high-pressure region to weigh the crystal and provide a differential-weight signal for controlled-diameter crystal growth. The TV camera transmits an image of the growing crystal using a large quartz banana-shaped light pipe which is displayed on the console monitor, as shown in figure A-3. For safety reasons, all growth-control functions are conducted outside the containment room using the control module also shown in figure A-3. A high-strength window is provided for viewing the puller from the outer control room (figure A-4).

A.1.2 GaAs Substrate Preparation

Figure A-5 is a drawing of the substrate preparation facility consisting of slicing and polishing operations. A ultra-low vibration Silicon Technology Corp. 5-1/2-in. ID saw is used for wafering. This machine, shown in figure A-6, is equipped for automatic operation and with a universal table for slicing

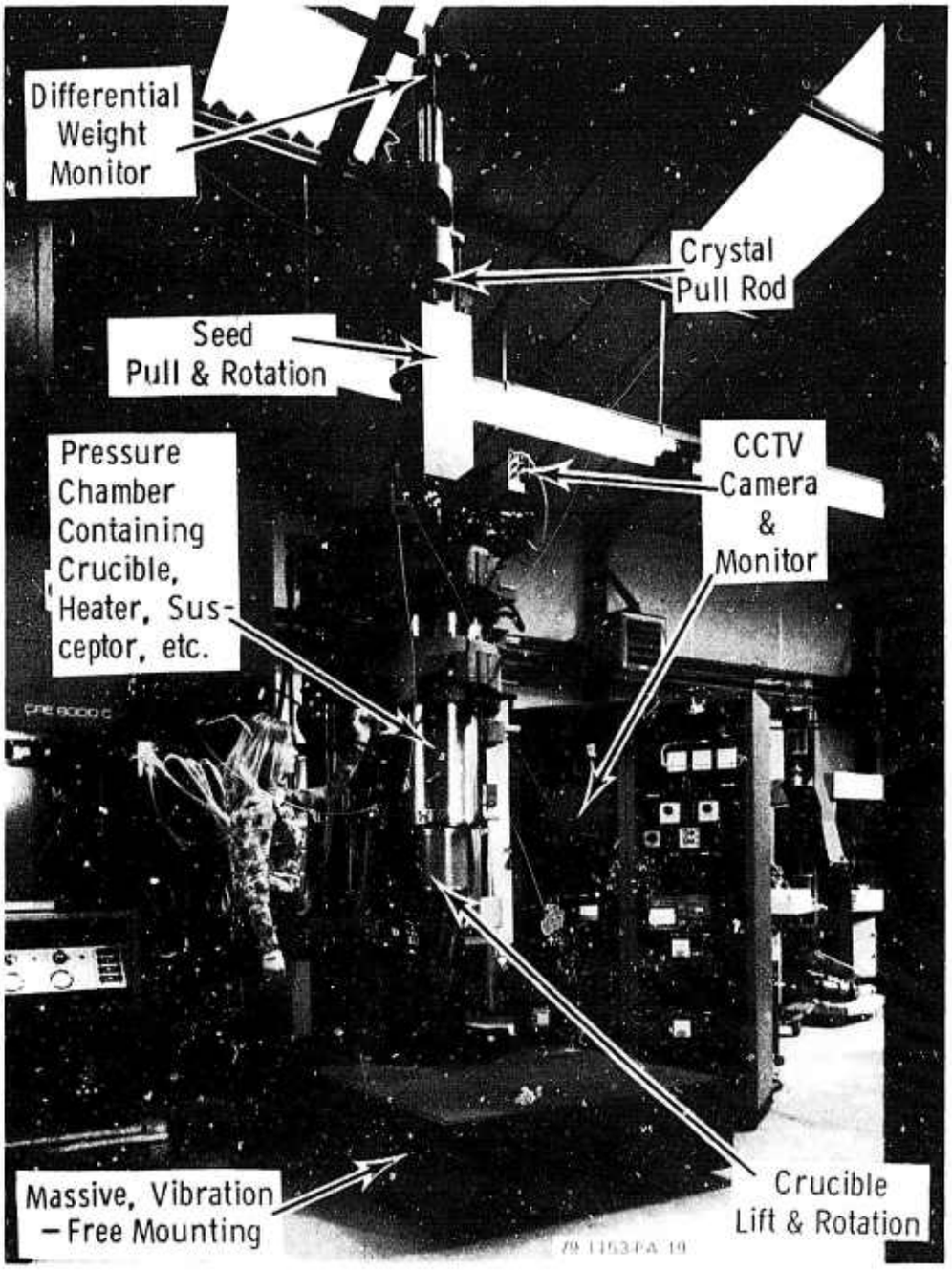

Figure A-2. Melbourn High Pressure LEC Crystal Puller

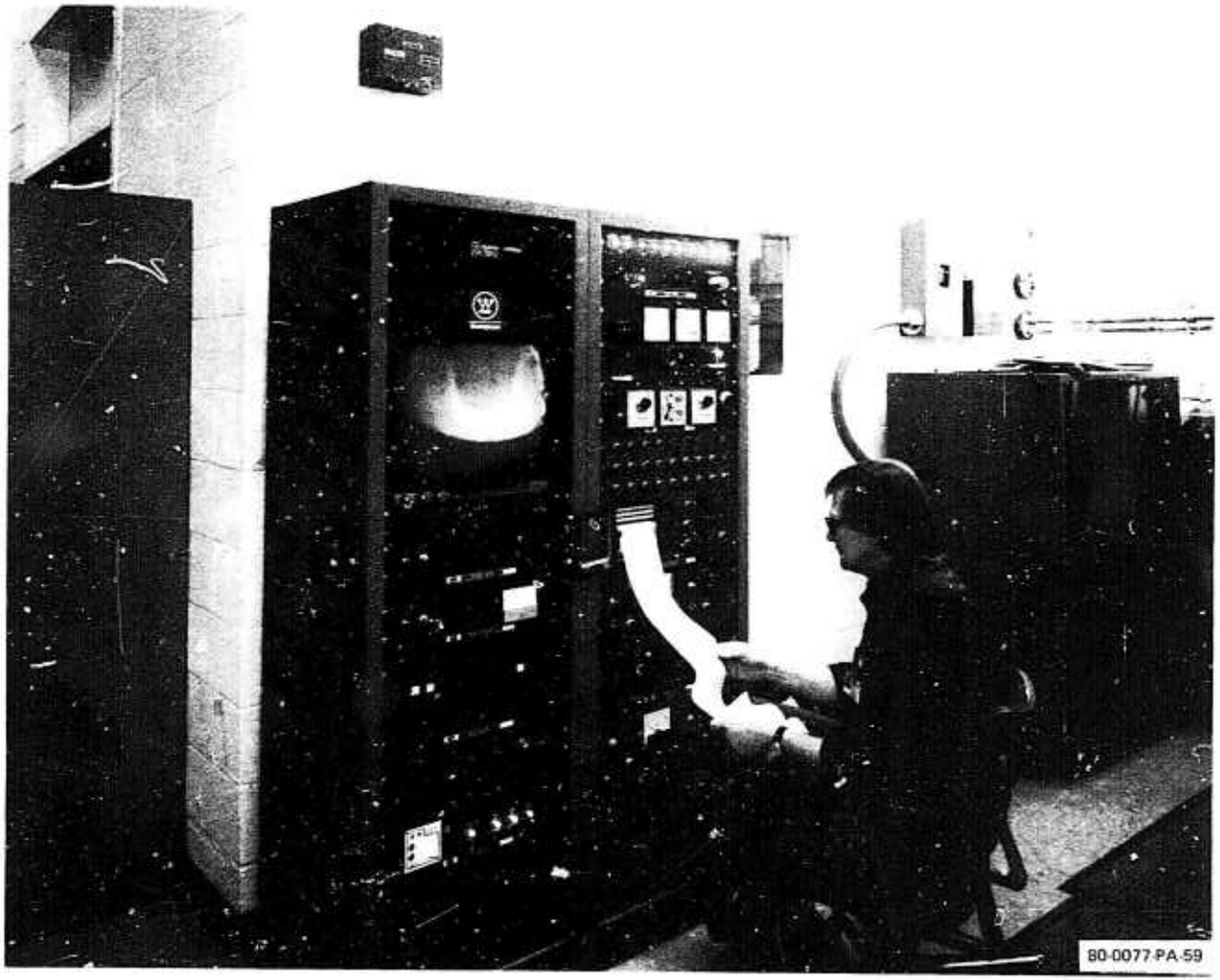

Figure A-3. Melbourn LEC Control Panel (Puller Is Located Within Containment Area)

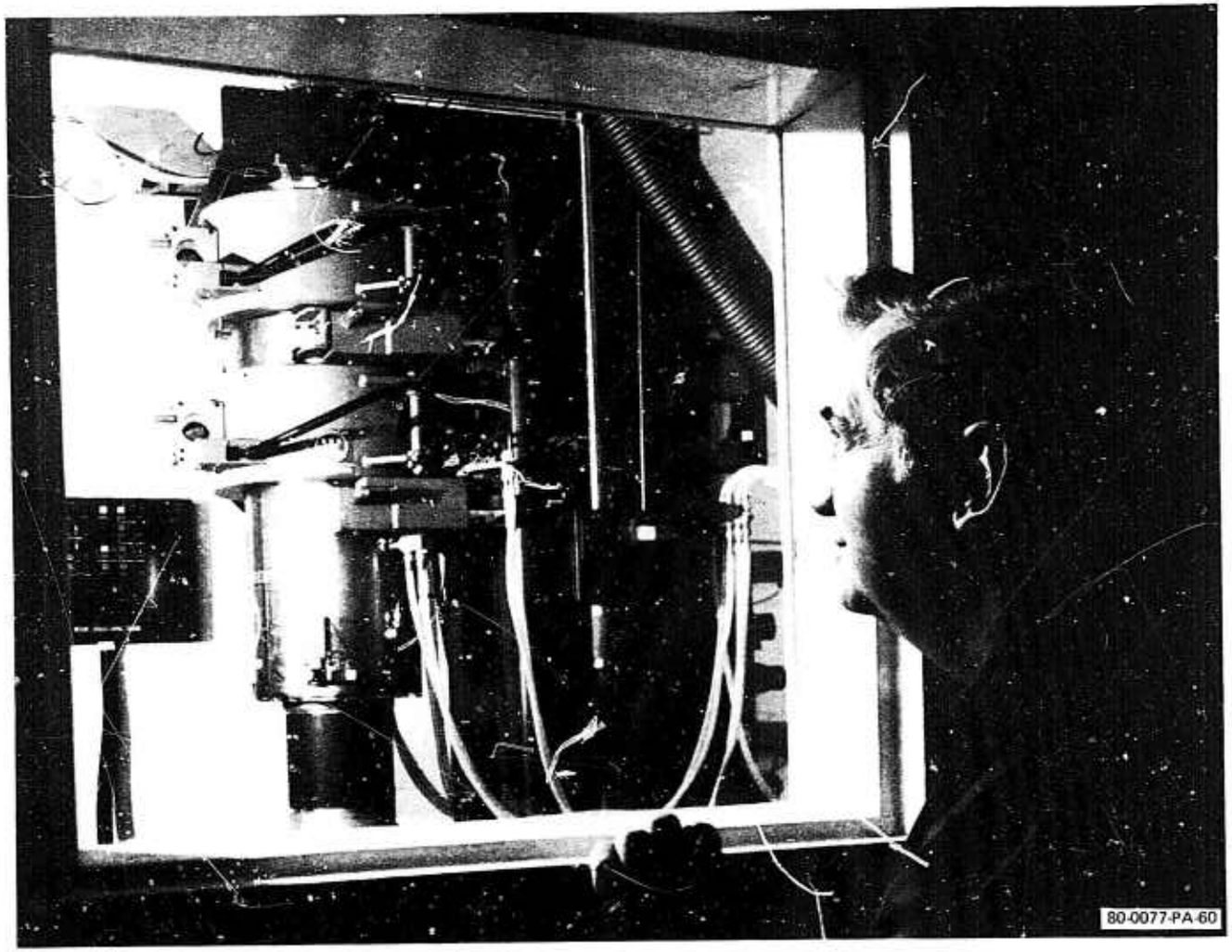

Figure A-4. Melbourn LEC Puller Through Viewing Window of Containment Room

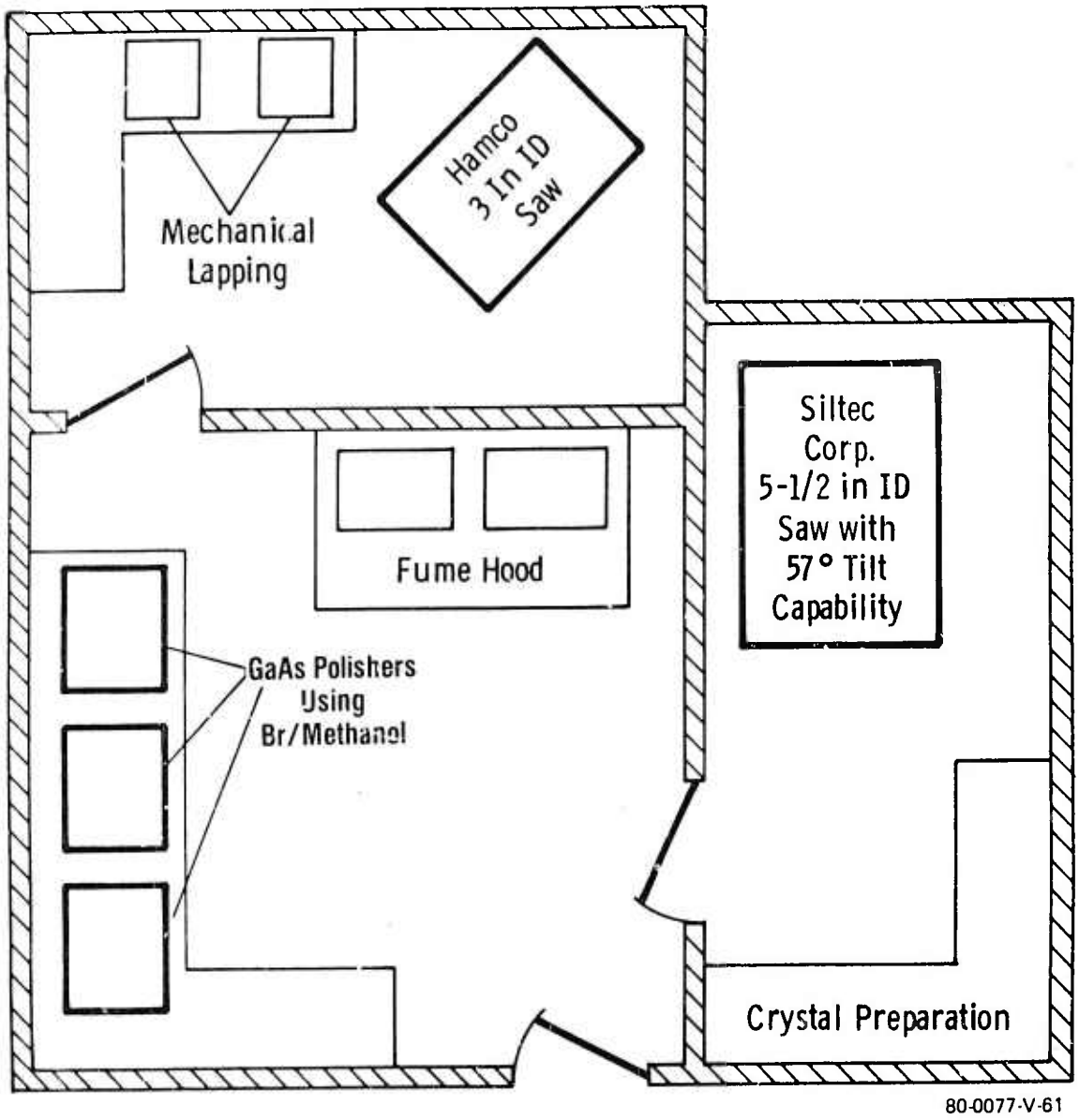

Figure A-5. Layout of Crystal Sawing and Wafer Polishing Facility Used for Preparing 3-in. Diameter GaAs Wafers

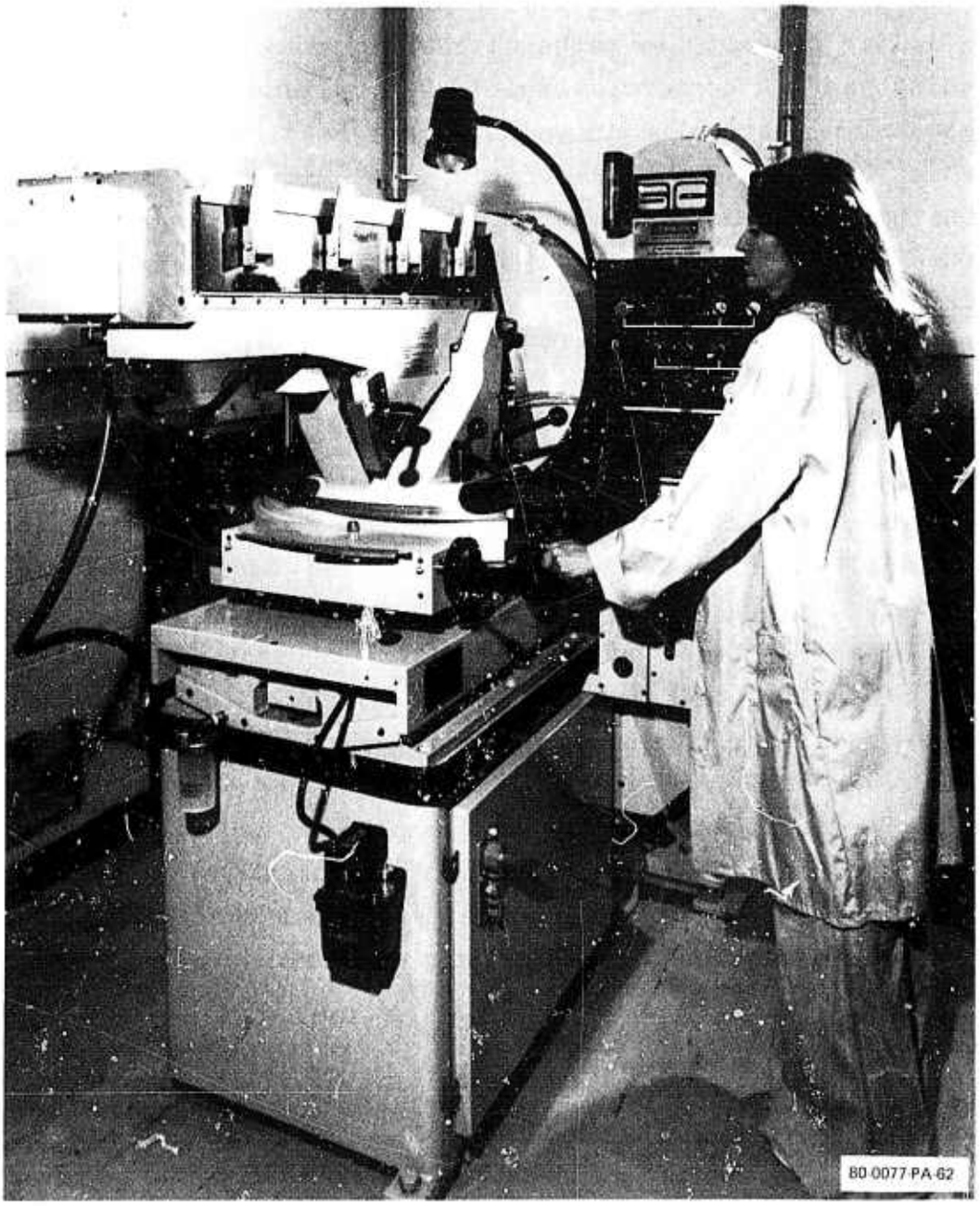

Figure A-6. Automated 5½-in. ID Saw for Precision Slicing of GaAs Wafers

accurately off-orientation. In particular, <111> -grown crystals can be sliced at the required 54-degree angle to prepare (non-circular) <100> oriented slices.

Wafers are polished for device processes using a diluted bromine (0.5 percent) in methanol technique on a smooth-napped polishing pad. A commercial Multipol-4 polisher developed for Br-methanol polishing is shown in figure A-7, which is capable of polishing up to 15 2-in. diameter wafers, simultaneously. Modifications have been made to enable up to nine 3-in. wafers to be polished using this apparatus. In addition, a Strausbaugh polishing machine was modified to prevent corrosion effects on steel components and is used to polish individual 3-in. wafers for evaluation purposes.

A.2 GaAs CRYSTAL GROWTH

Liquid-encapsulated Czochralski (LEC) growth was first demonstrated experimentally in 1962 by Mazelsky et al.* for the growth of volatile PbTe crystals and has since been developed by Mullins et al.** for several III-V crystals. In this Czochralski technique, the dissociation of the volatile As from the GaAs melt contained in a crucible is avoided by encapsulating the melt in an inert molten layer of boric oxide and pressurizing the chamber with a non-reactive gas, such as nitrogen or argon, to counterbalance the As dissociation pressure. In-situ compound synthesis can be carried out from the elemental Ga and As components since the boric melts at 460°C before significant As sublimation starts to take place. Compound synthesis occurs rapidly and exothermally at about 820°C under a sufficient inert gas pressure (~30 atm) to prevent sublimation of the arsenic component. Crystal growth is initiated from the 1237°C stoichiometric melt by seeding and slowly pulling the crystal through the transparent boric oxide layer.

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* E.P.A Metz, R.C. Miller and R. Mazelsky, "A Technique for Pulling Crystals of Volatile Materials," J. Appl. Phys. 33, 2016 (1962).

** J.B. Mullin, R.J. Heritage, C.H. Holliday and B.W. Straughan, "Liquid Encapsulated Pulling at High Pressure," J. Crystal Growth 3,4, 281 (1968).

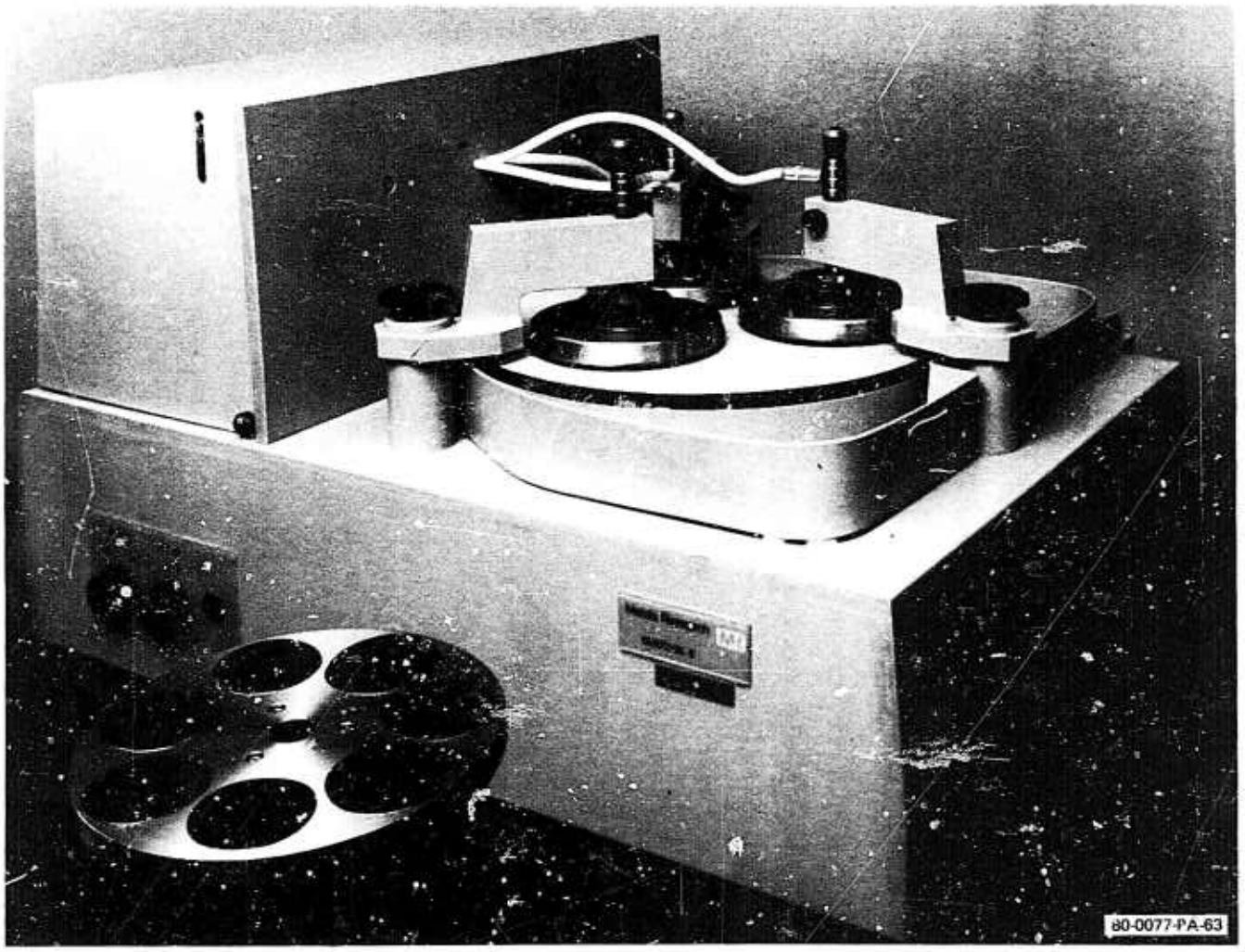

Figure A-7. Bromine-Methanol Etch Polishing of Flat GaAs Wafers

Transfer of the Melbourn growth technology to Westinghouse was initiated during October and November of 1978 by evaluation tests of the Westinghouse puller at the manufacturer's facilities in England. Six growth runs were carried out by Westinghouse and Metals Research personnel which resulted in two 3-in. diameter <100> -oriented Cr-doped GaAs crystals which were free of major crystalline defects.

After the Melbourn puller had been installed at the R&D Center, additional growth runs were conducted under the supervision of Metals Research personnel as part of the GaAs growth technology transfer. The GaAs growth puller and associated substrate preparation facilities became fully operational under Westinghouse supervision in April 1979. Since then, a number of 2- and 3-inch diameter <100>-GaAs crystals free of major structured defects (such as twin planes, inclusions, and precipitates) have been grown successfully. A photograph of two nominally 3-in. diameter semi-insulating GaAs crystals weighing approximately 2.75 kg is shown in figure A-8.

Figure A-8. Example of 3-in. Diameter Semi-Insulating <100> - GaAs Crystals Grown in Westinghouse Melbourn LEC Puller

Semi-insulating GaAs crystals have been prepared from undoped and Cr-doped melts contained in both fused silica and pyrolytic boron nitride crucibles. Figure A-9 shows a typical starting charge in a 6-in. diameter pyrolytic boron nitride crucible. The high-purity elemental arsenic and gallium is barely visible through the transparent boric oxide disc.

Some of the semi-insulating GaAs crystals have been sawed and polished to provide substrates for device fabrication. Selection of Cr-doped and undoped crystals was based on structural, chemical, and electrical characterizations which are described in section A.3.

A.3 CHARACTERIZATION OF GaAs CRYSTALS

A.3.1 Crystalline Perfection

*,**Although dislocation-free growths have been achieved in the past in small diameter (≤1/2 inch) GaAs crystals, today's state-of-the-art single crystals at diameters greater than 2 in. are characterized by quite high densities of point defects and dislocations.

The problem of high dislocation density is illustrated in the x-ray reflection topographs shown in figures A-10 and A-11. The topograph shown in figure A-10 was obtained from a (100) GaAs substrate cut from a 1.2 kg crystal grown in the <110>-direction by the modified Bridgeman boat growth technique. This crystal was purchased from an outside supplier. The substrate (approximately 2-1/2 in. maximum dimension) contains severely dislocated regions (near the left-hand edge of figure A-10) corresponding to high densities of dislocations which have coalesced into lineage boundaries within which non-reflecting crystal grains with slight angular misorientations have developed. Photomicrographs of regions

*B.C. Grabmaier and J.G. Grabmaier, "Dislocation-Free GaAs by the Liquid Encapsulation Technique," J. Cryst. Growth 13,14, 635 (1972).

**A. Steinemann and U. Zimmerli, "Dislocation-Free Gallium Arsenide Single Crystals," Proc. Intl. Cryst. Growth Conf., Boston (1966) p.81.

Figure 9. Photograph of 6-in. Diameter Pyrolytic Boron Nitride Crucible Containing Elemental Ga and As Charges and $(B2)_3$ Dice

A and B are shown in figure A-12 after treatment with an Abrahams-Buiocchi etchant*** which selectively attacks dislocations lying in the (100) substrate surface. A one to one correlation between dislocation features in the micrographs and the features of the x-ray topographs is demonstrated. The micrograph of figure A-12a shows that the dislocation density in region A (the non-reflecting part of the topograph) exceeds 10^6 cm^{-2} and that the lineage boundaries in region B (figure A-12b) are aligned in the <110> direction. Other areas of the boat-grown substrate (figure A-10b) show a uniformly distributed density of dislocations similar to that typically observed in large-diameter LEC-grown substrates, an example of which is shown in the topograph of figure A-11 for a 3-in. diameter (100) substrate taken from near the tang-end of a <100>- oriented, undoped GaAs crystal pulled from a pyrolytic boron-nitridec crucible. In general, LEC-grown substrates do not

***M.S. Abrahams and C.J. Buiocchi, "Etching of Dislocations on the Low Index Faces of GaAs," J. Appl. Phys. 36(9) 2855 (1956)

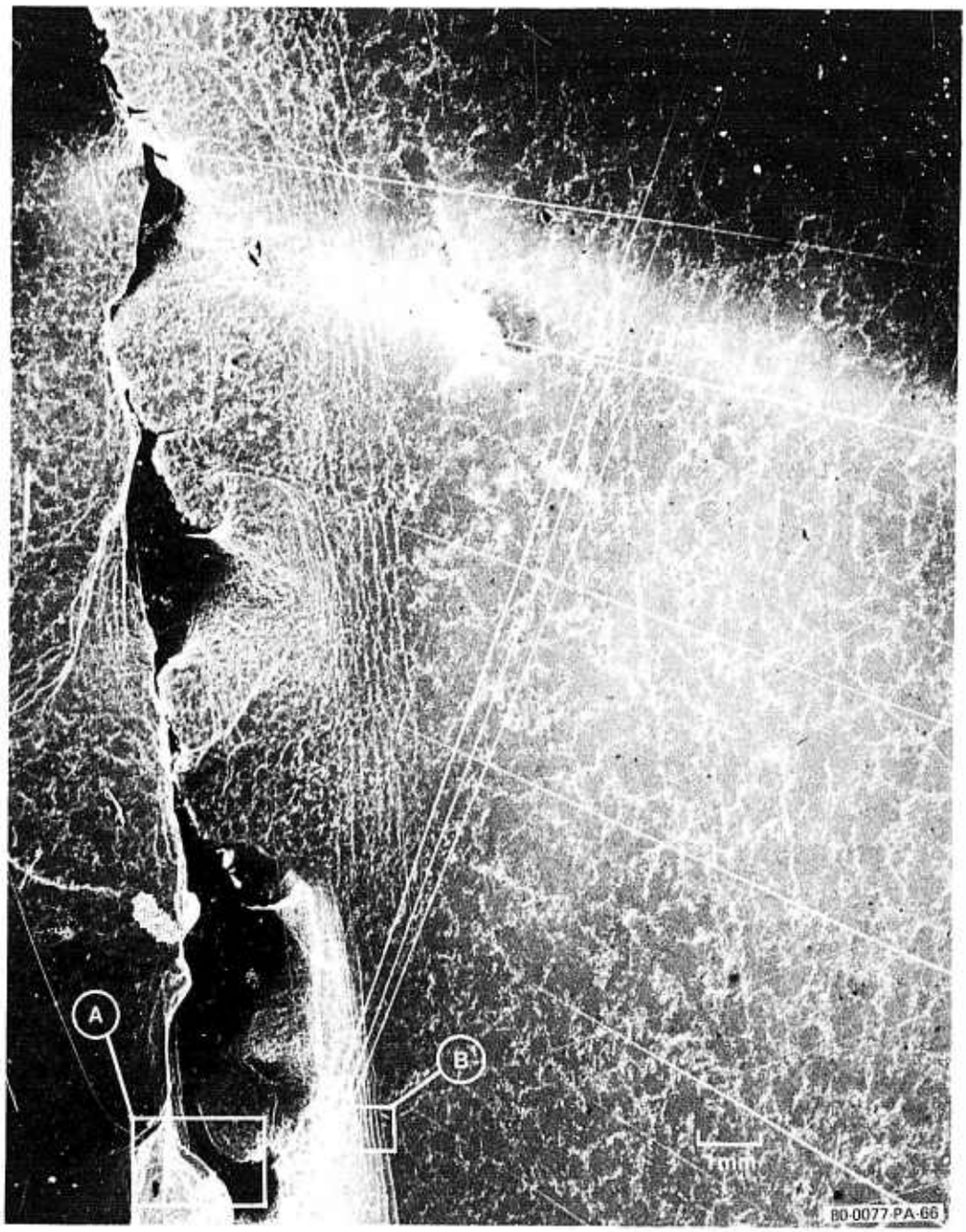

Figure A-10. Reflection X-Ray Topograph (g = <315>) of Boat-Grown GaAs Substrate Showing High Background Dislocation Density and Lineage Structure

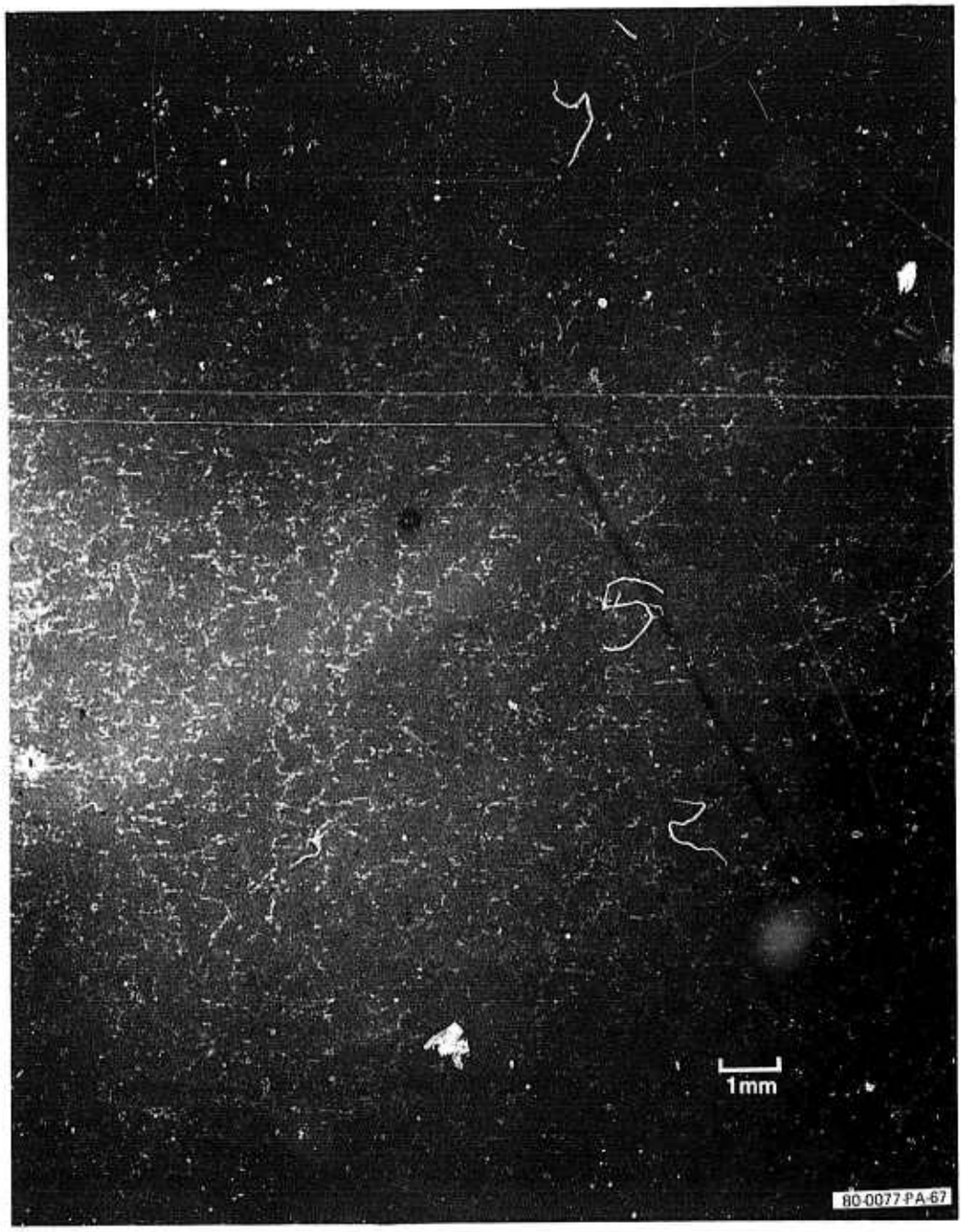

Figure A-11. Reflection X-Ray Topograph (g = <315>) of LEC-Grown GaAs Substrate-Material Pulled From Boron Nitride Crucible

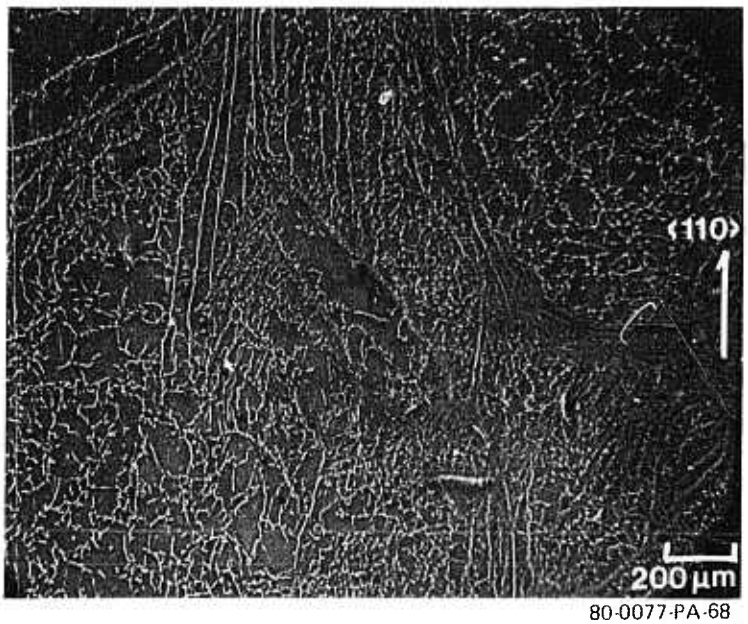

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Figure A-12a. High Density Dislocation in Boat-Grown Material Corresponding to Region A of Figure A-13 (Abrahams and Buiocchi et Chart)

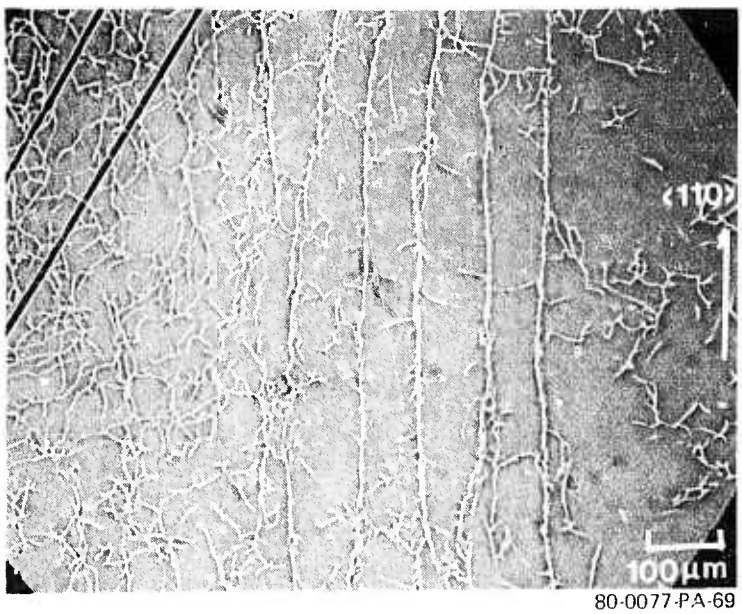

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Figure 12b. High Density Dislocation Lineage in Boat-Grown Material Corresponding to Region B of Figure A-13 (Abrahams and Buiocchi et Chart)

show regions of severe lineage since such features will quickly degenerate into a polycrystalline structure and cause single crystal growth to terminate.

Figure A-13 gives a comparison of the etch pit densities observed in boat-grown and LEC grown crystals. Dislocation densities in the low to mid 10^4-cm^{-2} range are typical of substrates from crystals presently being prepared by LEC growth at our laboratories.

A.3.2 Residual Impurity Content

Since carrier mobility is a strong function of the ionized impurity scattering, the availability of semi-insulating GaAs substrates of low residual-impurity content is of crucial importance to the development of a viable direct-ion-implantation FET technology. Table A-1 shows the results of mass spectrographic analysis comparing LEC-grown GaAs samples with substrates obtained from boat-grown crystals. These data, which were supplied through the courtesy of Metals Research Ltd., were obtained using

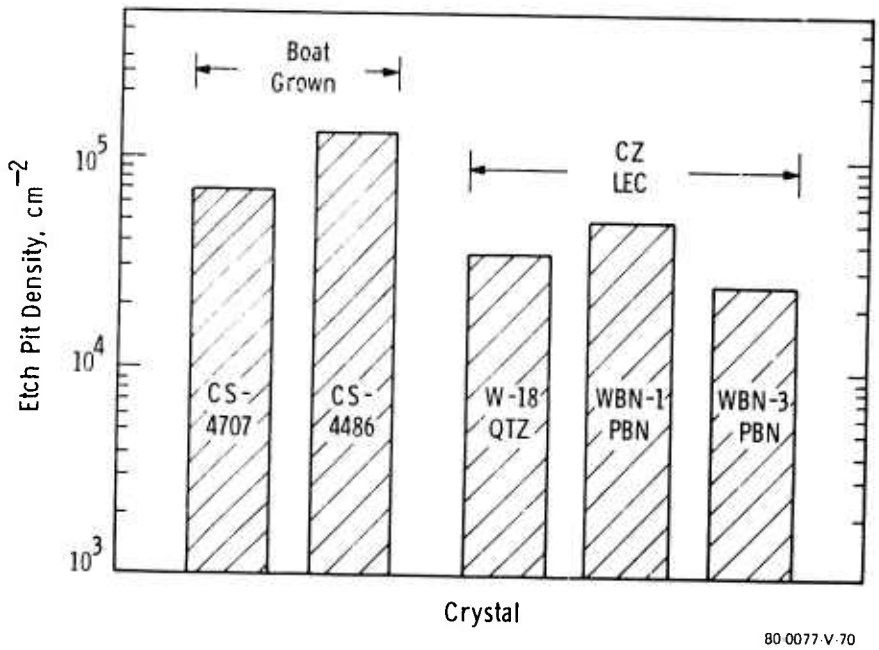

Figure A-13. Comparison of Etch Pit Densities in Large-Area LEC-Grown (3-in. Diameter) and Boat-Grown (2½-in. Max Dimension) GaAs Substrates

TABLE A-1

MASS SPECTROGRAPHIC ANALYSIS RESULTS (PPM, WT) FOR SEMI-INSULATING GaAs SUBSTRATES FROM DIFFERENT SUPPLIERS (DATA SUPPLIED BY METALS RESEARCH LTD)

Element \ Sample	LEC		Gradient Freeze	Horizontal Bridgeman
	Coracle	Manual (Undoped)		
B	0.2	1.0	--	--
Na	--	0.004	--	0.45
Mg	0.7	--	0.07	0.06
Al	0.01	0.01	0.4	0.3
Si	0.3	0.2	0.2	0.49
P	0.25	0.01	0.006	0.45
S	0.15	0.16	0.06	3.2
K	0.01	0.006	0.003	0.97
Ca	0.2	0.05	0.002	0.31
Cr	1.0	--	0.5	3.6
Fe	0.01	--	0.05	0.02
Ni	--	--	--	--
Cu	--	--	--	0.01
Zn	--	--	0.003	--
Te	--	--	--	0.88

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a JEOL-01 BM2 Spark Gap Mass Spectrometer at Plesseys Ltd., Caswell, England -- an instrument used exclusively for GaAs analyses. The data demonstrate residual shallow-donor impurities in the low 10^{16}-cm^{-3} range and Cr-dopant concentrations between 10^{16} and 10^{17} cm^{-3} in LEC growths at Metals Research Ltd.

The initial growths at Westinghouse have been directed towards improving the purity of semi-insulating GaAs crystals through the use of silicon-free, pyrolytic boron nitride crucibles. Secondary ion mass spectrometry (SIMS) bulk analyses of GaAs material pulled from both quartz and pyrolytic boron nitride crucibles are shown in table A-2 and compared with analyses of boat-grown GaAs. The data was obtained using a Cameca IMS3F ion microanalyzer at Charles Evans and Associates of San Mateio, Ca. SIMS data (in counts/sec) for a wide range of impurity species were obtained (using oxygen and cesium ion beams) but for clarity, only data for selected impurity species are shown in table A-2. The data permits comparisons between the residual impurity content of

TABLE 2

SIMS BULK ANALYSIS DATA (COUNTS/SEC) OF SELECTED IMPURITY SPECIES IN VARIOUS GaAs SUBSTRATES

	Boat-Grown		(W)-LEC Grown		
	Qtz	Qtz	Qtz	Qtz	PBN
C	35,000	17,000	48,000	19,000	15,000
O	335,000	205,000	757,000	245,000	203,000
Si	930	1,400	2,000	720	460
S	13,000	6,400	26,000	15,000	5,500
Se	60	20	210	10	30
Te	170	150	110	250	170
Cu	500	355	560	335	450
Zn	150	105	730	65	81
Mn	475	43	75	37	44
Cr	8,400	8,340	21,800	1,380	1,515

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different GaAs samples and clearly demonstrate that the lowest impurity content is achieved in LEC growths from pyrolytic boron nitride crucibles. The carbon, oxygen, and sulfur counts for this sample are near the detectable background of the SIMS instrument.

Quantitative analysis of the silicon and chromium concentrations can be obtained from the SIMS bulk-analysis data by profiling standard reference GaAs samples which have been implanted with silicon and chromium implants, respectively. The silicon and chromium concentrations in LEC- and boat-grown GaAs samples obtained this way are tabulated in table A-3. Residual silicon concentrations of less than 7×10^{15} cm^{-3} is observed in GaAs/PBN samples compared to levels in the low 10^{16}-cm^{-3} range in samples grown in quartz containers. The residual chromium content in undoped GaAs ranges from the low 10^{15} to 1×10^{16} cm^{-3}, compared with typical concentrations in the (1 to 2) $\times 10^{17}$-cm^{-3} range in CR-doped GaAs.

TABLE 3

QUANTITATIVE SIMS ANALYSIS OF Si AND Cr CONCENTRATIONS FOR GaAs MATERIAL GROWN UNDER VARIOUS CONDITIONS

		Silicon 10^{16} cm^{-3}	Chromium 10^{16} cm^{-3}
CS	Cr-doped/qtz	1.5	8.5
CS	Cr-doped/qtz	2	8
MR 123	Cr-doped/qtz	2	20
W-4	Cr-doped/qtz	1.5(seed) 2(tang)	6(seed) 22(tang)
W-18	Undoped/qtz	1	1
WBN-1	Undoped/PBN	0.7	1
WBN-3	Undoped/PBN	0.5	0.2
W-19	Cr-doped/qtz	1	4(tang)
WBN-4	Cr-doped/PBN	0.5	2(seed)

CS denotes boat-grown substrates from Crystal Specialties

MR denotes LEC substrates from Metals Research

W denotes LEC substrates grown at Westinghouse

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Figure A-14 illustrates SIMS profiling of a typical power FET channel formed by ^{29}Si implantation into LEC-grown Cr-doped GaAs substrate. The data indicate the pile-up of the chromium impurities at the surface, due to Cr redistribution during annealing, and silicon, due to knock-on events during implantation. The redistribution of silicon and chromium in undoped GaAs/PBN substrates following implantation, nitride capping, and annealing is currently being investigated. The much lower concentrations of residual chromium and silicon concentrations anticipated in these samples is depicted in figure A-14.

A.3.3 Electrical Characterization

In addition to chemical impurity analyses, improvements in semi-insulating GaAs substrates for both Cr-doped and undoped material can be assessed through electrical and thermal stability characterization as well as by measurements of transport properties of active FET layers formed by direct ion implantation. Unfortunately, direct measurements of the carrier mobilities and net

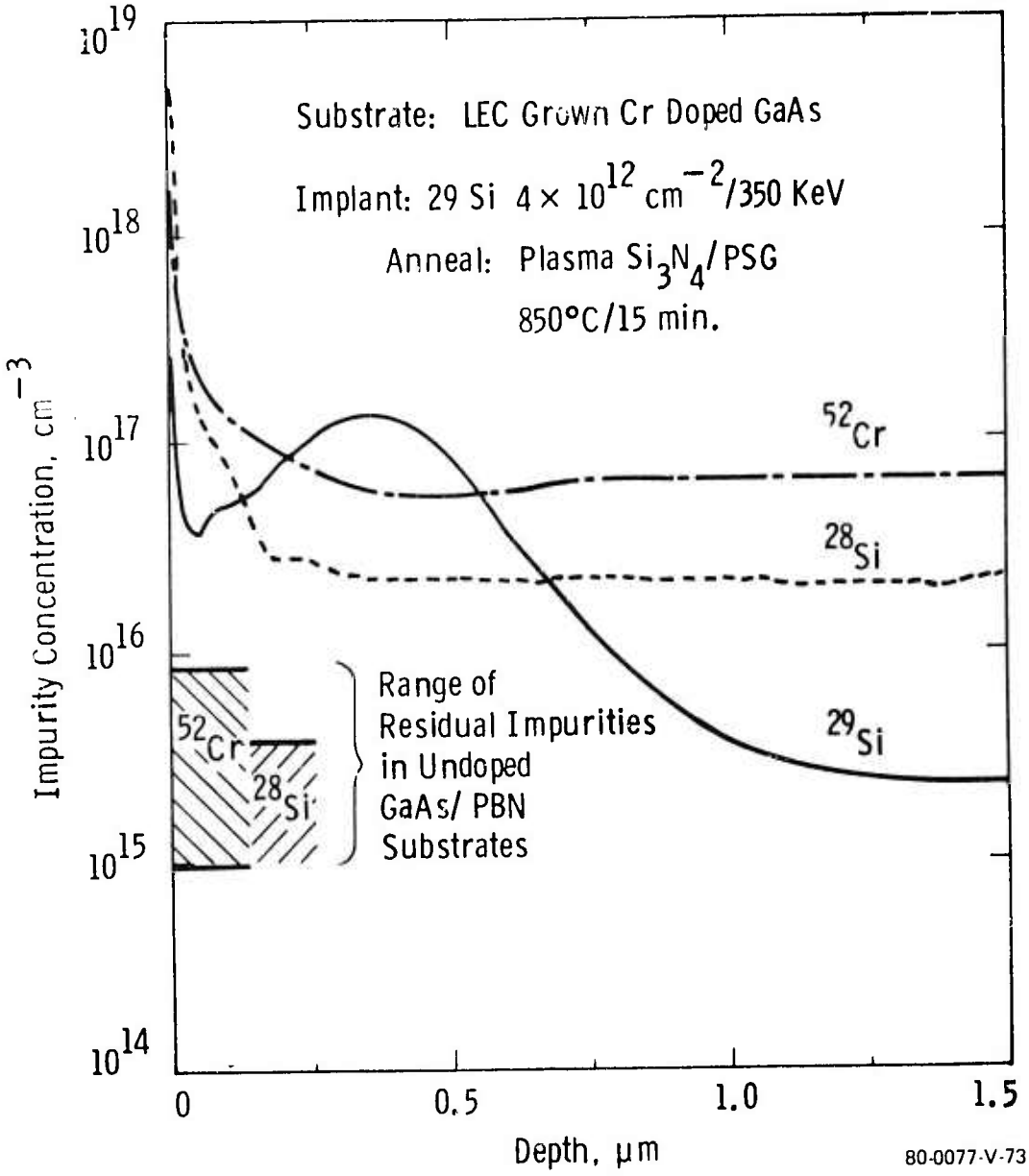

Figure A-14. SIMS Profiles of Silicon and Chromium Distributions in Cr-Doped GaAs Substrate Implanted with ^{29}Si, Capped and Annealed

TABLE A-4

RESISTIVITY MEASUREMENTS FOR AS-GROWN SUBSTRATES FROM GaAs CRYSTALS GROWN UNDER VARIOUS CONDITIONS

Crystal and Remarks		Resistivity (Ω cm)
BOAT-GROWN		
CS	Cr-doped/qtz	2×10^9
CS	Cr-doped/qtz	2×10^9
CS	Cr-doped/qtz (4486)	4.7×10^8
LEC-GROWN		
MR 123	Cr-doped/qtz	3×10^9
W-4	Cr-doped/qtz (seed end)	5.8×10^8
W-4	Cr-doped/qtz (tang end)	1.4×10^9
W-8	Cr-doped/qtz (seed end)	4.7×10^8
W-8	Cr-doped/qtz (mid boule)	8.0×10^8
W-8	Cr-doped/qtz (tang end)	4.3×10^8
W-18	Undoped/qtz (seed end)	2.5×10^3
W-18	Undoped/qtz (mid boule)	2.4×10^3
W-18	Undoped/qtz (tang end)	2.4×10^3
W-19	Cr-doped/qtz (seed end)	5.2×10^8
W-19	Cr-doped/qtz (mid boule)	7.7×10^8
W-19	Cr-doped/qtz (tang end)	1.0×10^9
W-23	Undoped/qtz (seed end)	9.0×10^5
W-23	Undoped/qtz (mid boule)	2.2×10^7
W-23	Undoped/qtz (tang end)	2.7×10^7
WBN-1	Undoped/PBN (seed end)	8.0×10^7
WBN-3	Undoped/PBN (seed end)	2.8×10^7
WBN-3	Undoped/PBN (mid boule)	8.8×10^7
WBN-4	Cr-doped/PBN (seed end)	7.4×10^8
WBN-6	Undoped/PBN (seed end)	4.8×10^7

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donor and acceptor concentrations in the semi-insulating GaAs substrate itself are made difficult by the very high sample impedance and the complexity of data interpretation.*

Substrate qualification is based principally upon achieving: (1) $\gtrsim 10^7$-ohm-cm range resistivities in the substrate material, before and after it is subjected to thermal annealing and (2) high electron mobilities in active layers implanted directly in the substrate. Table A-4 shows measurements of resistivity for As grown substrates from GaAs crystals grown under various conditions. The data demonstrate (WBN-3 and WBN-6) that resistivities approaching 10^8 ohm-cm can be obtained in As-grown, undoped GaAs crystals pulled from high-purity silicon-free boron nitride crucibles without resorting to the addition of a compensating chromium dopant during growth, as is normally required for growths from standard silica crucibles. In contrast, undoped GaAs crystals pulled from standard quartz crucibles show wide variations in substrate resistivity. For example, as shown in table A-4, crystal W-18 pulled from a standard quartz crucible yielded material with resistivities in the 3×10^3-ohm-cm range while another crystal, W-23, pulled under near identical conditions yielded material with resistivities in the 10^6 to 10^7-ohm-cm range over the entire crystal length. Variable-temperature Hall effect measurements of undoped GaAs grown from a quartz crucible are shown in figure A-15. The data indicates a relatively deep donor impurity with $N_D \sim 10^{17}$ cm^{-3} and $E_D = 0.43$ eV for this low resistivity substrate.

After establishing the semi-insulating behavior of the as-grown GaAs substrates, the polished slices are qualified further by means of a resistivity measurement, immediately following an encapsulated anneal of the semi-insulating slice, to determine whether any conducting surface layers have formed as a result of thermal treatment. The encapsulation consists of a 500-Å plasma-enhanced Si_3N_4 deposition overlaid with 1500Å of 420°C CVD phosphorus-doped glass (PSG) applied to both surfaces. The wafers are annealed for 20 minutes at 860°C in flowing forming gas, after which the encapsulant is stripped and the resistivity measurement is made.

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*D.C. Look, "On the Characterization of Semi-insulating GaAs by Hall, Photo-Hall, Photoconductivity and Photomagnetoelectric Measurements," J. Elec. Materials, 7:147 (1978).

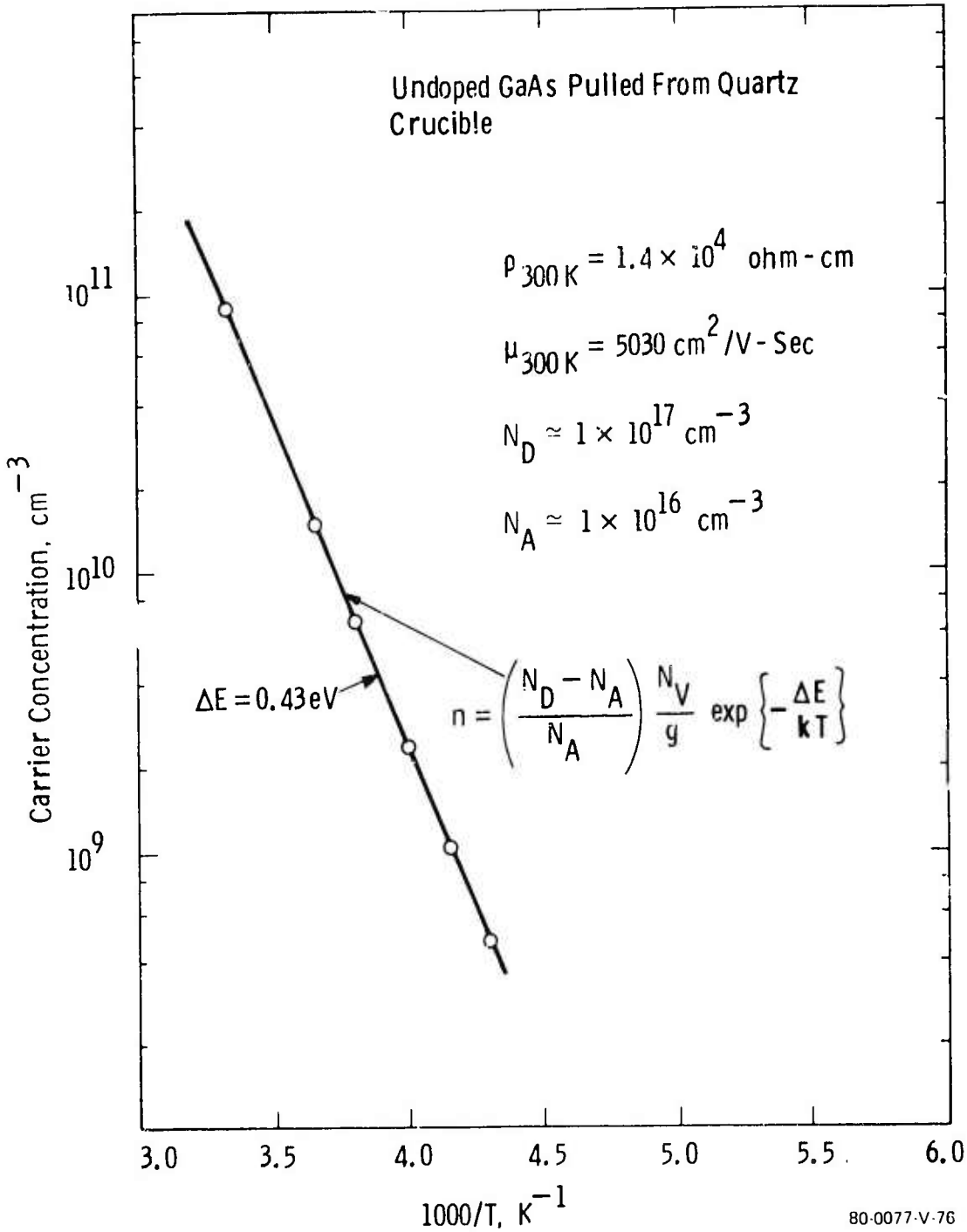

Figure A-15. Hall Effect Analysis of High Purity GaAs Grown Under Undoped Melt in Quartz Crucible

If the surface sheet resistance exceeds $10^6\ \Omega/\square$, the wafer is judged to satisfy the qualification criterion for direct ion implantation. Undoped GaAs substrates from ingots pulled from PBN crucibles show no degradation of semi-insulating behavior as a result of thermal treatment. For example, the undoped wafers of crystal WBN-3 exhibited sheet resistances in 10^9 $\Omega/\square$ -range in the As-grown state and in the 10^8-$\Omega/\square$ range after thermal treatment.

Substrates regarded as suitable for direct ion implantation are implanted under the following conditions:

Substrate temperature:	Ambient
Alignment:	7 deg off <100>
Implant species:	Si^{29},
Dose:	$3 \times 7 \times 10^{12}\ cm^{-2}$
Energy:	200 to 400 keV

Parallel implants are carried out at several different doses on bare and encapsulated substrates. For the encapsulated substrates, the encapsulation is identical to that used for the unimplanted anneal. After implantation, the active implants are profiled by capacitance-voltage techniques to determine profile integrity and to estimate activation efficiencies.

Assessment of the influence of the substrate-impurity content can be obtained indirectly from Van der Pauw Hall characterization of the active FET n-type layer to determine the activation efficiency and the carrier mobility in the implanted layer. Table A-5 gives active channel mobilities and activation efficiencies for several GaAs substrates which have undergone implantation and electrical characterization. ^{29}Si implants into semi-insulating GaAs/PBN substrates have resulted in the highest electron mobilities which have been reported to date. Channel implants with peak donor concentrations between 0.8 and $1.3 \times 10^{17}\ cm^{-3}$ show low-field Hall mobilities which fall within the 4,800 to 5,000-cm^2/V-sec range, compared with mobilities of about 4,200 cm^2/V-sec for Cr-doped GaAs substrates prepared by LEC or boat growth. A mobility of about 5,200 cm^2/V-sec is predicted

TABLE 5

ACTIVE CHANNEL MOBILITIES AND RAW ACTIVATION EFFICIENCIES FOR GaAs SUBSTRATE MATERIAL GROWN UNDER VARIOUS CONDITIONS

Substrate		Implant [Dose (cm^{-2}) and Energy (kev)]	Mobility (cm^2/v-sec)	Raw Activation Efficiency (%)
BOAT-GROWN				
CS	Cr-doped/qtz		3800 - 4200	30 - 90
LEC-GROWN				
W-4	Cr-doped/qtz		4200	
WBN-1	Undoped/PBN	4×10^{12} @ 350	4680	75
		5×10^{12} @ 350	4715	
		3.5×10^{12} @ 350	4780	
		4.5×10^{12} @ 300	5060	
WBN-3	Undoped/PBN	4×10^{12} @ 350	4780	
		5×10^{12} @ 350	4760	
		3.5×10^{12} @ 300	4785	
		4.5×10^{12} @ 300	4560	

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theoretically for this doping level. Recently, an electron mobility of 5,600 cm^2/V-sec has been measured in lightly-doped channel layers (6×10^{16} cm^{-3}) formed by direct implantation and a series of experiments to determine direct implanted channel mobilities at low implantation doses are presently in progress to demonstrate the very high purity of semi-insulating GaAs grown from pyrolytic boron nitride crucibles. The measured mobilities in directly-implanted channel layers in semi-insulating GaAs/PBN substrates and in Cr-doped GaAs substrates are compared to theoretical bulk mobilities in figure A-16. In addition to these high direct-implant channel mobilities, implants into undoped GaAs/PNB substrates exhibit consistent and reproducibly high activation efficiencies of about 75 percent (versus variable activation efficiencies ranging from 30 to 90 percent in Cr-doped GaAs substrates) and predictable implant profiles which exhibit high uniformity over large substrate areas and from slice-to-slice. (See Appendix E.)

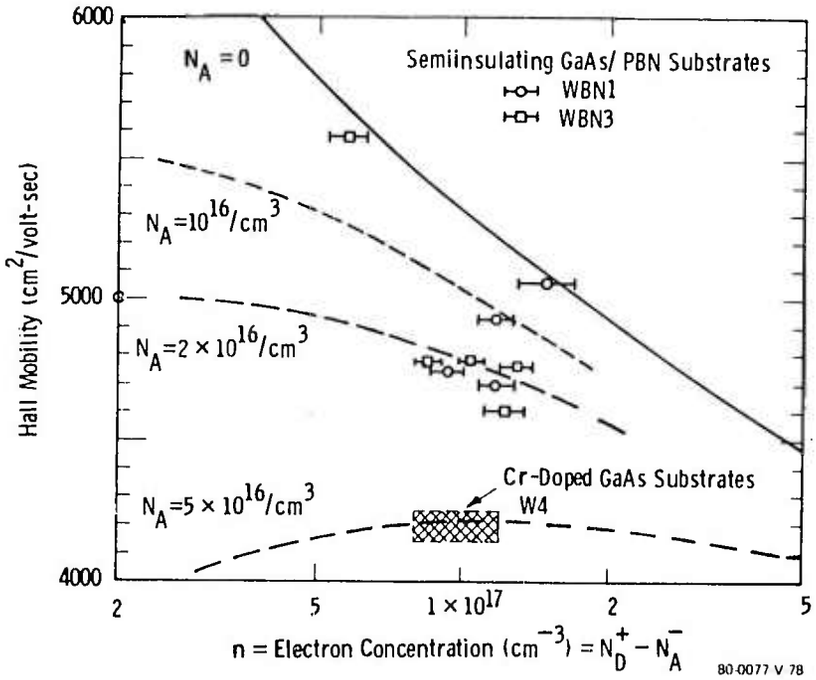


Figure A-16. Measured Directly Implanted Channel Mobilities in Cr-Doped GaAs and Undoped GaAs/PBN Substrates Compared with Theoretical Bulk Mobilities

APPENDIX B
OHMIC CONTACTS

APPENDIX B
OHMIC CONTACTS

B.1 INTRODUCTION

Good ohmic contacts are essential to the performance of both power and low-noise field-effect transistors (FET's). For power transistors, the source contact resistance can be a major parasitic resistance. For low-noise devices, the thermal noise in the source contact is a gate-to-source noise voltage which will be amplified along with the weak input signal. Hence, the reduction of the source and drain ohmic-contact resistance in Westinghouse power FET's represents a major accomplishment in the present phase of this contract.

Our investigation focused on alloyed-junction ohmic contacts. These contacts can be fabricated by techniques which are compatible with monolithic circuit-fabrication techniques. Typically, a thin film of eutectic composition AuGe is electron-beam evaporatd onto a clean GaAs surface. Further films of Ni, Pt, Pd, Au, or TiW are deposited on top of the AuGe to form a sandwich with desirable electrochemical and mechanical properties. Then the wafer and the metal sandwich is heated in a reducing atmosphere to cause interdiffussion of the metals and the GaAs. Upon cooling, epitaxial regrowth forms a metallurgical junction, which has a high electrical conductance per unit area (mhos/cm^2). The inverse of this quantity is the specific contact resistance, with units of (ohm-cm^2).

We found that certain aspects of the fabrication procedure and equipment design were just as important for making good contacts as was the composition of the particular metallization system. Most important among these are the cleaning of the GaAs surface prior to metals deposition, the design and use of the alloying boat, and proper control of the alloy furnace atmosphere. Because of uncontrolled variables in these areas, Westinghouse ohmic contacts were typically in the high 10^{-5} to low 10^{-4} ohm-cm^2 range

one year ago. Improvements made as a result of the recent effort in this area have allowed us to produce 3.5×10^{-6} ohm-cm^2 typical ohmic contacts.

B.2 MECHANISM OF CONTACT FORMATION

The fundamental mechanism by which the ohmic contacts are formed is due to the interaction of heated AuGe on GaAs. Ga is soluble in Au and, hence, it outdiffuses into the metal allowing the Ge to diffuse in and substitute for the Ga. On the periodic chart of the elements, Ga, Ge, and As follow sequentially; therefore, the substitution of group IV Ge for the group III element Ga provides an ideal n-type donor. Consequently, a degenerate n+ region forms at the boundary of the metallurgical junction.

Other metals are deposited along with the AuGe to improve the quality of the ohmic contact. Nickel is especially beneficial because it wets the GaAs, thereby making a more uniform contact. Nickel also alloys with any excess germanium to prevent balling of the ohmic metalization. Platinum is also helpful because it is a dense metal which remains chemically inactive in these circumstances and seals the contact with a film that resists oxidation. These effects were seen in our early results, which caused us to change to our present ohmic metallization of 1100Å AuGe, 500Å Ni, and 400Å Pt.

B.3 EXPERIMENTAL CONSIDERATIONS

B.3.1 Equipment

The alloying furnace is a resistance-heated, clamshell-type tube furnace. The quartz tube has an inner diameter of 5.5 cm and is 100-cm long. The capped end of the tube extends out into the laboratory for room temperature loading and unloading of the wafer. Measurements of the temperature profile along the axis of the tube identified a 3-1/2-in. long flat zone where the temperature is constant to $\pm$ 10°C. Alloying is always done at the center of this flat zone.

A reducing atmosphere for the alloying furnace is provided by flowing a mixture of 10 percent hydrogen and 90 percent nitrogen through the quartz tube. Our flow rate is monitored at 1.2 ft^3/h,

which provides one tube volume of gas every five minutes. When the furnace is not in use for alloying, it is maintained at operating temperature (set point = 720°C) with dry nitrogen flowing at 1.2 ft^3/h. To prepare for alloying, the forming gas is turned on for half an hour before the wafer is loaded into the alloying boat. Then an additional half hour purge is done before the boat is inserted into the hot region of the furnace. These long purges with forming gas are an improvement in the procedure which ensures a moisture-and oxygen-free atmosphere for alloying.

During alloying, the wafers are carried in a massive graphite boat which is supported by a quartz push rod (see figure B-1). The boat is approximately 3 in. long by 2 in. wide by 1/8 in. thick. It has a 1/8 in. thick removable lid. A chromel-alumel thermocouple is embedded in the boat to monitor its temperature during alloying.

One important function provided by the thick graphite boat is the reduction or elimination of radial and axial thermal gradients in the furnace. Measurements made during the alloying cycle

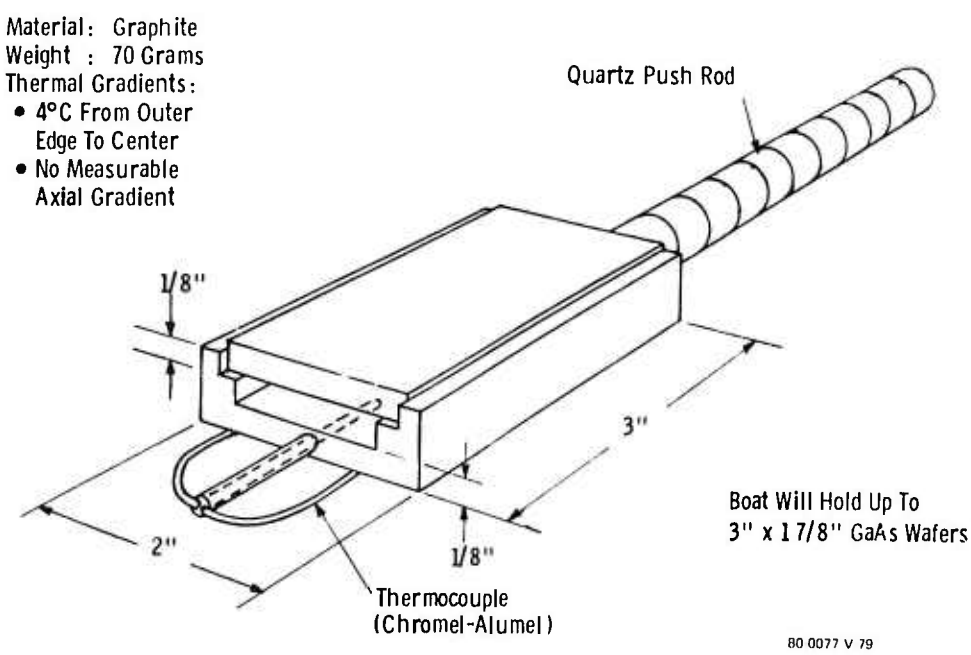


Figure B-1. For Alloying Large GaAs Slices

indicate a maximum of $4^{o}C$ variation from edge to center of the boat and no detectable axial variation. Thus, we are assured of uniform heating for even a large 2-in. x 2-in. wafer. This is a significant improvement over the old alloying boat which consisted of two 10-mil thick graphite sheets. Radial variations of $40^{o}C$ were possible with the old system. Further, axial variations of $80^{o}C$ were possible because the old procedure did not always alloy in the flat zone of the furnace.

Another important advantage of the massive boat is in the repeatability of the alloying temperature cycle. The total mass of the boat plus lid is 70g. Even a large GaAs wafer (2 in^2 x 15 mils) will have a thermal mass 55 times smaller than the boat. Since the heat capacity of the wafer is such a small fraction of the total, the time vs temperature cycle no longer depends on the size of the wafer. So in contrast to results obtained on strip heaters, our test results from small chips work equally well for full-size wafers.

B.3.2 Procedure

To test the merits of a particular ohmic-contact metallization scheme, we start with a clean GaAs wafer and photolithographically define a test pattern. Then, immediately prior to metallization, a clean GaAs surface is prepared by doing a light surface etch. After metallization, the photoresist is dissolved and unwanted metal is rejected, then the wafer is scribed into many small chips. The test chips are alloyed at different temperatures, then measured. The results are plotted to show specific contact resistance vs alloying temperature. Desirable qualities are very low contact resistance at some particular alloying temperature and acceptably low contact resistance ($< 4 \times 10^{-6}$ ohm-cm^2 for this study) over a wide temperature range.

Very early in this series of experiments, we demonstrated the importance of the preclean etch prior to metallization. Our earliest tests were done on vapor-phase epitaxial GaAs using a AuGe/Ni/Pt metallization. Without a preclean etch step, the best result obtained was a specific contact resistance $R_C = 2 \times 10^{-5}$

ohm-cm^2. After these results, a preclean etch was always included in the process.

Our best preclean-etch procedure begins with a five-minute soak in 1:1, concentrated hydrochloric acid:water, which removes surface oxides. The GaAs etch is made of equal parts of ammonium hydroxide (27 percent NH_3) and hydrogen peroxide (30 percent diluted one part to 400 parts of water. The GaAs is etched for two minutes, which removes 400A from the surface, then put in a stop bath of one part ammonium hydroxide to 15 parts water. Wafers are removed from the stop bath and blown dry without a rinse. They are immediately put under vacuum in the metallization system. Exposure to room air is never allowed to exceed four minutues after the stop bath.

After metallization, rejection of unwanted metal, and scribing into chips, the chips are ready for alloying. The furnace tube is thoroughly flushed with forming gas, as previously described. Alloying is done by a peak-temperature method. To begin the alloying cycle, the alloying boat is inserted by means of the quartz push rod into the center of the flat-temperature zone of the furnace. The alloying boat sits in the center of the flat zone while its temperature rise is monitored. When the thermocouple voltage indicates that the desired peak-alloying temperature has been reached, the boat is withdrawn from the furnace and allowed to cool in the room-temperature end of the tube. The chip remains in the forming-gas atmosphere until it has cooled to below 200°C. Then the furnace tube may be uncapped and the chip removed from the boat. Figure B-2 shows the time vs temperature alloy cycle for a 460°C alloy temperature. If the boat were left in the furnace indefinitely, its steady-state temperature would reach 620°C.

B.3.3 Measurement

Each test chip contains about 40 test patterns. Measurements are made on about six test patterns to determine the contact resistance. An ohmic-contact test pattern and sample-contact resistance calculation are shown in figure B-3. The test pattern consists of

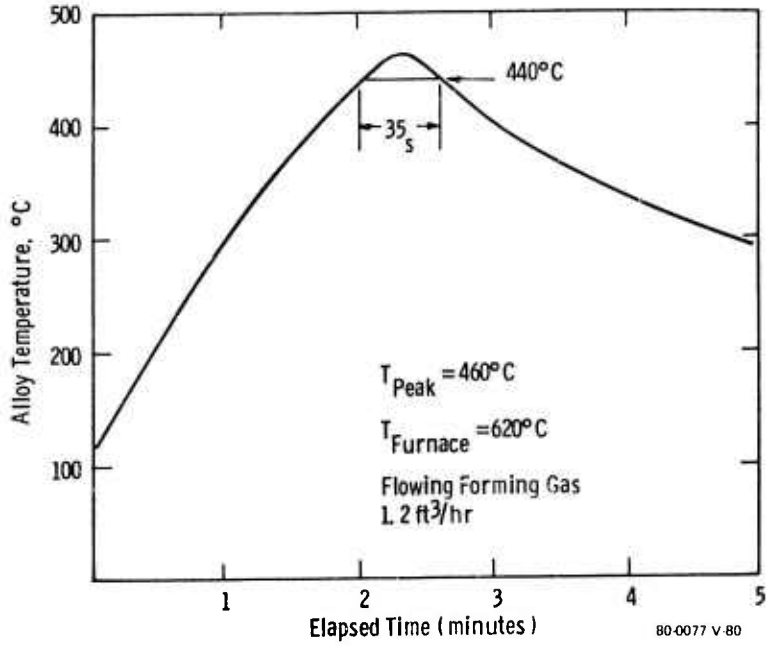


Figure B-2. Alloy Cycle for Ohmic Contacts to GaAs Using Massive Graphite Boat

six dots in a field with graduated rings surrounding the dots. The six rings have a mean diameter of 100 μm. The rings make gaps in the contact metallization which are graduated from 2.5 μm up to 16 μm.

Measurements are made by passing a constant current (typically 10 mA) from a dot to the surrounding field and recording the voltage which develops across the gap. Effects due to probe-contact resistances are avoided by using the four-point probe method. Gap size is determined by photographing the rings for one pattern at 1000X. Then the photographs are measured with a ruler.

Calculations of the ohmic-contact resistance is done with the aid of a Hewlett-Packard Model 9815 Programmable Calculator. Input data are the test current and gap size vs voltage. A linear least-squares fit to the gap vs voltage data is extrapolated back to the gap spacing which gives zero voltage. This spacing is a negative number whose absolute value corresponds to twice the transfer

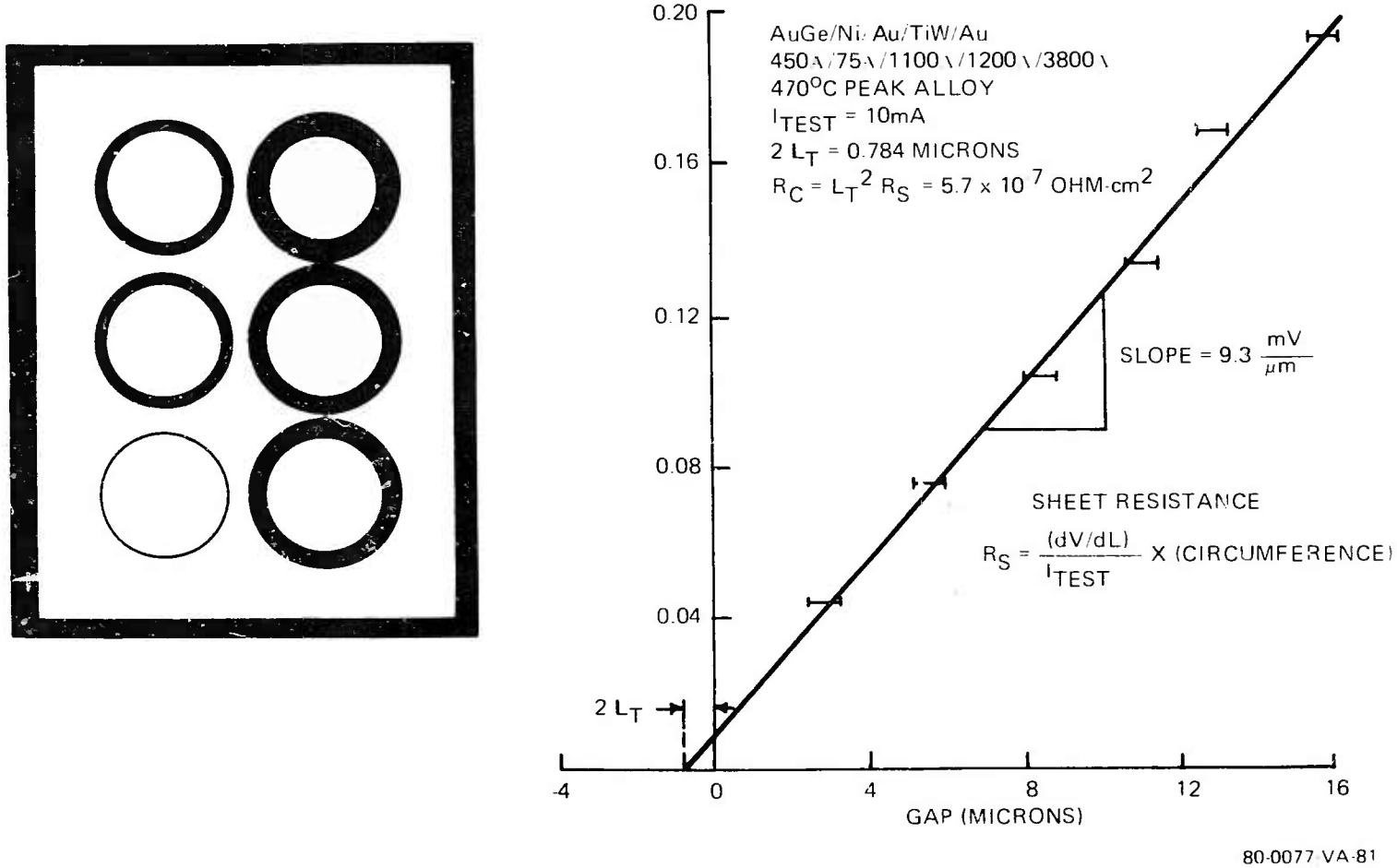


Figure B-3. Ohmic Contact Test Pattern and Sample Contact Resistance Calculation

length. The meaning of the transfer length (L_T) is illustrated in figure B-4. For our planar geometry, the amount of current flowing from the semiconductor into the ohmic contact falls off exponentially from the edge contact. The characteristic decay length is called the transfer length. The sheet resistance of the semiconductor (R_S) is calculated from the slope of the gap spacing vs voltage, knowing the test current and sample geometry. Finally, the specific contact resistance is calculated from the formula, $R_C = R_S (L_T)^2$.

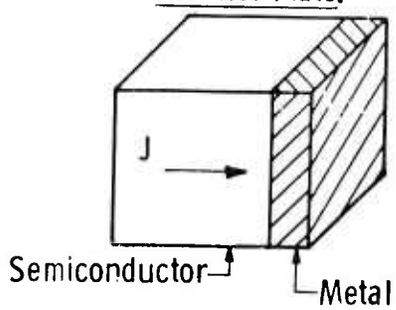
The largest source of error in the measurement is in the determination of the gap ring size. Random errors in a good data set contribute about 0.15-micron uncertainty to the measurement of L_T. Systematic error in deciding which visible features correspond to the edge of the ohmic contact can be easily contribute another 0.15-micron error (that is 0.15 mm on a 1000X photograph). On our typical test wafer with a sheet resistance of 400 $\Omega/\square$, a specific contact resistance of $10^{-6}\ \Omega$ - cm^2 represents a transfer length of 0.5 micron. This is about the same size as our random-plus-systematic error of 0.3 micron. Thus, we are wary whenever our measurements indicate less than $10^{-6}\ \Omega$ -cm^2 specific-contact resistance. We can only state with certainty that such contacts are indeed very good contacts.

B.3.4 Results and Discussion

The typical dependence of specific-contact resistance on alloying temperature is illustrated in figure B-5. Below about 410°C, there is insufficient interdiffusion of the GaAs and the ohmic metallization, which results in a non-ohmic contact. Above that temperature, the Au-Ga alloy etch of the GaAs surface is activated to the extent that oriented epitaxial regrowth occurs upon cooling. The ohmic contact is made through these epitaxial regions.* The quality of the ohmic contact and the size of the epitaxial regions increase with temperature until about 470°C. Above that temperature, random precipitation occurs upon cooling, which degrades the ohmic contact. The net effect is to give a parabola-shaped plot for specific-contact resistance vs temperature, with the resistance minimum occurring around 470°C.

* A. Christou, Solid-State Electronics 22, 141 (1979).

Parallel Plate:



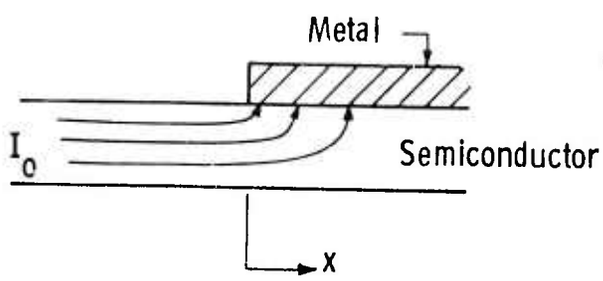
At the Interface We Get a Conductance Per Unit Area (mhos/ cm^2)

$G_c = J/V_c$ J = Current Density

V_c = Voltage Drop Across Contact

$R_c = 1/G_c$ (ohm - cm^2)

Planar:



- $I = I_0 e^{-x/L_T}$

  Where I_0 = Total Current

  L_T = Transfer Length

  R_s = Sheet Resistance of Semiconductor

- $L_T = \sqrt{\frac{R_c}{R_s}}$

  or

- $R_c = (L_T)^2 R_s$

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Figure B-4. Definitions of Specific Contact Resistance

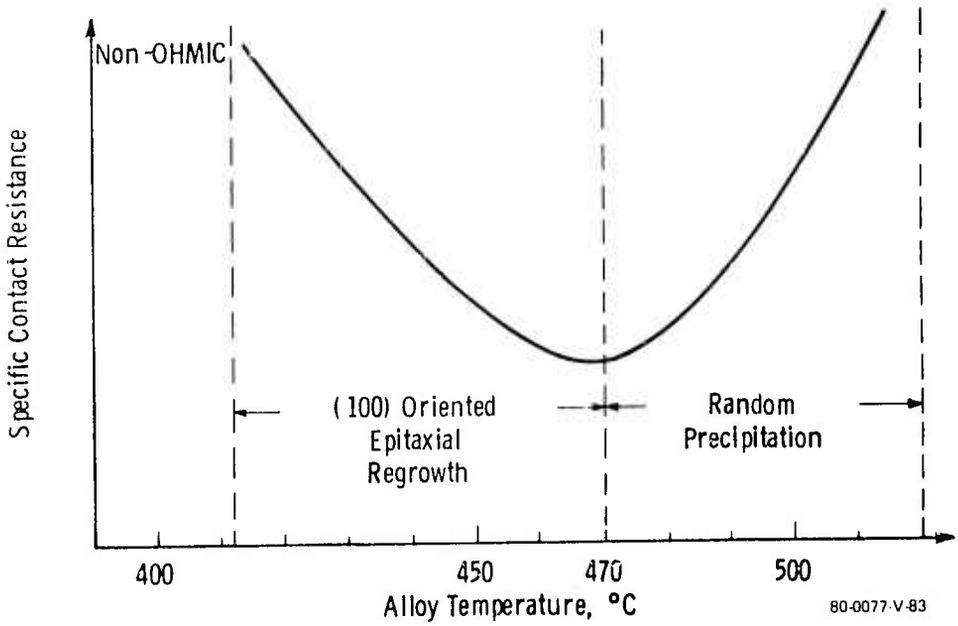

Figure B-5. Dependence of AuGe Based Ohmic Contacts to GaAs on Alloy Temperature

During the course of the program, we investigated several different metallization schemes. These are listed in table B-1 and their specific-contact resistance vs temperature behaviors are plotted in figure B-6. The wafers were implanted with Si directly into Cr-doped substrates. A deep-channel implant and a surface-fill implant resulted in a carrier density of about 10^{17} cm^{-3} at the contact.

The results from the AuGe/Ni/Pt metallization show possible Cr interference. It is well known that Cr can outdiffuse to the surface during the post-implantation anneal** (see figure B-7). To check this possibility, we split a wafer and etched 1000Å from the surface of one half, then processed both halves identically. The results from these halves are replotted in figure B-8 along with results obtained with this metals system on the earlier epitaxial material. The etched half-wafer shows the expected parabolic dependence of contact resistance on alloying temperature, with an acceptable minimum $R_C = 3.0 \times 10^{-6}$ Ω-cm^2.

** Huber, et al.

TABLE B-1

METALLIZATION SCHEMES

Metallization	R_c^{min}	@ T
1200Å AuGe/500Å Ni	1.4×10^{-5} Ω-cm^2	@ 580°C
600Å AuGe/500Å Pd	3.5×10^{-6}	470°C
1100Å AuGe/500Å Ni/400Å Pc	3.0×10^{-6}	500°C
450Å AuGe/75Å Ni/1075Å Au	2.0×10^{-6}	500°C
450Å AuGe/75Å Ni/1075Å Au/1200Å TiW/3800Å Au	4.0×10^{-7}	500°C

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The unetched half-wafer shows no such parabola and high contact resistance over the whole temperature range, $R_C = 1.4 \times 10^{-5}\ \Omega\ cm^2$. Since the data from the epitaxial material were taken before the new boat and alloying procedure were in use, they cannot be plotted as a parabola. The range of the results, however, shows that R_C's in the low $10^{-6}\ \Omega$-cm^2 range can be expected with the AuGe/Ni/Pt metallization. This Cr-interference effect also explains the erratic behavior of the AuGe/Ni sample.

Our best results were obtained with the AuGe/Ni/Au/TiW/Au metallization. These results are replotted for emphasis in figure B-9. Not only did it give a low minimum-contact resistance of $4 \times 10^{-7}\ \Omega$-cm^2 at 500°C, but it also gave excellent results at 470°C and 530°C. On these three test chips, a total of 18 test patterns were measured. An average value of $1.0 \times 10^{-6}\ \Omega$-cm^2 was observed, and every pattern tested had a specific contact resistance less than $1.7 \times 10^{-6}\ \Omega$-cm^2. A histogram of this result is shown in figure B-10. Also shown in figure B-10 is the percent of the gate-to-source parasitic resistance which would

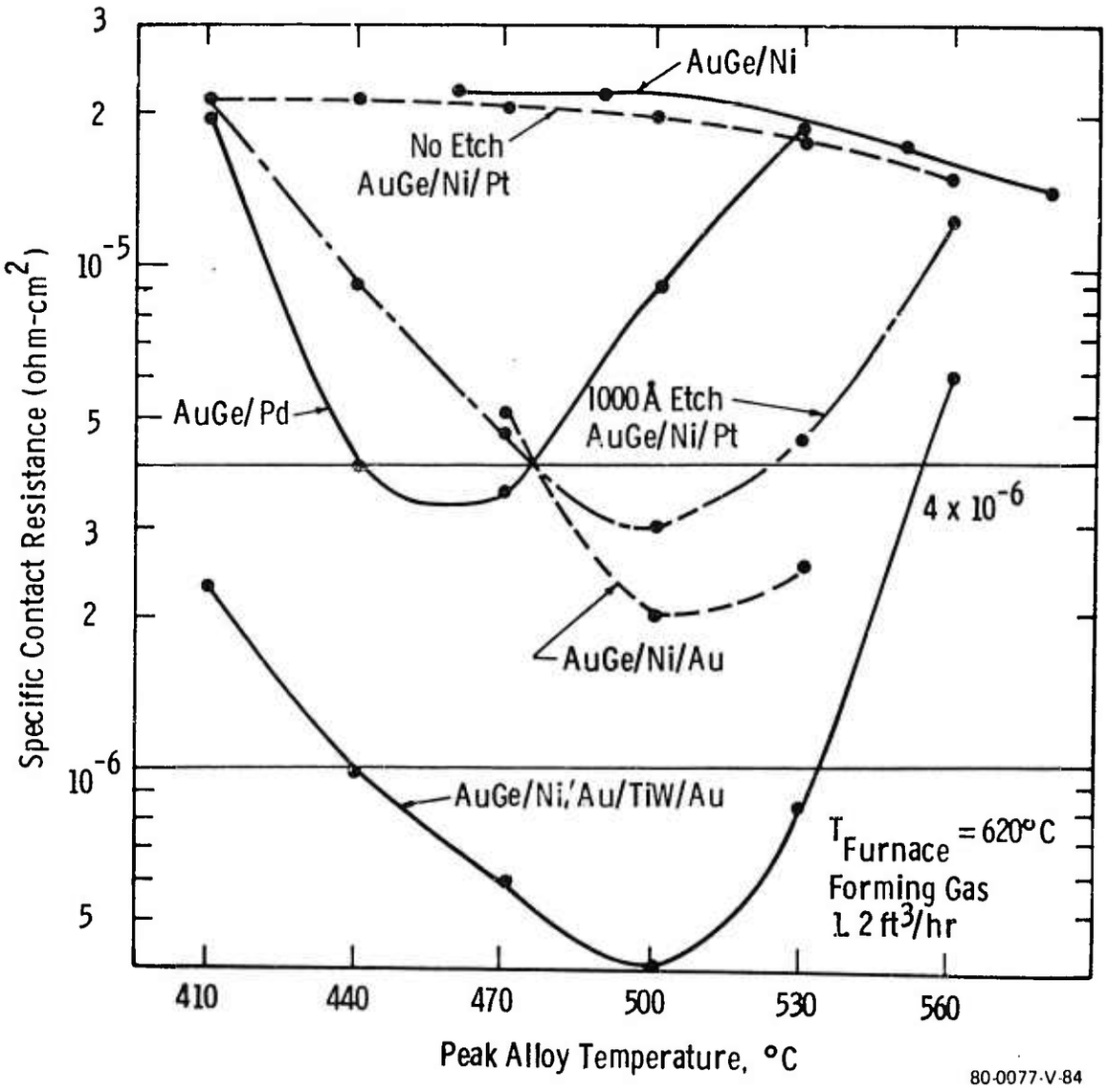

Figure B-6. Specific Contact Resistance of Five Contact Metallizations on Direct Ion-Implanted GaAs

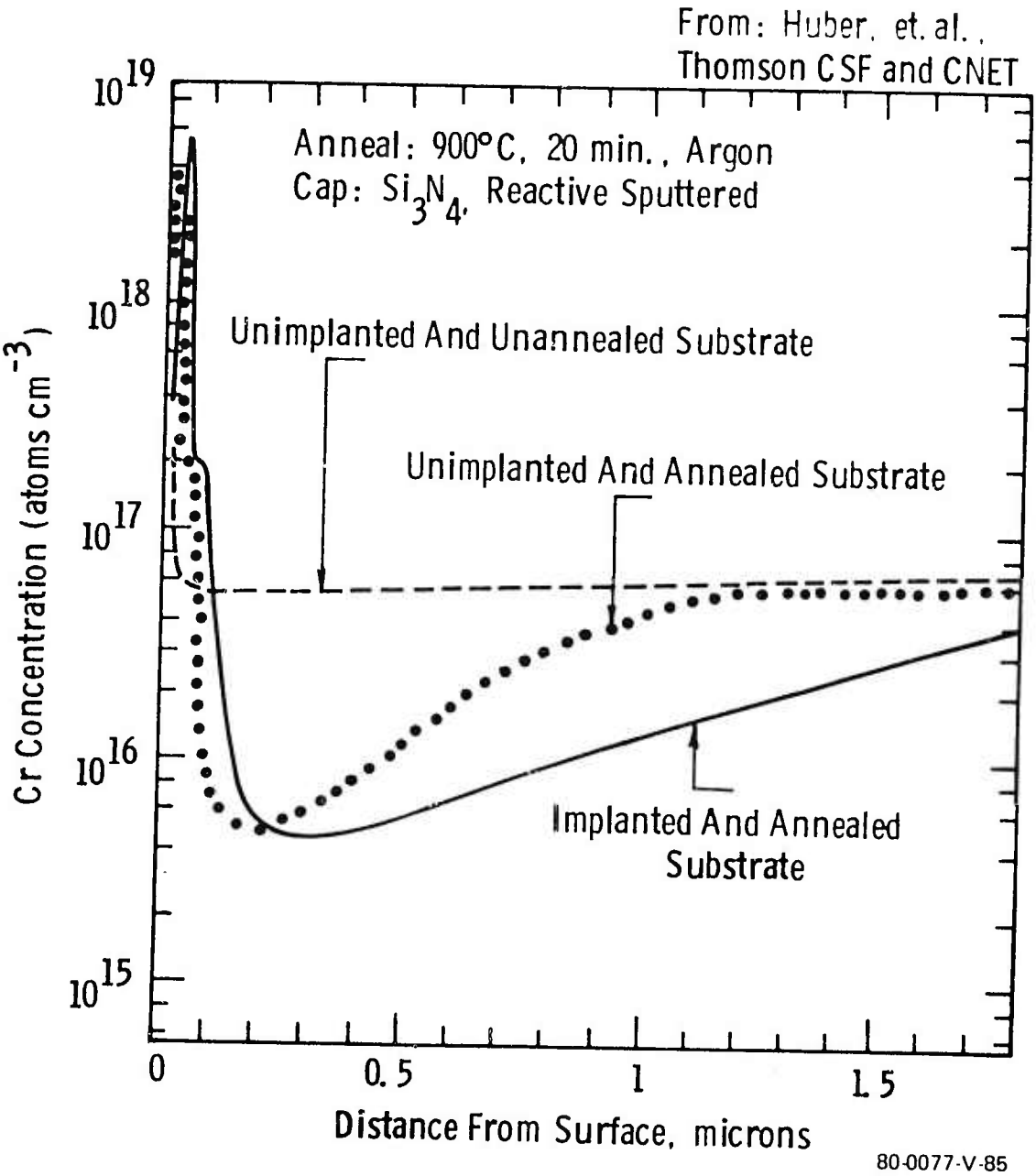

Figure B-7. Chrome Redistribution in Semi-Insulating GaAs After Ion Implantation Anneal

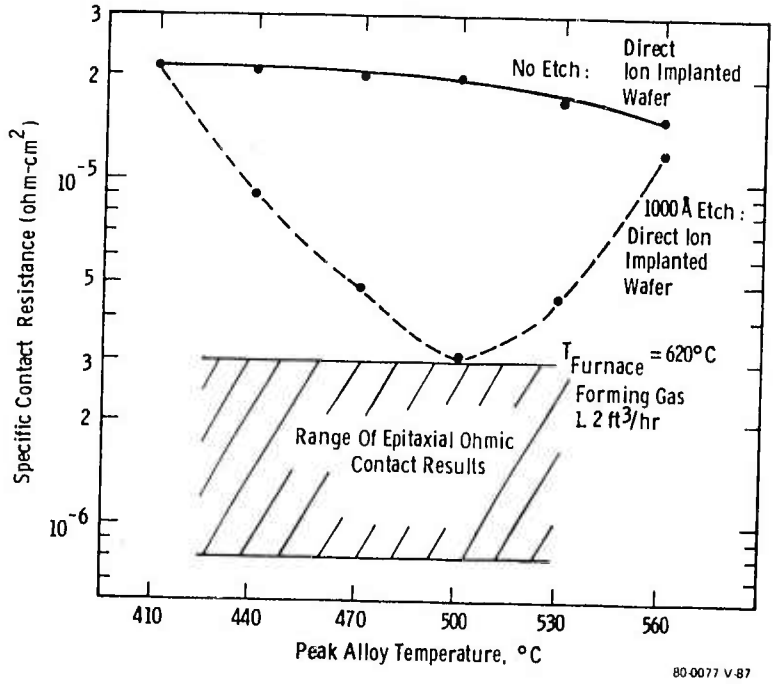

Figure B-8. AuGe/Ni/Pt Ohmic Contact Performance on Directed Ion Implanted and VPE GaAs Samples

be due to the ohmic-contact resistance for a FET with a 1.0-micron source-to-gate length. Because of improvements in our ohmic-contact technology, the contact resistance no longer represents the major contribution to the parasitic-source resistance.

However, these initial results on the AuGe/Ni/Au/TiW/Au system are not the final solution because of yield and fabrication problems. These problems revolve around the incompatibility of using sputtered TiW with a chlorobenzene-treated-photoresist rejection technique. Sputtered TiW bridges the photoresist and will not lift off without severe mechanical abrasion (swabbing) and intense ultrasonic treatments. These treatments cause many of the ohmic contacts to peel off resulting in an unacceptable loss in yield. The peeling problem can be overcome by the use of the dielectric-assisted lift off technique. With this technique, we obtained 95 percent yield across an entire wafer with $R_C = 1.3 \times 10^{-6}\ \Omega\text{-cm}^2$ at 470°C.

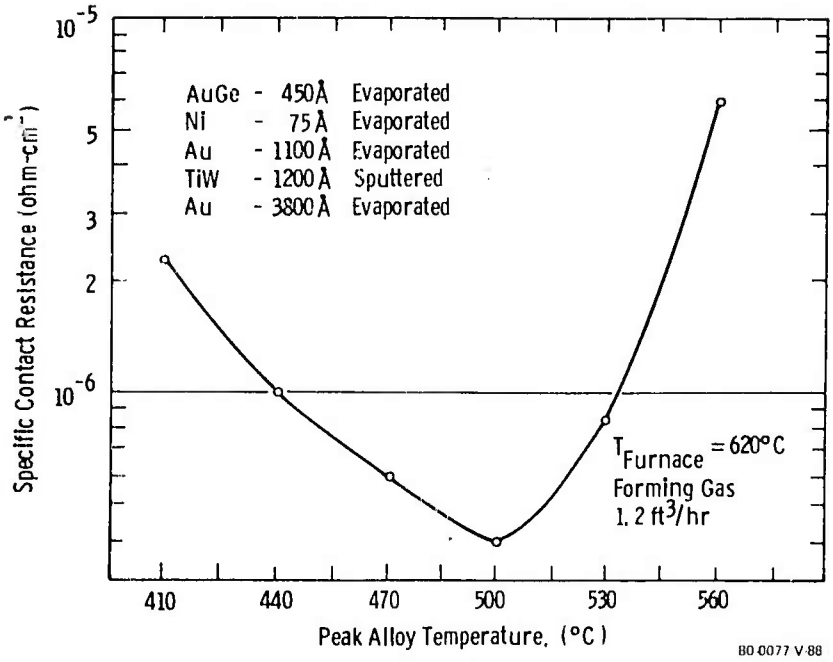

Figure B-9. Specific Contact Resistance of AuGe/Ni/Au/TiW/Au on Direct Implanted GaAs Substrates

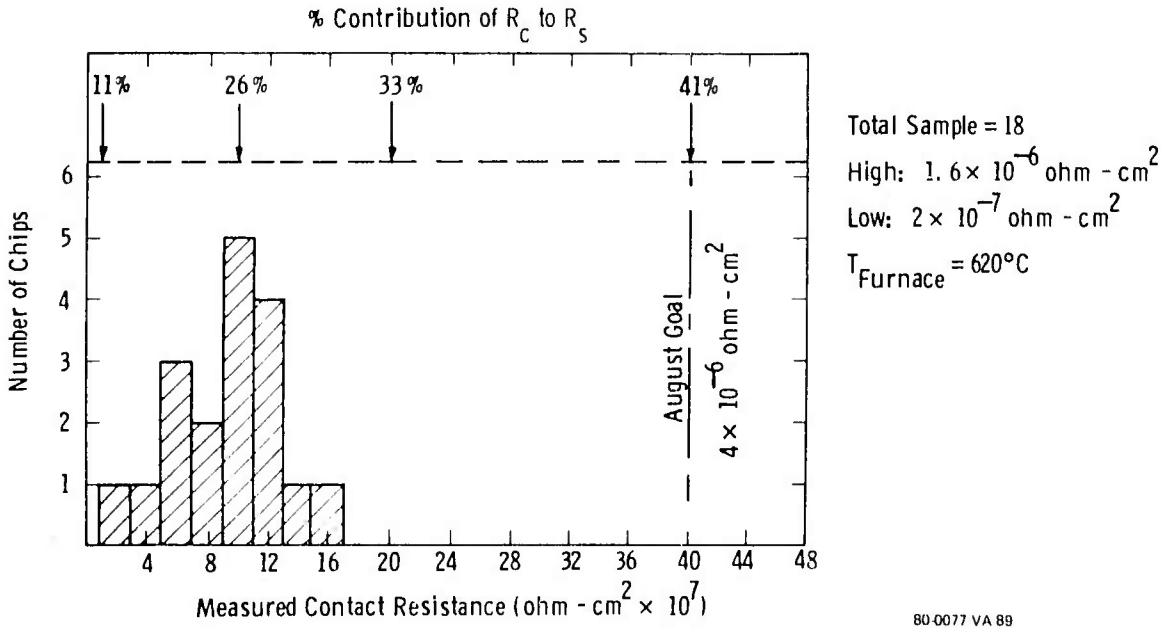

Figure B-10. Reproducibly Low Contact Resistance of AuGe/Ni/Au/TiW/Au Ohmics Alloyed at 470°C, 500°C, and 530°C

Unfortunately, dielectric assisted lift off is not compatible with the rest of our present monolithic-circuit fabrication process. It could be integrated into the current process, but with considerable difficulty. For the time being, we are continuing with the AuGe/Ni/Pt metallization.

APPENDIX C

CONTROLLED VAPOR-PHASE EPITAXY OF LARGE-AREA GALLIUM ARSENIDE

APPENDIX C

CONTROLLED VAPOR-PHASE EPITAXY OF LARGE-AREA GALLIUM ARSENIDE

C.1. INTRODUCTION

C.1.1 Background on Growth of GaAs for Microwave Devices

Effer[1] introduced the $Ga/AsCl_3H_2$ system for the growth of gallium arsenide in 1965. Using arsenic trichloride vapor in hydrogen over high-purity gallium metal 10^{15} cm^{-3}, n-type material was prepared on conducting and insulating gallium arsenide substrate wafers. Following the announcement of the Gunn effect, several electronics laboratories began to take a keen interest in gallium arsenide as a material for microwave devices. Wolfe, Foyt and Lindley[2] published their findings on an interface-dip problem and a successful C-V analysis method for impurity profiling, and Cairns and Fairman[3] announced the sharp dependence of impurity incorporation on arsenic trichloride mole fraction. Shaw[4] published findings concerning the deposition characteristics of the epitaxial gallium arsenide and their dependence on the arsenic-to-gallium ratio in the vapor phase, together with findings concerning the liquid gallium source mechanism that indicated an inherent instability in the growth process. Further detailed work on the mole fraction effect and thermodynamic analysis by Dilorenzo, et al.[5] produced 10^{13} cm^{-3} 200,000 mobility films at $77^{o}K$ and went a long way to explaining the impurity incorporation dependence on arsenic trichloride pressure. A method for controlled arsenic trichloride overpressure in the seed zone due to Nozakietal[6] and Cox et al.[7] suppressed the impurity concentration so as to produce insulating buffer layers of gallium arsenide which could be overdoped with sulfur or selenium to produce FET channels.

In a study of dopant injection techniques and incorporation mechanism, DiLorenzo and Luther[8] highlighted the problem with the $AsCl_3$-Ga process: an inadequate control of growth rate due to an

uncontrolled As/Ga ratio problem earlier described by Shaw. By the use of vapor-phase etching (Nozaki et al.) and heat-pipe furnaces (Hollan et al.)[9], many of the instability problems could be circumvented and successful use of this process has been obtained at many research laboratories. Nevertheless, the requirements of controlled epitaxy are very trying, especially for FET or mixer layers where submicron layer widths are required and the variation of the pinch-off voltage of the FET Schottky barrier depends on the square of the layer width. Not only is the control of epitaxy with area required to 100Å and 1×10^{16} cm^{-3} (in 4000Å and 1E17), but the deviation from run to run must also be within this tolerance. Doerbeck et al.[10] reported a method of correcting overlength/overdoped wafers using a self-limiting etch technique. In principle, a reverse-biased Schottky barrier was formed between the sample and an electrolyte. When the diode reached breakdown condition, current was drawn and anodization occurred. Of course, where the layer was so narrow that the depletion region extended into the substrate, no current flowed; hence, the self-limiting nature of the process. With repeated anodization and stripping, the whole wafer could be brought to the pinch-off condition. To date, this method suffers in that multilayered FET layers cannot be optimized, neither can device layers on conducting substrates. In addition, reported results apply only to small 10-cm^2 wafers. Clearly the inherent instability of a liquid-gallium source has been permitted to impinge on the control of epitaxy in the past. This source-saturation mechanism has contributed to poor control of: carrier concentration, thickness, surface morphology, compensation, and yield of wafers - all pertinent device manufacturing parameters. Since we are looking toward a process with sufficient control where subsequent layer optimization is not required after epitaxy, the recognized $Ga/AsCl_3/H_2$ reactor is inadequate.

The cheapest and most reliable method of achieving control of the As/Ga ratio is to use solid-source gallium arsenide with arsenic trichloride vapor in hydrogen. This technique has been

available since the early days of GaAs technology, Ewing and Greene[11] for example, but not used successfully for device layers because of impurity problems. However, solid-state reactors became more attractive with the availability of pure starting material (gallium and arsenic) and the work of Crossley et al.[12] on FET manufacture using this process.

C.1.2 The Current Westinghouse Thrust

Westinghouse vapor-phase epitaxy intends to supply device programs with a steady flow of the best available epitaxial GaAs wafers for research and development of new and improved microwave devices, in addition to the pilot production of material for state-of-the-art electronic devices for military systems. By the use of recently available pure raw materials, substantial scaling up of the process, and the use of automatic sequencers, we have successfully demonstrated a first-rate capability in GaAs epitaxial growth. Improvements in all aspects of layer characteristics have been achieved: improved channel Hall mobilities, reduced defect density, increased wafer area, improved wafer uniformity, sharper cut off into the buffer layer, higher-resistivity buffer layers, and additional multilayers for advanced FET design. These improvements in layer properties are in addition to system reproducibility and safety interlocks that arise as a result of automation.

The Westinghouse work begins with the synthesis of pure semi-insulating gallium arsenide monocrystals of great size. Three Kg crystals of 3-inch diameter on (100) axis have been prepared in silica and boron nitride crucibles using boric oxide encapsulant.[13] In general, the seed (higher purity) end of a crystal is reversed for use as solid source ingot. It is the transport of these crystals that gives the desired control of epitaxy over 3-inch diameter substrate wafers (45 cm^2 area).

C.2. $AsCl_3/H_2$ VAPOR PHASE EPITAXY REACTOR

C.2.1 Essential Features of Reactor Design (See figure C-1.)

(a) GaAs solid source

(b) Automatic sequencer

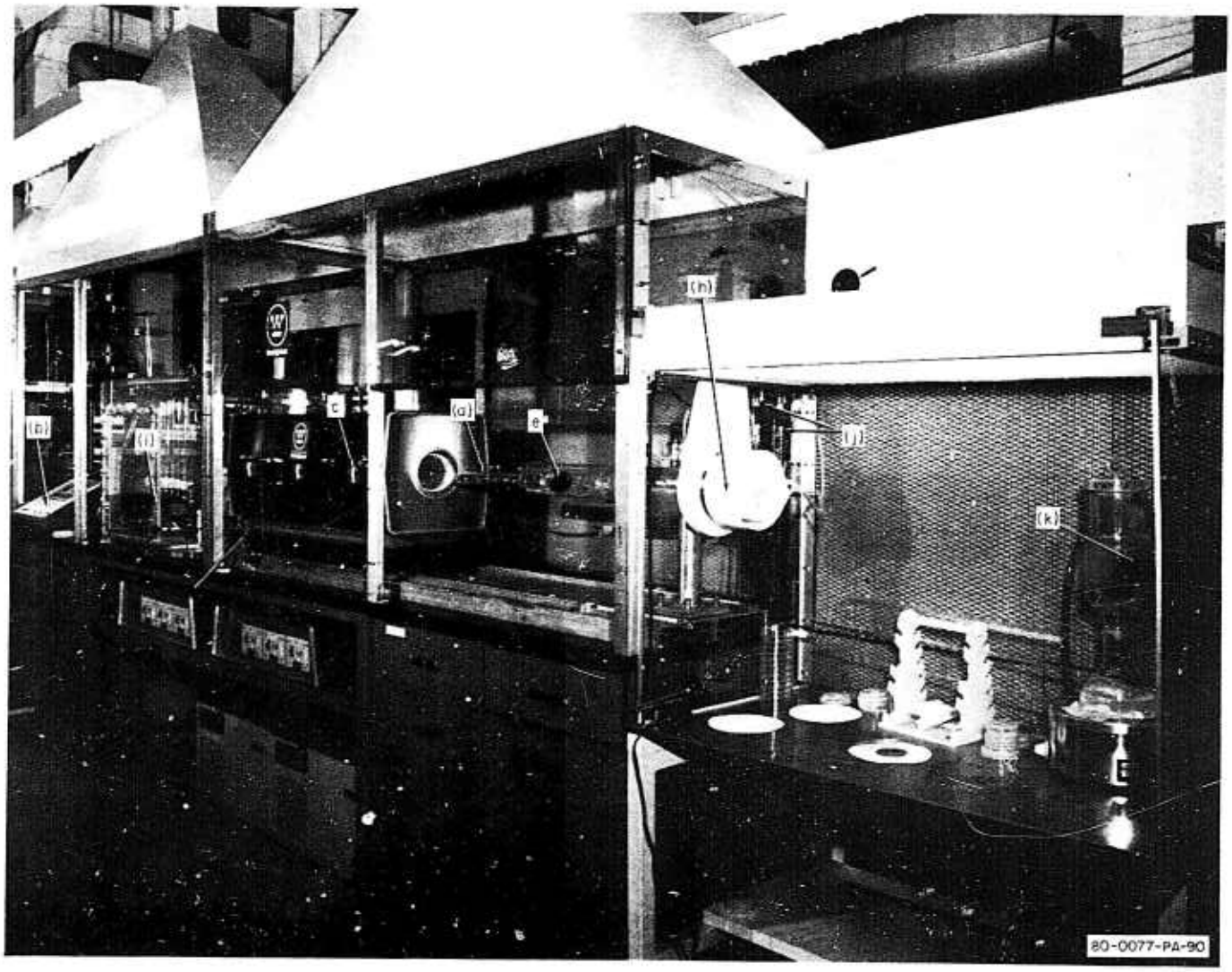

Figure C-1. Epitaxial Growth Equipment for the Deposition of 3-in. Diameter Epitaxial Gallium Arsenide Films

(c) Heat pipe furnace (roll-on type)

(d) Short response time flow lines

(e) 3-1/2-in. diameter reaction chamber

(f) Electronic injection valves

(g) Short response time reaction zone

(h) Exhaust traps to remove all by-products

(i) Mass flow controllers

(j) Safety interlocks

(k) Soxhlet wafer cleaners

At the outset, it was decided that one of the currently available electronic sequencers should provide for the running of the reactor performing all functions, including hydrogen flush, nitrogen flush, furnace on, furnace off, seed etching (two levels), layer growth, sulfur doping (four levels), silicon doping (four levels), chromium doping, oxygen doping, and several safety interlocks and defeat mechanisms. It was envisaged that the operator should only need to clean and load/unload wafers and initiate a program. Figure C-2 shows the sequence and flow diagram. The sequence could hold ~ 80 steps in its memory operating on 18 channels. Since the average growth program consists of ten steps, eight layer types can be stored in the sequencer memory. Subtle changes in program for optimization can be performed before use or even during the program. The use of an electronic 'brain' for the reactor means improved safety, improved yield, and improved reproducibility.

The furnace was of the roll-on type, having six temperature-controlled zones for predictable oven-profile control. The source zone contained a sodium heat pipe and could be observed through a gold-coated mirror in the blind end of the furnace. The assembly was electrically driven onto the reaction chamber in 4 sec and would heat source and seed to 800 and 750°C in ~ 2 min.

The bore of the furnace was two inches in the source zone (inside the heat pipe) and six inches in the seed zone in order to accommodate the complex reaction tube design and the large-substrate dimensions (see figure C-1). The gas-flow circuits consist of five essential regions (see figure C-2).

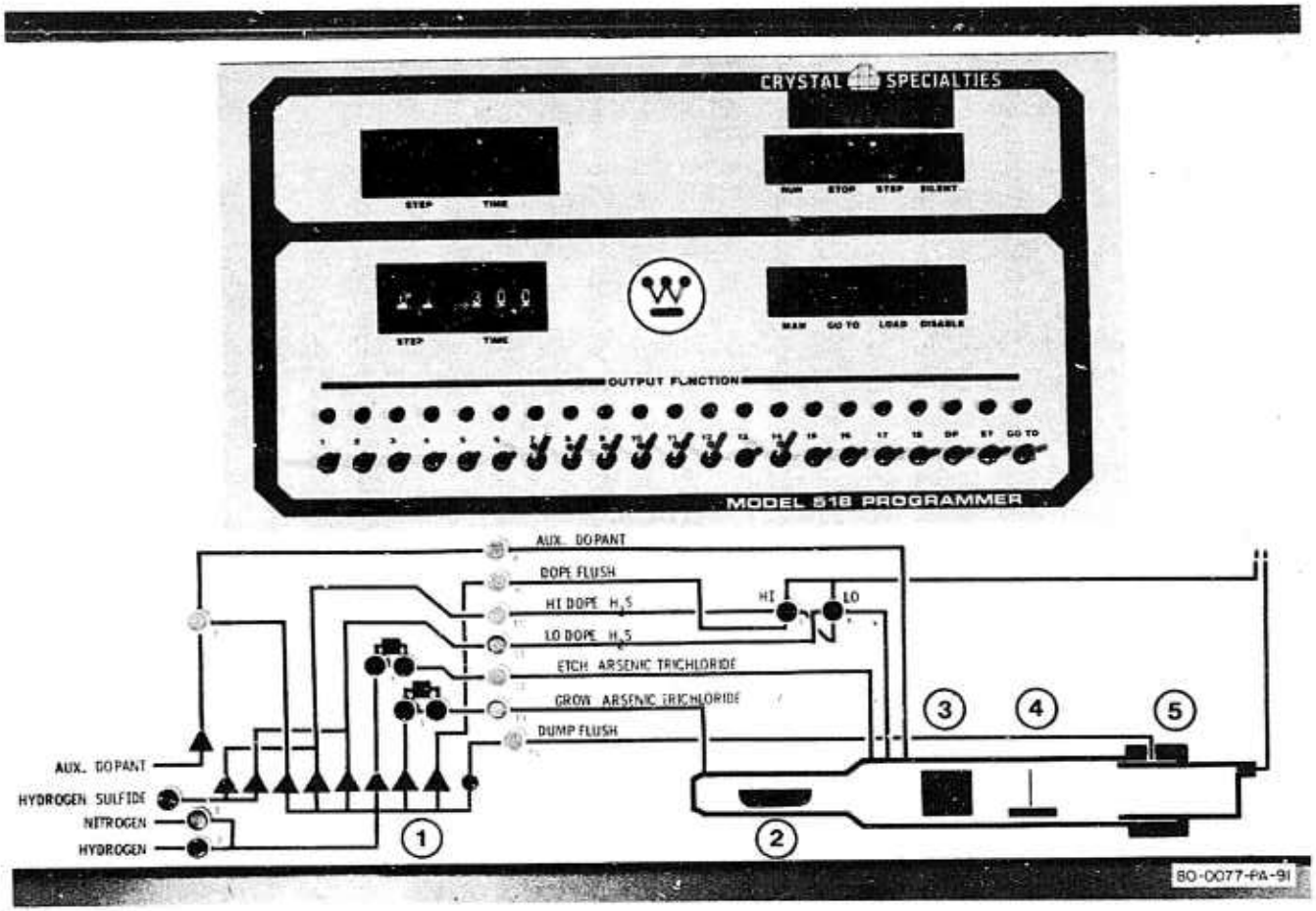

Figure C-2. (Upper) Automatic Sequencer that Controls Epitaxial Deposition
(Lower) Flow Diagram of the Epitaxy Machine

a. Gas Control Circuits. Manually-set mass-flow controllers (⊕) govern the rate of flow of the indicated gases in the direction set by the electronically operated flow valves (0). For instance; the grow circuit flows with hydrogen or nitrogen, as set by the input valves and at a rate set by the mass-flow controller, either directly into the reactor or through the $AsCl_3$ chamber, and hence into the reactor, entering the reaction tube downstream of the source material. This information is programmed into the sequencer. The temperature bath surrounding the $AsCl_3$ chambers was set at $24^{o}C$ giving a mole fraction variation of 1 through 10×10^{-3} at $2 - 25 \times 10^{-5}$ mole/min, depending on the flow settings selected by the programmer. The etch line has the same characteristics except it enters the reactor between the source and seed regions.

The dopant gases flow through mass-flow controllers to the dopant injection valves. The control of interface shapes during epitaxy is affected by the proximity and design of the electronic injection valve, the swept volume between injector and seed, and the reactor sweep time. The program selects one of four levels of dopant for the desired impurity for one particular step.

b. Source Zone. The source zone contains the raw material for growth, solid lumps of gallium arsenide for this work. However, by the inclusion of a heat-pipe and a transparent view-port, provision for liquid gallium, source work is made. A baffle consisting of a tight-fitting evacuated silica envelope separates the 2-in. diameter source zone from the 3-1/2-in. diameter seed zone.

c. Injection Zone. The injection zone is a narrow region between the source baffle and the seed baffle that allows the reactant vapors from the source to be modified by injected material; $AsCl_3$ for etching or buffer growth, hydrogen sulfide or silane at varying concentrations for multilayer growth, and oxygen or chromium-doped vapors for buffer layer improvement. It is the sequencing of these vapors by the program that determines the ultimate wafer properties.

d. Seed Zone. The seed zone is separated from the injection zone by a tight-fitting evacuated baffle. This reduces reactor-sweep time and enhances wafer uniformity. The wafers (up to 3-in. diameter) are mounted facing the gas stream adjacent to the baffle with a further baffle downstream.

e. Exhaust Zone. This zone is most important if only because all wafers for processing in the reactor must pass through it. By virtue of an interlocking tube arrangement and a reverse-flow mechanism, the deposition on the reaction chamber is prevented and all byproductes are removed at the end of each growth sequence before unloading the wafers. This eliminates downtime for reactor cleaning and assists in providing reproducible epitaxial wafer characteristics. Over 100 layers have been grown without reactor dismantling.

C.3 RESULTS

Large-area (45 cm^2) wafers of semi-insulating and conducting wafers have had epitaxial layers deposited on them in this growth system. After growth, the surface morphology is excellent; apart from the characteristic edge facet, the surfaces are as good, if not better than, the underlying substrate.

C.3.1 Layer Types

Layers for mixer diodes are 0.8-μm thick 1.1×10^{17}-cm^{-3} deposited on a conducting substrate. n^+ buffer layers were interposed between the substrate and active layer to provide a controlled electrical interface away from the metallurgical junction. This device requires a 10^{18}-cm^{-3} layer ~ 0.5 μm followed by a 1.0×10^{17} -cm^{-3} layer. The interface between the buffer layer occurs within 500Å. Figure C-3 shows the narrow range of carrier-concentration uniformity over the 10-cm^2 slice and also depicts the interface properties of a thin layer. Nondestructive carrier profiling was performed on the epitaxial wafers by using two closely spaced mercury contacts[14] with a coaxial mercury vacuum probe[15] and a Miller profiler.[16] The two Schottky-barrier approaches require no ohmic contact and the coaxial probe minimizes series resistance-a problem with FET-channel profiling.[17] The outer coaxial contact

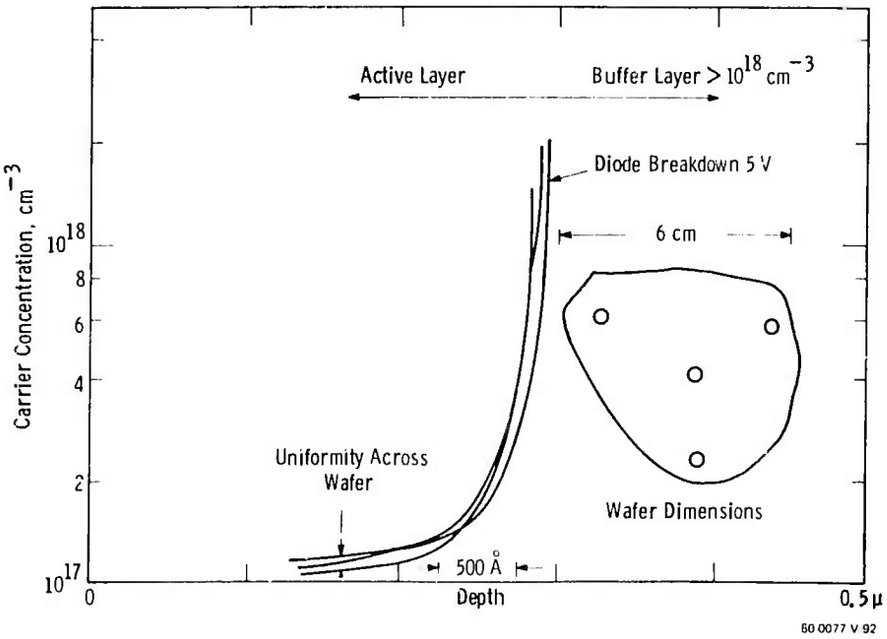

Figure C-3. Carrier Concentration Depth Profiles for Mixer Diode Construction

was much larger in area than the central test diode and contributed little error to the measurement. By the use of monitor-insulating wafers, the active-layer mobility was estimated at 4900-5000 cm^2/volt sec. The wafers were prepared using a program involving high arsenic trichloride mole fraction and sequential sulfur injection. Ten consecutive (~ 20 cm^2, each) wafers were within the 10 percent tolerance indicated above.

C.3.2 Planar FET Layers

Using undoped GaAs source material or Cr-doped source material together with high arsenic trichloride pressure (10^{-2} atm), it is possible to grow semi-insulating buffer layers. Sulfur-doped channels on the surface were prepared by hydrogen sulfide injection. The critical properties of this device include high low-field mobility in the channel, accurate prediction of channel-carrier concentration, uniformity of channel properties with area, sharp-channel knee dropping into buffer layer, and large-area wafers with flat topography for device fabrication. Figures C-4 and C-5 give an idea of the high yield of usable material from

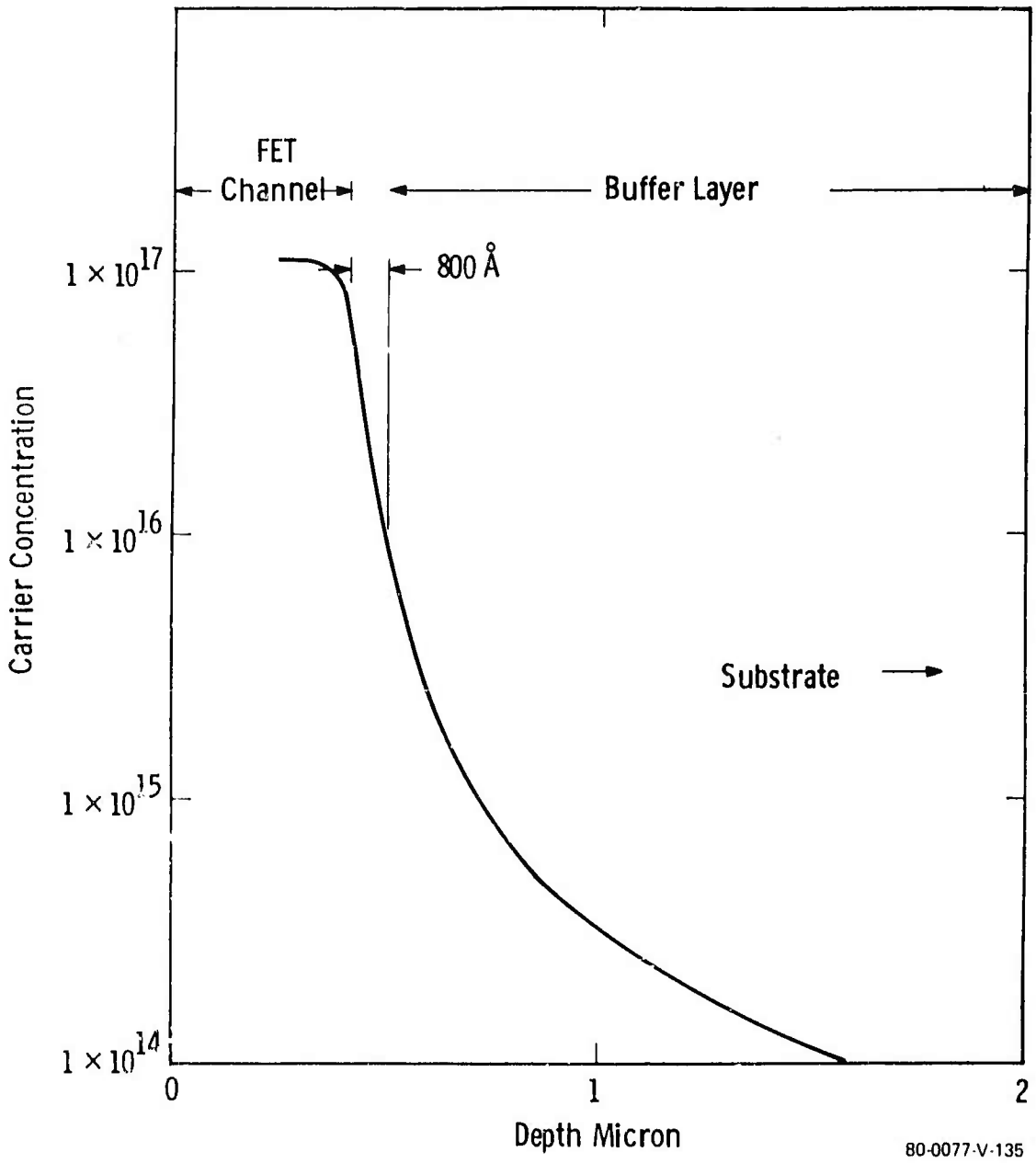

Figure C-4. Carrier Concentration Depth Profile for a Conventional Transverse FET

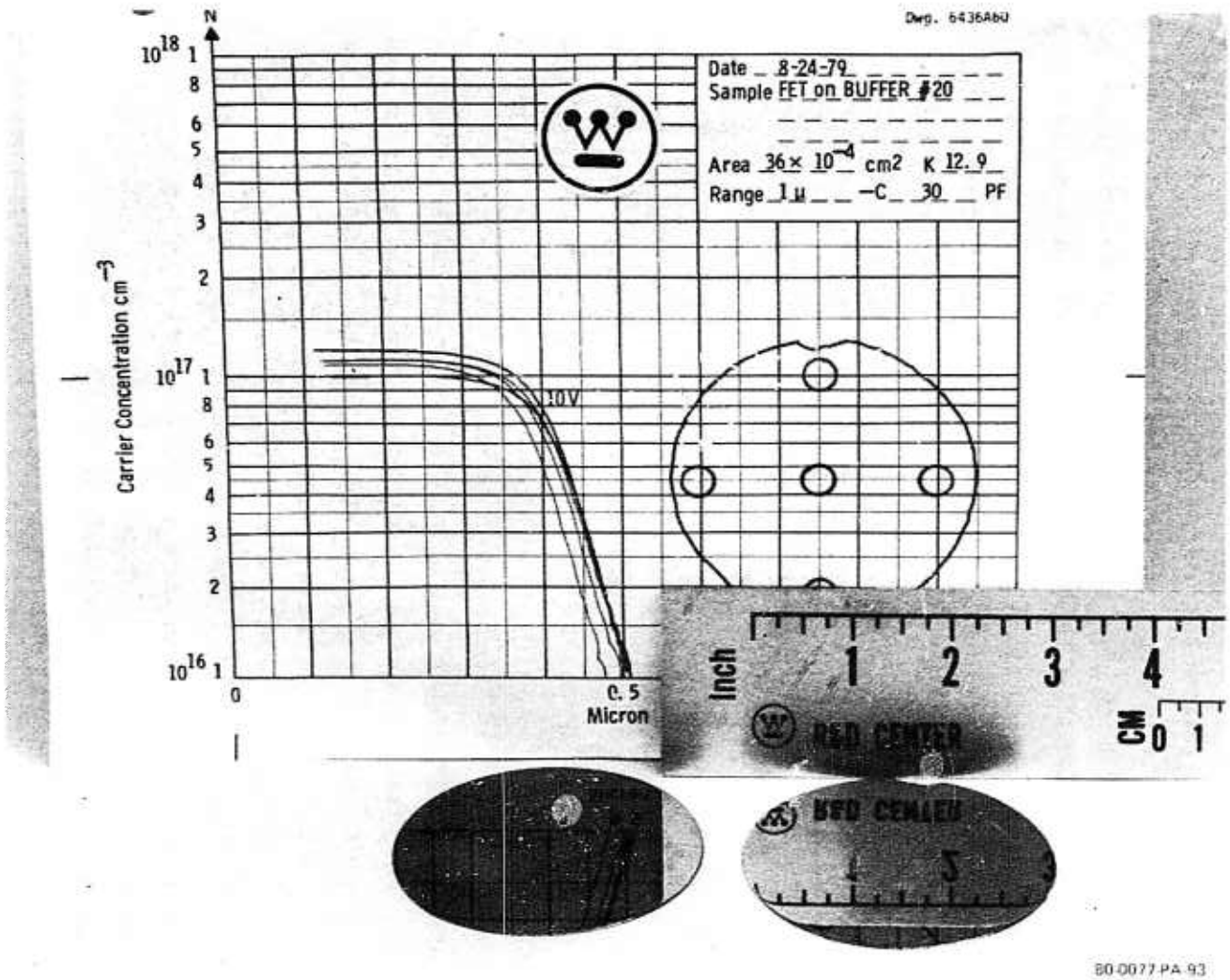

Figure C-5. Uniformity and Surface Morphology of 3-in. Diameter Epitaxial FET Films

this process. Doerbeck[10] reported, after anodization, changes in ungated FET current of 15 percent over a 16 cm^2 wafer. However, channel current varies directly with channel depth, whereas pinch-off voltage varies with the square of the channel depth. This variation in channel current constitutes a change in pinch-off voltage of ~5V on a 10-V diode over 16 cm^2; whereas our automated growth method offers a change in pinch off of 1V in 10V over 45 cm^2 of epitaxial wafer, as shown in figures C-5. A reproducible 5300-cm^2/Volt sec channel mobility has been observed in the Hall measurements on 1×10^{17}-cm^{-3} FET layers. These results, taken with others from the literature, indicate that Westinghouse material compares very favorably with state-of-the-art materials growth for FET production (figure C-6). As the epitaxial multi-layered structures become more ambitious, problems with characterization using the conventional metallized-Schottky diode are experienced. With any highly-doped structure where the breakdown voltage is only a few volts, the diodes usually break down before sufficient depletion data has been obtained. Manual etching and measurements have been used in the past for layer analysis. An automated method of achieving the same result is the Polaron[18] post office plotter.[19] This uses an electrolytic Schottky barrier and etching technique which sequentially removes material and then records the zero-bias capacitance measurements from which N_d vs depth data are calculated. Figure C-7 gives some examples of this method of evaluation of epitaxial multilayers.

a. HIFET. The High-Doped contact field effect transistor (HIFET) is a 3000Å 1×10^{17}-cm^{-3} channel on an insulating buffer ~2μ; a conventional FET, except for the addition of an n^+ surface layer to enchance the ohmic contact and reduce the noise figure in the final devices.

b. VFET. The epitaxial Vertical Field Effect Transistor (VFET) is a Westinghouse proprietary design for a high-power device that does not require an insulating subtract. While the conventional FET is a transverse device, the VFET is vertically inclined with source and drain at the substrate and surface of the epitaxial

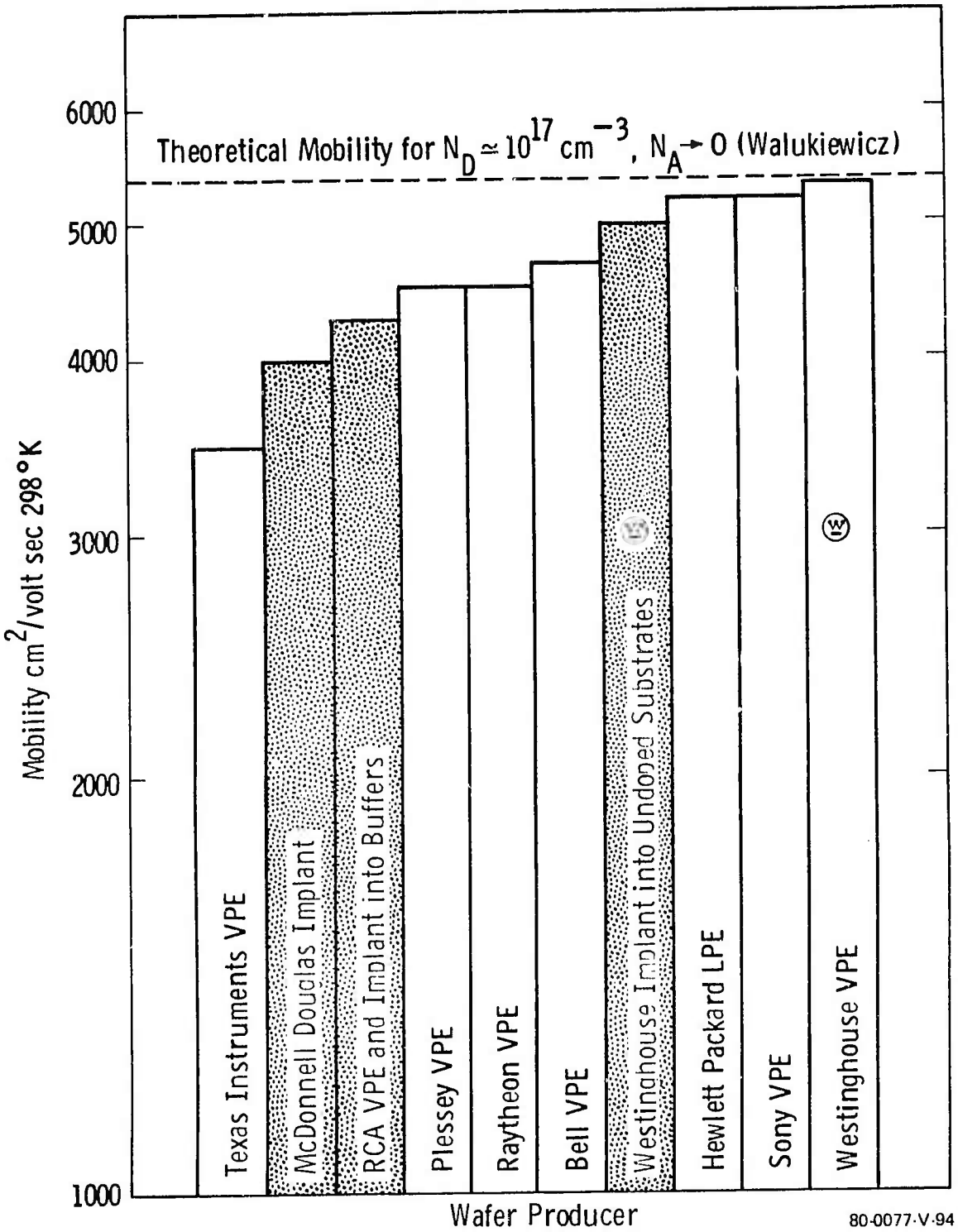

Figure C-6. Comparison of Published Room Temperature Electron Mobility Values for FET Films with Theory

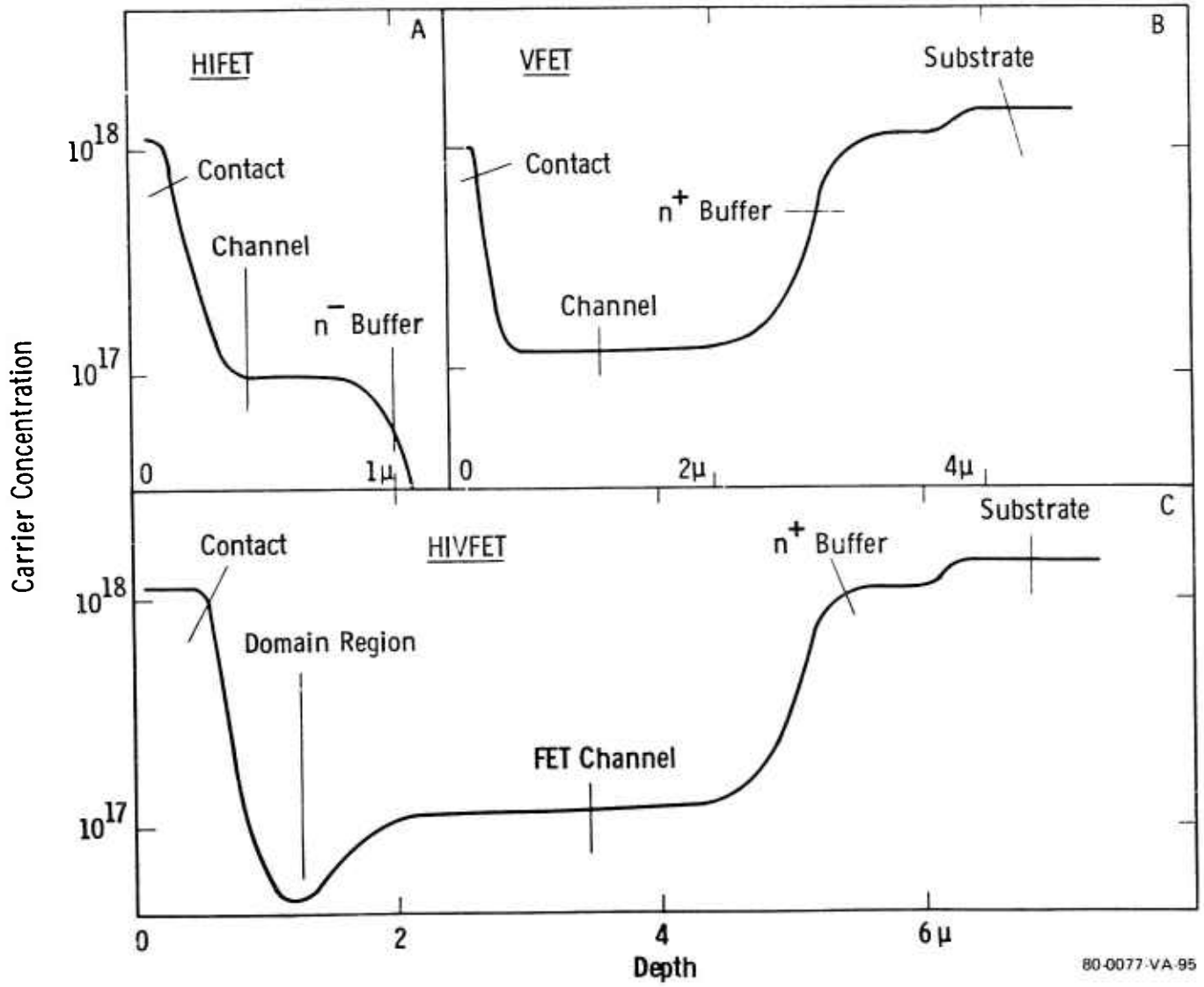

Figure C-7. Various Carrier Concentration Depth Profiles Held in the Memory of the Automatic Growth System

region. Pinch off occurs between two opposed gates judiciously placed between the ohmic contacts after the channels have been etched out. The substrate is n^{++} and first an n^{++} epitaxial region is grown to displace the electrical interface from the metallurgical junction. The channel is 1.2×10^{17} cm^{-3}. Sulfur-doped gallium arsenide 3μ thick is then deposited, followed by a surface-contact layer to reduce ohmic-contact resistance.

c. HIVFET. High-doped contact vertical field-effect transistor (HIVFET). With a vertical construction, it is possible to grade the properties of the channel between the source and drain. In this case, we have reduced the carrier concentration by placing a notch in the profile. The notch is expected to form a domain in the operating device and thereby increase the breakdown voltage and hence the power available. Figure C-8 shows a cleaved and stained cross-sectional micrograph of the multilayered HIVFET.

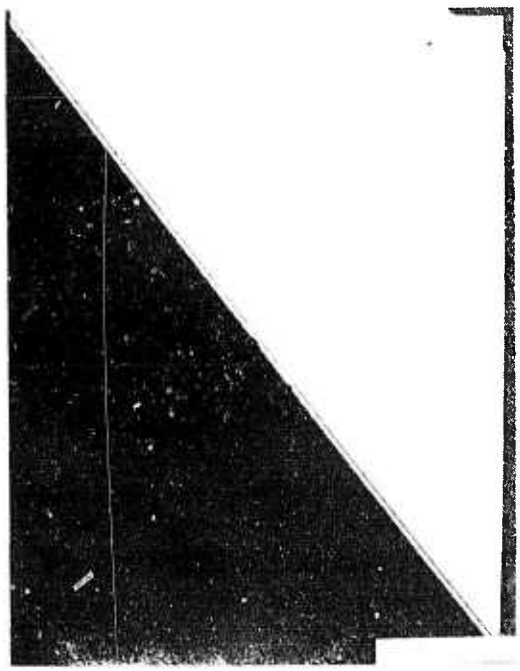

Figure E-8. Cleaved and Stained Cross Section of HIVFET Structure

C.4 SUMMARY

The Westinghouse gallium arsenide vapor-phase arsenic trichloride process is now capable of large-area, uniform growths with tightly controlled but widely variable properties. Using recently available in-house high-purity gallium arsenide ingots (synthesized and pulled in the Melbourne Czochralski growth system) as source material, we have been able to achieve reproducible 10^{13}-cm^{-3} buffer layers for isolation of FET channels with excellent surface morphology. Sequentially grown 0.3 - 0.5 μsulfur-doped FET channels have demonstrated a near-theoretical Hall mobility of 5300 cm^2/volt sec at $1.3 \times 10^{17} cm^{-3}$ and $298^{\circ}K$. Using substantial automation, the horizontal epitaxial-growth unit is capable of 15 percent variation in pinch-off voltage across a 3-inch diameter (100) substrate wafer. This represents control of thickness to 500Å and control of carrier concentration to 1×10^{16} cm^{-3} over 45 cm^2 of gallium arsenide. The memory in the automatic sequencer can hold up to ten programs for differing device requirements. Thus far, we have supplied buffer layers, FET layers, and mixer layers with a number of internal variants. Fully characterized with Hall measurements and mobility and carrier concentration profiles, these layers represent the promise of manufacturing control of gallium arsenide epitaxy for commercial enterprise.

C.5 FUTURE WORK

Problems of instability of the arsenic-to-gallium ratio over the growing wafers do not arise with solid-source work. The arsenic-to-gallium ratio is fixed at 4/1. This provides for a very reproducible process, but it is by no means clear that a ratio of 4/1 is optimum.

Different arsenic-to-gallium ratios could produce desirable properties in particular, epitaxial multilayers. Wood[20] has observed large changes in the electrical properties of germanium-doped GaAs with arsenic-to-gallium ratio where the gp IV atom behaves amphoretically. Thompson[21] has also shown degenerate 10^{19} cm^{-3} Si-doping in vapor phase epitaxy (VPE) layers by

adjusting the arsenic-to-gallium ratios; systems that can utilize the arsenic-to-gallium ratio to assist in profile control have an advantage. The Arsine 410A crystal-specialties reactor with suitable in-house modification will enable the investigation and utilization of these stoichiometric effects. Delivery of this machine is expected in February 1980 (figure C-9).

Concurrently, work on oxygen-doped and chromium-doped buffer layers will be pursued with the horizontal process. We also intend to investigate silicon doping of FET channels.

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Figure C-9. A10 Arsine Growth Reactor

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APPENDIX D

DIRECTLY IMPLANTED GaAs MONOLITHIC X-BAND RF AMPLIFIER UTILIZING LUMPED ELEMENT TECHNOLOGY*

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APPENDIX D

DIRECTLY IMPLANTED GaAs MONOLITHIC X-BAND RF AMPLIFIER UTILIZING LUMPED ELEMENT TECHNOLOGY*

A monolithic GaAs amplifier containing four lumped inductors and two interdigital capacitors has been fabricated with over 20-percent yield on a 1.25 x 2.5-mm chip using direct-ion implantation. The overall amplifier exhibits a one-stage gain of 6 dB centered at 7.1 GHz with a 10-percent bandwidth. No post-fabrication adjustment on any tuning element was required to achieve design goals. One key to the potential of this largechip "monolithic" technolgy is the fact that the per-area yield of the passive circuitry (L's, C's) is generally 50 to 100 times as great as the yield-limiting mechanisms in the active channel of the power FET's. As a result, adding passive circuitry to the FET chain in a controlled lithographically-defined manner only decreases the number of chips per wafer, rather than geometrically reducing the chip yield.

In order to establish a GaAs integrated-circuit technology to eventually reduce the cost of multistage X-band power amplifiers below $100/amplifier, we have been studying the uniformity and reproducibility of direct-ion implantation utilizing a 400-kV Varian Extrion Ion implanter, Model 400-10. We are presently utilizing 6-to 18-cm^2 GaAs substrates which are implanted at 400 keV with 3-5x10^{12} cm^{-2} dose utilizing Si^+ as a dopant. Post-implantation capping is carried out in a modified LFE plasma nitride despoition system at 341°C and the wafer annealed for 15 min at 860°C in forming gas.

In the device process, a 900-μm gate FET having a 1-micron gate and a 6-micron S-D spacing is fabricated utilizing AuGe/Pd/Au ohmic contacts. The input and output matching circuits contain four lumped inductors ranging from 0.15 nH to 1.25 nH plus two 1 pF interdigital capacitors. The circuit metals are over 1 micron

thick to minimize circuit losses. As can be seen in the photograph, figure D-1, the overall size of the one-stage amplifier is only about 3 mm^2, leading us to believe that lumped, high-Q X-band circuit elements can offer substantial size-reduction potential over distributed circuits of the same bandwidth.

The lumped-element circuit design for this amplifier was performed at the Westinghouse Advanced Technology Labs in Baltimore by Mr. D. Maki.

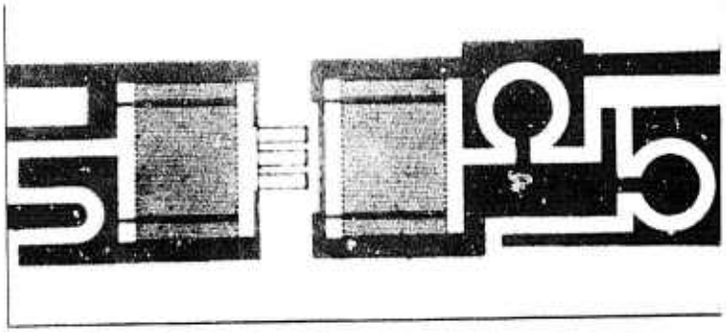

Figure D-1. Ten Percent Bandwidth Monolithic Amplifer

*This work was supported in part by the Defense Advanced Research Projects Agency, through the Office of Naval Research under Contract N00014-78-C-0268.

APPENDIX E
ION IMPLANTATION

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ION IMPLANTATION

E.1 INTRODUCTION

The thrust of the ion-implantation effort under this program is to develop a technology to selectively implant X-band power FET structures directly into 3-in. diameter semi-insulating GaAs substrates. A number of steps toward those goals have been achieved during this reporting period. Implantation facilities have been upgraded from 1-in. to 3-in. wafer diameter. $^{29}Si^+$ channel implants and either $^{28}Si^+$ or $^{29}Si^+$ + $^{34}S^+$ n^+ implants have been demonstrated to yield excellent reproducibility and electrical characteristics. Encapsulation facilities have been scaled up from 1-in. diameter to 2-in. diameter and the 3-in. objective appears to be feasible. Moreover, qualification procedures have been improved to permit implantation to prespecified concentration and depth into semi-insulating substrates. (All work on buffer layer implants has been terminated). Westinghouse has developed its own internal source of undoped and Cr-doped semi-insulating wafers. These wafers are grown, cut, and polished on site; they are always available on short notice in both 2-in. and 3-in. diameters, and they pass the ion-implantation qualification tests. As a result of these improved substrates and improved encapsulation procedures, low-field mobility values have risen from 3700 cm^2/Volt-sec at 0.8 - 1.0 x 10^{17} cm^3 to ~4750 cm^2 Volt-sec and 5500 cm^2/volt-sec at 1.2 x 10^{17} cm^3 and 0.6 x 10^{17} cm^2/Volt-sec, respectively. Extensive Hall-effect studies have provided valuable insights on the effect of deep traps on mobility and the threshold dose for n-implant activation. Extensive profiling studies have identified a tradeoff in channel mobility and profile abruptness associated with Cr doping. A selective channel-implant technology through nitride has been

developed. In conjunction with the above, optimum n^+-implant parameters have been established. The peak electron concentration is limited to approximately 1.5×10^{18} cm^3 as a result of the self-imposed constraint of all ambient-temperature implant technology, but 40-Ω/□ n^+ pads can still be achieved.

Section E.2 discusses new equipment that has been added to the implantation facility and the technology developed for its utilization. Section E.6 discusses qualification and uses this as a vehicle to describe activation and mobility obtained in Westinghouse and vendor supplied semi-insulating GaAs. Section E.7 is used to demonstrate concentration and profile reproducibility. Section E.8 discusses ambient temperature Si^+ and $Si^+ + S^+$ n^+ implants.

E.2 EQUIPMENT

E.2.1 Varian/Extrion 400-10 Ion Implanter

A new 400-kV Varian/Extrion ion implanter became operational at the Westinghouse Research and Development Center in mid-January 1979. This production machine, shown in figure E-1, is devoted almost exclusively to implantation of III-V semiconductors and replaces a 200-kV research machine used previously. The current machine features preacceleration mass separation; two-axis electrostatic scanning; and a 25-wafer, cassette-loading, ambient-temperature end station for batch processing. This end station permits use of 3-in. diameter LEC wafers as well as smaller pieces or irregular wafers from boat-grown ingots. Choice of this end station was based on consideration of the irregularity of available wafers, unavailability of a heated commercial end station with sufficient throughput, and the advantage of ambient-temperature implantation in allowing photoresist masking for selective implants. The machine was ordered with a tandem research chamber in front of the production chamber in the event that hot implants became necessary, and a design for heating in the production chamber was formulated for the same purpose. State-of-the-art n-channel mobility, profile integrity, and reproducibility has been achieved, however, by using ambient temperature $^{29}Si^+$ implants so that neither of these options have been implemented.

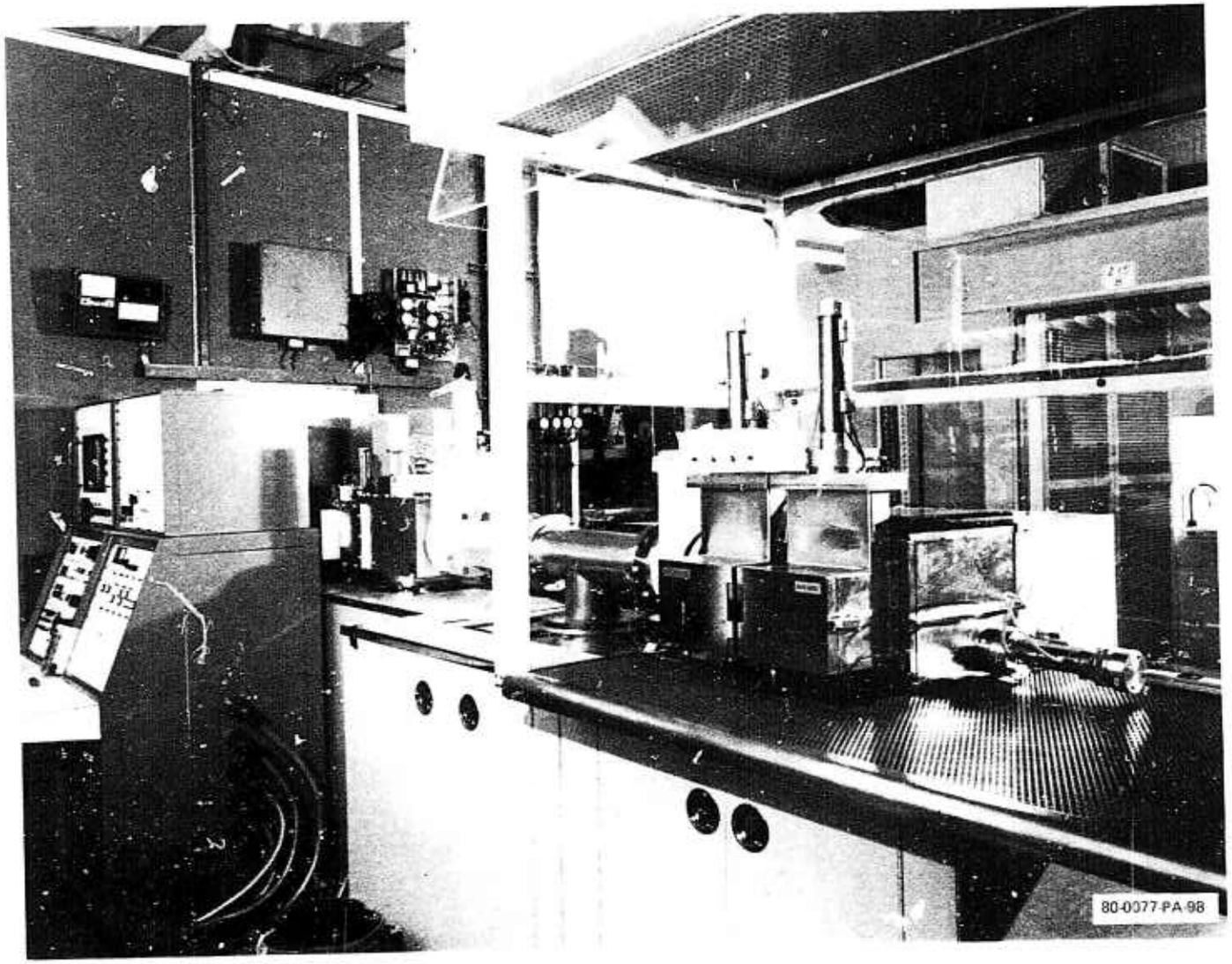


Figure E-1. Varian/Extrion Ion Implanter

The 400-kV implanter can be operated readily at voltages between 40 and 400 kV. These voltages imply limits on the projected range of maximum concentration (R_M) of approximately 400Å and 4400Å, respectively, for $^{29}Si^+$ in GaAs. The upper voltage limit leads to a channel depth too great to optimize power/unit periphery even when the implant is performed through a 1000-Å thick Si_3N_4 capping layer. Best results achieved to date have been obtained using 300-kV to 350-kV channel implants to yield an effective channel depth of approximately 3300A and a surface fill implant at 100-125 kV to place a concentration peak at the Si_3N_4/GaAs interface to facilitate subsequent ohmic contact formation. Both implants fall well wihtin the limits of the implanter and avoid the problems of doubly-charged or molecular implants.

As delivered, this machine is supplied with a tray of gas sources to provide B, P, and As beams for implantation of silicon. A duplicate tray containing SiF_4, SF_4, O_2 and A has been substituted. SiF_4 is employed to generate the $^{29}Si^+$ beam used for FET-channel implants; a typical mass spectrum is shown in figure E-2. The use of a $^{29}Si^+$ beam instead of $^{28}Si^+$ avoids possible

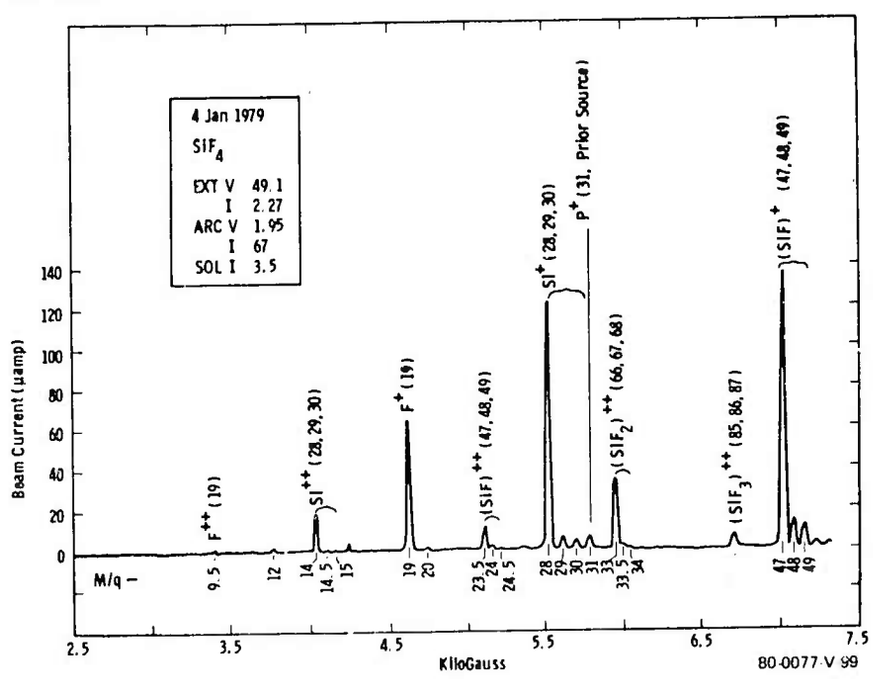


Figure E-2. Mass Spectrum of Silicon Source ($Si4_4$) in 400-kV Implanter

contamination by N_2^+ or CO^+ radicals and yields a stable low current suitable for channel implants. $^{28}Si^+$ is sometimes used for high-dose implants of n^+ source-and-drain implants. Careful measurement of the silicon-isotope currents demonstrates that beam contamination by N_2, CO, or hydride formation is negligible. SF_4 was chosen as a result of similar consideration to yield a pure $^{34}S^+$ beam. $^{34}S^+$ beams are employed for coimplantation with $^{29}Si^+$ of n^+ source-and-drain pads. $^{16}O^+$ beams have been employed for isolation implants and studies of deep levels on mobility and device performance. Argon was included for use in an early qualification scheme.

E.3 LFE PND-301-MQ6 PLASMA-ENHANCED DEPOSTION OF Si_3N_4 ENCAPSULANTS

Initial GaAs encapsulation work at Westinghouse focused on Si_3N_4 deposited using the pyroltic technique described by J.P. Donnelly of Lincoln Laboratories. This technique employs reaction of SiH_4 and NH_3 to form a Si_3N_4 layer on 680°C GaAs at a rate of 200Å to 300Å/minute. Rapid heating to the growth temperature and rapid growth is required to minimize GaAs decomposition. The requirement for rapid heating demands low thermal mass and exotic design to achieve fast, uniform response over even a small area. Samples sizes of 1-1/8 in and 5/8 in. were achieved; this size is barely acceptable for precision photolithography. Operation of the pyrolytic equipment requires a high degree of art to achieve proper timing and reactant mixing. Good profile integrity and Hall mobilities of 3700 cm^2/Volt-sec at peak concentrations of 1×10^{17} cm^3 were achieved for optimized pyrolytic Si_3N_4 encapsulation. These films contained an uncontrolled oxygen concentration of 5 to 15 percent as a result of leaks, residual oxygen, and degassing of the chamber walls. Modifications to minimize oxygen content resulted in Si_3N_4 layers that cracked or extruded GaAs during the 860°C postimplant anneal.

Plasma enhanced deposition of Si_3N_4 was determined to be the encapsulation technique of choice. A cross-sectional view of the LFE experimental reactor is shown in figure E-3. An inductive RF coil couples the bulk of the 13.56-MHz RF energy into ionizing and

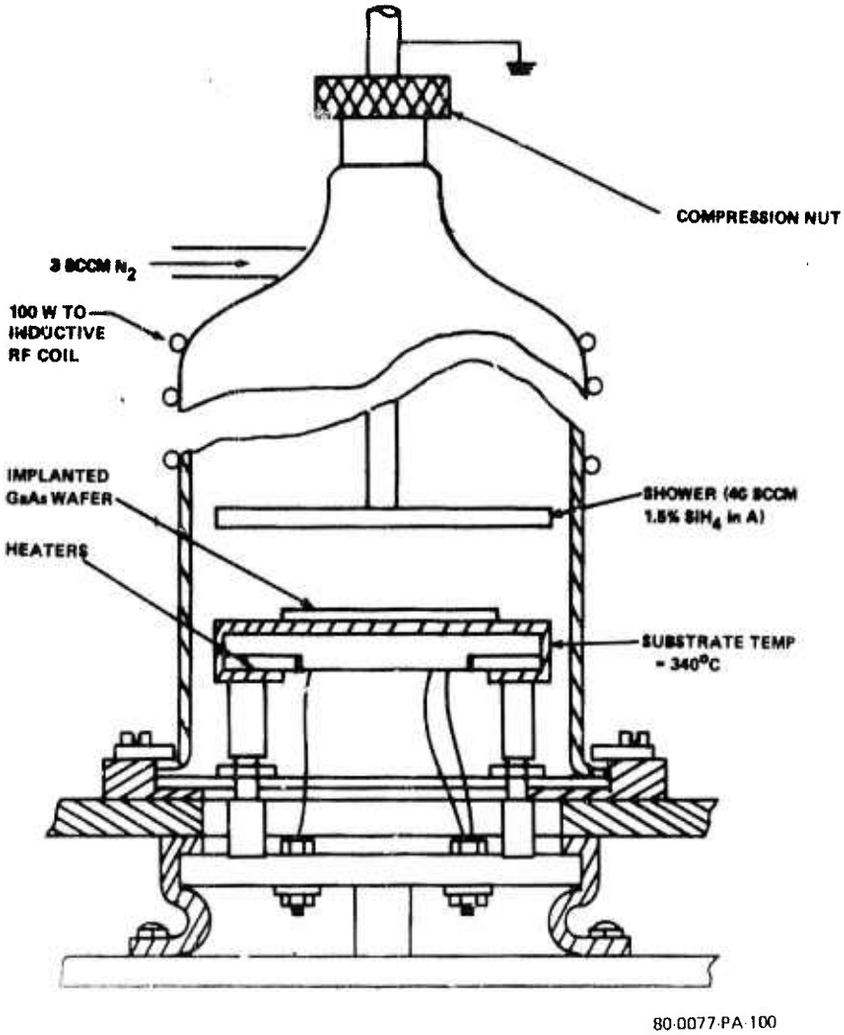


Figure E-3. Cross Section of Plasma-Enhanced Si_3N_4 Deposition System

dissociating an N_2 gas stream that enters at the top of the reaction chamber. One to one and a half percent SiH_4 in A is fed coaxially through the zone in stainless-steel tubing to prevent premature decomposition of the SiH_4. The SiH_4 enters the reaction chamber proper through a 5-in. diameter showerhead placed 5/8 in. above the sample. A fraction of the RF power is coupled to the showerhead to achieve SiH_4 decomposition by capacitive coupling to the sample stage. This configuration permits elimination of the more common reactant NH_3 which always contains H_2O and hence leads to oxygen contamination of the nitride. Deposition rate is a strong function of substrate temperature for temperatures below 260°C, and Si_3N_4 encapsulants for GaAs that perform well at 860°C annealing have not been achieved for deposition temperatures below 300°C. A 340°C deposition temperature was chosen to ensure volatilization of excess surface As, which occurs at 327°C, while minimizing oxidation that results when wafers are inserted on the preheated substrate stage. This technique then permits desorption of absorbed contaminants that can be trapped under the encapsulant decomposition of GaAs inherent in deposition at temperatures in excess of 550°C. The RF field configuration minimizes the density of high-energy ions and the electric field strength in the neighborhood of the GaAs surface and threrefore minimizes the surface radiation damage and/or nonstoichiometric sputtering that could be substantial in desposition by RF sputtering.

Optimization of the plasma-enhanced deposition of Si_3N_4 was achieved by varying the mass-flow controlled N_2 and 1-1/2 percent SiH_4 in A rate at RF power of 100W and substrate temperature of 340°C. Optimum deposition was achieved on N_2 flow rate of three sccm and a 40-sccm rate for the SiH_4 mixture. This yields an encapsulant that is viable to 1000°C on GaAs with uniform optical constants and $\pm$10 percent thickness uniformity of $\pm$100Å.

Unfortunately, deposition of viable encapsulants requires extremely precise control of the SiH_4/N_2 reactant ratio. Daily recalibration must be performed to compensate for zero offsets and RF coupling to the mass-flow controllers and gradual degradation of the SiH_4 mass-flow sensor. A valuable tool for this recalibration is the automatic ellipsometer, a detailed ellipsometer study of index of refraction and thickness as a function of deposition time is shown in figure E-4. This figure shows that a single layer analysis of the optical data implies a time-dependent growth rate and refractive index that is not physically reasonable. A two-layer analysis indicates a constant growth rate of a film with a refractive index of 1.93, which is consistent with a plasma deposited Si_3N_4. This is preceded by a 90-Å layer of index 1.54 which is presumable SiO_2; this layer is too thick to be a native oxide on the Si substrate. Figure E-5 shows an Auger profile through a 500-Å plasma nitride layer on GaAs after annealing at 860°C for 15 minutes. Although there was a problem with a high-oxygen background during this Auger measurement, this data is presented because it clearly demonstrates an SiO_2 layer at the Si_3N_4/GaAs interface and the out diffusion of Ga into the SiO_2 as a result of annealing. Ga does not diffuse into the Si_3N_4 proper, and neither Ga nor As in detected on the free surface. This interfacial layer is not acceptable since it results in reduced channel mobility and erratic surface activation. It has been found that a two-minute preburn in the N_2 reactant eliminates the interfacial layer; presumably, this layer is the result of reaction of SiH_4 with O_2 that is rapidly desorbed from the chamber surfaces when the RF discharge is first initiated. Figure E-6 shows the infrared absorbance spectrum of a 2000Å plasma Si_3N_4 layer on GaAs relative to bare GaAs in the case where the preburn was used. This demonstrates that the broadening and displacement of the Si-N absorption band associated with oxygen contamination has been eliminated.

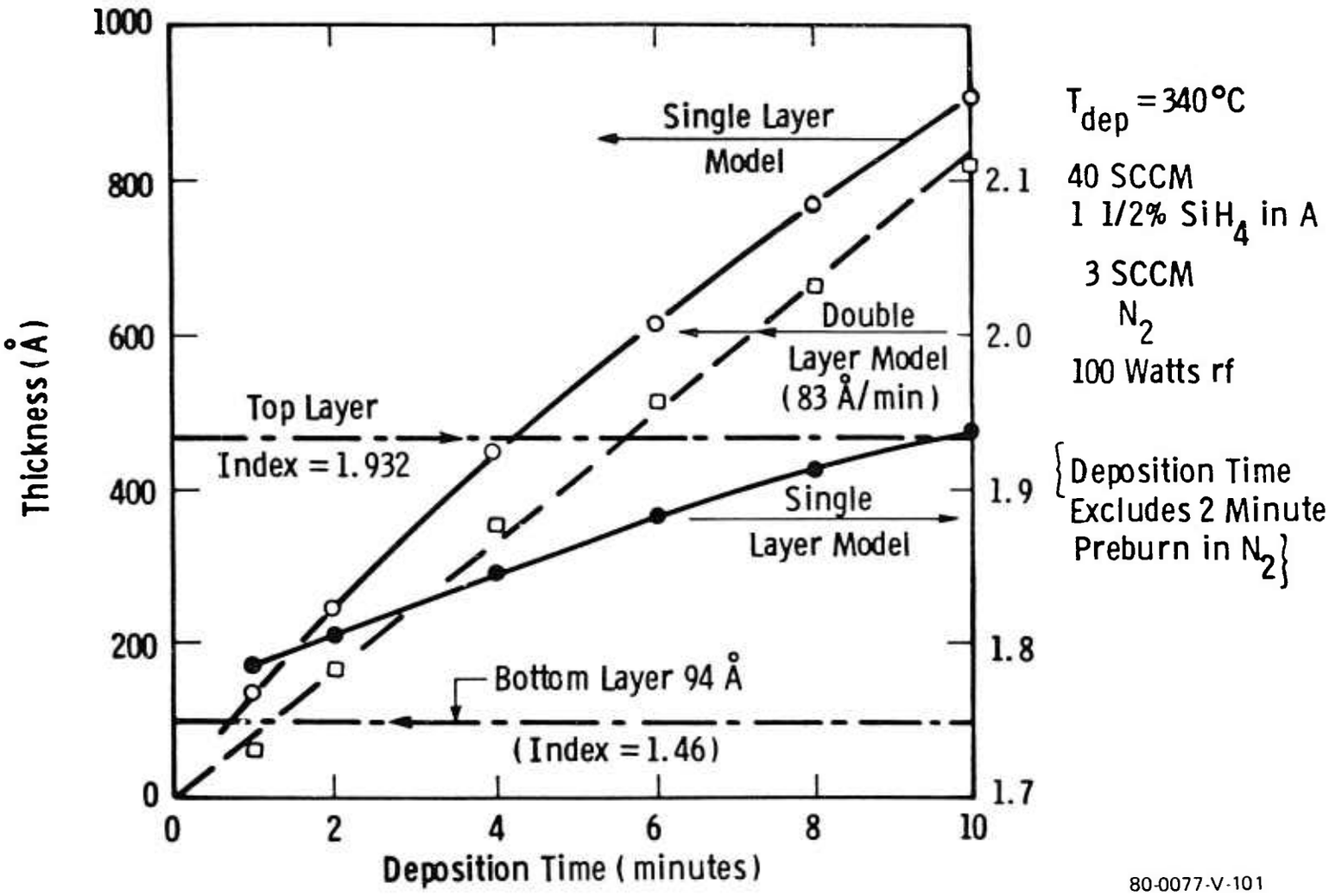


Figure E-4. Ellipsometer Analysis of Plasma Si_3N_4 on Si

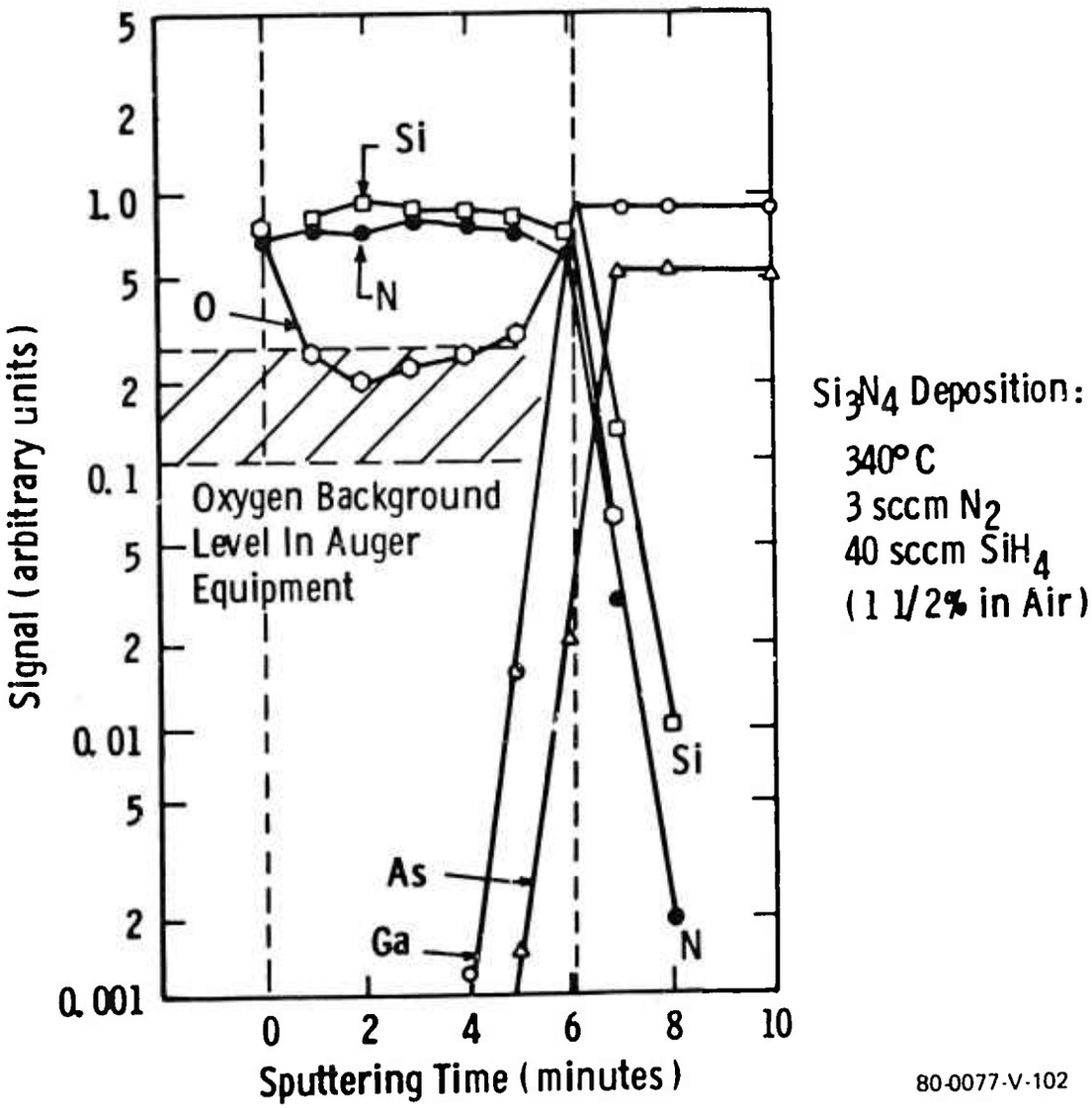


Figure E-5. Auger Profile Through Annealed Plasma Si_3N_4 on GaAs: 860°C, 15 min. Anneal

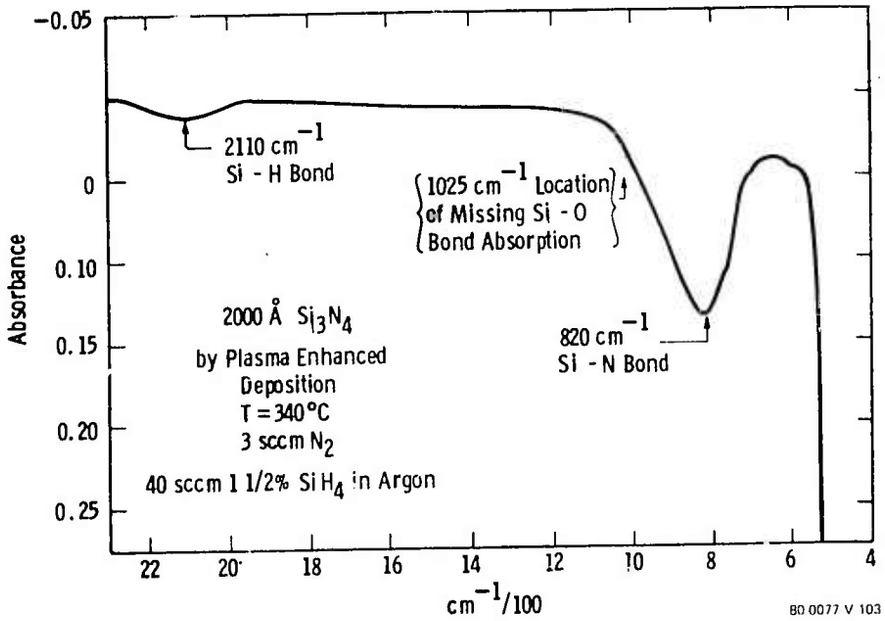


Figure E-6. Infrared Absorbance Spectrum of Plasma-Deposited Si_3N_4 on GaAs

E.4 FINAL ECAPSULATION AND ANNEALING

Prior to annealing, a second encapsulant layer of 2500Å, 7 percent phosphorus-doped SiO_2 (PSG) is laid down by chemical-vapor desposition. The phosphorus doping is employed to ensure that this glass becomes plastic at the 860°C annealing temperature and does not lead to stress damage associated with differences in thermal expansion coefficients. The glass itself is an essential element in the registration of selective implants and prevents pit formation at pinholes in the primary Si_3N_4 encapsulant. Details of the PSG deposition are not critical except that it must be performed at low temperature (400-450°C) due to the poor oxidation resistance of the plasma nitride.

All anneals are performed in a forming-gas atmosphere using the furnace shown in figure E-7. This figure shows 3-in. wafers on an early pallet configuration. Subsequently, very low camber, high thermal platforms have been added in order to achieve the low wafer distortion required for subsequent photoresist processing. Annealing is performed by automatically ramping the

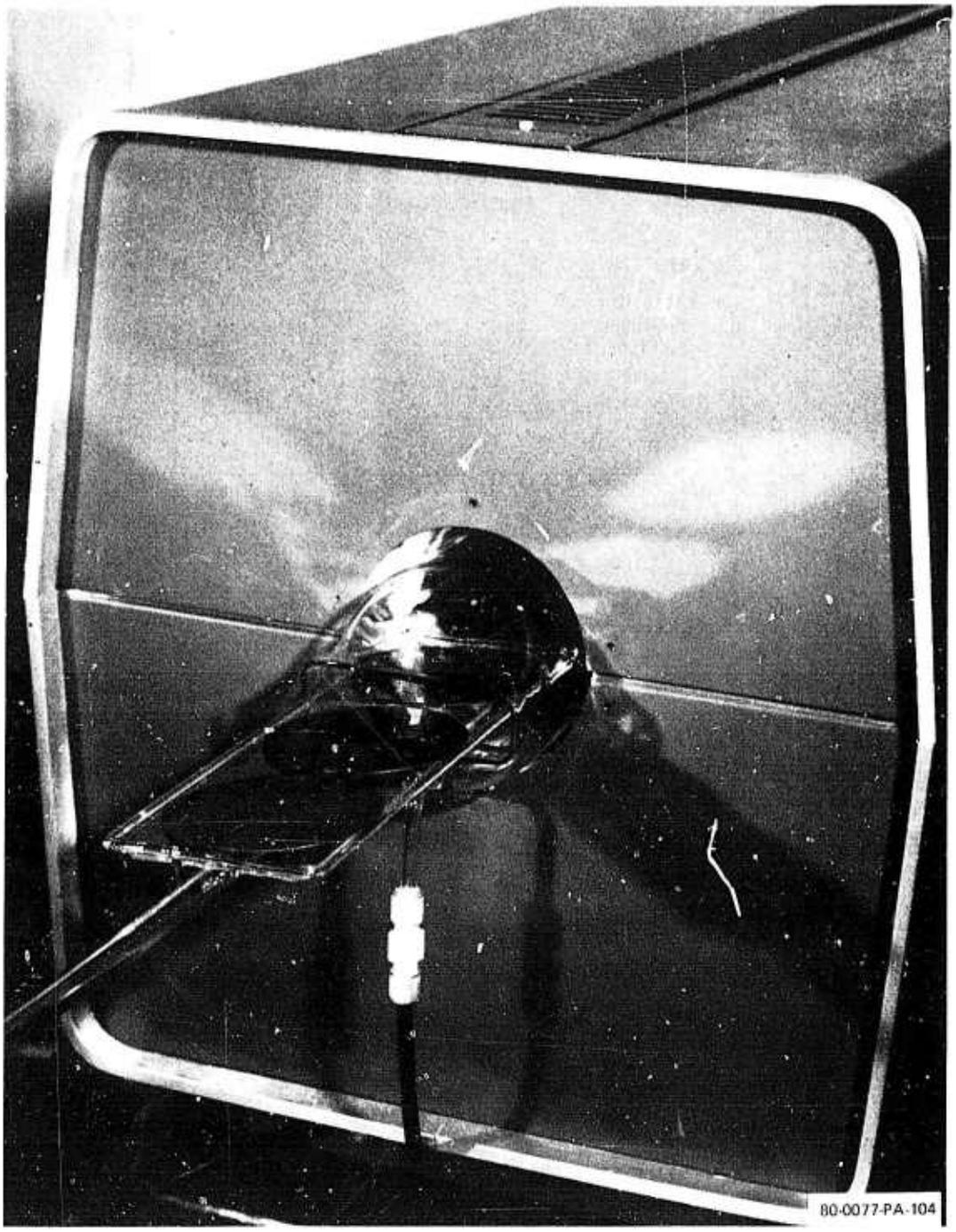


Figure E-7. Ramp Annealing Furnace (Prior to Installation of High Thermal Conductivity Wafer Support). 3-in. Diameter Wafer Included to Show Size

furnace to achieve the time-temperature characteristic shown in figure E-8. This procedure minimizes thermal shocks that result in distortion and reduced mobility as well as improving reproducibility.

E.5 SELECTIVE ION-IMPLANT TECHNOLOGY

Figure E-9 and E-10 outline the procedure used to achieve selective ion implantation. Figure 9(a) shows the substrate encapsulated with Si_3N_4/PSG and photoresist applied for definition of the active channel. A Kasper photoaligner is employed for this and all subsequent photoresist steps. A Veeco ion miller is employed to remove PSG from the active channel window (figure 9(b). Implantation of the channel is performed through the Si_3N_4, and the photoresist/PGS, Si_3N_4 acts as the beam stop in the remaining areas. Figure 9(c) shows the sample after deposition of a second PSG layer and photoresist definition for the implant of n^+ source-and-drain pads. The PSG window is opened and the n^+ implant is performed as described above (figure 10(a)). Annealing is performed

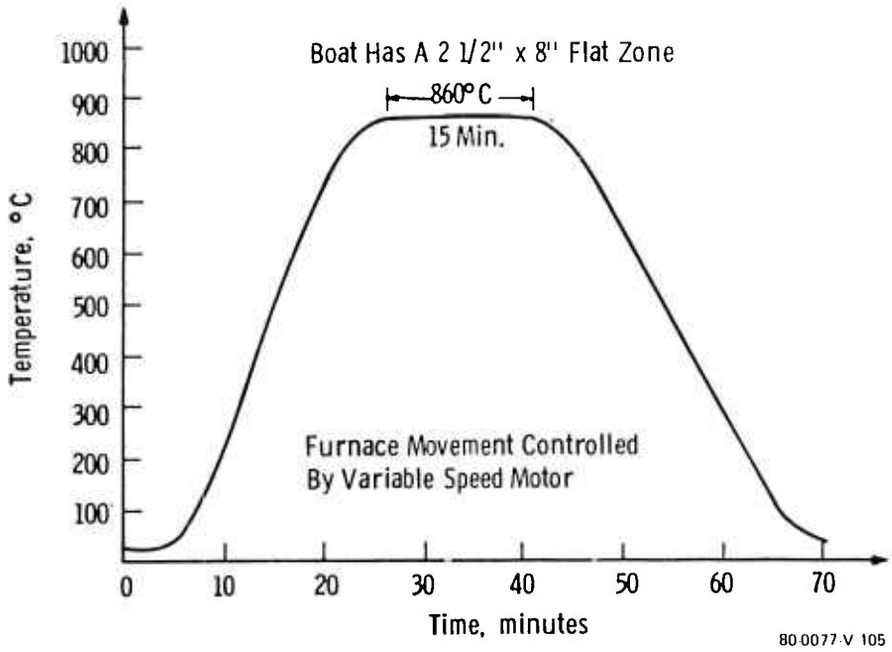


Figure E-8. Ramped Temperature Profile of Westinghouse Anneal Furnace for Implanted GaAs

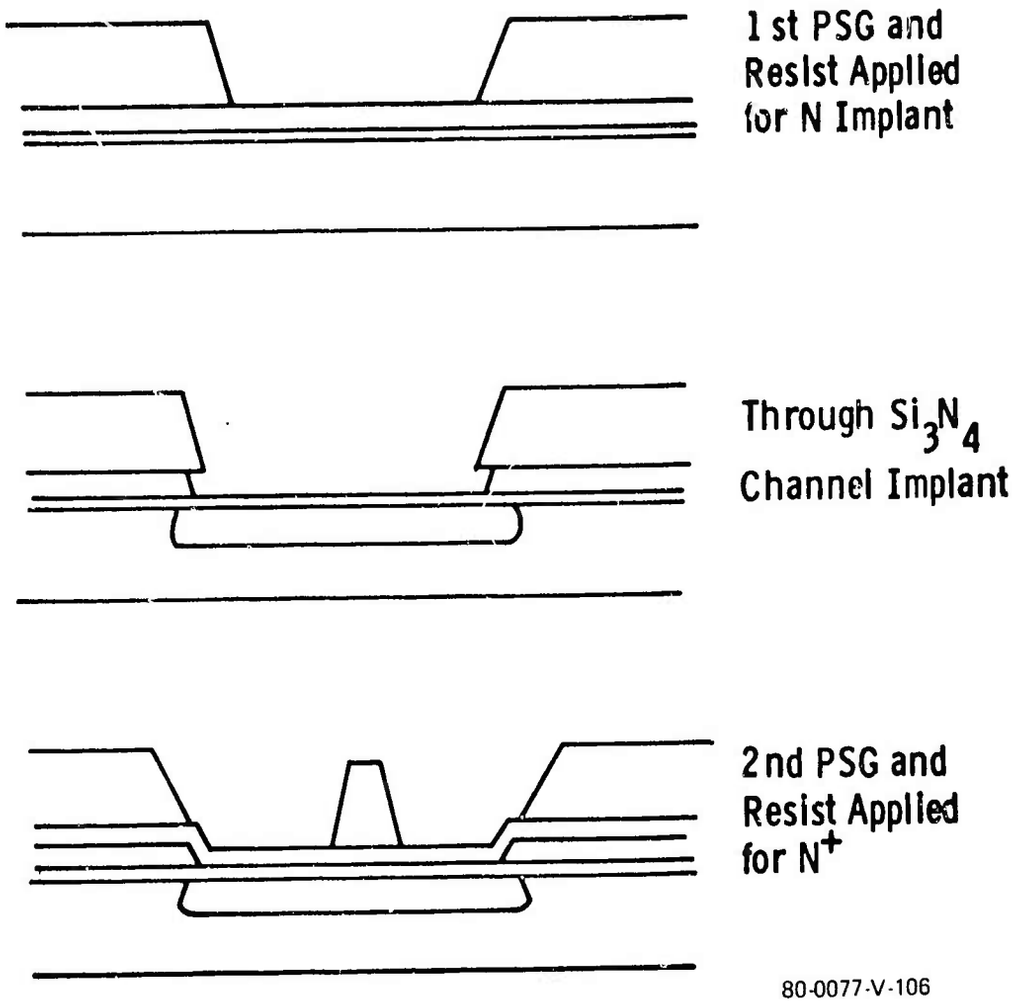
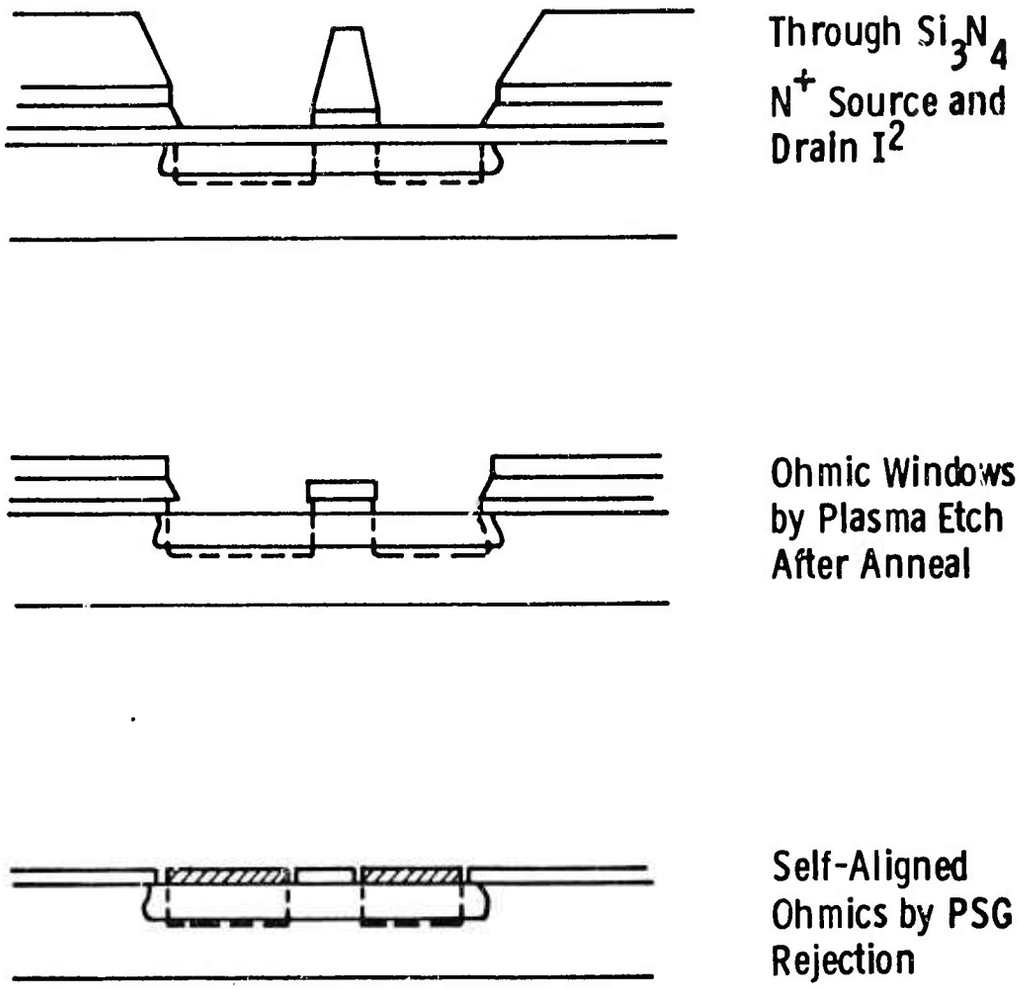


Figure E-9. Selective Implantation Fabrication Sequence



Figue E-10. Selective Implantation Fabrication Sequence (Cont'd)

after removal of the second photoresist so that the n^+ region is encapsulated by Si_3N_4, alone. Deposition of ohmic-contact metals and contact forming follows opening the Si_3N_4 from the n^+ pads by plasma etching in a plasma etcher (figure 10(b)). Chemical etching of the PSG yields a structure with selfaligned source-drain contacts ready for gate and circuit fabrication. In cases where n^+ pads are not used, annealing is performed after the second photoresist is used to define ion-milled registration marks cut into the GaAs, itself.

E.6 QUALIFICATION FOR ION IMPLANTATION

Qualification for ion implantation is an experimental process for determining whether a semi-insulating GaAs ingot exhibits the conversion, activation, profile integrity, and mobility characteristics required for ion implantation. This is performed in lieu of an ability to grow semi-insulating GaAs reproducibly or to specify satisfactory ingots in terms of fundamental material parameters. Appropriate qualification processes are determined by the class of GaAs substrate, encapsulation technique, implant type, and technology details so that the qualification technology is not transferable. The Westinghouse qualification process has evolved during this reporting period as a result of improved substrates and encapsulation as described below.

The Westinghouse qualification at the beginning of this program involved the following measurements:

1. As received-sheet resistivity
2. Resistivity after 750°C bare anneal in H_2
3. Resistivity after 860°C encapsulated anneal
4. Resistivity after argon implant and 860°C encapsulated anneal
5. Hall effect after typical channel-implant processing
6. C-V profiling after typical channel-implant processing

The first test has been specified at $\rho \geq 10^7$ ohm-cm and has remained fixed. Particularly, old ingots in our purchased inventory and the seed ends of undoped LEC ingots may fail this test. The second test can provide a definite indication of

failure if gross n-type conversion occurs. Less dramatic failures where $\rho_{\square} = 10^6 - 10^7$ ohm and conversion type cannot be established providing no useful data since the material may pass all of the encapsulated anneal test. The second test in no longer used.

Test number 3 has been specified at $\rho \geq 10^7$ ohm/□ and has remained fixed. This value was determined by comparison with the equivalent full-channel sheet resistance of active layers (5×10^2 ohm/□), low-leakage objectives at pinchoff, and geometrical considerations. Test fabrication runs have demonstrated that good discrete FET's can be achieved despite a $\rho \cong 5 \times 10^5$ ohm/□ failure, but that the circuit losses on such material are not acceptable.

Test number 4 can reveal radiation-induced conversion problems although these problems can be concealed by surface depletion. The same problems are definitely identified in the active implant tests, however. Inert-gas implant tests for conversion have been discarded.

The Hall effect measurements used in test number 5 are designed to permit subsequent device implantation to a specified active-channel charge. As many as eight samples are implemented to doses between 3×10^{12} and 8×10^{12} cm^2. Half of these samples receive only the 250 to 400-kV $^{29}Si^+$ implant. The other half receive the channel implant plus a surface-fill implant to yield an approximately constant chemical concentration to the surface. Room-temperature Hall measurements are made on Van der Pauw samples to yield the active concentration per unit area. Typical plots of active concentration vs implanted dose are shown in figures E-11, E-12, and E-13. The raw data is shown as well as the data corrected for surface depletion and its associated linear-differential activation efficiency and threshold dose. The depletion correction is dependent on whether or not a surface-fill implant is performed and, to a lesser extent, on concentration. The depletion is consistent with 0.6-eV surface barrier. (This correction is checked later with a measurement of the zero-bias depletion of a Schottky barrier contact.) Figure 11 refers to a vendor-supplied Cr-doped, 2-in. LEC ingot. The data is

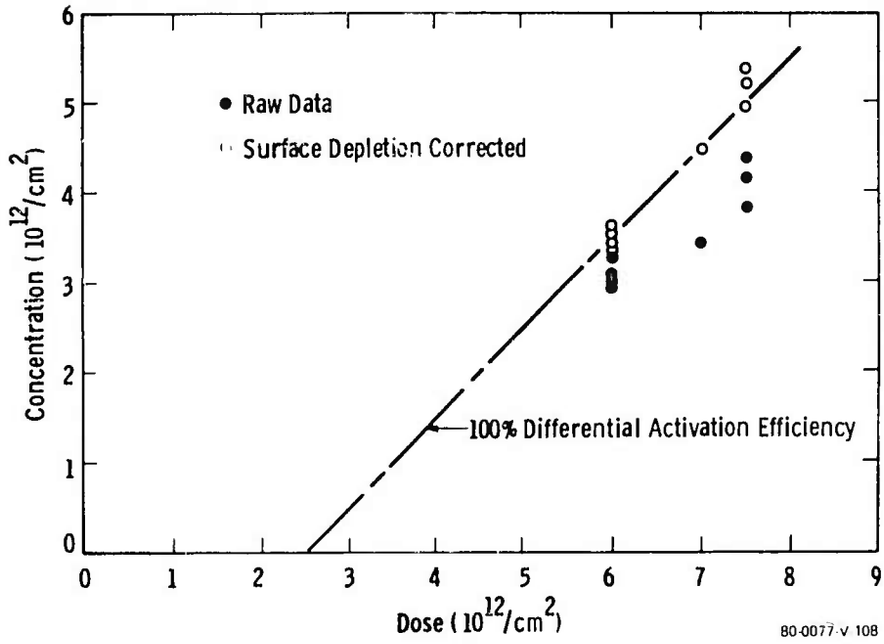


Figure E-11. Differential Activation Efficiency and Threshold Dose in Cr-Cped LEC-GaAs

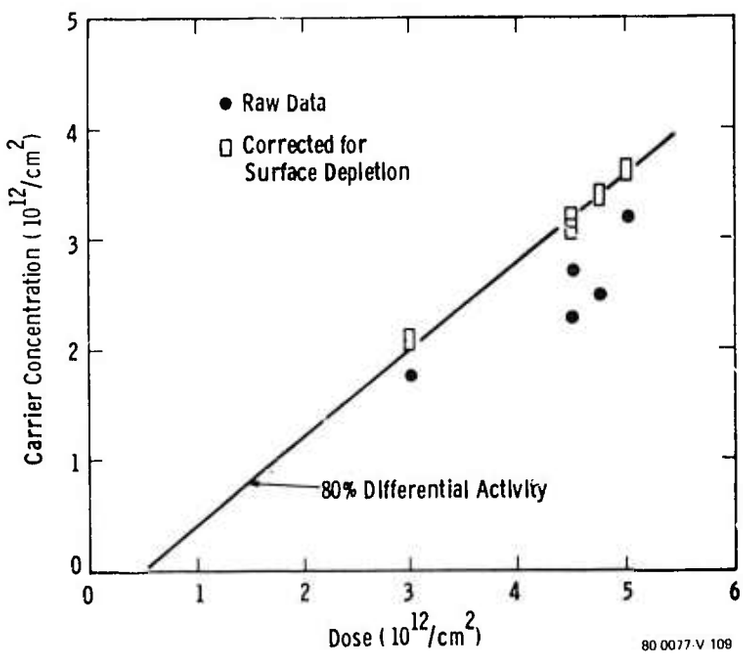


Figure E-12. Differential Activation Efficiency and Threshold Dose in Undoped, PBN-Grown LEC GaAs

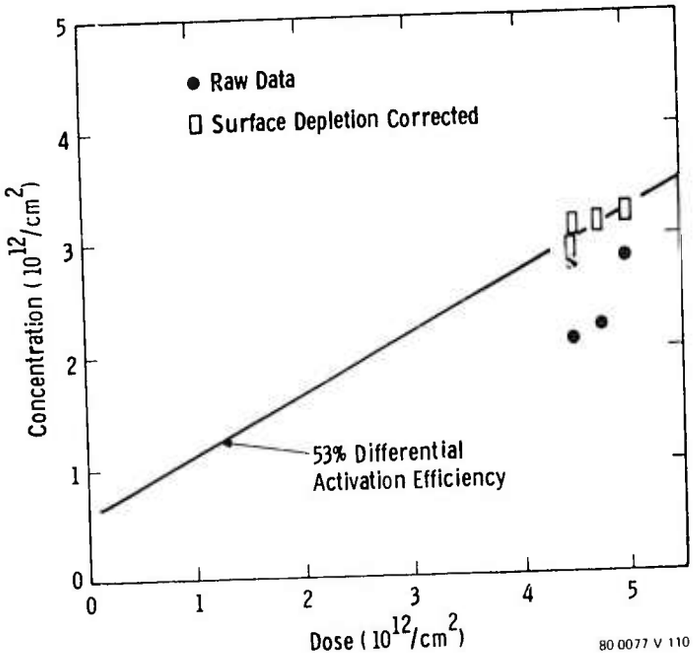


Figure E-13. Differential Activation Efficiency and Threshold Dose in n Conducting GaAs

comparable to Westinghouse Cr-doped ingots. The differential-activation efficiency lies between 80 and 100 percent in all cases. Boat-grown ingots yield similar data, except that the differential-activation efficiency is 60 to 80 percent and the threshold doses fall between 1 and 2 x 10^{12} cm^2. SIMS analysis of both LEC and boat-grown ingots suggests that the threshold dose is correlated with the excess Cr concentration. Figure 12 refers to an undoped Westinghouse ingot grown in PBN. The corrected data indicate a differential-activation efficency of 80 percent and a threshold dose of approximately 0.5 x 10^{12} cm^2. If it is asumed that the threshold is the result of the requirement to fill uncompensated deep acceptors prior to observing free carriers, this value implies an uncompensated deep acceptor density of 1.2 to 1.6 x 10^{16} cm^3. This material yields exceptional reproducibility as a result of the low density of defect levels and proportionally lower axial and radial gradients in this density. A similar analysis applied to Cr-doped material yields

uncompensated acceptor densitites of 6 x 10^{16} cm^2 to 1.2 x 10^{17} cm^3 and the density gradient of uncompensated deep levels in boat-grown ingots can be so large that the implant dose must be adjusted according to position along the ingot. Figure 13 shows the activation data for a contaminated undoped ingot that failed test no. 1 due to excessive bulk n-type conductivity. This is reflected in the active concentration of 0.5 x 10^{12} cm^2 in the unimplanted sample. This test was performed to demonstrate that a threshold dose would not appear in a case where uncompensated acceptors were known to be absent. Figure E-14 shows surface Hall-mobility measurements versus peak-carrier concentration for the qualification specimens shown in figures 11 through 13. In some cases, mobilities at liquid-nitrogen temperature is shown as well as the ambient temperature values.

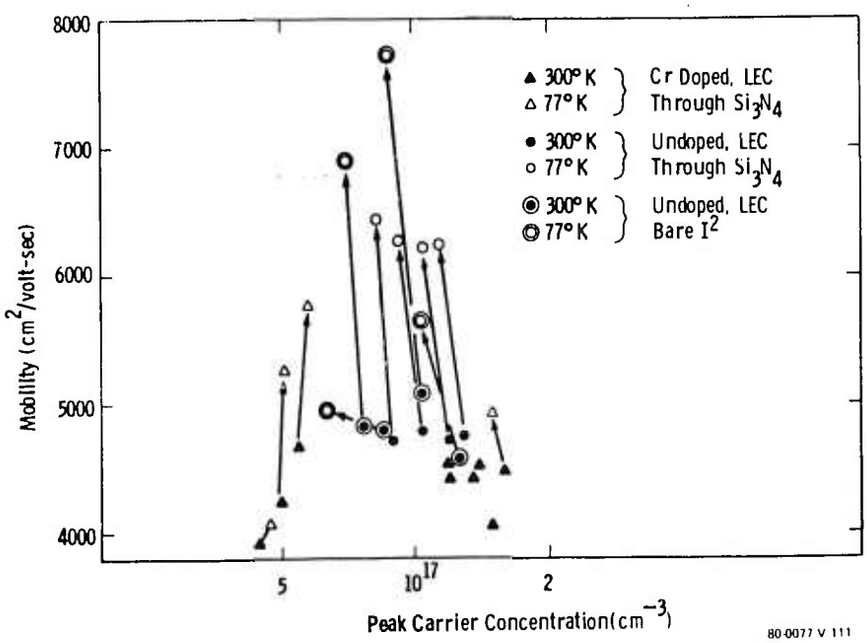


Figure E-14. Detail of Mobility Values Comparing Doped and Undoped Values and Bare and Encapsulated Implants

It should be noted that the mobility is deduced from

$$\mu = \int_0^\infty \mu^2(z)n(z)dz \Big/ \int_0^\infty \mu(z)n(z)dz$$

where n(z) is the carrier concentration at a depth z in the layer where the mobility is $\mu(z)$ and both the numerator and denominator are obtained directly from the van der Pauw measurement; no theoretical corrections are introduced. Also, if n(z), is a simple guassian and a linear expansion of $\mu(z)$ is performed in n(z), it can be shown that the equivalent uniform concentration for this mobility is the maximum concentration divided by the square root of two. Since none of the guassians are simple and many of the samples contain surface fills, peak channel concentration is taken as the independent variable; comparisons with uniform epitaxial layer data should be made with caution.

The reproducibility and uniformity of the Hall mobility in undoped ingots grown in PBN (μ = 4750-4900 cm^2/volt-sec) is very impressive. Two ambient temperature values fall outside this range and both refer to bare implants. It is clear, particularly from the corresponding 77°K mobility values, that the bare implants lead to both anomalously superior and inferior performance. We believe that this is due to the competing effects of the experimental difficulty of surface cleaning for encapsulation after implementation and of forward knock-on implantation. It is also clear that implantation through Si_3N_4 does not lead to overriding excess-defect densities in contrast to intuitive fears. The reproducibility of mobility values in Cr-doped ingots is not particularly good. The mean mobilities in Cr-doped LEC ingots is 4400-4500 cm^2/volt-sec and the best Cr-doped, boat-grown ingots exhibit values of 4200-4400 cm^2/volt-sec. These reductions imply higher defect densities in the Cr-doped densities, and the more substantial reductions in the 77°K values confirm this result.

Figure E-15 compares Westinghouse mobility data averages for different substrate types and encapsulation processes with theoretical values of 300°K mobility as a function of carrier concentration. This figure includes two descriptions of the

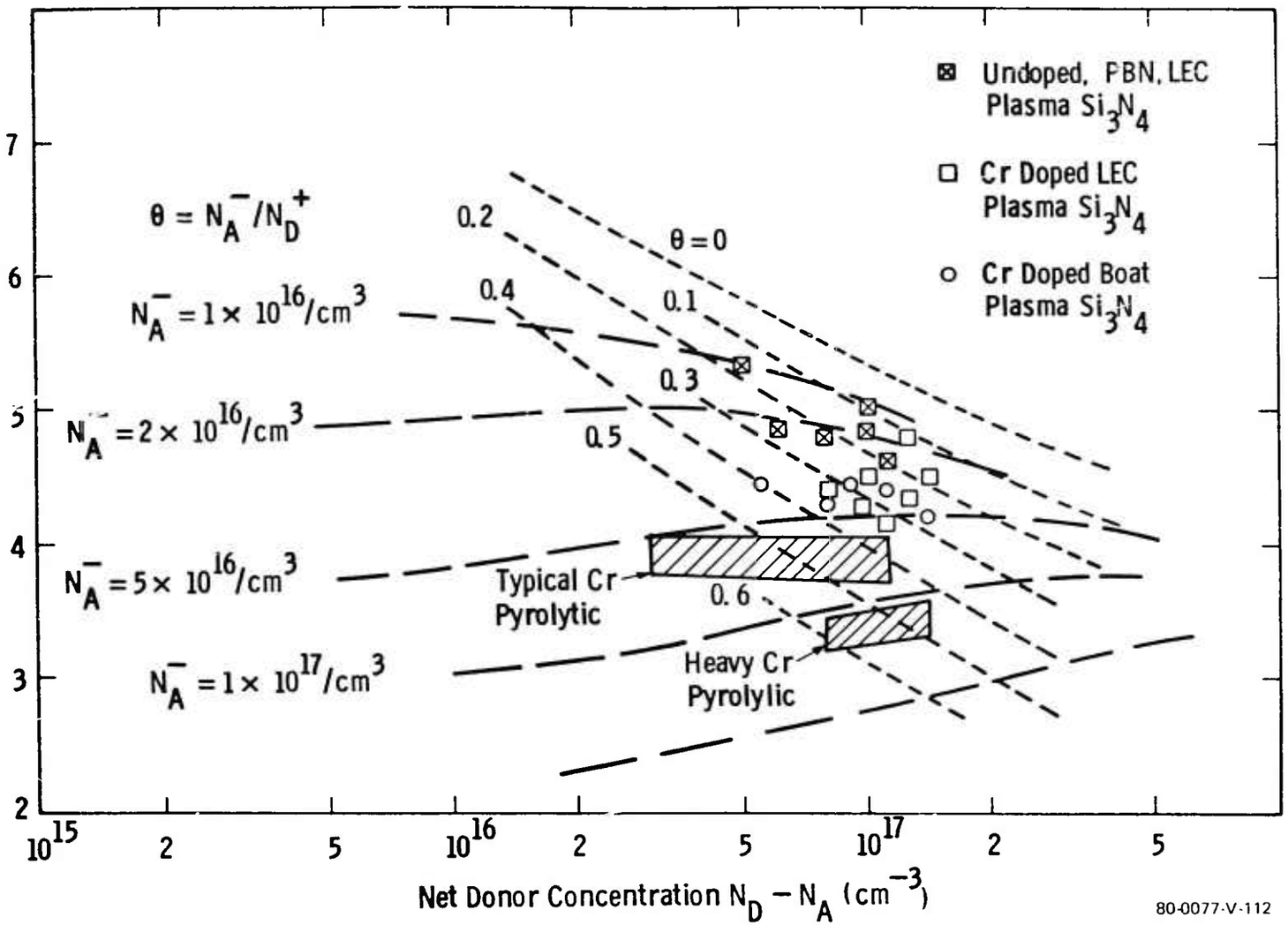


Figure E-15. Comparison of Typical Mobility Data by Substrate and Encapsulation Process with Theoretical Mobility vs Charged Impurity Density

effect of ionized-impurity concentration in reducing mobility. The measured mobility should follow lines of constant compensation if the primary source of these defects is unannealed damage or Si_{Ga} which is, therefore, proportional to dose. The measured mobility data should follow lines of constant ionized-acceptor concentration if the primary contribution is the grown-in impurity concentration plus an additive constant due to the encapsulated anneal. This additive constant is evident in the older pyrolytic encapsulation data. There is an argument to indicate that the additive constant is not significant for the plasma-encapsulated, undoped samples, i.e., we have oxygen concentration data in these As-grown samples and, if we assume that oxygen is the only significant donor present, the total acceptor concentration can be obtained from this data and the threshold data for uncompensated donor activation. The mobility data is consistent with this value.

We can conclude the following from the data described above:

1. Undoped, PBN-grown GaAs ingots grown at Westinghouse yield excellent and reproducible high-mobility-implanted FET's.

2. Use of Cr-doped ingots implies a sacrifice in both mobility and reproducibility.

3. The Westinghouse plasma-enhanced encapsulation process yields state-of-the-art mobilities and its contribution to mobility-limiting defect density is less than or equal to the inherent defect density in the best substrate material available.

C-V profiling of qualification samples (test 6) is employed to estimate the activation efficiency of surface-fill implants, to measure the standard deviations of the profile, and to ensure that surface anomalies and deep tailing are absent. A front-surface concentric Schottky pattern and a "Miller" (Lehighton Electronics) capacitance profiler are used for this purpose. Figure E-16 shows the profile of one of the Cr-doped samples presented originally in figure E-11. The uniformity of activation can be estimated and the depletion at zero bias is consistent with an 0.8-eV barrier without anomalous surface activation or compensation. A joined half-guassian analysis can be performed to obtain the projected range and the standard deviations. In this particular case, implants

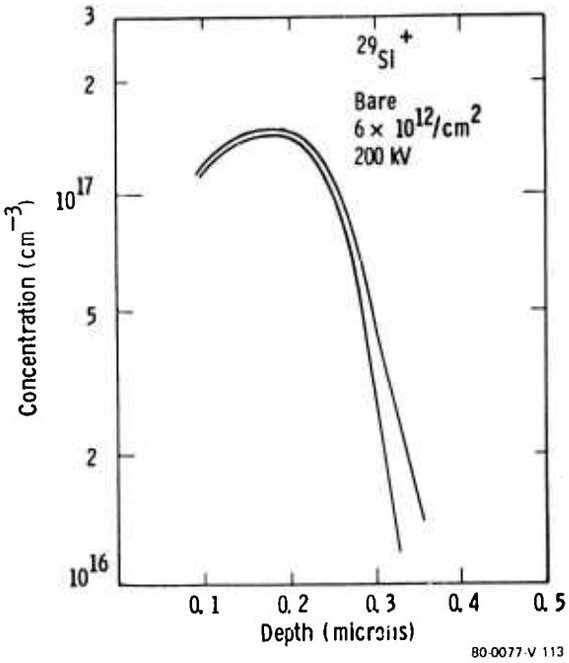


Figure E-16. Profile of a 200-kV Si Implant Into Cr-Doped, LEC GaAs

were performed over a wider than normal energy range so that R_M, σ_p, σ_s, and σ_d could be measured as a function of energy. The results are shown in figure E-17. R_p agrees with tabulated values. R_M plus G_p values allow a calculation of the shallow and deep standard deviations σ_s and σ_d. The calculated σ_d agrees with experimental values, while the σ_s value cannot be estimated because not enough of the shallow profile is measured. The projected standard deviation does not agree with tabulated values; third order moment corrections are not valid either. The deep standard deviation in Cr-doped ingots appears to be independent of energy and may be determined by the profile of out diffusion Cr on the deep profile side. This hypothesis is demonstrated in figure E-18 by comparing active-layer profiles in undoped and Cr-doped LEC substrates grown at Westinghouse. There is some precision SIMS profile data to indicate that the abrupt cutoff in the Cr-doped substrate case is due to Cr

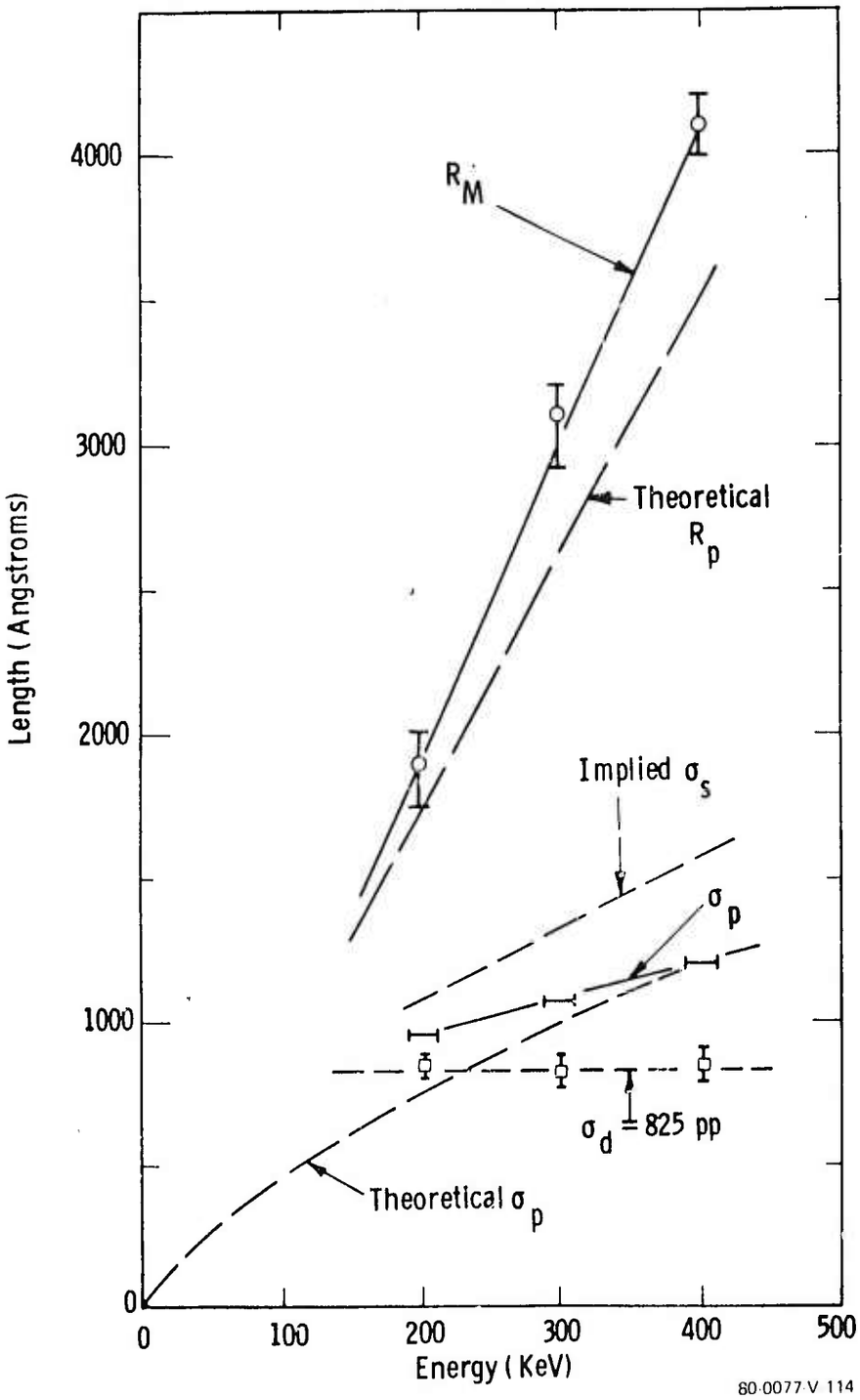


Figure E-17. Profile Parameters in Cr-Doped, LEC GaAs

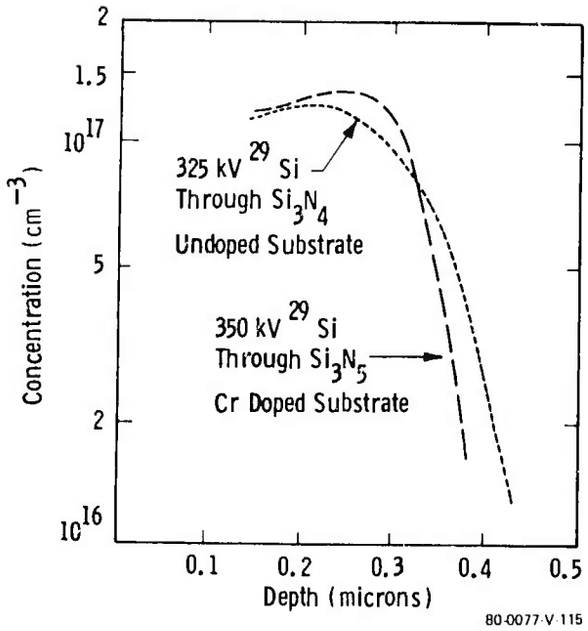


Figure E-18. Comparison of Net Donor Concentrational Profiles in Doped and Undoped GaAs Substrates

compensation and a gradient in the Cr concentration, rather than in the activation of implanted $^{29}Si^{+}$.

Figure E-19 shows the peak-donor concentration as a function of dose for the undoped PBN samples shown originally in figure E-12. Note that the data can be fitted to the same threshold dose (0.5×10^{12} cm^2) which would suggest that the model of filling deep acceptors is valid. If the previous differential-activation efficiency is combined with the peak-concentration data, a projected standard deviation of 1100Å is obtained and this is consistent with measured profiles. A similar analysis of the contaminated ingot samples shown in figure E-13 leads to similar results, except that the extrapolated threshold dose is zero instead of negative. This agrees with the statement that the anamalous activity is bulk rather that surface conversion phenomena.

The activation profiles in undoped, PBN-grown ingots agree reasonably well with both tabulated values and chemical profiling. Cr doping leads to a significantly sharper profile, but a price is

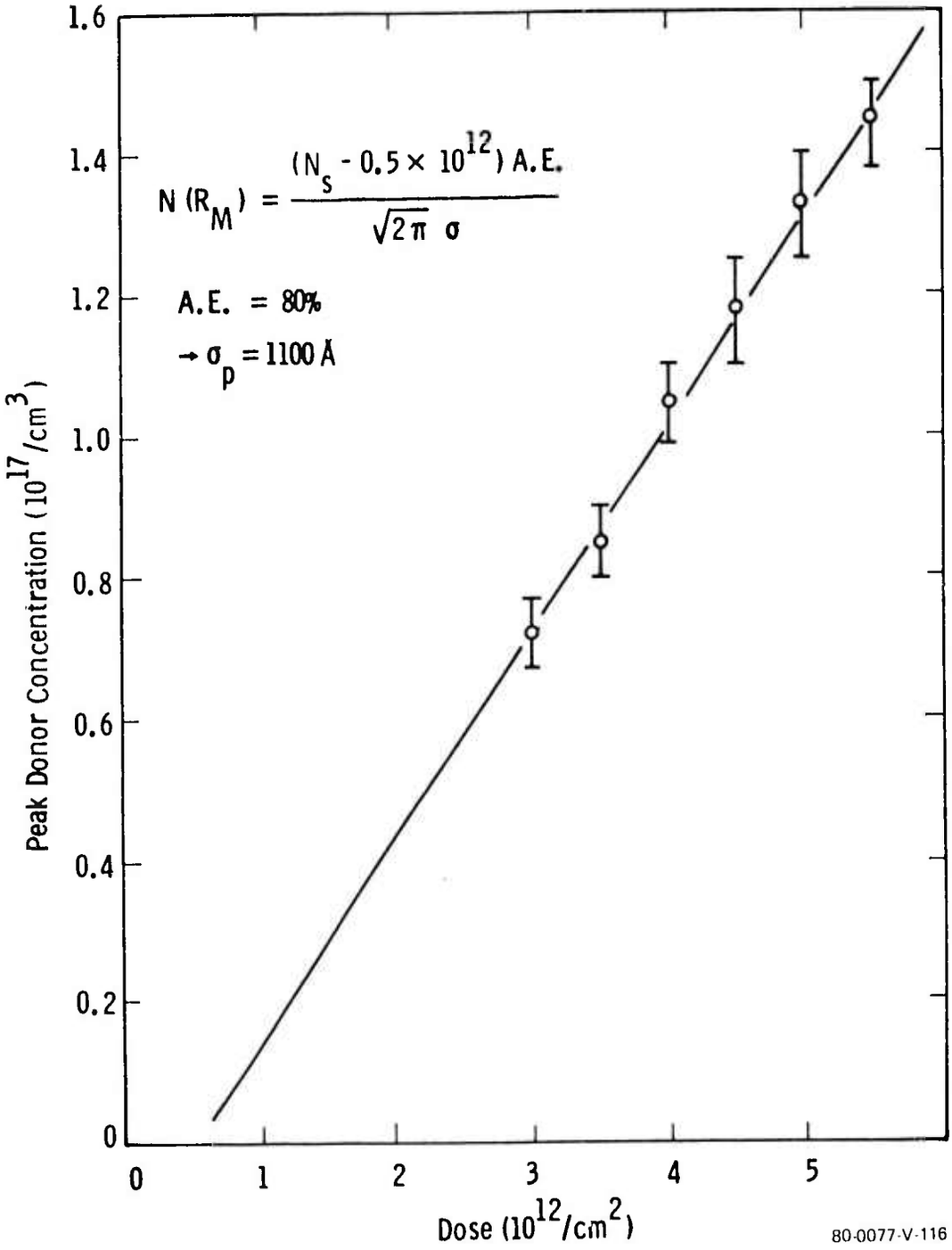


Figure E-19. Peak Donor Concentration vs Dose for Qualified, Undoped, PBN-Grown GaAs

paid in terms of average mobility and both profile and mobility reproducibility. Better transconductance near pinchoff and the possibility of reduced leakage at high source-drain voltage may be an overriding consideration; this question is being addressed.

E.7 IMPLANATION REPRODUCIBILITY

The range of implant profiles of interest for FET profiles is quite limited. This occurs in the first instance because the active concentration (N_s) must be held $\leq 3 \times 10^{12}$ cm^2 while maximizing N_s to increase the full channel current. In the case of an implanted layer, $V_{PO} = QN_sR_p/E$ so that the implant energy determines pinchoff voltage through the projected range. This energy also determines the projected standard deviation which in turn determines the maximum electron concentration per cm^3. Figure E-20 shows the maximum channel concentration that can be achieved as a function of the projected range in the GaAs substrate. This is shown for limiting gate recesses of 0 and 1500Å and assuming $N_s = 3 \times 10^{12}/cm^2$. The range of interest is a narrow band extending from 1.7×10^{17} cm^3 at 2000Å to 1.1×10^{17} cm^3 at 3000Å. The narrow range of interest demands corresponding reproducibility in the activation efficiency and profile to obtain useable material. The adjustment available during fabrication is a $\pm$250Å adjustment in gate recess depth which can do no more than adjust N_s by $\pm 0.4 \times 10^{12}$ and adjust V_{PO} by $\pm$0.8 volts.

Figure E-21 shows the profile objectives used during the early and later phases of this program. The early profiles employ the deep, low-concentration range with a low value of N_s while the later profiles approach the opposite extreme. Figure E-22 indicates the profile reproducibility achieved shortly after plasma nitride was introduced. Although reproducibility across slices and on adjacent areas was shown, surface-activation efficiency varied along the axis of the boat-grown boules. Figures E-23 through E-29 indicate the reproducibility currently achieved. Figures E-23 through E-25 refer to identical implants into Westinghouse, undoped, PBN LEC GaAs. Figures E-27 through E-29 refer to Westinghouse, Cr-doped, LEC GaAs where figures E-27 and E-28 refer to identical implants, as does the figure E-28-29 pair.

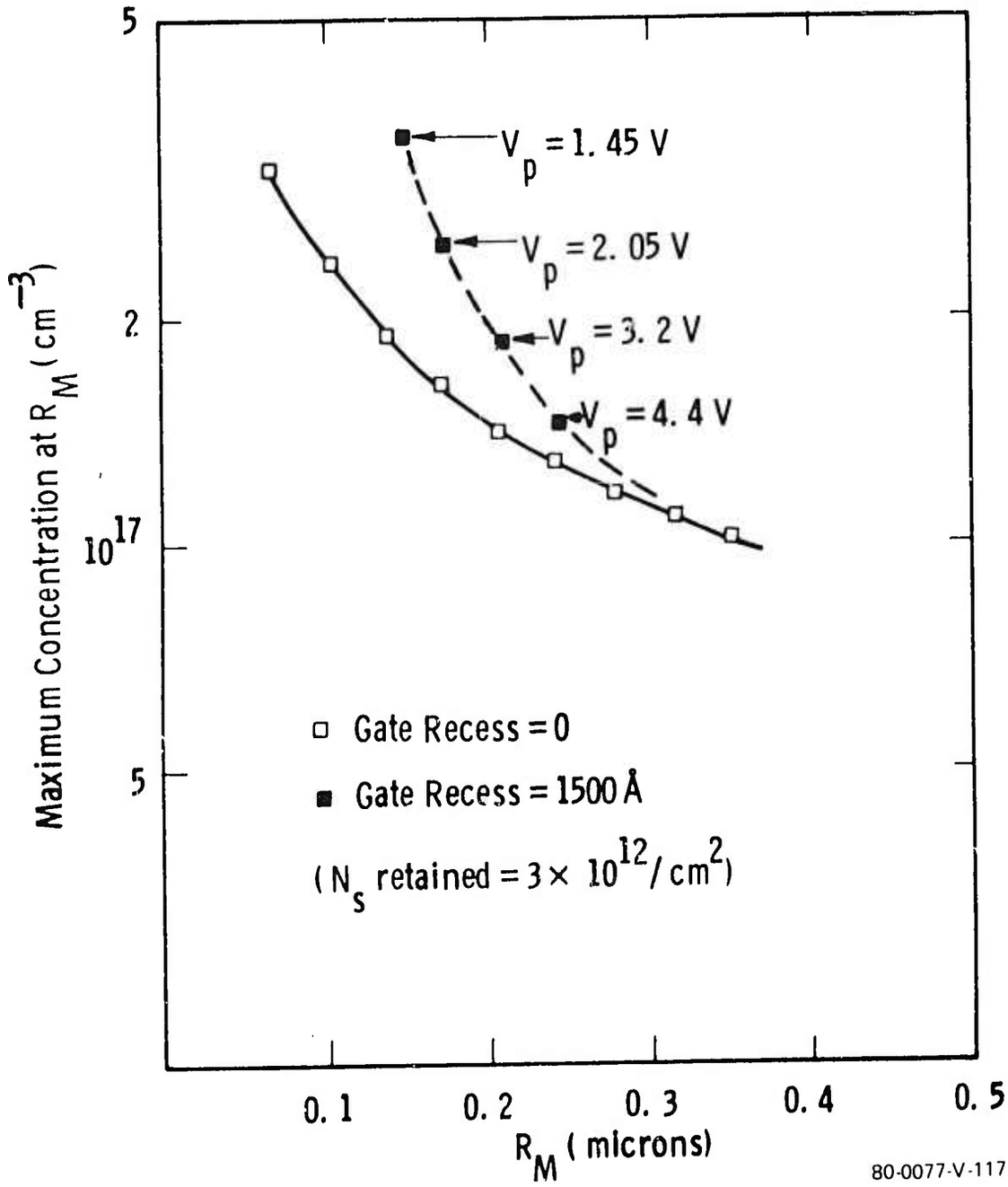


Figure E-20. Maximum Channel Concentration as a Function of Range

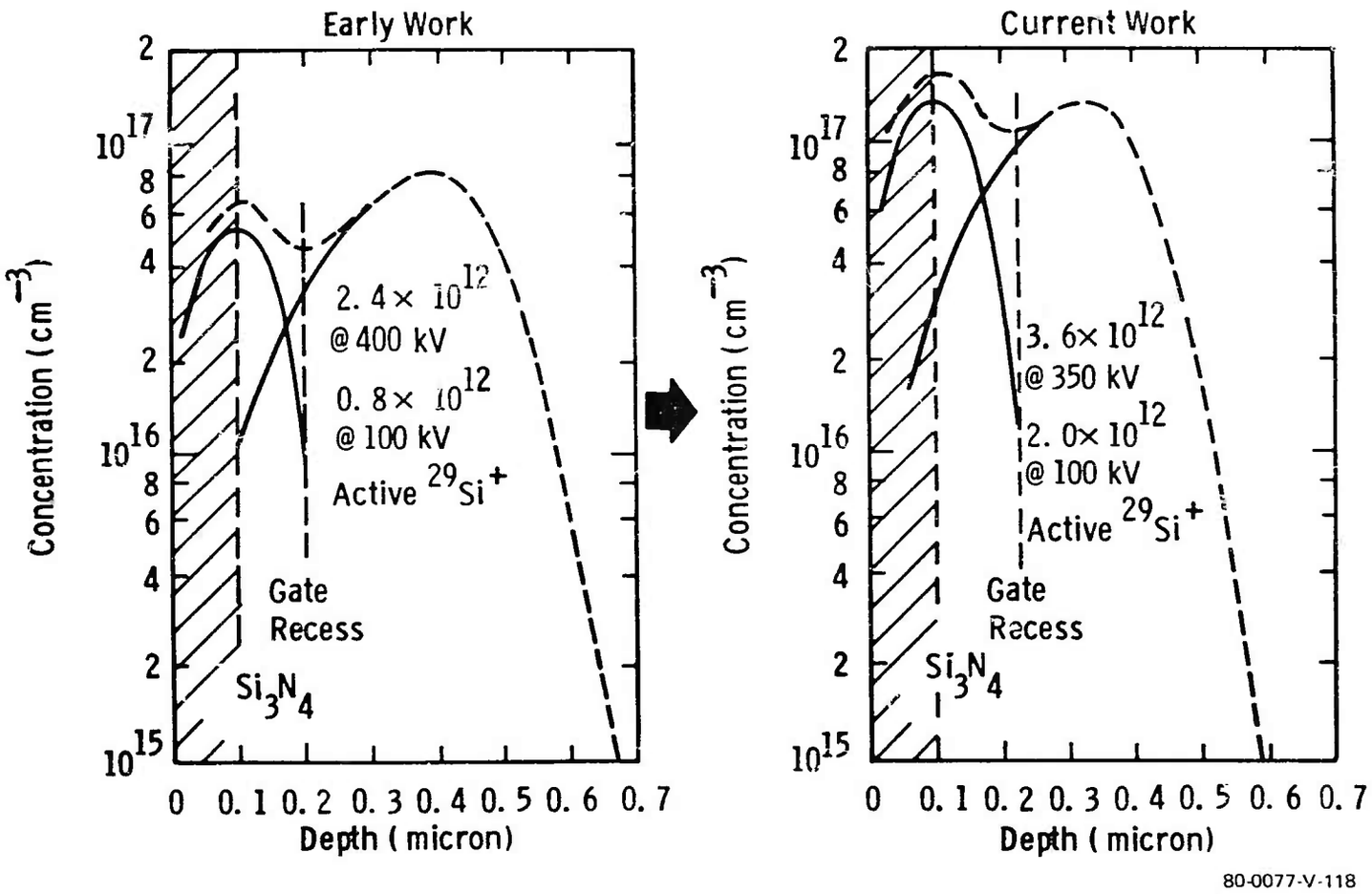


Figure E-21. Implant Profiles Under Investigation for GaAs Power FET's

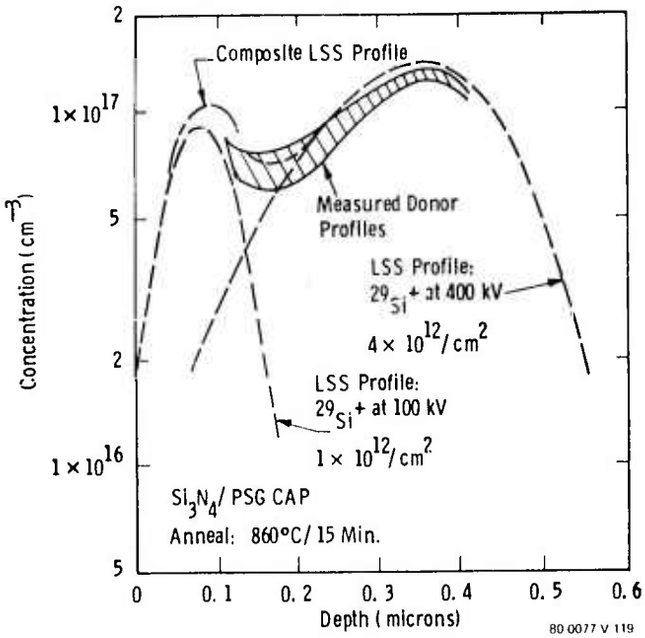


Figure E-22. Profile Reproducibility in Boat-Grown, Cr-Doped Ingots

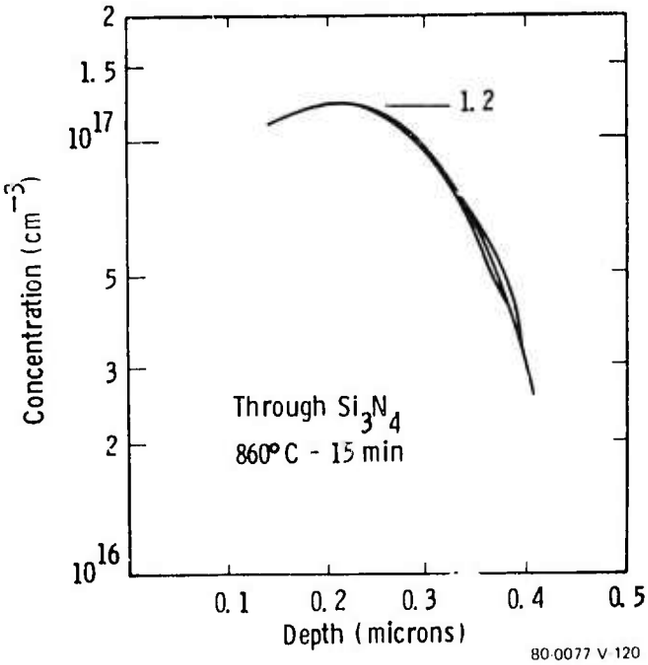


Figure E-23. $^{29}Si^{+}$ 5.5 x 10^{12} at 325kV Plus 2 x 10^{12} at 125kV in Undoped PBN-Grown GaAs Sample A

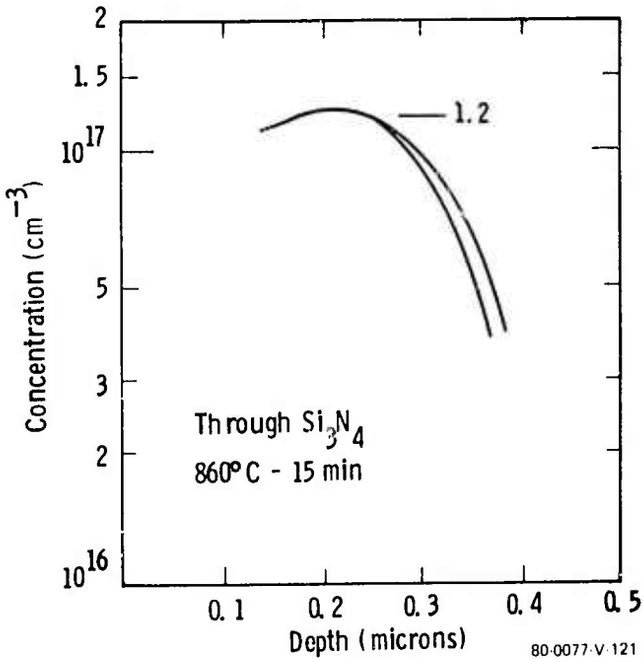


Figure E-24. $^{29}Si^{+}$ - 5.5 x 10^{12} at 325kV Plus 2 x 10^{12} at 125kV in Undoped PBN-Grown GaAs Sample E

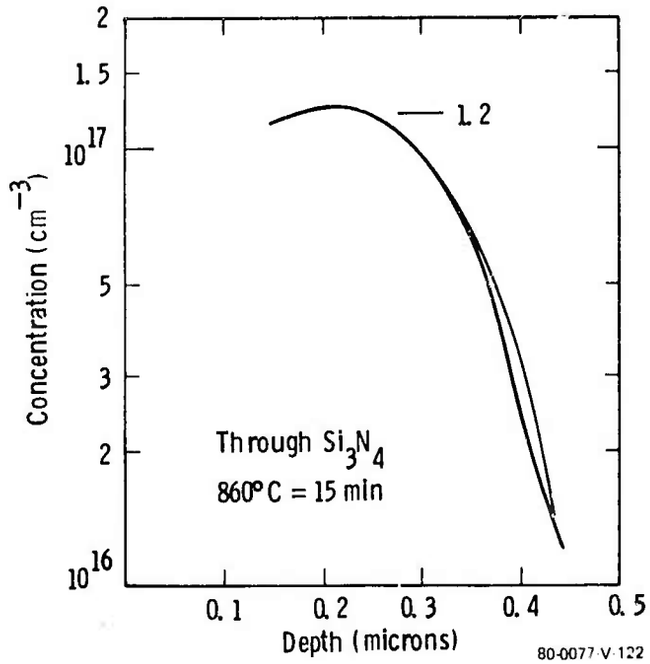


Figure E-25. $^{29}Si^{+}$ = 5.5 x 10^{12} at 325kV Plus 2 x 10^{12} at 125kV in Undoped PBN-Grown GaAs Sample F

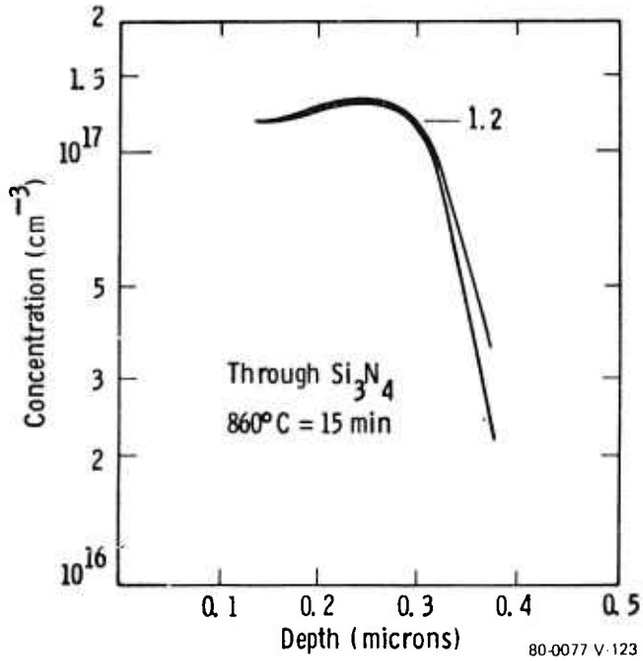


Figure E-26. $^{29}Si^{+}$ - 7 x 10^{12} at 350kV, 3 x 10^{12} at 125kV in Cr-Doped LEC GaAs Sample C

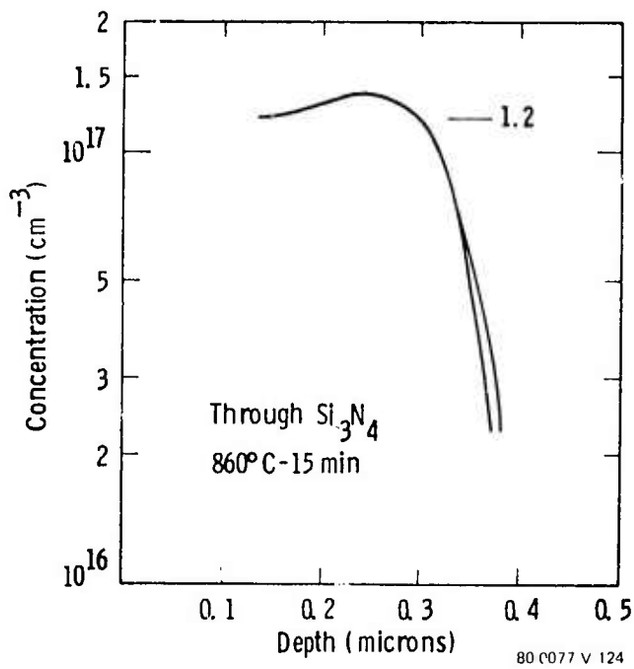


Figure E-27. $^{29}Si^{+}$ - 7 x 10^{12} at 350kV 3 x 10^{12} at 125kV in Cr-Doped LEC GaAs Sample B

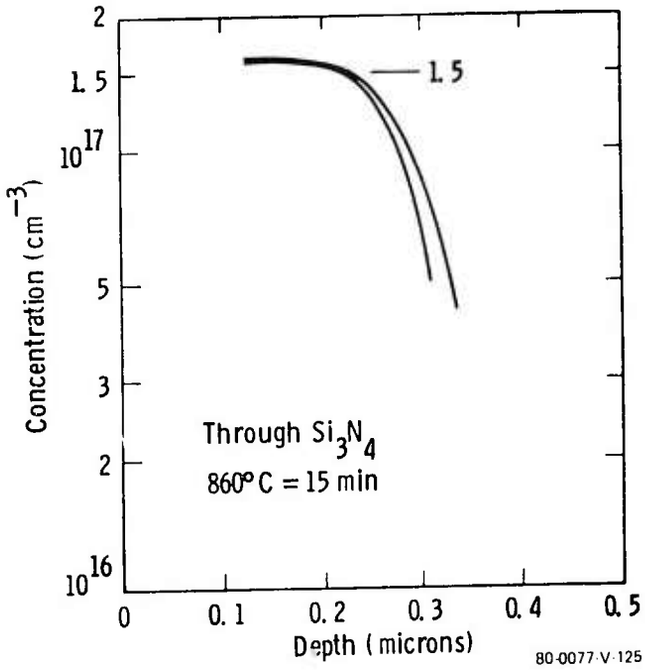


Figure E-28. $^{29}Si^{+}$ - 7 x 10^{12} at 300kV 3 x 10^{12} at 125kV in Cr-Doped LEC GaAs Sample D

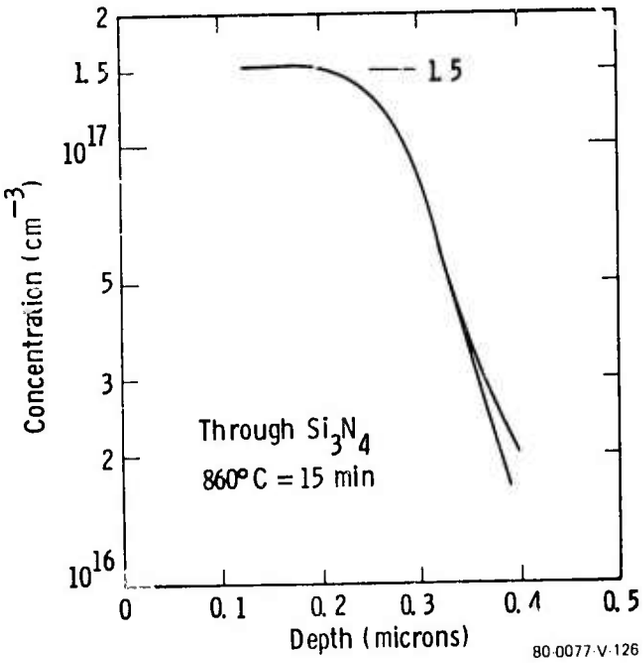


Figure E-29. $^{29}Si^{+}$ - 7 x 10^{12} at 300kV 3 x 10^{12} at 125kV in Cr-Doped LEC GaAs Sample G

The E-28-29 pair do exhibit significant differences at the deep edge of the channel; this is characteristic of high-concentration profiles in Cr-doped material. It is significant to note that figures E-23 through E-29 were obtained from uniform implant pads embedded in selectively-implanted wafers slated for one device fabrication run. Figures E-23 to E-29 show all of the wafers initiated for that run and all of the wafers were delivered.

Figure E-30 shows the saturated source-drain current of those samples prior to gate recess as a function of active concentration measured by Hall effect on equivalent uniform-implant specimens. A data block corresponds to an old run into a low-quality boat-grown boule whose activation efficiency was too low to permit gate recess. This shows that the saturated current is linearly related to N_s by a saturation velocity of 1.20 - 1.25 x 10^7 cm/sec independent of material quality and low field mobility. The variation in saturated current or in N_s should not be taken as a measure of reproducibility since the variations were planned to compensate for charge removal differences expected during gate recess due to concentration differences in the three groups of samples. The spread in apparent saturation velocity of ± 2 percent is a valid indicator of the reproducibility that has been achieved.

E.8 n^+ SOURCE-DRAIN CONTACT IMPLANTS

Selective-ion implantation of n^+ source-and-drain pads may be an important technology for achieving low source resistance to increase gain and for reducing field crowding at the drain to increase the drain breakdown voltage.

Figure E-31 shows contours of concentration versus depth and lateral position of a selective n^+ implant embedded in an active-channel layer. The concentration versus depth is taken from experimental data for Si implants; the lateral distribution is calculated assuming that the lateral standard deviation of the n^+ implant is equal to the measured projected deviation. It is clear that this spreading will have a significant effect on the effective source-gate spacing. Any n^+ technology that leads to

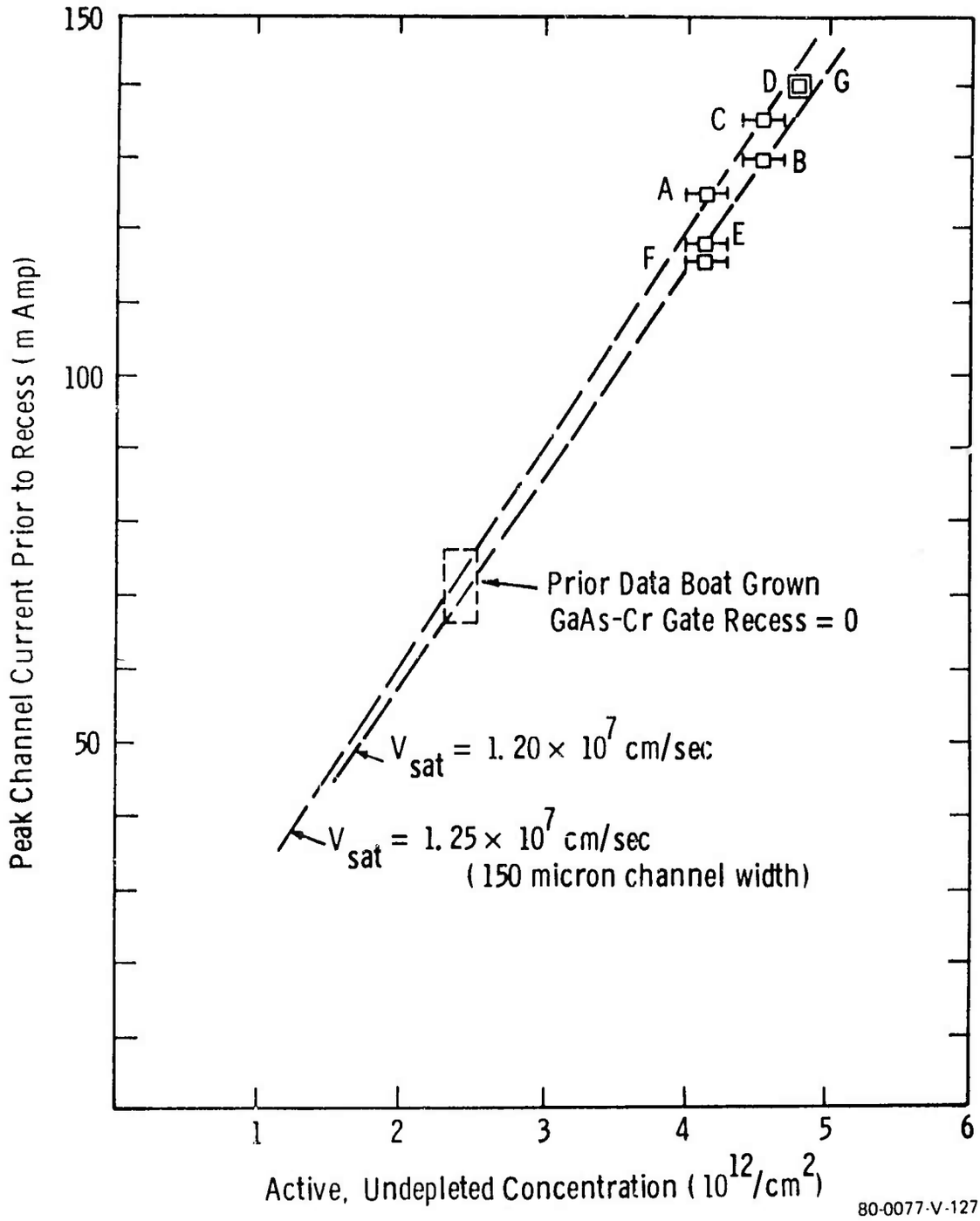


Figure E-30. Correlation of Active Concentration and I_{DSS} Prior to Gate Recess. (Letter Designations Refer to Samples Shown in Figures E-23 through E-29.)

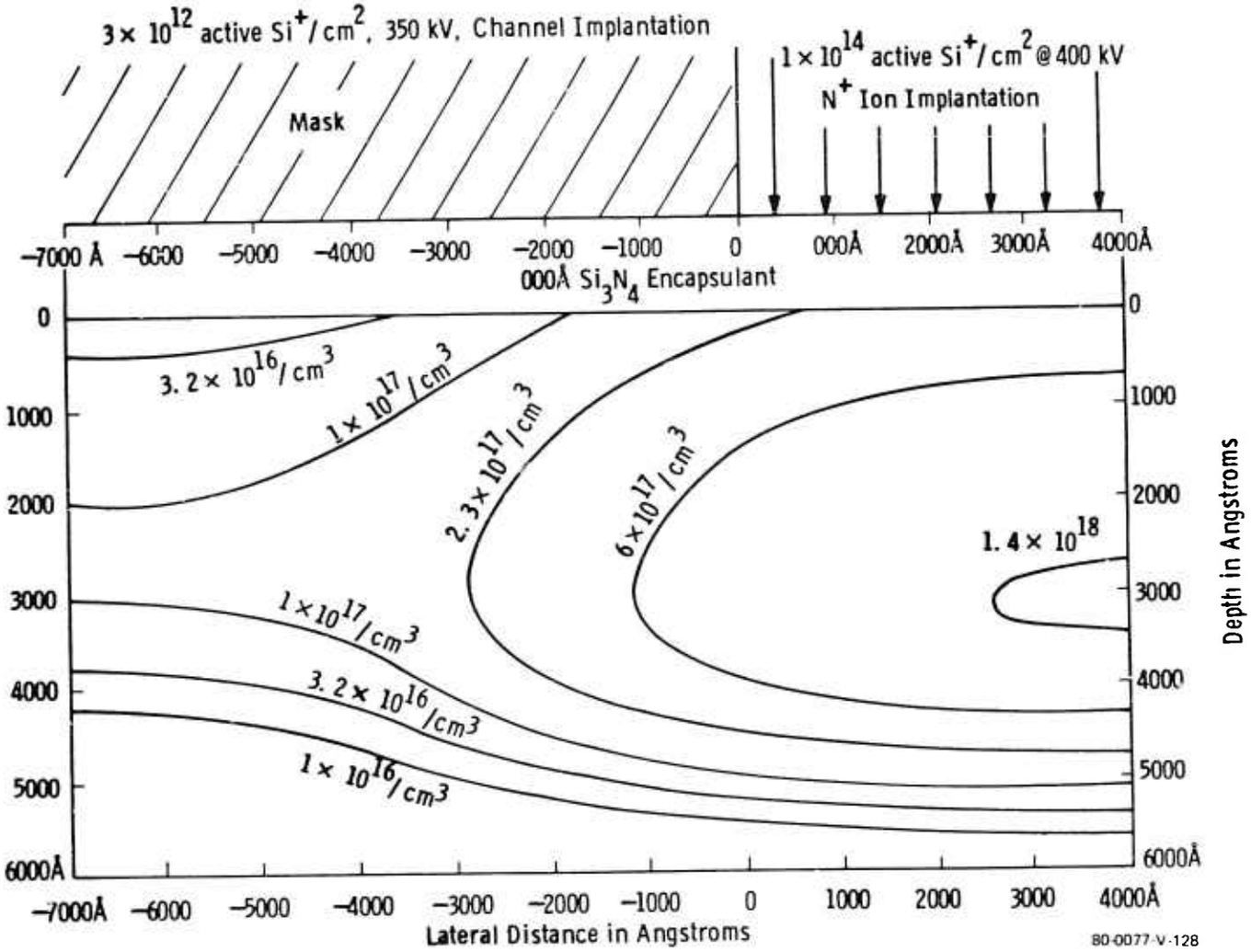


Figure E-31. Concentration Profile Section for As Selective n^+ Implant in an Active Channel

significant, uncontrolled indiffusion will also lead to uncontrolled lateral diffusion and either gatesource shorting or erratic characteristics. The concentration profile shown in figure E-31 appears to be ideal with regard to avoiding field crowding at the corner of the drain metallization; the surface concentration is not particularly high, but $R_C = 1 \times 10^{-7}\ \Omega\text{-cm}^2$ specific contact resistances have been achieved at this concentration.

Activation of n^+ layers achieved by ambient-temperature Si implants is not a well-controlled process in Cr-doped ingots. (The behavior of these n^+ implants in undoped ingots has not been examined to date.) Figure E-32 shows the activation efficiency, sheet-carrier concentration, and mobility as a function of Si dose for bare 260kV implants in a Cr-doped LEC ingot. The activation efficiency is a constant at low dose (after correcting for surface depletion), and the mobility drops normally with concentration. In this particular case, the active concentration saturates at a relatively low concentration of $4.4 \times 10^{13}/\text{cm}^2$ at a dose of $7.5 \times 10^{13}/\text{cm}^2$. In other ingots, such as the boat-grown ingot shown in figure E-33, the activation may start to degrade at lower doses while the active concentration continues to increase through doses of $10^{15}/\text{cm}^2$. Profile studies indicate that the increased activity beyond doses of $2 \times 10^{14}/\text{cm}^2$ is due to profile broadening rather than improved concentration/cm^3.

Saturation of the activate concentration is associated with the onset of amphoteric doping of the implanted Si followed net differential formation of acceptors. This is shown more clearly in figure E-34 which plots mobility versus peak concentration for the samples shown in figure E-32. At intermediate doses, the data follow a locus-of-constant-compensation ratio ($N_D + N_A/n \approx 1.4$) indicating that the acceptor concentration is proportional to the dose. At lower doses, the data follows a locus-of-constant-background acceptor density, as mentioned. At the upper end of the dose range, the primary effect of additional implanted Si is to degrade the compensation ratio ($N_D + N_A/n - 2.7$). The details of this degradation are erratic.

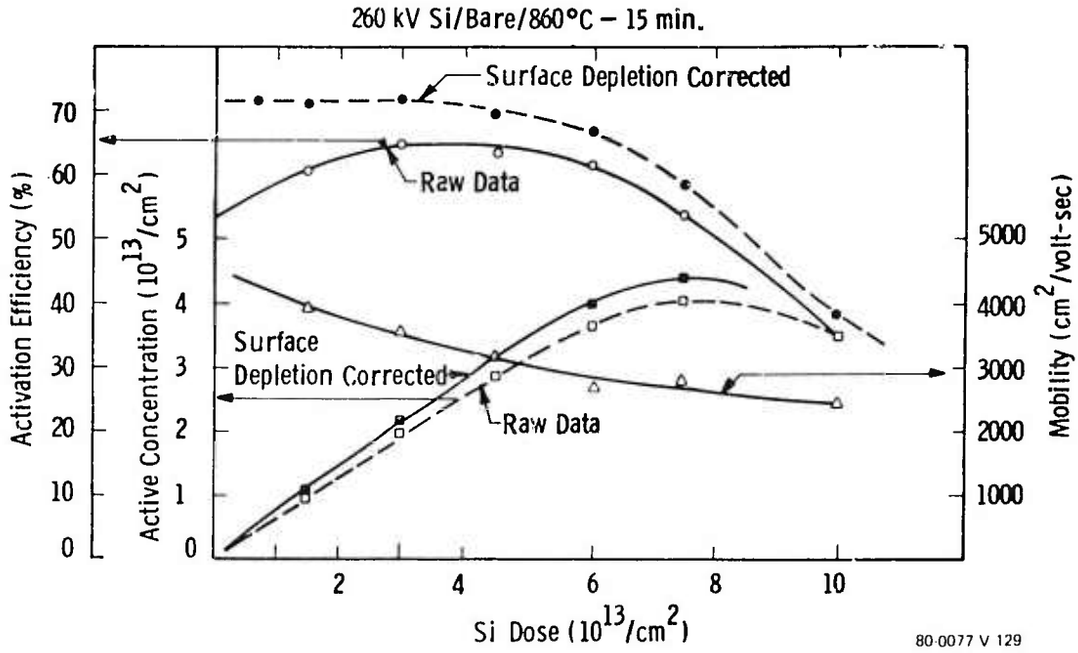


Figure E-32. Van Der Pauw Data for Intermediate Dose n^+ Implants Into Cr-Doped, LEC GaAs

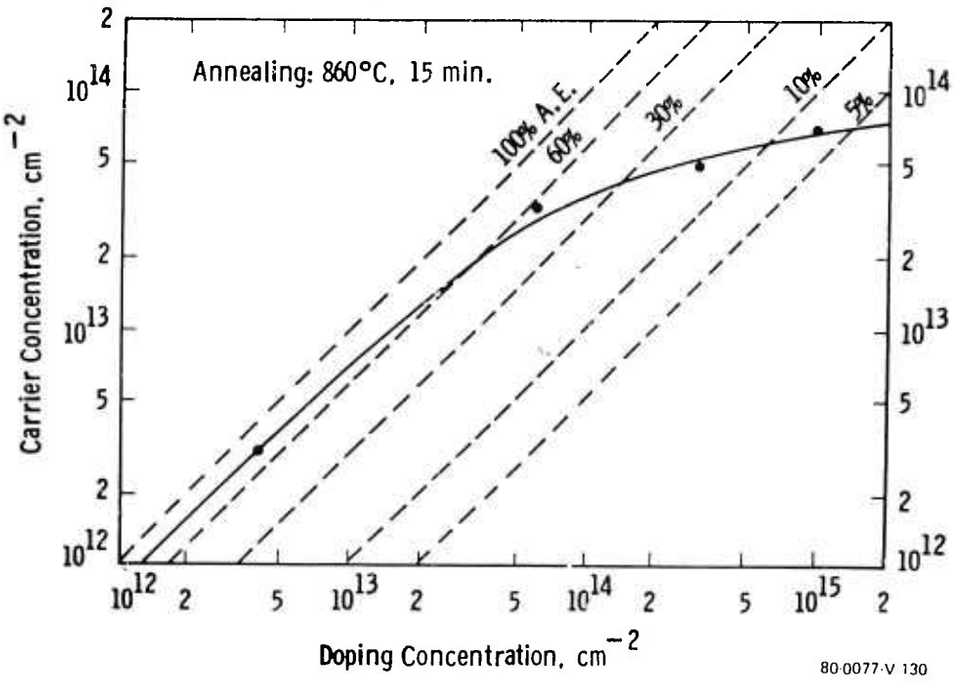


Figure E-33. Activation of Si n+ Implants Into Cr-Doped, Boat-Grown GaAs

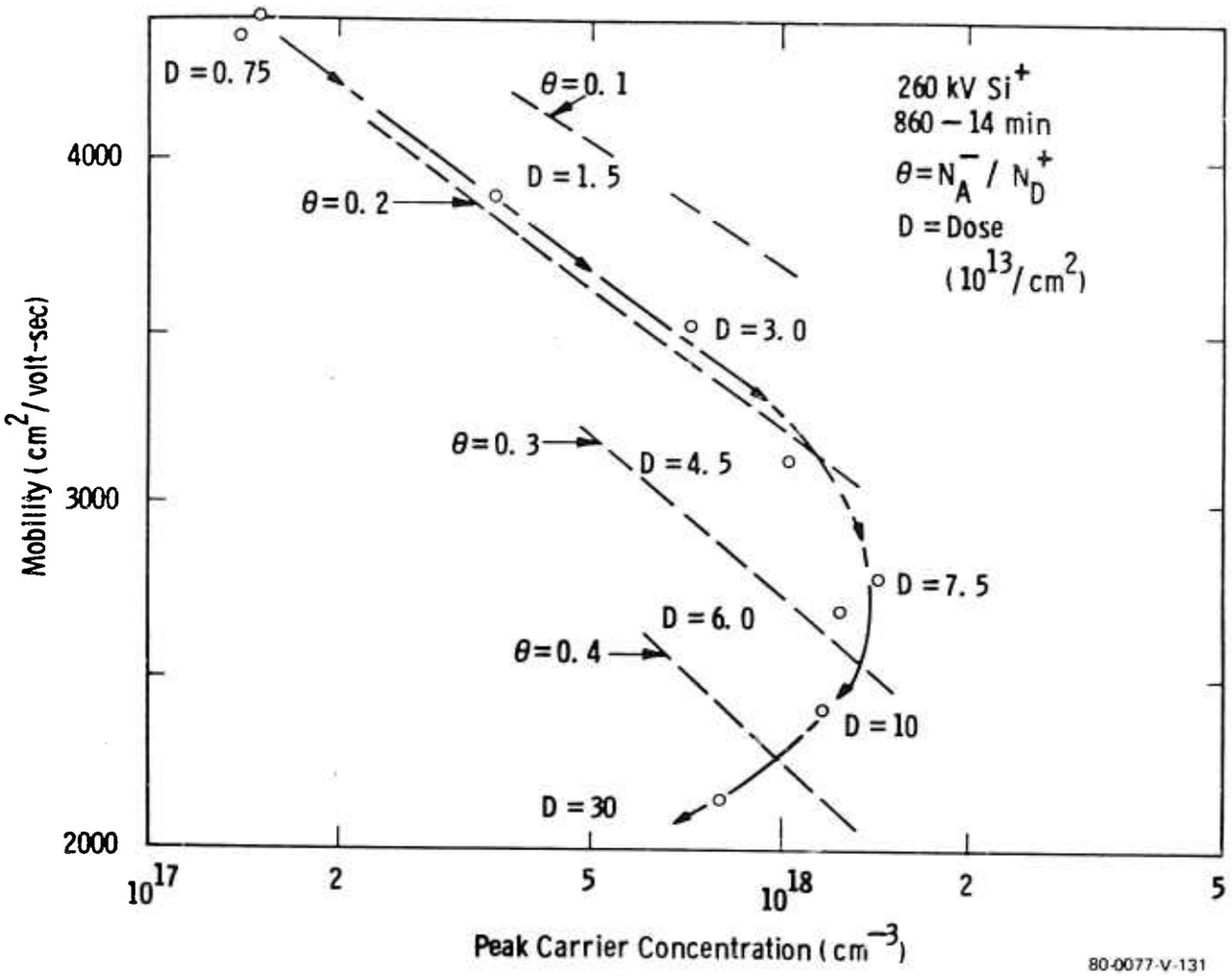


Figure E-34. Mobility vs Concentration for n+ Implants Showing Compensation Ratio Dependence on Dose

One technique for achieving lower resistance n^+ layers is to employ the higher doses but to anneal at higher temperatures to achieve better donor activation. Figure E-35 demonstrates that 40 Ω/□ layers can be achieved at 3×10^{14} Si/cm^2 and 1000°C anneals. This technique is unattractive both because it is not compatible with the standard channel anneal and because it leads to severe indiffusion. Figure E-35 also shows data achieved using a coimplant of Si and S with 860°C. This approach is based on the concept that providing a donor to occupy vanancies on the As sublattice will force more of the Si onto the Ga sublattice. Figure E-36 shows capacitance-etch profiles of S, Si, and Si plus S n^+ implants. The deep tail of the coimplant can be attributed to the characteristic indiffusion of the sulfur. The presence of the sulfur doubles the activation efficiency of the implanted Si and the mobility improves as a result of the improved compensation ratio. The results of a study of the cooperative effects of coimplantation in Cr-doped LEC GaAs is shown in figure E-37 where the sheet resistance and mobility are indicated at the 300kV S and

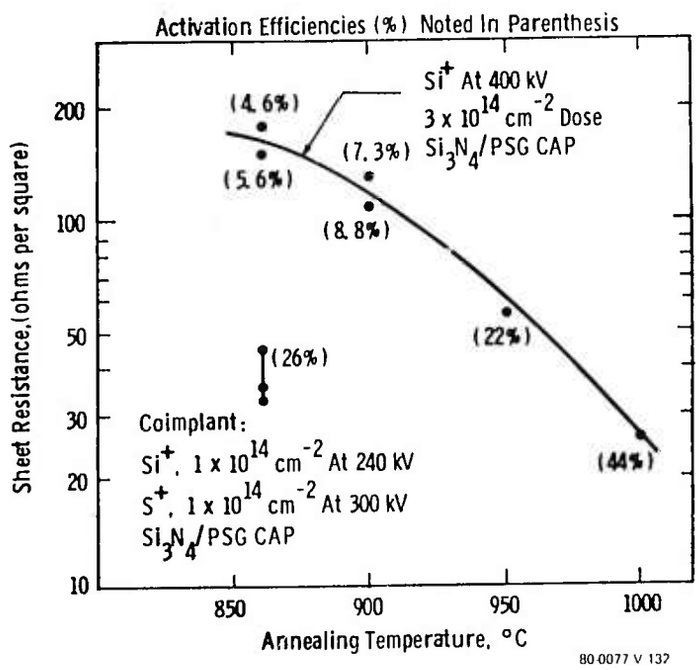


Figure E-35. Effect of Annealing Temperature on Sheet Resistance of n^+ Implants in Si GaAs

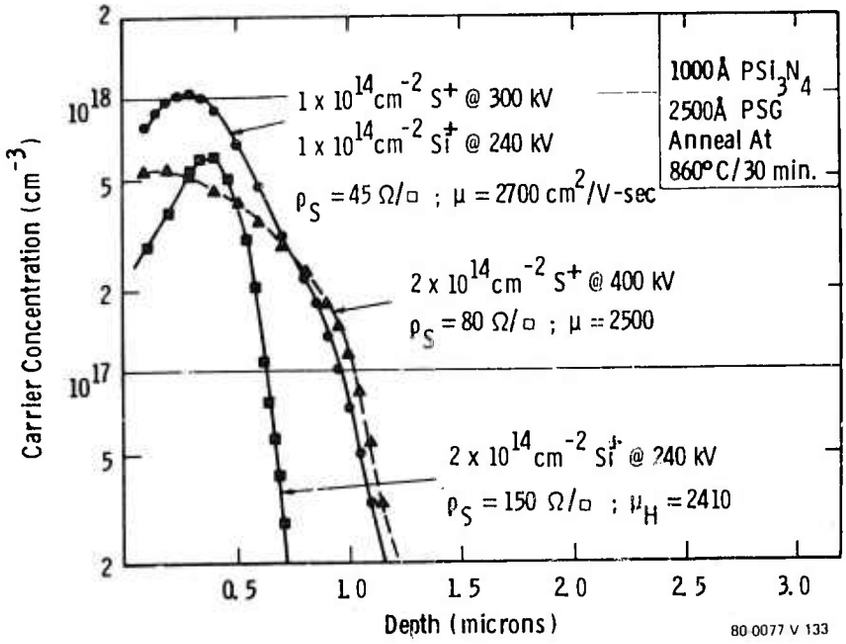


Figure E-36. Comparison of Si, S, and Si + S n^+ Implants

and 260-kV Si doses used. This shows that at a constant total dose, the best mobilities are achieved when both Si and S implantation are employed and that a satisfactory n^+ layer can be achieved at a Si dose of $4.5 \times 10^{13}/cm^2$ and S dose of $3 \times 10^{12}/cm^2$.

The role of S diffusion in these coimplants is complex. It appears that if the S concentration is excessive, a profile tail reminescent of S indiffusion is observed; if the S concentration is in "proper" proportion to the Si concentration, the tail is absent and the activation efficiency and mobility are improved dramatically.

It can be concluded that Si plus S coimplantation can be used to achieve effective n^+ layers through ambient-temperature implantation.

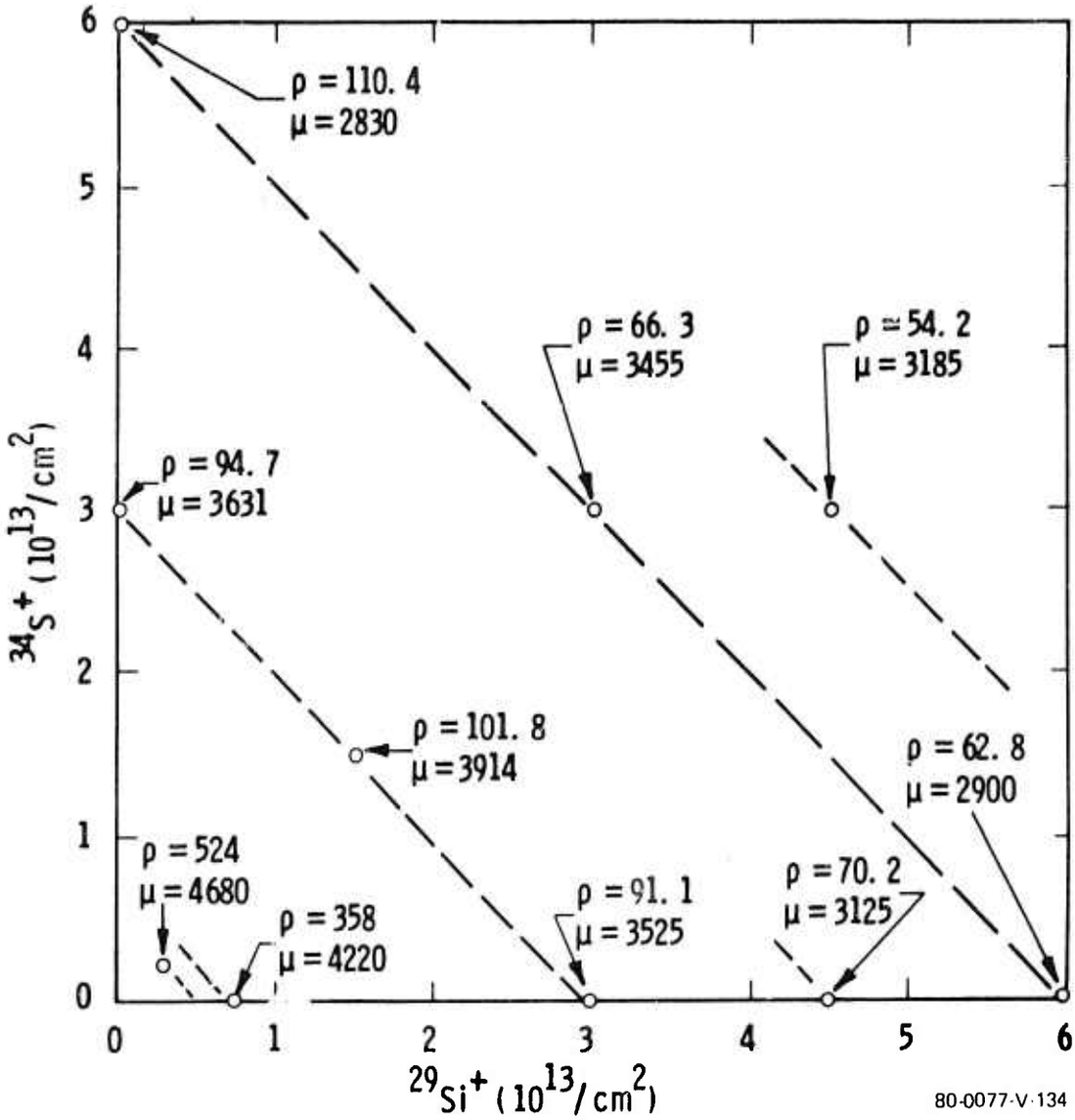


Figure E-37. Sheet Resistance - Mobility Characteristics of Si-S Coimplantation

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