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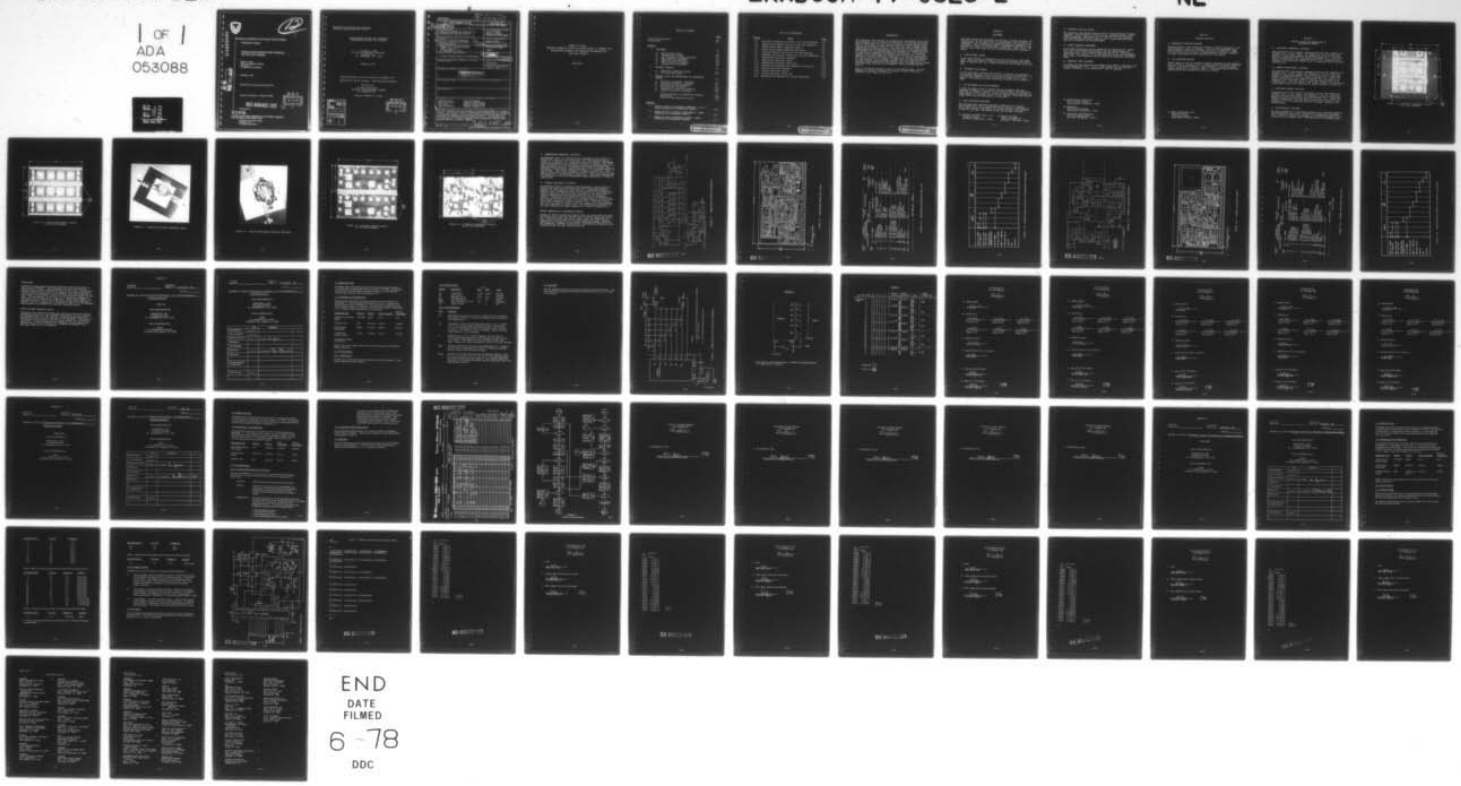

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Manufacturing Methods & Technology Technical Report

ERADCOM-77-0526-2

# MANUFACTURING METHODS AND TECHNOLOGY FOR TAPE CHIP CARRIER

Stanton R. Jones
William R. Rodrigues de Miranda
Honeywell Inc.
St. Petersburg, Florida 33733

FEBRUARY 1978

Quarterly Report for Period Ending 31 December 1977

(Approved for Public Release – Distribution Unlimited)

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**ECOM**

US ARMY ELECTRONICS RESEARCH & DEVELOPMENT COMMAND
FORT MONMOUTH, NEW JERSEY 07703

CONTRACT NO. DAAB07-77-C-0526
HONEYWELL INC.
St. Petersburg, Florida 33733

Manufacturing Methods and Technology
Technical Report ERADCOM-77-0526-2

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Prepared for

US Army Electronics
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Ft. Monmouth, NJ

Contract #DAAB07-77-C-0526

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| | |
|---|---|
| Tape Chip Carrier | Outer Lead Bonding |
| Hybrid Microcircuit | Automatic Feed Mechanism |
| Film Carrier | Material Handling System |
| Inner Lead Bonding | Automatic Assembly Line |

20. ABSTRACT (CONTINUE ON REVERSE SIDE IF NECESSARY AND IDENTIFY BY BLOCK NUMBER)

This report describes the work performed during the second quarter of a 26 month contract. The contract is aimed at establishing and demonstrating the feasibility of an automated assembly line for hybrid microcircuits using tape chip carrier technology for semiconductor devices whenever practical. The automated line will also make use of automatic substrate handling equipment to move partially assembled devices in and out of magazines.

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QUARTERLY TECHNICAL REPORT FOR PERIOD ENDING 31 DECEMBER 1977

MANUFACTURING METHODS AND TECHNOLOGY ENGINEERING FOR

TAPE CHIP CARRIER

CDRL C-002

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# INTRODUCTION

The purpose of this program is to demonstrate the concept of an automated assembly line for hybrid microcircuits, through the establishment of techniques for tape carrier mounting of semiconductor chips, burn-in and testing of these chips on tape and their placement into representative hybrid circuits. The tape Chip Carrier (TCC) system permits mounting of semiconductor chips on reels of sprocketed film. The system is an established means of automating the interconnection of individually packaged semiconductor chip devices. It has been adapted to the fabrication of hybrid microcircuits used in the manufacture of certain commercial computers. Its overall adaptation to the hybrid microcircuit industry is expected to be greatly enhanced by this program. The automated assembly line will make use of an automatic feed mechanism at each process step, and magazines to transport substrates and partially assembled circuits between process points.

This is the second quarterly report on the MM&T program. At this important milestone, Honeywell is pleased to report excellent progress in all areas of activity.



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## SECTION 1

## EQUIPMENT

This task covers the evaluation of existing, in-house equipment for possible use for the MM&T tasks to be performed, and the review of requirements and preparation of specifications for equipment to be purchased. Each of the major pieces of equipment required for the program are listed on the PERT Chart (CDRL-A001, August 1977). Updates in this area since the last reporting period are discussed below.

### A. REEL-TO-REEL PLATER

It has been decided to subcontract the gold plating of lead frame tape. There are several vendors who have the equipment and experience to perform this job. Vendor selection will be made later this year.

### B. AUTOMATIC WIRE BONDER

A visit was made to Kulicke and Soffa[1] to discuss the automatic wire bonding equipment which will be dedicated to the ECOM line. We are currently awaiting a quote from K&S on a Model 1415-3 wire bonder. An automatic pattern recognition feature will be added in 1979.

### C. DIE PLACEMENT AND EPOXY DISPENSER

A visit was made to K&S to discuss the die placement and epoxy dispenser equipment to be used on the ECOM program. Awaiting quote from K&S on a special machine, which features automatic placement of semiconductor or capacitor chips with an operator controlled pickoff stage, which can be autovated at a later date.

### D. TAPE INSPECTION EQUIPMENT

The in-house tape inspection equipment consisting of a manual spooler/despooler with a Bausch and Lomb[2] Sterio 7 microscope is still under review to determine if any modifications are required. If such is the case, the modifications will be made in-house.

(1) Kulicke and Soffa (K&S), Inc.
Prudential Road
Horsham, Pennsylvania 19044

(2) Bausch and Lomb
1400 N. Goiodman St.
Rochester, New York 14602

## E. CAPACITOR PICK AND PLACE

The automatic feed system concept design is approximately 60 percent complete. This system will utilize an air substrate handler feed/pickup mechanism. Substrates will be fed onto the belt transport from one magazine and then picked up into a second magazine after capacitor placement has been performed.

## F. WAFER INSPECTION EQUIPMENT

A new wafer inspection station (Mechanization Associates[3], Model 110), has been purchased by Honeywell for the Hybrid Receiving Inspection area. This station steps from die to die automatically and allows the inspector to ink rejected dice during the presettable dwell time. This inspection station should be operational by March 1978.

## G. AUTOMATIC TEST EQUIPMENT

A program has been generated for Random Access Memory (34030405) test on the Macrodata[4] 150. A static test program for the Minilaser Counter (34030411) on the Fairchild[5] 5000 is complete.

(3) Mechanization Associates
153 E. Evelyn Avenue
Mountainview, California 94041

(4) Macrodata
20440 Corisco Street
Chatsworth, California 91311

(5) Fairchild Instrumentation
1725G Technology Road
San Jose, California 95070

## SECTION 2

## MATERIAL HANDLING

### A. MECHANICAL SUBSTRATE HANDLER

Detailed design of the mechanical substrate handler described in the first quarterly report is complete. Build of an operational substrate handler to be used in conjunction with the Weltek[1] (Model 44) thick film screen printer is approximately 90 percent complete. A patent disclosure has been submitted for this design.

### B. AIR SUBSTRATE HANDLER

Detail design of the air substrate handler described in the quarterly report ending 30 September 1977 is approximately 95 percent complete. Build of a working prototype is approximately 50 percent complete (target completion is February 1978). A patent disclosure has been submitted for the proposed air substrate handler.

(1) Wells Electronics Inc.
Weltek Division
1701 Main Street
South Bend, Indiana 46613

## SECTION 3

## DESIGN, LAYOUT AND MANUFACTURE OF ENGINEERING SAMPLES

### A. ELECTRONIC COMMUTATOR (34030402)

Five electrically and visually acceptable devices were shipped on 27 December 1977. A test report (see Appendix A) for the first submission of engineering samples was prepared and sent to ECOM under Honeywell Letter RDC-K-601-115, dated 29 December 1977. Figure 3-1 shows a photograph of the assembled hybrids still attached in the standard 2 by 2 substrate format prior to conformal coat of the chip bonding areas.

### B. RANDOM ACCESS MEMORY (34030405)

Five electrically and visually acceptable devices were shipped on 30 December 1977. A test report (see Appendix B) for the first submission of engineering samples was prepared and sent to ECOM under Honeywell Letter RDC-K-601-117, dated 4 January 1978. Figure 3-2 shows a photograph of the assembled hybrids still attached in the standard 2 by 2 substrate prior to conformal coating of the chip bonding areas. The test fixture used to make contact with the hybrid input/output pads on the substrate is shown in Figure 3-3 and 3-4.

### C. MINILASER COUNTER (34030411)

Five electrically and visually acceptable devices were shipped 29 December 1977. A test report (see Appendix C) for the first submission of engineering samples was prepared and sent to ECOM under Honeywell Letter RDC-K-601116, dated 30 December 1977. Figure 3-5 shows a photograph of the assembled hybrids still attached in the standard 2 by 2 inch substrate prior to conformal coating of the bonding areas.

### D. DISCRIMINATOR (34030408)

The first submission of engineering samples have completed assembly and preconformal coat tests. Delivery is scheduled for February 1978. Figure 3-6 shows a photograph of the assembled hybrids still attached in the standard 2 by 2 substrate prior to conformal coat.

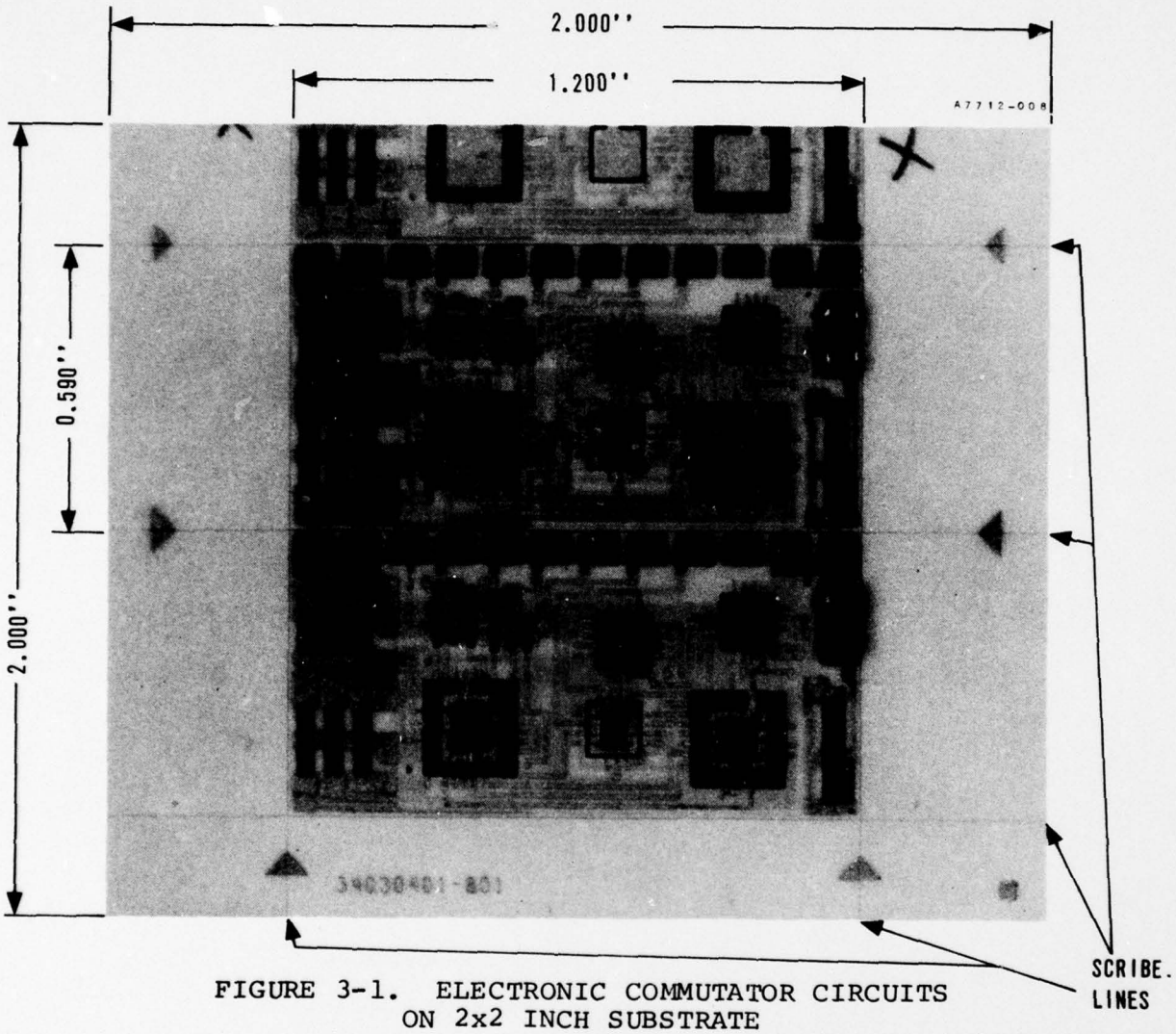


FIGURE 3-1. ELECTRONIC COMMUTATOR CIRCUITS ON 2x2 INCH SUBSTRATE

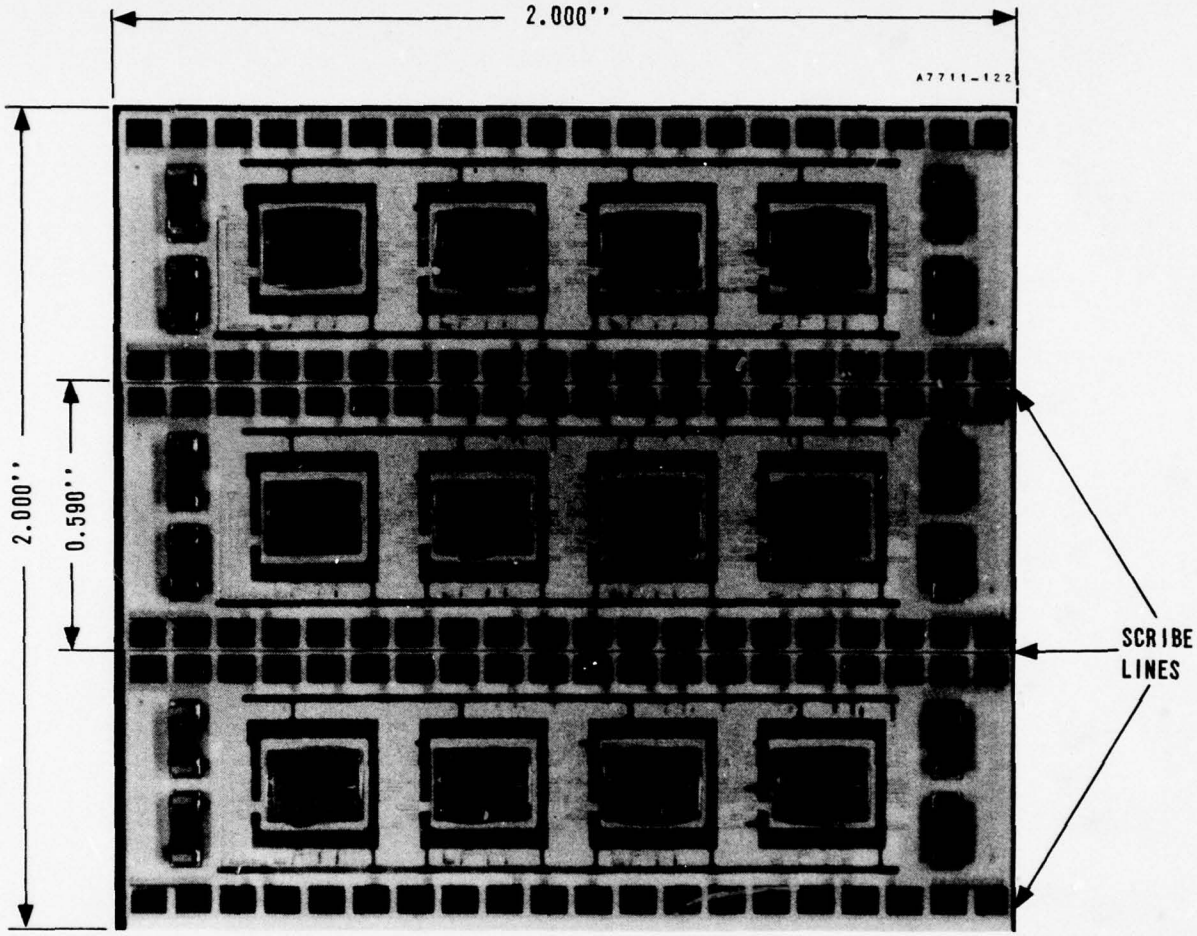


FIGURE 3-2. RANDOM ACCESS MEMORY CIRCUITS
ON 2x2 INCH SUBSTRATE

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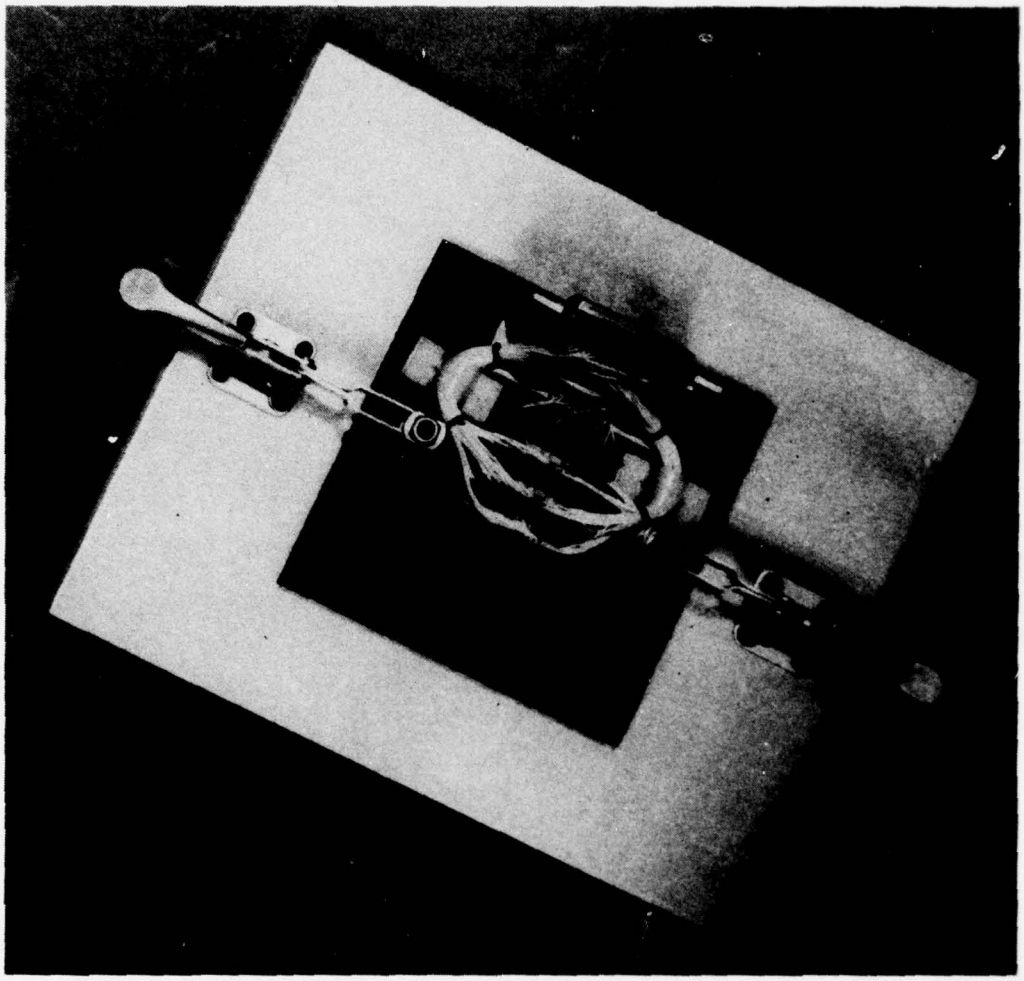

FIGURE 3-3. RANDOM ACCESS MEMORY SUBSTRATE PROBER

C7801-18

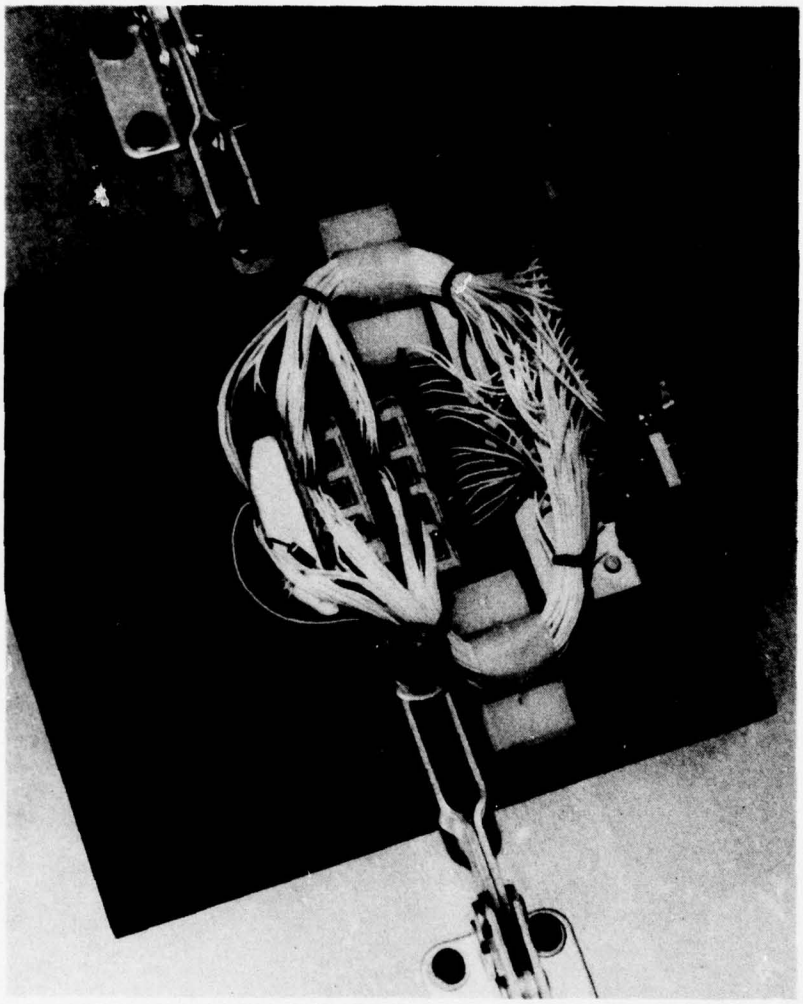

FIGURE 3-4. RANDOM ACCESS MEMORY SUBSTRATE TEST HEAD

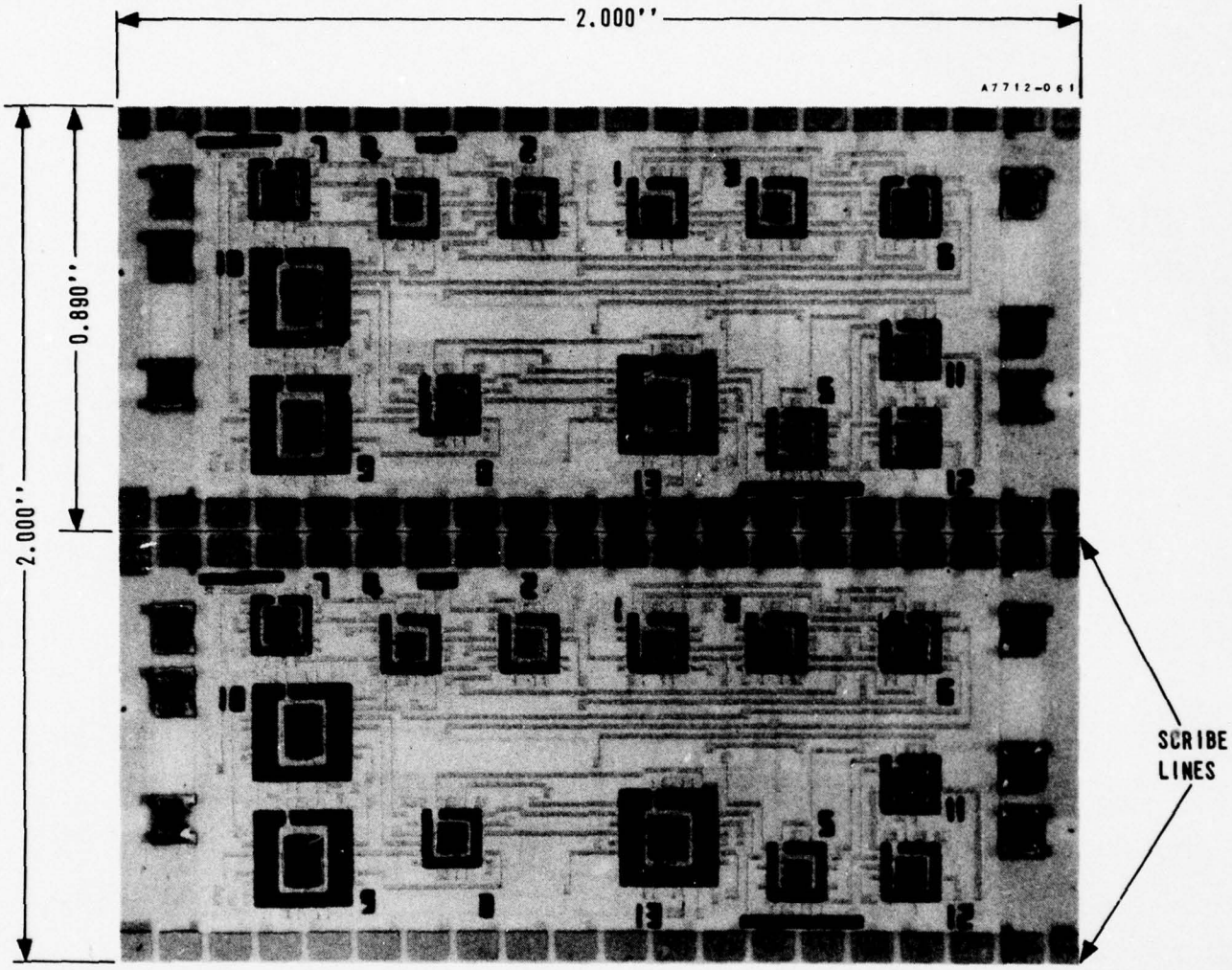


FIGURE 3-5. MINILASER COUNTER CIRCUITS
ON 2x2 INCH SUBSTRATE

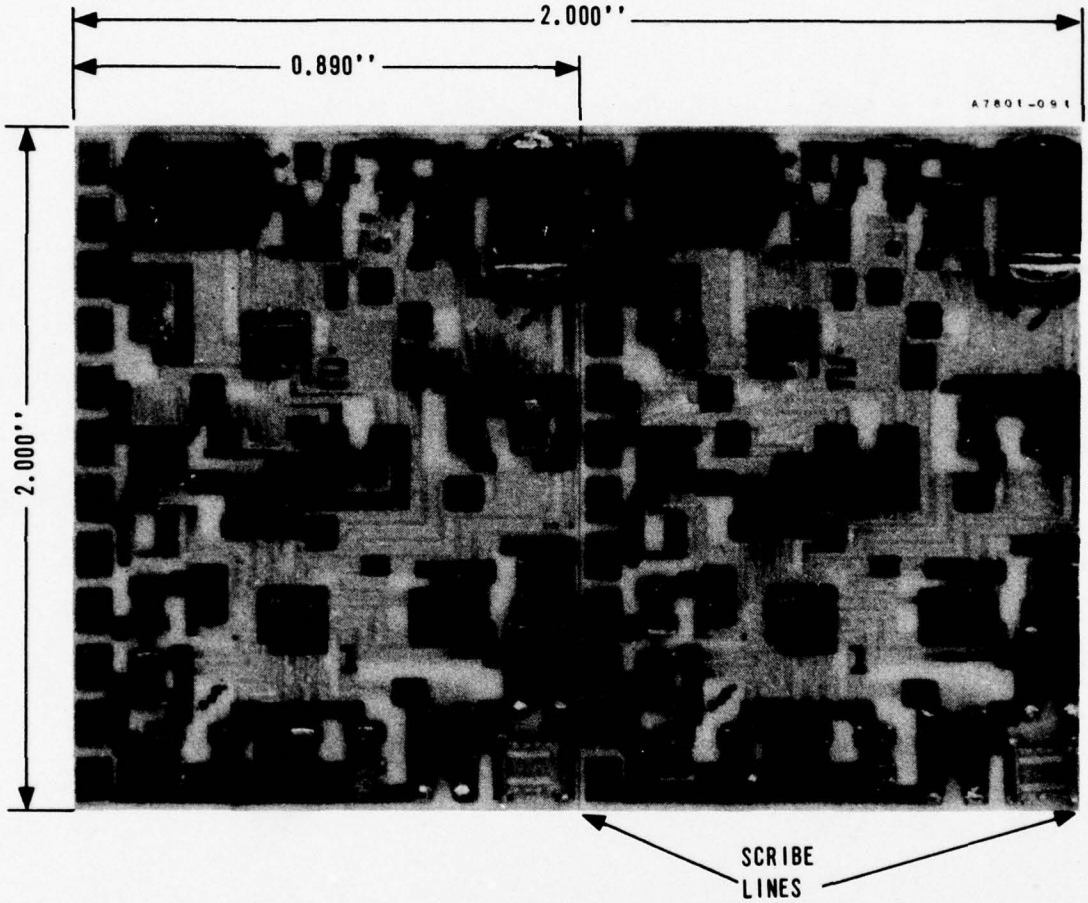


FIGURE 3-6. SINCGARS DISCRIMINATOR CIRCUITS ON 2x2 INCH SUBSTRATE

## E. TEMPERATURE CONTROLLER (34030415)

Considerable effort is presently being expended on this circuit to develop the final test and functional trim fixturing/procedures. Design is in process for a functional-trim test fixture. Breadboard tests and evaluations are scheduled to begin in February 1978, along with the design of a circuit probing fixture and associated test box/interfacing cabling. Discussions with ECOM will be held later to determine if this circuit can be delivered in its intended package or form factor. The circuit schematic is shown in Figure 3-7. The hybrid layout which will be used for build is shown in Figure 3-8 and the parts list is illustrated in Figure 3-9. The current manufacturing schedule for the first engineering sample submission is shown in Figure 3-10.

## F. CRYSTAL OSCILLATOR (34030418)

Considerable effort is presently being expended on this circuit to develop the final test and functional trim fixturing/procedures. Design of a functional-trim test fixture is scheduled to begin in February 1978. Breadboard tests and evaluation is also scheduled to begin in February, along with the initiation of the design for a circuit probing fixture and associated test box and interface cabling. Discussions with ECOM will be held later to determine if this circuit can be delivered in its intended package or form factor. The circuit schematic is shown in Figure 3-11. The hybrid layout which will be used for build is shown in Figure 3-12, and the parts list is illustrated in Figure 3-13. The manufacturing schedule for the first engineering sample submission is shown in Figure 3-14.

## SECOND SUBMISSION OF ENGINEERING SAMPLES

During the second engineering sample build, all chips which use the 5 millimeter outer lead bond tooling will be TAB'ed, where ever possible. Purchase orders for wafers, masks, tape, and thermodes for these chips will be placed in the next reporting period. Detailed manufacturing schedules for the second engineering sample build for the Commutator, SINCGARS Discriminator, and Minilaser Counter will be prepared during the next reporting period.

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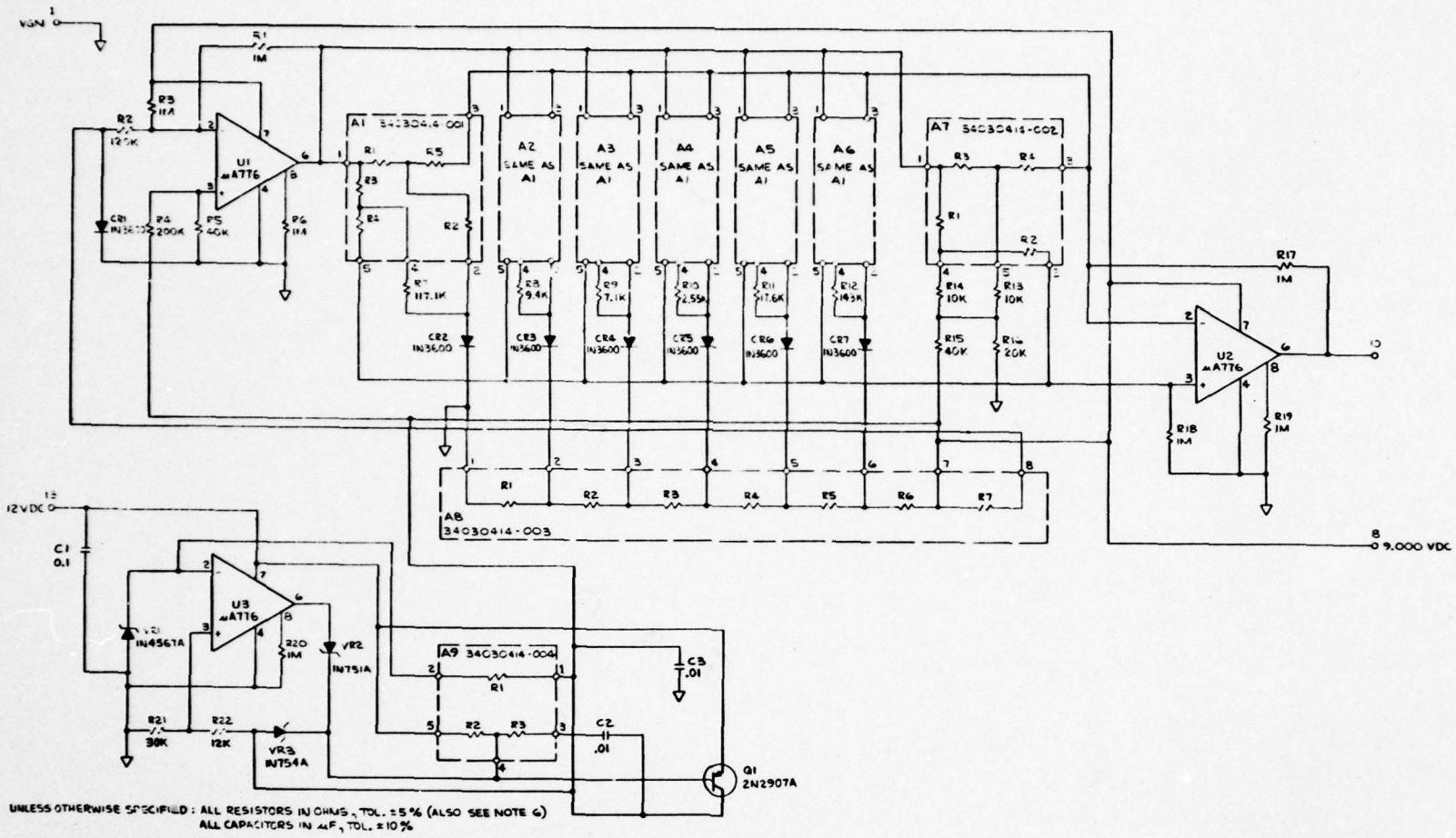


FIGURE 3-7. TEMPERATURE CONTROLLER SCHEMATIC

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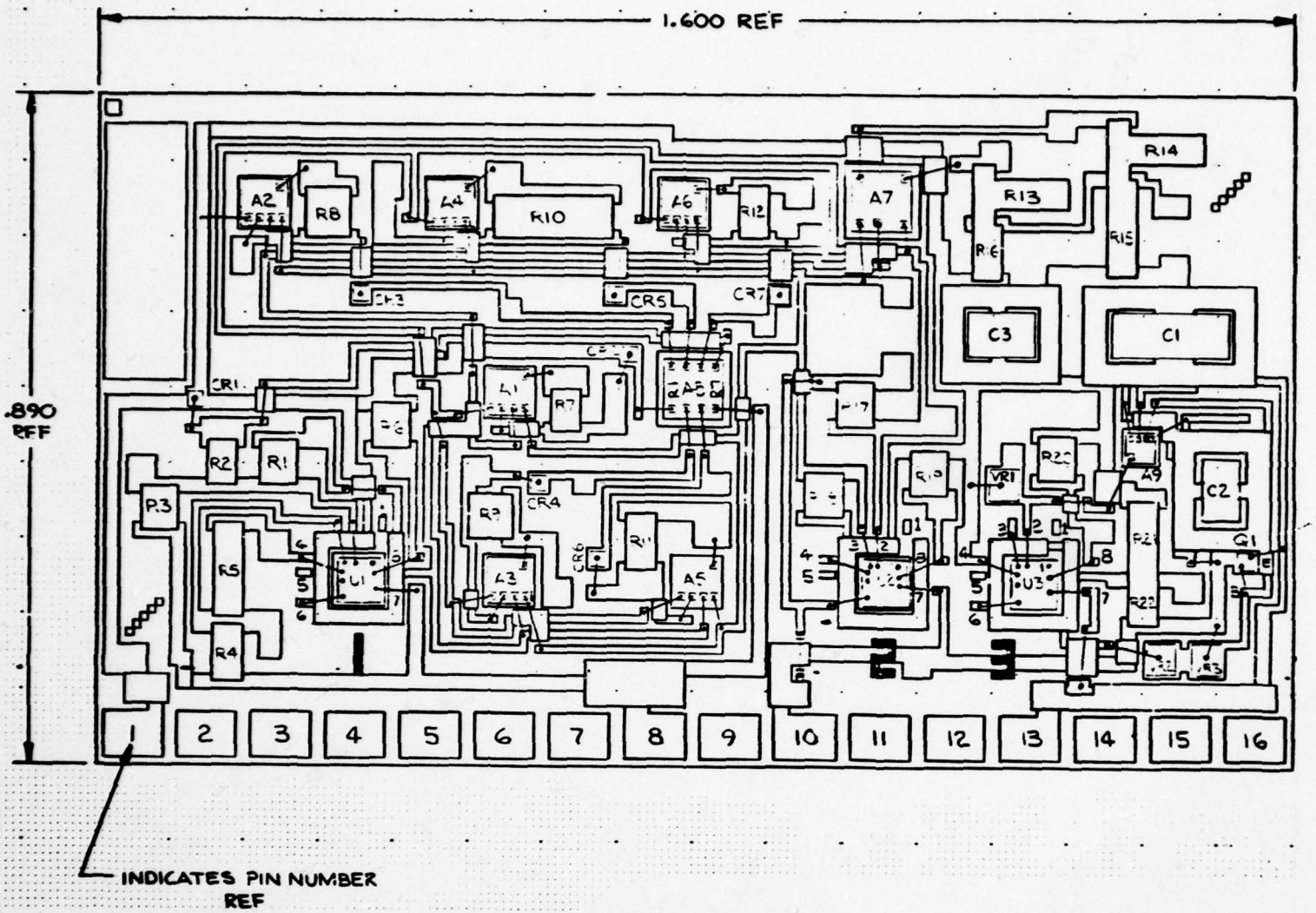


FIGURE 3-8. TEMPERATURE CONTROLLER LAYOUT

| PARTS LIST | HONEYWELL AVIONICS DIVISION ST. PETERSBURG FLORIDA | CODE IDENT 09128 | PL34030415-001 | REV A | DATE 12-22-77 |
|---|---|---|---|---|---|
| CONTRACT NUMBER | | LIST TITLE MM+T TEMP CONT.HYB ASSY | | REV AUTH NO. E0155531 | SHEET 1 |

| FIND NO | QTY | PART NUMBER | DESCRIPTION | REMARKS | CODE IDENT |
|---|---|---|---|---|---|
| | REF | 34030415 | MM+T TEMP CONT.HYB ASSY | MIN. REVISION - | |
| 1 | 1 | 34030413-001 | M.I.B.TEMP. CONTROLLER | | |
| 2 | 2 | 0805W5R103K50PS | .01 UF CAP | C2,C3, VICLAN | |
| 3 | 1 | 1505W5R104K25PS | CAP. 0.1UF, 25V | C1, VICLAN | |
| 4 | 7 | AU PAD 1N3600 | DIODE | CR1-CR7,FAIRCHILD | |
| 5 | 1 | 1NC751A | DIODE, ZENER | VR2, MOTOROLA | |
| 6 | 1 | 1NC754A | DIODE, ZENER | VR3, MOTOROLA | |
| 7 | 1 | AU PAD 1N4567A | DIODE,ZENER | VR1 COMPENSATED DEVICES | |
| 8 | 1 | AU PAD 2N2907A | TRANSISTOR | Q1 SEMICOA | |
| 9 | 6 | AU PAD 34030414-001 | RESISTOR ARRAY | A1-A6 | |
| 10 | 1 | AU PAD 34030414-002 | RESISTOR ARRAY | A7 | |
| 11 | 1 | AU PAD 34030414-003 | RESISTOR ARRAY | A8 | |
| 12 | 1 | AU PAD 34030414-004 | RESISTOR ARRAY | A9 | |
| 13 | 3 | T.A.B. UA776 | T.A.B. I.C. | U1,U2,U3 FAIRCHILD | |
| 14 | AR | FMS40616 | WIRE,BOND,GOLD | TYPE II,.001DIA,GOLD | |
| 15 | AR | FMS40599 | EL.COND.EPOXY ADH. | TY II,ABLEBOND 36-2 | |
| 16 | AR | DUPONT 8956 | SOLDER PASTE | 62-36-2 | |
| 17 | AR | R6100 | COAT,CONFORMAL | DOW CORNING | |
| 900 | REF | FPS18032 | MARKING | .09 REF HIGH CHAR. METH H5 AND/OR B2 | 09128 |
| 901 | REF | 34030416 | TEST | | |

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FIGURE 3-9. TEMPERATURE CONTROLLER PARTS LIST

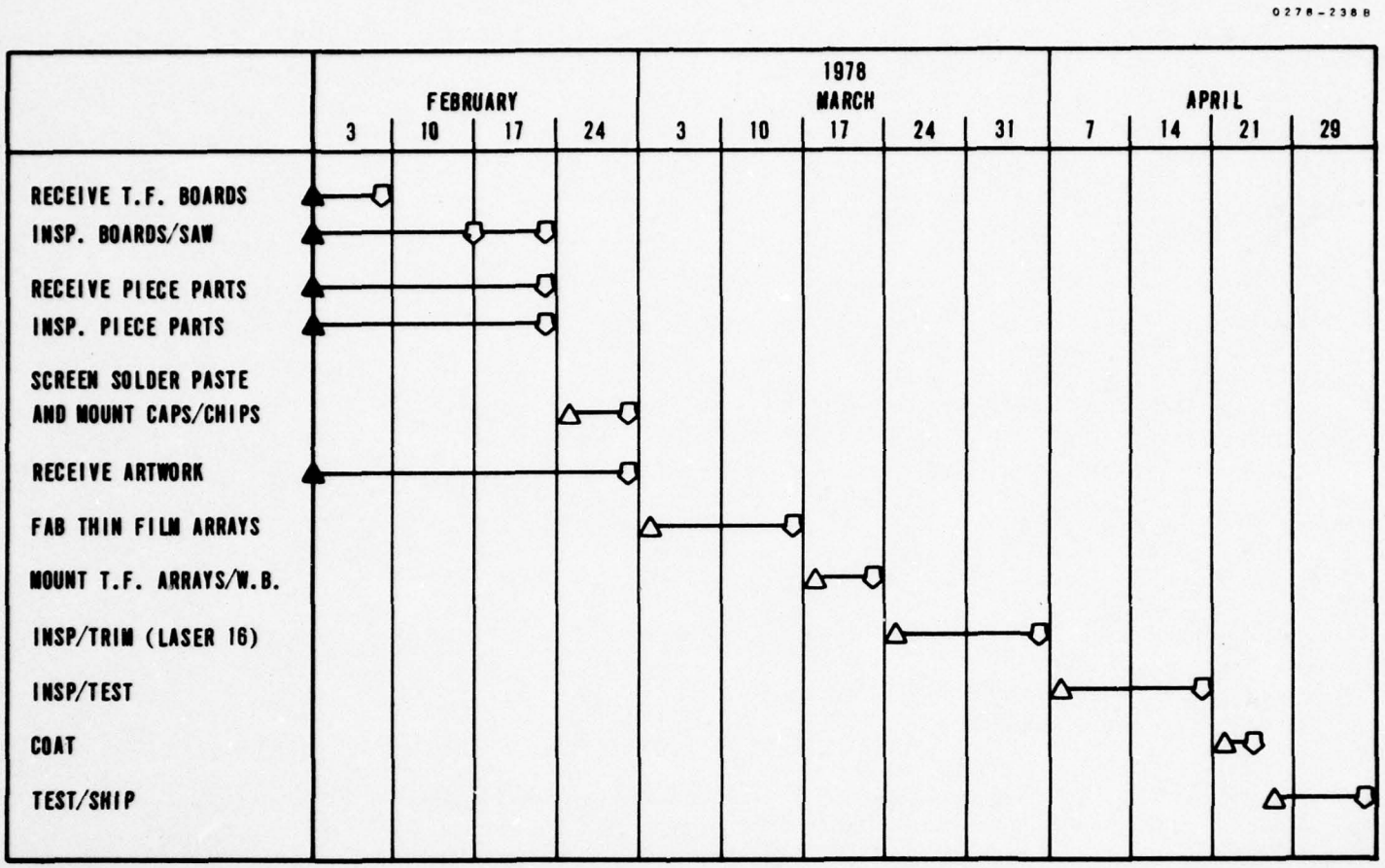


FIGURE 3-10. MANUFACTURING SCHEDULE FOR TEMPERATURE CONTROLLER

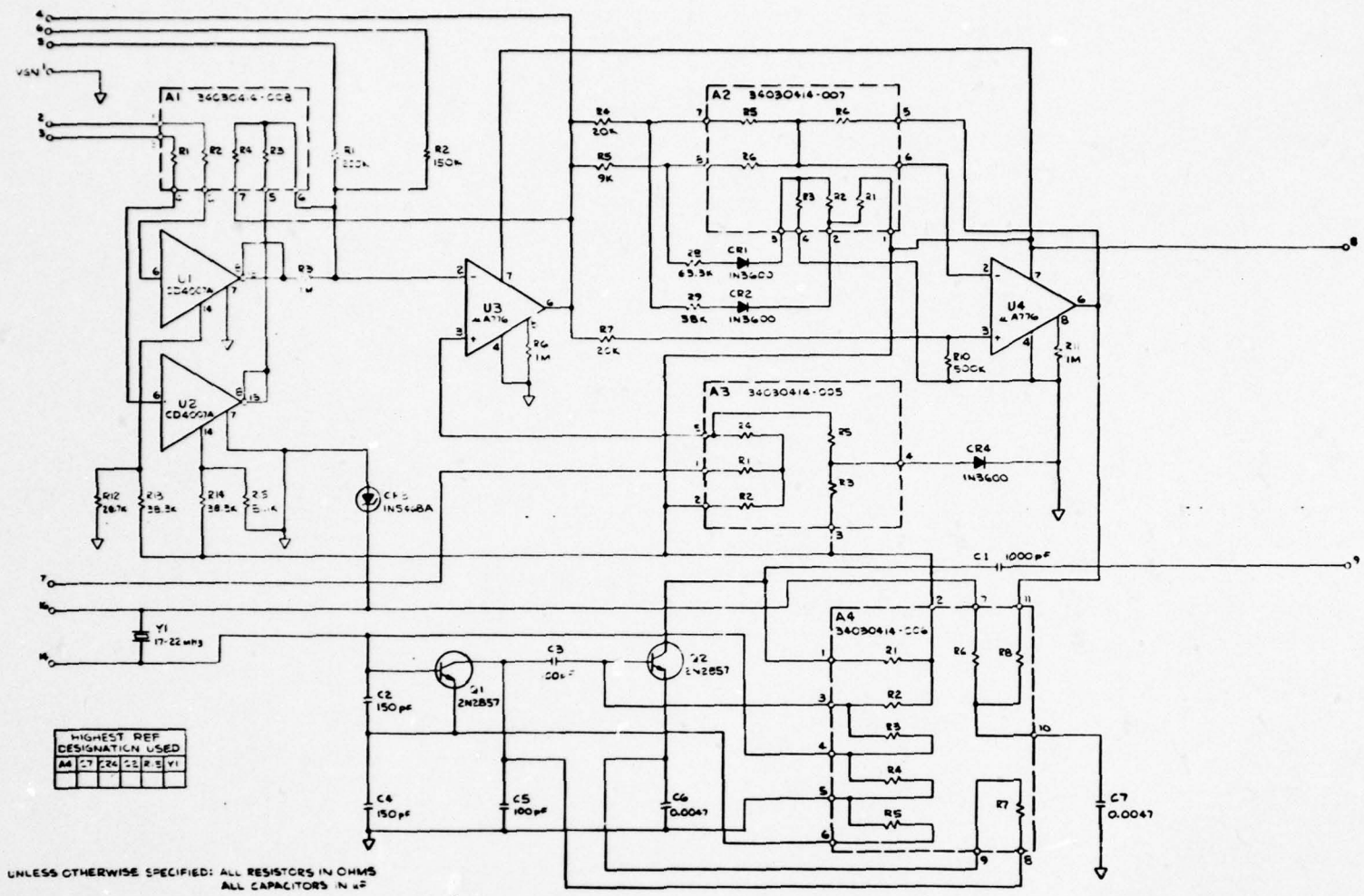


FIGURE 3-11. CRYSTAL OSCILLATOR SCHEMATIC

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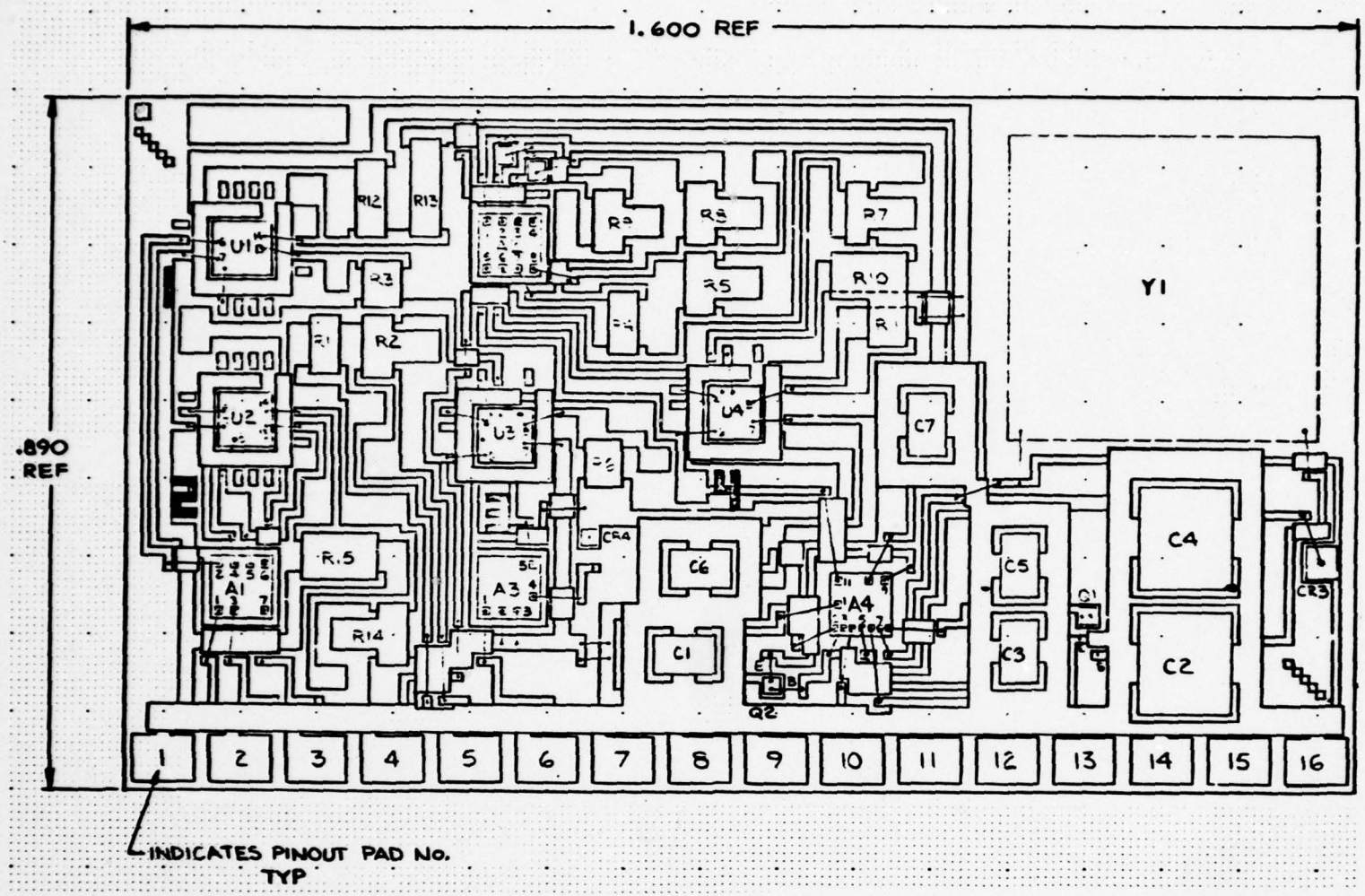


FIGURE 3-12. CRYSTAL OSCILLATOR LAYOUT

| PARTS LIST | HONEYWELL AVIONICS DIVISION ST. PETERSBURG FLORIDA | CODE IDENT 09128 | PL34030418-001 | REV - | DATE 12-22-77 |
|---|---|---|---|---|---|
| CONTRACT NUMBER | | LIST TITLE MM&T CRYSTAL OSCILLATOR | | REV AUTH NO. E0155533 | SHEET 1 |

| FIND NO | QTY | PART NUMBER | DESCRIPTION | REMARKS | CODE IDENT |
|---|---|---|---|---|---|
| 0 | REF | 34030418 | MM&T CRYSTAL OSCILLATOR | MIN. REVISION - | |
| 1 | 1 | 34030417-001 | M.I.B.CRYSTAL OSCILLATOR | | |
| 2 | 2 | ATC100B151KC300 | CAPACITOR | C2,C4 AM TECH CER | |
| 3 | 2 | 0805W5R102K25PS | CAPACITOR, 1000PF | C1,C3 VICLAN | |
| 4 | 1 | 0805C0G101F25PS | CAPACITOR, 100PF | C5 VICLAN | |
| 5 | 2 | 0805W5R472K25PS | CAPACITOR, .0047 UF | C6,C7 VICLAN | |
| 6 | 3 | AU PAD 1N3600 | DIODE | CR1,CR2,CR4 FAIRCHIL FAIRCHILD | |
| 7 | 1 | 1N5468A | DIODE | CR3 MOTOROLA | |
| 8 | 2 | AU PAD 2N918 | TRANSISTOR | Q1,Q2 FAIRCHILD | |
| 9 | 1 | AU PAD 34030414-005 | RESISTOR ARRAY | A3 | |
| 10 | 1 | AU PAD 34030414-006 | RESISTOR ARRAY | A4 | |
| 11 | 1 | AU PAD 34030414-007 | RESISTOR ARRAY | A2 | |
| 12 | 1 | AU PAD 34030414-008 | RESISTOR ARRAY | A1 | |
| 13 | 2 | T.A.B. CD4007A | TAB I.C. | U1,U2 RCA | |
| 14 | 2 | T.A.B. UA776 | T.A.B. I.C. | U3,U4 FAIRCHILD | |
| 15 | 1 | 7271351 | CRYSTAL | Y1 PIEZO | |
| 16 | AR | FMS40616 | WIRE,BOND,GOLD | TYPE II,.001 DIA.,GO | |
| 17 | AR | FMS40599 | EL.CONV.EPOXY ADH. | TY II,ABLEBOND 36-2 | |
| 18 | AR | FMS40600 | EPXY.ADH.ELEC.INSUL. | TY 2B,ABLEBOND 789-3 | |
| 19 | AR | DUPONT 8956 | SOLDER PASTE | 62-36-2 | |
| 20 | AR | R6100 | COAT,CONFORMAL | DOW CORNING | |
| 900 | REF | FPS18032 | MARKING | .09 REF HIGH CHAR METH H5 AND/OR B2 | 09128 |
| 901 | REF | 34030419 | TEST | | |

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FIGURE 3-13. CRYSTAL OSCILLATOR PARTS LIST

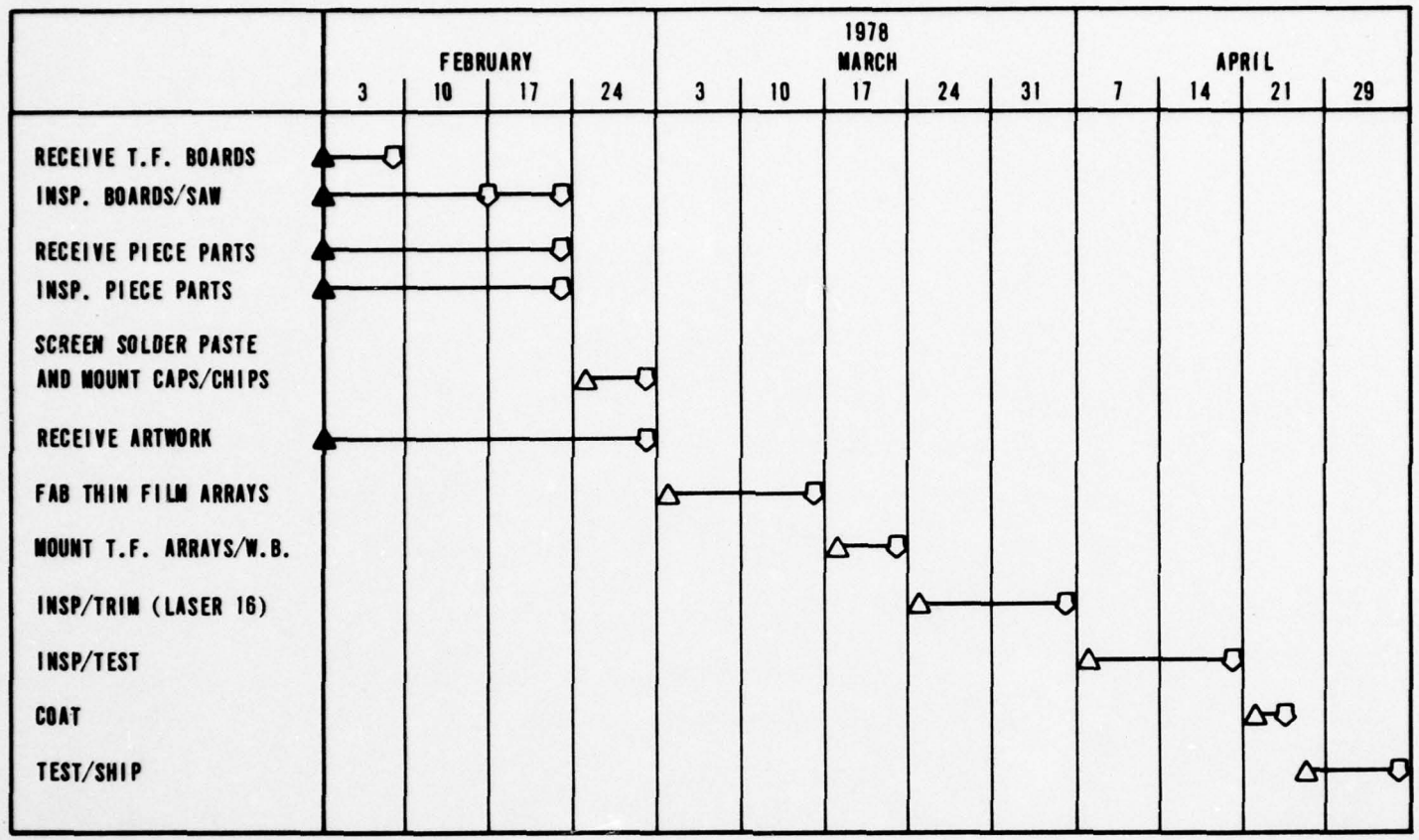



FIGURE 3-14. MANUFACTURING SCHEDULE FOR CRYSTAL OSCILLATOR

## CONCLUSIONS

During the second reporting period excellent progress was made in most areas of endeavor. The equipment definition continues on schedule with no major problems foreseen at this time. The material handling system design continues on schedule with good progress of the two parallel approaches: the mechanical feed system and the air feed system. Both designs continue to show excellent promise at this time. The manufacture of the first lot of engineering samples is continuing with the Electronic Commutator, Random Access Memory and Minilaser Counter Circuits being delivered during this reporting period. The first submission of engineering samples for the SINCGARS Discriminator is scheduled for the next reporting period.

## PLANS FOR NEXT REPORTING PERIOD

During the next reporting period, the delivery of the first lost of engineering samples for the SINCGARS Discriminator will be complete. The mechanical and air feed substrate handling system design and operational model build are expected to be completed. Evaluation of the mechanical feed system with the Weltek printer will be nearing completion. Detailed manufacturing schedules for the second engineering sample build of Commutator, SINCGARS Discriminator and Minilaser Counter will be available.

Appendix A

Universal Report No. _____

Originator's Report No. Commutator - 001

Revision _____

REPORT OF TEST ON Electronic Commutator - Lot 1 - First Submission of Engineering Samples

CDRL B001

TEST PERFORMED BY:

HONEYWELL, INC.
AVIONICS DIVISION
ST. PETERSBURG, FLA. 33733

TEST AUTHORIZED BY:

ECOM
FT. MONMOUTH, NJ 07703
CONTRACT NO. DAAB07-77-C-0526

Universal
Report No. _____

Originator's
Report No. Commutator - 001

Revision _____

REPORT OF TEST ON Electronic Commutator - Lot 1-First Submission of Engineering Samples

TEST PERFORMED BY:

HONEYWELL, INC.
AVIONICS DIVISION
ST. PETERSBURG, FLA. 33733

TEST AUTHORIZED BY:

ECOM
FT. MONMOUTH, NJ 07703
CONTRACT NO. DAAB07-77-C-0526

| | Date | Signature | |
|---|---|---|---|
| Test Initiated | 12-22-77 | | |
| Test Completed | 12-22-77 | | |
| Report Written By | 12-27-77 | S. Jones: S. Jones | |
| Technician | | | |
| Test Engineer | | | |
| Supervisor | 12-27-77 | W. Miranda: William R. Miranda | |
| Supervisor | | | |
| | | | |
| Government Repr. (if applicable) | | | |
| | | | |
| Final Release | 12-27-77 | | |
| | | | |

## 1.1 Reason for Test

Acceptance tests were performed on the first lot of engineering samples to be delivered to ECOM under Contract DAAB07-77-C-0526. The purpose of these tests is to demonstrate that these samples are functional and meet the specifications listed in paragraph 1.3.2.

## 1.2 Description of Test Apparatus

The equipment listed below was used to perform the tests specified in paragraph 1.3. The Commutator Manual Test Fixture is a special piece of test equipment built by Honeywell. This test fixture contains the loads and switches necessary to provide the test conditions specified in paragraph 1.3.3. Figure 1 shows the schematic of this fixture.

| Equipment Used | Model # | HI ID # | Last Calibrated | Due For Calibration |
|---|---|---|---|---|
| Ambitrol Twin Power Supply | TW-4005 | 30229 | N/A | N/A |
| Simpson VOM | 260 | CG19-18 | 7/18/77 | 7/18/78 |
| Fluke Digital Multimeter | 8600A | CG13567 | 12/6/77 | 7/6/78' |
| Fluke Digital Counter-Timer | 1952A | CG13243 | 9/15/77 | 3/15/78 |
| Commutator Manual Test Fixture | | | | |

NOTE: The power supply output levels were set with the aid of the Fluke Digital Multimeter.

## 1.3 Test Procedure

### 1.3.1 Test Circuit

The test circuit for the Electronic Commutator is shown in Figure 2. The switch outputs are listed in Table I.

1.3.2 Specifications:

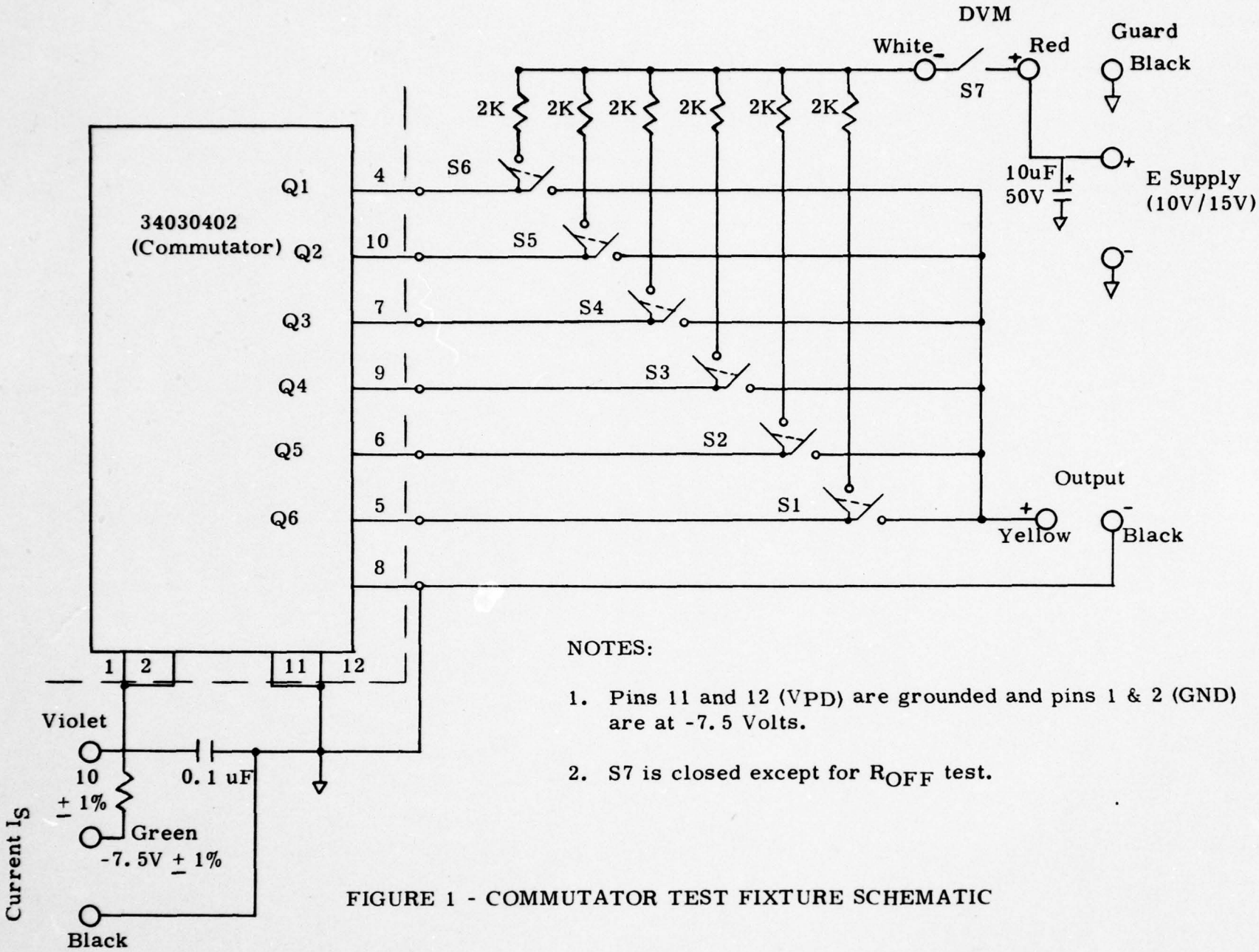
| Symbol | Parameter | Limit Min. | Limit Max. | Units |
|---|---|---|---|---|
| $T_C$ | Clock Period | 0.325 | 0.425 | Seconds |
| $T_D$ | Data Period | 1.3 | 1.7 | Seconds |
| $T_I$ | Identifier Period | 0.65 | 0.85 | Seconds |
| $R_{ON}$ | "On" Resistance | -- | 50 | Ohms |
| $R_{OFF}$ | "Off" Resistance (V=15V) | 100 | -- | Meg Ohms |
| $I_S$ | Supply Current | -- | 2 | Ma |

1.3.3 Test Conditions:

| Test | Condition |
|---|---|
| $T_C$ | Measure the clock period, Pin 9 U3, it shall be 0.375 ± 0.050 sec. Note: Refer to Test $T_I$. The narrow high state time intervals are the clock period $T_C$. |
| $T_D$ | Connect 2K 1/4 watt ± 5% resistors from pins 5, 6, 9, 7, 10 and 4 to a +10V ± 1% power supply referenced to Pin 8. Measure the "on" or low state interval at each of the specified pins. Interval at Pins 5, 9, & 10 shall be 0.75 ± 0.1 seconds. Interval at pins 6 7 and 4 shall be 1.5 ± 0.2 seconds. |
| $T_I$ | Connect pins 5, 6, 9, 7, 10 and 4 together "wire-or" and to a +10V power supply referenced to Pin 8 through a 333 ohm 1/4 watt ± 5% resistor. The identifier period is the double width "high" state. Measure the width of this period; it shall be 0.75 ± 0.1 seconds. |
| $R_{ON}$ | Using the same test set-up as for the measurement of $T_I$. Measure the "on" state voltage level at the "wire-or" connection to ground. The level shall be less than 250 millivolts. |
| $R_{OFF}$ | Connect a DVM with a 10M-ohm input resistance as follows. Input Hi to +15V, Lo to Pin 5, 6, 9, 7, 10, 4 or 5. The DVM guard shall be at the potential of Pin 8 per Figure 2. The voltmeter shall read less than 1.5 volts during the interval when the output under test is off (approximately 8 secs.). |

## 1.4 Test Data

The five engineering samples being delivered passed all functional tests. Test data sheets which contain the test results for Serial Numbers 3, 4, 5, 7 and 8 are attached.



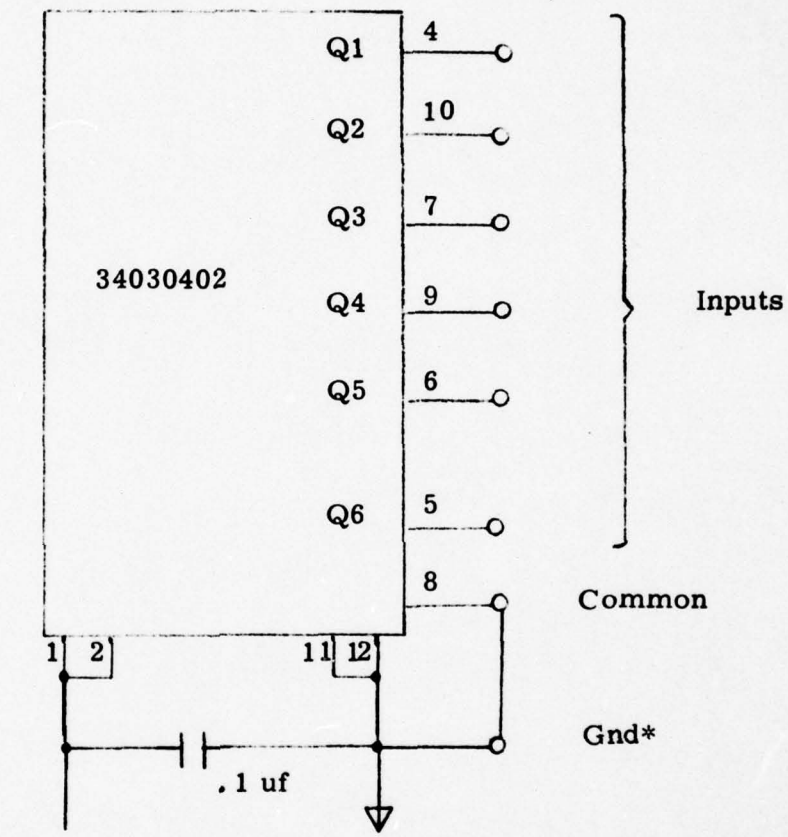

NOTES:

1. Pins 11 and 12 (VPD) are grounded and pins 1 & 2 (GND) are at -7.5 Volts.

2. S7 is closed except for $R_{OFF}$ test.

FIGURE 1 - COMMUTATOR TEST FIXTURE SCHEMATIC

FIGURE 2




*-7.5V±1%

*Note that for test purposes pins 11, 12 (VPD) is grounded and pins 1, 2 (GND) are at -7.5Volts.

## TABLE I

| Clk. Pulse | E | D | C | B | A | Inhibit As Built | Inhibit Should Be | Pin | Output Switch "On" |
|---|---|---|---|---|---|---|---|---|---|
| 0.375 sec 0 | 0 | 0 | 0 | 0 | 0 | $\bar{A}\ \bar{B}\ \bar{C}$ | $\bar{A}\ \bar{B}\ \bar{C}$ | | |
| 1 | 0 | 0 | 0 | 0 | 1 | | | 5 | Q6 |
| 2 | 0 | 0 | 0 | 1 | 0 | | | | |
| 3 | 0 | 0 | 0 | 1 | 1 | $A\ B\ \bar{C}$ | | | |
| 4 | 0 | 0 | 1 | 0 | 0 | | $\bar{A}\ \bar{B}\ C$ | | |
| 5 | 0 | 0 | 1 | 0 | 1 | | | | |
| 6 | 0 | 0 | 1 | 1 | 0 | | | 6 | Q5 |
| 7 | 0 | 0 | 1 | 1 | 1 | | | | |
| 8 | 0 | 1 | 0 | 0 | 0 | $\bar{A}\ \bar{B}\ \bar{C}$ | $\bar{A}\ \bar{B}\ \bar{C}$ | | |
| 9 | 0 | 1 | 0 | 0 | 1 | | | | |
| 10 | 0 | 1 | 0 | 1 | 0 | | | 9 | Q4 |
| 11 | 0 | 1 | 0 | 1 | 1 | $A\ B\ \bar{C}$ | | | |
| 12 | 0 | 1 | 1 | 0 | 0 | | $\bar{A}\ \bar{B}\ C$ | | |
| 13 | 0 | 1 | 1 | 0 | 1 | | | 7 | Q3 |
| 14 | 0 | 1 | 1 | 1 | 0 | | | | |
| 15 | 0 | 1 | 1 | 1 | 1 | | | | |
| 16 | 1 | 0 | 0 | 0 | 0 | $\bar{A}\ \bar{B}\ \bar{C}$ | $\bar{A}\ \bar{B}\ \bar{C}$ | | |
| 17 | 1 | 0 | 0 | 0 | 1 | | | | |
| 18 | 1 | 0 | 0 | 1 | 0 | | | 10 | Q2 |
| 19 | 1 | 0 | 0 | 1 | 1 | $A\ B\ \bar{C}$ | | | |
| 20 | 1 | 0 | 1 | 0 | 0 | | $\bar{A}\ \bar{B}\ C$ | | |
| 21 | 1 | 0 | 1 | 0 | 1 | | | | |
| 22 | 1 | 0 | 1 | 1 | 0 | | | 4 | Q1 |
| 23 | 1 | 0 | 1 | 1 | 1 | | | | |
| 24 | 1 | 1 | 0 | 0 | 0 | $\bar{A}\ \bar{B}\ \bar{C}$ | $\bar{A}\ \bar{B}\ \bar{C}$ | | |
| 0 | 0 | 0 | 0 | 0 | 0 | $\bar{A}\ \bar{B}\ \bar{C}$ | $\bar{A}\ \bar{B}\ \bar{C}$ | | |
| 1 | 0 | 0 | 0 | 0 | 1 | | | 5 | Q6 |
| 2 | 0 | 0 | 0 | 1 | 0 | | | | |

Switch Off

Switch On

COMMUTATOR
P/N 34030402-001

S/N 3
Date 12-22-77

1. Input Current

0.3 mA
2 mA max.

2. Data Period

| | | |
|---|---|---|
| 0.762 | 0.763 | 0.762 |
| 0.75 ± 0.1 sec. | 0.75 ± 0.1 sec. | 0.75 ± 0.1 sec. |
| (Pins 5 & 8) | (Pins 9 & 8) | (Pins 10 & 8) |
| 1.524 | 1.524 | 1.524 |
| 1.5 ± 0.2 sec. | 1.5 ± 0.2 sec. | 1.5 ± 0.2 sec. |
| (Pins 6 & 8) | (Pins 7 & 8) | (Pins 4 & 8) |

3. Identifier Period

0.762
0.75 ± 0.1 sec.

4. Clock Period (0.375 ± 0.05 sec.)

0.381
Clock Pulse

5. $R_{ON}$ (0.250 Volts Max.)

SRJ
Testman's Initials

6. $R_{OFF}$ (1.5 Volts Max.)

SRJ
Testman's Initials

OP 2 852

COMMUTATOR
P/N 34030402-001

S/N 4
Date 12-22-77

1. Input Current

0.3 mA
2 mA max.

2. Data Period

| | | |
|---|---|---|
| 0.743 | 0.743 | 0.743 |
| 0.75 ± 0.1 sec. (Pins 5 & 8) | 0.75 ± 0.1 sec. (Pins 9 & 8) | 0.75 ± 0.1 sec. (Pins 10 & 8) |
| 1.486 | 1.485 | 1.485 |
| 1.5 ± 0.2 sec. (Pins 6 & 8) | 1.5 ± 0.2 sec. (Pins 7 & 8) | 1.5 ± 0.2 sec. (Pins 4 & 8) |

3. Identifier Period

0.743
0.75 ± 0.1 sec.

4. Clock Period (0.375 ± 0.05 sec.)

0.371
Clock Pulse

5. $R_{ON}$ (0.250 Volts Max.)

SRJ
Testman's Initials

6. $R_{OFF}$ (1.5 Volts Max.)

SRJ
Testman's Initials

OP 2 852

COMMUTATOR
P/N 34030402-001

S/N 5
Date 12-22-77

1. Input Current

0.3 mA
2 mA max.

2. Data Period

| | | |
|---|---|---|
| 0.740 | 0.739 | 0.739 |
| 0.75 ± 0.1 sec. (Pins 5 & 8) | 0.75 ± 0.1 sec. (Pins 9 & 8) | 0.75 ± 0.1 sec. (Pins 10 & 8) |
| 1.479 | 1.478 | 1.478 |
| 1.5 ± 0.2 sec. (Pins 6 & 8) | 1.5 ± 0.2 sec. (Pins 7 & 8) | 1.5 ± 0.2 sec. (Pins 4 & 8) |

3. Identifier Period

0.739
0.75 ± 0.1 sec.

4. Clock Period (0.375 ± 0.05 sec.)

0.369
Clock Pulse

5. $R_{ON}$ (0.250 Volts Max.)

SRJ
Testman's Initials

6. $R_{OFF}$ (1.5 Volts Max.)

SRJ
Testman's Initials

OP 2 852

COMMUTATOR
P/N 34030402-001

S/N 7
Date 12-22-77

1. Input Current

0.3 mA
2 mA max.

2. Data Period

| | | |
|---|---|---|
| 0.782 | 0.782 | 0.782 |
| 0.75 ± 0.1 sec. (Pins 5 & 8) | 0.75 ± 0.1 sec. (Pins 9 & 8) | 0.75 ± 0.1 sec. (Pins 10 & 8) |
| 1.564 | 1.563 | 1.563 |
| 1.5 ± 0.2 sec. (Pins 6 & 8) | 1.5 ± 0.2 sec. (Pins 7 & 8) | 1.5 ± 0.2 sec. (Pins 4 & 8) |

3. Identifier Period

0.781
0.75 ± 0.1 sec.

4. Clock Period (0.375 ± 0.05 sec.)

0.391
Clock Pulse

5. $R_{ON}$ (0.250 Volts Max.)

DRJ
Testman's Initials

6. $R_{OFF}$ (1.5 Volts Max.)

DRJ
Testman's Initials

OP 2 852

COMMUTATOR
P/N 34030402-001

S/N 8
Date 12-22-77

1. Input Current

0.3 mA
2 mA max.

2. Data Period

| | | |
|---|---|---|
| 0.779 | 0.779 | 0.779 |
| 0.75 ± 0.1 sec. (Pins 5 & 8) | 0.75 ± 0.1 sec. (Pins 9 & 8) | 0.75 ± 0.1 sec. (Pins 10 & 8) |
| 1.558 | 1.558 | 1.558 |
| 1.5 ± 0.2 sec. (Pins 6 & 8) | 1.5 ± 0.2 sec. (Pins 7 & 8) | 1.5 ± 0.2 sec. (Pins 4 & 8) |

3. Identifier Period

0.779
0.75 ± 0.1 sec.

4. Clock Period (0.375 ± 0.05 sec.)

0.389
Clock Pulse

5. $R_{ON}$ (0.250 Volts Max.)

DRJ
Testman's Initials

6. $R_{OFF}$ (1.5 Volts Max.)

DRJ
Testman's Initials

OP 2 852

Appendix B

Universal Report No. _____

Originator's Report No. RAM -001

Revision _____

REPORT OF TEST ON Random Access Memory - First Submission of Engineering Samples

CDRL B001

TEST PERFORMED BY:

HONEYWELL, INC.
AVIONICS DIVISION
ST. PETERSBURG, FLA. 33733

TEST AUTHORIZED BY:

ECOM
FT. MONMOUTH, NJ 07703
CONTRACT NO. DAAB07-77-C-0526

Universal Report No. _____

Originator's Report No. RAM -001

Revision _____

REPORT OF TEST ON Random Access Memory - First Submission of Engineering Samples

TEST PERFORMED BY:

HONEYWELL, INC.
AVIONICS DIVISION
ST. PETERSBURG, FLA. 33733

TEST AUTHORIZED BY:

ECOM
FT. MONMOUTH, NJ 07703
CONTRACT NO. DAAB07-77-C-0526

| | Date | Signature | |
|---|---|---|---|
| Test Initiated | 12-29-77 | | |
| Test Completed | 12-29-77 | | |
| Report Written By | 12-30-77 | S. Jones S. Jones | |
| Technician | | | |
| Test Engineer | | | |
| Supervisor | 12-30-77 | W. Miranda William R. Miranda | 1/3/78 |
| Supervisor | | | |
| | | | |
| Government Repr. (if applicable) | | | |
| | | | |
| Final Release | 12-30-77 | | |
| | | | |

## 1.1 Reason for Test

Acceptance tests were performed on the first lot of engineering samples to be delivered to ECOM under contract DAAB07-77-C-0526. The purpose of these tests is to demonstrate that these samples are functional and meet the test requirements delineated in paragraph 1.3.

## 1.2 Description of Test Apparatus

The equipment listed below was used to perform the tests specified in paragraph 1.3. The Lambda power supply was used in parallel with the Macrodata test station supply to provide the necessary supply current to the unit under test (UUT). The Lambda supply output level was set to 5.0V with the aid of the Simpson voltmeter.

| Equipment Used | Model # | HI ID # | Last Calibrated | Due For Calibration |
|---|---|---|---|---|
| Macrodata Memory Test Station | 150 | CG4972-1 | 12/20/77 | 2/20/78 |
| Lambda Power Supply | LP521-FM | CG11713 | 3/4/77 | 3/4/78 |
| Simpson VOM | 260 | X19-224 | 3/2/77 | 3/2/78 |

## 1.3 Test Description

### 1.3.1 General Description of Test Program

The deliverable RAM's were exercised by a modified GALPAT program. A description of the tests which were performed by this program are listed below.

GALPAT: Galloping Ones and Zeroes Pattern Subroutine

USAGE: Tests all bits in the array, the addressing, the interaction between bits and pattern and sequence dependency for transient performance for all possible address transitions from one location to another.

OPERATION: A background pattern is written through the memory. Starting at the first memory location a testword is written. The testword is usually the complement of the background pattern. The memory is then read at all background locations in the following sequence:

- o read background location
- o read testword location
- o read background location
- o increment background location pointer

The sequence is continued until all background positions in memory have been tested. The testword pattern is then moved to the next location and the previous sequence is repeated. Each succeeding location in the memory is tested following the same sequence. Note: There were 4,198,403 tests executed in this memory test.

### 1.3.2 Detailed Program Description

The detailed Macrodata program form which was used for acceptance tests is shown in Figure 1. The logic flow diagram for the test sequence is illustrated in Figure 2.

## 1.4 Test Data

The five engineering samples being delivered passed the functional tests described in paragraph 1.3. Test Data Sheets which contain the test results for Serial Numbers 4, 5, 7, 8 and 9 are attached.

# MACRODATA MD-150 SERIES TEST SYSTEM

## CONTROL MEMORY (CTRLM) PROGRAMMING FORM

DEVICE _____ PROGRAMMED BY _____ DATE _____ TEST PURPOSE _____ PAGE ____ OF ____

DOCUMENT NO. _____ APPROVED BY _____ DATE _____ _____ TAPE NO. ____ , ____

| CONTROL MEMORY ADDRESS (OCTAL) | | JUMP ADDRESS OR INDEX (13 22 21 20 19 18 17 16) | C R W (15 14 13) | COMMAND (12 11 10 9 8) | DATA (7 6 5 4) | ADDRESS (3 2 1 0) | CONTROL MEMORY ADDRESS OCTAL (r1 or 3) | BINARY | |
|---|---|---|---|---|---|---|---|---|---|
| 140/340 | Z = | | | | | | ; 4,0 ; | 1 100 000 | LJ = 1, G → A |
| 141/341 | Z = | | | | | | ; 4,1 ; | 1 100 001 | JANN → 141, A+1 → A, WRITE |
| 142/342 | Z = | | | | | | ; 4,2 ; | 1 100 010 | NOP, G → A, T ↔ B |
| 143/343 | Z = | | | | | | ; 4,3 ; | 1 100 011 | JANN → 145, T ↔ B, A → X, A+1 → A |
| 144/344 | Z = | | | | | | ; 4,4 ; | 1 100 100 | NOP, G → A |
| 145/345 | Z = | | | | | | ; 4,5 ; | 1 100 101 | NOP, A ↔ X, Read |
| 146/346 | Z = | | | | | | ; 4,6 ; | 1 100 110 | JINN → 0, T ↔ B, A ↔ X, Read |
| 147/347 | Z = | | | | | | ; 4,7 ; | 1 100 111 | DCJN → 151, T ↔ B, A+1 → A, Read |
| 150/350 | Z = | | | | | | ; 5,0 ; | 1 101 000 | NOP, G → A |
| 151/351 | Z = | | | | | | ; 5,1 ; | 1 101 001 | DCJX → 146, A ↔ X, Read |
| 152/352 | Z = | | | | | | ; 5,2 ; | 1 101 010 | JANN → 143, T ↔ X, A+1 → A |
| 153/353 | Z = | | | | | | ; 5,3 ; | 1 101 011 | JSBI → 141, G → A |
| 154/354 | Z = | | | | | | ; 5,4 ; | 1 101 100 | J → 3, G → A |
| 155/355 | Z = | | | | | | ; 5,5 ; | 1 101 101 | |
| 156/356 | Z = | | | | | | ; 5,6 ; | 1 101 110 | |
| 157/357 | Z = | | | | | | ; 5,7 ; | 1 101 111 | |
| 160/360 | Z = | | | | | | ; 6,0 ; | 1 110 000 | |
| 161/361 | Z = | | | | | | ; 6,1 ; | 1 110 001 | |
| 162/362 | Z = | | | | | | ; 6,2 ; | 1 110 010 | |
| 163/363 | Z = | | | | | | ; 6,3 ; | 1 110 011 | |
| 164/364 | Z = | | | | | | ; 6,4 ; | 1 110 100 | |
| 165/365 | Z = | | | | | | ; 6,5 ; | 1 110 101 | |
| 166/366 | Z = | | | | | | ; 6,6 ; | 1 110 110 | |
| 167/367 | Z = | | | | | | ; 6,7 ; | 1 110 111 | |
| 170/370 | Z = | | | | | | ; 7,0 ; | 1 111 000 | |
| 171/371 | Z = | | | | | | ; 7,1 ; | 1 111 001 | |
| 172/372 | Z = | | | | | | ; 7,2 ; | 1 111 010 | |
| 173/373 | Z = | | | | | | ; 7,3 ; | 1 111 011 | |
| 174/374 | Z = | | | | | | ; 7,4 ; | 1 111 100 | |
| 175/375 | Z = | | | | | | ; 7,5 ; | 1 111 101 | |
| 176/376 | Z = | | | | | | ; 7,6 ; | 1 111 110 | |
| 177/377 | Z = | | | | | | ; 7,7 ; | 1 111 111 | |

JUMP ADDRESS OR INDEX (OCTAL)

X = NOT PUNCH

Address
X100 A → A
X101 A+1 → A
X110 G → A
X111 X → A
A100 A+1 → A
A101 A+1 → X
A110 EXT → A
A111 A+1 → X
X = 1 A → T
X = 0 X → X

Data
B000 T → T
B001 T → T
B010 T → T
B011 B → T
B100 T+1 → T
B101 T+2 → T
B110 EXT → T
B111 T-1 → T
B = 1 T → B
B = 0 B → B

Command
00000 JSBI
00100 LJ
00110 LY
01000 NOP
01010 JSB
01011 RSB
01100 JFZ
01110 TCY
10000 J
10001 JOZ
10010 JAEX
10011 JAEN
10100 ICX
11000 JANX
11001 JANN
11010 DCJX
11011 DCJN
11100 JTNB
11101 JTNM
11110 ICXC

Shift Modifier
00 T_0 → A_0
01 0 → A_0
10 1 → A_0
11 EXT → A_0
T Shift (Y_0 = 0)
00 T_0 → T_0
01 0 → T_0
10 1 → T_0
11 Random → T
T Shift (Y_0 = 1)
T → B_0
B_0 → T_0

15-FORM-CTRLM

FIGURE 1 - MACRODATA PROGRAM



BEST AVAILABLE COPY

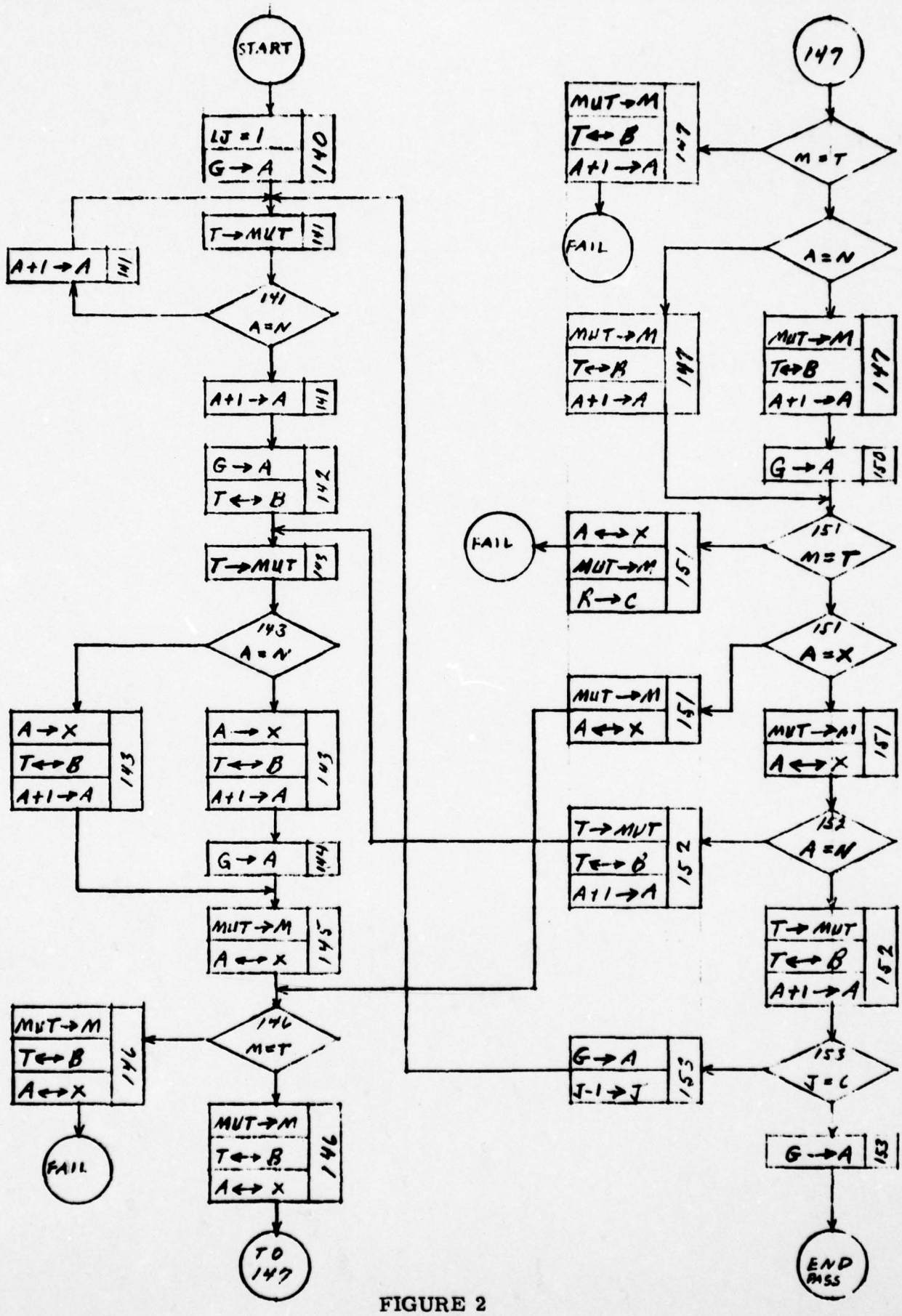



FIGURE 2
LOGIC FLOW DIAGRAM

RANDOM ACCESS MEMORY
P/N 34030405-001
S/N 4
DATE 12-29-77

1. MACRODATA TEST

PASS MCQ

Pass/Fail and Testman's Initials

OP 2 852

RANDOM ACCESS MEMORY
P/N 34030405-001
S/N 5
DATE 12-29-77

1. MACRODATA TEST

PASS MCQ
Pass/Fail and Testman's Initials

OP 2
852

RANDOM ACCESS MEMORY
P/N 34030405-001
S/N 7
DATE 12-29-77

1. MACRODATA TEST

PASS MCQ
Pass/Fail and Testman's Initials

OP 2 8521

RANDOM ACCESS MEMORY
P/N 34030405-001
S/N 8
DATE 12-29-77

1. MACRODATA TEST

PASS MCG

Pass/Fail and Testman's Initials

OP 2 852

RANDOM ACCESS MEMORY
P/N 34030405-001
S/N 9
DATE 12-29-77

1. MACRODATA TEST

PASS MCa
Pass/Fail and Testman's Initials

OP 2 1852

Appendix C

Universal Report No. _____

Originator's Report No. Minilaser - 001

Revision _____

REPORT OF TEST ON Minilaser Counter-First Submission of Engineering Samples

CDRL B001

TEST PERFORMED BY:

HONEYWELL, INC.
AVIONICS DIVISION
ST. PETERSBURG, FLA. 33733

TEST AUTHORIZED BY:

ECOM
FT. MONMOUTH, NJ 07703
CONTRACT NO. DAAB07-77-C-0526

Universal
Report No. _____

Originator's
Report No. Minilaser - 001

Revision _____

REPORT OF TEST ON Minilaser Counter-First Submission of Engineering Samples

TEST PERFORMED BY:

HONEYWELL, INC.
AVIONICS DIVISION
ST. PETERSBURG, FLA. 33733

TEST AUTHORIZED BY:

ECOM
FT. MONMOUTH, NJ 07703
CONTRACT NO. DAAB07-77-C-0526

| | Date | Signature | |
|---|---|---|---|
| Test Initiated | 12-29-77 | | |
| Test Completed | 12-29-77 | | |
| Report Written By | 12-29-77 | S. Jones S. Jones | |
| Technician | | | |
| Test Engineer | | | |
| Supervisor | 12-29-77 | W. Miranda Wm R. Miranda 12/30/77 | |
| Supervisor | | | |
| | | | |
| Government Repr. (if applicable) | | | |
| | | | |
| Final Release | 12-29-77 | | |
| | | | |

## 1.1 Reason for Test

Acceptance tests were performed on the first lot of engineering samples to be delivered to ECOM under contract DAAB07-77-C-0526. The purpose of these tests is to demonstrate that these samples are functional and meet the static and dynamic test requirements specified in paragraphs 1.3.1 and 1.3.2.

## 1.2 Description of Test Apparatus

The equipment listed below was used to perform the tests specified in paragraph 1.3. The Dynamic Test Fixture is a special piece of test equipment built by Honeywell. This test fixture contains the circuitry and switches necessary to perform the dynamic tests specified in Paragraph 1.3.2. Figure 1 shows the schematic of this fixture.

| Equipment Used | Model # | HI ID # | Last Calibrated | Due For Calibration |
|---|---|---|---|---|
| Ambitrol Twin Power Supply | TW-4005 | 30229 | N/A | N/A |
| Fluke Digital Multimeter | 8600A | CG13567 | 12/6/77 | 7/6/78 |
| Fairchild Digital Tester | 5000 | CD4632-1A, 1B, 1K | 9/20/77 | 1/4/78 |

NOTE: The power supply output level was set with the aid of the Fluke Digital Multimeter.

## 1.3 Test Procedure

### 1.3.1 Static Testing

The static tests specified below were performed on the Fairchild 5000 Digital Test Station. The software program used to control the Fairchild test station during these tests is listed in Table I.

(a) Apply a ground (GND) to Pin 30 of the unit under test (UUT) to make the following measurements.

| Fairchild Test # | UUT Pin | Voltage (V) |
|---|---|---|
| 1 | 14 | >2.7 |
| 2 | 15 | >2.7 |
| 3 | 23 | >2.7 |
| 4 | 32 | >2.7 |
| 5 | 33 | >2.7 |
| 6 | 39 | >2.7 |
| 11 | 25 | <0.5 |
| 12 | 26 | <0.5 |
| 13 | 34 | <0.5 |
| 14 | 36 | <0.5 |
| 15 | 38 | <0.5 |

NOTE: Apply the following potentials and measure the resulting current.

| Fairchild Test # | UUT Pin | Voltage (V) | Current |
|---|---|---|---|
| 7 | 16 | 5.0 | 10 uA max. |
| 8 | 17 | 5.0 | 10 uA max. |
| 9 | 18 | 5.0 | 10 uA max. |
| 16 | 2 | 2.7 | 20 uA max. |
| 17 | 3 | 2.7 | 20 uA max. |
| 18 | 4 | 2.7 | 20 uA max. |
| 19 | 5 | 2.7 | 20 uA max. |
| 20 | 27 | 2.7 | 20 uA max. |
| 21 | 31 | 2.7 | 20 uA max. |
| 22 | 22 | 2.7 | 20 uA max. |
| 23 | 24 | 2.7 | 20 uA max. |
| 24 | 2 | 0.4 | -0.8 mA max. |
| 25 | 3 | 0.4 | -0.8 mA max. |
| 26 | 4 | 0.4 | -0.8 mA max. |
| 27 | 5 | 0.4 | -0.8 mA max. |

NOTE: Force the following current and measure the resulting voltage.

| Fairchild Test # | UUT Pin | Voltage (V) | Current |
|---|---|---|---|
| 10 | 19 | 0.4V Max. | 20mA |

(b) Remove the ground (GND) to Pin 30 of the UUT to make the following measurements.

| Fairchild Test # | UUT Pin | Voltage (V) |
|---|---|---|
| 28 | 37 | >2.7 |
| 29 | 35 | <0.5 |

NOTE: Apply the following potential and measure the resulting current.

| Fairchild Test # | UUT Pin | Voltage (V) | Current |
|---|---|---|---|
| 30 | 30 | 0.4 | -0.8 ma max. |

### 1.3.2 Dynamic Testing

Configure the circuit per Figure 1 to perform the following tests.

a) 640 yard range: close S4; S3 and S5 are open. Initialize the circuitry by momentarily closing switch S1 for 100 ns minimum. The display shall be blank. Momentarily close S2 for 100 ns minimum after S1 has been opened. The display shall then read 640. (Note: The display may read 630 or 650 due to a race problem in the test fixture circuitry.)

b) Over-Range: Close S5; S3 and S4 are open. Initialize the circuitry by momentarily closing switch S1 for 100 ns minimum. The display shall be blank. Momentarily close S2 for 100 ns minimum after S1 has been opened. The display will then read decimal points (3) only.

c) Under-Range: Close S3; S4 and S5 are open. Initialize the circuitry by momentarily closing switch S1 for 100 ns minimum. The display shall be blank. Momentarily close S2 for 100 ns minimum after S1 has been opened. The display will then read decimal points (3) only.

### 1.4 Test Data

The five engineering samples being delivered passed all static and dynamic functional tests. Test Data Sheets which contain the test results for Serial Numbers 3, 4, 5, 6 and 7 are attached.

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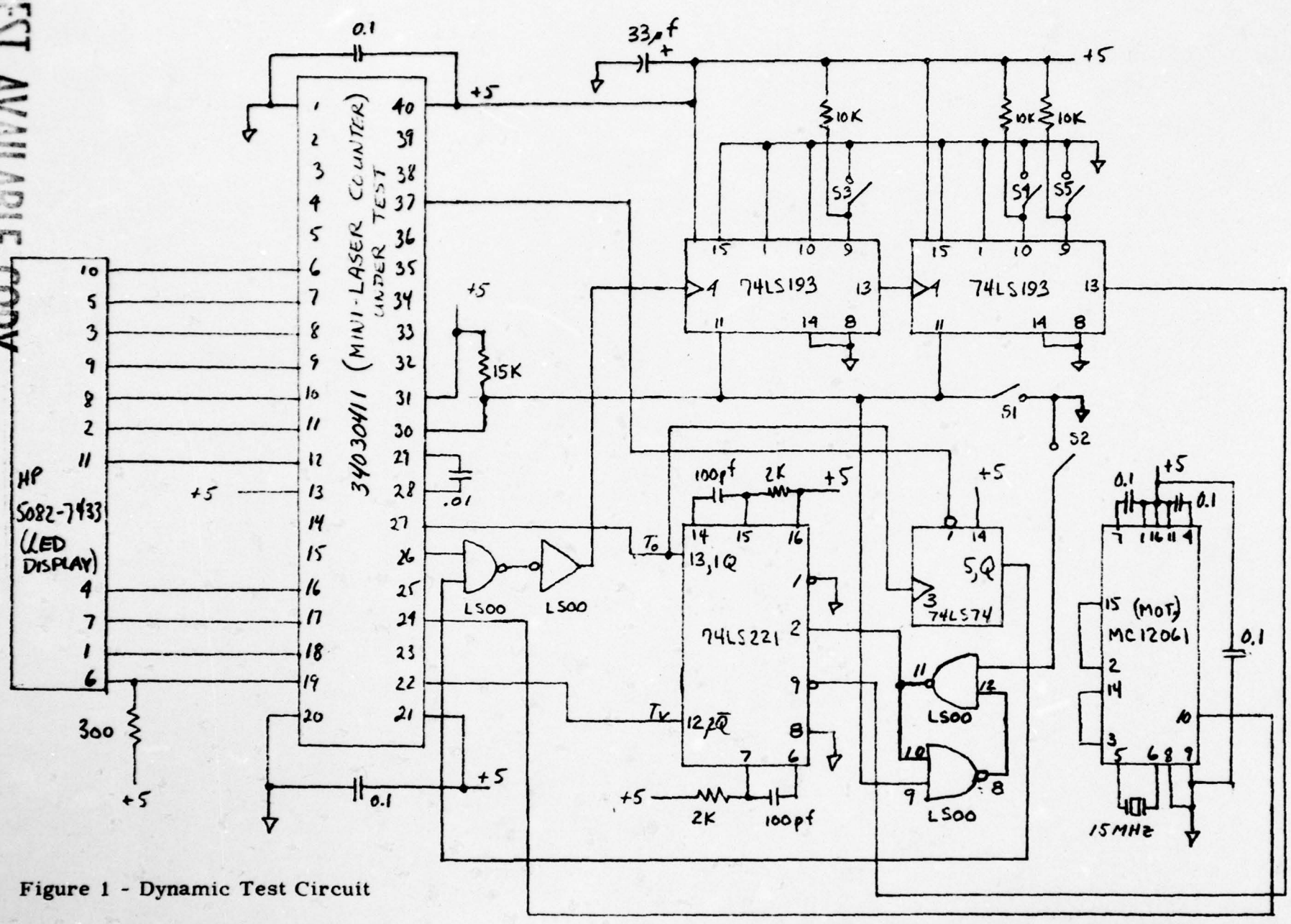


Figure 1 - Dynamic Test Circuit

Table I. - Program Listing for Fairchild Static Tests.

```
FTCP
MINILASR

*T   1

0425007300000. 10A000000000. 110000000000A. 1240000000004:
1300000000004. 2140007014000. 251523323339: 2C0100500012:
AA0750002700:

*T   2
1240000000004: 2105007016000. 251710000000: 2C0100500012:
AA0440000000:

*T   3
2142000001900. AA0640000000:

*T   4
2140000002500: 252634363000: AA2650000005:

*T   5
2102707000200. 250304052731: 2C0100500012. AA2520000003:


*T   6
21FFFFFF2200. AA2540000005:

*T   7
21FFFFFF2400. AA2560000005:

*T   8
2104006000200. 250304050000. AA3600000000.

*T   9
1240000000000. 2140000003700. AA0750002700.

*T  10
2140000003500. AA2650000005:

*T  11
2104006003000. AA3600000000.

*T  12

FFFF:
```

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```
ID  = MINILASR
STN = 1
S N = 00003
00001     4.312 V
00002     4.300 V
00003     4.334 V
00004     4.351 V
00005     4.352 V
00006     4.183 V
00007     0.040UA
00008     0.035UA
00009     0.032UA
00010   0.0000 V
00011   0.1583 V
00012   0.1842 V
00013   0.2022 V
00014   0.1285 V
00015   0.1775 V
00016      0.00UA
00017      0.01UA
00018      0.00UA
00019      0.00UA
00020   -  0.01UA
00021      0.00UA
00022      0.00UA
00023      0.00UA
00024  -0.2000MA
00025  -0.2009MA
00026  -0.2016MA
00027  -0.2004MA
00028     4.364 V
00029   0.2214 V
00030  -0.2434MA
```

CP 2 052

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MINILASER COUNTER
P/N 34030411-001

S/N 3
Date 12-29-77

1. Test

640
630, 640 or 650

2. Under-range (Three decimal Points)

SRJ
Testman's Initials

3. Over-range (Three decimal Points)

SRJ
Testman's Initials

OP 2
85.2

```
ID  = MINILASR
STN = 1
S N = 00004
00001     4.316 V
00002     4.307 V
00003     4.336 V
00004     4.356 V
00005     4.351 V
00006     4.176 V
00007     0.047UA
00008     0.042UA
00009     0.040UA
00010    0.1055 V
00011    0.1145 V
00012    0.1000 V
00013    0.1014 V
00014    0.1157 V
00015    0.1502 V
00016      0.00UA
00017      0.00UA
00018  -   0.01UA
00019      0.00UA
00020      0.00UA
00021      0.00UA
00022      0.00UA
00023      0.00UA
00024  -0.2167MA
00025  -0.2104MA
00026  -0.2125MA
00027  -0.2152MA
00028     4.341 V
00029    0.1973 V
00030  -0.2509MA

<>
```

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MINILASER COUNTER
P/N 34030411-001

S/N 4
Date 12-29-77

1. Test

640
630, 640 or 650

2. Under-range (Three decimal Points)

SRJ
Testman's Initials

3. Over-range (Three decimal Points)

SRJ
Testman's Initials

OP 2/852

```
ID  = MINILASR
SIN = 1
S N = 00005
00001     4.322 V
00002     4.312 V
00003     4.327 V
00004     4.351 V
00005     4.350 V
00006     4.187 V
00007     0.052UA
00008     0.046UA
00009     0.042UA
00010   0.1115 V
00011   0.1319 V
00012   0.1288 V
00013   0.1268 V
00014   0.1466 V
00015   0.1354 V
00016      0.00UA
00017      0.00UA
00018      0.00UA
00019      0.00UA
00020  -   0.01UA
00021      0.01UA
00022      0.00UA
00023  -   0.01UA
00024  -0.2031MA
00025  -0.2021MA
00026  -0.2008MA
00027  -0.2029MA
00028     4.362 V
00029   0.1023 V
00030  -0.2523MA
```

OP 2 852

<>

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MINILASER COUNTER
P/N 34030411-001

S/N 5
Date 12-29-77

1. Test

640
630, 640 or 650

2. Under-range (Three decimal Points)

DRJ
Testman's Initials

3. Over-range (Three decimal Points)

DRJ
Testman's Initials

OP 2 852

```
ID  = MINILASR
STN = 1
S N = 00006
00001     4.312 V
00002     4.304 V
00003     4.326 V
00004     4.356 V
00005     4.356 V
00006     4.195 V
00007     0.050UA
00008     0.034UA
00009     0.036UA
00010    0.1100 V
00011    0.1667 V
00012    0.1963 V
00013    0.1771 V
00014    0.1330 V
00015    0.1451 V
00016      0.00UA
00017      0.00UA
00018      0.00UA
00019      0.00UA
00020  -   0.01UA
00021      0.00UA
00022  -   0.01UA
00023      0.00UA
00024  -0.2050MA
00025  -0.2065MA
00026  -0.2069MA
00027  -0.2079MA
00028     4.343 V
00029    0.2194 V
00030  -0.2462MA

<>
```

CP 2 852

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MINILASER COUNTER
P/N 34030411-001

S/N 6
Date 12-29-77

1. Test

640
630, 640 or 650

2. Under-range (Three decimal Points)

DRJ
Testman's Initials

3. Over-range (Three decimal Points)

DRJ
Testman's Initials

OP 2
852

```
ID  = MINILASR
STN = 1
S N = 00007
00001     4.314 V
00002     4.300 V
00003     4.335 V
00004     4.355 V
00005     4.351 V
00006     4.188 V
00007     0.054UA
00008     0.041UA
00009     0.040UA
00010    0.1162 V
00011    0.1130 V
00012    0.1843 V
00013    0.1911 V
00014    0.1492 V
00015    0.1508 V
00016      0.00UA
00017      0.00UA
00018  -   0.01UA
00019      0.00UA
00020      0.00UA
00021      0.00UA
00022      0.00UA
00023      0.00UA
00024  -0.2181MA
00025  -0.2154MA
00026  -0.2150MA
00027  -0.2181MA
00028     4.344 V
00029    0.2119 V
00030  -0.2407MA
```

OP 2 852

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MINILASER COUNTER
P/N 34030411-001

S/N 7
Date 12-29-77

1. Test

640
630, 640 or 650

2. Under-range (Three decimal Points)

SRJ
Testman's Initials

3. Over-range (Three decimal Points)

SRJ
Testman's Initials

OP 2
852

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