A DIGITAL-TO-VIDEO CONVERTER FOR AIRBORNE TELEVISION DISPLAYS

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Avionics Laboratory

July 1977
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    A digital to video converter has been developed for Low Level nap-of-the-earth experimental helicopter flight studies. The converter accepts data from a digital computer and converts it to a standard 525 line television display. The converter can also generate a shades of gray or color video display.
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1. INTRODUCTION

This report covers the design and fabrication of a digital to video converter which accepts data from a digital computer and converts it to a standard 525 line television display. The system was developed for low level nap-of-the-earth helicopter flight studies and will be flight tested in the Experimental Vehicle for Avionics Research (EVAR) which is a CH-53 helicopter instrumented for Avionics R&D programs.

Operation of Army aircraft during day and night conditions at or below tree top level requires the pilot to be aware of the upcoming terrain characteristics. At present, low level operations are performed with the pilot dedicated to the task of piloting the vehicle. The copilot verbally informs the pilot of upcoming terrain from hand-held maps. At night, this is extremely difficult. Improving the method of informing the pilot of approaching terrain, thus reducing the hazards of low level night flight, are the desired goals of this project.

The design goal was to develop a general purpose computer driven display whose information content was entirely determined by the computer software. However, contour maps and various aircraft symbology were the two main items to be displayed.

Approximately 300 digital integrated circuits and static MOS RAM memory circuits were used in the design of the converter which has a memory capacity of 131 thousand bits.

2. SYSTEM REQUIREMENTS

The system requirements were:

a. The converter must be interfaced with the existing airborne computer system and be compatible with standard 525 line television systems.

b. The display must have a 256 by 256 bit resolution capability.

c. There must not be any "break-up" of the presently displayed image during the update period from the computer.

d. The display format must be square rather than the usual 4 by 3 aspect ratio.

3. DESIGN APPROACH AND MEMORY ORGANIZATION

The system requirement of not "breaking-up" the displayed data during the data update dictated the basic design approach and memory organization. A system block diagram showing the converter interfaced to the rest of the system is shown in Figure 1. The computer is a Singer/Kearfott SKC-2000 with a customized I/O controller to which the converter is directly interfaced.

Figure 1. System block diagram
The memory was organized into two arrays of 256 by 256 bits or 65K bits each which are alternately written into the computer and read out into the television display. The read memory acts as a refresh to the television display and its timing is controlled by the television horizontal and vertical synchronizing signals. The write memory is loaded from the computer, essentially at whatever rate the computer desires.

The memories are organized and displayed on the screen as shown in Figure 2. Since there are only 240 visible lines per field available, it was decided to display 230 lines of data per field, leaving a margin of 5 lines on the top and bottom of the screen.

The entire memory is fabricated on 16 printed circuit boards, 8 per memory array. The computer word length is 32 bits and each memory board stores a vertical "slice" of memory 32 bits wide. A memory board has eight 4 by 256 memory chips plus four 8 bit shift register chips, which when inter-connected with other memory boards forms a 256 bit shift register controlled by the reading operation. The data is written into memory, from the computer, one word at a time and read out eight words or one line at a time into the shift register. The data is then shifted out into a video driver at approximately 7 MHz. The requirement to have a nearly square format determined the 7 MHz video data rate. This compression of the data gives an effective horizontal resolution of approximately 340 bits if data were displayed across the full screen at the 7 MHz rate. A block diagram of the converter is shown in Figure 3.

4. COMPUTER INTERFACE AND WRITE CONTROL

The computer interface is a straight-forward hand-shaking type of control. The write control logic was designed around a 4 us word time or 250 kHz data rate. One memory can be loaded in less than 8 ms, provided the computer has data available when requested by the converter. Thus, the memory can be updated at approximately twice the field rate of the television system.

The memories are not random accessed by the computer since the contour map mode requires an entire update. The entire matrix of data (block transfer) is sent to the converter sequentially from word 0 through 1839 and a simple address counter keeps track of the data. The computer provides a 4 MHz clock which was used to control the write operation. Data lines are terminated in line receivers and bussed to the entire memory.

When a memory has been fully updated, no further data requests are sent to the computer. The updated memory waits until the read or refresh memory has completed a scan and the television system is in the start of the vertical blanking period. At this time the memories are switched without breaking-up the displayed image and the process repeats.

5. READ CONTROL

The timing of the reading operation is controlled by the television synchronization signals, namely, the horizontal and vertical drive signals. When the vertical drive is received, five horizontal drives are counted in order to vertically position the start of the first valid line of data to be displayed. At this point, a horizontal counter determines the starting point of the first
8 CARDS PER MEMORY BANK. EACH CARD IS A VERTICAL SLICE OF THE DISPLAY 32 BITS WIDE.

<table>
<thead>
<tr>
<th>MEM CARD</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
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<tr>
<td>BIT</td>
<td>0-31</td>
<td>0-31</td>
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<td>0-31</td>
<td>0-31</td>
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<td>0</td>
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<td>19</td>
<td>20</td>
<td>21</td>
<td>22</td>
<td>23</td>
</tr>
<tr>
<td>L1NE</td>
<td>1832</td>
<td>1833</td>
<td>1834</td>
<td>1835</td>
<td>1836</td>
<td>1837</td>
<td>1838</td>
<td>1839</td>
</tr>
</tbody>
</table>

WORDS ARE TRANSFERRED FROM COMPUTER IN ORDER FROM 0 TO 1839.

WORDS ARE READ OUT OF MEMORY 8 WORDS OR ONE LINE AT A TIME, AND ARE SHIFTED OUT INTO VIDEO BIT 0 FIRST.

Figure 2. Memory matrix layout and display format
Figure 3. Digital to video converter
bit of information to be shifted into video. Horizontal positioning was necessary because of the requirement for a square data format centered within the standard 4 by 3 television raster. During this counting period, the read control housekeeping functions are performed. The read memory is accessed and loaded into the shift register. After the starting point is determined, the 7 MHz shift clock is enabled, shifting out the 256 bits of data into video. At the end of the shifting period, the read memory address counters are advanced and the cycle repeats line by line. After a field has been scanned and the entire read memory converted to video, the memory is read again at the television field rate of 60 Hz unless the write memory has been loaded and switched to the read mode.

The read/write memory address lines are alternately switched between arrays of memory through multiplexer circuits which are under control of the read/write control logic.

Since the read operation takes a very small percentage of the time (one read per television line or every 63.5 us) the read operation occurs as a periodic interrupt to the write operation, which is essentially continuous.

The vertical resolution requirement allowed identical data to be repeated for both odd and even fields of the television system.

Figures 4 and 5 show examples of contour maps and Figures 6 through 9 show alphanumerics and typical symbology. The alphanumerics and symbols are software generated since the greatest flexibility was desired to determine their size and shape during these initial investigations. Figures 4 through 9 are photographs of the television monitor as driven by the converter.

6. SHADES OF GRAY CAPABILITY

Shortly after the converter was in operation, it became apparent that a shades of gray capability would greatly improve the usefulness of the display in the contour map mode. Although not originally designed for shades of gray, a design modification was incorporated to achieve this mode of operation. The multiplexer, write control, and one read control circuit board were redesigned as interchangeable replacements when it is desired to use shades of gray. Four shades are possible by simultaneously reading both memory arrays and converting the two bit output to four levels with a simple D/A converter before the video driver.

In this mode, the writing operation occurs alternately between memories, one line at a time in each memory. This requirement was determined by the contour map whose computation is done a line at a time. Due to the amount of computation required to generate a map, the updating process is much slower than the television scan rate and the new data can be seen progressing down the screen since we are now reading both memories simultaneously. However, for this initial investigation, it was considered acceptable. The symbology update rate is sufficiently fast to eliminate this problem.

A shades of gray map is shown in Figure 10. Figure 11 shows the same map in a non-shades of gray presentation. Comparison of the two figures shows the desirability of having the shades of gray capability for elevation interpretation. Figure 12 shows a partially updated map.
Figure 4. Contour map

Figure 5. Contour map
Figure 6. Alphanumeric and typical symbology

Figure 7. Alphanumeric and typical symbology
Figure 8. Alphanumerics and typical symbology

Figure 9. Alphanumerics and typical symbology
Figure 10. Shades of gray map

Figure 11. Non-shades of gray presentation
The shades of gray was also converted to a color presentation by a simple color generator\textsuperscript{2} which takes the four gray levels, mixes and sums them into three color levels for use in a 3-gun television monitor. The color presentation is a further improvement over the black and white display.

7. FABRICATION

The converter was fabricated with off-the-shelf digital integrated circuits and 4 by 256 bit static ROD RAM memory integrated circuits. The electronic components were mounted on 21 printed circuit boards which plugged into a printed circuit mother board. A fan provides cooling air since the memory circuits are rated at 70-degrees centigrade.

Originally destined to be a laboratory model, the packaging was done conservatively to provide for future modifications. It was later ruggedized for airborne use and is, therefore, larger (10 by 16 by 26) than need be. Figure 13 shows the completed converter.

8. CONCLUSIONS

All of the original design goals were met and the converter has been performing satisfactorily for several months in the laboratory.

Figure 13. Completed converter
The use of static MOS RAM memory circuits permitted a very straightforward memory organization, although not necessarily the most compact.

The shades of gray and color capability greatly enhances the display in the contour map mode and is a desirable feature.

9. FUTURE PLANS

The present model of the converter will be undergoing flight test evaluation in the near future.

A second model which will have eight shades of gray and a resolution of 512 by 512 bits is in the early design stage. It will also incorporate a built-in symbol generator and will be microprocessor controlled.

10. ACKNOWLEDGEMENTS

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