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ENGINEERING DESIGN HANDBOOK

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ENGINEERING DESIGN HANDBOOK
RELIABLE MILITARY ELECTRONICS

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LIST OF SYMBOLS

SYMBOL	-DEFINITION
<i>A</i>	Arbitrary constant
<i>b</i>	Ratio of electron mobility to hole mobility
b_i	Input susceptance
b_i'	Input susceptance, intrinsic transistor
<i>B</i>	Susceptance
<i>C</i>	Capacitance
<i>C</i>	Modified capacitance for Clapp oscillator
C_0, C_1, C_2, C_3, C_4	Orthogonal coefficients
C_{0c}, C_{2c}	Corrected orthogonal coefficients
C_{20}	Fixed capacitance
C_{21}	Capacitance change per unit voltage
C_{40}	Fixed capacitance
C_{41}	Capacitance change per unit voltage
C_{be}	Base-emitter capacitance
C_c	Collector capacitance
C_{cb}	Junction capacitance—base to collector
$C_{e0}, C_{e1}, C_{e2}, C_{e3}, C_{e4}$	Orthogonal static coefficients
C_i	Input capacitance of transistor
C_{k0}, C_{k1}, C_{k2}	Orthogonal small-signal coefficients
C_n	Neutralizing capacitance
C_o	Output capacitance of transistor
C_p	Primary capacitance
C_s	Secondary capacitance
C_t	Specific temperature change, degrees/watt
C_C	Capacitance across coupling inductance
C_D	Diffusion capacitance
C_{Ln}	Negative limit contour
C_{Lp}	Positive limit contour
C_S	Standard capacitance
C_T	Transition capacitance
<i>D</i>	Denominator function
<i>D</i>	Percentage distortion
<i>D</i>	Denominator function
<i>e</i>	Electron charge
<i>E</i>	Electron energy in electron-volts
E_g	Gap energy width
E_F	Fermi electron energy
<i>f</i>	Frequency
f_1	Minimum operating frequency, transformer amplifier
f_{2a}	Transformer resonant frequency
f_{2a}'	Transformer resonant frequency
<i>A b</i>	Transformer resonant frequency
f_{2c}	Transformer resonant frequency
f_{max}	Maximum oscillation frequency, transistor
f_{n1}	Lower noise corner frequency

LIST OF SYMBOLS (Continued)

SYMBOL	DEFINITION
f_{n2}	Upper noise corner frequency
f_T	Gain-bandwidth product frequency
f_α	Alpha cutoff frequency
f_β	Beta cutoff frequency
$F(E)$	Fermi distribution function
g	Conductance
g_{11}	Input conductance
g_{12}	Reverse conductance
g_{21}	Forward conductance
g_{22}	Output conductance
g_4	Conductance
g_{bc}'	Feedback conductance, Giacoletto config.
g_{be}'	Input conductance, Giacoletto config.
g_c	Modified output conductance or h_o
g_{ca}	Average value of g_c
g_{ce}	Output conductance, Giacoletto config.
g_{cn}	Negative limit value of g_c
g_{cp}	Positive limit value of g_c
g_{cs}	Static value of g_c
g_f	Forward conductance
$g_f'_{\max}$	Maximum value of g_f'
g_{fa}	Average value of g_f
g_{fn}	Negative limit value of g_f
g_{fp}	Positive limit value of g_f
g_{fs}	Static value of g_f
g_i	Input conductance
g_i'	Intrinsic input conductance
$g_i'_{\max}$	Maximum value of g_i'
g_{i0}, g_{i1}, g_{i2}	Values of input conductance
g_{ia}	Average value of input conductance
g_{in}	Negative limit value of input conductance
g_{ip}	Positive limit value of input conductance
g_{is}	Static value of input conductance
g_m	Transconductance, Giacoletto config.
g_m'	Effective transconductance, FET, with source degeneration
$g_{m\max}$	Maximum transconductance
$g_{m\min}$	Minimum transconductance
g_{m1}	Control grid transconductance
g_{m2}	Screen grid transconductance
g_o	Output conductance
g_{oa}	Average value of output conductance
g_{on}	Negative limit value of output conductance
g_{op}	Positive limit value of output conductance
g_{os}	Static value of output conductance
g_p	Plate conductance
g_r	Reverse conductance
g_{Dp}	Diffusion conductance— p -type material
G	Conductance parameters
G_d	Shunt input conductance

LIST OF SYMBOLS (Continued)

SYMBOL	DEFINITION
h	Planck's constant
h_{11}	Input hybrid parameter
h_{12}	Reverse hybrid parameter
h_{21}	Forward hybrid parameter
h_{22}	Output hybrid parameter
h_f	Forward hybrid parameter
h_{fb}	Common-base forward hybrid parameter
h_{fc}	Common-collector forward hybrid parameter
h_{fe}	Common-emitter forward hybrid parameter
h_i	Input hybrid (impedance) parameter
h_{ie}	Input hybrid parameter with RF emitter
h_o	Output hybrid (admittance) parameter
h_{ob}	C-B output hybrid parameter
h_{oc}	C-C output hybrid parameter
h_r	Reverse hybrid parameter
h_{rb}	C-B reverse hybrid parameter
h_{rc}	C-C reverse hybrid parameter
H	Hybrid parameters
i_b	Small-signal base current
i_c	Small-signal collector current
i_e	Small-signal emitter current
i_f	Current in feedback resistor
i_i	Input current
i_o	Output current
i_s	Source current
i_B	Instantaneous total base current
i_C	Instantaneous total collector current
i_E	Instantaneous total emitter current
i_L	Instantaneous total load current
i_O	Instantaneous total output current
i_S	Instantaneous total source current
I_b	Base current, Ebers-Moll equation
I_{b1}	Base current component, Ebers-Moll equation
I_{B2}	Base current component, Ebers-Moll equation
I_{ba}	Average base current
I_{bm}	Base current for maximum collector dissipation
I_{bn}	Negative limit base current
I_{ba}	Base current component, Ebers-Moll equation
I_{bp}	Positive limit base current
I_{bt}	Saturation base current
I_{bz}	Base current when $I_{co} = i_C = -I_{bz}$
I_c	Collector current, Ebers-Moll equation
I_{cmax}	Maximum collector current
I_{c1}	Collector current component, Ebers-Moll equation
I_{ca}	Average collector current
I_{cm}	Collector current for maximum dissipation
I_{cn}	Negative limit collector current
I_{co}	Collector current component, Ebers-Moll equation
I_{cp}	Positive limit collector current

LIST OF SYMBOLS (Continued)

SYMBOL	DEFINITION
I_{cr}	Peak dynamic collector current
I_{c1}	Peak collector current on static load line
I_{cz}	Collector nominal cutoff current I_{co}
I_d	Drain current
I_e	Emitter current
I_{ea}	Average emitter current
I_{em}	Emitter current for maximum collector dissipation
I_{en}	Negative limit emitter current
I_{ep}	Positive limit emitter current
I_{ez}	Emitter current (zero value) minimum i_C condition
I_n	Negative limit current
I_{oa}	Average output current
I_{om}	Output current for peak dissipation
I_{on}	Negative limit output current
I_{op}	Positive limit output current
I_{oz}	Output current at collector cutoff
I_p	Positive limit current
I_s	Static current value
I_{sa}	Average source current
I_{sm}	Source current at peak dissipation
I_{sn}	Negative limit source current
I_{sp}	Positive limit source current
I_{sz}	Source current at collector cutoff
I_t	Total current in cross-coupling network
I_B	Base current
I_B	DC value of base current
I_{B1}	Instantaneous base current, condition 2
I_{B1}	Instantaneous base current, condition 1
I_{BM}	Maximum value of signal base current
I_C	Collector current
I_C	DC value of collector current
I_{CM}	Maximum value of signal collector current
I_E	DC value of emitter current
I_{EM}	Maximum value of signal emitter current
I_O	DC output current
I_{OM}	Maximum value of signal output current
I_S	DC source current
I_{SM}	Maximum value of signal source current
j	Imaginary operator for shifting phase by 90 deg
k	Boltzmann's constant
k	Arbitrary constant
k	Coefficient of coupling for inductors
k	Ratio $I_b(R_i + R_L)/V_{CC}$
k_0	Nominal amplification for mixer = $0.5 g_{f'_{\max}} R_L$
k_c	Critical coupling coefficient
K	Amplification
K_0, K_1, K_2	Legendre gain coefficients
K_a	Average amplification
K_f	Feedback voltage gain
xx	

LIST OF SYMBOLS (Continued)

SYMBOL	DEFINITION
K_i	Current gain
K_{\max}	Maximum amplification
K_{\min}	Minimum amplification
K_n	Negative limit amplification
K_p	Positive limit amplification
K_s	Static amplification value
K_v	Voltage amplification
K_v	Forward amplification with feedback
K_v'	Modified forward amplification with feedback
K_{vr}	Voltage gain at reference frequency
K_L	Loop gain with feedback
K_S	Total stage amplification, R F amplifier
L	Inductance
L'	Inductance modified by capacitor in Clapp oscillator circuit
L_1	Primary inductance
L_2	Secondary inductance
L_2, L_3	Oscillator inductances
L_{eff}	Effective inductance
L_n	Electron diffusion length
L_n'	Electron diffusion length, collector region
L_p	Hole diffusion length
L_C	Inductance of coupling coil
L_{C1}	Effective inductance in presence of C_C
L_L	Leakage inductance
L_T	Total inductance
m	Mass of electron
m	Has value $0.5 g_1'_{\max} Z_s$
m_e^γ	Electron mass near edge of conduction band
m_h^γ	Hole mass near edge of valence band
M	Mutual inductance
n	Number of electrons per unit volume
n	Exponent
n	Order of orthogonal polynomial
n_e	Number of electrons per unit volume
n_{eff}	Effective number of electrons per unit volume
n_h	Number of holes per unit volume
n_i	Number of thermally generated carriers per Unit volume
n_i	Input turns
n_{iG}	Thermally generated carriers per unit volume in germanium
n_{iS}	Thermally generated carriers per unit volume in silicon
n_n	Number of electrons in n-type material
n_o	Output turns
n_p	Number of electrons in p-type material
n_p	Primary turns
n_s	Secondary turns
p_i	Number of thermally generated holes per unit volume
p_n	Number of holes in n-type material

LIST OF SYMBOLS (Continued)

SYMBOL	DEFINITION
p_p	Number of holes in ptype material
pF	Picofarads or $\mu\mu\text{F}$
P_c	Collector power dissipation
Q	Tuned circuit @factor
Q	Quiescent point or static point
Q_a	Quiescent point "a"
Q_b	Quiescent point "b"
Q_c	Q -factor for coupling circuit
Q_{rs}	@factor of parametric amplifier at its idler frequency
Q_s	Q -factor of parametric amplifier at its signal frequency
Q_s	Stored charge
Q_t	Unloaded tuned Q -factor
Q, R, S, T	Matrix relations of arbitrary and independent variables
r_b	Base resistance
$r_{bo'}$	r_b at reference temperature T_o
r_c	Collector resistance
r_d	Resistance in Tee representation
r_i	Input resistance
r_m	Mutual resistance
R	Resistance component
R'	Resistance
R_1, R_2, R_3	Resistances
R_b	Base resistance
R_{bc}	Feedback resistance
R_{c1}	Collector load resistance
R_{c2}	Collector load resistance (feedback)
$R_e, R_{e0}, R_{e1}, R_{e2}, R_{e3}$	Emitter resistances
R_n	Neutralizing resistance
R_s	Source resistance
R_x	Base-return resistance (unknown)
R_{CC}	Collector supply resistance
R_L	Load resistance
R_{L1}, R_{L2}	Specific load resistances
R_{LD}	Dynamic load resistance
R_S	Standard resistance
R_S	Resonant resistance
Re	Real part of
S_c	$\partial i_c / \partial I_{co} + 1$
S_{c1}	$\partial i_c / \partial I_{co} + 1$
$S_{c1'}$	$\partial i_c / \partial v_{b'}$
S_c	$\partial i_c / \partial I_{co}$
S_e'	$\partial i_c / \partial v_{b'}$
t	Ratio of R_{LD}/R_L
t_f	Fall time
t_r	Rise time
t_s	Storage time
T	Absolute temperature
T	Set of network trees
T	Time constant
$2-T$	Set of network two-trees

LIST OF SYMBOLS (Continued)

SYMBOL	DEFINITION
T_o	Reference temperature
u	Arbitrary dependent variable
U	Unilateral gain
v	Arbitrary dependent variable
v_b	Signal component of base voltage
v_c	Signal component of collector voltage
v_e	Signal component of emitter voltage
v_{eb}	Signal component, emitter-base voltage
v_i	Input voltage, signal component
v_o	Signal component of output voltage
v_s	Signal component of source voltage
v_s	Signal voltage
v_B	Instantaneous total base voltage
v_C	Instantaneous total collector voltage
v_E	Instantaneous total emitter voltage
v_F	Fermi drift velocity
v_O	Instantaneous total output voltage
v_S	Instantaneous total source voltage
V	Voltage
V	Internal trees of network
V_b	Instantaneous plate voltage
V_{ba}	Average base voltage
V_{bm}	Base voltage at maximum dissipation
V_{bn}	Negative limit base voltage
V_{bp}	Positive limit base voltage
V_{bt}	Base voltage for saturation
V_{bz}	Base voltage for collector cutoff
V_c	Instantaneous grid voltage, collector voltage
V_{ca}	Average collector voltage
V_{cb}	Collector-to-base voltage
V_{cm}	Collector voltage at maximum dissipation
V_{cn}	Negative limit collector voltage
V_{cp}	Positive limit collector voltage
V_{csat}	Collector saturation voltage
V_{ct}	Saturation collector voltage
V_{cz}	Collector voltage at cutoff
V_{ea}	Average emitter voltage
V_{em}	Emitter voltage at maximum dissipation
V_{en}	Negative limit emitter voltage
V_{ep}	Positive limit emitter voltage
V_{ez}	Emitter voltage at cutoff
V_g	Gate voltage, field-effect transistor
$V_{EB}^{(j)}$	Base terminal voltage
V_n	Negative limit voltage
V_{oa}	Average output voltage
V_{on}	Negative limit output voltage
V_{op}	Positive limit output voltage
V_{oz}	Output voltage at cutoff
V_p	Positive limit voltage

LIST OF SYMBOLS (Continued)

SYMBOL	DEFINITION
V_{sa}	Average source voltage
V_{sn}	Negative limit source voltage
V_{sp}	Positive limit source voltage
V_{sz}	Source voltage at cutoff
V_B	Applied bias voltage
V_B	Static value of base voltage
V_{BB}	Plate supply voltage
V_{BB}	Base supply voltage
V_{B10}	Plate voltage at essentially zero grid bias
V_{BM}	Maximum value of base signal voltage
V_C	Applied collector voltage
V_C	Static value of collector voltage
V_{CC}	Plate supply voltage for equivalent ideal transistor
V_{CC}	Collector supply voltage
V_{CM}	Maximum value of collector signal voltage
V_E	Static value of emitter voltage
$V_{EB'}$	Base voltage at base-emitter junction under high-injection conditions
V_{EE}	Emitter supply voltage
V_{EM}	Maximum value of emitter signal voltage
V_O	Static value of output voltage
V_{OM}	Maximum value of output signal voltage
V_{OO}	Output circuit supply voltage
V_S	Static value of source voltage
V_{SM}	Maximum value of source signal voltage
V_{SS}	Source supply voltage
$W_{i,o}^{i,o}$	Driving-point two-trees
$W_{i,o}^{i,o}$	Transfer two-trees
W_o	Power input
x	Arbitrary independent variable
x_s	Current ratio variable
X	Arbitrary source vector
X_L	Reactance component
X_L	Load reactance
X_O	Link reactance
y	Arbitrary independent variable
y	Source-sink admittance
y_{11}	Input admittance
y_{12}	Reverse transfer admittance
y_{21}	Forward transfer admittance
y_{22}	Output admittance
y_c	Modified output admittance = h_o
y_{ca}	Average modified output admittance
y_{cn}	Negative limit value, y_c
y_{cp}	Positive limit value, y_c
y_{cs}	Static value, y_c
y_f	Forward admittance
y_f'	Intrinsic forward admittance
y_{fa}	Average value of forward admittance

LIST OF SYMBOLS (Continued)

SYMBOL	DEFINITION
y_{fn}	Negative limit value of forward admittance
$y_{fo'}$	Forward admittance at reference temp.
y_{fp}	Positive limit value of forward admittance
y_{fs}	Static value, forward admittance
y_i	Input admittance
y_i'	Intrinsic input admittance
y_{ia}	Average input admittance
y_{in}	Negative limit input admittance
$y_{io'}$	Input admittance at reference temp.
y_{ip}	Positive limit input admittance
y_{is}	Static value, input admittance
y_o	Output admittance
y_{oa}	Average output admittance
y_{on}	Negative limit output admittance
y_{op}	Positive limit output admittance
y_{os}	Static value output admittance
y_r	Reverse transfer admittance
y_r	Feedback admittance
y_r	Reference source-sink signal admittance
y_u	Equivalent total feedback admittance
Y	Y parameters
Y_0, Y_1	Coefficients of power-series expansion of admittance function
Y_0, Y_2, Y_4, Y_6	Shunt admittance elements of ladder network
Y_1, Y_2, Y_3, Y_4	Admittances
Y_1, Y_3, Y_5	Series admittance elements
Y_{cp}	Primary-side shunt capacitive admittance
Y_{cs}	Secondary shunt capacitive admittance
Y_f	Overall forward admittance
Y_{fa}	Overall average forward admittance
Y_{fn}	Overall negative-limit value Y_f
Y_{fp}	Overall positive-limit value Y_f
Y_{fs}	Overall static value Y_f
Y_i	Overall input admittance
Y_{max}	Maximum value of admittance Y
Y_{min}	Minimum value of admittance Y
Y_{pm}	Primary magnetizing admittance
Y_{sm}	Secondary magnetizing admittance
Y_t	Admittance equal to $1/(r_b' + R_s)$
Y_T	Transfer admittance
z	Turns-ratio, n_s/n_p
z_{11}	Input impedance
z_{12}	Reverse impedance
z_{21}	Forward impedance
z_{22}	Output impedance
z_{23}	Mutual impedance
z_{32}	Mutual impedance
z_f	Forward impedance
z_{fb}	Forward impedance C-Base

LIST OF SYMBOLS (Continued)

SYMBOL	DEFINITION
Z_{fc}	Forward impedance C-Collector
Z_i	Input impedance
Z_{ib}	Input impedance C-Base
Z_{ic}	Input impedance C-Collector
Z_o	Output impedance
Z_o	Output impedance
Z_{ob}	Output impedance C-Base
Z_{oc}	Output impedance C-Collector
Z_r	Reverse impedance
Z_{rb}	Reverse impedance C-Base
Z_{rc}	Reverse impedance C-Collector
Z	Relative impedance level
Z	Z_i parameters
Z_1, Z_3, Z_5, Z_7	Series impedances, ladder network
Z_2, Z_4	Impedances of network
Z_e	Emitter impedance
Z_i	Input impedance
Z_j	Terminal impedance
Z_r	Total impedance in reference circuit
Z_r	Impedance at reference frequency
Z_s	Source impedance ("spreading resistance")
Z_L	Load-circuit impedance
Z_{LD}	Tuned or untuned load impedance
Z_O	Crystal impedance
Z_T	Transfer impedance
α	Current gain
α	Arbitrary source parameter
α_I	Reverse current gain
α_N	Forward current gain
β	Current gain
β	Proportionality factor
γ	Multiplication factor $0 < \gamma < 1$
γ_c	Current increment $\partial I_{co} / \partial T$
$\gamma(h)$	Hybrid factor $= 1 + h_f - h_r + \Delta(h)$
δ	Number $\ll 1$
Δ_L	Arbitrary single parameter
Δf_o	Frequency increment
Δg_c	Total change in g_c
Δg_f	Total change in g_f
Δg_i	Total change in g_i
$\Delta g_i'$	Total change in g_i'
Δg_o	Total change in g_o
$\Delta(h)$	Value is $h_i h_o - h_f h_r$
Δi_b	Base current change
Δi_b	Base current change
Δi_c	Collector current change
Δi_c	Emitter current change
Δi_o	Output current change
Δi_s	Source current change

LIST OF SYMBOLS (Continued)

SYMBOL	DEFINITION
ΔI_{co}	Change in I_{co}
ΔK	Change in amplification
ΔK_{σ}	RMS change in K in oscillator
ΔP_c	Change in collector dissipation
ΔT	Change in temperature
Δv_b	Base voltage change
Δv_c	Collector voltage change
Δv_e	Emitter voltage change
Δv_o	Output voltage change
Δv_s	Source voltage change
ΔV_{neg}	Negative voltage change from static
ΔV_{pos}	Positive voltage change from static
$\Delta(y)$	Value is $y_i Y_o - y_f y_r$
Δy_c	Change in y_c
Δy_f	Change in y_f
Δy_i	Change in y_i
Δy_o	Change in y_o
$\Delta(z)$	Value is $z_i z_o - z_f z_r$
$\Delta \omega$	Radian frequency increment
$\Delta \omega_o$	Radian frequency increment
κ	Efficiency factor
κ_1	Control grid efficiency factor
κ_2	Screen grid efficiency factor
λ_F	Mean-free-path
A	$A = q/(kT)$
μ	Triode amplification factor
μ_{12}	Control grid to screen amplification factor
σ	Conductivity
σ_i	Intrinsic conductivity
σ_n	n-type conductivity
σ_p	p-type conductivity
σ_p'	Collector p-type conductivity
$\sigma(g)$	$g_i + g_f + g_r + g_o$
$\sigma(R)$	Summation $r_b' + R + R_c$
σR	Summation $r_b' + R + R_L$
$\sigma(y)$	$y_i + y_f + y_r + y_o$
$\sigma(z)$	$z_i - z_f - z_r + z_o$
τ_p	Lifetime in PNP transistors (minority carriers)
τ_F	Relaxation time
ϕ'_{ab}	"Contact" or barrier potential
ω	Radian frequency
ω_0	Ladder oscillator radian frequency
ω_1	Nominal R - C radian frequency ($\omega_1 RC = 1$)
ω_a	Roll-off radian frequency knee, emitter follower
ω_b	Level-off radian frequency knee, emitter follower
ω_o	Nominal resonant radian frequency
ω_r	Reference radian frequency, parametric amplifier
ω_{rs}	Idler radian frequency, parametric amplifier
ω_s	Signal radian frequency, parametric amplifier

FOREWORD

This book was originally published by Prentice-Hall under the title *Handbook of Transistor Circuit Design*. Its author, Dr. Keats A. Pullen, Jr., of the Ballistic Research Laboratories, Aberdeen Proving Ground, selected as his goal the presentation of a unified approach to the design of reliable transistor circuits, and also the presentation of an approach that based the design on fundamental properties capable of rather precise specification. Experience based on the developed techniques has proved that the approach was uniquely oriented to serve as an aid to the design of reliable circuits.

More recent experience has shown that the ideas developed in the book had a much broader scope than was originally conceived, and, with certain modifications, the described procedures can help the reader and user to increase potential reliability of circuits based on the improved understanding by as much as an order of magnitude or more. In addition, the techniques are equally applicable to field-effect transistors (FET's) and other active devices.

In the original edition, the first few chapters were included to provide the junior reader with a brief review of the physics of transistor operation. With this new edition, the review material is being condensed substantially, and new material having more direct applicability to reliability physics is developed. The scope is also enlarged through the inclusion of some largely new material bearing on the operating theory and properties of field-effect transistors of both the diode and the insulated-gate varieties.

The nature of the fundamental physical limitations for devices which affect the design of circuits is of particular importance to the applications specialists, because these kinds of limitations have a way of keeping designers from reaching a desired goal. One such limitation, which we shall call the gain-power limitation, has been responsible for the fact that the output power per transistor available from tuned class C amplifiers has remained at approximately 50 W for the past decade in spite of the predictions commonly publicized ten or so years ago. A revised Chapter 3 is reserved to the consideration of these limitations.

The chapters dealing with circuit design procedures and those in which the basic algebraic relations are developed present material that can be applied to field-effect transistors as well as to the more common bipolar types. In addition, as indicated, with relatively small changes the same techniques can be applied equally well to the design of electron tube circuits. In all of these applications, one of the most vital steps in optimization of the design is to redesign to find the minimum supply voltages (particularly for the collector) which produce required conditions of operation. It should **never** be forgotten that a base-junction voltage change of **less than a quarter of a volt** can change device collector current by **one thousand times**.

One of the important considerations in any circuit design problem is having the proper information available to enable the designer to obtain a reliable circuit. The development of the required information on characteristics and parameters, and the ordering of them in the most useful form is often called "information engineering". The techniques of information engineering are used extensively in the handbook, although this usage is largely implicit. A new appendix, Appendix H, has been added in which a discussion of the basic principles of information engineering is included for the use of the reader. An additional new appendix, Appendix I, also has been added in which the Fermi or diffusion mode of operation of field-effect transistors is described briefly.

PREFACE

The word “handbook” is defined in *Webster's New Collegiate Dictionary* as “a manual; a guidebook”. In the engineering and scientific fields, a handbook is understood to be a book containing a relatively brief but thorough and complete exposition of a given subject or group of subjects.

Based on the above definitions, this Handbook is a handbook in the dictionary sense, and, in fact, it is more than a handbook. It might be called a “reliability” handbook inasmuch as it is a guidebook to a systematized approach to the design of circuits using active devices under conditions of minimum dissipation. It is a handbook also in the sense that information on related science, which has proven useful in the design of reliability into circuits for active devices, has been included. Several of the techniques, notably the topological method and the orthogonal handling of nonlinearities, have been developed to provide a higher degree of usefulness than previously had been available.

The orientation of this handbook is in one sense practical and in another sense analytic. It is practical in that it gives design procedures which can significantly improve the potential reliability of transistor circuits. These procedures are coordinated and consistent with one another, and they are selected in a way that takes advantage of the more stable properties of the active devices.

This handbook is analytic in the sense that the methods used are subjected to considerable mathematical and scientific scrutiny prior to adoption and also because a considerable body of analytic procedure not previously applied extensively in electronics is utilized for improving the finally resulting circuits. The use of organization procedures for characteristic data of semiconductor devices leads to a better understanding of the devices themselves, and it also leads to more efficient design procedures. Likewise, the use of topological methods of analysis of sections of circuits makes possible coordination of relatively complex subnetworks in the synthesis of circuits to specified characteristics.

The first chapter contains a descriptive review of the properties of conductors, semiconductors, and insulators and develops the conductivity and mechanical relations required for generation of diode and transistor action. It is followed by a chapter on the theory of specification of data for devices, the chapter leading to establishment of the parameters and the variables used in this handbook.

The third chapter discusses methods of measurement of the properties established as important in transistors and related devices. Many useful measurement techniques are described. The following chapter includes derivations of the basic operating equations for typical operating configurations and develops many of the significant relations among the standard representations.

In addition to the main chapters, the Handbook contains an extensive table of symbols and definitions and a series of nine appendices discussing important peripheral questions such as the derivation of small-signal distortion equations—both through the use of trigonometric relations and orthogonal input-output relations—considerations on elliptical load contours, and topological equation derivations. An extensive bibliography is reproduced from the Prentice-Hall edition, and an extensive set of typical

characteristic curves on bipolar transistors also is included. The remaining appendices include a convenient nomograph for solving the transistor gain/admittance equations, and two additional appendices, one dealing with the principles of information engineering, and the other with the significance of the Fermi limitation on the operation of field-effect transistors.

The Engineering Design Handbooks fall into two basic categories—those approved for release and sale, and those classified for security reasons. The US Army Materiel Command policy is to release these Engineering Design Handbooks in accordance with current DOD Directive 7230.7, dated 18 September 1973. *All* unclassified Handbooks can be obtained from the National Technical Information Service (NTIS). Procedures for acquiring these Handbooks follow:

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CHAPTER 1

BASIC PRINCIPLES

1-0 PURPOSE OF THIS HANDBOOK

The principal objective of this handbook is to develop and describe a systematic method of design of transistor circuits. This method is capable of providing reasonably accurate results quickly and easily. In accomplishing this purpose, however, it is desirable to include a limited amount of theory of the behavior of the devices in their circuits in order to clarify the reasons for some of the design procedures. Because of the relative confusion in the semiconductor field over the choice of variables and parameters, and because of the sketchiness of the tabular data on the parameters, it also appears desirable to discuss briefly some of the simpler measurement techniques that can be used by the circuit designer for checking the properties of active devices.

The casual reader of the table of contents might think that including material on such subjects as symbology, topology, orthogonal polynomials, appropriate choice of variables and parameters, selection of the common electrode, methods of measurement, and the best form of network configuration represents an unnecessary digression from the major purpose of this volume. Review of the wide variety of approaches to circuits appearing in articles, papers, and textbooks, however, shows that the subject of circuit design for transistors contains many contradictions. It is for this reason that an effort must be made to establish a single consistent system of design that includes the most important individual techniques as limiting cases. Such a system can be useful and helpful to the practical designer because it makes unnecessary the use of a variety of alternative methods that for one reason or another may be of limited applicability.

The system of design described in this book has other important advantages that may not be immediately obvious. For example, the characteristics of operation of a circuit can be analyzed by the described method to the extent that a considerable part of the experimental test time usually required in the laboratory becomes unnecessary. As a consequence, the reliability of operation obtained is such that appreciably less coordination

time may be required to obtain unified operation of the complete system. The objective of the first four chapters is to develop the techniques and procedures required with this systematized approach.

After the basic information problems have been evaluated, the subject of the subsequent four chapters is the design and the stabilization of simple circuits. Chapter 5 considers the design of four basic configurations:

1. Common-emitter amplifiers
2. Common-base amplifiers
3. Common-collector amplifiers
4. Degenerative-emitter amplifiers.

Chapter 6 discusses the stabilization problem, the problem of keeping the transistor operating properly over a range of both ambient temperature and power dissipation. Following this chapter on stabilization, attention is next directed to transformer-coupled amplifiers, and the design of a variety of types of these amplifiers is considered. Transformer-coupled transistor amplifiers are much more important than their tube counterpart because the use of a transformer with a transistor may permit reduction of the total circuit power input by a factor of two or three as compared with a few percent change in the sum of heater and plate power input if a transformer-coupled tube circuit is used. The final chapter in this group, Chapter 8, considers the design of RF and IF amplifiers, including also a discussion of the problem of automatic control of gain.

The next three chapters examine the fundamental principles of operation of different types of oscillators, examining in particular the problem of initiation and build-up of oscillation. The first chapter of the group discusses the mathematics of relatively linear feedback networks. The second applies the theory to *L-C* oscillators, and the third develops the theory for use with *R-C* oscillators.

In Chapter 12, the theory and design of mixers and converters are considered and the relation of their behavior to the characteristics of oscillators and am-

plifiers studied. The use of parametric amplifiers and tunnel diodes is also discussed.

In Chapters 13 and 14 the design of circuits having high degrees of nonlinearity, such as multivibrators and counting circuits, is analyzed. The objective in both these chapters is to provide a systematic approach that gives as complete a picture of the behavior of typical circuits as is possible. Likewise, design procedures are considered in detail.

Such material as is available on tunnel diodes at the time of writing is being included in appropriate sections of this book. In particular, some notes on the measurement of the current-voltage relation and the negative conductance of the device is explained in Chapter 3, some comments on the use of the devices as amplifiers in Chapter 8, some notes on mixer applications in Chapter 12, and bi-stable applications in Chapter 14.

Because of the breadth of coverage of the material in this book, it of necessity cannot be a textbook but must build to a considerable extent on other documents. For this reason an extensive list of bibliographical references is included. References to particularly important papers include a brief synopsis of the content. Two general references that might be noted separately are *Conductance Design of Active Circuits* (Ref. 1), and Chapter 12 of *Radio Engineering Handbook*, edited by Henney (Ref. 2). These references indicate some of the more fundamental procedures in greater detail than they can be recounted here. The first of these gives considerable detail information on the application of similar techniques to tube circuit design, and shows how the additional data can be used to enhance reliability and efficiency.

1-1 PROPERTIES OF CONDUCTORS

Solid materials can be separated into three different classes, namely, conductors, insulators, and semiconductors. The group of conductors includes largely the metals having valences one, two, and three. All of these materials have large numbers of free electrons for conduction of electric currents. In terms of the valence and conduction bands, this means that at normal or room temperature there are available unoccupied energy positions to which the electrons can move with only very small increments of applied energy. In terms of the theory of quantum energy states, at the temperature of absolute zero, there is a group of states all of which are occupied, and there is a higher energy group of states all of which are vacant. As the temperature of the material is gradually increased a few of the states occupied at absolute zero become unoccupied, and the

electrons that occupied them move into some of the higher energy states. As a consequence, as is shown in Fig. 1-1, whereas the probability of occupancy of any given energy state at absolute zero temperature is either unity or zero, as the temperature is increased the probability of occupancy of any one given state near the edge of the nominally occupied area may decrease to a value as small as one-half, and the probability of occupancy of a state in the nominally unoccupied area may rise to as much as one-half.

Now, the curves in Fig. 1-1 imply that there is a continuous distribution of possible energy states available in the conductor. Actually, although there may be a very great number of possible states available over the range, there actually is a finite number of them, and they are located at finitely spaced increments from one another. In addition, there are actually ranges of energy, or energy bands, for any given material in which there are no occupiable states for the electrons at all. These areas may be difficult to find in a material whose atoms are not arranged in an orderly fashion (such a material may be called an amorphous or a polycrystalline material) because such a disorder introduces distortion into the fields around the individual atoms, and may thereby introduce spurious levels. These additional levels are sometimes called trapping levels.

Materials that have a high electrical conductivity are ones in which the boundary between the occupied and the unoccupied states (commonly called the Fermi potential) falls in one of the bands having closely spaced possible energy levels. In these materials the removal of an electron from an occupied state to a previously unoccupied state requires very little energy, and as a result, the normal variation of energy from atom to atom and from electron to electron, as a consequence of thermal probability distributions, is sufficient to provide for the required transfer energy. Ample quantities of conduction electrons are therefore available in any material in which the Fermi potential falls within one of the bands of permitted energy levels (Fig. 1-2).

As the temperature of any material is increased from room temperature, the distribution of probability of occupancy changes as indicated in Fig. 1-3, and the conductivity of conductors changes as a consequence. A relatively reduced slope of the probability contour across the conduction band results, and the lattice vibrations of the molecules increase, increasing the effective area of the lattice atoms and decreasing the mean-free-path of the electrons and also their relaxation time. This effect reduces the conductivity of a conductor but may increase the conductivity of semiconductors.

The interference of the lattice with the passage of electron waves through a conductor depends to a large

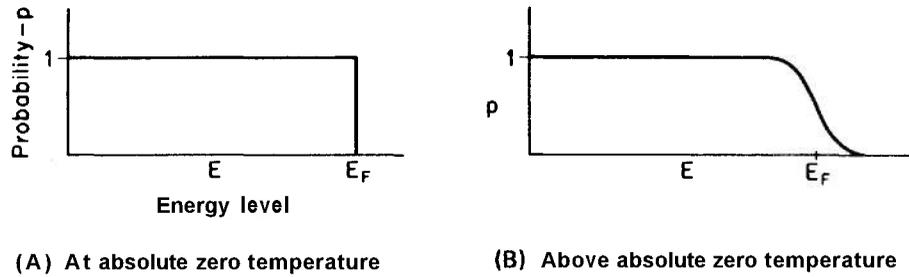


Fig. 1-1. Fermi Energy Distribution

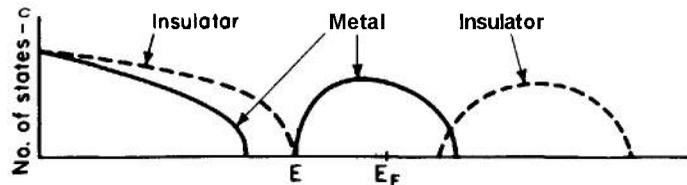


Fig. 1-2. Distribution of Occupation States

extent on the irregularity of the structure, because it has been shown that under ideal conditions an electron can traverse approximately a hundred atomic distances between collisions. Consequently, in a work-hardened crystalline material such as copper wire, the irregularities resulting from movement of crystal groups with respect to one another decreases the mean-free-path, thereby decreasing the conductivity, which is given by the equation*

$$\sigma = ne^2\tau_F/m = n_{eff}e^2\tau_F/m \quad (1-1)$$

where τ_F is the relaxation time of electrons having energy corresponding to the Fermi potential, \leftrightarrow is the

conductivity, n (or n_{eff}) is the effective number of electrons per unit volume, e is the electronic charge, and m is the mass of the electron. The relaxation time is related to the mean-free-path λ_F and the Fermi drift velocity v_F in accordance with the equation

$$\tau_F v_F = \lambda_F \quad (1-2)$$

The magnitude of the mean-free-path is inversely proportional to the absolute temperature in degrees Kelvin, with the result that the conductivity is approximately inversely proportional to the absolute temperature.

1-2 PROPERTIES OF INSULATORS

With nonconductors, or insulators, however, the situation is quite different. Insulators are materials in which there are no available conduction electrons, because the Fermi potential falls in an energy band in which there are no occupiable electron states. In fact, the insulator has a large energy gap between the energy states possessing electrons and the lowest available unoccupied states. An electron could easily surmount the cliff possessed by the insulator if an energy-state stairway were available. The conductor in effect has such a built-in stairway for conduction electrons be-

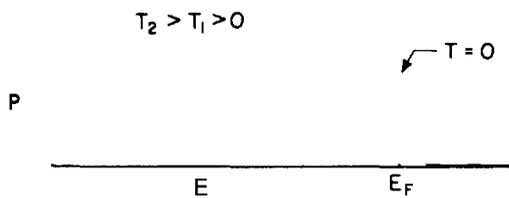


Fig. 1-3. Effect of Temperature on Energy

*Eqs. 1-1 through 1-4 are from Ref. 4. (See Equations 9-6, 11-8, and 11-32 and Problem 9-3).

tween the occupied states and the unoccupied states, and the insulator has not. As a result, in an insulator the electrons are trapped in a manner that makes it very difficult for them to break away from their individual atoms and carry an electric current.

The Fermi distribution function $F(E)$ (Refs. 3, 4), which gives the probability of any existing energy state being filled, may be stated mathematically in terms of the equation

$$F(E) = 1/[1 + \exp \langle q(E - E_F)/(kT) \rangle] \quad (1-3)$$

where E is the electron energy in electron volts, E_F is the Fermi potential, k is Boltzmann's constant, T is the absolute temperature, and q is the electron charge. For very small values of T , the exponent is either very large in magnitude and positive, or large and negative. As a result, the value of $F(E)$ is either unity or zero. As the value of T becomes larger, a gradually longer transition range develops about the value $E \approx E_F$, with the result that the transition becomes more gradual, as is shown in Fig. 1-1. For practical purposes, the number of electrons available for use in conduction is a function of the derivative of the Fermi distribution function in the neighborhood of the Fermi potential, because when the derivative is zero, either at low energy where the value of the function is unity or at high energy where it is zero, there is no possibility of making use of available energy levels. The levels are either all full or there are no electrons available.

If, therefore, a material is available in which the Fermi level occurs in the middle of a range of energy for which no permitted levels exist, and the Fermi derivative function is zero at the edges of the forbidden band, then no conductivity can develop, and the material is an insulator. The edges of the range of energy levels for conduction electrons may be determined from the derivative function

$$dF/dE = \langle 1/(kT) \rangle / [\exp \langle q(E - E_F)/(kT) \rangle + 2 + \exp \langle q(E_F - E)/(kT) \rangle] \quad (1-4)$$

Evidently, unless the value of E is nearly equal to that of E_F , or T is very large, the value of the denominator is very, very large, and the derivative is very nearly zero. In fact, if $E - E_F$ is as much as five or six kT 's, then the value of the derivative is small to the point of being negligible. Materials that are normally classed as insulators have a forbidden band between fifty and five hundred kT 's wide, with the result that if the Fermi level is properly spaced within the band,

infinitesimal numbers of electrons are available for conduction purposes at ordinary room temperature. As the temperature is increased, however, the value of kT becomes larger, and the value of the distribution function slopes off more and more gradually because of the increased value. A point is finally reached at which electrons do become available as a result of thermal action, and conduction commences. With glass, for example, the temperature at which conductivity becomes significant is in the neighborhood of 500°F. The cliff is generated by the forbidden band in the insulator, and the ladder is provided by the sloping of the distribution function. Only when the slope is sufficiently gradual to reach across the forbidden band does the insulator begin to conduct, because only then are electrons of sufficient energy available to step across the cliff.

1-3 PROPERTIES OF SEMICONDUCTORS

The semiconductor is neither a conductor nor an insulator, but it sometimes behaves like one, and sometimes like the other. At ordinary temperatures, semiconductors have a small but finite conductivity; the value may range from that of a very poor conductor, typically $\sigma = 100$ mho square centimeters per centimeter, to a value as small as 0.001 to 0.0001 mho square centimeters per centimeter, or a rather good insulator. The conductivities of first quality insulators normally are measured in micromhos or small fractions of a micromho. The range of conductivity of a semiconductor is a consequence of the narrow width of the forbidden band within which lies the Fermi potential for the material. Thermal ionization and crystal dislocations can then provide an adequate number of charged carriers to give the conductivity.

The number of conducting charges available in a pure semiconductor depends in large degree on the accuracy and uniformity of the crystallization of the semiconductor material. Every defect in the structure is a focal point for the generation of current carriers. Consequently, to be satisfactory, semiconductors used in many electronic applications are required to have an extraordinarily high order of regularity and perfection. Otherwise, a high inherent conductivity exists in the material, and it is difficult to obtain proper control of the properties of a device constructed from the material.

Certain materials when introduced into the crystal structure alter the behavior of the crystal in a manner which makes available additional carriers, and thereby increases the electrical conductivity. These materials,

or impurities, may either make additional carriers available thermally, or they may cause the release of one type of carrier alone. If, for example, a few stray atoms of tin, which crystallizes in the same form as most normal semiconductors like germanium and silicon, are introduced into the crystal, and the atoms introduced have a narrow forbidden band, then the impurity can cause rapid generation of thermal carriers. Other materials that have a different number of valence electrons from the matrix crystal provide polarized carriers when introduced into the lattice.

1-4 TYPES OF SEMICONDUCTORS

Of the wide variety of semiconductors available to the device designer, the materials of greatest overall importance are silicon and germanium. Historically, the first semiconductor used in electronics was galena, or lead sulfide; it was used as a rectifier in many early crystal radio sets. Somewhat later, the cuprous oxide rectifier was developed, making it the first extensively used intermetallic semiconductor. At a somewhat later date the selenium rectifier was developed to overcome the deficiencies of the cuprous oxide units. The next few paragraphs discuss briefly some of the semiconductor materials that are finding application in diodes and transistors, and also some of the materials that show potential for being useful when technological problems of utilizing them have been solved.

1-4.1 GERMANIUM

Germanium is a semiconductor of valence four, or one that is inherently neutral in polarity when crystallized in a tetrahedral bond arrangement. The normal crystallizing pattern for this material is the face-centered cube. Germanium has the narrowest width of forbidden band that can be used effectively in diodes and transistors, namely, approximately 0.7 V.

The rating of the width of the forbidden band in terms of volts (or electron volts) measures the energy difference across the gap or band. Potential times electron charge gives electron energy. For this reason, and because it is common practice in the field of electronics, the energy differences are given in electron volts, or volts for short.

The narrow energy gap of germanium limits the maximum temperature to which it may be used effectively as a semiconductor. As will be shown in par. 1-5, it is necessary that semiconductor materials for use in diodes and transistors be altered or doped with impurities that give them the ability to conduct by means of

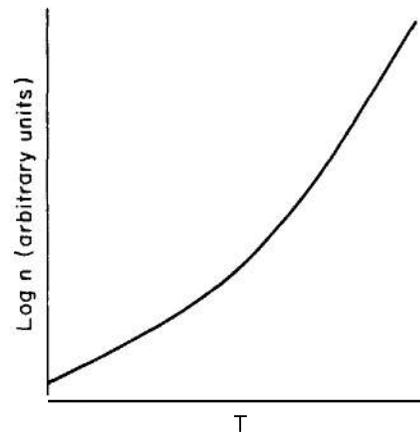


Fig. 1-4. Variation of Number of Charged Particles With Temperature

either positive or negative charges. This being the case, it is important that the conductivity due to thermal effects be kept small compared to the conductivity due to the doping materials over the range of operating temperatures. The number of conducting particles in a neutral semiconductor (single crystal) is given by the equation (12-19 from Ref. 4)

$$n_e = n_h = 2(2\pi kT/h^2)^{3/2} (m_e^* m_h^*)^{3/4} \times \exp \langle -qE_g / (2kT) \rangle \quad (1-5)$$

where n_e and n_h are the numbers of electrons and holes, respectively, k is Boltzmann's constant, T is the absolute temperature in degrees Kelvin, h is Planck's constant, m_e^* and m_h^* are the equivalent masses of the electrons and holes, near the edges of the conduction and the valence bands, respectively, and E_g is the gapwidth energy. This equation shows that the number of charged particles available is a function of the three-halves power of the temperature times an inverse temperature exponential. The value of this product increases rapidly with temperature, as is shown in Fig. 1-4.

1-4.2 SILICON

Silicon is used extensively in both standard and switching diodes and in transistors, and it has replaced germanium almost completely in the power rectifier field. Silicon has some important advantages compared to germanium, and also some important disadvantages. The first and possibly the most important advantage is

that it has a gap energy of approximately 1.2 V, or almost twice that for germanium. The second advantage is shown by the number of thermally-generated carriers in the two materials at room temperature (300°K)*

$$\begin{aligned} \text{For silicon:} \quad n_i &= 1.5 \times 10^{10}/\text{cc} \\ \text{For germanium:} \quad n_i &= 2.4 \times 10^{13}/\text{cc} \end{aligned} \quad (1-6)$$

The simplified equations for the values of n_i^2 as a function of temperature for the two materials are (Refs. 5, 6)

$$\text{Germanium:} \quad n_i^2 = 3.1 \times 10^{32} T^3 \exp(-9100/T) \quad (1-7)$$

$$\text{Silicon:} \quad n_i^2 = 1.5 \times 10^{33} T^3 \exp(-14,000/T)$$

The ratio of these two equations gives a measure of the relative change rate with temperature

$$n_{iS}^2/n_{iG}^2 = 5 \exp(-4900/T) \quad (1-8)$$

Since $\exp(7)$ is approximately equal to 10^3 (actually $e^{6.9} = 10^3$), the value of the ratio of n_{iS}^2/n_{iG}^2 at $T = 300^\circ\text{K}$ is approximately 5×10^7 . Similarly, at 400°K , the ratio has a value of 2.5×10^5 , showing that the thermal carrier concentration rises about 22 times faster in silicon than it does in germanium, but the number of charges still is a factor of 500 smaller than that in germanium at 400°K . The derivative expression also shows that the rate of increase of n_{iS}^2 is greater than that of n_{iG}^2 .

*Large energy gaps are useful in semiconductor materials principally for the reasons that a large energy gap in a material gives it an extremely small level of thermal conduction, and that a material with a large energy gap is one which can be used in a high temperature environment. A very low value of thermal base conductance in conjunction with good doping conditions in the emitter and the collector makes possible a relatively higher value of current gain, and a lower input admittance. Normally, a diffused base region, with epitaxial construction, is required to make optimum use of the low base conductivity available, and to give optimum high-frequency performance. Even though the rate of increase of conductivity with temperature may be larger with a wide-gap material than with a narrow-gap one, the larger value of the gap width may more than offset the rate of rise of conductivity. This is the condition in silicon as compared to germanium.

Another advantage of silicon compared to germanium is the higher value of avalanche voltage or breakdown voltage that applies with silicon devices. This higher breakdown voltage is to a considerable extent a result of the relatively high inherent resistivity available in silicon. Whereas germanium diodes are limited to applied voltages less than 150 to 200 V, silicon junctions have been used successfully to over 1,000 V.

Semiconductor silicon has three limitations that have delayed its application in electronics. The first of these is the difficulty encountered in growing perfect single crystals. The technological problems of producing the required grades of silicon have been solved, however, and large numbers of silicon diodes and transistors are being produced. Other technological problems with respect to making devices are the control of the formation of junctions, and controlling surface phenomena (passivation), to minimize leakage current. Probably the most important limitation of silicon, important because it is an inherent characteristic, is the relatively low value of the diffusion constants for charge carriers compared to germanium. These constants are less than a third of the corresponding values for germanium, with the result that the frequency limit for a silicon transistor of a given structural design is at most a third of the corresponding high-frequency limit for a corresponding germanium unit.

1-4.3 DIAMOND

Diamonds have not found any use for either diodes or for transistors because of fabrication and doping problems. It appears reasonable to suppose that the best grade of commercial diamonds available may be sufficiently free of defects to be usable as the raw material for semiconductor devices, and the gap energy certainly is sufficiently wide that the range of operating temperature for a device made from it would be excellent. Because of its hardness and the difficulty in diffusing it with the proper combination of impurities, however, it may find its first application as a crystallizing base for a more routine semiconductor material.

The mobilities of the carriers in a diamond are somewhat higher than those for silicon, but not as high as those for germanium. It is, therefore, one of the best potential materials for use in high temperature devices, devices required to operate to several hundred degrees centigrade. Until single-crystal diamonds can be obtained economically and can be diffused with the necessary conduction zones, the diamond probably will have only textbook interest as a semiconductor material.

1-4.4 ALPHA-TIN

The alpha form of tin—at least in theory—is usable as a semiconductor, although its use is limited by its very narrow energy gap to temperatures considerably below normal room temperature. A superficial examination of its properties indicate that it might have some applicability as a material for use in diodes and transistors. How it might behave in its super-conducting region is of considerable interest. For example, transistors or diodes made from alpha-tin would require cooling at least to the temperature of dry ice, but they might make sufficient additional power economy available to be worth the development. A germanium-tin mixture might be useful, because less cooling might then be required. Mobilities appear to be nearly the same as those of germanium.

1-4.5 INTERMETALLICS

Certain compounds that have the electron-doublet type of bonding exhibited by carbon compounds and by crystalline semiconductors can be formed from elements in other than the fourth group of the periodic table. These compounds can be crystallized in the regular face-centered cubic lattice, and they can show the properties possessed by germanium and silicon when they are crystallized in the single-crystal form. Table 1-1, adapted from Jenny (Ref. 7), indicates the properties possessed by some of the possible combinations having promise as basic materials for semiconductor devices. It also includes a listing of the gap energy and mobilities.

Most of the intermetallic compounds having potential application belong to the group that may be called the IIIA-VA group, made up of the elements N, P, As, Sb, Bi, of group VA and the elements B, Al, Ga, In, and

Tl of group IIIA. There is at least one additional group of combinations that may be found to have possibilities once problems of chemical formation, purification, and crystallization can be solved; these combinations belong to what may be called the IIIB-VA group, consisting of the elements Sc, Y, La, and the rare earths in addition to the elements of group V.

Mixtures of intermetallic compounds can be formed just as mixtures of the various table IVA semiconductors may be formed. In these materials, the band gap energy is intermediate between that for either compound alone. The use of a uniform distribution of the mixtures throughout the bar of semiconductor does not provide optimum operating conditions, however, as the use of a higher concentration of the intermetallic having the higher gap energy in the emitter zone has been shown to increase markedly the injection efficiency of an emitter structure, making a larger number of emitter carriers available for diffusion to the collector.

There are other compounds that could be used as basic semiconductor material, but these materials are so complicated in structure that the probability of getting a good single crystal from which to make semiconductor devices is relatively small. A more complete table of possible intermetallic compounds is listed in Table 1-2. This table is divided into two sections, the first part including the materials on which the most work has been done, and the second those materials with small probability of being useful.

The doping of the intermetallic semiconductor with impurities to provide polarized semiconductor material is discussed separately in the paragraph on types of semiconductor, inasmuch as some special problems occur in accomplishing the polarization.

The so-called dry-disk rectifiers, using typically copper oxide or selenium make use of combinations of elements that behave as intermetallic compounds. The copper oxide rectifier, for example, uses cuprous oxide as the active material. The behavior of these devices is so irregular that they will not be discussed further here.

TABLE 1-1
SEMICONDUCTOR PROPERTIES

<i>Semiconductor</i>	E_g (electron volts)	U_e	U_h
a-Sn	0.08	3,000	?
Ge	0.7	3,900	1,900
Si	1.1	1,500	500
SiC	2.8	>100	>20
C (diamond)	6.0-7.0	1,800	1,200
InSb	0.18	65,000	1,000
InAs	0.33	20,000	200
GaSb	0.68	4,000	700
InP	1.25	>4,000	>100
GaAs	1.35	>5,000	>400
AlSb	1.52	≅ 400	≅ 400
GaP	2.25	>100	>20

1-5 INTRINSIC AND DOPED SEMICONDUCTORS

A refined semiconductor material may be classified either as an intrinsic material or one that has been altered by the deliberate addition of impurities that alter its electrical properties. The latter type of material is referred to as a "doped" semiconductor. Most of the semiconductor material used in diodes and in transistors is of the doped variety; because, however, any doped or polarized semiconductor must be prepared

from a single-crystal specimen of highly purified intrinsic crystal, intrinsic material must be discussed first.

1-5.1 INTRINSIC SEMICONDUCTOR

An intrinsic semiconductor is one containing the smallest possible amount of impurities after refining. Experiment has shown that any irregularities in the crystal structure or any impurities crystallized into it reduce the resistivity of the material by the process of introducing ionization centers. Because the total number of ions that move about in a semiconductor is limited by chemical physics to a quantity called the intrinsic number, or n_i (or p_i , to which it is equal), the presence of a large number of ionization centers makes necessary rapid recombination and, as a result, the period of existence of each ionized element is small. The lifetime of each charge must be large compared to the particle diffusion time across the base for transistor action to occur. The ions available in an intrinsic semiconductor that is not under optical or electrical stimulation always occur in matched pairs, one negative, or electron, and one positive, called a hole or vacancy in solid-state physics.

The manner in which the relatively high conductivity of an impure semiconductor is produced is rather curious, because in general the material must be electrically neutral in the absence of electrical fields. If the impurities are limited to compensating impurities and the crystallization takes place in such a way that the impurities can pair off and form a group of intermetallic compounds in the lattice, then the conductivity of the overall crystal will not be altered by the presence of the impurities. Unfortunately, however, it is difficult if not impossible to bring the stray atoms into such positions that they can form intermetallic compounds in the lattice, with the result that microscopic volumes of the crystal are polarized with one polarity, and adjacent volumes are neutral or of the opposite polarity. As a consequence, in each of these volumes, an excessive number of carriers compared to intrinsic material is available. The large number of conducting charges

available causes the conductivity of the material to be relatively high.

A crystal can be extremely pure and have a relatively high conductivity if there are many defects and dislocations in the crystallization, as each and every location at which such a defect causes a grain boundary acts to accelerate the generation of carriers. For this reason, the number of carriers of one type is in excess on one side of the boundary, and the number of the other is in excess on the other side. The large number of carriers again markedly increases the conductivity of the material. Because the variations in the conductivity of different regions of the semiconductor material used in transistors have a strong influence on the behavior of the resulting devices, the crystals used for semiconductor devices must have the highest possible purity, and must be crystallized with as high a degree of regularity as is possible. After crystals of the proper perfection have been produced, they may be altered by the introduction of the proper dilutants to give the required polar characteristics.

1-5.2 POLAR SEMICONDUCTORS

Semiconductors may be made polar, or they can be made to favor one type of carrier in preference to the other, by introduction of very small amounts of a material possessing a different number of valence electrons. The most logical impurities to choose for semiconductors like germanium and silicon are materials having valences either three or five, materials falling in the groups IIIA or IIIB, or VA or VB in the periodic table. The materials in group III have three valence electrons, yielding a doped semiconductor of the acceptor, or positive type, when introduced into a semiconductor material. Similarly, the introduction of materials from group V makes an extra electron available, producing a donor or negative type semiconductor.

Because the simplest intermetallic semiconductors are made from crystalline compounds of materials in the third and fifth groups of the periodic table, they cannot be doped readily with other materials from the same group. As a consequence, they use materials from

**TABLE 1-2
INTERMETALLIC SEMICONDUCTORS**

Those of high probable usefulness (see Table 1-1 for properties):

InSb GaAs SiC GaSb InP AlSb GaP

Other materials:

AlP AlAs InP InAs Ag₂TlTe₂ CuInSe₂
CuAlS₂ Cyanthron Indanthracene Anthracene

either periodic groups II or VI as doping ingredients, giving either acceptor or donor structures as with ordinary Semiconductors. The resulting polarized semiconductors behave in a similar manner to either doped germanium or silicon.

1-5.3 NEGATIVE, OR N-TYPE SEMICONDUCTORS

If a group V material is introduced into a semiconductor crystal lattice in low concentration, possibly one atom in 10^6 to 10^9 , then very little overall damage is done to the uniformity of the crystallization of the single-crystal semiconductor. Normally, the N-type semiconductor that results has sufficient donor impurity added to increase the available number of negative carriers by from one to many orders of magnitude with respect to the concentration in intrinsic material. For germanium, this means that greater than 10^{14} impurity atoms are required in each cubic centimeter (4.45×10^{22} atoms), and for silicon, greater than 10^{11} impurity atoms per cubic centimeter (5.03×10^{22} atoms). The minimum impurity ratio for germanium then is $1:1.85 \times 10^8$, and for silicon, $1:3.35 \times 10^{11}$. The maximum number of polar impurities a crystallized semiconductor can absorb without disturbing the crystallization depends on the doping impurity used and its method of application, and also somewhat on the polarity and the semiconductor itself. High concentrations of impurity atoms are required in the emitters and the high density edge of the graded bases in high-frequency transistors and particularly in tunnel, or "Esaki", diodes.

The presence of electrons from the donor atoms in the semiconductor causes a reduction of the number of holes or positive charges present in the lattice, since the increased number of electrons causes the recombination of holes to occur much more rapidly than can occur in intrinsic material. The number of holes present in an N-type semiconductor can be determined from the equation

$$n_n p_n = n_i^2 \quad (1-9)$$

where the subscript n refers to N-type material, n and p indicate electrons and holes, respectively, and n_i is the number of carriers in intrinsic material.

1-5.4 POSITIVE, OR P-TYPE SEMICONDUCTORS

In a similar manner, a positively polarized type of semiconductor, one in which the current carriers are holes (the absence of electrons), is formed by the introduction of very small amounts of materials from groups IIIA or IIIB of the periodic table. The methods of introduction of these materials into the semiconductor are the same as with donor impurities; experience has shown, however, that, in a reproducible manufacturing process, larger concentrations of some doping materials can be added to a specific intrinsic semiconductor than can others. This is the reason that more NPN silicon transistors have been available than PNP, whereas for several years more PNP transistors were made from germanium than were NPN units.

As a consequence of the ion-product law, the presence of increased numbers of p-type, or hole, carriers in a semiconductor material causes a considerable reduction of the number of electrons available for conduction purposes. Consequently, the conduction of current in acceptor-type materials depends on the hole-carriers. As the total number of one type of carrier is increased in a polar material with respect to intrinsic material, the conductivity is increased proportionately. The ion-product law for p-type materials takes the form

$$n_p p_p = n_i^2 \quad (1-10)$$

The majority carriers here are the p_p , or hole, carriers, and the minority carriers are the n_p , or electrons.

1-5.5 OHMIC CONTACTS

One of the problems in the utilization of doped semiconductor materials is the making of ohmic, or low resistance, contacts on the material. Making such contacts is an art all by itself, because the solders used have to include the right materials to wet the surface, and must also have expansion coefficients that are compatible with the material on which they are placed. Often a doping agent is placed in the solder to improve the characteristics of the contact, and sometimes, as in surface-barrier transistors, the entire junction may be plated on the semiconductor. The flux used in soldering is often important in assuring adequate wetting of the surface and in distributing the contact area sufficiently in width to keep the contact resistance to a small value.

1-6 SEMICONDUCTOR DIODES

Diodes are two-terminal devices that pass current with comparatively little difficulty in one direction, but pass only very small amounts of current in the reverse direction. Ideally, a diode should have high conductance, greater than 0.01 mho for any voltage across it in the conduction direction, and should have only a very small conductance, less than ten micromhos, in the reverse direction. In practice, no diodes meet these ideal conditions, vacuum diodes having high conductance when the anode is more positive with respect to the cathode than approximately minus 0.3 V. For more negative voltages, the conductance is virtually zero. Semiconductor diodes have very small values of conductance for collector-to-cathode potential, less than a few tenths of a volt, and have high conductance for more positive values of potential. The voltage at which transition occurs in a diode depends on both the semiconductor material itself, and also on the doping conditions in the two sections of the diode.

A semiconductor diode is made from a piece of doped semiconductor, the doping consisting either of only one type or of two zones, one being doped P-type and the other N-type. In some applications, the doping in one of the zones has been diffused into the semiconductor, and then the device is said to have a graded junction rather than an abrupt junction. One or more leads is now soldered to the segment of semiconductor, one for a point-contact diode, and two for a junction diode. These soldered leads must make ohmic contacts on the surface.

If the piece of semiconductor used for making the diode is not a single crystal and free of defects, large numbers of carriers will be available, and ready conduction in either direction can result. The result in the diode is a poor forward-to-backward ratio, and in a transistor, very low current gain.

When the diode is polarized in the conduction direction, the majority carriers in the P- and N-type regions are swept toward the junction by the applied field, and they recombine with the majority carriers from the opposite side of the junction, thereby causing current to flow. When a reverse potential is applied, however, the field tends to accelerate only the minority carriers toward the junction, and draws the majority carriers away from it. Diode current flow continues until the majority carriers in the neighborhood of the junction have all combined with minority carriers, at which time the current decays to an extremely small value. Then minority carriers occupy positions in the neighborhood of the boundary to establish electrical equilibrium in the diode.

1-10

Historically, the earliest semiconductor diodes used were a form of point-contact diode, the galena crystal detector. Most of the diodes used as detectors still are point-contact diodes, because junction diodes tend to have an excessively large shunt capacitance. Junction diodes find a wider application in the field of power rectification, because shunt capacitance is relatively unimportant, whereas current capacity is very important.

1-6.1 POINT-CONTACT DIODES

Point-contact diodes are really a special form of junction diode in that the junction layer is introduced into the semiconductor through chemical action on the point resulting from current pulsing or other processing techniques. These diodes are made by soldering a small semiconductor wafer to a terminal to give an ohmic contact on one side, and bringing the catwhisker contact, a specially pointed wire, against it. The wire may contain a trace of indium or gallium or other material if a high conductance diode is required. After contact is made, the diode is pulsed with pulses of current from a capacitor to weld the point to the semiconductor and to transfer enough material from the point to establish a junction region in the wafer.

The point-contact diode has a very small internal capacitance across the junction because of the fine wire used in the contact point, but it does include a small amount of series inductance instead. Because the internal series resistance in such a device is comparatively small, the device can be useful to frequencies as high as several hundred megahertz. Point-contact silicon diodes have been used in radar equipment to frequencies as high as 30,000 MHz, and possibly higher. Their principal application has been as a nonlinear device for frequency conversion or mixing.

1-6.2 JUNCTION DIODES

Junction diodes have the rectifying junction formed internally within the piece of semiconductor material from which they are made. The junction may be formed by growing it in the semiconductor as it is crystallized from a molten bath, or it may be formed either by an alloying or diffusing or other process. The properties of the various kinds of structures depend primarily on such things as doping levels, presence and numbers of traps, layer thicknesses, variations in doping levels, particularly near the junction, and related factors, including the kinds of materials.

The properties of junction diodes can be varied to a wide degree by control of doping levels and trap levels.

Typically, in specialized diodes, only one of the two regions is likely to be heavily doped and have a high conductivity as a result. This condition helps to assure a high back resistance in the device. The region of the low doping level should be sufficiently thin that it does not introduce high body resistance, yet at the same time it should be sufficiently thick that the voltage breakdown level meets requirements.

The presence of traps very close to the junction boundary can cause major changes in the overall properties of the diode. The trap density should be sufficiently small that normal conduction characteristics are not altered significantly, but should be large enough to enhance the recombination rate on reversal of the applied field.

The total number of carriers which must be removed by recombination on field reversal is a function of doping levels on both sides of the junction, and also on the thicknesses of the respective layers. High-speed switching diodes of necessity must be ones in which both the total number of recombinations is kept to a minimum and the total time required for recombination is also minimum. Further, only the minority carriers are of concern. An important factor in accomplishing the goal of removal of excess minority carriers is the provision of traps in the neighborhood of the junction for removal of the minority carriers in the thin low-conductivity region of the diode.

It should be noted that a variety of special-purpose diodes—such as hot-carrier diodes, Esaki or tunnel diodes—are used for special functions in electronic circuits. Their properties are such that they perform a number of functions not readily accomplished by other more conventional techniques. Design of circuits for use with them is too specialized for separate consideration herein.

1-6.3 CONTROL RECTIFIERS

A series of devices which are called diodes or rectifiers but which are really multilayer switches (or groups of multilayer switches with associated blocking diodes) are in extensive use today. They have properties that closely parallel those of thyratrons and ignitrons, and in fact have largely replaced these electron tubes for a wide variety of applications. Essentially, they function through the action of a grid or gate electrode that blocks conduction until a previously chosen set of conditions exist, at which time the device is switched to a high-conductivity state. It remains in this state until reversal of the applied voltage occurs.

These control rectifiers can be built to be unilateral, in that they control in only one direction; or bilateral,

in that they can control in either direction. (The latter may be called “symmetric” control rectifiers.) Typically, when ordinary control rectifiers are used on AC, they are used with a series blocking diode or rectifier to prevent conduction in the reverse direction (and to assure turnoff), as otherwise self-destruction can result. When they are used on DC, an inductor normally is included in the power circuit to provide the required polarity reversal.

1-7 TRANSISTORS

A transistor is an amplifying device capable of controlling the flow of power in an auxiliary circuit. It is made of doped semiconductor, and normally has a minimum of three leads, at least one of which is attached to the semiconductor through an ohmic contact. The only kinds of transistors which will be considered and discussed in any detail in this book have a multiplicity, three or more, ohmic contacts. The design procedures that are described apply to bipolar and to field-effect transistors with minor modifications, and they also can be adapted to use with high-vacuum electron tubes with somewhat more extensive modifications. The procedures for handling the required changes are discussed in Chapter 3, where the physical nature and properties of the various active devices under consideration are discussed in relation to the circuit design procedures involved.

1-7.1 THE BIPOLAR TRANSISTOR

Standard bipolar transistors which are made from layers of doped semiconductor material, silicon, germanium, gallium arsenide, etc., generally take the form of a sandwich structure consisting of an emitter layer and a collector layer of relatively high-conductivity polar material separated by a very thin layer of lower-conductivity material of opposite polarity to that of the emitter and collector zones. It is important to use the highest possible conductivity material in the emitter layer and, except in contact with the base region, a reasonably high-conductivity material in the collector. A very thin layer of relatively low-conductivity material adjacent to the base can help to assure a high-breakdown voltage between collector and either the base or the emitter, and it will help to increase device reliability where the ability to withstand high voltages may be important. Use of high-conductivity material otherwise helps to minimize both emitter- and collector-spreading resistances, and thereby minimizes parasitic impedance problems.

The high-conductivity emitter region is generated by the introduction of high levels of doping, and it makes possible high injection capabilities from the emitter to the base region. The low conductivity of the base region and its very small thickness assure that a minimum of recombination will occur during transport of injected carriers across the base into the emitter from the base. (This function can also be achieved with heterojunction devices without significant differences in doping level if the activation voltage for injection into the emitter is substantially greater than that for injection into the base.) The spreading resistance in the base region may be minimized by maximizing the perimeter of the base contact adjacent to the emitter contact, and keeping the path length from the base contact to the active zone under the emitter as short as possible as well.

The value of the collector spreading resistance encountered with a bipolar transistor is somewhat less critical than the values of the base- and emitter-spreading resistances, but it can increase the overall amplification of an amplifier and reduce the effective stability of the stage. The overall voltage gain from the active base-to-emitter junction to the active collector-to-base junction is the critical factor affecting phase stability of amplifiers, and it must be held to closely controlled values depending on the design and application.

The various techniques for making bipolar transistors—grown junction, alloy, multiple diffusion, epitaxy, and combinations of them—lead to devices having different values for the important parasitic parameters. Generally, the planar-epitaxial manufacturing techniques lead to the best all-around characteristics for typical bipolar devices. Graded doping may be introduced in any of the layers, and long-perimeter active regions can be developed using these techniques. The very critical control required to achieve reproducible results has been achieved, and yields as a result are excellent.

1-7.2 FIELD-EFFECT TRANSISTORS

Two basic classes of field-effect transistors are presently available—the junction device, or J-FET, and the insulated gate device, variously known as IGFET devices and MISFET devices (the Metal-Insulator-Semiconductor devices are often mislabeled **MOSFET** devices for Metal-Oxide-Semiconductor, but other elements such as nitrogen may be used for formation of the insulating material). These devices are essentially charge-control devices like bipolar transistors and electron tubes, but they have some unique properties which are developed in the discussion in Chapter 3 and Appendix I.

Field-effect transistors generally have two modes of operation, the first being the conventional Shockley mode, and the second being an exponential mode variously called either the Fermi mode or the diffusion mode. This latter mode of operation is really the limiting mode in that it bounds the maximum value of transconductance per unit current which can be developed at 39,000 **pmhos** per mA, the same limit as applies under low-injection conditions with the bipolar transistor.

The junction FET device has been shown to develop the stated 39,000 pmhos per mA over as much as four to five or more orders of magnitude of current. This effect is noted at small values of drain current through the device, but the use of appropriate channel doping procedures, at least theoretically, can increase the range of current over which the effect can be achieved.

Study of the properties of insulated-gate devices shows that a similar effect is observed, but for reasons not yet fully understood, the limit appears to approach $\Lambda/2$, or 19,500 pmhos per mA. (This probably is a consequence of the dissymmetry of the channel.) Again, the effect is noted at small values of channel current. At extremely small values of current, approaching leakage current, the measured value of A decreases as a result of bulk and surface leakage. The control efficiency is defined later in this volume in terms of an efficiency parameter called kappa (κ).

The insulated-gate device is more subject to failure as a result of electrical breakdown than are either the bipolar or the diode field-effect transistors. As a consequence, selection of devices is significantly affected by the transient voltage fields which may be encountered. Failures with bipolar and junction FET devices are more likely to be thermal in nature, and generally can be prevented through appropriate design for load-shedding.

1-7.3 OTHER ACTIVE DEVICES

For reasons that will be evident in Chapter 3, other kinds of electron devices are still important in military electronics. In particular, it can be anticipated that electron-tube devices will continue to be required in special applications to a sufficient extent that brief notes on their application in military systems are included briefly in this revision of the handbook. These notes show primarily how the described techniques for use with transistors can be simply adapted to use with tube circuits.

The triode electron tube has characteristics which parallel those of field-effect transistors. The principal difference to be noted is the fact that the output admit-

tance for the triode tube is as much as several orders of magnitude higher than that of the FET device. Also the tube under normal use conditions does not encounter a saturation diode line, since it is seldom biased to operate near this contour. The contour readily may be observed by operating the tube as a diode with its grid and plate connected together. Input conductance is near zero for these devices except under bias conditions for which the grid is positive with respect to the contact potential contour (roughly the zero-bias contour). These tubes normally display values of the κ -parameter ranging from near unity at extremely small currents to as small as 0.0001 at large values of current. With tubes having exceptionally low leakage, the value of κ may approach unity for several orders of magnitude of plate current.

Tetrode and pentode electron tubes behave like triodes under variation of screen voltage and like field-effect transistors under variation of plate voltage. In short, plate conductance for these devices is very small, whereas the screen-to-plate transconductance is typically between 0.01 and 0.3 times that between control grid and plate. Input conductance is near zero except under positive-bias conditions.

The capability that the designer has to change characteristics of the tetrode or pentode tube through variation of the screen voltage makes these devices essentially variable-power devices having very low output admittances. They are essentially current source devices. To use them properly, one should select the lowest screen voltage which will give a modest margin of safety in producing the desired output power. Detail discussions of use of all kinds of electron tubes under conditions maximizing reliability are included in other books published by the writer (Refs. 1, 8). The discussion in these books includes a broad spectrum of kinds of circuit applications and also a broad spectrum of kinds and types of tubes.

1-8 NONLINEARITY CONSIDERATIONS IN ACTIVE DEVICES

The idea that active devices can be linearized has been accepted for many years in spite of the fact that all reasonable evidence points to the contrary. The assumption that linearity could be postulated can be shown analytically to apply only over a small range dependent on the function $\kappa\Lambda$ and the current level involved.

The erroneous impression has been supported by the fact that often degeneration can occur which is dependent on a relatively constant ratio such as the amplifica-

tion factor for a tube or the β for a transistor. The consequence of the degeneration is an apparent linearization that does prove useful in approximations. Typically at least one of the parameters involved in the linearization is sufficiently undependable as a characterizing parameter that the losses resulting may be much more damaging than the gains.

The basic equations for solid-state active devices, as stated in Eqs. 2-16 and 2-17, are clearly exponential in character, and, as such, they present very nonlinear relationships for voltages and currents. This situation is taken advantage of in the logarithmic converters developed for use with analog computing equipment. The equations are modified from true logarithmic by such parameters as spreading resistances, variations in values of κ 's, high-injection corrections, and other related effects, but basically and inherently the devices are nonetheless exponential in character, and therefore they are very nonlinear.

All of the different kinds of active devices known to exist at the present time appear to be solid-state in nature, and they are best represented in terms of transadmittance configurations. The currents in these devices are exponential functions of the voltages applied across the active junction regions. In theory, four different kinds of active transducers might be available for use as amplifier mechanisms, the four being transadmittance devices, (transadmittors), trans-impedance devices, trans-current-gain, and trans-voltage-gain devices. At the present stage of understanding of physical systems, **only** the first two appear to be of significant importance. In theory, some kind of a magnetic amplifier may be developed which will prove to be a true trans-impedor. Present-day magnetic amplifiers obtain their power control properties through the action of appropriately placed diodes, and hence hardly can be considered as ideal trans-impedance devices.

There appears to be a real problem in trying to control a current by another current in such a way that a power gain occurs without the basic control being a voltage control. A through vector can control an across vector or an across vector a through vector with a potential power gain being available, but such does not appear to be true of the action of one through vector on another or one across vector on another. For this reason, no consideration is given herein to either the trans-current or the trans-voltage gain situations. Devices displaying true applications of these trans-vector configurations, of course, may be discovered eventually. If such proves to be the case, it will be necessary to evaluate the linear and nonlinear properties of the resulting devices to determine what modifications in

the applicable theory are required for their effective use.

There is good reason to believe that the principle of duality will be useful with trans-impedance devices, and it may be the key to the application of the techniques to be described to trans-impedors.

Those properties of the active devices which are patently nonlinear should be included in the device model as part of the intrinsic model, and those parameters and characteristics which are relatively independent of currents and voltages should be treated as part of the external circuit. For example, capacitances may vary with either applied voltage or stored charge, and hence must be taken as part of the active model. On the other hand, the spreading resistances— r_b , r_c , and r_e —are relatively independent of currents and voltages, and hence may be treated as part of the passive imbedding network.

The analysis of the separation of parameters and components of a device and its network into active components and imbedding components for the passive network has been rather haphazard in many respects. In addition to separation of components into groups which are fixed in value and those whose magnitude is a function of a current or a voltage, it is also important that the reduction to representing elements through the use of network theorems not be allowed to introduce elements whose value vary in an unrealizable way with such parameters as frequency. Reduction of the base input impedance for a bipolar transistor in terms of either a pure hybrid representation or in terms of a pure admittance representation leads to physically unrealizable networks whose element values are functions of frequency. This independence may be minimized only by use of an admittance representation for the intrinsic device and extracting the base-spreading resistance as a separate entity. Under these conditions, the frequency dependence is reduced to tolerable limits for the kinds of application normally encountered in military and commercial equipment. The application of either Thevenin's or Norton's theorems should be avoided if at all possible except in instances where the percentage bandwidth required of the network is very small, certainly less than 10%.

1-9 TRANSISTOR NOISE

The noise generated in transistors may be divided among three different types, the $1/f$ type,* the uniform

type, and the f type (Fig. 1-5). These definitions are based on the variation of the average noise intensity with frequency because the noise amplitude as a function of frequency decreases with increasing frequency in the $1/f$ region, because it is relatively independent of frequency in the frequency-independent region, and because the average amplitude increases with frequency increase in the f region.

These three regions are separated by transition frequencies that are defined as f_{n1} and f_{n2} , where f_{n1} is the corner frequency between the $1/f$ and uniform regions, and f_{n2} is the corner frequency between the uniform and the f regions. The values of these two frequencies and the value of the noise figure in the region of uniform noise as a function of frequency are the data on noise, which are important to the designer in that they define the noise characteristics of the transistor throughout its operating range.

Strictly, as is always true of noise signals, the amplitudes indicated by the relations are the averages of their mean-square values, because noise is by nature a completely unpredictable condition on an instant-by-instant basis. At any one instant, the spectrum of the noise energy as a function of frequency may, and in general will, differ widely from the nominal value indicated by the rms average. Over the long term, or on the average, however, the value of the noise power does approximate the distributions indicated.

The noise in the low-frequency, or so-called $1/f$, region, is similar in its general characteristics to flicker noise in vacuum tubes. This type of noise is introduced into a transistor through imperfections resulting from crystal flaws or surface defects in the device. The proper treatment of the surfaces of the transistor, or passivation, normally reduces to rather small values the flicker type of noise. The presence of an excessive amount of this type of noise may indicate the existence of "tunneling" or areas of potentially unstable surface or junction conditions. It may introduce irregularities into either the output conductance or the input conductance of the device. A few commonly used transistors do have high values of f_{n1} , but in general the devices most commonly used have values of f_{n1} that are less than 100 Hz.

The corner frequency f_{n2} is of considerable importance in transistor circuit design because it also specifies the maximum switching rate for a conventional R - C multivibrator (Ref. 9). The period corresponding to this frequency in radians is approximately equal to

*Strictly, this is an f^{-n} region, where the value of n may be, but need not be, unity. The more common values of n encountered are 0.5 and 1.0. In this region, the value of n is always positive.

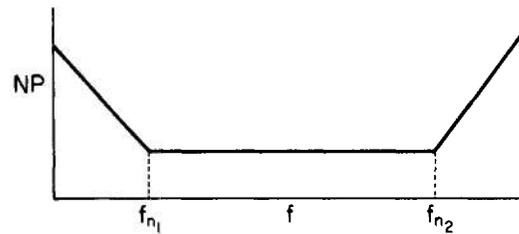


Fig. 1-5. Variation of Noise Power per Cycle With Frequency

the time required for the transport of an individual carrier across the base region of the transistor. These numbers are not numerically equal, but agree within a factor of 2. The noise for frequencies above this frequency increases because the nonuniformity of current flow becomes the controlling factor in noise produc-

tion. The comparatively long drift time in diffusing across the base region is long enough, compared to the period of the wave, to permit phase irregularities to be introduced as a consequence of beam transit time. This noise is similar to drift noise in klystron tubes.

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CHAPTER 2

VARIABLES AND PARAMETER RELATIONS

2-0 INTRODUCTION

The representation of the junction transistor in terms of static variables like voltages, currents, small-signal parameters, immittances, and ratios of immittances, can take a wide variety of forms. The utility of any of these forms of representation of a device depends on the relative magnitudes and the stabilities of the variables and the parameters and their relations to one another. For this reason, it is important to evaluate the various possible arrangements in which the properties of the device can be expressed in terms of basic physics, and to select the form of presentation that expresses these characteristics in the form that minimizes the precision required of measurement and minimizes the error encountered from changes in temperature and other environmental conditions. The purpose of this chapter is to make a brief examination of the parameter and variable problem to select a system of representation that can be used effectively for a wide variety of applications.

Since the representation of the characteristics of devices like transistors is extremely complex (from seven to ten small-signal parameters alone may be required), it is essential that the data be organized in a manner to provide the required information in the simplest and the most direct manner. As a result, it is important at each stage of the development of a system of symbology, variables and parameters to evaluate the comparative importance of the various types of data, so that the more important factors can be displayed prominently and those of reduced importance be given less emphasis. This organization should be so arranged that maximum ease of measurement and maximum use of the information results and a minimum of difficulty is introduced by thermal and other forms of instability.

The first subject to be discussed in this chapter is the symbology required in order to develop a general system of nomenclature that can be used for the presentation of variables and parameters throughout this book. After this discussion, the possible choices of input and output variables are considered and a preferred combination is selected that provides the required device data in convenient form. This selection must be coordinated

with the plotting arrangements used for the data on the variables.

The remaining paragraphs of the chapter are concerned with the selection of a form of relation of small-signal parameters that makes possible direct design with a minimum of difficulty for a comprehensive group of types of circuits, and the selection of the basic configuration to be used in general design problems. The relations selected should be optimum for as wide a variety of important design problems as possible, and should yield other designs as limiting cases. The configuration selected should make possible the measurement of the properties of the device with a minimum interference from associated circuitry. These paragraphs must solve the controversial questions of the small-signal parameters to be used in the book and the question of the appropriate common electrode for the transistor. The chapter is closed with tabulations of the relations among the various systems of parameters.

2-1 SYMBOLOGY

The set of symbols used in this book, a complete tabulation of which is included in the List of Symbols, is based on the standard system developed by the Institute of Radio Engineers and the American Institute of Electrical Engineers.* Some minor modifications have been made in the system because the use of the small-signal methods to be described makes possible much more complete calculations than have heretofore been possible and also makes necessary some additions and modifications to the system to take full advantage of the improvements made possible by the methods.

The system of identification of the terms in the small-signal equations for operation of a transistor or for any network having an input and an output circuit (two-port network) until recently consisted of identifying the sets of terminals as set one and set two, with the immittances bearing two numbers each (Y_{11} , Y_{21} , h_{12} , etc.).

*The IRE and AIEE have merged to form the Institute of Electrical and Electronics Engineers (IEEE).

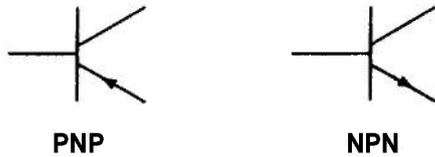


Fig. 2-1. Standard Transistor Symbols

This method has been replaced in the United States by the use of a subscript *i* for the input current and voltage, and a subscript *o* for the output current and voltage. The designation of the immittances has been changed completely, typical sets in the revised system reading y_i , y_f , y_r , and h_i , h_f , and h_o . This system of symbology has not met with favor abroad inasmuch as the words for input, forward, reverse, and output in other languages are completely different from the English words, with the result that the subscript letters have no significance. Just what the conclusion of the attempts at coordination will be is not currently clear, but because the use of the letters does conform with convenient usage in English it will be used, along with a subscript *e*, for the modified output admittance in this handbook.

The graphic symbols used for representation of transistors and transistor-like devices have been in a state of confusion for many years. Fairly general agreement has been reached, both here and abroad, on the symbol originally introduced by the Bell Laboratories for representation of the point-contact transistor. This symbol, shown in Fig. 2-1, is not particularly satisfactory for junction transistors, but it has had general acceptance.

Ideally, a graphic symbol can be expected to fulfill the following conditions if it is to be of maximum utility:

1. It should represent the device physically in a way that gives some indication of the behavior of the device.
2. It should be easy to draw.
3. It should be consistent with other related symbols.

A symbol consisting primarily of horizontal and vertical lines with a minimum of slant lines and circles would be the most satisfactory arrangement to draw, and it might also best fulfill the consistency and physical representation requirements. The symbols shown in Fig. 2-2 were introduced by Lo, Endres, et al. (Ref. 1). Each can be rendered somewhat easier to draw by the use of the format shown in Fig. 2-3, a form that appears to be generally satisfactory. Some of the other symbols

that have been used are shown in Fig. 2-4. Although the writer tends to prefer either the symbols of Lo, Endres, et al. or the modified forms of them, the standard IEEE symbols will be used in this volume.

2-2 INPUT AND OUTPUT VARIABLES

The current and voltage variables used in the presentation of the static data on junction transistors must be selected to yield information on both the output and input characteristics in a manner that is, as far as possible, free of environmental variations. For example, the output relation, which involves normally the collector voltage and the collector current, is expressed in terms of one of the input variables, because the input controls

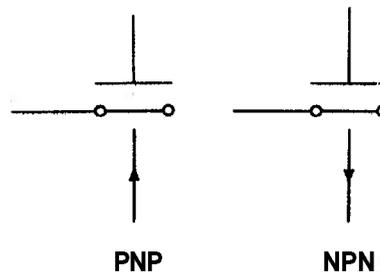


Fig. 2-2. Symbols of Lo, et al

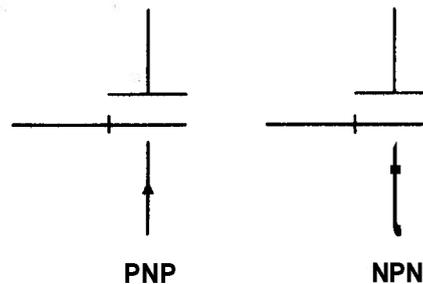


Fig. 2-3. Modified Lo Symbols

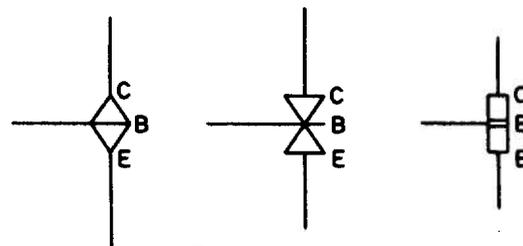


Fig. 2-4. Other Symbols

the exact combination of output values obtained with the device. The fact that the value of the Fermi potential of the semiconductor material is strongly a function of temperature makes desirable the use of input current as the additional variable, in spite of the fact that the output current is controlled by a combination of the Fermi potential and the doping levels. Both the base current and the emitter current have been used quite extensively as this input variable, but the trend has for some time been toward the use of base current.

This choice of base current is actually dictated by requirements on precision of measurement. The base current, the emitter current, and the collector current all must be known, and are related by the equation

$$i_b + i_e + i_c = 0 \quad (2-1)$$

The collector current i_c , which is usually taken as the output current in circuits, and the current having the smaller magnitude between the remaining base current i_b and emitter current i_e are selected as the plotting current variables. The use of the smaller in magnitude of the two possible input currents as the plotting variable relaxes the accuracy and precision requirements on the measurement of the device currents because the mathematically difficult feat of differencing two large numbers with high precision need not be performed. Table 2-1 shows the measurement accuracies required for the emitter and collector currents and for the current gain, alpha (α) to get base current and beta (β) accuracies of 10%.

The use of collector voltage and current as the coordinates in conjunction with contours of constant base current has received general acceptance for presentation of the output relations for transistors. However, an input relation is also required, presenting the two input variables in terms of one of the output variables. This input relation is normally presented on a separate set of curves, although there is at least one method of combining the two sets of data into one family.

The set of variables selected for the input contour relations may include either the group input voltage and current and output voltage, or the group input voltage and current and output current. There are a number of combinations of each of these groups, and the ease and convenience of use can be altered considerably by the shift from one form to another. For this reason, a careful examination of the properties of each is required.

The form of data presentation in which both sets are combined on a single chart includes both contours of constant base current and contours of constant base

voltage on a single coordinate array of collector current and collector voltage (Fig. 2-5). This arrangement is convenient because the construction of one load contour on the set of curves makes possible direct reading of both the input current and input voltage. The curves are excellent for applications in which no small-signal data are required, but they become somewhat crowded if four sets of small-signal contours are added. Furthermore, they do not present the static data in a form that can be used easily for determination of small-signal data by differencing. For this reason, where small-signal data are required, one of the two-graph presentations is more convenient. The selection of the optimum form of the two-graph presentation is next considered.

2-3 PLOTTING ARRANGEMENTS

The configurations used for the input and output families of data should present both the current-voltage relations for the input circuit, and the current-voltage relations for the output circuit in a form that simplifies the direct coordination of the input and the output characteristics. In the following paragraphs, the use of both the contours of input voltage and of input current as a function of output voltage and current is discussed, and then other configurations using separate input families are considered.

The plotting of the input variables in terms of the collector voltage may be accomplished in at least four ways. The contour lines may represent constant values for either the base current, the base voltage, the collector voltage or collector current. And the coordinate scales for use with each possible contour variable in the establishment of a graph may be subject to selection also. Because the output curve family consists of voltage, of constant value of input current as a function of the output voltage and current, and because corresponding points on the input and output families must be coordinated in the process of design of a circuit, the use of input curves based on contours of constant value of the input current, one of the coordinates then being base voltage and the other either collector voltage or collector current, appears to have significant advantages. One or the other of these two arrangements has been used on data sheets published by device manufacturers. For example, Amperex and Valvo GMBH have for some time plotted the input family in much the same way as is done in this book, Fig. 2-6, and Fairchild, RCA, and others have published curves with the collector current as the third variable rather than collector voltage. Typical examples of these curves are included in Appendix E.

In the amplification region, region **11**, the collector current varies but little with change of collector voltage and a **fixed** base current, with the result that considerable crowding can occur. When plotted as a function of collector voltage, however, the curves spread out in a form that facilitates the use of the available data. This form of the curves is particularly helpful in the estimation of admittance parameters.

The input relations as a function of collector current are most useful in region III, the current-saturation region. In this region, the base voltage changes rapidly and the collector current also changes rapidly, and the data on saturation conditions required in switching design are available. With devices intended primarily for use in switching circuits, the combination of the standard collector family of curves having the base current as the contour variable in conjunction with a base family also having the base current as the contour variable and the base voltage and collector current as the coordinates may prove more useful than the corresponding input family with collector voltage as the coordinate. However, the difference is so small that the advantages of using collector voltage in region II make it the preferred coordinate for general use.

One difficulty in plotting the input contours as a function of collector current is that it is more difficult

to sweep the collector current than it is the collector voltage. The current can be swept by sweeping the voltage in region **111**, but the action is unsatisfactory in region II because of the slow variation of I_c with V_c .

Contours of constant value of the collector voltage have frequently been used in the past as a means for presenting the input characteristics. There appears to be a trend away from this format, however, for reasons discussed in the next paragraph on information content. **These** curves are difficult to plot on automatic curve-tracers, and they are rather difficult to use effectively.

2-4 INFORMATION CONTENT

One of the important considerations in the development of a system of data presentation on any device like a tube or a transistor is the organization of the information and the data to make all important factors readily available, and to provide the less important data in a manner which makes them available, but does not stress them or weight them excessively. A typical question, the answer to which might be found by the use of the concept of the value of information, is the selection

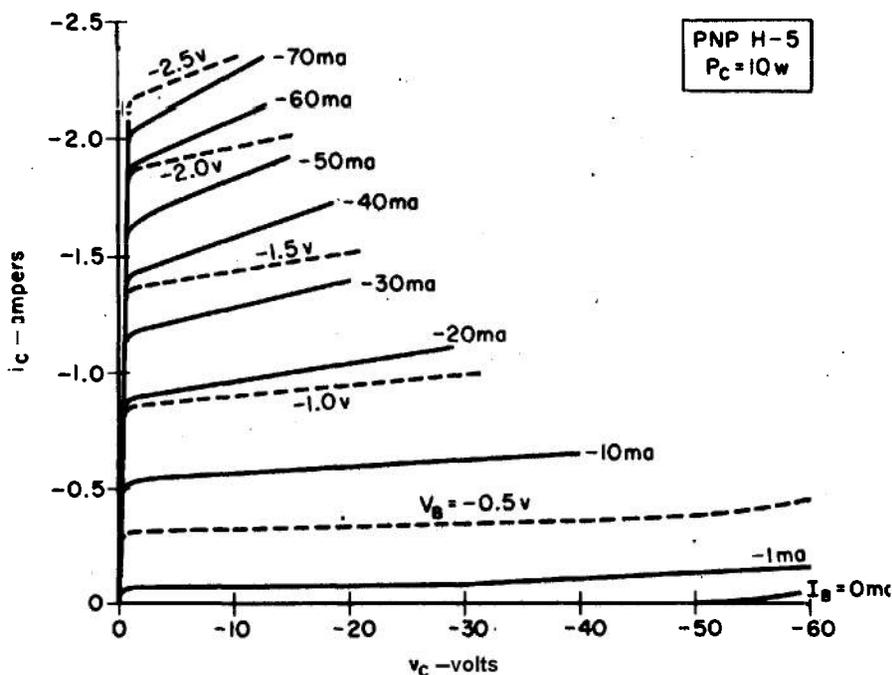


Fig. 2-5. Combined Input-output Curves. Curves courtesy Minneapolis Honeywell Regulator Co.

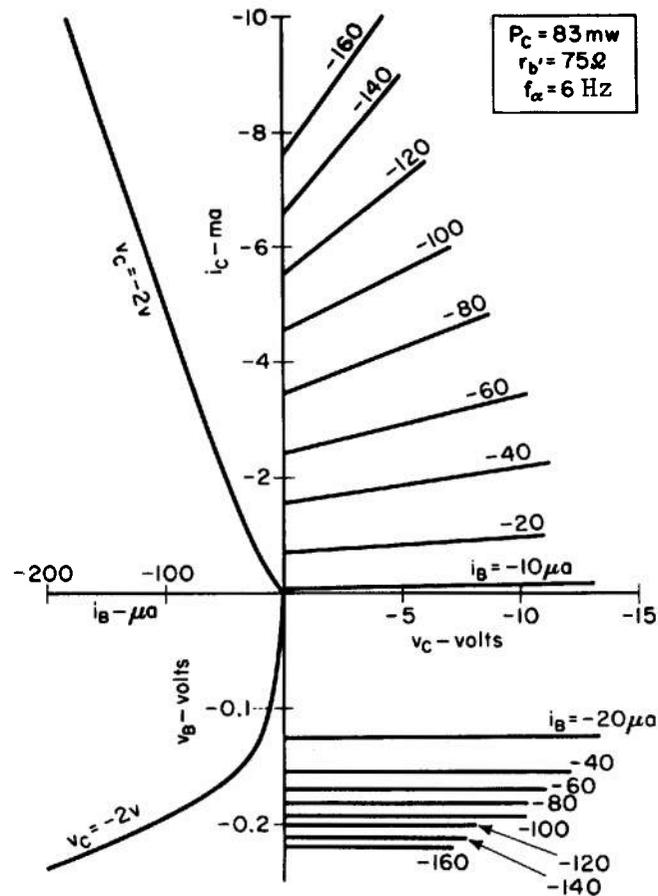


Fig. 2-6. Typical Curves—OC45. Courtesy Amperex Electronics Corp.

of the appropriate component of current for use in plotting data sheets for transistors.

When the junction transistor was first introduced many manufacturers provided their characteristic data on the devices in terms of collector voltage and current, and emitter current. Users soon found that design was inconvenient at best using this arrangement, because it was extremely difficult to get a reasonably accurate estimate of the current in the base lead from these data. And, unfortunately, that information was needed quite often. The use of two currents nearly equal in value as plotting variables made necessary the determination of the third current by the process of subtracting two relatively large numbers to get the value of a smaller number. This differencing operation is strongly disapproved of by mathematicians because the precision required of the original data to obtain an accuracy of even 50% in the smaller may be extreme. Table 2-1 shows the precision required for determining the base current of a transistor to an accuracy of 10% when the emitter

current, the collector current, and either the α or β are given.

Clearly, the most extreme accuracy may be required of the values of the emitter and collector currents to get any sort of precision in the value of the base current. The base current must be selected as a plotting variable, rather than the emitter, if the precision requirements are to be reasonable.

TABLE 2-1
PRECISION REQUIREMENTS ON CURRENT GAIN

α	β	Precision:	i_c	i_e
0.5	1.0	10%	5%	
0.75	3.0	1.67%	1.25%	
0.9	9.0	0.55%	0.50%	
0.95	19	0.27%	0.25%	
0.98	49	0.10%	0.10%	
0.99	99	0.05%	0.05%	
0.995	199	0.026%	0.025%	

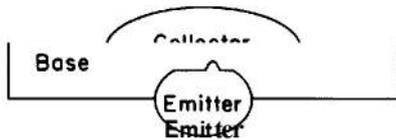


Fig. 2-7. Crystallization Defect

2-4.1 VOLTAGE EFFECTS

The potential stress applied from emitter to collector has a strong influence on the behavior of a transistor both at very low values of voltage and at relatively large values. In the region between, the voltage has relatively little influence on the magnitude of current flow. The current-voltage behavior at very low voltages determines the minimum dissipation in the transistor for any given value of collector current, and is for that reason very important. In a similar manner, the variation of collector current with collector voltage at large values of voltage tells a good deal about the characteristics of the individual transistor, since it shows where avalanche current multiplication and severe thermal heating occur. If the value of voltage at which avalanche multiplication occurs is abnormally low, defects of crystallization such as are shown in exaggerated form in Fig. 2-7 are probably present. A bump or point on the boundary between either the emitter and base or the collector and base causes an area of higher than normal potential stress, and causes the multiplication of the number of carriers at an abnormally low voltage. A transistor can short-through (punch-through) at such points. Unless a device approaches failure from punch-through, this kind of boundary defect has little effect on the behavior of the input circuit, but it alters the output characteristics significantly. The output family of curves appears somewhat as shown in Fig. 2-8.

Thermal effects in the transistor introduce a hysteresis effect into the output contours as a function of base current, and they also introduce a typical heating effect into the input contours when they are plotted in terms of collector voltage. (The base current contours curve toward minimum magnitude of base voltage as the collector voltage is increased.) This effect is usually only barely noticeable on a sweep-curve analyzer such as the Tektronix Model 575 analyzer. It shows up best when the sweep rate is low enough so that thermal heating has time to occur.

Clearly, the behavior of an input family of curves based on contours of base current in terms of base voltage and collector voltage can be used to provide

some idea as to the behavior of the device in its proposed operating circuit and also to detect possible defects. The choice of the collector voltage as the third variable on the input contours is dictated by the fact that under all but saturation conditions the magnitude of the collector voltage per se is more important to device behavior than is the value of the collector current.

The contour set that best expresses the properties of a device presents the data in terms of the variables that are most stable and significant for representing it. Since the output contours are without question more important than the input contours with most devices, the variables for plotting the output curves are the most important to select correctly. The selection of contours of constant magnitude of base current plotted in terms of collector voltage and collector current clearly gives the output characteristics in terms of the most sensitive variables, and gives them in the form showing the highest order of thermal stability.

The coordination of the input and the output families of data can improve the usefulness of both families of curves. Unless the families are so arranged that corresponding points on the two families can be readily located, full information on static behavior is not readily available. To facilitate data transfer, the collector voltage may be chosen as the abscissa on both graphs. If, then, base-current contours are plotted as a function of collector voltage with base voltage as the negative ordinate, the transfer of a point on the output family of curves to the input family requires only the location of a point on one of the base-current contours of the input family vertically below the corresponding point on the output family. If a set of intersections of

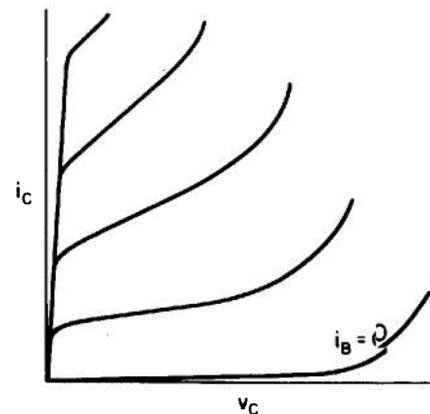


Fig. 2-8. Output Curves for a Transistor With Crystallization Defect

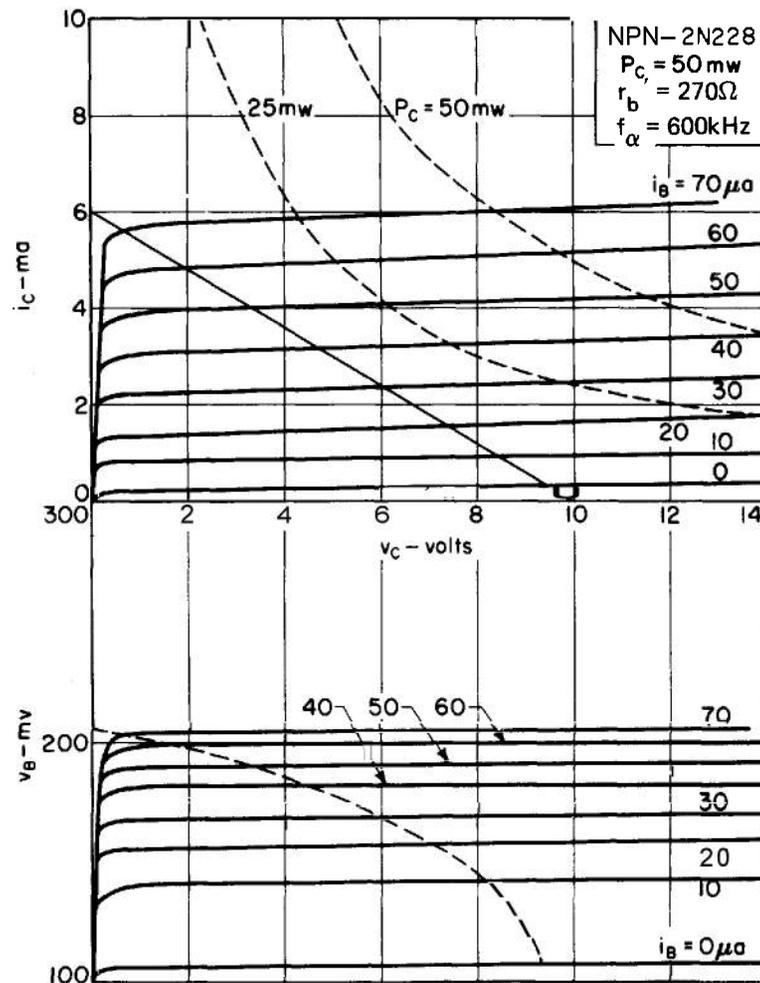


Fig. 2-9. Curve Set for 2N228 Transistor

a load line with the base-current contours on the output family is transferred, one by one, to the input family, then the corresponding input contour may be drawn and static characteristics be tabulated at any desired points by the help of vertical transfer lines (Fig. 2-9).

2-4.2 PARAMETER DATA

In addition to information on the static variables, it is necessary to know something of the small-signal behavior of the devices. In the next paragraph the possible small-signal parameters that may be used are considered, and the ones for use in this handbook are selected. In this paragraph the organization of the parameter data for optimizing design effectiveness is examined.

Middlebrook (Ref. 2) and others have shown that the junction transistor requires between 7 and 10 small-

signal parameters for a full representation. Of these parameters, at least 5 are either resistances or conductances, a minimum of 2 are capacitances, 1 may be an inductance, and 1 may be a time-delay corresponding to diffusion time. At frequencies so low that the capacitance and inductance may be neglected, either 4 or 5 conductances (or resistances) may be used to represent the device. Some of these conductances affect the output behavior primarily, and others the input behavior. Because it can be shown that the static data on active devices like transistors are often less stable than are the corresponding small-signal data such as forward admittance, some method of presenting the small-signal data in a form emphasizing their stability should be used. The form should permit ready coordination with the corresponding static relations. This representation can be made on separate graphs, or it can be coordinated with the graphs of static data by superposing

contours of constant-parameter values on them. The present trend is toward provision of more extensive amounts of small-signal data (cf. Amperex and Fairchild data sheets), but the means of coordination are still not completely adequate.

In a coordinated plot, the small-signal data that may be associated with the output curve family conveniently consist of parameters affecting the output behavior of the device, namely, the forward transfer function and the output function. Correspondingly, the small-signal data that are of the most importance with respect to the input characteristics are the input function, and possibly the reverse transfer function. The reverse transfer function is rather inconvenient to measure directly, and in fact it is usually measured indirectly. It is usually determined from values of the parameters y_o and $1/z_o$ (or h_o), the first being the output admittance with the input short-circuited to signal currents, and the second the output admittance with the input open-circuited to signal currents. The value of y_r then is given by the equation

$$\begin{aligned} y_r &= y_i(y_o - h_o)/y_f, \quad \text{or} \\ h_r &= h_i(h_o - y_o)/h_f \end{aligned} \quad (2-2)$$

The value of y_r or h_r may be calculated directly from this equation on the rare occasions that it is required. The contour of constant value for h_r may be plotted on the input family instead of that for y_r . This substitution will be shown to yield a complete set in the next paragraph. Eq. 2-2 may be modified to yield any of the other reverse transfer parameters as required.

2-5 BASIC SMALL-SIGNAL RELATIONS

A considerable variety of different sets of small-signal parameters has been used in the representation of the active behavior of transistors. A similar situation existed to some extent with tubes in the early days, but standardization of parameters was simplified by the fact that the input function and the reverse transfer function both are of relatively little importance with tubes. Since this is not the case with junction transistors and many related devices, it is necessary with them to consider a more complete representation. The purpose of this paragraph is to evaluate the various groups of parameters that have had a reasonable amount of usage, and to determine from the evaluation which set appears to be potentially the most useful for circuit design. In making this determination consideration

must be given to factors such as ease and accuracy of measurement, the optimum measurement configuration, the group that will give the simplest and most direct design procedure consistent with easy extension to high-frequency operation, the relation between the configuration and the physical theory of operation, and the determination of the set that can simplify insofar as possible the problem of design of reliable circuits. As will be evident directly, this analysis leads more toward an admittance (or conductance) type of representation than toward any of the others. The reason the hybrid, or H , parameters have proven satisfactory in many applications is that in many respects they are closely related to the admittance parameters. As noted by Armstrong (Ref. 3), their deficiencies as high-frequency parameters are largely a result of deviations from a pure admittance form.

Basically, the easiest approach to the representation of a network device is based on the examination of the various forms of its equivalent network representations to find a configuration that conforms relatively well with the physical behavior of the device and at the same time gives a realizable equivalent network for use with a set of small-signal parameters amenable to direct and reasonably accurate measurement. Once the basic arrangement has been selected, then the modifications required to realize the maximum usefulness of the selected parameters may be made, including the modifications required to correct for such unideal properties as base-spreading resistance.

Network representation of an active device, commonly based on the so-called black box*, is based on one of the following sets of equations (Fig. 2-10)

$$\begin{aligned} i_i &= y_i v_i + y_r v_o \\ i_o &= y_f v_i + y_o v_o \end{aligned} \quad (2-3)$$

$$\begin{aligned} i_i &= g_i v_i + g_r v_o \\ i_o &= g_f v_i + g_o v_o \end{aligned} \quad (2-4)$$

*The name "black box" is used to signify that the type or configuration of components within a specified closed black line or "box" need not be known exactly to specify the external current-voltage relations at each of the ports. This independence of internal configuration may not be valid except at a fixed frequency if the magnitudes of the capacitance and inductance components are to be independent of frequency. A symmetrical set of current and voltage equations is used in conjunction with terminal and transfer immittances. One of the chief assets of the three-terminal, two-port, black-box configuration is the ease with which it can be modified to take account of changes of the external circuit configuration. Such a change is the change of the common terminals. (Some authors have been calling this by the name "opaque box".)

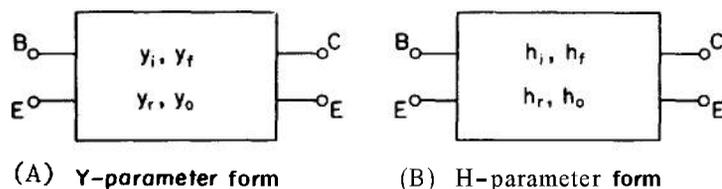


Fig. 2-10. Transistor Black-box Representation

for the admittance and conductance form of the equations, respectively. (The long-standing use of g as the symbol for conductance in electrical engineering dictates the form of Eq. 2-4. The use of g as the symbol for the inverse H parameters for this reason is not adopted in this book. It has received little acceptance in IEEE standards and is used relatively little.) The hybrid form of the equations is

$$\begin{aligned} v_i &= h_i i_i + h_r v_o \\ i_o &= h_f i_i + h_o v_o \end{aligned} \quad (2-5)$$

Another set sometimes used is the impedance set

$$\begin{aligned} v_i &= z_i i_i + z_r i_o \\ v_o &= z_f i_i + z_o i_o \end{aligned} \quad (2-6)$$

The remaining two sets, commonly used with cascaded networks, are seldom used with transistors. They are often used with lattice networks.

There are a number of sets of parameters that do not fit closely in the black-box pattern, the most important being those originally introduced with the point-contact transistor, a special set of resistance parameters. These parameters proved quite satisfactory with point-contact transistors, and also are reasonably satisfactory for low-frequency circuits using junction transistors, but their values are difficult to measure directly. The value of the mutual resistance r_m is particularly difficult to measure because there is no way of making it directly accessible at the terminals of the device. In addition, the value of r_c is difficult to measure because of its very high value, typically many megohms.

2-5.1 THE H PARAMETERS

The H parameters include one impedance parameter, one admittance parameter, and two dimensionless parameters that may be determined in terms of the ratio of two admittances or two impedances as desired. The termination conditions for each of the four H parameters, and also the termination conditions for the other black-box parameters are tabulated in Table 2-2. In this table, a notation of infinite impedance indicates that the terminating impedance should be a minimum of 10 to 100 times the nominal impedance level at the specified port, and zero that it should be well less than a tenth the nominal impedance at the port, and less than a hundredth if possible. The values marked large and small should be selected to make possible good bridge balance relations. For that reason, they cannot be specified more closely.

An examination of Eq. 2-5 shows that h_i is a small-signal impedance, h_o is a small-signal admittance, and the ratios, h_f and h_r , are current and voltage ratios, respectively. Now, the use of an impedance for h_i is inconsistent with the nature of the transistor because when base-spreading resistance is neglected the input immittance can be shown to be characterized by a parallel resistance-capacitance combination (Refs. 1, 4). Such a parallel combination is more conveniently represented by an admittance of the form $g_i + jb_i = g_i + j\omega C_i$ than it is in the form

$$(r_i - j\omega C_i r_i^2)/(1 + \omega^2 C_i^2 r_i^2)$$

where $r_i/(1 + \omega^2 C_i^2 r_i^2)$ is the resistive component of h_i in terms of the capacitance of the transistor and its shunt resistance, and the equivalent series capacitance is

$$C_i \langle 1 + 1/(\omega^2 C_i^2 r_i^2) \rangle$$

Naturally, both of these expressions represent the same immittance, but both components of h_i are strongly dependent on angular frequency, whereas in the admittance form only the conductance g_i is weakly dependent on frequency. This dependence corresponds in general behavior to the transit time conductance in tubes, rising linearly with frequency, from a frequency in the neighborhood of $\frac{1}{\tau}$ —which in a later paragraph is defined as the noise corner frequency f_{n2} (Ref. 5).

The output admittance term for the set of H parameters is represented by a combination of a parallel capacitance and resistance. Strictly, the capacitance from the collector is divided between the base and the emitter in a transistor, with the larger component normally being to the base. These two capacitances are paralleled in the output admittance function, but they divide, one being part of the feedback immittance with the H parameters. No difficulties are encountered in the use of the h_i parameter with transistors.

The forward transfer ratio for the H parameters measures the current gain of the transistor, and is a useful number in its own right. It has considerable similarity to the mu (μ), or amplification factor for tubes, in that it is relatively constant over the full operating range of the transistor. It does vary in value slowly as the total current through the transistor increases, because the voltage gradients in the base region reduce the active region of the device quite rapidly as the total current is increased.

The forward transfer ratio is commonly known by a number of different names, including the β in the common-emitter configuration, and the a in the common-base configuration. It is also known by the symbols,

h_f or h_{fe} and h_{fb} , for common-emitter and common-base configurations, respectively. The value of h_f or β is usually included in the tabulated data for any transistor.

The reverse transfer ratio, or reverse voltage gain, varies in value as a function of operating conditions, and is rather inconvenient to measure. Its value is small compared to the values of h_i and h_f , but not necessarily with respect to h_r . It is for that reason difficult to handle when transformations of configuration are being made in H parameters. The use of parameters and a configuration that render the reverse transfer immittance negligible compared to the remaining three immittances can significantly simplify transistor circuit design.

2-5.2 THE TEE PARAMETERS

The tee parameter configuration may be established in either one of two different forms, the one using a current generator, and one using a mutual resistance r_m . The former is used with point-contact transistors, the latter with junction transistors. The current-generator form has also found use in the analysis of high-frequency circuits for junction transistors. Because of the difficulties encountered in measuring the magnitudes of the resistance values for the tee parameters—in particular r_m , r_c , and r_d —they are more commonly used as an aid to circuit analysis than in design. A modified form containing both resistance and conductance terms may also be used in this way. Fig. 2-11 shows the commonest form of equivalent network. Since this ar-

TABLE 2 2
TERMINATION CONDITIONS

Parameter	Termination		Parameter	Termination	
	Input	Output		Input	Output
h_i	Z large	$Z = 0$	y_i	Z large	$Z = 0$
h_o	$Z = \infty$	Z large	y_o	$Z = 0$	Z large
h_f	Z large	$Z = 0$	y_r	Z small	$Z = 0$
h_r	$Z = \infty$	$Z = 0$	y_c	$Z = 0$	Z small
			r_c	$Z = \infty$	Z large
z_i	Z large	$Z = \infty$	z_f	$Z = \infty$	$Z = \infty$
z_o	$Z = \infty$	Z large	z_r	$Z = \infty$	$Z = \infty$

rangement does not have the properties of a black-box representation, the conversion from one common electrode to another offers difficulties in addition to the measurement problems.

2-5.3 THE Z PARAMETERS

The impedance equations express the circuit relations for one form of black-box representation in which all the parameters are dimensionally the same. These parameters have been used to some extent in the design of low-frequency circuits, and they do fall within the group that can be measured directly with a comparatively simple bridge. Since the representation of an impedance, $Z = R + jX$ takes the form of a series combination of resistance and reactance, and transistor immittances tend to behave as parallel combinations, this set of parameters is of limited usefulness.

2-5.4 THE PI PARAMETERS

The pi parameters, sometimes called the Giacoletto parameters, have been developed to represent the physical characteristics observed in junction transistors. As a consequence, they provide a good delineation of the characteristics of the devices. They are made up of a set of conductance and susceptance elements in conjunction with a resistance, the base-spreading resistance, and they are in many ways interchangeable with the admittance parameters discussed in the next paragraph. As shown in Fig. 2-12, the transistor is represented by a set of admittances arranged in a typical pi configuration.

The pi parameters are based on admittances for the common-emitter configuration, and are somewhat more complex to convert to other configurations than are black-box arrangements. They can be modified into a current-generator form, or they can be used with the current generator replaced by a forward conductance. They make an excellent basis for representation in the analysis of high-frequency circuits.

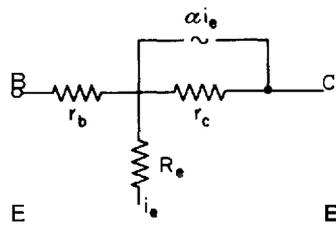


Fig. 2-11. Tee Equivalent for a Transistor

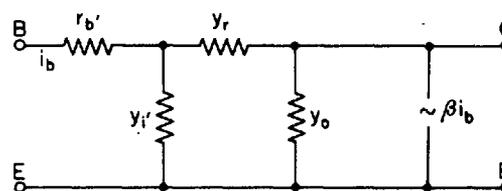


Fig. 2-12. Pi Equivalent for a Transistor

The individual parameters include, in addition to the base-spreading resistance, the input admittance, the forward admittance, which is the equivalent of the transconductance in a tube, the output admittance, which is equivalent to the plate conductance, and a feedback admittance. The value of the forward admittance is roughly proportional to the emitter current in the device, and consequently is also proportional to collector current to a reasonable approximation. The input admittance has a value that is likely to differ widely from one device to the other, rather than having a value which is nearly the same from device to device as with the forward admittance. Because of this difference in behavior, the separate data given for the two admittances simplify circuit design.

The output and the feedback admittances also have relatively wide ranges of variation. In addition to the variation from device to device, the value of the output admittance has an apparently rapid variation with frequency. Actually, this latter variation is a result of feedback action. If either r_b , or the feedback admittance is zero, then the output admittance is rather well-behaved as a function of frequency.

2-5.5 THE Y OR G PARAMETERS

The Y parameters, which at low frequency reduce to the G parameters, have many points in common with the pi parameters just discussed, and they have points in common with the hybrid parameters as well. Like the impedance parameters, the basic Y parameter set is homogeneous in that all four are admittances. And, like the output parameter of the hybrid group and the input and output parameters of the pi group, both the input and the output parameters of this group are represented by a parallel combination of conductance and susceptance.

The admittance parameters are defined by the equations

$$i_i = y_i v_i + y_r v_o \quad (2-3)$$

$$i_o = y_r v_i + y_o v_o$$

$$\begin{aligned} i_i &= g_i v_i + g_r v_o & (2-4) \\ i_o &= g_f v_i + g_o v_o \end{aligned}$$

For the present discussion, the susceptance components are neglected, and Eq. 2-4 used instead of Eq. 2-3. The basic form of the equations shows that the parameters may be determined by voltage and current measurements at the terminals. Because the currents in any transistor are determined by the relation given in Eq. 2-1

$$i_b + i_e + i_c = 0 \quad (2-1)$$

it is evident that if in Eqs. 2-3 and 2-4 i_i is taken to be i_i and i_o as i_c , Eq. 2-4 may be converted to the form that gives the relations in terms of the emitter current as input and the collector as output by a simple addition

$$\begin{aligned} i_i + i_o &= i_b + i_c = (g_i + g_f)v_i + (g_r + g_o)v_o = -i_e \\ i_o &= g_f v_i + g_o v_o = i_c \end{aligned} \quad (2-7)$$

Since $v_i = v_b = -v_{eb}$, and the emitter current has a negative sign in the first of the equations, and since the output voltage must be replaced by $(v_c - v_e)$, the equations take the form

$$\begin{aligned} i_e &= (g_i + g_f)v_o - (g_r + g_o)(v_c - v_e) \\ &= \sigma(g)v_o - (g_r + g_o)v_c & (2-8) \\ i_c &= -(g_f + g_o)v_c + g_o v_e \end{aligned}$$

where $\sigma(g) = g_i + g_f + g_r + g_o$. In a similar manner, the equations may be rewritten in terms of the base and the emitter currents

$$\begin{aligned} i_b &= g_i v_b + g_r v_e & (2-9) \\ i_e &= (g_i + g_f)v_b + (g_r + g_o)v_e \end{aligned}$$

From these equations, making a substitution to get v_c in terms of v_e , the modified form becomes

$$\begin{aligned} i_b &= g_i v_b + (g_i + g_r)v_e & (2-9a) \\ i_e &= (g_i + g_f)v_b + \sigma(g)v_e \end{aligned}$$

A substitution table, Table 2-3, may be prepared showing the substitutions required to convert the common-emitter equations into the correct form for the common-base or the common-collector configurations.

For each configuration, the A factor takes the same form for admittance and for impedance parameters. The σ factor is the sum of the admittances

$$\sigma(y) = y_i + y_f + y_r + y_o$$

The A factor is clearly independent of configuration because it has the same value for each arrangement. The modified output parameters, which are components of the A factor, are included for completeness in Table 2-3, and are discussed in detail in the next paragraph.

The parameter conversions for the hybrid parameters are again based on the current node equation, Eq. 2-1, in terms of the basic equations for the Hparameter configuration

$$\begin{aligned} v_i &= h_i i_i + h_r v_o & (2-5) \\ i_o &= h_f i_i + h_o v_o \end{aligned}$$

These equations must first be solved for the appropriate value of i_i , or i_b , and i_o , or i_c before they may be used in conjunction with Eq. 2-1 in a configuration change. When this is done, the equations take the form

$$\begin{aligned} i_i &= v_i/h_i - (h_r/h_i)v_o & (2-5a) \\ i_o &= (h_f/h_i)v_i + (h_o - h_f h_r/h_i)v_o \end{aligned}$$

In this form, the currents can be combined as desired to provide the correct values of currents for the common-base and the common-collector configurations if the original equations represent the device in the common-emitter arrangement. As is readily evident, the equations for the hybrid parameters do not lend themselves readily to this type of transformation, but give

TABLE 2-3
PARAMETER CONFIGURATION CONVERSIONS

Parameter	C-Emitter	C-Base	C-Collector
Input	Y_i	$\sigma(y)$	y_i
Forward	y_f	$-(y_f + y_o)$	$-(y_i + y_r)$
Reverse	y_r	$-(y_r + y_o)$	$-(y_i + y_r)$
output	Y_o	y_o	$\sigma(y)$
Mod. output	y_o	$y_i y_o / \sigma(y)$	y_c
A factor	$y_i y_o - y_f y_r$	$y_i y_o - y_f y_r$	$y_i y_o - y_f y_r$

rather complicated coefficients. The corresponding transformation is simple and direct with admittance parameters, and the modified Eqs. 2-5a actually are the basic equations for the admittance relations, but in terms of the hybrid coefficients.

Factors that affect the selection of the parameters for use with an active device include the ease of measurement of the important characteristics, the precision with which they can and must be measured, the reliability with which they can be measured, and the configuration in which they can best be measured. In the paper by Follingstad (Ref. 6) the conclusion is drawn that the hybrid parameters show somewhat better reliability than the admittance parameter data, and that they are better than the impedance parameters. A re-examination based on the optimum circuit configuration for the determination of the minimum set of device parameters in a form that is independent of the circuit configuration permits the development of a somewhat different order for the utility of the hybrid and admittance parameters. If the optimum set is taken as y_i, y_f, y_o , and either y_c or h_r (they are the same), it develops that this set in the common-emitter configuration can be measured with a precision well within the required tolerances.

Ideally, the admittance parameter set that can be shown to be most convenient to use includes the input, the output, the forward admittance, and the admittance A factor. The operating equations derived in the fourth and later chapters use these four parameters to the almost complete exclusion of the reverse admittance. Because of the fact it is almost impossible to measure the A factor directly, however, the use of a modified set of admittance parameters, which minimizes the calculation required to determine the A factor, is indicated. Such a set is discussed next.

The modified Y parameters. This set of admittance parameters can satisfy both the problems of measurement accuracy and also those of design simplification, giving the advantages of both the hybrid and the admittance parameters. At the same time they relax the precision required on measurement of parameters con-

siderably compared to either the H or the normal Y parameters because of the elimination of the differencing of a product that may be required in the calculation of the value of the A factor.

The first three parameters of this set, $y_i, y_f,$ and y_o , are identical with the corresponding parameters of the regular admittance set, and the fourth is identical with the output admittance in the hybrid system h_r . As a matter of convenience and to keep a consistent pattern of notation, this parameter is identified by the new symbol y_c . This parameter always appears in conjunction with the input admittance in the form $(y_i y_c)$, and this product has already been shown to be the invariant known as the A factor. An examination of the corresponding relations for the hybrid parameters shows (Table 2-6) that no such convenient interrelations exist among the hybrid parameters.

The principal forms of terms in which the parameter y_r appears are the A factor and the σ factor

$$\Delta(y) = y_i y_o - y_f y_r \quad (2-10)$$

$$\sigma(y) = y_i + y_f + y_r + y_o \quad (2-11)$$

In Eq. 2-11, the term y_r and usually the term y_o may be neglected compared to the remaining terms because of the relations of their values in the common-emitter configuration

$$y_f > y_i \gg y_o > y_r \quad (2-12)$$

Consequently, the use of $\Delta(y)$ and $\sigma(y)$ can simplify many calculation problems in design of transistor circuits.

The discussion to this point has neglected the presence of the base-spreading resistance in practical transistors. At low frequencies, appreciably below the β -cutoff frequency, such a procedure is convenient and useful. Strictly, however, it is necessary to take the admittance parameters as the values for an intrinsic

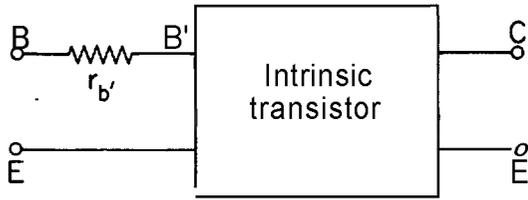


Fig. 2-13. Effect of Base-spreading Resistance

ideal transistor and to extract the base-spreading resistance as a separate entity in higher-frequency applications. The effect of this change is considered in the next few paragraphs.

2-6 COMPLETE SMALL-SIGNAL RELATIONS

The complete representation of a typical transistor in terms of small-signal parameters requires the inclusion of the base-spreading resistance, and it requires the correction of the internal admittance parameters to compensate for the effect of this resistance, Fig. 2-13. Since the input admittance of the transistor is finite rather than zero, a loss of input voltage occurs across this resistance and the input admittance also is altered by it. The net input admittance for a transistor having base-spreading resistance is given by the equation

$$y_i = 1/(r_{b'} + 1/y_{i'}) = y_{i'}/(1 + y_{i'}r_{b'}) \quad (2-13)$$

where the primes indicate the internal values of the admittances. This equation may also be solved for the internal admittance in terms of the terminal value

$$y_{i'} = y_i/(1 - y_i r_{b'}) \quad (2-13a)$$

The differencing in the denominator of this equation shows that difficulties may be anticipated in the determination of accurate values of $y_{i'}$ under high-current conditions.

In a similar manner, the portion of the input voltage that is effective in producing an output current change is that which is applied across $y_{i'}$. Its value may be found to be determined by the equation

$$v_{b'}/v_b = 1/(1 + y_{i'}r_{b'}) \quad (2-14)$$

Then the effective terminal transconductance or transadmittance is given by the equation

$$y_f = y_{f'}/(1 + y_{i'}r_{b'}) \quad (2-15)$$

or

$$y_{f'} = y_f/(1 - y_i r_{b'}) \quad (2-15a)$$

Fortunately, the value of $r_{b'}$ is relatively constant, so that the correction of the measured values of g_i and g_f to the internal values is relatively simple.

2-7 CONSIDERATIONS AFFECTING PARAMETER SELECTIONS

In the previous paragraphs, the parameters that can be used for representation of the small-signal behavior of transistors have been considered, and their properties in design briefly discussed. In this paragraph, the relations of the parameters to the physics of junction transistors and factors affecting their measurement are analyzed in more detail.

Many writers have pointed out that there is no particular need for the set of small-signal parameters used to have any significance to the physics of the device. If, however, a set can be selected that can both represent the device physically and at the same time provide useful data more convenient to use for circuit design, then many advantages in the ease of use result. Ease of measurement is likewise of great importance, because the design data must be readily obtainable.

Reference to the derivations of the characteristics of transistors in terms of junction geometry shows that the input and output relations in a transistor are determined in terms of admittance relationships, with the input circuit being the emitter, and the output the collector (Refs. 1, 4). The equations for the emitter current and the collector current in particular are expressed in terms of changes of barrier potential with respect to the Fermi potential: The general equations for base and collector currents, as given by Lo and Endres, are as follows (Lo, Eq. 7-1)

$$I_B = \sigma(G) - \{ \exp[\Lambda(V_B - I_B r_{b'})] \} (G_{11} + G_{21})/\Lambda - \{ \exp[\Lambda(V_C + I_B r_{b'})] \} (G_{12} + G_{22})/\Lambda \quad (2-16)$$

$$I_C = - (G_{21} + G_{22})/\Lambda + [\exp(\Delta I_B \gamma_b)] \quad (2-17)$$

$$\times [G_{21} \exp(-\Delta V_B) + G_{22} \exp(\Delta V_C)]$$

where the $\sigma(G)$ has the value $\sigma(G) = G_{11} + G_{12} + G_{21} + G_{22}$ and the values of the G 's are defined by the equations (Lo, Eq. 8-26)

$$G_{11} = b\sigma_i^2 [\coth W/L_p + \sigma_n L_p / \sigma_p L_n] / [(1 + b)^2 \sigma_n L_p] \quad (2-18)$$

$$G_{21} = -b\sigma_i^2 [\operatorname{cosech} W/L_p] / [(1 + b)^2 \sigma_n L_p] \quad (2-19)$$

$$G_{12} = -b\sigma_i^2 [\operatorname{cosech} W/L_p] / [(1 + b)^2 \sigma_n L_p] \quad (2-20)$$

$$G_{22} = b\sigma_i^2 [\coth W/L_p + \sigma_n L_p / \sigma_p L_n] / [(1 + b)^2 \sigma_n L_p] \quad (2-21)$$

and the symbol definitions are

- W = base width
- L_p = hole diffusion length
- σ_n = n-type conductivity
- σ_p = p-type conductivity
- σ_i = intrinsic conductivity
- L_n = electron diffusion length
- $\sigma_{p'}$ = collector p-type conductivity
- $L_{n'}$ = collector electron diffusion length
- b = ratio of mobilities of electrons and holes $\doteq 2.1$ for germanium
- $\Lambda = q/(kT)$

These equations as they stand apply to a **PNP** transistor. To obtain the corresponding equations for an **NPN** unit, it is necessary to interchange the p and n subscripts throughout, and to invert b to give the ratio of the mobilities of the holes and electrons.

It is important to note that these equations take the form of nonlinear admittances throughout, in that they reduce on expansion of the exponentials to an expansion of either base or collector current in terms of first and higher powers of the applied voltages, V_B and V_C . Consequently, it would appear that the devices behave as nonlinear admittances. Additional corroborating information can be noted in the fact that the

irregularities in the diffusion of carriers through the base region introduce an effective capacitance, the diffusion capacitance, in parallel with the input conductance, and a similar capacitance whose magnitude is dependent on voltage is introduced by the boundary charge fields for the device.

The diffusion capacitance is a function of the emitter and base currents because it measures the irregularity or granularity of the current flow through the base region. The ratio of the conductance to the capacitance at the input of a transistor is expressed in terms of the lifetime of the minority carriers in the base region (Lo, Eq. 8-46)

$$g_{Dp}/C_{Dp} = 1/\tau_p \quad (2-22)$$

where τ_p is the lifetime. The magnitudes of both the capacitance and the conductance are proportional to the square of the ratio of the base width to the mean-free-path, $(W/L_p)^2$ or $(W/L_n)^2$, depending on whether the transistor is a **PNP** unit or an **NPN** unit, respectively. If the capacitance depended only on the first power of the ratio, then the diffusion time of the particle across the base would be the prime factor controlling the capacitance. Because it depends on the square of the ratio, however, one can deduce that an additional factor dependent on the uniformity of flow must be considered. The second (W/L) factor, for small values of the ratio, is an approximation to the expansion of the decay exponential $[1 - \exp(-W/L)]$.

The transition capacitances in transistors develop as a result of the stresses across the junctions themselves. The emitter transition capacitance, across the forward-biased base-emitter junction, is large because of the small forward voltage applied to the junction, whereas the collector capacitance is quite small because of the relatively large reverse bias across the collector junction. This capacitance may be represented by the equation (Lo, Eq. 7-2)

$$C_T = AV^{-n} \quad (2-23)$$

where A is an arbitrary constant dependent on the semiconductor material and its processing, and the expo-

ment n is typically 0.5 or 0.333, depending on the distribution of the impurity atoms in the neighborhood of the emitter or the collector junction.

The conductivity of the base region as determined externally depends on the square of the ratio of the base width to the mean-free-path, just as does the diffusion capacitance. As with the capacitance, if recombination irregularities did not contribute to the current, and to the conductivity, this factor would depend strictly on the volume of the active base region. Because the ratio is squared, however, the recombination irregularities are a prime cause of the base current. The same exponential relation given in terms of its first-term expansion applies

$$(W/L) = [1 - \exp(-W/L)] \quad (2-24)$$

In addition to this internal conductance in the base region of a transistor, a finite amount of resistance must of necessity be present between the active region of the base and the base-lead connection. This resistance, known commonly as the base-spreading resistance, would be small except for the fact that the base material must have a very small value of conductivity if the magnitude of the input conductance is to be kept small. If the base conductivity is large, then the recombination of minority carriers takes place more rapidly, and a considerable portion of the emitter current may flow out the base lead instead of flowing on to the collector. The resulting short lifetime of the carriers makes transistor action possible only in devices having extremely thin base layers.

The electrical properties of the transistor, which must be represented by the data and the representing equivalent circuit, can be tabulated in terms of the following parameter relations:

1. A forward admittance, which at low frequencies is approximately proportional to emitter current

$$g_f \doteq 35 \times I_e (\text{in mA}), \text{ mmoHs} \quad (2-25)$$

2. An input admittance roughly proportional to base current for currents, such that $r_b' < 1/g_i'$

3. Transition capacitances, which are a function of junction voltages

4. A diffusion capacitance that is proportional to the emitter current

5. Output admittances g_o and g_c , which are functions of both collector voltage and collector current

6. A base-spreading resistance, which is relatively constant but not completely so.

2-8 MEASUREMENT CONSIDERATIONS

Follingstad (Ref. 6) has made an extremely thorough analysis of the measurement of transistor parameters, and has determined the accuracy limitations that apply to them (Ref. 6). These results show that the best accuracy in measurements in general can be obtained using certain hybrid parameters and using some admittance parameters in the common-emitter configuration. On the basis of this, Follingstad has concluded that the hybrid parameters, because a greater variety of them are amenable to acceptable measurement, are better.

Further examination of Follingstad's data, however, shows that in the common-emitter configuration, some of the admittance parameters may be measured with somewhat greater accuracy and reliability than the hybrids, and others with roughly equal accuracy. Because the years of experience in the use of transistor devices since Follingstad's paper have shown that the common-emitter configuration permits the measurement of device parameters with a minimum of dependence on circuit parameters, a re-examination of the conclusions drawn appears desirable.

The desirability of the use of admittance parameters is supported by both practical and theoretical considerations. Among the practical considerations is the availability of high-frequency measuring devices for measuring the values of the given set of parameters. A number of organizations, among them General Radio and Wayne-Kerr, for example, have developed bridges designed for admittance measurements on high-frequency devices, both passive and active. The reason that admittance measurements were selected is readily discernible from some of Follingstad's curves, because he shows that both h_{11} and h_{12} are marginal for low values of base current, whereas both y_i and y_o can be measured with adequate accuracy. The data in Table 2-4 are condensed from the curves, and a replot from his curves in Figs. 2-14, 2-15, and 2-16.

In Table 2-4, region 1 is the current-cutoff region, 1-2 the weak-conduction region adjacent to region 1, region 2 is the strong conduction region, and 3 the low- β saturation region, and the classifications of accuracy are:

TABLE 2-4
EXPECTED ACCURACIES OF PARAMETER MEASUREMENTS

Parameter	Region	H-CB	H-CE	Y-CB	Y-CE
Input	1	3	3	1	1
	1-2	2	3	1-2	1
	2	1	2-3	2-3	1
	3	1-2	1	3	2-3
Forward	1	3	2-3	1	1
	1-2	1	1	1	1
	2	1	1	1-3	1
	3	2	2-3	3	1-3
Reverse	1	3	3	1	1
	1-2	2	3	2	1
	2	1	3	3	1
	3	1	2	3	1-3
output	1	1	2-3	1	1
	1-2	1	1	1	1
	2	1	1	1-2	1
	3	2-3	2-3	3	2

- 1. error less than 0.5%
- 2. error between 0.5 and 2.0%
- 3. error greater than 2.0%.

Clearly, in all regions except region 3, the accuracy of all of the Ydata is excellent (common-emitter configuration). The accuracy of the h_o data is generally adequate, particularly grounded base, but the rest of the h parameter data is rather spotty, good here and bad there.

The basic data given by Follingstad have been replotted in Figs. 2-14, 2-15, and 2-16 to show in more detail the comparative accuracies available for the common-base and common-emitter configurations. Fig. 2-14

shows the data for $g_i, g_f, g_o,$ and $h, , CE,$ and Figs. 2-15 and 2-16 show the accuracy curves for h_i and h_r in the common-emitter configuration, and several of the parameters in the common-base configuration. Because the curves are for sweep measurements, bridge methods can give a further improvement of accuracy.

The adequacy of the set of parameters selected for representing transistors must be measured against the tolerance requirements in their use in design, and their stability with time and from device to device. The most important design parameter should if possible be one of great stability so that the design may be oriented for reliability by keeping dissipations conservative and by allowing ample margins for the less-important parame-

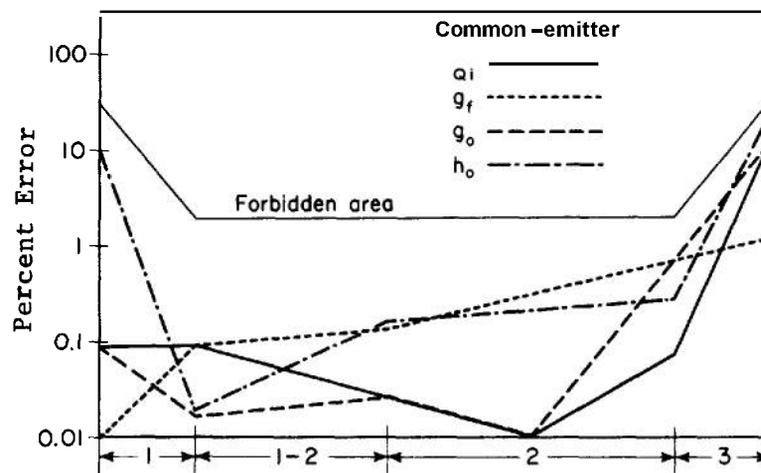


Fig. 2-14. Parameters With Satisfactory Tolerances

ters. The use of y_f and y_i provides just such a separation. The value of y_i is relatively smaller and less stable than the value of y_f , which is the parameter that controls the output current, the two being the most important parameters in design of most transistor circuits.

2-9 GENERALIZED CHARACTERIZATION OF ACTIVE DEVICES

Eqs. 2-16 and 2-17 can be generalized from the modified common-base form given in terms of base and collector currents and the corresponding voltages. (As has been done in these equations, V_{EB} in Lo's equations may be replaced by $-V_B$, and when the value of

V_{CB} is large compared to V_B , the value of V_{CB} , which is normally taken with respect to the base, may be replaced by the collector-to-emitter voltage V_C . If the value of V_C is small, the conversion to common-emitter requires the replacement of the V_C with the expression $(V_C - V_B)$, where the new V_C is measured from collector to emitter.) The modification of these equations must first take account of the bias potential barrier developed in the base region as a result of high-injection conditions, by replacing the Fermi parameter A by the modified Fermi parameter A' , in the form:

$$A' = A(1 + m) \tag{2-26}$$

where the m factor, having a magnitude less than one-

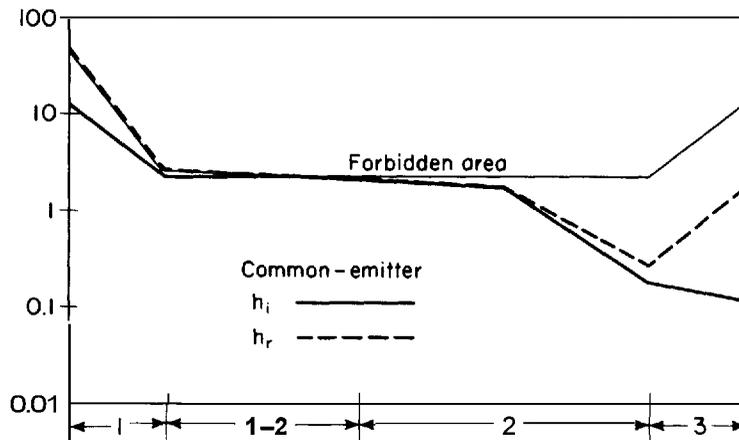


Fig. 2-15. Unsatisfactory Parameters

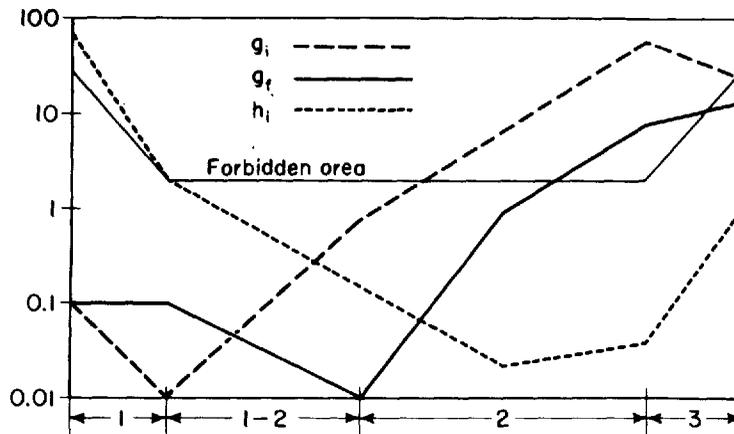


Fig. 2-16. Tolerances With Common-base Configuration

half, makes correction for the barrier potential developed between the base region and the base lead as a result of changes in doping level resulting from the flow of majority carriers into the base to maintain electrical neutrality.

This equation may be further generalized, however. It can then be applied correctly to other kinds of solid-state active devices, including electron tubes. When this is done, the $(1 + m)^{-1}$ is replaced by the kappa parameter mentioned in Chapter 1. Doing this leads to an efficiency factor κ which may have values in excess of unity under high-injection conditions with an NPN transistor. The value is somewhat less than two with the NPN device, and somewhat greater than 0.7 with the PNP device.

With electron tubes and field-effect transistors, the value of κ may be nearly unity with structurally perfect devices at very small values of current (when the current channel is of infinitesimal thickness), but it may decrease to values less than 0.001 at very high values of current. As is noted in Chapter 1, this condition is essential for the development of efficient high-power transmitting devices, tubes or solid-state. Only when the impedance levels and voltage levels can be made sufficiently high can substantial amounts of power be controlled conveniently.

The real advantage in use of both the efficiency factor and the Fermi parameter in device characterization is that they both are largely independent of extraneous environmental parameters and phenomena. The value of κ does depend on current flow in the output terminal of the active device, but it otherwise is largely independent of environment. (It can be affected by the introduction of lattice disruptions from nuclear radiation, since disruptions, by encouraging recombination, tend to reduce output current. Nonetheless, the variation of the κ at a given current level with the integrated radiation level is small unless the device virtually has been destroyed.)

For an NPN transistor, the value of κ under high injection may be as much as 1.7; for a PNP transistor it approaches 0.7. The change in κ values from unity for germanium transistors is somewhat less than for silicon. The exact values depend on the semiconductor material, and also on device polarity. The current level at which this transition takes place is dependent on the current level required to produce a substantial change in the density of the majority carriers in the base region of the transistor. (Strictly speaking, the distribution of the total number of majority carriers in the entire active base region must change substantially.) This change of density introduces a contact-potential effect between the junction region and the terminal and either in-

creases or decreases the effective Fermi potential Λ^{-1} . It clearly would be helpful to know more about the nature of this transition region in practical devices, and to have data and curves on typical devices.

The reason for the behavior of the κ factor as a function of device current which is noted with electron tubes and field-effect transistors is simply that electrostatic shielding prevents the control field applied to the grid or the gate from affecting current flow in the middle of a wide channel. If a column of electrons or other charge carriers are moved from one place to another under the guidance of an electrostatic guiding field, this field will have an influence on only the outermost layers, and carriers within the column will be shielded from the field by charges adjacent to them. The deeper within the column, the more complete the shielding, and the smaller the influence of the controlling field on the carriers. For this reason, unless the column of charge carriers is of infinitesimal thickness, the central charge moves uncontrolled, and does not obey the solid-state equations governing charge motion. It is for this reason that the κ -factor is called an efficiency factor, as it actually indicates in a general way the efficiency with which the field can control total current flow.

With field-effect transistors, it is at least theoretically possible to limit the central, or uncontrolled, component of current by grading the density of polar molecules to have a distribution proportional to the function $(e^{\lambda x} + e^{-\lambda x})/\lambda$ with respect to the channel centerline. If the value of λ is sufficiently large, it is possible theoretically to maximize the current density against the depletion region and keep it minimized in the channel center. In this way, field-effect transistors having values of κ approaching unity under normal operating conditions theoretically can be designed.

Field-effect devices readily can be shown to have values of κ approaching unity for diode-type devices at small currents, and that they have values approaching at least 0.5 for insulated-gate devices under similar conditions. Analytically, this condition can be shown to depend on the existence of the potential jump across the Debye region bounding the depletion zone in the channel. When the electric field across the Debye region exceeds that in the adjacent depleted zone, the current control obeys the Fermi admittance equation:

$$y_{f\bullet} = \Lambda I_d \quad (2-27)$$

with a value of κ being in the range between 0.5 and 1.0. When the field in the adjacent depleted zone exceeds that across the Debye region, then the conventional

Shockley admittance equation applies, and the value of κ in Eq. 2-27 will be typically less than 0.2.* It may be much, much less than 0.2, by several orders of magnitude in some instances. Clearly, knowledge of the manner of variation of κ with device current can be of prime importance in the study and design of reliable circuits.

All active devices presently available have a transmission delay time associated with their amplification action. In the normal theory, this delay is represented by a transmission line. The delay time is a consequence of the fact that the point of control and the point of utilization of the current flowing cannot be made to coincide and, as a result, a small—but finite—time is required for the effect of control to be observed at the output. Careful measurements of delay time with bipolar transistors has shown that under small-signal conditions this delay is essentially independent of device currents and voltages. A similar situation on delay time can be expected to be true with field-effect transistors, and it is approximately true with tubes.

The input characteristics for the general active device have a wider range of variation than do the corresponding transfer characteristics. The input admittances for field-effect transistors and electron tubes, for example, are largely capacitive (except at very high frequencies). On the other hand, the input characteristics for the bipolar transistor are substantially more complex because of the relatively high input admittance and the series spreading resistance which are encountered.

Practically, it is possible to represent the general active device in terms of an intrinsic immittance “opaque” box (sometimes called a black-box representation) and an imbedding network which includes the relatively stable parasitic immittances representing the balance of the network. With admittance-type devices, the parasitic elements are generally series, or impedance, elements (the capacitance from input to output can be an exception), whereas with impedance-type devices, the parasitic elements tend to be parallel, or admittance, elements.

The reason for the nature of the parasitic elements is relatively easily determined. A parallel or shunt admittance connected to an intrinsic admittance device readily can be absorbed directly into the opaque-box representation unless it is isolated by series elements from the intrinsic device. Similarly, series elements readily can be lumped into an impedance intrinsic device without affecting the overall structure. The evident consequence of this is that a full representation of an

immittance-type device includes both the intrinsic active device surrounded by alternating shunt admittance imbedding nets and series impedance nets, the innermost being the dual of the active device itself. In fact, this discussion and description apply to active devices with any number of terminals, starting with tunnel diodes (which are negative admittance devices), and continuing through transistors and more sophisticated active arrays.

With bipolar transistors, the most important parasitic elements include the spreading resistances— r_b' , r_e' and r_c' —and the associated inductances, and possibly the feedback capacitance. With field-effect transistors and tubes, lead inductance and resistance and feedback capacitances are the more important parasitic elements. (Cathode-interface impedance also can be critical with tubes.) Transit-time effects become important with all three at high frequencies.

Three limiting frequencies are really vital to the operation of all these devices. The first two of these are the noise corner frequencies mentioned in Chapter 1. The lower of these is the frequency below which noise in excess of that predicted by thermal noise can be expected to occur. The increase of noise below this frequency is an inverse function of frequency in that it increases with decreasing frequency. Different kinds of devices appear to obey different laws in this region—linear, root, or power.

The second noise corner frequency is that frequency above which the “granularity” of current flow introduces added noise. This frequency really limits the usefulness of the device as a low-noise RF amplifier, and it also establishes an oscillation limit frequency in terms of an R-C or multivibrator-type configuration. Circuits which must operate with a minimum of added noise should use devices operating between these two noise frequencies, f_{n1} (the lower), and f_{n2} (the upper). Values for the respective frequencies are seldom available.

The third frequency of importance, called the maximum oscillation frequency f_{max} , is the maximum frequency at which the transistor, when imbedded in an appropriate lossless network, can deliver a unity power gain from output to input. In other words, the active device can just supply the losses of the input in such a phase as to maintain oscillation. This frequency is often provided for devices whose application is expected to be with RF equipment, but it may not be given for switching transistors, which often make the best low-noise RF amplifiers.

*The analysis of this problem is given in BRL Memorandum Report 1746 and BRL Report 1301.

2-10 RELATIONS OF FREQUENCY PARAMETERS FOR TRANSISTORS

The frequency parameters f_β , f_{n1} , f_{n2} , and f_T , f_{max} are all used on occasion in the description of the response properties of transistor amplifiers. The first two represent corner frequencies at which the amplification of the amplifier changes from one frequency relation to another, and the third and fourth represent corner frequencies at which changes in the noise characteristics occur. The fifth frequency is more convenient to use than the first in calculations involving frequency characteristics of amplifiers because the reduction of the frequency to half increases the gain by 6 dB. The f_{max} is important in that it is the maximum frequency at which unity gain can be developed. It is the maximum oscillation frequency.

Three of these frequencies are closely related to one another. The relations are

$$f_\beta = (1 - \alpha)f_a, \quad f_a = (\beta + 1)f_\beta$$

$$f_{n2} = \sqrt{f_a f_\beta} = f_a \sqrt{(1 - \alpha)} = f_a / \sqrt{(\beta + 1)} \quad (2-28)$$

$$f_{n2} = f_\beta \sqrt{(\beta + 1)} = f_\beta / \sqrt{(1 - \alpha)}$$

Since at least one of the three frequencies is normally known for any transistor, and either the α or β also is known, all three frequencies are easily determined.

The importance of f_β originally was considerably overrated in the literature on transistors, because design of the input circuit to allow for input capacitance, a common practice with tube amplifiers, accounts not only for the β frequency but also for base-spreading resistance and the source impedance of the driver circuit. For this reason it is seldom given, and the value of f_β is given in its stead. Because the corner frequency for the noise spectrum is considerably more difficult to measure directly, it is doubtful if the user can hope to have the value of f_{n2} replace f_a as the principal corner frequency given on data sheets, and as a consequence, the relations of Eq. 2-28 are of considerable importance to designers.

The frequency at which the effective β is unity is also related to the α - and β -cutoff frequencies and, with transistors having a high value of β , is almost equal to the α -cutoff frequency. This frequency is equal to the gain-bandwidth product for the device. It can be con-

verted into the other frequencies through the equations*

$$f_\beta = [f_T]/\beta \quad f_T = \beta f_\beta$$

$$f_a = (\beta + 1)f_T/\beta \quad f_T = \beta f_a/(\beta + 1) \quad (2-29)$$

$$f_T = \alpha f_a$$

Because for large values of beta $\beta/(\beta + 1)$ is almost unity, a distinction between f_a and f_T may need to be drawn only for devices having values of β less than approximately 25.*

The maximum oscillating frequency f_{max} is really an overall figure of merit for the transistor in that it takes into account the value of f_T , and also the capacitances and the base-spreading resistance for the device. Its value is given by the equation (Ref. 7)

$$f_{max} = \sqrt{\alpha f_a / (8\pi r_b' C_c)} = \sqrt{f_T / (8\pi r_b' C_c)} \quad (2-30)$$

$$= \frac{1}{4\pi} \sqrt{\frac{g_f}{r_b' C_i C_c}}$$

The importance of the frequency for unity gain is shown by this equation.

Other parameters and variables are important in the design of transistor circuits. However, because practical selections have been made for them that are completely adequate technically, only a brief enumeration is required. One of the most important remaining variables is the breakdown, or avalanche voltage for the collector junction. The minimum value of this voltage permitted in transistors conforming with specifications is needed by the designer to design his circuit to comply with the limitation.

The permissible dissipation limit on a transistor is also important to the user. Device manufacturers normally provide data on this limit, but the value may not always be consistent with good usage, particularly when maximum reliability is important. A method of checking the conservatism of this rating is described in the next chapter.

2-11 POWER RELATIONS

The power gain in the transistor amplifier is a function of the operating configuration, and depends on the

*In practice, the value of f_T is considerably less than f_a . The principal cause is transmission delay time, resulting from diffusion through the base region, and another cause may be r_c' and C_{cb} . The gain across r_c' applies a feedback voltage to C_{cb} and causes the magnitude of h_{fe} to drop to unity at a lower frequency.

values of the input and output impedance. The configuration that gives the maximum power gain is the one in which the device shows a minimum dependence on the circuit properties. Eqs. 2-31, 2-32, and 2-33 show that this condition is obtained with the common-emitter configuration. This is an additional reason for the use of the small-signal parameter values on the common-emitter basis. The power gain for a transistor amplifier in the common-emitter configuration is given by the equation

$$\begin{aligned} |K_v K_i| &= y_f^2 R_L / [1 + y_i R_s + y_o R_L \\ &\quad + y_i y_c R_s R_L] [y_i (1 + y_c R_L)] \\ &= y_f^2 R_L / [1 + y_o R_L \\ &\quad + y_i R_s (1 + y_c R_L)] [y_i (1 + y_c R_L)] \end{aligned} \quad (2-31)$$

The corresponding equation for the common-base amplifier is

$$\begin{aligned} |K_v K_i| &= (y_f + y_o)^2 R_L / [1 + \sigma(y) R_s \\ &\quad + y_o R_L + y_i y_c R_s R_L] \\ &\quad [\sigma(y) + y_i y_c R_L] \end{aligned} \quad (2-32)$$

In the common-collector configuration, the equation is

$$\begin{aligned} |K_v K_i| &= (y_i + y_f)^2 R_s / [1 + y_i R_s + \sigma(y) R_s \\ &\quad + y_i y_c R_s R_s] \\ &\quad [y_i (1 + y_c R_s)] \end{aligned} \quad (2-33)$$

The numerators for each of these equations are very nearly equal if $R_e = R_L$. For this reason, the controlling factor in power gain is the effect of the $\sigma(y)$ term in the denominators of the common-base and common-collector equations. With the common-base equation, a small value of R_s reduces the denominator term to approximately the same size as the denominator for the common-emitter equation. A similar analysis shows that the common-emitter gain is larger than the maximum gain available with the common-collector configuration.

An important remaining problem of concern to the designer is the determination of the values of the parameters that have been found of importance in design when inadequate small-signal data are available. Even though the data available on transistors are often more effective than those on other active devices, they frequently prove inadequate when serious design work is contemplated. A method of making the required

evaluation of the parameters in terms of orthogonal and Legendre polynomials is explained briefly in Appendix C, and is used extensively in some of the later chapters of this handbook.

2-12 RELATIONS AND CONVERSIONS OF PARAMETERS

The conversion of small-signal data from one configuration to another is a relatively simple process on the admittance basis, but is somewhat more complicated in other configurations such as the hybrid arrangement. Because of the variety of data published by different manufacturers, it is convenient for the user to have conversion tables for transforming parameters in one system among the three configurations, and also to have substitution tables for converting from one set of parameters to another.

In each of the conversion tables, the reference configuration used in this volume is the grounded-emitter configuration, because the data provided usually are adaptable to it. Occasionally the data on transistors intended for use at very high frequencies are presented in the common-base form. They are almost never given under common-collector conditions. The common-base data may be converted to common-emitter data by equating the value of the parameter in terms of the common-emitter components to the given values and solving. (A "small difference" problem may result.)

The exact forms of the conversion equations are given in these tables, the forms as derived from transformation of the basic black-box equations. These equations can be simplified in many cases, and then yield the forms that are normally used. This simplification in particular is required with the common-base hybrid parameters.

It is possible, within the limitations derived by Follingstad, to use combinations of configurations for the measurements if desired. For example, the input conductance or admittance may be measured in the common-emitter configuration, and the forward in terms of the input admittance in the common-base configuration. Similarly, the output admittance may be measured either in the common-base or the common-emitter configuration because the measurements are equivalent.

Tables of equivalences, Tables 2-5 through 2-17, which have been adapted from a set published in *Electronic Design* (Ref. 8), provide the reader with a fairly complete listing of the conversions among the more commonly used parameters, and are based on the common-emitter parameters. Table 2-5, which has already

been given in this chapter as Table 2-3, is repeated here for completeness, since it is extremely useful.

TABLE 2-5
CONFIGURATION CONVERSION FOR Y PARAMETERS

Parameter	C-Emitter	C-Base	C-Collector
Input	y_i	$\sigma(y)$	y_i
Forward	y_f	$-(y_f + y_o)$	$-(y_i + y_f)$
Reverse	y_r	$-(y_r + y_o)$	$-(y_i + y_r)$
output	y_o	γ_o	$\sigma(y)$
Mod. output	y_o	$\frac{y_i y_o}{\sigma(y)}$	y_o
Δ factor	$y_i y_o - y_f y_r$	$y_i y_o - y_f y_r$	$y_i y_o - y_f y_r$

where $\sigma(y) = y_i + y_f + y_r + y_o$; $\gamma_o y_o = \Delta(y) = y_i y_o - y_f y_r$

TABLE 2-6
CONFIGURATION CONVERSION FOR H PARAMETERS

Parameter	C-Emitter	C-Base	C-Collector
Input	h_i	$\frac{h_i}{\gamma(h)}$	h_i
Forward	h_f	$-\frac{[h_f + \Delta(h)]}{\gamma(h)}$	$-(1 + h_f)$
Reverse	h_r	$\frac{[\Delta(h) - h_r]}{\gamma(h)}$	$(1 - h_r)$
output	h_o	$\frac{h_o}{\gamma(h)}$	h_o
A factor	$\Delta(h)$	$\frac{\Delta(h)}{\gamma(h)}$	$\gamma(h)$

where $\gamma(h) = [1 + h_f - h_r + \Delta(h)]$; $\Delta(h) = h_i h_o - h_f h_r$

Note that the A factor is not invariant in this case.

TABLE 2-7
CONFIGURATION CONVERSION FOR Z PARAMETERS

Parameter	C-Emitter	C-Base	C-Collector
Input	z_i	z_i	$\sigma(z)$
Forward	z_f	$z_i - z_f$	$z_o - z_f$
Reverse	z_r	$z_i - z_r$	$z_o - z_r$
Output	z_o	$\sigma(z)$	z_o
Δ factor	$z_i z_o - z_f z_r$	$\Delta(z)$	$\Delta(z)$

where $\Delta(z) = z_i z_o - z_f z_r$; $\sigma(z) = z_i - z_f - z_r + z_o$

Again, the A factor is invariant.

TABLE 2-8
CONVERSION FROM NETWORK TO IEEE PARAMETERS

<i>Hybrid</i>	<i>Admittance</i>	<i>Impedance</i>	<i>Conductance</i>
$h_{11} = h_i$	$y_{11} = y_i$	$z_{11} = z_i$	$g_{11} = g_i$
$h_{21} = h_f$	$y_{21} = y_f$	$z_{21} = z_f$	$g_{21} = g_f$
$h_{12} = h_r$	$y_{12} = y_r$	$z_{12} = z_r$	$g_{12} = g_r$
$h_{22} = h_o$	$y_{22} = y_o$	$z_{22} = z_o$	$g_{22} = g_o$
	$y_c = h_o$		$g_c = h_o$

TABLE 2-9
CONVERSION BETWEEN Y AND Z PARAMETERS

<i>Z to Y</i>	<i>Y to Z</i>
$z_i = \frac{y_o}{y_i y_c}$	$y_i = \frac{z_o}{\Delta(z)}$
$z_f = \frac{-y_f}{y_i y_c}$	$y_f = \frac{-z_f}{\Delta(z)}$
$z_r = \frac{-y_r}{y_i y_c} = \frac{y_c - y_o}{y_f y_c}$	$y_r = \frac{-z_r}{\Delta(z)}$
$z_o = \frac{1}{y_c}$	$y_o = \frac{z_i}{\Delta(z)}$
$\Delta(z) = z_i z_o - z_f z_r$	$y_c = \frac{1}{z_o}$
	$\Delta(y) = y_i y_o - y_f y_r = y_i y_o$

TABLE 2-10
CONVERSION BETWEEN H, Y, AND Z PARAMETERS

$h_i = \frac{1}{y_i} = \frac{\Delta(z)}{z_o}$	$h_r = \frac{y_c - y_o}{y_f} = \frac{z_r}{z_o}$
$h_f = \frac{y_f}{y_i} = -\frac{z_f}{z_o}$	$h_o = y_c = \frac{1}{z_o}$

TABLE 2-11
CONVERSION BETWEEN H, Y, AND TEE PARAMETERS

$r_d = \frac{1}{y_c} = \frac{1}{h_o}$	$r_m = \frac{-y_f}{y_i y_o} = \frac{-h_f}{h_o}$
$r_b = \frac{y_o}{y_i y_c} = \frac{\Delta(h)}{h_o}$	$r_a = \left(\frac{y_o}{y_c} - 1 \right) y_f = \frac{-h_r}{h_o}$
$r_o = \frac{y_i + y_f}{y_i y_c} = \frac{1 + h_f}{h_o}$	

TABLE 2-12
CONVERSION OF *H* PARAMETERS TO *R* PARAMETERS

<i>Parameter</i>	<i>C-Emitter</i>	<i>C-Base</i>	<i>c-collector</i>
r_e	$\frac{-h_r}{h_o}$	$\Delta(h)_b - h_{rb}$	$\frac{1 - h_{rc}}{h_{oc}}$
r_b	$\Delta(h) - h_r$	$\frac{h_{rb}}{h_{ob}}$	$\frac{\Delta(h)_c + h_{fc}}{h_{oc}}$
r_c	$\frac{1 + h_f}{h_o}$	$\frac{1 - h_{rb}}{h_{ob}}$	$\frac{-h_{fc}}{h_{oc}}$
r_d	$\frac{1 - h_r}{h_o}$	$\frac{1 + h_{fb}}{h_{ob}}$	$\frac{h_{rc}}{h_{oc}}$
r_m	$\frac{h_f + h_r}{h_o}$	$\frac{h_{fb} + h_{rb}}{h_{ob}}$	$\frac{h_{fo} + h_{rc}}{h_{oc}}$

TABLE 2-13
CONVERSION FROM *R* PARAMETERS TO *Z* PARAMETERS

<i>Parameter</i>	<i>C-Emitter</i>	<i>C-Base</i>	<i>c-collector</i>
Input	$r_e + r_b$	$r_e + r_b$	$r_b + r_c$
Forward	$r_e + r_m$	$r_b + r_m$	r_o
Reverse	r_e	r_b	r_d
output	$r_e + r_d$	$r_b + r_o$	$r_e + r_d$

TABLE 2-14
CONVERSION FROM *Z* PARAMETERS TO *R* PARAMETERS

<i>Parameter</i>	<i>C-Emitter</i>	<i>C-Base</i>	<i>C-Collector</i>
r_e	z_r	$z_{ib} - z_{rb}$	$z_{oc} - z_{rc}$
r_b	$z_i - z_r$	z_{ib}	$z_{ic} - z_{fc}$
r_c	$z_o - z_f$	$z_{ob} - z_{fb}$	z_{fo}
r_d	$z_o - z_r$	$z_{ob} - z_{rb}$	z_{rc}
r_m	$z_r - z_f$	$z_{fb} - z_{rb}$	$z_{fo} - z_{rc}$

TABLE 2-15
CONVERSION OF *Z* PARAMETERS TO *H* PARAMETERS

$z_i = \frac{\Delta(h)}{h_o}$	$z_f = -\frac{h_f}{h_o}$	$z_r = \frac{h_r}{h_o}$	$z_o = \frac{1}{h_o}$
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TABLE 2-16
MISCELLANEOUS RELATIONS

$$\alpha = \frac{y_f}{y_i + y_f} = -h_{fb} \quad \beta = \frac{y_f}{y_i} = h_{fb}$$

$$g_{i'} = \frac{g_i}{1 - g_i r_{b'}}$$

$$g_i = \frac{g_{i'}}{1 + g_{i'} r_{b'}}$$

$$y_{i'} = \frac{y_i}{1 - y_i r_{b'}}$$

$$y_i = \frac{y_{i'}}{1 + y_{i'} r_{b'}}$$

$$g_{f'} = \frac{g_f}{1 - g_i r_{b'}}$$

$$g_f = \frac{g_{f'}}{1 + g_{i'} r_{b'}}$$

$$y_{f'} = \frac{y_f}{1 - y_i r_{b'}}$$

$$y_f = \frac{y_{f'}}{1 + y_{i'} r_{b'}}$$

TABLE 2-11
RCA (GIACOLETTO) PARAMETERS

$$g_{b'e} = g_{i'}$$

$$g_{ce} = g_o$$

$$g_m = g_{f'} - g_r \doteq g_{f'}$$

$$g_{b'c} \doteq \frac{(g_c - g_o)g_i}{g_f}$$

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CHAPTER 3

DEVELOPMENT OF INTRINSIC DEVICE THEORY AND RELATED FUNDAMENTAL LIMITATIONS AND THEIR MEASUREMENTS

3-0 INTRODUCTION

In this chapter, the representation of the basic four-pole or two-port network will be developed from fundamentals and transformed into a structure consistent with the physics of solid-state active devices. Based on this structure and long-established limitations which apply to active networks, a basic philosophy of design of networks is developed which provides the essential guidelines which can assure that the resulting network will show a maximum reliability.

3-1 THE BASIC TWO-PORT NETWORK

A general relationship for a two-port network in terms of undetermined parameters may be derived which can be transformed into any of the six standard configurations (several of which are noted in Chapter 2)—the admittance, the impedance, the hybrid, the inverse hybrid, and the two ladder-lattice configurations. The basic relations take the form

$$\left. \begin{aligned} &= Qx + Ry \\ v &= Sx + Ty \end{aligned} \right\} \quad (3-1)$$

where the input and output relations are

$$\left. \begin{aligned} x_s - \alpha u &= x \\ y + \Delta_L v &= Ty \end{aligned} \right\} \quad (3-2)$$

and

- Q, R, S, T = matrix relations of arbitrary and independent variables
- u, v = arbitrary dependent variables
- x, y = arbitrary independent variables
- x_s = arbitrary source vector
- α = arbitrary source parameter
- Δ_L = arbitrary single parameter

When Eqs. 3-1 are substituted into Eq. 3-2, and rearranged and simplified, the result is

$$\left. \begin{aligned} (1 + \alpha Q)u + R\Delta_L v &= Qx_s \\ \alpha Su + (1 + T\Delta_L)v &= Sx_s \end{aligned} \right\} \quad (3-3)$$

These relations may be solved for the usual input and transfer relations

$$\begin{aligned} u/x_s &= [Q + \Delta_L(QT - RS)] / [(1 + Q\alpha) \\ &\quad \times (1 + T\Delta_L) - \alpha\Delta_L RS] \end{aligned} \quad (3-4)$$

$$v/x_s = S / [(1 + Qx)(1 + T\Delta_L) - \alpha\Delta_L RS] \quad (3-5)$$

These two basic relations, which define all input and transfer relations for the opaque-box two-port network, may be converted to the more familiar form by a series of simple substitutions. The resulting equations are tabulated in Chapters 2 and 4 and in other texts. The substitutions are:

TABLE 3-1

NETWORK VARIABLE RELATIONS

Parameter	Admit	Imped	Hybrid	Inv. Hyb.	Frwd Lat.	Rev Lat.
v	i_i	v_i	v_i	i_i	v_o	v_i
x	i_o	v_o	i_o	v_o	i_o	i_i
Y	v_i	i_i	i_i	v_i	v_i	v_o
x_s	v_o	i_o	v_o	i_o	i_i	i_o
Δ_L	v_s	i_s	i_s	v_s	—	—
α	Z_L	Y_L	Z_L	Y_L	—	—
Q	Z_s	Y_s	Y_s	Z_s	—	—
R	y_i	z_i	h_i	j_i	A'	A
S	y_r	z_r	h_r	j_r	B'	B
T	y_f	z_f	h_f	j_f	C'	C
$QT - RS$	y_o	z_o	h_o	j_o	D'	D
	Δy	Δz	Δh	Δj	—	—

where the various **A** functions are defined in terms of the differences of two products ($QT - RS$). The terms not included in this table are relatively ill-defined, and generally are not used. Of particular note is the fact that the admittance and the impedance configurations can be shown to be adaptable to use with the indefinite admittance matrix and with the indefinite impedance matrix, respectively. This fact and the fact that existing active devices are ones in which across variables control through variables makes the admittance approach of prime importance in the material to follow.

The indefinite admittance matrix is of considerable use in network design because it presents in a convenient tabulated form the data needed for conversion among common-emitter (C-E), common-base (C-B), and common-collector (C-C) configurations. This matrix takes the form

$$Y_i = b \begin{pmatrix} e & & \\ & b & c \\ e & \begin{pmatrix} \sigma_y & - (y_i + y_r) - (y_r + y_o) \\ - (y_i + y_f) & y_i & y_r \\ c & - (y_f + y_o) & y_f & y_o \end{pmatrix} \end{pmatrix} \quad (3-6)$$

where $\sigma(y) = y_i + y_f + y_r + y_o$. It is used by deleting the appropriate row and column corresponding to the reference terminal to provide the parameters in the configuration in use. In these terms, a general equation for gain may be written in the general form

$$Y_T = (y_F \pm \Delta y Z_r) / \left[1 + \sum y_{jj} Z_j + \Delta y \left(\sum_{i \neq j} Z_i Z_j \right) \right] \quad (3-7)$$

where Y_T is the transfer admittance, y_{jj} is the appropriate diagonal term of the matrix and Z_j is the related external impedance, and Δy easily can be shown to be invariant and to take the form

$$\Delta y = y_i y_o - y_f y_r \quad (3-8)$$

In the numerator of Eq. 3-7, the plus sign applies for the C-B amplifier, and the minus with the degenerative-emitter amplifier. The Z_r is the total impedance in the reference circuit. In the C-B amplifier, this is primarily the base-spreading resistance and, with the degenerative-emitter amplifier, it is the emitter return impedance.

As is shown in Appendix B on topological techniques, the transfer trees which are part of the transfer immittance function normally do not have any passive elements contacting the reference node. The only time they will include such elements occurs when there is a superfluous node which is not included in the transfer tree. The active forward-transfer element of the network and the source-sink element both may contact the reference node, or if the return end of either does not contact reference, it may be necessary to include a passive element to provide the contact. This is explained in more detail in Appendix B and also in the writer's book on *Topological and Matrix Methods*. The discussion included here only shows why the additional term is in the numerator of Eq. 3-7.

The topological-matrix procedure for establishing the overall transfer and driving-point immittances for fairly general networks including active devices and nonlinear elements is particularly effective in that it does not require the rather complex set of rules which are encountered using the flow-graph procedures, and it also alleviates problems in establishing signs cor-

rectly. It further minimizes the number of term cancellations, thereby greatly reducing chances of error.

The polarities which must be selected with voltages and currents can easily be chosen incorrectly when standard Kirchhoff's law techniques are used. The likelihood of a sign error being made in a problem which is set up topologically is sufficiently reduced that very substantial advantages may be achieved through topological analysis. In addition, rather complex problems can be handled in a systematic way by using the tree-sectioning procedures described, and the amount of waste motion resulting is kept to a minimum.

Notes on Thevenin's and Norton's Theorems: Thevenin's and Norton's theorems are often used as the way for establishing a simple model for a transistor in a circuit, and under situations in which the percentage bandwidth of the circuit is small (typically 5% or less), the procedure is eminently successful. Under conditions of large percentage bandwidth, however, it is important to re-examine the validity of the procedure as a modeling technique.

If one assumes that the basic network is in fact a series R-C network, its Norton equivalent may be found by inversion of the impedance expression into the appropriate admittance expression. The equations are, for the impedance Z

$$Z = R - j/(\omega C) \tag{3-9}$$

which then becomes

$$Y = (\omega^2 C^2 R + j\omega C)/(1 + \omega^2 C^2 R^2) \tag{3-10}$$

In this equation, the conductance term G takes the form

$$G = \omega^2 C^2 R/(1 + \omega^2 C^2 R^2) \tag{3-11}$$

and clearly, G is only independent of frequency f if $|\omega CR| > 1$.

Similarly, the susceptance term B takes the form

$$B = \omega C' = \omega C/(1 + \omega^2 C^2 R^2) \tag{3-12}$$

and now, the value of B is linearly dependent on ω only if $|\omega CR| < 1$, or the inverse condition.

Clearly, the conductance can be independent of ω only when the capacitance is *improperly* dependent on ω , and vice versa. If the change in values for these

terms is essentially negligible over the frequency range of operation, these difficulties do not introduce problems. But for the large percentage-bandwidth application, or *a nonlinear application in which strong out-of-band interference may exist*, the only equivalent network which is realizable or usable is the one whose geometric configuration coincides with the equivalent physical structure. The only acceptable alternative is the use of complete duality, replacing currents with voltages, resistances with conductances, and inductances with capacitances, etc. The new circuit graph must also be the complete dual of the original graph.

3-2 THE GENERALIZED SOLID-STATE EQUATIONS

The basic equations developed for the back-to-back diodes in representing transistor structures apply with only minor changes to other transadmittance devices such as electron tubes and field-effect transistors. The first step in this generalization is based on consideration of the fundamental Ebers-Moll (E-M) equations (Eqs. 2-16 through 2-21) in a simplified form. The relations are

$$\left. \begin{aligned} I_b &= I_{b0} + I_{b1} \exp(\Lambda V_b) + I_{b2} \exp(\Lambda V_c) \\ I_c &= I_{c0} + I_{c1} \exp(\Lambda V_b) + I_{c2} \exp(\Lambda V_c) \end{aligned} \right\} \tag{3-13}$$

where

- I_b = base current, E-M equations
- I_c = collector current, E-M equations
- I_{b0}, I_{b1}, I_{b2} = base current components, E-M equations
- I_{c0}, I_{c1}, I_{c2} = collector current components, E-M equations
- V_b = instantaneous plate voltage
- V_c = instantaneous collector voltage
- A = $q/(kT)$

As ordinarily used, the I_{b0} and the I_{c0} terms represent leakage terms. In practice, however, one can consider that substantial amounts of output (collector, plate, or drain) current flow in an active device may be uncontrolled as far as the gate (or base or grid) electrode is concerned. Those currents which are shielded from the control electrode by layers of current adjacent to existing "depletion" fields flow under the control of the sink electrode and essentially are not controlled by the control electrode. One can imagine that "layers" of this column of current are successively "peeled off" and extinguished one-by-one as the depletion field is in-

creased. Each layer, until it is in the process of being peeled off, flows devoid of control through the channel.

In this sense, then, at least one additional term may be combined into the I_{c0} term in the more general active device. This additional term is a weak function of both base and collector voltages in that its magnitude varies with these voltages even though it represents an uncontrolled component of current. In this sense, the second of Eqs. 3-13 may be rewritten in the form

$$I_{c0} = I_{c00} + I_{c01} + I_{c1} \exp(\Delta V_b) + I_{c2} \exp(\Delta V_c) \quad (3-14)$$

In Eq. 3-14, the I_{c00} term almost always can be neglected with military-quality components, and the I_{c2} term is at least less than the I_{c1} term. The magnitude of the I_{c01} term may be large compared to any of the remaining three, however, and it does have at least a weak dependence on both V_b and V_c , i.e., the variation in the magnitude of its value is slow with these voltages.

In light of this discussion, the I_{c00} , I_{c01} , and I_{c2} terms may be grouped together as a new $I_{c'}$, leading to the equation

$$I_c = I_{c'} + I_{c1} \exp(\Delta V_b) \quad (3-15)$$

and it may be solved for the I_{c1} term in the form

$$I_{c1} \exp(\Delta V_b) = I_c - I_{c'} = I_c \kappa \quad (3-16)$$

where the κ measures the control efficiency of the control voltage in that it determines that percentage of the total device current which is directly controlled by the voltage V_b . For this reason, κ may be called the "efficiency factor".

If Eq. 3-15 is differentiated with respect to V_b , one gets the result

$$\partial I_c / \partial V_b = \Delta I_{c1} \exp(\Delta V_b) \quad (3-17)$$

Substituting into this equation from Eq. 3-16 then gives

$$\partial I_c / \partial V_b = \kappa \Delta I_c = \gamma_f \quad (3-18)$$

showing that the efficiency factor is indeed important in the small-signal design of active circuits. In fact, this factor is of outstanding importance in the design of

circuits for handling large blocks of power in tuned circuits. It is discussed further in the paragraphs on limitations applicable to reliable design in later paragraphs of this chapter.

Some notes on typical values for the efficiency factor for typical devices are in order. At very small values of device current, but substantially above the leakage levels, this factor may have a near-unity value with both electron tubes and field-effect transistors. (It has a value near unity with bipolar transistors under these conditions as well.) This condition exists because the thickness of the Debye region is roughly equal to the half-width of the channel through which the current is flowing, and as a result almost all of the current is controlled fully.

With electron tubes, this mode of operation was called the "starved mode" of operation. It was exploited by one manufacturer of electronic instruments in the early 1950's, and apparently was reasonably successful provided the tubes used were selected with sufficient care to assure that leakage currents were minimal. The tubes were used under voltage and current conditions for which no effort was made to assure compliance with what is called "bogey" characteristics. As a result, one could not be sure how many tubes he would have to try to get one which worked properly. Fortunately, failure rates were fantastically low for tubes used in this way!

Field-effect devices were found to have operating regions in which the κ factor could have values approaching unity (for junction, or DIFET, devices) or one-half for insulated-gate (or MISFET) devices.* It is believed that the lack of symmetry accounts for the reduced values which can be obtained with insulated-gate devices, although to date no analytical proof has been seen by the writer. The value of κ approaching unity with DIFET devices typically is observed over as many as five orders of magnitude of current.

The correction for high-injection conditions for bipolar transistors has been noted in the series of publications of the SEMICONDUCTOR ELECTRONICS EDUCATION COMMITTEE among other places, and is derived in Volume 4 of that series. This correction exists as a result of the variation of the density of the majority carriers between the active base-emitter junction and the external base connection. This variation creates an electric field which increases the required base voltage applied to PNP devices, and de-

*Evans and Pullen, "Letter to the Editor", *Proc IEEE*, Jan. 1966. F. Zieber, Final Report, *Design and Development of Radiation Hardened Field-Effect Transistors*, Contract DA-04-200-AMC-725(X), 1966.

creases that required for NPN devices. In fact, the net voltage V_{EB} , at the device junction can be expressed in terms of the equation

$$V_{EB}' = V_{EB}^{(j)} + \phi'_{ab} \quad (3-19)$$

where ϕ'_{ab} is the barrier potential across the graded charge distribution, V_{EB}' is the terminal potential after subtraction of ohmic losses, and $V_{EB}^{(j)}$ is base terminal voltage. When account is taken of the potential ϕ'_{ab} in terms of charge densities and diffusion rates, the value of $V_{EB}^{(j)}$ is found to be

$$V_{EB}^{(j)} = V_{EB}' / (1 + m) \quad (3-20)$$

where m is defined in terms of drift velocities for holes and electrons in the base region. Eq. 3-20 then is substituted for V_b in Eq. 3-14

$$I_c = I_{c00} + I_{c01} + I_{c1} \exp[\Delta V_{BE}' / (1 + m)] + I_{c2} \exp(\Delta V_c) \quad (3-21)$$

Technically, the $[\Delta V_{BE}' / (1 + m)]$ factor may require inclusion in the I_{c1} term for small values of V_c ; since, however, $\Lambda^{-1} = 0.026$ V, approximately, if the value of V_c exceeds 0.5 V, the correction usually can be neglected.) The change this makes in the forward admittance equation is small, i.e.,

$$\partial I_c / \partial V_b = \Lambda I_c / (1 + m) \quad (3-22)$$

The maximum magnitude for the value of m in germanium is 0.35; for silicon, 0.45.

Strictly, there is a component of I_{c2} which should be included in Eq. 3-22 as a consequence of the presence of the voltage from Eq. 3-20 as a component of V_c , but since I_{c2} is so very much smaller than I_{c1} with most transistor devices, it generally is neglected. To be precise in the analysis, it is necessary to recognize that the voltage V_c is really V_{CB} , and it takes the form:

$$V_{CB} = V_{CE} - V_{BE}' / (1 + m) \quad (3-23)$$

The changes in V_{BE}' usually are small compared to those in V_{CE} .

It is evident from these equations that more data of a practical nature on such parameters as κ and m are

required in circuit design. These parameters are functions of device current in particular. This writer has yet to see data on either of these factors on any device on any data sheet.

The effects of spreading resistances have been ignored so far in the discussion. In any practical situation, it is essential that they be taken into account, since they have important influence on both the frequency response and on circuit behavior in general. In addition, the effect of each of the spreading resistances is different.

The primary effect of base-spreading impedance is to limit the control efficiency which can be obtained at the base. A significant part of the applied signal voltage incident on the base terminal for a transistor may be lost across this impedance, and the amount is a function of base current and operating frequency. The voltage division effect can be minimized by operating the device in a current-drive mode, but the variable losses as a function of current and frequency which are at least reasonably well defined are replaced by a variable current gain which is ill-defined at best.

Base-spreading resistance present in an amplifier in the voltage-gain configuration can introduce a frequency break-point into the response of an amplifier which can be ignored if the device is used as a current amplifier. The approximate defining equation for this break-point is

$$\omega C_i r_b' = 1 \quad (3-24)$$

and the approximate equation for the usual β break-point is defined by the equation

$$\omega C_i / g_i' = 1 \quad (3-25)$$

where g_i' is the conductive component of the intrinsic input admittance, and C_i the capacitive component. Eq. 3-25 is the one which always applies, both under voltage and current-source conditions, and Eq. 3-24 applies under voltage-source conditions.

The input admittance in the common-base configuration includes a much larger value of input conductance, namely, $\sigma(g)$, which is equal to, $g_f' + g_r' + g_o'$ of the admittance four-pole. Under these conditions, Eq. 3-24 has little influence on circuit gain as a function of frequency, and in Eq. 3-25, the conductance term is replaced by $\sigma(g)$, leading to a much higher corner frequency. This is one of the reasons that the use of the common-base configuration is to be pre-

ferred at high operating frequencies when transformer or inductive coupling can be used.

Emitter-spreading resistance has the same effect on a circuit as an emitter-degeneration resistance, and limits the effective transconductance which can be developed in the overall circuit. Emitter degeneration can be very useful as an adjunct in circuit design, because it makes linearization and stabilization possible. Circuits are surprisingly sensitive to this resistance, as can be recognized from the inequality

$$\sigma(y)Z_e = \kappa \Delta I_e Z_e \leq 0.1 \tag{3-26}$$

where the κ takes the form $(1 + m)^{-1}$ for the bipolar transistor, I_e is the emitter current, and Z_e is the emitter impedance. This equation may be approximated, for transistors having large values of β , in the form:

$$y_f Z_e = \kappa \Delta I_e Z_e \leq 0.1 \tag{3-26a}$$

which is close enough for most applications. Its use is discussed in later chapters.

Collector-spreading resistance introduces problems primarily through its contribution to increasing the output load impedance of an amplifier, thereby increasing the overall voltage gain and increasing the possibilities of circuit instability. In practical situations, the voltage gain developed across the output-spreading resistance should be limited to whichever is smaller of either unity or approximately 0.2 times the voltage gain of the circuit neglecting the spreading resistance. The corresponding equation for gain for the unity-maximum case is:

$$\kappa \Delta I_c r_c \leq 1 \tag{3-27}$$

where again the κ -factor is a function of the m parameter.

3-3 FUNDAMENTAL DESIGN LIMITATIONS

The developments which took place in electronics and radar during World War II brought out a variety of relations that have seen little use in the civilian market, and many of them have not been readily available to either students or practicing designers. Since these relations are important to designers of military equipment in particular, they are developed in considerable

detail in the paragraphs that follow. The resulting concepts then can be readily applied to circuits by the design procedures described in the remainder of this handbook, leading to substantial improvement in reliability.

3-3.1 THE VOLTAGE GAIN LIMITATION

The development of radar brought with it the need to be able to amplify very weak signals in the presence of strong ones, and for the first time made the question of stability and freedom from ringing a prime consideration in tuned amplifiers. These tuned amplifiers frequently were required to have voltage amplifications as great as a million overall, with no change in operating frequency permitted.

The basic criterion which must be satisfied, both for each individual amplifier stage and for the amplifier as a whole, is that the loop amplification of individual elements as well as of the assembled groups of elements must be rigidly limited to assure that stability will not be impaired. This stability problem is essentially a phase-sum problem. If an input voltage is applied to the amplifier or stage in question, then the voltage returned through feedback to be summed into the input voltage is the product of this voltage by the amplification "around the loop" from input back to input

$$K_L = K_v \times K_f \tag{3-28}$$

where K_v is the forward voltage amplification to the output, and K_f is the feedback "amplification" from the output back to the input on an open-loop basis. The modified forward amplification $K_{v'}$ then takes the form:

$$K_{v'} = K_v / (1 - K_v K_f) \tag{3-29}$$

and the phasor term $(1 - K_v K_f)$ determines both the variation of the signal amplitude and the signal phase.

Clearly, one of the requirements of any amplifier to which Eq. 3-28 applies is that $|K_v K_f|$ must be small compared to unity, or a potentially unstable situation can develop. In addition, significant phase shift in the output circuit compared to the input can occur even with relatively small values of $|K_v K_f|$, values as small as 0.1 or 0.2, for example. In such a situation, as much as 5- to 10-deg phase discrepancy per stage can be encountered.

Where phase stability is of prime importance, it is evident that values of $|K_v K_f|$ should be less than 0.01 if at all possible, as then there is reasonable chance that

the cumulative phase angle discrepancy in a system may be limited to a fraction of a radian. The design of an amplifier meeting this limitation can be both difficult and painstaking, and the mechanical realization of the calculated design can be even more difficult. The design techniques described in later paragraphs of this handbook offer possibly one of the best ways of achieving the required results.

Early radar experience quickly showed that the limit on per-stage gain K_v for achieving amplitude and phase stability with minimum to modest ringing proved to be approximately 10. (It is apparently possible to get device gains of 100 with common-grid or common-base circuits, but the required impedance transformation required to match the input circuit for the succeeding amplifier typically reduces the overall stage gain back to approximately 10.) This means that the maximum permitted value for K_f is approximately 0.01 to 0.02, for a power isolation possibly as much as 40 dB. Where phase stability is of primary importance, the maximum permitted value for K_f is nearer 0.001 than 0.01.

Evidently, it is very important to control and restrain the circulation of carrier-frequency currents throughout any multistage amplifier, since if five stages overall are involved, the isolation from output back to input must be about 0.01^5 or 10^{-10} ! This is the reason that radar IF amplifiers were designed to be provided power in the vicinity of the middle stage, and R-C decoupling was used in both directions for supply voltages, and L-C decoupling for heater currents. All voltage feed points were in addition individually bypassed, and grounds grouped within the channel in such a way as to prevent circulation of carrier-frequency currents in the channel.

Clearly, there is really nothing magic about the value of K_v of 10. The magic number, if one exists, is in fact the "invariant" $K_v \times K_f$, whose value must be sufficiently small to limit the phase and amplitude excursions in the signal. This is the basic stability criterion. But there definitely is an upper limit on the value of K_v , at least in a practical way, since there is a lower practical limit on how small K_f can be made successfully in production-type equipment. The internal stage voltage gain from input to output on control-separation amplifiers can be significantly higher, since the input admittances for these devices are sufficiently high that the return feedback gain is severely reduced thereby.

This limitation on voltage gain has very interesting consequences, particularly in design for reliable operation. It may be developed in terms of Eq. 3-18, which expresses the intrinsic transadmittance

$$K_v = -y_f Z_L = -\kappa \Lambda I_c Z_L \quad (3-30)$$

In this equation, it is evident that $I_c Z_L$ represents a value of a voltage, namely, the instantaneous voltage across the load impedance Z_L .

It is possible to relate the voltage $I_c Z_L$ to the minimum possible supply voltage V_{CC} which can be used with the ideal device in question to produce the required operating characteristics. The minimum supply voltage may then be defined in terms of the equation

$$I_c Z_L = -\kappa \eta V_{CC} \quad (3-31)$$

where η is a parameter which relates the output load voltage to the supply voltage. η normally has a value between 0.2 and 1.0. Substituting Eq. 3-31 in Eq. 3-29 gives the result:

$$K_v = -\kappa \eta \Lambda V_{CC} \quad (3-32)$$

This equation may be solved for the minimum supply voltage V_{CC} (neglecting saturation voltage) for a device in a circuit to give

$$|V_{CC}| = |K_v| (\kappa \eta \Lambda)^{-1} + V_{c\text{sat}} \quad (3-33)$$

In Eq. 3-33, the value of κ ranges between roughly 0.0001 and 2.0, typical values of η are less than unity, and $V_{c\text{sat}}$ is the maximum saturation voltage. As a result, with bipolar transistors, the minimum value of supply voltage required for a circuit can be expected to be roughly a twentieth of the voltage gain. This means that the range of required supply voltage is between 0.5 and 10V, the lower voltage limit applying to the common-emitter configuration, and the higher to the common-base configuration.

The significance of this relation *cannot* be overemphasized easily. The properties of the device and its associated circuitry are controlled largely by the current level selected for operation, and *there is little point to selecting a supply voltage for the output circuit which is more than marginally greater than given by Eq. 3-33*. Selection of a higher voltage leads either to excessive power dissipation, excessive gain with its inherent instability, or combinations of these conditions. In short, the selected supply voltage should be *as small as possible* consistent with the demands on the circuit.

This discussion should not be implied necessarily to mean that the base supply voltage provided for base

bias current and voltage necessarily can be as small as that for the collector. Since crude stabilization of circuits is frequently obtained by controlling the base current in a transistor, the supply voltage provided for this function must be sufficiently large to assure that an adequate constancy of current level can be achieved. This and this alone is the justification for use of a large voltage, yet the current requirement for these circuits is sufficiently small that a substantial decrease in power dissipation and a substantial improvement in reliability could be achieved through the use of separate power sources for these two functions. In comparison, then, one source of high current and low voltage is required, and one of higher voltage but substantially smaller current also is required. Using a common source for both clearly leads to the worst features of each!

3-3.2 CURRENT GAIN LIMITATION CONSIDERATIONS

The voltage gain limitation is electrostatic, or charge-control, in nature. It is particularly important with transadmittance devices, which tend to have a relatively high input impedance and tend to become regenerative by passing through a zero-admittance (infinite impedance) condition. It is important further because it has the smallest rate of decay with distance of known static fields.

The network dual of the voltage gain limitation is the current gain limitation. It is technically possible for this also to be critical, but at present its consequences are much less severe than its dual. Probably the principal reason for this is the rapidity of decay of magnetic fields associated with currents. Additional reasons are the dependence on rate-of-change of current, since only changing fields create voltage and currents, and the nonexistence of true trans-impedance devices.

The control of magnetic fields proves to be one of control of fluctuating currents. The more that can be done to keep current fluctuations isolated and out of wires and shielding structures, the more freedom there is from coupling currents and fields. Size of loops carrying fluctuating currents should be kept to an absolute minimum unless the inductive properties of the loop are essential to the operation at hand. Even then, the loop or coil should be so designed and so installed that it generates its field efficiently, so that an adequate quality factor, or Q , is obtained, and so that coupled fields and circulating currents induced and generated by the field are limited to regions where they are required and otherwise kept to a practical minimum.

3-4 RELATION OF THE κ -FACTOR TO POWER CAPABILITY

The κ -factor is of much greater importance than might seem the case on casual examination. If one examines the voltage gain equation, Eq. 3-30, one notes that when solved for Z_L it gives

$$Z_L = |K_v| / (\kappa \Lambda |I_c|) \quad (3-34)$$

Eq. 3-34 shows that the load-circuit impedance Z_L is an inverse function of κ , and it also shows that for high values of κ and I_c , the required level of Z_L can become unbearably small. In fact, it is so low that serious problems can be encountered in matching to even 50-ohm cable. The problems of building reliable power amplifiers at even the level of 50 W per device can become very difficult. And so it is that the long-predicted transistors capable of developing more than 50 W per device in a tuned amplifier are largely still predicted!

The importance of κ can be clearly recognized from a re-examination of Eqs. 3-33 and 3-34 and comparing them with Eq. 3-37:

$$|V_{CC}| = |K_v| (\kappa \eta \Lambda)^{-1} \quad (3-35)$$

$$Z_L = |K_v| / (\kappa \Lambda |I_c|)^{-1} \quad (3-36)$$

$$W_0 \propto |V_{CC}| |I_{c \max}| \quad (3-37)$$

where $|I_{c \max}|$ is the peak magnitude of the device current and W_0 is power input. Since the magnitude of V_{CC} is inversely proportional to κ , and the impedance level is also, for any $|I_{c \max}|$, power output capabilities are inversely proportional to κ as well.

Typical peak current levels for all kinds of solid-state active devices cluster around 10 A at the present stage of development. Even the most sophisticated transistor suitable for RF operation apparently has a peak current rating of about 20 to 25 A, and high-power electron tubes typically have similar ratings. (Some special super-high-power tubes do have substantially higher power and current ratings, however.) As a consequence, for a kilowatt per device to be practical, a value of V_{CC} significantly in excess of 100 V is indicated, and a maximum value for κ less than 0.02 is essential. Such a value is readily attainable with electron tubes and with field-effect devices. As a result, power electron tubes and/or field-effect devices probably both will be

around for some time to come. And electron tubes can be expected to keep their corner on very-high-power applications even longer still, although they may be replaced eventually by completely new kinds of devices.

The bipolar transistor will continue to be effective as a power switch for turning large blocks of power on or off, as it is usually possible to design switching circuits so that regeneration and ringing during switching are extinguished in either the cut-off or the saturation modes which normally follow the switching interval.

3-5 ELECTRON TUBE APPLICATION CONSIDERATIONS

The previous discussion shows both that electron tubes can be expected to “be around” for a while yet, and also that they have a military significance. They do in addition have some unique features which are worthy of recounting at this point, because the properties in question give them particular versatility, and also because there are no documents which are in print and readily available which give a meaningful discussion of these properties. A fuller discussion can be found in *Conductance Design & Active Circuits* which is out of print but may still be found in some engineering libraries. Typical triode and pentode curves providing for design of tube circuits having minimum power dissipation are shown in Appendix H, and in par. 3-7.5 on mixer design, for a multigrad mixer tube (Figs. 3-1, 3-2(A), and 3-2(B)).

The discussion that follows will be divided into subparagraphs based on general classes; i.e., triodes, tetrodes, pentodes. Each subparagraph starts with a brief discussion of the behavior of the class of devices as compared to bipolar or FET devices, and it is continued with a discussion of the unique properties of particular interest to the circuit designer. Where it is appropriate, a brief discussion of the ways the characteristics of the device can be expressed meaningfully is included. Unfortunately, with all classes of active devices, there is a tendency for device makers to overlook the problems of device application in terms of their basic parameters. These notes may help users devise their own characterization data for solving similar kinds of problems.

3-5.1 TRIODE TUBES

Triode tubes have a considerable resemblance to field-effect transistors in that the grid serves as a series of gates, controlling the current flow being channeled from cathode (source) to plate (drain). Since the carriers are “boiled out” of the cathode structure by the heat

supplied by the heater, a cloud of carriers forms behind the grid, and a current flow of magnitude dependent on grid and plate voltages results.

Triode tubes tend to have rather large values of output conductance (g_p or y_o) as a result of the field distributions between grid and plate, and the fact that the plate behaves as a diode with respect to the channel sections between grid wires through which current flows. Typically, plate current increases at a slower rate with plate voltage than it does with grid voltage; the ratio of the rate of change with grid voltage to that with plate voltage commonly is called the amplification factor for the triode. The typical range of values for this ratio is between 2 and 125.

The amplification factor, or μ , of a triode tube was long considered to be a fundamental parameter of tube behavior. It was convenient, because, like β , its value was apparently slow-varying. But, like β , it is ill-defined from device to device, since its value is a function of the poorly stabilized plate conductance parameter. The transconductance parameter, on the other hand, is a function of a slowly changing κ , which does not vary greatly from device to device, in addition to the Fermi parameter and the device (plate) current.

Examination of the characteristic curves for triode tubes shows that plate current rises rapidly with plate voltage. In fact, power increases at the approximately 2.5 power of plate voltage for constant grid bias. At constant plate voltage, however, power is linear with plate current. Clearly, the preferred mode of operation is with minimum plate supply voltage which will permit the development of the required plate current. The equation for the required plate-supply voltage may be obtained from modification of Eq. 3-33:

$$V_{BB} = V_{BI0} + V_{CC} \quad (3-38)$$

where V_{BI0} is the plate voltage at the required plate current with the grid bias at essentially zero volts at the zero bias contour, and the value of V_{CC} used may neglect the V_{csat} term since it will be small compared to the first term on the right in Eq. 3-33.

Typically, the supply voltage is increased by approximately 10 to 20% to allow for variations due to differences in plate conductance from tube to tube and to allow for the contact potential normally encountered in the tube. (This is the reason the earlier statement says “grid bias is essentially zero volts”, not exactly zero volts.) Contact potential developed on the grid of a tube may vary between as little as 0.3 V negative and approximately 2 V negative, depending on device design and cathode temperature.

The difficulties in the use of amplification factor as a design parameter are recognized readily if one notes that each of the following tubes has the same nominal value of μ :

Tube Type	Typical zero-bias g_p	Corresponding I_b
12AU7	177	13 mA
6J5/6SN7	220	13 mA
12RH7	340	27 mA
5687	613	33 mA

In each instance, the typical values of g_p and I_b correspond to those for approximately half-rated power dissipation. These conditions occur at about 100 V on the

plate for the 12AU7 and the 6J5/2SN7 tubes and at about 70 V for the other two.

This discussion leads one rather directly to an important deduction about triode characteristic curves for tubes; they ignore important relations for the devices. An examination of the variation of μ with operating conditions shows that it is *not* either a constant for a given sample tube nor is it repeatable from sample to sample for a given tube type. On the other hand, the value of transconductance does present a repeatable set of contours as a function of I_b and V_b from tube sample to tube sample, and as a result presents a sound basis both for efficient design and for reliable operation of the device in its circuit.

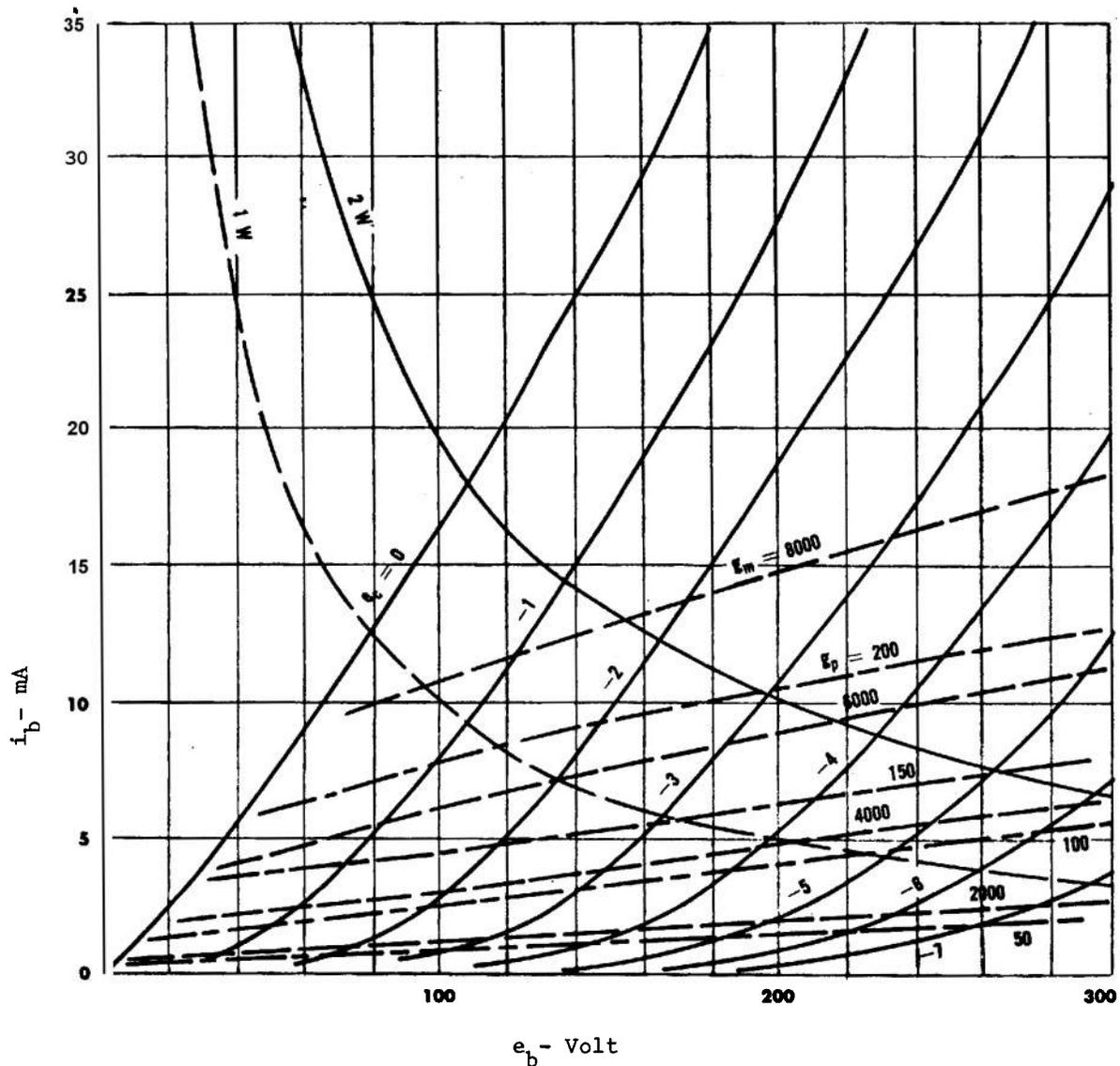


Fig. 3-1. Plate Characteristic Curves, Tube 6BQ7A

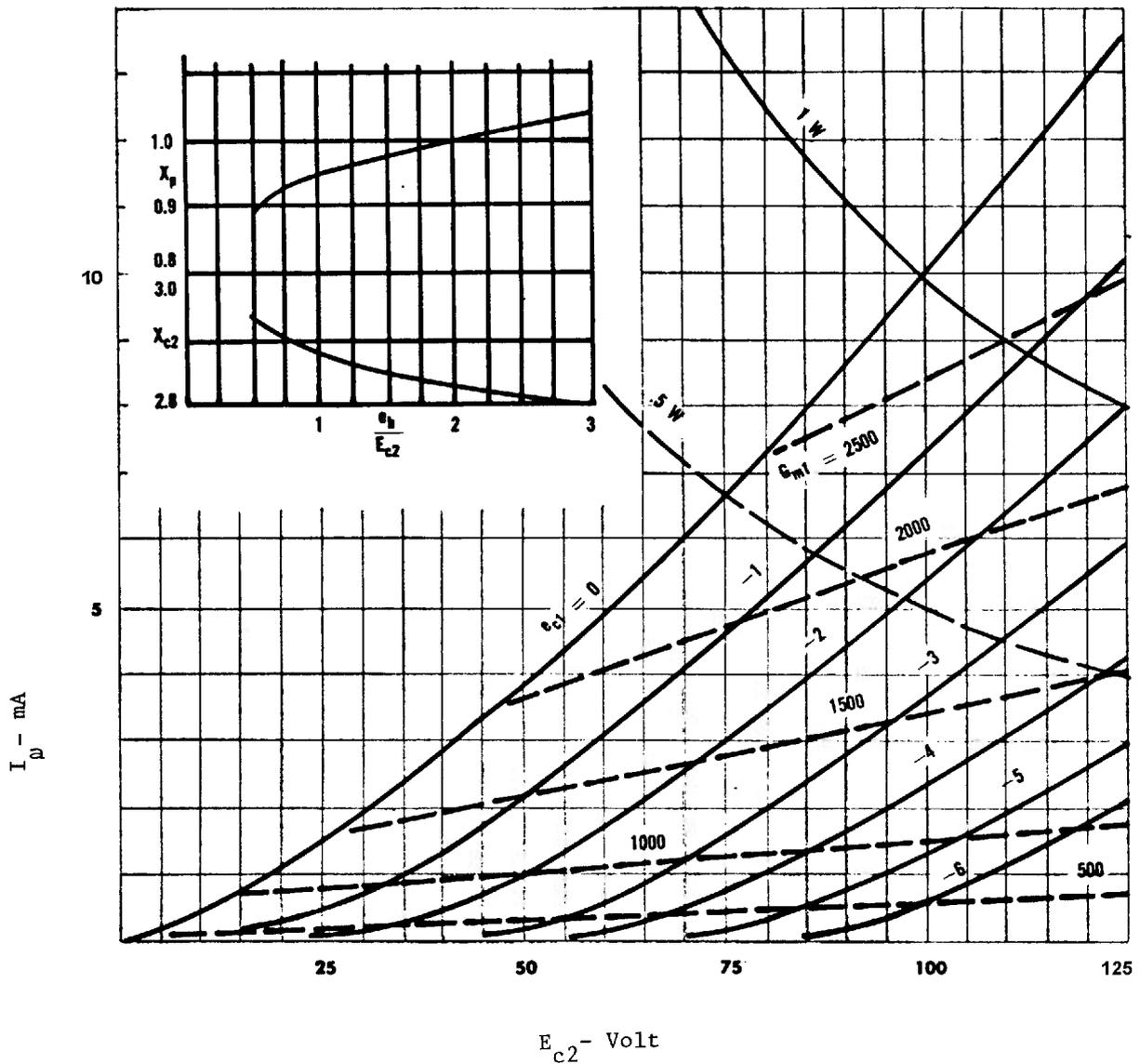


Fig. 3-2(A). Screen Characteristics Curves, Tube 6BE6(1)

3-5.2 TETRODE AND PENTODE TUBES

Tetrode and pentode tubes have electrical characteristics which in many ways parallel those of triodes, but they have some significantly different characteristics as well. As with the generalized active device, the transconductances g_{mi} from control-grid to plate with tetrodes and pentodes are defined in terms of the κ equation (Eq. 3-18), which takes the form

$$g_{m1} = \kappa_1 \Lambda I_b \tag{3-39}$$

The κ parameter here carries a subscript because both the control grid and the screen grid voltages control plate current, and as a result may have transconductance efficiency factors. For the screen-to-plate transconductance, the equation takes the form

$$g_{m2} = \kappa_2 \Lambda I_b \tag{3-40}$$

and the values of the two κ 's will differ substantially. In fact, the so-called screen grid μ for these tubes can be defined in terms of the ratio of the two κ 's

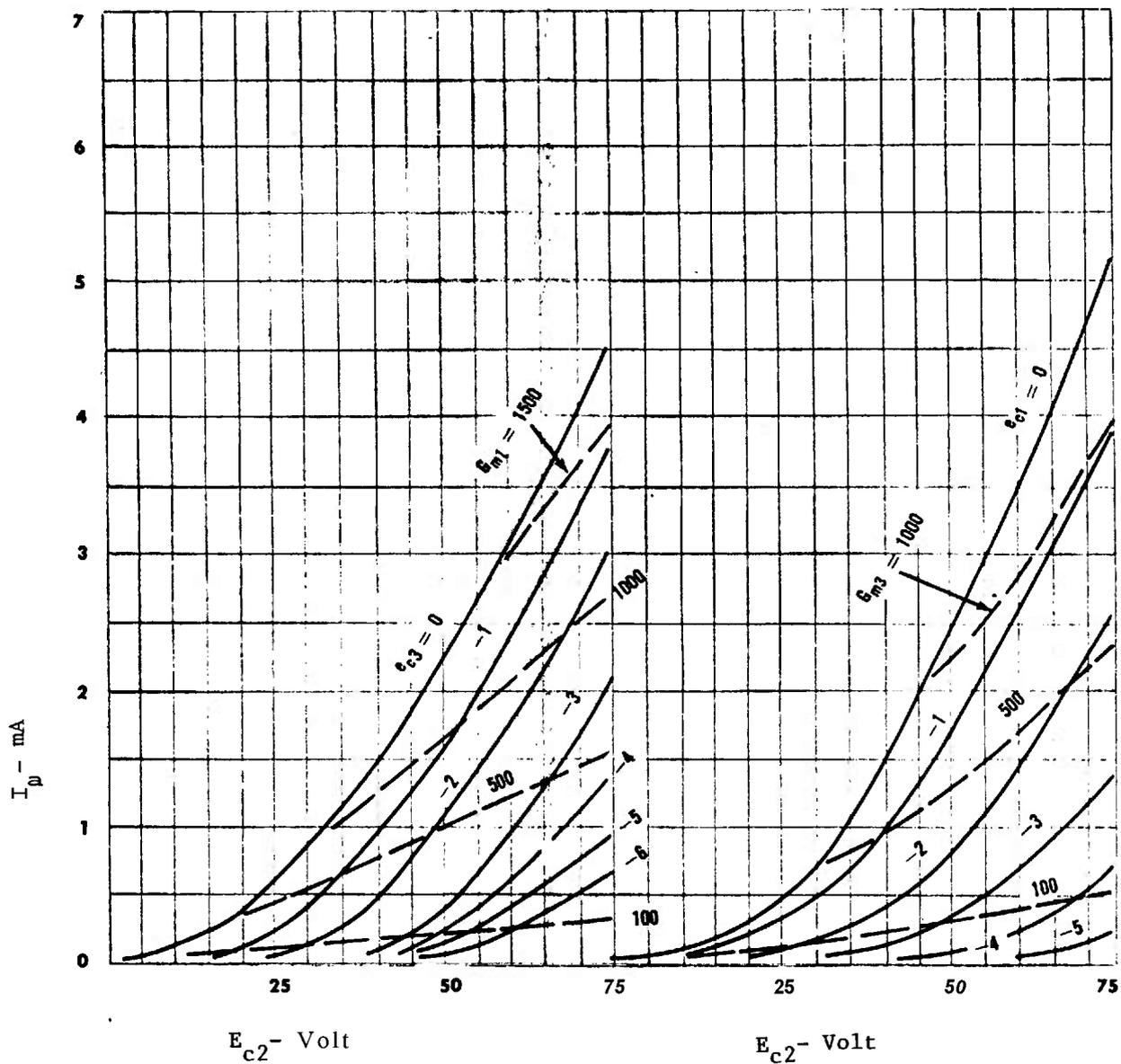


Fig. 3-2(B). Screen Characteristics Curves, Tube 6BE6(2)

$$\mu_{12} = \kappa_1 / \kappa_2 \quad (3-41)$$

Typically, the range of values of μ_{12} is roughly from approximately 2 to possibly 50 or more.

Eqs. 3-39 and 3-40 indicate that whereas the plate currents for tetrodes and pentodes, as with triodes, vary substantially with operating voltages, the values of transconductances are defined essentially by plate current. With tetrodes and pentodes, however, the values of the plate conductances under normal operating conditions are very, very small compared to both g_{m1} and g_{m2} . As a result, static curves for these devices should be based on the variables I_b , V_{c1} , and V_{c2} , and not on V_b . Once static curves are plotted on the revised basis, and contours of constant V_{c1} and g_{m1} as a minimum plotted as a function of I_b and V_{c2} under conditions that a constant ratio of V_b / V_{c2} is maintained, the resulting set of curves proves to be almost ideal for the design of circuits based on the criteria of minimum stress and minimum power dissipation. Correction curves can be used for adjusting the current levels and transconductance levels for different ratios of plate-to-screen voltage.

A study of power output relations for power tetrode and pentode amplifiers shows an interesting result. As the screen voltage V_{c2} is increased from zero, with a constant supply voltage V_{bb} , the power output capacity of the amplifier increases at first, but then it levels, so that further increases of screen voltage provide *no further* increase in output power. Since the input power increases as the 2.5 power of screen voltage, however, the only consequence of further increase of screen voltage above the critical value is a rapid increase of dissipation, and a rising tendency for self-destruction of circuit components.

This concept of the use of minimum screen voltage has not been used largely because the characteristic curves for tetrodes and pentodes are plotted as a function of I_b and V_b for usually a single fixed value of V_{c2} , and the designer, even if he is aware of the importance of correct selection of screen voltage, has no satisfactory way of making the proper design adjustments for selecting the proper voltage. Rather than attempting to correct the basic design data deficiencies, the approach chosen by device makers has been to attempt to build "better" devices. The writer has seen many power amplifier circuits in which the screen voltage

applied was from 1.5 times to several times that required, and it sometimes was as much as 1.5 to 2 times manufacturer's peak rated values!

If reduction of screen voltage does cause a degradation of design characteristics, a tube (or other active device) having a higher value for g_{m2} should be selected, not higher supply and operating voltages as apparently is the normal procedure. The penalties of the voltage exponent law are just too severe to risk careless increases in the selected supply voltage.

With frequency multipliers (of the tuned harmonic type), the results of increase of screen voltage are even more dramatic and startling. Initially, power output increases as the screen voltage is increased from zero. The output levels off shortly, at roughly the point where the peak conduction angle equals a half cycle of the output wave, then power output *drops steadily* as the current flow damps the tuned output circuit. As before, power input rises catastrophically, and the tube soon can't take it!

3-5.3 MULTIGRID TUBES

Applications are frequently encountered in which more than one independent point of control is required for mixing signals into a combined output. This function normally is accomplished by the use of multigrid tubes which have between three and six internal grids. Typically there are two control grids which are used for injecting the two signals. These grids are separated by one or more shield grids (screen grids) to minimize capacitive coupling and to provide final acceleration of the electron stream toward the plate.

These tubes are devices in which the principal function is the variation of the transconductance from one grid to plate by variation of the voltage applied to the second. The range in variation is a strong function of the screen voltage as is the case with any conventional tetrode or pentode tube.

The variation of the transconductance is obtained primarily by current diversion with the typical multigrid tube. The current may either be diverted at the first control grid, as is the case when the local oscillator signal in a frequency conversion is introduced at this point, or it may be diverted to the screen as a result of the bias on the second control grid.

It is interesting to note that the point of injection of the high-amplitude converter signal has a significant effect on both the conversion efficiency for the tube and also on the total power dissipation. Applying the converter signal on the first control grid leads to a substantial reduction of the average cathode current and leads to a substantial reduction of total input power compared to applying the converter signal on the second control grid. At the same time, however, the conversion efficiency is reduced when the converter signal is applied to the first control grid. As a result, a critical trade-off must be made, one which often is accomplished best by reduction of screen voltage.

The noise generated in multigrid tubes is primarily a function of plate current and current division between screen and plate. It is not directly dependent on transconductance (other than through the dependence of transconductance on space current). As a consequence, it is of considerable importance to the user to know how to obtain both a maximum transconductance per unit current, and also a maximum change of transconductance for a given maximum current. None of these relations can be expressed in tractible form in terms of any control-grid bias value.

It is, in fact, very helpful to have screen characteristic curves similar to those found most helpful for pentode tubes in determination of the proper operating environment for a converter tube. It is also important to have curves which show the variation of transconductance on one control grid with variation of bias on the other, with the coordinate system based again on screen voltage and plate current. The only source of these curves known to the author is his *Conductance Curve Design Manual* (Ref. 1) and Fig. 3-2.

Conversion action in any kind of a conversion device is dependent on the manner of variation of either conductance or transconductance (or possibly variation of resistance or transresistance in yet unbuilt devices) as a function of the control signal bias. The conversion properties may be developed either in terms of a power-series expansion on the nonlinear characteristics of the active device, or an orthogonal-series expansion in similar format. The procedure for doing the latter is described in Appendix C. The orthogonal-series expansion in terms of Legendre polynomials is really a regrouping of the standard power-series expansion in a form which gives independence of different-order harmonic components. Ideally, the normal mixer action is based on the square-law, or second-order, term, and the equation normally used for determination of conversion gain is based on an assumption of predominance of the square-law term

$$K_c = 0.25 \frac{(g_{m \max} - g_{m \min}) Z_L}{(g_{m \max} + g_{m \min})} \quad (3-42)$$

where Z_L is the tuned impedance of the load circuit at the output frequency.

Examination of typical curves on mixer or multigrid tubes shows that as the screen voltage is increased from zero, the available maximum transconductance at zero bias at first increases rapidly, and then levels off to a relatively slowly changing number regardless of either screen voltage or plate current. This leveling or transconductance occurs at a screen voltage substantially less than the recommended operating voltage for the device. As a matter of fact, calculations of element dissipations made at the recommended screen voltage value usually indicate that the device will exceed its dissipation rating if the conversion signal voltage either decreases substantially or fails.

A study of typical curves on these tubes, Fig. 3-3, indicates that for best signal-to-noise ratio, the input signal should be applied on the number one control grid, and the local oscillator or switching signal to the second control grid. This arrangement leads to a maximum value of effective κ and a minimum noise figure, but it also leads to maximum total dissipation at the given screen voltage. The screen voltage chosen should be that which defines the point at which κ begins its sharp decrease with increased screen voltage.

3-5.4 POWER APPLICATION CONSIDERATIONS

One of the consequences of the discussion of the basic limitations in par. 3-2 is that in order to get substantial blocs of power from any amplifier operating under reasonable input and output matching conditions, it is essential that the active devices used have κ -values which are substantially less than unity. At the present state of development of solid-state technology, this means that high-power amplifiers must be based generally on electron-tube devices such as multielement tubes, klystrons, and traveling-wave tubes. Varactor diodes can be used effectively in the intermediate power range as signal up-converters, and eventually other solid-state devices capable of producing intermediate amounts of power at least undoubtedly will be developed. But they can be expected to be specialized devices or devices having κ -values which are substantially less than unity. Clearly, field-effect transistors have a significant potential in at least the intermediate-power range, and they eventually may prove capable of developing fairly substantial amounts of power.

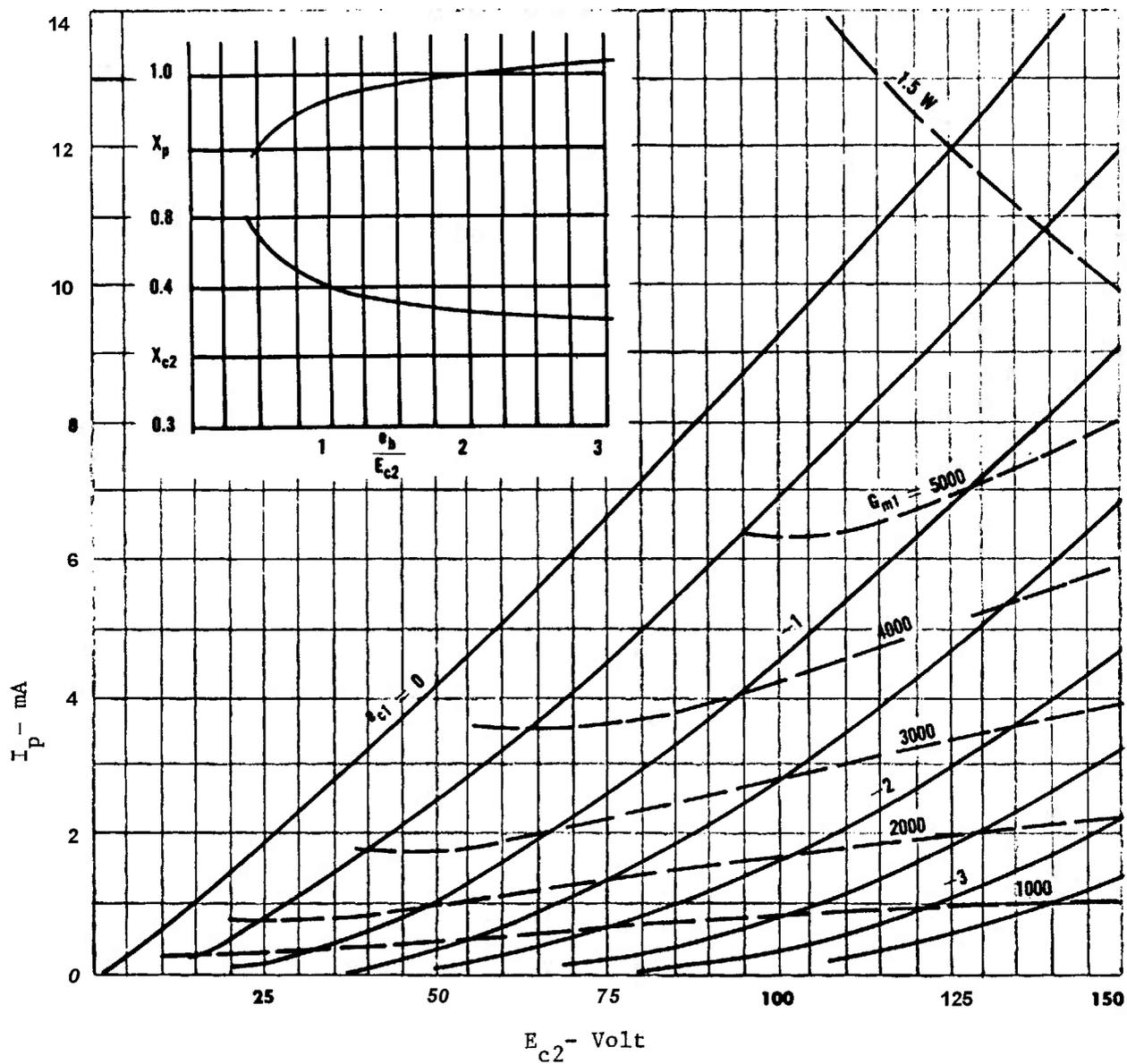


Fig. 3-3. Screen Characteristic Curves, Tube 6BH6

3-6 CRITERIA FOR RELIABILITY

Design for reliability requires the coordination of a wide variety of properties and characteristics for components, both mechanical and electronic. It is of particular importance that static and small-signal electrical characteristics be coordinated properly, since lack of coordination is one of the important causes of poor reliability.

Normally, a study of reliability is a negative sort of operation in that it is approached through examination and control of the causes of nonreliability, or low reliability. As has been noted in earlier paragraphs in this chapter, however, it is possible to take a positive approach on important facets of the problem based on the discussion in par. 3-4. One of the key differences which makes possible the use of a positive approach is the proper use of the techniques of information engineering in the development of characterization criteria.

Probably the first and prime step in the establishment of reliability criteria is the establishment of the boundaries which represent the limitations on the controlled characteristics for the component or device in question. Some of the limitations are commonly known: breakdown voltage, power dissipation limitation, current-density limitations, and similar factors. Many, however, are either poorly known, or possibly not known at all. Often it is these factors which cause difficulties in circuits.

The ultimate limit in reliability is achieved when failures are truly random and completely unpredictable. Superficially, this would seem to indicate that the failure rate for all components should be equal under the normal range of operating conditions. Practically, however, it is impossible to achieve a system in which the failure rate for all parts is identical, and a different criterion must be selected.

If one examines the behavior of components in systems, one finds that there normally is a region of operation in which failures are rare or unlikely, but when operating conditions reach a possibly undefinable level, the probability of failure rises substantially. Conversely, with any given configuration, improvements in reliability as a result of redesign may be easy to obtain to a certain level of improvement, and then become progressively more difficult to obtain.

Improvement of reliability in terms of these criteria generally makes more sense than either attempting to attain an excessively high value for all components or being satisfied with an excessively small value based on the poor reliability of the few components. Limitation of collector supply voltage to the minimum which permits the devices to perform as required provides a very

economical way of improving the reliability of a given circuit. Typically, this may require that the collector and the base supply voltages be provided from separate sources, with the base supply providing a substantially higher voltage but at a sharply reduced current level. The voltage level required for the base supply will be about the same as is used normally for the entire circuit.

The optimization of the reliability of a system on a circuit-by-circuit basis might appear to be an excessively time-consuming and difficult problem. Actually, however, such need not be the case, since it is entirely practical to test at the design stage (on paper) the effects of voltage reduction on circuit performance. Since it is necessary to limit voltage gain for reasons of circuit stability, proceeding in this manner might lead to an occasional additional amplifier circuit but it should at the same time lead to substantially reduced power consumption and substantially reduced cooling problems. Both of these are important criteria for reliability.

There are other important criteria affecting reliability. For example, the problem of keeping dust, dirt, and moisture out of a set of equipment is relatively simple if the proper filters are used and the air pressure within the operating unit is maintained at a value greater than ambient. These requirements almost would appear to be so obvious that they would be trivial but, unfortunately, such is not the case.

The air which is circulated through equipment for cooling purposes should be introduced into the equipment chambers directly as it leaves the cleaning, mixing, and distributing network. It should not be introduced through a mixing chamber which is open to dust, moisture, and diversion (as would be the case if the interior of a shelter were used as the mixing chamber).

Introduction of the cooling air at an elevated pressure assures that all air leakage taking place is **out** of the instrumentation. This assures that dust cannot easily slip in through cracks, and it thereby reduces the difficulty of assuring a tight seal on the compartment. The positive pressure differential also minimizes the leakage of moist air back into the compartment after the power has been turned off.

The air should be forced through the required filters by fans which are so placed that air leakage into the compartment around the fan is minimized. Fairly tight filters can be used if proper drive fans are available, whereas otherwise, inadequate filtering or inadequate cooling must be accepted.

Equipment must be designed to operate reliably under the most adverse conditions it can be expected to encounter during normal use. For example, in an aircraft which may be parked in the direct sun on a ramp,

it can well be that in the tropics the internal equipment temperature may approach the boiling point of water. One of the most important design problems which must be solved with such equipment is finding ways of assuring that such equipment can be ground-tested without it failing because of the adverse environment. Circulating fans which will cool the equipment down, along with some kind of "vestigial" air conditioning equipment, must then be provided which will provide the requisite cooling. And protection must be available to prevent the equipment from being activated until adequate cooling has been achieved.

It is not possible to discuss all of the possible criteria which require consideration in order to maximize reliability at minimum overall cost. The previous paragraphs discuss some of the more severe problems the author has encountered, and the reader should be able to extend the list based on his own experience.

3-7 INFORMATION ENGINEERING

One of the ideas which has of necessity required considerable attention in this chapter has been the idea of information engineering. (This term is defined in Appendix H, and the subject is discussed in greater detail there.) The development of knowledge on the limitations to the capabilities of active devices has of necessity required an examination of the relative importance of the different kinds of information available on different devices in order to determine what should be specified for characterizing the respective devices. Only through doing this can one maximize the chance of assuring any kind of reliability, let alone one which approaches that which *should be readily available*.

One view which the reader may have drawn from the discussion in this chapter is that the information which is provided with active devices frequently differs substantially from that which defines the simplest and most direct determination of reliable circuit configurations. The summaries in this paragraph are for this reason included to emphasize at least one way in which the required data may be organized to assure better opportunities for the development of higher *assured reliability at the design stage*.

As has been pointed out by Frosch (Ref. 2), it is not always essential that *all* parts of a system have essentially equal reliability; the required level of reliability is a function both of what can be obtained on a cost-effective basis, and also it is a function of the importance of the part or assembly in achieving the most vital parts of the goal for which the instrument has been built. A circuit to operate a light used for verification

at a glance that everything is in normal operation does not necessarily have to be as reliable as the basic circuits themselves, for example, *unless* instantaneous verification of proper operation *must be available to the user at all times throughout the mission*.

Clearly, however, this consideration does not justify a poor reliability if a better reliability can be obtained at substantially the same cost. Use of expensive and complex redundancy-type techniques should be used only after optimum reliability has been obtained based on the best possible design philosophy.

Probably the least expensive overall approach to improved reliability is the design of characteristics and parameter displays (technical data sheets) in a way which maximizes the ease of obtaining and using the critical parameters which can assure increased reliability. This is particularly true if these data are made available as supplementary information to standard device data sheets. Curiously, the additional information which usually is required either is known rather precisely, as with the Fermi parameter A , or it would only need to be known approximately as with m and κ .

In preparing revised information display sheets, it is important that the user's problems be considered as well as the maker's, as often one of the underlying reasons for demand for commercial engineering services is the difficulty of extracting critical kinds of information from a specification sheet. (Typically, the designer only knows that he has problems, but he may not know their source.) The required engineering information for use of the device should be readily available from the data sheet by the average engineer if reliability of operation of the resulting network is even modestly important. There should be *no need* for the designer to *limit* his *device alternatives* to those with which he has had extensive experience.

3-7.1 DATA FOR BIPOLAR TRANSISTORS

The curve data which are required for presenting static characteristics of these devices include the typical output curves as a function of base current, but they also should show input characteristics as a function of a third parameter. Convenience of use and coordination with the output curves suggests the basic format shown in Figs. F-17 and F-78 for PNP and NPN transistors, respectively. The input characteristics must be expressed in a form which gives clear coordination over the active operating range for the device. It is for this reason that plotting coordinates have been chosen as V_c , and V_b along with I_c , and the contouring based on I_b in the curve set in Appendix F. Only this kind of a

configuration can be used simply and directly in conjunction with standard collector families of curves.*

The expanded curves shown in Appendix F provide an excellent presentation of static environmental conditions, but they present no useful data on small-signal conditions, which are equally vital to the design of both amplifying and switching circuits. The selection of small-signal parameters must be made among such items as

$$\beta \text{ (or } h_{fe}), h_{ie}, y_{ie}, f_{\alpha}, f_{\beta}, f_r, f_{max}, f_{n1}, f_{n2}, \Lambda, m, r_b, r_e, r_c$$

various capacitances, and other parameters. Some of these parameters are slowly varying in some sense, and many are either simple or complex functions of voltages and/or currents. Some are nearly independent of voltages and currents, and others are strongly dependent on them. They may also be functions of temperature.

The parameters selected for use should be the ones which fulfill as many of the following criteria as possible:

1. They should have a strong direct effect on circuit behavior.
2. They should depend on device design and as little as possible on manufacturing variations.
3. They should depend on variables which are controlled.
4. They should be accessible to contour plotting on static curve sets.

Based on these criteria, one can conclude that preferred small-signal parameters include

$$f_r, f_{max}, f_{\alpha}, f_{n1}, f_{n2}, \Lambda, C_{cb}, r_b, r_e, \text{ and } r_c$$

The intrinsic input admittance can be expressed approximately in terms of the equation:

$$y_{i^*} = \Lambda I_b (1 + m)^{-1} \tag{3-43}$$

and the intrinsic output admittance can be estimated to adequate accuracy from the slope of the I_b contours in those rare cases where it is really needed. (Usually, if the number is needed in the design process, the procedure can be assumed to be one which will lead to an unreliable design if the author's experience is typical.)

It is interesting to note that based on Eqs. 3-14 and 3-43, one would expect that the small-signal β and the DC β were equal. Of course, this is not true, although

* This same kind of curve set is used by some foreign manufacturers. See Appendix E.

there is a relation based on an integral between them. Actually, both of these equations are approximations in that they have neglected components dependent partly on base and partly on collector voltage, and the component of collector current which is dependent on collector voltage is substantially larger than the component of base current. When these two correction terms are included, then the ratio of Eq. 3-14 and Eq. 3-43 does not yield a value of small-signal β which is equal to the DC β .

Now, the data for f_{α} , f_r , and f_{max} at least are related to one another, so that usually one of the group may be selected provided the data required for deriving the others are known at least approximately. Good practice in the design of a circuit requires the designer to select an operating frequency less than f_{n2} if at all possible, and f_{n2} may be from ten to thirty percent of f_{max} , for example. All of these frequencies are functions of V_c and I , and, as a result, one of them should be contoured on a collector curve family for the benefit of workers who do have to use the devices near their limit frequencies. The frequency f_{n1} is not, to the author's knowledge, dependent on any other defined device parameter, so its approximate value should be published to indicate where the upper edge of the excess low-frequency noise band may be. The approximate value of f_{n2} also should be provided to indicate that frequency above which excess high-frequency noise may be expected. Typical values for these frequencies should be adequate.

The approximate data on the important diffusion and transition capacitances are defined in terms of the f_{α} , f_r and f_{max} group of frequencies. The preferred frequency to select could well be dependent on the relation between frequencies and capacitances, and requires more detailed analysis than apparently is available at present.

The value of m is a function of device current, and it has a limit magnitude of less than 0.45 for presently used materials. Its sign is positive with PNP transistors, and negative with NPN devices. Its maximum value and the point at which it becomes significant are dependent on basic device design and on the device (output) current. Some data on the variation of m with I should be made available.

The manner of variation of C_{cb} with device operating characteristics and applied voltages and currents apparently needs clarification. A substantial set of contours of this parameter supported by an analytic development of the theoretical basis of the curves would appear to be desirable.

The values of the various spreading resistances are primarily of importance in the determination of the

limits of the effects they can have on circuit behavior. For this reason, it appears desirable to have a typical value and a value below which a given percentage of devices can be expected to have their values of these resistances included as a minimum requirement. These data—the typical, say the **95%** confidence value—could be very useful to the serious designer of specialized circuits, particularly if he is concerned with making substantial improvements in circuit reliability.

Because of their special nature, both the Fermi parameter and the device β deserve some special notes. The Fermi parameter is defined as the ratio of electron charge q to the product of the Boltzmann constant by the absolute temperature kT , i.e., $q/(kT)$. It is a fundamental physical parameter which is dependent only on absolute temperature. Material processing has no effect on its value; neither do nuclear radiation fields or other related phenomena. Yet it specifies the important forward properties of the device as well as the input properties. In principle, it also specifies the output and reverse admittances as well. Those people who have known how to use it have found it extremely valuable, but values of r_b are vital to its successful use.

3-7.2 BETA (β)

The parameter β historically originated with the point-contact transistor, and it was applied to junction transistors because it appeared to be relatively constant in value as viewed from the basic back-to-back diode equations. The apparent constancy soon proved itself to be an illusion because the variation of β with collector current follows a shape similar to that shown in Fig. 3-4. Particularly, the β 's of different devices made in exactly the same way could vary by a range of at least ten to one, so much so that until just recently at least it has been common practice to sort production into as many as three or more different groups and sell them as different devices having different EIA registration numbers.

The reasons for the variability of the β are not hard to find. The definition of β mathematically is

$$\beta = \partial I_c / \partial I_B \quad (3-44)$$

where the base current I_B is further defined by the equation

$$I_B + I_E + I_C = 0 \quad (3-45)$$

In this last equation, I_E is a small difference of two

larger currents, and mathematically such differences are *always* suspect.

Further, the transistor itself performs exactly this mathematical differencing, and only a small difference between the generated emitter current and the extracted collector current flows out of the base lead. As a result, small variations in carrier lifetime in the base region and in the thickness or the conductivity of the base region can, *and do*, cause substantial changes in I_B and make control of the value of β very difficult at best.

The variation of the β in a given transistor is easily explained. At very small values of device current, all flow is by diffusion. As the current level increases, an aiding field is generated in the base as a result of diffusion, and throughflow increases, causing an increase in β . Theoretically, the β can be doubled through the influence of this field. As the current is increased further, however, the density of minority carriers entering the base first substantially exceeds the equilibrium value, and then may eventually exceed either the intrinsic value n_i for nonpolar semiconductor, or even the majority carrier equilibrium level. Since approximate charge neutrality must be maintained in the base region, additional majority carriers are drawn into the base region (it is this change in majority carriers which introduces the polarizing voltage which makes the m -factor significant), and the lifetime of the minority carriers in the base drops sharply. The result is a sharp decrease in β .

3-7.3 THE FIELD-EFFECT TRANSISTOR

The representation of the static characteristics of the field-effect transistor is similar in some respects to that for the bipolar transistor, and in some respects to that for electron tubes. The device is voltage (or charge) controlled, but it draws negligible control electrode current. On the other hand, the control of current is in principle temperature-sensitive in that the nominal control voltage required to establish a given current is very temperature sensitive.

The large segment of effectively “uncontrolled” current flowing in the FET device reduces the apparent temperature sensitivity of the bias contours to a point that even though the FET is theoretically as temperature sensitive as the bipolar device, for practical purposes the change in position of the bias contours is quite small. This is important since there is no space-charge cloud formed by thermal emission reducing the temperature sensitivity of this device as there is with the electron tube.

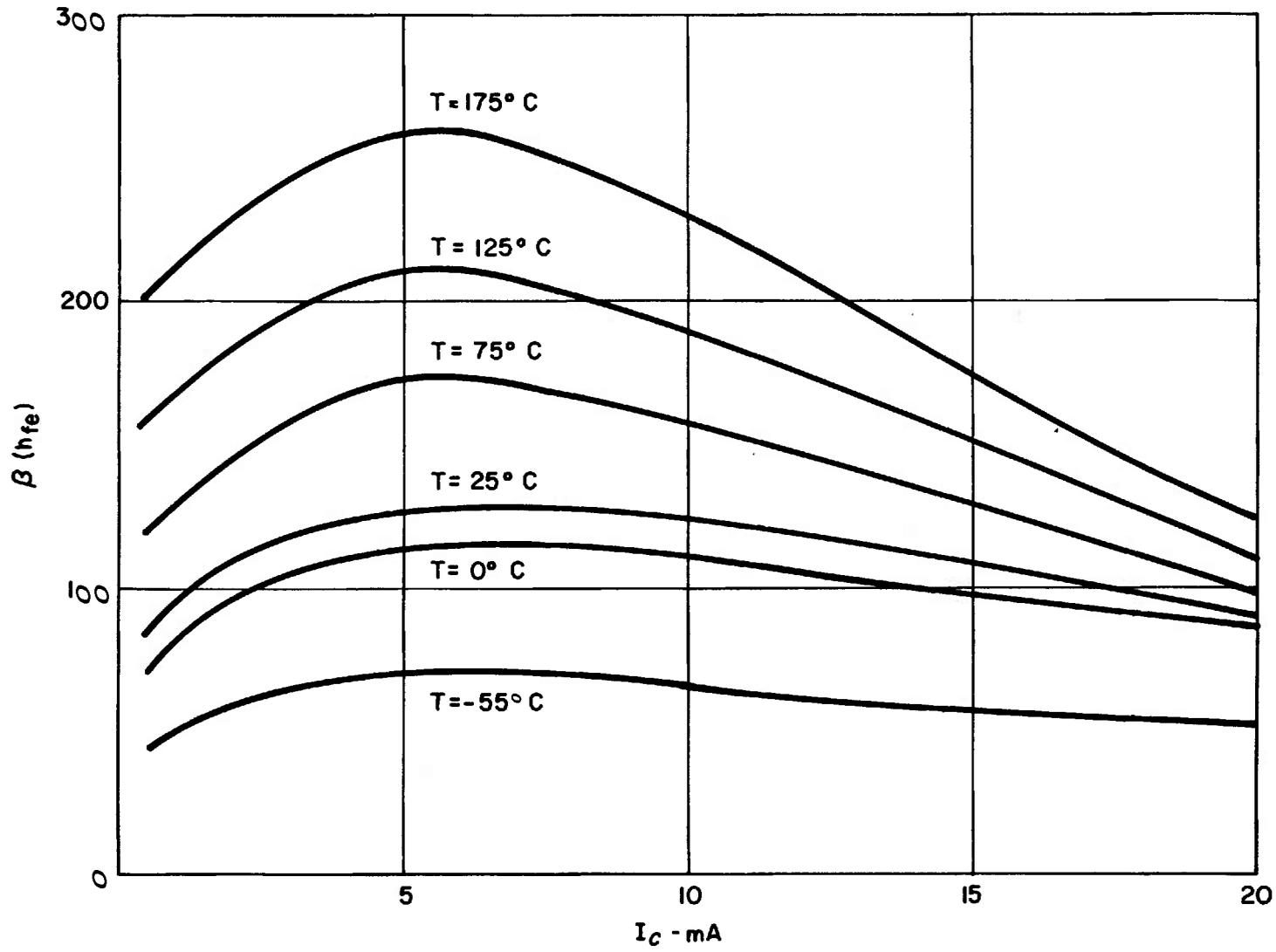


Fig. 3-4. Curve of $\beta(h_{fe})$ vs I_c for NPN Transistor 2N736

Existing static characteristic curves used with FET devices appear to provide the design data required for establishment of the proper operating environment. The small-signal data which control point-by-point operation of the circuit are completely missing, however. It is generally recognized that FET devices are transconductance devices, and that their transconductances are primarily a function of output current (drain current). This being the case, the user is entitled to ask the question of how he can get the necessary data.

Examination of the static curves indicates that the variation of transconductance with drain voltage for these devices is probably slow, sufficiently slow that for a first approximation it may be assumed to be zero. If, then, a curve of the value of the κ -factor as a function of device current, or the curve of transconductance as a function of device current is provided, adequate data on the transconductance will be available. (If the κ -curve approach is selected, it may have two ordinate scales—one for κ , and the other for the product of κ and λ at a typical operating temperature. Both ordinate and abscissa scales may be linear, or they may be logarithmic if the range of operation to be covered is sufficiently large.)

The selection of the format for presenting these data represents an important decision, one which is particularly vital to the designer who must apply the device in a network. As is shown in the paragraphs that follow, a strong case easily can be made for including these data in some form on a data sheet; the only problem is the selection of the most effective and useful forms.

Plotting the log of the transconductance against the log of plate current is possibly the most direct and a very useful way to present the data in question. This method of presentation has the advantage that no calculations are required involving any of the factors— κ , λ , or I_d —in determining the effective transconductance. (A linear plot of transconductance against drain current is completely unsuitable in that it restricts excessively the ability of the designer to use his device at low current levels.) This procedure does not make any data on the value of the transconductance efficiency available, however, and data on the way efficiency varies with device current level can be extremely useful.

On the other hand, presenting only the value of the efficiency, or the product of the efficiency by the room-temperature value of the Fermi parameter makes necessary a considerable amount of calculation to get to the important data on transconductance. Consequently, provision of only a curve of κ vs device current also is undesirable.

A combination plot probably is the best answer, one giving values of both $\log g_m$ against \log drain current, and $\log \kappa$ against \log drain current. When this is done, the device can be used either in its low-current (and low-power) mode effectively, or it is possible to select optimum operating conditions for maximizing reliability in the normal operating range. It should be noted that tolerances of $\pm 50\%$ and -25% should be quite adequate for values of κ , and transconductance data which are within 20% either way should be relatively easy to provide.

The reasons why the transconductance and the κ -data cannot readily be obtained from static data are readily displayed. In the first place, the transconductance g_m is defined, as before, as

$$g_m = \partial I_d / \partial V_g = \kappa \Lambda I_d \quad (3-46)$$

where I_d is the drain current and V_g the gate voltage. In a similar way, the κ -factor may be defined in terms of the equation

$$\kappa = g_m / (\Lambda I_d) = [1 / (\Lambda I_d)] (\partial I_d / \partial V_g) \quad (3-47)$$

where Eq. 3-47 is a rearranged form of Eq. 3-46.

In both of these equations, the desired parameter value is a function of the partial derivative of Z , with respect to V_g and, in both cases, the values are rather well controlled and rather stable. In fact, the precision with which the Fermi parameter may be stated is better than 10% *even* allowing for device temperature variation; and it can be within one percent if the appropriate value of absolute temperature is used. Since the value of κ is a slowly varying function of drain current and device geometry and construction, it is probably definable to within 10% or better.

Curiously, the values of static drain current as a function of gate voltage are relatively ill-defined in comparison to the value of κ . In addition, even if the values of drain current as a function of gate voltage were well-defined, the variation of small-signal transconductance from one contour to the next is sufficiently rapid that either an excessively smoothed average must be accepted or an excessively noisy value must be accepted. Since the small-signal value defined in terms of Eq. 3-46 is far more dependable and more precise, the taking of small differences of large numbers to obtain a value of transconductance is totally unjustified.

The figure of merit for these devices should be made part of the standard data provided. In addition, one might surmise that there are noise corner frequencies of which f_{n1} and f_{n2} are typical which are of sufficient importance that their values should be provided.

The impedance of the depletion zone and its capacitance to source and to output are both characteristics of substantial significance for FET devices. The effects of these parameters on device behavior can be minimized by basic device design, since the design which maximizes the effective value for κ as a function of drain current also will minimize the series impedance of the depletion region.

The channel impedance is important in at least two ways—one in that it can introduce what might be called source-spreading resistance, and another in that it can contribute to instability through introducing series impedance in the output section of the channel. These impedances correspond generally to emitter and collector spreading resistances in the bipolar devices, but their magnitudes tend to be much larger than for the bipolar devices.

The source-spreading resistance must of necessity be kept to a minimum since it limits the effective transconductance g_m' , which can be obtained through normal degenerative action

$$g_m' = g_m - (1 + g_m Z_s) \quad (3-48)$$

where Z_s is the source “spreading” resistance in the channel. Evidently the maximum effective transconductance approaches $(Z_s)^{-1}$ as an upper limit, and evidence of existence of this limiting impedance may be found by an examination of the relation of g_m' and I_d . In its absence, a continuing increase of g_m' with I_d is to be expected.

Probably, measurement of collector spreading resistance may be accomplished when required by the use of an AC impedance bridge, with the measurement made on the path from drain to gate. Since both capacitance and impedance may depend on the operating current through the device, provision should be made to apply normal operating potentials during the test. Standard capacitance measuring procedures, obtaining first a capacitance balance and then introducing series resistance for quadrature balance could be required.

3-7.4 ELECTRON TUBES

The discussion of data presentation for electron tubes must be divided into two sections: the first being for triodes, and the second for multigrid tubes. Many

of the considerations already discussed for semiconductor devices also apply to electron tubes, but in different combinations, but there are several unique situations which require special consideration.

The static characteristic curves for the triode electron tube differ markedly from those of transistor devices because the output conductance for triode tubes is almost as large as the transconductance. Typically, it may be as little as one hundredth of the transconductance, but with power tubes it may be as large as half the transconductance. As a result, there is a different shape curve which represents current-voltage relations with these devices. The curve shape is similar to that for a diode in its forward-conduction direction.

As with solid-state devices, the positions of the static contours for a triode are relatively unstable, and much more unstable than the positions of the transconductance contours as a function of plate current. This means that a set of static contours of constant bias as a function of plate voltage and plate current gives the user a completely inadequate statement of the small-signal characteristics of the device. The problem of taking small differences of inaccurately known large numbers (fuzzy values) to approximate numbers which can be specified rather precisely in other ways again is encountered.

Because of the nature of the devices, it is desirable to plot contours of constant transconductance directly on the standard plate family of characteristic curves for triode tubes. In addition, it is desirable to have contours of constant plate conductance plotted directly on these curves, since the plate degeneration term is typically important. It is of particular interest to note that whereas the positioning of the plate conductance characteristic contours is rather unstable as a consequence of the variability of the positions of the bias contours, the relative magnitude of the correction term frequently is sufficiently small that the instability is of reduced importance in this equation

$$g_m' = g_m / (1 + g_p Z_L) \quad (3-49)$$

where g_p is the plate conductance. With these data and Eq. 3-48, it is possible to obtain the kind of point-by-point small-signal information which makes it possible even to calculate switching time and rates for multivibrators. It is also possible to establish operating conditions required for the initiation of transfer in a switching circuit.

Additional data which can be useful for triode tubes include approximate figures of merit, which specify the maximum useful operating frequency, and data which

define the relation of signal-to-noise ratio to operating conditions. A set of curves—which specify on the typical triode plate characteristic curve family the contours of power gain to noise power for a typical (high) operating frequency and also include the open-grid-circuit V_b vs I_b contour—can be used to help select the optimum operating conditions for the tube as a small-signal preamplifier.

3-7.5 MULTIGRID TUBES

The characteristic curve configuration selected for use with multigrid devices such as tetrodes, pentodes, mixers, and converters should permit the designer to operate the device at the lowest screen voltage at which desired operating conditions can be obtained. This means that a screen characteristic curve set (sometimes called triode-connection curves) should be used for data configuration. Since here again both g_{m1} and g_{m2} are dependent on plate current, and can be obtained much more accurately through use of equations like Eqs. 3-32 and 3-33 than by estimating from imprecisely specified static screen-bias contours, contours of constant value of at least g_{m1} should be included. With devices whose use is intended to include variations of V_{c2} as a part of normal operation, contours of constant value of g_{m2} can also be very helpful.

With the mixer type of multigrid tubes, additional curves showing the relation of mixer voltage swing to change in transconductance on the small-signal input make the design of various kinds of converter circuits much simpler. As noted previously, Eq. 3-42 can be used with curves similar to those in Figs. 3-2(A) and 3-2(B) to determine the conversion conductance. The important requirement for any mixer or converter design is that it be possible to read the transconductance as a function of conversion signal on a point-by-point basis. This is difficult at best, and may be virtually impossible without special characteristic curves of the types described.

Possibly one of the most efficient ways of calculating conversion transconductance is based on the material included in Appendix C. The detail techniques are described there and in Chapter 12.

3-8 MEASUREMENT TECHNIQUES

There are two basic types of measurements required for the determination of the small-signal behavior of transistors, and a number of special measurement techniques required for some of the remaining parameters. The basic measurements are for self-immittances and

for transfer immittances. Self-immittances are measured by introducing a small magnitude of alternating signal either into the input or the output, and comparing the voltage across the transistor itself with the voltage across a standard resistance. The voltages across the respective immittances, the standard and the unknown, may be repeated by the use of isolation amplifiers, and their magnitudes compared by adjusting the magnitude of one to equal that of the other through the use of a calibrating potentiometer. Typical circuits for making these driving-point immittance measurements are shown in Fig. 3-5. Methods of measuring r_b and C_c will be described in later paragraphs of this chapter.

Fig. 3-5(B) shows one method of measuring the parameters y_o , and y_c or h_o . Because the shunting capacitance from collector to emitter is normally small compared to the collector conductance, it often can be ignored in low-frequency measurements. The signal voltage from B_1 to ground is repeated by an isolation amplifier, and a portion of it compared against the voltage from B_2 to ground to determine the effective collector admittance. A variable capacitance could be placed in parallel across the standard resistance to give an approximate measurement of the equivalent capacitance from collector to emitter if desired.

The circuits in Fig. 3-5(B) and (C) may be used either with the base terminal of the transistor bypassed to ground to give a low-impedance input circuit, or they may be used with the base circuit open to signal frequency. In the former case, the measurement gives the value of y_o , and in the latter, the value of y_c (or h_o). Both these measurements are useful in connection with the design procedures discussed in the remaining chapters of the book.

The method of measuring y_o and y_c shown in Fig. 3-5(B) is excellent for use with low-power transistors, but it is difficult to use with power transistors, primarily because of the difficulty of building a high-current power supply having good voltage regulation and a high internal signal impedance. An arrangement that can be used with power transistors with their relatively high collector admittances is shown in Fig. 3-5(C). In this circuit, the signal is introduced in series with the collector supply, and the standard resistance is placed in series with the signal source and the collector. A repeater amplifier with an isolation transformer is used to separate and amplify the voltage developed across the standard resistance. The amplified voltage is then compared with the voltage on the collector to give the approximate value of the conductance. As long as the gain of the amplifier is adequately controlled by feedback, a relatively small value of standard resistance

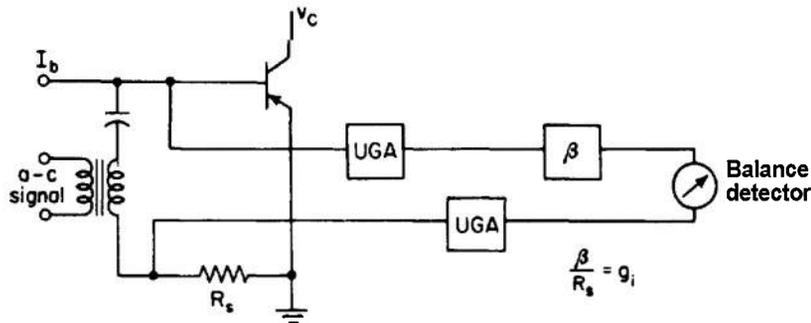
may be used to measure the conductances normally encountered with power transistors.

Although the use of an isolating transformer may appear to be undesirable, actually, if it is properly loaded, it can be calibrated and is somewhat more satisfactory than a differential amplifier for the purpose. A small error in the differential action can be quite serious, whereas no such error can develop with a transformer, only ratio or phase errors, which are much easier to calibrate and maintain than is the differential action. The use of a load resistor whose value is in the neighborhood of 10,000 ohms across the output winding of a unity-ratio transformer having an open-circuit reactance in excess of 50,000 ohms at the measuring frequency gives a circuit capable of accuracies in the neighborhood of a percent after calibration. The coupling coefficient for the transformer should be as nearly unity as possible, greater than 0.999 being desirable.

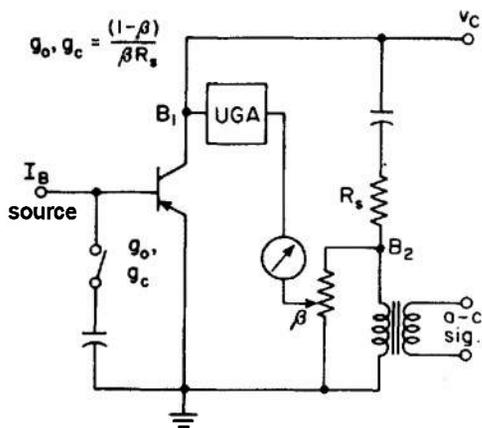
The better the grade and quality of the transformer, the more accurate the results that can be obtained.

The trans-immittance parameters are all basically measured in a similar manner, with the input signal applied at one point, and the output taken from a completely different terminal on the device. These parameters may be called transfer functions, transfer ratios, transadmittances, or trans-impedances. The ones of particular interest in the balance of this book are the parameters h_f or h_{fe} and y_f or y_{fe} . The reverse trans-immittances can also be measured by the use of the same basic circuit as for the forward.

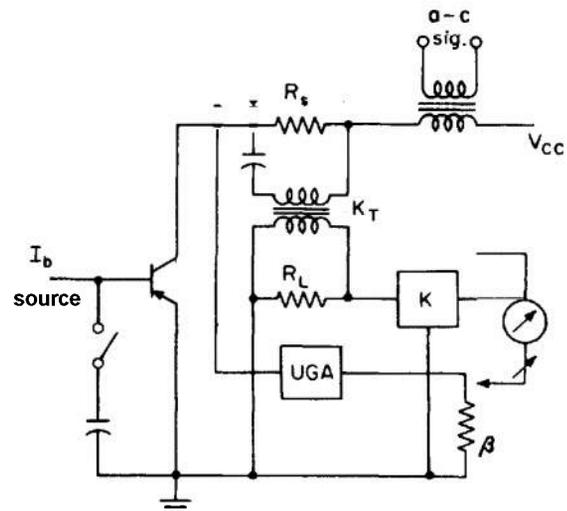
These transfer immittances can be either transfer admittances or impedances or they can be transfer voltage ratios or current ratios. The transfer voltage and current ratios are really the ratios of a transfer impedance to a self-impedance, or a ratio of a transfer admit-



(A) Basic Input and Forward Immittance Circuits



(B) Output Admittance-Low Power



(C) Output Admittance-High Power

Fig. 3-5. Typical Circuits

tance to a self-admittance, with the result that they may be classed as immittances.

The basic circuit for the measurement of either h_f or y_f is shown in Fig. 3-6. The only difference between these two measurements is the point at which the reference signal is extracted. If the reference signal is extracted at the point A, ahead of the current-limiting resistor R_s , the measurement is that of the current ratios, or β or h_f . If the reference voltage is extracted at the point B at the base lead, then the measurement gives the forward admittance y_f . The value of the load resistor R_L used with either of these circuits is normally less than 100 ohms because the measurements of y_f and h_f both are based on a short circuit in the output. The allowable resistance that may be used in the collector circuit is limited by the source impedance of the power supply and by the two output admittances. The value of R_L should lie in the range

$$R_{cc} \ll R_L \ll 1/y_c \text{ or } 1/y_o$$

where R_{cc} is the effective source impedance of the collector power supply, including any metering circuits used. This resistance must also be sufficiently small to permit the development of the required value of collector voltage.

3-9 HIGH-FREQUENCY PARAMETERS

In addition to the measurements of the low-frequency components of the small-signal parameters, it is necessary to measure at least three additional parameters, for example, r_b , C_i and C_c . These are the minimum components required in the interpretation of the

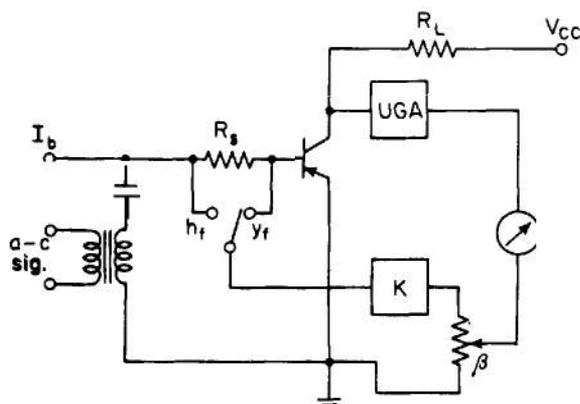


Fig. 3-6. Transfer Immittance Bridge

characteristics of any given device. Several methods for the measurement of these parameters are now considered.

First, a brief consideration of the properties to be expected in the device as a result of typical values of these parameters can be helpful because it indicates the type of data required for them. The value of the parameter r_b varies slowly with frequency, and is relatively independent of base current. It may vary somewhat with collector voltage because the collector voltage determines the current distribution in the base region.

3-9.1 CAPACITANCES

The internal base-to-emitter capacitance of a transistor consists of two components, one dependent primarily on the magnitude of the collector voltage, and the other on the magnitude of the emitter current. As a consequence, the input capacitance variation can best be presented in terms of contours of constant value plotted on either the input or the output curve family. Because the collector current is nearly equal to the emitter current for the majority of useful transistor devices, the contours may be introduced on the output family of curves. Fig. 3-7 shows how such curves might look on a hypothetical transistor.

The capacitance between the collector and the base of a transistor, or the feedback capacitance, is also a function of its operating conditions. The principal component of capacitance varies with the voltage from collector to base, having the form

$$C = kV_{cb}^{-n} \tag{3-50}$$

where the value of n is either 0.5 or 0.33.

3-9.2 METHODS OF MEASUREMENT OF INPUT PARAMETERS

The methods used for measuring the values of r_b , C_i and g_i all separate the different components on the basis of measurements at different frequencies. One quick method of getting a rough value of r_b and C is based on the method described for measurement of g_i . First a measurement of g_i may be made, only a special potentiometer is used as the standard instead of a simple standard resistor. Once a sine-wave balance has been obtained at measuring frequency with the full resistance in the potentiometer used as the standard, a capacitance decade box, C_s , may be introduced, changing the circuit of R_i in Fig. 3-5(A) to that shown in Fig.

3-8. First, the approximate value of C_i required may be calculated from the equation

$$C_s = C_i / (g_{i'} R_s) \tag{3-51}$$

$$= (g_{i'} + g_{f'}) / (2\pi f_{\alpha} g_{i'} R_s) \tag{3-51}$$

The nominal value of the sum of $(g_{i'} + g_{f'})$ may be obtained (for this equation) from the emitter current if desired. The capacitor C_i is set to the value indicated by Eq. 3-51, and the potentiometer adjusted with a square-wave input until the Lissajous figure is flattened to a horizontal line. Once the setting of the potentiometer has been optimized, then the capacitance may be readjusted and R_s trimmed until neither direct nor quadrature components of current remain. When this condition exists, the component values may be determined in terms of γ , the decimal reading R_s on the standard potentiometer, and the total gain βK applied

to the signal voltage developed across the transistor input. The parameter values are

$$g_{i'} = \beta K / (\gamma R_s) \tag{3-52}$$

$$r_{b'} = (1 - \gamma) R_s / (\beta K) \tag{3-53}$$

$$C_i = (\beta K) C_s \tag{3-54}$$

A possible circuit for the complete standard including R_s and C_i is shown in Fig. 3-8.

Two methods of estimating $r_{b'}$ are available which are based on low-frequency data. The first of these is based on the fact that, at least approximately, the input admittance of the transistor, neglecting base-spreading resistance, is linear with emitter or base current. The input resistance of the device is

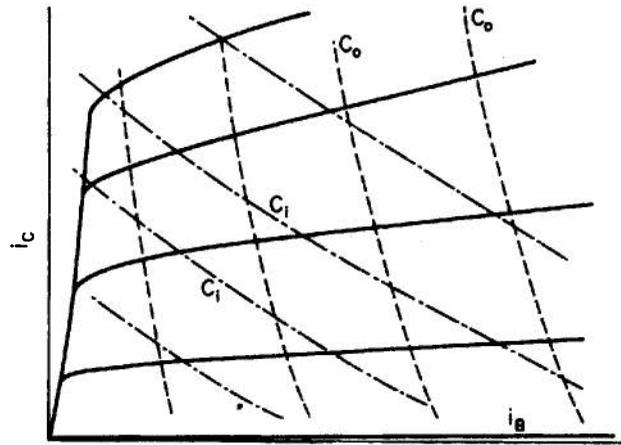


Fig. 3-7. Contours of C_i (---) and C_o (—) As a Function of Operating Conditions

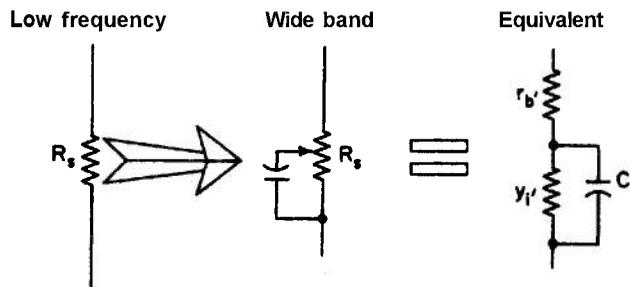


Fig. 3-8. Standard Admittance Representation for Transistor Input

$$1/g_i = r_b + 1/g_i \quad \text{or} \quad g_i = g_i/(1 + g_i r_b) \quad (3-55)$$

Solving for the internal conductance in terms of the external gives the equation

$$g_i = g_i/(1 - g_i r_b) \quad (3-56)$$

As long as the operating conditions are such that the value of $(g_i r_b)$ is less than 0.5, then g_i may be written in the form

$$g_i = g_i \Delta i_B \quad (3-57)$$

When Eq. 3-55 is solved for r_b in terms of two different values of base current, i_{B1} and i_{B2} , the resulting equation is

$$r_b = (i_{B1}/g_{i1} \Delta i_b) - (i_{B2}/g_{i2} \Delta i_b) \quad (3-58)$$

where

$$\Delta i_b = i_{B1} - i_{B2}$$

The presence of r_b does not affect the determination of the internal value of current gain, but it does affect the determination of the values of the input and forward admittances. The effect of r_b on circuit behavior is sufficiently important that the sensitivity of g_i and g_f to the value of r_b may help rather than hinder circuit behavior. The corrected values of g_i and g_f , namely, g_i and g_f , are given in Eqs. 3-56 and 3-59

$$r_b = 2/g_{i1} - 1/g_{i2} \quad (3-58a)$$

The estimate of the value of r_b obtained from Eq. 3-58 will be correct to within at most a factor of two. The resulting value of r_b may be used in Eq. 3-59 for the determination of g_f . It is usually convenient to take the value of i_{B1} twice that for i_{B2} , in which case the value of r_b is given in terms of the modified form of Eq. 3-58

$$g_f = g_f/(1 - g_f r_b) \quad (3-59)$$

The collector voltage should be kept constant for this measurement.

There is an additional method of determining the approximate value of the base-spreading resistance that depends on low-frequency measurements exclusively. This method is based on the fact that the reduction in the value of g_f from g_f , 39,000 micromhos per mA, is due primarily to base-spreading resistance. As a consequence, the values of g_i and g_f may be measured for a specified value of emitter current, and g_f may be determined by multiplying 39,000 by the emitter current in milliamperes. The value of r_b is

$$r_b = (1 - g_f/g_f)/g_i \quad (3-60)$$

The point at which the evaluation is made may be selected in the region where g_f is approximately half of the nominal value g_f to minimize the calculating and the measuring errors.

True high-frequency measurements of the base-spreading resistance for a transistor are readily made with most high-frequency admittance bridges. The first step is the selection of a test frequency sufficiently high that the reactance of the input capacitance C_i is small compared to r_b . Next, a lower frequency may be selected, and both r_b and C_i may be measured in terms of series components, the initial value of r_b being used to guide the measurements. After the value of r_b has been subtracted from $1/g_i$ to give $1/g_i$, the approximate equivalent circuit is complete. The only problems that may be encountered in this procedure are the problems of controlling the static operating point of the active device without influencing the readings. A number of bridges have been developed that include provision for the introduction of the required bias conditions. Among these are the General Radio "Transadmittance" meter, and the Wayne-Kerr bridges. Other bridges that are naturally suited to these measurements are described in the papers by Zawels (Ref. 3), Molozzi, Page, and Boothroyd (Ref. 4), and by Turner (Ref. 5). Zawels' bridge is typical of the special devices created for these measurements, and is discussed in the next paragraph.

Fig. 3-9 shows a method of introducing an input test signal into a transistor for measuring r_b , g_i , and C_i

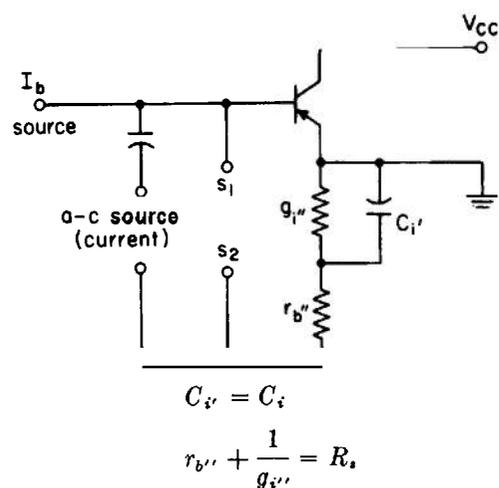


Fig. 3-9. Bridge for Wide-band Input Admittance Measurement (AC source is square-wave current isolated with respect to ground.)

either in one operation with the use of a square wave, or by making separate balances at several frequencies separated by two to three decades from one another. The establishment of balance in a circuit such as this is organized in steps in the order that permits them to be accomplished independently of one another. The most convenient order to use with this bridge is to make the r_b' balance first, adjusting the value of the R_s standard at a very high frequency. Then a low-frequency balance may be made to adjust the G_i' standard to the proper value. This adjustment is followed by one C_i at an intermediate frequency. A Lissajous-balance test should now show a relatively good balance as a function of frequency from audio frequencies to a frequency in excess of the upper noise-corner frequency f_{n2} . If the test signal is large, curvature in the form of a parabolic balance condition will be noted, but it will be symmetrical about the vertical axis if the bridge is properly balanced.

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CHAPTER 4

CIRCUIT PARAMETER RELATIONS

4-0 INTRODUCTION

The basic operating equations for transistor amplifiers may be determined in terms of either an equivalent black-box configuration and relation, a modified black-box relation, or on the basis of an arbitrary equivalent circuit, such as the Bell Laboratories tee resistance circuit, or the RCA pi circuit.

The principal advantage in the use of a black-box representation in the derivation of equations for an active circuit is that the equations obtained do not depend on the configuration used for the active device. The conversion of the small-signal parameters among the different configurations may be complicated, but the equations need not be changed because of a change of ground-point. The equations for the three standard forms of amplifiers, the common-emitter, the common-base, and the common-collector, and the equations for the degenerative-emitter amplifier are derived in this chapter, both neglecting the base-spreading resistance as a separate component, and also including it. In all these derivations, the internal properties of the intrinsic transistor are represented by the modified admittance parameters discussed in Chapter 2.

In addition to the routine method of derivation based on Kirchhoffs Laws, topological methods are helpful. The topological method gives the small-signal equations for both the driving-point and the transfer relation with a minimum of waste motion, and also minimizes the possibility of error in the derivation. The procedure for derivation of equations topologically is explained in Appendix B. Topological methods have been used extensively in the establishment of circuit equations in later chapters of this book.

4-1 BASIC EQUATIONS FOR SIMPLE AMPLIFIERS

The amplification equation for the common-emitter amplifier, Fig. 4-1, can be derived directly from the basic current equations, Eq. 2-3 and the input and the output relations

$$i_b = y_i v_b + y_r v_c \tag{4-1a}$$

$$i_c = y_f v_b + y_o v_c \tag{4-1b}$$

$$v_s = i_b R_s + v_b \tag{4-1c}$$

$$v_c + i_c R_L = 0 \tag{4-1d}$$

Substituting for v_b and v_c gives the equations

$$i_b(1 + y_i R_s) = y_f v_s - y_o R_L i_c \tag{4-2a}$$

$$i_b y_f R_s + i_c(1 + y_o R_L) = y_f v_s \tag{4-2b}$$

These equations may be solved for i_b and i_c in terms of v_s to give the driving-point and the transfer admittances. The resulting admittance equations provide the relations between the currents and the input voltage in convenient form. The value of i_b/v_s is

$$Y_{is} = i_b/v_s = [y_i + \Delta(y)R_L]/[1 + y_i R_s + y_o R_L + \Delta(y)R_s R_L] \tag{4-3}$$

or, in terms of the value at the transistor terminals, (for $R_s = 0$), the equation is

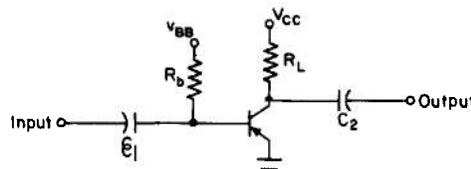


Fig. 4-1. Common-emitter Amplifier

$$Y_i = i_b/v_b \quad (4-4)$$

$$= [y_i + \Delta(y)R_L]/[1 + y_oR_L]$$

The first of these equations gives the input admittance with the source resistance R_s , included as part of the transistor, and the second, with it isolated from the transistor.

The input-output relation may be calculated by solving Eq. 4-2 for the collector current in terms of input voltage

$$Y_f = i_c/v_i \quad (4-5)$$

$$= y_f/[1 + y_iR_s + y_oR_L + \Delta(y)R_sR_L]$$

This equation gives the forward admittance, or the output current for a given input voltage, for the overall circuit. In this case there is no reason to determine the gain from the input terminals of the transistor to its output, because the overall circuit gain is the value desired. This equation may be changed into a voltage-gain equation or a current-gain equation by a simple transformation, multiplying both sides of the equation by $(-R_L)$ for the voltage amplification, and by R_s for the current amplification. For the derivation of the current gain equation from fundamental relations, the input relation, Eq. 4-1c, is replaced by the equation

$$i_s = v_b + G_s v_b \quad (4-1c')$$

where G_s and R_s are reciprocals of one another.

In all these equations, the only place in which the reverse admittance appears is in the A factor

$$\Delta(y) = y_i y_o - y_f y_r \quad (4-6)$$

Because the evaluations in Chapter 2 show the use of the y_r parameter in one other form of term, the $\sigma(y)$ term, and the value of y_r in the common-emitter configuration is negligible compared to the balance of the terms, the use of y_i , y_f , y_o , and $\Delta(y)$ simplifies the design of circuits significantly. At least potentially, the value of $\Delta(y)$ is formed from the difference of two products, and the values of the two products can be

approximately equal. For this reason its value should be measured directly. Since there appears to be no method of measuring the factor as a whole directly, it has been determined by the use of the artifice

$$\Delta(y) = y_i(y_o - y_f y_r / y_i) = y_i y_o \quad (4-6a)$$

where y_o is the output admittance with the input circuit showing high-impedance to signal currents. It is readily measured, and as a result, the question of subtraction is avoided completely. In the balance of this book, the A factor is written as $y_i y_o$ instead of $\Delta(y)$. This factor is one of the invariants in an admittance configuration for an active device.

The amplification equation could have been derived without mentioning which variables were voltages and which currents, and what type of immittance parameters were used. This can be verified by comparing the equations for voltage gain in terms of hybrid parameters and admittance parameters

$$K = -y_f R_L / [1 + y_i R_s + y_o R_L + \Delta(y) R_s R_L] \quad (4-7)$$

$$K = h_f G_s R_L / [1 + h_i G_s + h_o R_L + \Delta(h) G_s R_L] \quad (4-8)$$

Clearly, in converting Eq. 4-7 into Eq. 4-8, y_f has been replaced by $h_f G_s$, y_i has been replaced by h_i , y_o by h_o , $\Delta(y)$ by $\Delta(h)$, and R_s by G_s . In other words, to get Eq. 4-8, both the numerator and the denominator of Eq. 4-7 may be divided by $y_i R_s$, and the balance of the manipulations consist of substitution of the respective H-parameter symbols for the y -symbols. As long as the parameters used are based on the same transistor configuration, this interchange can be used for common-base and common-collector amplifiers as well as the common-emitter circuit. The formulation of the respective terms can be performed dimensionally if desired, because both the numerator and the denominator of a gain equation must be dimensionless.*

*Linville has also reported the implications of this paragraph in his report *The Theory of Two-Ports*, J. G. Linville, Stanford University Electronic Research Labs Technical Report TR1505-2 (October 15, 1959).

When the equation for current gain is transformed into the H-parameter form, the product of G_s and R_s is unity, leaving only h_f in the numerator and

$$[1 + h_i G_s + h_o R_L + \Delta(h) G_s R_L]$$

in the denominator. If, therefore, the value of G_s is small (current drive), then the amplification, with R_L relatively small, reduces to h_f , the transistor current gain.

Although the derivation of these equations was based on the equations for the base current and the collector current, it could equally well have been based on emitter and collector currents (common-base), or on base and emitter currents (common-collector). In each of these cases, the input signal may either be introduced in series by the use of a voltage and a series impedance, or in parallel with a current and a shunt admittance. Either way, the output is developed in a load impedance. This is the reason for the importance of Table 2-3. For these two configurations, the amplification equations take the following forms. . .

Common base:

$$K = [y_f + y_o] R_L / [1 + \sigma(y) R_s + y_o R_L + y_i y_c R_s R_L] \quad (4-9)$$

Common collector:

$$K = [y_i + y_j] R_L / [1 + y_i R_s + \sigma(y) R_L + y_i y_c R_s R_L] \quad (4-10)$$

The first of these equations, Eq. 4-9, may be verified by using the sum of Eqs. 4-1a and 4-1b with Eq. 4-1b and the additional equations

$$\begin{aligned} v_s &= i_e R_s + v_e; & v_c + i_c R_L &= 0; \\ i_e + i_b + i_c &= 0 \end{aligned} \quad (4-11)$$

and Eq. 4-10 may be verified by the use of Eq. 4-1a with the sum of Eqs. 4-1a and 4-1b along with the additional equations

$$\begin{aligned} v_s &= i_b R_s + v_b + i_e R_L; & v_c + i_c R_L &= 0 \\ i_e + i_b + i_c &= 0 \end{aligned} \quad (4-12)$$

The input admittances may also be calculated by solving for the input current in terms of either the source or the terminal voltage. For the common-base amplifier, the input admittance in the emitter circuit takes the two forms

$$Y_{i_{b_s}} = [\sigma(y) + y_i y_c R_L] / [1 + \sigma(y) R_s + y_o R_L + y_i y_c R_s R_L] \quad (4-13)$$

$$Y_{i_b} = [\sigma(y) + y_i y_c R_L] / [1 + y_o R_L] \quad (4-14)$$

for the source admittance and the terminal admittance, respectively. Eqs. 4-13 and 4-14 can be formed by substitution of the appropriate conversion values from Table 2-3 in Eqs. 4-3 and 4-4, respectively.

The corresponding equations for the common-collector amplifier may be derived either by substitution from Table 2-3 or by solution of the basic equations. The input admittances for this amplifier are

$$Y_{i_{c_s}} = y_i (1 + y_c R_L) / [1 + y_i R_s + \sigma(y) R_L + y_i y_c R_s R_L] \quad (4-15)$$

$$Y_{i_c} = y_i (1 + y_c R_L) / [1 + \sigma(y) R_L] \quad (4-16)$$

for the two conditions.

With the common-collector amplifier, the output signal is applied effectively in the input circuit, reducing the net signal voltage applied from base to emitter. This is the reason that the σ term appears in the denominator of these expressions and the gain expression for this configuration. The effective input admittance is markedly reduced by the effect of the load resistance, and the converse is shown to be true in the next paragraph.

The output admittances may be determined from the basic current relations by transformation of input for output parameters and vice versa, or they may be determined by evaluating the ratio of current to voltage in the output circuit. The equations to be solved are

$$i_b = y_i v_b + y_r v_c \quad (4-1a)$$

$$i_c = y_f v_b + y_o v_c \quad (4-1b)$$

$$v_o + i_b R_s = 0 \tag{4-17}$$

The value of the ratio i_c/v_c or Y_o , is given by the equation

$$Y_o = [y_o + y_i y_c R_s] / [1 + y_i R_s] \tag{4-18}$$

Once again, this equation may be transformed from that for the common-emitter configuration to that for the two other standard configurations. The modified admittance equation for common-base operation is

$$Y_o = [y_o + y_i y_c R_s] / [1 + \sigma(y) R_s] \tag{4-19}$$

Clearly, the output admittance of this amplifier is much smaller than that for the common-emitter configuration. In fact, as the source resistance R_s is increased, the output admittance decreases rapidly, but for very small values of R_s , the output admittance is independent of which of these configurations is used.

The output admittance for the common-collector configuration may also be written with the aid of the conversion table. Instead of the $\sigma(y)$ appearing in the denominator, however, in this case it appears in the numerator. Consequently, the output admittance is comparatively large

$$Y_o = [\sigma(y) + y_i y_c R_s] / [1 + y_i R_s] \tag{4-20}$$

This high output admittance corresponds to the relatively high value of output conductance that may be obtained with the conventional cathode follower. Because the first term of the numerator is very large compared to the second, the value of R_s used can have little if any effect on the magnitude of the numerator. It can, however, have an appreciable effect on the value of the denominator. Consequently, as the source impedance of the signal source is increased for an emitter follower, an appreciable increase of the value of the denominator can cause a significant reduction of the available output admittance, and the circuit may not behave as desired. This phenomenon is also noted with cathode followers, in that the output admittance of a circuit incorporating impedance-boost on the input side often has a relatively low output admittance. The

difficulty is commonly avoided by the use of a circuit similar to that shown in Fig. 4-2.

4-2 MODIFIED BLACK-BOX PARAMETERS

It is not possible to simplify the representation of a transistor to an admittance black-box except at low frequencies, since the base-spreading resistance present in the base lead of the transistor prevents the frequency response from conforming with that of the admittance form. It is entirely practical, however, to modify the admittance representation by the introduction of a series resistance in the base lead to make allowance for the discrepancy, and the resulting representation is sufficiently accurate for the majority of routine applications. This modification may be made directly in the equations for the common-emitter and the common-collector amplifiers, and the corrected small-signal equations are easily derived, but special consideration is required for the common-base configuration (Figs. 4-3, 4-4, 4-5).*

The modification of the equations for the common-emitter circuit to take account of base-spreading resistance requires the addition of the equivalent resistance r'_b to the source resistance of the voltage source supplying the signal to the transistor. At the same time, the input admittance for the transistor amplifier must be

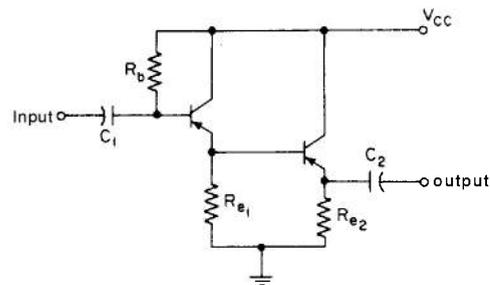


Fig. 4-2. Amplifier Coupling Using Emitter-followers

*Strictly r'_c and r'_e also should be included for a complete representation.

determined, including the base-spreading resistance internal to the transistor. The modified amplification for this amplifier may be written

$$K = -y_f R_L / [1 + y_i (R_s + r_{b'}) + y_o R_L + y_i y_c (R_s + r_{b'}) R_L] \quad (4-21)$$

In effect, the original source resistance becomes the sum of two parts, the first being due to the resistance of the voltage source, and the second due to base-spreading resistance. Similarly, the input admittance becomes, for the two cases

$$Y_{i\epsilon} = i_b / v_s = [y_i' + y_i y_c R_L] / [1 + y_i (R_s + r_{b'}) + y_o R_L + y_i y_c (R_s + r_{b'}) R_L] \quad (4-22)$$

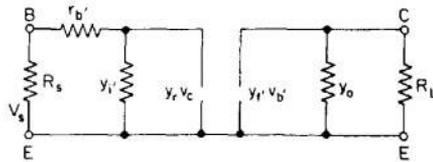


Fig. 4-3. Circuit Representation—Common-emitter Transistor Amplifier

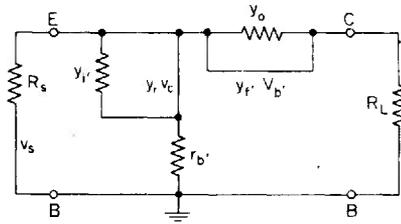


Fig. 4-4. Common-base Amplifier

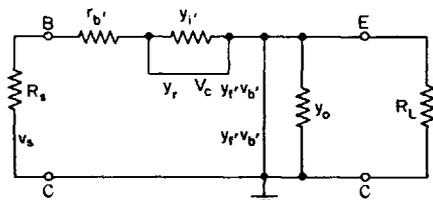


Fig. 4-5. Common-collector Amplifier

$$Y_i = y_i (1 + y_c R_L) / [1 + y_i r_{b'} + y_o R_L + y_i y_c r_{b'} R_L] \quad (4-23)$$

The corresponding equation for the output admittance is

$$Y_o = [y_o + y_i y_c (R_s + r_{b'})] / [1 + y_i (R_s + r_{b'})] \quad (4-24)$$

If $R_s = 0$, then this equation may be written as

$$Y_o = (y_o + y_i y_c r_{b'}) / (1 + y_i r_{b'})$$

A similar set of equations may be derived for the common-base configuration. One significant difference must be taken into account in this configuration, namely, the fact that the base-spreading resistance is introduced into the grounded, or base, lead rather than in either the emitter (input) or the collector (output) circuit. In effect, it lifts the internal common element of the transistor off ground and makes it part of the series circuit. This introduces a $y_i y_c$ term into the numerator of the amplification equation

$$K = (y_f + y_o + y_i y_c r_{b'}) R_L / [1 + \sigma(y') R_s + y_i r_{b'} + y_o R_L + y_i y_c (r_{b'} R_s + r_{b'} R_L + R_s R_L)] \quad (4-25)$$

The complete equation for the input admittance is

$$Y_{i\epsilon} = [\sigma(y') + y_i y_c (r_{b'} + R_L)] / [1 + \sigma(y') R_s + y_i r_{b'} + y_o R_L + y_i y_c (r_{b'} R_s + r_{b'} R_L + R_s R_L)] \quad (4-26)$$

This equation may be reduced to the actual input admittance of the transistor by taking R_s to be zero

$$Y_i = [\sigma(y') + y_i y_c (r_{b'} + R_L)] / [1 + y_i r_{b'} + y_o R_L + y_i y_c r_{b'} R_L] \quad (4-27)$$

The equation for the output admittance, including $r_{b'}$, is

$$Y_o = [y_o + y_i y_c (R_s + r_{b'})] / [1 + \sigma(y') R_s + y_i r_{b'} (1 + y_c R_s)] \quad (4-28)$$

Unless topological methods are used for the derivation of this equation, difficulties may arise in the establishment of the correct set of current and voltage relations to use with the basic black-box equations. The following tabulation of the basic relations required in the derivation is included for the convenience of the reader

$$\begin{aligned}
 i_b + i_c + i_e &= 0, \quad v_b' + v_e' = 0 \\
 i_e &= (y_{i'} + y_{f'})v_e' - (y_r + y_{o'})v_c' - v_e' \\
 i_c &= -y_{f'}v_e' + y_{o'}(v_c' - v_e') \\
 v_c' &= -i_c R_L + i_b r_b' \\
 v_s &= v_e' + i_e R_s - i_b r_b' = v_e + i_e R_s \\
 v_c'' + i_c R_L &= 0, \\
 v_c' &= v_c'' + i_b r_b' = [v_c'' - i_c r_b' - i_e r_b']
 \end{aligned}
 \tag{4-29}$$

The equations for determination of amplification and the input admittance take the form

$$\begin{aligned}
 i_e[1 + \sigma(y')R_s + (y_{i'} + y_{f'})r_b'] \\
 - i_c[-(y_{i'} + y_{f'})r_b' \\
 + (y_r + y_{o'})R_L] = \sigma(y')v_s \\
 - i_e(y_{f'} + y_{o'})(R_s + r_b') \\
 + i_c[1 + y_{o'}R_L - y_{f'}r_b'] = -(y_{f'} + y_{o'})v_s
 \end{aligned}
 \tag{4-30}$$

These equations may be used for the calculation of K_b' , Y_{ib_s} , and Y_{ib} , but they cannot be used for the determination of Y_{ob} . This must be determined from a pair of equations in which the value of v_c' has not been replaced by $-i_c R_L + i_b r_b'$. These equations are

$$\begin{aligned}
 i_e[1 + \sigma(y)R_s + (y_{i'} + y_{f'})r_b'] \\
 + i_c(y_{i'} + y_{f'})r_b' &= (y_r + y_{o'})v_c'' \\
 i_e[(y_{f'} + y_{o'})R_s + y_{f'}r_b'] + i_c(1 - y_{f'}r_b') &= y_{o'}v_s
 \end{aligned}
 \tag{4-31}$$

Routine solution of these equations leads to the value of output admittance given in Eq. 4-28.

Because the input circuit is the base circuit, as it is in the common-emitter amplifier, the equations for the common-collector amplifier can be obtained directly by replacing R_s by the sum of R_s and r_b' . The resulting equations are

$$\begin{aligned}
 K_C &= (y_{i'} + y_{f'})R_L/[1 + \sigma(y')R_e \\
 &+ y_{i'}(1 + y_c R_e)(r_b' + R_s)]
 \end{aligned}
 \tag{4-32}$$

$$\begin{aligned}
 Y_{ic_s} &= y_{i'}(1 + y_c R_e)/[1 + \sigma(y')R_e \\
 &+ y_{i'}(1 + y_c R_e)(r_b' + R_s)]
 \end{aligned}
 \tag{4-33}$$

$$\begin{aligned}
 Y_{ic} &= y_{i'}(1 + y_c R_e)/[1 + \sigma(y')R_e \\
 &+ y_{i'}r_b'(1 + y_c R_e)]
 \end{aligned}
 \tag{4-33a}$$

$$\begin{aligned}
 Y_{oc} &= [\sigma(y') + y_{i'}y_c(r_b' + R_s)]/[1 \\
 &+ y_{i'}(r_b' + R_s)]
 \end{aligned}
 \tag{4-34}$$

4-3 THE DEGENERATIVE AMPLIFIER

Often in an amplifier some resistance is introduced into the emitter circuit, Fig. 4-6, to provide the kind of degeneration commonly obtained by the use of a cathode resistor in a tube circuit. The modifications this makes in the equations are not extensive, but they do introduce significant changes into the circuit behavior. The set of equations required for this derivation are

$$\begin{aligned}
 i_b &= y_{i'}v_b' + y_r v_c \\
 i_c &= y_{f'}v_b' + y_{o'}v_c
 \end{aligned}
 \tag{4-35}$$

$$\begin{aligned}
 v_s &= v_b + (i_b + i_c)R_e + i_b R_s = v_b' \\
 &+ (i_b + i_c)R_e + i_b(R_s + r_b') \\
 v_c + i_c R_L + (i_b + i_c)R_e &= 0
 \end{aligned}
 \tag{4-36}$$

When these equations are solved for the voltage amplification, the resulting equation is

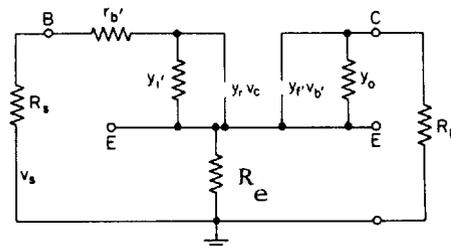


Fig. 4-6. Emitter Degenerative Amplifier

$$K_d = -[(y_f' - y_i' y_c R_e) R_L] / [1 + \sigma(y') R_e + y_i' (R_s + r_{b'}) + y_o R_L + y_i' y_c \langle R_e R_L + (R_s + r_{b'}) (R_e + R_L) \rangle] \quad (4-37)$$

If the value of R_e is zero, this equation reduces to the standard form for the common-emitter amplifier. With the resistance R_e in the emitter return, the emitter is no longer at ground potential, and a $y_i' y_c$ term is present in the numerator of the transfer equation.

These equations may also be solved for the driving-point admittances for the circuit, both with and without a source-resistance component in the input. The input admittance equations are

$$Y_{ids} = y_i' [1 + y_c (R_e + R_L)] / [1 + \sigma(y') R_e + y_i' (R_s + r_{b'}) + y_o R_L + y_i' y_c \langle R_e R_L + (R_s + r_{b'}) (R_e + R_L) \rangle] \quad (4-38)$$

$$Y_{id} = y_i' [1 + y_c (R_e + R_L)] / [1 + \sigma(y') R_e + y_i' r_{b'} + y_o R_L + y_i' y_c \langle R_e R_L + r_{b'} (R_e + R_L) \rangle] \quad (4-39)$$

The presence of the emitter resistance R_e increases the complexity of the equations considerably, even more than does the presence of the base-spreading resistance $r_{b'}$. The usual simplifications do reduce the complexity of the equations, however.

The output admittance is calculated in the same manner as it has been in previous examples. As usual, no substitution is made for v_c , only one for v_b . The equation that results is

$$Y_{od} = [y_o + y_i' y_c (R_s + R_e + r_{b'})] / [1 + \sigma(y') R_e + y_i' (R_s + R_e + r_{b'}) + y_o R_L + y_i' y_c \langle R_e R_L + (R_s + r_{b'}) (R_e + R_L) \rangle] \quad (4-40)$$

It is significant to note that both, the input and the output admittances of the amplifier can be reduced appreciably by the introduction of the emitter resistance, as the σ term in the denominators of Y_{ids} and Y_{id} normally is large compared to the balance of the

denominator terms, and the $\sigma(y') R_e$ term in the denominator of Y_{od} likewise is large compared to the remaining terms.

The effect of the introduction of emitter resistance on the input and the output admittances of the amplifier are best shown by taking the ratio of the admittances with and without R_e present. This ratio is

$$Y_i / Y_{id} = \{1 + [\sigma(y') + y_i' y_c R_L] R_e\} / [1 + y_i' r_{b'} + y_o R_L + y_i' y_c r_{b'} R_L] \quad (4-41)$$

Consequently, the value of Y_i may be many times that of Y_{id} . In a similar manner, the ratio of the output admittances may be calculated to determine the effect of the emitter degeneration. This ratio is

$$Y_o / Y_{od} = [1 + \langle (y_i' + y_f') R_e / [1 + y_i' (R_s + r_{b'}) + y_i' y_c \langle R_e / [1 + \langle (y_i' y_c R_e / [y_o + y_i' y_c \langle R_s + r_{b'} \rangle] \rangle] \rangle] \rangle] \quad (4-42)$$

The second bracket of this expression has the value

$$0.5 \leq [1 / \langle 1 + (y_i' y_c R_e / [y_o + y_i' y_c (R_s + r_{b'})] \rangle] \leq 1.0 \quad (4-43)$$

Consequently, the value of the ratio lies in the range

$$0.5 \left[1 + \frac{(y_i' + y_f') R_e}{1 + y_i' (R_s + r_{b'})} \right] \leq Y_o / Y_{od} \leq \left[1 + \frac{(y_i' + y_f') R_e}{1 + y_i' (R_s + r_{b'})} \right] \quad (4-44)$$

The term in brackets can have a value that is large compared to unity, so that the output admittance is strongly affected by emitter degeneration, just as is the input admittance.

4-4 SYMBOL TABLES AND DEFINITIONS

One remaining preliminary of considerable importance to the designer and the user of this book is a listing of the special symbols used for identification of different typical operating conditions. A complete table of definitions used in this book is included in the List of Symbols, and only the most important symbols and parameters, along with their definitions, are considered in this chapter.

The identification of the different current, voltage, and admittance values for typical operating conditions with transistors should be sufficiently complete to enable the user to identify his different conditions of operation easily and consistently, so that all other users will know the significance of his symbols. For this reason, it has not been possible to delay selection of terminology until the standardizing committees both recognize a need, and also recognize that something must be made available for the user.

The behavior of a nonlinear circuit may be expressed in terms of voltage differences, or it may be expressed in terms of the small-signal characteristics of the circuit as a function of operating conditions. The usual method of doing this has been in terms of voltage differences. This method is satisfactory as long as the accuracy requirements are comparatively small and the design criteria are sufficiently flexible to permit ample dissipation margins. Unfortunately, the development of compact, light-weight, low-power equipment is not readily possible when voltage-difference methods are used, because it is not possible to tell in sufficient detail what the characteristics of the circuit are. For similar reasons, it is desirable that the values of the small-signal data be identified at several different points if the design is to take into account the range of variation to be expected in the active devices. A detailed study of the methods of evaluating distortion in amplifiers is given in condensed form in *Radio Engineering Handbook* (Ref. 1). For that reason, only the results are included here. One derivation that seems to offer difficulties to many is worked out in Appendix A. The amplitudes of other harmonic components may be determined in a

similar manner. The equations that apply when the second harmonic distortion predominates, and when the third predominates, are

$$D = 25(K_p - K_n)/(K_p + K_n) \text{ percent} \quad (4-45)$$

$$D = 100(K_p + K_n - 2K_s)/3(K_p + K_n + 6K_s) \text{ percent} \quad (4-46)$$

Orthogonal polynomial techniques are the best to use when the variation of amplification with bias is not uniform, because they make possible both the determination of the magnitudes of the harmonic components, and the direct evaluation of the significance of the irregularities that may be noted. The use of this technique is described in Appendix C.

The standard voltage, current, and impedance symbols used with transistors include instantaneous total values, the DC value, the instantaneous value, the maximum value of the varying component, and the supply values. In addition, most-positive values, most-negative values, cutoff values, average values, and total changes are included in Tables 4-1 through 4-4 because these values are of considerable importance to the design procedures that follow. The tables are separated into three groups, one for voltage symbols, one for current symbols, and the third for admittance symbols. The fourth includes the conductance symbols that may be used at low frequency.

In the admittance and conductance tables, the primes have been omitted. If the base-spreading resistance is separated from the transistor, leaving an intrinsic internal device, then y_i symbols and y_f symbols should be primed. It may in some cases be necessary to prime the y_o symbol, because the base-spreading resistance affects the impedance of the base to ground, but the y_c parameter need not be primed under any conditions.

In addition, the symbol definitions in Table 4-5 are of considerable importance in the chapters to follow.

Table 4-6 tabulates the various important admittance equations derived in this chapter and three important equations from Chapter 5. These equations have been grouped in this form to facilitate their application to design problems.

TABLE 4-1
TRANSISTOR VOLTAGE SYMBOLS (Emitter Reference)

<i>Conditions</i>	<i>Base</i>	<i>Collector</i>	<i>Emitter</i>	<i>Input</i>	<i>Output</i>
Instantaneous total	v_B	v_C	v_E	v_S	v_O
d-c (no-signal)	V_B	V_C	V_E	V_S	V_O
Instant. signal component	v_b	v_c	v_e	v_s	v_o
Max. value of varying component	V_{BM}	V_{CM}	V_{EM}	V_{SM}	V_{OM}
Peak positive bias	V_{bp}	V_{cp}	V_{ep}	V_{sp}	V_{op}
Peak negative bias	V_{bn}	V_{cn}	V_{en}	V_{sn}	V_{on}
Cutoff bias	V_{ba}	V_{ca}	V_{ea}	V_{sa}	V_{oa}
Average value	V_{ba}	V_{ca}	V_{ea}	V_{sa}	V_{oa}
Total change	Δv_b	Δv_c	Δv_e	Δv_s	Δv_o
Value for max. collector dissipation	V_{b_m}	V_{c_m}	V_{e_m}		
Supply voltage	V_{BB}	V_{CC}	V_{EE}	v_{SS}	V_{OO}

TABLE 4-2
TRANSISTOR CURRENT SYMBOLS

<i>Conditions</i>	<i>Emitter</i>	<i>Base</i>	<i>Collector</i>	<i>Input</i>	<i>Output</i>
Instantaneous total	i_E	i_B	i_C	i_S	i_O
d-c value, no-signal	I_E	I_B	I_C	I_S	I_O
Instantaneous signal component	i_e	i_b	i_c	i_s	i_o
Max. value of varying component	I_{EM}	I_{BM}	I_{CM}	I_{SM}	I_{OM}
Peak positive bias	I_{ep}	I_{bp}	I_{cp}	I_{sp}	I_{op}
Peak negative bias	I_{en}	I_{bn}	I_{cn}	I_{sn}	I_{on}
Cutoff bias	I_{ea}	I_{ba}	I_{ca}	I_{sa}	I_{oa}
Average value	I_{ea}	I_{ba}	I_{ca}	I_{sa}	I_{oa}
Total change	Δi_e		Δi_c	Δi_s	Δi_o
Max. collector dissipation	I_{em}	I_{bm}	I_{cm}	I_{sm}	I_{om}

TABLE 4-3
TRANSISTOR ADMITTANCE SYMBOLS" (Common Emitter)

<i>Conditions</i>	<i>Input</i>	<i>Forward</i>	<i>Output Admittances</i>		<i>Amplification</i>
			<i>Short-Input-Open</i>		
Instantaneous	y_i	y_f	Y_0	y_o	K
Static value	y_{i_s}	y_{f_s}	Y_{o_s}	y_{o_s}	K_s
Peak positive bias	y_{ip}	y_{fp}	Y_{op}	y_{op}	K_p
Peak negative bias	y_{in}	y_{fn}	Y_{on}	y_{on}	K_n
Average value	y_{i_a}	y_{f_a}	Y_{o_a}	y_{o_a}	K_a
Total change	Δy_i	Δy_f	ΔY_o	Δy_o	ΔK
Conversion	$0.25\Delta y_i$	$0.25\Delta y_f$	$0.25\Delta Y_o$	$0.25\Delta y_o$	$0.25\Delta K$

**Short-Input-Open* means that the output admittances in the left column are taken with input short-circuited; those in the right column are taken with input open-circuited.

TABLE 4-4
TRANSISTOR CONDUCTANCE SYMBOLS* (Common Emitter)

<i>Conditions</i>	<i>Conductance</i>		<i>Output Conductance</i>		<i>Amplification</i>
	<i>Input</i>	<i>Forward</i>	<i>Short-Input-Open</i>		
Instantaneous	g_i	g_f	g_o	g_c	K
Static value	g_{i_s}	g_{f_s}	g_{o_s}	g_{c_s}	K_s
Peak positive bias	g_{i_p}	g_{f_p}	g_{o_p}	g_{c_p}	K_p
Peak negative bias	g_{i_n}	g_{f_n}	g_{o_n}	g_{c_n}	K_n
Average value	g_{i_a}	g_{f_a}	g_{o_a}	g_{c_a}	K_a
Total change	Δg_i	Δg_f	Δg_o	Δg_c	AK
Conversion value	$0.25\Delta g_i$	$0.25\Delta g_f$	$0.25\Delta g_o$	$0.25\Delta g_c$	$0.25\Delta K$

**Short-Input-Open* means that the output admittances in the left column are taken with input short-circuited; those in the right column are taken with input open-circuited.

TABLE 4-5
COMMONLY USED SYMBOLS

α_N	Current gain from emitter to collector
α_I	Current gain from collector to emitter
β	Current gain from base to collector
$h_{f_o} = h_f$	Current gain from base to collector.
f_α	Alpha cutoff frequency, the frequency for which the current gain, common-base, is 70 percent of the low-frequency value.
f_{n1}	Flicker-noise corner frequency
f_{n2}	Upper noise corner frequency
f_{max}	Maximum frequency at which a power gain \geq unity can be obtained with a transistor
f_T	Frequency for which $ h_f = \beta = 1$
$C_D \doteq C_i$	Input capacitance, base to emitter
r_b', r_{bb}'	Base-spreading resistance
C_C	Collector capacitance, base bypassed to ground
C_O	Collector capacitance, base not bypassed to ground
r_e'	Emitter series resistance (within the semiconductor)
r_c'	Collector series resistance
t_r	Time for current to rise from minimum to maximum nominal value in switching circuit
t_f	Time for current to fall from maximum magnitude to nominal minimum value in switching circuit
t_d	Ohmic delay time. Interval between the rise of the applied input pulse and the start of the rise of the output pulse generated by minority carriers.
t_s	Storage time. Time interval between the start of fall of the input pulse and the start of the decay of minority carrier flow at the output.

TABLE 4-6
IMMITTANCE EQUATIONS

Equations for Common-Emitter Amplifier

When $r_{b'}$ = 0:

$$Y_{i_s} = y_i(1 + y_c R_L) / [1 + y_o R_L + y_i R_s(1 + y_c R_L)] \quad 4-3r$$

$$Y_i = y_i(1 + y_c R_L) / (1 + y_o R_L) \quad 4-4r$$

$$Y_f = y_f / [1 + y_o R_L + y_i R_s(1 + y_c R_L)] \quad 4-5r$$

$$Y_o = (y_o + y_i y_c R_s) / (1 + y_i R_s) \quad 4-18$$

When $r_{b'} \neq 0$:

$$Y_{i_s} = y_i(1 + y_c R_L) / [1 + y_o R_L + y_i(1 + y_c R_L)(r_{b'} + R_s)] \quad 4-22$$

$$Y_i = y_i(1 + y_c R_L) / [1 + y_o R_L + y_i r_{b'}(1 + y_c R_L)] \quad 4-23$$

$$Y_f = y_f / [1 + y_o R_L + y_i(1 + y_c R_L)(r_{b'} + R_s)] \quad 4-21r$$

$$Y_o = [y_o + y_i y_c(r_{b'} + R_s)] / [1 + y_i(r_{b'} + R_s)] \quad 4-24$$

Equations for Common-base amplifier

When $r_{b'}$ = 0:

$$Y_{i_b} = (\sigma(y') + y_i y_c R_L) / [1 + y_o R_L + \sigma(y') R_s + y_i y_c R_s R_L] \quad 4-13$$

$$Y_{i_b} = (\sigma(y') + y_i y_c R_L) / (1 + y_o R_L) \quad 4-14$$

$$Y_{f_b} = (y_f + y_o) / [1 + y_o R_L + \sigma(y) R_s + y_i y_c R_s R_L] \quad 4-9r$$

$$Y_{o_b} = (y_o + y_i y_c R_s) / [1 + \sigma(y) R_s] \quad 4-19$$

When $r_{b'} \neq 0$:

$$Y_{i_b} = [\sigma(y') + y_i y_c(r_{b'} + R_L)] / [1 + y_o R_L + \sigma(y') R_s + y_i(r_{b'} + y_c(r_{b'} R_s + r_{b'} R_L + R_s R_L))] \quad 4-26$$

$$Y_{i_b} = [\sigma(y') + y_i y_c(r_{b'} + R_L)] / [1 + y_o R_L + y_i r_{b'}(1 + y_c R_L)] \quad 4-27$$

$$Y_{f_b} = (y_f + y_o + y_i y_c r_{b'}) / [1 + y_o R_L + \sigma(y') R_s + y_i(r_{b'} + y_c(r_{b'} R_s + r_{b'} R_L + R_s R_L))] \quad 4-24r$$

$$Y_{o_b} = [y_o + y_i y_c(r_{b'} + R_s)] / [1 + y_i r_{b'}(1 + y_c R_s) + \sigma(y') R_s] \quad 4-28$$

Common Collector Configuration (R_L replaced by R_s)

When $r_{b'}$ = 0:

$$Y_{i_{cc}} = y_i(1 + y_c R_s) / [1 + \sigma(y) R_s + y_i R_s(1 + y_c R_s)] \quad 4-15$$

$$Y_{i_{cc}} = y_i(1 + y_c R_s) / [1 + \sigma(y) R_s] \quad 4-16$$

$$Y_{f_{cc}} = (y_i + y_f) / [1 + \sigma(y) R_s + y_i R_s(1 + y_c R_s)] \quad 4-10r$$

$$Y_{o_{cc}} = [\sigma(y) + y_i y_c R_s] / [1 + y_i R_s] \quad 4-20$$

When $r_{b'} \neq 0$:

$$Y_{i_{cc}} = y_i(1 + y_c R_s) / [1 + \sigma(y') R_s + y_i(1 + y_c R_s)(r_{b'} + R_s)] \quad 4-33$$

$$Y_{i_{cc}} = y_i(1 + y_c R_s) / [1 + \sigma(y') R_s + y_i r_{b'}(1 + y_c R_s)] \quad 4-33a$$

$$Y_{f_{cc}} = (y_i + y_f) / [1 + \sigma(y') R_s + y_i(1 + y_c R_s)(r_{b'} + R_s)] \quad 4-32r$$

$$Y_{o_{cc}} = [\sigma(y') + y_i y_c(r_{b'} + R_s)] / [1 + y_i(r_{b'} + R_s)] \quad 4-34$$

Complete Emitter-Degenerative Amplifier

$$Y_{i_{de}} = y_i [1 + y_c(R_s + R_L)] / [1 + y_o R_L + \sigma(y') R_s + y_i(r_{b'} + R_s) + y_c(R_s R_L + (r_{b'} + R_s)(R_s + R_L))] \quad 4-38$$

$$Y_{i_{de}} = y_i [1 + y_c(R_s + R_L)] / [1 + y_o R_L + \sigma(y') R_s + y_i(r_{b'} + y_c(R_s R_L + r_{b'}(R_s + R_L)))] \quad 4-39$$

$$Y_{f_{de}} = [y_f - y_i y_c R_s] / [1 + y_o R_L + \sigma(y') R_s + y_i(r_{b'} + R_s) + y_c(R_s R_L + (r_{b'} + R_s)(R_s + R_L))] \quad 4-37r$$

$$Y_{o_{de}} = [y_o + y_i y_c(r_{b'} + R_s + R_L)] / [1 + \sigma(y') R_s + y_i(r_{b'} + R_s)(1 + y_c R_s)] \quad 4-40$$

Feedback Degenerative Amplifier

$$Y_{i_f} = [y_i(1 + Y r_{b'}) + y_i y_c R_L(1 + Y r_{b'}) + \sigma(y') Y R_L] / [1 + y_o R_L + y_i r_{b'}(1 + y_c R_L + Y R_L)] \quad 5-32$$

$$Y_{f_f} = [y_f + Y(1 - y_i r_{b'})] / [1 + Y R_s + y_o R_L + y_i(r_{b'} + R_s)(1 + y_c R_L + Y R_L) + \sigma(y') Y R_s R_L] \quad 5-31r$$

$$Y_{o_f} = [y_o(1 + Y R_s) + y_i y_c(r_{b'} + R_s) + Y(1 + y_i r_{b'})] / [1 + y_i(r_{b'} + R_s) + Y R_s] \quad 5-33$$

REFERENCE

1. K. Henney, Ed., *Radio Engineering Handbook*, Fifth Ed., McGraw-Hill Book Co., Inc., New York, 1959, Chapter 12.

CHAPTER 5

DESIGN OF TRANSISTOR *R-C* AMPLIFIERS

5-0 INTRODUCTION

The steps in the design of transistor amplifiers are, first, the preparation of a static design (or climate), and, second, the development of a small-signal, or dynamic, design. At the same time, the appropriate basic configuration for use with the active device must be selected. Because of the stability problem that develops with transistor circuits, the biasing configuration must be designed with considerable care. For this reason; the biasing problem is considered separately in Chapter 6. The static design procedure for use with transistors is relatively complex because neither of the input variables is negligible in any transistor configuration.

The specification of an appropriate static operating contour for an amplifier is based on the selection of a load line that permits the development of the required power output with conservative values of peak voltage, peak current, and peak power. The projection of this contour on the collector curve family usually is a straight line with a common-emitter amplifier, but it may be slightly curved for either a common-base or a common-collector amplifier. The discussion to follow considers first the full design procedure for the common-emitter *R-C* amplifier under several typical load-line conditions, and then similar problems for common-base, common-collector, and degenerative configurations.

5-1 COMMON-EMITTER *R-C* AMPLIFIERS

The construction of the static output load line for an *R-C* amplifier is based on the location of its two end points. One of these points is defined by the coordinates V_{CC} , 0, and the second by the coordinates 0, V_{CC}/R_L . The basic load contour is a straight line drawn through these two points.

Once the load line has been constructed on the output curve family, it must be transcribed to the input family. This process of transcription is easily accomplished if the preferred form of static data described in

Chapter 2 is used together with the curves in Appendix F. In Fig. 5-1, the intersection of the load line with any of the base-current contours may be noted, and the intersection point transferred vertically across to the corresponding base-current contour on the input family; this is done with each of the intersection points. Next, the input contour projection of the load contour may be drawn through the various transcribed points, and the data on input voltage and input and output current and output voltage may be tabulated, giving a complete set of static data.

The value of the voltage level in the base circuit is a function of the operating temperature of the transistor, and consequently will fluctuate considerably, but the voltage change from one base-current contour to the next is relatively fixed. As a result, the bias stabilization problem involves primarily the static behavior of the active device.

Once a trial static design has been selected, it is necessary to make a small-signal design to see if the static design provides an environment that makes available the required kind of operating conditions. This phase of design is of particularly critical importance, since it controls the eventual reliability of operation of the circuit. The importance of getting the desired operating conditions with minimum dissipation and minimum potential stresses cannot be overemphasized. Because power dissipation is dependent on the product of voltage and current, and is a function of static behavior, and the adequacy of the signal behavior is dependent on the small-signal characteristics, coordination of the two types of design requires a coordination of the static and small-signal characteristics. This kind of coordination is easily accomplished when conductance-type data sheets are used (Fig. 5-2), and a mean-square approximation to the small-signal data may be obtained by using the polynomial technique of Appendix C.

After the load contours are properly plotted on the input and output families of curves for a transistor, the values of the small-signal parameters at each of the intersections of the base bias contours with the load contour may be tabulated, and the appropriate values may be used with the equations derived in Chapter 4

in the calculation of the amplification and the driving-point admittances. For ordinary low-frequency operation, the black-box equations may be used directly, but for high-frequency operation, the effect of base-spreading resistance must be taken into account in the design.*

It is seldom possible to use a single-load contour for both the static and the small-signal operation of a transistor amplifier because the input admittance of transistors is relatively high compared to the usable output admittance level. Because the single load-line design forms the basis for handling all commonly used standard types of circuits, it is considered first. Example 5-1 shows the procedure.

*The nomograph provided in Appendix G may also be used if desired.

EXAMPLE 5-1. Design an amplifier utilizing a type 2N592 (34S) transistor, the supply voltage being 30 V, and the circuit as in Fig. 4-1. Calculate the amplification as a function of base current, and select operating conditions that will limit the distortion to 5%. Determine the values of the intrinsic parameters g_i' and g_f' using Eqs. 2-13 and 2-15. The load resistance is 6000 ohms, and the base-spreading resistance is 230 ohms.

The static and small-signal data for the transistor are listed in Table 5-1.

These data show that if correction for base-spreading resistance is important, the selected values for the contours for g_i and g_f must be more closely spaced for high values of base current if good data on g_i' and g_f' are to result. The extra values are required in the calculation of the value of the expression $(1 - g_i r_b')$ in Eqs. 2-13 and 2-15 because the product $g_i r_b'$ may have a value

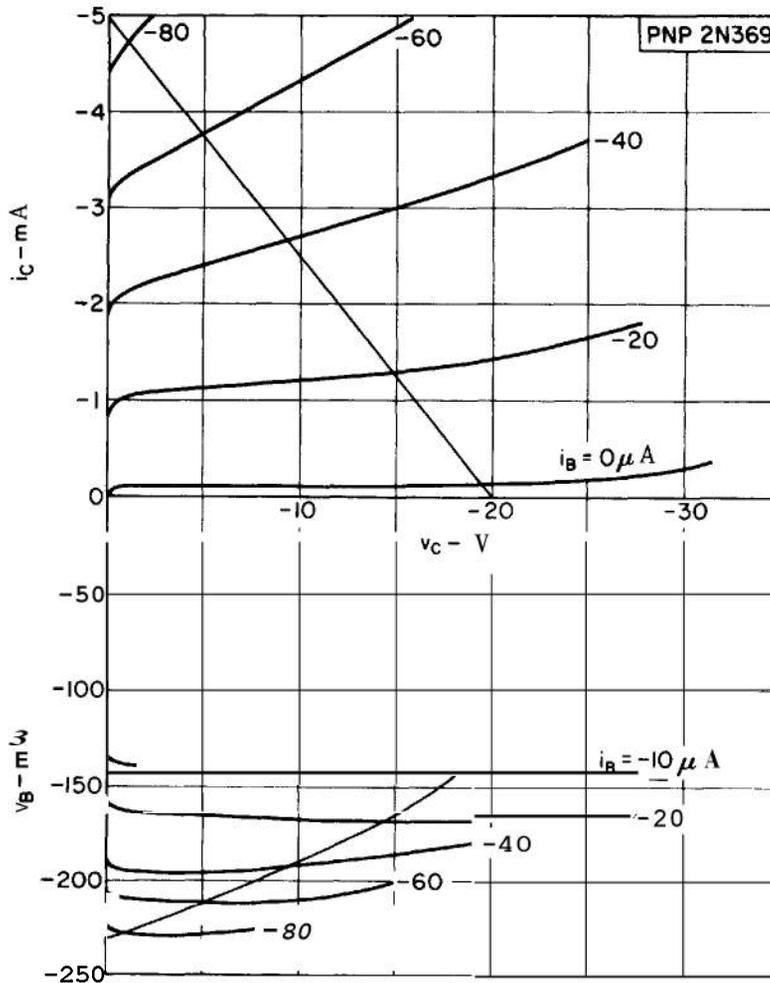


Fig. 5-1. Typical Load Contours

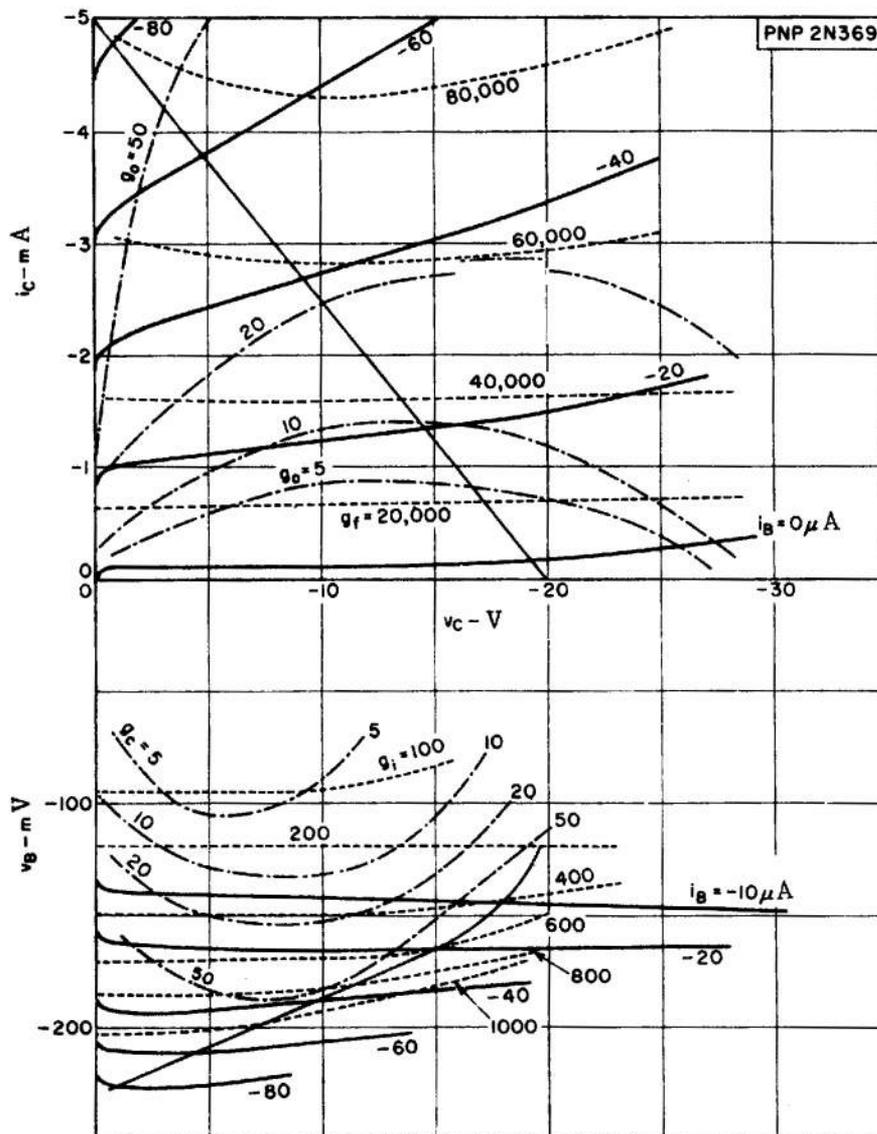


Fig. 5-2. Complete Data

TABLE 5-1
PARAMETER AND VARIABLE DATA

I_b μa	V_c volts	g_i pmho	g_f pmho.	g_o $\mu mho'$	g_c pmho	$g_{i'}$ pmho	$g_{f'}$ pmho	I_c ma
25	24	900	30,000	5.2	15	1135	37,830	1.0
50	18	1300	52,000	13	30	1860	74,150	2.0
75	12.3	1700	70,000	26	45	2794	115,000	2.95
100	7.6	2000	80,000	44	80	3700	148,000	3.72
125	3.4	2200	90,000	70	120	4453	182,200	4.42

approaching unity. The contours presented in Fig. 5-3 are of limited direct use for design at high frequency for the same reason. Because of the effect of the base-spreading resistance and emitter-current choking effects, the value of g_r can reach a maximum and then decrease slowly as the collector current is gradually increased (Fig. 5-4).

The amplifications and the driving-point admittances may now be determined. For this calculation, it is convenient to take the values of R_s of 0, 500, 2000, and 10,000 ohms to show the effect of the source impedance. Typical results are listed in Table 5-2.

The values of Y_i may be calculated both on the basis of the straight black-box parameters and also on the basis of the intrinsic parameters, and give approximately the same results. In a similar manner, the values of Y_o min are the value of output admittance with

$R_s = 0$, and Y_o max the value with $R_s = 10,000$ ohms.

In Eq. A-10, Appendix A, the distortion in an amplifier, assuming a linear variation of amplification with bias current, reaches 5% when the maximum amplification is 50% greater than the minimum, or, with a minimum amplification of 20, the maximum would be 30. The usable ranges are tabulated in Table 5-3.

The best operating conditions for minimum distortion are with an input source impedance of about 2000 ohms because the voltage gain is considerable and the distortion also is quite small. For a more accurate calculation of distortion with $R_s > 2000$ ohms, the technique of Appendix C should be used.

After the bias ranges have been selected for the amplifier as a function of the source resistance R_s , the required value of base-bias resistance may be selected. Table 5-3 shows that the range of bias is from 25 to 125

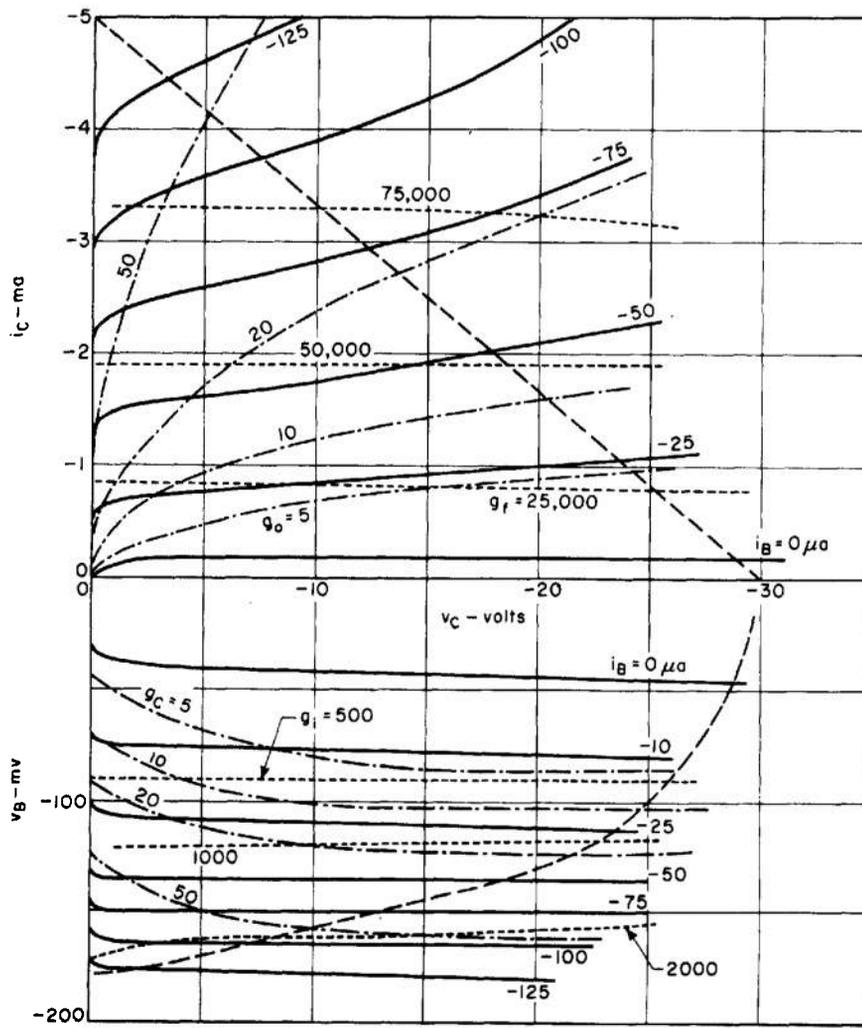


Fig. 5-3. Curves of 2N592 Transistor for Example 5-1

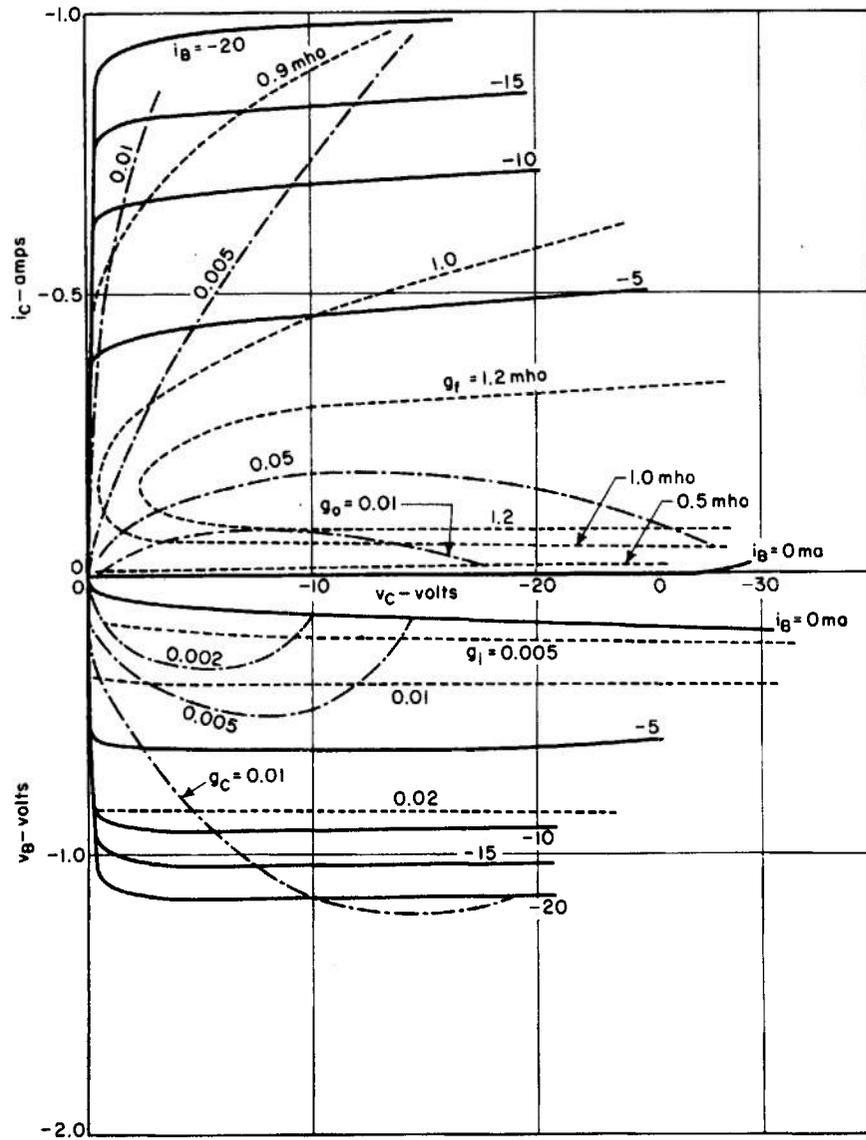


Fig. 5-4. Loop-back in Forward Conductance Contours for Example 5-1

TABLE 5-2
AMPLIFICATIONS AND ADMITTANCES

Bias	K_o	K_{500}	K_{2000}	$K_{10,000}$	Y_i	$Y_o \text{ min}$	$Y_o \text{ max}$
25	-175	-118	-60.2	-16.6	950	5.2	14.0 pmho
50	-287	-169	-75	-21.5	1424	13	28.8
75	-370	-183	-73.3	-17.4	1900	26	43.9
100	-380	-175	-66.4	-15.4	2340	44	78.5
125	-381	-173	-64	-13.7	2670	70	118

μA , giving a Q-point current of about $75 \mu\text{A}$. Since the supply voltage is 30 V, the bias resistance required is

$$R_b = 30 / (75 \times 10^{-6}) = 400,000 \text{ ohms}$$

The input coupling capacitance C_c is determined in terms of the input admittance calculated in Table 5-2. The capacitance may be determined in terms of the minimum operating frequency f_1 and the equation

$$C_c = Y_i / (2\pi f_1)$$

A rather large value of capacitance normally is required because the input admittance for the transistor is large.

5-2 COMPOUND LOAD LINES

A transistor R-Camplifier is seldom used under conditions that a simple load-line configuration applies. Consequently, the problem of handling compound load lines is of considerable importance to the circuit designer. First, a static load line must be plotted as has already been described, and then a suitable static operating point must be selected and the dynamic or active load line determined.

The load resistance selected for use with a transistor must provide the amount of collector current required for proper operation. This selection is one of the most important, yet poorly understood operations to be performed. The maximum available collector current must be sufficiently large so that the peak current required under load can be obtained without driving the transistor into saturation. For this reason, the maximum current at saturation along the static load line should be greater than 0.6 of the peak-loaded collector current (Fig. 5-5).

The positioning of the dynamic load contour for maximum available balanced output signal, given specified values of static load resistance and dynamic resist-

ance, may be established in terms of the ratio of the resistances

$$t = R_{LD} / R_L \text{ or } R_{LD} = tR_L \tag{5-1}$$

The coordinates of the static operating point in terms of the supply voltage and the static resistance are then

$$V_c = tV_{CC} / (t + 1) \tag{5-2}$$

$$I_c = V_{CC} / (R_L(t + 1)) \tag{5-3}$$

These equations are derived by the simultaneous solution of the basic relations

$$V_c = V_{cc} - tI_cR_L \tag{5-4}$$

$$I_c = I_{ct} - V_c / R_L \tag{5-5}$$

$$V_c = V_{cc} - I_cR_L \tag{5-6}$$

$$I_c = I_{ct} - V_c / (tR_L) \tag{5-7}$$

$$V_c = 2V_c \tag{5-8}$$

$$I_{ct} = 2I_c \tag{5-9}$$

In these equations, the points specifying I_{ct} and I_{ct} are shown in Fig. 5-5.

The given equations show that the value of I_{ct} need be only somewhat greater than the value of I_{ct} . In no case, with symmetric deviation, can it be as great as twice I_{ct} , since it has to have a value twice I_c . For this reason, a convenient starting point for design of a tran-

TABLE 5-3
AMPLIFICATION AND DISTORTION

Bias range	Amplification range	Nominal distortion	R_L
50 to 125	-287 to -381	3.5%	0
25 to 125	-118 to -175	4.9%	500
25 to 125	-60.2 to -75 to -64	1.4 (third)	2,000
25 to 125	-16.6 to -21.5 to -13.7	2.7 (third)	10,000

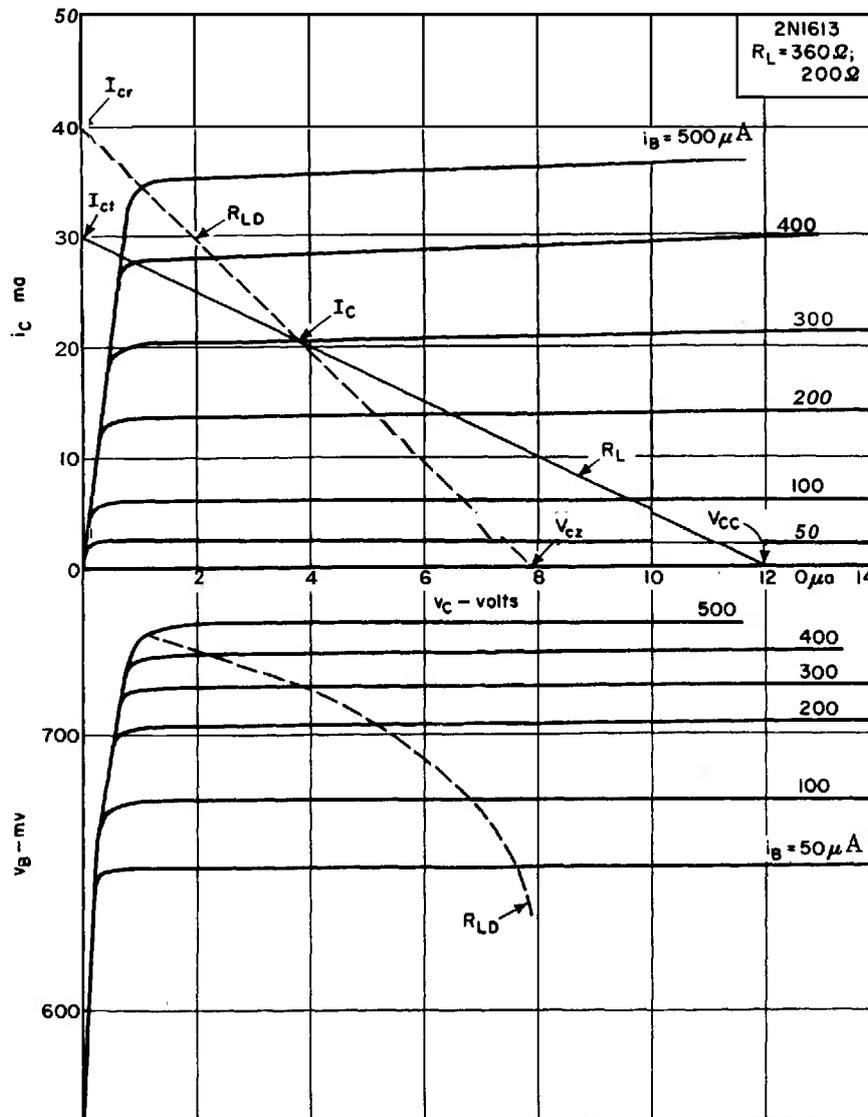


Fig. 5-5. Combination Load Lines

sistor amplifier is the selection of the collector current under dynamic saturation conditions. The value of the static saturation current selected may be approximately three-quarters of the dynamic saturation current, and its product with the collector supply voltage should be less than twice the rated collector dissipation if the peak transistor dissipation is kept within bounds. Then setting the static saturation current at three-fourths of the dynamic value leads to a dynamic load resistance half the static value, or $t = 0.5$.

Since combination load lines must be used with transformer coupled amplifiers and many transistorized amplifiers, the general technique of handling such

designs is described next, and the application to transformer-coupled amplifiers is considered in Chapter '7.

When an amplifier having different static and dynamic load lines is required, the design procedure followed differs in minor details from that for the simpler form of amplifier. First the static and dynamic load lines are plotted, and the static operating point, the Q-point, is located as previously described. It is unnecessary for the static load line to be transcribed to the input family, as the signal behavior is controlled by the dynamic load line. The intersections of the dynamic contour with the various base-current contours are transferred to the input family just as has already been

described, and the small-signal calculations are made using the parameter values read at respective intersections along these contours. The complete procedure is required even with cathode followers and emitter followers. All small-signal calculations must be based on data taken from the active or dynamic load contours.

EXAMPLE 5-2. Design an amplifier using the 2N592 transistor, with a static load resistance for the collector circuit of 10,000 ohms, and a dynamic load resistance of 5000 ohms. The collector supply voltage is 25 V.

The calculation of g_i' and g_f' and the remaining corresponding calculations made in Example 5-1 are left for the reader.

First the load contours are drawn as shown in Fig. 5-5. Then the small-signal data may be tabulated and the various calculations performed. Input conditions for the amplifier are taken the same as in Example 5-1. The nominal value of I_{cr} is 2.5 mA, and using Eq. 5-2 the collector voltage at the Q-point is 8.3 V. The static collector current is 1.67 mA. Solving Eqs. 5-2 and 5-3 for I_{cr} in terms of V_{CC} , R_L , and t gives

$$I_{cr} = 2V_{CC} / \langle R_L(1 + t) \rangle \tag{5-10}$$

Substituting gives a peak dynamic collector current of 3.33 mA. The dynamic load line passes through the points (-16.7, 0) and (0, -3.33).

The small-signal data as a function of base bias are listed in Table 5-4.

Using the value of R_{LD} of 5000 ohms and the trial values of R_s of 0, 500, 2000, and 10,000 ohms, the amplifications and conductances may be tabulated as in Table 5-5.

The data given in Table 5-5 show that the distortion is less than 5% under the conditions in Table 5-6.

The data for $R_s = 10,000$ ohms are irregular, largely because of the $g_i g_c R_s R_L$ term. As a result, a least-squares smoothing of the data by orthogonal polynomials is required for determination of distortion. For values of R_s as large as 10,000 ohms, the transistor behaves

as a current amplifier, and its current gain may be expressed by the equation

$$K_I = g_f/g_i \tag{5-11}$$

5-3 FREQUENCY RESPONSE

The frequency response of transistor amplifiers like those just considered is largely determined by the source impedance of the input circuit in conjunction with the input admittance characteristics of the transistor. The base-spreading resistance of the transistor may be lumped with the impedance of the voltage source in initial calculations, but it must be included separately when the source impedance is small.

The first step in making a calculation of the frequency response of a transistor amplifier is the determination of the α -cutoff frequency. Usually this frequency is given on the data sheet for the transistor. If it is not, however, it may be measured approximately in the laboratory. Because the value of this frequency is a wide-tolerance parameter, i.e., there is a considerable range within which it may lie, it is necessary that test measurements be made on a number of sample devices. A discussion of the α - and β -cutoff frequencies is included in Chapter 2.

The effective input capacitance of the transistor may be approximated next, since it is determined by the equation

$$\omega_\alpha C_i = (g_i + g_f) \doteq (g_i' + g_f') = 2\pi f_\alpha C_i \tag{5-12}$$

Because the total input capacitance is a function of both the emitter (or collector, approximately) current and the base-to-emitter voltage, the value of C_i varies from point to point over the operating area. For this reason, it would be convenient if designers had contour plots of the input capacitance as a function of collector current and the input voltage. The user then could easily

TABLE 5-4
SMALL-SIGNAL DATA

I_b	V_c	I_c	g_i	g_f	g_o	g_c
0	15.9	0.16
25	12.5	0.84	850	25,000	6	13
50	8.3	1.70	1300	45,000	17	32
75	4.1	2.52	1600	61,000	40	55
100	0.9	3.14	2000	72,000	110	200

**TABLE 5-5
AMPLIFICATIONS AND CONDUCTANCES**

I_b	K_o	K_{500}	K_{2000}	$K_{10,000}$	Y_i	Y_o min micromhos	Y_o max
25	-121	-84.5	-44.0	-12.4	1080	6	12.2
50	-207	-122	-44.8	-10.8	1390	17	31
75	-254	-137	-57.8	-14.1	1700	40	54
100	-232	-101	-37.7	-8.2	2580	110	196

**TABLE 5-6
CONDITIONS FOR < 5% DISTORTION**

Value of R_s	0	500 ohms	2000	10,000
Bias range	50-100	50-100	25-100	...

determine the approximate amount of capacitance with which he must deal.

Fig. 5-6 shows the effect of variation of the source resistance R_s on the frequency response of an ideal transistor having negligible base-spreading resistance. Under such conditions, the limitation on the maximum operating frequency of the transistor is largely determined by the values of the Q-factor for the tuned circuits that may be used with the device. If the impedance of the signal source is zero, the input reactive power into the amplifier rises linearly with frequency, whereas the output power remains relatively constant until output capacitance loading causes it to decrease.

If the power-gain equation in Chapter 2 is rewritten, making the substitutions

$$y_{i'} = g_{i'} + j\omega C_i,$$

where $|\omega C_i| > 1 > y_c R_L \doteq y_c R_L$ and, including r_b , it takes the form

$$K_s K_i / (g_{i'}^2 R_L) = 1 / (g_{i'} - j\omega C_i) [1 + (g_{i'} + j\omega C_i)(R_s + r_b)] \tag{5-13}$$

where the remaining terms in the denominator have been neglected because of the above inequality. For frequencies large compared to the β -cutoff frequency, this reduces to

$$K_s K_i / (g_i^2 R_L) = 1 / (-j\omega C_i) [1 + g_i (R_s + r_{b'}) + j\omega C_i (R_s + r_{b'})] \quad (5-14)$$

Clearly, below the β -cutoff frequency, determined by $g_i = \omega C_i$, the power gain is independent of frequency, and above, it decreases at least at a rate of 3 dB per octave. Above the frequency for which the second term in brackets has equal real and imaginary parts, the decrease is at the rate of at least 6 dB per octave.

A nomograph may be prepared to solve the elements of this equation. One prepared for the solution of either section is shown in Fig. 5-7. One of the scales of this nomograph is designated by g and r . It may be used with values of

$$(g_i' + g_f'), \quad g_i', \quad r_{b'}, \quad \text{or} \quad (R_s + r_{b'})$$

in the calculation of either frequency response or input capacitance, depending on which is required.

The first step in calculation requires use of elements 1, 3, and 5 in relating the β -corner frequency to the input capacitance and input conductance. These lines may also be used to calculate the corner frequency generated by the total source resistance, including base-spreading resistance, and the input capacitance. Lines 1, 2, and 4 may be used to calculate the value of a conductance-resistance product, and may be used in the calculation of such products as

$$g_i R_s, \quad g_i r_{b'}, \quad g_i (R_s + r_{b'}) g_f R_L, \quad (g_f + g_o) R_L, \\ \sigma (g') R_L, \quad g_o R_L$$

and similar terms. They may also be used for the calculation of $(g_i R_s)(g_o R_L)$ and similar terms by using the g_i scale on line 4 for $(g_o R_L)$ and the $(R_s + r_{b'})$ scale on line 1 for $(g_i R_s)$.

If the value of $g_i (R_s + r_{b'})$ is less than 25, then it is necessary to use scales 5, 6, and 7 to correct for the $g_i (R_s + r_{b'})$ in the determination of the corner frequency for the voltage-gain expression, but if it is greater, then the corner frequency is approximately the β -corner frequency determined by $\omega C_i = g_i$. When the correction is required, the value of the product

$g_i (R_s + r_{b'})$ found on line 2 is transferred to line 7, and the intersection of the straight line joining the frequency on line 5 with the appropriate product on line 7 with line 6 gives the corrected frequency. As the value of $g_i (R_s + r_{b'})$ becomes large compared to unity, the corrected frequency approaches closer to the β -cutoff frequency.

The axis line crossing scales 1, 3, and 5 in the drawing shows the calculation for $g_i' = 0.013$ mho, $C_i = 16,000$ pF, and $\omega = 2\pi f = 800,000$ rad per sec. Similarly, the axis line crossing scales 1, 2, and 4 shows the calculation for $g_i' = 0.009$ mho, $(R_s + r_{b'}) = 230$ ohms, and a product of 2.0 units. This point on scale 2 is transferred to scale 7 to complete the calculation of ω' as 1,600,000 rad per sec.

The scales 1, 3, and 5 may be used for calculation of the a-cutoff frequency in terms of $(g_i' + g_f')$ and C_i and the second scale for β on line 7 may be used to convert the result to the upper noise corner frequency. The reader will find this nomograph useful for many frequency-response calculations of a similar nature.

The collector transition capacitance can introduce a feedback component that will alter the frequency response of an amplifier. In resistance-coupled amplifiers, however, the load impedance in the collector circuit is sufficiently small that its effect usually can be neglected.

EXAMPLE 5-3. Determine the variation of the 3 dB frequency with input resistance for the 2N592 transistor, assuming its a-cutoff frequency is 0.4 MHz, and its β is 40. Take $g_f' = 50,000$ micromhos, $g_i' = 1250$ micromhos, and $r_{b'} = 230$ ohms.

The β -cutoff frequency may be read from the nomograph as 9800 Hz. To do this, first the value of β , and the value of $(g_i' + g_f')$ are used to calculate C_i , and this value of C_i used with the value of g_i' to determine β .

Next, the minimum value of $g_i' r_{b'}$ may be determined, and the maximum operating frequency is determined in two steps. First the frequency ω_i corresponding to values of C_i and $r_{b'}$ may be found with scales 1, 3, and 5, and then the value of ω_i on scale 5 converted to the maximum operating frequency on scale 6 by the use of the value $g_i' r_{b'}$ on scale 7. The value of ω_i is, because $C_i = 21,000$ pF, approximately 34,800 Hz, and a final corrected frequency of 44,900 Hz. The highest possible operating frequency of this transistor as a

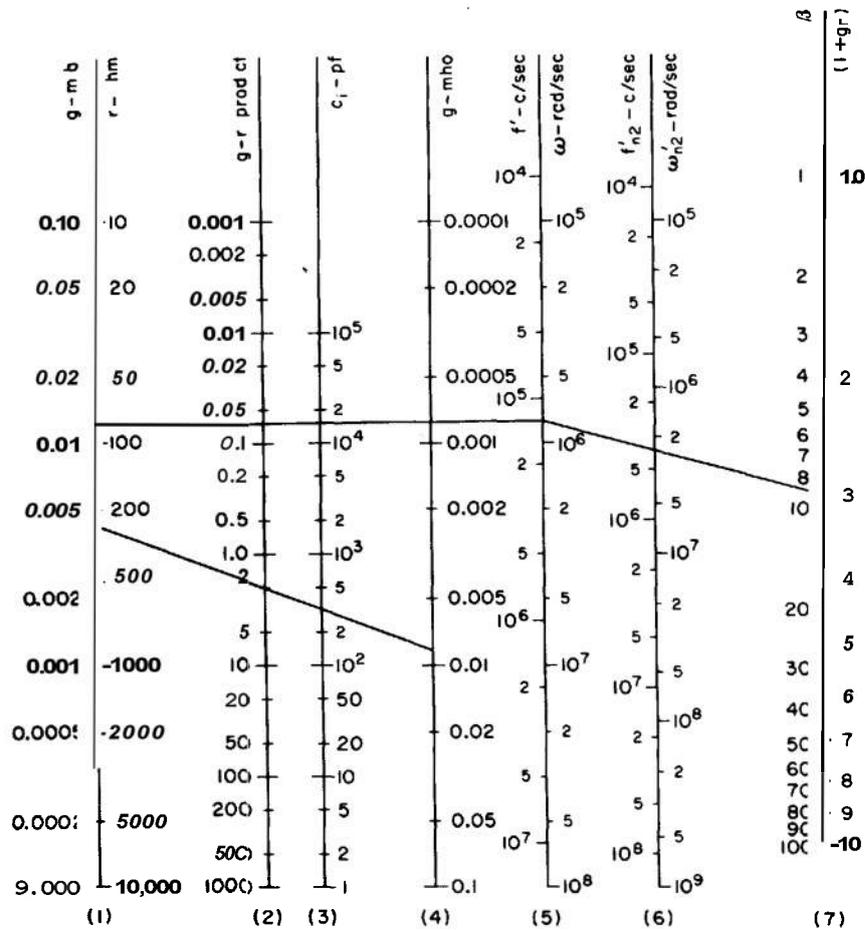


Fig. 5-7. Calculation Nomograph

voltage amplifier with less than 3 dB roll-off therefore is 44,900 Hz, and the lowest, 9800 Hz. Fig. 5-8 shows the variation of the corner frequency with R_s .

5-4 TOLERANCE CHECKING

One of the important steps in the process of design of circuits is the checking to determine the consequences of variations of the values for both the fixed components like resistors and also for the values of the small-signal parameters. The most important parameter of the transistor in tolerance checking is the input admittance, inasmuch as it is the most variable important factor. The two output admittances do vary appreciably, but their effect on the design is normally much less significant because of their relatively small magnitude. The forward conductance is a most important parameter, but its value is surprisingly stable with time

and from device to device of a given type of transistor. A tolerance range of $\pm 20\%$ is usually more than adequate for the forward conductance, but with many transistors the tolerance required on the input admittance may be as large as -50% to $+100\%$ or more.

A narrower range of tolerances is required for the fixed components used with the circuit. The process of checking for the effect of tolerances is not as complex as that which is used with triode tubes (Ref. 1). Because a good explanation of the procedure is contained in Ref. 1, only a sample problem is included in this book.

EXAMPLE 5-4. Assume that transistors for use in the circuit of Example 5-1 have approximately equal values of internal transconductance (equal g_f' values), but that the range of input conductance, for a given collector current, is from 70% to 150% of rated value. If the base-spreading resistances of all the transistors of the lot are approximately equal, calculate the amplifications and the input and output conductances for the

limit transistors. Take the value of r_b' as 230 ohms, assume that the values of g_f' , g_o' , and g_c' are unchanged from Example 5-1. The results are shown in Table 5-7.

The values of distortion for these various ranges of bias current should be determined using orthogonal polynomials. Table 5-8 includes only rough approximations to the actual values.

A similar solution may be prepared for the condition of reduced base current and base conductance as given in Table 5-9.

The values of g_f' have been copied directly from the original example, the values of g_i' have been scaled up or down from those of the original example, and the appropriate terminal values of g_i and g_f calculated. The

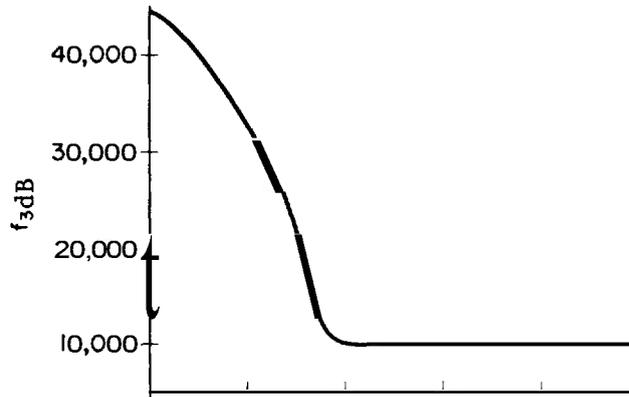


Fig. 5-8. Frequency Variation for Example 5-3

TABLE 5-7
 g_i 50% HIGH

I_b	V_c	si	g_f	g_o	g_c	g_i'	g_f'	I_c
37.5	24	1223	27,200	5.2	15	1703	37,830	1.0
75	18	1750	46,500	13.0	30	2790	74,150	2.0
112.5	12.3	2130	58,500	26	45	4191	115,000	2.95
150	7.6	2440	65,000	44	80	5550	148,000	3.72
187.5	3.4	2650	72,200	70	120	6680	182,200	4.45

I_b	K_o	K_{500}	K_{2000}	$K_{10,000}$	Y_i	$Y_o \text{ min}$	$Y_o \text{ max}$
37.5	-158.6	-96.6	-44.2	-11.4	1294	5.2	14.2
75	-254	-135.9	-53.1	-12.7	1914	13	29.1
112.5	-309	-141	-53.6	-12.4	2382	26	44.1
150	-309	-127.0	-46.0	-10.8	2860	44	78.6
187.5	-306	-117.2	-41.1	-9.2	3220	70	118.2

TABLE 5-8
DISTORTION ESTIMATES

R_i	$I_b \text{ range}$	$K \text{ range}$	Distortion	Component
Zero	75-187.5	254-309-306	3%	Second
500	37.5-187.5	96.6-141-117.2	2.2%	Third
2,000	37.5-187.5	44.2-53.6-41.1	1.8%	Third
10,000	37.5-187.5	11.4-12.7-9.2	1.3%	Third

TABLE 5-9
g_i 30% LOW

I_b	v_c	g_i	g_f	g_o	g_c	$g_{i'}$	$g_{f'}$	I_e
17.5	24	672	32,000	5.2	15	795	37,830	1.00
85	18	1002	57,000	13	30	1304	74,150	2.00
52.5	12.3	1349	79,400	26	45	1956	115,000	2.95
70	7.6	1622	92,100	44	80	2590	148,000	3.72
87.5	3.4	1816	106,100	70	120	3120	182,200	4.45

I_b	K_o	K_{600}	K_{2000}	$K_{10,000}$	Y_i	$Y_o \text{ min}$	$Y_o \text{ max}$
17.5	-186.6	-137.4	-77.0	-22.9	711	5.2	13.7
35	-314.6	-138.0	-99.3	-26.5	1097	13	28.4
52.5	-420	-239	-104.4	-26.1	1508	26	43.7
70	-441	-226	-91.8	-22.0	1900	44	77.9
87.5	-450	-213.7	-83.2	-19.5	2200	70	117.4

TABLE 5-10
RANGE OF OPERATION AND DISTORTION DATA

R_s	$I_b \text{ range}$	$K \text{ range}$	Distortion	Component
Zero	35-87.5	314.6450	4.5%	Second
500	35-87.5	204.8-239-213.7	1.1%	Third
2,000	17.5-87.5	77-104.4-83.2	2.1%	Third
10,000	17.5-87.5	22.9-26.5-19.5	1.8%	Third

range of operation and distortion data may be tabulated as in Table 5-10.

Once again, if reasonably exact data on distortion are desired, orthogonal polynomial techniques should be used.

The range of the effect of the parameter variations is large, and it must be allowed for in the process of design, either by the use of degeneration or by the use of special compensation techniques. Examples of such compensation may be found in the paragraphs on feedback amplifiers, pars. 5-7 and 5-8.

5-5 THE COMMON-BASE AMPLIFIER

The common-base amplifier is seldom used as a component of an R - C amplifier chain because of the fact that the current gain available is somewhat less than unity. Unless the interstage coupling circuit is capable of generating a current gain, therefore, no net amplification results in a series of cascaded common-base amplifiers.

The first step in the design of this type amplifier is the selection of an appropriate load contour. As with the common-emitter amplifier, it is convenient to plot the static and dynamic load contours on the output curve family, and then transfer them to the input

family. However, because the characteristic curves are commonly presented with the emitter as the reference electrode, a correction must be made for the fact that the output circuit now is from collector to base rather than collector to emitter.

This correction is easily made once the input and output contours for the load have been plotted in the common-emitter configuration. At each intersection of a base-current contour with the input load contour, the base voltage may be read and added to the collector voltage on the corresponding base-current contour for the output curve family. A new corresponding point may be plotted on the input family also, and a recorrection made if the base-current contour is not very nearly horizontal. The resulting points specify the common-base load contours for the input and the output curve families. The geometrical construction is shown graphically in Fig. 5-9.

Once the corrected operating contour has been established on both the input and the output curve families, then the balance of the design is routine. The values of the small-signal parameters are read at the selected points along the corrected operating contour and the calculations made using Eqs. 4-25 through 4-28. The input admittance for the common-base amplifier is at least 10 to 100 times larger than that for the corresponding common-emitter configuration, and the over-

all power gain is correspondingly less, but for applications in which a wider frequency-response range is required than can be obtained with the common-emitter configuration, the common-base circuit can be helpful. Example 5-5 gives an indication of the behavior that can be expected from a medium-frequency transistor used in the common-base configuration.

EXAMPLE 5-5. Using an HA-5002 transistor (NPN type), a supply voltage of 5 V, a load resistance R_L of 500 ohms, and a base-spreading resistance of 70 ohms, design a common-base amplifier and determine its circuit characteristics. Take the a-cutoff frequency of the transistor as 1 MHz.

The equation for amplification for the common-base amplifier, including base-spreading resistance, is

$$K = \frac{(y_{f'} + y_o + y_i y_c r_b) R_L}{[1 + y_i r_b + \sigma(y') R_s + y_o R_L + y_i y_c (r_b R_s + r_b R_L + R_s R_L)]} \quad (5-15)$$

The load line is plotted and corrected as described, giving the contour shown in Fig. 5-10. Then the small-signal data may be tabulated, and the input and forward admittances converted to intrinsic values by the use of the value for the base-spreading resistance. Then the amplifications and the input and output admit-

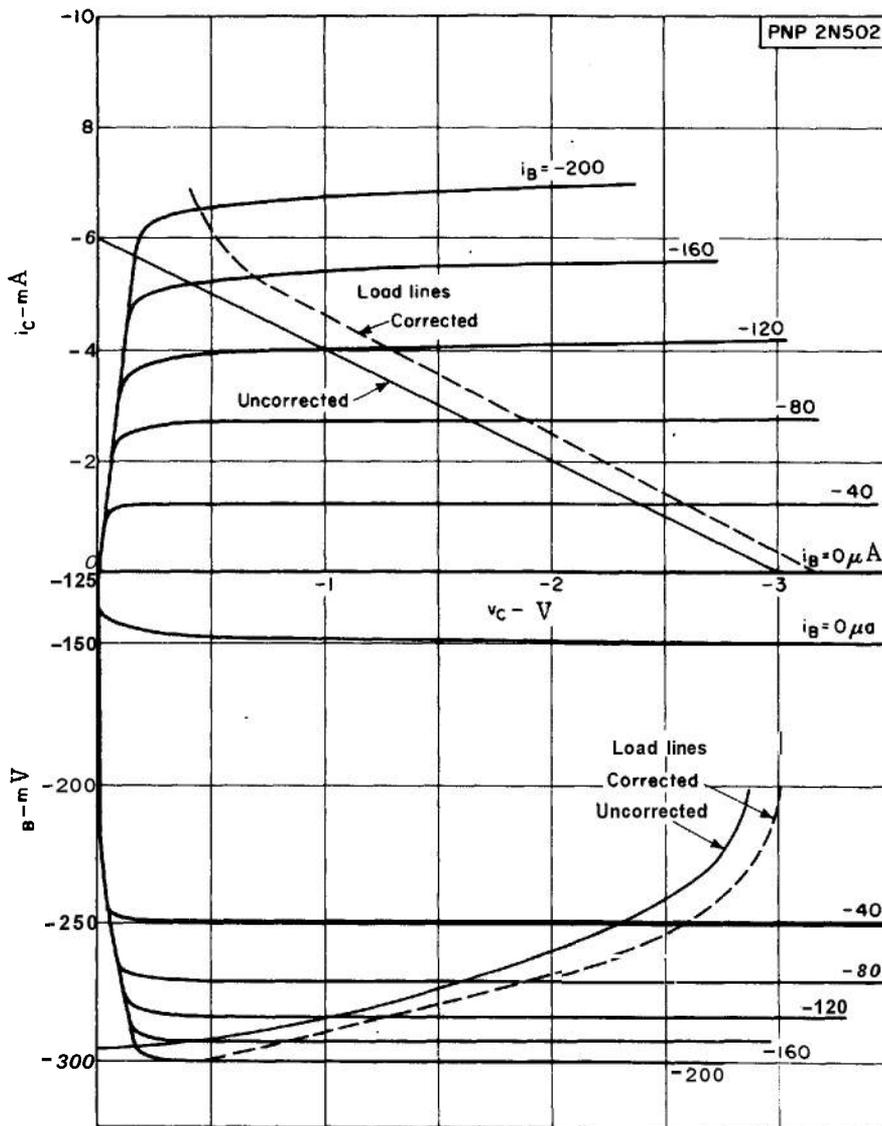


Fig. 5-9. Common-base Load Lines

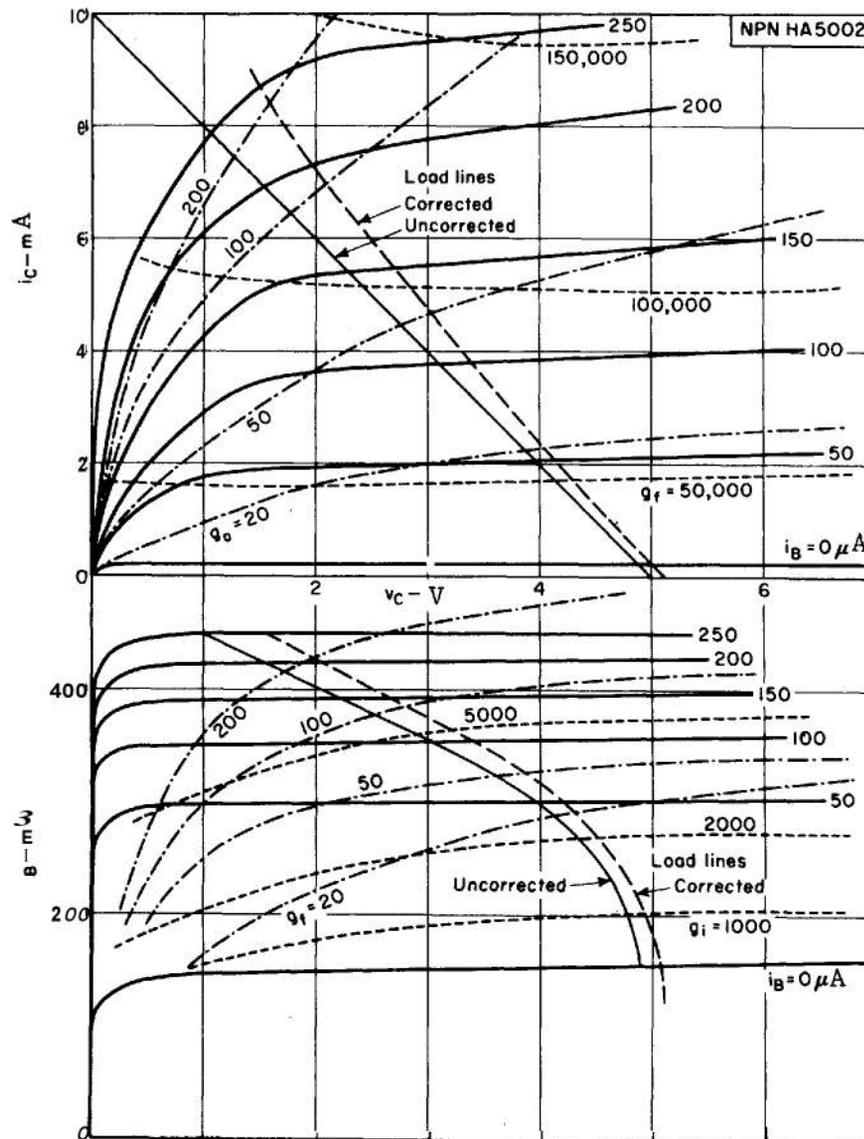


Fig. 5-10. Load Lines—Common-base Amplifier for Example 5-5

tances may be calculated. The data in Table 5-11 show these results, and include some adjustments in areas in which the data are somewhat incomplete.

For this problem, the source resistance R_s may be selected as one of the values of 0, 5, 10, or 20 ohms. The amplification and admittance values are as listed in Table 5-12.

The fact that $Y_{o,min}$ is larger than $Y_{o,max}$ is a result of the fact that a small source impedance gives a large output admittance, and vice versa.

The range of amplification that can be used for each set of operating conditions and the distortion and avail-

able total voltage change in the output circuit may now be tabulated as in the previous examples (Table 5-13). The required value of source resistance is almost unbelievably small because of the correspondingly large input admittance values noted in Table 5-12. The approximate value of input resistance varies over the range from 7 to 30 ohms.

Frequency Response. The frequency response of the common-base amplifier is determined primarily by the susceptance component of the input admittance of the transistor. If the equation for voltage gain is revised to include the capacitance, it takes the form

**TABLE 5-11
SMALLSIGNAL DATA**

I_b	I_c	V_c	g_i	g_f	$g_{i'}$	$g_{f'}$	g_o	g_c
0 μa	0.3 ma	5.0	0	0	0	0	0	0
20	1.1	4.7	1600	30,000	1,800	33,100	8	12
40	1.8	4.4	2700	51,000	3,330	63,000	14	20
60	2.4	4.05	3700	61,000	5,000	82,400	21	38
80	3.1	3.8	4500	70,000	6,560	102,000	33	50
100	3.8	3.5	5000	80,000	7,700	123,000	39	72
150	5.5	2.7	5800	105,000	9,760	177,000	70	120
200	7.4	1.85	6500	125,000	11,900	229,000	120	180
250	8.7	1.5	6700	138,000	13,200	260,000	220	300

**TABLE 5-12
AMPLIFICATIONS AND ADMITTANCES**

I_b	K_o	K_6	K_{10}	K_{20}	Y_i	micromhos	
						$Y_{\theta \text{ min}}$	$Y_{o \text{ max}}$
20	14.6	12.6	11.1	9.0	31,500	8.4	5.4
40	25.5	20.1	16.6	12.3	53,400	15.2	8.0
60	30.3	22.9	18.4	13.3	64,200	25.4	12.7
80	32.4	24.1	19.2	13.6	73,700	38.4	18.0
100	39.5	27.8	21.5	14.8	83,800	50.6	22.2
150	51.7	33.5	24.7	16.2	109,200	90.8	33.6
200	60.6	37.0	26.6	17.1	127,300	147.4	48.9
250	63.6	38.1	27.3	17.3	134,300	258	80.9

$$K = (g_{f'} + g_o)R_L / [1 + \sigma(g')R_s + g_{i'}r_{b'} + j\omega C_i(R_s + r_{b'})] \quad (5-16)$$

$$\omega = (1 + g_{i'}r_{b'}) / r_{b'}C_i, \quad R_s \rightarrow 0 \quad (5-17)$$

**TABLE 5-13
DISTORTION RANGE**

R_s	Δv_c	$I_b \text{ range}$	$K \text{ range}$	D
0	1.2	150-250 pa	51.7-63.6	2.6%
5	2.0	100-250	27.8-38.1	3.9%
10	2.55	60-250	18.4-27.3	4.9%
20	2.9	40-250	12.3-17.3	4.2%

For the second condition, the equation takes the form

$$\omega = (g_{i'} + g_{f'})R_s / \langle (r_{b'} + R_s)C_i \rangle = \omega_\alpha \quad (5-18)$$

This equation has been simplified by neglecting the terms involving y_i, y_c and y_o in both the numerator and the denominator. Two limiting conditions can be established for the maximum frequency for the amplifier, the first when R_s is small compared to $r_{b'}$, and the other when $R_s \gg r_{b'}$. For the first condition, the following limiting equation holds

The use of a voltage source gives an amplifier in which the frequency limitation depends on the value of $g_{i'}$, whereas the use of a moderately large value of R_s (a constant-current source) gives a much higher limiting frequency, approximately the a-cutoff frequency. This mode of operation is used extensively for high-frequency amplifiers. The further behavior of the circuit is considered in a later chapter.

5-6 THE COMMON-COLLECTOR AMPLIFIER

The common-collector amplifier is the transistor equivalent of the cathode follower used extensively as an impedance converter. This amplifier has properties that are useful when a low-impedance signal source is required, but it often can be replaced by a properly designed common-emitter amplifier. The procedure for design of the common-collector amplifier parallels that used with the common-base amplifier, but it differs in several important aspects. The general method of design of this circuit is first discussed in the next few paragraphs, and then an example is worked out to show the detail steps required in determining the characteristics of the circuit.

The construction procedure for the load lines required for the common-collector amplifier may be based on those used with the common-emitter amplifier. As with the common-base amplifier, an adjustment is required to correct for the changed configuration, but the correction with this circuit is for base-current flow in the output resistance. The effect of this current is to increase the voltage developed across the load resistance, and thereby to reduce the effective value of the voltage from collector to emitter (Fig. 5-10). Unless the transistor has a very small value of β , the change that results is very small, and often may be small enough that it may be neglected.

Both a static and a dynamic load line must be constructed for use with this amplifier, as the normal dynamic value of load impedance may be a small fraction of the static value, and it is impossible to make even moderately reliable calculations of the amplifier characteristics on the basis of the static load contour alone. Under true small-signal conditions, where the excursion is very small with respect to the Q-point, such a construction may not be necessary, but if the emitter current change is appreciable, both lines must be constructed. Even under small-signal conditions, an appreciable change in gain and terminal impedances can result from loading.

Once the operating load contour has been plotted, then the values of the respective small-signal parameters at the different intersections of the load line and the base-current contours may be tabulated as has been done in previous examples. These data may be used with Eqs. 4-32 through 4-34 for the calculation of the operating characteristics of the transistor emitter-follower.

The frequency-response characteristics of the emitter-follower are more complex than for either of the

amplifiers previously considered because the capacitive term appears in both the numerator and the denominator of the gain expression. As a result, as the operating frequency is increased, first a knee is reached at which the amplification decreases as a function of frequency (the denominator knee), and at a higher frequency, nominally the α -cutoff frequency, the amplification once again levels off because of the knee in the numerator polynomial. The two equations that govern the behavior are:

roll-off knee

$$\omega_a = [g_{i'} + g_{f'}(R_e/\sigma(R)) + 1/\sigma(R)]/C_i \quad (5-19)$$

level-off knee

$$\omega_b = (g_{i'} + g_{f'})/C_i \quad (5-20)$$

In Eq. 5-19, the value of $\sigma(R)$ is defined by the equation

$$\sigma(R) = r_{b'} + R_s + R_e \quad (5-21)$$

In these equations, if R_e is large compared to the balance of $\sigma(R)$, or $R_e > r_{b'} + R_s$, then the two frequencies for the two knees are about equal, and a flat frequency response can be obtained, but otherwise an equalizing circuit will be required to compensate for the roll-off between ω_a and ω_b .

EXAMPLE 5-6. Determine the characteristics of an emitter-follower using a type GT 761 PNP transistor. Take the supply voltage as 6 V, the value of R_e (or R_L) as 1200 ohms. Assume that the value of the base-spreading resistance is 75 ohms.

The reference load line may first be plotted as shown in Fig. 5-11 and the corrected load contour plotted from it. It is not necessary to read the values of the voltage correction from the input family as was required with the common-base amplifier, since the change in collector voltage is produced solely by the base-current flow. After the corrections are made and the corrected contour is plotted, it may be transcribed to the input curve family in the usual manner. Then the small-signal data and such static data as are required are listed in Table 5-14.

The values of g_o and g_e for this transistor are very nearly the same, indicating that the feedback conductance is extremely small. The very small value of base-spreading resistance also is indicative of an excellent input characteristic.

The amplification and the input and output admittances of the common-collector amplifier are calculated by the use of Eqs. 4-32, 4-33, and 4-34. The resulting data are given in Table 5-15.

Several things of interest can be noted from Table 5-15. The first is that whereas the amplification with zero source impedance ($R_s = 0$) rises with base current, the amplification decreases for the remaining co-

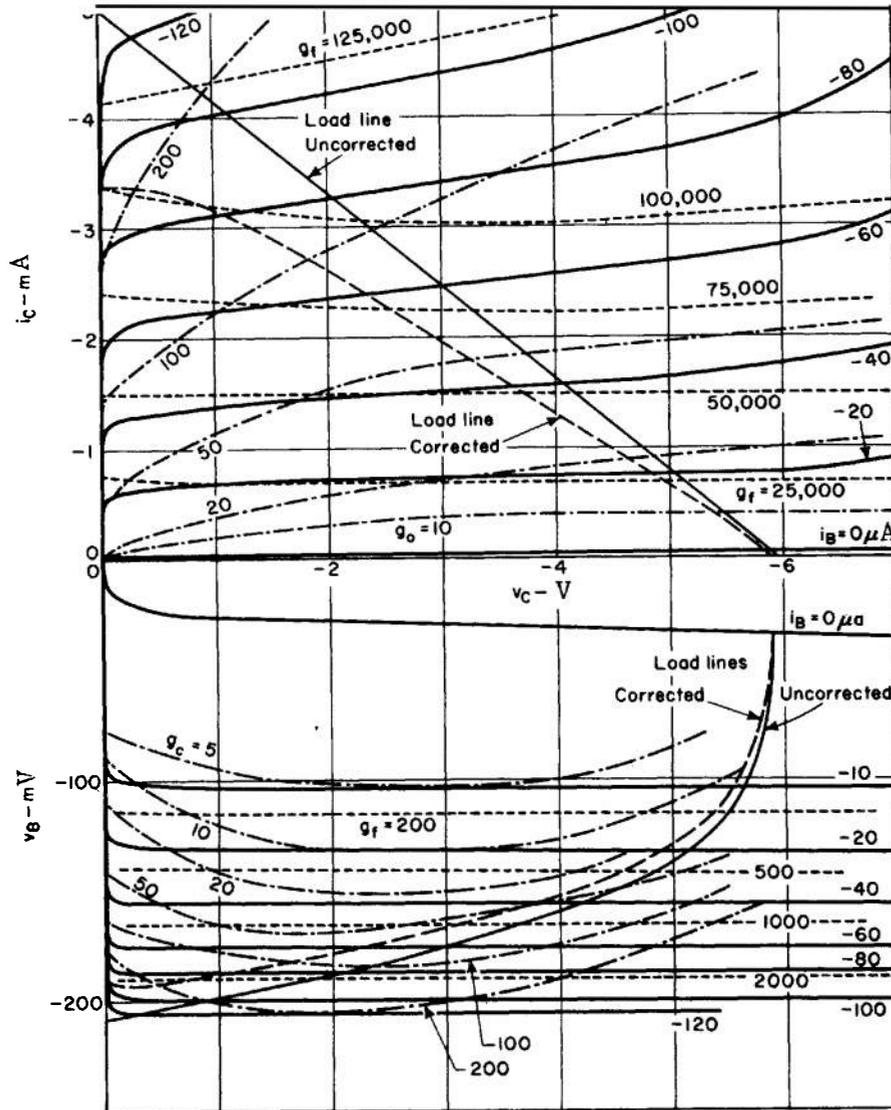


Fig. 5-11. Emitter-follower Load Line for Example 5-6. $R_e = 1200\Omega$

TABLE 5-14
DATA FOR COMMON-COLLECTOR AMPLIFIER

I_b pa	V_c volts	I_c ma	g_i pmho	g_f pmho	g_i' pmho	g_f' pmho	g_o pmho	g_e pmho
20	4.98	0.80	370	27,000	380	27,700	17	20
40	4.04	1.59	800	53,000	852	56,400	43	49
60	2.96	2.47	1600	83,000	1818	94,600	80	100
80	1.92	3.30	1940	103,000	2250	119,400	130	130
100	1.00	4.03	2200	119,000	2630	142,500	195	190

TABLE 5-15
SMALL-SIGNAL BEHAVIOR FOR COMMON-COLLECTOR AMPLIFIER

I_b μa	K_o	$K_{10\text{ K}}$	$K_{20\text{ K}}$	$K_{50\text{ K}}$	$K_{100\text{ K}}$	Y_i μmho	$Y_{o\text{ min}}$ $micromhos$	$Y_{o\text{ max}}$
20	0.972	0.873	0.794	0.622	0.458	10.9	28,080	6010
40	0.985	0.873	0.784	0.598	0.430	12.2	57,250	6460
60	0.992	0.845	0.736	0.530	0.361	15.6	96,420	5970
80	0.994	0.844	0.734	0.527	0.357	15.3	121,600	6420
100	0.994	0.840	0.727	0.518	0.350	15.0	145,100	7150

TABLE 5-16
IMPEDANCE VARIATION—EMITTER-FOLLOWER

R_s , ohms	Zero	4,000	10,000	20,000	50,000	100,000
Y_o , micromhos	145,100	71,800	41,400	24,800	12,000	7,150

lumps. This indicates that for an intermediate value of R_s , it should be possible to obtain a relatively constant value of amplification. In fact, if the value of R_s is set at 4000 ohms, the amplifications are 0.930, 0.938, 0.928, 0.929, and 0.927, values which for all practical purposes are identical.

In addition, the input admittance that is available with the circuit is rather lower than might have been expected, in that it is equivalent to 60,000 to 100,000 ohms. Such a circuit has the characteristics that are required with signal repeater circuits. The output admittance, however, which is very high for values of R_s near zero, is relatively small for the higher input resistances. It is actually quite stable, as is the input admittance, corresponding to about 175 ohms compared to the 8 to 30 when the value of R_s is nearly zero.

It is of interest to see just how the output admittance of the amplifier varies with variation of the value of R_s . The data required are given in Table 5-16, and the result is plotted in Fig. 5-12.

These data are tabulated for a base current of 100 μA .

It is clearly evident that if the lowest possible output impedance, or highest admittance, is required with a very low source admittance, it is necessary to cascade emitter-followers. For example, using two of the circuits in cascade yields a source admittance of about 15 micromhos, and, even when used with a source resistance of 100,000 ohms, may be expected to develop an output admittance of several hundredths of a mho. It is important that a separate emitter load resistance be used with the input emitter-follower if full advantage of the transforming action is required.

The distortion developed in emitter-follower amplifiers is extremely small, but because the amplifier requires a drive signal equal to the output, the low-distortion feature is at least somewhat illusory. In addition, the distortion is very strongly dependent on the magnitude of the load admittance because the voltage developed across the admittance is re-introduced into the input circuit to help provide the stabilization. For these reasons, even more than ordinary care must be used in the design of routine emitter-followers.

The frequency response that may be obtained with the amplifier whose design is developed above may be obtained from the equations for response derived previously. Because the value of the α -cutoff frequency for the GT-761 is listed as 10 MHz, a nominal average value for C_i may be calculated. If the average value for g_i' is taken as 80,000 $pmhos$, then the value of capacitance is 0.0013 μF . For a value of R_s , negligible compared to that for R_e , and $g_i' R_e \gg 1$, the frequencies ω_b and ω_d are nearly equal, and the response is uniform to a frequency at which the simple representation for the device is inadequate. For a source resistance equal to the load resistance R_e , then the frequency ω_d is half ω_b , and 6 dB loss occurs in the transition range. For values of R_s such that $R_s \gg R_e$, then the frequency ω_d is approximately equal to the β -cutoff frequency.

5-7 EMITTER-DEGENERATIVE AMPLIFIERS

The use of some emitter degeneration in an amplifier can often improve both its static operating characteris-

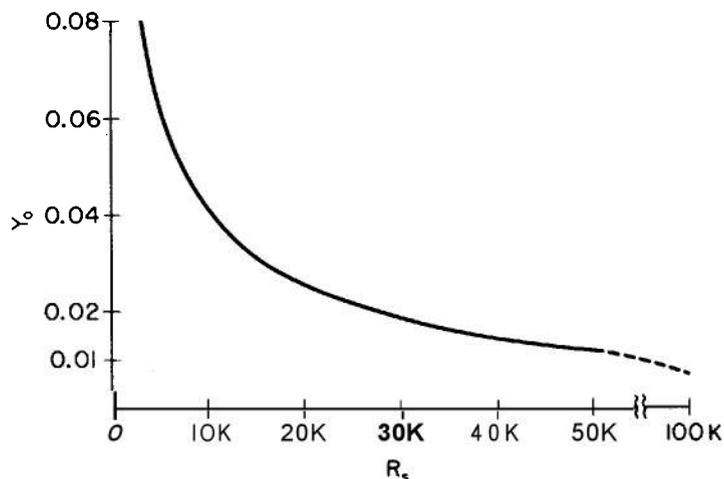


Fig. 5-12. Output Admittance as a Function of R_s for Example 5-6

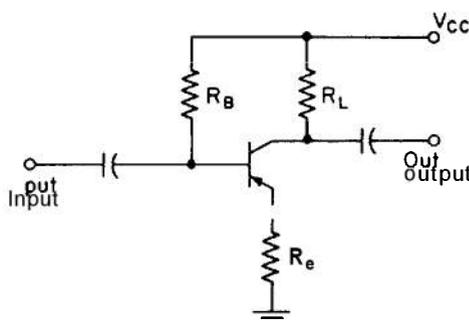


Fig. 5-13. Emitter-degenerative Amplifier

tics and its small-signal characteristics, Fig. 5-13. The use of DC emitter stabilization in fixing the static behavior is discussed in the next chapter, and the design of amplifiers with emitter stabilization of the small-signal characteristics is discussed in the next few paragraphs.

The load line for the degenerative amplifier is plotted in almost exactly the same way as that for the ordinary common-emitter amplifier. Although strictly there is a small correction required for base current, the position of the load line is usually changed but very little compared to its position for the simpler amplifier. After the load line is drawn, the static and the small-signal data are tabulated and the values of y_i and y_f are converted into the corresponding values for y_i' and y_f' . Once the data are tabulated and converted, then the small-signal characteristics, amplification, and input and output admittance, may be calculated. The amplification of the amplifier is

$$K_a = - (y_{f'} - y_i' y_c R_e) R_L / [1 + y_o R_L + \sigma(y') R_e + y_i' (r_{b'} + R_s) [1 + y_c (R_e + R_L)] + y_i' y_c R_e R_L] \quad (5-22)$$

The value of $\sigma(y') R_e$ may be small or it may be large, depending on the value of R_e selected for use. Because the value of $\sigma(y')$ is approximately equal to $y_{f'}$, the amplification can be determined almost completely by the ratio of R_L/R_e if the value of R_e selected is such that the denominator may be reduced to approximately $\sigma(y') R_e$. This requires that the remaining terms of the denominator sum to a value just a little greater than unity, and the $\sigma(y') R_e$ term be at least 10. Then the amplification equation takes the form

$$K_a = - y_{f'} R_L / [1 + \sigma(y') R_e] \doteq - R_L / R_e \quad (5-23)$$

The input admittance Y_{id} of the degenerative amplifier is appreciably smaller than that for the ordinary amplifier as a consequence of the $\sigma(y') R_e$ term in the denominator. The approximate ratio of the input admittance for the conventional amplifier to that for the degenerative amplifier is given by the equation

$$Y_{id} / Y_{ids} \doteq 1 + [\sigma(y') R_e + y_i' y_c R_e \sigma R] / [1 + y_o R_L + y_i' (r_{b'} + R_s) (1 + y_c R_L)] \quad (5-24)$$

where σR is defined as $\sigma R = (r_{b'} + R_s + R_L)$ and Y_{ids} is

$$Y_{id} = y_i' [1 + y_c(R_e + R_L)] / [1 + y_o R_L + y_i'(r_b' + R_s) + \sigma(y')R_e + y_i'y_c(\sigma R R_e + R_L(r_b' + R_s))] \quad (5-25)$$

In these equations, the corresponding forms at the transistor terminals, Y_{id} , and Y_i/Y_{id} , may be obtained by letting R_s be zero. Also, the value of R_r may be assumed to be small compared to R_L unless an extremely large amount of degeneration is required. The denominator of the quotient on the right-hand side of Eq. 5-24 normally has a value of approximately unity, in which case Eq. 5-24 may be reduced to the simplified form

$$Y_i/Y_{id} \doteq 1 + \sigma(y')R_e \quad (5-26)$$

The value obtained from Eq. 5-26 is within a factor of two of the correct value even with large values of r_b' .

The output admittance of the degenerative amplifier is also decreased as a result of the emitter degeneration. The ratio of the output admittances for the two conditions is given by the equation

$$Y_o/Y_{od} \doteq [(R_s + r_b')/\sigma R][1 + \langle \sigma(y')R_e + y_i'y_c R_e R_L \rangle / \langle 1 + y_o R_L + y_i'(r_b' + R_s) + \sigma(y')R_e + y_i'y_c[(r_b' + R_s)(R_e + R_L) + R_e R_L] \rangle] \quad (5-27)$$

Neglecting R_L , as is usually done, the equation reduces to

$$Y_o/Y_{od} \doteq [(r_b' + R_s)/\sigma R][1 + \langle \sigma(y')R_e \rangle / \langle 1 + y_i'(r_b' + R_s) \rangle] \quad (5-27a)$$

where the reduced value of Y_{od} is given by the equation

$$Y_{od} = [y_o + y_i'y_c\sigma R] / [1 + y_i'(r_b' + R_s) + \sigma(y')R_e + y_i'y_c(r_b' + R_s)R_e] \quad (5-28)$$

The value of $(r_b' + R_s)/\sigma(R)$ is normally rather close

to unity, with the result that the ratio is largely determined by the value of the $\sigma(y')R_e$ term. The overall value may be as large as from 10 to 50, depending on the amount of degeneration used.

Because the degenerated value of output admittance is so small, the effective admittance of the stage as a whole is dependent primarily on the value of R_L , which has been selected for use. In all but the common-collector amplifier, among the simple structures, the total admittance is almost completely dependent on the loading of the output circuit itself.

EXAMPLE 5-7. Design a degenerative amplifier using the HA 5003 transistor with a collector supply voltage of 20 V and a load impedance of 2000 ohms. Take $f_a = 1.5$ MHz. Select a value of R_e that can limit the overall amplification of the circuit to 0.2 of its nominal value determined from $y_f'R_L$.

The load lines may be plotted as shown in Fig. 5-2. The approximate base-spreading resistance is 360 ohms, as calculated from the values of forward conductance and input conductance. If the base bias current of 40 μ A is selected for the calculation of the degeneration factor, then $\sigma(y')R_e = 4$, giving a value of R_e of approximately 17 ohms. The error in the collector voltage due to base current may now be calculated; because the base current is a maximum of approximately 60 μ A, an error of 0.001 V is introduced, a negligible amount.

Once the suitability of the basic load line has been established, then the data may be tabulated for the calculation of the operating behavior of the transistor. The small-signal data are given in Table 5-17.

In this problem, the largest value of y_f has been calculated back from y_f' which has been estimated from the collector current and the value of the base-spreading resistance. The technique is described in Chapter 4.

The values of the amplification and the input and output admittance may be calculated from the data in Table 5-17. For this calculation, the values of R_e of 0, 500, 2000, and 10,000 ohms may be used.

These data show that the relative input admittance is still rather large, although it has been appreciably decreased by the degeneration. Because the maximum output admittance listed in Table 5-17 is less than 200 pmhos, the total admittance, combining the 500 pmhos for the 2000-ohm load and the output admit-

tance for the transistor, is less than 700 pmhos or more than 1400 ohms.

The amount of distortion that results in this circuit can be calculated by either the use of the distortion equations or by orthogonal techniques from the amplification data in Table 5-18. Because the procedures are the same as those used in previous examples, they will not be repeated here.

The frequency response may be determined by substituting $g_{i'} + j\omega C_i$ for $y_{i'}$ and evaluating the relative magnitudes of the frequency-independent and the frequency-dependent terms. If the $y_{i'}y_c$ terms in the numerator are neglected, and the denominator is solved for frequency, the resulting equation is

$$\omega = [1 + g_o R_L + (g_{i'} + g_{f'})R_e + g_{i'}(r_{b'} + R_s)]/[C_i \sigma R] \tag{5-29}$$

If the value of R_s is small, then this equation may be simplified to the form

$$\omega = [1 + g_o R_L + (g_{i'} + g_{f'})R_e]/[C_i(r_{b'} + R_s)] \tag{5-30}$$

This frequency is nearly equal to the α -cutoff frequency if $R_e > (r_{b'} + R_s)$, and otherwise is between the α - and β -cutoff frequencies. The value of ω may be calculated with the help of the nomograph in Fig. 5-7.

5-8 ANOTHER FEEDBACK AMPLIFIER

Another form of feedback amplifier may be constructed using collector-to-base feedback (Fig. 5-15). This arrangement stabilizes the amplification of the circuit, and also increases its input admittance. There is one special problem to solve with this amplifier, namely, taking proper account of the feedback resistor Y in the static design.

This feedback element introduces a shunt load resistance from collector to base, a voltage usually somewhat above ground potential, and as a result it introduces a

small alteration in the effective supply voltage for the amplifier. The current drawn by the feedback resistor normally is negligible in comparison to the load drawn by the transistor. Otherwise, the correction process becomes rather complex, as both voltage and current corrections are required.

The feedback current introduced into the base lead of the transistor is in phase-opposition to the input current introduced into the transistor, thereby decreasing the overall current gain. This current flow does not affect the position of the load contour significantly, however, but it reduces the signal current available for the base of the transistor. The amplification equations automatically take this division into account. The equations are

$$K = -[y_{f'} - Y(1 - y_{i'}r_{b'})]R_L/[1 + YR_s + y_{i'}(r_{b'} + R_s) \times (1 + y_c R_L + YR_L) + y_o R_L + \sigma(y')R_s YR_L] \tag{5-31}$$

The input and output admittances are defined by the equations

$$Y_i = [y_{i'}(1 + Yr_{b'}) + y_{i'}y_c R_L(1 + Yr_{b'}) + \sigma(y')YR_L]/[1 + y_o R_L + y_{i'}r_{b'}(1 + y_c R_L + YR_L)] \tag{5-32}$$

$$Y_o = [y_o(1 + YR_s) + y_{i'}y_c(r_{b'} + R_s) + Y(1 + y_{i'}r_{b'})]/[1 + y_{i'}(r_{b'} + R_s) + YR_s] \tag{5-33}$$

EXAMPLE 5-8. Design an amplifier using a collector-to-base feedback circuit. Select a value of Y such that the gain is reduced to 0.2 of the undegenerated value. Use an HA 5003 transistor with a collector supply voltage of 20 V, a load impedance of 2000 ohms, and f_a of 1.5 MHz.

TABLE 5-17
DATA FOR EMITTER-DEGENERATIVE AMPLIFIER

I_b μa	I_c ma	y_i $pmho$	y_f $pmho$	y_o $pmho$	y_c $pmho$	$y_{i'}$ $pmho$	$y_{f'}$ $pmho$	V_c
0	1.4	0	0	0	0	0	0	17
20	4.36	670	115,000	43	130	881	151,300	11
40	6.8	1050	150,000	85	190	1688	241,100	6.2
60	8.6	1500	148,500	200	380	3260	301,000	2.7

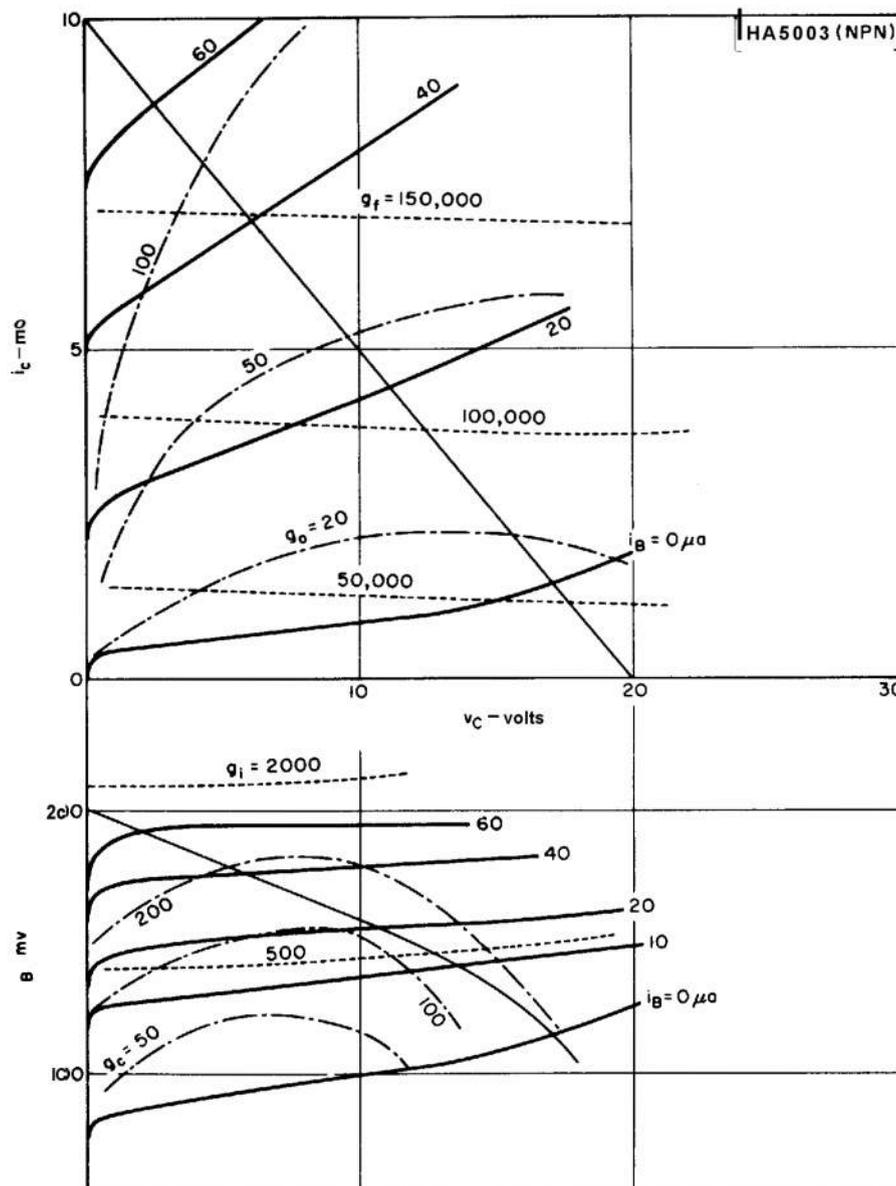


Fig. 5-14. Load Lines for Degenerative Amplifier HA 5003 (NPN) for Example 5-7

TABLE 5-18
EQUIVALENT CIRCUIT PARAMETERS

I_b	K_0	K_{500}	K_{2000}	$K_{10,000}$	Y_{id}	Y_{odo}	Y_{od50}
20	-74.0	-65.4	-48.0	-19.9	273	21.2	80.8
40	-78.6	-67.8	-44.7	-16.3	379	33.6	115.8
60	-69.7	-52.3	-29.9	-9.1	664	77.2	198

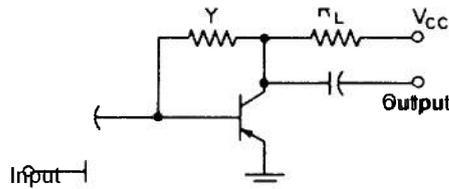


Fig. 5-15. Feedback Amplifier—Type II

As in Example 5-7, the first step is to determine the value of Y required by the use of the equation

$$\sigma(y')R_s Y R_L = 4 \quad (5-39)$$

with $R_s = 500, 2000,$ and $10,000$ ohms. Then the correction voltage required to compensate for the feedback network may be determined and the correction introduced into the circuit. Finally, the amplification and driving-point admittances may be calculated in the usual way. Because a typical value of $\sigma(y')$ is 0.1, the value of Y , with $R_s = 500$, is approximately 25,000 ohms (40 pmhos).

5-9 SUMMARY

Comparison of the various amplifier designs described in this chapter shows the differences in operating characteristics and indicates the areas of application for each. Factors which affect the selection of configuration include power gain, current gain, frequency characteristics, and distortion.

The common-emitter configuration is normally used because it has a relatively high input impedance and large current, voltage, and power gains. The high value of gain can be obtained for low-frequency signals, but the bandwidth available is considerably less than for the other configurations. Distortion is large but can be controlled by degeneration.

The common-base amplifier has a very low input impedance, and a current gain slightly less than unity. This configuration has a bandwidth approximately equal to that of the common-emitter amplifier with a low-impedance source and a maximum bandwidth equal to the α -cutoff frequency with a high-impedance source. It must be used with some form of transformer as an interstage device if an overall power gain is to result in cascaded common-base amplifiers. The use of the common-base configuration minimizes feedback from output to input and, as a result, simplifies the design of high-frequency amplifier cascades.

The common-collector amplifier has a high input impedance, possibly many times that for the common-emitter configuration, and a comparatively high output admittance also. Because the output signal developed is re-introduced into the input, the distortion in this amplifier is extremely small. The current gain is large compared to unity, but the voltage gain is slightly less than unity.

The emitter-degenerated amplifier combines some of the properties of the common-emitter and the common-collector amplifiers, using the emitter resistance to improve the input characteristics and to reduce the overall distortion. This circuit trades gain for reduced distortion and increased input impedance.

The common-collector amplifier can be used to provide input signal to a common-base or a common-emitter amplifier, giving in the former the transistor equivalent of the cathode-coupled amplifier and in the latter a follower-isolation amplifier. In these arrangements, the common-collector amplifier functions as a coupling transformer.

The shunt-feedback amplifier, with an impedance connected from its collector to its base, has a very low input impedance and uses current feedback instead of voltage as is the case with the emitter-degenerated form. This arrangement is used with very low impedance-signal sources or applications in which current-source operation is required with very small values of input impedance.

REFERENCE

1. K. A. Pullen, Jr., *Conductance Design of Active Circuits*, John F. Rider Publisher, Inc., New York, 1959.

CHAPTER 6

CIRCUIT STABILIZATION

6-0 INTRODUCTION

One of the major problems in the use of transistor circuits is the stabilization of operating conditions so that the circuit can give the required performance over an adequate range of environmental conditions.

6-1 THERMAL FACTORS

There are two principal thermal factors that affect the stability of transistor circuits, and others of lesser importance. The first of these thermal factors is the reverse-leakage current of the collector-base junction, so-called I_{co} , and the second the variation of V_b (V_{be}) with temperature. The leakage current increases rapidly as the temperature of the transistor is increased, and limits the conditions under which the transistor can provide effective operation (Fig. 6-1). This current, in conjunction with the current gain of the transistor, limits the minimum usable current through the common-emitter amplifier, thereby restricting the available range of operation.

Strictly, it is possible to use the transistor in the common-emitter circuit with very small values of cur-

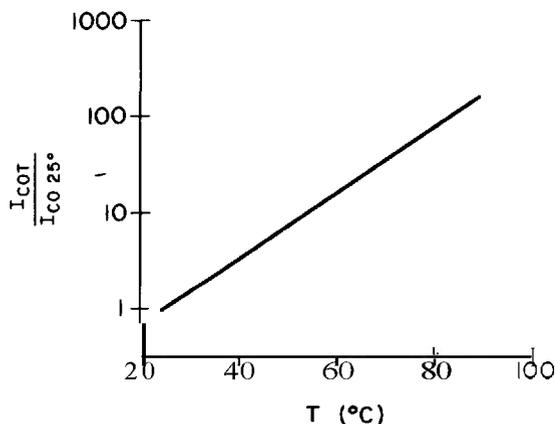


Fig. 6-1. Ratio of I_{co} at Temperature T to Value at $T = 25^\circ\text{C}$

rents, but the nonlinearity of the behavior of the device when the base current has a reverse polarity is so pronounced that it is not practical to attempt to do so. The currents in a transistor may be expressed in terms of the leakage current by the equations

$$I_B = [(1 - \alpha)I_E - I_{co}] = [y_i' I_E / (y_i' + y_f') - I_{co}] \quad (6-1)$$

$$I_C = \alpha I_E + I_{co} = [y_f' I_E / (y_i' + y_f') + I_{co}] \quad (6-2)$$

Solving Eq. 6-2 for I_E gives

$$I_E = (I_C - I_{co}) / \alpha = (y_i' + y_f')(I_C - I_{co}) / y_f' \quad (6-3)$$

These equations may be converted into any alternate form that might prove useful.

The variation of the base-to-emitter voltage with temperature for fixed magnitudes of base and emitter current is the second important thermal property of a transistor requiring compensation. The voltage between base and emitter affects the static operation of the transistor, and it also affects the small-signal operation. Because the static, or Q-point for the transistor varies rapidly with temperature if the base voltage is fixed, it is necessary to fix the Q-point in a way to assure that a full range of operating conditions are available over the required range of operating temperature. The static stability must be determined in terms of the practical circuit in use, and the circuit must be designed to provide the required stability.

The factors controlling the stability of a transistor circuit may be readily derived in terms of the circuit shown in Fig. 6-2. This circuit is the general bias circuit, and it can be readily converted into any of the three basic bias circuits (Ref. 1). By taking R_E equal to zero, and R_B infinite, the circuit reduces to the unstabilized form, and by taking $R_{c1} = 0$, it gives the simple feedback stabilizer.

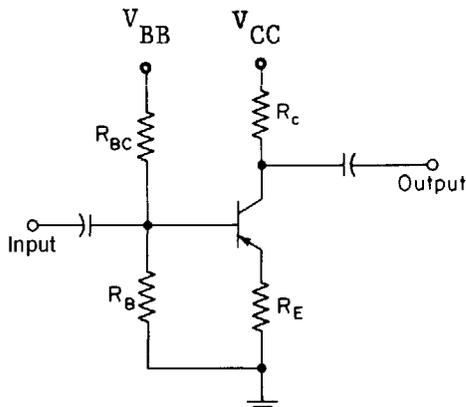


Fig. 6-2. Basic Stabilizing Circuit

The analysis of the bias circuit may be performed topologically, or it may be performed in terms of the equations

$$0 = i_f R_{BC} + i_b r_{b'} + i_e R_B + v_{b'e} \quad (6-4)$$

$$V_{BB} = - (i_f - i_b) R_B + i_b r_{b'} + i_e R_E = v_{b'e} \quad (6-5)$$

$$i_b = (1 - \alpha) i_e - I_{co} = y_i' i_e / (y_i' + y_f') - I_{co} \quad (6-6)$$

$$i_c = \alpha i_e + I_{co} = y_f' i_e / (y_i' + y_f') + I_{co} \quad (6-7)$$

Eqs. 6-6 and 6-7 are given in two forms. The first of the forms may be used with static calculations, and the second with small-signal calculations. In the latter form, they may be used extensively in basic small-signal derivations, but the value of I_{co} , being essentially constant, is neglected.

Eqs. 6-4 through 6-7 may be solved for the emitter current in terms of the base voltage and the leakage current to give

$$i_e = \frac{\{ [R_b R_{bc} + r_{b'} (R_b + R_{bc} + R_{c2})] I_{co} + (R_b + R_{bc} + R_{c2}) v_{b'} \}}{\{ (1 - \alpha) [R_b R_{bc} + r_{b'} (R_b + R_{bc} + R_{c2})] + R_b R_{c2} + R_b R_e + R_{bc} R_e + R_{c2} R_e \}} \quad (6-8)$$

Taking the partial derivatives first with respect to I_{co} and then with respect to $v_{b'}$ gives the following slopes

$$S_e = \partial i_e / \partial I_{co} = [R_b R_{bc} + r_{b'} (R_b + R_{bc} + R_{c2})] / [D] \quad (6-9)$$

where

$$[D] = \{ (1 - \alpha) [R_b R_{bc} + r_{b'} (R_b + R_{bc} + R_{c2})] + R_b R_{c2} + R_b R_e + R_{bc} R_e + R_{c2} R_e \}$$

$$S_{e'} = \partial i_e / \partial v_{b'} = (R_b + R_{bc} + R_{c2}) / [D] \quad (6-10)$$

Substituting $\alpha = y_f' / (y_i' + y_f')$ in these expressions gives the small-signal form

$$\partial i_e / \partial I_{co} = (y_i' + y_f') [R_b R_{bc} + r_{b'} (R_b + R_{bc} + R_{c2})] / [D'] \quad (6-9a)$$

$$[D'] = \{ y_i' [R_b R_{bc} + r_{b'} (R_b + R_{bc} + R_{c2})] + [R_b R_{c2} + R_b R_e + R_{bc} R_e + R_{c2} R_e] (y_i' + y_f') \}$$

$$S_{e'} = \partial i_e / \partial v_{b'} = (y_i' + y_f') (R_b + R_{bc} + R_{c2}) / [D'] \quad (6-10a)$$

These equations may be modified to give the change in the signal or active collector current by replacing the numerator $(y_i' + y_f')$ by (y_f')

$$S_{c1} = \partial i_c / \partial I_{co} = y_f' [R_b R_{bc} + r_{b'} (R_b + R_{bc} + R_{c2})] / [D'] \quad (6-11)$$

$$S_{c1'} = \partial i_c / \partial v_{b'} = y_f' (R_b + R_{bc} + R_{c2}) / [D'] = \beta S_{e'} \quad (6-12)$$

Because the information often required of the partial derivative with respect to I_{co} is the effective current gain, Eq. 6-11 may be converted into the form*

$$S_{c1} = \beta / \{ 1 + (1 + \beta) (R_b R_e + R_b R_{c2} + R_e R_{c2} + R_{bc} R_e) / (R_b R_{bc} + r_{b'} (R_b + R_{bc} + R_{c2})) \} \quad (6-13)$$

For $R_e = 0$ and R_b infinite, this equation reduces to

*Since this is a static analysis, α and β may be used.

$$S_{c1} = \beta/[1 + (1 + \beta)R_{c2}/(R_{bc} + r_{b'})] \quad (6-14)$$

Evidently, R_{c1} does not enter into the stabilization of the emitter or the collector current, although it will enter into the stabilization of the collector voltage through the product $i_c R_{c1}$.

Similarly, with $R_{c2} = 0$, Eq. 6-13 reduces to

$$S_{c1} = \beta/[1 + (1 + \beta)(R_b R_e + R_{bc} R_e)/ (R_b R_{bc} + r_{b'}(R_b + R_{bc}))] \quad (6-15)$$

Clearly, the emitter resistance is an important factor in this configuration, as the partial derivative decreases rapidly for increasing values of R_e . Because the change in collector current in these equations is the change in the active component, to obtain the total current change it is necessary to add unity (to add I_{co}) to S_{c1} to get S_{c1}' . The remaining stability factors that on occasion may be used are all directly derivable from S_e , S_e' , S_{c1} , and S_{c1}' . These four are normally the only ones required in circuit design.

The problem in stabilizing a transistor circuit is one of reducing the numerical value of the stability factor to the point where variations introduced by either $v_{b'}$ or I_{co} are small enough to permit adequate operation of the stage. In fact, the two stability factors are related by the equations

$$S_{c1}' = S_{c1}/[r_{b'} + R_b R_{bc}/(R_b + R_{bc} + R_{c2})] \quad (6-16)$$

or

$$S_{e'} = S_e/[r_{b'} + R_b R_{bc}/(R_b + R_{bc} + R_{c2})] \quad (6-17)$$

These equations indicate that operating stability in terms of the base voltage (internal) is improved by an increase in the value of $r_{b'}$. This is readily provided by inserting an external resistance in the base lead in series with $r_{b'}$. Such a circuit modification does not affect the current gain of the amplifier, but it may reduce the voltage gain.

*These derivations parallel those in *Junction Transistor Electronics*, by R. B. Hurley, John Wiley & Sons, Inc., New York, 1959.

EXAMPLE 6-1. Determine the stability factors to the collector current for a transistor having a current gain β of 100, a value of $r_{b'}$ of 500 ohms, $R_{c2} = 5000$ ohms, I_{cq} ($= I_C$) = 1.0 mA, R_e suitable for the required collector current with $V_{cc} = 10$ V. Then introduce 3 V of emitter degeneration, and redetermine the stability factors.

For the first condition, the voltage across R_{bc} is 5 V, and R_{bc} has a value of 500,000 ohms. An open circuit exists in the R_b position. In this configuration the maximum value of S_{c1} (minimum stability) is obtained when not R_{c2} but R_{c1} is 5000 ohms. The corresponding value of S_{c1} is exactly equal to the β of the transistor, or 100. If, however, R_{c2} is 5000 ohms and R_{bc} 500,000 ohms, the value of S_{c1} then is 49.7, giving a substantial improvement in stability.

The value of R_e must be 3000 ohms for 3 V of degeneration to be developed in the emitter circuit. Since approximately $10 \mu\text{A}$ of current must flow in the base lead itself, the current flow in the divider chain, $R_b - R_{bc} - R_{c2}$, designated i_f , should be greater than twice the base current, or between 30 and $50 \mu\text{A}$. Taking i_f as $50 \mu\text{A}$, then the values of R_b and R_{bc} are approximately 75,000 and 40,000 ohms, respectively. The overall stability factor S_{c1} with this arrangement is $S_{c1} = 4.93$. This means that a change in the leakage current in the base of the transistor is accompanied by a total collector-current change of only $(1 + S_{c1})I_{co}$ or $59.3 \mu\text{A}$ instead of the 1 mA change in the uncompensated arrangement.

In the process of introduction of the stabilization, the voltage and current gains for the transistor have been degraded. The input conductance of the transistor, correcting for degeneration, may be as small as 3.3 pmhos, and it has a conductance of approximately 50 pmhos in parallel with it, giving a net current gain of possibly 5. If, however, the resistor R_e is bypassed for signal-frequency currents, then only the feedback from the collector to the base degrades the current gain, and then only if the load resistance is placed at R_{c2} rather than R_e . The input conductance of the transistor itself is 400 pmhos (2500 ohms), and the voltage gain, assuming a low-impedance signal source, is 200. (For the source impedance to be low, the loading effects of R_{bc} and R_b on the source voltage must be negligible.)

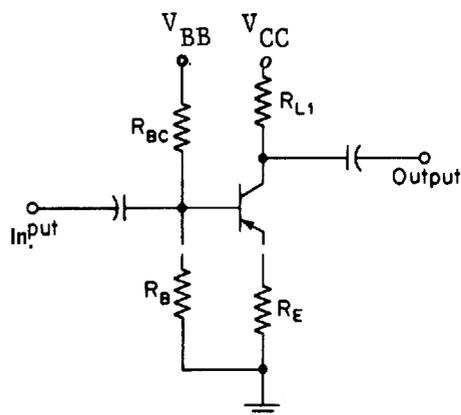


Fig. 6-3. Reduced Stabilizing Circuit

This means that the apparent value of the resistance of R_E will be decreased by a factor of 201, to approximately 225 ohms. The current gain of the amplifier is also reduced by this feedback, the final value being approximately 8.25. The overall voltage gain will also deteriorate if the signal source has appreciable impedance.

Returning the feedback resistor to R_{c2} instead of to the collector supply has severely deteriorated the characteristics of the amplifier, and has not introduced any noteworthy compensating advantages. If R_{c2} is reduced to zero, and the value of R_E made 5000 ohms, and the value of R_E readjusted accordingly, this loading does not occur, and the stability is reduced very slightly. The new value of S_{c1} is 5.05, or negligibly poorer than the previous best value of 4.93. The new value for R_{bc} is 140,000 ohms, and the equivalent parallel resistance for R_E and R_E is 49,000 ohms, or almost an open circuit in comparison with the input conductance of the transistor.

With the modified configuration having $R_{c2} = 0$ and $R_E = 5000$ ohms, the emitter resistor may be unbypassed, or a portion of it may be unbypassed, if an increase of input resistance (decrease of input conductance) is desired. The final circuit, using a combination of voltage and current stabilization on the base and emitter, is shown in Fig. 6-3.

The value of the rate of change of collector current with base voltage may also be calculated. For the simple circuit, with R_E infinite, and with collector feedback, the value of S_{c1} is 0.0002. Using the fully compensated design gives new value of S_{c1} of 0.00014, or only a small improvement. The simplest form for use of the equation for S_{c1} is

$$S_{c1} = \beta / [R_{eq} + r_{b'} + (\beta + 1)(R_E + R_{eq}R_{c2}/R_{bc})] \tag{6-18}$$

where $R_{eq} = R_b R_{bc} / (R_b + R_{bc})$. The objective is to reduce the value of S_{c1} , an operation that can be accomplished either by reduction of the numerator or by increase in the value of the denominator. Evidently, little can be done with the numerator. In the denominator, the first term may be small compared to the second. The last two terms may be simplified to read

$$\langle R_{c2}R_b / (R_b + R_{bc}) \rangle + R_E \tag{6-19}$$

where the value of R_{c2} should be small if a low input admittance is desired. The value of $R_b / (R_b + R_{bc})$ is less than unity, and R_b is roughly proportional to R_E . The final approximating equation then reduces to

$$S_{c1} \doteq A / R_E \tag{6-20}$$

where A is an arbitrary constant. Its value will be between 0.1 and 10.

6-2 DYNAMIC STABILITY

The variation of the base-to-emitter voltage also influences the values of some of the small-signal parameters for a transistor. In particular, the magnitudes of $r_{b'}$, $y_{i'}$, and $y_{f'}$ are strong functions of the operating temperature of the device. The forward conductance of a transistor has a dependence on temperature expressed by the equation

$$y_{f'} = y_{f'o} (T/T_o)^{-1} \tag{6-21}$$

It is accompanied by changes in the base-spreading resistance $r_{b'}$ and input admittance $y_{i'}$ in terms of the equations

$$r_{b'} = r_{b'o} (T/T_o)^{2.3} \quad y_{i'} = y_{i'o} (T/T_o)^{-3.2} \tag{6-22}$$

where the subscript o refers to the reference temperature, and its absence to the altered temperature (Ref. 2).

The effective forward admittance (transconductance) for the common-emitter amplifier is defined by the equation

$$Y_f = y_{f'}/[1 + y_{i'}(R_s + R_e + r_{b'}) + y_{f'}R_e + y_oR_L + y_{i'}y_c(R_s + r_{b'})(R_e + R_L) + R_eR_L] \quad (6-23)$$

Assuming that the terms involving y_o and y_c may be neglected, this equation reduces to

$$Y_f = y_{f'}/[1 + y_{i'}(R_s + R_e + r_{b'}) + y_{f'}R_e] \quad (6-24)$$

and the admittances may be replaced with conductances if desired. Taking the logarithmic derivative, and equating to zero gives the required value of R_s for stabilization of the effective forward admittance

$$R_s = -R_e + 1/2.2y_{i'} \quad (6-25)$$

These equations assume that the DC operating point for the transistor is stabilized in accordance with the method described. If then the total input admittance for an amplifier is calculated based on these relations, its value as a function of temperature, neglecting the effect of the output circuit, is given by

$$Y_i = y_{i'}(T/T_o)^{-3.2}/[1 + r_{b'o}y_{i'o'}(T/T_o)^{-0.9}] \quad (6-26)$$

Evidently, the input admittance varies rapidly with the absolute temperature T .

6-3 CONTROL OF THERMAL RUNAWAY

Thermal runaway may develop in a transistor if an increase in transistor temperature is accompanied by a significant increase in its power dissipation. Because the temperature rise of the transistor is a function of the power dissipated and of the thermal resistance in degrees per watt, the increase in dissipation per unit temperature change must be greater than the dissipation required to cause the unit temperature change if thermal runaway is to result.

The first question in the determination of conditions for thermal runaway is to determine the conditions under which maximum dissipation occurs, and also the

conditions under which dissipation rises and decreases with change of collector current. Writing the equation for the collector dissipation in terms of the collector current, and differentiating, gives the relation

$$P_c = v_c i_c = i_c(V_{cc} - i_c R_L) \quad (6-27)$$

$$dP_c/di_c = V_{cc} - 2i_c R_L \quad (6-28)$$

The condition for maximum dissipation is

$$i_c = V_{cc}/(2R_L) \quad \text{or} \quad v_c = V_{cc}/2 \quad (6-29)$$

Now, taking the temperature rise as defined by the equation

$$\Delta T = C_t \Delta P_c = (V_{cc} - 2i_c R_L) \Delta i_c C_t \quad (6-30)$$

where C_t is the specific temperature change in degrees per watt, the change in collector current in Eq. 6-30 is caused by changes in the value of I_{co} as a function of temperature. The substitution

$$\Delta i_c = \beta S_c \Delta I_{co} = \beta S_c \gamma_c \Delta T \quad (6-31)$$

may be made, where γ_c is the rate of change of I_{co} with temperature. Substitution in Eq. 6-30 gives

$$k \Delta T = \beta C_t S_c \gamma_c (V_{cc} - 2i_c R_L) \Delta T \quad (6-32)$$

where k is a constant of proportionality inserted into Eq. 6-30 for convenience. When k has a value greater than or equal to unity, the circuit is thermally unstable, and when it is less than unity, it is stable. Under unstable conditions the temperature continues to rise, and unless the term $(V_{cc} - 2i_c R_L)$ decreases sufficiently to restore stability before thermal damage occurs, the transistor will destroy itself. The importance of the factor S_c , the only adjustable element in the equation

other than $i_c R_L$, is clearly apparent. The data on γ_c are often given with the data on a transistor and the value of S_c can be evaluated as described earlier. The static values of i_c and S_c must be selected to assure that stable operation will result throughout the expected temperature range.

Eq. 6-32 shows that the temperature increment will be either zero or negative, and k zero or negative, whenever the value of i_c obeys the relation

$$i_c \geq V_{cc}/(2R_L) \quad (6-33)$$

This condition can be used for the stabilization of R-Amplifiers, since the output signal voltage must be developed across a load resistance, and such a resistance can be introduced into low-power amplifiers using transformers, but not into a high-power amplifier without causing excessive circuit losses.

Power amplifiers have a particularly serious stability problem in that the bias should be provided from a constant-voltage source, one which gives a voltage bias

that is a function of junction temperature, because the source must permit the peaks of current to flow without altering the static operating point. At the same time, the static resistance in the collector and the emitter circuits must be small because of the high efficiency requirement on the amplifier.

The only way in which the collector current of a power amplifier can be regulated is to set up a metering control circuit that measures the minimum total emitter current flowing in the transistor amplifier when the signal polarity reverses. A circuit that can provide control by reducing the static base voltage for the output transistors is shown in Fig. 6-4. The diode D , is used to charge the capacitor C_s to a voltage corresponding to the static current level as determined by the emitter-degeneration resistor for the power amplifier R_e . This voltage is amplified and inverted in phase to provide the base current for the amplifier by way of the emitter-follower. The value of the degeneration resistance R_e must be sufficiently small that the minimum voltage across it is less than 0.5 V to minimize power loss and to limit the degeneration introduced by it. The emitter-follower may be used as a driver amplifier for the drive signal, as well as a dissipation-limiting amplifier.

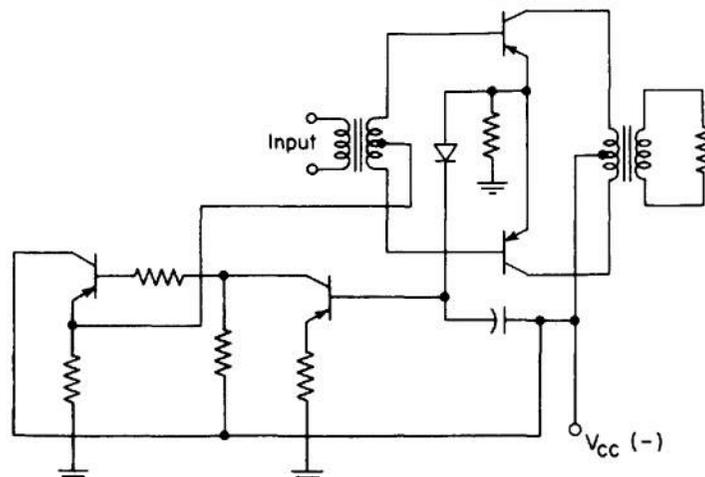


Fig. 6-4. Power Amplifier Protection Circuit

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1. H. Hellerman, A Generalized Theory of Transistor Bias Circuits, Paper 57-1023, American Institute of Electrical Engineers, New York.
2. R. A. Schmeltzer, "Stabilization of Transistor Gain Over Wide Temperature Ranges", *RCA Review*, June 1959.

CHAPTER 7

TRANSFORMER-COUPLED AMPLIFIERS

7-0 INTRODUCTION

Transformer-coupled circuits, including transistors, are used extensively because of the high current efficiency that can be obtained from them. The efficiency is much higher than with tube circuits because of the absence of heater power requirements for the transistor.

The use of coupling transformers is more important with transistor amplifiers than with tubes because of the high input admittance of the transistor. The converse admittance relation is true with tubes, so much so that in the early days of radio, matching transformers were used to compensate for low tube gains. The operating properties of the transformer-coupled tube amplifier have proved to be sufficiently inferior to the properties of resistance coupled amplifiers that the reduced power dissipation available proved to be unimportant except for power output circuits. The relatively high input admittance of the transistor and its consequent transformer loading, and the absence of heater power loss, make the power dissipation situation entirely different for the transistor amplifier. In addition, the resistive loading on the transformer reduces markedly the transformer distortion otherwise encountered.

The impedance ratio used for an interstage or an output coupling transformer must be selected in terms of the supply voltage and the available power that can be developed by the amplifier, and also in terms of the input load admittance of the load circuit. The open-circuit inductance of the output winding must be selected to give a reactance at least equal to the impedance of the load at the minimum operating frequency, and it should be several times the load impedance for best operating conditions. The turns-ratio is selected to give the correct input impedance.

Transformer-coupled amplifiers are used extensively as low-power and compact communication amplifiers, and with power output amplifiers. Transformers of the kind used in hearing aids may be able to pass a frequency band only approximately a decade wide, whereas an amplifier using larger transformers may

pass as much as two or three decades. Before the design of transformer-coupled amplifiers is considered in later paragraphs of this chapter, it is convenient and useful to examine the properties of transformers that are important in this circuit application.

The discussion of transformers can be separated into a discussion of the two basic types, namely, tightly coupled transformers, and loosely coupled. At least superficially, the behavior of both types is similar in that both have at least one resonant frequency per winding (the frequencies may coincide under certain conditions), and they may be represented in terms of either pi or tee equivalent circuits. The tee equivalent circuit has been used most commonly in representation of transformers, particularly tightly coupled units, but the pi representation has many advantages (Ref. 1). Fig. 7-1 shows that both leakage inductance values are required in each configuration. However, the significance of the leakage and mutual inductance elements is somewhat different in the two configurations. With the pi configuration, it is possible to calculate the leakage inductance from the physical configuration of the transformer, and the mutuals are related to the open-circuit inductances of the individual windings. Ref. 1 gives an excellent discussion of this configuration.

In addition to their leakage inductance, transformers also display input and output capacitance across the windings and also from winding to winding. These capacitances influence the behavior of the amplifier circuit quite markedly. The combination of the capacitances and the load resistance with the leakage inductance determines the high-frequency limitation, and the combination of the magnetizing inductances with the load resistance determines the low-frequency limitation of the circuit (Fig. 7-2). In transistor amplifiers, the interstage or output transformer is activated from a current source, and the current distributes among all of the paths as well as through the desired path, namely, R_L . The current efficiency, in terms of the network of Fig. 7-2, is given by the equation

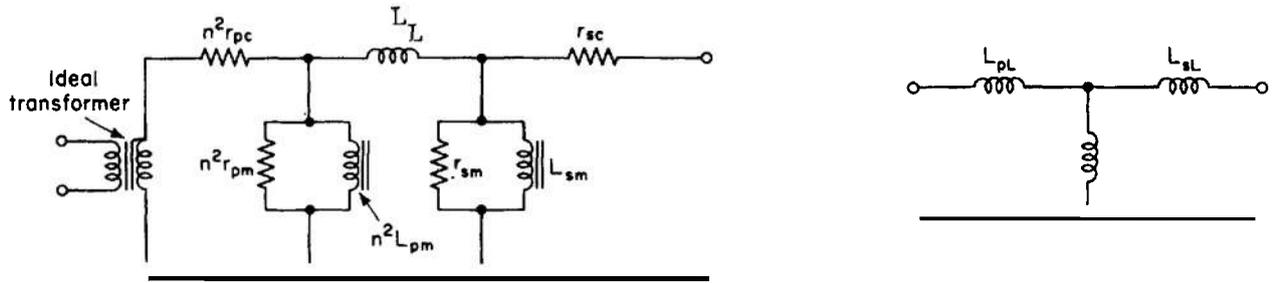


Fig. 7-1. Transformer Circuits

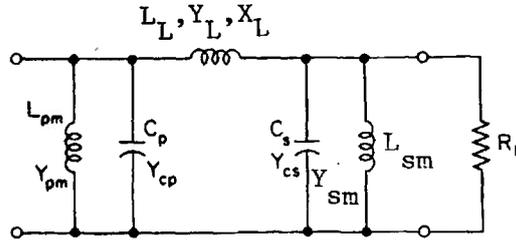


Fig. 7-2. Circuit With Capacitances (Unity Ratio)

$$i_L/i_i = 1 / \left([1 + (Y_{pm} + Y_{cp})X_L] [1 + (Y_{cs} + Y_{sm})R_L] + (Y_{pm} + Y_{cp})R_L \right) \quad (7-1)$$

The equation assumes a unity turns-ratio for the transformer. If the ratio is other than unity, the values may be scaled for the ratio. In this way, the step-up or step-down ratio in the transformer may be introduced through the use of an ideal transformer in conjunction with the associated equivalent network of Fig. 7-2.

In practical transformer-coupled amplifiers it is desirable to use a transformer whose magnetizing reactance is large compared to both the leakage reactance X_L and also with respect to

$$R_L(Y_{pm}X_L < 1; Y_{pm}R_L < 1, \text{ etc.}).$$

Then the operation of the amplifier is dependent primarily on the load termination and the capacitances. The minimum operating frequency is given by the equation

$$f_1 = R_L(L_{pm} + L_{sm}) / 2\pi L_{pm}L_{sm} \quad (7-2)$$

This equation is applied directly when the absolute minimum of size is essential. Introducing a turns-ratio $n_s/n_p = z$, this equation may be revised to read

$$f_1 = R_L(L_{pm}'z^2 + L_{sm}) / (2\pi L_{pm}'L_{sm}z^2) \quad (7-3)$$

where L_{pm}' is the actual magnetizing inductance prior to transformation to the secondary side of the transformer. In a well-designed transformer the values of $L_{pm}'z^2$ and L_{sm} are approximately equal.

For applications in which space and weight are somewhat less important, it is common practice to select a transformer that has a minimum total shunt reactance two to five times the load resistance. In this way, the low-frequency behavior of the amplifier may be considerably improved. A larger transformer having more iron and more wire of a larger diameter is required, giving improved magnetic and electrical characteristics. The leakage inductance L_L is much smaller in value, and the magnetizing inductances are larger, making the value of the current ratio given in Eq. 7-1 both closer to unity in magnitude and also unity over a much wider range of frequencies (a unity turns-ratio is assumed in this consideration).

The maximum operating frequency is dependent on the leakage inductance, the magnetizing inductances, and the input and output capacitances. The inductive

reactance of the magnetizing inductances, L_{pm} and L_{sm} , is sufficiently high in all but very marginal transformers that these factors often can be neglected as components of the high-frequency circuit. The maximum frequency is given in terms of the roots of the equation

$$\begin{aligned} s^4 L_{pm} L_{sm} L_L C_p C_s R_L &+ s^3 L_{pm} L_{sm} L_L C_p \\ &+ s^2 [L_{pm} L_{sm} C_p R_L \\ &+ L_{pm} L_{sm} C_s R_L + L_{pm} L_L C_p R_L \\ &+ L_{sm} L_L C_s R_L] \\ &+ s [L_{sm} (L_{pm} + L_L) + L_{sm} R_L \\ &+ L_{pm} R_L + L_L R_L] = 0 \end{aligned} \quad (7-4)$$

Depending on the negligible terms, several resonant frequencies may be established

$$f_{2a} = 1/2\pi R_L (C_p + C_s) \quad (7-5)$$

where

$$\begin{aligned} L_L \ll L_{pm}, L_{sm}, 4R_L^2 (C_p + C_s) \\ \ll [L_{pm} L_{sm} / (L_{pm} + L_{sm})] \end{aligned} \quad (7-5a)$$

$$f_{2a'} = [(1/L_{sm} C_s) - (1/C_s R_L)^2]^{0.5} / (2\pi)$$

where

$$\begin{aligned} L_L \ll L_{pm}, L_{sm}, 4R_L^2 (C_p + C_s) \\ \gg [L_{pm} L_{sm} / (L_{pm} + L_{sm})] \end{aligned}$$

If L_L is large compared to the magnetizing inductances, then the frequencies are given by the equations

$$\begin{aligned} f_{2b} = 1/(2\pi \sqrt{L_{pm} C_p}) \text{ and} \\ f_{2c} = \sqrt{[1/(L_{sm} C_s) - 1/(2C_s R_L)^2]} / (2\pi) \end{aligned} \quad (7-6)$$

Relatively large values of L_L compared to the values of L_{pm} and L_{sm} are inevitable with micro-miniature transformers, with the result that with them, the frequency limitation is likely to be caused by Eq. 7-6 rather than Eq. 7-5. With larger transformers, the limitation on frequency may be caused by either the leakage inductance and the capacitance, or it may be caused by the capacitance and the load resistance.

All terms in Eq. 7-4 that do not involve $L_{pm} L_{sm}$ may be neglected when L_{pm} and L_{sm} are very large, giving

$$s^2 (C_p + C_s) R_L + s^3 L_L C_p + s^4 L_L C_p C_s R_L = 0 \quad (7-4a)$$

The approximate resonant frequency under these conditions is given by the equation

$$f_{2d} = \sqrt{[(C_p + C_s)/(C_p C_s L_L) - 1/(2C_s R_L)^2]} / (2\pi) \quad (7-7)$$

This equation is the one applying to a high-quality transformer. Critical damping clearly is obtained only when the first term in the bracket is less than or equal to the second term, or when the load resistance is determined by the inequality

$$R_L^2 \leq C_p L_L / [4C_s (C_p + C_s)] \quad (7-8)$$

This loading condition may be comparatively easy to obtain with transistor amplifiers, but it has been almost completely overlooked with corresponding amplifiers using tubes.

The importance of the leakage inductance on the frequency response of a transformer circuit is dependent on the relative magnitudes of the inductive reactances X_{pm} and X_{sm} and the capacitive reactances of the distributed capacitances C_p and C_s . As long as the input signal is provided from a current source such as the collector circuit of a transistor, the effect of the inductance L_L may be neglected if the shunt reactances are large compared to R_L . If, however, the signal source behaves as a voltage generator, the leakage inductance can and does limit the frequency response. Then the limiting frequency may be determined in terms of one of the following equations

$$f_2 = R_L / (2\pi L_L)$$

or

(7-9)

$$f_2 = \sqrt{1/(L_L C_s) - [1/(2R_L C_s)]^2} / (2\pi)$$

where in the first equation C_s is negligible, and in the second it is not. These equations should be used for the determination of the frequency response limit when the transformer is activated by a low-impedance, or voltage, source.

7-1 DESIGN OF TRANSFORMER-COUPLED AMPLIFIERS

With the exception of the frequency-response calculations, the design of the transformer-coupled amplifier closely parallels that for the $R-C$ amplifier having a load line combination to consider. The static load line for the transformer-coupled amplifier has a slope corresponding to a very small value of resistance, the resistance of the primary winding. The slope of the dynamic load line is dependent on the load on the transformer. Since the load on the transformer may be a function of the operating point if it is determined by the input admittance of an additional transistor amplifier, the plotting of the load contour may introduce difficulties. The position of the contour may be a function of the signal amplitude as a result of current-averaging occurring in the input circuit.

The polarity with which the secondary winding of a coupling transformer is coupled from input to output can be important inasmuch as in one polarity the heavy-current direction for the load circuit may correspond to the direction of relatively small input current, and vice versa. Typical contours corresponding to these conditions are shown in Fig. 7-3. Because of the importance of these loading effects, it is necessary to design transformer-coupled amplifiers from the output back to the input.

The design of a simple output stage is relatively conventional, since the load impedance is nearly constant, varying principally as a function of frequency, and not as a function of the operating point. The techniques used for the design of the simple stage are extended for use with push-pull power amplifiers in a later paragraph.

The supply voltage selected for use with the collector circuit for a transformer-coupled transistor amplifier should be less than approximately 35 to 40% of the maximum rated voltage for the device (sufficiently low that the load line will not cross the bias curves in an avalanche region) to ensure that a breakdown failure will not occur during ordinary usage. The static load line may be drawn at the corresponding supply voltage with a slope corresponding to the DC resistance of the transformer winding. Dissipation contours, one corresponding to half of rated collector dissipation, and the other to full rated dissipation, should be plotted, and the Q-point for the power amplifier so selected that the

static dissipation does not exceed half the rated value, and the dynamic load line should be so oriented that it does not cross the contour for full rated dissipation.

If the transistor amplifier is one which only handles a small amount of power, the dissipation criterion is secondary, and the collector leakage current may be the principal factor controlling the design. Because of the extreme nonlinearity of the behavior of the transistor in the neighborhood of the contour for zero base current, it is necessary to select a static operating point that will ensure that a small-signal amplifier will have a minimum instantaneous collector current at least several times the open-base collector current when the operating temperature for the device has been elevated to the maximum operating temperature for the assembly. Al-

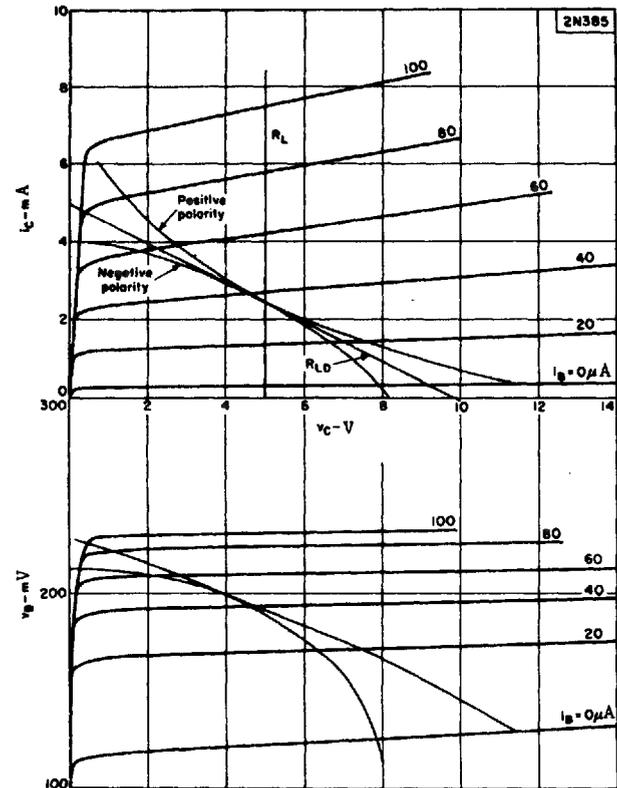


Fig. 7-3. Effect of Transformer Polarization in Interstage Load Line

though the transistor can be operated with reverse current flowing in the base lead (this is essentially what is done when the value of I_{co} is determined), the behavior is so nonlinear that operation under these conditions is not normally satisfactory. For this reason, data on either I_c or on I_e and β are helpful to the designer, particularly if they are given as a function of temperature. A convenient method for providing such data is shown in Fig. 7-4. The two graphs present contours showing the variation of collector current with collector voltage for fixed temperatures and either zero base current or zero emitter current. In this way, any irregularities in the behavior of the transistors in the low-current area may readily be recognized. (Valvo GMBH uses a correction curve set for this purpose on many of their transistors, Fig. 6-1 (Ref. 2).)

The use of either of these methods can lead to the use of the minimum acceptable value of static collector current, because the value of the current at any required temperature may be added to the peak signal current to give the minimum static current. The nominal value of the current gain β may be used to determine the peak output current change available in the collector circuit for the given input current change, and an impedance level may be selected that makes as full use of the current gain as possible. (The output admittance reduces the available current gain, particularly for large values of load impedance.)

The base-current contours corresponding to the minimum and the maximum instantaneous input current may be selected on the output curve family, as shown in Fig. 7-5. These two contours specify the minimum and maximum values of collector current, and their intersection with the line of static collector cur-

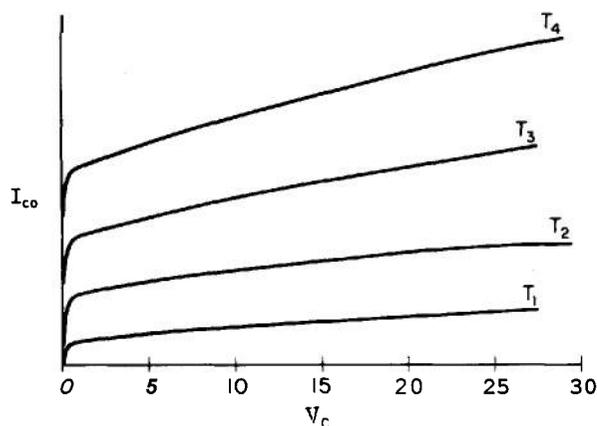


Fig. 7-4. Typical Contours of I_{co} vs V_c at Different Temperatures

rent, $X-X'$ shows the limiting condition for maximum (infinite) load impedance. If the contours for constant base current can be approximated adequately by straight lines, the maximum output power is obtained with the collector current change between the limit contours reduced to half the change available along the static load line. This condition is indicated by line $Y-Y'$. There is no advantage to using a load impedance greater than that required to produce the line $Y-Y'$, since the available collector-current change is reduced sufficiently that the available output power also is reduced at higher impedance levels. The voltage gain is increased, however.

The value of the dynamic load impedance selected should be smaller than the value given by the maximum power condition if the base-current contours cannot be approximated by straight lines. Such a curvature condition can occur if the dynamic load line crosses the contour of maximum base signal current in the neighborhood of its knee. The load impedance should be selected to yield a minimum collector voltage that is 0.5 to 1.0 V greater in magnitude than the value at the knee.

EXAMPLE 7-1. A transformer-coupled amplifier is required using the GT 761 transistor, the supply voltage being $V_{cc} = -3$ V, and the minimum collector current $I_{cp} = 0.8$ mA at $v_c = 5$ V. What is the maximum load resistance permitted if the base-current change is $40 \mu\text{A}$?

The total collector-current from a base current of $20 \mu\text{A}$ to $60 \mu\text{A}$ is 1.9 mA, giving a minimum change along the dynamic load line of 0.95 mA. The corresponding point along the $60 \mu\text{A}$ base contour is marked on Fig. 7-6, and the load contour drawn. The impedance for maximum power is nominally 5260 ohms. Since the contour curvature is high, however, the value that would be chosen would be less than this.

$$R_L = (5.0 - 0.5)/(2.2 - 0.8) = 3200 \text{ ohms}$$

The calculation of the amplification and distortion is similar to that described for the simple R-C amplifier.

7-2 CURVED LOAD CONTOURS

Curved load contours can be generated through the loading action of a nonlinear resistance, such as the input admittance of a transistor, or through the introduction of modifying voltages, either due to the current drawn in active devices, or through reactive components of voltage. The contours resulting from nonlinear

resistance and from external current-injection conditions are single-valued, whereas the contour resulting from reactive components of voltage are normally oval in shape. The plotting of each of these types of curved contours is now considered, and the applications to transistor circuits are analyzed in the next few paragraphs.

The load contour reflected onto the output of one transistor from the succeeding transistor is readily transcribed by transplotting the input admittance with the aid of the transformer impedance-ratio. The input contour for the output amplifier may be determined in conventional manner by transferring each intersection of the load line with a bias contour from the output to the input curve family. The approximate input power required is given by the equation

$$P_i = 0.125\Delta v_b \Delta i_b = 0.125(V_{bp} - V_{bn})(I_{bp} - I_{bn}) \tag{7-10}$$

The approximate admittance level is given by the equation

$$Y_i = \Delta i_b / \Delta v_b \tag{7-11}$$

The value of this admittance, and data on its variation with bias may be estimated using orthogonal polynomials if detailed data are not available on the small-signal parameters. The driving transistor is selected on the basis of its ability to dissipate at least three to four times the power given by Eq. 7-10, because the static dissipation must be at least twice the input power for class A operation for an amplifier.

Once the driver transistor has been selected, a trial supply voltage is chosen, and a minimum load line is plotted. This line is so located that it represents the minimum one capable of developing the required drive power. The impedance corresponding to the load-line slope may be determined, and the ratio of this impedance to the static input impedance of the transistor (or the product of the load-line impedance and the transistor input admittance) gives again the square of the turns-ratio for the coupling transformer.

After the turns-ratio for the transformer has been determined, the next step is the transfer of the load contour from the base circuit of the output transistor to the collector circuit of the driver transistor. The voltage and current changes in the base circuit are transformed by multiplying the voltage changes by the turns-ratio and dividing the current changes by the turns-ratio also. These changes may then be plotted on the collector family for the driver transistor. Both possible orientations for the load contour are shown on the sample curves.

EXAMPLE 7-2. Determine a suitable transistor to use as a driver for the 2N268 transistor whose curves are shown in Fig. 7-7. Also plot the load contours for the driver transistor for both polarities for transformer coupling. Take the static collector voltage to be 10 V, the base current 6.5 mA, and the static collector current as 500 mA. The transistor β is approximately 120.

The first thing to notice is that the static point chosen places the transistor under a heavy overload, because its rating in free air is 2 W, and the static dissipation level is 5 W. Consequently, the static collector current should be reduced to at most 100 mA.*

*Clearly, the supply voltage V_{CC} should be reduced!

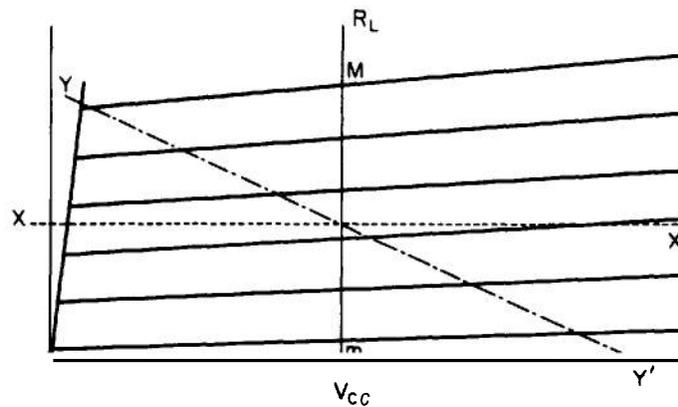


Fig. 7-5. Maximum Power Conditions—Idealized Curves

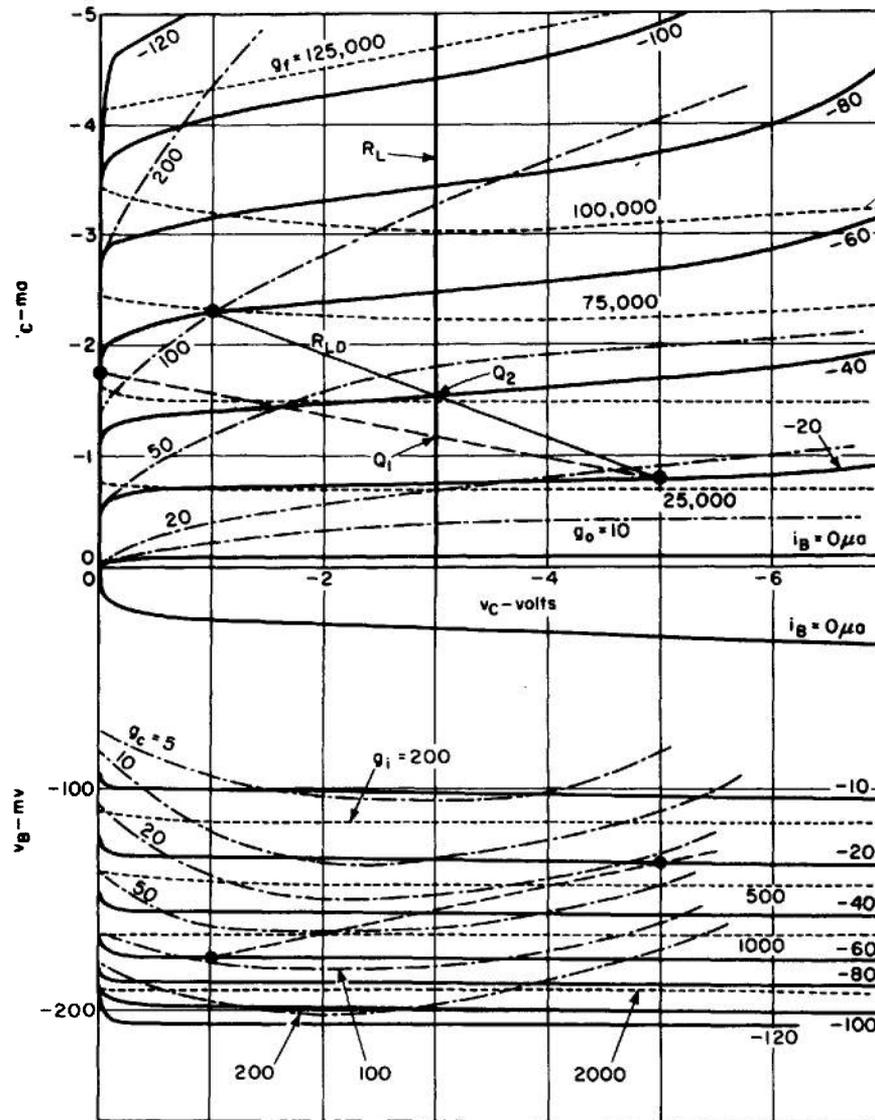


Fig. 7-6. Active Load-line Selection for Example 7-1

Because the data spread using a static point of 100 mA is inadequate for demonstration of the procedure, and the use of an adequate heat sink can increase the dissipation capacity of the device sufficiently to make possible the use of the load line through a combination of decreasing the static current and increasing the supply voltage, the design process will be completed. Reading from the input curves, the base-voltage change for a base-current change from 0 to 10 mA is 0.56 V, for an average input resistance of 56 ohms. The input power required to shift the collector current from I_c to saturation is 0.014×0.72 , or 12 mW.

Based on this power requirement, the driver transis-

tor should have at least 50 mW collector dissipation rating. A suitable transistor for this purpose is the type 2N369 (302) transistor. Choosing initial conditions for this device of $V_{CC} = -10$ V, and a static collector current of 1 mA, the trial load impedance is given by the equation

$$Z_L = V_{CC}/I_c$$

For the conditions stated, the value of Z_L is 10,000 ohms, giving a turns-ratio of 13.4:1. The basic data and the load-line data are given in Table 7-1.

The load contour and a magnified version of it are both plotted in Fig. 7-8. This contour is plotted in two different orientations, which can be obtained by reversal of the transformer polarity.

The major effect of the curvature of the load line is to cause a difference in the total voltage change from the neutral point for the two signal polarities. Because one contour represents a higher average power dissipation,

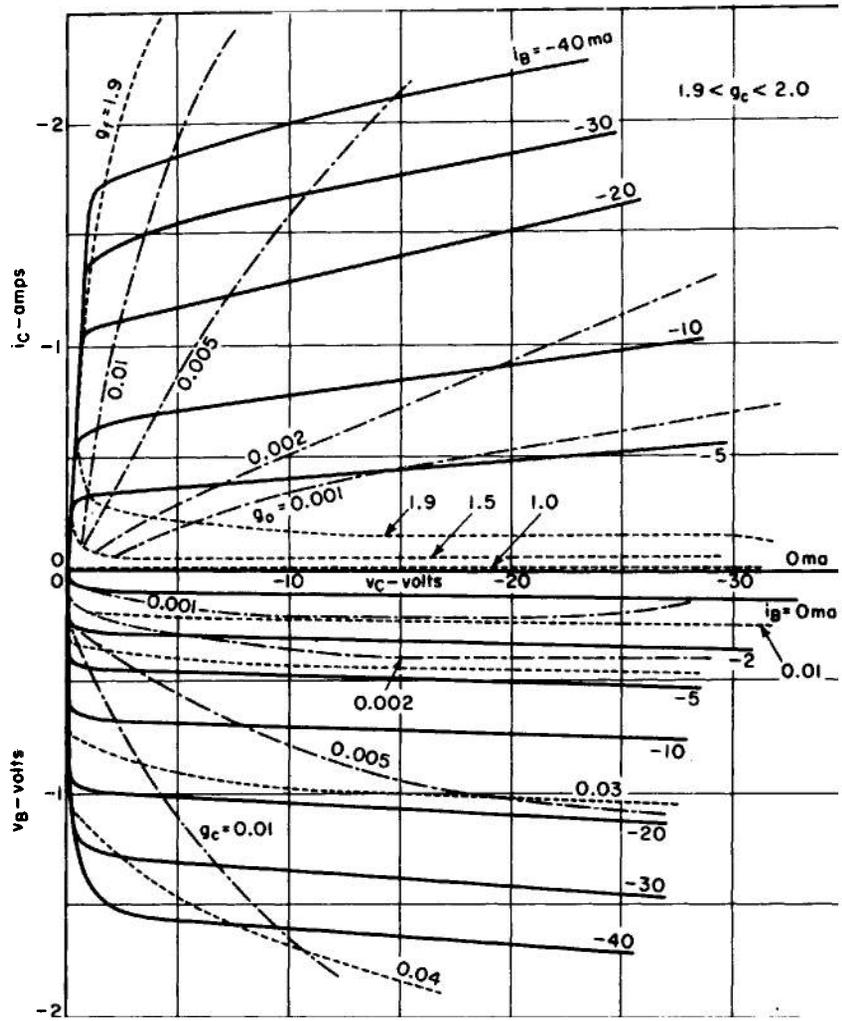


Fig. 7-7. Curves of 2N268 Transistor for Example 7-2

TABLE 7-1
LOAD CONTOUR DATA

i_B	Δi_b	Δv_b	$-n\Delta v_b$	$\Delta i_b/n$
0	-6	-0.42	5.61 v	-0.45 ma
2	-4	-0.21	2.81	-0.22
5	-1	-0.04	0.53	-0.07
6	0	0.00	0.00	0.00
10	4	0.15	-2.00	0.30
14	8	0.23	-3.07	0.60

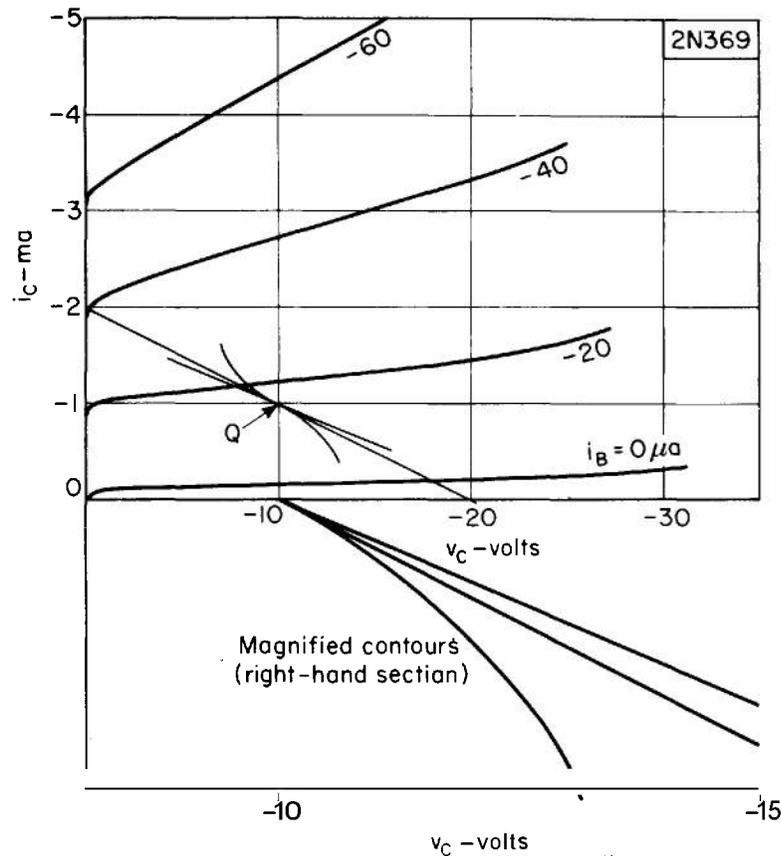


Fig. 7-8. Load Contours for Example 7-2

tion than the other for a given average position, the contour that is convex toward the origin should be selected.

This load contour may be transferred back from stage to stage, from output family to input, then from input to the output family of the previous amplifier, until corresponding points for the stages have been localized. Then the small-signal data at all these corresponding points may be tabulated and the overall gain of the amplifier calculated.

7-3 AMPLIFICATION CALCULATIONS

The calculation of the amplification for a transformer-coupled amplifier parallels the similar calculations for R-C amplifiers, but differs principally in the way the load resistance can be a function of the operating condition. It is therefore necessary to tabulate not only the small-signal data for the transistor as a function of operating conditions but also the value of the effective load impedance. Because many of the stages of the amplifier may be functioning as current amplifiers, the load impedance data may not be important. When they are, however, they can be determined as described.

EXAMPLE 7-3. Calculate the load impedances at typical points along the load line for the 2N369 (302) transistor.

Because the turns-ratio was shown in Example 7-2 to be 13.4:1, the square of the ratio is 179. If, then, corresponding points are found on the curve families, the corresponding values of R_L and Y_i may be tabulated.

i_B	0	2	5	6	10	14
Y_i	0.0069	0.0149	0.0221	0.0233	0.026	0.030
R_L	26,000	12,000	8100	7700	6900	6000

The small-signal data may be tabulated from the curves, and the balance of the calculation performed.

7-4 PUSH-PULL AMPLIFIERS

The amplifiers discussed so far have been relatively linear, or class A amplifiers, and have used only a single active device. The use of a pair of transistors in push-pull, however, makes possible operation under low-power static conditions yet a considerable amount of power under normal operating conditions. Amplifiers having these characteristics are variously known as class B, class AB, and class AB, operation.

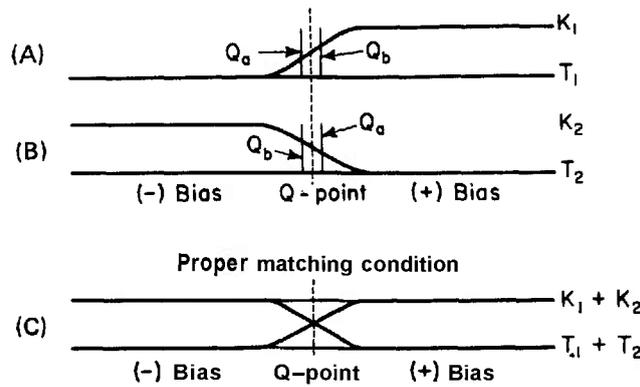


Fig. 7-9. Ideal Amplification Curves for Transistors in Push-pull Amplifier

For two transistors, or two active devices, to operate efficiently in push-pull, it is desirable for each device to provide the amplification over approximately one-half of the cycle, with first one device in the active condition and then the other (Fig. 7-8). The switching from one device to the other cannot be instantaneous, because the transition from the off-state to the on-state is gradual with devices like transistors and electron tubes. In addition, the effect of tolerances on the device is such that if an instantaneous transition did exist, it would be impossible to select devices that would switch simultaneously as required.

The characteristics that are well-suited to devices used in push-pull amplifiers are shown in Fig. 7-9. In the transfer region, the amplification should increase from zero at one edge to the specified amplification at the other edge in a linear manner. Throughout the active region the amplification should have the specified value. If then two devices are connected so that their static operating points, the Q-points, are at the center of the transfer region, an amplification that is independent of the operating point results, and essentially distortionless operation is obtained.

Although it is usually considered to be unnecessary to have small-signal data on devices used under large-signal conditions, the small-signal data are not only useful, but rather necessary. This is a result of the importance of proper matching of the amplification characteristics in the achievement of a low-distortion design. If, for example, the Q-point is selected at the point Q_a , then a dip in the amplification is produced in the neighborhood of the static operating point, and the distortion introduced into low-amplitude signals is excessive. Similarly, if the Q-point is selected at the point Q_b , then the amplification in the neighborhood of the static point will be larger than it should be, and

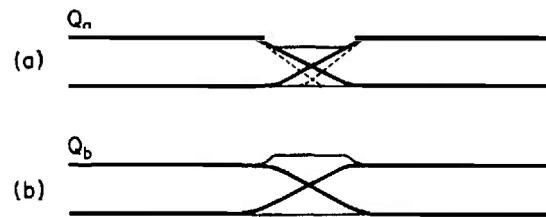


Fig. 7-10. Effect of Use of Different Q-points

once again, the small-signal distortion will be excessive. As is evident from the plots of Fig. 7-10, only a very small error in the value of the static amplification can introduce severe distortion conditions for small-amplitude signals.

In addition to the bias points, the designer has two other important methods of control of distortion in push-pull amplifiers. One of these methods is the adjustment of the effective source resistance for the input signal supplied to the amplifier, and the second is the return resistance in the emitter circuits for the transistors. The values of these resistances may be used in the adjustment of the amplification to relative uniformity.

The type of matching characteristics obtained as a function of base current differs significantly from that obtained as a function of base voltage. Consequently, it is important that the matching be selected to conform with the type of drive available for the transistor. If, for example, a feedback-stabilized amplifier is transformer-coupled to its driver, and the output impedance of the transformer has been selected to provide essentially constant-voltage drive (this condition exists only rarely), then the matching should be on a voltage basis, whereas ordinarily with a driver transformer driven from a transistor amplifier, current matching should be used. If the output amplifier is excited from a push-pull

common-collector amplifier (emitter-follower), then the drive conditions usually are constant-voltage, and voltage matching should be used. The examples show the differences that exist between the two conditions.

The establishment of a fixed Q-point with respect to transistor characteristics under variations of both ambient temperature and input signal level is a difficult problem with transistor amplifiers. The use of emitter degeneration is not satisfactory because the transistors draw more average current with signal input than without it. The use of a base-current limiting circuit is unsatisfactory for that reason. The base-to-emitter voltage is a function of circuit temperature, and the base current is a function of the signal amplitude, a rather incompatible combination.

The use of an emitter-follower to provide the signal to each transistor of the amplifier is one of the methods of making available a varying average base current under load (Fig. 7-11). The emitter of the driver transistor should be connected directly to the base of the power transistor for such an application. Another possible method is the use of a silicon diode in the forward direction, or a Zener diode to provide a reference voltage varying in a manner which matches the transistor variation (Fig. 7-12). In this method, the current through the diode network should be at least twice the peak base current, and the center-tap of the driver transformer is returned to the potential end of the diode.

The diode selected for use as a biasing element should have a voltage loss that is approximately equal to the base-to-emitter voltage for the transistors at their static operating point, and the voltage should vary as a function of temperature in step with the base voltage

variation. The diode should be mounted in close contact with the transistor, or only partial compensation will result, and the possibility of thermal runaway is increased thereby.

Other devices may be used for compensation to protect amplifiers from thermal runaway. Among the more commonly used devices are thermistors and lamp bulbs. The essential characteristic required is either a resistance variation with temperature, or a voltage variation with temperature.

The danger of thermal runaway can be minimized by providing operating conditions that make certain that the dissipation in the active devices decreases as the temperature rises. To do this, it is essential that the static value of current not increase under any conditions, or that the collector voltage decrease more rapidly than the collector current rises. Unfortunately, however, it is not possible to control dissipation by voltage reduction with class B amplifiers, and the control of the static current is rather difficult also. The fine adjustment required to set the static level of current when a thermistor or a diode regulator is used can be accomplished either by the use of a small value of resistance in the emitter circuit, since only a very small range of control is required, or it can be introduced by the use of a low-resistance potentiometer in series with the diode or the thermistor. Because the principal part of the voltage is controlled by the thermal-sensitive device, the adjustment has become rather noncritical.

EXAMPLE 7-4. Calculate the amplification as a function of bias for an amplifier using a pair of 2N174 transistors. Select an appropriate Q-point for the amplifier that will prove suitable in a push-pull amplifier.

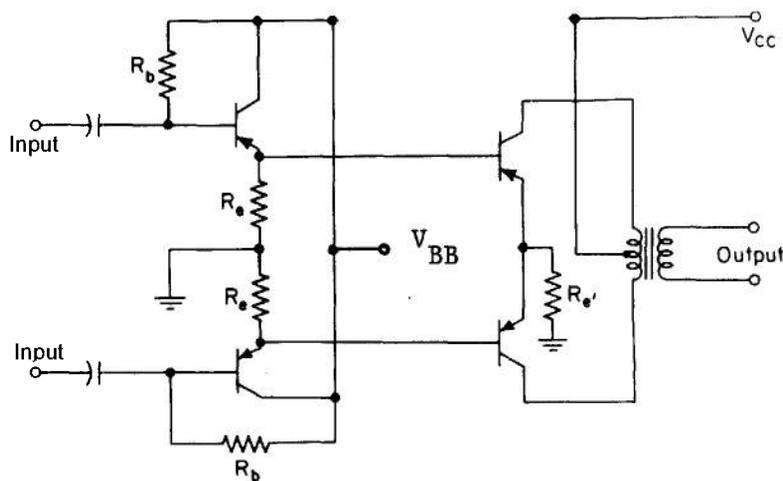


Fig. 7-11. Emitter-coupled Power Amplifier

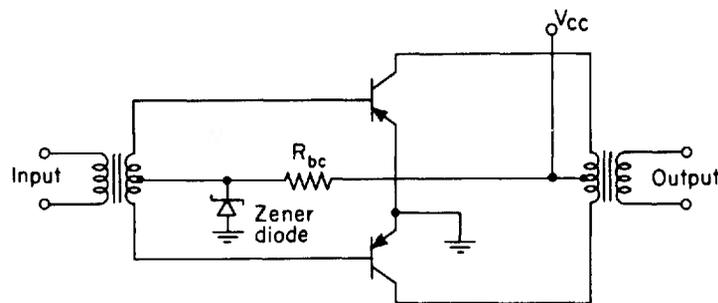


Fig. 7-12. Zener Diode Stabilizing Circuit

Discuss how a diode may be used for providing the static bias.

On the basis of the characteristic curves for this transistor, a supply voltage of 15 V appears reasonable, and a trial Q-point of 15 V, 150 mA may prove satisfactory. With the maximum collector current of 2 A, a dynamic load impedance of 8 ohms is required (Fig. 7-13).

The value of R_{LD} of 8 ohms is sufficiently small that the simple form for the equations for amplification may be used.

$$K = -g_f R_L / (1 + g_i R_s) \quad (7-12)$$

or

$$K_i = g_f R_s / (1 + g_i R_s) \quad (7-12a)$$

The value of R_s , which is used with these equations, depends on the characteristics of the input circuit. For convenience of calculation, values used for the calculation are $R_s = 0, 10, 20, 50,$ and 100 ohms. Based on these values, the amplification data may be listed as in Table 7-2.

The input resistance R_i is connected in shunt for the current gain equation, and in series for the voltage gain. The current gain values for smaller input resistance could be calculated, but the shunt loading is sufficient to reduce the gain excessively. The values of current gain for R_s (shunt) infinite are 100 at 2 mA, 97, 90, 102, 104, and 109, respectively, for the remaining values of current.

Possibly one of the most reliable ways of getting thermal compensation for a class B amplifier using transistors is shown in two forms in Fig. 7-14. In this arrangement, an ordinary diode, germanium or silicon as required, is used to control the base voltage of an emitter-follower amplifier that operates in class A. The

follower can set exactly the static potential on the base circuit for the power stage and at the same time provide a sufficiently low source impedance to assure adequate current capacity for the input circuit. For applications in which a suitable interstage transformer is available, the emitter-follower may be used to provide the DC level for the base circuit of the final, and the signal itself may be amplified and introduced into the base circuit of the final through the transformer. This latter circuit configuration is shown in Fig. 7-14(B). Either of these configurations may be used to make available the adjustment required on the static voltage on the input circuit, because a potentiometer connected in series with the charging diode gives the adjustment required to make possible the proper balance in amplification.

Because the current gain is relatively fixed at the ratio of g_f/g_i for the transistor amplifier when a series input circuit is used, and the ratio of g_f/g_i is relatively constant over the entire operating range, the power gain of the amplifier is approximately proportional to the voltage gain. The values of voltage gain as a function of base bias given in Table 7-2 are plotted as a function of the source resistance in Fig. 7-15. These curves show that the variation of the input impedance affects markedly the operating point, which should be used for best linearity, and they also show that small changes in the selected static point can seriously affect the linearity of the resulting push-pull amplifier. Fig. 7-16 shows the effect of variations of the static base current in half-milliampere steps for a source resistance of 20 ohms. Similar plots may be made for other values of R_s . The best static operating point with $R_s = 20$ ohms calls for a current appreciably less than 2 mA.

The composite plots of the amplification sum for a push-pull amplifier (Fig. 7-16), show how critical the selection of the appropriate value for the static bias is. The static current increment of a half milliampere between successive contours is almost negligible compared to the 40 mA full-scale current. Because class B

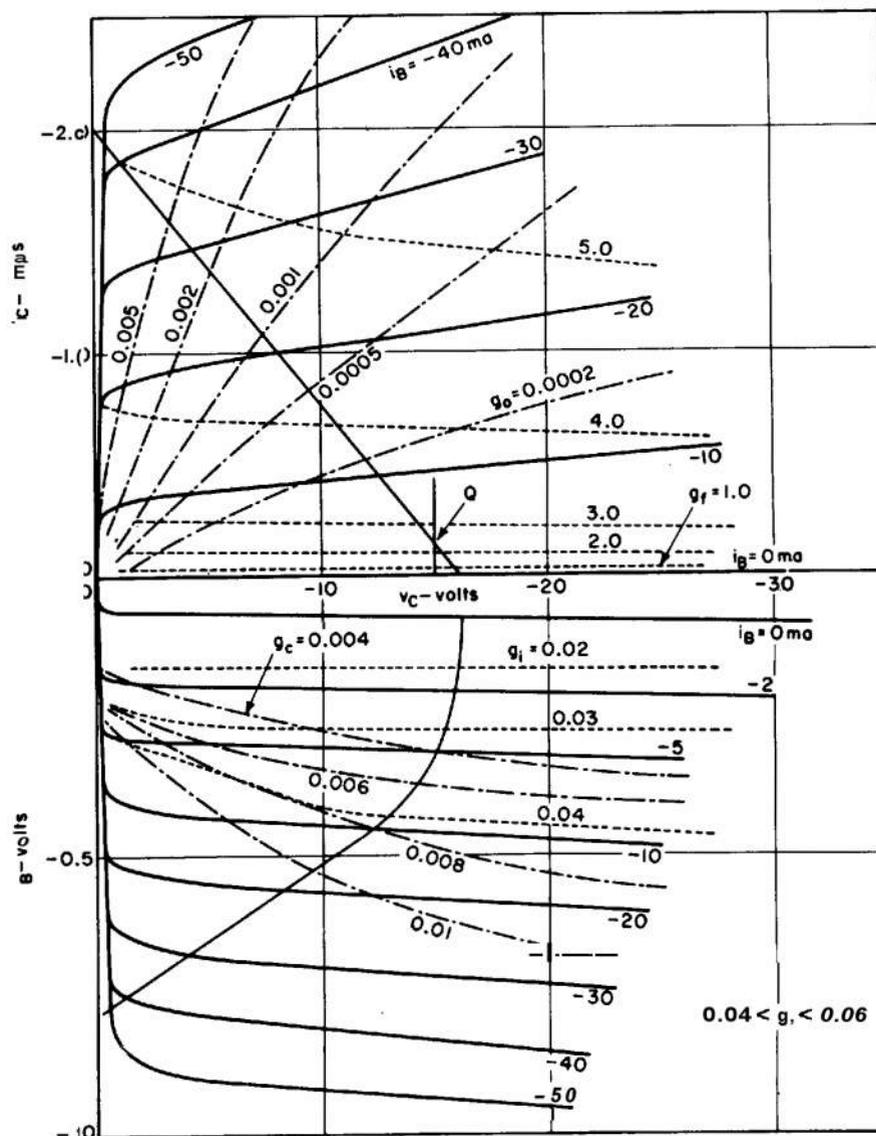
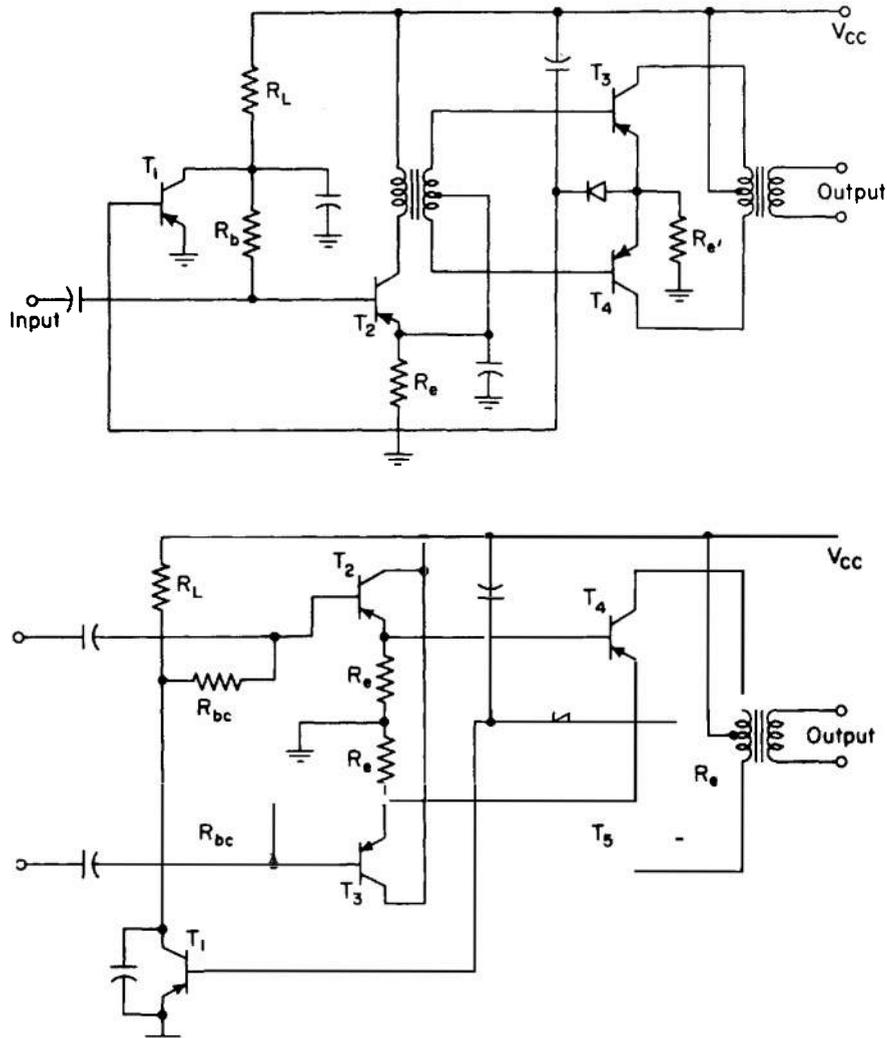


Fig. 7-13. Operating Characteristics of Power Transistor 2N174 for Example 7-4

TABLE 7-2
AMPLIFICATION DATA

i_B	v_c	i_c	g_i	g_f	$K_v \text{ min}$	$K_v \text{ max}$	$K_i \text{ max}$
2 ma	15 v	150 ma	0.024	2.4	5.1	19.2	70.6
5	14.2	240	0.031	3.0	5.9	24.0	73.0
10	12.5	460	0.040	3.6	5.8	28.8	72.0
20	8.0	1.01 amp	0.043	4.4	6.6	35.2	83.0
30	4.2	1.48	0.045	4.7	6.8	37.6	85.0
40	1.1	1.87	0.046	5.0	7.1	40.0	89.3



amplifiers normally have significant irregularity in the value of amplification near the Q-point, it is important that the static point be chosen to minimize the variation. The irregularity is a minimum with a static bias current of 0.5 mA, and the distortion characteristics and the balance of the data should be tabulated under this condition. Approximately 3% third-harmonic is introduced into small-amplitude signals.

The design of the thermal compensation circuit based on Fig. 7-14 requires data on both the thermal characteristics of the base voltage for the output transistors and also the thermal characteristics for the emitter-follower and the diodes. First the base voltage required on the output amplifier is noted, and then the base voltage required for the follower to provide the base-current margin for the final is noted. A transistor

suitable for use as the emitter-follower is the 2N270, static data for which are shown in Fig. 7-17. At room temperature a base voltage of approximately -120mV is required with the 2N174 power transistor at its static point. The corresponding total base voltage for the 2N270, as can be seen in Fig. 7-17, is -200 mV if the transistor is used as a direct signal driver with a static collector current of 10 mA, and 250 mV for 30 mA collector current if the transistor is used to provide the bias by way of a driver transformer.

Brief consideration shows why the two different operating conditions are required for the two methods of using the driver amplifier. When the driver transistor couples the signal into the base circuit of the amplifier directly, then the signal applied to the base terminal of the driver increases the current available for the base of

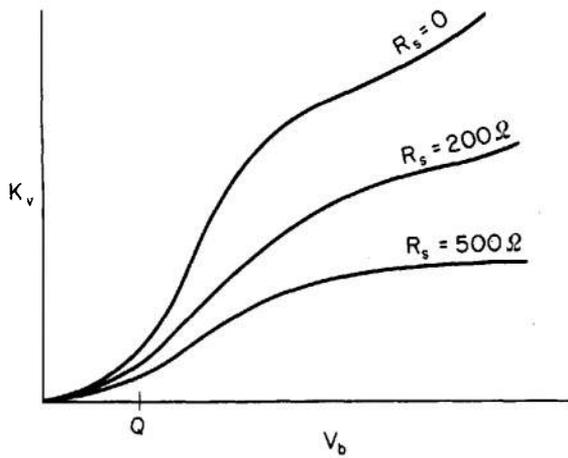


Fig. 7-15. Typical Variation of K_v With R_s and V_b

the output amplifier. When, however, the emitter-follower is used to provide the static bias, and a transformer is used to provide the signal, then signal current from the transformer flows through the driver emitter and it is not accompanied by a change in the base-to-emitter voltage. The only way the voltage can increase is through discharge of the emitter storage capacitor. For this reason, the static current level in the driver must be large enough to maintain the required emitter output voltage. The static emitter current in the driver must be equal to or greater than the peak base current of the final amplifier.

Typical operating conditions for the two forms of output amplifier are enumerated in Table 7-3.

7-5 REACTIVE LOAD LINES

Although many amplifiers use load elements requiring representation in terms of oval load contours, they usually can be represented and analyzed in terms of the equivalent resistive load contour. Occasionally, however, it is important to be able to analyze a circuit in terms of an elliptical load contour, including both the harmonic components and also the in-phase and the out-of-phase components.

The determination of the form of the load contour and the calculation of the amplification along it are discussed in the next few paragraphs. The analysis of the phase and frequency components is somewhat more intricate, particularly for the analysis of the oval load line. The process is described in Part C of Appendix C.

If a reactive load must be used for an amplifier, the shape of the load contour used is a function of frequency, with the result that a separate analysis is required for each frequency of interest. In performing such an analysis, the phasor form for the load impedance is substituted for the resistance in the appropriate form of the amplification equation.

The consideration of the effect of reactance in a circuit is usually most important in output or power amplifiers. Although the terms involving y_o and y_c can usually be neglected in the calculation of the characteristics of these amplifiers, they are included here. For the general case, the amplification equation, common emitter, may be written

$$K = \frac{-y_j(R_L + jX_L)}{(R_L + jX_L)[1 + y_iR_s + (y_o + y_c y_e R_s)]} \tag{7-13}$$

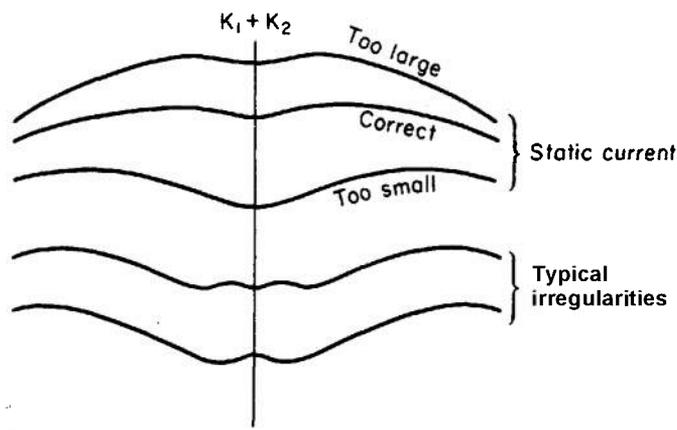


Fig. 7-16. Effect of Changes of Static Bias and Contour Irregularity

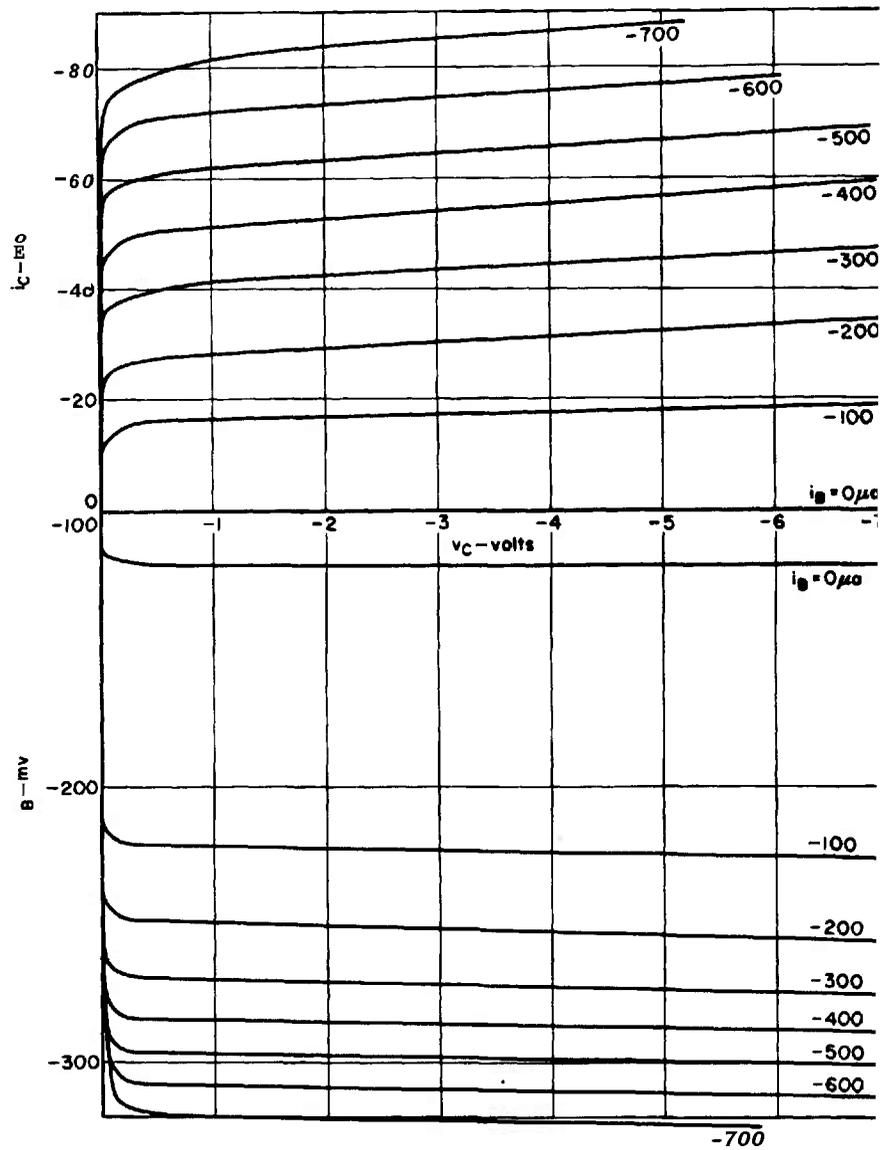


Fig. 7-17. 2N270 Curves

TABLE 7-3
COMPARATIVE DATA FOR POWER AMPLIFIERS

	(a)	(b)
R_{e0}	1 ohm	1 ohm
R_{e1}	120 ohms	120 ohms
R_{e2}	100 ohm potent.	100 ohm potent.
R_{e3}	3,000 ohms	3,000 ohms
R_{L1}	800 ohms	200 ohms
R_{L2}	7,500 ohms	7,500 ohms
R_b	80,000 ohms	10,000 ohms
V_e	+1 v	+5 v

This equation may be rationalized to eliminate the j terms in the denominator, giving

$$\begin{aligned}
 K &= -y_f(R_L + jX_L)[(1 + y_iR_s + R_L(y_o + y_{ic}R_s)) \\
 &\quad - jX_L(y_o + y_{ic}R_s)] / [(1 + y_iR_s \\
 &\quad + R_L(y_o + y_{ic}R_s))^2 + X_L^2(y_o + y_{ic}R_s)^2] \\
 &= -y_f[(1 + y_iR_s + R_L(y_o + y_{ic}R_s))R_L \\
 &\quad + X_L^2(y_o + y_{ic}R_s) + jX_L(1 + y_iR_s)] / [(1 \\
 &\quad + y_iR_s + R_L(y_o + y_{ic}R_s))^2 \\
 &\quad + X_L^2(y_o + y_{ic}R_s)^2] \quad (7-14) \\
 &= -y_f[(1 + y_iR_s)R_L + (R_L^2 + X_L^2)(y_o + y_{ic}R_s) \\
 &\quad + jX_L(1 + y_iR_s)] / [(1 + y_iR_s \\
 &\quad + R_L(y_o + y_{ic}R_s))^2 + X_L^2(y_o + y_{ic}R_s)^2] \\
 &= -y_f[(R_L + jX_L)(1 + y_iR_s) + (R_L^2 + X_L^2) \\
 &\quad (y_o + y_{ic}R_s)] / [(1 + y_iR_s + R_L(y_o + y_{ic}R_s))^2 \\
 &\quad + X_L^2(y_o + y_{ic}R_s)^2] \quad (7-15)
 \end{aligned}$$

With power amplifiers, this equation may often be simplified to the form

$$K = -y_f(R_L + jX_L) / (1 + y_iR_s) \quad (7-16)$$

In using either of these equations, the first step is the plotting of the resistive load line, that is, the line for $X_L = 0$. The second step is the plotting of the reactive component. This component does not depend on the magnitude of the collector current, but on either the integral or the derivative of the current. For this reason, the reactive voltage must be introduced at rela-

tively constant output current. This voltage change is stepped off along the base-current contours, since the reactive voltage does not affect the input currents appreciably. The amplification is therefore divided into two components

$$K = K_R + jK_L \quad (7-17)$$

The operator must be kept with the inductive component, not because the phasors are plotted at right angles, but because the rate-of-change has a maximum value when the magnitude of the net current change from the static value is zero. For a sinusoidal input signal $I_s \sin \omega t$ (or $V_s \sin \omega t$), the magnitude of the reactive voltage, in terms of the maximum change of collector voltage V_{cm} , may be given by the equation

$$v_{cL} = V_{cm} |K_L/K_R| \cos \omega t \quad (7-18)$$

This voltage is measured along a constant-base-current contour on both sides of the resistive contour, as is sketched in Fig. 7-18. In this figure, the ratio of $|K_L/K_R|$ has been assigned the value 0.20 for convenience of plotting, and the simplified form of the equation has been used.

The type of stage in which a reactive load line normally is required is a push-pull class B amplifier. If a 2N301 transistor is used in such an amplifier, and the load contour is plotted for one of the transistors, the result is shown in Fig. 7-19. After the contour has been plotted, the amplification and the other required design data may be compiled as has already been indicated.

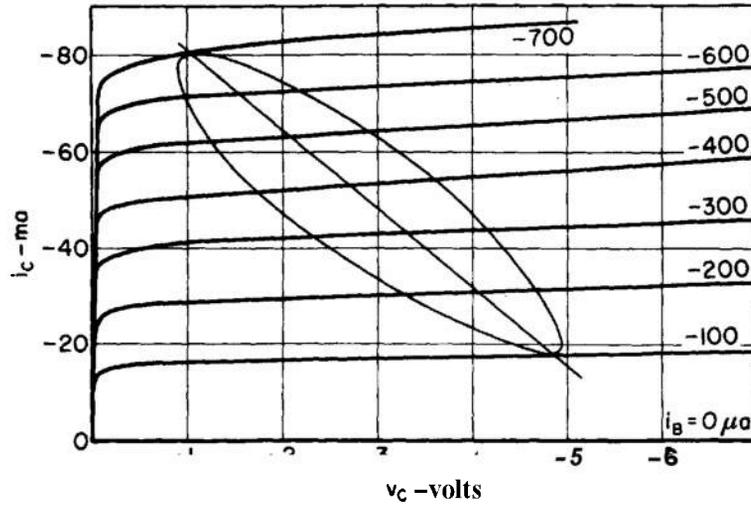


Fig. 7-18. Elliptical Load Line

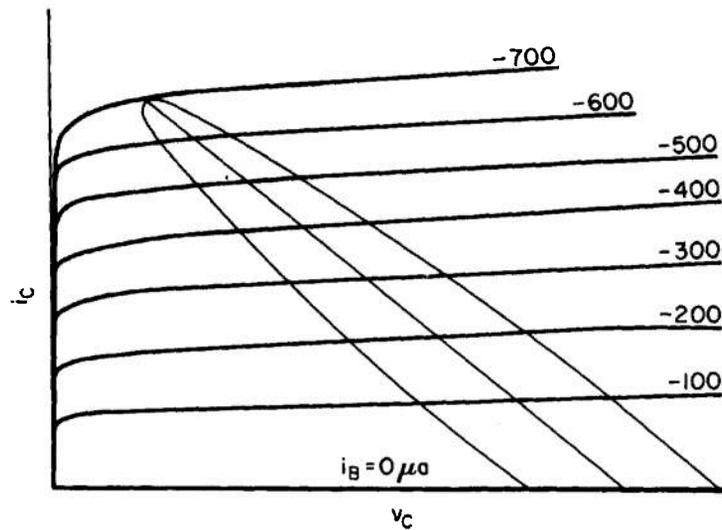


Fig. 7-19. Semi-elliptical Load Line

REFERENCES

1. H. W. Lord, "An Equivalent Circuit for Transformers in Which Nonlinear Effects Are Present", *Communication and Electronics*, American Institute of Electrical Engineers, November 1959.
2. *Valvo-Handbuch*, Halbleiter, Valvo GMBH, Hamburg 1, Germany, 1959.

CHAPTER 8

RF AND IF AMPLIFIERS

8-0 BASIC DESIGN

The design of an RF or an IF amplifier using transistors parallels rather closely the design of transformer-coupled amplifiers. Because of the input and output tuned circuits that must be used with them, these amplifiers are sensitive to feedback through the collector-base capacitance in addition to the parameters already considered. This capacitance tends to introduce instability and regeneration into the circuit, and makes necessary the use of relatively small load impedances in the collector circuits.

Transistors used for RF amplifiers differ from tubes in several important respects. First, the input and the forward transfer admittances for a given collector current are both large compared to the values for tubes. The forward admittance, for example, at about 39,000 pmhos per mA of collector current, is from fifteen to forty times as large as the corresponding tube transconductances. Also, the input capacitance is correspondingly larger. By comparison, the base-to-collector capacitance may be less than or equal to the grid-to-plate capacitance in a triode tube, and as a result of the relatively lower impedance level used with the associated circuitry, it is of considerably reduced importance. The remaining important difference is in the nature of the series impedances between the terminals of the device and the active junctions, the emitter and collector series r_e' , r_c' , and the base-spreading resistance r_b' . These resistances affect the operation of a transistor in several ways. The emitter series resistance increases the required drive power for the circuit, and, as a consequence of circuit degeneration, also limits the amplification that can be obtained. The base-spreading resistance increases the drive power required, and increases the tendency for instability in an amplifier. The collector series resistance increases the total impedance in the output circuit, increasing the total internal gain and, as a consequence, increases the probability of regeneration and reduces circuit stability. It also introduces phase-shift into the output circuit.

With transistor and triode tube amplifiers, it is necessary either to unilaterize the circuit (neutralize it usu-

ally) or to operate the device in the separation mode (grid or base grounded). These methods of operation limit the feedback coupling from the output to the input, and maximize the usable amplification. The presence of the base-spreading resistance tends to reduce the isolation between the output and the input in the transistor separation amplifier, and can increase its instability.

In either the base-separation or base-input mode of operation, the presence of the base-spreading resistance is a detriment to unilaterization or neutralization, as it makes both the circuit configuration and the component sizes more critical. The configuration for unilaterizing the base-separation circuit is considerably simpler because of the low value of input impedance for the common-base amplifier.

The general equation for the amplification for the common-base amplifier is given in Eq. 4-25. Modifying this equation to the proper form for use with tuned amplifiers gives

$$K = [(y_{f'} + y_o) + y_i y_c r_b'] Z_L / [1 + y_o Z_L + \sigma(y') Z_e + y_i r_b' + y_i y_c (r_b' Z_L + r_b' Z_e + Z_e Z_L)] \quad (8-1)$$

The regeneration is developed in this equation in terms of the expansion of the product $y_i y_c r_b' Z_L$

$$y_i y_c r_b' Z_L = (g_i' + j b_i')(g_c + j b_c) r_b' (R_L + j X_L) / [(R_L + j X_L) j B_C + 1] \quad (8-2)$$

The value of the denominator of Eq. 8-2, for a frequency near the resonance frequency ω_o may be written in the form, where

$$a = a + \Delta\omega \text{ and} \\ \omega_o^2 L_L C_L = 1,$$

$$j B_C R_L + 1 - X_L B_C = j \omega C_L R_L - 2 \Delta\omega L_L C_L \\ \doteq j \omega_o C_L R_L - 2 \Delta\omega L_L C_L \quad (8-3)$$

Substituting this into Eq. 8-2 gives

$$(g_i + jb_i)(g_c + jb_c)r_b j\omega L_L / (j\omega C_L R_L - 2\Delta\omega L_L C_L) = y_i y_c r_b Z_L \quad (8-4)$$

Rationalizing gives

$$\begin{aligned} y_i y_c r_b Z_L &= (g_i + jb_i)(g_c + jb_c)r_b j\omega L_L (-2\Delta\omega L_L C_L - j\omega C_L R_L) / (4\Delta\omega^2 L_L^2 C_L^2 + \omega_o^2 C_L^2 R_L^2) \\ &= [g_i(r_b \omega_o^2 L_L C_L R_L g_c + b_c r_b \omega_o \times 2\Delta\omega L_L^2 C_L) - b_i(b_c r_b \omega_o^2 L_L C_L R_L - 2g_c r_b \omega_o \Delta\omega L_L^2 C_L) + j(g_i(g_c r_b (-2\omega_o \Delta\omega L_L^2 C_L) + b_c r_b \omega_o^2 L_L C_L R_L) + b_i(g_c r_b \omega_o^2 L_L C_L R_L + b_c r_b \omega_o L_L \times 2\Delta\omega L_L C_L))] / (4\Delta\omega^2 L_L^2 C_L^2 + \omega_o^2 C_L^2 R_L^2) \end{aligned} \quad (8-5)$$

Near the resonant frequency, where $\omega_o \sqrt{L_L C_L} = 1$, the negative real term of the numerator of Eq. 8-5 is the predominant one, with the result that it may be approximated by

$$y_i y_c r_b Z_L = - (b_i b_c r_b R_L) / (\omega_o^2 C_L^2 R_L^2) \quad (8-6)$$

where R_{eff} is the effective tuned resistance of Z_L , and the reactive, or j , terms have been neglected because they can be tuned to zero as desired by adjusting C_L or L_L . This term appears in both the numerator and the denominator of Eq. 8-1, but the total value of the numerator is large compared to unity, whereas the value of the denominator lies in the neighborhood of unity, normally less than three or four at most for the total. For large values of Z_L and r_b , it is therefore possible for this negative term to cancel the positive terms in the denominator and to permit oscillation to develop. Since both b_i and b_c are proportional to the capacitances, and these capacitances are functions of V_c and I_c , the amount of negative conductance is proportional to the capacitance. The negative conductance and the capacitances are inverse functions of the collector voltage. Other than for unilateralization, there are two ways of minimizing the possibility of oscillation developing

with an amplifier using a given transistor; first, by raising the collector voltage and thereby decreasing b_c , and second decreasing R_{eff} either by using a higher C-tuned circuit, or by tapping the collector to a relatively lower impedance level on the tuned circuit. Tapping is preferred.

The reactance level of the circuit that provides the input signal to the emitter of the transistor should be so selected that the signal reaches the emitter without excessive reduction of the circuit Q-factor, and at the same time it is essential that the coupling be sufficiently tight to obtain efficient energy transfer. The problem of interstage coupling with transistors is complicated by the fact that the input admittance of the transistor is extremely large and its output admittance is extremely small. Consequently, a matching network is required that can readily match a low-impedance load to a high-impedance source. The input impedance may be as small as from 1 to 50 ohms, and the output impedance in general is larger than 1000 ohms, making the impedance transformation ratio required greater than 50.

8-1 COUPLING METHODS

The transformers used at audio frequency for adjusting coupling impedances are replaced at higher frequencies by some form of tuned circuit or transformer. The simplest arrangement, one which has found widespread use, is shown in Fig. 8-1. In this circuit, the inductor is placed in series with the collector, and a capacitive divider couples the collector to the emitter and to ground. If the Q-factor of the tuned circuit is sufficiently high for a resonant build-up to occur, even with resistive loading of the emitter across the capacitance from emitter to ground, then satisfactory operation will result. The condition required for such a circuit to function effectively is that the circulating current representing the stored energy must be large compared to the resistive current withdrawn by the emitter. If this condition exists, then the impedance step-down in the capacitive divider is determined approximately by the square of the capacitance ratio, and efficient energy transfer may be obtained. If there is any question as to the adequacy of the value of the Q-factor, then a tapped coil should be used, because the magnetic field of the coil then assures a square-law reduction of

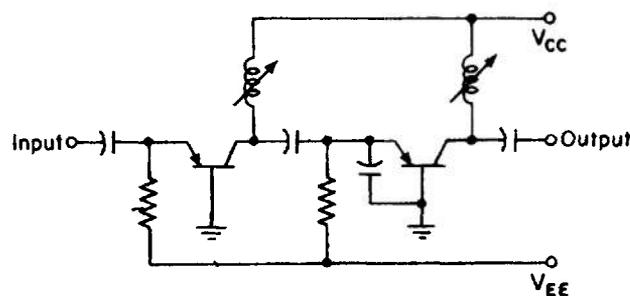


Fig. 8-1. Common-base Tuned Amplifier Coupling Circuit

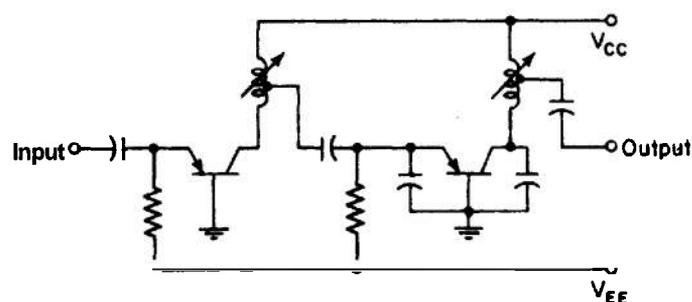


Fig. 8-2. Tapped Coupling Circuit

impedance. Such a coupling circuit is shown in Fig. 8-2. With the tapped-coil arrangement, a single capacitor may be used for tuning, rather than a series combination, and a large coupling capacitor may be used to introduce the signal into the emitter of the succeeding amplifier.

The capacitive divider arrangement often makes use of the input capacitance of the transistor as part of the capacitor C_2 , since C_i is relatively large, and often may be an appreciable part of the total required capacitance. A minimum stage-to-stage voltage or current gain of approximately 10 is desirable, and because the ratio of the collector impedance to emitter impedance is in the neighborhood of 100, an overall emitter-to-collector voltage gain of approximately 100 is required. Because the design of this coupling circuit is possibly the most critical stage in the design of an RF or an IF amplifier, it is examined in detail in the next few paragraphs.

EXAMPLE 8-1. Design an RF coupling circuit for use with a 10 MHz amplifier. For the purpose, assume that $(y_i + y_p)^{-1}$ is 30 ohms, and C_i is 200 pF.

Because the emitter of the driven transistor absorbs power from its driver amplifier, it is reasonable to assume that the loading from the emitter will reduce the Q-factor of the tuned circuit for the previous stage at

most to half its unloaded value. Assume that the impedance is 3000 ohms when loaded and 6000 ohms unloaded. The emitter impedance of 30 ohms then is transformed to 6000 ohms by the circuit. The capacitance ratio then is

$$(C_1/C_2)^2 = 30/6000 = 0.005$$

and the value of C_2/C_1 is 14:1. If then the unloaded Q-factor for the tuned circuit is 200 and loaded, 100, the inductance and capacitance for the tuned circuit are

$$\omega L = 1/(\omega C) = 6000/200 = 30;$$

$$\omega = 6.3 \times 10^7$$

$$L = 0.47 \mu\text{H}, C_1 = 529 \text{ pF}$$

Then, C_2 should have a value of about 7500 pF.

The extremely low impedance levels are clearly evident in terms of these capacitances. Because 30 ohms corresponds to approximately 33,000 μmhos forward conductance, the amplification obtained from an amplifier using this transistor is

$$K_v = g_f Z_L = 0.033 \times 3000 = 100$$

Since the step-down ratio in the coupling circuit is 14:1, however, the net gain is 7, not 10. To achieve a gain of 10, therefore, it is necessary to load the tuned circuit more heavily. This is most easily done by raising the collector impedance level (unloaded). If, for example, it is increased to 15,000 ohms, then the load impedance reflected from the emitter can be 3750 ohms instead of 6000 ohms, and the capacitance ratio is reduced to 11:1. The overall stage gain then is 9 and the loaded Q-factor is 40.

The use of the higher unloaded tuned impedance does not introduce difficulties due to regeneration because the emitter of the succeeding amplifier loads the tuned circuit regardless of its frequency setting. Consequently, the modified values for the components, again assuming an unloaded Q-factor of 200, are

$$L = 1.20 \mu\text{H}, \quad C_1 = 210 \text{ pF}, \quad C_2 = 2300 \text{ pF}$$

These values are appreciably more practical than those for the design with 6000 ohms unloaded impedance.

8-1.1 THE USE OF TAPPED COILS

Tapped coils may be used with amplifiers, and they are commonly used with oscillators for the reduction of the impedance level from collector to emitter. In this application, the unloaded impedance level is selected, and the tap is adjusted to reduce the impedance to the desired level. Tapped coils have the advantage that the change of current level is obtained magnetically rather than by way of the circulating current. Consequently, relatively lower Q-factor coils may be used effectively with large values of impedance step-down. The step-down in a tapped coil functioning as an auto-transformer is approximately proportional to the square of the turns-ratio

$$z_o/z_i = (n_o/n_i)^2 \quad (8-7)$$

Strictly, this equation applies only if the coefficient of coupling among the various turns of the coil is high,

and as a consequence, the leakage flux is small.

If a tapped inductor is used for the tuned circuit considered in Example 8-1, the tap should be placed at approximately 0.09 of the way along the coil from its supply end. (For an 11-turn coil, the tap should be placed one turn from the collector supply.) Because the coupling is relatively loose from one turn to another, the exact position for the tap must be found by trial and error.

8-1.2 OTHER COUPLING METHODS

Two remaining forms of coupling circuits are commonly used with transistor circuits, the first of which is the single-tuned transformer (Fig. 8-3), and the second, the double-tuned transformer (Fig. 8-4). With each of these transformers, the secondary, low-impedance winding is installed adjacent to the main tuned coil to provide magnetic coupling and signal transfer. Tuned lines may also be used for coupling elements.

The double-tuned transformer used with transistor RF amplifiers consists of one tuned high-impedance winding, and one low-impedance winding. The high-impedance winding is designed to have a relatively high loaded Q-factor, possibly 20% of the unloaded value, whereas the low-impedance winding is commonly designed to have a low value of loaded Q-factor, possibly as small as 2 to 5. Such an arrangement makes the tuning of only one of the circuits critical; the remaining circuit can be used over at least a 10 to 20% bandwidth.

The advantages of the transformer-coupled circuit over the simple tuned coupling circuit include ease of adjusting the bandwidth by variation of the tightness of coupling between the two windings, ease of signal injection compared to the tapped coil because of the absence of a high-capacity coupling capacitor, and ease of getting the appropriate turns-ratio compared to the tapped coil. Frequently, for example, it may be necessary to place a tap at a fraction of a turn on a tapped coil, whereas a tuned or an untuned coupling coil may have from several to many turns.

The design of the high-impedance winding follows the same procedure for both the single-tuned and the double-tuned transformers. The final value of the loaded Q-factor and the loaded impedance desired are selected, and the required inductance and capacitance

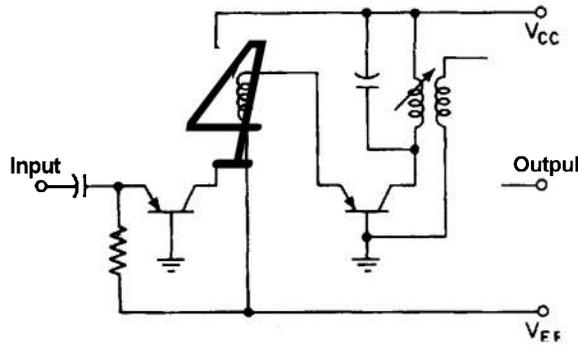


Fig. 8-3. Single-tuned Coupling Transformer Circuit

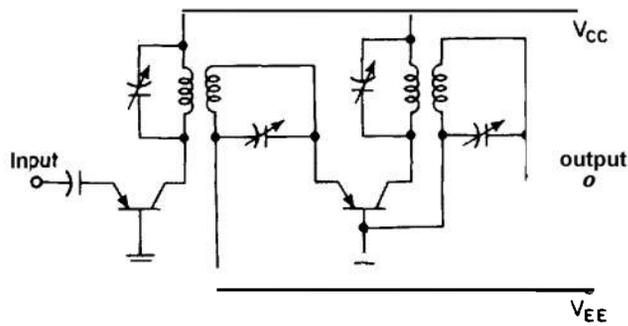


Fig. 8-4. Double-tuned Coupling Transformer Circuit

are calculated. The unloaded value of Q to be designed into the coil should be from a minimum of 4, to a maximum of 10 to 20 times the loaded value. Once the values of the inductances are known, the inductors may be designed by any of the standard methods.

The coupling inductor may be untuned, in which case its Q -factor is assumed to be unity, or it may be resonated with a capacitor, in which case its Q -factor lies in the range from 2 to 5. If the circuit is tuned, it may use either the series or parallel configuration as desired. For the series-tuned arrangement, the reactance of the inductor and its associated capacitor may be calculated from the equations

$$\omega L_C = 1/(\omega C_C) = Q_C/(g_{i'} + g_{f'}) \quad (8-8)$$

where the subscript C refers to the coupling components. Similarly, if the circuit is parallel-tuned, then the susceptances of the associated elements are given by the equations

$$\omega C_C = 1/(\omega L_C) = Q_C(g_{i'} + g_{f'}) \quad (8-9)$$

The respective circuits, with the transistor input represented by Y_i , are shown in Fig. 8-5.

Each of these circuits has certain advantages. The series circuit, for example, is excellent with regard to economy of parts, but at very high frequencies, a voltage step-down action from the effect of C_i and C_C must be taken into account. This is easily done, but it does increase the complexity of design somewhat. The parallel-tuned circuit, on the other hand, makes direct use of the input capacitance of the transistor as part of C_C , and as a result is easier to design at high frequencies. It may use more parts than the series-tuned circuit because of the DC path through the coupling circuit. In addition, because the reactance of the coil and capacitor are appreciably smaller in the parallel-tuned coupling circuit than in the equivalent series-tuned circuit, the problem of constructing an acceptable coupling inductor for use at very high frequencies may make the use of series-tuned circuits more convenient.

The untuned coupling circuit is normally designed for an approximate loaded Q of unity so that the coupling may be made as loose as possible. The coupling efficiency factor has an extremely broad maximum in the neighborhood of a reactance of the coupling coil equal to the terminating load impedance, with the result that relatively large changes of reactance can be tolerated without serious difficulties. When, however, an untuned coupling coil has an appreciable capacitive load component, then the value of inductance selected should be adjusted in accordance with the equation

$$L_c = L_{C1} / (1 + \omega^2 L_{C1} C_c) \tag{8-10}$$

where L_{C1} is the inductance determined from the equation $\omega L_{C1} = R_L$, R_L is the load resistance, and C_c the loading capacitance. The presence of the capacitance increases the effective value of the inductance, with the result that a smaller value of physical inductance is required.

After the designs of the tuning coil and the coupling coil, either tuned or untuned, are completed, the next step is the adjustment of the coupling to the correct value. This adjustment is easily made with the aid of a Q-meter, because adjusting the coupling circuit consists of moving the coil sufficiently close to the tuned coil to reduce its effective Q to the required value. The tuning capacitor C_L may be replaced by the tuning capacitor of the Q-meter for this adjustment, and any supplementary capacitance required for resonance may be placed in parallel with the capacitor in the measuring circuit. The combination is tuned to resonance and the Q measured. The coupling is adjusted to give the required value of Q at resonance.

The nominal value of coupling required for critical coupling is found in terms of the effective values of Q for the two tuned circuits. If the unloaded Q of the collector circuit is called Q_p , and the Q of the coupling circuit is called Q_c , then the critical value for the coupling k_c is given by the equation

$$k_c = 1 / \sqrt{Q_p Q_c} \tag{8-11}$$

If the coupling circuit is untuned except for the internal circuit and transistor capacitance, then Q_c may be taken as unity; otherwise it will be the loaded Q of the coupling link, normally between 2 and 10. The coupling for the tuned link can be as small as a half to a third the coupling required with an untuned link.

The form and the type of coupling circuit often must be selected on the basis of the physical configuration of the tuned circuit. For example, if it proves impossible to get sufficient coupling to use an untuned link, the design should be changed to use either a tuned link or a capacity divider. The capacity divider usually will prove satisfactory only if the total capacitance from emitter to ground is less than approximately 5000 pF and larger than the input capacitance of the transistor.

8-2 TRANSISTOR LOAD LINES

After the dynamic load impedance has been determined for the transistor amplifier, the design of the amplifier itself may be undertaken. The collector supply voltage for the amplifier may be selected based on the maximum voltage amplification permitted for the transistor, and if maximum operating characteristics at high frequency are required, a common-base circuit should be chosen. The voltage applied to a drift, or diffused-base, type of transistor in particular should provide as high a drift velocity as possible, consistent with the noise properties of the device. The selection of optimum operating conditions for an input amplifier stage is a critical operation, inasmuch as minimum noise conditions occur with a comparatively small collector supply voltage, yet a relatively higher voltage is required for maximum operating frequency.

The static load line is drawn at approximately constant voltage corresponding to the supply voltage and static resistance of the winding. Then the dynamic load

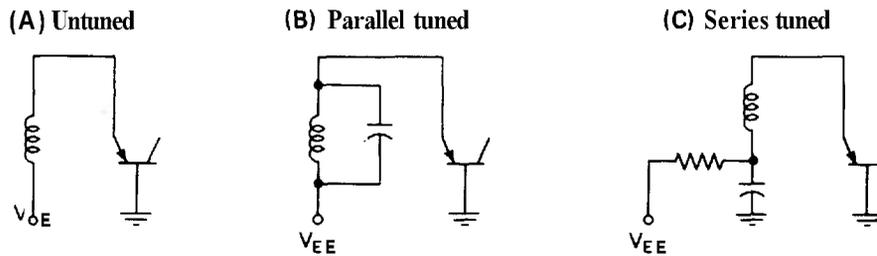


Fig. 8-5. Types of Inductive Coupling

line is plotted across it, intersecting it at the point corresponding to the desired forward conductance in the transistor. The slope of the load line should correspond to an impedance defined by the equation

$$Z_{LD} \cong (K_S)^2 / (g_{i'} + g_{f'}) \quad (8-12)$$

where K_S is the overall stage amplification from emitter to emitter or collector to collector, and $(g_{i'} + g_{f'})$ is the input admittance of the emitter of the common-base amplifier. The unloaded tuned impedance should be large compared to this value of Z_{LD} .

8-3 RELATIONS OF FREQUENCY LIMITATIONS

The various limiting frequencies used with high-frequency amplifiers are all related to one another through the basic transistor parameters, the current gain, the input and forward conductances, the base-to-emitter and base-to-collector capacitances, and the base-spreading resistance. Their relations are defined in par. 2-10.

It is desirable in connection with the design of high-frequency circuits to be able to determine to within a factor of at most 20% what the values of f_{\max} and f_{n2} are, inasmuch as they determine the points at which deterioration of the circuit behavior starts becoming serious, and where it becomes crucial. As long as the operating frequency is less than f_{n2} , the design procedure may be based on normal admittance techniques. At frequencies between f_{n2} and f_{\max} , the procedure is critical because of the low gain and the high noise levels.

If adequate data are known on a transistor, either of these frequencies may be determined directly, or they may be determined in terms of the value ω_{fb} , by the use of Eqs. 2-31 and 2-30. It is of interest to note that the two capacitances C_i and C_c play an extremely important part in the limitation of the maximum operating frequency f_{\max} whose value is

$$f_{\max} = [1/(4\pi)] \sqrt{g_{f'} / (r_b C_i C_c)} \quad (8-13)$$

This frequency f_{\max} is in reality a figure of merit of considerable importance for a transistor. A similar equation for f_{n2} may be derived

$$f_{n2} = [1/(2\pi C_i)] \sqrt{g_{i'} (g_{i'} + g_{f'})} \quad (8-14)$$

Either this equation or the equation in terms of ω_{fb} , is satisfactory for the determination of the noise-corner frequency.

It would appear reasonable to plot contours of constant value for the capacitances C_i and C_c on a family of characteristic curves as a means of presenting the data on the limiting frequencies. A sample of the form such a set of curves might take on a drift transistor is sketched in Fig. 8-6. It should be noted, however, that these curves are hypothetical and do not represent any specific transistor. These data in conjunction with the normal data provided on conductance data sheets should prove ample for design purposes.

8-4 NEUTRALIZATION AND UNILATERALIZATION

The neutralization of an amplifier is the process of introduction of compensating voltages or currents from output to input in such a manner as to prevent the direct exchange of energy between the input and the output. Unilateralization not only introduces compensating reactive components, but also compensating resistive components, so that the input and the output are completely isolated except for the amplification action in the active device.

The neutralization of the common-base amplifier is comparatively simple because the feedback elements of the device in this configuration are introduced solely by the base-collector capacitance, which is fairly stable in value, and the base-spreading resistance, which also is rather stable in value. In addition, the extremely small input impedance (large input admittance), coupled with the relatively low impedance isolating area in the base region reduces the effective coupling to a very small value.

The unilateralization of a common-emitter amplifier requires a more complex compensating network than is required for neutralization. At the same time, if properly adjusted, it provides better isolation. The common-base neutralizing circuit is a unilateralizing circuit as well, so that the common-base amplifier when properly neutralized shows complete isolation between its input and its output. The neutralization equation for the common-base amplifier is

$$C_n R_n = r_b C_c \quad (8-15)$$

where C_n is the neutralizing capacitance, connected from collector to emitter, and R_n is the neutralizing

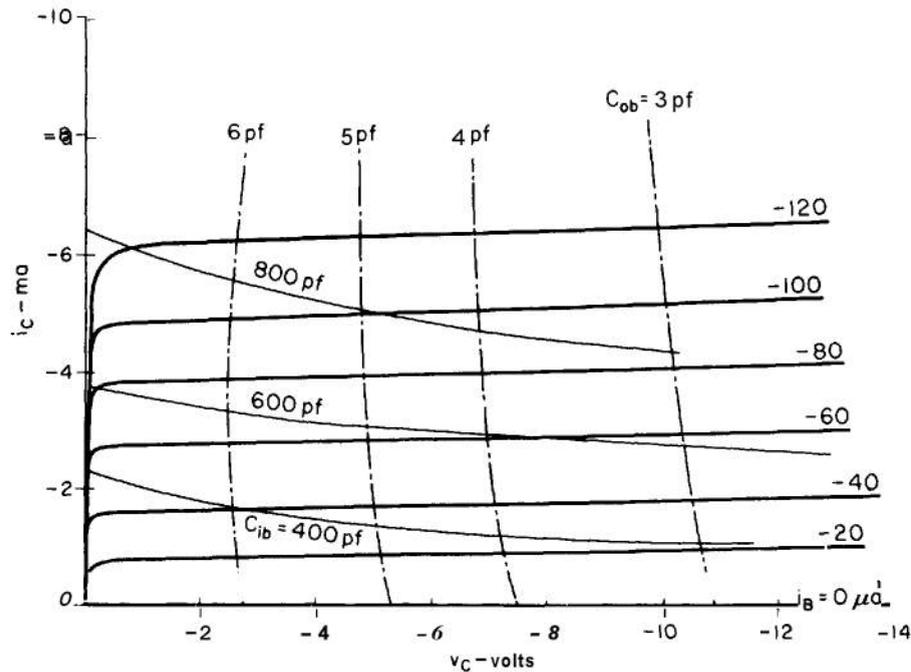


Fig. 8-6. Hypothetical Capacitance Contours

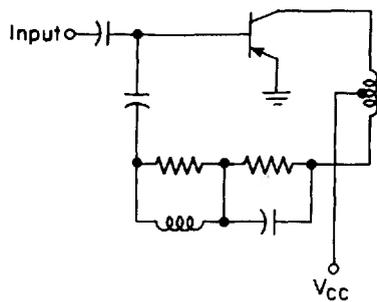


Fig. 8-7. Common-emitter Unilateralizing Circuit

resistance, connected from the emitter to ground, the base-return terminal.

Unilateralization of the common-emitter amplifier requires in addition to a set of R , L , and C components, an ideal transformer for the inversion of the phase of the feedback signal (Ref. 1). The circuit and the sizes of the components are defined in Fig. 8-7. If the equation for the input admittance is separated into input components and transfer components, and the transfer components are balanced out by their negatives, the stage is then unilateralized. Based on the equation

$$Y_i = y_i(1 + y_c R_L) / [1 + y_o R_L + y_i y_c (1 + y_c R_L)] \tag{8-16}$$

The denominator may be simplified by taking advantage of the relations

$$y_o R_L < 1 \quad y_c R_L < 1$$

The equation then takes the form

$$Y_i = y_i(1 + y_c R_L) / (1 + y_i r_{b'}) \tag{8-17}$$

The numerator term involving y_c may be replaced by the complete A factor, and only the transfer term retained, because from above, $y_o R_L < 1$

$$Y_i = [y_i(1 + y_o R_L) - y_f y_r R_L] / (1 + y_i r_{b'}) = [y_i - y_f y_r R_L] / (1 + y_i r_{b'}) \tag{8-18}$$

This is one of the few applications in which the use of the modified output admittance is less convenient than the basic form. This equation may be further simplified

by separating the two numerator terms, and then examining the significance of the result

$$Y_i = y_i/(1 + y_i r_b) - y_r(y_f R_L)/(1 + y_i r_b) \quad (8-19)$$

Evidently, if an immittance term is added that will identically cancel the second term on the right, the y_r term, then all that will be left is the input admittance resulting from the input circuit and the interaction of the input and the output, will be zero. The $y_f R_L$ term gives the internal gain in the transistor, and indicates that, as is already known, the voltage applied to the unilateralizing circuit must equal the output voltage of the amplifier. This makes necessary the use of an ideal, or unity-ratio, correction transformer. Then the balance of the equation gives the admittance that must be placed in the return path

$$y_u = y_r/(1 + y_i r_b) = 1/(1 + y_i r_b)/y_r \quad (8-20)$$

$$= 1/[(1 + g_i r_b + j\omega C_i r_b)/y_r]$$

$$= \frac{1}{\frac{1}{\frac{g_r + j\omega C_c}{1 + g_i r_b}} + \frac{1}{j\omega C_i r_b}} \quad (8-21)$$

The fact that y_r would represent the feedback admittance can easily be recognized because the amplification of the transistor causes the application of a relatively large signal voltage compared to the base voltage across the voltage side of y_r , and the comparatively high admittance from base to ground would cause an admittance that was connected between collector and base to act as a current source. As a result, the collector-to-base admittance and y_r may be taken as equivalent to one another with ordinary transistors.

The admittance elements that must be used in the feedback path in addition to the unity-ratio transformer have the values

$$g_r/(1 + g_i r_b); \quad C_c/(1 + g_i r_b) \\ C_c/C_i r_b; \quad g_r/C_i r_b \quad (8-22)$$

where the first and third are conductances, the second a capacitance, and the fourth an inductance. The first pair are connected in parallel, and the second pair are likewise connected in parallel. With the exception of

r_b , which is relatively constant, all of the basic elements, g_r , g_i , C_i , and C_c are a function of the operating conditions for the transistor. As a result, the conditions for unilateralization of the common-emitter amplifier are rather critical.

Since the value of g_r is extremely small, the first and fourth terms often may be negligible, and the circuit reduces to a series R - C circuit consisting of

$$C_c/C_i r_b \quad \text{and} \quad C_c/(1 + g_i r_b)$$

respectively.

8-5 CONTROL OF AMPLIFICATION

The automatic control of amplification in a transistorized amplifier, particularly one which is tuned, is a complicated process because of the variation of the input admittance of the transistor with its operating conditions. If the design can be made in a way that reduces the effect of the variations to a point that they may be neglected, then control is comparatively simple. When, however, the variations of input admittance have important effect on the behavior of the tuned circuits, then the process of design is of increased complexity.

The first question that must be considered in the establishment of transistorized amplifiers having automatic control of amplification is the determination of operating conditions required for varying the amplification. Superficially, the control of power amplification may be obtained either through the control of current amplification or voltage amplification or both. The current amplification for a transistor is relatively independent of the operating conditions from low current to high current. Consequently, the variation of amplification cannot be obtained through variation of current gain, but must be obtained by variation of voltage gain. Because the forward conductance of a transistor is approximately proportional to the current passed, it is necessary to have a current change of 10 to 1 to develop an amplification change of 10 to 1, and it is also necessary that the load impedance presented by the input terminals of the transistor not vary appreciably.

The input admittance of the transistor normally varies considerably with current, making necessary the loading of the input circuit with a fixed resistance if the input impedance is to be kept reasonably constant. This loading also keeps the bandwidth of the driving amplifier relatively constant as the operating conditions for the transistor change with signal level. This does

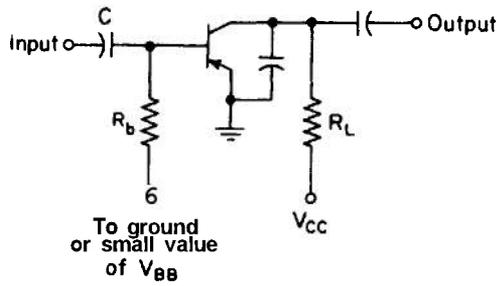


Fig. 8-8. Transistor Detector

not correct for the variation of input capacitance, however.

The design of the transistor circuitry to accommodate a varying control current as a function of signal level requires an amplitude detection circuit which can determine the approximate magnitude of the output signal level, and a control circuit that reduces the current in the various transistors as the detection circuit indicates increasing signal amplitude. Such a circuit may include a special isolation amplifier followed by a detector circuit and a DC control amplifier. The DC control amplifier may be required to have considerable amplification and appreciable power output because control of transistor amplifiers requires significant amounts of power.

An isolation amplifier operating at the normal operating frequency of the main amplifier is used to prevent the control detector from introducing a nonlinear loading onto the signal circuits. Normally this amplifier may be of the common-emitter type, particularly if its input is paralleled with the input to a common-base amplifier in the signal circuit. Detector loading should further improve the stability.

Either a diode detector, or a transistor functioning as a detector-amplifier, may be used for the detection function. Both of the circuits function in a similar manner, in that the base-emitter junction for the transistor provides the rectification when the transistor performs both functions. The rectification efficiency is reduced when both functions are combined in a transistor, however, because with separate elements the diode polarity may be such as to shift the static or DC level toward the active voltage level, whereas the base-diode rectification in the transistor is not really satisfactory because of its tendency to bias the transistor in the off direction instead of the on (Fig. 8-8).

The type of control amplifier required for regulating the characteristics of the variable-gain amplifier depends on the method selected for introducing the con-

trol. Because power is required for this function, the selection of the configuration requiring the minimum input power to the regulation circuit provides the maximum operating efficiency for the overall circuit. For this reason, the control signal is usually introduced into the base terminals. The only other possible selection, emitter control, requires up to 100 or more times as much current, and therefore would make the control power required excessively large.

The control of the amplifier current through the limitation of the base current may readily be accomplished by having the control circuit limit the total voltage applied to the respective bias resistors. A simple circuit for accomplishing this is shown in Fig. 8-9. In this circuit, the control voltage increases or decreases the total current flowing through the regulating transistor, thereby altering the voltage developed across its load resistance and changing the amount of base current available for the amplifier connected to it.

The control amplifier may be converted to a practical circuit by modifying it as shown in Fig. 8-10. In this modification, the output voltage obtained from the control amplifier is repeated by an emitter-follower, and the emitter-follower then controls the individual amplifier stages. This modification is advantageous in several ways. First, it permits the control amplifier itself to operate at comparatively small currents, and limits the loading that must be reflected on the detection circuit. Second, it makes the output admittance of the actual control circuit high because of the emitter-follower configuration that is used. The power amplifier then is self-stabilizing because of the degeneration. Third, the high output admittance of the follower helps the shunt capacitance to isolate the controlled stages from one another and helps to minimize the possibilities of regeneration.

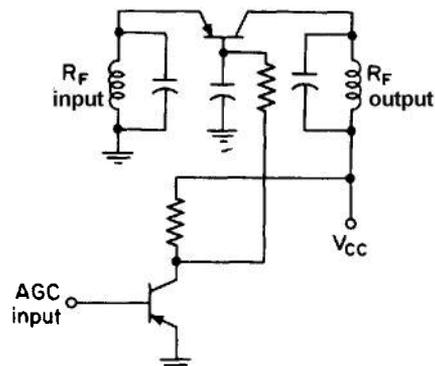


Fig. 8-9. Amplifier With AGC

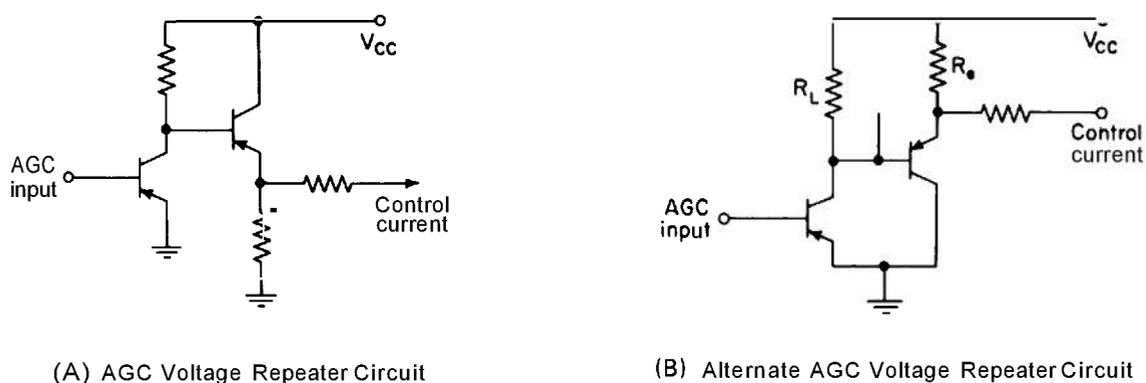


Fig. 8-10. Use of Transistor Polarity to Control Emitter-follower

Either polarity of transistor may be used for the control emitter-follower, because either of the configurations Fig. 8-10(A) or Fig. 8-10(B) will provide the required control. The use of a transistor of similar polarity to that of the amplifier transistors causes the follower to pass maximum current when the amplification of the amplifier is a maximum, providing high filtering action at the control point. At the same time, all of the base current for the amplifier transistors must flow through the control transistor using this configuration.

When the emitter-follower transistor and the amplifier transistors are of opposite polarity types, the control current is diverted through the emitter load rather than through the amplifier transistors, the output admittance of the emitter-follower is lower than can be obtained when both transistor types are the same. The current efficiency as a result is reduced, but the total power required for adjustment of amplification is increased because the control transistor draws current to divert it from the amplifier circuit.

EXAMPLE 8-2. Design a common-base amplifier using a 2N247 transistor, and provide a design having a range of amplification between 3 and 10.

The first step in design of this amplifier is to select the range of current that is to flow in the emitter circuit, and to select the corresponding range of base current. The effective input admittance of the amplifier at its emitter is approximately $35 i_e$ mhos, for an input resistance of 10 ohms with an emitter current of 0.003 A. If a shunt emitter load of 10 ohms is used, then the emitter current must be reduced in accordance with the equation

$$x/(1+x) = K_{\min}/2K_{\max} \quad (8-23)$$

This equation assumes that half of the available signal power is dissipated in the emitter loading resistance at minimum input signal. If the maximum amplification is taken as 10, the minimum 3, then the minimum value of x required is 3/17, and the minimum emitter current is 0.53 mA.

The approximate ratio of base current required, minimum amplification to maximum, is 3/17, or 0.176. The maximum value of the base current required to produce a collector current of 3 mA is 50 μ A. The control amplifier to use with the RF amplifier stage should develop a collector voltage change from approximately the supply voltage to a value approximately 15% of the supply voltage.

In applications in which the best possible signal-to-noise ratio is required, it is necessary that the input transistor itself absorb the majority of the available signal power with weak signals, and the parallel input load absorbs increasing amounts of power as the signal strength increases. In such an instance, the supplementary input load resistance should be 2 to 5 times the minimum input resistance of the transistor itself. Instead of a shunt resistance of 10 ohms, as has been selected, the shunt resistance should be between 30 and 50 ohms. The range of change of amplification is reduced in exchange for a higher sensitivity for weak signals.

8-5.1 THE EMITTER-FOLLOWER

The design of the emitter-follower providing the base current to the series of amplifiers is relatively conventional, the only critical feature being the selection of operating conditions capable of supplying an adequate magnitude of current at the required voltage. If the circuit of Fig. 8-10(A) is used, all of the emitter current flows into the base circuits of the transistors being con-

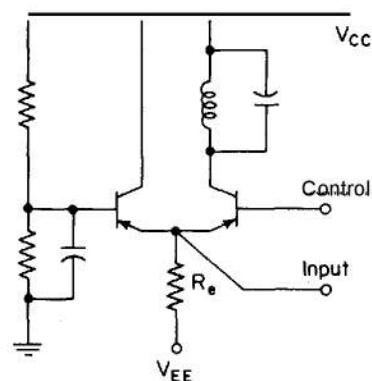


Fig. 8-11. Balanced RF Amplifier

trolled, and the power dissipated in the transistor is kept to a minimum consistent with reliable operation. With the circuit of Fig. 8-10(B), however, the current drawn by the transistor must be large compared to the control current, or the voltage cannot be reduced to an adequately small value. The power economy of (A) is considerably superior to that of (B).

8-5.2 OTHER RF CONFIGURATIONS

There are two important difficulties encountered with RF circuits of the type described thus far. The first, and probably the more important, is the variation of the input capacitance with operating current in the transistor. This makes the tuning of the amplifier vary with the operating conditions, and consequently can have serious consequences. The second factor is the variation of the input conductance with the operating point. This condition can be corrected for by the use of the loading resistance as described, but the total load conductance will vary with operating conditions, and the circuit Q-factor and tuning both will vary with voltage.

A differential-type amplifier (Fig. 8-11) can be used to correct for this situation, because the input circuit of a second transistor may be paralleled with the signal transistor and so connected that the conductive load and the shunt capacitance will remain relatively constant, but at the same time the collector current in the signal transistor can vary as required to provide the necessary variation of amplification. This amplifier can develop full sensitivity with weak signals, yet be readily controlled without the use of a shunt-static load. Such an arrangement *can* yield a high sensitivity and a relatively low distortion level.

The base voltage change that must be developed to shift the collector current from about 0.3 mA to 3.0

mA, or a base current from 5 to 50 μA is about 65 mV. Because signal is not introduced on the base lead with this circuit, voltage control can be used, particularly with a differential amplifier. The voltage applied on the AVC lead in Fig. 8-11 should have a polarity to cause the loading transistor to draw increased current as the input signal increases.

8-6 TUNNEL DIODE AMPLIFIERS

Tunnel diodes can be used as amplifiers because their negative conductance can be introduced to neutralize a portion of the positive resistance in an associated tuned circuit, thereby increasing the effective Q of the circuit.

The utilization of a negative-impedance device as an amplifier is possible only under very restricted conditions, because it is necessary for the device to provide most but not all of the energy required by the circuit losses. This means that the maximum value of the negative impedance, as a function of the control parameter, must be slightly less than the value of the circuit positive impedance. With NA devices like tunnel diodes, the diode must be inserted in shunt with the tuned circuit for this criterion to be fulfilled. The impedance level of the circuit must be adjusted to a value such that the net conductance is slightly positive. This is the reason a knowledge of the maximum value of the negative conductance of the active device is important.

The tunnel diode is the only wide-band negative conductance device at present available. Because of its wide-band properties, a circuit that is designed to be stable at a desired frequency can easily be oscillatory at another frequency in the spectrum (usually a higher frequency). Control of these spurious oscillations is one of the major problems in the utilization of tunnel diodes.

The maximum oscillation frequency for the tunnel diode when used as an amplifier of necessity must be considerably higher than its amplifying frequency. Consequently, the problem in circuit stabilization is one of preventing a net negative conductance at a higher frequency when the required amount of positive conductance is available at operating frequency.

Because of this situation, the tunnel diode is best used as a shunt loading element on a coaxial line. If the output end of the line is terminated resistively with a wide-band resistance, or one which decreases to a small value off resonance, then the likelihood of oscillation developing is minimized. Other than for the use of a parallel-tuned circuit as a load, a possible arrangement for assuring adequately small impedance at high frequency is the use of an additional loading resistance, as

shown in Fig. 8-12. In this figure, the potentiometer arrangement is used to adjust the bias to the critical level, and the RF choke is used for the introduction of the bias. The total resistance in this circuit must be kept small, or the adjustment of the bias voltage to the negative-resistance region (between 0.07 and 0.30 V for germanium) cannot be made.

The damping circuit for suppression of high-frequency gain may be placed across the diode terminals. With such an arrangement, the damping resistance should be a fraction of the nominal load impedance, and it should be isolated by a coupling capacitance of such size that the loading of the damping resistance can be neglected at the operating frequency.

Suppression of oscillation in tunnel-diode amplifiers is sufficiently difficult that it is desirable to make use of the oscillation if possible. Some techniques are under development for doing this, and it may also be done with converter circuits. Until many of these problems are solved, the main application of tunnel diodes will be in the field of switching circuits. Experiments made by the author have shown that amplification can be obtained using the circuit of Fig. 8-12, but the amplification compared to direct output with the diode removed from the circuit has been only about 3 times. Compared to the value with the diode loading the coaxial cable, however, the overall amplification is approximately 10 to 20 times.

8-7 SUMMARY

Although the emphasis has been placed on individual stages in this chapter, conventional techniques may be used to develop stagger-tuned amplifiers, But-

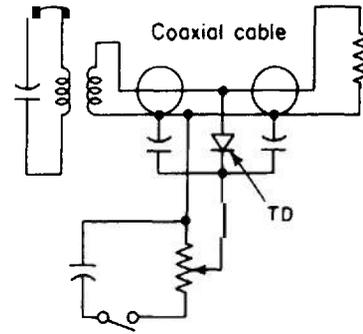


Fig. 8-12. Tunnel Diode Amplifier Circuit

terworth amplifiers, and similar configurations. For small-signal stages in which the small-signal parameters show essentially negligible change with the input signal, conventional design techniques, described in this chapter, apply. The frequencies and the Q-factors of the individually tuned circuits may be determined, and the transistor loading may be varied to help in the adjustment of the circuit to optimum band-pass characteristics. The amplifier must be of the fixed-gain variety in order that the equalization will not vary over the passband with changing signal levels.

For larger values of signal, when the parameters do vary appreciably with the instantaneous signal voltage, the method of design for variable-source-load impedances described in Chapter 7 may be used. In this instance the loading is averaged and the curved load lines, starting at the output are plotted back from stage to stage. Eventually a stage is reached at which linear techniques apply. The reader should not experience any difficulty extending the techniques described to such amplifiers.

REFERENCE

1. C. C. Cheng, "Neutralization and Unilateralization", IRE Trans., *PGCT*, June 1955, p. 138.

CHAPTER 9

NONLINEAR THEORY OF OSCILLATORS

9-0 INTRODUCTION

The development of effective procedures for design of oscillators must of necessity be based on a nonlinear or a piece-wise-linear approach, and should relate the limit-cycle characteristics in the phase plane to the overall behavior of the circuit. The discussion in this and the next two chapters is an expansion and an extension of the discussion of the principles of oscillator design published in *Conductance Design of Active Circuits* (Ref. 1). Because the procedure for design of oscillators must be developed from the basic nonlinear properties of the amplifying device in conjunction with the linear or nonlinear properties of the remainder of the circuit, the first chapter of the group discusses the nonlinear analytic procedures on which practical design work is based. This chapter is followed by one in which designs for L-C and crystal oscillators are developed and one in which practical designs for R-C and time-delay oscillators are developed. The discussion in Chapters 9 and 10 is concerned with four-terminal oscillators exclusively. Negative immittance operation is considered in connection with time-delay oscillators in Chapter 11.

9-1 CONDITIONS FOR FOUR-TERMINAL OSCILLATION

The development of an oscillating condition in an electronic circuit requires first that the output power at the frequency of oscillation be greater than the amount of power required to produce it, or there must be power gain in the active device. When this condition can be met, the following additional conditions must be fulfilled:

1. Operating conditions must be such as to minimize noise modulation.
2. The frequency-selection circuit must be properly designed.
3. The overall phase-shift in the circuit must be an integral multiple of 360 deg.

In addition to the frequency-amplitude restrictions, there are amplitude-time relations that must be satisfied, the exact relations depending on the type of operation desired. For sinusoidal or continuous-wave oscillators, the following additional conditions apply:

4. The amplification averaged over a single sinusoidal cycle, for stable operation, must be unity.
5. The instantaneous variation from unity must be as small as possible.
6. Sufficient amplification margin must be available at initiation to assure oscillator starting.

These conditions define the required properties for the final circuit and also indicate the design procedures that must be used.

9-1.1 MAXIMUM OSCILLATING FREQUENCY

The maximum oscillation frequency is that frequency for which a power gain of only unity, and no more, may be obtained from the active device. Mason (Ref. 2) has shown that this frequency f_{\max} is determined by the equation

$$U = |y_{21} - y_{12}|^2 / [4 \operatorname{Re} (y_{11}y_{22} - y_{12}y_{21})] \quad (9-1)$$

Drouillet (Ref. 3) has taken this basic relation to derive the maximum frequency of oscillation in terms of the normal parameters of the transistor. In the equation for U , the various y and g parameters are the overall values for the transistor as a whole, including base-spreading resistance and emitter and collector series resistances and their associated reactances. The maximum frequency is given by the condition for which Eq. 9-1 has a value of U of unity. The value of the numerator is

$$|y_{21} - y_{12}| = [g_i^2 / \{(1 + g_i r_b')^2 + (b_i r_b')^2 - \omega C_c\}^2]^{0.5} \quad (9-2)$$

Near the limiting frequency, $b_i r_b' \gg 1$ and $b_i r_b'$

$g_i r_{b'}$. In addition, the value of y_{12} is small in magnitude compared to that for y_{21} , and Eq. 9-2 reduces to

$$|y_{21} - y_{12}|^2 \doteq [g_{f'} / (b_i r_{b'}) - \omega C_c]^2 \tag{9-3}$$

$$\doteq [g_{f'} / (b_i r_{b'})]^2$$

Eq. 9-1 may be simplified by the help of this relation to read

$$[g_{f'} / (b_i r_{b'})]^2 = [4g_{f'} / (b_i r_{b'})] \times \omega C_c U \tag{9-4}$$

Setting $U = 1$ and $\omega = \omega_{\max} = 2\pi f_{\max}$ gives

$$\omega_{\max}^2 = g_{f'} / (4C_i C_c r_{b'}) = \alpha_o f_{\alpha} / (4C_c r_{b'}) \tag{9-5}$$

The resulting value of f_{\max} is

$$f_{\max} = [g_{f'} / C_i C_c r_{b'}]^{0.5} / (4\pi) \tag{9-6}$$

9-1.2 THE EFFECT OF NOISE

The initiation of oscillation in an oscillator is a result of the effect of thermal noise (and other forms of noise) shock-exciting the oscillator circuit, changing the overall amplification and affecting the phase stability at the same time. Consequently, in oscillators that must meet extreme requirements on frequency stability, it is essential that the transistor used have as small a noise signal voltage as possible, one having an upper noise corner frequency f_{n2} appreciably above the operating frequency for the circuit. In addition, the operating conditions selected for use with it should introduce a minimum of noise.

9-1.3 LOOP-AMPLIFICATION CONDITIONS

The forward conductance of the active device in the oscillator must be sufficiently large that, at the time of initiation, the overall amplification of the circuit is greater than unity. Also, as the oscillation develops, this amplification must gradually decrease until it stabilizes at an average value of unity as the output stabilizes itself. This average amplification of unity around the feedback loop through the active device and back through the return path can only be obtained by allowing the instantaneous amplification to vary somewhat, rising on one polarity of output, and decreasing on the other. For example, if a parallel L - C tuned circuit is

used as the output (or collector) load for the active device, and K_s is the feedback gain (strictly a loss), the equation for the loop gain may be written as

$$Y_f K_s (R + sL) / (s^2 LC + sCR + 1) = 1 \tag{9-7}$$

where Y_f is the forward admittance of the active device, L , R , and C are the component values for the tuned circuit, and s is the familiar Laplacian complex frequency (Fig. 9-1). In this equation, a considerable simplification may be obtained by making the substitutions

$$Y_f Z_L K_s = K \tag{9-8}$$

$$Z_L = L / (CR) \tag{9-9}$$

Eq. 9-7 then reads

$$K [1 + R / (sL)] / [1 + sL / R + 1 / (sCR)] \tag{9-10}$$

Now, the Laplacian operator may be replaced by the real-frequency operator that applies under oscillatory conditions. Then the following substitutions apply

$$s = j\omega = j(\omega_o + \Delta\omega) \tag{9-11}$$

$$\omega_o = [(1/LC) - R^2/L^2]^{0.5} \tag{9-12}$$

$$\omega = [1/(LC) - (1 + K)^2 R^2 / (4L^2)]^{0.5} \tag{9-13}$$

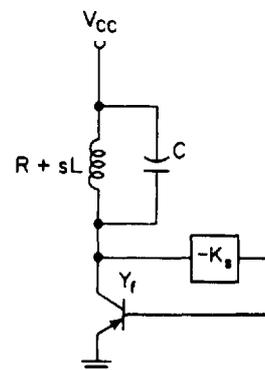


Fig. 9-1. Basic Oscillator Circuit

where Eq. 9-12 applies if $K = 1$, and Eq. 9-13 when $K \neq 1$. If, now, the change of frequency $\Delta\omega$ is determined in magnitude as a function of AK , keeping only the real-frequency term, the partial difference with respect to K is*

$$\begin{aligned} \Delta\omega/\Delta K &= (R^2/L^2 + j\omega R/L)/ \\ &[-2\omega + j(1 - K)R/L] \quad (9-14) \\ &\doteq -\omega_0/(2Q^2)* \end{aligned}$$

where Q is the loaded quality-factor of the tuned circuit including any and all circuit loading effects, both linear and nonlinear. Consequently, the shift of frequency is proportional to the change in amplification experienced over the oscillating cycle.

The variation of the frequency of oscillation with the operating conditions for an oscillator is a function of the amplification, and through the amplification, of the collector voltage and the emitter or the base current. It is a function of the effective resistance of the tuned circuit, and that resistance is a function of the coupled loads reflected on the tuned circuit from the input and the output circuits of the active device. These components are usually taken into account through the use of a shunt conductance such as G_d in Fig. 9-2. This equivalent loading conductance is introduced across a portion of the inductance of the tuned circuit with the aid of an ideal transformer having a turns-ratio K_s . (The ratio K_s may have the value of unity.) The total value of G_d is a function of g_i, g_f, g_r, g_o, r_b , and also any external loads required in the extraction of signal from the oscillator. Assuming that G_d has been calculated from the transistor data by the equations in Chapter 4, the equation for oscillation for the circuit is**

*Only the real terms have a significant effect on real frequency. The damping is a function of ω/Q .

**The transfer impedance Z_t may be derived topologically to be

$$\begin{aligned} Z_t &= sK_s L / [1 + sC(R + sL) \\ &+ K_s^2 G_d (R + sL) - sCG_d (L_1 L_2 - M^2)] \end{aligned}$$

where the primary inductance $L_1 = L$, the secondary inductance $L_2 = K_s^2 L$, and the mutual inductance is $K_s L$, giving the conditions for unity coupling in the transformer.

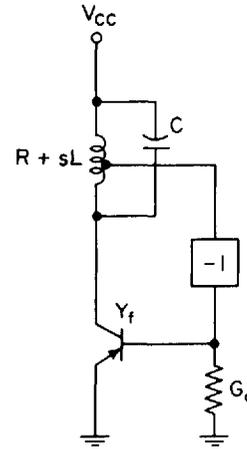


Fig. 9-2. Oscillator With Conductive Load on Feedback Network

$$\begin{aligned} s^2 LC + s(G_d L K_s^2 + RC - Y_f K_s L) \\ + 1 + G_d R K_s^2 = 0 \end{aligned} \quad (9-15)$$

If this is changed into the frequency-and-damping form, the result is

$$\begin{aligned} -\omega^2 LC + j\omega(G_d L K_s^2 + RC - Y_f K_s L) \\ + 1 + G_d R K_s^2 = 0 \end{aligned} \quad (9-16)$$

The required value of Y_f is directly proportional to the loading introduced by the conductance G_d , which is determined largely by the input conductance. With a transistor, the values of G_d and Y_f are nearly proportional over a moderate range of base and collector currents, with the result that if the $K_s^2 L$ term is large compared to RC , the circuit cannot be stabilized easily by variation of the operating point. Stabilization from action of the transistor itself requires that $K_s^2 G_d L$ have a magnitude approximately equal to the value of RC , and $Y_f K_s L$ must equal the sum of $K_s^2 G_d L$ and RC .

The frequency of operation for the oscillator of Fig. 9-2 is given by the equation

$$\omega = [1/(LC) + G_d R K_s^2 / (LC) - \langle K_s (G_d K_s - Y_f) / C + R/L \rangle^2 / 4]^{0.5} \quad (9-17)$$

Once again, the rate of change of ω with variation of either Y_f or G_d may be determined by taking the appropriate partial derivative. These partials are

$$\begin{aligned} d\omega/dY_f &= -K_s [K_s Y_f L - G_d K_s^2 L - RC] / (4\omega_0 C^2 L) \\ d\omega/dG_d &= RK_s^2 / (LC) - \langle K_s (G_d K_s - Y_f) / C + (R/L) \rangle K_s^2 / (2C) \end{aligned} \quad (9-18)$$

Proper use of these equations can permit at least a minimization of the frequency error due to the variation of transistor parameters. Clearly, the smaller the value of K_s , (the higher the step-down ratio), the smaller will be both of these errors. This condition is consistent with the use of the transistor in the conductance mode, with a voltage, or low-impedance source, and a current, or high-impedance output on the active device.

The amplification requirements may be summarized as follows. First, on initiation, the loop amplification must be appreciably greater than unity to assure reliable starting, and it must adjust itself to unity smoothly as the amplitude increases. The variation of amplification from cycle to cycle must be less than the variation over a given cycle of sinusoidal signal to assure a constant amplitude output. Secondly, the amplification over the operating cycle should vary as little as possible from the average value of unity if frequency stability is of prime importance. The mean-square variation of frequency should be minimized as a function of variations in the operating point, amplification, and input and transfer admittances.

9-1.4 CHARACTERISTICS OF THE FREQUENCY SELECTION CIRCUIT

The function of the frequency-selection circuit is to limit the range of frequencies over which the loop gain may approach unity to the range over which the oscillator is to operate. The frequency-selection circuit may consist of a tuned circuit with appropriate impedance-matching circuits, or it may consist of an R-C type delay circuit with appropriate matching circuits. It

could also consist of an appropriately designed delay line to generate a repetitive signal through time-delay action.

Because of the nature of resonant circuits, the fact that the region of maximum response has appreciable frequency width, the oscillating frequency is controlled by the time delay required to match the input and the output phase. This matching is required to provide energy reinforcement, just as the escapement in a watch or a clock must introduce a pulse of energy into the pendulum or the balance wheel at precisely the correct instant to maintain oscillation. The rapidity of the shift of phase across the resonant peak determines the rate-of-change of feedback phase with frequency, thereby limiting the maximum frequency deviation. Consequently, as shown in Eqs. 9-14 and 9-18, the percentage range of frequency error is an inverse function of the Q-factor of the tuned circuit, it being defined for Fig. 9-2 by Eq. 9-14.

In some types of oscillators, the inductance that has the components $R, j\omega L$, is replaced by the series combination of an inductance and a capacitance L' and C' the total series impedance being

$$Z_s = R + j\omega L' + 1/(j\omega C') \quad (9-19)$$

If this combination is substituted for $R + j\omega L$ in the oscillator equations, and the new equation is solved for the Q-factor, the result, if $L' = 10L$; $R' = 10R$; $C' = C/9$ is*

$$Q = [\omega_0 L' - 1/(\omega_0 C')] / R' = [L'/C]^{0.5} / (10R) \quad (9-20)$$

If, therefore, the Q-factor of the higher-inductance coil is the same as that of the smaller, then the overall effective Q of the circuit is severely limited. Unless the effective Q of the higher-inductance coil is much larger

*Clearly, although the net reactance is unchanged, the circuit damping has increased, for the same coil Q-factor, by the ratio L/L' . The rate of change of reactance with frequency has increased from L to $L' + L/(\omega^2 C') = 2L'$. The net effect is a negligible change in the rate-of-change of phase compared to the simpler circuit.

than for the smaller, no benefit can be obtained. Normally, the losses in the active circuit are much larger than the losses in the tuned circuit, with the result that the most beneficial change is a reduction of the overall impedance level of the coupling circuit.

It is impossible to separate the consideration of frequency and phase in any oscillator, because frequency is a measure of the rate of change of phase. The variation of frequency generated by circuit noise in an oscillator carries with it a corresponding shift of phase, and the net instantaneous phase at any moment is the phase sum of the noise phase and the signal phase returned through the feedback path. As a result, the higher the rate of phase progression across the peak of the response curve of the tuned feedback circuit, the smaller the total effect of random phase, and the more stable the frequency from the oscillator. Nonuniformity of amplification over the period of the sinusoidal wave also introduces a phase error into the returned voltage that, by reducing the voltage reinforcement in the tuned circuit, makes the phase progression less stable and consequently the frequency less stable.

9-1.5 EFFECT OF VARIATION OF AMPLIFICATION

The calculation of the effect of variation of amplification can be made by the use of statistical techniques supplemented by the inclusion of a term that gives the equivalent effect of the periodic variation. Because the amplification varies about a mean of unity, the first moments of the signal must have an average of zero when measured about a loop amplification of unity. For this reason, only moments of second or higher order need be considered. The most important of these

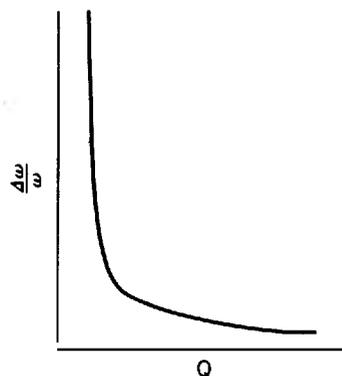


Fig. 9-3. Relation of $\Delta\omega/\omega$ to Q

is the mean-square deviation, which is defined in terms of the equation

$$\overline{\Delta K_e^2} = \overline{(K_L - 1)^2} \quad (9-21)$$

where the averaging may be carried out over some integral number of cycles of the output frequency.

The process of achieving both the condition of unity average loop amplification and a minimum value of $\overline{\Delta K_e}$ is of considerable importance, since both conditions must be satisfied simultaneously for maximum frequency stability. If the variation of amplification with input signal voltage is exactly linear, it is impossible to adjust the average amplification directly to unity unless there is a sharp discontinuity from the linear relation at one limit, or unless some device sensitive to signal voltage or power is incorporated to introduce a variation. Such an action may be accomplished by an automatic gain-control circuit or through the use of a power-sensitive device such as a thermistor to control the sensitivity of a bridge in terms of the signal power applied to one of its elements. If there is some curvature in the relation between amplification and signal voltage, then the development of a self-limiting condition can occur if the decrease in amplification for one signal polarity has a greater effect on the average amplification than the increase with the other polarity. If the effects exactly offset one another, or an increase of net amplification results, then unstable operation results, and the oscillator will tend to pulse or squegg.

With most of the conventional tube oscillators, a linear variation of amplification in conjunction with a sharp break introduced by grid rectification is used to provide linear operation and amplitude limiting. With transistor circuits, however, this arrangement may not be available to the designer because a low-impedance signal source is required for the control element, and no condition of a sharp break of the sort shown in Fig. 9-4 can readily be provided. Consequently, with transistor oscillators, it is necessary to take advantage of a second-order nonlinearity that reduces the average amplification, and a design procedure of substantially increased complexity is required as a result. For this reason, although the basic techniques explained in Chapters 7 and 11 of Ref. 1 apply to transistor oscillators, considerable extension is required to clarify the procedure.

The mean frequency deviation of the oscillator from its nominal operating frequency may be expressed in terms of the equation

$$\overline{\Delta\omega_\sigma}/\omega_o = \overline{\Delta K_\sigma}/(2Q^2) \tag{9-22}$$

where $\overline{\Delta\omega_\sigma}$ is the rms deviation of the instantaneous frequency from its nominal value, and $\overline{\Delta K_\sigma}$ is the rms deviation of the amplification. Strictly, these values include not only the nonlinearity of the amplifier itself as a result of the signal voltage, but also that due to noise as amplified in the circuit. The latter produces a random deviation of phase with time. Consequently, the $\overline{\Delta K_\sigma^2}$ term should be divided into at least two parts

$$\overline{\Delta K_\sigma^2} = \overline{\Delta K_{\omega\sigma}^2} + \overline{\Delta K_{N\sigma}^2} \tag{9-23}$$

where the sum of the squares relation is necessary since the correlation between the sinusoidal signal and noise is zero.

In practical applications, a nonzero derivative of frequency with time makes necessary a broadening of the bandwidth required for transmitting a signal. Because in the final analysis, the bandwidths of precision circuits can only be determined in terms of the equivalent noise-widening as observed in a narrow-band filter, knowledge of the most efficient methods of minimizing the ratio $\Delta\omega/\omega_o$ is of extreme importance. It is necessary for the stability of a calibrating source to be at least 10 times that of the device under test for a measurement of the effective noise bandwidth to give an indication of the absolute noise stability of the poorer signal. Otherwise, it is necessary that a series of oscillators be compared with each other, and each compared one-

by-one with all the others to get a practical measure of the value of $\Delta\omega_\sigma$.

The statement is frequently made that the stability of the output frequency of an oscillator is independent of the configuration in which the active device is used. Subject to certain limitations, this is correct, but it is important that the degradation of the circuit Q-factor by the active device be identical for the respective circuits, and also that the variation of the amplification with signal have the same characteristics and magnitude. Unless these conditions are fulfilled, however, the frequency stabilities will not be comparable.

The effect of variation of the Q-factor for a crystal on the possible frequency deviation for a crystal oscillator having a AK factor of 0.5 is indicated in the following table, the assumed frequency being 10^8 Hz.

Q	10^4	2×10^4	5×10^4	10^5	2×10^5	5×10^5
$\Delta\omega_o$	1.5 rad	0.38	0.06	0.015	0.004	0.0006
Δf_o	0.25 cps	0.06	0.01	0.0025	0.0006	0.0001

Consequently, if a crystal having a Q of 10^4 is used at 100 MHz, it is necessary that the variation of amplification over the signal voltage range be limited to an rms value of 0.2 for 0.1-Hz bandwidth. Evidently, a thermal regulator may be desirable if rapid and convenient starting is to be achieved. The very minimum excess gain that will assure starting is at least 10% for a

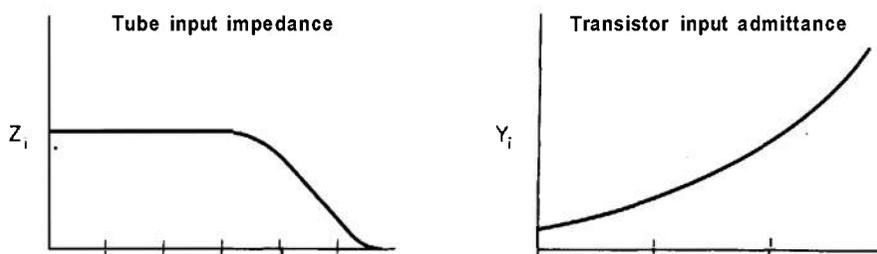


Fig. 9-4. Input Impedance

degenerative amplifier and 50 to 100% for ordinary circuits.

The Clapp and the Q-multiplier oscillators both can be designed to take advantage of the high order of constancy of gain of the emitter-follower circuit when it is arranged to have minimum loading. (This loading problem is often ignored when oscillators are designed around electron tubes as the active device.) It is of extreme importance that the loading be kept to a minimum, because the value of the Q-factor that must be used with the equation is the value *under operating conditions*.

9-2 AVERAGING OF AMPLIFICATION

The process of finding the conditions for which the average amplification is unity can be very complex if the variation of amplification with signal is irregular, and it can be quite simple if the variation is linear with signal. Normally it is convenient to calculate the amplifications at three points on the cycle of oscillation, namely, the positive limit of input signal, the negative limit, and the static value. From these three values the approximate linearity of variation may be determined in terms of the equation

$$AK = 0.25(K_p + K_n - 2K_s) \quad (9-24)$$

where AK , the deviation from linearity, ideally should be very small compared with the positive, negative, and the static values of the amplification; K_p , K_n , and K_s . If it is as large as from 10 to 25% of one of the typical amplification values, then a more complex method of averaging may be desirable; for example, the orthogonal polynomial method described in Appendix C. If it is less than 10%, a suitable averaging equation for the amplification is

$$K_a = 0.25(K_p + 2K_s + K_n) \quad (9-25)$$

Modified forms of this equation may also be used for averaging other circuit values when the behavior is relatively linear.

In addition to the use of orthogonal polynomials, the Fourier method may be used for averaging when the amplification is either relatively or significantly nonlinear. Both of these methods can be used to handle the determination of the average amplification in oscillators in which the nonlinearity is considerable. Exam-

ples of the use of each of these methods are included at the end of this paragraph, and a more complete explanation of the use of orthogonal and Legendre polynomials is included in Appendix C.

The polynomial method may be applied to either continuous data, in which case the input-output or the input-amplification relation is known in terms of a closed function, or it may be applied to discrete data for either of the functional relations. For the convenience of the reader, a table of Legendre coefficients for use with power-series expansions is included in the appendix, along with a discussion of the application procedures in simple problems. One of these tables assumes that the power-series term is uniquely defined and not continuously zero over any part of the range $-1 < x < +1$, and the second table gives the values for the conditions that the term is zero for all negative values of x , but is nonzero for values over the range $0 < x < +1$. It may be used for representation of diodes and class B circuits.

With the polynomial method, a series of polynomials that are mutually orthogonal when integrated (or summed) over the range from minus unity to plus unity are either fitted analytically (continuously) over the range of the variables to give the best least-squares fit between the approximating curve and the original function, or they are fitted to give a least-squares fit at a series of uniformly spaced data points over the range. The continuous-fitting method uses Legendre polynomials, and with discrete data, a discrete series known as orthogonal polynomials are used. The orthogonal polynomials have a close relationship to the Legendre polynomials in that they approach the latter when the increment approaches zero. The polynomial coefficients are first determined, corrected if necessary, and then each of the polynomials is replaced by its equivalent in the form of trigonometric (Chebycheff) polynomials, the angular functions being expressed in terms of multiple angles rather than in powers of the simple angle. After this substitution is made, then the coefficients for the corresponding multiple angles may be collected, and the result is a series of terms in the various harmonics of the applied frequency. These harmonics and their coefficients express the response of the network to a sinusoidal input signal.

The Fourier technique for calculation of the amplification is based on the analysis of the amplitudes of the harmonics generated in a circuit through the introduction of a sinusoidal input signal of given magnitude. The ratio of the fundamental output amplitude to the input magnitude gives the average amplification, and the ratios of the amplitudes of the higher harmonics to the output amplitude of the fundamental gives the dis-

tortion components for the overall circuit. This technique is applicable to oscillators because the input signal can be assumed to be a sine wave, and the distortion resulting from oscillator limiting can be assumed to be generated in a separate nonlinear circuit. The spectrum can be determined in terms of a sine-wave input, and the component amplitudes determined by the Fourier analysis. The process is easily applied when the detector characteristic is known in closed form, but it becomes more difficult with discrete data such as are normally encountered with active circuits.

Since the use of Fourier analysis for both discrete and for continuous data is well known and is described in most elementary electrical engineering textbooks, it will not be described in detail here. Fourier analysis, like the use of Legendre and orthogonal polynomials, gives the required answers easily and directly because of the orthogonality of harmonic trigonometric components. As with Legendre analysis, the ratio of the amplitudes of the output and input sinusoidal components gives the average amplification.

EXAMPLE 9-1. Determine the average amplification of an amplifier having a response defined by the equation

$$y = ax^2 \text{ over the range } 0 \leq x \leq 1$$

Both the gain function and the voltage function may be determined using the Legendre technique. For this problem, assume that the peak amplification in the conduction direction is **20**. With a square-law response starting at the static, or Q-point, this means that the peak output signal is 10 V.

The amplitude of the sinusoidal component may be found directly by reference to Table C-2 in Appendix C. The value of the coefficient for the voltage-output function may be determined by the use of the column for exponent $j = 2$, and for the gain function, for $j = 1$. The corresponding values for the other coefficients are

$$E_{e1} = 0.375, \quad C_{e3} = 7/48, \quad C_{ko} = 0.25, \\ C_{k2} = 5/16$$

Substituting in Eqs. C-7 and C-8 of Appendix C gives

$$K_o = 0.2109, \quad E_1 = \mathbf{0.429}$$

Multiplying the first by **20**, and the second by 10, gives the effective voltage output, **4.22** for the first case, and **4.29** for the second.

This result may also be obtained by the use of Fourier techniques, because if the input is $\cos \omega t$, the output is $10 \cos^2 \omega t$ over half the cycle, and zero over the other half. Using the Fourier integration equation for the fundamental component gives

$$E_1 = (10/\pi) \int_{-\pi/(2\omega)}^{\pi/(2\omega)} 0.5(1 + \cos 2\omega t) \sin \omega t dt \quad (9-26)$$

the integration being from $-\pi/(2\omega)$ to $+\pi/(2\omega)$. Integrating Eq. 9-26 gives the required answer

$$E_1 = \mathbf{4.244}$$

Three terms are obtained in the integration, two at fundamental frequency, and one at the third harmonic. All three contribute because of the half-period integration time.

This result can also be obtained in terms of orthogonal polynomial expansions just as it can in terms of Legendre and Fourier expansions. The details of the method of calculation are explained in Appendix C, and the process of making trapezoidal corrections is also explained. Assuming that a square-law relation is known in terms of either of the two following combinations of data, with $e_i = 0$ the static, or Q-point, the average amplification and output voltage are

e_i	0	0.1	0.2	0.3	0.4	0.5	0.6
e_o	0	0.1	0.4	0.9	1.6	2.5	3.6
K	0	2	4	6	8	10	12
e_i	0.7	0.8	0.9	1.0			
e_o	4.9	6.4	8.1	10.0			
K	14	16	18	20			

The data for e_o may be multiplied by the data in the $j = 1$ and $j = 3$ rows of the table for $2n + 1 = 21$, and each of them may be divided by the sum term S_j to give the required components, approximately 3.9 and **0.42**. In a similar manner, the values of the amplifications may be obtained by the use of the K data with rows 0 and 2. Normally, the value based on the amplification will tend to converge more slowly than will the value based on voltages because of the integration implied in the voltage determination.

The accuracy with which results can be obtained by these methods depends on the number of data points that are used for representing the behavior of the circuit. For example, if $n = 4$, the smoothing is poorer and a poorer set of data is likely to result. The accuracy of the results is significantly poorer with "one-sided" data than with complete data because of the difficulty of producing an identically zero value over an extended range.

The selection between the use of the approximate equations for the determination of the second and third harmonics and the use of polynomial methods is based on the number of data points available and the uniformity of the variation they possess. The presence of a sharp break in the contour, with data available for more than six points, makes the use of orthogonal techniques desirable. As long as no sharp break is noted in the data, calculation of the values at three points usually is sufficient. If the presence of a sharp break is suspected, however, as many data points as possible should be used.

9-3 STATIC CIRCUIT BEHAVIOR

The development of the static operating conditions for an oscillator is as complex as is the determination of the conditions for unity loop amplification. In fact, it is not possible to separate the two determinations because the manner of variation of amplification depends on the way in which the static biasing operation takes place.

The simplest method of regulating static behavior, rectification limiting, is difficult to achieve and use with transistor oscillators because of the relatively high conductance of the input circuit under amplifying conditions, and because of the relatively uniform variation of the input conductance. Consequently, the nonlinearity of the variation of the control current, as well as the nonlinearity of the variation of amplification, must be used in the stabilization of simple transistor oscillators.

The requirement that the input power for the feedback path be provided at an impedance level that is small compared to the input impedance of the device means that the input voltage will be approximately sinusoidal, whereas the input current will not be. It is, therefore, important to determine how the current variation affects the determination of the appropriate method of introducing control. An examination of the behavior of a typical transistor under equal increments of base voltage shows that the average base current, for a fixed operating point, will increase as the sinusoidal signal is increased in amplitude. This means that one

possible method of amplitude control for the transistor oscillator is through limiting its average base current, as the average forward conductance will then decrease as the magnitude of the signal current increases. A typical calculation of such a current averaging procedure is shown in Example C-1 in Appendix C.

Some limiting of average amplification may be obtained with a fixed operating point for an oscillator, because the effect of base-spreading resistance is greatest at high current. However, the range of variation usually is insufficient to assure reliable starting, with the result that some method of shifting the operating conditions to an area of reduced average amplification is desirable.

If the average base current is limited to a fixed value through the use of a series resistor, the increase of amplitude of the signal voltage is accompanied by the shift of the effective position of the output load contour as is shown in Fig. 9-5. The amplitude of the signal voltage corresponding to each load line is just that which will give the required average base current (or emitter current for a common-base circuit). If the amplitude of the oscillation still builds up, it is accompanied by a further shift of the position of the load line.

Through the points on this set of load lines a pair of limit contours may be drawn that represent the excursion for which the average base current exactly equals that for which the circuit has been designed. These contours are often convenient to use, so they may be sketched in, and the positive limit identified by the symbol C_{Lp} , and the negative by the symbol C_{Ln} . The positions of these contours can be determined by calculation of the average current at sets of data on base current on several load lines, and then the amplification calculations may be made as required along these contours and the static contour.

The only difference in determining the limit contours for the common-base oscillator as compared to the common-emitter is that the calculations are based on the sum of the collector and base currents rather than the base current alone. The correction for the load-contour curvature, which has already been discussed, may be required, but this correction may be made after the final steady-state load line is located.

9-4 CURRENT AVERAGING

The averaging of the base or the emitter current in the oscillator to find the limit points on any given load line is performed by either of two methods, the three-term averaging formula for applications in which the

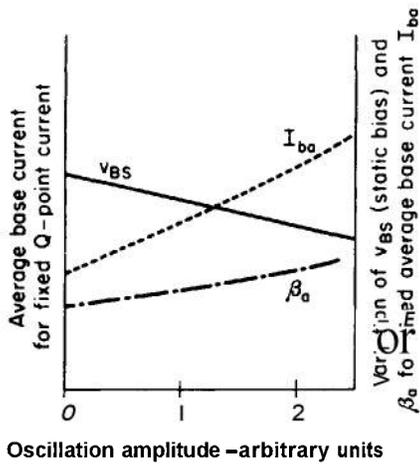


Fig. 9-5. Effect of Variation of Oscillator Amplitude

variation is relatively linear, or the orthogonal-polynomial method.

The averaging formula convenient for use with current variations which might be called square-law, is related to the formula used for the averaging of the loop amplification. It is

$$I_s = 0.25[I_p + 2I_s + I_n] \tag{9-27}$$

where I_a is the average electrode current, I_p the electrode current for the most positive value of signal voltage on the electrode, I_s the current at the intersection of the static and dynamic load contours (the Q-point current), and I_n the current at the most negative value of signal voltage. As long as only the first two derivatives of the electrode current are significant over the operating range of the transistor this equation gives adequate accuracy.

In oscillators in which higher orders of nonlinearity are present, the base or emitter current averaging cannot be accomplished by the simple formula, and it is necessary to turn to a more sophisticated method, such as orthogonal polynomials. The sample problem, Example 9-2, solved next shows the directness of the polynomial method and shows how it compares with the averaging equation.

EXAMPLE 9-2. An oscillator has been constructed with a circuit that limits the average base current to $90 \mu\text{A}$. If the following table gives the values of the base current for equal increments of base voltage and the current at the Q-point is $80 \mu\text{A}$, find the range of signal voltage and base current.

9-10

The averaging equation, Eq. 9-27, gives the result very quickly based on the table

V_b	100	110	120	130	140	150	160	170	180
I_b	10	20	35	55	80	110	145	185	230

The average currents for peak base-voltage amplitudes of $A V_0 = 20, 30,$ and 40 mV are $85.0, 91.25,$ and $100 \mu\text{A}$, respectively. Evidently, in the limiting condition a base-voltage change of approximately 56 mV is developed.

Using the polynomial method, the tables for $2n + 1 = 5, 7,$ and 9 may be used, and the first two components, namely C_0 and C_2 , may be used in the evaluation of the average current. Trapezoidal corrections may also be included if desired, because the exponent-two condition correction applies. (It is necessary for only the lowest coefficients to be nonzero for the correction process to be effective.) The typical calculation for $2n + 1 = 5$ to give the values of C_0 and C_2 follows.

The matrix equations for C_0 and C_2 , leaving blank rows for the odd coefficients, are

$$\begin{bmatrix} C_0 \\ \dots \\ C_2 \\ \dots \\ C_4 \end{bmatrix} = \begin{bmatrix} \frac{1}{5} \\ \dots \\ \frac{1}{7} \\ \dots \\ \frac{1}{70} \end{bmatrix} \begin{bmatrix} 1 & 1 & 1 & 1 & 1 \\ \dots & \dots & \dots & \dots & \dots \\ 2 & -1 & -2 & -1 & 2 \\ \dots & \dots & \dots & \dots & \dots \\ 1 & -4 & 6 & -4 & 1 \end{bmatrix} \begin{bmatrix} 35 \\ 55 \\ 80 \\ 110 \\ 145 \end{bmatrix}$$

From this equation, the values of $C_0, C_2,$ and C_4 are:

$$\begin{aligned} C_0 &= \left(\frac{1}{5}\right) [1 \times 35 + 1 \times 55 + 1 \times 80 + 1 \times 110 \\ &\quad + 1 \times 145] \\ &= \frac{425}{5} = 85 \mu\text{A} \end{aligned}$$

$$C_{0e} = [80 + 2 \times 85] / (3) = 83.3$$

$$\begin{aligned} C_2 &= \left(\frac{1}{7}\right) [2 \times 35 - 1 \times 55 - 2 \times 80 - 1 \\ &\quad \times 110 + 2 \times 145] \\ &= \frac{35}{7} = 5 \end{aligned}$$

$$C_{2e} = \frac{4 \times 5}{3} = 6.67$$

$$\begin{aligned} C_4 &= \left(\frac{1}{70}\right) [1 \times 35 - 4 \times 55 + 6 \times 80 - 4 \\ &\quad \times 110 + 1 \times 145] \\ &= 0 \end{aligned}$$

Substituting to find I_o gives

$$\begin{aligned} I_o &= 86.25 \mu\text{A, uncorrected} \\ &= 83.3 \pm 1.67 = 85 \mu\text{A, corrected} \end{aligned} \tag{9-38}$$

The uncorrected average current is **86.25 μA** . Similar calculations may be made using $n = 3$ and $n = 4$, giving corresponding average values of current. The correct operating conditions are with a signal magnitude of approximately 28 mV either side of the quiescent point, 140 mV.

Application Notes. The previous discussion is directed to the evaluation of the mathematical tools required for effective design of oscillators, whether they are based on the use of tubes, transistors, or other active devices as the amplifier elements. It is necessary to be able to locate the operating cycle in two respects, first with respect to the limits of current or voltage for the circuit, and second with respect to the overall, or loop, amplification of the oscillator if effective nonlinear design is to be achieved. The balance of this chapter is devoted to the development of the techniques of application of piece-wise linearization to oscillators using transistors, and the following two chapters are devoted to a detailed discussion of specific circuit applications, the first application chapter considering L - C oscillators and crystal oscillators, and the second considering R- C -type tuned oscillators.

9-5 BASIC DESIGN PROCEDURES

A general design procedure can be established based on the previous discussion. The first step, as always, is the location of the static and the dynamic load lines on the characteristic curves. A static value of collector voltage is first selected at a value less than one-third of the maximum rated collector voltage, and a static value of the operating current for the control electrode, either base or emitter, is selected. Then a series of trial load lines may be plotted, and transferred to the input family in the usual way (Fig. 9-6). The impedances for these load lines are given by the Z_i for the feedback network. Since the value of Z_i may vary as a result of conductance loading, the representing contour need not be a straight line. In case correction for curvature is required, an initial value of impedance at the static- or Q-point may be calculated based on the small-signal data at the rest-point. The appropriate slope may be determined, and the load contour plotted from the static-point in both directions to the adjacent bias contours. New values of slope may be calculated at each of the adjacent bias lines, and the load line curved just enough to give the correct slope at the bias contours. This process is continued until the full operating contour has been plotted. The corresponding input contour is plotted step-by-step as the output contour is constructed.

After a set of input and output load contours have been plotted, the next step is to mark points of equal base-voltage increment on the input family and transfer the points to the output family. Once these points have been located, the values for the current and voltage variables and the final values of the small-signal parameters may be tabulated from the curves. Then both the input admittance and forward amplification values and the average values for the control current may be calculated for use in the design procedure. The balance of the problem is concerned with the linear components such as inductors, capacitors, crystals, and similar energy-storage elements.

The derived-gain form of the orthogonal equations may be used to determine both the approximate input admittance and the forward transfer admittance for the transistor if adequate small-signal data are not available. This technique of determining the small-signal characteristics of a circuit from the static data is not as good as is using small-signal data in the form provided on some transistors in Appendices E and F, but because of the least-squares averaging obtained with the polynomial technique, it is appreciably better than evaluation at individual points. The mean value and the maximum change of the admittances are given in terms of the K factors of Eq. C-8, Appendix C, Part A, through the equation

$$\begin{aligned} Y_0 &= K_0 I / V, & Y_1 &= K_1 I / V \\ Y_{\min} &= Y_0 - Y_1, & Y_{\max} &= Y_0 + Y_1 \end{aligned} \quad (9-28)$$

where I is the current scaling factor, that factor by which each of the current entries must be multiplied to give the current in amperes, and V is the voltage scaling factor, equal to half of the total change. Example 9-3 shows how this can be done based on the data for Example 9-2.

EXAMPLE 9-3. Using the derived gain equations and the trapezoidal correction factors from Appendix C, calculate the average input admittance and the maximum and minimum admittances for the current-averaging problem, Example 9-2.

The values of C_{e1} and C_{e2} must now be calculated as they appear in the equation for K_0 . The equation for K_1 gives either the uncorrected or the corrected values of the second-harmonic component of amplification, depending on whether the coefficients are corrected or not. The values of Y_0 and Y_1 obtained for $V = 20$ mV are $Y_0 = 2750$ pmhos, and $Y_1 = 750$ or 1000 pmhos, depending on whether the data are uncorrected

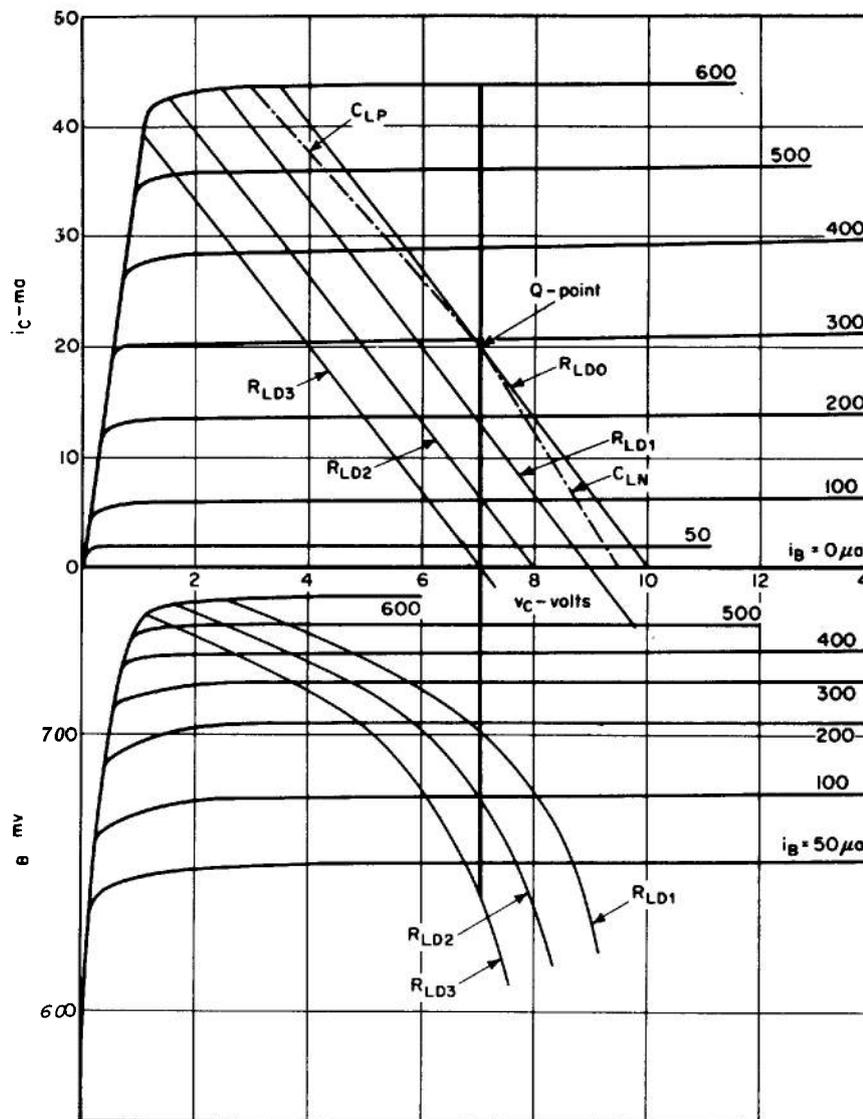


Fig. 9-6. Contour Development of 2N1613

or corrected, respectively. Similar values may be obtained for other typical operating conditions.

The value of K_0 or Y_0 is important in that it measures the linear behavior of the device, whether it is an input or a transfer coefficient. Similarly, the value of Y_1 or K_1 measures the distortion or nonlinearity in the circuit. The value of Y_0 or K_0 may be independent of the operating amplitude, in which case limiting in the am-

plification must be generated by variation of the static operating point. The value of Y_1 or K_1 must of necessity increase as the amplitude is increased, because the variations from linearity normally increase with increasing signal amplitude. The smaller the ratio of K_1/K_0 or Y_1/Y_0 , the smaller the distortion and the higher the frequency stability of the oscillator.

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CHAPTER 10

PRACTICAL L - C OSCILLATORS

10-0 INTRODUCTION

The development of practical designs of L - C oscillators based on the techniques described in Chapter 9 requires the coordination of network properties with the properties of active devices. It also requires the selection of transistors capable of functioning as required. With some minor limitations, any transistor that can be used below its upper noise corner frequency f_{nc} may be used effectively in an oscillator circuit. However, because some of the parameters of transistors introduce significant effects into the behavior of an oscillator circuit, a discussion of the factors that can deteriorate the performance of the circuit is important.

One of the parameter groups important in the design of oscillators is the group including the series element resistances r_e , r_b , and r_c . Each of these should be as small as possible because each has its own degrading effect on transistor behavior. The effect of the presence of r_e is to reduce the effective values of forward admittance available, limiting the effectiveness of a transistor as an active element. Similarly, the presence of r_b either makes signal injection into the base junction difficult or it introduces a regenerative effect into the overall circuit. The presence of r_c in the circuit tends to introduce instability inasmuch as it makes necessary the introduction of a phase-shift and more than the design amount of gain into the amplifier. A signal voltage proportional to the internal impedance r_e must be developed in addition to that required by the amplifier load circuit when this series impedance is present.

One type of transistor normally has comparatively large values for all three of these internal impedances, and at least one impedance, r_b , has both resistive and reactive components. This type of transistor, the grown-junction transistor, is for that reason relatively less satisfactory for oscillator use than many of the other common forms. Transistors having a base, whose conductivity increases toward the emitter junction can be made with the smallest values of r_b , and they also can be made with rather small values of r_e . The value of r_c present in a given transistor, particularly one of the alloy variety, depends primarily on the processing

details rather than on the physical design of the collector region. The epitaxial design of the mesa transistor is particularly effective because of its small value of r_c (Ref. 1).

Alloy and surface barrier transistors, meltback, graded-base, and mesa transistors all are likely to have the properties required for use in an oscillator. Other types may also have the required properties, but their characteristics should be given close scrutiny prior to selection for use in a circuit.

10-1 THE BASIC L - C OSCILLATOR

The basic equations for direct-coupled L - C oscillators may all be derived in terms of a single basic configuration, because the active device enters into the action primarily in the process of cancelling out the positive resistance of the frequency-selection circuit. This relation is a result of the fact that no matter how the configuration is arranged, the amplifier is required to provide a unity loop-amplification, and it is adjusted to do so. The method of adjusting the amplification to unity does not appear directly in this derivation, nor does the amount of energy required of the frequency-selection circuit by the active device appear in the equation.

The fact that all of the basic oscillator forms, common-emitter, common-base, and common-collector, can be studied on the basis of a single circuit has led to some confusion on the relative frequency stability of the three forms. As was shown in Chapter 9, the frequency stability of an oscillator depends primarily on the magnitude of loading reflected by the active device on the tuned circuit, and the magnitude variation of the amplification with signal level. This being the case, the best stability can be expected for the arrangement giving the smallest loading and the smallest variation of amplification. Evidently, the common-base oscillator circuit has reduced stability because of the input signal power required by the emitter of the transistor, and by the fact that it has a reduced power gain compared to the common-emitter configuration.

The selection of a configuration between the common-emitter and the common-collector form is somewhat more difficult. The power gain in the common-collector amplifier is much smaller than for the common-emitter, but the uniformity of loading and the uniformity of gain are both much better. Consequently, the selection between the two can be rather difficult. If the common-emitter circuit is properly designed, it can be used in excellent high-stability oscillators, but otherwise, the common-collector circuit often gives the most stable arrangement. That this is true can be recognized from the large amount of use made of Clapp and Q-multiplier type cathode-follower oscillators. The stability improvement in both examples is a result of the reduced and more uniform loading of the active device on the tuned circuit and on the more uniform amplification.

The basic oscillator configuration, which is important with energy-storage oscillators (oscillators in which frequency control is a result of exchange of energy between devices capable of possessing kinetic and potential energy), is shown in Fig. 10-1. This circuit utilizes an active amplifier and three reactive elements, two of which possess the same kind of energy-storage and the third which stores the alternate form of energy. If two of the elements are capacitors, the third is an inductor, and the oscillator is a Colpitts oscillator; if two are inductors, one is a capacitor, a Hartley oscillator. Normally the two inductors are both parts of a single tapped inductor, and a relatively high coefficient of magnetic coupling exists between the sections. The coupling simplifies the transformation of impedance required in oscillator circuits.

The basic equations for the general oscillator shown in Fig. 10-1 are rather similar to those derived in Chapter 9, in that they relate the amplification of the active device to the frequency-selection and transforming action of the storage circuit. They differ only in that the adjustment of the voltage amplification is obtained through the action of the two like-reactive elements directly, instead of including a separate factor for the adjustment. The common or ground point is taken at one end, or at the junction of unlike elements, if either the common-base or the common-collector circuit is used, and it is taken at the junction of like elements if a common-emitter circuit is used.

The input, output, and transfer characteristics of the circuit of Fig. 10-1 may be readily analyzed either by standard methods or topologically, giving the basic input, output, and transfer impedances as

$$Z_I = [(1 + Y_3/Y_1)/(Y_2 + Y_3)] / [1 + \langle Y_2 Y_3 / (Y_2 + Y_3) \rangle Y_1] \quad (10-1)$$

$$Z_O = [(1 + Y_2/Y_1)/(Y_2 + Y_3)] / [1 + \langle Y_2 Y_3 / (Y_2 + Y_3) \rangle Y_1] \quad (10-2)$$

$$Z_T = [1/(Y_2 + Y_3)] / [1 + \langle Y_2 Y_3 / (Y_2 + Y_3) \rangle Y_1] \quad (10-3)$$

If the substitutions required for a Colpitts oscillator are made, namely,

$$1/Y_1 = R_1 + j\omega L_1, \quad Y_2 = j\omega C_2, \quad Y_3 = j\omega C_3 \quad (10-4)$$

then these equations take the form

$$Z_I = \langle R_1 - 1/(j\omega C_2) \rangle / (j\omega R_1 C_2) = L_1 C_3 / \langle R_1 C_2 (C_2 + C_3) \rangle \quad (10-5)$$

$$Z_O = \langle R_1 - 1/(j\omega C_3) \rangle / (j\omega C_3 R_1) = L_1 C_2 / \langle R_1 C_3 (C_2 + C_3) \rangle \quad (10-6)$$

$$Z_T = -1/(\omega^2 R_1 C_2 C_3) = -L_1 / \langle R_1 (C_2 + C_3) \rangle \quad (10-7)$$

when the frequency is

$$\omega^2 L_1 C_2 C_3 = (C_2 + C_3)$$

These relations are subject to the restrictions $R_1 \ll 1/(\omega C_2)$ and $R_1 \ll 1/(\omega C_3)$.

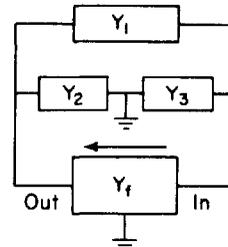


Fig. 10-1. General Oscillator

Taking the ratio of Z_I/Z_O shows that the impedance ratio, input to output, is

$$Z_I/Z_O = C_3^2/C_2^2 \quad (10-8)$$

This square relation only holds when the restrictions given on R_1 are valid; otherwise the loading current may be large compared to the charging current, which measures the circulating energy in the network.

In actual practice, the tuned network is loaded not only by its internal impedance but also by an output conductance that represents the loss component of the feedback circuit. This loss is primarily present on the output, but a small amount also is present on the input side of the network in typical applications. The circuit of Fig. 10-1 may be re-analyzed to include this shunt loading, and essentially the same results as those just derived will be obtained. Each of the shunt conductances may be converted into an equivalent series resistance by the typical conversion equation

$$R_s = gL/C \quad (10-9)$$

where g is the conductance, L is the associated inductance, and C is the capacitance in parallel with g . If the sum of R_s and the resistance R of L is small compared to the reactance of the individual capacitances in the circuit, or

$$1/\omega C_2 \gg R_1 + gL_1/C_3$$

then the transformation Eq. 10-9 may be made, and the input impedance equation may be written

$$Z_I = L_1 C_3 / [R_1 C_2 (C_2 + C_3 + C_2 R_1 g) + g L_1 (1 + g R_1) C_2^2 / C_3] \quad (10-10)$$

where g_{now} is the load conductance in parallel with C_3 . Normally, the term gR_1 under these conditions has a value small compared to unity, and can consequently be neglected. The equation for the input impedance may now be reduced to

$$Z_I = L_1 C_3 / [R_1 C_2 (C_2 + C_3) + g L_1 C_2^2 / C_3] \quad (10-11)$$

Dividing numerator and denominator by C_2^2/C_3 gives the modified result

$$Z_I = L_1 (C_3/C_2)^2 / [R_1 C_3 (C_2 + C_3)/C_2 + g L_1] \quad (10-11a)$$

The last terms in the denominators of Eqs. 10-11 and 10-11a convert the shunt conductance into the equivalent series resistance and scale them in accordance with the transformation ratio for the circuit. When $g = 0$, this equation reduces to Eq. 10-5.

The transfer term for this circuit may be evaluated similarly

$$Z_T = -L_1 C_3 / [R_1 C_3 (C_2 + C_3) + g L_1 C_2] \quad (10-12)$$

Clearly, the larger the internal resistance in the coil or the larger the shunt conductance on the output, the lower the transfer impedance. For optimum operation of a transistor oscillator, the second term in the denominator should be comparatively small, because only if the loading from the transistor is kept small are the required voltage-drive conditions available. This term may be kept small if the value of C_2 is kept small, and the value of C_3 and L_1 adjusted to re-establish resonance. Larger values of both are required. The ratio of C_3 to C_2 should be kept as large as possible within the other circuit limitations.

The limiting conditions for the tuned circuit of the general oscillator may consequently be summarized in terms of the following inequalities

$$\begin{aligned} \text{Re}(y_o) \times \text{Re}(Z_I) &< 1 \\ \text{Re}(y_i) \times \text{Re}(Z_O) &< 1 \end{aligned} \quad (10-13)$$

where the y_i and the y_o are the input and the output admittances of the transistor in the configuration used, and the Z_I and the Z_O are the tuned impedances of the frequency-selection circuit.

The shunt capacitances of the active device do not enter into consideration in this portion of the design problem because for practical purposes they may be lumped with the capacitances of the circuit itself. If the base-spreading resistance for the transistor were zero, the capacitances would enter only into the selection of the total values of capacitance, but since it is not zero, the decoupling effect in the input must be considered.

The Hartley oscillator differs from the Colpitts only in that the capacitors in the Colpitts are replaced by two magnetic-coupled inductors in the Hartley configuration, and the inductor is replaced by a capacitor. This arrangement does not require capacitors of as large a value as are required with the Colpitts, with the result that it is used for relatively low-frequency applications, whereas the Colpitts is more suitable for high-frequency applications.

The behavior of the Hartley circuit differs in one other significant way from that of the Colpitts, in that if the magnetic coupling between the two sections of the inductor is relatively high (it usually is), then transformer action can be utilized to obtain the required current gain to the output of the circuit. Consequently, smaller values of Q-factor can be used for the tuned circuit without loss of circuit efficiency. The input and the transfer impedance equations take the form

$$Z_I = [Y_1 Y_2 Y_3 + Y_2 Y_3 Y_4 - Y_1 Y_{23} Y_{32} - Y_4 Y_{23} Y_{32} - Y_{32} Y_{23} Y_{32}] / [Y_1 Y_2 Y_3 Y_4 - Y_1 Y_4 Y_{23} Y_{32} + Y_1 Y_2 Y_{32} Y_{23} + Y_1 Y_2 Y_{32} Y_{32} - Y_2 Y_4 Y_{23} Y_{32} - Y_2 Y_{32} Y_{23} Y_{32} - Y_1 Y_{23} Y_{32} - Y_1 Y_{32} Y_{23} Y_{32}] \quad (10-14)$$

$$Z_T = [Y_1 Y_2 Y_3 - Y_1 Y_{23} Y_{32} - Y_2 Y_{32} Y_{32}] / [Y_1 Y_2 Y_3 Y_4 - Y_1 Y_4 Y_{23} Y_{32} + Y_1 Y_2 Y_{32} Y_{23} + Y_1 Y_2 Y_{32} Y_{32} - Y_2 Y_4 Y_{23} Y_{32} - Y_2 Y_{32} Y_{23} Y_{32} - Y_1 Y_{23} Y_{32} - Y_1 Y_{32} Y_{23} Y_{32}] \quad (10-15)$$

If these equations are multiplied, numerator and denominator, by the product $Z_2 Z_3 z_{23} z_{32}$, and the substitutions of the various admittances and impedances made in accordance with the following equivalents

$$Y_1 = j\omega C_1, \quad Z_2 = R_2 + j\omega L_2, \quad Z_3 = R_3 + j\omega L_3, \\ Y_4 = g_4, \quad z_{23} = j\omega M, \quad z_{32} = j\omega M \quad (10-16)$$

and the additional substitutions made

$$\omega^2 = 1 / \langle C_1 (L_2 + L_3 + 2M + g_4 R_2 L_3 + g_4 L_2 R_3) \rangle \quad (10-17)$$

Eqs. 10-14 and 10-15 simplify to the form

$$Z_I \doteq [L_2 + C_1 R_2 R_3 - (L_2 L_3 - M^2) / (L_2 + L_3 + 2M)] / [C_1 (R_2 + R_3 - g_4 (L_2 L_3 - M^2) / C_1 (L_2 + L_3 + 2M))] \quad (10-18)$$

$$\doteq [L_2 - (L_2 L_3 - M^2) / (L_2 + L_3 + 2M)] / [C_1 (R_2 + R_3) - g_4 (L_2 L_3 - M^2) / (L_2 + L_3 + 2M)] \quad (10-18a)$$

$$\doteq (L_2 + M)^2 / \langle C_1 (R_2 + R_3) (L_2 + L_3 + 2M) \rangle \quad (10-18b)$$

when the coupling Coefficient is large. The transfer impedance is

$$Z_T \doteq -(L_2 + M)(L_3 + M) / C_1 (R_2 + R_3) (L_2 + L_3 + 2M) \quad (10-19)$$

These equations assume that the input conductance of the active device, g_4 , is small to comparable to the loss in the resistance components of the tuned circuit. This condition is required for effective amplitude control in the oscillator and also for a minimum magnitude of distortion and a maximum overall frequency stability.

In the transfer impedance equation, Eq. 10-19, the parallel combination of $(L_2 + M)$ and $(L_3 + M)$ determines the value of the numerator, and the total series dissipation resistance and the capacitance C_1 , the denominator. For the Colpitts circuit, the capacitances are series-summed. The shunt conductance is relatively unimportant with the Hartley oscillator as long as the coupling coefficient is high, or $L_2 L_3 - M^2$ is small compared to $(L_2 + L_3 - 2M)^2$. If the coupling is small, then the circulating current must be large compared to the load current in g_4 , as is the case with the Colpitts oscillator.

The product of the transfer impedance of the coupling network by the transfer admittance of the transistor gives the loop amplification of the oscillator circuit as a whole. This product is used with the small-signal data from the transistor curves to determine the limiting conditions. The transfer impedance is the product of the circuit Q by the combined parallel admittance of the elements Y_2 and Y_3 and as such can be evaluated in terms of the frequency, the Q, and the equivalent L or C . Because many low-power transistors have forward conductances in the range from 10,000 to 200,000

pmhos, the desired value of the transfer impedance for the coupling circuit lies between 5 and 200 ohms. Because the Q (loaded) for the circuit should be made as large as possible, in excess of 100 as a minimum, the effective RF resistance of the circuit must be much less than an ohm, often less than hundredths of an ohm. The nominal value of R_s is given by the equation

$$R_s = Z_I/Q^2$$

Consequently the design of the feedback circuits for use with transistor oscillators is a particularly critical process.

10-2 TUNED CIRCUIT DESIGN

The range of values for the trans-impedance for the coupling circuit of a transistor oscillator is at least an order of magnitude smaller than the corresponding values for tube oscillators. As a result, extremely small values of inductance and large values of capacitance are required for use in the tuned feedback circuits. In particular, the difficulty encountered in finding capacitors having the required stability of capacitance along with low internal inductance and leakage can make the practical design of the coupling circuit the most critical part of the entire design procedure.

Normally, the tuning capacitors for an oscillator are either mica or air capacitors, and they may be either fixed or variable, depending on the application. Air capacitors are not readily available with capacitances in excess of 1000 pF, and mica capacitors suitable for use in electronic equipment seldom have capacitances greater than 10,000 to 20,000 pF. As a consequence, a simple Hartley oscillator cannot be expected to function adequately at frequencies below about 15 MHz, as the capacitive reactance of a 0.01 mF capacitor such as is required with the transistor version is 1 ohm at 15 MHz. In a similar manner, a Colpitts oscillator using a transistor cannot be expected to function properly at frequencies under 50 MHz, as an adequate network for providing the ratio of C_1/C_2 cannot be assembled using available capacitors.

The low-frequency limitation on transistor oscillators may be surmounted by the use of a Hartley configuration with collector connected to a tap. In this way, a relatively smaller capacitance capacitor can provide a large value of apparent capacitance at the collector terminal. Such an arrangement is shown schematically in Fig. 10-2. Then, the impedance level for the frequency-selection circuit can be as much as ten or more times

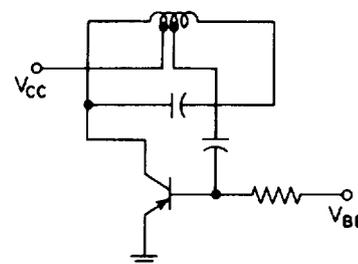


Fig. 10-2. Hartley Oscillator

the levels used for the transistor connections, and the general stability of the circuit can be greatly enhanced. The transistor is almost too good an amplifier! When the operating frequency is sufficiently high that the total series capacitance required is less than or in the neighborhood of 1000 pF, then the circuit configuration used may be the Colpitts circuit, and for lower frequencies, the standard Hartley or the tapped version of it may be used.

The self-resonant frequency, under excitation, of the inductors and capacitors of a coupling network should be at least ten times the operating frequency of the oscillator, and, where possible, it should be even larger. Otherwise, the internal parasitic parameters of the components can seriously degrade the general performance to a point that the general oscillator stability may be unsatisfactory.

Testing for the self-resonant frequencies is accomplished with the help of a grid-dip meter. With an inductor, the operating frequency of the grid-dip oscillator is varied until a frequency is found at which power is absorbed from the oscillator. This test is made with the inductor disconnected from all associated components, tubes, transistors, resistors, or capacitors, but it should be made with the inductor left in its normal operating environment. The absorption frequencies are ones at which the internal inductance resonates with the internal stray capacitances. The lowest frequency at which this phenomenon is noted is called the self-resonant frequency; above this frequency additional absorption frequencies may be found.

With a capacitor, the resonant frequency is found in a similar manner. First, however, the leads for the capacitor are shorted together in a manner that makes the amount of lead inductance a minimum. The grid-dip oscillator is coupled magnetically to the shorted leads, and its frequency is varied until an absorption condition is found. This frequency also is a self-resonant frequency. With a mica capacitor this frequency is much higher than with ordinary paper or film capaci-

tors, and typically is about 37 MHz for a 1000 pF capacitor. Since such a capacitor has 4 ohms capacitive reactance at its resonant frequency, it is evident that a considerable problem can be expected because of the low impedance levels at which the circuit must function.

The fact that the input capacitance of a transistor may be as much as 100 or more times as large as its output capacitance makes the use of unbalanced pi circuits, with C_3 much larger than C_2 , a necessity with Colpitts circuits, and it also makes essential an impedance step-down to the input with the Hartley circuit. Otherwise, it would be possible to use a balanced circuit as an impedance transformer. The high value of conductance reflected from the transistor input makes the use of a balanced network inadvisable, because it adversely affects the frequency stability.

Two examples of the design procedure for oscillators are now considered to show the detail procedure and the problems that may be encountered. For the first of these examples, the 2N247 transistor has been selected as the active device.

EXAMPLE 10-1. Design a Hartley oscillator for operation at 10 MHz, the oscillator to use the 2N247 transistor. Make a design assuming a standard Hartley configuration, and then redesign using a tapped configuration. Take the value of the effective forward admittance as 25,000 pmhos.

The transfer impedance associated with the transistor is 40 ohms for unity loop gain. For a circuit Q-factor of approximately 100, the reactance level for the transfer impedance is 0.4 ohm. The coefficient of coupling for the windings may initially be selected as unity, and a simultaneous solution made for L_2 and L_3 in terms of the frequency equation and the equation for Z_T .

For a given total inductance, L_T , where $L_T = L_2 + L_3 + 2M$, the maximum possible value for the mutual inductance, M , under conditions of unity coupling occurs when the two inductors L_2 and L_3 have equal value. Then the mutual inductance is equal in magnitude to both L_2 and L_3 , and is one-quarter of the total inductance if a series-aiding connection is used. A table (Table 10-1) may be prepared showing the relative magnitude of the mutual inductance as a function of the ratio $a = L_3/L_2$. The value of a gives the voltage ratio across the inductors for unity coupling between the coils. These data are also plotted in Fig. 10-3. If the coupling is less than unity, the ratio is the product of the value of a and the value of the coupling factor k . The equation for Z_T may be rewritten in the form

$$Z_T = -k\sqrt{a}L_2[1 - (k - 1/k)\sqrt{a} + 2(k^2 - 1)a]/[R_2 + R_3 - g_4 \times (L_2L_3 - M^2)/\langle C_1(L_2 + L_3 + 2M)\rangle]C_1 \quad (10-20)$$

$$\cong -M[1 - (k - 1/k)\sqrt{a} + 2(k^2 - 1)a]/C_1[R_2 + R_3 - g_4(L_2L_3 - M^2)/\langle C_1(L_2 + L_3 + 2M)\rangle] \quad (10-20a)$$

$$\cong -\omega M/Q \quad (10-20b)$$

This last form applies either if the value of k is approximately unity or if the value of a is very small compared to unity so that the numerator of Eq. 10-20a has a value approximately equal to M . The value of M required may be determined using this equation, and the value of L_T corresponding to it may be determined. Finally the value of C_1 may be calculated.

If a trial value of M of one-fifth of the total inductance is selected, the total impedance level is 200 ohms. For a Q of 100, the value of capacitance, C_1 , required is 0.01 mF, and the inductance required is 0.03 μ H. Evidently the inductance size is excessively small and the capacitance size excessively large for an effective design.

Either the use of a tapped coil having a higher impedance level or the use of a smaller value of a is desirable for this oscillator. If the value of a is 0.15, and the capacitance required is 1000 pF, the corresponding inductance is 0.3 μ H. This inductor requires approximately three times the number of turns as the inductor for the straight design. The collector is tapped down on the coil so that the higher impedance level does not increase the transfer gain in the circuit, Fig. 10-4.

The approximate output impedance level of the tuned circuit is $0.06 \times 200 = 12$ ohms, because

$$(L_3 + M)/L_T = 1 - (L_2 + M)/L_T$$

and the output impedance is approximately

$$Z_O = (L_3 + M)^2/\langle L_T C_1(R_2 + R_3)\rangle \quad (10-21)$$

This impedance is certainly negligible compared to the input resistive component of the transistor. Consequently, all of the circuit conditions comply with design requirements, and the final small-signal design may be completed. The input impedance corresponding to the transfer impedance of 42 ohms may be deter-

TABLE 10-1
RELATIVE MAGNITUDE OF MUTUAL INDUCTANCE AS A FUNCTION
OF a

a	\sqrt{a}	L_2/L_T	$(L_2 + M)/L_T$	M/L_T
0.005	0.071	0.873	0.935	0.0617
0.01	0.10	0.826	0.909	0.0826
0.02	0.141	0.768	0.877	0.1086
0.05	0.224	0.668	0.817	0.1492
0.10	0.316	0.577	0.759	0.182
0.15	0.387	0.520	0.721	0.201
0.20	0.447	0.499	0.691	0.213
0.30	0.547	0.419	0.647	0.229
0.40	0.632	0.376	0.613	0.237
0.50	0.707	0.344	0.587	0.243
0.60	0.774	0.317	0.564	0.246
0.70	0.836	0.297	0.545	0.248
0.80	0.894	0.279	0.528	0.249
0.90	0.950	0.263	0.513	0.250
1.00	1.00	0.250	0.500	0.250
1.10	1.048	0.238	0.488	0.250
1.50	1.224	0.202	0.451	0.247
2.00	1.414	0.172	0.414	0.243
3.00	1.732	0.134	0.366	0.232
4.00	2.00	0.111	0.333	0.222
5.00	2.236	0.096	0.309	0.213
6.00	2.446	0.084	0.292	0.208
7.00	2.642	0.075	0.274	0.199
8.00	2.828	0.068	0.263	0.193
9.00	3.00	0.062	0.250	0.187
10.00	3.162	0.058	0.240	0.182
20.00	4.462	0.033	0.182	0.149
50.00	7.071	0.015	0.114	0.109
100	10	0.008	0.091	0.083
200	14.14	0.004	0.066	0.062

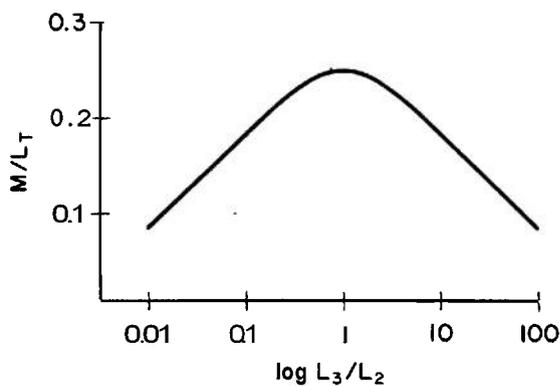


Fig. 10-3. Ratio of M/L_T to L_3/L_2
 $L_T = L_2 + L_3 + 2M$

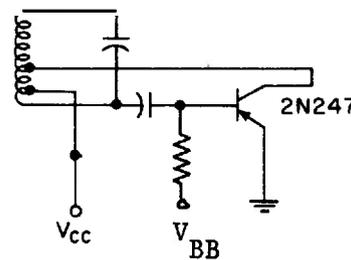


Fig. 10-4. Oscillator Circuit

mined by the use of Eq. 10-18b, and the values used for establishment of the dynamic load conditions. The resulting impedance is 144 ohms.

If a new design is made with $a = 0.01$ for a turns-ratio of 10, the total inductance is 12 times the mutual inductance, and the total is $0.72 \mu\text{H}$. This increases the

available collector impedance to approximately 436 ohms. A still higher value would be helpful. Because the value of M is the mean of the values of L_2 and L_3 (assuming a coupling coefficient k of approximately unity), L_3 is considerably less than either M or L_2 in magnitude.

A static supply voltage of 5 V may be selected because the curves in Fig. 10-5 do not permit design at a higher voltage level. The initiating point should be selected to give a forward conductance somewhat greater than 25,000 pmhos; a suitable selection is a collector current of 0.8 mA. Through this point, the reference load line should be drawn and then transcribed to the input family.

At this stage of design, it is evident that the voltage

scale is too compact to permit an efficient design calculation to be made; consequently, a replot of the curves has been made on Fig. 10-6 that spreads the range from 4.5 to 5.5 V out over the full chart. Then the design process may be continued. A series of trial load lines parallel to the reference line may be drawn, and the static operating limits on each determined. Then the set of conditions yielding unity loop amplification may be found.

Evidently, effective design of useful oscillators at reasonable impedance levels requires that the transistors be used at relatively small values of forward conductance and at relatively small collector current. For this reason, curve data for transistors for oscillator service should be based on a maximum collector current value

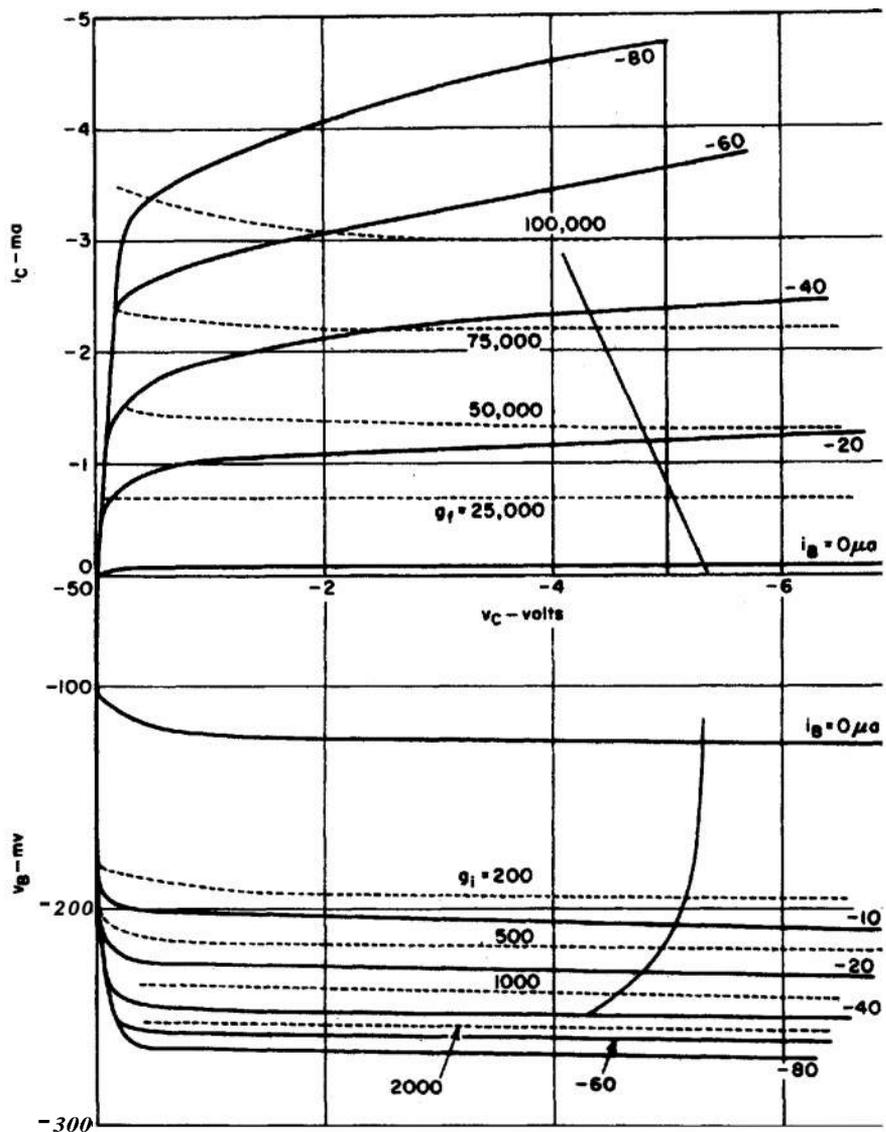


Fig. 10-5. 2N247 Oscillator

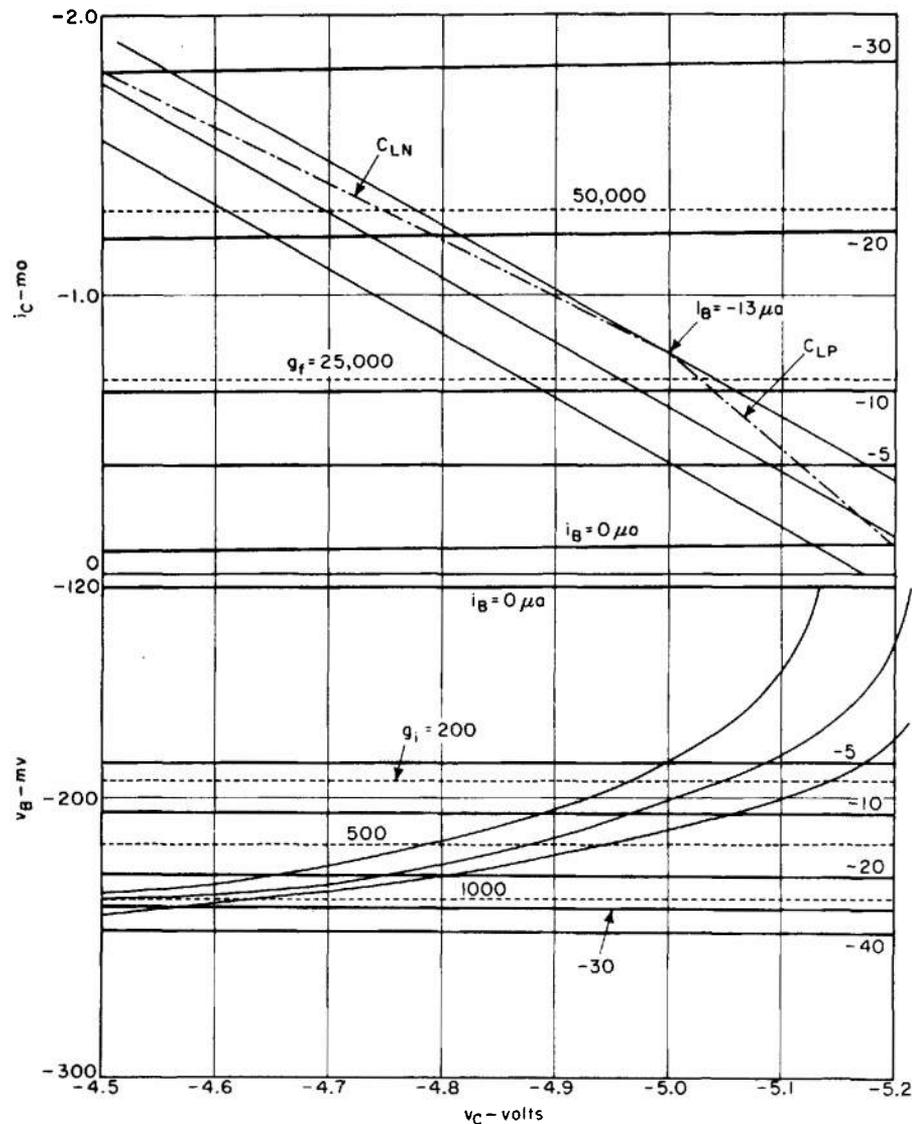


Fig. 10-6. Expanded Curves

of 1 or 2 mA. Operation under these conditions also minimizes the effect of base-spreading resistance because the input admittance of the internal junction then is conveniently small.

The averaging of the forward conductance can be achieved directly by use of orthogonal polynomials as described in Appendix C, or by the use of the formula

$$Y_{fa} = 0.25(Y_{fp} + 2Y_{fs} + Y_{fn}) \quad (10-22)$$

As described in the previous chapter, a series of points are marked on the input load contour, these points

being spaced at equal voltage increments from the static value. These points are transferred to the output load line and either of the averaging techniques is applied to the data obtained from them. The series of points that gives the correct average value of current represents the full range of operation of the transistor along any given load contour. The forward admittances are averaged over the full operating range, and the one providing unity loop amplification represents the correct limit cycle.

EXAMPLE 10-2. Design a Colpitts oscillator using an SBDT-10X transistor, the oscillator to operate at 100 MHz. The base-to-emitter capacitance is 60 pF.

The output capacitance of a transistor such as the SBDT-10X unit is about 2 pF. The reactance of this capacitance is 833 ohms, and including the circuit Q-factor, the resonant impedance may be up to 100 times this value, possibly more if the output admittance of the transistor has a sufficiently small real component. A static operating point may be selected at -3V and 0.8 mA. The optimum load impedance for use with this static condition is the one giving the maximum potential power output

$$Z_I = V_{cc}/I_{cs} = 3.0/0.0008 = 3750 \text{ ohms}$$

Assuming a Q of 100 for the circuit, the value of X_I is 37.5 ohms, and the required value of capacitance is 44.4 pF.

The forward conductance of the transistor may be determined by an orthogonal expansion of the gain function in terms of the output currents and input voltages. In Fig. 10-7, the output load line has been transferred to the input family and five equal increments of base voltage have been marked at spacing of 10 mV, giving a total excursion of 20 mV either side of the static-point. If the fundamental component of amplification is calculated and divided by 0.020, the forward conductance results. It has an average value of 23,700 pmhos at a static current of 0.8 mA. The tabulated data follow..

Datum Point	V _b	V _c	I _c	I _d
0	125m	4.4m	0.43m	103μ
1	135	3.64	0.62	148
2	145	3.00	0.80	192
3	155	1.91	1.10	260
4	165	0.90	1.36	322

If the table for $2n + 1 = 5$ in Appendix C is used to calculate uncorrected and corrected values for the C_j 's, the corrections being applied up to the third order only as a consequence of the small number of defining data, the results are

$$\begin{aligned} C_{0u} &= 0.862 & C_{0c} &= 0.841 \\ C_1 &= 0.468, \\ C_{2u} &= 0.037, & C_{2c} &= 0.049, \\ C_{3u} &= 0.003, & C_{3c} &= 0.008, \\ C_4 &= 0.0041 \end{aligned}$$

The average value of collector current is 0.853 mA, and the average value of forward conductance is the 23,700 pmhos previously listed.* The average value of the in-

put admittance may also be determined from the same data. The corresponding coefficients are

$$\begin{aligned} C_{0b} &= 213, & C_{1b} &= 110, \\ C_{2b} &= 34, \\ C_{3b} &= 0.5, & \text{and } C_{4b} &= -0.2. \end{aligned}$$

The corresponding input conductance is

$$G_i = 0.000112/0.020 = 5600 \text{ μmhos}$$

This corresponds to an input resistance of 180 ohms.

Consequently, if base-spreading resistance can be neglected (its value is approximately 51 ohms for the SBDT-10X), the transfer impedance for the feedback network is somewhat greater than 42.2 ohms, and its output impedance must be appreciably less than 90 ohms. The approximate step-down is given by the ratio C_2/C_3 . The ratio of the input to the transfer to the output impedances for the general circuit may be written in a combined form to cover both the Colpitts and Hartley oscillators

$$Z_I/Z_T/Z_O = L_2/M/L_3 = (C_3/C_2)/1/(C_2/C_3) \tag{10-23}$$

With Z_I having a value of approximately 3750 ohms, and Z_T of 42 ohms, the ratio of C_2/C_3 is approximately 1/80, and the ratio of Z_I/Z_O is approximately 6400. The effect of base-spreading resistance and the loss of forward conductance at high-frequency may reduce the available amplification, however, and make the use of a smaller ratio of capacitances necessary (Ref. 2). The effective reactance of the input capacitance for the transistor is less than 30 ohms at 100 MHz, and the magnitude of the forward conductance may be less than half the nominal value, its phase delay as much as 60 deg. An additional loss of half is required to correct the phase-shift. As a result, the value of transfer impedance used must be increased at least to 170 ohms, and the capacitance ratio C_2/C_3 must be larger than 0.05.

10-3 CIRCUITS FOR COMMON-BASE OSCILLATORS

The tuned coupling circuit, which is required for use with a common-base oscillator, differs in two ways from that for the common-emitter oscillator, first in that phase-inversion is not required, and second in that the impedance ratio required is considerably larger because of the extremely low input impedance of the

*There are insufficient data for accurate determination of a value of C_4 or for correcting it.

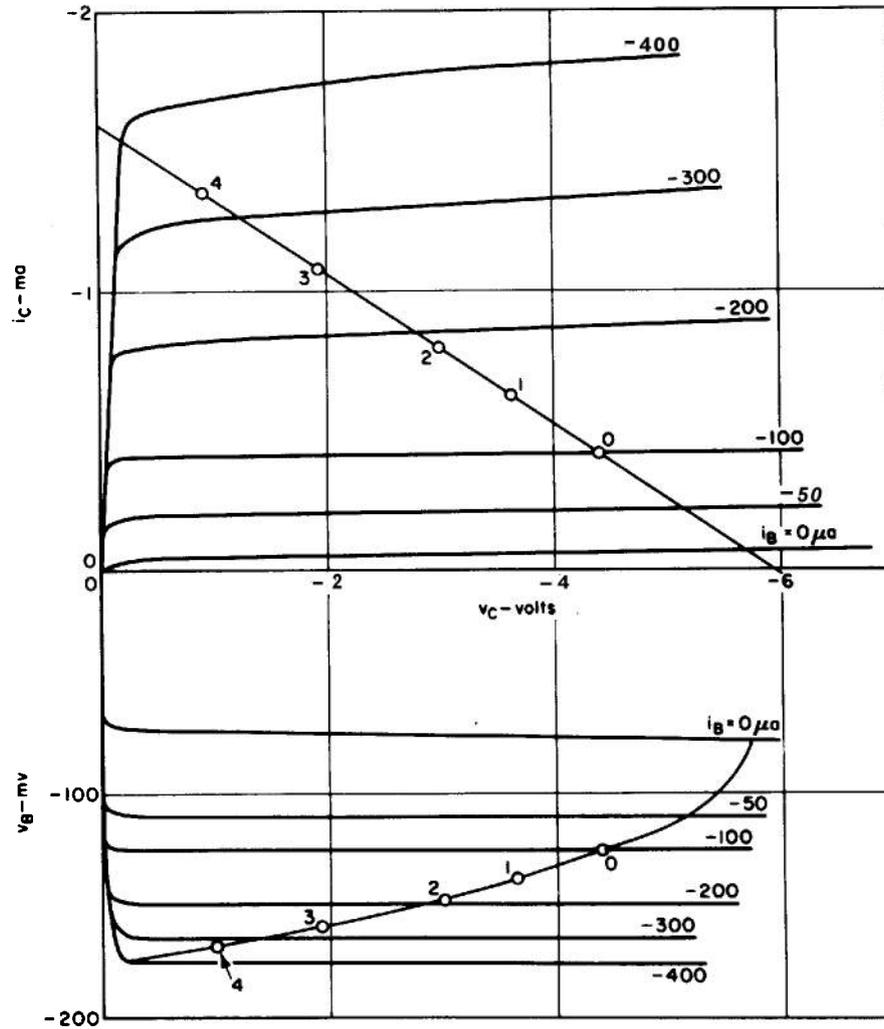


Fig. 10-7. Design of Colpitts Oscillator SBDT-10X for Example 10-2

active device. Instead of having an RF ground in the middle of the coil or at the tap between the two capacitors, the ground for the common-base circuit is at one end of the coil (Fig. 10-8). The equations for the Hartley oscillator in its common-base configuration need no other change than noting that L_2 in the numerator of now is the total inductance, and L_3 is only a part of it. A similar change is required for the Colpitts oscillator in its common-base configuration, the input capacitance in the numerator of the input impedance expression now being

$$C_2' = C_2 C_3 / (C_2 + C_3)$$

The tapped coil arrangement is the better one to use

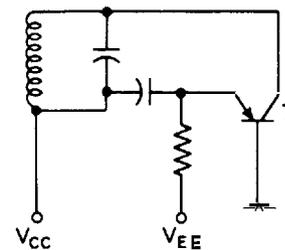


Fig. 10-8. Common-base Oscillator

where possible with the common-base circuit, because the impedance ratio required is too large to handle through the action of the circuit Q-factor. Typically, the ratio may be as large as 2000 : 1, and the corre-

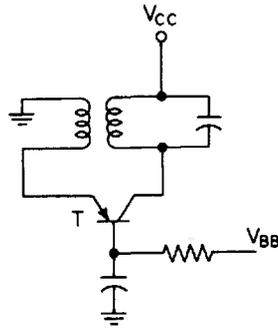


Fig. 10-9. Common-base Inductively-coupled Oscillator

sponding capacitance ratio would be 45 : 1. An operating Q-factor for the circuit as large as 200 or more is required for efficient and stable operation.

Because of the magnitude of input current required by the active device in the common-base circuit and its resultant low input impedance, a magnetic-coupled circuit (Fig. 10-9) often is desirable as the frequency-selection and feedback network. The tuned circuit should be placed at the point in the circuit in which the loading due to the transistor is a minimum. In both the common-emitter and the common-base circuits, this location is in the collector circuit because the shunt capacitance and the shunt conductance both are smallest there. The selection of the collector return for the tuned circuit is much more important with the common-base oscillator because of the much higher input conductance in the emitter return than in the base.

Inductive coupling is convenient in another way, in that the capacitance values required for construction of the feedback circuit are considerably smaller than the values required in the Colpitts and the Hartley circuits. An untuned link is used to couple energy into the input, either the base or the emitter, and it is partially resonated by the input capacitance of the device. In the common-base circuit, the effect of base-spreading resistance is minimized and the energy can be introduced comparatively effectively.

The value of the reactance of the output link should at most be equal to the equivalent input resistance of the circuit, or

$$X_o G_i \leq 1 \tag{10-24}$$

where X_o is the reactance of the output link. Then the coupling between the link and the tuned circuit should be adjusted until sufficient power for the development

of unity loop amplification is provided to the input. The ease of adjustment of feedback through the variation of the magnitude of the coupling coefficient makes this type of design particularly convenient to use.

The procedure for the design of common-base oscillators closely resembles that for the common-emitter oscillator. For an exact design, it is desirable to make the configuration correction already described which transfers the common-emitter load contours into common-base contours, and then to adjust for constant emitter current, because the emitter current is stabilized in this type of circuit. The limit contours are established in the same manner as before, except for the fact that the emitter current is averaged rather than the base current, and the small-signal equations used are for the common-base configuration.

The small-signal equations for the impedances of the feedback circuit using magnetic coupling are

$$Z_I = L_1 / (R_1 C) \tag{10-25}$$

$$Z_T = -k \sqrt{L_2 L_2} / (R_1 C) = -M / (R_1 C) \tag{10-26}$$

$$Z_O \doteq j\omega L_2 + j\omega^3 M^2 C / (1 - \omega^2 L_1 C + j\omega R_1 C) \tag{10-27}$$

$$Z_O \doteq j\omega L_2 + M^2 / (R_1 L_1 C) \tag{10-27a}$$

where the resonant frequency is defined as $\omega^2 L_1 C = 1$. Evidently, the first two are resonant in nature, that is, they depend on the resonance of L_1 and C , whereas, because of the relatively small coupling, Z_O does not depend on the resonance to any great extent. When the last equation is simplified at resonance to give the form of Eq. 10-27a, further simplification by substitution for M gives the form

$$Z_O = j\omega L_2 + k^2 L_2 / (R_1 C) \tag{10-28}$$

For large values of k , the value of Z_O will depend on the resonant circuit; for small values, on the coupling link. For this reason, a small value of coupling that will give the required transfer impedance with a reasonable value of L_2 should be selected.

The effective value of the secondary inductance L_2 may actually be increased through the action of the load capacitance from the input of the active device, the

modified value of the inductance being given by the equation

$$L_{\text{eff}} = L_2/[1 - L_2C_i/(L_1C)] \quad (10-29)$$

If the magnitude of the ratio in the denominator is greater than 0.1, then the value of L_2 should be chosen to allow for the effect of the difference. Otherwise, the tuned impedance of the output circuit may be excessive.

10-4 A SERIES-MODE OSCILLATOR

A series-mode circuit like that shown in Fig. 10-10 is commonly used in the construction of crystal oscillators, and it may also be used with L-C circuits if adequate step-down is incorporated. An extremely large value of Q-factor is desirable in the series element Y_s to give maximum frequency stability and minimum series impedance at resonance. Since the circuit must be used in the common-base configuration, current gain is required at the input point to provide for the less-than-unity gain from the emitter to the collector. This is the reason the inductor is shown tapped. The auto-transformer action gives the current gain required.

The equations for use with this coupling circuit, where G_i is the input admittance of the associated transistor, are

$$Z_I \doteq L_T(1 + G_iZ_s)/[R_T C(1 + G_iZ_s) + G_i(L_1 + C(R_1R_2 - \omega^2(L_1L_2 - M^2)))] \quad (10-30)$$

$$Z_T \doteq (L_1 + M)/[R_T C(1 + G_iZ_s) + G_i(L_1 + C(R_1R_2 - \omega^2(L_1L_2 - M^2)))] \quad (10-31)$$

$$Z_O \doteq \langle Z_s(1 - \omega^2L_2C) + j\omega[L_1 - \omega^2C(L_1L_2 - M^2)] \rangle / \langle j\omega[R_T C(1 + G_iZ_s) + G_i(L_1 + C(R_1R_2 - \omega^2(L_1L_2 - M^2)))] \rangle \quad (10-32)$$

For small values of Z_s , Eq. 10-32 reduces to

$$Z_O \doteq L_1/[CR_T + G_iL_1 + CR_1G_iZ_s] \quad (10-33)$$

For Eqs. 10-30 through 10-33, the following conditions apply

$$\begin{aligned} \omega^2[C(L_1 + L_2 + 2M) + G_iC(R_1L_2 + R_2L_1)/(1 + G_iZ_s)] &= 1 \\ Z_i = Z_1 + Z_2 + 2Z_{12} = R_1 + R_2 + j\omega(L_1 + L_2 + 2M) &= R_T + j\omega L_T \\ Y_c = j\omega C, \quad Z_s = R_s + j/(\omega L_s - 1/(\omega C_s)) & \\ R_T \ll \omega L_T, \quad L_1L_2 - M^2 \ll (L_1 + L_2 + 2M)^2 & \end{aligned} \quad (10-34)$$

When G_iZ_s is approximately unity, Eqs. 10-30 through 10-33 may be simplified to

$$Z_I \doteq L_T/R_T C \quad (10-35)$$

$$Z_T \doteq (L_1 + M)/\langle R_T C(1 + G_iZ_s) \rangle \quad (10-36)$$

$$Z_O \doteq L_1/[G_iL_1 + C(R_T + R_1G_iZ_s)] \quad (10-37)$$

The crystal impedance Z_s affects principally the characteristics of the transfer and output impedances, decreasing the transfer impedance sharply and increasing the output impedance off the resonant frequency, $\omega^2 = 1/(L_sC_s)$. In this application, the value of G_i , the input admittance for the active device, must be sufficiently large to make $G_iR_s \geq 1$. Otherwise, the frequency-selection action will be inadequate. When a transistor capable of meeting other limitations such as the noise-corner limitation is selected, the effect of the input capacitance of the device normally may be neglected in the design process.

EXAMPLE 10-3. Design a crystal oscillator based on the circuit of Fig. 10-10 using the SBDT-10X used in Example 10-2. Determine if load-line corrections are required, and determine suitable values for the impedances in Eqs. 10-35 through 10-37. Take the initial operating point as $V_{cc} = -3 \text{ V}$ and $I_{cs} = -0.8 \text{ mA}$.

Since less than 0.2 V correction is required on the load-line position for conversion from common-emitter to common-base operation, the correction need not be made. However, the corrected line is plotted as a matter of interest in Fig. 10-11. Next, orthogonal polynomials may be used to evaluate both g_p' and $(g_i' + g_p')$, taking the value of r_b' and correcting the values read from the curves. The tuned circuit may be designed to provide the proper value of Z_i and the turns-ratio selected through the relation

$$Z_I/Z_T = (n_1 + n_2)(1 + G_iZ_s)/n_2 \quad (10-38)$$

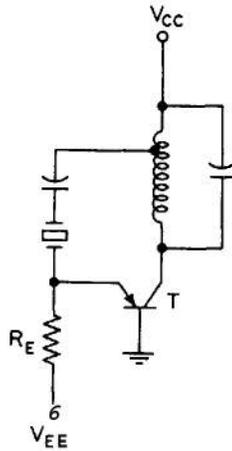


Fig. 10-10. Crystal Oscillator

where n_1 is the number of turns in L_1 , and n_2 is the number in L_2 . This relation implies that the coils L_1 and L_2 are both parts of a single complete coil and the coefficients by which the numbers of turns are multiplied are thereby identical. The tap is obtained by way of a soldered contact on one of the turns at the appropriate position. Solving Eq. 10-38 for the transfer impedance gives

$$Z_T = n_2 Z_I / \langle (n_1 + n_2)(1 + G_i Z_s) \rangle \quad (10-39)$$

Evidently, the higher the crystal impedance, the lower the transfer impedance for any given value of turns-ratio, $n_2/(n_1 + n_2)$. In practice, a value of $G_i R_s$ in the neighborhood of unity probably is optimum. Consequently, a crystal having a very small value of series resistance at resonance is of paramount importance in this application.

The use of the load line drawn on the curves for a Z_I of 3750 ohms, gives a forward gain of approximately 86 in the common-emitter configuration. Including $G_i R_s = 1$ in the common-base configuration decreases the common-base amplification to a value of 43. Solving Eq. 10-39 for n_1/n_2 gives a value of 43.4 ($Z_T = 42.2$; $Z_I = 3750$). For stability reasons, a lower load impedance for the collector circuit may be chosen, since regenerative instability may develop with such a high value of Z_I . The input admittance is approximately 31,000 pmhos, and the forward admittance 23,000 pmhos, neglecting the base-spreading resistance. The calculation of the corrected values is left as an exercise for the reader. A crystal having a series impedance less than 30 ohms at resonance is required.

10-5 OTHER CIRCUITS

The variety of circuits that can be analyzed and designed through the combination of conductance techniques and topological procedures is only limited by the user's ingenuity. The determination of the input and output impedances and the transfer impedance for a given network provides all the data on the feedback network required for the coordination of the device with its circuit. As long as a set of input and output curves are available on a given transistor, the curves being in a form that permits convenient reploting of the load lines and the reading of the required coordinates, orthogonal polynomials can be used to convert the coordinate data into estimated operating conditions, and an approximate set of operating specifications can be obtained. If full data on small-signal parameters are available, a better design that delineates the operating limits closely can be developed.

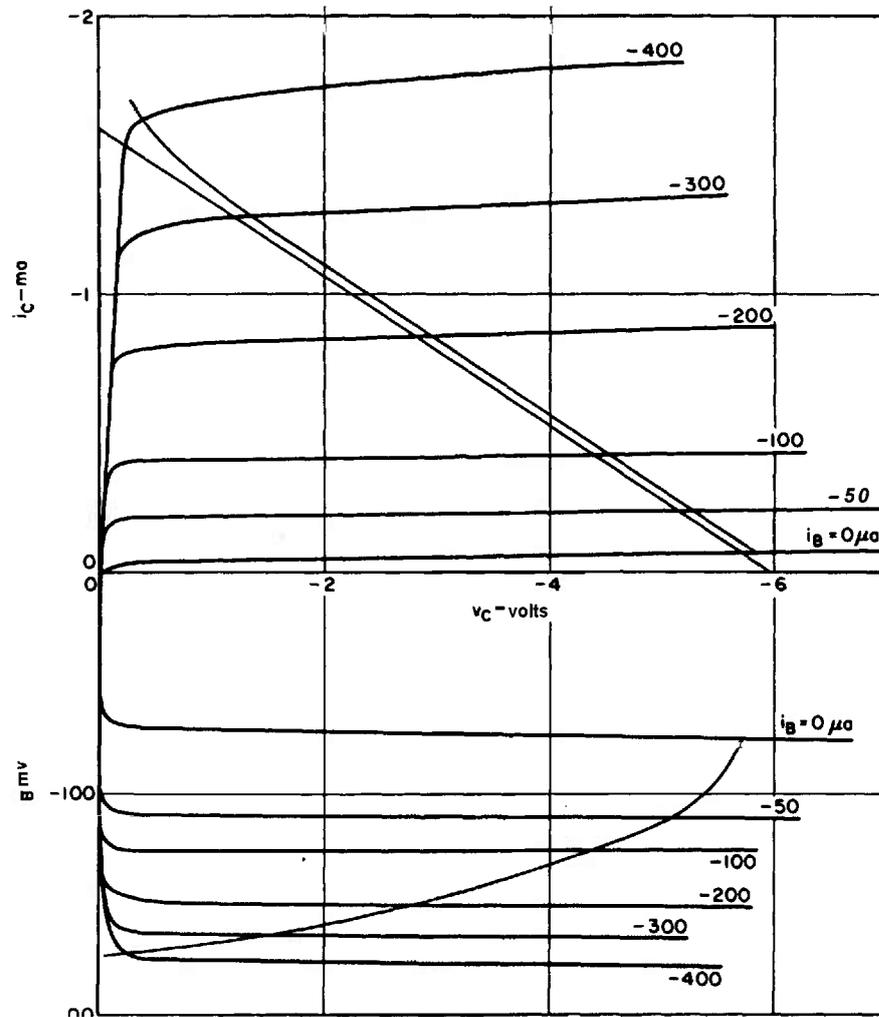


Fig. 10-11. Correction for Common-base Configuration of a Crystal Oscillator

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2. R. D. Middlebrook, "A New Junction-Transistor High-Frequency Equivalent Circuit", *IRE Trans., PGCT*, Conv. Rec., 1957, p. 120.

CHAPTER 11

R-C OSCILLATORS AND TIME-DELAY OSCILLATORS

11-0 INTRODUCTION

The underlying theory of operation of phase-shift oscillators and time-delay oscillators is similar to that of the L-C oscillators just considered. It differs primarily in some differences in boundary conditions that are a result of the type of elements used in the feedback circuits. There are some specific differences between the R-C and the T-D oscillators, which also will be discussed in the paragraph on time-delay circuits.

11-1 TYPES OF R-C CIRCUITS

There are two basic types of R-C feedback circuits, namely, the phase-inverting, and the nonphase-inverting. The inverting types are used with active configurations that generate a phase-reversal of their own, whereas the noninverting type are normally used with more complex circuits in which both current and voltage gain are available and the output voltage is in phase with the input.

The inverting feedback circuits typically make use of some form of ladder network as shown in Fig. 11-1. The Z components in this network Z_j usually are all of one type, for example, all resistors or all capacitors, and the Y components Y_k are all of the alternate type. With R-C ladder networks, one type of element provides energy storage, whereas the other introduces dissipation of energy. Although any number of sections may in theory be used in a ladder network, the use of less than three sections introduces practically impossible operating conditions for the development of oscillations in an inverting circuit, and the use of more than four makes possible the development of more than one mode of oscillation. Ordinarily the ladder *used* is a three-section ladder with either an input or an output resistive termination.

The noninverting circuits normally are based on some form of Wien-bridge arrangement such as is shown in Fig. 11-2. The amplifier *used* with this circuit must have both current and voltage gain, and must

have an output voltage in phase with its input. For these reasons, a minimum of two active devices is required for the associated amplifiers. Either of the amplifier configurations shown in Fig. 11-3 may be used for the active path with these oscillators, the more complex one having built-in gain stabilization.

The use of R-C circuits presents difficulties with transistors as the active devices because of the problem of their low, but not zero, input impedance. The design of a transfer network to couple a current source to a low, but not zero, impedance load is appreciably more difficult than coupling from a current source to a voltage load, as is possible with oscillators using electron tubes. As with L-C oscillators, the limitation of amplification in an R-C oscillator can only occur effectively if the source impedance from which the transistor is excited is small compared with the input impedance of

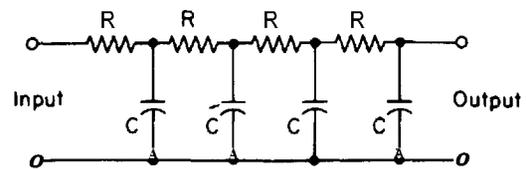


Fig. 11-1. Typical Ladder Network

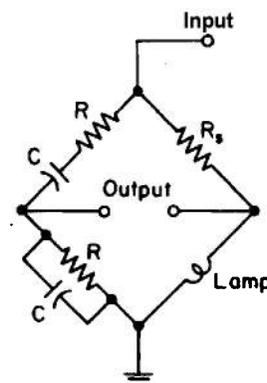


Fig. 11-2. Wien-bridge Circuit

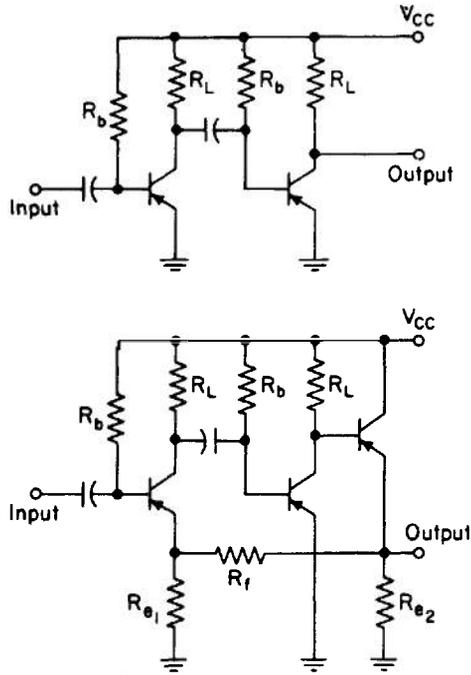


Fig. 11-3. Typical Amplifiers

the transistor itself. Because even in a common-emitter configuration the base input admittance may be as large as 0.001 mho, the relatively high output impedance associated with many R-C networks makes the design of an oscillator around the circuit difficult unless an emitter-follower is used to match impedances. This situation applies equally to the inverting and to the noninverting circuits.

The zero-phase-shift or bridge circuit is designed in a manner that gives it a maximum amplification over a narrow range of frequencies, in the middle of which is the frequency of zero-phase-shift. Typically, the bridge consists of a combination of dissipation and storage elements used in conjunction with similar elements arranged in the dual network configuration as shown in Fig. 11-4. (The network dual arrangement for a series R-C network is a parallel R-C network, for example.) More complex configurations may be used if desired, and a greater frequency stability may be obtained if the rate-of-change of phase with frequency is increased. Normally, however, a simple R-C dual configuration such as is shown in Fig. 11-4 is used with zero-phase R-C oscillators.

The amplitude-stabilization of the R-C oscillator introduces a special set of problems to the designer. Because of the relatively low equivalent Q of the frequency-selection circuit, bias limiting is not practical with

these circuits because of the associated distortion, and some form of thermal bridge limiting is normally chosen. Both the forward and the feedback gain must be kept quite uniform over the operating range of the oscillator, which may be as much as four decades of frequency.

The operation of the Wien-bridge oscillator closely parallels that of the Meacham crystal oscillator as far as phase characteristics are concerned. In one, the amplitude and phase are controlled by the RLC-properties of the crystal in conjunction with a fixed series resistance, the second arm of the bridge consisting of a thermal combination for controlling the signal amplitude. In the Wien-bridge circuit, the series elements on one half of the bridge consist of the dual R-C combinations, and the elements in the other half of the bridge again include a thermal element for controlling signal amplitude.

The next two paragraphs of this chapter analyze the properties of the typical forms of the feedback circuit for both inverting and noninverting networks, and include some typical design analyses. They are followed by a discussion of time-delay oscillators based on the use of delay lines as the feedback network. A brief discussion of one- and two-port negative immittances is also included.

11-2 THE BASIC FEEDBACK CIRCUIT—INVERTING FORM

The analysis of the basic ladder network (Fig. 11-5) without source or terminating impedance gives a considerable insight into the frequency-selective behavior of the phase-shift circuit. The series elements in this network are identified as impedances, Z_i typically, and the shunt elements as Y_j . For simplicity, the Z_i 's may

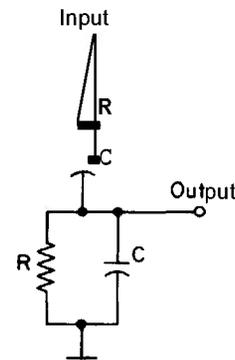


Fig. 11-4. R-C Selection Circuit

be replaced by Y_i 's for topological solution of the network and then the equation may be converted to include the series impedances by multiplication of the numerator and denominator of the appropriate impedance equation by the product of the series impedances.

Transistors, as tubes, are current-output devices, so that the form of network normally called for in the feedback path is the trans-impedance form. Several forms of the ladder network will be discussed in the next few paragraphs because a considerable amount of useful information can be gained thereby.

Topological techniques offer a convenient method for analyzing these coupling networks. A limited range of variations can then be made in input and output circuits without necessitating complete re-analysis. In addition, the process of analysis is simplified because of the elimination of unnecessary steps in the solution. The three impedance equations for the simplest configuration of three-section ladder network are

$$Z_I = [1 + Z_1Y_2 + Z_1Y_4 + Z_3Y_4 + Z_1Y_6 + Z_3Y_6 + Z_5Y_6 + Z_1Z_3Y_2Y_4 + Z_1Z_3Y_2Y_6 + Z_1Z_5Y_2Y_6 + Z_1Z_3Y_4Y_6 + Z_3Z_5Y_4Y_6 + Z_1Z_3Z_5Y_2Y_4Y_6] / [Y_2 + Y_4 + Y_6 + Z_3Y_2Y_4 + Z_3Y_2Y_6 + Z_5Y_2Y_6 + Z_5Y_4Y_6 + Z_3Z_5Y_2Y_4Y_6] \quad (11-1)$$

$$Z_T = 1/[Y_2 + Y_4 + Y_6 + Z_3Y_2Y_4 + Z_3Y_2Y_6 + Z_5Y_2Y_6 + Z_5Y_4Y_6 + Z_3Z_5Y_2Y_4Y_6] \quad (11-2)$$

$$Z_O = [1 + Z_3Y_2 + Z_5Y_2 + Z_5Y_4 + Z_3Z_5Y_2Y_4] / [Y_2 + Y_4 + Y_6 + Z_3Y_2Y_4 + Z_3Y_2Y_6 + Z_5Y_2Y_6 + Z_5Y_4Y_6 + Z_3Z_5Y_2Y_4Y_6] \quad (11-3)$$

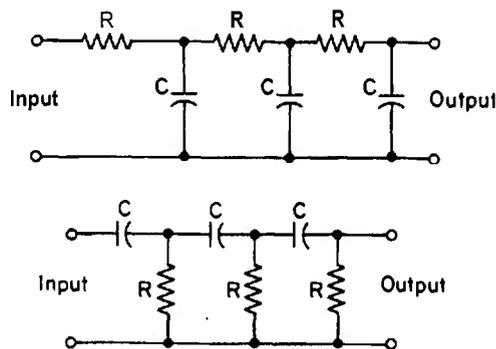


Fig. 11-5. Three-section R-C Network—Basic Forms

Examination of the denominator of the transfer term shows that the values of the powers of (ZY) for the respective terms are 0, 1, and 2 only. An R-C network formed from this combination of components, where either the Z 's are resistive and the Y 's are capacitive, or vice versa, cannot in any way develop 180deg phase-shift and unity gain without having infinite amplification. The minimum exponent difference that can yield 180 deg phase shift with a finite amplification is 3.

The denominator function, which represents a ladder network, has a frequency polynomial that can be solved in either of two forms, the one representing forward transmission, and the second, backward transmission. Essentially, the forward transmission mode is the impedance mode, with higher output impedance than input, and the backward transmission with a lower output impedance than input (higher output admittance). The denominator for the transfer function in Eq. 11-2 cannot be solved in useful form for either mode of transmission, as has already been shown. With the network modified by the inclusion of the input admittance Y_0 , however, the situation is completely changed, because either Y_0 can be factored out, and a solvable network established in terms of $Z_1, Z_3, Z_5, Y_2, Y_4,$ and Y_6 , or Y_6 may be factored out, and a similar solvable network established involving $Z_1, Z_3, Z_5, Y_0, Y_2,$ and Y_4 . These configurations are considered by Hooper and Jackets in their paper (Ref. 1).

The numerator of the input impedance function does have the required ratio of exponents of 3 because the range of terms is from a numeric, 1, to a cubic product of Y and Z . The numerator function, however, generates only zeros of input or transmission, and consequently is of little use in frequency determination.

Consequently, without a shunt source admittance in parallel with the source current, this network is not satisfactory for use in R-C oscillators. In fact, it is easy to verify this by construction of an oscillator that utilizes the ladder network in this form. No amount of amplification will make available the required conditions for oscillation, and the oscillator will not function.

The addition of an input shunt admittance (Y_0 in Fig. 11-6), however, changes the situation appreciably. There are 34 terms each in the expressions for the input and output impedances when Y_0 is included, 21 being in the denominator, and a net of 20 in the transfer impedance. (The sign of the numerator thus is the negative of that of the denominator terms.) The equations are

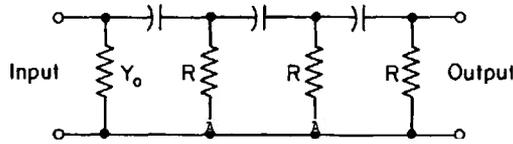


Fig. 11-6. Practical R-C Ladder Network (Forward Mode)

$$\begin{aligned}
 Z_T = & [1 + (Y_2 + Y_4 + Y_6)Z_1 + (Y_4 + Y_6)Z_3 + Y_6Z_5 \\
 & + (Y_2Y_4 + Y_2Y_6)Z_1Z_3 + (Y_2Y_6 + Y_4Y_6)Z_1Z_5 \\
 & + Y_4Y_6Z_3Z_5 + Y_2Y_4Y_6Z_1Z_3Z_5] / \{ Y_0[1 + Y_2Z_1 \\
 & + Y_4(Z_1 + Z_3) + Y_6(Z_1 + Z_3 + Z_5) \\
 & + Y_2Y_4Z_1Z_3 + Y_2Y_6(Z_1Z_3 + Z_1Z_5) \\
 & + Y_4Y_6(Z_1Z_5 + Z_3Z_5) + Y_2Y_4Y_6Z_1Z_3Z_5] \\
 & + [Y_2 + Y_4 + Y_6 + Y_2Y_4Z_3 + Y_2Y_6(Z_3 + Z_5) \\
 & + Y_4Y_6Z_5 + Y_2Y_4Y_6Z_3Z_5] \}
 \end{aligned}
 \tag{11-4}$$

$$\begin{aligned}
 Z_T = & 1 / \{ Y_0[1 + Y_2Z_1 + Y_4(Z_1 + Z_3) \\
 & + Y_6(Z_1 + Z_3 + Z_5) + Y_2Y_4Z_1Z_3 \\
 & + Y_2Y_6(Z_1Z_3 + Z_1Z_5) + Y_4Y_6(Z_1Z_5 + Z_3Z_5) \\
 & + Y_2Y_4Y_6Z_1Z_3Z_5] + [Y_2 + Y_4 + Y_6 + Y_2Y_4Z_3 \\
 & + Y_2Y_6(Z_3 + Z_5) + Y_4Y_6Z_5 + Y_2Y_4Y_6Z_3Z_5] \}
 \end{aligned}
 \tag{11-5}$$

The output impedance may be found from the input by making the following substitutions

$$\begin{aligned}
 Y_0 \rightarrow Y_6, \quad Y_6 \rightarrow Y_0, \quad Y_2 \rightarrow Y_4, \quad Y_4 \rightarrow Y_2, \\
 Z_6 \rightarrow Z_1, \quad Z_1 \rightarrow Z_5
 \end{aligned}
 \tag{11-6}$$

This substitution is possible because of the completeness of the symmetry of the topology of the network.

In these equations, if Y_0 has the value zero, the expressions reduce to the previous form. If, however, Y_0 is given a value large enough that the second denominator bracket may be neglected, then the

denominator of the transfer function is of order 3, and the possibility of construction of a successful phase-shift network exists.

The elements of the network, i.e., those in the Z group, and those in the Y group, are normally equal in immittance within each group, or they may be scaled in a manner that keeps the ratios of the immittances of corresponding elements in the Z and Y groups equal to the ratios for other corresponding elements. For equal immittances, that is, for $Y_2 = Y_4 = Y_6$ and $Z_1 = Z_3 = Z_5$, etc., and Y_0 as the source element, the denominator of the transfer function takes the form, where $Y_2 = j\omega C$ and $Z_1 = R$ and for a value of Y_0 large compared to Y_2 and $1/Z_1$

$$D = [1 + j\omega 6CR - \omega^2 5C^2R^2 - j\omega^3 C^3R^3] Y_0 \tag{11-7}$$

The operating frequency is specified by the 180 deg phase-shift condition, i.e., when the coefficient of the imaginary operator is zero and the real component is negative. This condition occurs when $\omega = \sqrt{6}/(CR) = \omega_0$. The corresponding value for the real components is -29 , making necessary an amplification of -29 to offset the network gain of $-1/29$.

The position of the capacitance and resistance elements in the basic ladder circuit has little effect on the operation of the circuit with the exception of a modification of the position of the multiplicative constant, the $\sqrt{6}$ above, which must be used with the values of capacitance and resistance to determine the operating frequency. The denominator expression given above is modified to its dual form when the resistor and the capacitor positions are interchanged, taking the form

$$\begin{aligned}
 D = & Y_0 [1 + 6/(j\omega CR) - 5/(\omega^2 C^2 R^2) \\
 & - 1/(j\omega^3 C^3 R^3)]
 \end{aligned}
 \tag{11-8}$$

The imaginary part of this expression, when equated to zero and solved gives the radian frequency

$$\omega_0 = 1/(RC\sqrt{6}) \tag{11-9a}$$

For the other circuit, it was

$$\omega_0 = \sqrt{6} / (RC) \quad (11-9b)$$

And the real part again is -29 . Thus, the effect of interchange of the positions of the capacitors and resistors is to shift the position of the factor $\sqrt{6}$, depending on whether the network is used as a low- or a high-pass filter.

If the numerator of the transfer function is imaginary instead of real (i.e., Y_0 is imaginary instead of real), then the function of frequency discrimination and amplitude loss may be changed in the real and the imaginary parts of the bracket in Eqs. 11-7 and 11-8. This can change the $\sqrt{6}$ to a $\sqrt{5}$ in the untapered circuit, or the factor $[k^2 + 2k + 3]^{0.5}$ to $[2k + 3]^{0.5}$ in the tapered circuit.

When a taper is included in the immittances in such a way that the scaling on the resistances and capacitances are inverse to each other, then the component sizes are related by the equation

$$k = (Y_2/Y_4) = (Y_4/Y_6) = (Z_3/Z_1) = (Z_6/Z_3) \quad (11-10)$$

When these relations are substituted into the equation for the transfer impedance, the denominator takes the form for $Y_2 = j\omega C_2$ and $Z_1 = R_1$

$$D = Y_0 \{ 1 + j\omega [1 + k(1 + (1/k)) + k^2(1 + (1/k)) + (1/k^2)] C_2 R_1 - \omega^2 [1 + k^2((1/k) + (1/k^2)) + k^3((1/k^2) + (1/k^3))] C_2^2 R_1^2 - j\omega^3 C_2^3 R_1^3 \} \quad (11-11)$$

The solution of this equation for the real and imaginary roots gives the above factors. The more important root equation is

$$\omega_0^2 = [k^2 + 2k + 3] / (C_2^2 R_1^2) = (k^2 + 2k + 3) \omega_1^2 \quad (11-12)$$

where the value of ω_1 is defined by the equation

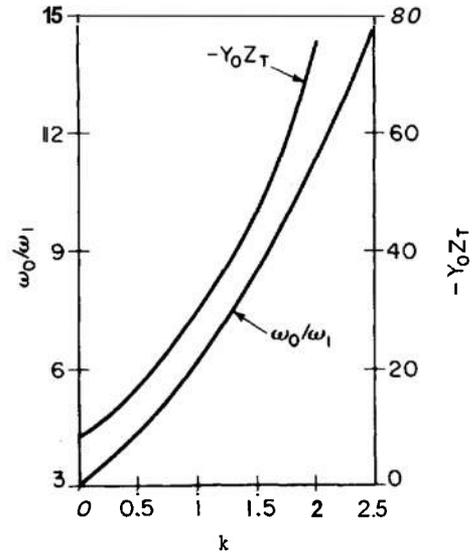


Fig. 11-7. Effect of Taper k on Network

$$\omega_1^2 = 1 / (C_2 R_1) \quad (11-12a)$$

Substituting the root equation back into the denominator gives the forward impedance for the network in the form

$$Z_T = 1 / \langle Y_0 (1 - 9 - 12k - 7k^2 - 2k^3) \rangle = 1 / \langle - Y_0 (8 + 12k + 7k^2 + 2k^3) \rangle \quad (11-13)$$

Both the required amplification and the operating frequency are consequently a function of k , for any specified product $C_2 R_1$. The value of the ratio ω_0/ω_1 and the value of the function $[8 + 12k + 7k^2 + 2k^3]$ as a function of k are shown in Fig. 11-7.

The feedback network can take an admittance form as well as an impedance form, in which case the input signal must have a low source impedance (Fig. 11-8). The output from the network may either be taken as the current flowing through Y_6 , or it may be taken as the voltage across Y_6 .

One limitation applies to the Y_0 component of the network, in that it must include a conductance element to permit the passage of collector current. Under spe-

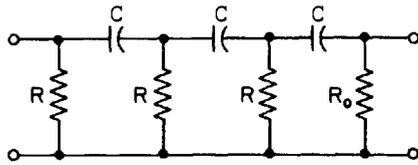


Fig. 11-8. Practical R-C Ladder Network (Reverse Mode)

cial conditions it is possible to avoid this constraint. These special cases are not considered here.

In the incorporation of R-C feedback networks into transistor oscillators, the output of a conventional transistor amplifier is best represented in the form of a current source. It is therefore desirable to use the transimpedance form of a circuit. The output characteristics of this form of R-C circuit are poorly suited to use in the forward transfer configuration in which Y_6 is the final output element, because the input admittance of the transistor is high, and the output admittance of the network is small. The reverse-transfer configuration, in which Y_0 , Y_2 , and Y_4 are ladder elements, however, and in which Y_6 is large, is better suited to the design requirements. The denominators for the two modes of operation are

Forward

$$\begin{aligned}
 D = & Y_0(1 + Y_2Z_1 + Y_4(Z_1 + Z_3) \\
 & + Y_6(Z_1 + Z_3 + Z_5) + Y_2Y_4Z_1Z_3 \\
 & + Y_2Y_6(Z_1Z_3 + Z_1Z_5) + Y_4Y_6(Z_1Z_5 + Z_3Z_5) \\
 & + Y_2Y_4Y_6Z_1Z_3Z_5]
 \end{aligned}
 \tag{11-14}$$

Reverse

$$\begin{aligned}
 D = & Y_6(1 + Y_0(Z_1 + Z_3 + Z_5) + Y_2(Z_3 + Z_5) \\
 & + Y_4Z_5 + Y_2Y_4Z_3Z_5 + Y_0Y_2(Z_1Z_3 + Z_1Z_5) \\
 & + Y_0Y_4(Z_1Z_5 + Z_3Z_5) + Y_0Y_2Y_4Z_1Z_3Z_5]
 \end{aligned}
 \tag{11-15}$$

The first of these equations applies to either the equivalent transfer impedance or to the transfer admittance if Y_0 is large compared to the remaining admittances Y_1 , Y_2 , Y_3 , Y_4 , Y_5 , and Y_6 as specified in Eqs. 11-4 and 11-5, whereas the second applies if Y_6 is large compared to the remaining admittances. For the forward-impedance circuit, the gain is determined in terms of the value of Z_0 divided by the bracket function, and for the backward-impedance circuit in terms of the value of Z_6 and the corresponding bracket function.

Emitter-followers may be required with the transistor amplifiers used with these oscillators if the network is used in the forward-admittance configuration (one provides the source signal for the network), or the forward-impedance configuration (it is used as a repeater for the output signal). If the network is used in the backward-impedance mode, correct matching of impedance levels results, but the limiting of amplitude of oscillation may be unsatisfactory. Emitter-followers are not essential if adequate limiting is obtained without them. The transistor is operating in the current-gain mode with this configuration, however, and as a result may provide poor waveform. When perfection of waveform is important, it is essential to use the forward-impedance mode with an emitter-follower to provide the input signal for the amplifier.

EXAMPLE 11-1. Design 1000 Hz R-C oscillators using as many as possible of the above configurations based on a transistor having a forward admittance g_f of 30,000 pmhos, an input admittance of 150 pmhos, and a base-spreading resistance of 100 ohms. Assume that the other parameters of the device may be neglected, and assume that adequate oscillator limiting will occur in any configuration. (In other words, make a linearized design; any of the designs described in Chapters 9 and 10 could be studied for nonlinearity problems.)

First the conditions required for the establishment of a forward-transfer oscillator for use with a transistor having a β of 200 may be examined.

The range of voltage gain in the transistor is limited by the forward conductance of the device multiplied by the effective load resistance, which is here $1/g_i$, the input resistance. The minimum amplification will be $g_f Z_0$, and the maximum $g_f/g_i = \beta$. The resistance required in the frequency-selection network must lie between Z_0 and $1/G_i$ and at the same time, the minimum permitted value for the expression $g_f Z_0$ is 29. The following inequality expresses the relation

$$g_f Z_0 \ll g_f R_2 \leq g_f/g_i = \beta \tag{11-16}$$

This simplifies to

$$29 \ll g_f R_2 \leq 200$$

Evidently, these conditions cannot be met, because the ratio of the minimum to the maximum number is only 7. An emitter-follower amplifier is therefore required as a matching section between the output of the transfer network and the input of the active device.

If, on the other hand, the backward-transfer network is utilized, then the amplification of the feedback network is controlled by Z_6 , which nominally may have a value of approximately 2000 ohms. The values of R_0 , R_2 , and R_4 would be greater than 5000 ohms, and the value of Z_6 would be reduced by loading to give a loop amplification of 40 to 50, more or less. Selection of values of R_0 , R_2 , and R_4 in the neighborhood of 10,000 or more ohms, and Z_6 to have a total of 750 ohms, including the transistor input, means that a forward conductance of approximately 40,000 pmhos is required. The corresponding value of Y_6 is 1333 pmhos, which is considerably more than the input admittance of the transistor, 200 pmhos. Consequently, a consistent design is obtainable under these conditions. The combined value for Y_6 should be as near an order-of-magnitude larger than G_i as possible.

The ladder elements, with resistive components of 10,000 ohms include capacitances of value 0.0065 mF for the high-pass configuration, and 0.039 mF for the low-pass configuration for the normal, untapered, network. The effect of network taper may now be considered.

The maximum value of k that can be permitted is determined by the current gain available in the active device. Although it might appear superficially that there was advantage in using a value of k appreciably greater than unity with the reverse-transfer network (Hooper's current feedback network), the limitations on the termination impedance Z_6 offset any apparent advantages. The feedback loss increases so rapidly that the use of a value of k in excess of 2.50 is likely to introduce serious difficulties. A value of k of 0.5 is

convenient for many ordinary applications, because then the feedback loss is 16, making an amplifier amplification of 16 necessary. The corresponding frequency factor is $\sqrt{4.25}$, or 2.060. This factor is in the numerator with low-pass networks, in the denominator with high-pass. In the backward-transfer mode, the network must have the high-pass configuration, because the source element Y_0 is a part of the frequency-selection network instead of being a driver impedance, as with the forward-transfer configuration.

11-2.1 MULTISECTION LADDERS

As an example of multisection ladders, a four-section ladder may be used for the frequency-determining feedback path. Such a network, if properly terminated at either end, will have a single operating frequency, and since only 45 deg per section phase shift is required, it will not have any more loss than does a corresponding three-section tapered filter. The transfer equation for such a network is

$$Z_T = Z_0/[1 + 10ZY + 15Z^2Y^2 + 7Z^3Y^3 + Z^4Y^4 + Z_0(4Y + 10Y^2Z + 6Y^3Z^2 + Y^4Z^3)] \tag{11-17}$$

where Y and Z are the network immittances, and Z_0 is either the input or the termination impedance, as required.

The simplest method of getting the coefficients for the terms of the transfer equations is by the establishment of an addition chain based on the continued-fraction expansion of the ladder network (for a detailed discussion see Ref. 2). It takes the form:

TABLE 11-1
EXPONENT OF (yZ)

Function	0	1	2	3	4	5	6	7	8	9
Y_1	1									
F_1	1	1								
Y_2	2	1								
F_2	1	3	1							
Y_3	3	4	1							
F_3	1	6	5	1						
Y_4	4	10	6	1						
F_4	1	10	15	7	1					
Y_5	5	20	21	8	1					
F_5	1	15	35	28	9	1				
Y_6	6	35	56	36	10	1				
F_6	1	21	70	84	45	11	1			
Y_7	7	56	126	120	55	12	1			
F_7	1	28	126	210	165	66	13	1		
Y_8	8	84	252	330	220	78	14	1		
F_8	1	36	210	462	495	286	91	15	1	
Y_9	9	120	462	792	715	364	105	16	1	
F_9	1	45	330	924	1287	1001	455	120	17	1

In Table 11-1, each row is formed from the two rows above it. To obtain Y_{j+1} , for example, the values of the coefficients for Y_j and F_j are added directly. Similarly, to find the coefficients for F_{j+1} , the coefficients for F_j are added to those for Y_{j+1} after Y_{j+1} has been multiplied by YZ to *shift each coefficient one column to the right*. The F term is the frequency-determination term, and the Y term is the one whose value should be made negligible for efficient operation. In terms of these functions, the transfer impedance takes the form:

$$Z_T = Z_0/[F_j + Z_0 Y_j] \tag{11-18}$$

or

$$Z_T = Z_{2n}/[F_j + Z_{2n} Y_j]$$

where Y_j and F_j are the overall ladder functions. A factor involving a function of k is also required when the network is tapered. The network design should be such that the second term in the bracket in Eq. 11-18 is small compared to the F_j term.

11-2.2 MODIFIED TWO-SECTION LADDER

There is one other phase-shift type circuit that is important because of its simplicity and freedom from loading effects. It is a modification of the two-section ladder, and it behaves as a three-section ladder with a low-impedance termination. The basic configuration is shown in Fig. 11-9. The input admittance in this arrangement consists of a parallel combination of a Y and a Z element, and the transfer impedance takes the form

$$\begin{aligned} Z_T &= 1/[(Y + 1/Z)(1 + 3YZ + Y^2 Z^2) \\ &\quad + 2Y + Y^2 Z] \\ &= Z/[1 + 6YZ + 5Y^2 Z^2 + Y^3 Z^3] \end{aligned} \tag{11-19}$$

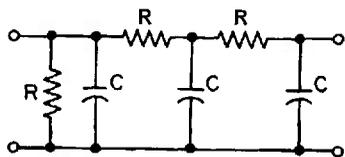


Fig. 11-9. Modified Form of Network

If Z is resistive, the frequency-dependent terms are all in the denominator, and the resonant frequency is given by

$$\omega = \sqrt{6} / (RC) \tag{11-20}$$

The transfer resistance is $R/29$, the sign being negative. If, however, Z is capacitive, then the resonant frequency determined by

$$\omega = \sqrt{5} / (RC) \tag{11-21}$$

and the transfer impedance at this frequency is $5R/29$, positive, not negative. The operating frequencies are slightly different, and one is zero-phase, the other 180 deg phase. An emitter-follower on the output of the network is required to minimize the loading introduced by the amplifier.

11-3 ZERO-PHASE-SHIFT NETWORKS

Networks having a maximum amplitude response at zero phase-angle may be used in conjunction with amplifiers having a phase-shift of either zero degrees or 360 deg to produce an additional form of $R-C$ oscillator, of which the Wien-bridge oscillator is typical. This oscillator is somewhat critical in adjustment because of a relatively slow phase-shift with frequency in the neighborhood of maximum response. The most commonly used form of this network is shown in Fig. 11-10(A), and an additional form, which sometimes is useful, is shown in Fig. 11-10(B). There are a number of variations of this circuit in use, but their modes of operation usually reduce to one of the two forms shown.

These oscillators use amplifiers that have their gain stabilized closely to a fixed value, typically 3, and use a thermistor bridge arrangement to provide the small amount of variation required to develop the loop-gain, somewhat greater than unity, needed to start the oscillator. A typical bridge circuit is shown in Fig. 11-11. The thermally-sensitive resistance R_T changes its resist-

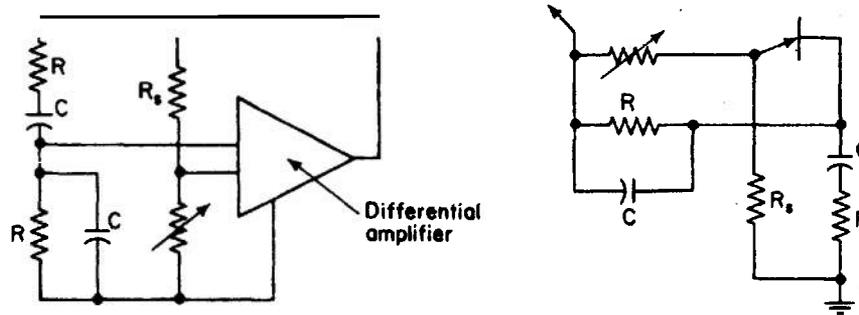


Fig. 11-10. Wien-bridge Oscillators

ance in the presence of signal, the change being in such a direction as to reduce the loop amplification, thereby stabilizing the operation and giving optimum waveform.

The feedback network for the zero-phase oscillator may be analyzed to give its input, its transfer, and its output impedances. The ordinary form of the Wien-bridge network is used as a voltage-transfer configuration, and as a result requires an emitter-follower used as a repeater. One of the other oscillators described in this paragraph uses the same frequency-selection circuit in inverted form to control oscillation, and a third uses the configuration in a low-impedance circuit for generation of high-frequency signals.

The three basic equations for use with the Wien-bridge network of Fig. 11-11 are

$$Z_I = (Y_1 Y_2 + Y_1 Y_3 + Y_2 Y_3 + Y_1 Y_4 + Y_2 Y_4) / [Y_1 Y_2 Y_3 + Y_1 Y_2 Y_4 + Y_0(Y_1 Y_2 + Y_1 Y_3 + Y_2 Y_3 + Y_1 Y_4 + Y_2 Y_4)] \approx R_0 \tag{11-22}$$

$$Z_T = Y_1 Y_2 / [Y_1 Y_2 Y_3 + Y_1 Y_2 Y_4 + Y_0(Y_1 Y_2 + Y_1 Y_3 + Y_2 Y_3 + Y_1 Y_4 + Y_2 Y_4)] \approx R_0 / 3 \tag{11-23}$$

$$Z_O = [Y_1 Y_2 + Y_0(Y_1 + Y_2)] / [Y_1 Y_2 Y_3 + Y_1 Y_2 Y_4 + Y_0(Y_1 Y_2 + Y_1 Y_3 + Y_2 Y_3 + Y_1 Y_4 + Y_2 Y_4)] \approx (R + R_0 + 1/(j\omega C)) / 3 \tag{11-24}$$

These equations hold as long as $R_0 < R$.

The principal design problem in connection with an oscillator of these general characteristics is getting it to start reliably at all frequencies over a range of many decades, and making certain that the net amplitude of oscillation is not a function of time or frequency after the initial build-up. The first condition can be achieved if the minimum initial starting amplification (closed-loop) is between 1.25 and 1.5, since then some gain margin is available, and the second requires that the amplification not reach large values compared to unity. In addition, the variation of the resistance of the thermal device with time must be slow compared to the minimum oscillation frequency.

A form of oscillator that is excellent for use at discrete frequencies or for use as a variable-frequency oscillator at high frequencies is shown in Fig. 11-12. This oscillator makes use of current drive and provides an output voltage for use in exciting the amplifier. The

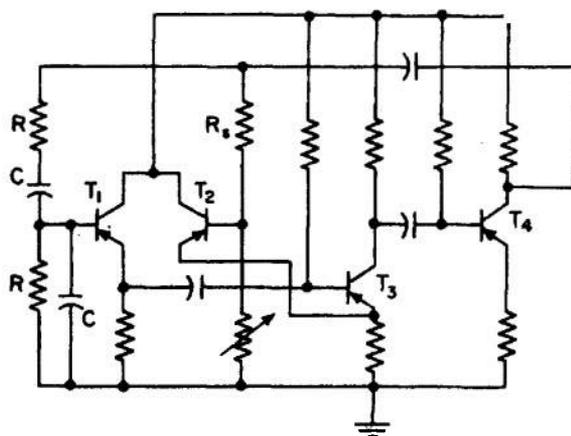


Fig. 11-11. Typical Transistorized Wien Oscillator

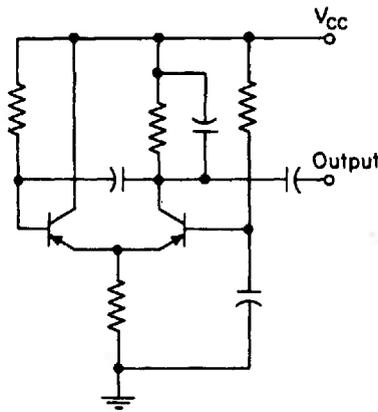


Fig. 11-12. Additional Wien-bridge Oscillator

output impedance for this network is comparatively high. The equations are

$$Z_T = \frac{(Y_3 + Y_4)/[Y_1Y_3 + Y_2Y_3 + Y_3Y_4 + Y_1Y_4 + Y_2Y_4]}{\cong \langle R + 1/(j\omega C) \rangle / 3} \quad (11-25)$$

$$Z_T = \frac{Y_3/[Y_1Y_3 + Y_2Y_3 + Y_3Y_4 + Y_1Y_4 + Y_2Y_4]}{\cong R/3} \quad (11-26)$$

$$Z_O = \frac{(Y_1 + Y_2 + Y_3)/[Y_1Y_3 + Y_2Y_3 + Y_3Y_4 + Y_1Y_4 + Y_2Y_4]}{\cong 2R/3 + 1/(j3\omega C)} \quad (11-27)$$

Because the transfer impedance is dependent on the value of resistance in the frequency-selection circuit, variation of frequency can only be obtained by change in capacitance in this form of circuit. A variable capacitor may be used only if its minimum capacitance is relatively large compared to the input capacitance of the amplifier. This condition can be met with an emitter-follower input stage using a high-frequency transistor.

The extremely high transadmittance available with transistors makes possible the use of very small values of R . The associated amplifier should be designed to have a transadmittance that is degenerated to a value slightly greater than $3/R$ with the resistance selected for the network, and a small range of adjustment should be provided to permit the compensation for small errors in parts values.

Two possible circuits for generating a stabilized forward admittance of the required value are shown in Fig. 11-13. The circuit (A) obtains stabilization through the comparison of two signal currents in transistors 1 and 2, whereas the circuit (B) obtains the stabilization through the comparison of two signal voltages and amplification of the difference in the difference amplifier. The first of the circuits is somewhat simpler, but has a smaller stability than the latter because its efficiency is dependent on the stability of the forward admittance of the individual transistors. However, because the stability and reproducibility of the forward admittance of transistors is rather good as long as the collector currents in the two transistors are equal, the balance may be expected to be good, possibly within 5%. The relations applying to Fig. 11-13(A) are

$$G_f = \frac{3[g_{f1}/(1 + (g_{i1} + g_{r1})R_e)]g_{f3}R_L/}{[3(1 + (g_{i2} + g_{r2})R) + (g_{f2}/(1 + (g_{i2} + g_{r2})R_e))]g_{f3}R_L]} \quad (11-28)$$

When $g_{f2}R_e \ll g_{f2}R_L$ and $g_{f3}R \gg 1$, this reduces to

$$G_f \cong 3/R - 3\Delta g_f^2/(g_{f1}^2 R) \quad (11-29)$$

where $g_{f1}R_e \geq 10$ and $g - g_{f1} = \Delta g_f$. The transistor T_3 is used as an emitter-follower to make it possible to take full advantage of the available gain in the balance amplifiers. Otherwise, the value of R_L will not be sufficiently large compared to R_e to make Eq. 11-29 applicable.

The second circuit, which makes the comparison at the input through the use of an input emitter-follower and balance circuit, applies the difference voltage to the amplifier, and can consequently make full use of the amplification available in it. The emitter-followers used in the input comparison circuit have high inherent stability at signal frequency, a fraction of a percent or better.

The larger the undegenerated gain of the amplifier can be made, the smaller is the variation in overall amplification. Circuits like those shown can be redesigned to provide Q multiplication for tuned circuits, and the effective Q available may be adjusted through the use of gain-adjustment circuits.

Automatic amplitude stabilization may be introduced into either of these amplifiers to provide self-limitation. In the first circuit, this is accomplished by decreasing the feedback voltage, and by placing either a negative-coefficient thermistor in the emitter of T_2 or a positive-coefficient device in the emitter of T_1 . Either

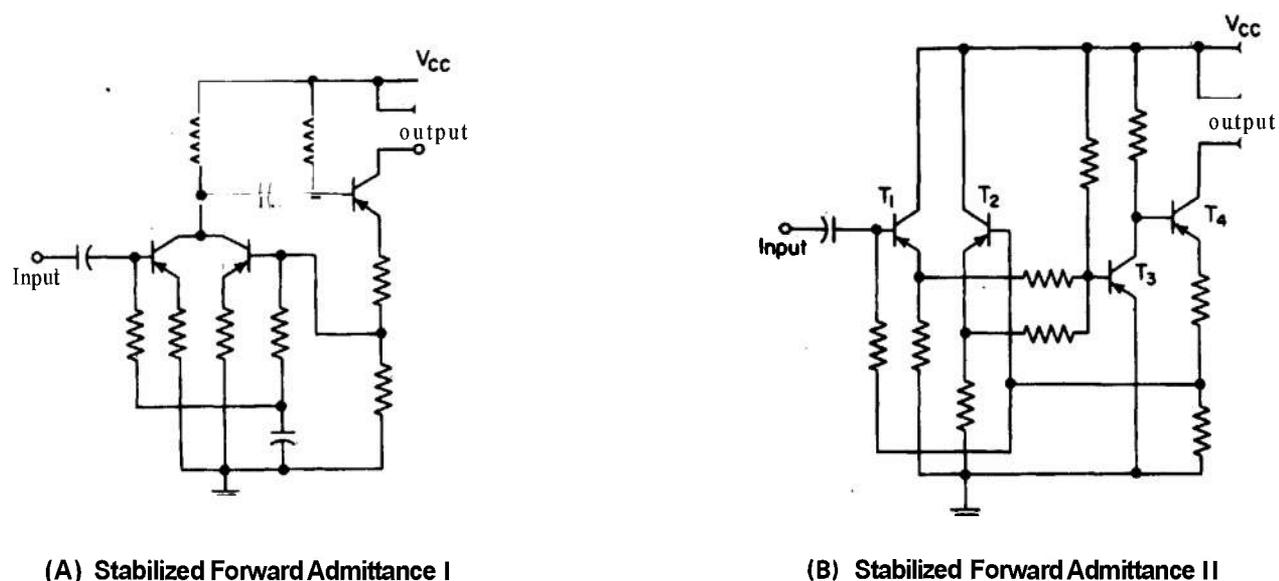


Fig. 11-13. Stabilized Forward Admittance Circuits

of these will disturb the balance in a manner to readjust the value of G_f as is required.

Amplitude stabilization may be introduced into the second amplifier in the balancing circuit through the use of a thermistor in the appropriate coupling circuit. Because it is possible to operate this balance circuit with no DC in it, the sensitivity to signal level can be made considerably greater than is possible in designs in which the thermal element must pass both signal and static current. The principal problem in this circuit is the control of phase-shift, because phase delay is introduced as a result of capacitive loading on the balance detection terminal. The range of operating frequency of this circuit is limited by the effect of this phase-shift.

The role of the direct and the feedback paths in an oscillator may be interchanged successfully. An oscillator using a Wien-bridge in such a modification is shown in Fig. 11-14. The direct-feedback path in this circuit is through the voltage divider into the emitter of the amplifier transistor, whereas the frequency-selection path, by letting a cancelling component of voltage reach the base of the amplifier at all but the oscillation frequency, limits action to the desired frequency range. This configuration has the advantage that the two parts of the bridge are normally placed at the point of lowest impedance in the circuit, and the amplification is not limited by loading to the extent it might be otherwise.

With all sinusoidal oscillators, whether of energy-

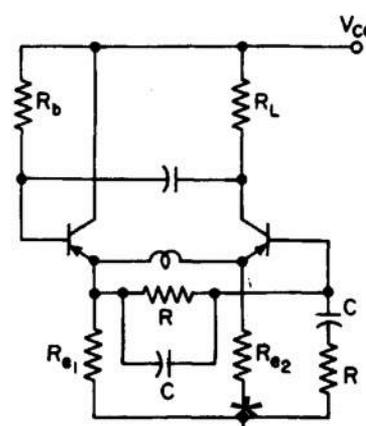


Fig. 11-14. Emitter-coupled Oscillator

storage or of phase-shift type, the design procedure is based on analysis of the feedback network as a trans-impedance, and then coordination of the driving-point impedance characteristics of the network with its trans-impedance and with the transadmittance of the active device(s) in the associated circuit. Determination of limiting conditions is based on the **known** nonlinear characteristics of the active devices. If available, the small-signal data are used for determination of the limiting conditions, or they may be approximated by a technique like the polynomial technique.

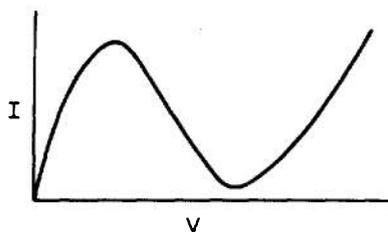


Fig. 11-15. Negative Admittance

11-4 NEGATIVE IMMITTANCE DEVICES

The special amplifiers described for development of a fixed magnitude of gain in connection with the R - C oscillators above are special examples of what may be called negative immittance amplifiers. These amplifiers are used to supply the losses in a given circuit, thereby either increasing its efficiency or possibly increasing the selectivity of a circuit by providing part of the energy required by the circuit losses.

Just as there are two types of immittance, namely, impedance and admittance, there are two types of negative immittance, one of which is used to neutralize a shunt conductance in an associated circuit, and the other to neutralize a series resistance in an associated circuit. Except for the fact that negative immittance can only be developed over a narrow range, these two types would be indistinguishable. Typically, however, a negative admittance has characteristics similar to those shown in Fig. 11-15. Outside of a narrow range, the current flowing through the device increases relatively uniformly with increasing applied voltage, but within the critical range, an increase in voltage brings about a decrease of current. Devices and circuits having this property also have a shunt dynamic capacitance associated with them.

With negative impedance devices, outside the critical region the voltage across the device rises as the current through it rises, but within the critical range the voltage decreases with increase of current. These devices have a dynamic series inductance associated with them.

Negative immittance devices and negative immittance circuits may have either one or two ports (two or three terminals), the more usual ones having a single port. Among the exceptions, the Q -multiplier and the Clapp oscillator circuits are typical of negative admittance configurations having three terminals (Fig. 11-16). Most of the oscillators considered in Chapter 10 could have been analyzed as negative immittance circuits. The transfer, or two-port, approach has been

used in this handbook because it appears to simplify and clarify the dynamics of the circuits.

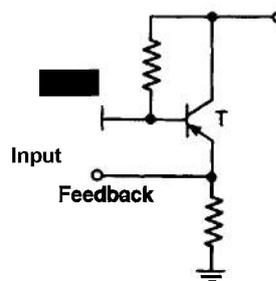
11-5 TIME DELAY OSCILLATORS

There is another type of oscillator that is of considerable interest, though so far it has been relatively little used. This form of oscillator uses an artificial delay line as its frequency-establishing element. Either the transmitted signal can be used to perform the switching action, or a reflected signal may be used. The simplest circuit of this type is shown in Fig. 11-17. It uses a multivibrator having a normal switching time somewhat longer than that desired from the overall circuit in conjunction with a delay line having somewhat dispersive characteristics. The delay in this line should increase with increasing frequency. The switching pulse from the emitter circuit is coupled into the delay line and used to initiate the reversal of the state of the multivibrator.

In spite of the bad waveform of this type of oscillator, its repetition rate is constant because of the relatively sharp rise in the output of the delay line allowing for but little variation in the switching instant. As long as the normal switching rate of the amplifier as a multivibrator is somewhat slower than the delay time in the delay line, operation will be at the minimum rate supportable by the line, and the frequency stability will be comparable with a good L - C oscillator.

The design of the active circuits for this application calls first for the design of a multivibrator having the appropriate repetition rate, and the insertion of a delay line to provide the required control action.

The delay line may be placed in other positions in the circuit as well as that shown in Fig. 11-17. It may be coupled from emitter to emitter; it may be inserted in any other position that will increase the total delay in the circuit by a fixed amount; or it may be arranged to

Fig. 11-16. Q -multiplication Circuit

provide a shunt-switching action as is generated by the circuit above. When the delay is placed in series with the main signal path, it is important that some reduction of high-frequency response be introduced to prevent the control from shifting from the fundamental rate to the second or a higher harmonic in a more-or-less random fashion. Some shunt capacitance across the amplifier load resistance can provide the required delay (Fig. 11-18).

11-6 SUMMARY

The design of oscillators is the science of the interconnection of linear selective networks and nonlinear networks to cause a conversion of energy from a DC

source into a cyclic energy. Each section of the complete network may be analyzed in a fashion that permits interconnection without need for matching adjustments. That is, the design of each section is analyzed on the basis of the conditions that will apply when the sections are interconnected. The driving-point impedances, both input and output, are required for the linear network to make the design for the nonlinear section, and the transfer impedance is also required for the determination of the conditions of unity average loop amplification. The use of these data with the small-signal data on the active devices permits the adjustment of the amplification to the value required for oscillation to develop, and permits the determination of the conditions required for a given amplitude of oscillation to develop.

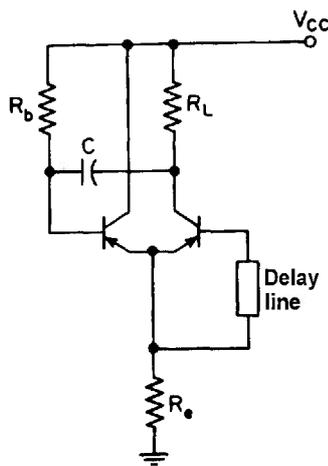


Fig. 11-17. Delay-line Oscillator I

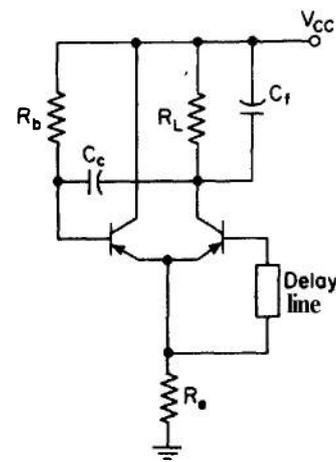


Fig. 11-18. Stabilized Delay-line Oscillator II

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1. D. E. Hooper and A. E. Jackets, "Current Derived Resistance-Capacitance Oscillators Using Junction Transistors", *Electronic Engineering*, August 1956, p. 333.
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CHAPTER 12

DESIGN OF MIXERS AND CONVERTERS

12-0 INTRODUCTION

Mixers and converters are used to shift the carrier frequency of a modulated wave without altering its modulation structure. A properly designed mixer or converter makes use of an unmodulated sinusoidal signal to vary the electrical characteristics of a nonlinear device in such a way that a second modulated signal, of considerably smaller amplitude, will experience a time variation of amplification. The modulation is thus transferred to a new carrier at the sum or the difference frequency, or one of their multiples. The mixer uses the nonlinear device solely for the multiplication action required to achieve the transfer, whereas the converter uses a single tube or transistor for both the oscillation and the multiplication functions.

12-1 CONVERSION CONDUCTANCE

The value of conversion conductance or conversion gain developed by a circuit depends on the characteristics of the associated nonlinear device and also on the type of circuit with which the device is used. It also depends to a considerable extent on the manner of application, inasmuch as the amount of nonlinearity in the device may either be minimized or enhanced by fairly small variations in the circuit parameters. The next few paragraphs explain the determination of the conversion characteristics of several typical nonlinear behavior patterns, and following this discussion, some of the possible methods of taking maximum advantage of the conversion properties of practical devices are studied.

The simplest converter relation to analyze mathematically is the one in which the conversion conductance or the conversion gain is a linear function of the voltage from the reference oscillator. In this case, the gain relation may be written

$$K = K_0 + K_1x \quad (12-1)$$

where $x = v_b/v_{\max} = \sin \omega_r t$ in the absence of input signal. The more correct form, including the signal, is

$$x = \sin \omega_r t + k_s \sin \omega_s t \quad (12-2)$$

where k_s is a function of time, and is the ratio of the amplitude of the desired signal and its accompanying noise to the amplitude of the reference signal, and ω_s and ω_r are the instantaneous angular frequencies of the composite signal and the reference voltages, respectively.

If Eq. 12-1 is integrated to give the output voltage in terms of the input ratio x , the result is

$$v_0 = V_a[K_0x + 0.5 K_1V_a x^2] \quad (12-3)$$

Next, the expression for x should be substituted, giving

$$v_0 = V_a K_0 x + 0.5 K_1 V_a^2 [\sin^2 \omega_r t + 2 \sin \omega_r t \times k_s \sin \omega_s t + k_s^2 \sin^2 \omega_s t] \quad (12-4)$$

For mixer applications, the only term of importance is the sine-product term, consequently, the balance may be discarded

$$v_{0c} = 0.5 K_1 V_a^2 k_s [\cos (\omega_r - \omega_s)t - \cos (\omega_r + \omega_s)t] \quad (12-5)$$

It is more convenient to express the value of K_1 in terms of the greatest and the smallest values, K_p and K_n , than in terms of the derivative. Then $K_1 V_a$ takes the form

$$K_1 V_a = 0.5 (K_p - K_n) \quad (12-6)$$

Substituting, and recalling that the input signal voltage is $V_a k_s$, gives

$$v_{oc}/v_{is} = 0.25 (K_p - K_n) [\cos (\omega_r - \omega_s)t - \cos (\omega_r + \omega_s)t] \quad (12-7)$$

This equation shows that because v_b is the amplitude of the signal voltage, the output will be available at the radian frequencies $(\omega_r - \omega_s)$ and $(\omega_r + \omega_s)$. Normally, all that is required to select the appropriate frequency is to introduce a frequency-selective circuit that develops sufficient impedance at the specified frequency to facilitate the transfer of energy to the following circuitry.

Although the development of mixing through linear variation of amplification (sometimes mis-called linear mixing) is probably the simplest way of obtaining moderate efficiency, it is by no means the only possible method of mixing, nor is it necessarily the best method of mixing. For example, it is only approximately half as efficient as the piecewise-linear mixer, which develops two fixed values of amplification over two ranges of bias

$$\begin{aligned} K &= K_n; & v_i < 0 \\ K &= K_p; & v_i > 0 \end{aligned} \quad (12-8)$$

This input relation gives a conversion efficiency of $K_c = 0.4244$, or a detection efficiency of 0.2122, rather than the 0.250 or **0.125**, respectively, for the square-law mixer or detector. The value of the conversion amplification can be up to twice the above values if diode-clamp mixing is used, and it may be up to three times the listed value if both diode clamping and peak (rather than average) mixing is produced. Table 12-1 indicates the range of conversion efficiencies that may be anticipated. Quadratic mixing is normally produced by transistors and tunnel diodes, and piecewise-linear by diodes under conditions of relatively large reference-voltage input.

12-2 TRANSISTOR MIXERS

The basic requirement for mixer action with transistors is principally that the circuit must behave in a manner that will provide a varying amplification as a function of reference voltage, but a negligible variation

as a function of the received signal. First, it is necessary to determine the conditions under which sufficient variation of amplification can be obtained to give effective mixing action. The amplification equation is

$$K = -y_f R_L / [1 + y_e (r_b + R_s) + y_c R_L + y_o R_L] \quad (12-9)$$

where $y_f = g_f + j\omega C_f$, and the terms in $y_o R_L$ and $y_c R_L$ may be neglected. Eq. 12-9 then reads

$$K = -y_f R_L / [1 + (g_e + j\omega C_e)(r_b + R_s)] \quad (12-10)$$

In this equation, three of the parameters are proportional to the emitter current in the transistor, namely, y_f , g_e , and C_e . Consequently, for effective mixing, the second term of the denominator,

$$(g_e + j\omega C_e)(r_b + R_s)$$

must be less than or at most equal to unity. When ωC_e is small compared to g_e at the frequency chosen for use on the mixer or converter transistor, then the product $g_e (r_b + R_s)$ controls whether proper mixing can be obtained. If, however, the operating frequency is such that ωC_e is greater than g_e , then the product $\omega C_e (r_b + R_s)$ will control the operating behavior.

The two equations expressing the limitation on effective mixing indicate that two conditions must be fulfilled. The first of these is that the internal or source resistance of the source of input signal should be small, and the second is that the base-spreading resistance of the transistor also should be small. Only under conditions in which both of these factors are sufficiently small that the product terms are less than or approximately equal to unity will effective mixing be possible. These conditions may be stated as

$$\begin{aligned} g_e (r_b + R_s) &\leq 1 & \text{or} & & g_e (2r_b) &\leq 1 \\ \omega C_e (r_b + R_s) &\leq 1 & \text{or} & & \omega C_e (2r_b) &\leq 1 \end{aligned} \quad (12-11)$$

TABLE 12-1
CONVERSION AMPLIFICATION

Type of Mixing	Type of Output	Conversion Gain
Quadratic: $K = K_o + K_1 v_r$	Average	$0.25(K_p - K_n)$
Piecewise linear: $K = K_p$ when $v_r \geq 0$ $K = K_n$ when $v_r < 0$	Average Peak	$0.42(K_p - K_n)$ $0.5(K_p - K_n)$

If, then, the maximum value of R_s is set equal to r_b' , as indicated by the second equation of each group, the maximum operating current may be set in terms of the appropriate inequalities

$$C_i \leq 1/(2\omega r_b') \text{ or } g_{i'} \leq 1/(2r_b') \quad (12-12)$$

These two equations may be solved in terms of the nomograph, Fig. 12-1. The maximum forward conductance and the maximum emitter current may be read directly from the nomograph based on the assumption that the diffusion capacitance is approximately the total input capacitance of the transistor.

These nomographs can be used to determine the maximum forward conductance that can be obtained efficiently in a transistor circuit. The required reference signal power for the mixer of Fig. 12-2 can be determined by reading the total peak-to-peak base voltage change Δv_b and the total peak-to-peak emitter current change Δi_e . The input power then is

$$P_r = 0.125 \Delta v_b \Delta i_e = 0.125 \Delta v_b (\Delta i_b + \Delta i_c) \quad (12-13)$$

This amount of power must be made available to the emitter lead in the mixer if maximum mixing efficiency and the best possible noise figure are to result. The maximum conversion amplification is given by the equation

$$K_c = 0.25 (Y_{fp} - Y_{fn}) R_{LD} \quad (12-14)$$

where R_{LD} is the impedance at the output frequency, and Y_{fp} and Y_{fn} are the effective values of forward admittance. In this equation, one of the Y_f terms is the value at maximum current, and the other at minimum.

Which is which depends on the polarity of the transistor.

The amplification of the mixer as a function of the bias voltage may be expressed in terms of an algebraic relation for the effect of source impedance

$$K = k_0(1 + x)/(1 + m + mx) \quad (12-15)$$

where the range for x is from -1 to $+1$, $k_0 = 0.5 g_{fmax} R_L$, $m = g_{imax} Z_s/2$, and $1 + 2m$ is the maximum value of the denominator as established in terms of y_i' , ω , C_i , and r_b' . The conversion amplification is expressed in terms of this equation, where $(K_p - K_n) = 2K_i$ is the total change of amplification with a negligible value of the parameter m . As long as the value of m is less than 0.5, the conversion conductance can be expressed in terms of the equation

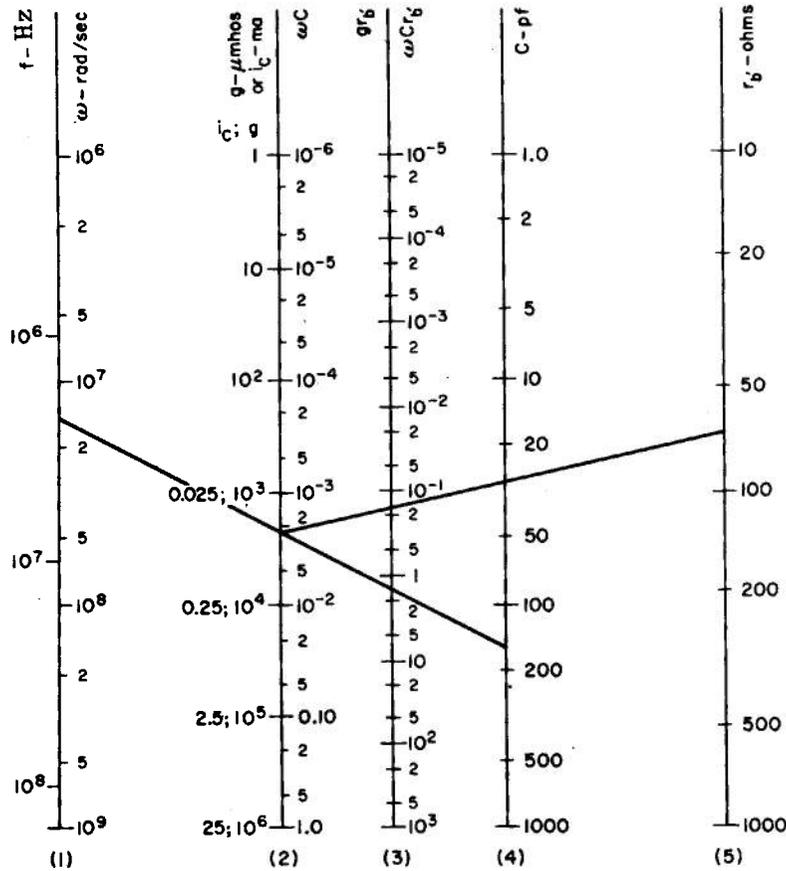
$$K_c = \frac{0.25(K_p - K_n)}{(1 + m)^2} (1 + [3m^2/5(1 + m)^2] + [3m^2/7(1 + m)^4] + \dots) \quad (12-16)$$

This expression reduces to the normal function for $m = 0$, and the ratio of the bracket $\langle \rangle$ expression divided by $(1 + m)^2$ can be approximated by the expression

$$K_c = 0.25(1 + 0.6 m^2)/(1 + m)^2 \quad (12-16a)$$

Consequently, the equation shows that the effect of the denominator term is to reduce the conversion amplification.

The mixer transistor may be used as its own oscillator, but the amount of conversion conductance that can be obtained under these conditions, as oscillator stabil-



Note: if value of g on line 2 is forward conductance, g_f , then current scale may be used, not otherwise

Fig. 12-1. Calculation Nomograph

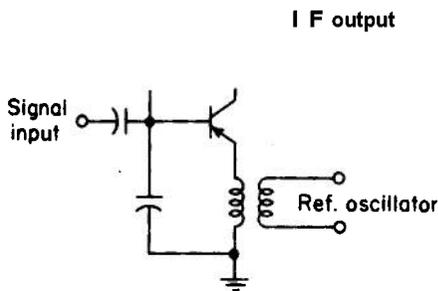


Fig. 12-2. Transistor Mixer.

ity is important, is quite small. The reason for this condition is that good frequency stability requires the changes in amplification to be small over the operating

cycle, whereas effective conversion action requires as large a change as possible. In addition, the larger the conversion amplification obtained for a given maximum forward conductance, the higher the overall signal-to-noise ratio. This condition is typical of mixers, in that the noise is primarily noise generated in the IF passband, whereas the magnitude of the converted signal under linear conversion conditions is proportional to the total change of forward conductance.

EXAMPLE 12-1. Design a mixer for operation at 5 MHz, using a 2N247 transistor in the configuration of Fig. 12-2. Take the collector supply voltage as 10 V, the value of r_b as 40 ohms, and the value of R_c may be left to be determined. The a-cutoff frequency for the 2N247 transistor is 30 MHz.

First, the effective input capacitance corresponding to the a-cutoff frequency may be calculated. Assuming a maximum current of 1 mA, the approximate forward conductance is 0.04 mho, and the capacitance is

$$C_i = g_{f'} / \omega = 0.04 / (2 \times 10^8) \\ = 2 \times 10^{-10} = 200 \text{ pF}$$

At a frequency of 5 MHz, this capacitance has a time constant with $r_{b'}$ of

$$C_i r_{b'} = 7 \times 2 \times 10^{-10} \times 40 = 8 \text{ nsec}$$

The resulting value of m is 0.120 for a linear mixing circuit. If the source impedance of the signal circuit is kept sufficiently small, less than 100 ohms, for example, the behavior of the circuit should prove satisfactory.

The effect of $g_{f'}$ may also be checked, as a matter of routine. The product of $r_{b'}$ and $g_{f'}$ is given by the equation

$$g_{f'} r_{b'} = 0.0008 \times 40 = 0.032$$

Consequently, the capacitance component is the one of importance in the limitation of the conversion amplification.

The magnitude of input signal from the reference oscillator to give full modulation of the transistor may be calculated. The required power is

$$P = 0.125 \Delta v_b \Delta i_e = 0.125 \times 0.130 \times 0.001 \\ = 0.15 \text{ mW}$$

This amount of mixer power makes available up to 10,000 pmhos of conversion conductance. For a conversion gain of 30, the load impedance of the converter load is only a few ohms at the reference frequency.

The balance of the static design can now be completed. The average base current should produce a collector current of approximately 0.5 mA, and the collector current then varies from about 0.1 mA to a peak of 1 mA. The approximate value of base current required is 8 μ A.

The input circuit for the signal still must be designed. The average input conductance is approximately 400 pmhos, and the average input capacitance is approximately 100 pF. Unless variable capacitance mixing is

desired, it is necessary to minimize the effect of capacitance variation on the tuning of the input circuit. The nominal reactance level of 100 pF at 5 MHz is 200 ohms, a value much higher than can be tolerated in the circuit. It is necessary to reduce this reactance to a value which when resonated develops an effective source impedance less than 40 ohms at the base if the conversion gain is not to be degraded significantly. Consequently, for a source reactance of 1 ohm at the base, the Q-factor circuit must not exceed 40 if R_s is to be 40 ohms or less. A parallel capacitance of approximately 0.02 mF in parallel with the base is required. Assuming a loaded Q of 40, and a nominal drive impedance for the tuned circuit of 1000 ohms, a capacitance step-down ratio of 5 is required if the unloaded Q of the tuned circuit is sufficiently large that the load current drawn by the base is small compared to the circulating or reactive current in the tuned circuit.

The fact that the nominal impedance level for the reference oscillator signal is 130 ohms does not necessarily mean that the source impedance to the emitter should be this high; Practically, it is desirable to keep the source impedance sufficiently small that the product $g_{f'} Z_s$ has a value considerably less than unity, particularly at signal and output frequencies. Because the average value of $g_{f'}$ is 0.02 mho, the value of Z_s should be less than 30 ohms.

12-3 DIODE MIXERS

The diode mixer is used under conditions in which transistors cannot be made to function satisfactorily. The diode has a series resistance component and a shunt capacitance component across the junction just as does a transistor, but the shunt capacitance may be only a hundredth of the diffusion capacitance of the transistor, and the series impedance may also be smaller by a factor of from 2 to 10. This combination of conditions makes the diode at least potentially able to operate as a mixer to a frequency 100 to 1,000 times as high as the transistor. The reference oscillator voltage required by the diode is from 10 to 20 times that required of the transistor.

Diode mixing is generated by the use of the diode under piecewise-linear conditions developed on a large-

signal basis. In effect, the diode acts as a switch, either turning the circuit on or turning it off. This switching, although it takes place in a range of 0.1 or 0.2 V, is not sufficiently sharp that the characteristics are strictly piecewise-linear with less than 2 to 3 V of reference signal voltage.

The conversion amplification for the diode mixer is limited by the fact that in the forward direction the amplification is unity, and in the reverse direction, it is very nearly zero. For this reason, its value is appreciably less than unity, a maximum of 0.424 for the most commonly used circuit configurations. In spite of this, a diode can be convenient because a higher overall amplification often can be obtained by the use of a diode under piecewise-linear conditions and following it by a transistor amplifier operating at the output frequency.

12-4 DIODE MEASUREMENTS

One of the problems in the use of diode mixers is the selection of devices capable of giving effective mixer action. The principal property of a diode that affects mixer action is its switch-off time. When any semiconductor diode is switched very rapidly from the forward to the reverse polarity, the diode current has a form similar to that shown in Fig. 12-3. The current in region A would not exist except for the time required to sweep out charge carriers.

Diodes may be tested for the effect of the reverse-conduction loading shown in region A by the use of the circuit in Fig. 12-4 in conjunction with a conventional Q-meter. When this loading is present, if a diode with either no bias or reverse bias is coupled across a tuned circuit, a significant loss of Q-factor circuit can result. With a diode having small loss, the Q-reduction is normally very small.

12-5 DIODE AMPLIFIERS

Diodes can be used successfully as amplifiers if their characteristics include very small equivalent series resistance and a reasonably large capacitance change as

a function of reverse bias voltage. Such amplifiers are known as parametric amplifiers. They take advantage of the fact that a variable capacitance can affect the tuning of a circuit. If the capacitance is controlled by a voltage of relatively high frequency and large amplitude, then the amplification of a low-frequency signal can be achieved.

The properties required of diodes for this application, aside from those of stable characteristics, are a large rate of variation of capacitance with injection voltage, and a relatively large value of positive bias for the initiation of the conducting region. In addition, the

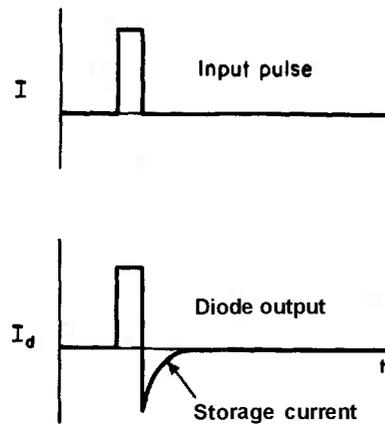


Fig. 12-3. Diode Storage

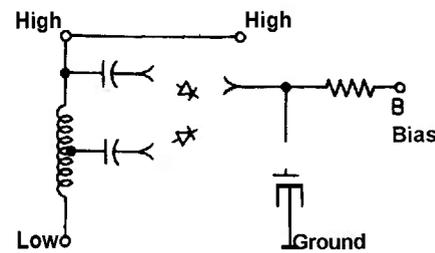


Fig. 124. Diode Test Circuit Using "Q-meter"

total voltage swing in the reverse direction to the Zener, or avalanche-breakdown voltage should be large.

Suitable diodes for use in amplifier service may be found using the tester described in par. 12-4. The potentiometer varies the back-bias, and makes possible the measurement of effective capacitance as a function of the diode current. Diodes having a large capacitance variation, but introducing only small reductions of circuit Q-factor are essential for this application.

Either stable amplification or potentially unstable amplification may be obtained from variable-reactance diode circuits. If the reference injection frequency ω_r is large compared to the signal frequency ω_s , two possible output frequencies normally are obtained from the variable-reactance amplifier, namely, $\omega_r + \omega_s$ and $\omega_r - \omega_s$. It is possible to obtain output at the frequency ω_s also if the proper operating configuration is selected. The limit on the amplification available at the frequency $(\omega_r + \omega_s)$ is sufficiently small that it seldom can be used, and the relatively more unstable operation at the lower frequency $(\omega_r - \omega_s)$ is usually used for developing a larger amplification.

The equation for amplification in the parametric amplifier may be derived either in terms of the active circuit including the parametric diode, or it may be derived in terms of the complete circuit, including input and output coupling. For the initial discussion, the simplified equation is the best to use, because the mutual coupling impedances play no significant part in the behavior of the circuit. The basic circuit, the current and voltage graphs, and the incidence matrices for the simplified parametric amplifier circuit are shown in Fig. 12-5. The trees (this derivation is being made topologically) are

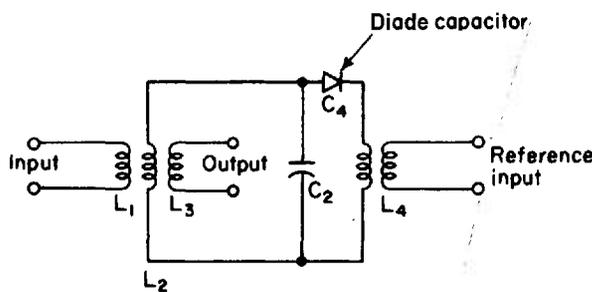


Fig. 12-5. Parametric Amplifier

y trees

$$yY_{L1}Y_{C2}, yY_{C1}Y_{C2}, yY_{L1}Y_{L2}, yY_{C1}Y_{L2}, yY_{L2}Y_{C2}$$

Other trees

$$Y_{L1}Y_{L2}Y_{C2}$$

From these trees, the transfer admittance and the voltage amplification for the network at fundamental frequency may be determined. After multiplication of both sets of trees by $Z_{L1}Z_{L2}$, the voltage gain is

$$K_v = 1/[(1 + Z_{L1}Y_{C1})(1 + Z_{L2}Y_{C2}) + Z_{L1}Y_{C2}] \tag{12-17}$$

When this is simplified by the substitutions

$$\begin{aligned} Z_{L1} &= R_1 + j\omega L_1, & Z_{L2} &= R_2 + j\omega L_2 \\ Y_1 &= j\omega C_1, & Y_2 &= j\omega C_2 \end{aligned} \tag{12-18}$$

and the further simplifications made that

$$\begin{aligned} \omega_s^2 &= 1/\langle L_1(C_1 + C_2) \rangle, & \omega_s^2 L_2 C_2 &\ll 1, \\ & & \text{and } \omega_s R_2 C_2 &< 1 \end{aligned}$$

the voltage gain is, at the angular frequency, ω_s ,

$$v_s = v_i / \langle j\omega_s R_1(C_1 + C_2) \rangle = -jQ_s v_i \tag{12-19}$$

In a similar manner, the transfer gain for the reference frequency may be determined in terms of the trees of the reference-frequency network. The trees are

y_r trees

$$y_r Y_{L1} Y_{L2}, y_r Y_{L1} Y_{C2}, y_r Y_{L2} Y_{C1}, y_r Y_{C1} Y_{C2}, y_r Y_{L1} Y_{C2}$$

Other trees

$$Y_{L2} Y_{C1} Y_{C2}, Y_{L1} Y_{L2} Y_{C1}$$

Making the same simplification as before, the equation for voltage gain takes the form

$$K_{vr} = (1 + Z_{L1}Y_{C1})/[(1 + Z_{L1}Y_{C1})(1 + Z_{L2}Y_{C2}) + Z_{L1}Y_{C2}] \tag{12-20}$$

As in the previous case, this is the reference voltage developed across the capacitor C_2 , which is varied by the applied voltage. If the two equations for voltage gain are solved for the output voltage across C_2 in terms of the input voltages v_i and v_r , the sum of the two gives the total voltage generating intermixing across the variable capacitor. To determine the current or the voltage amplification that may be generated in the circuit, therefore, it is necessary to determine the ratio of the signal-frequency voltage generated with the reference-frequency signal applied, to that with the reference signal absent. The signal-frequency current may be determined from Eq. 12-19

$$\begin{aligned} i_{c2s} &= C_2 v_i / \langle R_1 (C_1 + C_2) \rangle \\ &= \omega_s C_{20} Q_s V_i \sin \omega_s t \end{aligned} \quad (12-21)$$

For this equation, the value of C_2 may be taken to be constant, or it may be expressed in terms of the constant part of the total capacitance

$$\begin{aligned} C_2 &= C_{20} + C_{21}x, \quad -1 \leq x \leq +1 \\ x &= v_i / V_{c2r} \end{aligned} \quad (12-22)$$

(For a linear variation of capacitance, C_{21} is half the total change in value.)

The total change in C_2 is controlled by the magnitude of reference signal applied to the capacitor. The total instantaneous voltage across it is

$$\begin{aligned} v_i &= (v_{c2r} + v_{c2s} + v_{c2rs}) \\ v_i &= -jQ_s V_i \sin \omega_s t + V_{c2rs} \sin \omega_{rs} t \\ &\quad + (1 + Z_{L1} Y_{C1}) \times V_r \sin \omega_r t / [(1 + Z_{L1} Y_{C1}) \\ &\quad (1 + Z_{L2} Y_{C2}) + Z_{L1} Y_{C2}] \end{aligned} \quad (12-23)$$

Because C_{21} is the average rate of change, the ratio of v_i / V_{c2r} must be used, where the value of V_{c2r} is given by the equation

$$\begin{aligned} V_{c2r} &= V_r (1 + Z_{L1} Y_{C1}) / [(1 + Z_{L1} Y_{C1}) \\ &\quad (1 + Z_{L2} Y_{C2}) + Z_{L1} Y_{C2}] \\ &= V_r / [1 + Y_{C2} (Z_{L2} + Z_{L1} / (1 + Z_{L1} Y_{C1}))] \end{aligned} \quad (12-24)$$

The mixing action that occurs in the reactance diode can either produce a voltage or a current modulation.

Because resonant build-up is required in this circuit to develop the amplification, voltage injection at the idler frequency $\omega_r - \omega_s$ is necessary for correct operation of the circuit. Consequently, the voltage developed across the reactance diode at idler frequency should be determined. In terms of the signal and reference voltages, it is formed from Eq. 12-24 and the expression

$$\begin{aligned} v_{c2rs} &= C_{21} V_i \sin \omega_s t \sin \omega_r t / \\ &\quad \langle j\omega_s R_1 (C_1 + C_2)^2 \rangle \end{aligned} \quad (12-25)$$

where the constant component of C_2 , C_{20} , has been discarded in the expansion of $[1/(C_1 + C_2)]$ in power-series form. This expression may be converted to eliminate the j term in the denominator by performing the indicated integration of the sine $\omega_s t$ into a negative cosine term; the correct integration coefficient is already in the denominator. The equation then becomes

$$\begin{aligned} v_{c2rs} &= C_{21} V_i \cos \omega_s t \sin \omega_r t / \\ &\quad \langle \omega_s R_1 (C_1 + C_2)^2 \rangle \end{aligned} \quad (12-26)$$

Recognizing that

$$\begin{aligned} \sin \omega_r t \cos \omega_s t &= 0.5 [\sin (\omega_r + \omega_s) t \\ &\quad + \sin (\omega_r - \omega_s) t] \end{aligned}$$

the voltage introduced into the circuit at idler frequency becomes

$$\begin{aligned} v_{c2rs} &= -C_{21} V_i \sin (\omega_r - \omega_s) t Q_s / \\ &\quad \langle 2(C_1 + C_{20}) \rangle \end{aligned} \quad (12-27)$$

Now, at the idler frequency, $\omega_{rs} = (\omega_r - \omega_s)$, the circuit $L_2 C_2$ is tuned to resonance to maximize the idler current, which then is

$$\begin{aligned} i_{c2rs} &= V_{c2rs} / R_2 = -C_{21} V_i \sin \omega_{rs} t Q_s / \\ &\quad \langle 2(C_1 + C_2) R_2 \rangle \end{aligned} \quad (12-28)$$

This equation may be converted to the idler voltage across the capacitor by multiplication by $1/j\omega_{rs} C_2$, giving

$$v_{c2rs'} = Q_s Q_{rs} C_{21} V_i \cos \omega_{rs} t / \langle 2(C_1 + C_2) \rangle \quad (12-29)$$

Now, this voltage introduces a signal-frequency component at the nonlinear capacitor. The resulting signal voltage is

$$\begin{aligned} (C_1 + C_2)V_{c2} &= (C_{20} + C_{21}x)v_i \\ &= C_{20} + C_{21}(\sin \omega_r t + (V_{rs}/V_{c2r}) \\ &\quad \cos \omega_{rs} t)^2 V_{c2r} \end{aligned}$$

Taking the conversion terms only gives

$$\begin{aligned} (C_1 + C_{20})V_{c2} &= C_{21}(V_{c2r} \sin^2 \omega_r t \\ &\quad + V_{rs}^2 \sin \omega_r t \cos \omega_{rs} t \\ &\quad + V_{rs}^2 \cos \omega_{rs} t / V_{c2r}) \\ &\doteq C_{21} V_{rs} \sin \omega_s t = V_{c2s'} \\ &= C_{21} Q_s Q_{rs} V_i / \langle 2(C_1 + C_{20})^2 \rangle \end{aligned} \quad (12-30)$$

The resonant voltage across the capacitor is

$$V_{c2rs''} = C_{21}^2 Q_s^2 Q_{rs} v_i / \langle 2(C_1 + C_{20})^2 \rangle$$

and the gain is

$$V_{c2s''} / V_{c2s} = C_{21}^2 Q_s Q_{rs} / \langle 2(C_1 + C_{20})^2 \rangle \quad (12-31)$$

This is the approximate equation for the amplification of the parametric diode amplifier.

The proper behavior of this circuit requires that $C_1 > C_{20} > C_{21}$, with the result that the reference frequency is of necessity large compared to the signal frequency. Only then will the conditions assumed in the derivation prove valid. Based on these conditions, the amplification is a function of the circuit Q at the signal frequency and at the idler frequency also, and it de-

pends on the numerical ratio of the different capacitances of the circuit.

EXAMPLE 12-2. Design a parametric amplifier, assuming it is required to operate at 30 MHz, and that its idler frequency has been selected as 300 MHz. Design a possible circuit, assuming the static capacitance of the diode is 3 pF, and its change C_{21} is 2 pF.

The value of C_1 may be chosen as 25 pF, giving an inductance of 1.2 μ H for L_1 . Similarly, the value for L_2 is approximately 0.08 μ H. Selecting a value of Q_1 , of 200, and 300 for Q_{2rs} gives a potential current gain of approximately 750. Because the input and output coupling links can be expected to drop the net values of Q_1 , and Q_{2rs} to approximately 50 and 100, respectively, a maximum net gain of about 60 may be available at 30 MHz. The reference frequency is 330 MHz. The diode series resistance should be less than R_2 , a fraction of an ohm.

Noise Figure. The principal advantage of the parametric amplifier is its extremely small noise temperature, less than 100°K over the frequency range from approximately 10 MHz to greater than 2000 MHz. The parametric diodes currently available can be expected to function as amplifiers to frequencies of nearly 1000 MHz, and future diodes may be expected to function effectively to even higher frequencies.

12-6 COMPLETE EQUATIONS FOR PARAMETRIC AMPLIFIERS

The general equations for the straight-through parametric amplifier (Fig. 12-6), including inductive input and output coupling, can be established topologically by the technique described by Coates and Mayeda (Refs. 1, 2). Using the series configuration, the equation for amplification may be established in the fashion described in Appendix B. A total of 35 trees is required in the solution, 3 in the transfer terms, and the balance in the denominator. In terms of admittances, the forward admittance equation reads

$$\begin{aligned}
 Y_f = & -Y_s Y_L y_{11} y_{22} y_{33} y_{12} y_{23} [y_{c2} y_{c4} + y_{c2} y_4 + y_{c4} y_4] / \\
 & [-y_{11} y_{22} y_{33} (y_{23} y_{32} Y_s + y_{12} y_{21} Y_L) (y_{c2} y_{c4} \\
 & + y_{c2} y_4 + y_{c4} y_4) - y_{12} y_{21} y_{23} y_{32} (y_{c4} + y_4)] \\
 & + (y_{11} y_{33} y_{12} y_{21} y_{23} y_{32} - y_{11} y_{22} y_{23} y_{32} Y_s Y_L \\
 & + y_{12} y_{21} y_{23} y_{32} Y_s Y_L + y_{22} y_{33} y_{12} y_{21} Y_s Y_L) \\
 & (y_{c2} y_{c4} + y_{c2} y_4 + y_{c4} y_4) + (y_{22} y_{12} y_{21} y_{23} y_{32} Y_s Y_L \\
 & + y_{22} y_{12} y_{21} y_{23} y_{32} Y_s + y_{11} y_{22} y_{12} y_{21} y_{23} y_{32} Y_L) \\
 & (y_{c4} + y_4) + (y_{33} y_{12} y_{21} y_{23} y_{32} Y_s \\
 & + y_{11} y_{12} y_{21} y_{23} y_{32} Y_L) (y_{c2} y_{c4} + y_{c2} y_4 + y_{c4} y_4)]'
 \end{aligned}
 \tag{12-32}$$

This equation may be multiplied through by $z_{11} z_{22} z_{33} z_{12} z_{21} z_{23} z_{32}$, and then the numerator and denominator are both divided by the product

$$(y_{c2} y_{c4} + y_{c2} y_4 + y_{c4} y_4) (1 + z_{11} Y_s) (1 + z_{33} Y_L)$$

to give the equation

$$\begin{aligned}
 Y_f = & -[z_{21} / (1 + z_{11} Y_s)] [z_{32} / (1 + z_{33} Y_L)] Y_s Y_L / \\
 & [z_{22} + (y_{c4} + y_4) / (y_{c2} y_{c4} + y_{c2} y_4 + y_{c4} y_4)] \\
 & - [(z_{11} z_{23}^2 + z_{12} z_{33}) Y_s Y_L / (1 + z_{11} Y_s) \\
 & (1 + z_{33} Y_L) + z_{12}^2 Y_s + z_{23}^2 Y_L]
 \end{aligned}
 \tag{12-33}$$

In this equation, it is important to keep the negative term in the right-hand portion of the denominator relatively small so that the first two terms will control the amplification characteristics of the circuit. The second term actually introduces the required negative resistance and increases the amplification of the circuit. The way this action occurs is now considered.

The conversion of the second term requires transformation and substitution as follows

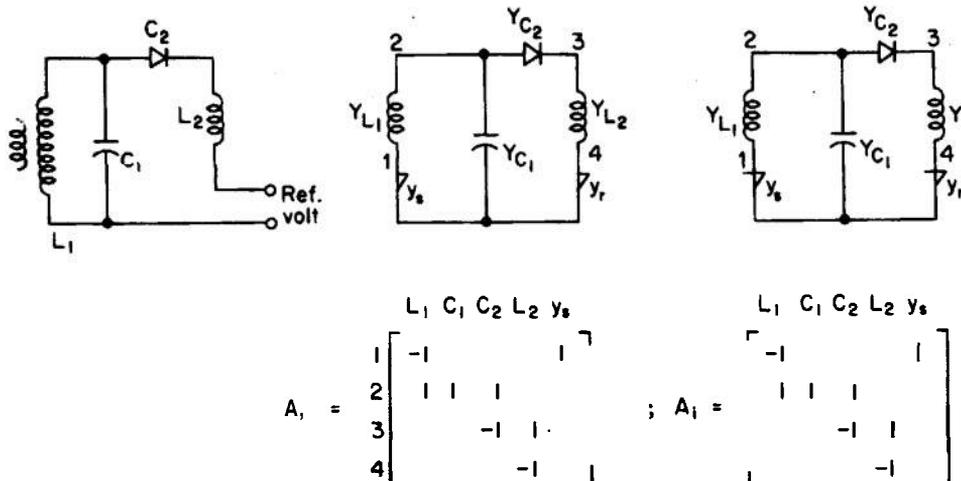


Fig. 12-6. Graphs of Simplified Parametric Amplifier

$$\begin{aligned}
 y_{c2} &= j\omega C_2, & y_{c4} &= j\omega(C_{40} + C_{41}x) \\
 z_4 &= 1/y_4 = R_4 + j\omega L_4 + r_d, & z_{22} &= R_2 + j\omega L_2
 \end{aligned}
 \tag{12-34}$$

where $x \doteq \sin \omega_s t$ and r_d is the damping introduced from the reference oscillator. Strictly, there is a component of frequency ω_s , the signal frequency, and $\omega_{rs} = (\omega_r - \omega_s)$, the idler frequency, also in x , but these terms may be neglected because their magnitudes are small in comparison with the pump frequency ω_p . Substituting gives

$$\begin{aligned}
 & z_{22} + (y_{c4} + y_4)/(y_{c2}y_{c4} + y_{c2}y_4 + y_{c4}y_4) \\
 &= R_2 + j\omega L_2 + \{[1 + j\omega(C_{40} + C_{41}x) \\
 & \quad (R_4 + r_d + j\omega L_4)] / [j\omega C_2(1 + j\omega(C_{40} + C_{41}x) \\
 & \quad (R_4 + r_d + j\omega L_4)) + j\omega C_4]\} \\
 &= (R_2 + j\omega L_2) + (1 + j\omega(C_{40} + C_{41}x) \\
 & \quad (R_4 + r_d + j\omega L_4)) / \{j\omega(C_2 + C_{40} + C_{41}x) \\
 & \quad [1 + j\omega(C_2(C_{40} + C_{41}x)/(C_2 + C_{40} + C_{41}x)) \\
 & \quad (R_4 + r_d + j\omega L_4)]\}
 \end{aligned}
 \tag{12-35}$$

Next it is necessary to expand the fraction in terms of the components that involve only C_{40} and those involving $C_{41}x$. When this is done, the equation takes the form

$$\begin{aligned}
 & R_2 + j\omega L_2 + (1 + j\omega C_{40}(R_4 + r_d + j\omega L_4)) / \\
 & \quad [j\omega(C_2 + C_{40}(1 + j\omega C_2 \times (R_4 + r_d + j\omega L_4)))] \\
 & \quad - j\omega C_{41}x / [j\omega(C_2 + C_{40}(1 + j\omega C_2 (R_4 + r_d \\
 & \quad + j\omega L_4)))]^2 = z_{22} + (y_{c4} + y_4) / \\
 & \quad (y_{c2}y_{c4} + y_{c2}y_4 + y_{c4}y_4)
 \end{aligned}
 \tag{12-36}$$

In this equation, the second and third terms cancel at signal frequency ω_s , leaving the resonant resistance of L_2 , and the value of the last, or conversion, term to be determined. Neglecting the remaining terms, and taking

$$Y_f = I_s \sin \omega_s t / v_s = f(y)$$

gives

$$\begin{aligned}
 v_s &= I_s \sin \omega_s t [R_2 - C_{41}x / \{j\omega[(C_2 + C_{40}) \\
 & \quad \times (1 + (j\omega C_2 C_{40}(R_4 + r_d + j\omega L_4) / \\
 & \quad (C_2 + C_{40}))]\}^2]
 \end{aligned}
 \tag{12-37}$$

where the coupling terms have been neglected. These terms determine the negative immittance of the circuit. Multiplying through by $\sin \omega_s t$ and substituting for x gives

$$V_{c2s} = I_s (R_2 \sin \omega_s t - (\sin \omega_s t \sin \omega_r t / D)) \tag{12-38}$$

where D is given by the equation

$$D = [j\omega((C_2 + C_{40})(1 + j\omega C_2 C_{40}(R_4 + r_d + j\omega L_4) / (C_2 + C_{40})))]^2 \tag{12-39}$$

Eq. 12-38 may be converted to a new form, remembering that $1/(j\omega)$ is indicative of an integration

$$\begin{aligned}
 v_{c2} &= I_s (R_2 \sin \omega_s t + C_{41} \cos \omega_s t \sin \omega_r t / \\
 & \quad [2\omega_s (C_2 + C_{40})^2 (1 + j\omega C_2 C_{40}(R_4 + r_d \\
 & \quad + j\omega L_4) / (C_2 + C_{40}))^2])
 \end{aligned}
 \tag{12-40}$$

Because

$$\begin{aligned}
 \sin \omega_r t \cos \omega_s t &= 0.5 [\sin(\omega_r - \omega_s)t \\
 & \quad + \sin(\omega_r + \omega_s)t]
 \end{aligned}$$

Eq. 12-40 may be rewritten as

$$\begin{aligned}
 v_{rs} &= v_s C_{41} \sin \omega_r t / [2\omega_s (C_2 + C_{40})^2 (1 + j\omega C_2 C_{40} \\
 & \quad (R_4 + r_d + j\omega L_4) / (C_2 + C_{40}))^2] R_2
 \end{aligned}
 \tag{12-41}$$

where the terms involving fundamental signal frequency have been neglected, and only the signal frequency has been inserted in the denominator ω terms. The value of ω , which belongs in the inner bracket of the denominator, is the idler angular frequency ω_{rs} . The

idler resonance condition may be introduced into the inner bracket, and it reduces to the form

$$j\omega_{rs}C_2C_{40}(R_4 + r_d)/(C_2 + C_{40})$$

giving the value of the idler voltage introduced into the idler circuit

$$v_{rs} = -v_s C_{41} \cos \omega_{rs} t / \langle 2\omega_s \omega_{rs} R_2 (C_2 + C_{40}) \times C_2 C_{40} R_4 \rangle \quad (12-42)$$

The Qvalues for the signal and the idler circuits may be introduced into this equation, since they are

$$Q_s = 1 / \langle \omega_s R_2 (C_2 + C_{40}) \rangle$$

$$Q_{rs} = (C_2 + C_{40}) / \langle \omega_{rs} C_2 C_{40} (R_4 + r_d) \rangle \quad (12-43)$$

Making the substitution gives

$$v_{rs} = -v_s C_{41} Q_s Q_{rs} \cos \omega_{rs} t / 2(C_2 + C_{40}) \quad (12-44)$$

Now, the total signal voltage across the variable capacitor is

$$v_t = V_s Q_s \cos \omega_s t + V_{rs} \cos \omega_{rs} t + V_{c4r} \sin \omega_r t$$

$$= -V_s Q_s [\cos \omega_s t + C_{41} Q_{rs} \cos \omega_{rs} t / \langle 2(C_2 + C_{40}) \rangle] + V_{c4r} \sin \omega_r t \quad (12-45)$$

This voltage may be applied to the nonlinear capacitor to give the resulting mixing components. Because a charge circulation at the sum and difference frequencies results from the capacitance variations, their excitation magnitudes may be determined in terms of the equation

$$(C_2 + C_{40})v_{c4} = (C_{40} + C_{41}x)v_t \quad (12-46)$$

Taking the nonlinear component gives the equation

$$(C_2 + C_{40})v_{c4} = C_{41}xv_t$$

Solving for v_{c4} and substituting for v_t gives

12-12

$$v_{c4} = C_{41}(\sin \omega_r t + \langle V_{rs} \cos \omega_{rs} t / V_{c4r} \rangle) V_{c4r} / (C_2 + C_{40})$$

$$= C_{41} V_{c4r} (\sin^2 \omega_r t + 2V_{rs} \sin \omega_r t \cos \omega_{rs} t / V_{c4r}) / (C_2 + C_{40}) \quad (12-47)$$

The resulting signal-frequency excitation voltage is

$$v_{c4s'} = C_{41} V_{rs} \sin \omega_s t / (C_2 + C_{40}) \quad (12-48)$$

$$= C_{41}^2 Q_s Q_{rs} v_i / \langle 2(C_2 + C_{40})^2 \rangle$$

The resonant current resulting from this excitation voltage is

$$i_{s'} = v_{c4s'} / R_2 = C_{41}^2 Q_s Q_{rs} / \langle 2(C_2 + C_{40})^2 R_2 \rangle \quad (12-49)$$

and the resonant voltage is

$$v_{c4s''} = C_{41}^2 Q_s^2 Q_{rs} / \langle 2(C_2 + C_{40})^2 \rangle \quad (12-50)$$

Finally, the approximate voltage gain is

$$v_{c4s''} / v_{c4s} = C_{41}^2 Q_s Q_{rs} / \langle 2(C_2 + C_{40})^2 \rangle \quad (12-51)$$

12-7 TUNNEL DIODE MIXERS

Tunnel diodes can be used as mixers at extremely high frequencies, and, at least potentially, can be more efficient than conventional diodes in the application. They normally function as square-law devices, but they have an extremely high rate of curvature, and consequently require a relatively small magnitude of reference voltage. Normally they are biased in the positive-conductance region near zero bias, and are biased just sufficiently positive to make certain that the range of swing for the reference voltage will be from zero voltage to the voltage corresponding to the maximum negative conductance for the device (Fig. 12-7, point A).

Relatively high conversion efficiency is available for these devices for two reasons, first because the conductance slope is higher than with conventional diodes, and second because of the increased change that results for a given peak value of conductance from the availability of both negative and positive values of conductance within a narrow voltage range.

Tunnel diodes can be used as modulators, and in functioning as modulators, can amplify an applied signal. In this application, the signal to be amplified is

used to shift the static operating point of the diode, which is biased in the region B in Fig. 12-7. This shift changes the average negative conductance of the diode, which is also coupled to a tuned circuit tuned to a higher frequency than signal requiring amplification. The result of the shift is a variation of the oscillation amplitude of the diode oscillator of considerably greater magnitude than that of the applied signal. Rectification of the resulting carrier produces an amplified replica of the input signal.

The tunnel diode when used in the modulator mode will provide some of its own rectification, and may contribute some instability to the circuit. In addition, the amplification produced is not necessarily linear because of the variation of the device properties with bias. In spite of these features, however, it appears that the modulator mode is possibly one of the better ways to use the tunnel diode as an amplifier.

12-8 PRODUCT DETECTORS

Product detectors are of growing importance partly because they are essential components of phase detectors, and partly because they provide a superior method of separating signal from noise. Product detectors are actually special mixers because they detect by comparing the received signal with a sinusoidal signal of specified frequency. The frequency is equal to that of the carrier for amplitude modulation, or displaced somewhat from that of the carrier for CW or code signals.

Phase detectors are made from a pair of modulators or product detectors so connected that one signal is applied to both channels, whereas the other is applied in push-pull (Fig. 12-8). The output of the two sections is so arranged that the net output voltage is a function of the phasor difference voltages developed in the two sections. With a phase angle of 90 deg between the two input signals, the output is zero with a properly balanced circuit, and it increases nearly linearly with phase angle for difference angles between 90 deg and 45

or 135 deg, and then less rapidly with further changes.

These detectors are particularly useful in that they can recognize the signal independent of its accompanying noise, and can control the operation of additional circuits with nearly complete independence of the noise. For example, a phase detector may be used to maintain a locally generated signal in almost exact quadrature with respect to the received signal, and an additional phase detector, having its reference signal maintained at an angle 90 deg out-of-phase with respect to the reference used in the main detector may be used to generate an AVC voltage that is almost completely immune to noise effects.

Diodes are normally selected for phase detectors, because balance in the active elements is of prime importance in these circuits. Transistors may be used for ordinary product detectors, however, because they give both excellent conversion and amplification when properly used. The design of product detectors using transistors follows the same pattern as is used for mixers. The problems encountered in the design of transistorized product detectors are greatly simplified compared to those encountered in the design of mixers because of the fact that often input capacitances and base-spreading resistance may be neglected in the design of low-frequency product detectors.

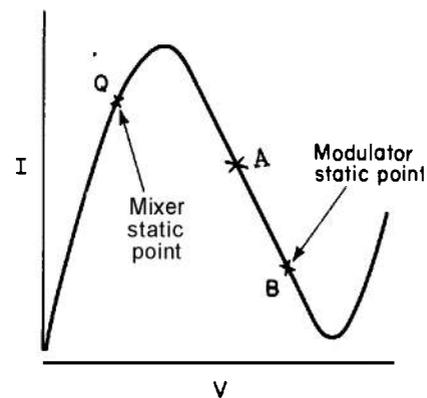


Fig. 12-7. Tunnel Diode Mixer and Modulator

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CHAPTER 13

TRANSISTOR MULTIVIBRATORS

13-0 INTRODUCTION

Multivibrators are oscillators having cycles in which instants of active instability are followed by periods of quiescence. The unstable condition is of the runaway nature, or is completely unstable in the mechanical sense. During the quiescent period, one or more active devices in the configuration are placed in an inactive condition through the shifting of the current and voltage on a control element, producing a condition of essentially zero amplification. An extremely large value of loop amplification may develop during the unstable period, causing nearly instantaneous switching of the circuit from one of the quiescent conditions to the other, or causing switching to a quasi-stable condition and then back to the quiescent condition.

The transistorized multivibrator is somewhat more complicated in behavior, and somewhat more complicated to design, than its vacuum-tube counterpart, primarily because of the effect of the series base-spreading resistance in the base lead of the device. The procedures already developed for design of tube multivibrators fortunately are applicable with minor modifications, however (Refs. 1, 2). A familiarity with the basic principles of design discussed in these references is assumed in the discussion to follow.

The high input conductance of the base circuit of transistors under conduction conditions introduces curvature into the load lines, and also reduces the available gain from the transistors to a point where achievement of satisfactory oscillation conditions can be relatively difficult. For this reason, the use of emitter-followers as coupling devices is extremely common with transistor multivibrators, and related switching circuits.

The amount of saturation current drawn by the base of the conducting transistor may be as much as 10 to 50% of the collector current, because the transistor is usually switched into a fully saturated condition. Unless the base circuit can pass the required current and the coupling capacitor can provide it momentarily, the switching of a transistor multivibrator can prove to be irregular and unreliable. The circuit of Fig. 13-1, in

which the base bias is obtained directly from the collector supply, may not switch satisfactorily, particularly if the supply voltage is large and the load resistors and the base-bias resistors are large in value. The difficulty usually can be avoided by dropping the value of the base-bias resistors and returning them to the collectors of the alternate transistors, as in the circuit in Fig. 13-2. When this is done, the series resistance required between collector and base is sufficiently small that positive switching can be achieved.

The procedure for design of a multivibrator is first to make designs that assure stable operation of the transistors in the two quiescent states, and then to make the design capable of active transition. It is at least possible in theory to make two static designs and then find that the transition cannot occur either spontaneously or under excitation. This being the case, a rather careful check of the active conditions during the switching cycle is required. Regenerative switching cannot commence unless the loop amplification of the circuit exceeds unity by a considerable margin for a period sufficient to give an average amplification of unity over the complete period.

Nominally, regenerative switching in the circuit under discussion starts at unity loop amplification, but it is necessary to maintain such a value of amplification

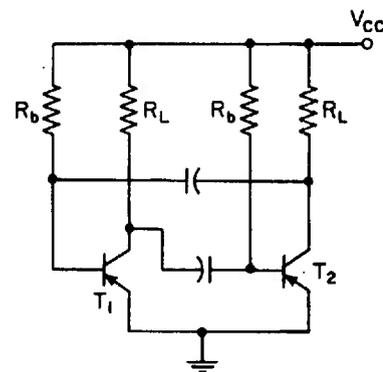


Fig. 13-1. Transistor Multivibrator

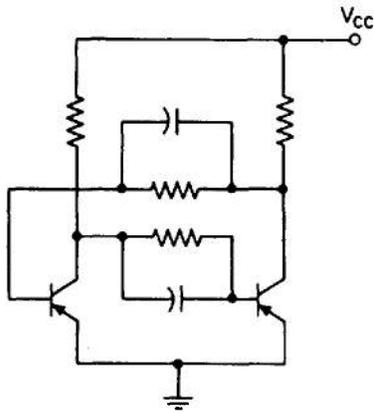


Fig. 13-2. Modified Transistor Multivibrator

or more throughout the balance of the switching cycle if the regeneration is to continue. The loading of the conducting transistor on the partially-conducting one can be sufficiently heavy to limit the loop amplification to a value that is either about unity or even less than unity, with the result that the amplification available in the transistors must build up more rapidly than with tube circuits if reliable switching is to result.

The achievement of a satisfactory cutoff operating condition is comparatively simple unless reverse-breakdown can develop at low voltage in the base circuit of the transistor. (This can happen with diffused-base transistors.) The cross-coupling capacitor, which helps to provide the cutoff bias, has but little load on it as a result of the input conductance of the nonconducting transistor, so that cutoff decay is quite slow in occurring, and the change of base voltage required for cutoff, less than approximately 0.150 V with respect to the emitter for small-signal transistors, is easily obtained.

The first step in design of the circuit to satisfy saturation conditions is to determine the minimum base current that can produce relatively heavy collector saturation. The average base current value initially may be selected to be half to three-fourths of this current. This initial value may require some readjustment when the effect of loading in the driven amplifier is considered. Fortunately, the amplifier driven by the saturated stage is biased to nonconducting conditions, and its input conductance is the leakage conductance of the base-to-emitter diode. For small-signal transistors, this conductance usually is less than 0.001 mho (over 1000 ohms). The load contours may take a form similar to that sketched in Fig. 13-3. Both a typical resistive load line and a possible form for the actual contour, somewhat exaggerated, are shown in this figure. The final average base current should be selected to be half of the average

current flow along the high-impedance section of the load line between saturation and the turning point, and the base-bias circuit should be designed to provide the required base current.

The load line for collector currents less than the turning-point value of necessity must be nearly parallel to the contour of constant voltage, because the total load reflected from the saturated transistor to the output circuit of its companion is little greater than the value of the base-spreading resistances for the devices. As a first approximation, it may be assumed that the saturation-load condition develops primarily below the nominal value of current at the Q-point, and the slope of the contour shifts quickly to be parallel with the reference load line for higher currents. For this reason, the contour may be approximated initially by two lines, one of slope r_b through the point $V_{CC}, 0$, and the second parallel to the reference load line through the selected collector saturation current and voltage. This approximate combination contour may be transferred to the input family, and the approximate small-signal data tabulated to permit the correction of the contour position.

The position of the critical turning points for the load contour is defined in terms of the product of the input conductance and load resistance. For this reason, it is important to note on both the input and the output contours the points at which the product $g_i R_L$ takes value such as 0.1, 0.2, 0.5, 1.0, 2.0, 5.0, 10, etc. These values determine the correction of the slope of the contour in terms of the equation

$$R_{LD} = R_L / (1 + g_i R_L) \quad (13-1)$$

In this equation, the g_i is the input conductance for the transistor whose input is in parallel with R_L , namely the coupled transistor.

Corresponding points in the operation of the pair of transistors may be located on the contour curves because the input curves may be identified with one transistor, and the output curves with the other. It is necessary to use the saturation conditions as the starting point because this condition behaves as the equalizing condition. The saturation conditions on the input curves correspond to a nonconducting condition on the coupled transistor, and may be identified with the zero-current section of the output curves. Similarly, the low-current region on the input curves corresponds to the saturation conditions on the output curves.

If a detailed analysis, including capacitive effects, is made of the operating cycle of the transistor multivibrator, it turns out that their behavior is more complex

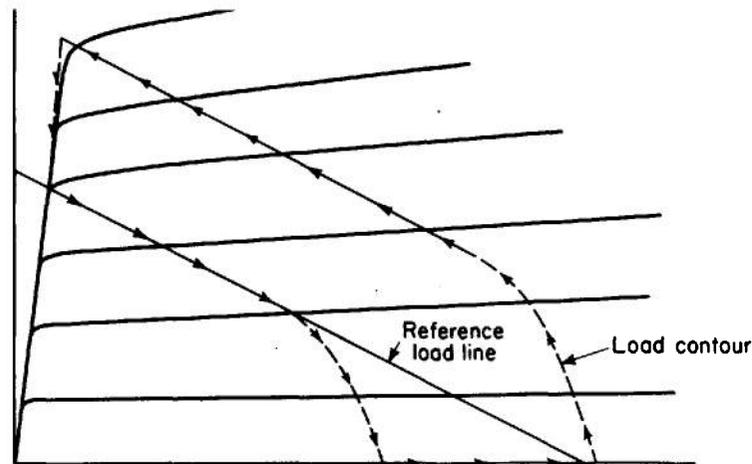


Fig. 13-3. Load Contour Path for Multivibrator

than appears to be the case from the previous discussion. The base current on the saturated transistor starts to decay along a modified exponential as soon as the associated transistor has been switched to the off-condition. The rise of the input resistance of the conducting transistor, along with the sharp rise in collector voltage on the companion transistor, initially minimizes the decrease of base voltage, and maintains the conducting transistor in the "on" condition. After a short period, however, the collector voltage rise terminates, permitting a shift of the operating point of the conducting transistor toward nonconduction. When the weakly-conducting transistor draws sufficient current to make the loop-gain of the circuit unity, switching starts, and the slope of the load line begins to change as described previously.

The curved load contours for switching in the two directions may not be identical because the entire action is modified by the action of the circuit capacitances and the internal variable capacitances of the devices as well. In addition, the switching to conduction on the input of the transistor is relatively more gradual with transistors than with tubes, particularly when compared to the width of the active amplification range for the device under comparatively low-current conditions. With transistors, the base voltage change required to shift operation from cutoff to the static operating point may be as small as 40 to 100 mV, and the range to carry the device into full saturation may be an additional 30 to 60 mV, whereas with a tube, the bias change over the active control area, with negligible grid current, may be several volts, and the additional saturation voltage may be a volt. The narrower range of active region with

transistors is a consequence of the twenty-times higher transfer efficiency available.

Because of the continuous drain of base current in the conducting transistor, the equations for the calculation of the switching period for a transistor multivibrator differ appreciably from the equations developed for tube-type circuits. Examination of a typical set of input characteristics for a transistor shows, however, that as the operating point leaves the saturation region, the base-to-emitter voltage changes very slowly at first and the input load contour is often nearly horizontal during the corresponding period. The significant break in the slope of the load line occurs simultaneously on the two sets of curves.

Because the total change in the base voltage over the active part of the cycle of one of the transistors is only 100 to 200 mV, and the total voltage change in the collector circuit may be as much as 10V, a considerable change of the collector voltage from the saturation value may occur before the transistor coupled to it can experience sufficient bias change to start it into the conduction region and bring about active switching. The typical waveforms to be expected in the conventional circuit are shown in Fig. 13-4.

EXAMPLE 13-1. Design a multivibrator using the type 5001 (Hughes) transistor, and assume a supply voltage of 7 V. Use a static load resistance of 1400 ohms, draw the corresponding load line, and try different static points as the basis for the design.

Fig. 13-5 shows the reference load line for this example. Base current values of 20, and 40 μA may be selected for the static design values, and the operating characteristics expected from each may be determined. The approximate base-spreading resistance for this

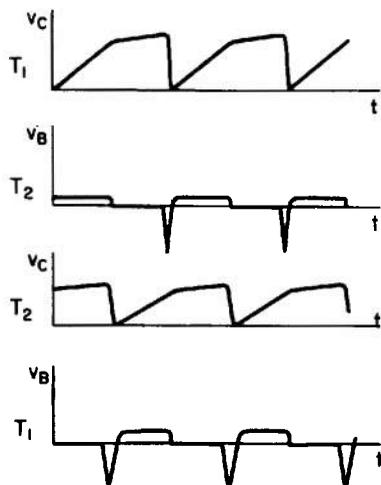


Fig. 13-4. Multivibrator Waveforms (Typical)

transistor is 270 ohms. Paralleling the value of r_b' with the value of R_L , 270 ohms with 1400 ohms, gives 225 ohms. The effective load resistance therefore varies between 225 and 1400 ohms. The load line corresponding to 225 ohms is also plotted through V_{CC}, O on the figure.

The next step in design is the determination of the correct base-current value. The switching cycle may initially be assumed to be symmetrical, so that the base current for each transistor of the multivibrator is turned on for half the time. Evidently, the average base current during the conduction period for either transistor must be twice the overall average value, giving the active base currents for the two conditions as 40 and 80 μA .

The voltage on the base of the transistor during conduction ($i_b \text{ max} = 40 \mu A$) is 172 mV, and for zero base current, 110 or less mV. This means that the change required for a base-current change of 40 μA is 62 mV. Further examination shows that 90 mV change is required with a current change of 80 μA .

Because of the short conduction time of a multivibrator compared to its period, active switching occurs at very small values of current in the initially-extinguished transistor. This also is the region of small forward conductance. With a large value of base-bias resistance, therefore, the capacitor that couples the collector of the nonconducting transistor to the base of the conducting transistor will quickly develop full supply voltage across itself because of the high base conductance in the conducting transistor. Consequently, the base voltage will drop rapidly and turn this transistor off unless the base biasing resistance is sufficiently

small that an appreciable part of the required base current may flow through it. The time constant of this circuit depends on both the circuit capacitance and its resistances, and also on the base resistance of the transistor

$$C_c(R_L + R_b / (1 + G_i R_b)) = T \tag{13-2}$$

where R_L is the static load resistance, R_b is the base biasing resistance, and G_i is the effective input conductance for the transistor as given in Chapter 4. In this equation, the value for R_L is in the neighborhood of or less than 1000 ohms, and the typical value of G_i in the active region is as large as 0.002 mho or possibly larger. The result is to place a minimum value on the coupling capacitors below which the circuit does not function.

Suran has shown that the maximum operating frequency of a multivibrator is approximately equal to the noise-corner frequency (Ref. 3).

$$f_{n2} = f_m = f_a / \sqrt{\beta + 1} \tag{13-3}$$

Using this frequency with the preceding equation and an approximate value of $1/G_i$ of 1000 ohms, the minimum value of the coupling capacitance C_c that can be used with the circuit is 150 pF. In practice, the value used should be at least 10 times this value unless special circuits are used.

Eq. 13-2 shows that the rate of decay of the charge in the coupling capacitance is a function of the load resistance in series with the collector to which the capacitor is coupled. Normally, the value of R_b is sufficiently large that it has little effect on the value of the expression $R_b(1 + G_i R_b)$, and consequently its value should be selected based on the switching characteristics rather than on frequency-response characteristics.

Selection of the static operating point for the base circuit at a high value of base current rather than low is better for the following reasons:

1. Reduced sensitivity to device characteristics at high base current, particularly with saturation
2. Ineffective clamping at high conduction unless the average current is high
3. Reduced total device dissipations with saturation
4. Possibly somewhat faster switching.

The variation of current gain from device to device is less significant with multivibrators when the transistor is biased near the saturation region than when it is not, although even then the behavior is by no means in-

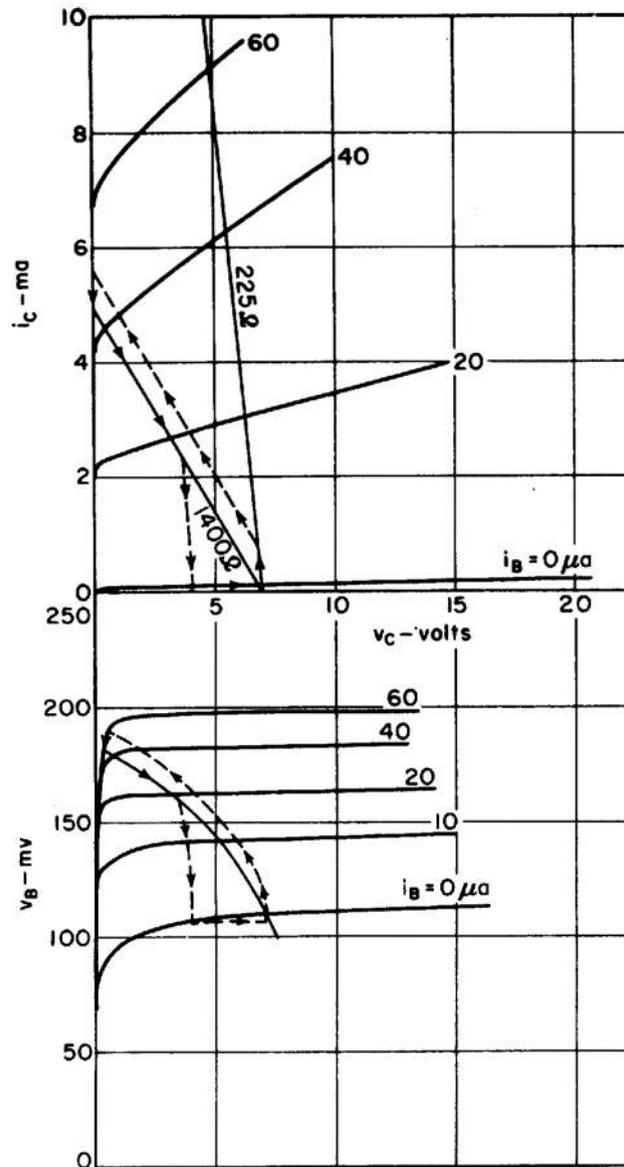


Fig. 13-5. Design of Multivibrator for Example 13-1

dependent of current gain. This reduced sensitivity is a result of the increased clamping under full conduction, since at saturation the base current increases sharply and thereby defines an endpoint more sharply. A sharp discontinuity in characteristics is required to produce accurate clamping. The reduced dissipation is a result of the lower voltage applied from collector to emitter in the saturation (negligible dissipation occurs when the device is cut off) and it is **also** a result of more rapid switching from the one state to the other. The more rapid switching is a result of increased loop amplification.

The fact that the transistor saturates sharply and then drifts out of the saturation condition means that the peak current flow will be appreciably greater than that which would be noted from finding where the base-current contour for twice the static base current approaches the saturation line. Averaging of the base current along the drift contour may be accomplished by the use of any of the averaging formulas, the Legendre or orthogonal method, the Fourier method, or any other convenient method. Although **between** switching episodes, there will be some curvature to the contour

of current plotted as a function of time, it is comparatively small.

13-1 LOOP AMPLIFICATION

So far, no consideration has been given to the fact that the average loop gain of the multivibrator must equal unity over the operating cycle, as is necessary with any oscillator. During the switching period, the amplification of the circuit may reach values as high as several hundred or possibly even several thousand. The fact that the minimum amplification cannot be less than zero indicates that the conduction time during which the loop amplification is very high must of necessity be only a small fraction of the repetition period of the oscillator. This condition can be altered by capacitances in the transistors and in the circuit, because on an instant-by-instant basis the capacitances do decrease the effective amplification and at the same time alter the duration of the switching period. If the amplification is computed on an instant-by-instant basis, including the effects of both circuit and device capacitances, the switching time will be found to depend on the integrated amplification, and the times of completion of the switching function also will be found to be correct.

Much more rapid decay of charge occurs in the coupling capacitor connected to the base of the conducting transistor than in the one connected to its collector. This means that the collector voltage nearly reaches the supply voltage, after which the second transistor begins to switch on and the final rapid decrease occurs. This is quite different than is the situation with tube multivibrators, because the discharge of the coupling capacitor connected to the grid of the conducting tube leaves it in a state of full conduction, and negligible change of plate voltage occurs until conduction commences in the nonconducting tube.

13-2 OTHER USABLE CONFIGURATIONS

The symmetrical multivibrator configuration just discussed is the basic configuration, and in one of its many modifications is possibly the most commonly used. Its waveform deficiency often makes the use of a different configuration desirable, namely, one which gives a more accurately formed square wave. One such configuration is the emitter-coupled multivibrator. This circuit in its tube arrangement is also the simplest one, giving a reasonably accurate square-wave output.

Typical circuits for the tube and the transistor versions of this circuit are shown in Fig. 13-6.

The operating cycle of this circuit is somewhat different than that for the conventional symmetrical circuit, because in one state, the output transistor is operating at its static point, and in the other, its current is cut off. The input transistor either draws a decaying collector current, or is cut off, as shown in Fig. 13-7.

The duration times for each half of the cycle of this multivibrator are not necessarily equal. If the design is arranged so that the bias resistances of the circuits can be adjusted, however, the dwell-times can be made approximately equal for either polarity of the wave. Because the output transistor either is operating under static conditions, with a constant base current, or it is turned off, the waveform is very nearly square in shape.

The bias point for the output transistor should be placed reasonably near the saturation region, but need not be at full saturation. The bias point for the input transistor must be sufficiently high to yield a loop gain for the circuit having a peak value large compared to unity. If these conditions are fulfilled, and the coupling capacitor is sufficiently large to permit the oscillations to develop, then normal multivibrator action can be achieved.

The emitter-follower action on the input transistor helps to reduce the input-conductance loading on the coupling circuit, making it possible to have an appreciable value of R_{b1} without having it swamped out by the input conductance. Consequently, the frequency can be controlled by the base-bias resistance to a much greater extent than is possible with the ordinary transistor multivibrator. Also the charge and decay of the capacitor is considerably less dependent on the input conductance of the transistor. The input resistance for the emitter-follower may appear to be as large as 50,000 or 100,000 ohms or more, making possible the use of a 10,000- to 20,000-ohm bias resistance. During the part of the cycle that the emitter-follower is conducting fully, the amplifier coupled to it is turned completely off, and the full multiplication of input impedance is available at the base of the follower. Consequently, the behavior of this circuit is almost identical with that of the corresponding tube multivibrator.

EXAMPLE 13-2. Design an emitter-coupled multivibrator using a 2N592 transistor. Determine a possible set of operating conditions, and select a set of component values that will assure multivibrator action. In addition, estimate the multivibrator period when the coupling capacitor has a capacitance of 0.02 mF.

If 15V is taken as the supply voltage, 3000 ohms the load for the output stage, and a protective resistance of 2000 ohms is used in the collector circuit of the input

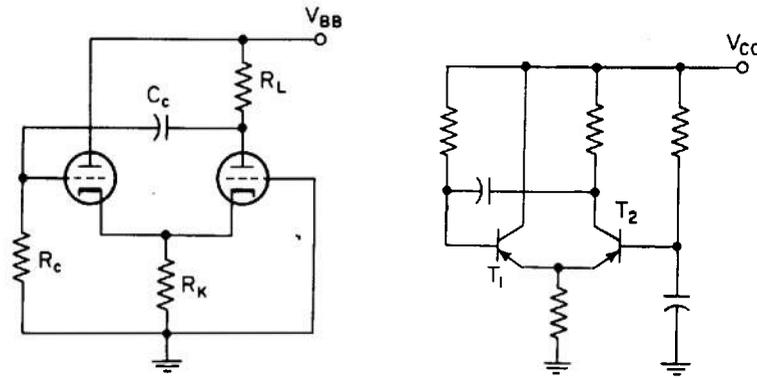


Fig. 13-6. Emitter-coupled Multivibrator

transistor, the load contours shown in Fig. 13-8 result. The input transistor requires a load resistor to limit its dissipation, but this load resistor must be smaller than that for the output transistor because the current flow in the input transistor must be greater than that in the output to obtain proper switching action.

If the active base current for the output transistor is taken as $125 \mu\text{A}$, the corresponding emitter-current flow is approximately 4.4 mA . If, now, an initial static emitter voltage is taken to be 0.5 V with respect to the emitter-return, the required emitter-return resistance is 110 ohms . The base of transistor T_2 must be bypassed to ground (emitter-return) if effective switching is to result. The base voltage required is 175 mV greater than the emitter voltage, or 675 mV . To reduce the current in T_2 to zero, the base-to-emitter voltage must be reduced to less than 45 mV , or the minimum emitter current during the conduction period for the input transistor T_1 must be at least 25% greater than the static conduction current in the emitter of T_2 . The time required for the emitter current to decay from its maximum value to the value that initiates conduction in

T_2 is approximately half the overall switching period of the circuit.

The calculation of the two quiescent periods for the two states of the multivibrator is relatively conventional. During the period for which T_1 is nonconducting, the discharge of C_c through R and R_{b1} controls the inactive period. The total voltage change at the base of T_1 is essentially equal to the voltage change across R in series with T_2 . As a result of the conduction in T_1 prior to switching, the voltage across C_c is equal to the voltage difference $V_{CC} - V_{bc}$, where V_{bc} is the voltage on the base of T_1 just prior to the initiation of switching. This voltage must be just large enough to block off conduction in T_2 . It is determined by first setting the emitter voltage so that T_2 is extinguished, and then finding first the emitter current for T_1 required to develop the voltage and second the base-to-emitter voltage for T_1 to make the current flow possible. The total voltage V_{bc} is the sum of the resulting base-to-emitter voltage and emitter return voltage. Because the base-bias resistor is returned to the collector supply rather than emitter, the total voltage applied to C_c is the difference of that across R , and that across R_b . This voltage must decay to the value required to initiate conduction in T_1 . The decay period is a function of the equation

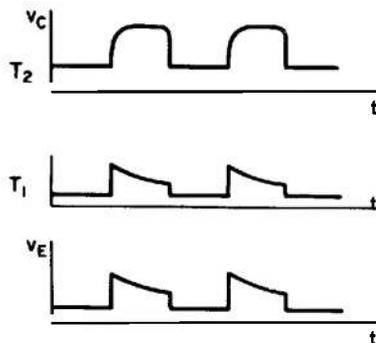


Fig. 13-7. Typical Emitter-coupled Waveforms

$$t = (R_L + R_{b1})C_C \ln \left[\frac{(V_{CC} - V_d)}{(V_{CC} - V_L + V_{bc})} \right] \quad (13-4)$$

where V_d is the voltage from the base of T_1 to emitter return for initiation of conduction of T_1 , V_L is the voltage across T_2 for full conduction through it, and V_{bc} again is the base voltage at extinction for T_1 . Because the nominal value of R_{b1} is

$15/0.000125 = 120,000$ ohms
 if input loading can be neglected, the time constant is approximately

$$t = 120,000 \times 10^{-8} \ln [(15 - 0.6)/(15 + 11 - 0.6)]$$

$$= 2.4 \times 10^{-8} \ln (11.7)$$

This is approximately 1.2 msec. (Note that the 0.6 V has been neglected in this calculation.)

The passive conduction period for T_1 is shorter than for T_2 , as the input conductance of the transistor T_1 introduces considerable loading into the circuit. The switching time is approximately 20% of the value mentioned.

The extremely small amount of voltage change required from base to emitter on a transistor, coupled with the overall circuit characteristics of the emitter-follower, may make desirable the use of some additional series resistance in either the base or the emitter circuits of the transistors. An increase in the value of the emitter resistance R_e from 110 to 500 ohms is an effective way of increasing the range of voltage change, because the amplification of the circuit is still available, and the range of voltage that can be tolerated by the emitter-follower is greatly increased. With a 100-ohm emitter resistor and 1900 ohms protective load for T_1 , the total change that can be developed in the emitter of the follower is 0.75 V, whereas with 500 ohms and protective load of 1500 ohms, the maximum change is 3.75 V.

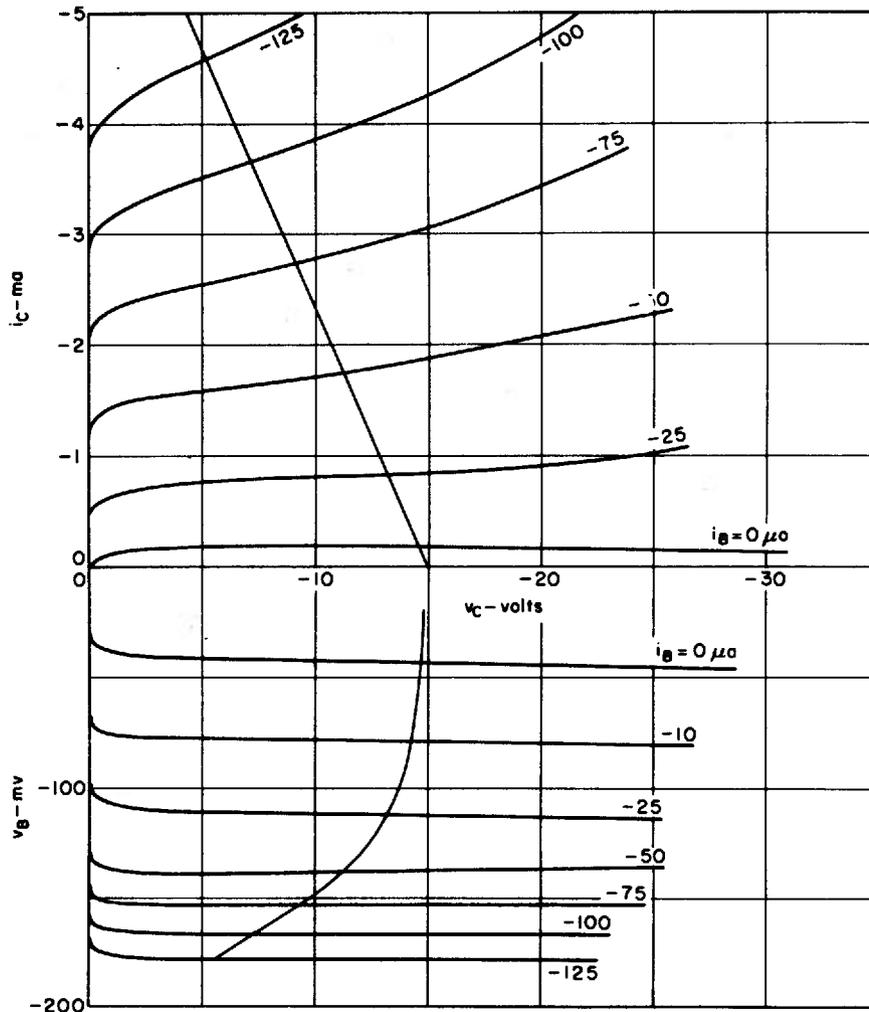


Fig. 13-8. Input Load Line for Example 13-2

The load contour for the output transistor during its deactivation cycle follows the general pattern shown in Fig. 13-9. The collector voltage rises until the emitter-follower saturates, at which time the collector voltage remains approximately fixed, and the collector current, except for capacitor charging-current, drops to zero. The initiation of reversal cannot occur until the voltage across the capacitor approximately equals that between the collector supply terminal and the saturation voltage required on the base of T_1 . Voltage decay at the base terminal then permits the emitter of the follower to drift downward in accordance with the discharge rate until the trigger level is again reached, this time in reverse direction. The total approximate discharge time constant is determined in terms of the rates, where $s_1 = 1/T_1$ and $s_2 = 1/T_2$

$$\left. \begin{aligned} & s_1 C_C (R_L + R_{b1} / (1 + G_i R_{b1})) \\ & \doteq s_1 C_C (R_L + 1/G_i) \\ \text{for } G_i R_{b1} > 1 \\ & s_2 C_C (R_L + R_{b1} / (1 + G_i R_{b1})) \\ & \doteq s_2 C_C (R_L + R_{b1}) \end{aligned} \right\} \quad (13-5)$$

where G_i is the input conductance of the emitter-follower. The first time constant is small compared to the second, because G_i limits the resistance component when it is large. The dwell times depend on the ratio of the nominal voltage change Δv_0 to the actual switching change Δv_1 or Δv_2 as required. If either of the Eqs. 13-5 are written as $s_1 R_1 C_1$ or $s_2 R_2 C_2$, then the times may be determined in terms of the equation

$$T_i = R_i C_i \ln (\Delta v_0 / \Delta v_i) \quad i = 1, 2 \quad (13-6)$$

Since, however, the value of R_i may vary with the bias value, strictly a step-by-step determination of T is required. As a first approximation, the formula used with tube multivibrators may be used.

Because the total current through the output transistor is 4.4 mA, and the emitter resistance is 500 ohms, the total base voltage on the transistor is $2.20 + 0.17 = 2.37$ V. The bias resistance for the output transistor then is $12.6 / 0.000125 = 100,000$ ohms. For the input transistor, the static operating conditions may be set so that both transistors will draw approximately the same current if the coupling capacitor is removed; then the actual quiescent position may be altered somewhat to improve the equality of the two halves of the cycle. Taking both base currents equal to $110 \mu\text{A}$, the emitter

current for T_1 is about 4.2 mA, that for T_2 , 3.9 mA, for a total of 8.1 mA, or a total emitter voltage of 4.05 V. This is satisfactory because $110 \mu\text{A}$ through the 100,000-ohm resistors leaves the required 4.0 V available for the bases of T_1 and T_2 . The correct current is approximately $108.5 \mu\text{A}$, and the emitter and base voltages are 4.0 and 4.17 V, respectively.

The bypass capacitor on the base of T_2 must be sufficiently large so that the base voltage does not change appreciably compared to the base bias range, which is about 100 mV. A 10-mV change during the quiescent period is the maximum that can be tolerated. If a repetition rate of 500 Hz is required, for example, the size of bypass capacitance may be determined in terms of the equation

$$CV = iT \quad (13-7)$$

where the half-cycle time T is 0.001 sec, and i is half the average change in static current between the two quiescent periods. Solving for C gives

$$C = 100iT$$

where i is in amperes and T in seconds. For this example, the value of i is half of $125 \mu\text{A}$, and the capacitance is between 6 and 10 mF.

The approximate amplification of the combination of the two transistors may be obtained by the use of the equation for the cathode-coupled amplifier as derived in Ref. 1, Chapter 6. It is

$$K = g_{f1} g_{f2} R_e R_L / [1 + (g_{f1} + g_{f2}) R_e] \quad (13-8)$$

This amplification may be as large as 93 for the circuit under consideration, because the values of g_{f1} and g_{f2} are about 0.075 mho, and the net R_L for $R_e \pm R_L = 3000$ ohms is 2500 ohms. This condition occurs when the denominator is approximately $2g_f R_e$.

If the input conductance of the input transistor is calculated on the basis of $g_i = 0.001$ mho as an average value, the effective value is about 38 pmhos, considerably more than the 10 pmhos selected for the bias resistor in the preceding analysis. This means that the circuit must be redesigned to accept a bias resistance of at most 10,000 ohms. This may be done in either of two ways, by dividing the bias resistance into a 10,000-ohm and a 90,000-ohm section, and placing a large bypass capacitor at the tap, the 10,000-ohm section being connected to the base, or by dividing the supply voltage to

provide approximately 6 V, bypassing the tap, and returning a base-bias resistance of about 10,000 to 20,000 ohms to the tap. The size of the bypass capacitor again should be chosen to keep the change to approximately 10 mV.

13-3 OTHER ARRANGEMENTS

Probably the most useful modification that can be made in a transistorized multivibrator is the introduction of emitter-followers coupled to the collectors of each of the amplifiers (Fig. 13-10). This arrangement makes the signal voltage available at low impedance instead of relatively higher impedance, and can increase the signal-output voltage available. These followers may be coupled directly to the collectors as in

Fig. 13-10, or they may be used as coupling elements between the coupling capacitors and the base leads of the amplifier transistors as in Fig. 13-11. This modification makes possible the use of better operating conditions, since the $R-C$ coupling network now has a considerably higher load impedance than otherwise. The result is a simplified design for low-frequency multivibrators. It has the disadvantage of requiring an additional voltage supply for the returns from the emitter resistors for the followers. It is a better configuration, however, because it makes possible the use of the base-bias resistors as the resistance component of the frequency-determining network.

The general procedure of design that has been described can be adapted to most forms of multivibrators, and the calculation of switching rate may be made by the method described in *Conductance Design of Active*

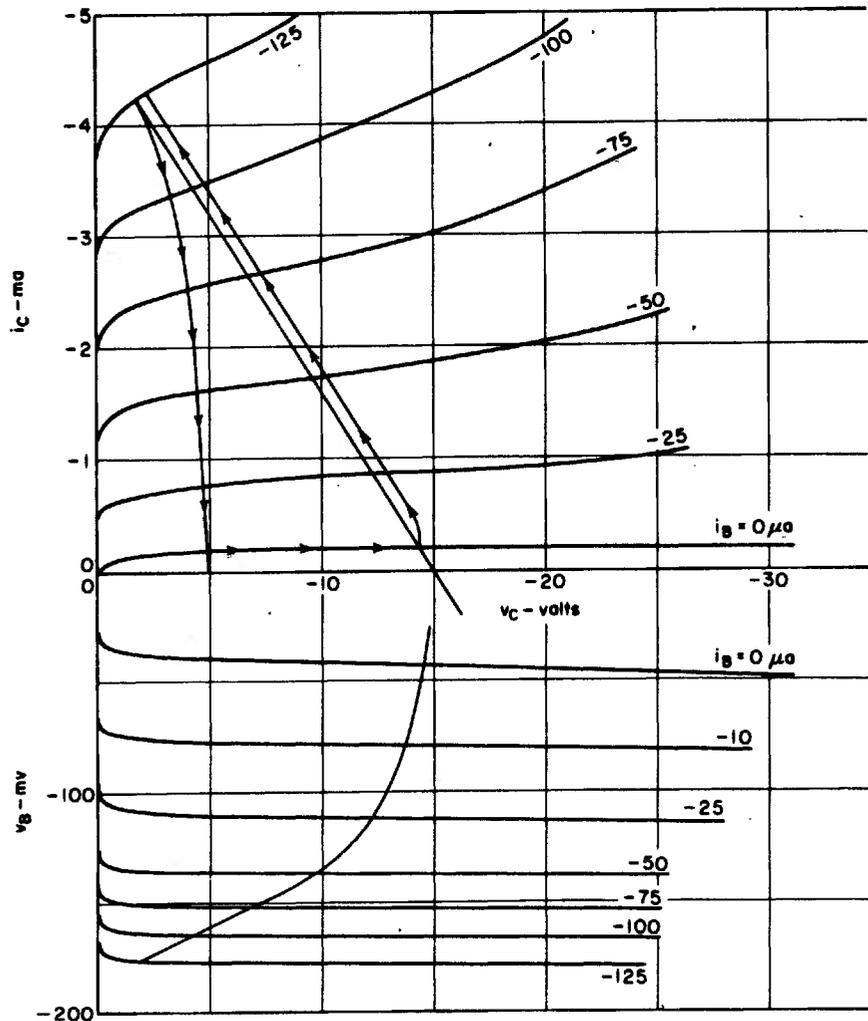


Fig. 13-9. Output Contour

Circuits (Ref. 1). The only change required is the substitution of the correct amplification equations. The calculation of the maximum repetition frequency may

be made directly by the use of the equation for the noise-corner frequency as has been described by Suran and Reibert (Ref. 3).

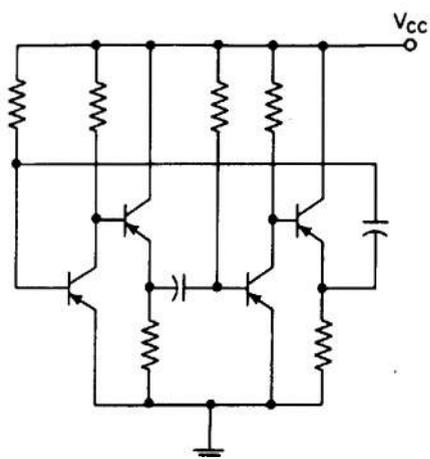


Fig. 13-10. Emitter-follower-coupled Multivibrator-collector Type

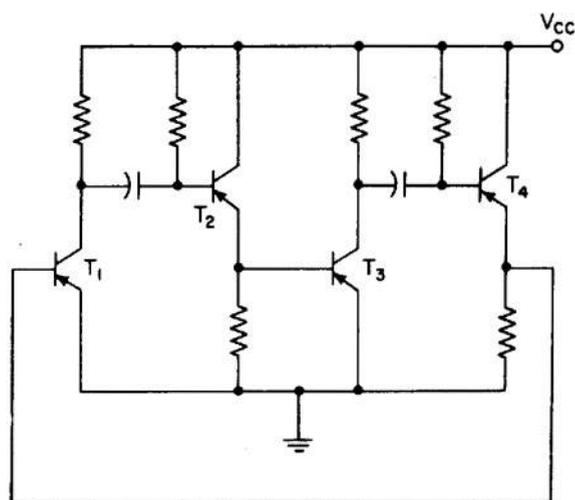


Fig. 13-11. Emitter-follower-coupled Multivibrator-base Type II

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2. K. A. Pullen, Jr., "Conductance Design of Relaxation Circuits", IRE *Trans.*, Conv. Rec., 1953.
3. J. J. Suran and F. A. Reibert, "Two-Terminal Analysis and Synthesis of Junction Transistor Multivibrators", *Proc. IRE*, March 1956.

CHAPTER 14

SWITCHING AND SAMPLING CIRCUITS

14-0 INTRODUCTION

Many switching circuits use multivibrators with resistive return paths in parallel with the collector-to-base coupling capacitors. The presence of these DC paths makes possible the locking of the circuit in either of its static states. The discussion in this chapter starts with consideration of the method of modifying an ordinary multivibrator to produce a unit that requires a trigger pulse to switch it, the so-called univibrator, or single-shot multivibrator. This discussion is followed by a study of bi-stable, or flip-flop circuits. Several different forms of each of these circuits are considered, and the means of controlling and triggering them also are examined. A number of examples of the basic methods of use of the various configurations are included, among which is the control of a diode matrix by counting circuits. The design of such diode matrices is discussed briefly, and their use in the control of sampling circuits described. In addition, par. 14-10 includes a brief explanation of a method of construction of bi-directional counting circuits, and explains how they may be made into bi-directional decade counters. The chapter concludes with a brief discussion of tunnel-diode switching circuits and a brief resume of the general contents of the handbook.

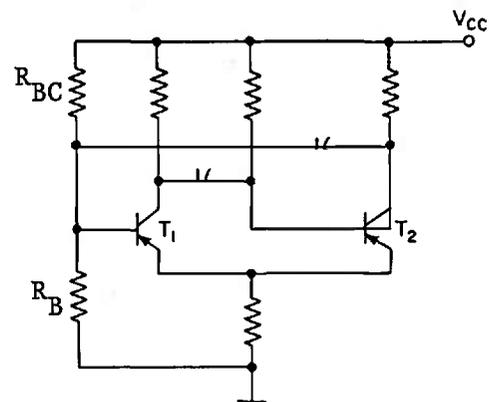
14-1 UNIVIBRATORS

of one of the transistors by an amount sufficient to reduce the overall loop gain to a value less than unity.

A typical circuit for a symmetrical univibrator is shown in Fig. 14-1. The transistor T_1 is blocked in the nonconducting condition by the action of the divider. The pulse shapes shown at the various points in the circuit indicate the relative magnitudes of the voltages. The pulse shapes assume positive direction for the collector voltage with respect to the emitter so that an increase in conduction may be indicated by an upward shift in base voltage. The triggering pulse may be introduced either on the nonconducting transistor, in which case the pulse tends to turn it on, or it may be introduced on the conducting transistor, in which case the pulse tends to turn it off.

The value of amplification during transition in each transistor is large enough so that free-running switching can occur unless one transistor is switched nearly completely nonconducting as previously explained. Consequently, some common-bias resistance in the emitter return usually is required, and the fixed bias voltage shown in Fig. 14-1 is also required. Normally the one transistor is biased just beyond current cutoff to make certain that stray pulses will not trigger the circuit.

The introduction of the initiation voltage for the univibrator is best accomplished at a point outside the main switching path. Because both the bases and the



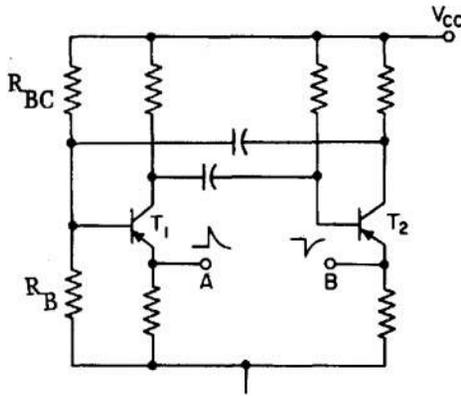


Fig. 14-2. Univibrator Triggering

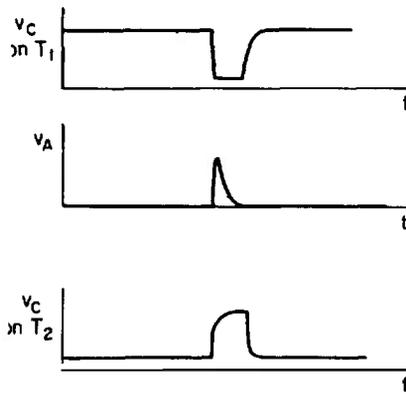


Fig. 14-3. Voltage Waveforms

collectors of the transistors are in the switching path for a conventional symmetrical univibrator, either one of the base-return leads or one of the emitters may be used for triggering, or a diode injection circuit may be used. Some of the possible positions for introduction of the control signal are shown in Fig. 14-2. Emitter-injection circuits are particularly convenient, because pulse integration is minimized.

If the injection is made into either one of the bases or one of the collectors of the transistors, even with isolating diodes, the behavior of the loop is altered by conductive loading during the activation period. The potential diagrams of the circuit shown in Fig. 14-2 are included in Fig. 14-3. In each of these potential diagrams, the collector potential is measured vertically upwards with respect to the emitter, so the relative polarity of the initiation pulses may be deduced directly.

The emitter bias used with the univibrator should be

sufficiently large so that the resistance from the base to the emitter-return on the nonconducting transistor can be between 1000 and 10,000 ohms. With the lower value, an isolation resistance as shown in Fig. 14-4 may be desirable, but with the larger value, it is unnecessary. The base-bias resistance for the second base is made sufficiently small to place the second transistor in a saturation condition, and the emitter resistance is just sufficiently large to permit the cessation of current flow in the nonconducting transistor.

EXAMPLE 14-1. A multivibrator is to be converted to a univibrator by the introduction of a divider circuit and a common-emitter bias resistance. The base-to-emitter voltage for current cutoff is 100 mV, and that for saturation is 200 mV. The divider circuit is to carry a current equal to the saturation base current in the conducting stage, namely, 80 μ A. The collector saturation current is 7.0 mA, and the collector supply voltage is 10 V. Design the modifications required to convert this circuit to a univibrator.

The series bias resistances for the base terminals of the two transistors as a multivibrator are between 100,000 and 120,000 ohms because the resistance is about 12,000 ohms per volt, and the voltage is approximately 9 V. If the base-tap point for the nonconducting transistor T_1 is placed 6000 ohms above ground, and a 5000-ohm additional leak resistance is used, the voltage at the base is approximately 0.5 V, the emitter voltage should also be 0.5 V. For a collector saturation current in the conducting transistor of 7.0 mA, the required emitter resistance then is 70 ohms, this resistance being bypassed by a large capacitor. An additional resistance of 30 ohms may be connected in series with either of the transistors as desired for the introduction of the trigger pulse. The collector load resistances are nominally 1360 ohms. A 1500-ohm resistor probably would be used.

The base-circuit configuration for T_2 is unchanged, the base return resistance remaining at 100,000 ohms,

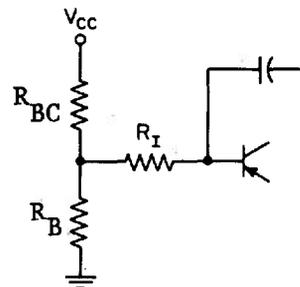


Fig. 14-4. Position of Isolation Resistance .

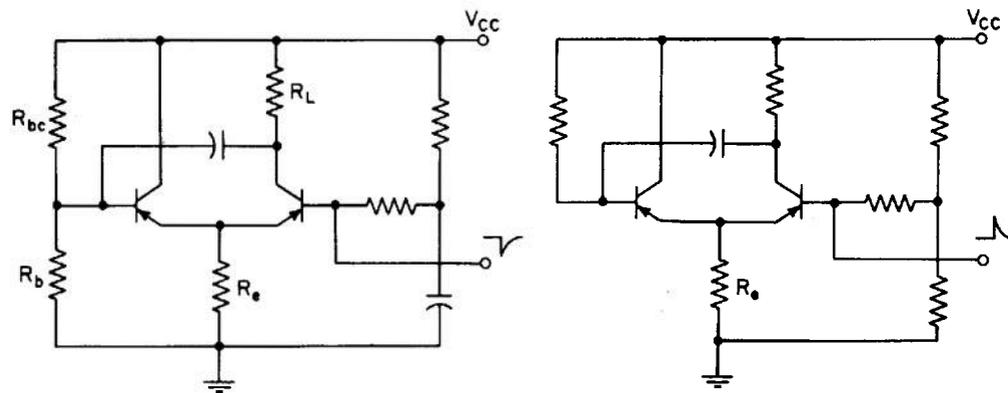


Fig. 14-5. Emitter-coupled Univibrator

and the coupling capacitors of such a size that the required pulse duration results.

14-2 THE EMITTER-COUPLED UNIVIBRATOR

The emitter-coupled univibrator is closely related to the corresponding multivibrator, and is modified from it in an exactly similar manner as was the symmetrical univibrator. This circuit is particularly convenient in that it has a "loose" base connection that may be used for pulse injection.

This univibrator differs from the symmetrical one in that there are two different ways of setting up the trigger circuit, one for taking a positive pulse on the spare base connection, and one for taking a negative pulse. With the symmetrical circuit, it is only necessary to move the injection resistance from one emitter to the other, whereas with the emitter-coupled univibrator, it is necessary to shift the bias networks instead. If the base on T_1 is biased to conducting conditions, then a pulse having the same polarity as the collector voltage must be introduced into the injection base lead, whereas if the input base is biased to nonconducting, then the input pulse has opposite polarity from the collector voltage, Fig. 14-5.

The design of the bias-locking circuits for the emitter-coupled univibrator closely parallels that for the symmetrical type, but it differs in several important respects. In the first place, operation with the second transistor T_2 nonconducting is better for generation of long pulses, because it makes possible the use of a larger R-C constant in the feedback path. Similarly, for high

frequencies, a reverse situation may be somewhat better, because the value of the R-C constant is then reduced appreciably by the base input resistance. Otherwise, circuit conversion for opposite-polarity trigger pulses requires an interchange of the bias networks.

14-3 THE BASIC BI-STABLE CIRCUIT

When the coupling capacitors of any of the multivibrators described in Chapter 13 are paralleled with an appropriate resistance, and the bias circuits are modified to provide voltage division, a circuit that can be triggered into either of two states results (Fig. 14-6). The adjustment of the required bias circuits is somewhat critical, however, and as a result they require rather careful design. Otherwise, although the circuit may switch easily in one direction, it may prove to be considerably more difficult to switch in the reverse direction, and may behave more like a univibrator than a bi-stable circuit.

A typical circuit for one form of transistorized bi-stable circuit is shown in Fig. 14-6. In this circuit, the current flow through the bias path should be sufficient to provide the required base-saturation current for the conducting transistor with the other transistor in a nonconducting state. At the same time, it must not be large enough to limit the available loop amplification through excessive shunting of the output current through the auxiliary network. The design must be capable of functioning in the presence of the static collector current I_{co} of the transistor as well. For purposes of design, a shunt leakage resistance capable of passing appreciably more than the maximum value of

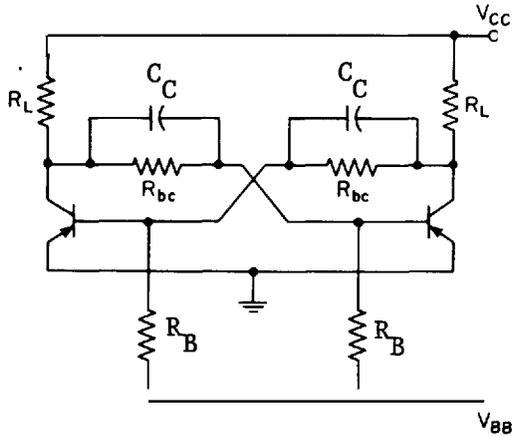


Fig. 14-6. Bi-static Current

I_{co} should be connected in parallel with the base-collector circuit of each transistor, and then the design made including this amount of leakage current. If the design can switch this load, then satisfactory operation of the circuit over the required temperature range can be expected.

The base-emitter voltage required to place a transistor in saturation is relatively important in all switching circuits, and is critically important in some forms such as the DCTL circuits. If, for example, one transistor in a switching system is capable of conducting strongly with a value of base voltage for which it should be nonconducting, the circuit may block in one state. Likewise, if one of the transistors requires a larger bias voltage for the conducting state than the other, then the circuit will be more difficult to switch in one direction than the other, and circuit operation may be unsatisfactory. As long as the current gain in the transistors is sufficiently large to provide some margin in the switching current, it is not particularly important in typical circuits. In fact, frequently there will be no correlation whatsoever between transistors that function and the current gain as measured by a static test if the minimum required value is available.

Those who have worked with bi-stable circuits made with tubes are aware that the balance and values of the grid voltages with the tubes out of the socket must be adjusted correctly to provide efficient switching conditions. The same situation is true with the transistors and other components in the resistive cross-coupled flip-flop circuit. In addition, the transistors should have available a minimum current gain of at least 10 along with matched values of base-to-emitter voltage. Small wonder, therefore, is it that the construction of a satis-

factory bi-stable circuit using transistors is more difficult than making a similar circuit for use with tubes.

Sometimes a bi-stable circuit will be erratic in spite of everything seemingly being right, the current gains adequate, the voltages balanced, and the devices balanced. One of the most insidious causes of erratic operation under these conditions is an over-sensitive circuit. For example, it is possible for the circuit to be so sensitive that it switches not just the way that is intended, but it may also switch back on a single pulse. In other words, the circuit does not lock out after switching on a single pulse, but detects the tail of the pulse and accepts it as an additional trigger signal. This condition easily can develop with a circuit using steering diodes to direct the switching pulse. Shortening the duration of the switching pulse is one possible solution to this problem, but the shortening usually must be done by reduction of the base-return R component, and not the C-component, of the coupling network.

The introduction of switching pulses is best achieved in either the collector or the emitter terminal of one of the transistors, not in the base circuit. If the pulses are introduced into a collector, steering diodes are normally used to route the pulse to the proper transistor. This pulse usually is a downward-directed pulse.

The pulses may also be introduced into the emitter circuit. In this case, an extremely low-impedance drive source is required, because the transistor loading is very heavy. Considerable additional circuitry is required for this mode of triggering, so it seldom is used. Emitter-injection is used in connection with the reversible decade counter described later, where it is used to reset the decade.

The minimum size coupling capacitor in the switching circuit is dependent primarily on the base-to-emitter capacitance, and through it on the noise-corner frequency. The required value of capacitance may be calculated in terms of the base-to-emitter voltage during conduction and the collector-to-emitter voltage during nonconduction, the minimum value being set by the value required to compensate the circuit response to-constant delay as a function of frequency. If the capacitance selected for the coupling capacitor is larger than the minimum size, it overcompensates the circuit and speeds the switching somewhat. The actual value of capacitance selected should be at least twice the minimum value determined in terms of the equations

$$\begin{aligned} C_C/C_{be} &= V_{bt}/(V_{ce} - V_{bt}) \\ 2\pi f_{\alpha} C_{be} &= (g_i' + g_f') \end{aligned} \tag{14-1}$$

where C_{be} and C_c are the base-to-emitter and the coupling capacitances, respectively, V_{cz} is the collector-to-emitter voltage of the transistor in the nonconducting state, and V_{bt} is the base-to-emitter voltage under conditions of full conduction.

The minimum capacitor size may be calculated in terms of the required charge in micro-micro-coulombs (pC), because the charge may be reduced to a capacitance in terms of the base-to-emitter voltage, and the inverse ratio of the voltages used to correct for the potential division. The equation for the capacitance then takes the form

$$C_c = C_{be} V_{bt} / (V_{cz} - V_{bt}) = Q_s / (V_{cz} - V_{bt}) \quad (14-2)$$

Data on Q_s are given by some manufacturers.* The use of the equation for the a-cutoff frequency enables the user to obtain a reasonably good approximate value for C_c at almost any condition in the operating range of the transistor, because the value of $(g_{f'} + g_{f'})$ in micromhos is approximately 39,000 times the emitter current in milliamperes.

When large values of current are drawn through the transistors in a bi-stable circuit, and the supply voltage is reasonably near to the rated maximum value, it is possible for a phenomenon known as "latching" to occur. This phenomenon is caused by the avalanche-type behavior of the transistor at high values of collector voltage and current. The behavior of typical contours of constant base current for large values of v_c and i_c are shown in Fig. 14-7 (replotted from the RCA data-sheet on the 2N1300 transistor). The lines of constant base current, instead of turning approximately horizontal but continuing to rise slowly, actually dip to a lower voltage as the collector current increases, and then start to rise. When latching occurs, the transistor switches "off" to the higher-current lower-voltage intersection of the load-line crossings with the avalanche section of the base-current contour.

If the collector supply voltage is large enough that the load line crosses the base-current contour in the avalanche region, a stable operating point simulating the normal nonconducting conditions results, but it occurs at relatively high collector dissipation, and can

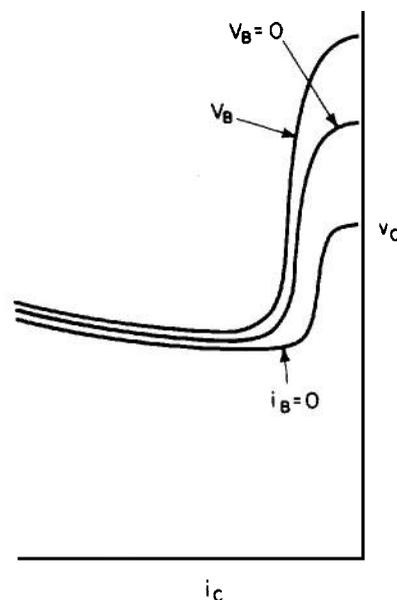


Fig. 14-7. Avalanche Collector-voltage Effect

cause the destruction of the transistor. Consequently, the collector supply voltage selected must be sufficiently small so that the load line will not cross the avalanche sections of the base-current contours. A circuit that may be used for the selection of satisfactory transistors not subject to this difficulty or for selection of a voltage for the collector supply for which latching will not occur is shown in Fig. 14-8. The value selected for V_{cc} should be less than the rated value of BV_{ce} and frequently less than half BV_{cb} , and it should exceed the finally selected voltage for the circuit by at least 1 or 2 V. The push switch in Fig. 14-8 is closed to place the transistor in saturation. The voltmeter should read the same voltage after opening the switch as it did before closing it. Otherwise, latching is occurring and either the transistor or the voltage is unsuitable.

14-4 THE EMITTER-FOLLOWER BI-STABLE CIRCUIT

The simple bi-stable circuit just described is somewhat marginal in its operation, in that the base-loading through the cross-coupling network limits the switching speed and also limits the output power that can be

*See the data sheet published by Radio Corporation of America on the 2N1300 transistor for further data on the Q_s method.

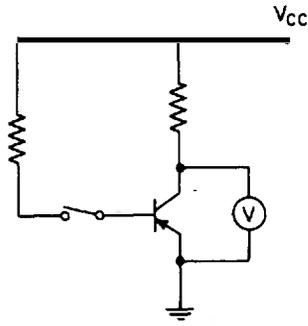


Fig. 14-8. Avalanche Test Set

developed by the circuit. This difficulty is commonly corrected by the use of emitter-followers either to drive the cross-coupling networks or the bases of the switching transistors. The use of the emitter-follower directly on the collector of the switching transistors is convenient for the development of switching pulses for a group of load transistors, whereas the use at the base input improves the switching properties of the circuit itself. The use of the followers at the bases of the switching transistors does not increase the load-driving characteristics unless the loads can be activated from the voltage available in the base circuit of the switch units.

Both of these configurations may require additional power input compared to the flip-flop circuit itself, but the power distribution is sufficiently more effective that the increase in requirement may be surprisingly small. Where power capabilities are adequate, the use of these coupling followers can be well worth-while. Design of the combined circuit is based directly on the design of the simple switching circuit and the design of emitter-followers.

EXAMPLE 14-2. Design a counting circuit using a 2N1300 transistor with a collector voltage of -5 V and a base-return voltage of 5 V. Calculate the minimum value of the cross-coupling capacitance.

An approximate replot of the static data provided with the 2N1300 transistor is included in Fig. 14-9. The input family given is only approximate, as the data given on the device show the variation of the base voltage for a given base current most effectively in the saturation region, but not as the curves break into the active area.

If a contour of constant collector current is superimposed on the input family, it takes the form shown by the dash contour, showing that as the base current increases, so does the base voltage. The amount of variation of base voltage with large changes of base current in the saturation region (for a given value of

collector current) is so small that the significance of the curves is really quite small for applications other than switching. For example, a base-current change from 0.5 mA to 5 mA with a fixed collector current of 20 mA carries an accompanying change of 50 mV in base voltage. This change indicates a base-spreading resistance of less than 10 ohms.

The resistive load contour for the switching circuit, neglecting the effect of the cross-coupling circuits, is drawn in a conventional fashion. The contour plotted in Fig. 14-9 corresponds to a resistive load of 125 ohms. This load line does not tell the whole story, however, because the coupling load must be included. This load both increases the load current in the resistor and decreases the available collector voltage. The circuit loading coupled to the collector of the conducting transistor is just that which results from current flow in the coupling network, whereas the loading coupled to the collector of the nonconducting transistor includes both the network and the input current for the base of the conducting transistor. The result is that the equivalent supply voltage is

$$V_{CC'} = [V_{CC}/(1 + G_C R_L)] + \frac{V_{BB} G_C R_L}{(1 + G_C R_L)} \quad (14-3)$$

where R_L is the load resistance in the collector circuit, G_C is the instantaneous value of the conductance of the cross-coupling network, including the loading resulting from the input conductance of the other transistor, and V_{CC} and V_{BB} are the collector and the base supply voltages, respectively. Because the polarities of the two supplies are usually different, and the second term is small in value, the effective collector supply voltage is somewhat less than the nominal value.

The conversion of the approximate load contour to the actual contour may be started at the saturation condition, because at that point, the value of $R_f = 1/G_C$ is equal to the sum of the resistances R_{CB1} and R_{B2} . The corrected value V_{CC} is determined in terms of Eq. 14-3, and a process of integration back along the contour may be started. For the present problem, the current in the coupling network may be taken as 2 mA under saturation conditions. The total resistance ($R_{CB1} + R_{B2}$) is 2500 ohms. This gives a value of $V_{CC} = -4.52$ V, and the parallel combination of resistances is 119 ohms. The load contour corresponding to this condition also may be plotted as in Fig. 14-9 as long dashes. Neglecting the capacitance loading, transfer takes place along this line until the base of the second transistor starts to draw appreciable current.

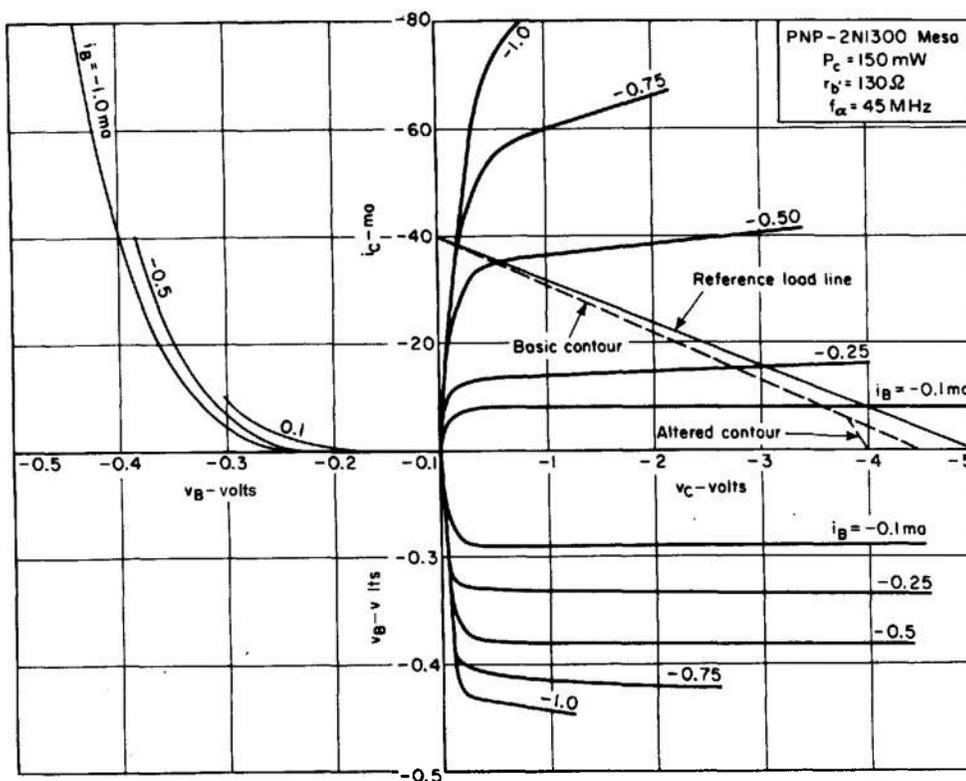


Fig. 14-9. Switch Circuit Calculation

Then the value of R_x changes, and the slope of the corresponding part of the load contour changes to correspond to the new conditions. Because the first transistor now is nonconducting, conditions that will provide a specified base current to the second, conducting, transistor should be found. This is easily accomplished by setting $R_{BC1} = R_x$, $R_{B2} = 2500 - R_x$, and the saturation base current for the second transistor as I_{bt} . The resulting equations are

$$(R_L + R_x)I_{bt} = V_{CC} - V_{bt} \tag{14-4}$$

$$(R_t - R_x)(I_t - I_{bt}) = (V_{bt} - V_{BB}) \tag{14-5}$$

where I_t is the total current in the divider network. These equations may be solved for R_x , giving

$$R_x = \frac{[V_{CC} - V_{BB} + I_{bt}(R_t - R_L) - \sqrt{(V_{CC} - V_{BB})^2 - 2I_{bt} \times (R_t + R_L)(V_{CC} + V_{BB} - V_{bt}) + I_{bt}^2(R_t + R_L)^2}]}{2I_{bt}} \tag{14-6}$$

Only the negative radical is used because the positive gives values of R_x greater than R_t .

If the radical is examined for the possible presence of zeros, it turns out that its value is always positive, and that it may have either a minimum or a maximum in the possible range of use. Differentiating the terms in the radical with respect to k , where k is defined in terms of the equation

$$kV_{CC} = I_{bt}(R_t + R_L)$$

gives the equation

$$(2k - 2)V_{CC}^2 - 2V_{BB}V_{CC} + 4V_{bt}V_{CC} = 0 \tag{14-7}$$

This reduces to the general relation for k

$$(V_{BB}/V_{CC}) - 2(V_{bt}/V_{CC}) = k - 1 \tag{14-8}$$

This equation is plotted in Fig. 14-10 for different values of the ratio V_{bt}/V_{CC} . Two particularly useful points are those for $V_{BB} = -V_{CC}$, for which case $k = -V_{bt}/V_{CC}$, and with $V_{BB} = 0$, giving a value of $k = 1 - 6$, where ϵ is a small positive increment, or $\epsilon = -2V_{bt}/V_{CC}$.

For the circuit under consideration, therefore, the optimum value of k is small, approximately 0.08, but a somewhat larger value should be selected to make certain that the current gain is adequate. The saturation value of the base current is approximately 0.8 mA, and the corresponding base voltage, 0.400 V. The total resistance of 2500 ohms and saturation current of 0.8 mA in the base correspond to a value of k of 0.4. The circuit may be redesigned for a resistance load ($R_c + R_L$) of 1000 ohms, giving a value of 0.16, possibly as close to the optimum as is practical without the use of emitter-followers. The balance of this design is based on the value of the factor k of 0.40. Solving Eq. 14-6 for R_x gives a value of 1088 ohms, or nominally 1000 ohms, leaving 1500 ohms for R_{CB1} and R .

The collector voltage at which the variation of the load line from the reference sets in may be determined by finding the point at which the base voltage crosses the zero-base-current line. It is given by the equation

$$V_{ct} = (V_{bz}R_L/R_{bz}) + V_{BB}(1 - R_L/R_{bz}) \tag{14-9}$$

where V_{bz} is the base voltage for zero base current, and V_{ct} is the corresponding value of collector voltage for the associated transistor. In this instance, with $v_B = 0.3$ V, the transfer starts when the collector voltage has risen to 3.83 V. At this point, the load contour curves away from the plotted linear contour. The total change of base voltage to full saturation is an additional 0.1 V, corresponding to a further increase at the collector of 0.167V to 4.00V. The modified contour is sketched on the figure. The total voltage change is approximately 3.7 V.

If emitter-followers are introduced for each of the coupling circuits, then the collector load resistance in series with each of the switching transistors may be increased, because only a small part of the switching power is drawn from the main switching transistors. The peak current through the switching transistors now may be limited to 10 mA, and the switching power for the coupling network drawn from the emitter-followers. The modified circuit is shown in Fig. 14-11. If, now, the total current through each emitter-follower is taken as 20 mA, the total resistance R , is approximately 500 ohms. A total of 200 ohms of this resistance is between the emitter of the follower and the base of the switching transistor, and the balance of 300 ohms is placed between the base and the base supply. The maximum dissipation in the follower transistor is $0.010 \times 5 = 50$ mW, well within the 150 mW rating of the 2N1300 transistor at 25°C. The resulting value of k is

$$0.001 \times 500/5.0 = 0.1$$

approximately the optimum value. The required load resistor for the switching transistors is now 500 ohms instead of the former 125 ohms. Interestingly enough,

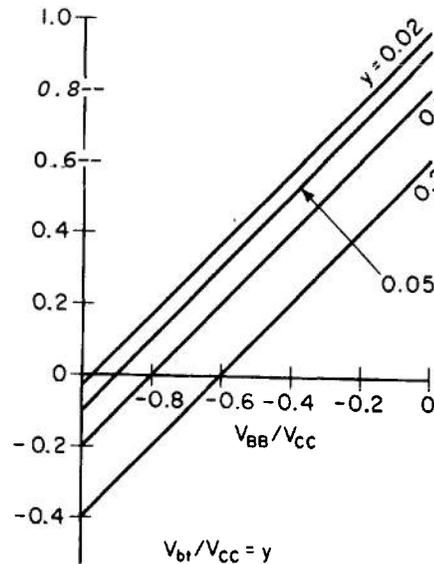


Fig. 14-10. Relation for Voltage Division

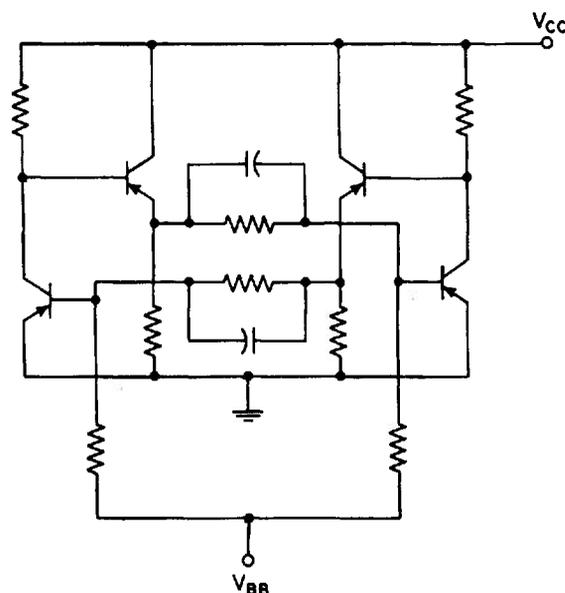


Fig. 14-11. Emitter-follower-coupled Flip-flop

the total power consumption is about the same as without the followers, because the modification makes possible a more effective use of the available energy. The gain in the emitter-followers is well over **0.75**, the value at which an even trade of capacitance and resistance will occur between the base of the follower and the load resistance in the switching transistor and the output impedance of the follower is so low that only the base-spreading resistance of the switching transistor limits the switching rate in the balance of the circuit.

14-5 DIRECT-COUPLED SWITCHING CIRCUITS (DCTL)

The operating conditions for which k equals $1 - \delta$ in Example 14-2 correspond to what is sometimes called "direct-coupled transistor logic", or **DCTL** circuitry. These circuits differ in that the bases and the collectors of the switching transistors are cross-connected with no separating resistance or capacitance at all. Because of the direct connection, no base-return resistance is required, as can be verified from Fig. 14-12. This type of circuit can be used primarily because the voltage on the base terminal of the conducting transistor is greater with respect to its emitter than is its collector voltage, and in fact the collector voltage under conduction is slightly less than the base voltage required to cause current flow in the device. There may be as much as **200 to 300 mV** difference between the two points under saturation conditions. Because of the

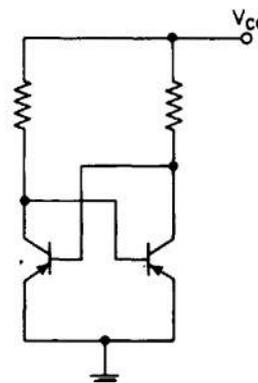


Fig. 14-12. Direct-coupled Transistor Flip-flop

large amount of base current that flows in the conducting transistor, only a few tenths of a volt change are developed between the off and the on states with **DCTL** circuits, with the result that although the basic switching circuit is simple, its control circuitry may be somewhat more critical than is required with standard circuits.

The principal problem with these circuits is one of getting adequate balance in the values of base voltage at which saturation and turn-off for the respective transistors occur. Because the total switching range is from a change as small as **50 mV** to as much as **100 mV** from start of conduction to saturation, to assure reliability it is desirable to have the values of base voltage of the respective transistors in a specific switching unit correspond to within approximately **10 mV**. No form of

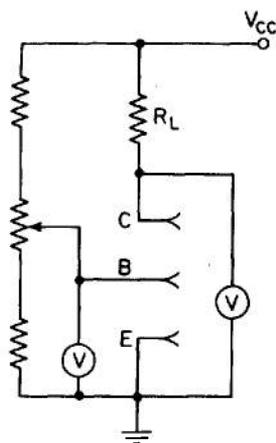


Fig. 14-13. Saturation Voltage Tester

alpha tester can check this, since it is to a large extent dependent on the base-spreading resistance of the individual transistors. Fortunately, a simple testing device can be used for the purpose. Its basic circuit is shown in Fig. 14-13. With this device, the transistors to be used are adjusted, one-by-one, until a specified degree of saturation results, for example, a collector-to-emitter voltage of 0.200 V, and the base voltage required to produce the condition is noted. Some types (code numbers) of transistors will be found to vary widely, whereas others may be formed into a small number of groups. If the transistors are coded and used in groups, with all of the transistors in critical position for a given individual circuit taken from the same group, this difficulty can be avoided. The groups are typically 10 mV wide.

The small voltage change available from the DCTL flip-flop makes necessary the use of some auxiliary circuits for output and pulse-direction. These additional transistors to some extent offset the extreme simplicity of the flip-flop itself, but even so, the circuit can prove to be very useful. Possibly the simplest method of controlling the basic flip-flop is based on the circuit shown in Fig. 14-14. This circuit, one of several reported by Clark, obtains its pulse-direction through the use of collector clamping (Ref. 1). If either transistor T_2 or T_3 is in the conduction state, the corresponding T_1 or T_6 is unable to develop any voltage change, because its partner is saturated and limits the collector voltage change in the trigger transistor to a few tenths of a volt. With the transistor of the pair, T_2 , or T_3 , which is not in the conduction state, however, the full collector-supply voltage is available, and a strong trigger pulse can be formed. When a trigger pulse is introduced on the trigger line, therefore, it is routed into the proper side of the circuit and coupled into the switching circuit

through the capacitor, thereby changing the state of the circuit.

The transistors used with this flip-flop are driven very hard into saturation, and consequently may not switch as rapidly as with some circuits. The circuit simplicity, however, may make its use desirable in place of a faster circuit. The output signal for triggering the succeeding stage may be extracted directly from either T_3 or T_4 , or it may be obtained from either T_2 and T_3 . In any case, the trigger signal should take the form of a pulse with this circuit.

The transistors T_2 and T_3 are included in the circuit to give the full voltage change of which the circuit is capable. The waveform available on the collectors of these transistors includes switching transients in addition to a reasonably rectangular waveform because of the fact that they are used for the introduction of the switch direction control signals. As a consequence, they may not have a sufficiently square waveshape for applications such as control of a diode matrix. The waveshape should be adequate for triggering an additional counter in a binary chain, however. Actually, a switching pulse for the next binary element in a chain probably could be obtained from the collector of either T_3 or T_4 , because these transistors do switch sufficiently hard to pulse the control circuit of a succeeding stage.

The main problems in the design of a complete functioning circuit based on Fig. 14-14 are two, first, the proper selection of the transistors, and second, the selection of the proper size of coupling capacitor for the interstage circuit. Empirically, the capacitance value should depend at least approximately on Eqs. 14-1 and 14-2, although loop amplification can act to increase the value required. For this reason, over-compensation is essential.

EXAMPLE 14-3. Design a DCTL circuit for use with the 2N217 transistor, using a supply voltage of 7 V for the flip-flop itself. Take the α -cutoff frequency as 0.4 MHz, and use a load resistance of 5600 ohms.

The only points in question in this circuit are the adjustment of the size of the coupling capacitor and the setting of the pulsing transistors so they will pulse the circuit properly. Based on a base voltage of 200 mV, and a voltage across C_c of 5 V, the minimum coupling capacitance allowed by Eq. 14-2 is

$$C_c = (0.20/7) \times 2 \times 10^{-8} \\ = 8 \times 10^{-10} \text{ pfd or } 800 \text{ pfd}$$

Introducing a factor of 4 gives a value of 3200 pF as a good starting point for design.

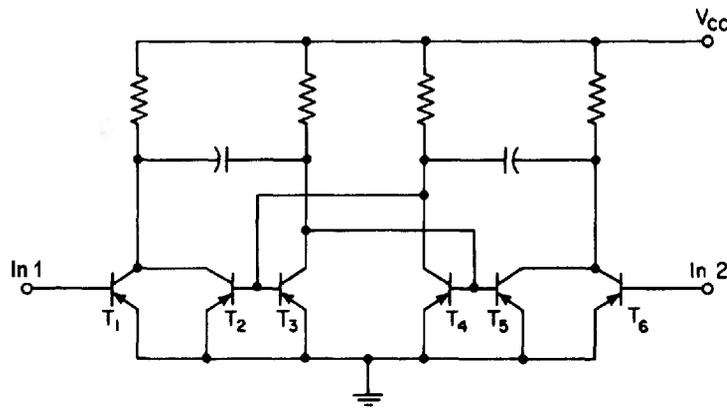


Fig. 14-14. Direct-coupled Transistor Logic Binary

The base of the routing transistor should be biased to draw a few microamperes current, just enough to reduce the collector voltage to about 10% less than its supply. Then the circuit will be sensitive to a low-impedance trigger voltage of between 20 and 50 mV, and it will pulse the output of the appropriate directing transistor sufficiently to switch the circuit. To determine the amplitude of input pulse required, it is only necessary to work backward from the desired change of collector current in the trigger amplifier.

14-6 USE OF DCTL CIRCUITS WITH SWITCHING MATRICES

One of the ideal applications of DCTL binary circuits is the control of switching matrices that are used to control and route signals from one set of inputs to a different set of outputs. This paragraph describes the modifications that may be helpful in making the binary circuit control a matrix, and the next paragraph discusses the design of diode matrices for use with the binaries. A later paragraph describes how such a circuit can be used to control the input of a telemeter modulator.

To achieve clean switching in any kind of switching circuit, it is necessary that the control signals be as free as possible of unwanted signals or noise. The transistors T_2 and T_3 in the DCTL circuit have rather good collector-voltage waveforms, but not sufficiently good for use with a switching matrix, because the voltage does vary from the nominal value during the switching transient. For this reason, an additional pair of repeater transistors may be used in parallel with T_2 and T_3 , but they must have separate outputs to keep out the switching signals. The circuit shown in Fig. 14-15 serves the purpose excellently. The signals developed across the col-

lector loads are excellent square waves and have ample amplitude to produce a precise switching action. Depending on the amount of loading developed in the matrix, the amplifier may be used directly, or it may be used to control an emitter-follower controlling the matrix.

The emitter-follower form of matrix control has proven to be nearly ideal, since the output voltage can be extremely stable, and also a type of transistor can be selected that causes the transistor to draw considerable current when it is providing power to the matrix. If the counter and signal-output circuits use PNP transistors, it is common for an NPN transistor to be required for the follower application. The amplifiers and the followers may be designed by the conventional methods already described.

14-7 DIODE MATRICES

Diode matrices are commonly used to convert the switching data generated by a binary counter to another counting base, such as sequential or decimal counting. These matrices may be made to perform either as "and" gates, in which case the matrix detects the fact that all of its inputs are in a specified state, usually referred to as the on or "and" state, or as "or" gates, in which case the matrix detects the fact that one or more of its inputs is in the "on" state. Typical simple "and" and "or" gate circuits are shown in Fig. 14-16. With the "and" gate, the output is clamped to the bias source except when all of its input terminals are biased to block conduction. When the blocking condition occurs, a specified signal may be transmitted through the gate with negligible loss, but otherwise the clamping action of one or more of the diodes prevents the transmission of the specified signal. On the other hand, with

the "or" gate, the presence of an "on" state potential on any one of the inputs to the gate causes the transmission of the signal pulse.

The design of the logic for the diode matrix is an extremely complicated process that will not be discussed in this handbook because it is rather well described in some of the texts on computing machinery. A simple discussion of the process is included in *Transistor Electronics* (Ref. 2). It is of particular importance to the user, however, to know the properties of diodes, which are important in the construction of effective switching matrices.

Ideally, the diodes used in making switching matrices should have infinite conductivity in the forward direction, and zero conductivity in the reverse direc-

tion. Practically, the conductivity in the reverse direction is considerably more important in diode matrices than that in the forward direction because only one diode may be in series with the signal path, whereas there may be large numbers of them in parallel. Some of the tree-type combining matrices use a smaller number of diodes for the same switching combinations, but have more series-connected diodes in their circuits. With them, the forward conductance can be more important.

The forward-to-reverse resistance ratio limits the number of diodes that can be used in a diode matrix without excessive loading developing from diode leakage. The nominal operating impedance for the square

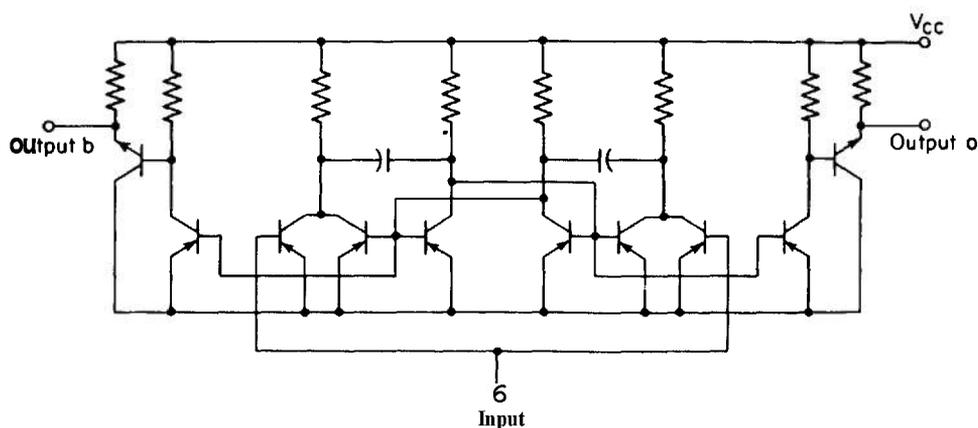


Fig. 14-15. Matrix-switching DCTL

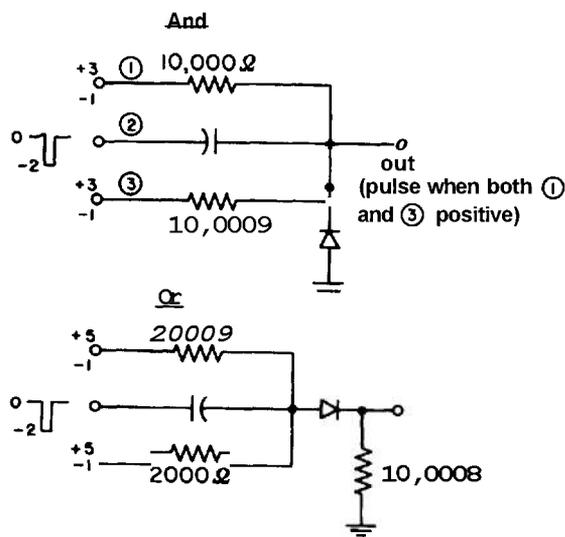


Fig. 14-16. "And" and "Or" Diode Circuits

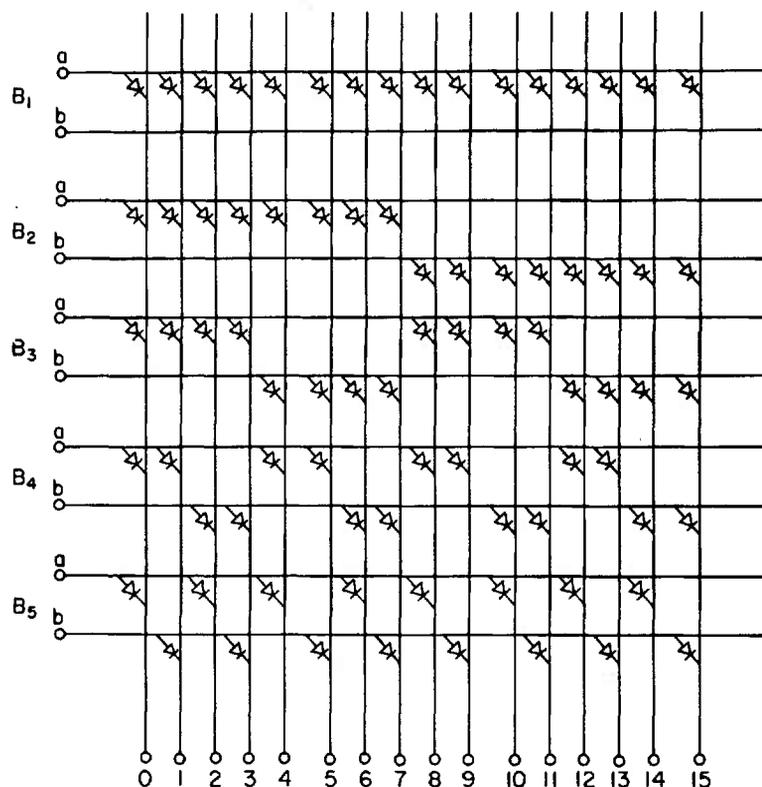


Fig. 14-17. Binary-consecutive Matrix

matrix may be estimated by determining the admittance

$$g_s = \sqrt{mg_f g_r} \quad (14-10)$$

where m is the number of diodes connected to a given transmission path, and g_f and g_r are the average forward and reverse conductances, respectively. The value of g_s should be at most a hundredth to a thousandth of the value of g_f for minimum loading on the signal, and the series impedance between signal input and signal output should be approximately the reciprocal of g_s .

Evidently for a diode to be satisfactory for matrix use with at least 10 diodes involved per output circuit, its reverse conductance should be less than a micromho. In the circuit shown in Fig. 14-17, the 32 output channels have 5 diodes per circuit, whereas the control circuits have 16 diodes each. Fortunately, the source impedance level for the control circuits can be kept very small by the use of emitter-followers in the control circuits, so that the number of diodes per output is important, whereas the number per binary control path is relatively less important.

The diodes used for switching matrices, besides having a very large forward-to-back ratio and a high back-resistance, should be all-glass or plastic encased, and they should be as small as possible within the physical resistance and current limitations. Metal-case diodes tend to be unsatisfactory for this application because of the crowded structure necessary in matrices and the ever-present possibility of development of bridging shorts. In addition, some metal-cased diodes are somewhat deficient in reverse resistance, and are consequently of little use in switching matrices. Hermetic sealing is also important, because it is the most effective method of making certain that operating characteristics are stable with time.

The diode matrix may be used as a multiple switch, or it may be used as a signal combining and switching arrangement. If the matrix is used for combining pulse or AC signals, then the number of diode gate circuits through which the signal must pass in reaching the output is relatively unimportant, whereas if the matrix is used for the selection of different individual DC signals, then the number of diodes can be of considerable importance.

14-8 A TELEMETERING COMMUTATOR

The diode matrix, along with an oscillator and countdown circuit, can be used effectively in a static telemetering commutator for use in research vehicles carrying magnetometers. Because of the sensitivity of the magnetometers, it is not possible to use mechanical commutators in this application, and commutation for a sequential telemeter requires some kind of an electronic network. The diode matrix, in simplified form, and its associated repeater network for repeating the input voltage in waveform and magnitude are shown in Fig. 14-18. In the form shown, no diode bias voltages are introduced in series with the main signal paths, just the base-to-emitter voltage for the repeater transistors, but it has the disadvantage that it is not possible to introduce any given signal into more than one input without interfering with operation of the circuit. Because repeated measurements within a normal switching cycle may be required at spaced intervals of time, the modification shown in Fig. 14-19 can be used with those channels for which multiple operation is required.

The interval of dwell on any one channel need not be limited to a single stepping period, but can be any binary multiple of it, two, four, eight, etc. Consequently, a great deal of flexibility is available in these units. In contrast to mechanical commutators, the duty factor of the transistorized commutator can be nearly 100%, because the series coupling impedances used between the signal source and the diodes provide the

required isolation and permit simultaneous switching. The input impedance of the emitter-followers is sufficiently high and the diode impedance in the transient condition is sufficiently high that the series resistance has negligible effect on the circuit during signal transmission. During the block period, however, it prevents the application of a low-impedance short on the voltage source.

The emitter-follower circuit used in this commutator is interesting in that the transistor T_2 , which is placed in the emitter return of T_1 , is connected to provide a high dynamic impedance to the emitter of the transistor T_1 , thereby making the output signal voltage almost exactly equal to the input signal voltage. The action of the diode matrix keeps all but a single one of the principal transistors T_1 , in an inactive condition, thereby preventing the mixing of signals between channels.

The linearity of the repeater circuit with its two transistors and the matrix switch depends primarily on the back-resistance of the diodes used in the matrix. With

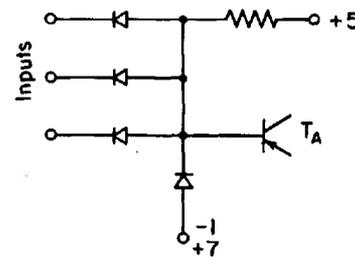


Fig. 14-19. Paralleling Diode Circuit

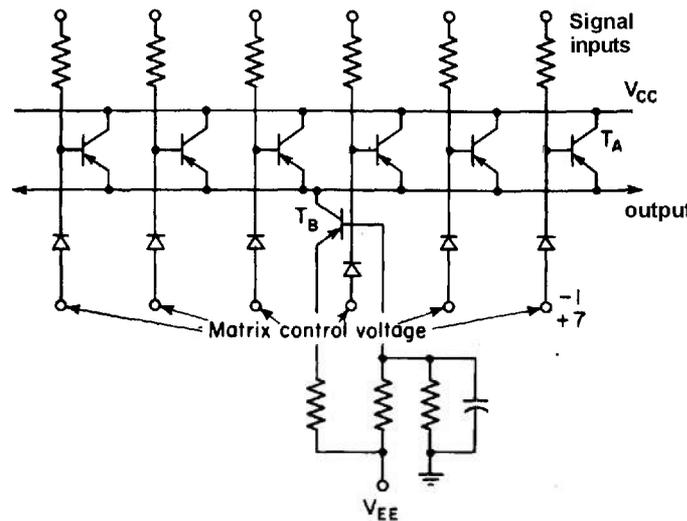


Fig. 14-18. Signal Repeater

diodes having back-resistances in the 1 to 10 megohm range, it is possible to get linearities that are better than 0.5% with a properly designed circuit.

14-9 BI-DIRECTIONAL COUNTERS

Normally, electronic counters based on flip-flop circuits are used to count in only one direction, but with minor changes, it is possible to make them bi-directional. The direction of count in a binary counter may be reversed by the transfer of the pulse-coupling network from outputs A to outputs B in Fig. 14-20. That this is the case may be seen from the counting diagrams shown in Fig. 14-21. The direction of progression of the counter with the couplings transferred is diametrically the opposite of that before transfer, and as a consequence, it constitutes a reversal of counting direction.

The introduction of a pair of "or" circuits between the two outputs of one counter binary unit and the input to the following binary can then select the routing of the pulses from one binary to the next if the two "or" circuits are switched in a complementary manner, that is, the one passes signal when the other is switched off.

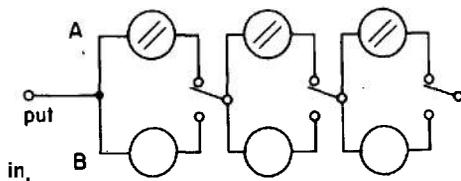


Fig. 14-20. Basic Bi-directional Counter

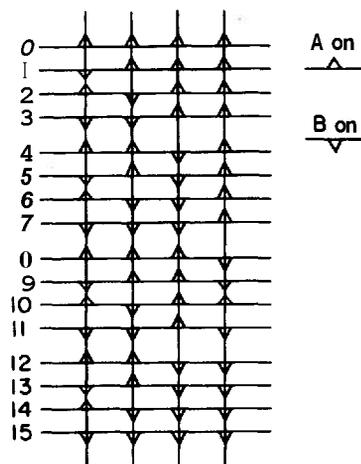


Fig. 14-21. Count in 4-bit Binary Counter

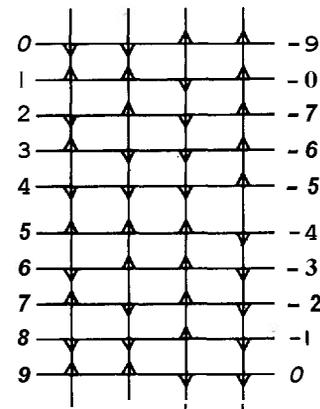


Fig. 14-22. Reversible Decade Counter

Such a configuration can therefore form a bi-directional counter, the only additional requirement being that a sensing circuit be provided ahead of the counter to sense the sign of the count. These counters are useful for counting the difference between a reference frequency and an unknown frequency. If count pulses arrive once per period of the signal being counted, there is no possibility of detecting the polarity of the count, but if the drift of the signal with respect to a reference signal can be measured several times per period, then the direction of drift can be used to control the counting direction. The discussion of the logic of such a system is beyond the scope of this handbook.

The bi-directional counter may be made into a binary decade counter if a count combination is used that is completely symmetrical. Fortunately, such a combination can be found which will convert a four-bit counter into a scale-of-ten counter that has skew-symmetrical final-count values. Such a configuration may be based on the 4-bit counter by taking the range of 3 through 12 from a 0 through 15 counter (Fig. 14-22). The counts on collector-group A are numbered 0 through 9 against the count numbers 3 through 12, and the counts on collector-group B numbered from 0 to -9 against the count numbers 12 through 3, namely, in the reverse order. The switching-level diagram shows that the count positions on group B, for a given number, correspond exactly to the count in reverse direction, for the same given number, with that in group A.

The only remaining problem is to install two "and" circuits, one for each direction, which detect the counts of three-reverse and twelve-forward. These two "and" circuits reroute the counting pulse to the appropriate reset circuit, in the positive-counting direction to reset the counter from 12 to 3, and in the negative-counting

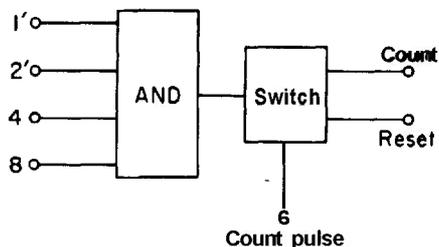


Fig. 14-23. Count Routing Circuit

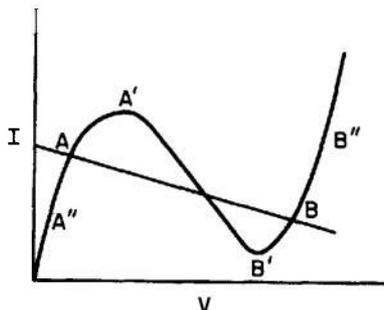


Fig. 14-24. Tunnel Diode Switch Circuit

direction to reset the counter from 3 to 12. If necessary, a lock-out circuit can also be installed to deactivate all count-transfer circuits during reset, thereby assuring reliable operation. One form the circuit might take is shown in Fig. 14-23.

14-10 TUNNEL DIODE SWITCHES

The tunnel diode is an excellent example of a two-terminal switch that has great potential for use in computers. Its principal advantages are its small size, high speed, and small power consumption.

Tunnel diodes can be used in countdown circuits by arranging them to take advantage of the two stable states, A and B, in Fig. 14-24. To accomplish switching, it is necessary to trigger the operating conditions either from A through A' to B or from B through B' to A. Then either of the indicated switching cycles results.

To produce, from a single-pulse type, first a switch from A to B and then from B to A, a circuit somewhat like that shown in Fig. 14-25 is required. If a negative pulse is applied to the input, and TD₁ is in the low-voltage condition, the pulse tends to take TD₁ from A to A' and TD₂ from B to B'. Diode TD₂ then switches to B and reduces the voltage across TD₁ so that diode

voltage B' is reached and it switches also. The next pulse takes TD₁ from A to A' and switches TD₂ back in the process. Then standard diode routing techniques can be used to introduce an output pulse from this counter into additional circuits.

Tunnel diodes can be used as pulse-forming amplifiers because a voltage sufficient to change the diode bias from A to A' will switch it to state B, and one capable of shifting the bias from B to B' will return the diode to state A.

The load resistance selected for use with a tunnel diode should be of such a value that a small lock-out margin, typically 20 mV, is available at point A, and possibly 50 to 100 mV at point B. These values specify both the load resistance and the supply voltage. Because switching is controlled at point A, the margin at B must be sufficient to provide usable values of R₀ and R₁.

The capacitor C is the memory element for the circuit, and controls the direction of switching. It should be sufficiently large to permit completion of change of state and prevent multiple switching.

14-11 SUMMARY

The two basic types of circuit design for use with active devices and with transistors in particular are the combination static-small-signal design, which is required with amplifiers of all types, and switching design, which is required with transfer-of-state circuits such as multivibrators, flip-flops, and other switching circuits. With the first of these types, small-signal data in some form for the active devices are required in addition to static data. Although it is possible to mini-

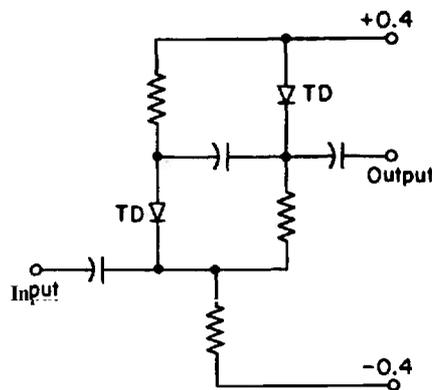


Fig. 14-25. Possible Tunnel-diode Bi-static Circuit

mize the dependence on these small-signal data by the use of least-squares smoothing techniques, such as the orthogonal polynomial procedure considered in Appendix C, much more adequate design can be obtained if the small-signal data are available. The first few chapters of this handbook develop forms in which these data can be provided most effectively, considering the stability of the various parameters with operating conditions and the relations of the data to the operating characteristics of the devices as a function of voltage, current, and frequency. The following group of chapters develops the basic equations and design procedures depending on the selected admittance plus base-spreading resistance representation, and applies them by a consistent procedure to a variety of circuits. Particular attention is given to the subject of oscillator design and the coordination of the properties of the linear and the nonlinear parts of the circuit to determine the limiting conditions of stable operation. A detailed discussion of the design of electronic mixer circuits is included, including an analysis of the effect of amplification variation on the mixer action in the circuit.

The final two chapters discuss the properties of circuits having a high degree of nonlinearity. The design objective with these circuits is to cause operation in two or more different states successively. The small-signal characteristics are important in these circuits only in that they make possible the calculation of the transition properties from one state to the other. Because it is seldom necessary to make detailed calculations of the loop amplifications, as a general rule the data required on these devices may be limited to static input and

output data. Implicit data on some of the small-signal data are required; for example, the ratio of the forward transfer admittance to the input admittance in the current gain, and the sum of the conductances and the capacitances in the frequency limits such as the a-cutoff frequency, and the base-spreading resistance. Orthogonal techniques can give an adequate estimate of these parameters for use with switching circuits.

Appendix A contains a derivation of the small-signal distortion equations. In addition, the appendices include a discussion of the use of topological techniques in the determination of driving-point and transfer equations for both linear and active circuits (Appendix B) and a discussion of the orthogonal method of approximating small-signal data (Appendix C). Appendix D includes a bibliography of papers and books used in the preparation of this handbook, and includes some notes on papers of particular significance in the development of the described techniques, and Appendix E describes one of the better sets of curve data presently available. Appendix F includes an assortment of curves on transistors in current use. These curves are organized in accordance with the principles of Chapters 2 and 3, and, where possible, they include small-signal data as well as the static. The static data are readily obtainable with some of the standard transistor curve tracers. Appendix G includes a nomograph for small-signal calculations and a variety of problems grouped by chapters. In addition, Appendix H contains a discussion of principles of information engineering, and Appendix I contains a discussion of the diffusion mode of operation of FET devices.

REFERENCES

1. E. G. Clark, "DCTL Complementing Flip Flop Circuits", *1957 Transistor and Solid State Circuits Conference*, Philadelphia, Pa.
2. R. B. Hurley, *Transistor Electronics*, John Wiley & Sons, Inc., New York, 1959.

APPENDIX A

DERIVATION OF DISTORTION EQUATIONS

The derivation of the equation for distortion of a nonlinear device in terms of voltage differences has been available for many years. The equation takes the form

$$D = 50(\Delta V_{\text{pos}} - \Delta V_{\text{neg}})/(V_p - V_n) \% \quad (\text{A-1})$$

The voltage differences in the two polarities, ΔV_{pos} and ΔV_{neg} , both represent averaged values of the amplification in the two directions, the one showing the average increase, and the other the average decrease. In this appendix, the distortion equations in terms of small-signal behavior are derived, based on an assumption of a linear variation of amplification with input voltage. Under these conditions, the distortion generated is principally a second-harmonic. First the variation of amplification with input signal should be established.

$$K = K_0 + K_1 v_b \quad (\text{A-2})$$

and the limiting values of amplification are given by the equations

$$\begin{aligned} K_p &= K_0 + K_1 \Delta v_b, & K_n &= K_0 - K_1 \Delta v_b \\ \Delta v_b &= V_{b_p} - V_{b_n} = V_{b_s} - V_{b_n} \end{aligned} \quad (\text{A-3})$$

If Eq. A-2 is integrated to give the output voltage, it gives

$$v_o = \int_{-\Delta v_b}^{+\Delta v_b} K dv_b = \int_{-\Delta v_b}^{+\Delta v_b} [K_0 + K_1 v_b] dv_b \quad (\text{A-4})$$

over the limits from $(-A v_b)$ to $(+A v_b)$. The result takes the form

$$v_o = K_0 v_b + K_1 v_b^2/2 \quad (\text{A-5})$$

before the substitution of the limits, and a similar form involving $A v_b$ after substitution.

The value of v_b may be expressed in terms of a sinusoidal input signal

$$v_b = V_B \sin \omega t \quad (\text{A-11})$$

and then Eq. A-5 takes the form

$$v_o = K_0 V_B \sin \omega t + (K_1 V_B^2 \sin^2 \omega t)/2 \quad (\text{A-6})$$

$$= K_0 V_B \sin \omega t + 0.25 K_1 V_B^2 [1 - \cos 2\omega t] \quad (\text{A-7})$$

From this last equation, the relation of the second harmonic to the fundamental is given by the equation

$$D = 100 K_1 V_B^2 / (4 K_0 V_B) = 25 K_1 V_B / K_0 \quad (\text{A-8})$$

If, now, the limit amplifications K_p and K_n are defined by the following equations, assuming predominate second harmonic

$$K_p = K_0 + K_1 V_B, \quad K_n = K_0 - K_1 V_B \quad (\text{A-9})$$

The differences and sums of these equations are

$$K_p - K_n = 2 K_1 V_B, \quad K_p + K_n = 2 K_0 \quad (\text{A-12})$$

Substituting these in Eq. A-8 gives

$$D = 25(K_p - K_n)/(K_p + K_n) \% \quad (\text{A-10})$$

The procedure for calculation of the third-harmonic component parallels that given.

APPENDIX B

TOPOLOGICAL EQUATION DERIVATION

B-1 PROPERTIES OF "NETWORK TREES"

The algebra involved in the derivation of the operating equations for transistor amplifiers is sufficiently complex that the use of simplifying methods of derivation can be very helpful. Flow graphs are useful for this purpose when only the transfer function is required, but other methods are required if both driving-point and transfer functions are required. One method that has proven extremely helpful in applications where both driving-point and transfer functions are required is the use of graph theory, or network topology, in the determination of the small-signal equations. Topological design is based on Kirchhoffs laws and several properties of "network trees".

1. With nodal networks, the self-admittance of the network may be expressed in terms of the quotient of the sum of tree products divided by the sum of the tree products for the network with the admittance terminals short-circuited.

2. A tree product is the product of a group of admittances so selected that each vertex is touched by at least one admittance and no closed paths or circuits are formed by the selected admittances.

3. The sum of the tree products includes all possible trees that can be formed using the given set of vertices.

4. No element of a tree (no branch) can appear more than once in any product in a network that contains no mutual inductance.

5. Active devices such as tubes or transistors have separate current and voltage representations; for example, the transconductance of a tube has a current element in the plate circuit, and a voltage element in the grid.

6. Trees for active circuits include some that may be called partial trees and others that are complete trees. Partial trees are ones found in either the current or the voltage graph, but not on both, whereas complete trees appear on both. These complete trees may

have different orientations for the two diagrams, but they have the same admittance components.

7. The relative orientations of the elements in the current representation and the voltage representation of a tree determine the sign of the tree. A series of transformations is made to determine the sign.

The application of these rules to the design of transistor circuits minimizes the probability of making errors of algebra because it establishes setup and checking routines that can be applied as the derivation is being made.

B-2 BASIC STEPS

The first step in the analysis of a circuit to obtain its driving-point or transfer immittance is the establishment of the composite circuit diagram. All passive elements may be represented as resistances in the usual way so that they are readily recognized, and then special symbols may be used to represent the special active elements, the current and voltage "immittances" that appear in the circuit. For transistors, the active elements are the transadmittances, y_f and y_r . In addition, the input and output voltages and currents may be represented by the special symbols. Such a composite diagram for a simple transistor amplifier is shown in Fig. B-1.

Next, the composite diagram may be separated into a voltage graph and a current graph. Each of the passive elements is included in both graphs, but only voltage components are included in the voltage graph and current elements in the current graph. The special symbols shown in Fig. B-2 are required both for voltage and current components of admittances and also for source and sink elements.

The voltage source element has the same properties as are possessed by a battery, that is, when the voltage is reduced to zero (removal) a short circuit remains. The current-sink element, which behaves as an ammeter, also presents a short circuit on its removal. On the other hand, however, the current source and the volt-

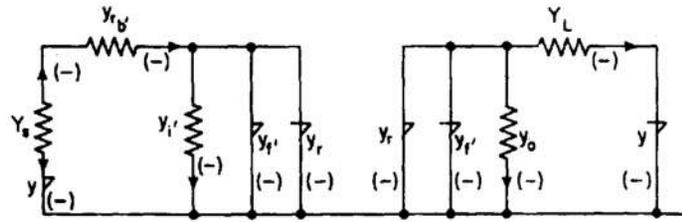


Fig. B-1. Topological Diagram of Transistor Amplifier (Negative end of admittance indicated by arrowhead.)

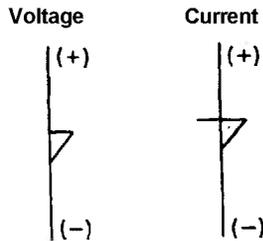


Fig. B-2. Voltage and Current Source Sink Symbols (and Transfer Symbols)

age sink both disappear from in parallel with an admittance when they are removed, so that an open circuit results. The same general properties can, with some limitations, result with the trans-elements. With tubes and transistors, the elements are voltage sinks and current sources, and hence represent open circuits on removal, whereas with a mutual inductance, the elements are current sinks and voltage sources, and in this case behave as short circuits on removal. The direction and type of action must be considered.

The trees may now be tabulated for either the current or the voltage graph. The required number of trees is determined as described in par. B-3. If the number of trees corresponding to the maximum are tabulated, only part of them are trees for the full network. Each tree of one graph may be checked against the other graph, and those that form trees on both graphs are called complete trees, those that form circuits or other defective trees are called partial or incomplete trees. Each defective tree for one graph has a corresponding but different defective tree present in the companion graph. After the incomplete trees are discarded, the remaining trees are separated into two groups, one containing the source admittance element y , and one not containing the source element. The complete topological equation for the network now reads

B-2

$$yW_{i'o}^{i'o} + V = T \tag{B-1}$$

where T is the tree sum, V is the sum of the trees not involving the y element, and the W term the sum of the y -tree terms with the y factored out. Because the y representing the source element acts as a generator or power source, the equation may be solved for $(-y)$ to give $(T = 0)$

$$Y_{i'o,i'o} = (-y) = V/W_{i'o}^{i'o} \tag{B-2}$$

The use of this equation and its equivalent for transfer networks for the derivation of driving-point and transfer immittance equations and the formation of its components is the subject for discussion in this Appendix.

The transfer admittance function may be determined in a similar manner. To set up the respective current and voltage networks for the determination of the trees for a transfer network, a source element is placed to activate the input terminal pair (in parallel if a current source and in series if a voltage) and a sink element is placed in the output circuit (in series with the load if a current sink, and in parallel with the load if a voltage). Then the trial trees may be determined from the current and voltage graphs, the partial trees eliminated, and the remaining trees sorted into those including y and those not including y as before. The transfer tree equation reads

$$yW + V = T_i \tag{B-3}$$

where the properties of W and V are dependent on whether the expression is for a transfer admittance or a transfer impedance. This equation is again equated to zero, because the y symbol represents both the energy source and the sink as before, and the solution for $(-y)$ again found

$$(-y) = V/W \tag{B-4}$$

If a voltage source and a current load are included in the circuit, the equation is for a transfer admittance, and the transfer term is in V , whereas if a current source and a voltage load are included in the circuit, the equation is for a transfer impedance and the transfer term is in the denominator, indicating that the transfer equation should be written as

$$(-1/y) = W/V \tag{B-5}$$

The denominators of Eqs. B-4 and B-5 are the internal network terms (typically

$$[1 + y_o R_L + y_i (R_s + r_b)(1 + y_o R_L)]$$

for the common-emitter amplifier).

The polarity sign associated with an individual tree may be determined by establishing a transformation table, and determining the number of interchanges and sign changes required to bring the symbol arrangements into coincidence. The table is established by writing one column for each significant node of the network, and arranging the admittances of the tree so each admittance is used only once, and one of the admittances is in each column. There may be two different arrangements for the two graphs, and the sign is determined by the number of changes required to bring the positions and the polarities of the symbols to coincidence.

As an example, consider the current and voltage graphs shown in Fig. B-3. If the transposition table is prepared based on the tree $Y_B Y_C Y_D$, the table takes the form

	$Y_B Y_C Y_D$			
	1	2	3	
v	Y_B	Y_C	Y_D	
i	Y_B	Y_D	Y_C	
Transpose	Y_B	Y_C	Y_D	$(-1)^1$

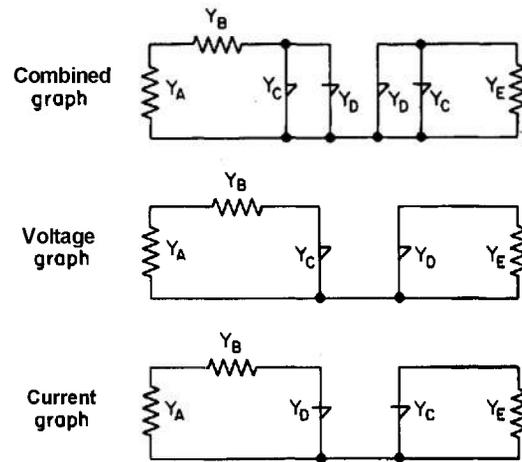


Fig. B-3. Voltage and Current Graphs

It is necessary to transpose the C and D terms in the current row to produce coincidence with the voltage row, and, because one sign change is required, the term has a negative polarity, giving a negative tree. If the total number of sign changes, including one for each individual transposition and one for each final sign reversal is even, the sign of the tree is positive, if odd, then negative.

EXAMPLE B-1. Derive the equations for input admittance and voltage gain for a simple transistor amplifier whose combined circuit graph is shown in Fig. B-4(A). Assume that the series resistance R_s in the base lead includes both the base-spreading resistance r_b , and the series source resistance R_s , and determine the equation for $R_s = 0$.

First the voltage and current graphs are drawn as shown in (B) and (C) in Fig. B-4. Directions are assigned on an arbitrary basis to each passive resistance because these signs are used in the polarity determination for the trees. Otherwise the symbols for passive resistances are conventional. The transfer elements and the source and sink elements use the special symbols shown in Fig. B-2. The complete set of partial trees for the voltage graph may now be tabulated for the driving-point (input) admittance.

y terms:

$$yY_iY_L, yY_iY_L, yY_oY_i, yY_oY_o, yY_oY_r, \\ yY_iY_r, yY_oY_o, yY_oY_L, yY_rY_i$$

Other terms:

$$Y_{y_i}Y_L, Y_{y_i}Y_o, Y_{y_i}Y_r, \\ Y_{y_o}Y_r, Y_{y_o}Y_o, Y_iY_LY_r$$

In each of these groups, those in the first row represent full trees, and the second row partial trees of the voltage graph. The corresponding partial trees of the current graph are

y terms:

$$yY_oY_r, yY_oY_o, yY_rY_L$$

Other terms:

$$Y_{y_i}Y_r, Y_{y_i}Y_o, Y_iY_LY_r$$

Writing the quotient for $(-y)$, but using all positive signs between terms gives the equation

$$(-y) = [Y_{y_i}Y_L + Y_{y_i}Y_o + Y_{y_i}Y_r] / \\ [Y_iY_L + y_iY_L + y_oY_i + y_iY_o + y_rY_r] \tag{B-6}$$

where the last term in each bracket will be shown to have a negative sign.

The signs of the various terms may now be determined as previously demonstrated.

The terms in the first four of these tables are identical, so the signs of all the corresponding trees are positive. The last two tables both required one interchange to make them identical, so the trees are negative. All other terms can be shown to be positive, giving the driving-point admittance as

$$Y_{ii} = [y_i(1 + y_oR_L)] / [1 + y_oR_L + y_iR_i \\ (1 + y_oR_L)] \tag{B-7}$$

where both numerator and denominator have been multiplied by R_iR_L and the A factor has been replaced by y_iy_o . If R_i is allowed to go to zero, R_i becomes r_{p_i} , and this equation then reduces to

yY_oY_o			yY_iY_L			yY_oY_o			
1	2	3	1	2	3	1	2	3	
v	y	$-Y_i$	y_o	Y	$-Y_i$	Y_L	y	y_i	y_o
i	y	$-Y_i$	y_o	Y	$-Y_i$	Y_L	Y	y_i	y_o
		(+)			(+)			(+)	
yY_oY_L			yY_iY_r			$Y_{y_i}Y_r$			
1	2	3	1	2	3	1	2	3	
v	y	y_i	Y_L	y	y_r	y_r	Y_i	y_r	y_r
i	y	y_i	Y_L	y	y_r	y_r	Y_i	y_r	y_r
		(+)			(-)			(-)	

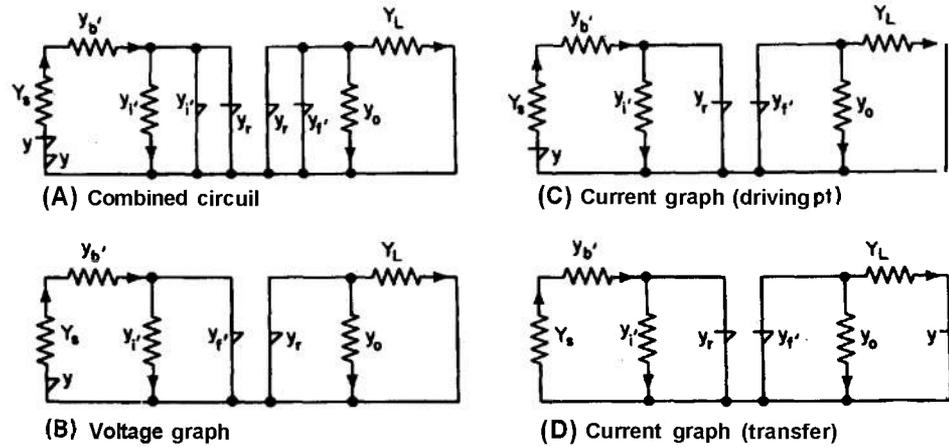


Fig. B-4. For Example B-1

$$Y_i = \frac{[y_v(1 + y_c R_L)]}{(1 + y_c R_L) [1 + y_o R_L + y_v r_v]} \quad (B-8)$$

Reference to Eq. 4-23 shows that this is the equation previously derived.

The principal change required in the derivation of the transfer admittance is the moving of the y element in the current graph to a position in series with Y_L (Fig. B-5(A)). The trees having y as a factor are unchanged for the transfer problem: only the remaining terms are changed. The only one representing a complete tree is

$$y_f Y_i Y_L$$

The polarity of this term is of interest. The data for its determination are given:

	1	$y_f Y_i Y_L$	2	3	
v	Y_i	y_f	Y_L		
i	$-Y_L$	$-Y_i$	y_f		
T_1	y_f	$-Y_i$	$-Y_L$		(-)
T_2	$-Y_i$	y_f	$-Y_L$		(-) ²
S	Y_i	y_f	Y_L		(-) ⁴

thus giving a positive sign for the term.

Fig. B-5(B) shows the graph configuration for the determination of the transfer impedance. The complete trees for this network are

$$y$$

$$-y y_v y_f$$

Other terms:

$$y_v y_i y_o, y_v y_f y_r, Y_i y_i y_o, Y_i y_f y_r$$

The transfer equation, introducing the correct sign, takes the form

$$(-y) = \frac{[1 + y_o R_L + y_v (R_s + r_v)]}{(1 + y_c R_L) [-y_f R_s R_L]} \quad (B-9)$$

The transfer impedance then is

$$(-1/y) = \frac{-y_f R_s R_L}{(R_s + r_v)(1 + y_c R_L)} \quad (B-10)$$

The corresponding transfer admittance is

$$(-y) = y_f / [1 + y_o R_L + y_c (R_s + r_b) (1 + y_o R_L)] \quad (\text{B-11})$$

The only difference other than sign between these equations is the presence of $R_s R_L$ in the numerator of Eq. B-10 and its absence in Eq. B-11.

Significantly, the only negative terms in the driving-point admittance terms or the internal terms of the transfer immittance are those involving the $y_f y_r$ factor. These two graph elements interchange on the current and the voltage graphs, and require an odd number of exchanges to bring them into coincidence. The voltage-gain equation is obtained by multiplying Eq. B-11 by R_r , and the current-gain equation by multiplying Eq. B-10 by Y_L .

EXAMPLE B-2. As a further example of the use of the topological method, the equations for the common-base amplifier may be derived, showing the ease with which the complications otherwise present may be avoided. The complete correct relations for this amplifier are given in Eqs. 4-9, 4-13, 4-14, 4-19, 4-25, 4-26, 4-27, 4-28, and 4-29. The difficulty results in taking account of the effect of base-spreading resistance.

The basic network and the various graphs are shown in Fig. B-6. The complete trees for the input admittance are

y terms:

$$y Y_s y_f y_r, y Y_s y_c y_o, y Y_s y_b y_o, y Y_s y_c Y_L, y y_b y_c y_o, y y_b y_f y_r, y y_b y_f Y_L, y y_b y_o Y_L, y y_c y_o Y_L, y y_f y_r Y_L, y y_b y_c Y_L, y y_b y_r Y_L, y Y_s y_b Y_L$$

Y_s terms:

$$Y_s y_b y_c y_f, Y_s y_b y_c y_o, Y_s y_b y_c Y_L, Y_s y_b y_f Y_L, Y_s y_b y_o Y_L, Y_s y_b y_o Y_L, Y_s y_c y_o Y_L, Y_s y_f y_r Y_L$$

In terms of these trees, the input admittance is

$$Y_{in} = [\sigma(y) + y_c y_o (r_b + R_L)] / [1 + y_o R_L + \sigma(y) R_s + y_c r_b + y_c y_o (r_b R_s + r_b R_L + R_s R_L)] \quad (\text{B-12})$$

and, with $R_s = 0$, it is

$$Y_i = [\sigma(y) + y_c y_o (r_b + R_L)] / [1 + y_o R_L + y_c r_b (1 + y_o R_L)] \quad (\text{B-13})$$

after multiplication by $R_s r_b R_L$. If r_b is taken as zero,

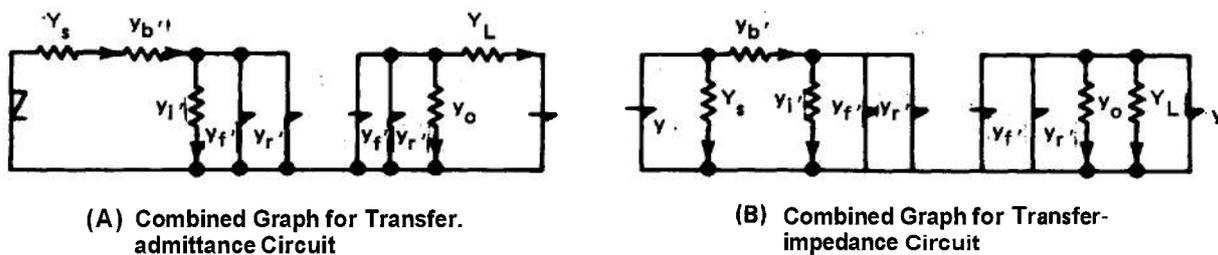


Fig. B-5. Combined Transfer Graph for Example B-1

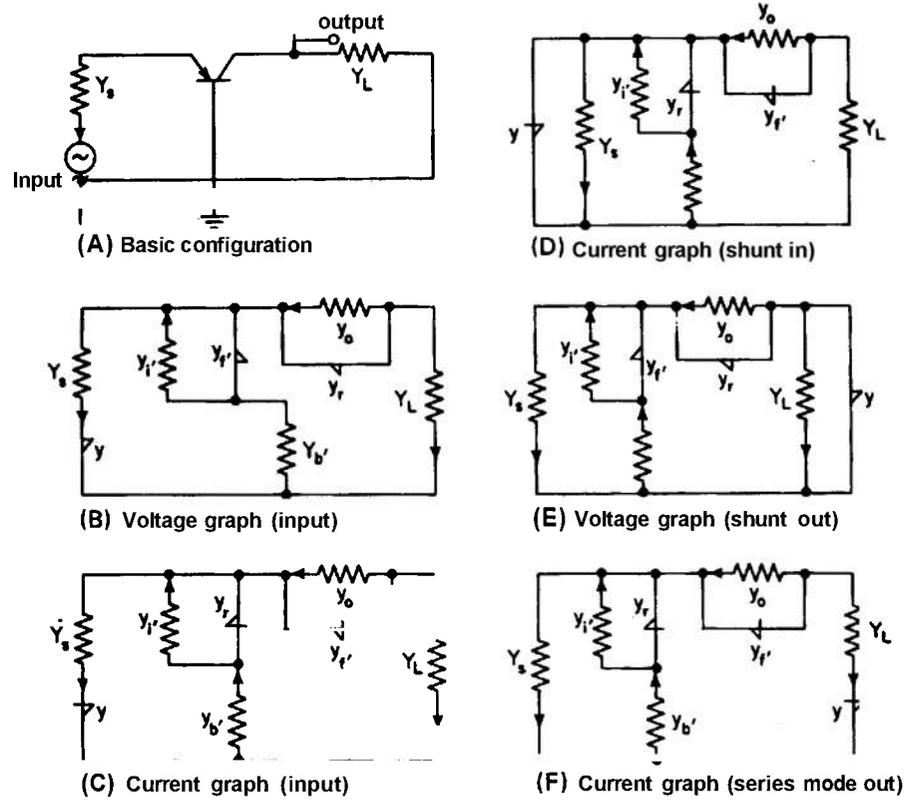


Fig. B-6. For Example B-2

then the equation simplifies to the corresponding form in Chapter 4.

The forward-current gain may be determined by the use of the graphs in Figs. B-6(D) and (E). The complete trees may be tabulated as follows

y terms:

$$y y_b y_r, y y_b y_o, y y_r y_o, y y_r y_r$$

Other terms:

$$Y_s y_b Y_L, y_b y_r Y_L, y_b y_r Y_L, y_b y_r Y_L, \\ y_b y_o Y_L, Y_s y_r Y_L, Y_s y_b y_o, Y_s y_r y_o, Y_s y_r y_r, \\ Y_L y_r y_o, Y_L y_r y_r, y_b y_r y_o, y_b y_r y_r$$

From these trees, the following transfer admittance equation may be formed

$$(1/Z_f) = (-y) = [1 + \sigma(y)R_s + y_r r_b + y_o R_L + y_r y_o (r_b R_L + r_b R_s + R_s R_L)] / [(y_r + y_o) + y_r y_o r_b] \quad (B-14)$$

The resulting equation for current gain is

$$K_i = [(y_r + y_o) + y_r y_o r_b] R_s / [1 + \sigma(y) R_s + y_r r_b + y_o R_L + y_r y_o (r_b R_L + r_b R_s + R_s R_L)] \quad (B-15)$$

The output voltage is divided by the load resistance to convert the output signal to current and give the current gain.

The transfer admittance for the same circuit and its voltage gain may both be established from a corresponding set of complete trees

y terms:

$$\begin{aligned}
 &yY_{y_b y_o}, \quad yY_{y_b Y_L}, \quad yY_{y_i y_o}, \quad yY_{y_i Y_L}, \\
 &-yY_{y_f y_r}, \quad yy_b y_i y_o, \quad -yy_b y_f y_r, \quad yy_i y_b Y_L, \\
 &yy_b y_f Y_L, \quad yy_b y_r Y_L, \quad yy_b y_o Y_L, \quad yy_i y_o Y_L, \\
 &-yy_f y_r Y_L
 \end{aligned}$$

Other terms:

$$Y_{y_b y_f Y_L}, \quad Y_{y_b y_o Y_L}, \quad Y_{y_i y_o Y_L}, \quad -Y_{y_f y_r Y_L}$$

The equations for the transfer admittance and voltage gain resulting from these trees are

$$\begin{aligned}
 (-y) = &[(y_f + y_o) + y_i y_c r_b] / [1 + \sigma(y) \\
 &R_s + y_i r_b + y_o R_L + y_i y_c (r_b R_L \\
 &+ r_b R_s + R_s R_L)] \quad \text{(B-16)}
 \end{aligned}$$

$$\begin{aligned}
 K = &[(y_f + y_o) + y_i y_c r_b] R_L / [1 + \sigma(y) \\
 &R_s + y_i r_b + y_o R_L + y_i y_c (r_b R_L + \\
 &r_b R_s + R_s R_L)] \quad \text{(B-17)}
 \end{aligned}$$

B-3 TREE DETERMINATIONS

One of the critical problems in the use of the topological method is the calculation of the number of trees required in the establishment of one of the immittance expressions. Knowing this number precisely is helpful in that once the specified number of trees is found, the search can be terminated.

The "maximum" number of trees is determined by establishing a determinant having $(v - 1)$ rows and columns, where v is the number of vertices. The diagonal numbers in this determinant give the number of elements, on either the current or the voltage graph, contacting the specified vertex, and the off-diagonal terms are the negatives of the number of elements coupling two vertices directly. In the voltage graph (Fig.

$$T_M = \begin{vmatrix} 2 & -1 & 0 \\ -1 & 3 & 0 \\ 0 & 0 & 3 \end{vmatrix} = 15$$

B-4(B)), for example, the determinant takes the form, where T_M indicates the maximum

This maximum number gives the total number of trees and partial or incomplete trees in the specified network. The minimum number of trees in general may be called T_m , and in particular may be represented as T_i , T_b , T_f , or T_o . This number is the difference in the total positive and total negative trees in the network. The T_i is used to identify the number of trees in the input immittance for the network, the T_b the number in the basic network with the y -factor eliminated, the T_f the number of trees in the transfer immittance for the network, and T_o the number of trees in the output immittance. The difference between T_b and T_f may be either positive or negative, depending on whether or not there is a phase reversal in the transfer immittance. The magnitude of the difference indicates the number of terms in the transfer part of the immittance function if terms involving the A-factor are omitted. Because the A-factor terms include equal numbers of positive and negative trees, they are not counted in the procedures to be described.

The establishment of the minimum number of trees for any network requires first the establishment of the incidence matrices for both the current and the voltage graphs. The incidence matrix for a chosen graph contains $(v - 1)$ rows, one less than the number of vertices, and the one eliminated is usually that having the most connections (the ground). The number of columns in this matrix is equal to the number of elements of the chosen graph, and one column is assigned to each element. After the rows have been assigned numbers corresponding to the vertices of the graph, the identification of the connection pattern is introduced by identifying by plus or minus one the fact that a given admittance contacts a specified vertex, and by zero the fact that it does not. The origin end of the admittance, in accordance with the arrowhead symbol, has the positive unity, and the terminal the negative unity.

After the incidence matrix has been formed, it can be noted that there are at most two nonzero entries in any column, and the number of entries in a given vertex row gives the number of elements incident at the vertex. Because one of the entries on many of the elements may be to the common ground, many columns may have only one entry.

After both the current and the voltage incidence matrices have been formed from a corresponding current and voltage graph, the product of the two may be formed to give the required tree determinant

$$T_m = A_i \times A_v^t \tag{B-18}$$

where A_i is the current incidence matrix, and A_v^t is the transpose of the voltage incidence matrix.* The correct combination of A_i and A_v may be formed for any of the forms of network desired, and the calculation (Eq. B-18) made. Extra terms corresponding to the A-factor terms may be added, and the separation of trees from partial trees started.

The approximate number of terms involving the A-factor may be estimated directly from the graph configuration. In driving-point admittances, there is normally a A-factor term in the numerator if there is a nonzero impedance connected across the port opposite to that at which the admittance is being determined. Likewise, there is a A-factor term in the denominator only if there is an external impedance at the point of measurement and a nonzero terminating impedance on the opposite port. The presence of a return impedance like an emitter-degeneration resistance for a common-emitter amplifier, or base-spreading resistance in the common-base amplifier makes available additional Δ -factor combinations, for example, input-output, input-return, and output-return, which appear in the denominator.

In the transfer function, all the A-factor terms in the denominator of the driving-point admittance are present, and a term may be present in the transfer factor if a return impedance is present, but not otherwise. The sign of the term resulting from a return impedance must be checked, as it may or may not be the same as the balance of the transfer terms.

* If the matrices to be multiplied are

$$A = \begin{pmatrix} a & b \\ c & d \end{pmatrix}, \quad B = \begin{pmatrix} e & f \\ g & h \end{pmatrix}$$

then the product $A \times B^t$ is defined by the equation

$$A \times B^t = \begin{pmatrix} ae + bf & ag + bh \\ ce + df & cg + dh \end{pmatrix}$$

EXAMPLE B-3. Establish the incidence matrices for the transfer admittance condition with the common-emitter amplifier, and determine the minimum number of trees T_f . Also determine the basic number of trees T_b .

The incidence matrices are

$$A_i = \begin{matrix} & y & Y_t & y_{i'} & y_{f'} & y_r & y_o & Y_L \\ \begin{matrix} 1 \\ 2 \\ 3 \end{matrix} & \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & - \\ 0 & -1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 1 & 1 \end{bmatrix} \end{matrix}$$

$$A_v = \begin{matrix} & & & & & & & \\ \begin{matrix} 1 \\ 2 \\ 3 \end{matrix} & \begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 0 & \\ 0 & -1 & 1 & 1 & 0 & 0 & \\ 0 & 0 & 0 & 0 & 1 & 1 & 1 \end{bmatrix} \end{matrix}$$

The product of these matrices gives a determinant in the form

$$T_f = \begin{vmatrix} 1 & 0 & -1 \\ -1 & 2 & 1 \\ 0 & 1 & 2 \end{vmatrix} = 3 + 1 = 4$$

Because the circuit contains both an input and an output resistance, there is one A-factor term in the denominator of the expression, but none in the numerator.

The value of T_b is obtained by deleting the y column from both of the incidence matrices, and recalculating. However, because one of the vertices is eliminated by the removal of the y element, only two rows remain, namely, rows two and three. The tree determinant is

$$T_b = \begin{vmatrix} 2 & 1 \\ 1 & 2 \end{vmatrix} = 3$$

This result shows that the transfer term is positive. The signs of the respective trees may be calculated from the product of incidence matrices by deleting all columns not corresponding to the tree, in both matrices, and then multiplying. If the tree is negative, the matrix has a negative unity value. If it is positive, the matrix value is plus unity, and if the configuration is not a complete tree, the product has the value zero.

In circuits having the general ladder form but considerable complexity, it is possible to build the trees from sections or building blocks. Because the overall combination must possess the properties of a tree, it is

necessary to determine the kind of building blocks that can be used. The principal components for the construction of complex trees include smaller trees, two-trees of at least four types, and three-trees. The types of two-trees are:

1. One-terminal-pair two-trees, that is, networks having a single tree connected to each of the terminals and one connecting branch or element between the trees missing. Each vertex touches at least one tree element, and one tree may consist of a single vertex.

2. Two-terminal-pair (two-port) two-trees, which show two-tree properties at both ports. They are designated by the symbol $2-T$, as are the two-trees in 1.

3. Two-port two-trees having two-tree properties only at the left-hand port. They are designated $2L-T$.

4. Two-port two-trees having two-tree properties at the right-hand port. They are designated as $2R-T$. It is also possible to establish definitions for multi-port two-trees.

The three-tree is similar to the two-tree except that with it the network is separated into three individual trees. This configuration requires a minimum of two ports.

A two-tree or a three-tree has either two or three trees, respectively, as constituent parts, and each vertex of the network forming the two- or three-tree is located on one of the tree components. Null-trees, or isolated vertices, as well as more complex trees may be included in the set.

When a network is separated into sections in the determination of the complete tree set, all possible tree

combinations of each type should be tabulated, and then the sums of the tree configurations of each type determined. For a two-tree, the product representing one term of the sum is the product of the two component trees, and a three-tree the product of the three individual component tree products. Only certain types of configurations may be used together, as otherwise circuits may be developed. Some of the permitted combinations follow:

T	$2-T$		T	$2L-T$	
T	$3-T$	T	$2-T$	$2-T$	T
$2R-T$	T		$2R-T$	$2-T$	T
$2-T$	$2R-T$	T	$2R-T$	$2R-T$	T
$2-T$	T	$2-T$	$2R-T$	T	$2L-T$

The use of network partitioning in determining the overall tree sum is best shown by an example.

EXAMPLE B-4. Use partitioning to determine the complete tree sum function for the three-section ladder network with input admittance shown in Fig. B-7(A). To do this, partition the network as shown in Fig. B-7(B).

The pi section, (1) of this network, can form the three trees shown in Fig. B-7(C), and two two-trees, one of the R variety and the other a standard one-port two-tree. Section (2), the left "ell" section, can form a tree, a pair of two-trees, or a three-trees. Similarly, Sec. (3) can form either a tree or two two-trees. The possible forms for all of these structures are shown in Fig. B-7(D).

The tree combinations that result are tabulated

$$\begin{aligned}
 T_1 \times 2-T_2 \times 2-T_3 &= (Y_1Y_3 + Y_1Y_2 + Y_2Y_3)Y_4Y_6 \\
 T_1 \times 2-T_2 \times 2L-T_3 &= (Y_1Y_3 + Y_1Y_2 + Y_2Y_3)Y_4Y_7 \\
 T_1 \times 2L-T_2 \times 2L-T_3 &= (Y_1Y_3 + Y_1Y_2 + Y_2Y_3)Y_6Y_7 \\
 T_1 \times 2L-T_2 \times 2-T_3 &= (Y_1Y_3 + Y_1Y_2 + Y_2Y_3)Y_6Y_6 \\
 T_1 \times 3-T_2 \times T_3 &= (Y_1Y_3 + Y_1Y_2 + Y_2Y_3)Y_6Y_7 \\
 2-T_1 \times 2-T_2 \times T_3 &= Y_2Y_4Y_6Y_7 \\
 2R-T_1 \times T_2 \times 2-T_3 &= Y_1Y_4Y_6Y_6 \\
 2R-T_1 \times T_2 \times 2L-T_3 &= Y_1Y_4Y_6Y_7 \\
 2R-T_1 \times 2-T_2 \times T_3 &= Y_1Y_4Y_6Y_7 \\
 2-T_1 \times T_2 \times 2-T_3 &= Y_2Y_4Y_6Y_6 \\
 2-T_1 \times T_2 \times 2L-T_3 &= Y_2Y_4Y_6Y_7
 \end{aligned}$$

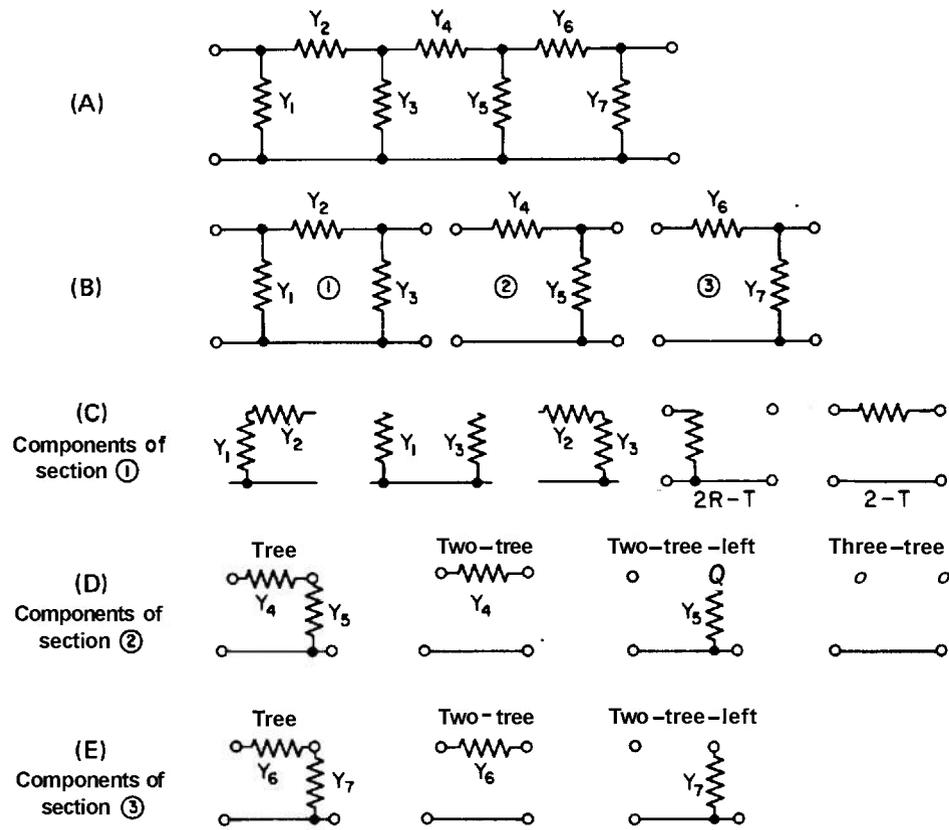


Fig. B-7. Use of Tree Partitioning for Example B-4

APPENDIX C

LEGENDRE AND ORTHOGONAL POLYNOMIALS
PART AUSE OF LEGENDRE AND ORTHOGONAL
POLYNOMIALS

The conversion of either curves or discrete data into a form in which they can express a relation in terms of a relatively small number of expressions is best done in terms of some form of orthogonal functions rather than in terms of a power series. Unless the property of orthogonality is used, an increase of accuracy through the addition of an extra element requires a complete revision of the previous solution. This orthogonality property is the factor that makes Fourier analysis useful, and it likewise is the factor that makes possible rapidly converging solutions with a minimum of work using any of the common polynomials, Legendre, orthogonal, Bessel, Laguerre, Hermite, Jacobi, and others. The discussion in this appendix is limited to the application of Legendre and orthogonal polynomials in the determination of spectral components directly from an input-output relation or an input-amplification relation.

Orthogonal functions have the property that the sum or integral, as applicable, of the products of two different functions of the set has a value zero. A summation, or integral, of the product of the function being represented and one of the polynomials resolve the function into components that are proportional to the components of the representing set. Because it is frequently convenient to expand transfer functions in terms of power series, the following tables permit direct conversion of the series into its corresponding orthogonal representation. An expansion table for functions varying over the range $-1 < x < +1$ and a table for functions having zero value over the range $-1 < x < 0$ follow on succeeding pages.

The diagonal of the matrix of numbers in Table C-1 is a dividing line between diagonal-type rows that are

alternatively zeros and a series of numbers and a series of diagonal rows all of whose numbers are zeros. This is a consequence of the orthogonality relations of the polynomials. All polynomials above zero order are orthogonal with a constant, because the zero-order polynomial is in fact a constant. Similarly, all polynomials above the first are orthogonal with respect to a function that is linear in x , and so on with higher orders.

An example of the usefulness of this set of tables is shown by the development of the polynomial expansion of the function

$$f(x) = (1 + x)/(1 + k + kx) \quad (\text{C-1})$$

If an attempt is made to expand this function directly by integration, the resulting integrals become extremely difficult to handle, since logarithmic terms develop. If, however, the function is first expanded in a power series, the resulting series readily may be handled by Table C-1 unless $|kx| > (1 + k)$. Then the series is a diverging series. Because the maximum value of k is likely to be less than unity, and the range for x is from minus unity to plus unity, the maximum value of the ratio $kx/(1 + k)$ is one-half. The expansion then will converge, and the series takes the form

$$f(x) = [1/(1 + k)] + [1/(1 + k)]^2 x - [k/(1 + k)^2] x^2 + \dots \quad (\text{C-2})$$

From this equation, the following values for the K 's in the coefficient equations, Eqs. C-3 may be determined,

$$\begin{aligned}
 K_2 &= -2k / \langle 3(1+k)^3 \rangle \\
 &\quad - 4k^3 / \langle 7(1+k)^5 \rangle - \dots \\
 K_3 &= 2k^2 / \langle 5(1+k)^4 \rangle + \dots \\
 K_4 &= -8k^3 / \langle 35(1+k)^5 \rangle + \dots
 \end{aligned}
 \tag{C-3}$$

From these equations and the fact that the conversion gain is $0.5K_1$, (Eq. 12-5), the conversion conductance can be determined from the equation for K_1 (Eq. C-3). Evidently, the larger the value of k , the degeneration, the lower the conversion conductance, because the correction terms make a maximum of 20% increase, whereas the $1/(1+k)^2$ multiplier reduces the conductance by as much as a factor of four.

Table C-2 may be used for the reconstruction of Table C-1, in which case the terms whose sum of order and exponent is odd are zero, and even are nonzero, or it may be used for the construction of a table in which the sign of the function in the negative range is positive also. Then the terms for which the sum of order and exponent is even are zero-valued, and the value of the odd order twice that given in Table C-2. The coefficients for a Legendre expansion of a given continuous function $f(x)$ over any selected interval may be found from the equation

$$C_n = [(2n + 1)/2] \int_{-1}^1 f(x)P_n(x)dx \tag{C-4}$$

where the interval over which $f(x)$ is nonzero may extend from -1 to $+1$, or the function may be zero over part of the range. The coefficients in the two tables were determined by the use of this equation.

The expressions for each of the polynomials $P_n(x)$ may be substituted, one at a time, in Eq. C-4, along with the function $f(x)$ and the appropriate value of n to determine the multiplying factor to be used in representing a given function. The first few polynomials are

$$\begin{aligned}
 P_0(x) &= 1, & P_1 &= x, \\
 P_2(x) &= 0.5(3x^2 - 1) \\
 P_3(x) &= 0.5(5x^3 - 3x), \\
 P_4(x) &= 0.125(35x^4 - 30x^2 + 3) \\
 P_5(x) &= 0.125(63x^5 - 70x^3 + 15x) \\
 P_6(x) &= 0.0625(231x^6 - 315x^4 \\
 &\quad + 105x^2 - 5) \\
 P_7(x) &= 0.0625(429x^7 - 693x^5 \\
 &\quad + 315x^3 - 352) \\
 P_8(x) &= 0.0078125(6435x^8 - 12012x^6 \\
 &\quad + 6930x^4 - 1260x^2 + 35)
 \end{aligned}
 \tag{C-5}$$

In these equations, it should be remembered that x may be replaced by its equivalent $x = \cos \theta$ to give the

TABLE C-1
EXPANSIONS FOR COMPLETE FUNCTIONS

Ord/Exp	0	1	2	3	4	5	6
0	1.00	0	1/3	0	1/5	0	1/7
1	0	1.00	0	3/5	0	3/7	0
2	0	0	2/3	0	4/7	0	10/21
3	0	0	0	2/5	0	4/9	0
4	0	0	0	0	8/35	0	24/77
5	0	0	0	0	0	8/63	0
6	0	0	0	0	0	0	16/231

TABLE C-2
EXPANSIONS FOR ONE-SIDED FUNCTIONS

Ord/Exp	0	1	2	3	4	6	6
0	1/2	1/4	1/6	1/8	1/10	1/12	1/14
1	3/4	1/2	3/8	3/10	1/4	3/14	3/16
2	0	5/16	1/3	5/16	2/7	25/96	5/21
3	-7/16	0	7/48	1/5	7/32	2/9	3/16
4	0	-3/32	0	9/128	4/35	9/64	12/77
5	11/32	0	-11/384	0	11/320	4/63	11/128
6	0	13/256	0	-13/1280	0	13/768	8/231

equations as a trigonometric multiangle series, and they can also be written as power series if desired. The multiangle (Chebycheff-form) equations are

$$\begin{aligned}
 P_0(\theta) &= 1, & P_1(\theta) &= \cos \theta, \\
 P_2(\theta) &= 0.25(3 \cos 2\theta + 1) \\
 P_3(\theta) &= 0.125(5 \cos 3\theta + 3 \cos \theta) \\
 P_4(\theta) &= 0.015625(35 \cos 4\theta \\
 &\quad + 20 \cos 2\theta + 9) \\
 P_5(\theta) &= 0.0078125(63 \cos 5\theta \\
 &\quad + 35 \cos 3\theta + 30 \cos \theta) \\
 P_6(\theta) &= 0.001953125(231 \cos 6\theta \\
 &\quad + 126 \cos 4\theta + 105 \cos 2\theta + 50) \\
 P_7(\theta) &= 0.0009765625(429 \cos 7\theta \\
 &\quad + 231 \cos 5\theta + 175 \cos 3\theta \\
 &\quad + 189 \cos \theta) \\
 P_8(\theta) &= 0.00006103525625(6435 \cos 8\theta \\
 &\quad + 3432 \cos 6\theta + 2772 \cos 4\theta \\
 &\quad + 2520 \cos 2\theta + 1225)
 \end{aligned}
 \tag{C-6}$$

The decimals may be rounded off as desired, because not more than three significant figures should be required in normal applications.

These values for the successive polynomials in terms of $n\theta$ may be substituted for the polynomial form, giving the unknown function in terms of the polynomials. The resulting equation gives the amplification of the respective harmonics in terms of the coefficients. The coefficients may be arranged in terms of either the amplification function or the output function to give

the harmonic amplitudes. In addition, conversion equations may be written in a form to convert from one set of coefficients to the other. These various sets are

Basic output function form:

$$\begin{aligned}
 E_0 &= C_{e0} + C_{e2}/4 + 9C_{e4}/64 + 50C_{e6}/512 \\
 &\quad + 1225C_{e8}/16,384 \\
 E_1 &= C_{e1} + 3C_{e3}/8 + 15C_{e5}/64 \\
 &\quad + 175C_{e7}/1024 \\
 E_2 &= 3C_{e2}/4 + 5C_{e4}/16 + 105C_{e6}/512 \\
 &\quad + 2520C_{e8}/16,384 \\
 E_3 &= 5C_{e3}/8 + 35C_{e5}/128 + 189C_{e7}/1024 \\
 E_4 &= 35C_{e4}/64 + 63C_{e6}/256 + 693C_{e8}/4096 \\
 E_5 &= 63C_{e5}/128 + 231C_{e7}/1024
 \end{aligned}
 \tag{C-7}$$

Derived gain form:

$$\begin{aligned}
 K_0 &= C_{e1} + 9C_{e3}/4 + 225C_{e5}/64 \\
 &\quad + 1225C_{e7}/256 \\
 K_1 &= 3C_{e2} + 45C_{e4}/8 + 525C_{e6}/64 \\
 K_2 &= 15C_{e3}/4 + 105C_{e5}/16 + 4725C_{e7}/512 \\
 K_3 &= 35C_{e4}/8 + 945C_{e6}/128 \\
 &\quad + 10395C_{e8}/1024 \\
 K_4 &= 315C_{e5}/64 + 2079C_{e7}/256 \\
 K_5 &= 693C_{e6}/128 + 9009C_{e8}/1024
 \end{aligned}
 \tag{C-8}$$

The corresponding equations based on the input-gain relation are

Basic gain form:

$$\begin{aligned}
 K_0 &= C_{k0} + C_{k2}/4 + 9C_{k4}/64 + 25C_{k6}/256 \\
 &\quad + 1225C_{k8}/16,384 \\
 K_1 &= C_{k1} + 3C_{k3}/8 + 15C_{k5}/64 \\
 &\quad + 175C_{k7}/1024 \\
 K_2 &= 3C_{k2}/4 + 5C_{k4}/16 + 105C_{k6}/512 \\
 &\quad + 315C_{k8}/2048 \\
 K_3 &= 5C_{k3}/8 + 35C_{k5}/128 + 189C_{k7}/1024 \\
 K_4 &= 35C_{k4}/64 + 63C_{k6}/256 \\
 &\quad + 693C_{k8}/4096 \\
 K_5 &= 63C_{k5}/128 + 231C_{k7}/1024
 \end{aligned} \tag{C-9}$$

The corresponding derived input-output relation is

$$\begin{aligned}
 E_{k1} &= C_{k0} - C_{k2}/8 - C_{k4}/64 - 5C_{k6}/1024 \\
 &\quad - 35C_{k8}/16,384 \\
 E_{k2} &= C_{k1}/4 - C_{k3}/16 - 5C_{k5}/512 \\
 E_{k3} &= C_{k2}/8 - 5C_{k4}/128 - 7C_{k6}/1024 \\
 &\quad - 7C_{k7}/2048 \\
 E_{k4} &= 5C_{k3}/64 - 7C_{k5}/256 - 21C_{k7}/4096 \\
 &\quad - 21C_{k8}/8192 \\
 E_{k5} &= 7C_{k4}/128 - 21C_{k6}/1024 - 33C_{k8}/8192 \\
 E_{k6} &= 21C_{k5}/512 - 33C_{k7}/2048
 \end{aligned} \tag{C-10}$$

Orthogonal polynomials are used instead of the Legendre form when the data are known at equally-spaced discrete points. These polynomials are closely related to the Legendre polynomials, and can be manipulated by identical procedures with the exception that the integration is replaced by a Summation. Polynomials based on discrete data are of particular use with active devices because of the form in which their characteristic curve data are provided.

The equations for evaluation of the coefficients may be given in terms of summations, or they may be expressed in terms of matrix products. The parallelism

with the evaluation for Legendre polynomials is best shown in terms of the summations, but actual calculations are best made in terms of matrix representation. The summation form of the coefficients are

$$\begin{aligned}
 C_{kn} &= | P_n(0) | \sum_{h=0}^K K(h)P_n(h) / \sum_{h=0}^K [P_n(h)]^2 \\
 C_{en} &= | P_n(0) | \sum_{h=0}^K E(h)P_n(h) / \sum_{h=0}^K [P_n(h)]^2
 \end{aligned} \tag{C-11}$$

The first term on the right-hand side of each of these equations is required to give a dimensionally correct value for the coefficient. With it present the coefficient is dimensionally identical with the function being represented.

When the raw data give the functional behavior in terms of an input-output relation, then the second equation of Eqs. C-11 is used for determining the coefficients. The equations based on the basic output function are used for the input-output analysis, and the derived-gain equations for the gain and admittance. When the data are given in terms of the input-amplification relation, then the first of Eqs. C-11 is used for the coefficients, and the basic gain and derived output form of the equations are used.

The Conversion of the Gain-form of the Coefficients into the Equivalent Admittance or Impedance

To determine the admittance components, for example, the input variable is taken as input voltage, and it is rescaled to have a range from -1 to $+1$; the output variable is then taken as output current. The "amplification" is determined with Eqs. C-11, and it gives the magnitude of the current in terms of the arbitrary input scale of plus or minus one. If, therefore, the current magnitudes determined from Eqs. C-7 through C-10 are given in amperes, and the values are divided by the voltage increment corresponding to the voltage interval from zero to either plus or minus unity, the quotients are admittances. The equations typically take the form

$$y_j = E_j/\delta v \tag{C-12}$$

where δv is half the difference of the voltages v_p and

v_n . If the output variable is selected as a voltage, then a voltage gain results. An impedance or a current gain may be determined by the use of a current as the input variable.

In Eqs. C-11 for the coefficients, the value of the denominator is always known once the number of data points is known and the order of n is selected. Consequently, the value of the denominator summation may be called S_j , and its value is included in the listings of the tabular values for the orthogonal polynomial $P_n(h)$. Also, the following relation can be given for the extreme values $P_n(0)$ and $P_n(k)$, where $k + 1$ is the total number of data points used in the summation

$$|P_n(0)| = |P_n(k)| \tag{C-13}$$

The tabular values of the discrete polynomials differ from Legendre polynomials in two significant ways, first in that the numbers are tabulated as integers rather than as decimals, and second that the endpoint values may not have a magnitude greater than all interior points, as is the case with the Legendre polynomials. For large numbers of data points and small polynomial order, the end values may have the greatest magnitude, however, as the polynomials then have characteristics closely approaching those of the Legendre polynomials. The development of orthogonal polynomials is clearly explained in Ref. 1.

The matrix procedure for calculation of the basic coefficients for use in the equations for the component amplitudes is based on Eqs. C-11. In the following matrix equation, the order of the individual matrices is indicated under each matrix, and those which are diagonal in form (all elements of $[a_{ij}]$ for which $i \neq j$ are identically zero) are identified by a D placed above the matrix. The equation is

$$\begin{matrix} D \\ [S_j] \end{matrix} \times \begin{matrix} D \\ [C_j] \end{matrix} = \begin{matrix} D \\ [P_j(0)] \end{matrix} \times \begin{matrix} D \\ [P_j^t(x)] \end{matrix} \times \begin{matrix} D \\ [f(x)] \end{matrix} \tag{C-14}$$

$\begin{matrix} m \times m & m \times 1 & m \times m & m \times (2n+1) & (2n+1) \times 1 \end{matrix}$

Because the matrix $[S_j]$ is nonsingular, the equation may be solved for $[C_j]$ to give

$$[C_j] = [S_j]^{-1} \times [P_j(0)] \times [P_j^t(x)] \times [f(x)] \tag{C-15}$$

The second and third matrices on the right-hand side of the equation may be combined into one matrix, thereby simplifying the calculation. Whereas the tabu-

lations of these polynomials usually are based on $P_j(h)$, the tables of values herein are those of the product of $|P_j(0)|$ and $P_j(h)$, and they are identified by the symbol $R_j(h)$. The resulting matrix equation is

$$[C_j] = [S_j]^{-1} \times [R_j^t(h)] \times [f(h)] \tag{C-16}$$

$\begin{matrix} m \times 1 & m \times m & m \times (2n+1) & (2n+1) \times 1 \end{matrix}$

where $[S_j]^{-1}$, because of its diagonal form, may be written in either form

$$[S_j]^{-1} = [1/S_j] \tag{C-17}$$

The tables of polynomial numbers listed in this appendix give the values of R_j^t and S_j , where the variable j gives the order of the polynomial and indicates the number of the row in R_j^t , and the h , which ranges from 0 to k , identifies the specific point at which a given measurement was made. The columns of R_j^t correspond to the respective data points.

For the benefit of the reader who is unfamiliar with the process of matrix multiplication, the following example is included. When the matrices a_{ij} and b_{jk} are to be multiplied, the first step is to be sure that they are arranged to place the common index (in this example, j) on the left matrix so that it specifies the columns, and on the right matrix so that it identifies the rows. The number of columns of the left matrix must equal the number of rows of the right matrix. Then successive pairs of numbers, the one taken consecutively across the desired row of the left matrix and the other taken consecutively down a selected column of the right matrix, are multiplied, and the sums added. If these matrices are

$$a_{ij} = \begin{bmatrix} a_{11} & a_{12} & a_{13} & a_{14} \\ a_{21} & a_{22} & a_{23} & a_{24} \end{bmatrix} b_{jk} = \begin{bmatrix} b_{11} & b_{12} & b_{13} \\ b_{21} & b_{22} & b_{23} \\ b_{31} & b_{32} & b_{33} \\ b_{41} & b_{42} & b_{43} \end{bmatrix} \tag{C-18}$$

then the product is given by terms in the form

$$a_{i1}b_{1k} + a_{i2}b_{2k} + a_{i3}b_{3k} + \dots \tag{C-19}$$

In this matrix made from terms of the form (Eq. C-19),

the possible values for i are 1 and 2, and those for k are 1, 2, and 3. The final matrix has two rows and three columns, and the four-by-four dimensions on the component matrices have disappeared into the summations. Such a product summation may readily be prepared on a desk calculator.

As an example of the use of these procedures, the

V_b, mv	100	110	120	130	140	150	160	170	180
$I_b, \mu\text{A}$	10	20	35	55	80	110	145	185	230

The nominal static point may be selected at 140 mV and 80 μA , and the exact average currents for different ranges of base voltage, 120 to 160, 110 to 170, and 100

average current flow and the components of current change may be determined, and the corresponding admittance components evaluated.

A circuit is required to provide an average current of 90 μA , and the following values of current flow, as a result of equal increments of applied voltage

to 180, may be determined by the use of Tables C-6, C-7, and C-8. The calculations for the range 110 to 170 mV are

$$\begin{bmatrix} C_{e0} \\ C_{e1} \\ C_{e2} \\ C_{e3} \\ C_{e4} \\ C_{e5} \end{bmatrix} = \begin{bmatrix} 3 \\ \frac{1}{8} \\ \frac{1}{84} \\ 6 \\ \frac{1}{84} \\ \frac{1}{84} \end{bmatrix} \times \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 9 & 6 & 3 & 0 & -3 & -6 & -9 \\ 25 & 0 & -15 & -20 & -15 & 0 & 25 \\ 1 & -1 & -1 & 0 & 1 & 1 & -1 \\ 9 & -21 & 3 & 18 & 3 & -21 & 9 \\ 1 & -4 & 5 & 0 & -5 & 4 & -1 \end{bmatrix}$$

$$\times \begin{bmatrix} 20 \\ 35 \\ 55 \\ 80 \\ 110 \\ 145 \\ 185 \end{bmatrix}$$

$$= \begin{bmatrix} \frac{1}{7} \\ \frac{1}{8} \\ \frac{1}{84} \\ 6 \\ \frac{1}{84} \\ \frac{1}{84} \end{bmatrix} \times \begin{bmatrix} 630 \\ -2310 \\ 1050 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 90 \\ -82.5 \\ 12.5 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

The values of C_{e3} , C_{e4} , and C_{e5} all are zero for all of the sets of data as a result of the square-law relation selected for the input-output ratio. The values of the

various important parameters and coefficients may be tabulated as follows

ΔV_b	40	60	80	
C_{a0}	85	90	96.4	
C_{a1}	55	82.5	110	
C_{a2}	5.0	12.5	26.3	
I_a	86.25	93.1	103.0	(C-21)
G_0	2750	2750	2750	
G_1	750	1250	1977	
$0.5\Delta V_b$	20	30	40	

Evidently, the corrections can be important on all of the values. The conductance values are in micromhos, and the average current I_a is in microamperes. A little practice in conjunction with either a desk calculator or a slide rule and the user can make calculations such as these in much less time than is required to measure the corresponding results.

The tables of values for $R_j^t(h)$ and S_j follow.

TABLE C-3
 $R_j^t(h); 2n + 1 = 4$

h	0	1	2	3
$j = 0$	1	1	1	1
1	9	3	-3	-9
2	1	-1	-1	1
3	1	-3	3	-1

$j =$		S_j		
	0	1	2	3
0	4			
1		20		
2			4	
3				20

TABLE C-4
 $R_j^t(h); 2n + 1 = 5$

h	0	1	2	3	4
$j = 0$	1	1	1	1	1
1	2	1	0	-1	-2
2	2	-1	-2	-1	2
3	1	-2	0	2	-1
4	1	-4	6	-4	1

$j =$		S_j			
	0	1	2	3	4
0	5				
1		5			
2			7		
3				10	
4					10

TABLE C-5
 $R_j^t(h); 2n + 1 = 6$

h	0	1	2	3	4	5
$j = 0$	1	1	1	1	1	1
1	5	3	1	-1	-3	-5
2	25	-5	-20	-20	-5	25
3	5	-7	-4	4	7	-5
4	1	-3	2	2	-3	1
5	1	-5	10	-10	5	-1

$j =$		S_j				
	0	1	2	3	4	5
0	6					
1		14				
2			84			
3				90		
4					28	
5						252

TABLE C-6
 $R_j^t(h); 2n + 1 = 7$

h	0	1	2	3	4	5	6
$j = 0$	1	1	1	1	1	1	1
1	9	6	3	0	-3	-6	-9
2	25	0	-15	-20	-15	0	25
3	1	-1	-1	0	1	1	-1
4	9	-21	3	18	3	-21	9
5	1	-4	5	0	-5	4	-1

$j =$		S_j				
	0	1	2	3	4	5
0	7					
1		28				
2			84			
3				6		
4					154	
5						84

TABLE C-7
 $R_j^t(h); 2n + 1 = 8$

h	0	1	2	3	4	5	6	7
$j = 0$	1	1	1	1	1	1	1	1
1	7	5	3	1	-1	-3	-5	-7
2	7	1	-3	-5	-5	-3	1	7
3	49	-35	-49	-21	21	49	35	-49
4	7	-13	-3	9	9	-3	-13	7
5	7	-23	17	15	-15	-17	23	-7

$j =$		S_j				
	0	1	2	3	4	5
0	8					
1		24				
2			24			
3				264		
4					88	
5						312

TABLE C-8
 $R_j^t(h); 2n + 1 = 9$

h	0	1	2	3	4	5	6	7	8
$j = 0$	1	1	1	1	1	1	1	1	1
1	4	3	2	1	0	-1	-2	-3	-4
2	28	7	-8	-17	-20	-17	-8	7	28
3	98	-49	-91	-63	0	63	91	49	-98
4	14	-21	-11	9	18	9	-11	-21	14
5	4	-11	4	9	0	-9	-4	11	-4

$j =$	0	1	2	3	4	5
0	9					
1		15				
2			99			
3				495		
4					143	
5						117

TABLE C-9
 $R_j^t(h); 2n + 1 = 10$

h	0	1	2	3	4	5	6	7	8	9
$j = 0$	1	1	1	1	1	1	1	1	1	1
1	27	21	15	9	3	-3	-9	-15	-21	-27
2	6	2	-1	-3	-4	-4	-3	-1	2	6
3	294	-98	-245	-217	-84	84	217	245	98	-294
4	162	-198	-153	27	162	162	27	-153	-198	162
5	6	-14	1	11	6	-6	-11	-1	14	-6

$j =$	0	1	2	3	4	5
0	10					
1		110				
2			22			
3				1430		
4					1430	
5						130

In the remaining tables, only even values of n are used, and only half of the table is presented. The balance of the table is symmetrical or anti-symmetrical with respect to the part listed, symmetry being indicated by the letter S, and anti-symmetry by A S. Each additional term is the negative of the corresponding listed term when the symbol is A S. With the symbol

S the signs are the same. For example, in Table C-10, the series of numbers for $j = 2$ are 75, 25, -5, -30, -45, -50, and, completing the series, -45, -30, -5, 25, and 75. Those for $j = 3$ are 30, -6, -22, -23, -14, 0, and 14, 23, 22, 6, and -30 for the additional terms.

TABLES OF ORTHOGONAL
POLYNOMIALS

TABLE C-10
 $R_j^t(h); 2n + 1 = 11$

h	0	1	2	3	4	5	Sym.
$j = 0$	1	1	1	1	1	1	S
1	5	4	3	2	1	0	AS
2	75	30	-5	-30	-45	-50	S
3	30	-6	-22	-23	-14	0	AS
4	18	-18	-18	-3	12	18	S
5	3	-6	-1	4	4	0	AS

$j =$	0	1	2	3	4	5
0	11					
1		22				
2			286			
3				143		
4					143	
5						52

TABLE C-11
 $R_j^t(h); 2n + 1 = 13$

h	0	1	2	3	4	5	6	Sym.
$j = 0$	1	1	1	1	1	1	1	S
1	18	15	12	9	6	3	0	AS
2	22	11	2	-5	-10	-13	-14	S
3	11	0	-6	-8	-7	-4	0	AS
4	891	-594	-864	-486	99	576	756	S
5	242	-363	-198	121	286	220	0	AS

$j =$	0	1	2	3	4	5
0	13					
1		91				
2			91			
3				52		
4					6188	
5						3094

TABLE C-12
 $R_j^t(h); 2n + 1 = 15$

h	0	1	2	3	4	5	6	7	Sym.
$j = 0$	1	1	1	1	1	1	1	1	S
1	7	6	5	4	3	2	1	0	AS
2	91	52	19	-8	-29	-44	-53	-56	S
3	637	91	-245	-406	-427	-343	-189	0	AS
4	1,001	-429	-869	-704	-249	251	621	756	S
5	11,011	-12,584	-10,769	-484	8251	11,000	7425	0	AS

$j =$	0	1	2	3	4	5
0	15					
1		40				
2			408			
3				3,060		
4					6,460	
5						116,280

TABLE C-13
 $R_j^t(h); 2n + 1 = 17$

h	0	1	2	3	4	5	6	7	8	Sym.
j = 0	1	1	1	1	1	1	1	1	1	S
1	8	7	6	5	4	3	2	1	0	AS
2	400	250	120	10	-80	-150	-200	-230	-240	S
3	196	49	-49	-105	-126	-119	-91	-49	0	AS
4	676	-169	-507	-507	-312	-39	221	403	468	S
5	1,352	-1,183	-1,352	-507	468	1,079	1,144	715	0	AS

j =	0	1	2	3	4	5
0	17					
1		51				
2			1,938			
3				969		
4					1,292	
5						12,597

TABLE C-14
 $R_j^t(h); 2n + 1 = 19$

h	0	1	2	3	4	5	6	7	8	9	Sym.
j = 0	1	1	1	1	1	1	1	1	1	1	S
1	27	24	21	18	15	12	9	6	3	0	AS
2	51	34	19	6	-5	-14	-21	-26	-29	-30	S
3	408	136	-56	-178	-240	-252	-224	-166	-88	0	AS
4	5,508	-612	-3,492	-4,077	-3,186	-1,512	378	2,043	3,168	3,564	S
5	102	-68	-98	-58	3	54	79	74	44	0	AS

j =	0	1	2	3	4	5
0	19					
1		190				
2			266			
3				2,090		
4					33,649	
5						874

TABLE C-15
 $R_j^t(h); 2n + 1 = 21$

h	0	1	2	3	4	5	6	7	8	9	10	Sym.
j = 0	1	1	1	1	1	1	1	1	1	1	1	S
1	10	9	8	7	6	5	4	3	2	1	0	AS
2	18,050	12,635	7,790	3,515	-190	-3,325	-5,890	-7,885	-9,310	-10,165	-10,450	S
3	285	114	-12	-98	-149	-170	-166	-142	-103	-54	0	AS
4	49,419	0	-26,010	-34,680	-31,365	-20,706	-6,630	7,650	19,635	27,540	30,294	S
5	65,892	-32,946	-58,956	-44,506	-13,396	18,071	40,018	47,923	41,548	23,868	0	AS

j =	0	1	2	3	4	5
0	21					
1		77				
2			100,947			
3				1,518		
4					301,070	
5						533,715

PART B TRAPEZOIDAL CORRECTIONS

In theory one might expect the Legendre and the orthogonal procedures to yield identical results, and in fact when the value of n is sufficiently large, they do converge to common values. Because electronic problems often take a form that makes available only a limited group of data this convergence cannot be assured, and it is convenient to be able to estimate the corrections for the various coefficients to give the results as determined on the basis of Legendre polynomials with continuous data.

The results obtained using the orthogonal values based on the tables included in Part A, Appendix C, often give results that are good enough for routine applications. In fact, error only shows up conclusively when an attempt is made to fit data calculated on the basis of a specified relation known in closed form to an orthogonally equivalent solution. Separate correction is required for the even-order terms and for the odd-order terms because of the way the odd-order coefficients zero out in the calculation of an even-order coefficient, and vice versa.

The correction multipliers may be set up in a matrix form and used to correct the coefficients to those of the corresponding Legendre coefficients. This matrix is useful because of the triangular form of its entries. The coefficients take the form shown in Table C-16. Similar coefficients for correction of exponents of five and greater may be prepared. For example, the order five-exponent-five coefficient is

$$C_{5c} = \frac{4n^4 C_5}{(2n-1)(2n-3)(n-1)(n-2)} \tag{C-20}$$

The proper means of analysis for the determination of the respective coefficients is to introduce a power-series with arbitrary coefficients, both in closed form and numerically, and determine from the resulting expressions the correct conversion equations for correcting the terms. The coefficients should convert the numerical values to the forms given in Table C-1.

**TABLE C-16
COEFFICIENT CORRECTION TABLE**

Ord/Exp	0	1	2	3	4
0	C_0	0	$\frac{[f(q) + nC_0]}{(n+1)}$	0	$f(q) + \frac{nC_2}{2n-1} + \frac{C_4[108n^4 - 594n^3 - 1540n^2 - 1985n - 930]}{2(n-1)^2(2n-3)(n-1)}$
1	0	C_1	0	$C_1 - \left[\frac{C_3(3n-1)}{(2n-1)(n-1)} \right]$	0
2	0	0	$\frac{2n^2 C_2}{(2n-1)}$	0	$\frac{2nC_2}{(2n-1)} - \frac{5C_4}{3} \left[\frac{180n^3 + 308n^2 + 397n + 186}{(2n-1)(n-1)} \right]$
3	0	0	0	$\frac{2n^3 C_3}{(2n-1)(n-1)}$	0
4	0	0	0	0	$\frac{4n^3 C_4}{(n-1)(2n-3)(n-1)}$

PART C

ELLIPTICAL LOAD LINES

Orthogonal analysis techniques may also be used in the evaluation of the circuit properties of a transistor-reactive-load operating combination. The principal requirement that must be fulfilled by the circuit for the technique to be described to apply is that the load contour have what may be called central symmetry, i.e., on each radial through the center, or static Q-point, the displacement to one side of the center is exactly equal to the displacement to the other side of the center.

The first step in the analysis of an elliptic contour is to tabulate the current and voltage data at the successive base-current contours, and to make an orthogonal analysis of one of the two sections of the contour from one bias limit to the other limit. The result will be expressed in terms of a complete set of coefficients of order zero, one, two, three, up through some number commonly five. The odd coefficients represent the in-phase components of the relation, and may be kept unchanged. The even coefficients are re-assembled into a curved contour like the original one, except that a new central plotting point is selected at one of the extremities. This process is indicated graphically in Figs. C-1 through C-4. Fig. C-1 shows the original contour with the bias curves superimposed. Fig. C-2 shows the result of replotting the curve as a function of bias current, and also shows the position of the contour formed by the odd-order components. Replotting in effect reconstitutes the contour by plotting differences from the odd-order contour, thereby bending it down to the horizontal axis. The differences are plotted above and below this contour as the axis. The even-order contour resulting has altered limits, since the Q-point on one side is taken as one limit, that on the other side as the second limit, and the point of intersection of the even-contour with the axis is taken as the new Q-point. The replotted curve is shown in Fig. C-3.

The scale used for plotting this contour may now be altered to provide the correct quadrature relation (Fig. C-4). The scale selected for the replotting must be one which will give proper emphasis to the respective values, so that the final curve will properly fit the available data. The process is explained in some detail in Ref. 2, Chapter 12.

The relation among the various data points for the symmetric and the asymmetric portions of the contour may readily be expressed in terms of arc-trigonometric

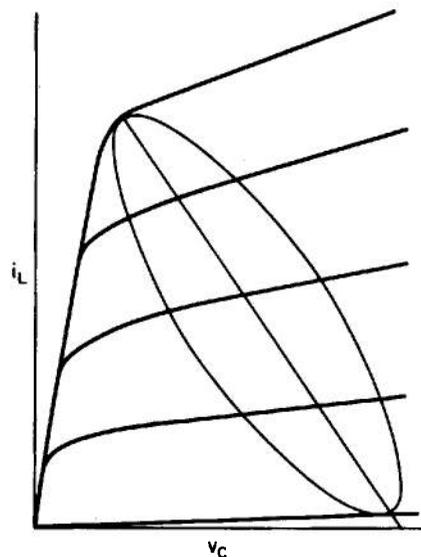


Fig. C-1. Basic Elliptic Contour

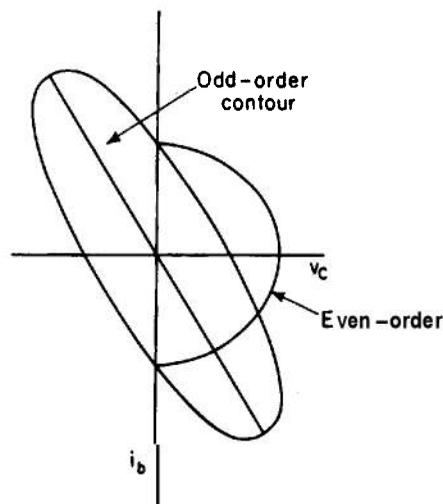


Fig. C-2. Replotted Contour

TABLE C-17
DIRECT AND QUADRATURE
ANGLE RELATIONS

Direct		Quadrature	
Angle	Bias Increment	Angle	Bias Increment
Arcsin 0	0	Arccos 0	$n\Delta i$
Arcsin 1/n	Δi	Arccos 1/n	$\Delta i\sqrt{n^2 - 1}$
Arcsin 2/n	$2\Delta i$	Arccos 2/n	$\Delta i\sqrt{n^2 - 4}$
Arcsin 3/n	$3\Delta i$	Arccos 3/n	$\Delta i\sqrt{n^2 - 9}$
etc.		etc.	
Arcsin 1	$n\Delta i$	Arccos 1	0

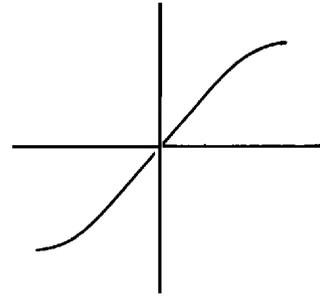


Fig. C-4. Replotted and Rescaled Even Contour

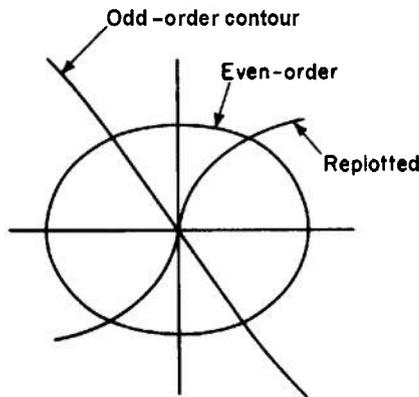


Fig. C-3. Separated Contours

relations. In effect, the symmetric or in-phase portion uses points linearly spaced in terms of the base-current spacing, and the asymmetric portion in terms of the complementary arc-function. The data points are associated in terms of Table C-17. In this table, $n\Delta i$ is the total magnitude of the bias excursion either side of the Q-point.

These direct and quadrature coefficients are independently combined to give the magnitudes of the direct and the quadrature components of each harmonic in accordance with Eqs. C-7. The harmonic-time multiplier for the direct components take the form $\cos kwt$, where k is the harmonic order, and $\cos (kwt + 90^\circ)$ for the quadrature components.

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APPENDIX D

BIBLIOGRAPHY

The bibliography that follows in this appendix lists a large number of the references consulted in the process of preparing this handbook. In general, only the title, author, and source are given, but for some articles or references considered to contain particularly important material bearing on the development of this book, brief notes on the contents have been included. This list is by no means all-inclusive, but it may prove helpful to the reader.

The list is divided into some sixteen different categories to facilitate locating different items, and is further subdivided alphabetically according to authors. The individual topics are:

1. Diode technology
2. Semiconductor technology
3. Transistor technology
4. Transistor characteristics
5. General circuits
6. Stabilization
7. DC amplifiers

8. AC amplifiers
9. Tuned amplifiers
10. Transistor oscillators
11. Transistorized regulated power supplies
12. Transistorized computing circuits
13. Transistor pulse circuits
14. Transistor noise
15. Transistor circuits
16. General nonlinear elements

Detailed reference has been made to these sources as required, and only brief reference where little direct use has been made of the material.

The following list includes some of the books that may prove useful to the reader for correlative reading. With the exception of *Conductance Design of Active Circuits*, none of them consider transistor circuit design on a coordinated basis, but they contain much useful basic data on the devices or on semiconductor physics:

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APPENDIX E

A DISCUSSION OF AVAILABLE EXTENDED DATA

The data provided by some manufacturers on their transistor devices are of an excellence that makes worthwhile a detailed examination of their form and also a comparison against representing equations. The curve data on two transistors typical of advanced presentation are described in this appendix, and their form compared to the equations derived by Regis and Lake (Ref. 1). The transistor curves in question have been extracted from *Valvo Handbuch*, Halbleiter, 1960. Any one of a number of other foreign or American device manufacturers might equally well have been selected.

The transistors in question are the **OC30** and the **OC170**, the former presenting an excellent example of static data for low-frequency operation, and the latter an outstanding example of data for high-frequency operation. The tabular data provided on these devices are not discussed here other than to state that they too tend to be more complete than those provided as a general practice.

Certain differences in symbolism exist between standard practice in the United States and in Europe, making desirable the presentation of the equivalence table (Table E-1).

Priming of the parameters listed indicates an intrinsic value within the basic transistor in the US system. The European practice for designating the common electrode, a designation which may not be required if techniques in this handbook are followed, is to follow the above with an *e*, *b*, or *c* to indicate a common emitter, base, or collector. The *e* subscript is omitted in this handbook, but the *b* and the *c* subscripts are used for the common-base and the common-collector configurations as required.

Two families of basic curves are provided on the **OC30** transistor, Fig. E-1(A) presenting the general group, and Fig. E-1(B) the low-voltage group. These two sets both include a collector family of curves and a base family in compatible form. In addition, the set in Fig. E-1(A) contains two other curves, one of base current as a function of collector current with a fixed collector voltage in the second quadrant, and a contour of base current against base voltage for fixed collector voltage in the third quadrant. The collector family is in

the first quadrant, and the base family in the fourth. The two curves in the second and third quadrants represent data at the same collector voltage, and can be used for approximating both the beta and the forward conductance of the device, but at relatively low accuracy.*

In addition to these families of basic curves, contours are also provided for the determination of the base current with an open emitter return and the emitter current with an open base return. These data are helpful in the determination of the stability of a circuit using the device. Because the change in floating-potential of the base with temperature is known theoretically, a contour expressing this relation is only needed if the theoretical values for some reason do not give accurate results. The nominal values for this, given by Nosov and Khazanov, are -0.0023V per deg for germanium, and -0.0020V per deg for silicon (Ref. 2).

The static data presented on these curves are consequently adequate for static design problems. They have only one limitation—the small-signal data are rather inaccessible.

The data provided for the **OC170** transistor in Fig. E-2 are possibly the most complete the writer has seen. Only the base-input contours are missing in the static data. The small-signal data are nearly complete, but the coordination of the different data is somewhat inconvenient. One of the small-signal correction contours, that for g_{22e} , is missing on Fig. E-2(D). This curve is available on the remaining graphs, and probably can be used to correct for the missing contour.

Fig. E-2(G) is particularly interesting in that it gives considerable information on the variation of the device parameters as a function of frequency. The behavior of all but two of the curves is as might be expected; the two worthy of further discussion are the curves for g_{11e} (g_i) and g_{22e} (g_o). As explained by Regis and Lake (Ref 1), the rise in the value of g_{11e} with frequency is due to the shunting-out of the internal conductance of the input by the input capacitance. The conductance

*Curve data courtesy of Amperex Electronics Corp.

remaining is that due to base-spreading resistance. The frequency at which the conductance rise initiates is between the β -cutoff frequency and the upper noise-comer frequency fn_c . The increase in g_{22e} is a result partially of the time delay due to diffusion and drift

introduced by y_{21e} through the effect of r_b' . If base-spreading resistance is zero, this increase would be zero.

As a matter of interest, it is convenient to include the equations derived by Regis and Lake for representation

TABLE E-1
EQUIVALENT SYMBOLS

Voltage:							
U.S.	v_c	v_B	V_{CC}	V_{BB}	V_{EE}	V_s	U
Europe	U_{cE}	U_{BE}	U_O	U_{bat}		U_s	U
Current:				Resistance:		Power:	
U.S.	i_B	i_C	i_E	r_b', r_{bb}'	P_c	P_i	P_o
Europe	I_B	I_C	I_E	r_{bb}'	N_c	N_i	N_o
Tot. Inp. Power:			Crit. Freq.		Gain:		
U.S.	—————		f_a	f_β	f_T	K	K_i
Europe	$N =, N_{bat}$		f_{ab}	f_{α}	$f(\alpha=1)$	v_{uc}	v_{ii}
Parameters:							
U.S.	$y_i = g_i + jb_i = g_i + j\omega C_i$			$y_f = g_f + jb_f = g_f + j\omega C_f$			
Europe	$y_{11} = g_{11} + jb_{11} = g_{11} + j\omega C_{11}$			$y_{21} = g_{21} + jb_{21} = g_{21} + j\omega C_{21}$			
U.S.	$y_r = g_r + jb_r = g_r + j\omega C_r$			$y_o = g_o + jb_o = g_o + j\omega C$			
Europe	$y_{12} = g_{12} + jb_{12} = g_{12} + j\omega C_{12}$			$y_{22} = g_{22} + jb_{22} = g_{22} + j\omega C_{22}$			

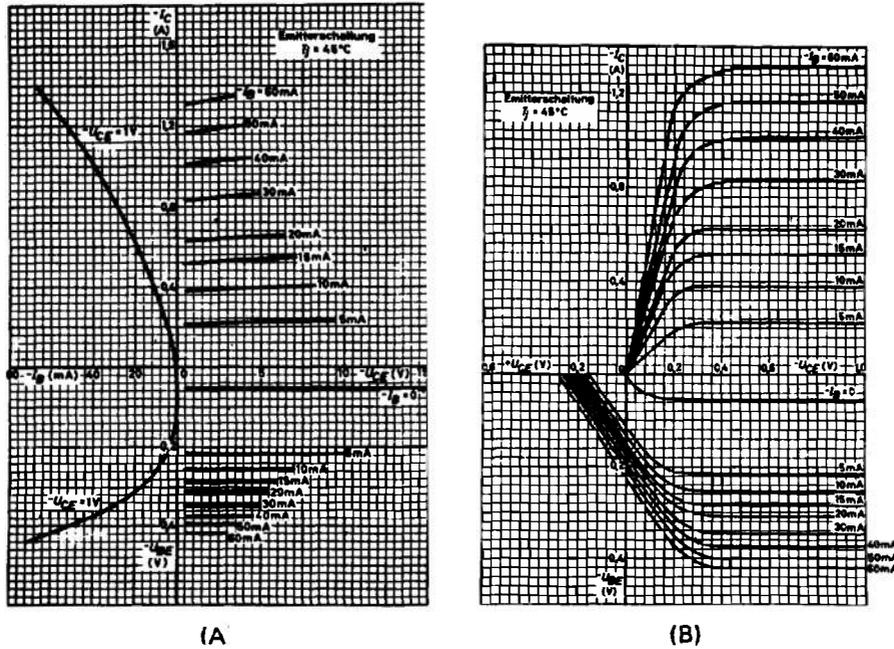
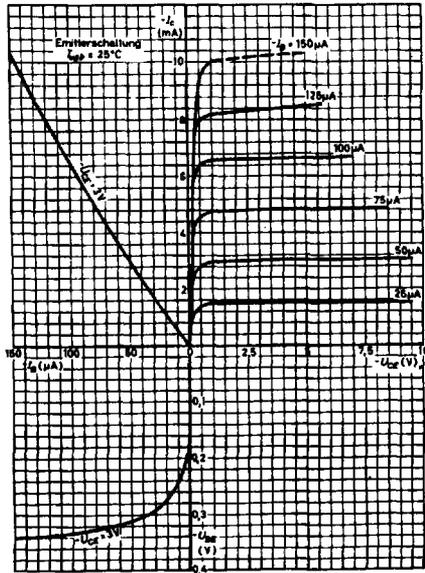
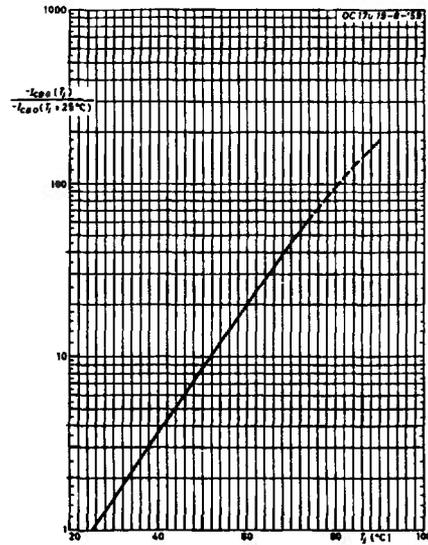


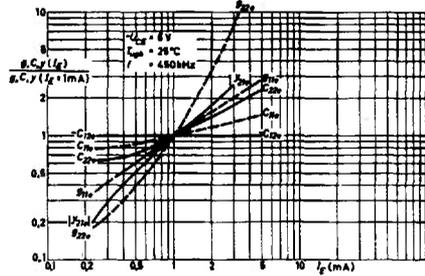
Fig. E-1. OC30 Transistor



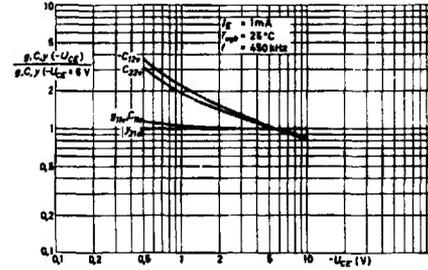
(A)



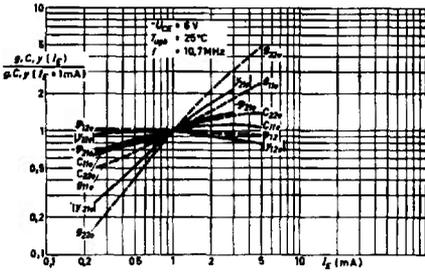
(B)



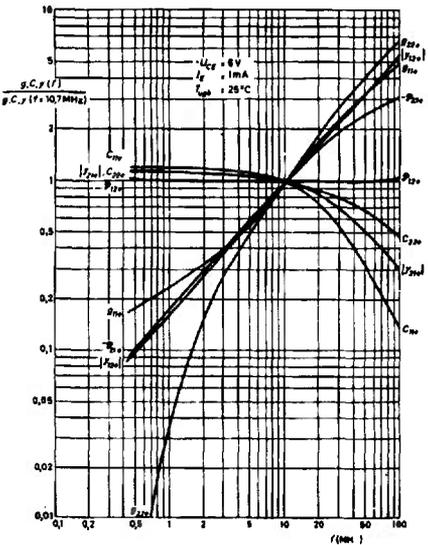
(C)



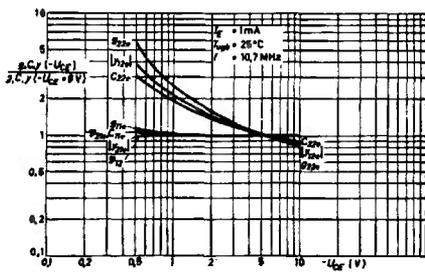
(D)



(E)



(F)



(G)

Fig. E-2, OC170 Transistor

of curves similar to those shown in Fig. E-2(G). This representation, although derived for drift transistors, gives a good indication of the behavior of many com-

mon types of transistors. The equations, in the terminology of this handbook, are

$$\begin{aligned}
 y_i &= (g_{i'} + j\omega C_{i'})/[1 + r_{b'}(g_{i'} + j\omega C_{i'})] \\
 y_f &= [g_{f'} \exp(-j\pi f/4f_a)]/[1 + r_{b'}(g_{i'} + j\omega C_{i'})] \\
 y_r &= -(g_{r'} + j\omega C_{r'})/[1 + r_{b'}(g_{i'} + j\omega C_{i'})] \\
 y_o &= g_{o'} + j\omega(C_{o'} + C_{o''}) + \frac{[g_{f'}(g_{r'} + j\omega C_{r'}) \exp(-j\pi f/4f_a)]r_{b'}}{[1 + r_{b'}(g_{i'} + j\omega C_{i'})]} \\
 y_c &= g_{o'} + j\omega(C_{o'} + C_{o''}) + \frac{[g_{f'}(g_{r'} + j\omega C_{r'}) \exp(-j\pi f/4f_a)]}{(g_{i'} + j\omega C_{i'})}
 \end{aligned}$$

In these equations, the prime values correspond to those for the intrinsic transistor for which $r_{b'}$ is zero, and the double-prime capacitance is the capacitance between the collector lead and the base lead. At low frequencies, the value of y_o may be represented by $y_{o'}$ or conversely.

The curve for g_{i1e} on Fig. E-2(G) levels to a constant value as the frequency is reduced, a condition not recorded on the contour. It turns horizontal rather sharply below a frequency of 0.5 MHz. Similarly, the curve for g_{22e} turns horizontal at reduced values of

frequency, but off the lower limit of the graph scale.

Superficially it would appear that the high-frequency values of g_{22e} or g_o should be only a few times greater than the low-frequency value. This is not the case as a result of the relatively large value of $C_{r'}$ and the effect of $\exp(-j\pi f/4f_a)$, shifting the reactance into a conductance component. This fictitious conductance causes g_{22e} to continue to rise for over a decade increase of frequency, and causes the change to be of several orders of magnitude as can be noted on Fig. E-2(G).

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APPENDIX F

CHARACTERISTIC CURVES FOR SOLID-STATE DEVICES

A collection of characteristic curves on semiconductor devices is included in this appendix to help the reader apply small-signal techniques to typical problems for solid-state devices. Some of these curves include superposed contours of the small-signal parameters and as a result lend themselves directly to the solution of problems in which reliability is an important factor. The balance of the devices are represented in terms of static characteristics, but, because of the coordinated form of the curves, approximations to the small-signal data can be made by the least-squares fitting techniques described in Appendix C or through the use of the transconductance-efficiency relation.

Power contours for half- and full-rated collector dissipation have been included when they fall within the scope of the curves being presented. These contours are also helpful in assuring reliable operation. Where extreme reliability and stability are essential, however, additional drift tests with a sweep-type tester can be helpful. The technique described in Chapter 3, using contours of constant base current as a function of base voltage and collector voltage, is most helpful for these tests. The transistor is operated in the repetitive-sweep condition for a few seconds, and then the base-drive current is removed. The drift of the zero-current contour, as the transistor cools, serves as a measure of the stability. The total power dissipated may be increased in steps until moderate to severe drifting occurs. The maximum steady-state dissipation then is approximately 15% of the peak value indicated on the curves.

Additional families of curves on transistor devices may be obtained easily with an analyzer such as the

Tektronix Model 575, and photographs made from the curves may be replotted in the form presented in this appendix. Little difficulty will be encountered if adequate spread can be obtained for the input contours. The zero-suppression circuit described facilitates the preparation of the input family as required.

The reader should note that the curves presented are typical for ordinary production units of the specified code number, but may not necessarily be typical of the bogey, or ideal, transistor of the specified type. As a consequence, the data provided should be treated as being approximate, and an operating margin should be provided to allow for the variations which must be expected among typical devices such as those measured. Where the number of samples have permitted, and sufficient manufacturer's data have been available, the samples have been sorted to find the device in the group most nearly like the specifications. Otherwise, the unit measured has been selected partly on the basis of the one appearing to be the most representative of the group available. In particular, the degree of stability was weighted heavily in the process of selection.

The improvement of solid-state devices is continuing sufficiently rapidly so that even if the enclosed curves did represent ideal devices at the time of measurement, the passage of a few months or years can be expected to bring about sufficient improvements with the result that new curves should have to be taken to determine the characteristics of the devices then in production. This is particularly true if large numbers of the devices are required or if the reliability of the circuits using transistors is an important consideration.

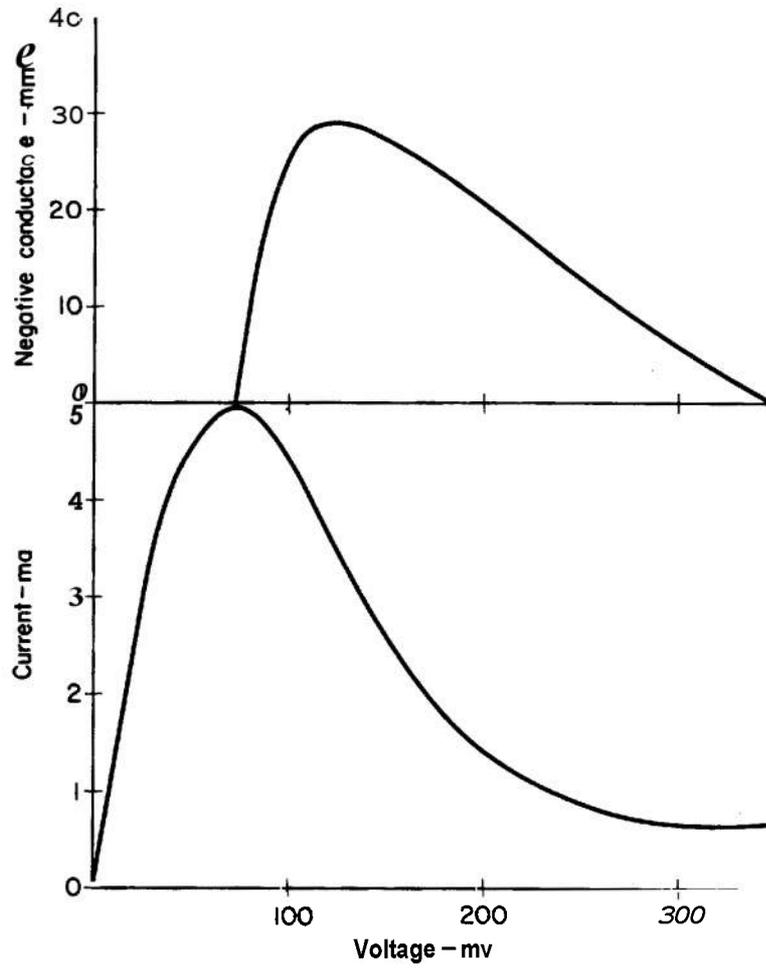


Fig. F-1. ZJ56A-47 (GE)

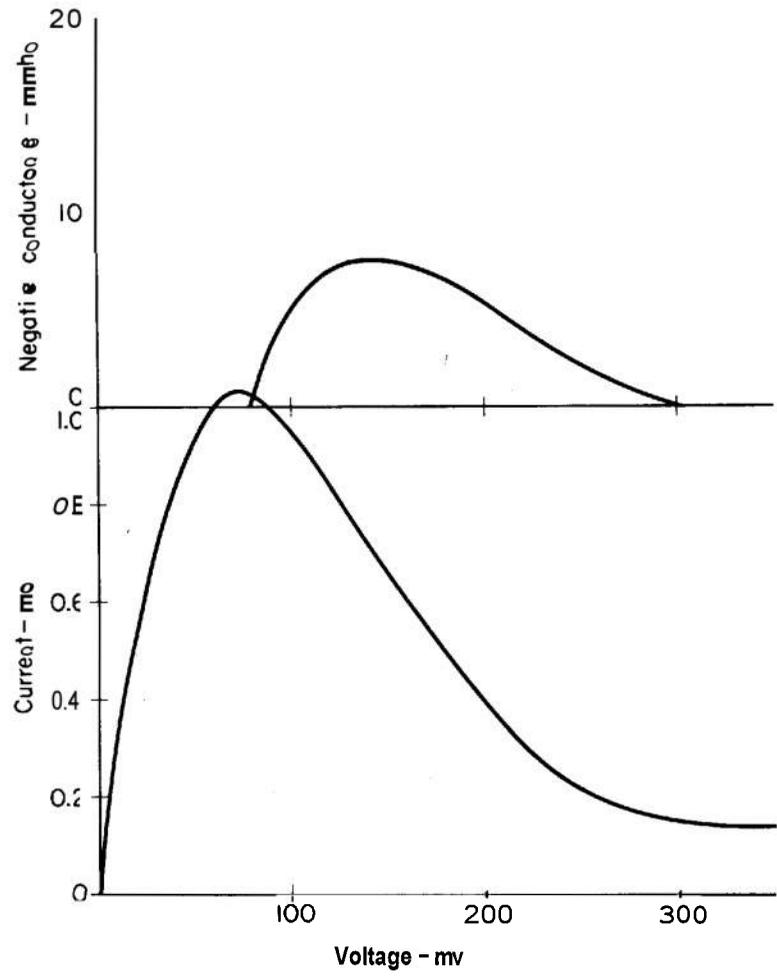


Fig. F-2. ZJ56-013 (GE)

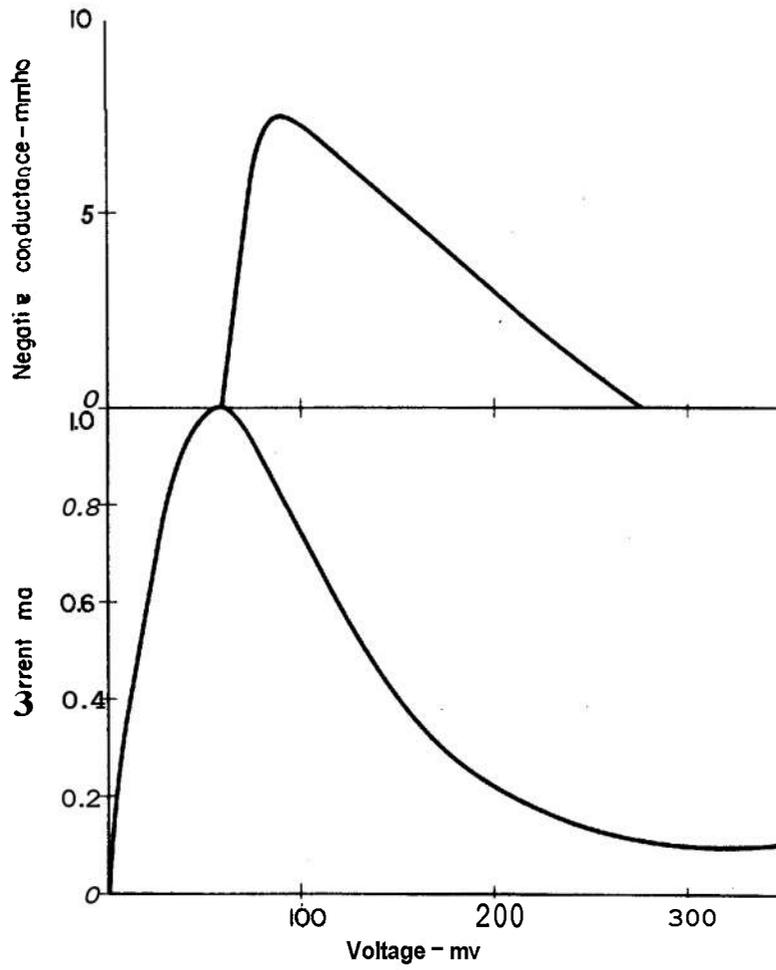


Fig. F-3. ZJ56-017 (GE)

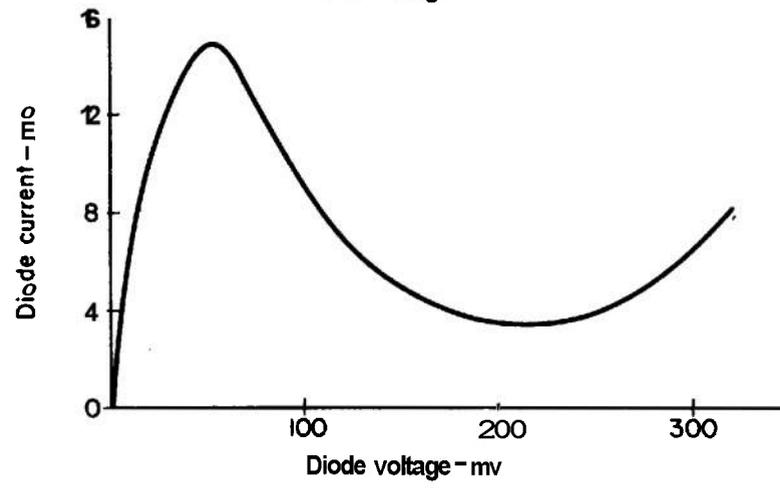
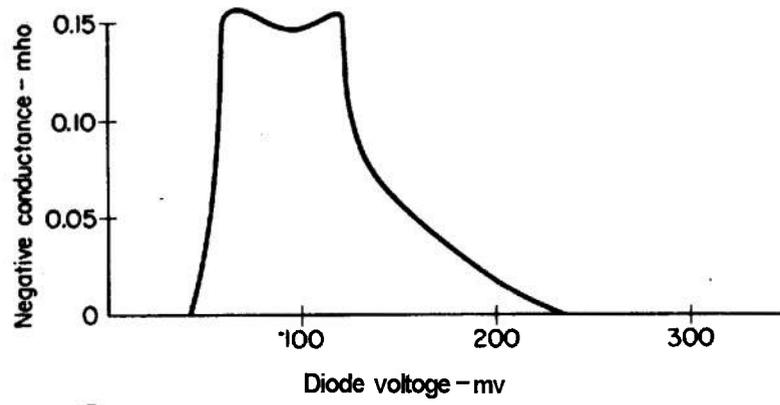


Fig. F-4. TD-2 (GT)

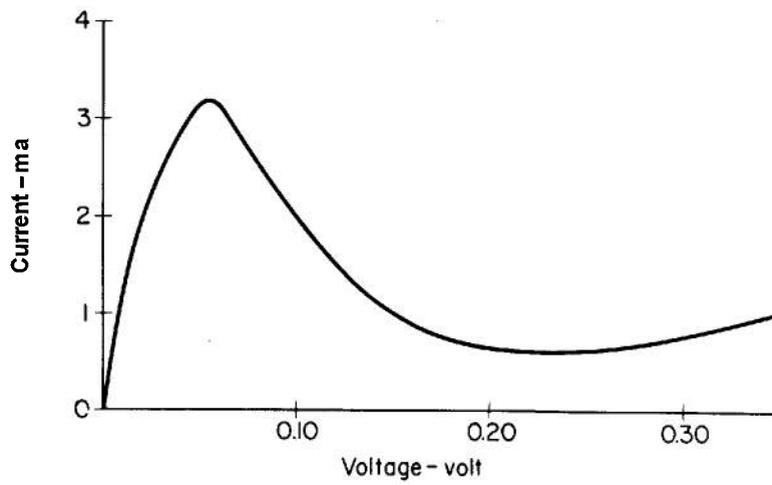
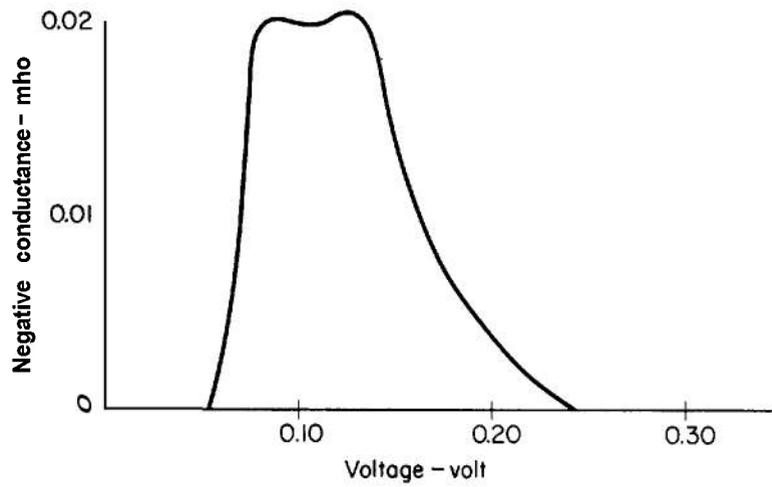


Fig. F-5. Orange Dot (RCA)

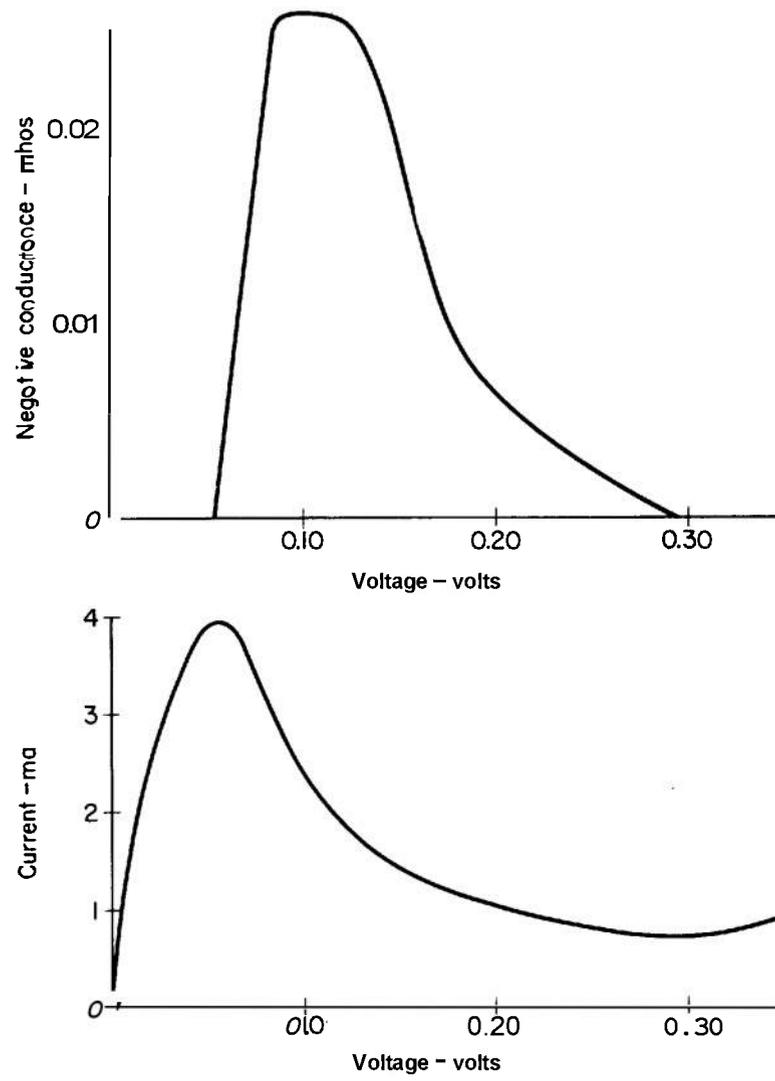


Fig. F-6. Yellow Dot (RCA)

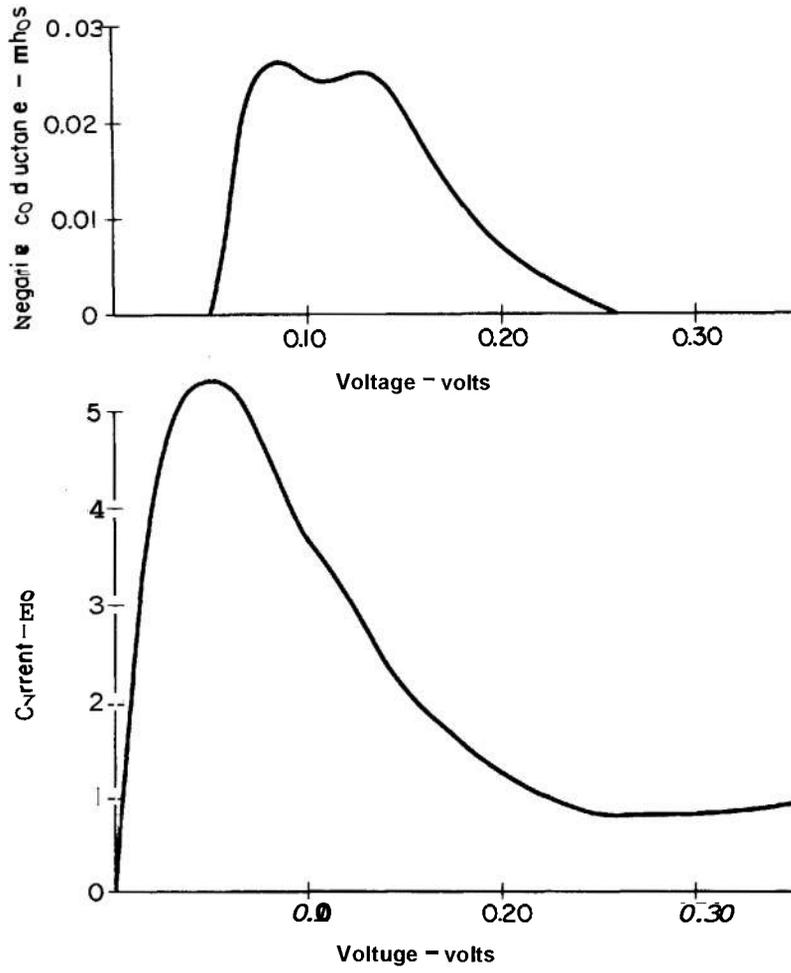


Fig. F-7. Blue Dot (RCA)

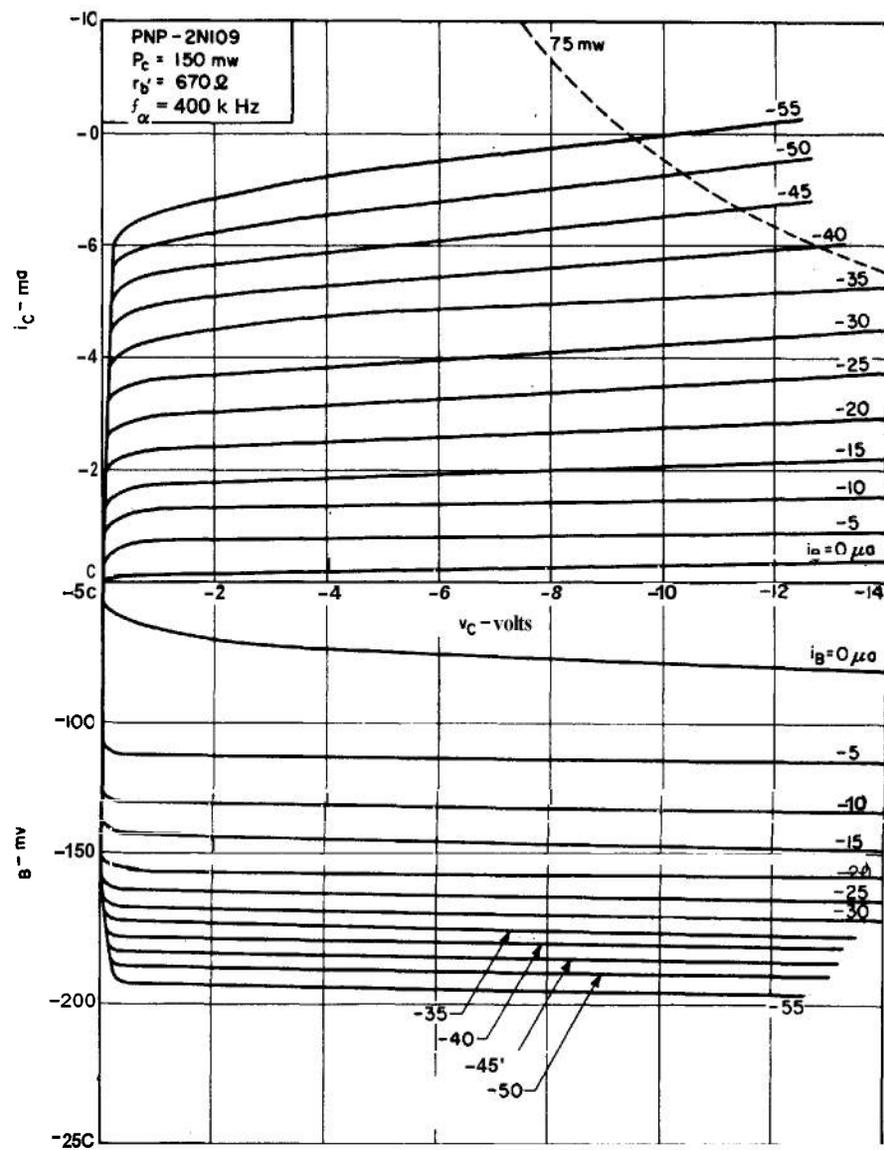


Fig. F-8. PNP-2N109

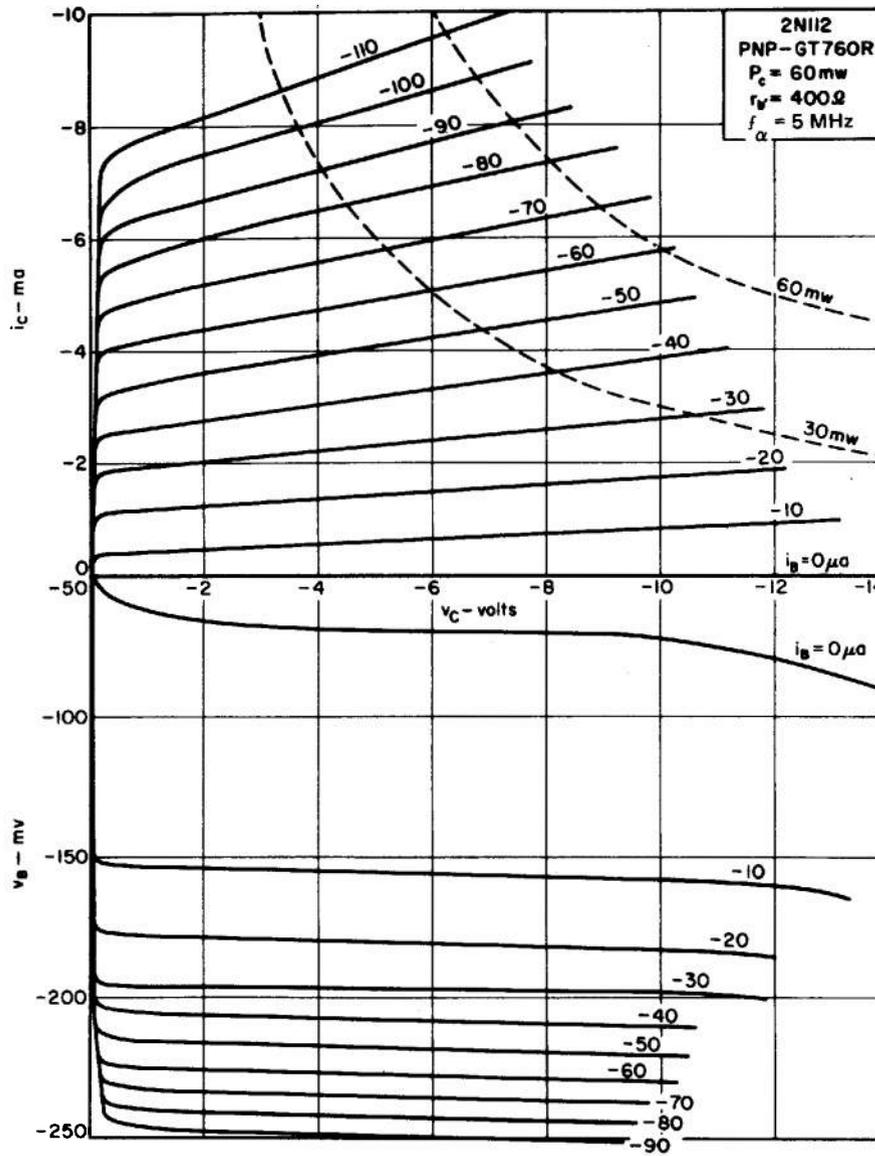


Fig. F-9. 2N112

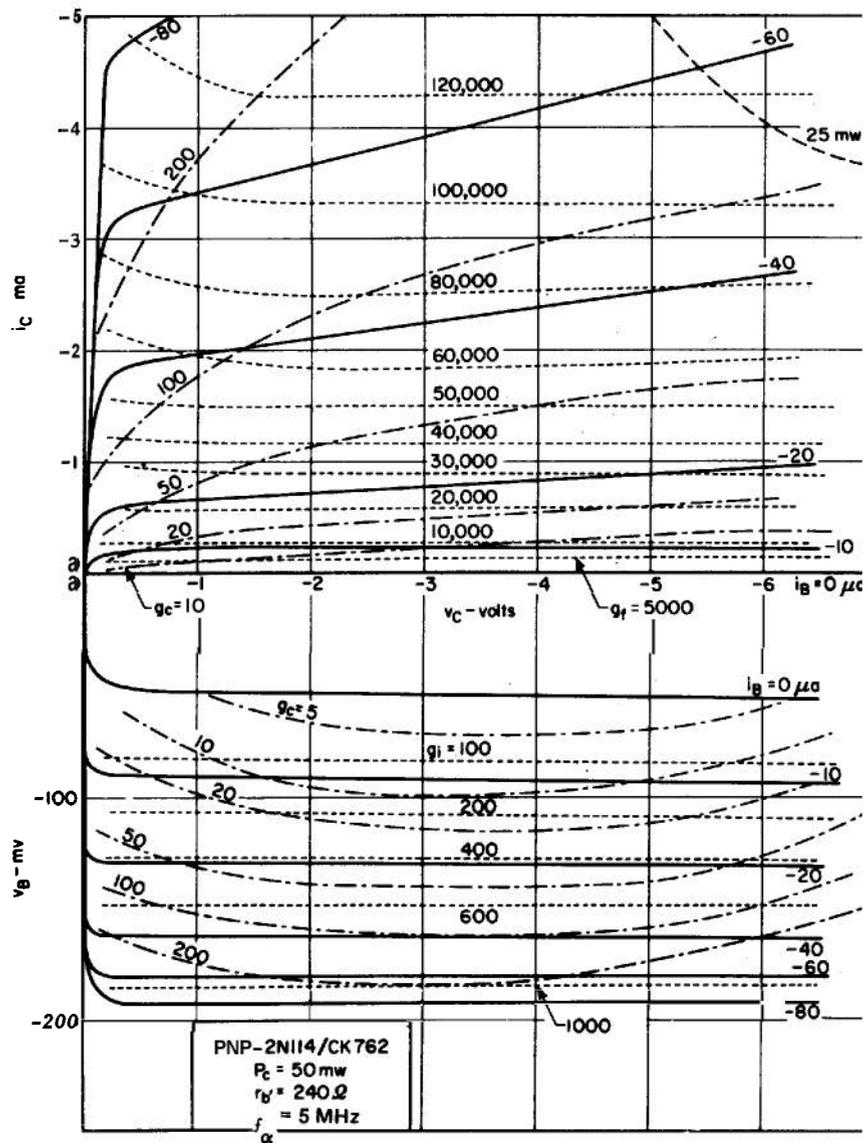


Fig. F-10. PNP-2N114/CK762

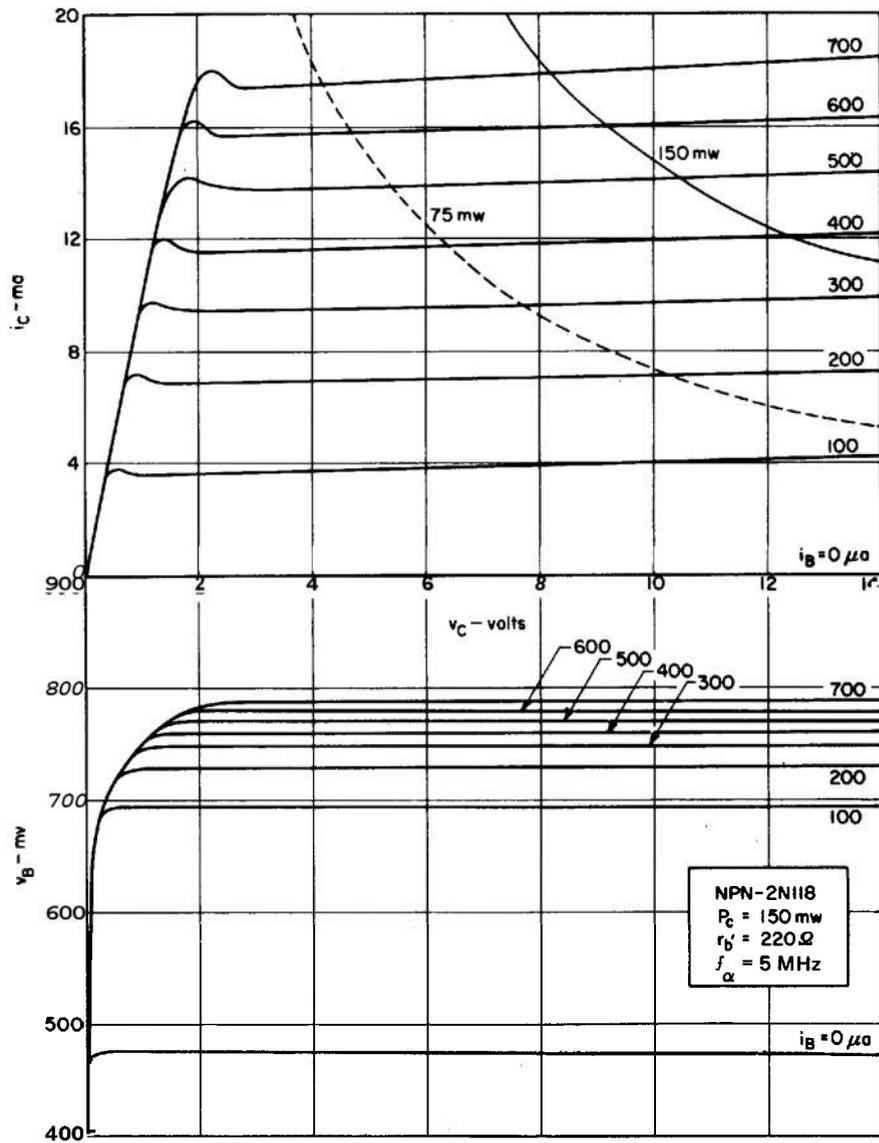


Fig. F-11. NPN-2N118

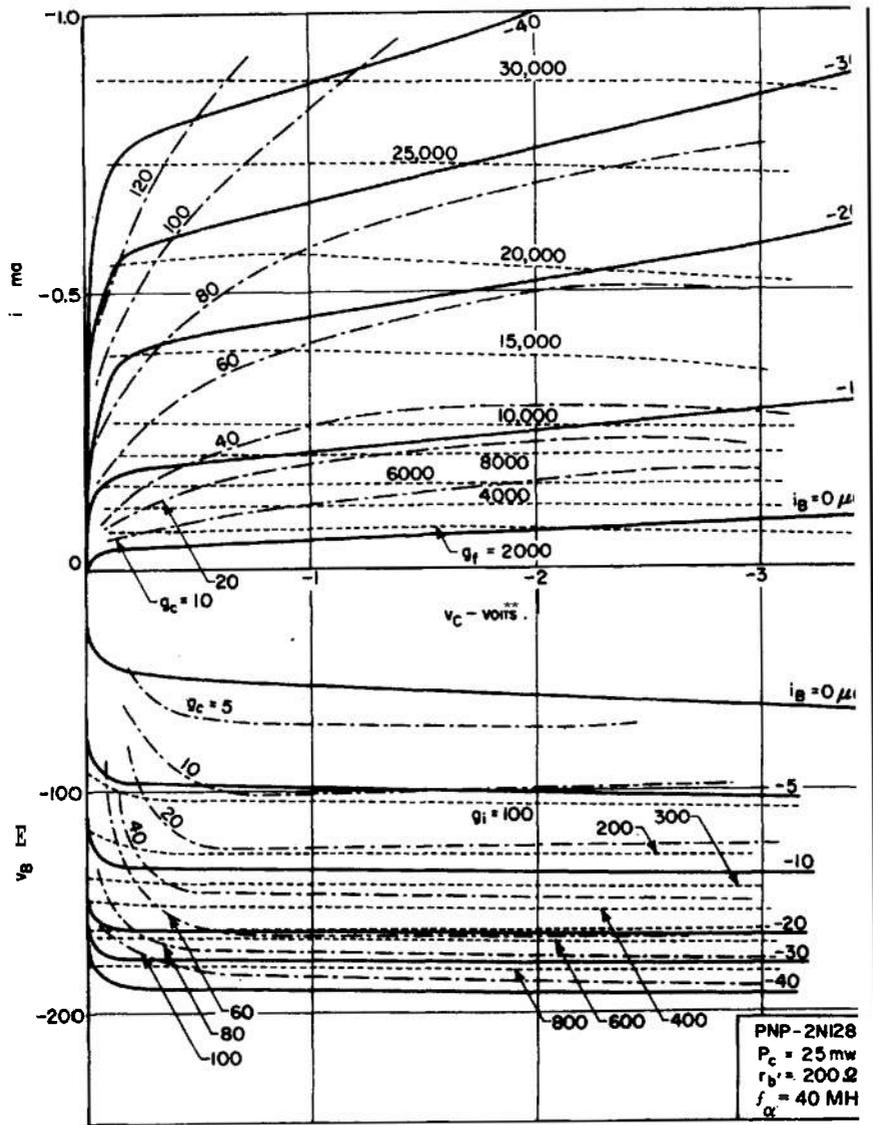


Fig. F-12. PNP-2N128

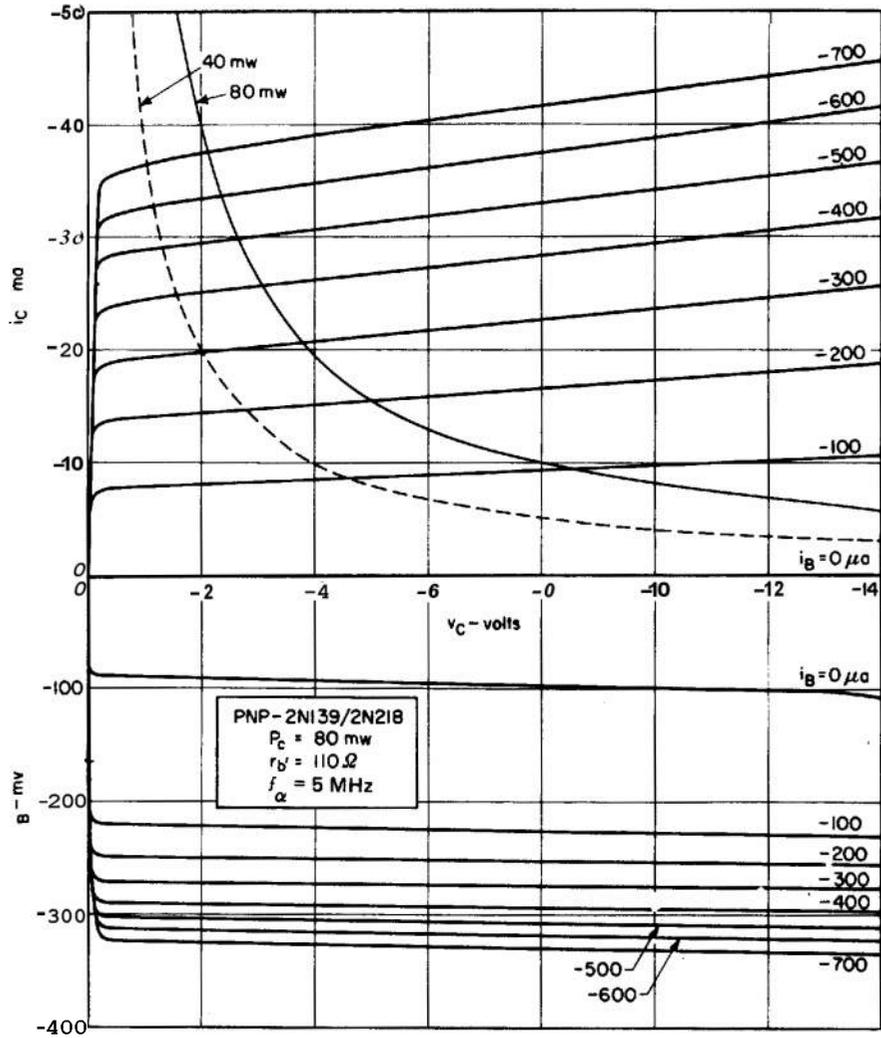


Fig. F-13. PNP-2N139/2N218

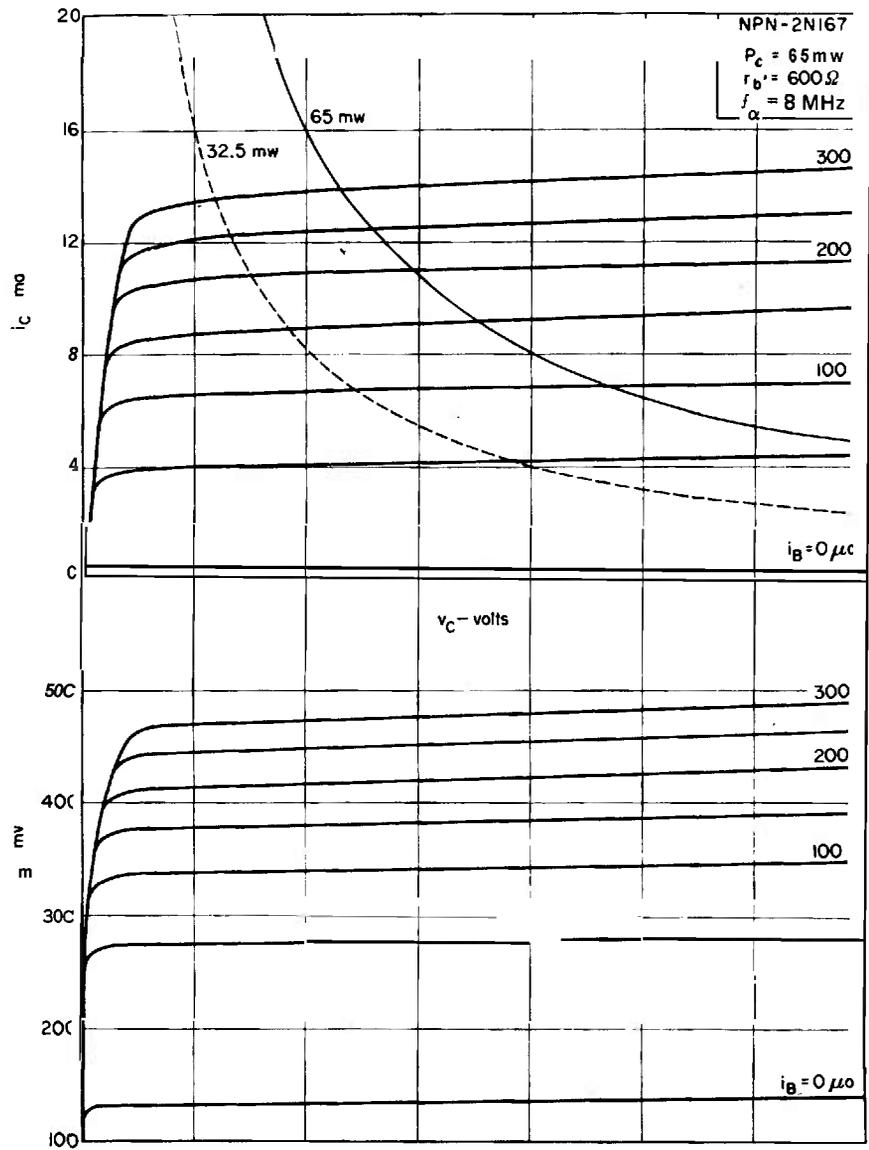


Fig. F-14. NPN-2N167

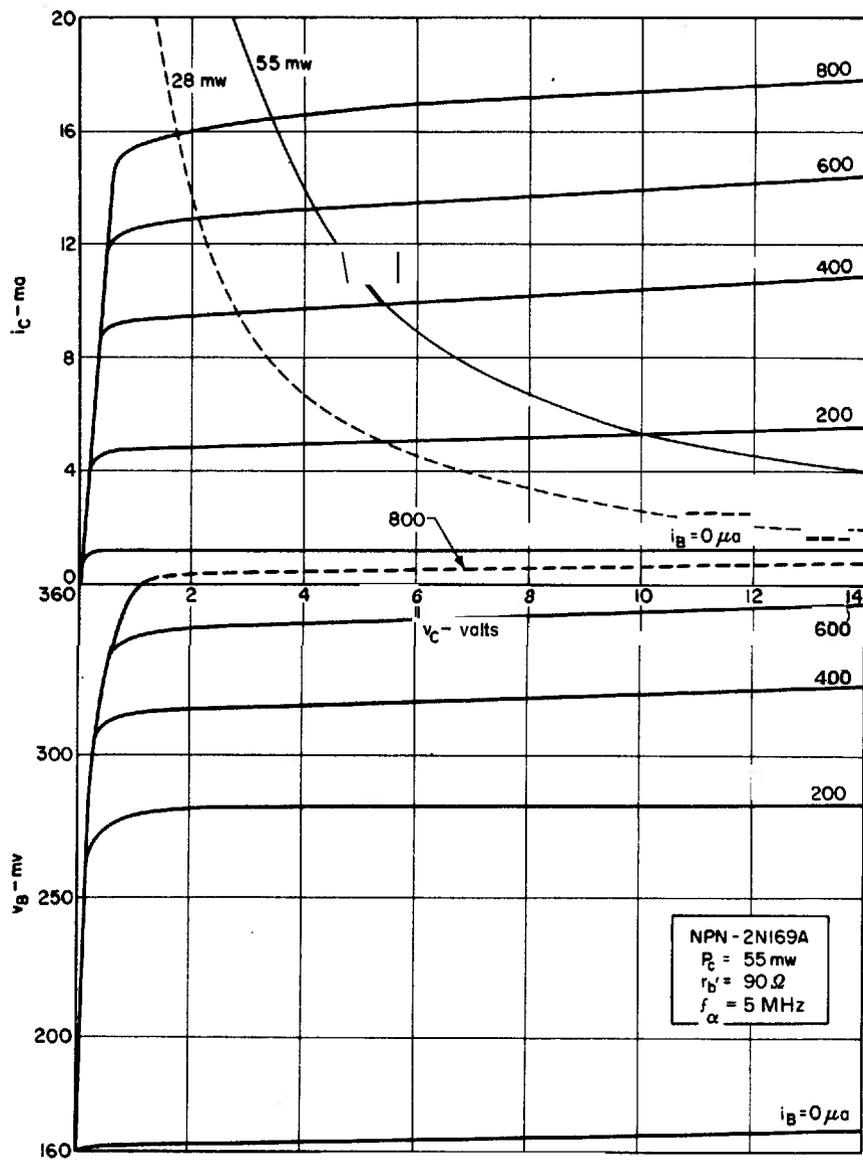


Fig. F-15. NPN-2N169A

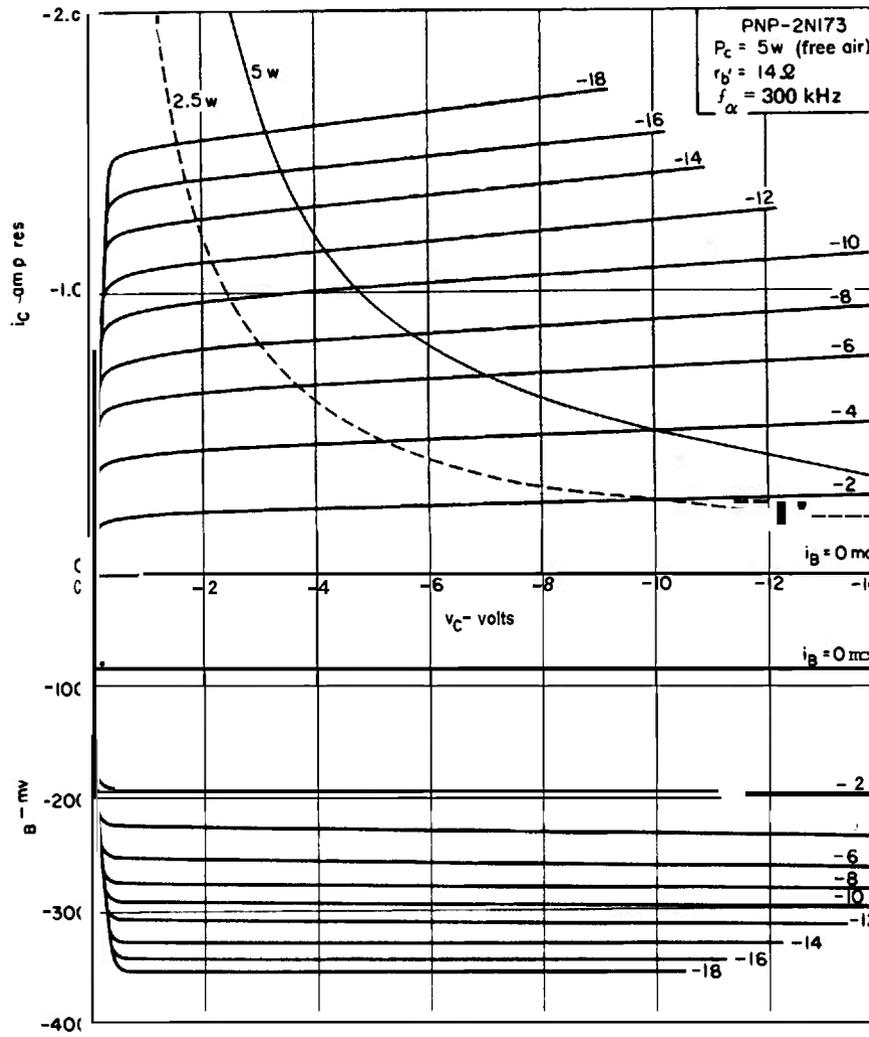


Fig. F-16. PNP-2N173

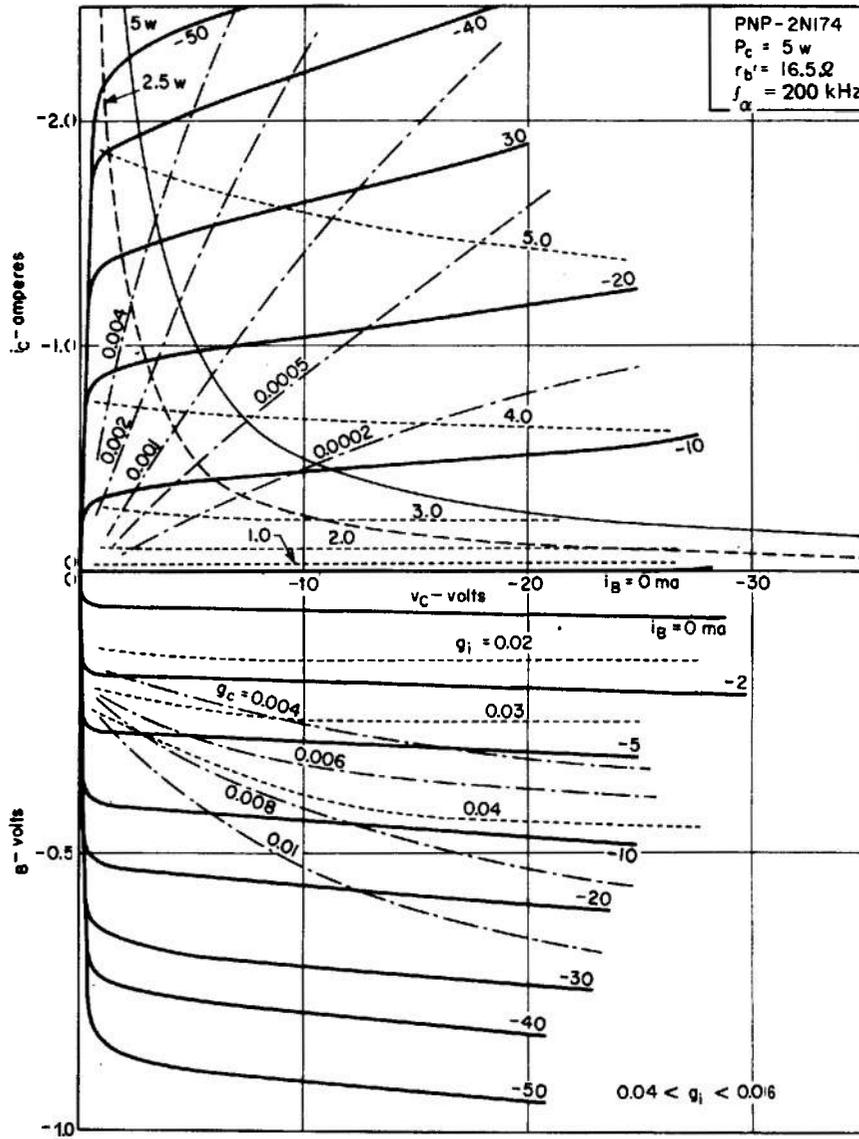


Fig. F-17. PNP-2N174

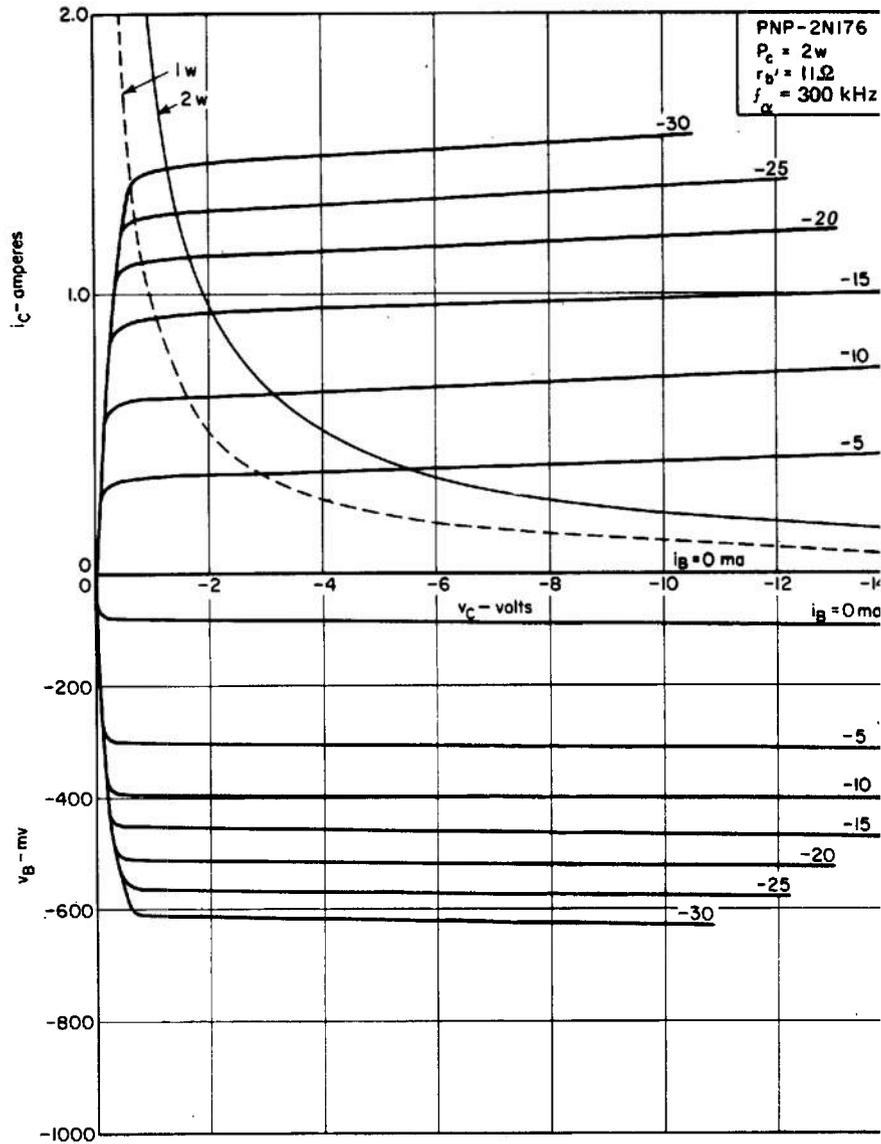


Fig. F-18. PNP-2N176

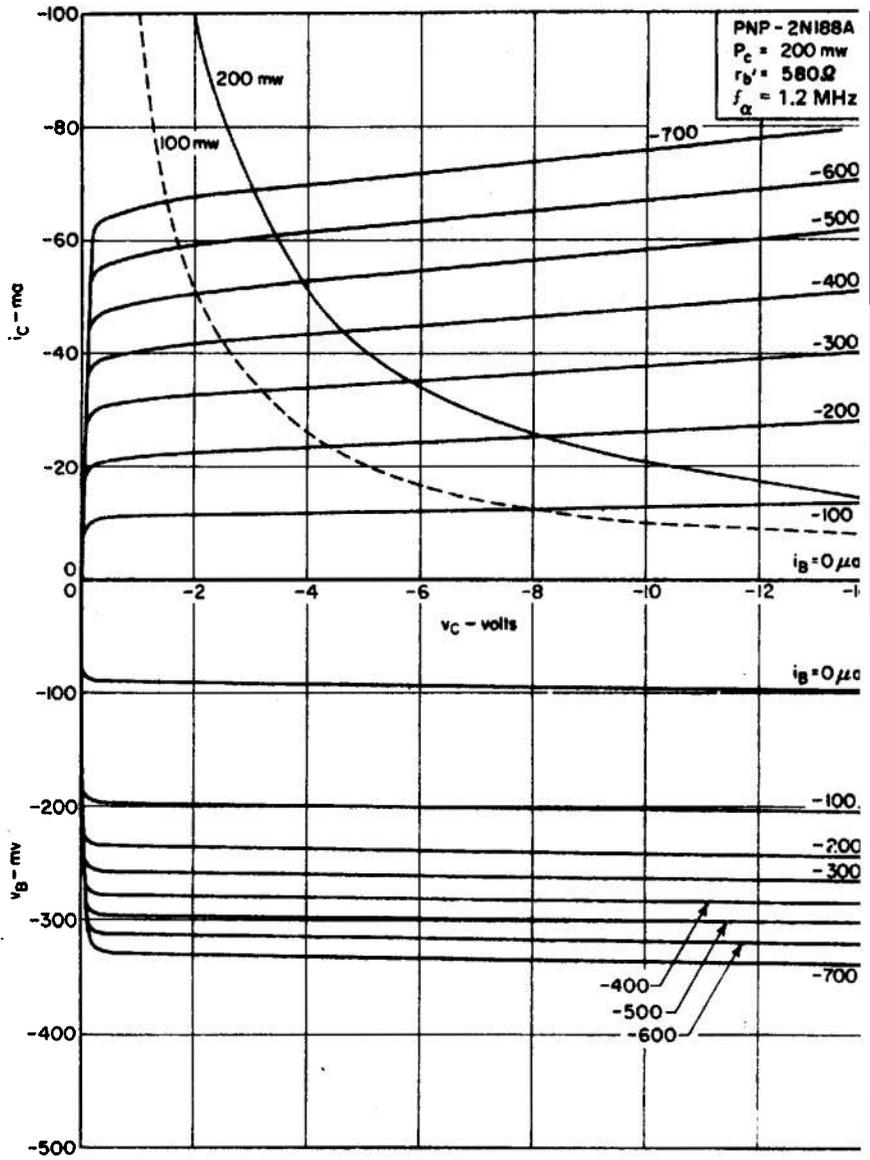


Fig. F-19. PNP-2N188A

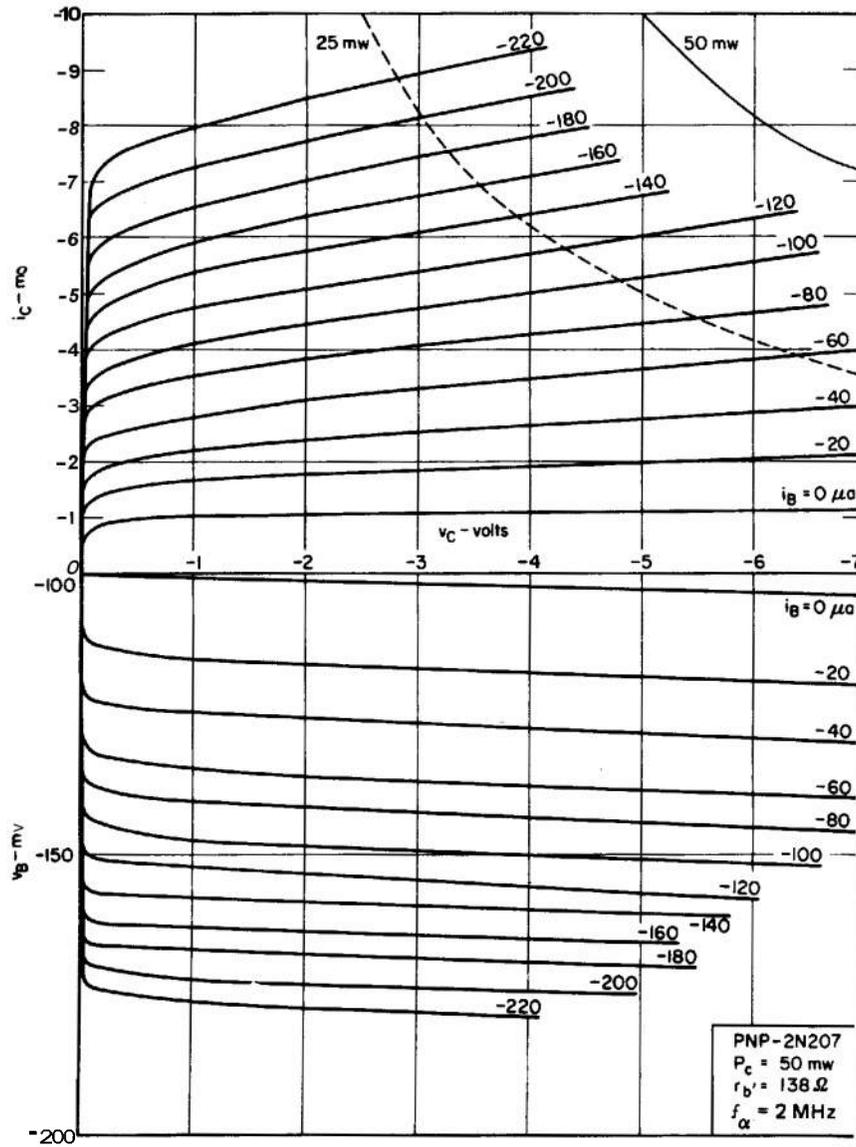


Fig. F-20. PNP-2N207

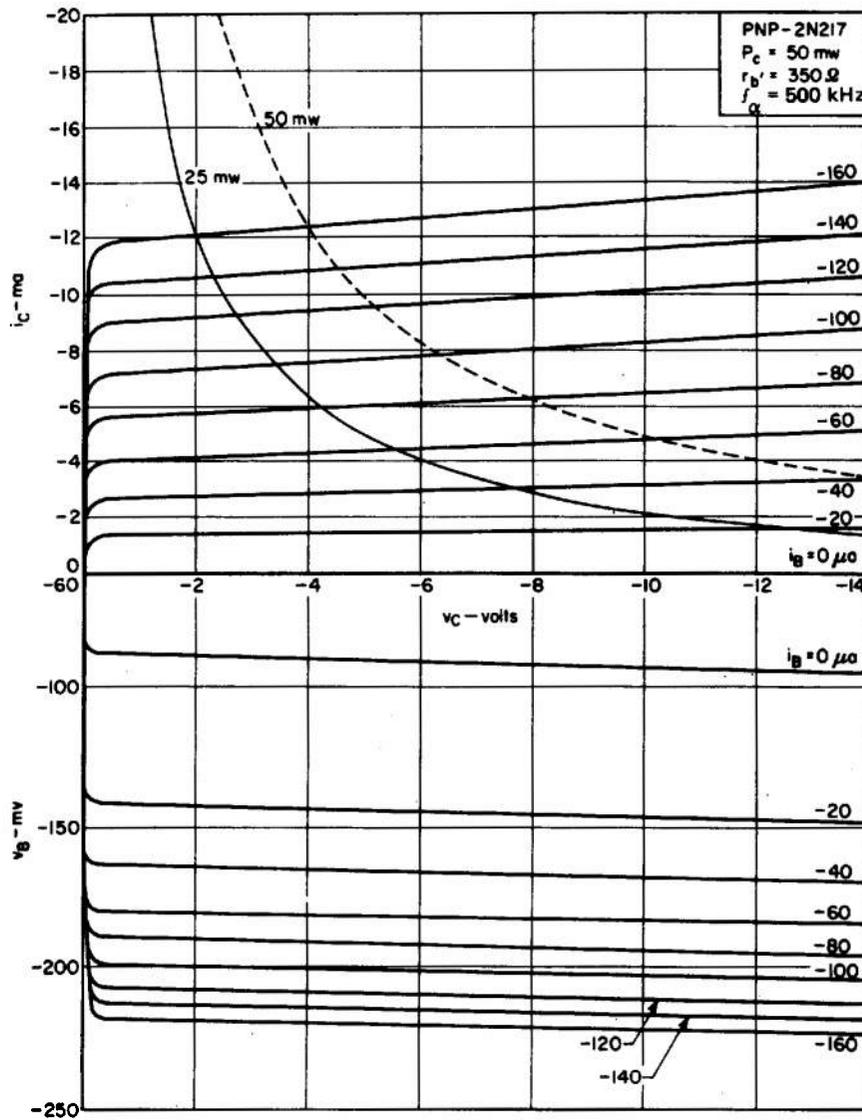


Fig. F-21, PNP-2N217

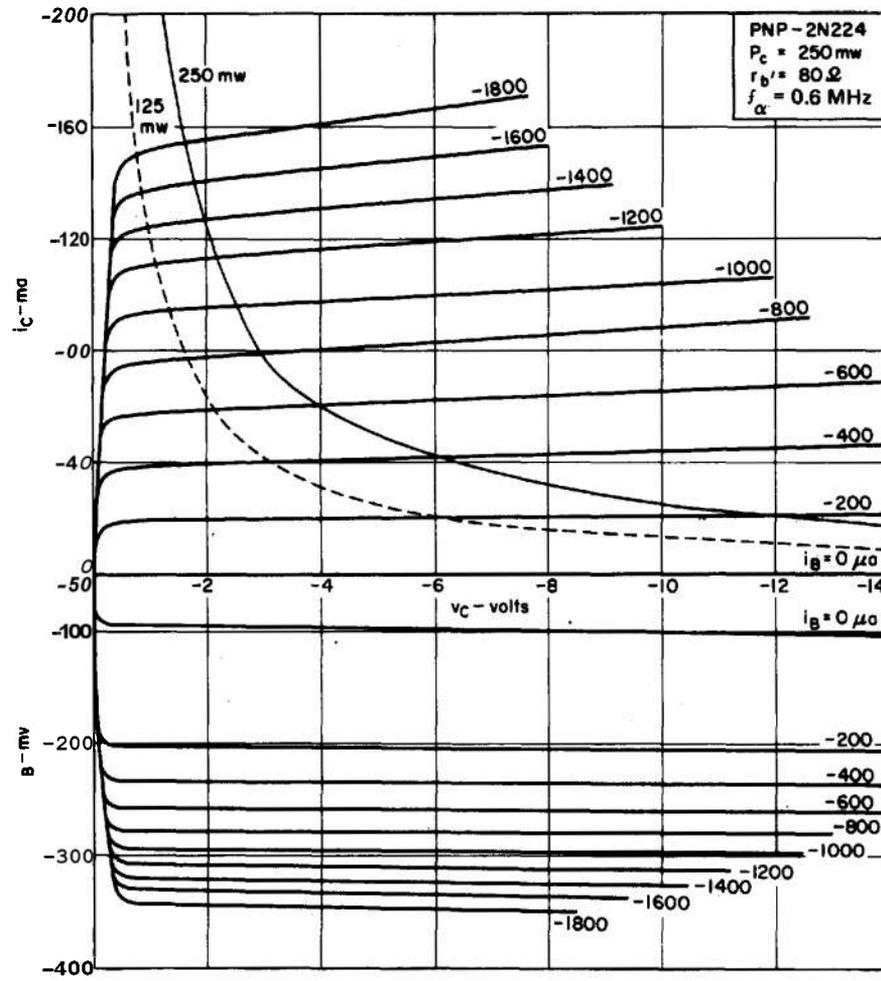


Fig. F-22. PNP-2N224

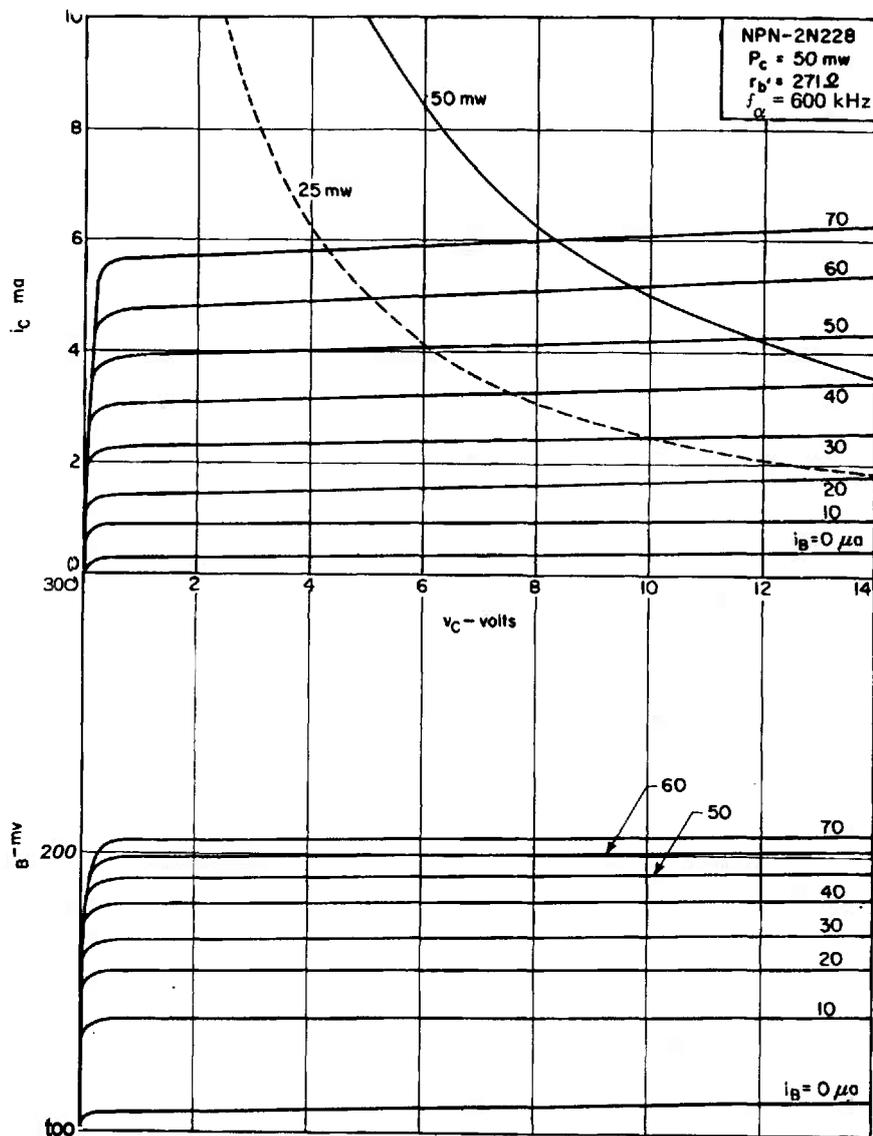


Fig. F-23. NPN-2N228

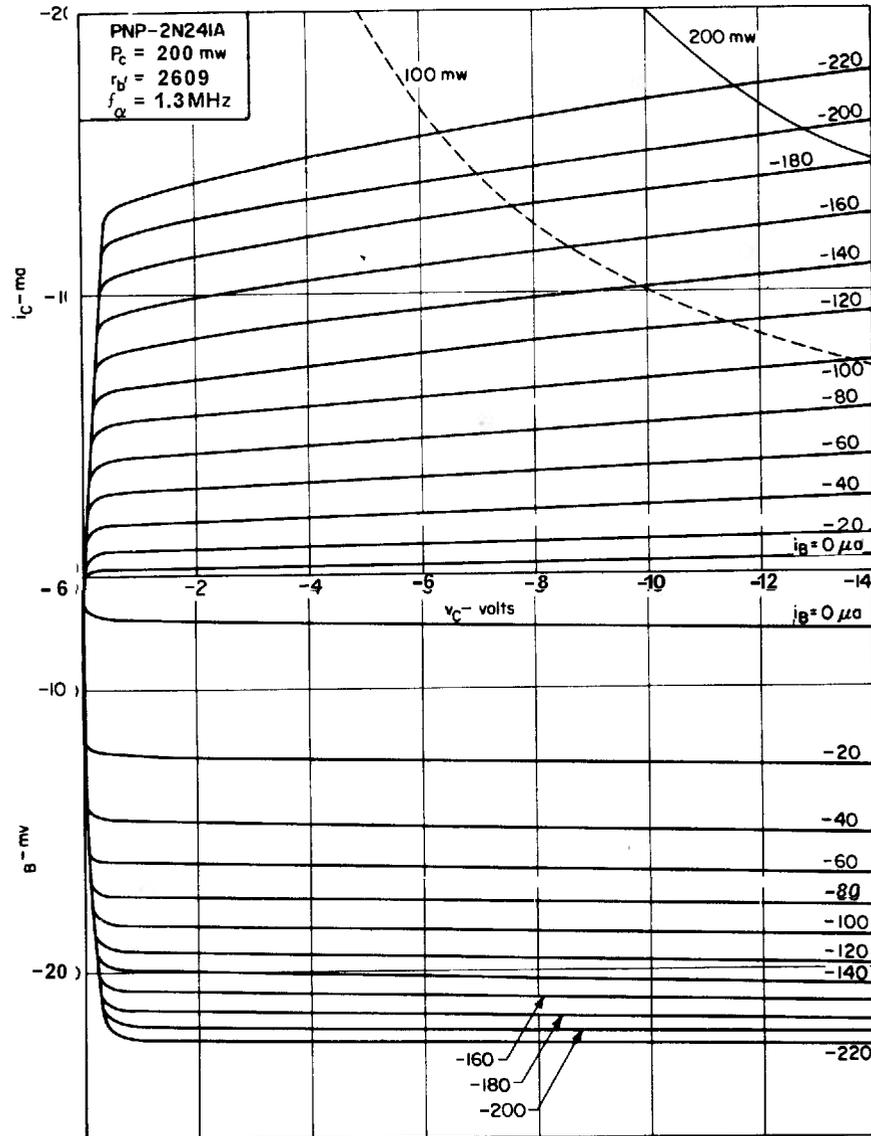


Fig. F-24. PNP-2N241A

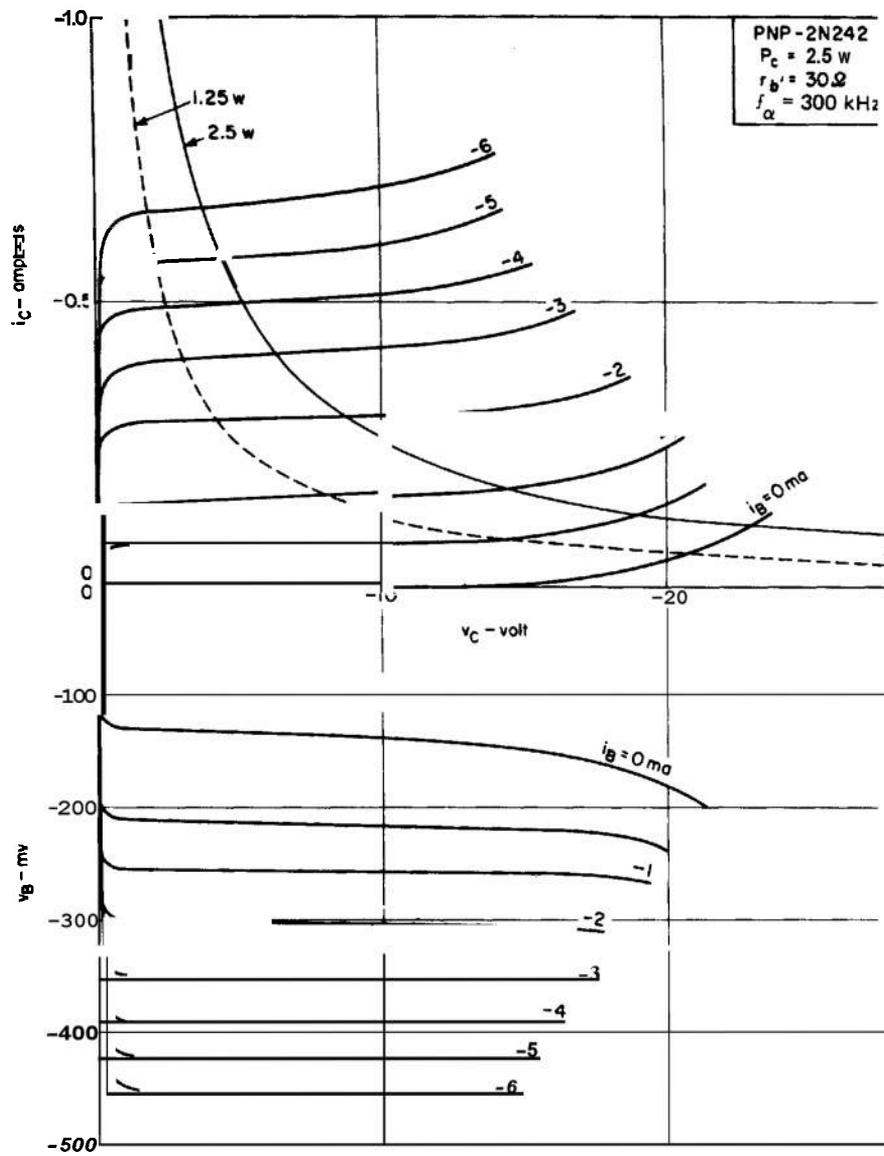


Fig. F-25. PNP-2N242

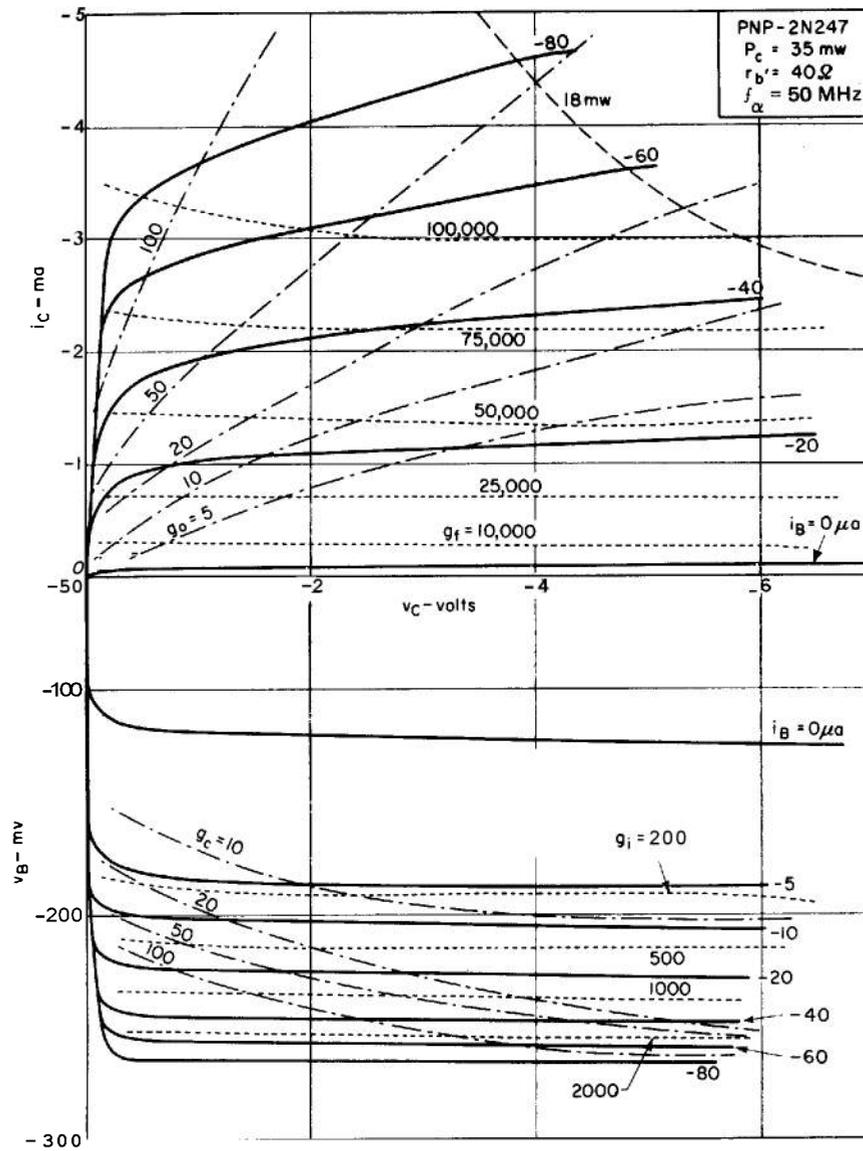


Fig. F-26. PNP-2N247

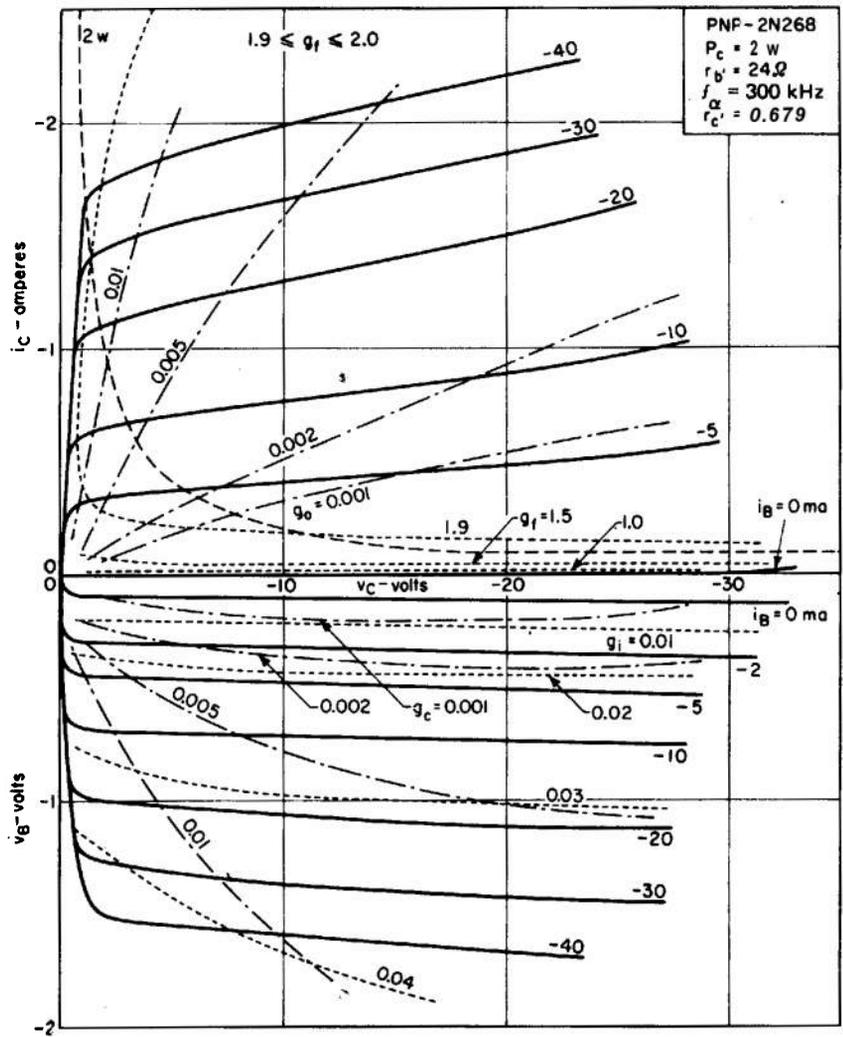


Fig. F-27. PNP-2N268

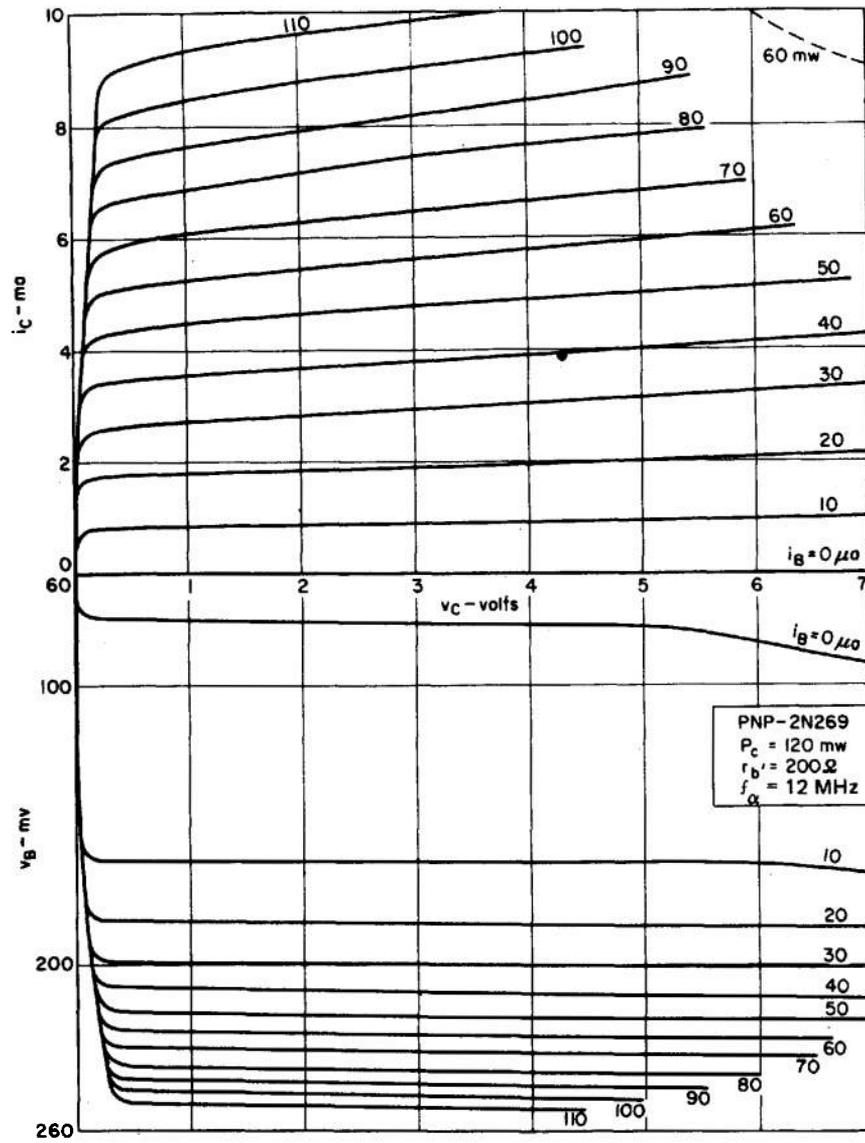


Fig. F-28. PNP-2N269

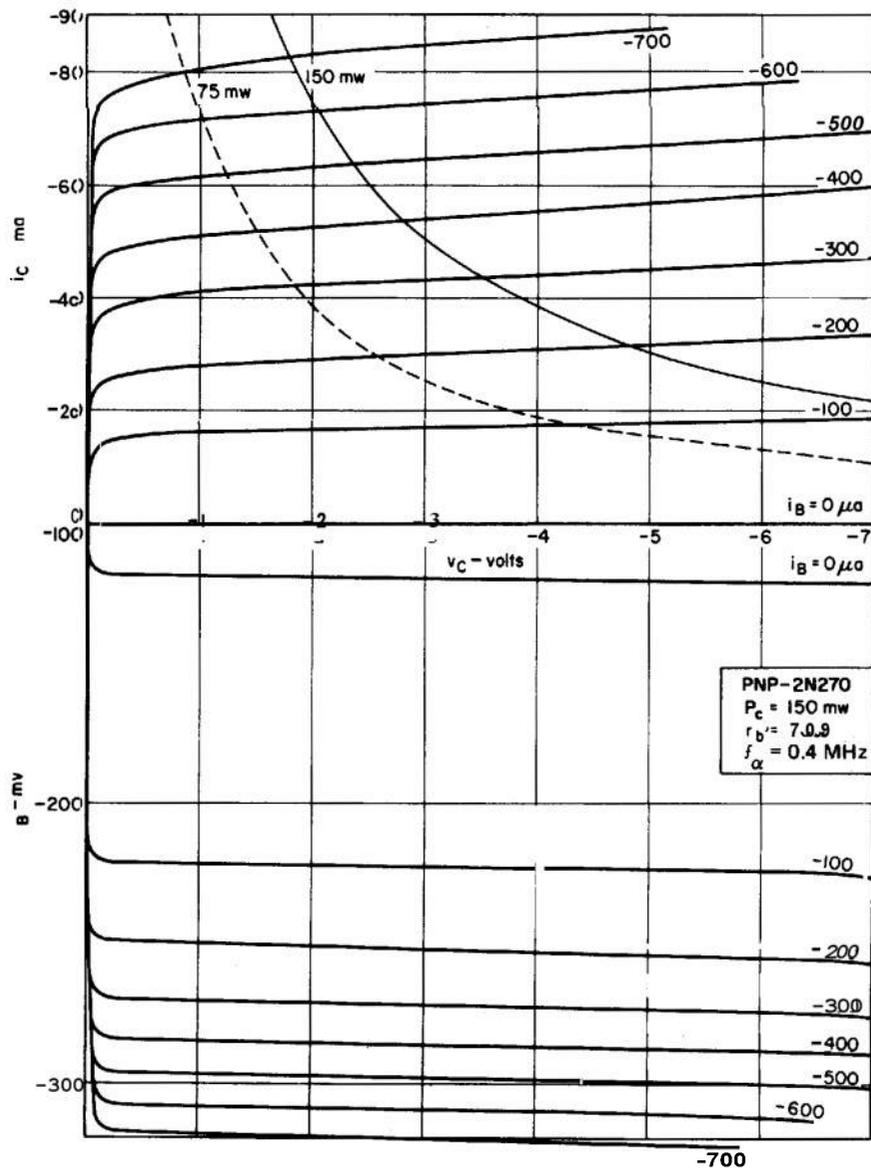


Fig. F-29. PNP-2N270

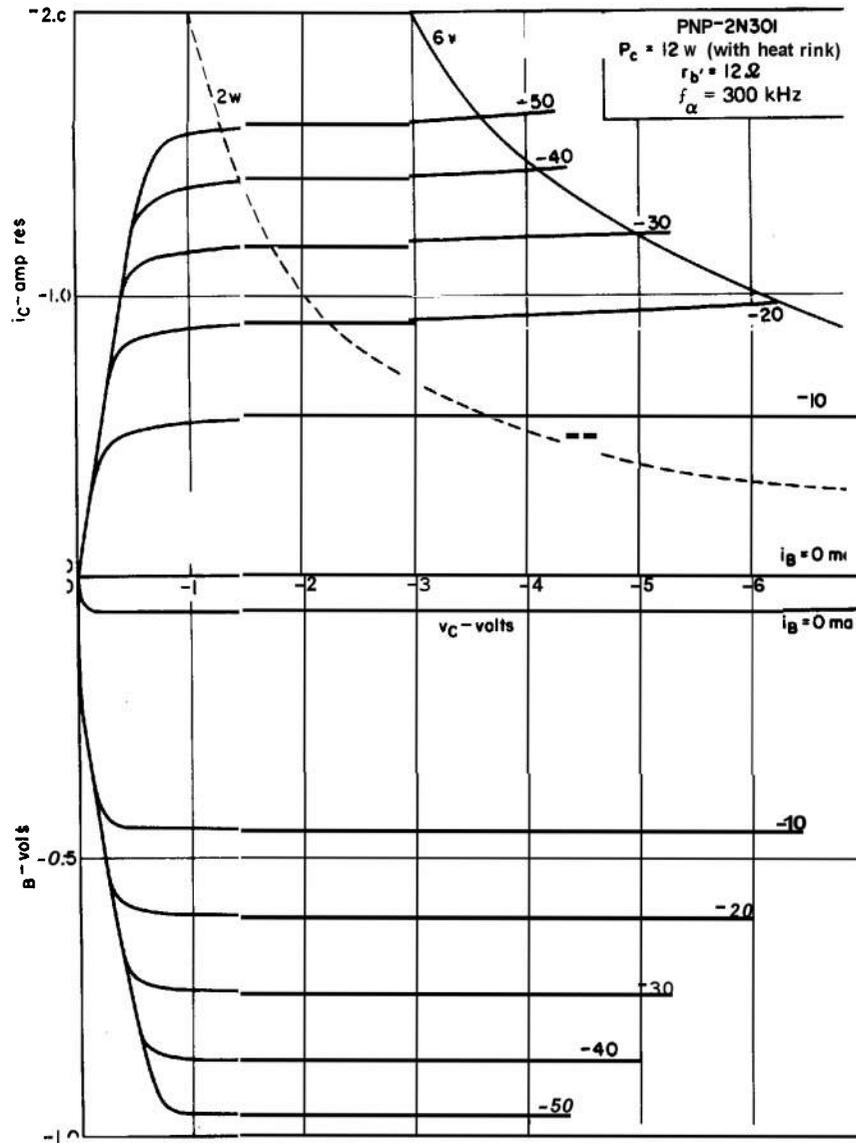


Fig. F-30. PNP-2N301

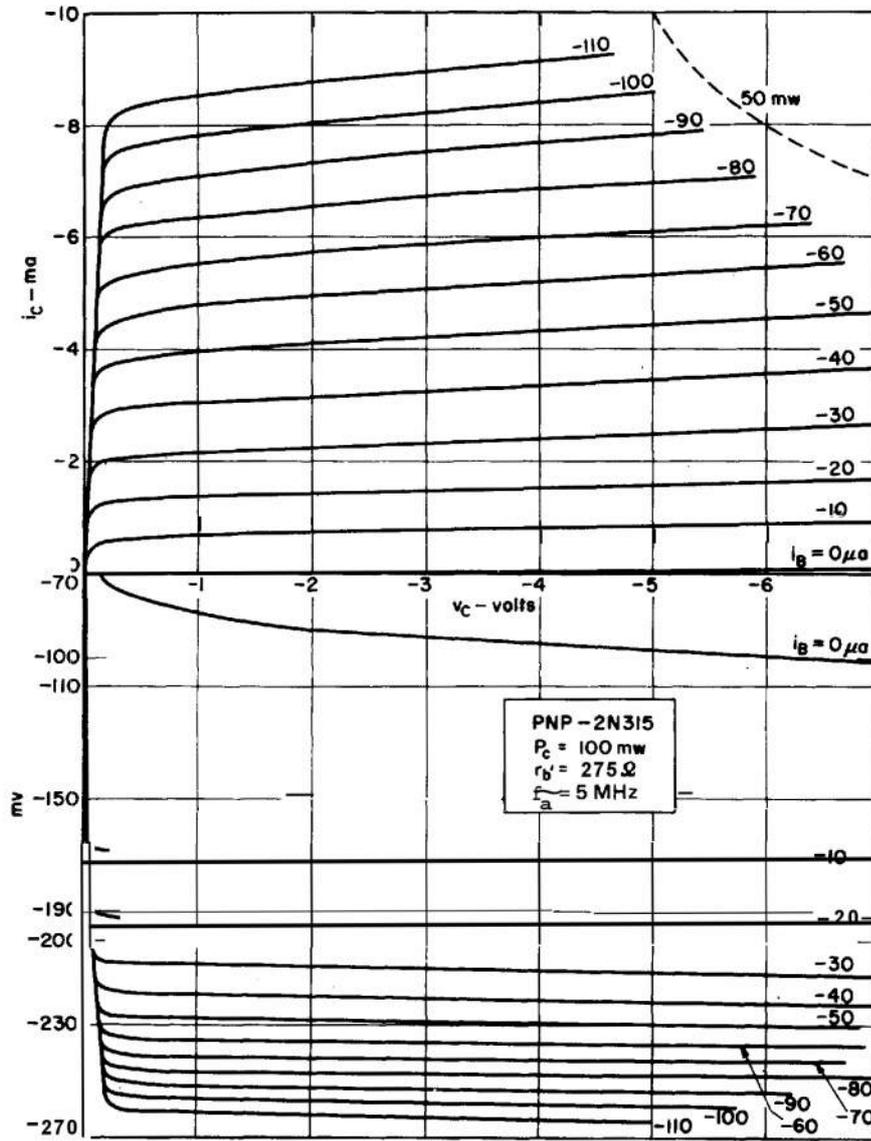


Fig. F-31. PNP-2N315

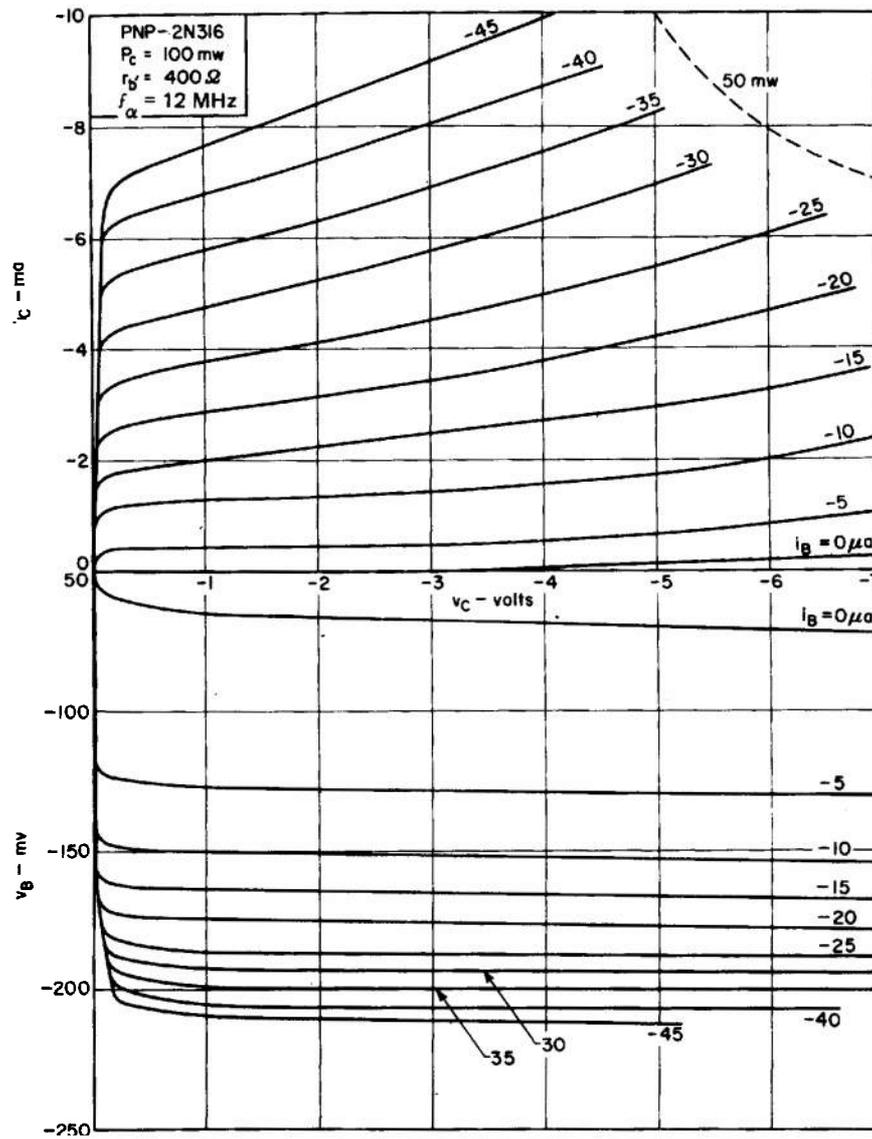


Fig. F-32. PNP-2N316

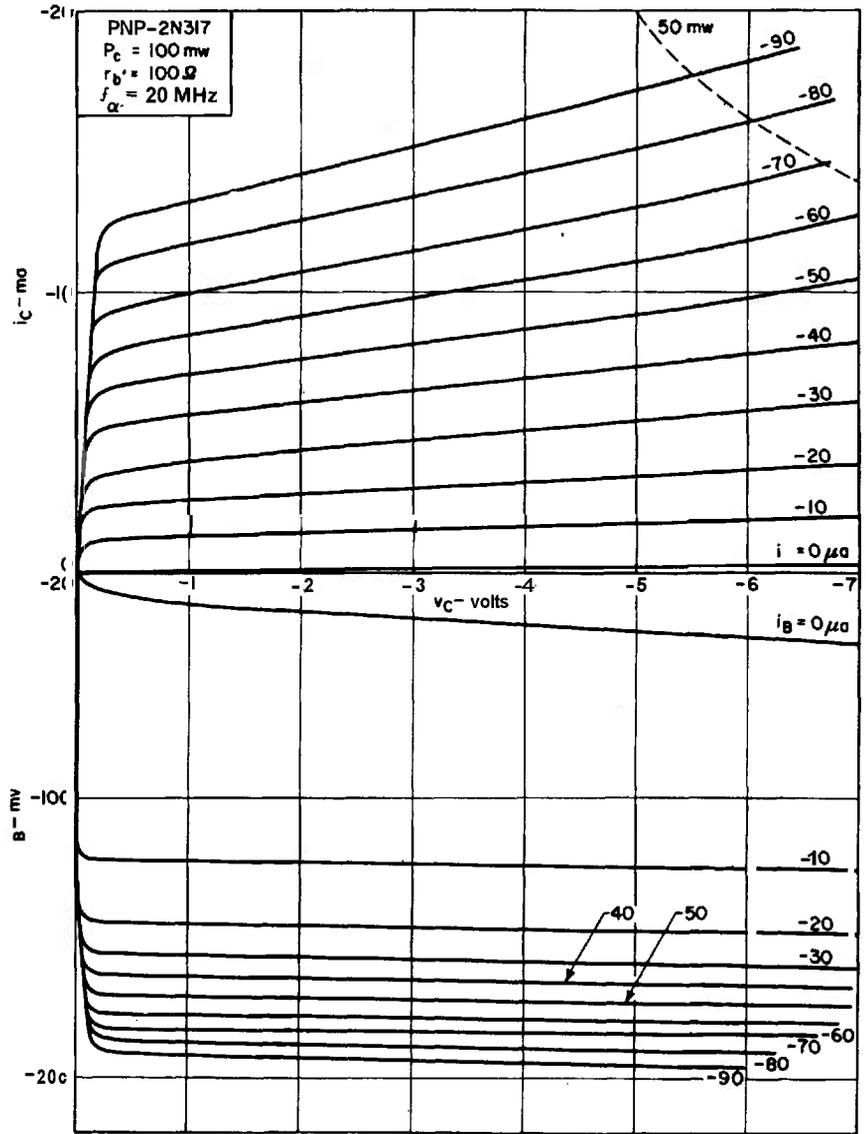


Fig. F-33. PNP-2N317

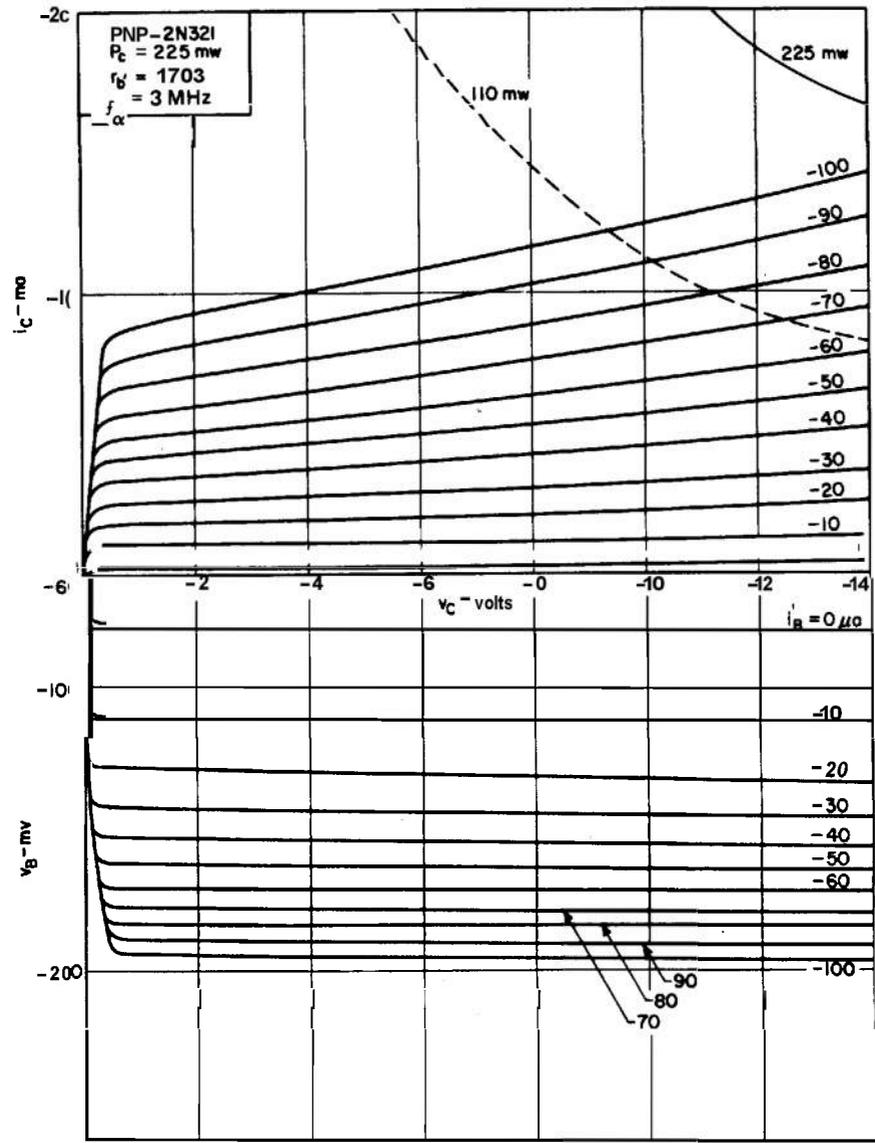


Fig. F-34. PNP-2N321

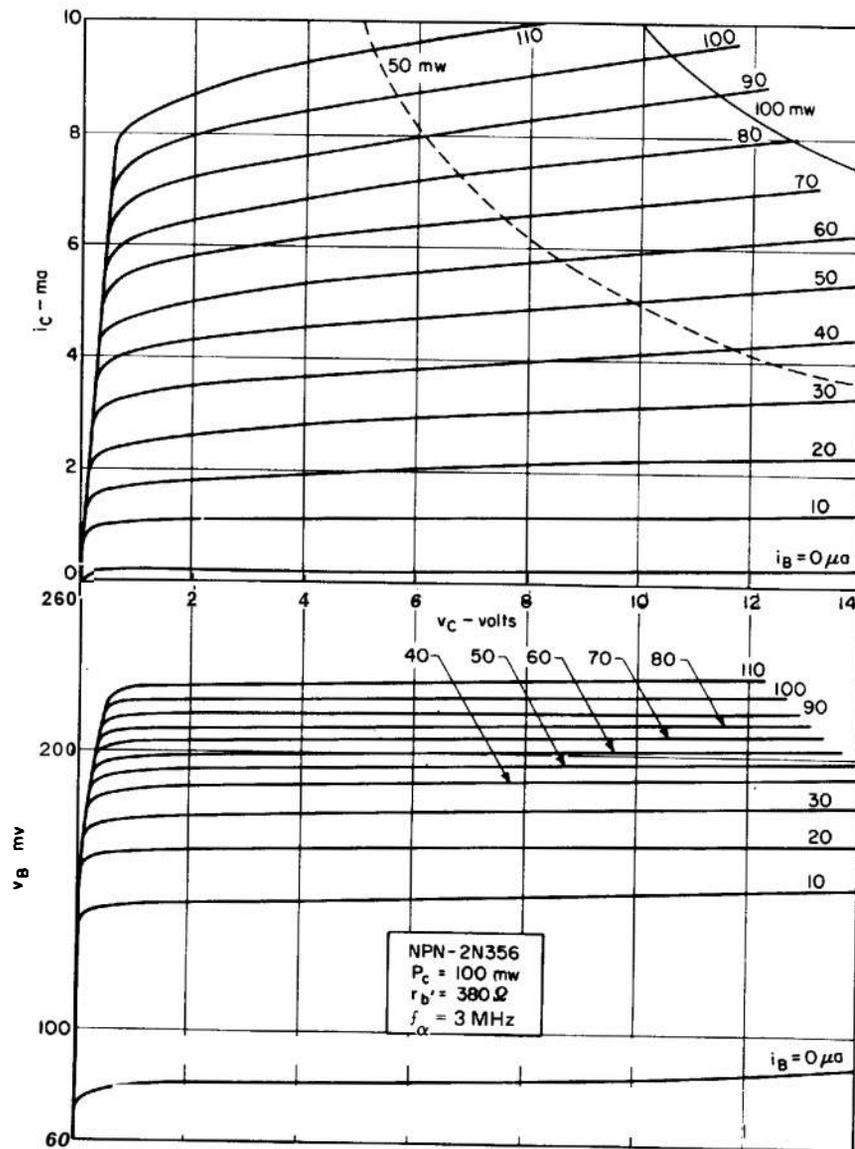


Fig. F-35. NPN-2N356

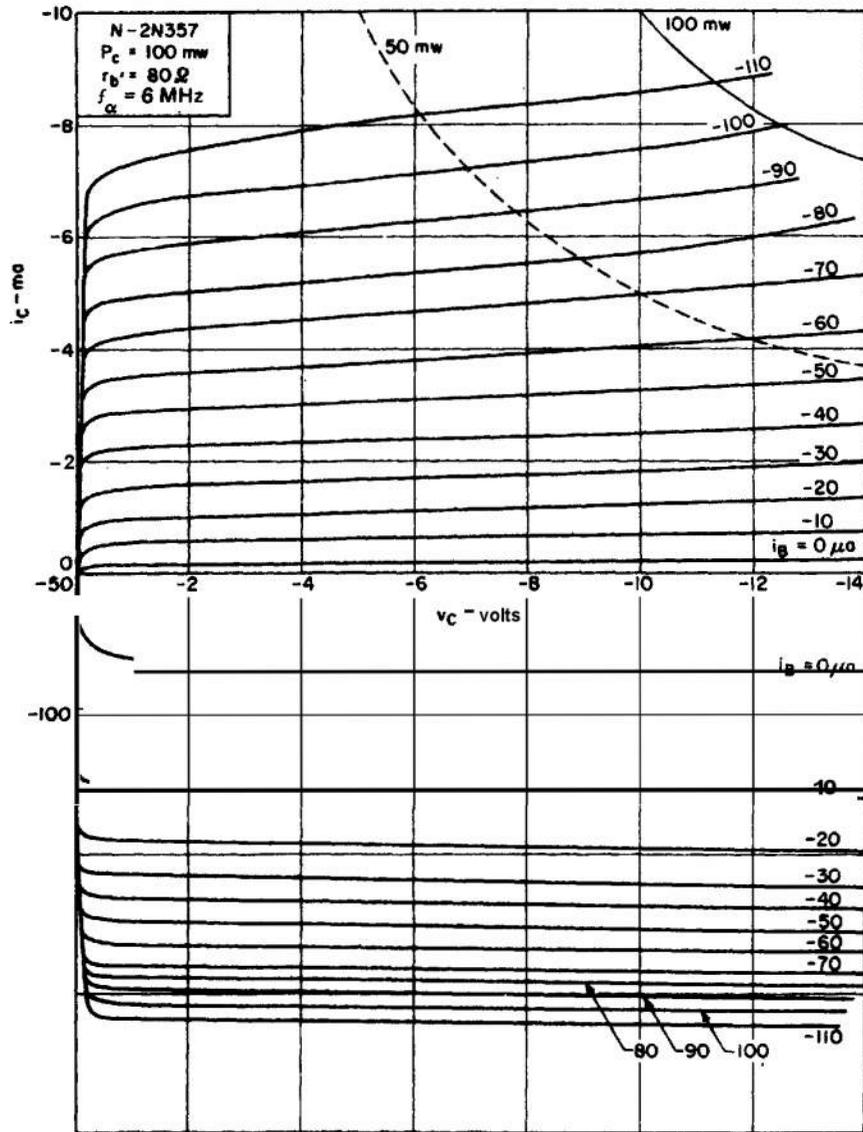


Fig. F-36. N-2N357

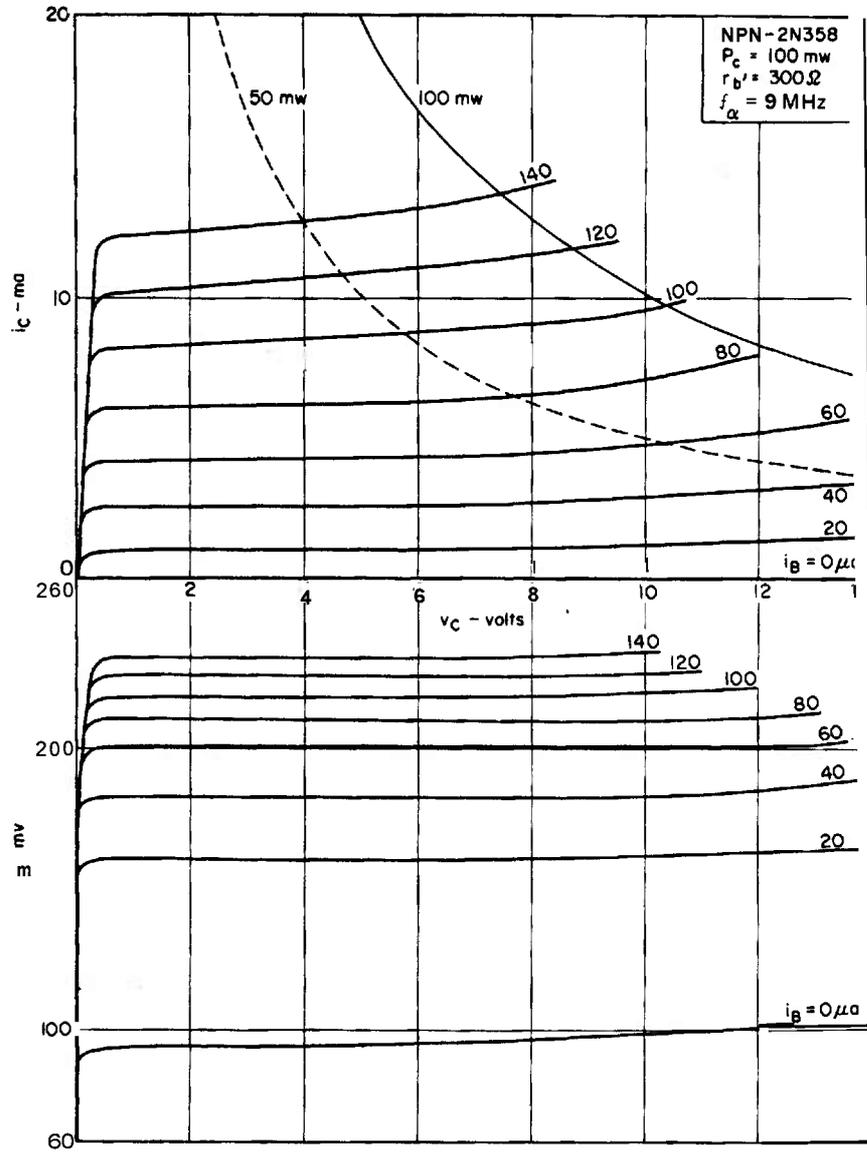


Fig. F-37. NPN-2N358

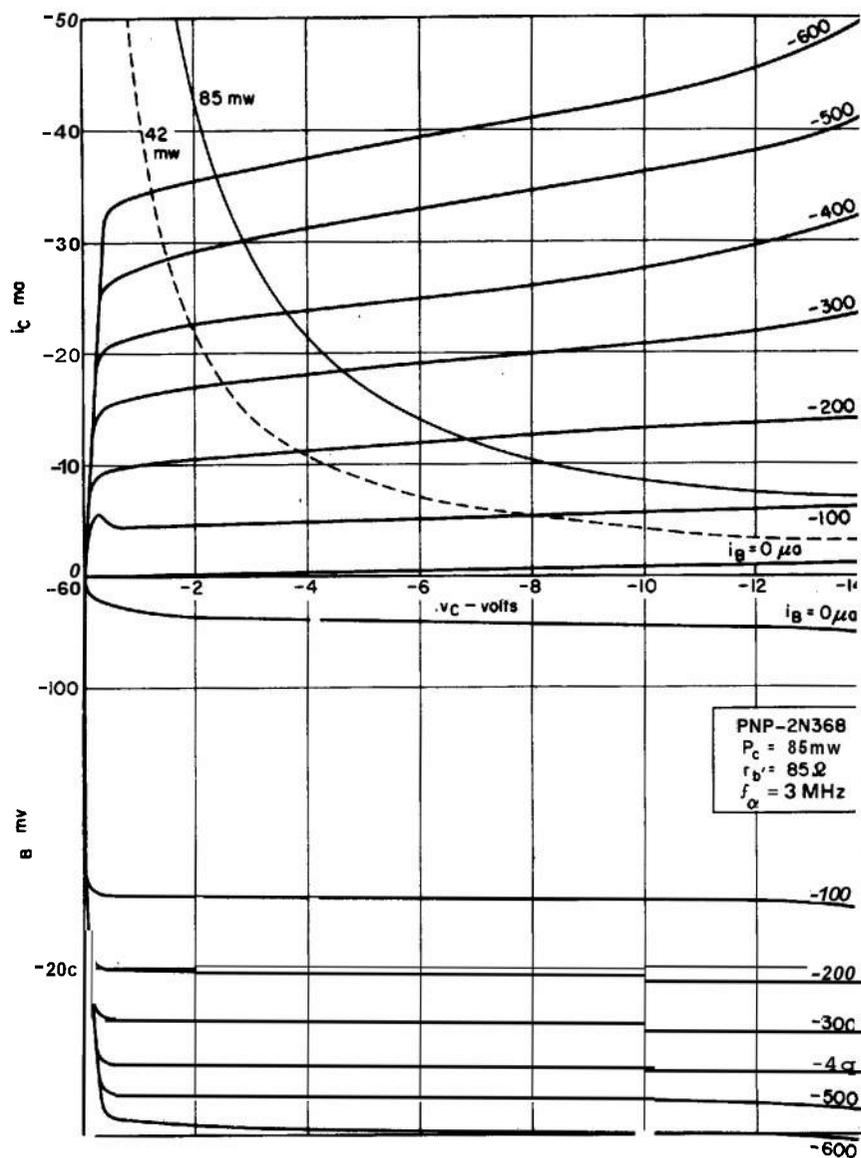


Fig. F-38. PNP-2N368

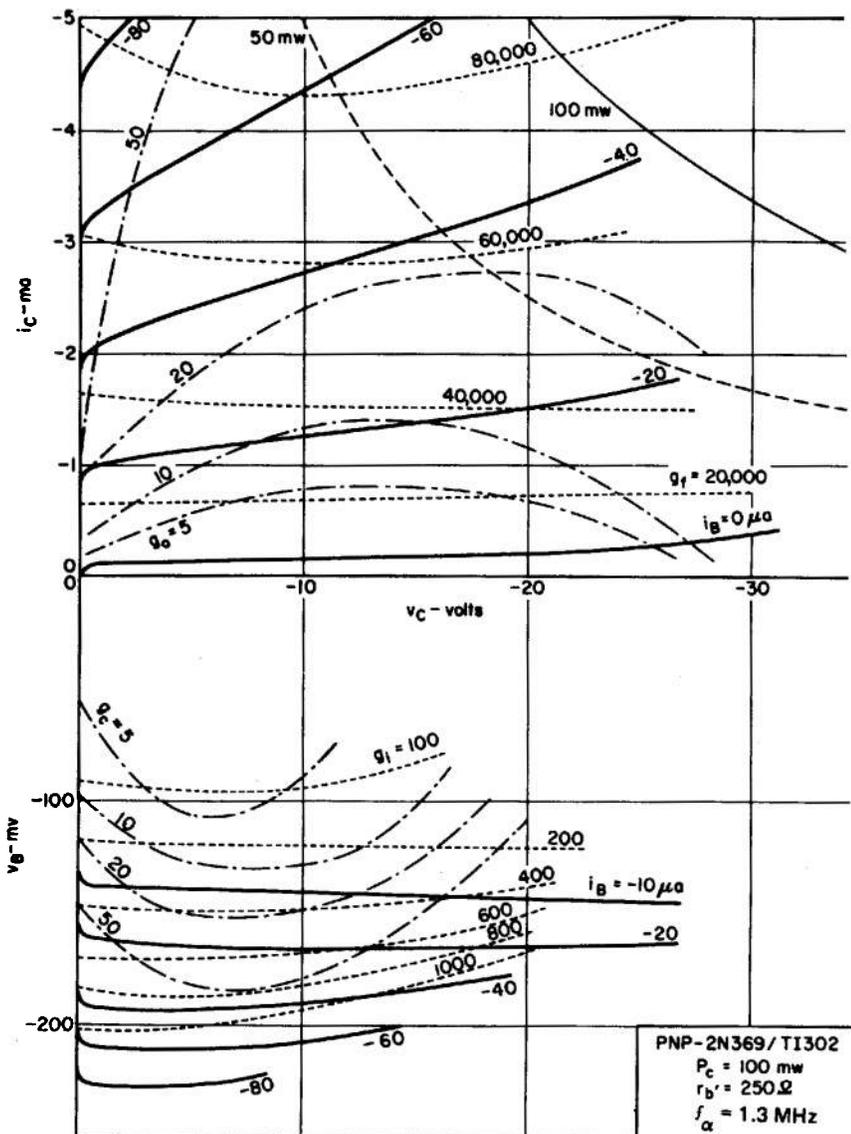


Fig. F-39. PNP-2N369/TI302

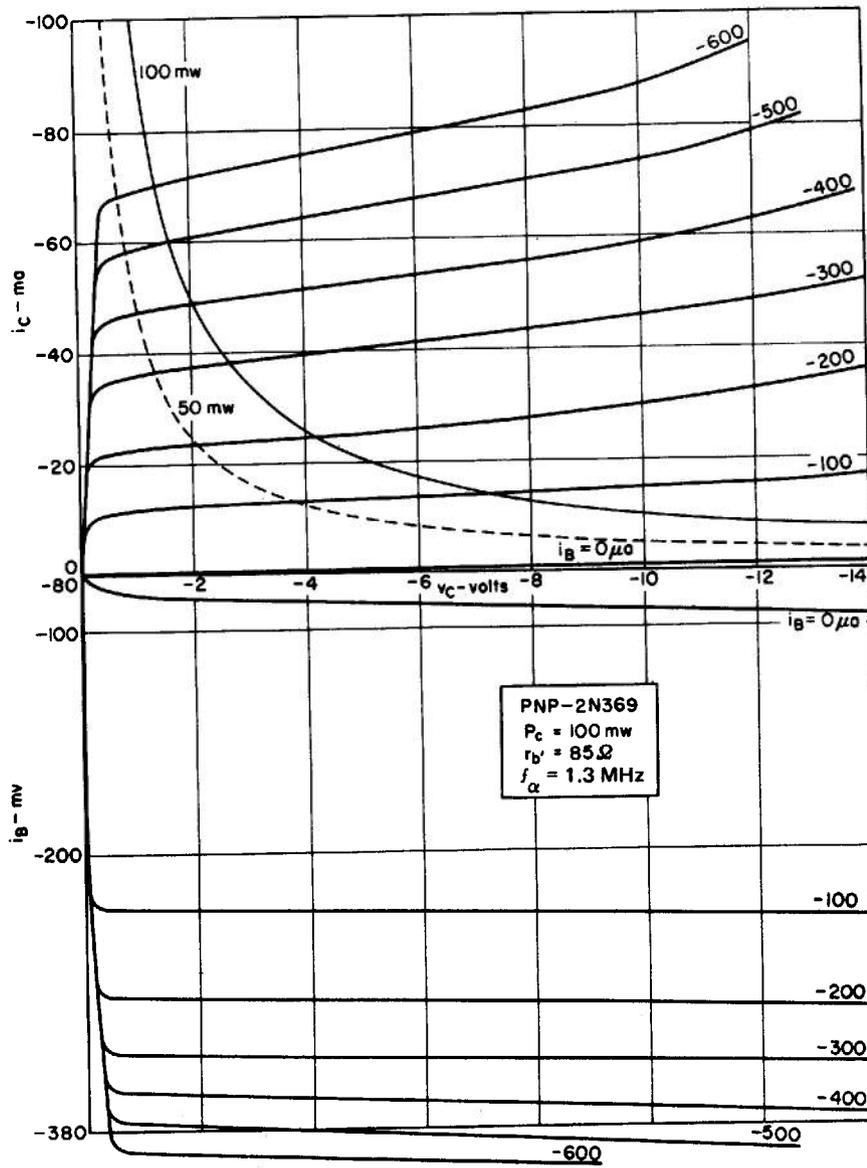


Fig. F-40. PNP-2N369

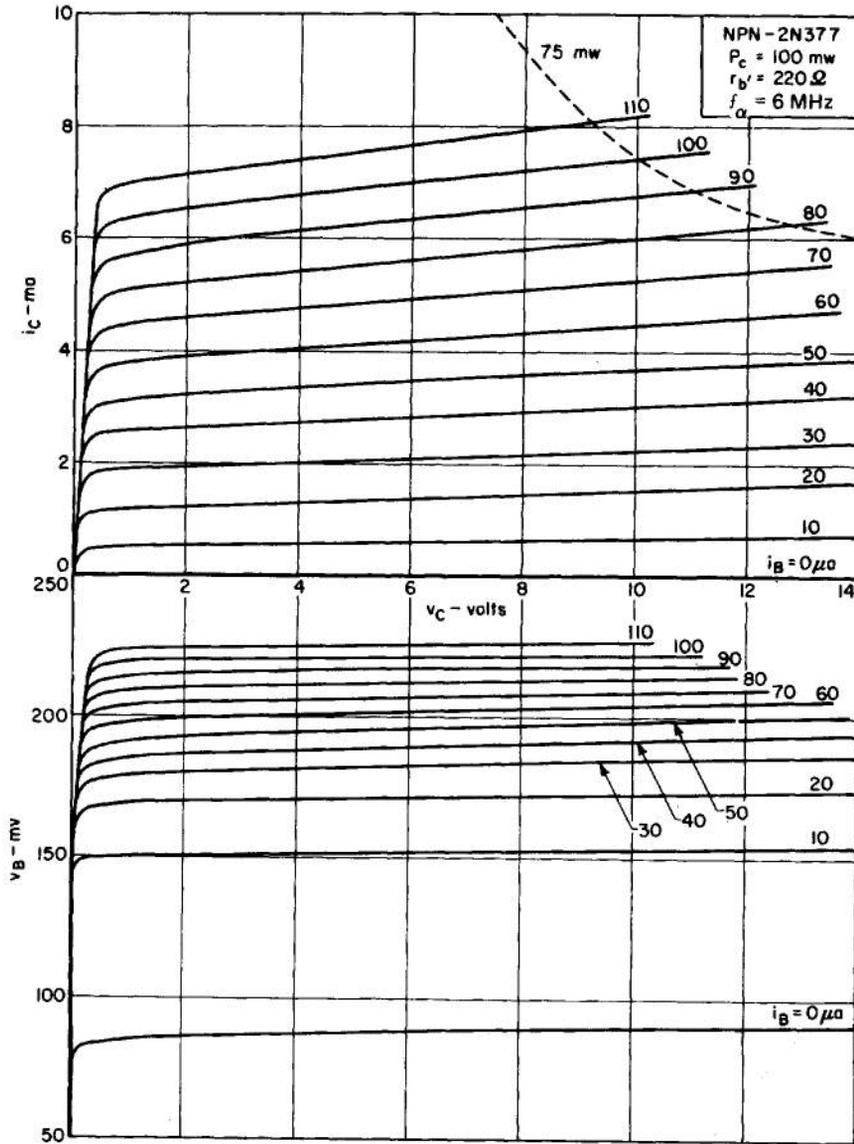


Fig. F-41. NPN-2N377

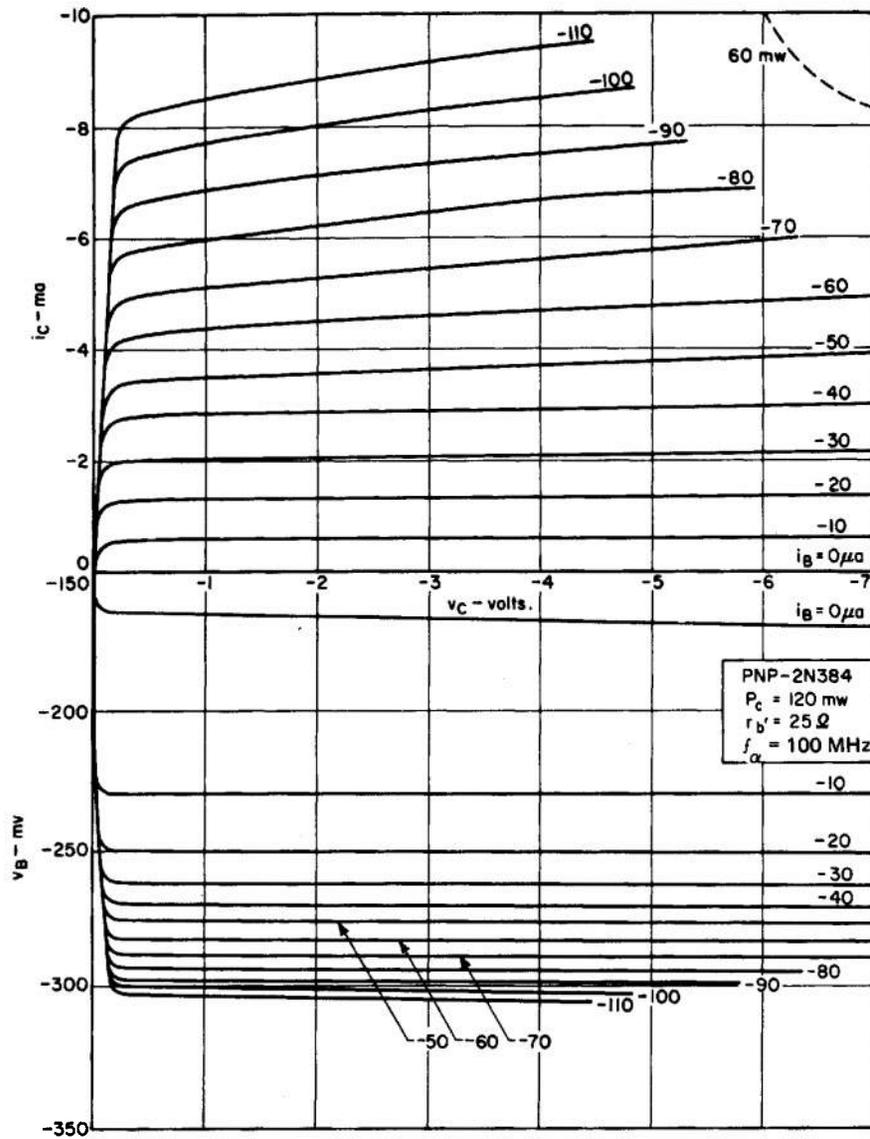


Fig. F-42. PNP-2N384

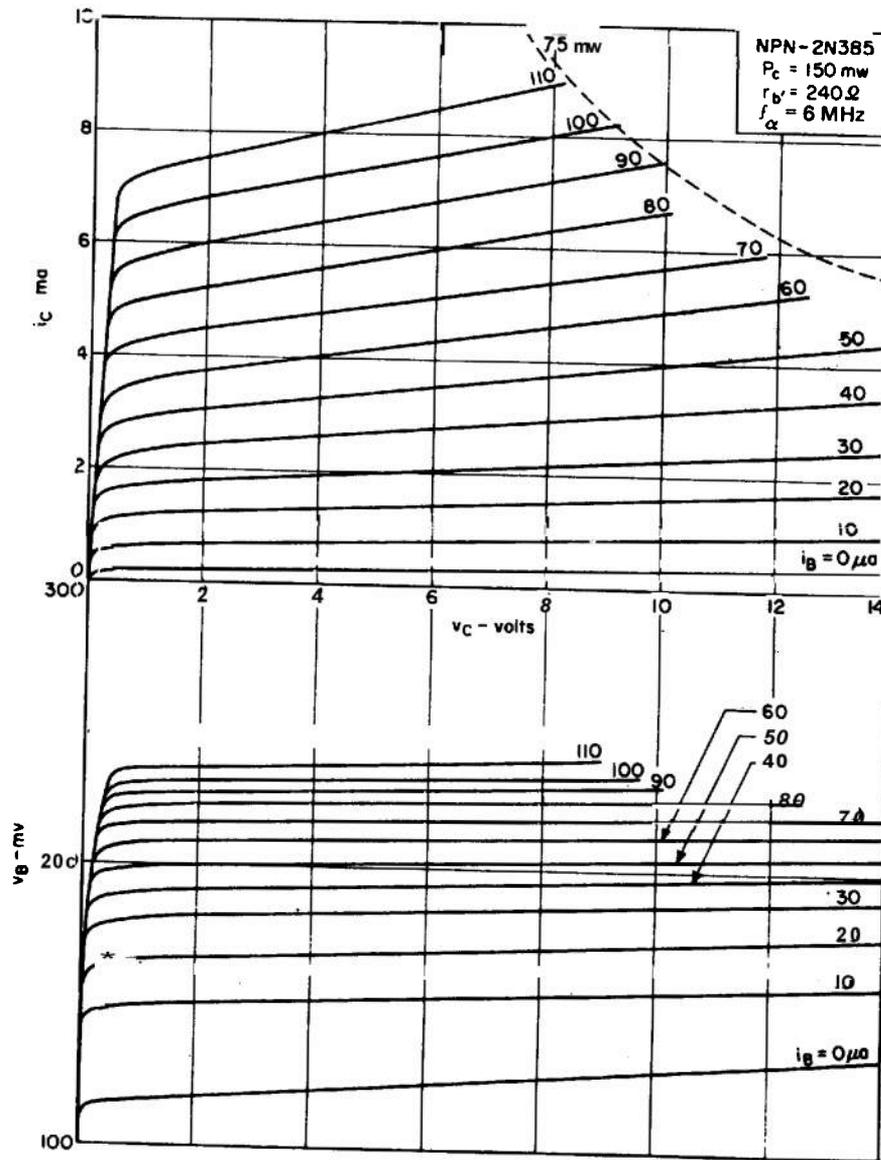


Fig. F-43. NPN-2N385

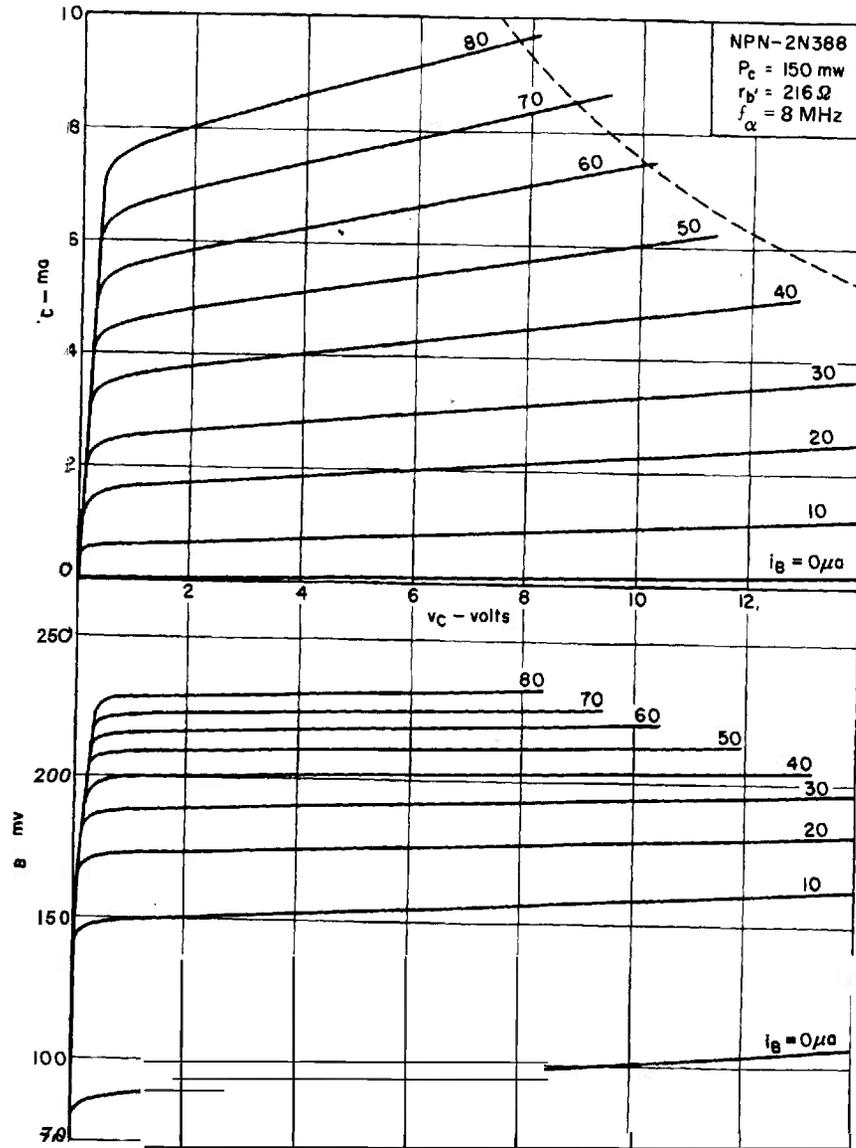


Fig. F-44. NPN-2N388

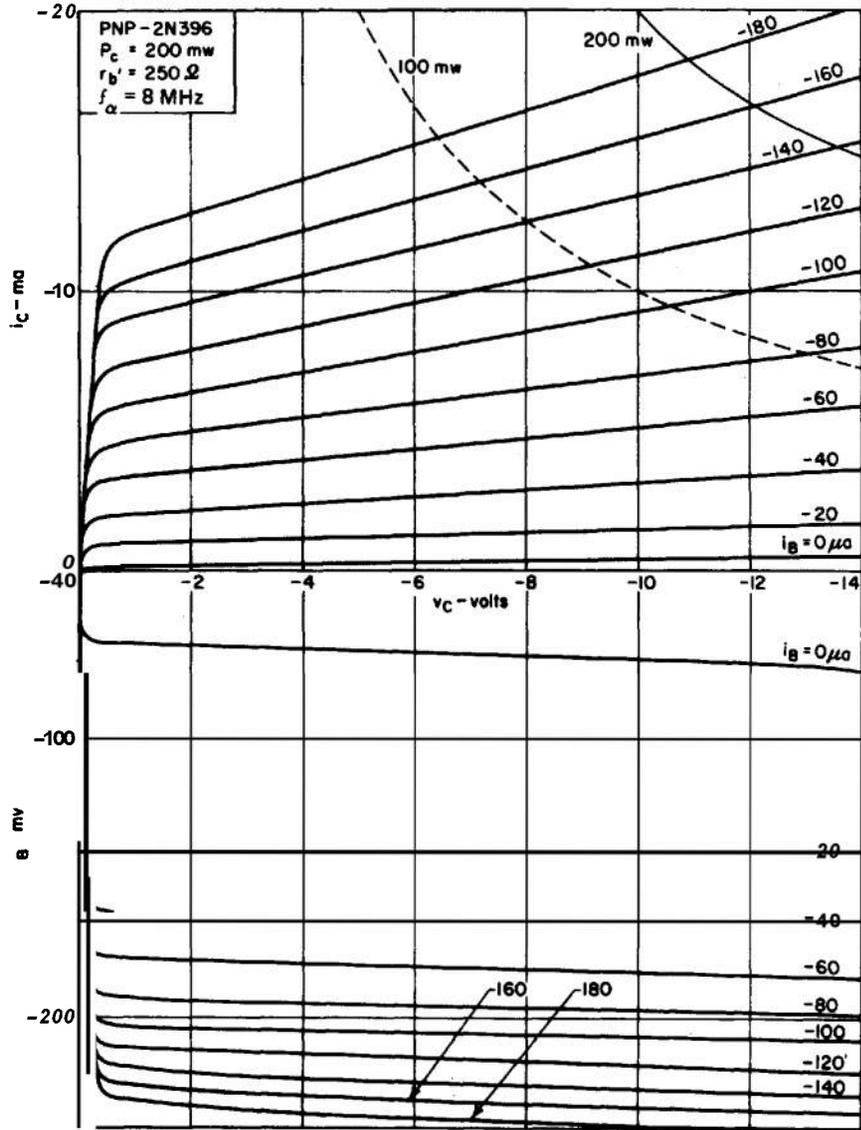


Fig. F-45. PNP-2N396

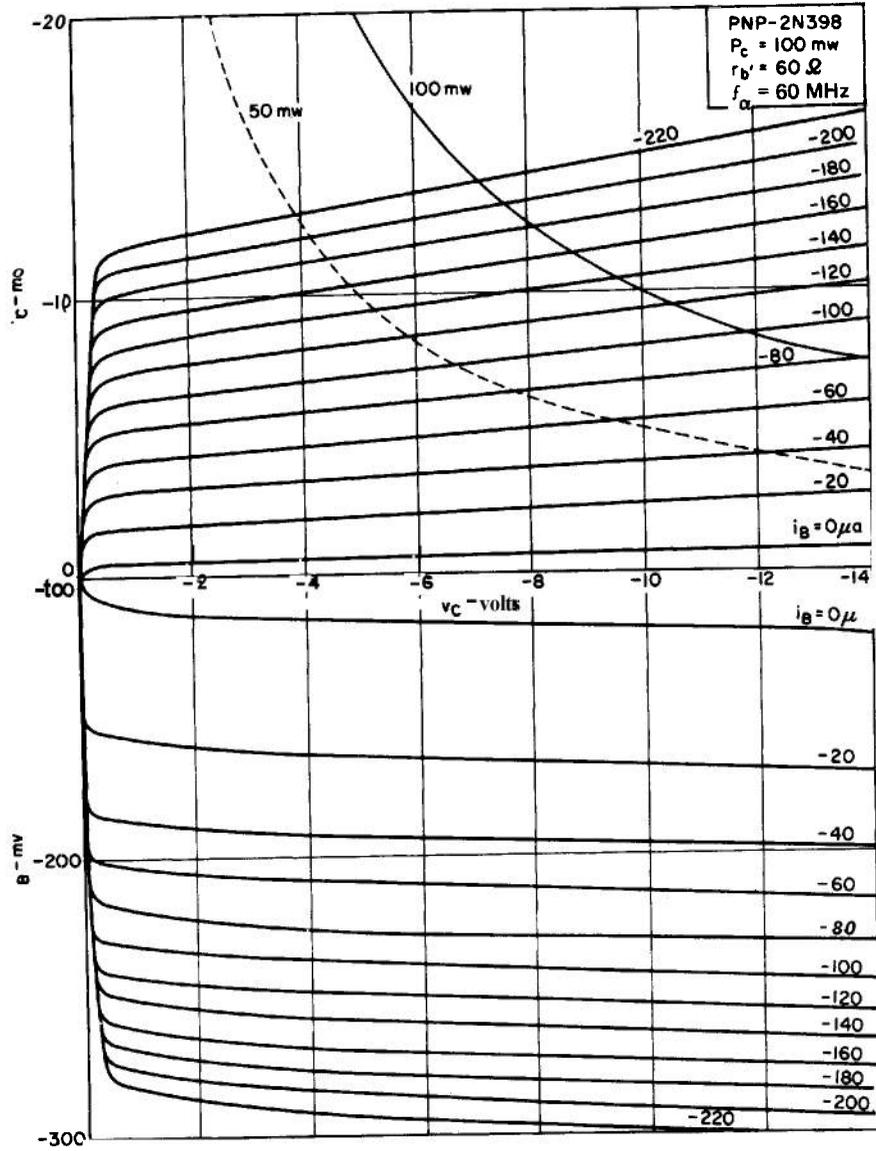
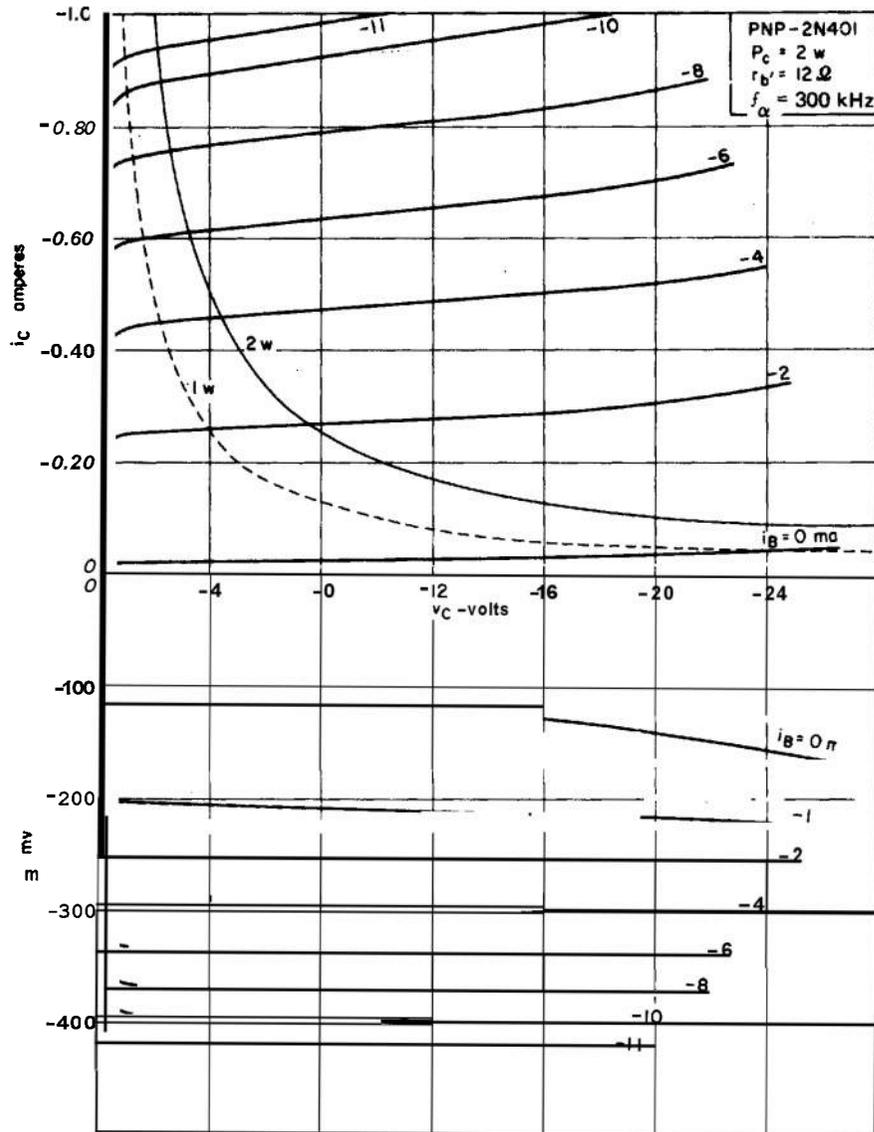


Fig. F-46. PNP-2N398



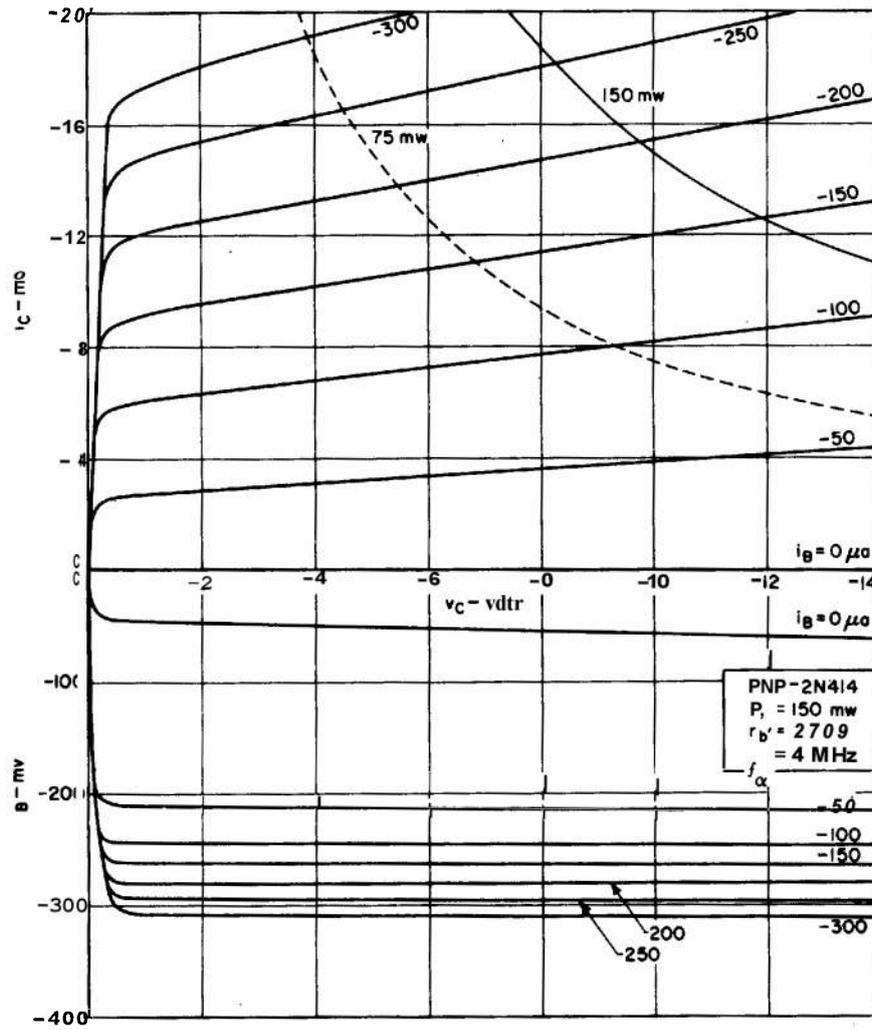


Fig. F-48. PNP-2N414

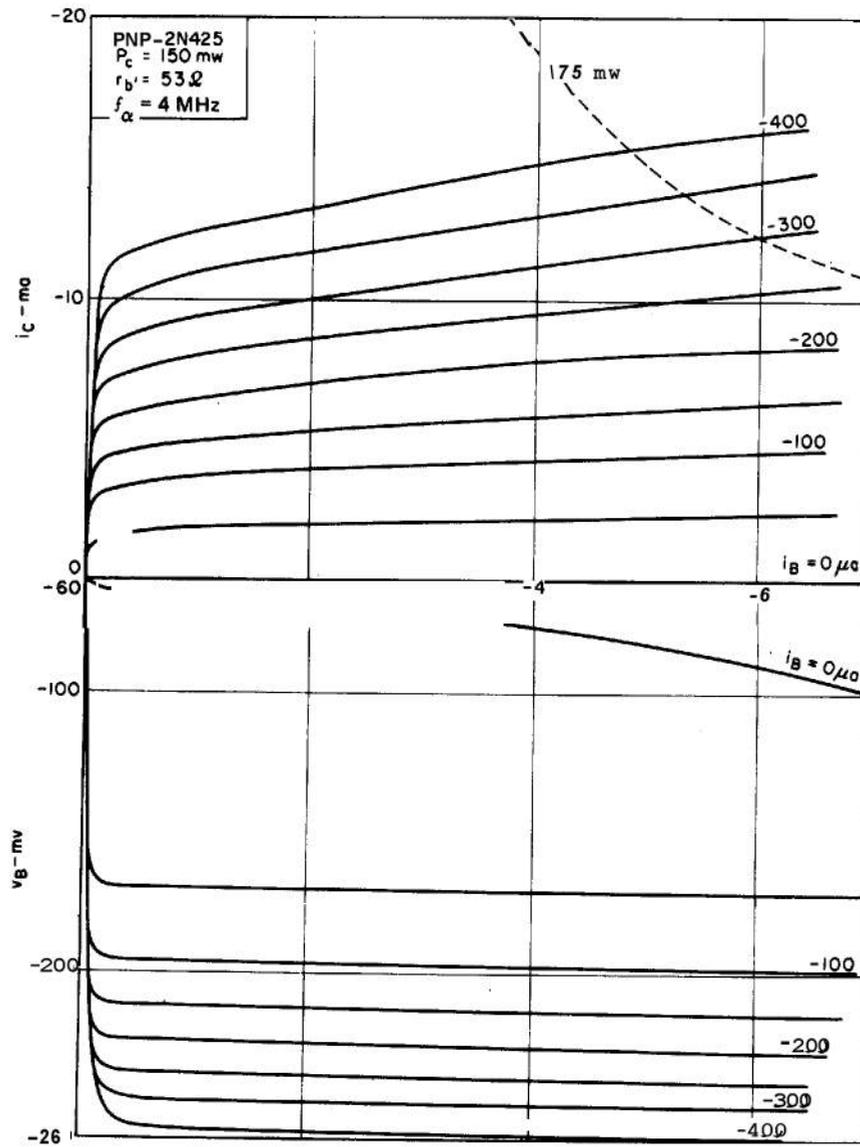


Fig. F-49. PNP-2N425

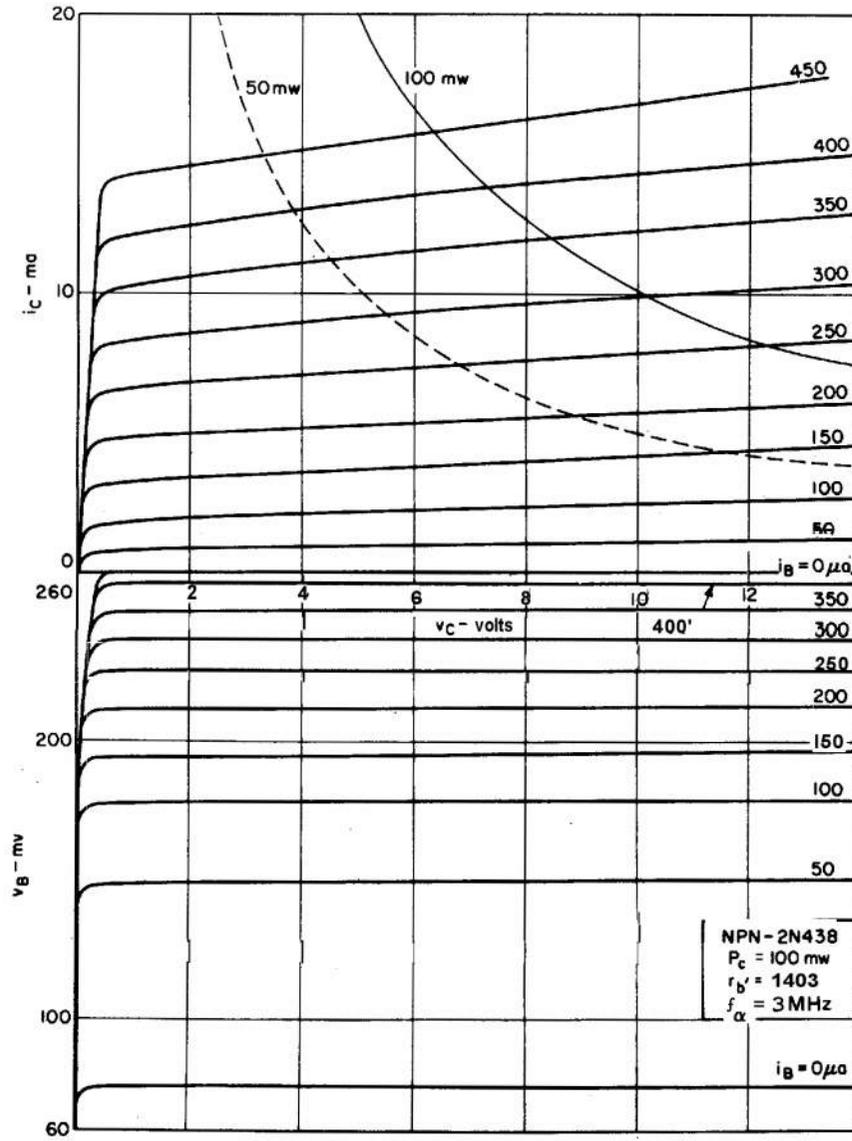


Fig. F-50. NPN-2N438

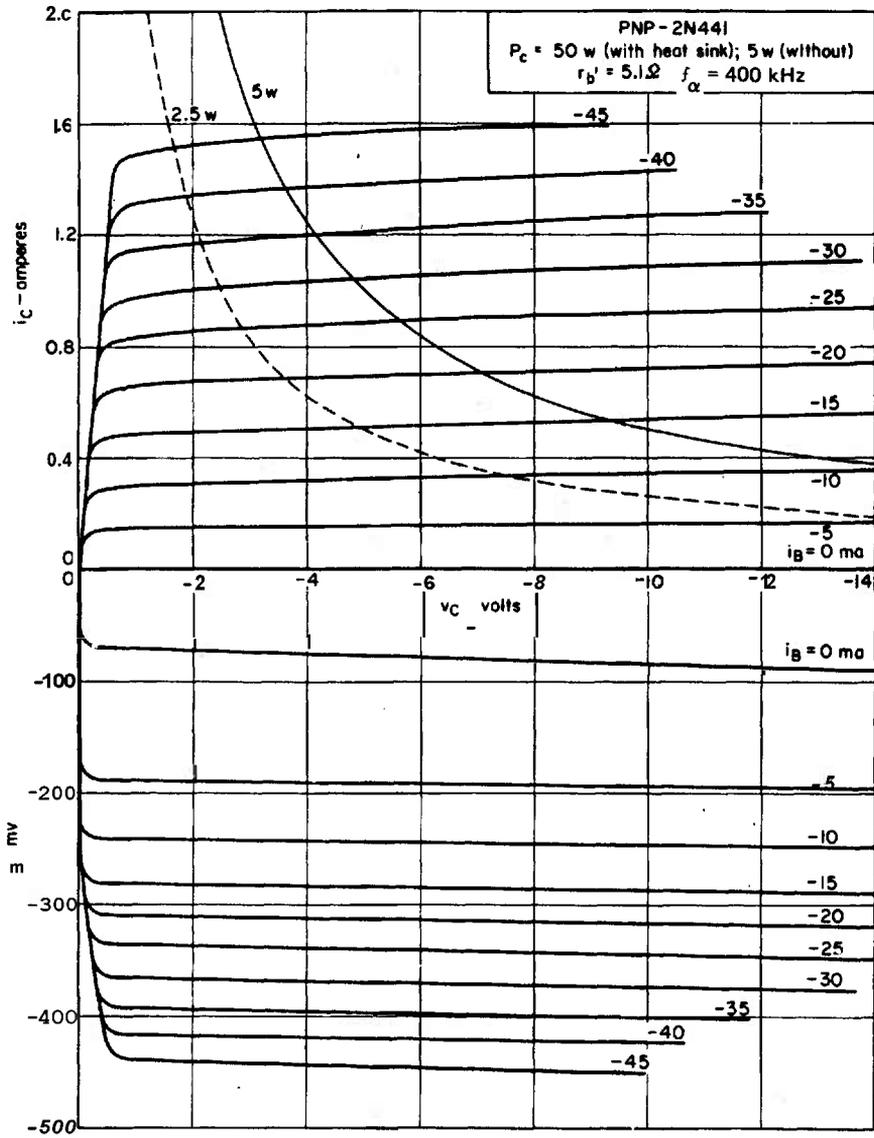


Fig. F-51. PNP-2N441

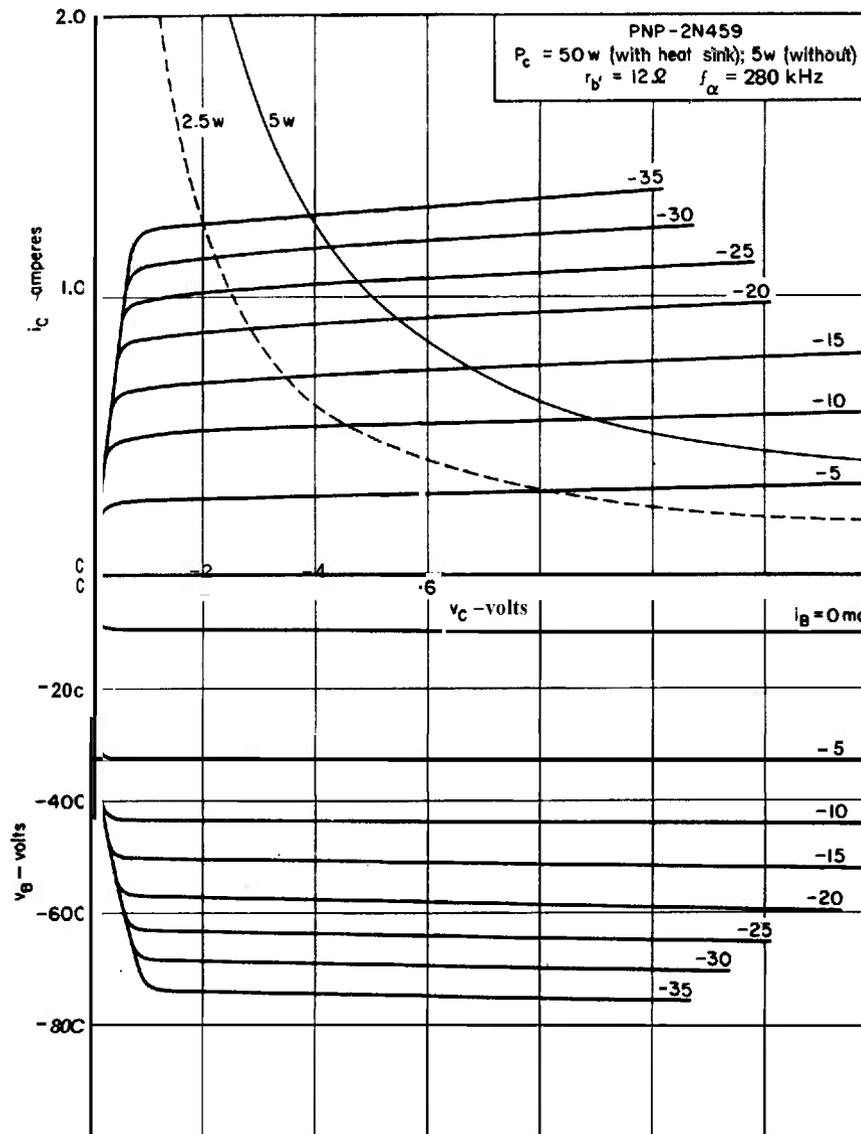


Fig. F-52. PNP-2N459

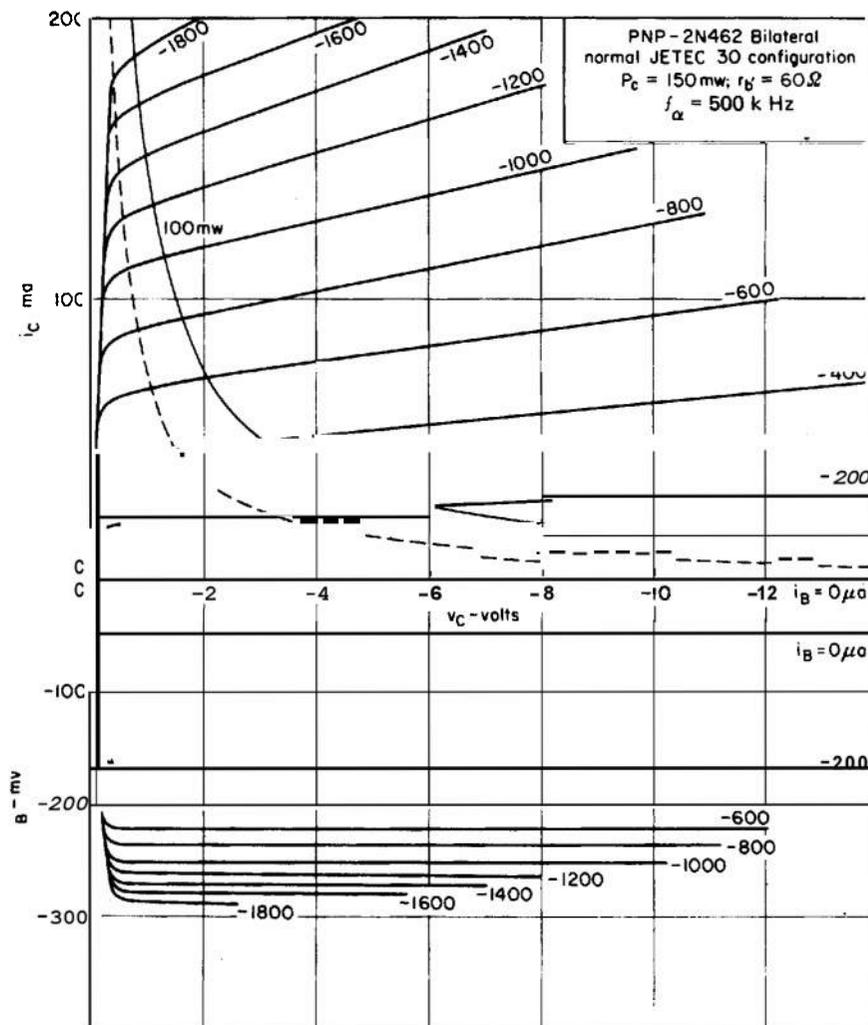


Fig. F-53. PNP-2N462 Bilateral

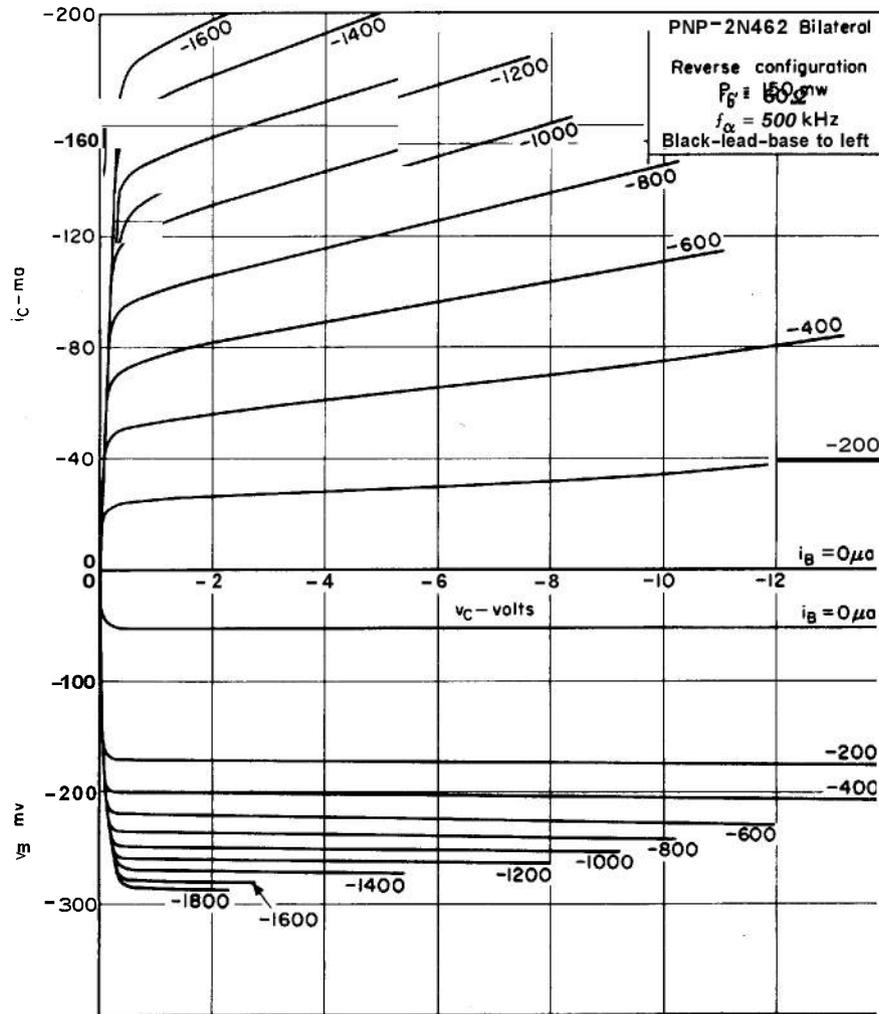


Fig. F-54. PNP-2N462 Bilateral

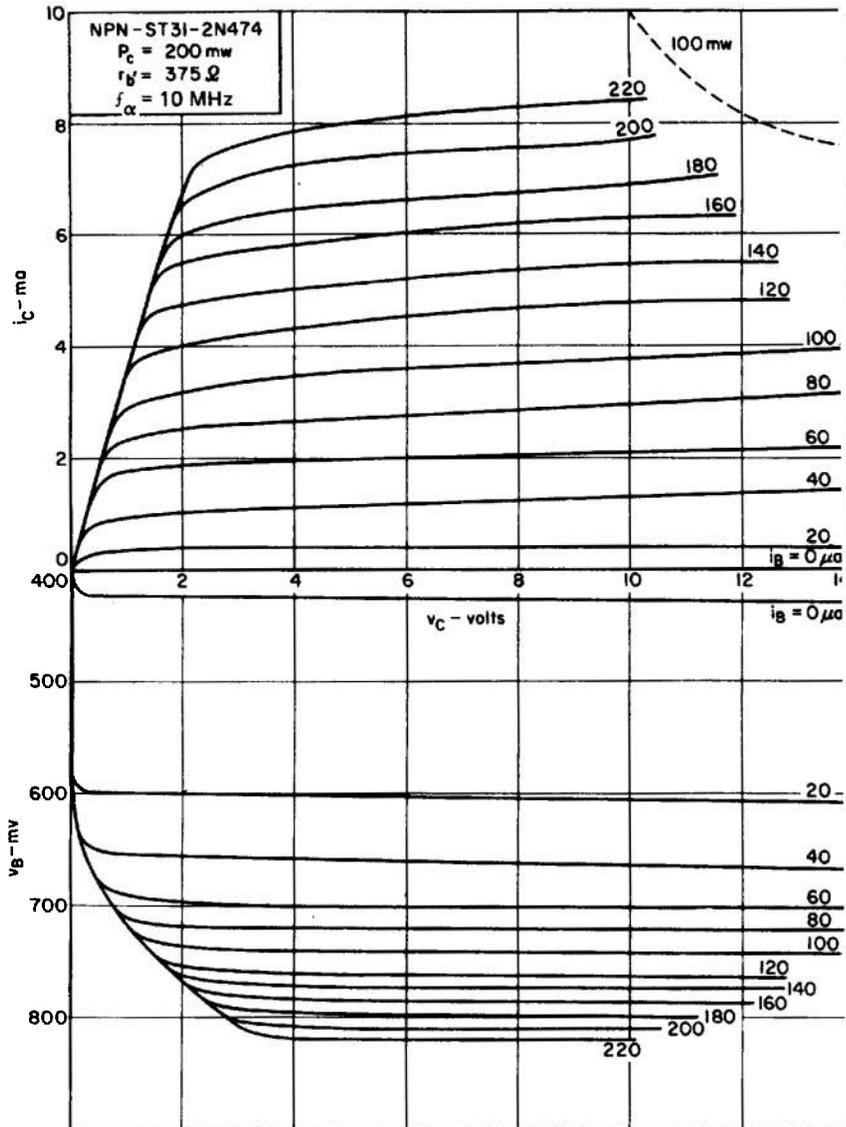


Fig. F-55. NPN-ST31-2N474

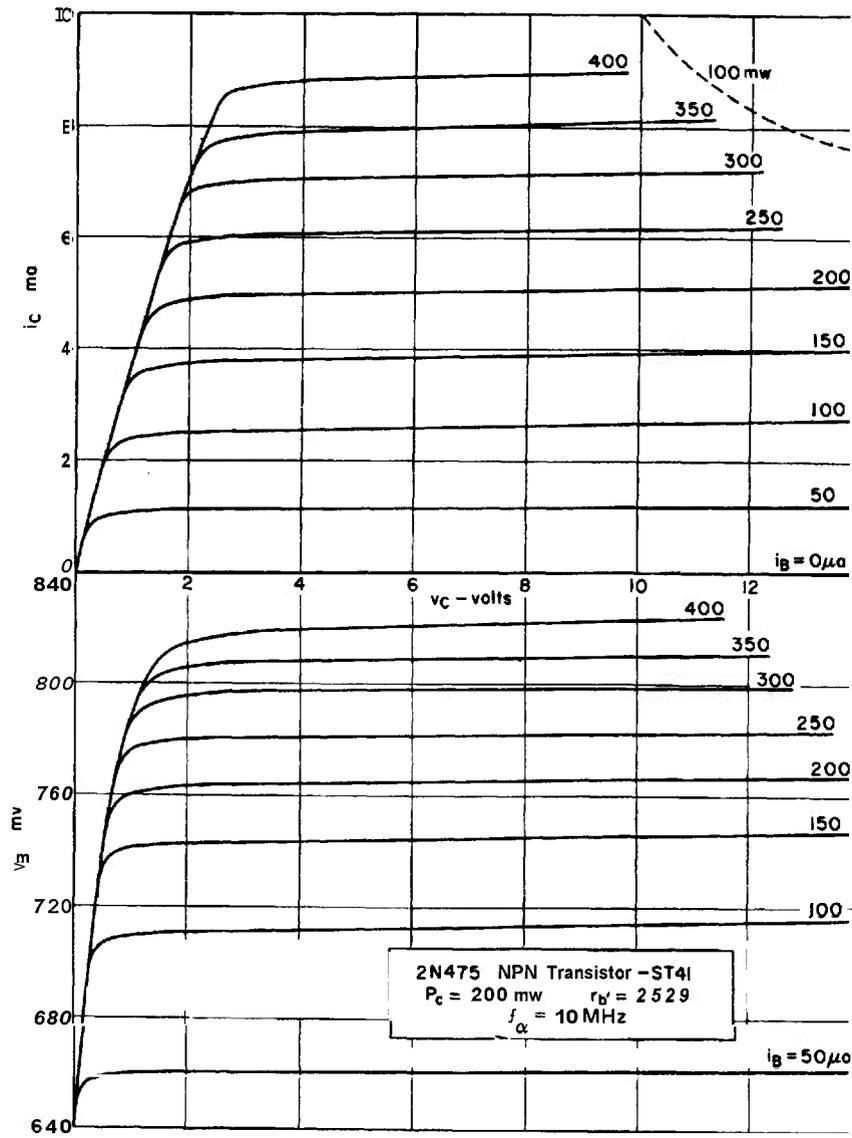


Fig. F-56. NPN-ST41-2N475

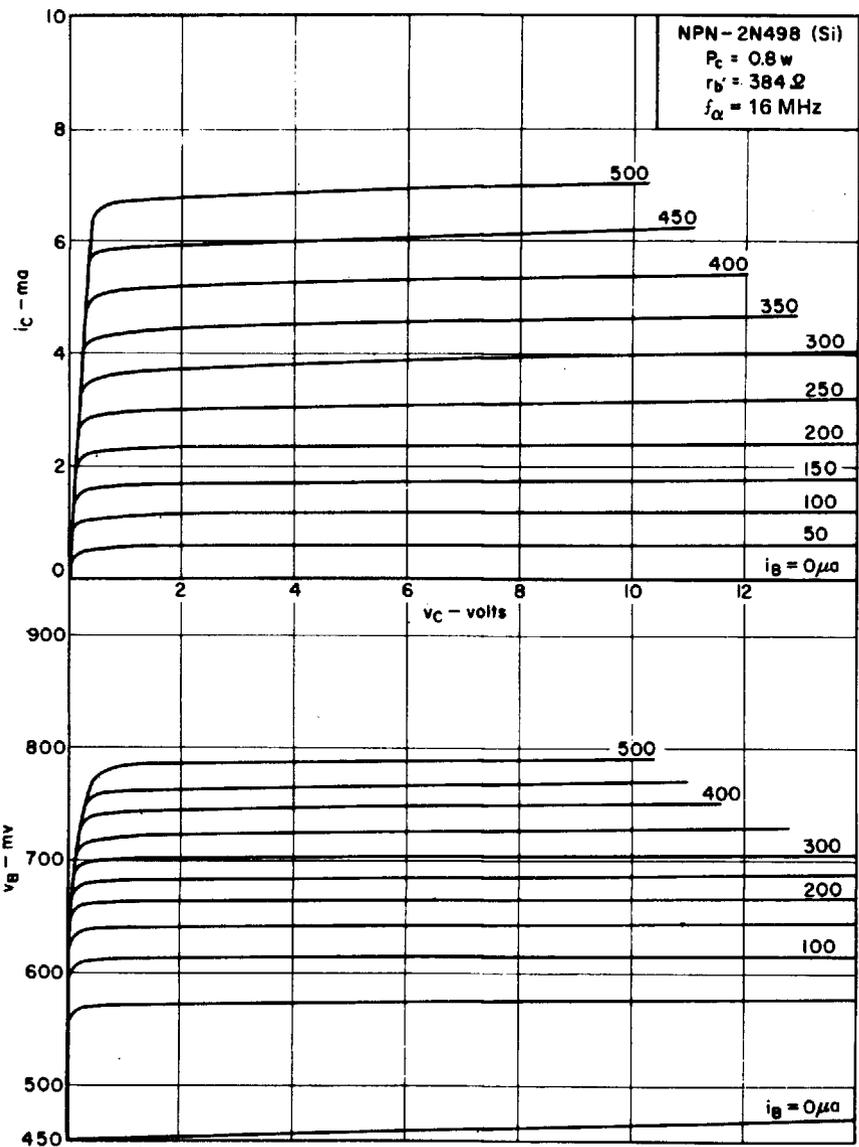


Fig. F-57. NPN-2N498 (Si)

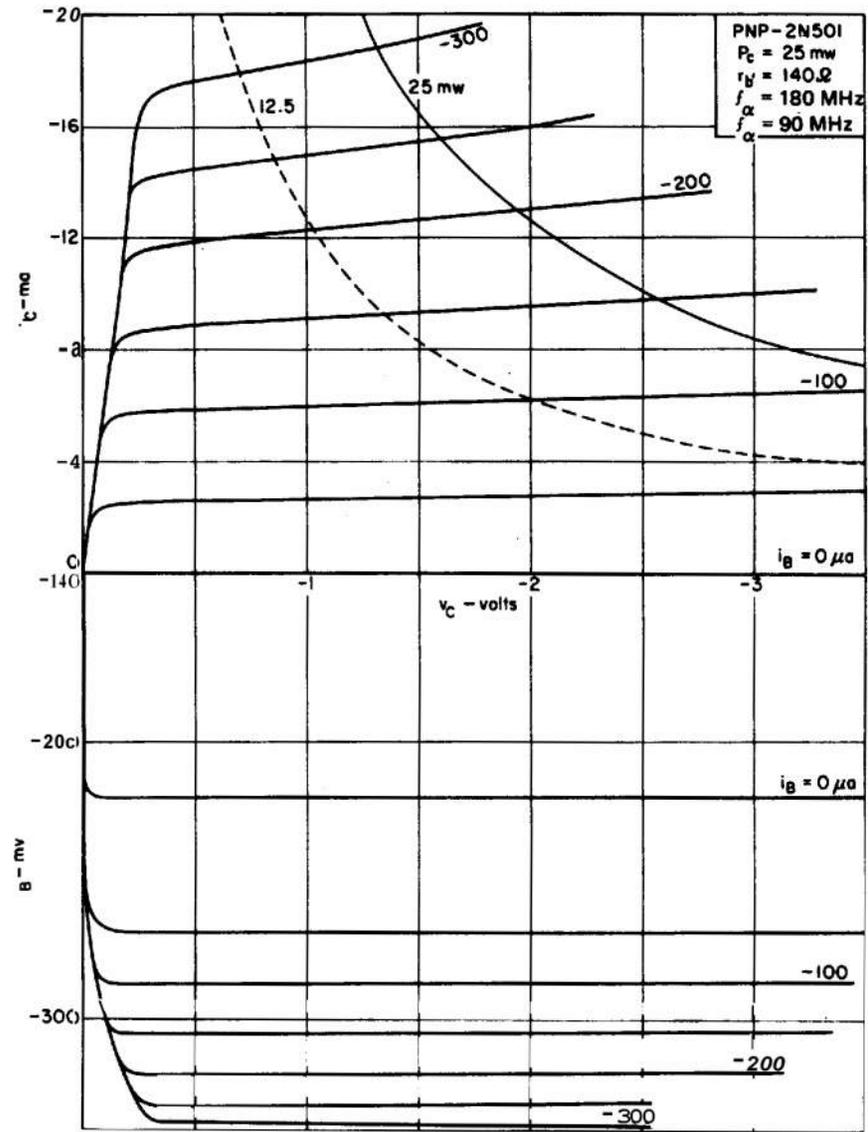


Fig. F-58. PNP-2N501

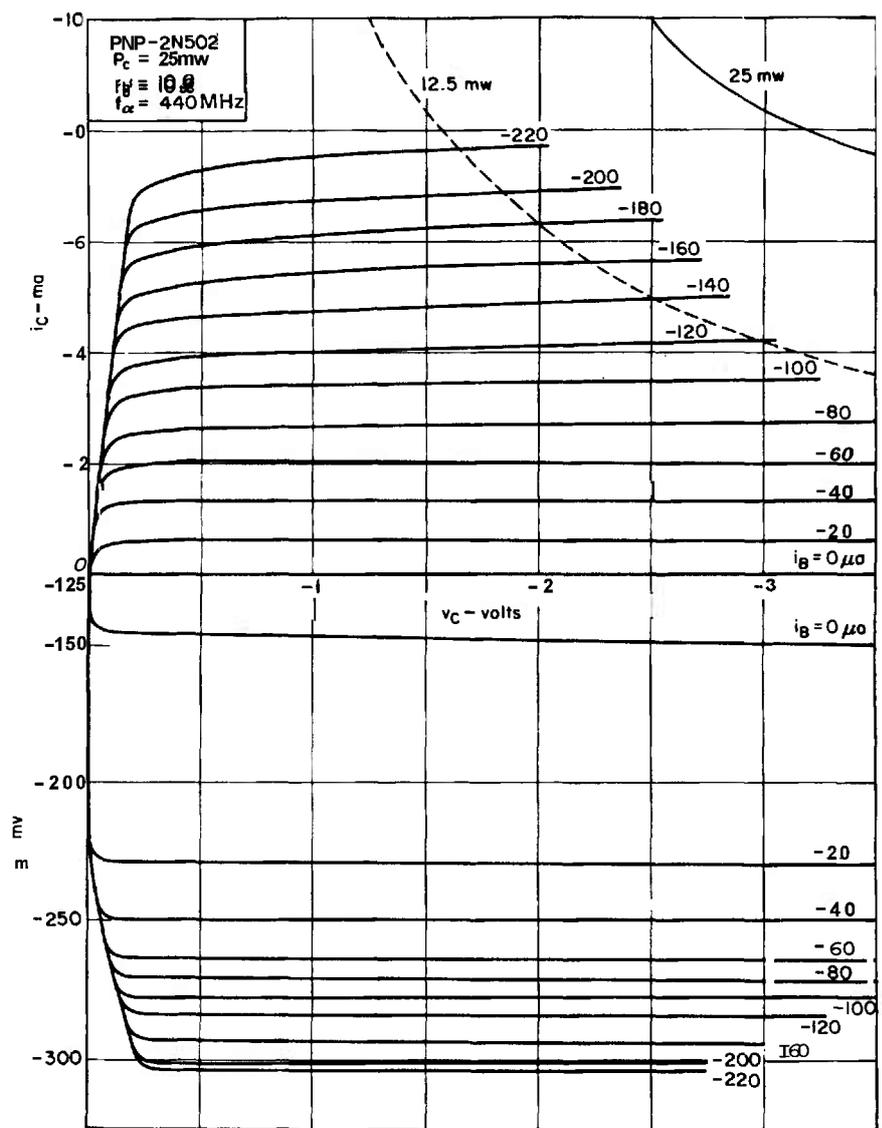
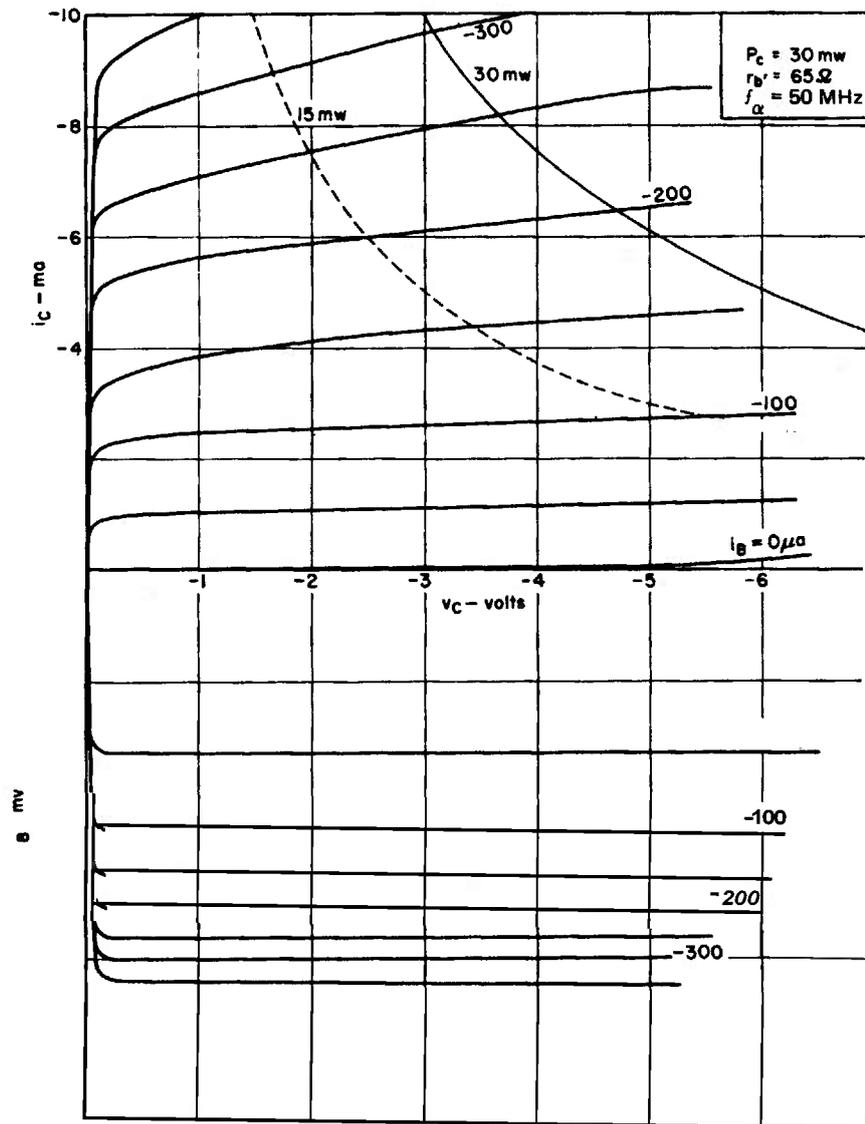


Fig. F-59. PNP-2N502



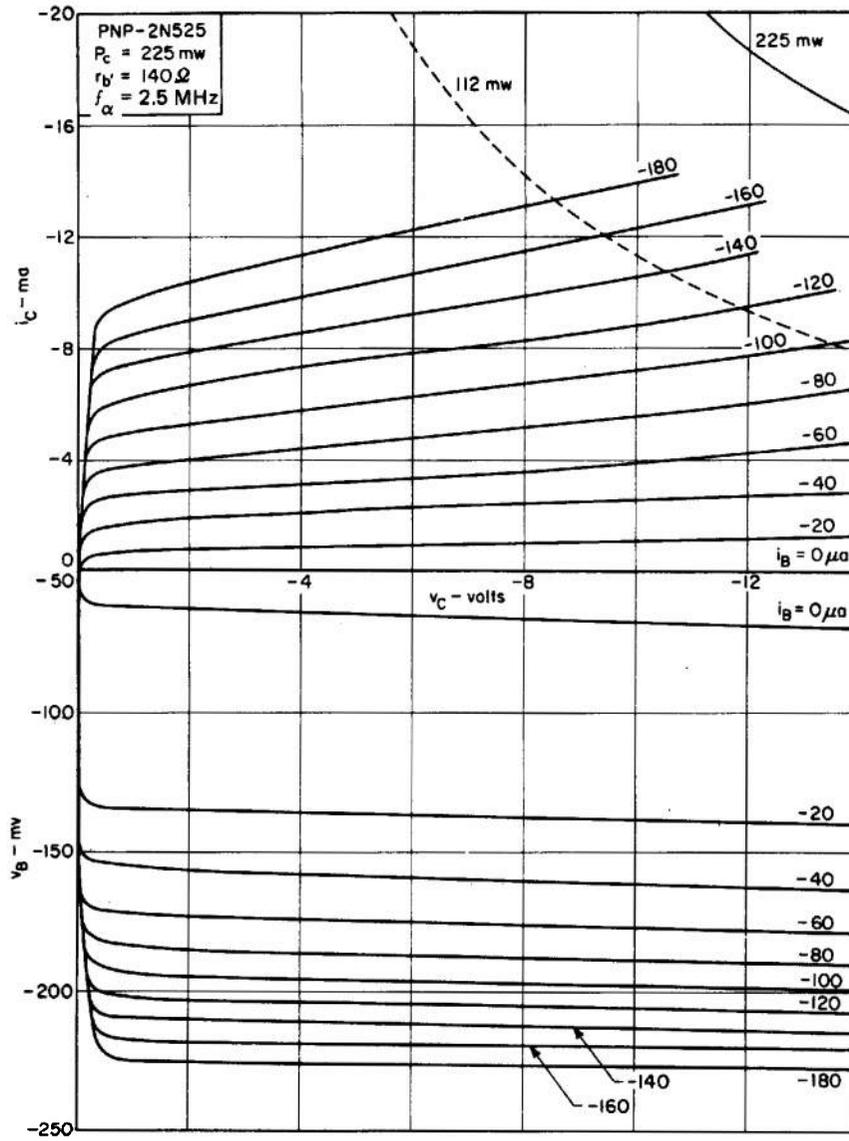


Fig. F-61. PNP-2N525

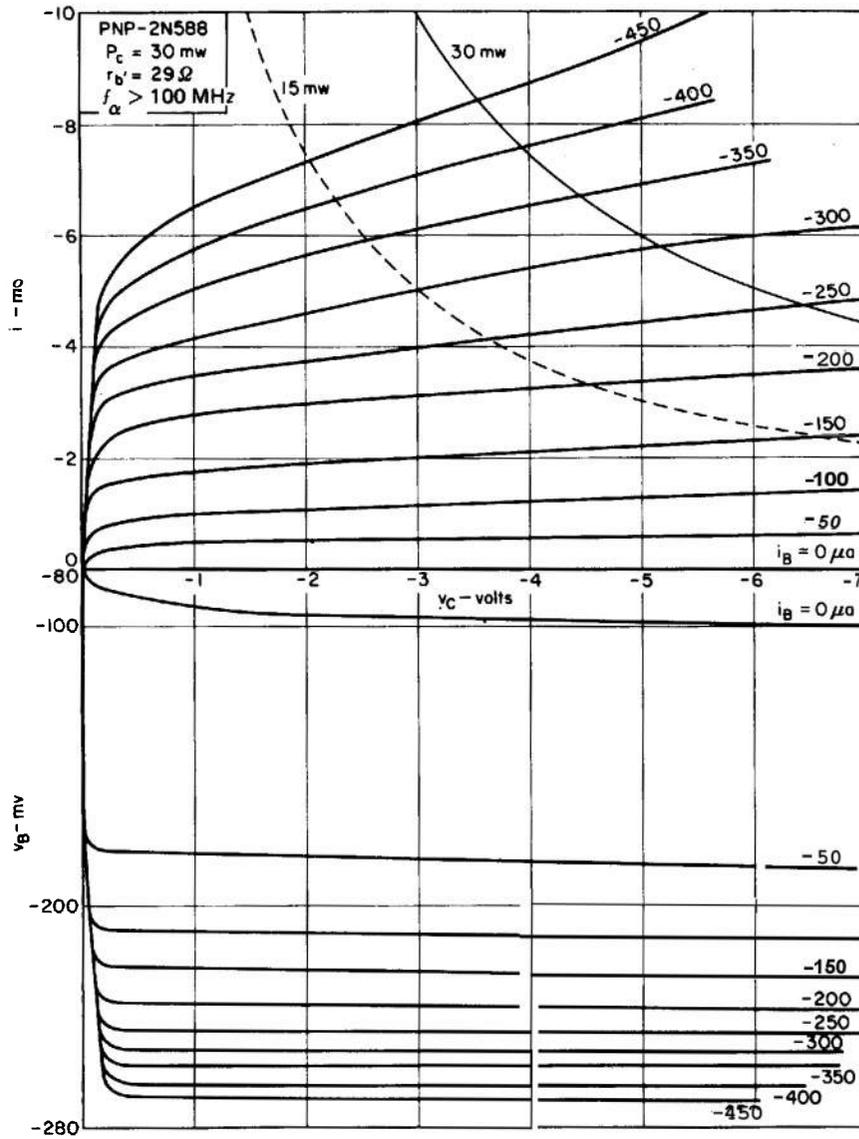


Fig. F-62. PNP-2N588

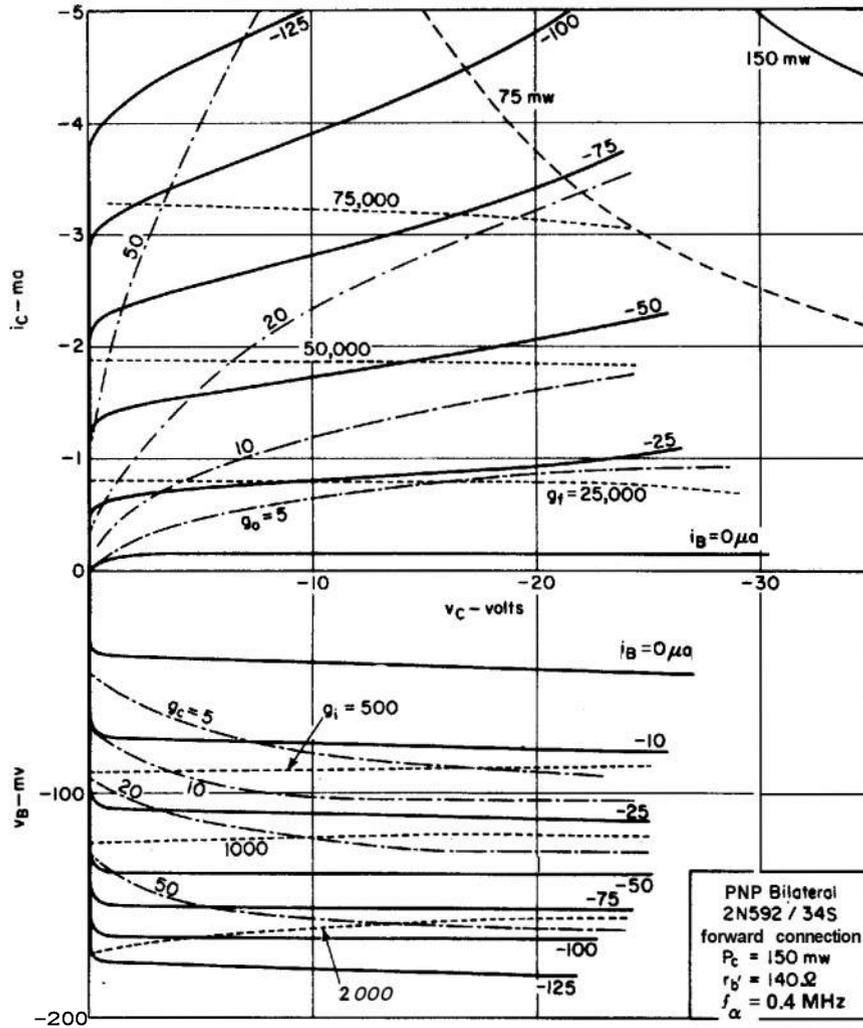


Fig. F-63. PNP-2N592/34S Bilateral

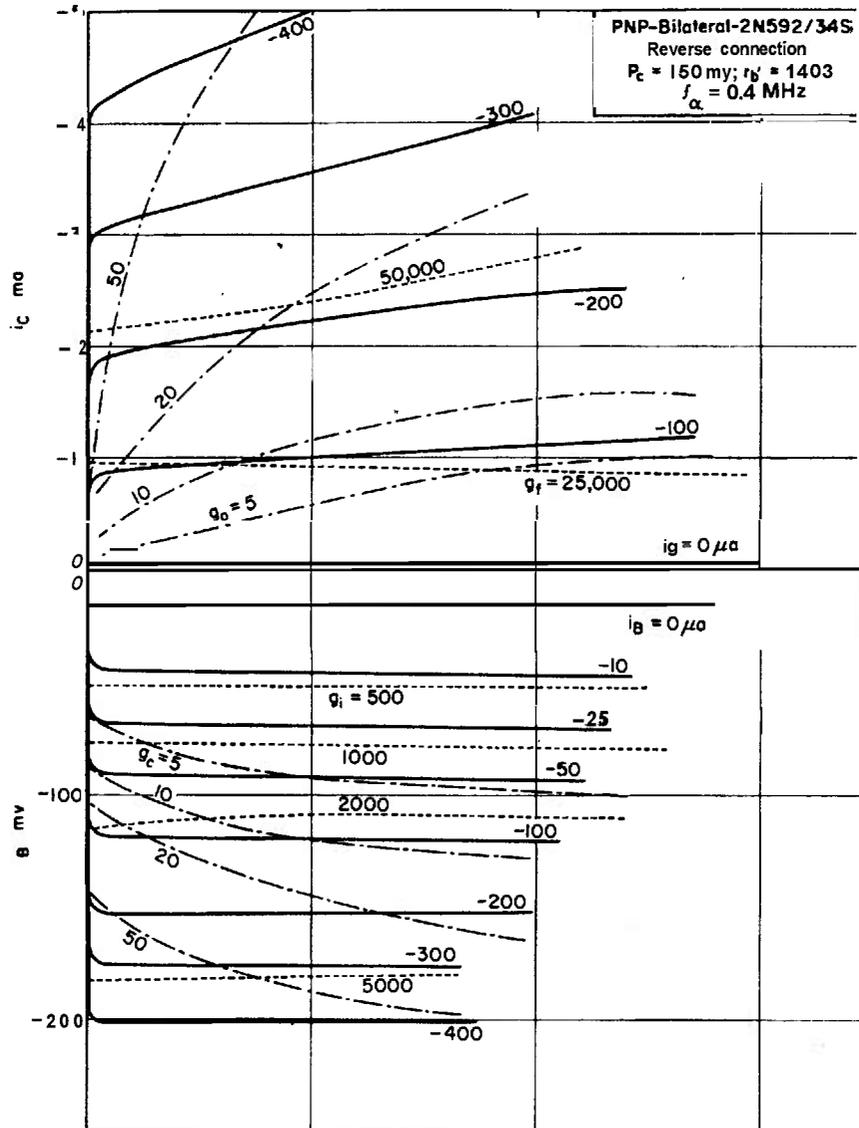


Fig. F-64. PNP-2N592/34S Bilateral

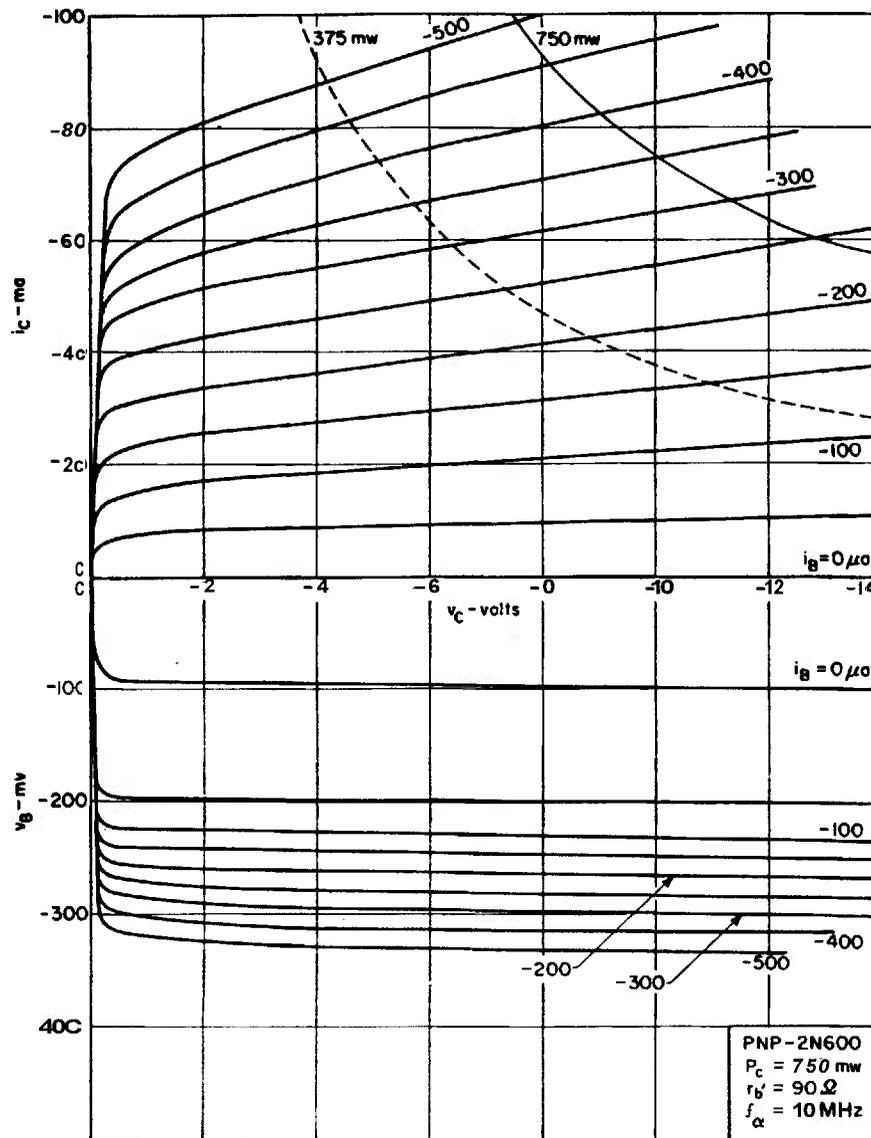


Fig. F-65. PNP-2N600

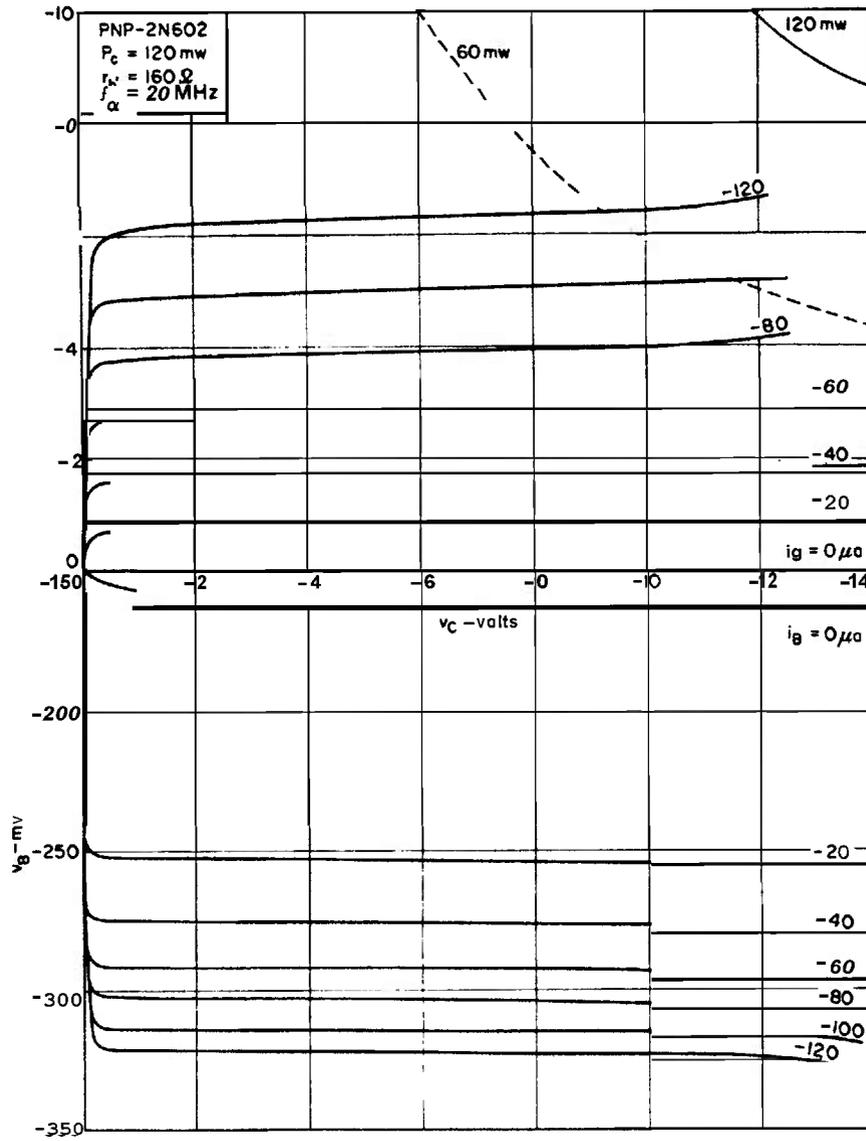


Fig. F-66. PNP-2N602

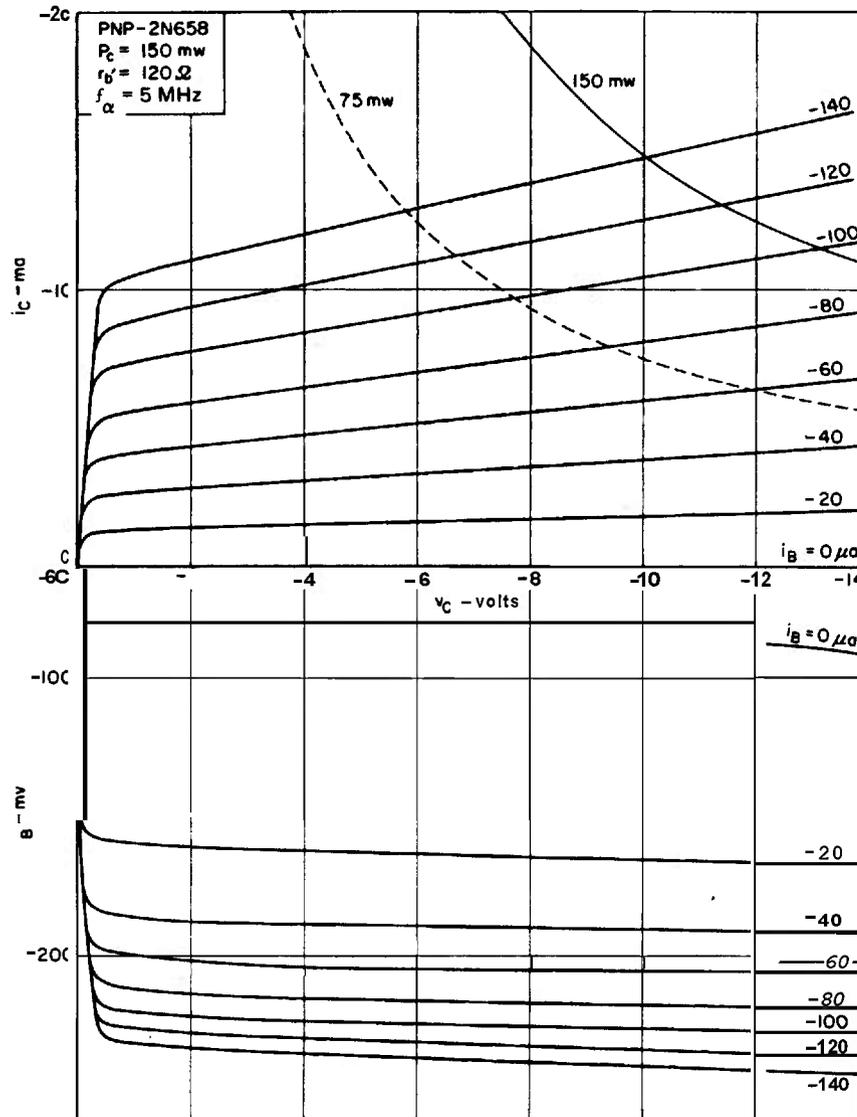


Fig. F-67. PNP-2N658

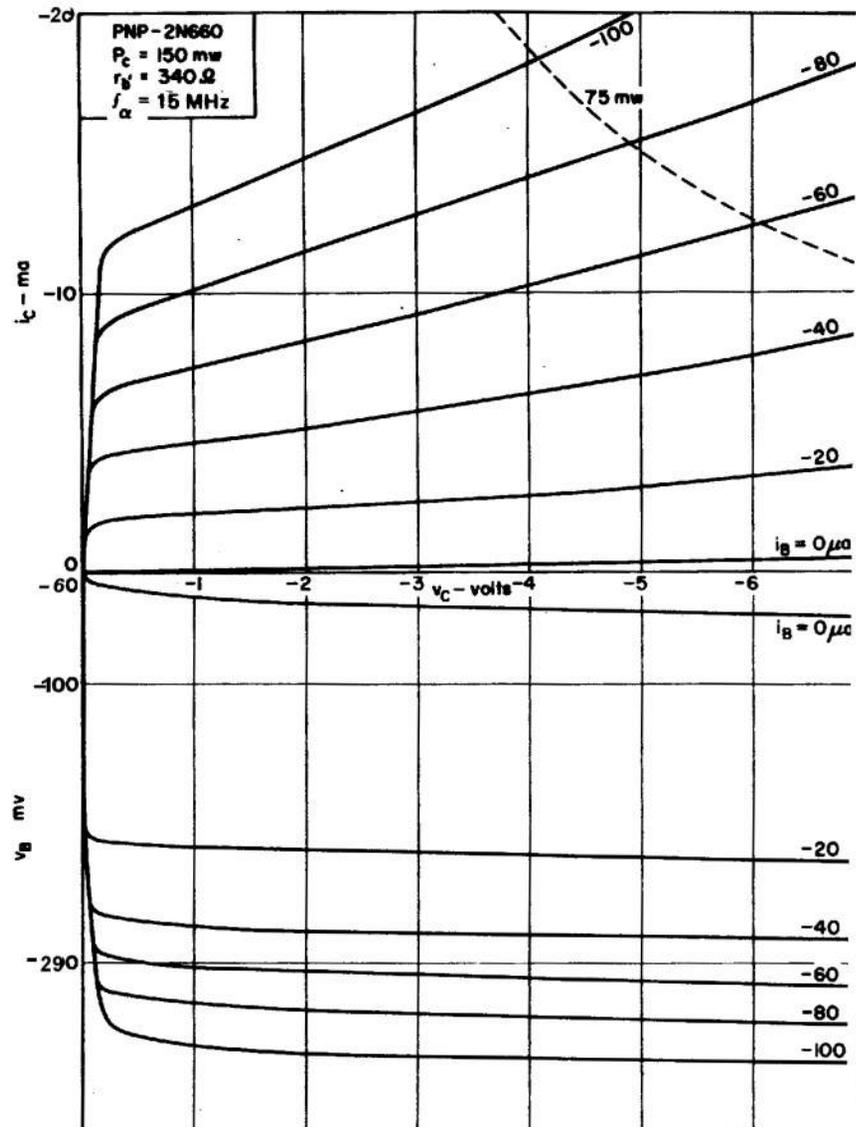


Fig. F-68. PNP-2N660

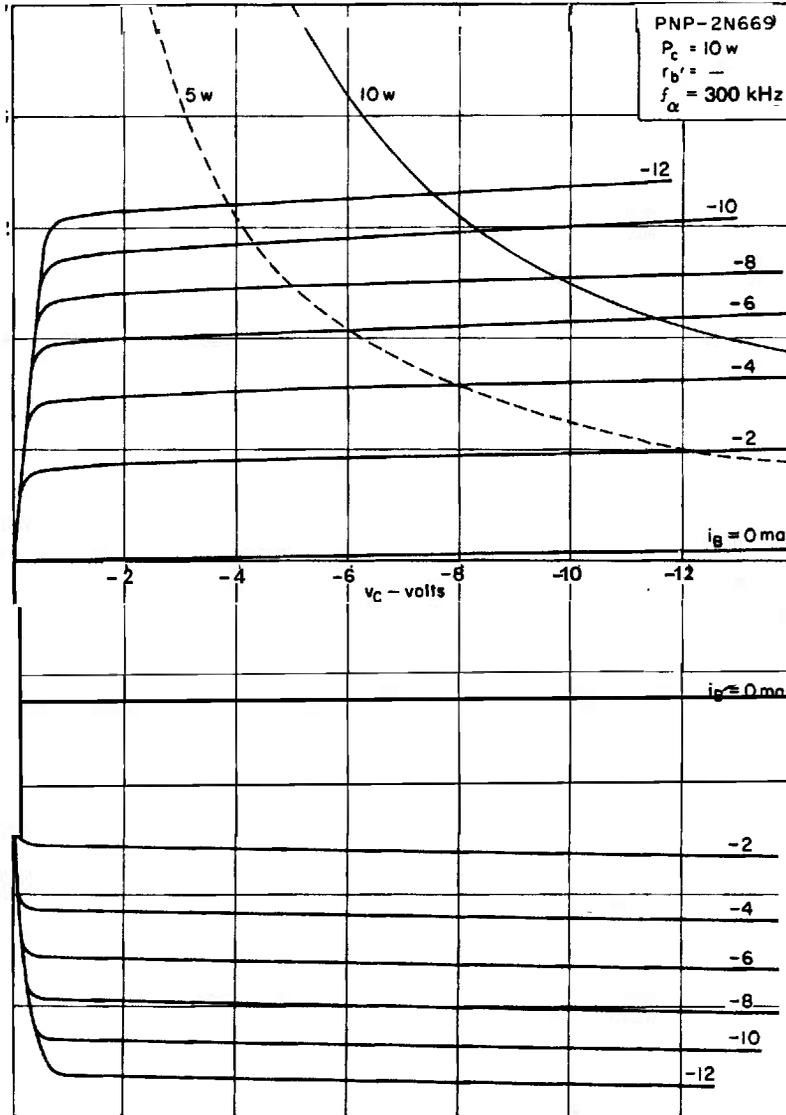


Fig. F-69. PNP-2N669

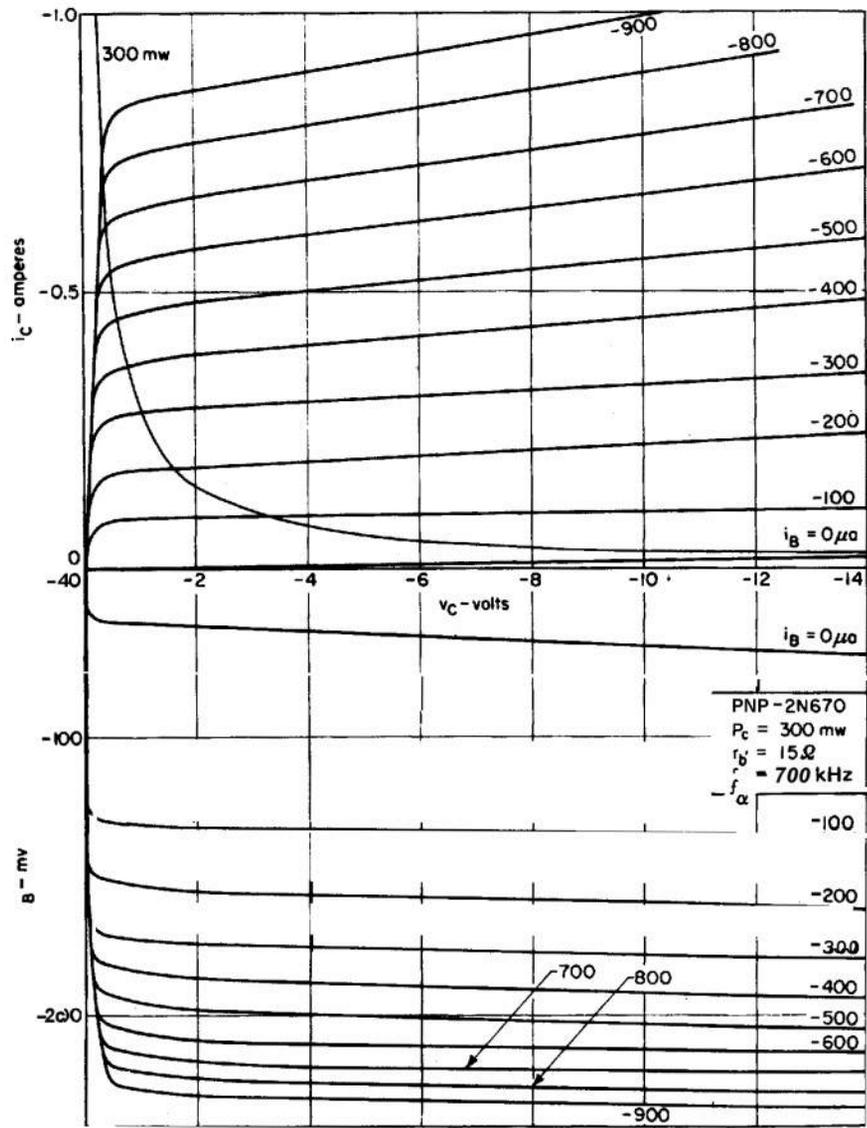


Fig. F-70. PNP-2N670

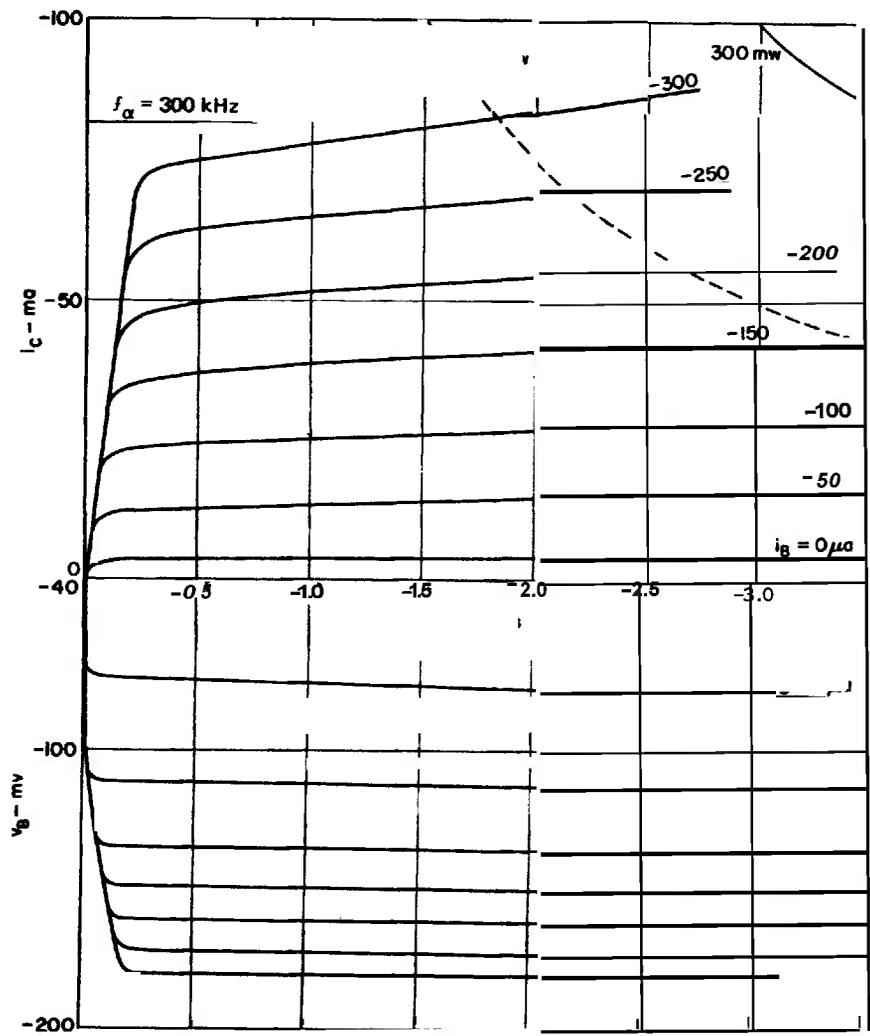


Fig. F-71. PNP-2N672

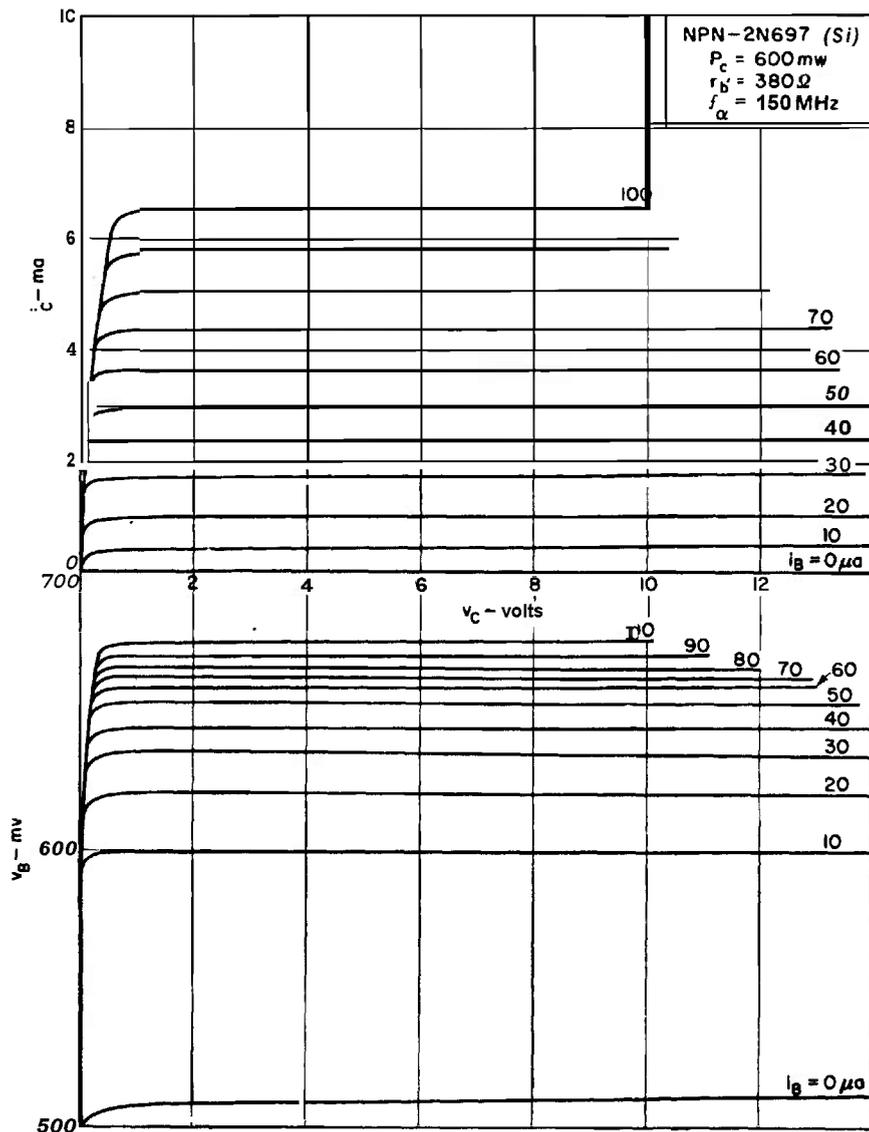


Fig. F-72. NPN-2N697 (Si)

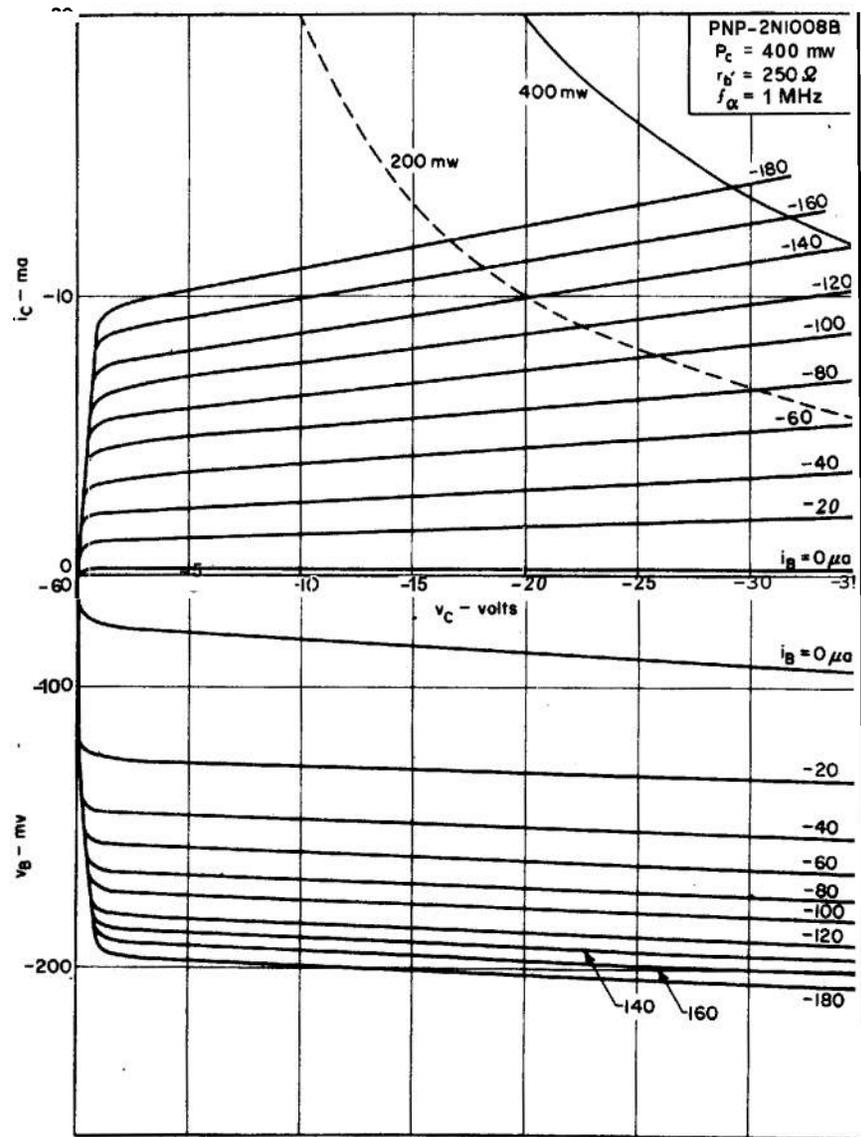


Fig. F-73. PNP-2N1008B

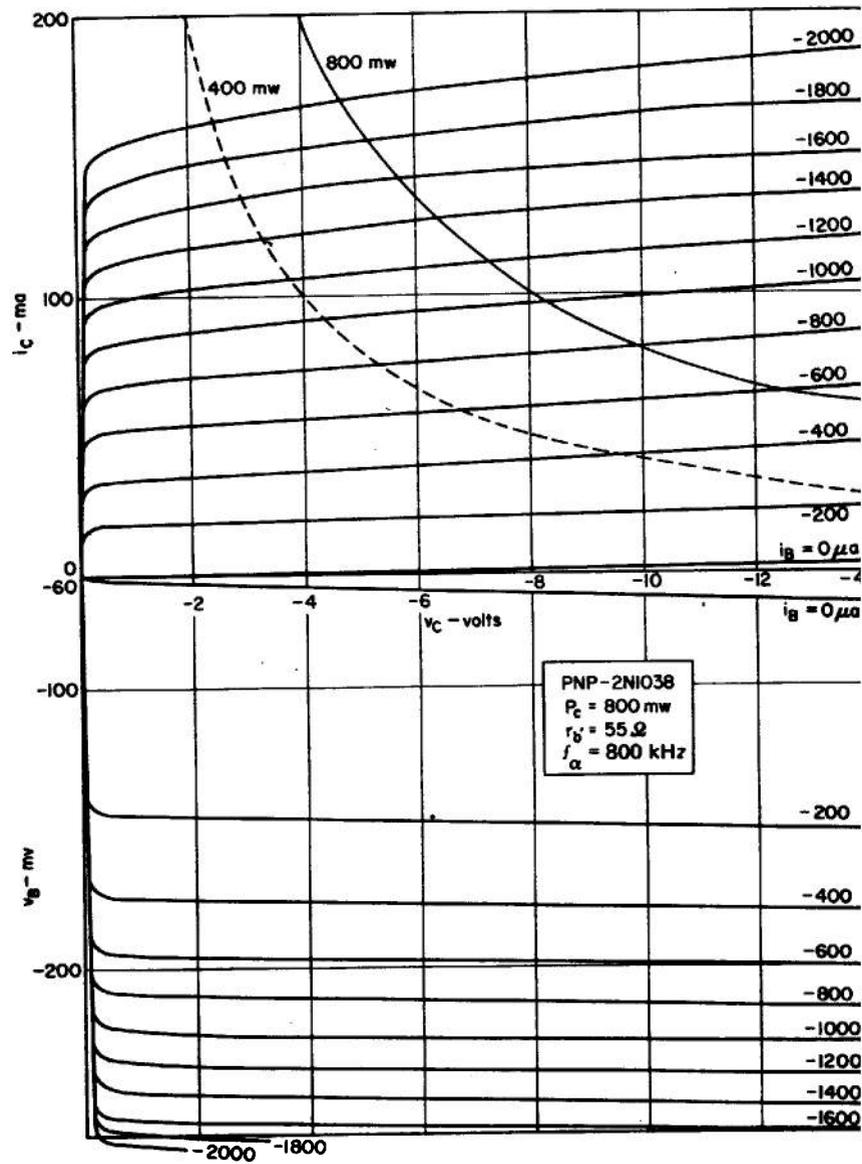


Fig. F-74. PNP-2N1038

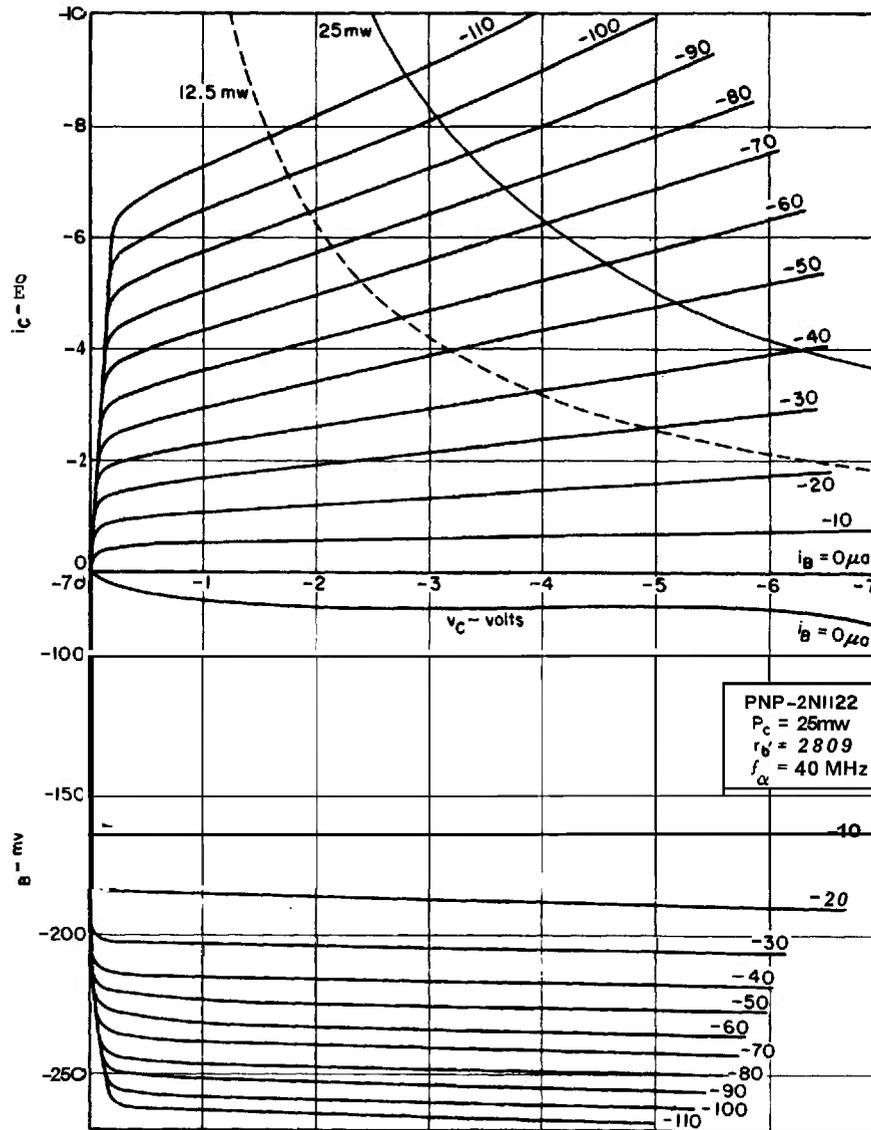


Fig. F-75. PNP-2N1122

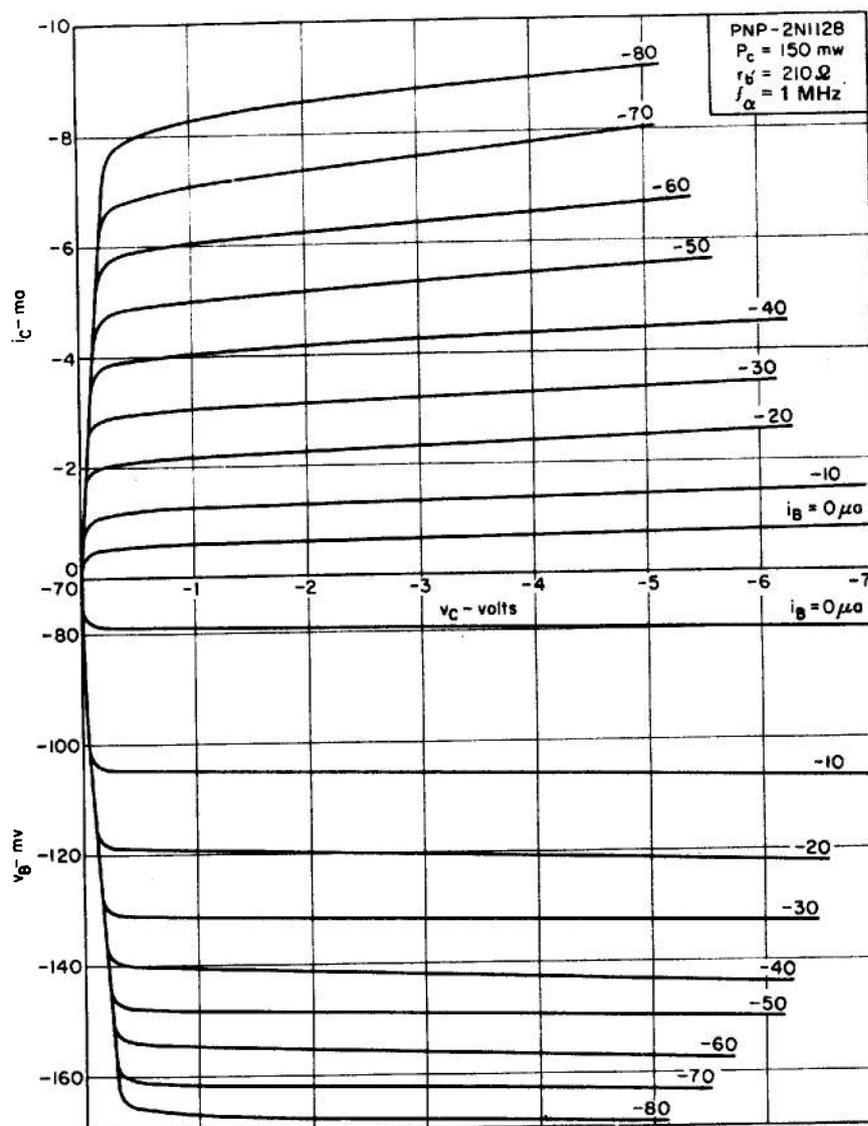


Fig. F-76. PNP-2N1128

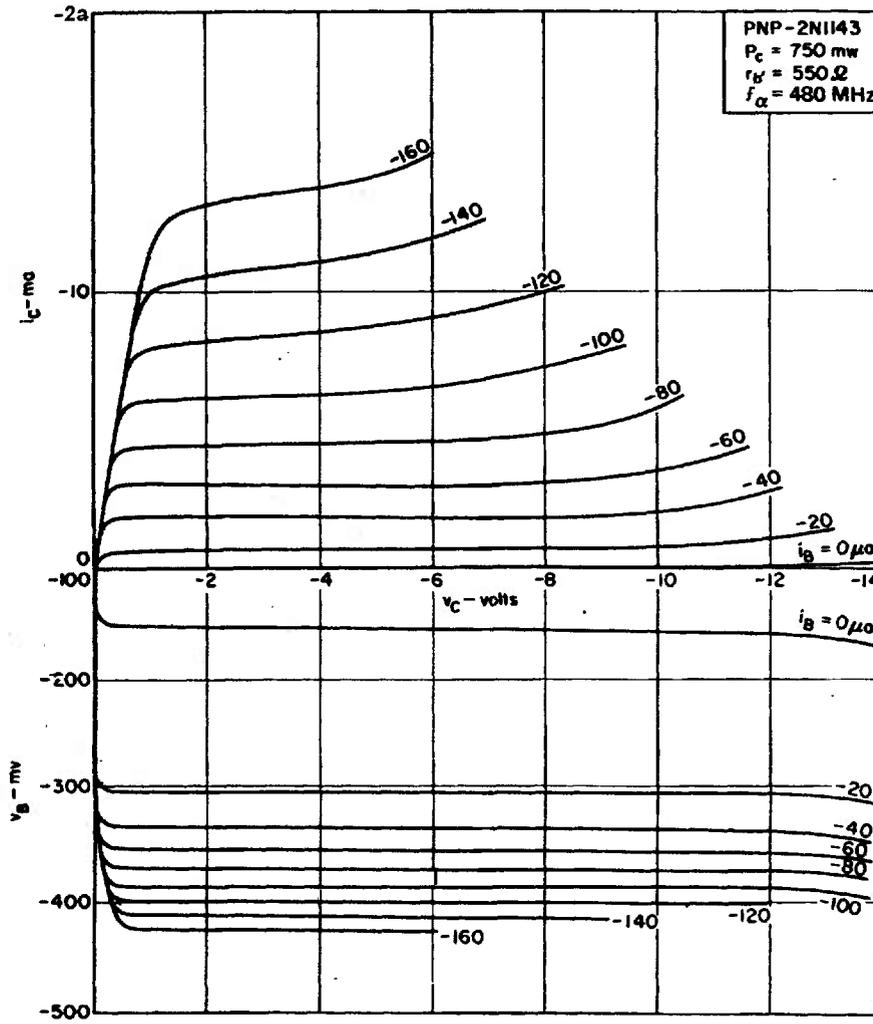


Fig. F-77. PNP-2N1143

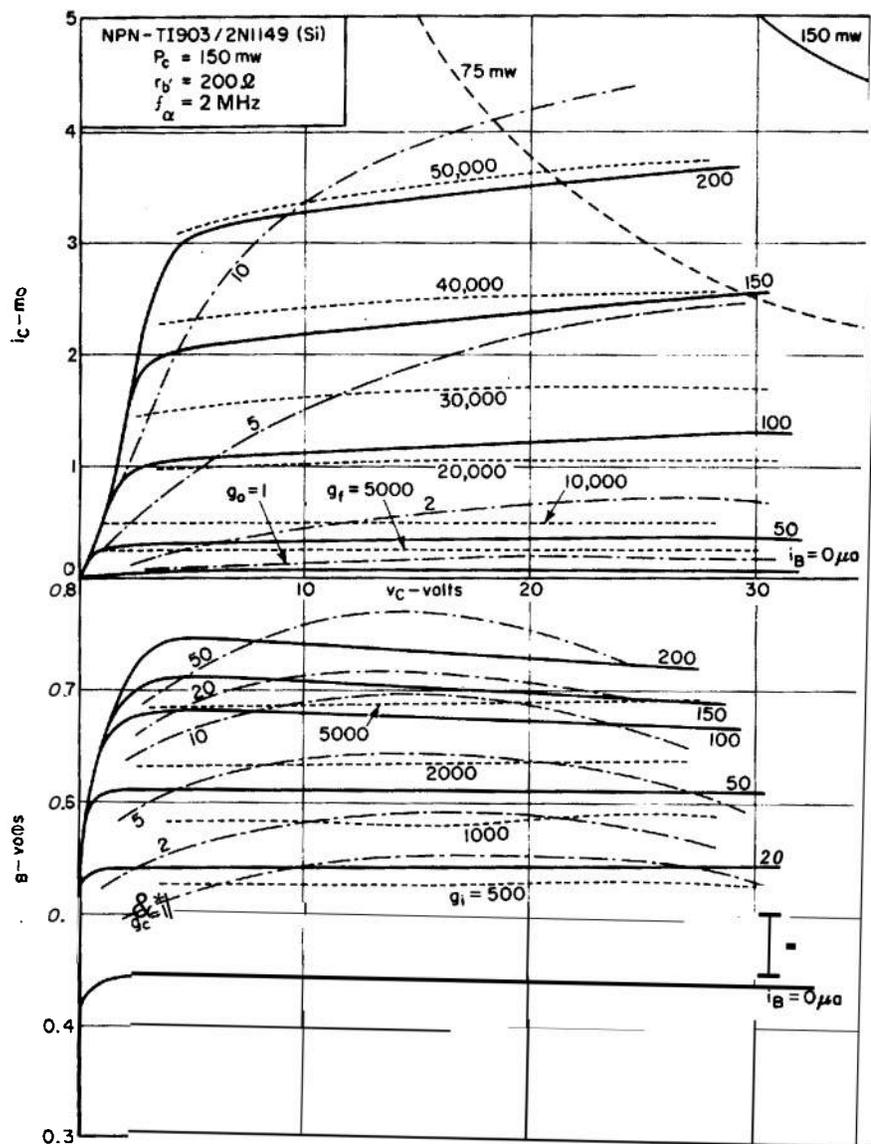


Fig. F-78. NPN-TI903/2N1149 (Si)

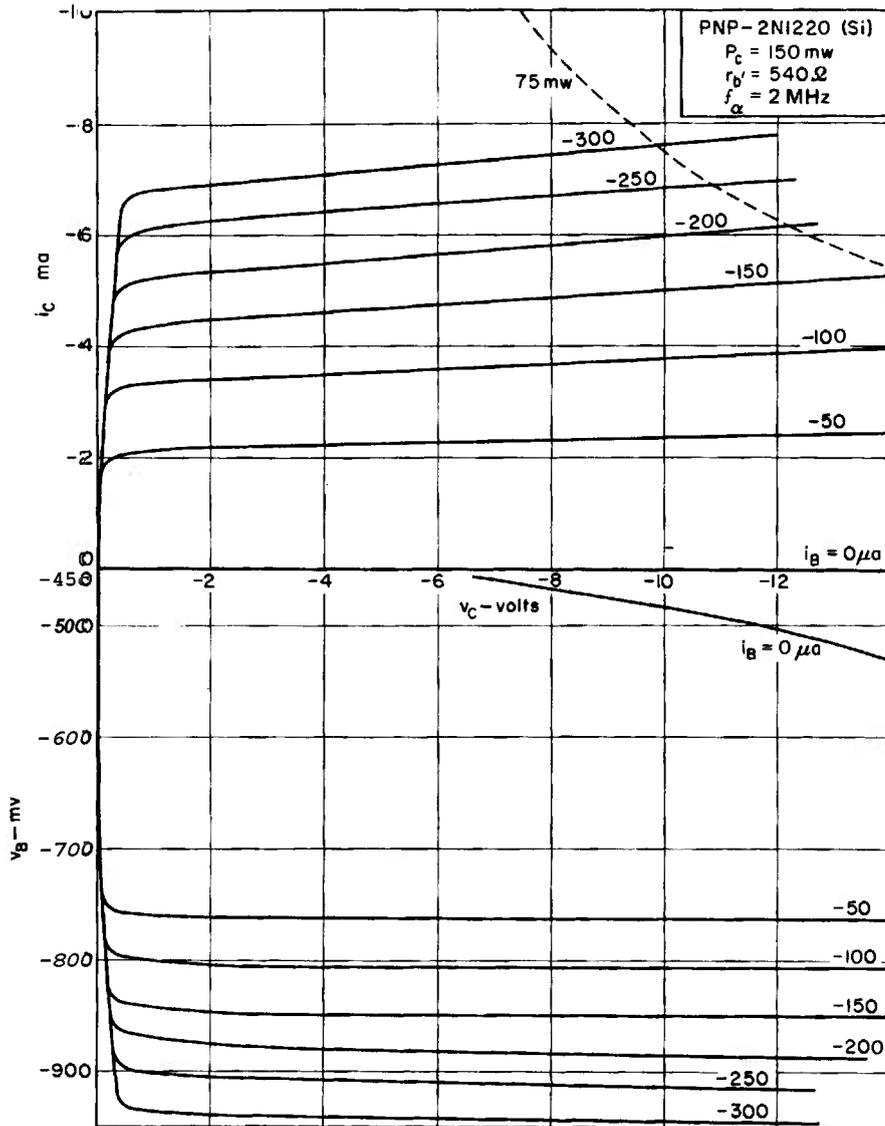


Fig. F-79. PNP-2N1220 (Si)

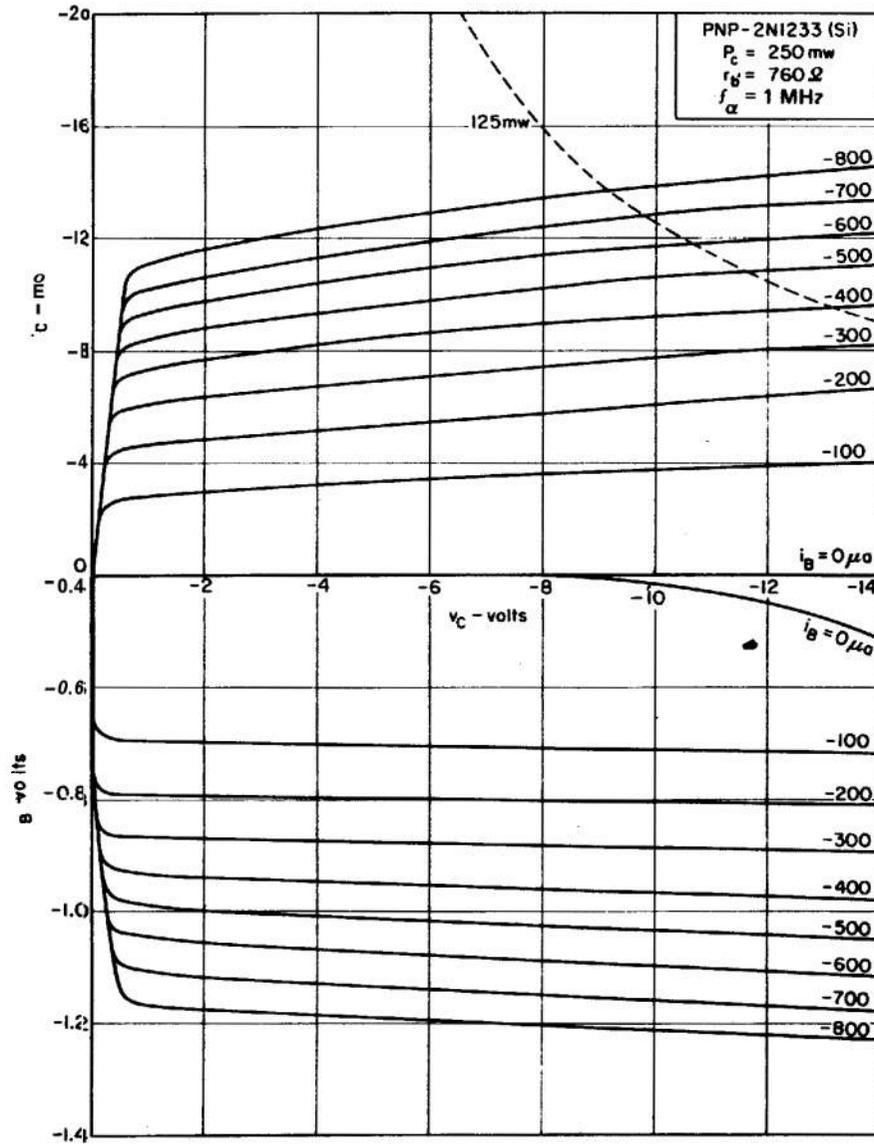


Fig. F-80. PNP-2N1233 (Si)

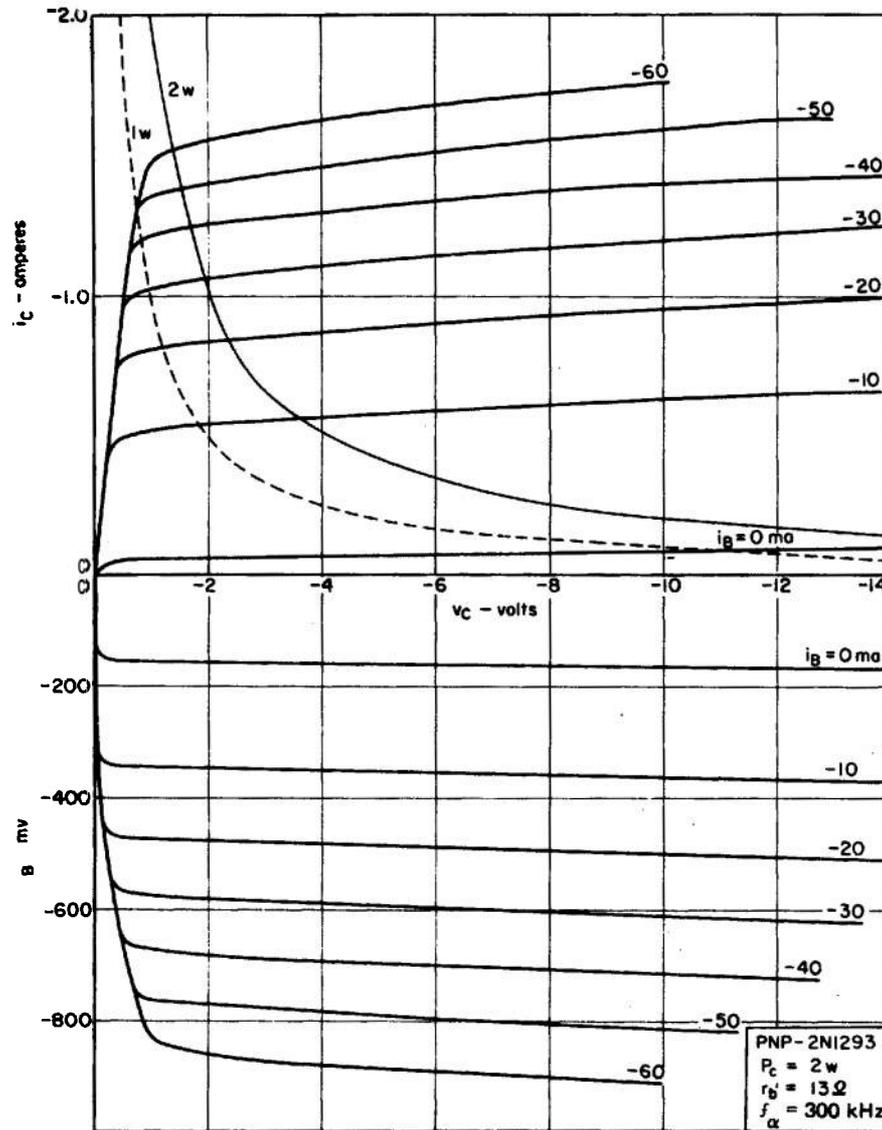


Fig. F-81. PNP-2N1293

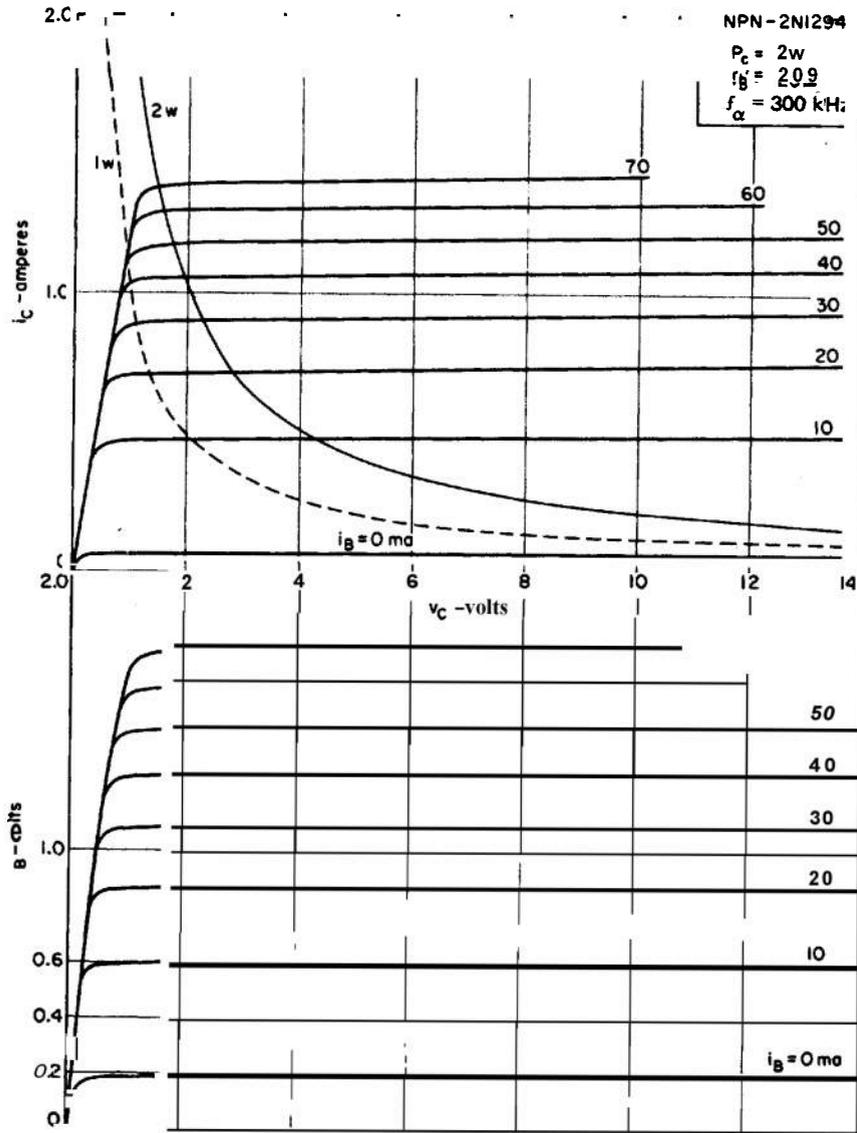


Fig. F-82. NPN-2N1294

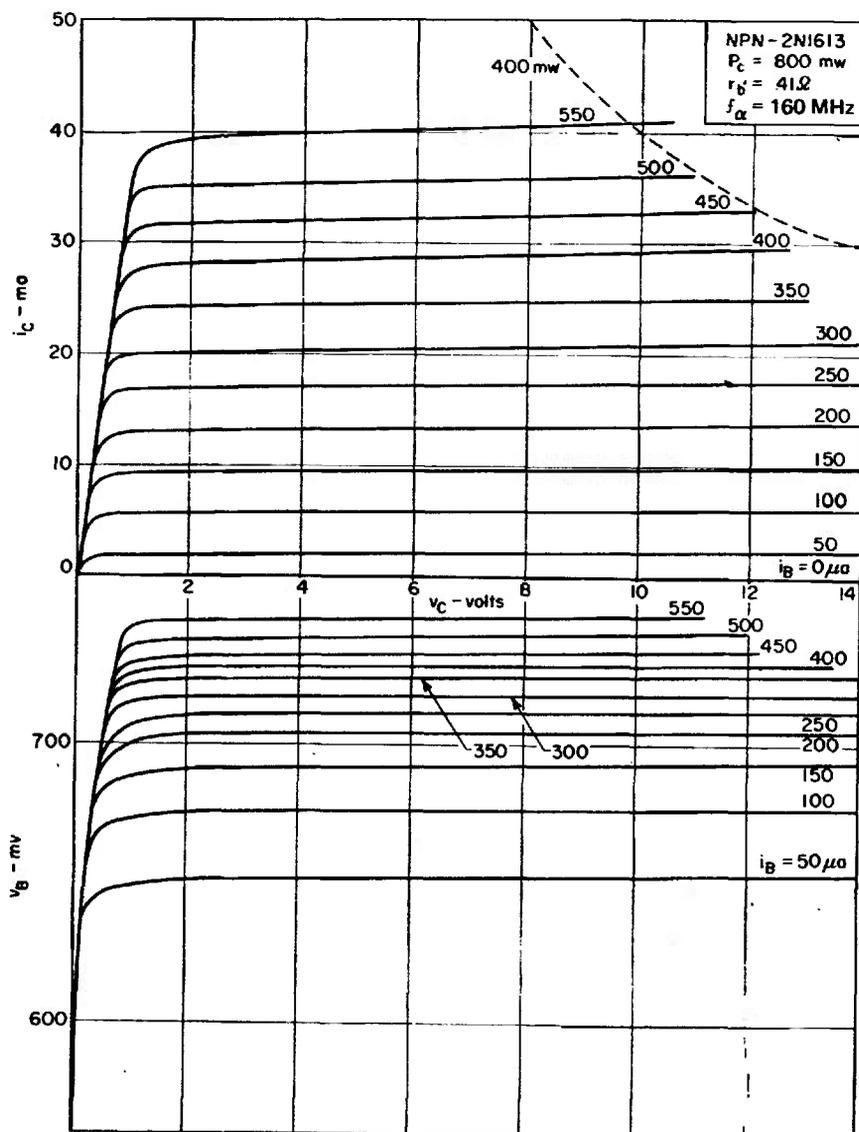


Fig. F-83. NPN-2N1613

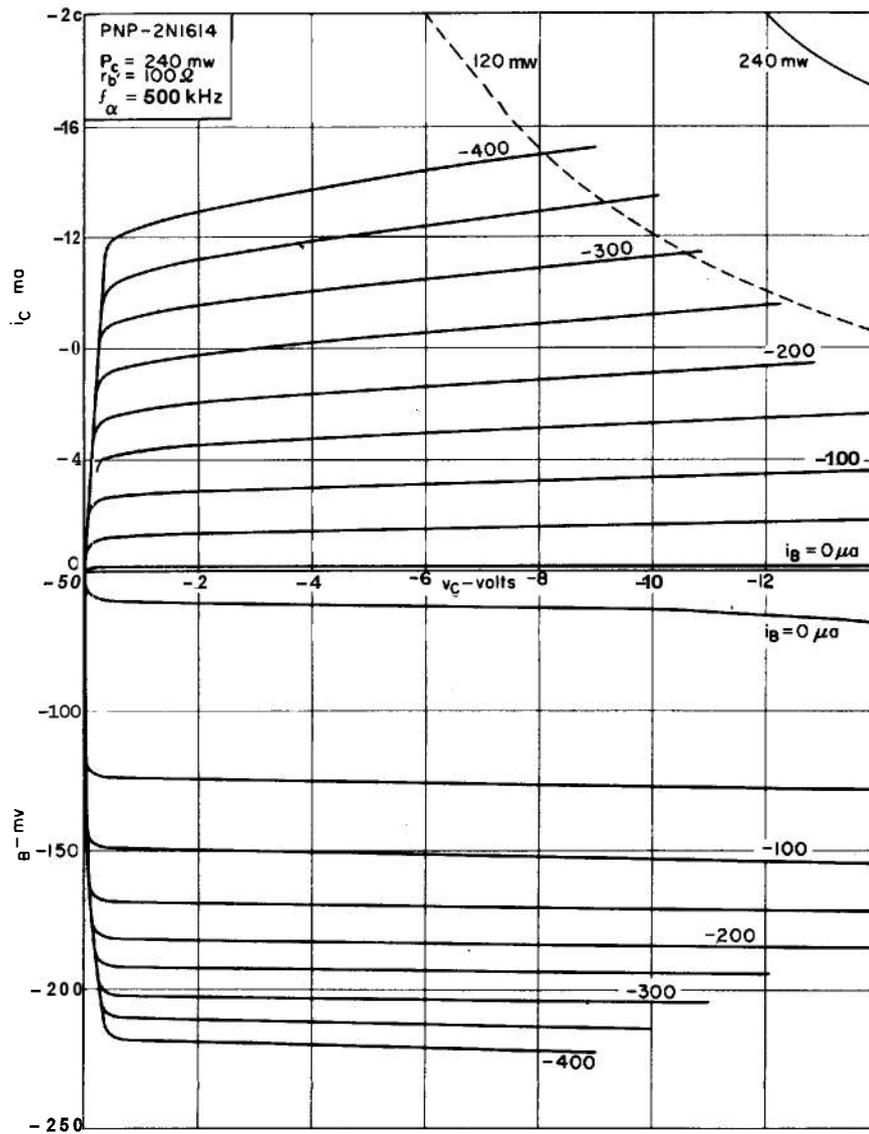


Fig. F-84. PNP-2N1614

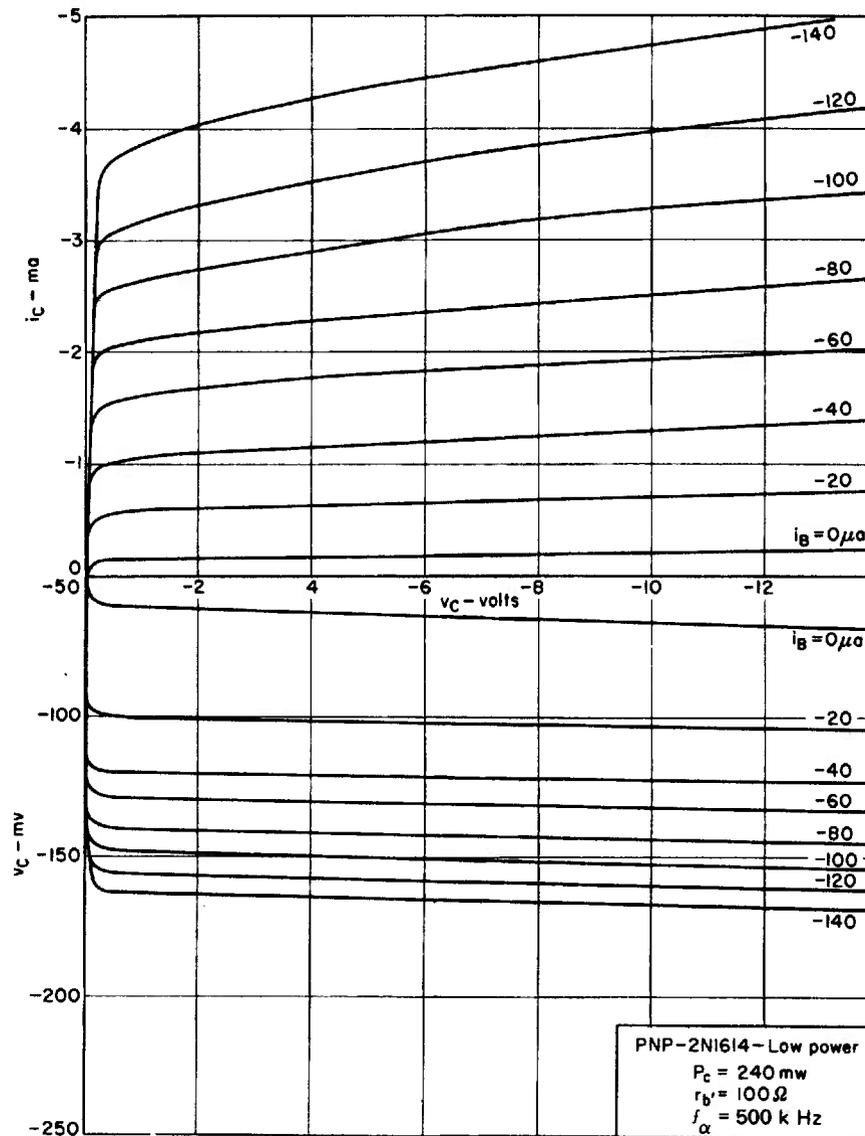


Fig. F-85. PNP-2N1614-Low Power

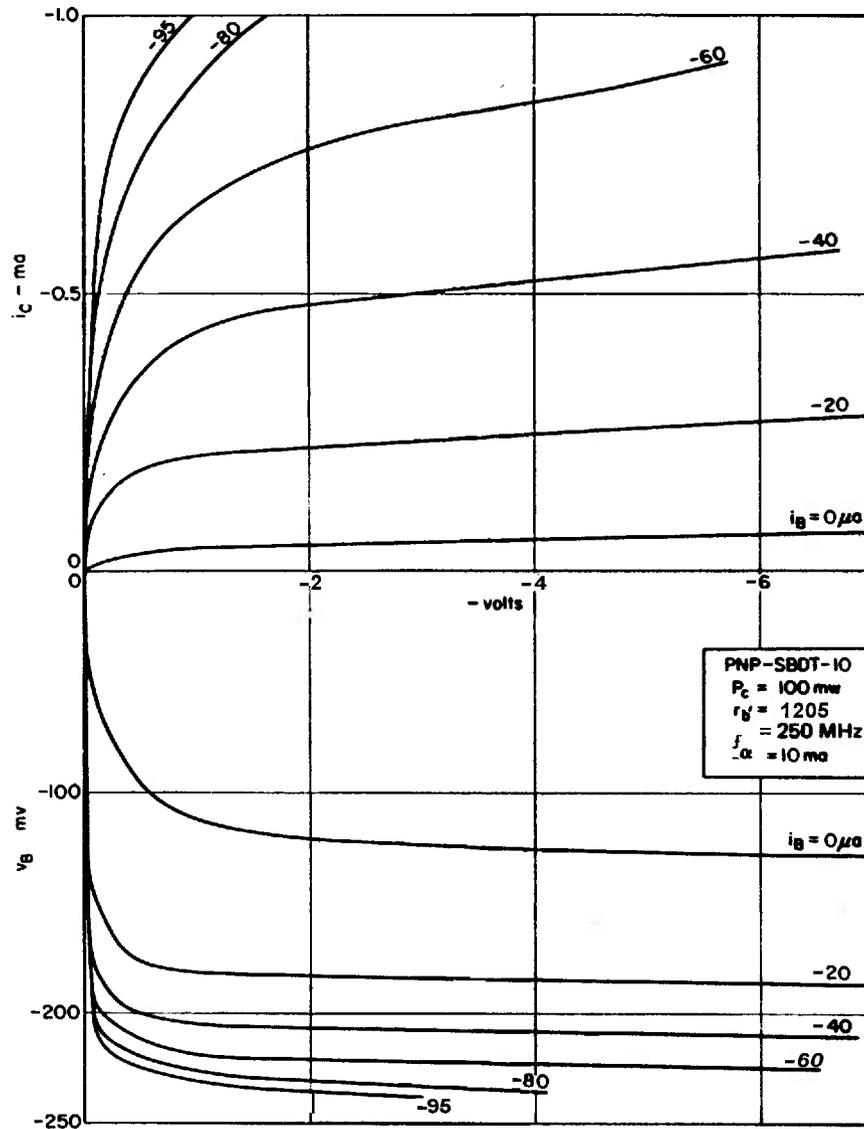


Fig. F-86. PNP-SBDT-10

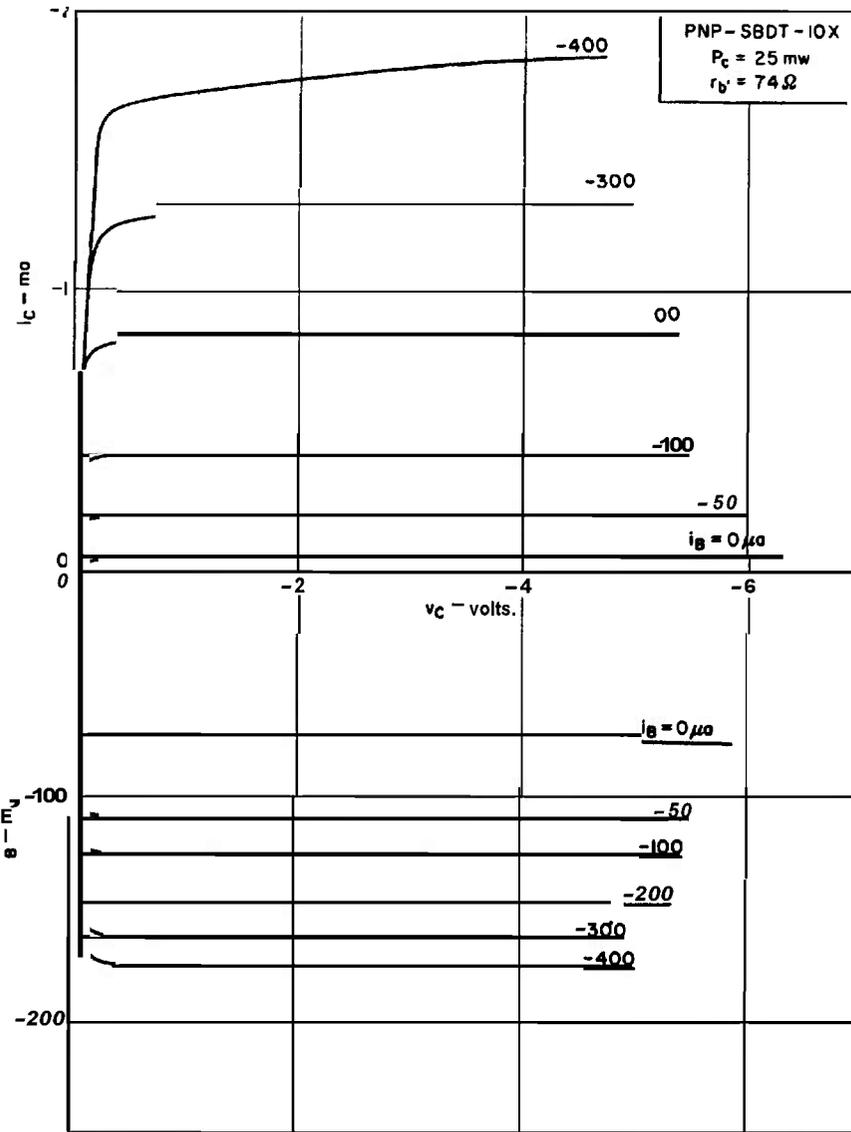


Fig. F-87. PNP-SBDT-10X

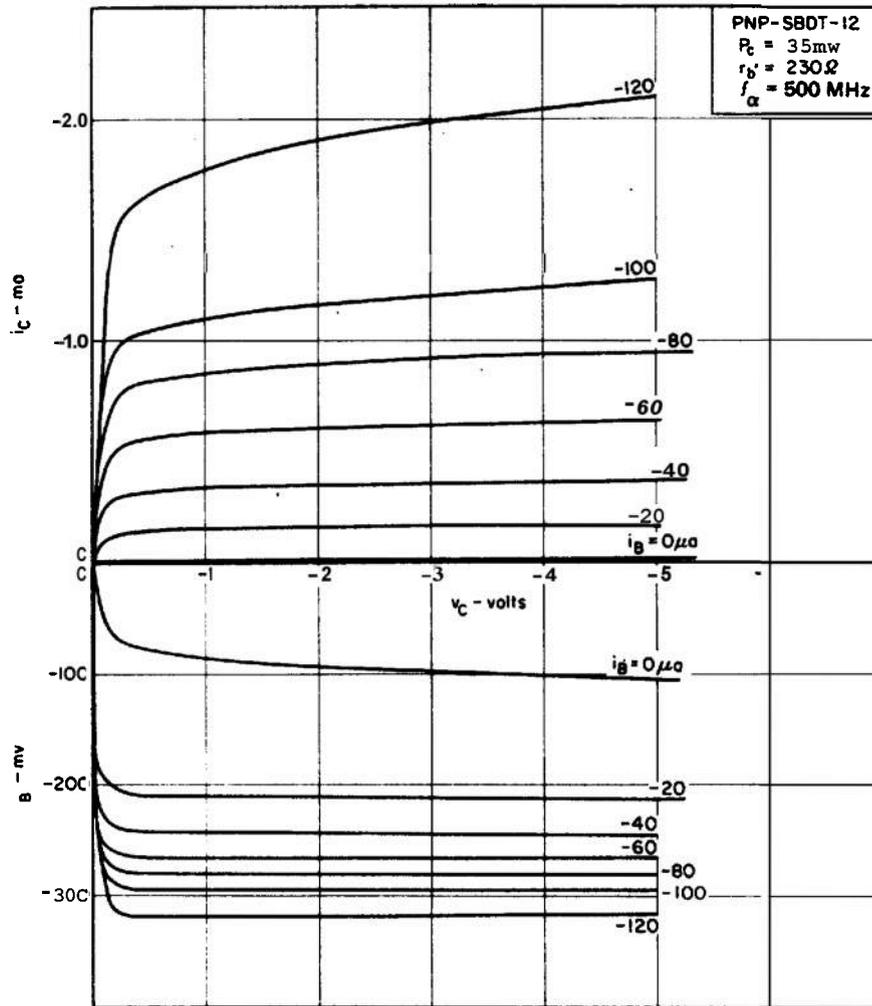


Fig. F-88. PNP-SBDT-12

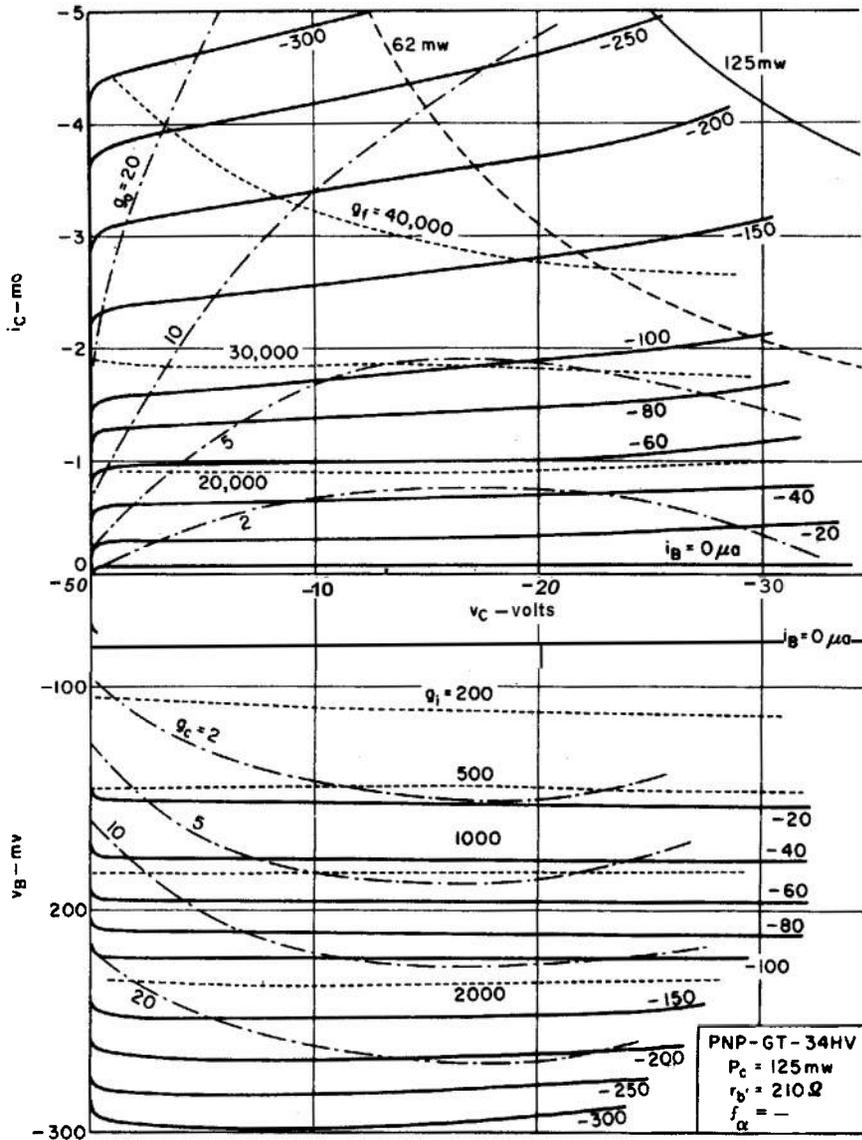


Fig. F-89. PNP-GT-34HV

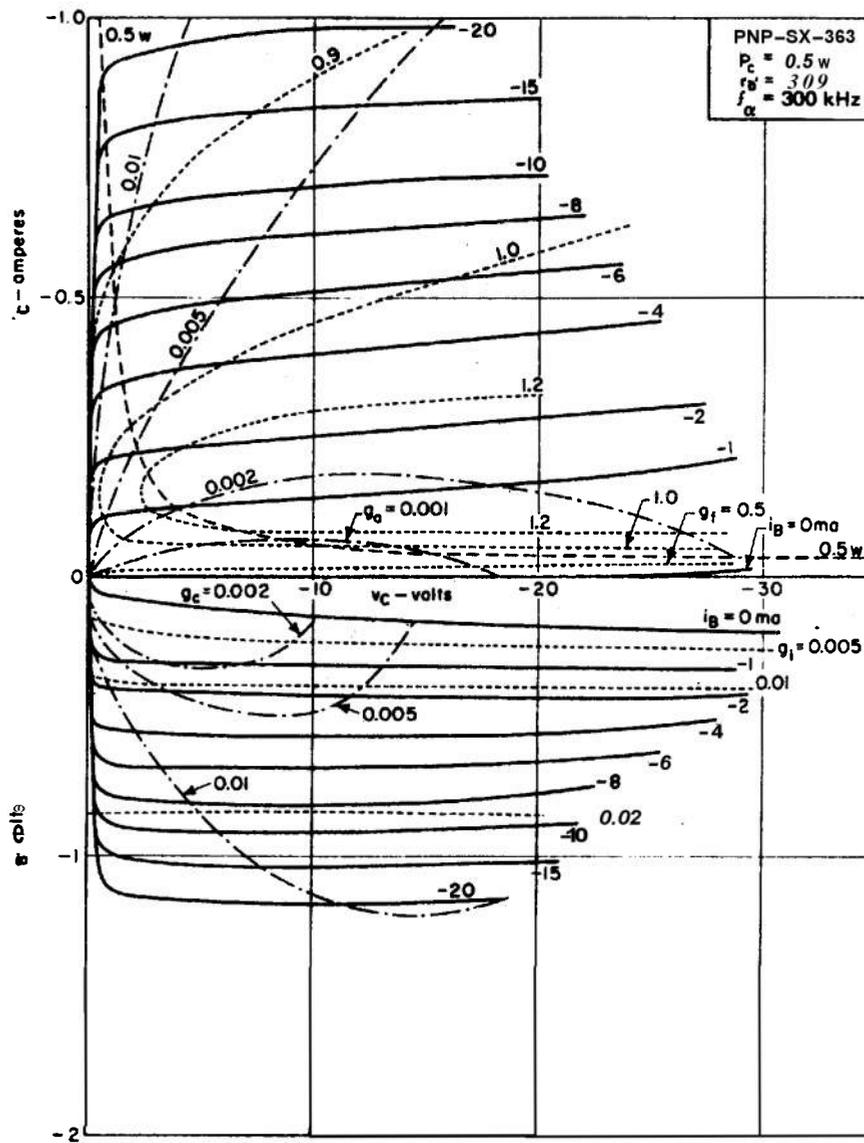


Fig. F-91. PNP-SX-363

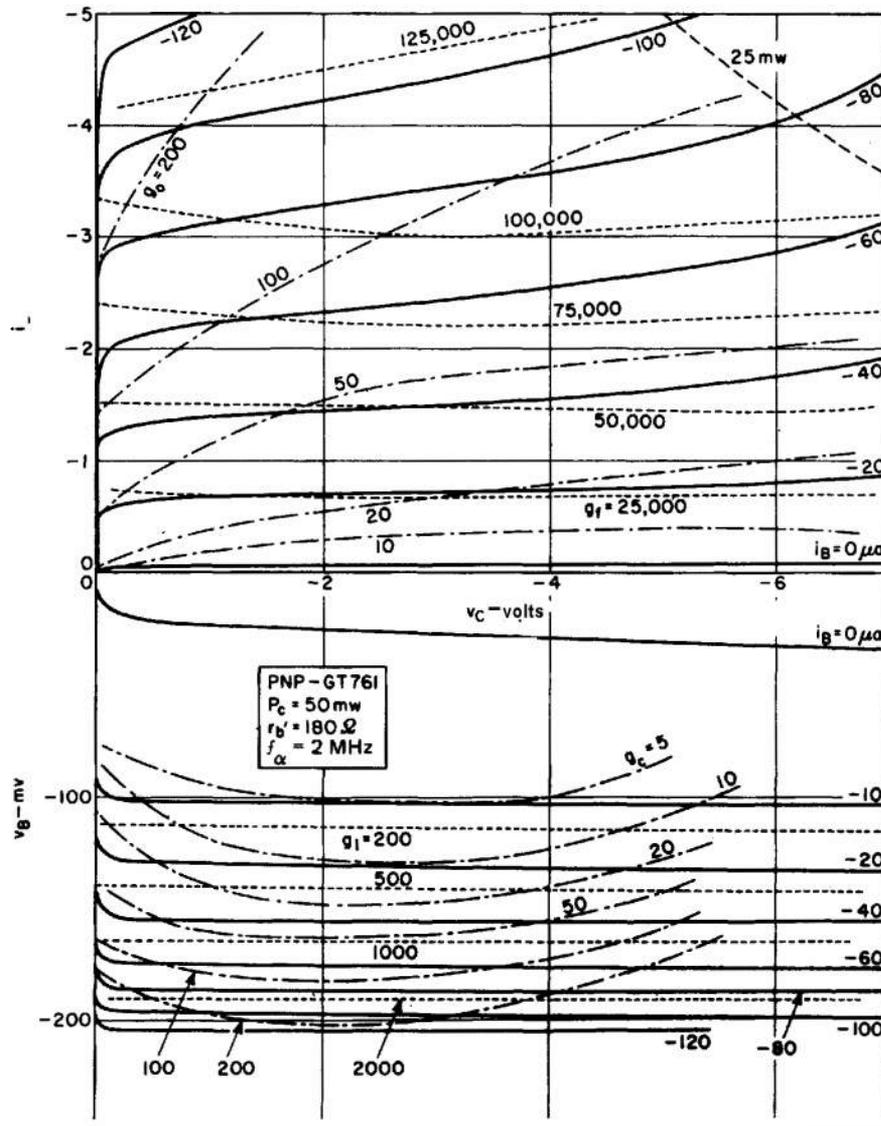


Fig. F-92. PNP-GT-761

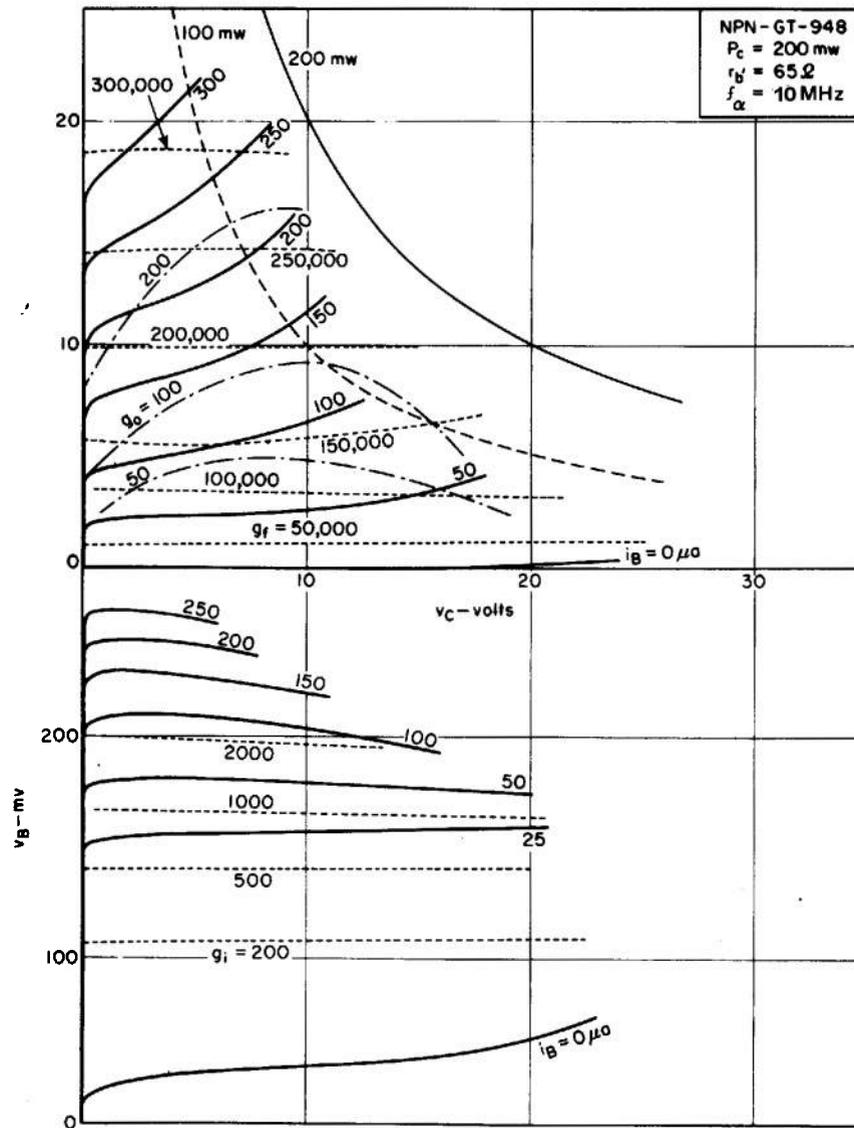


Fig. F-93. NPN-GT-948

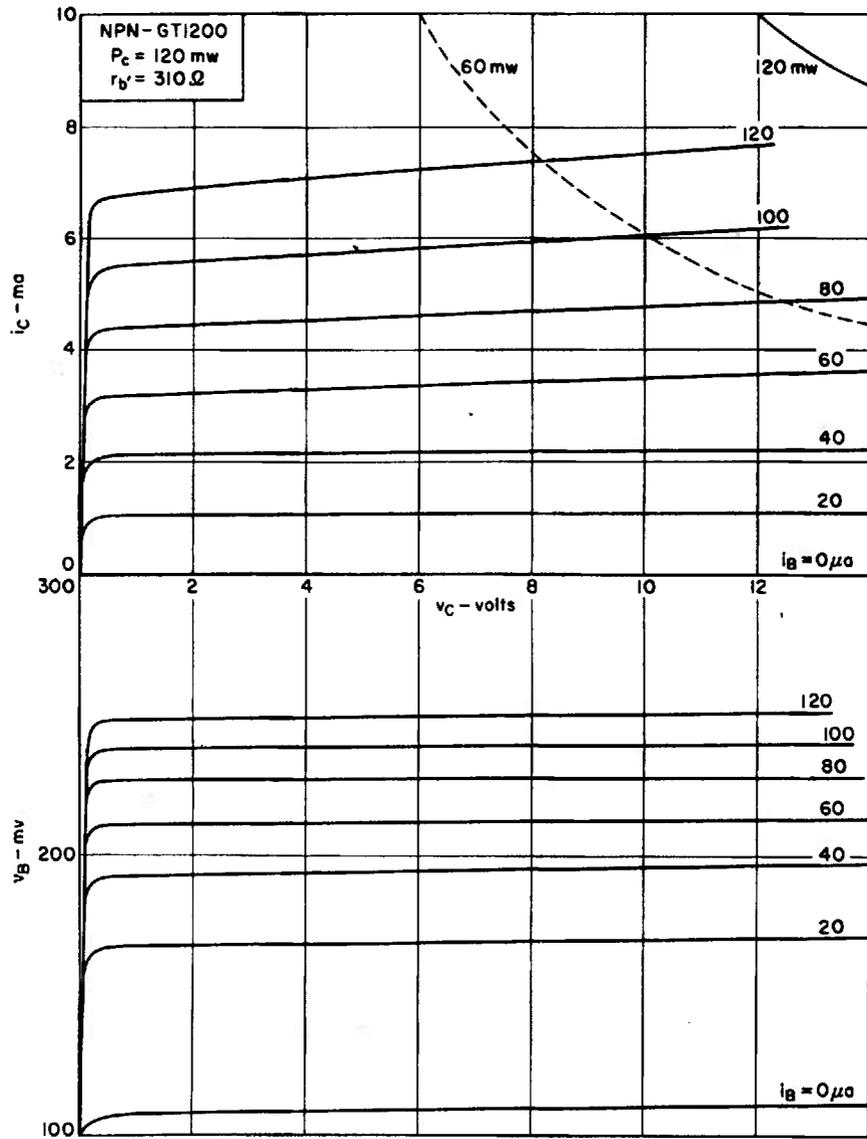


Fig. F-94. NPN-GT-1200

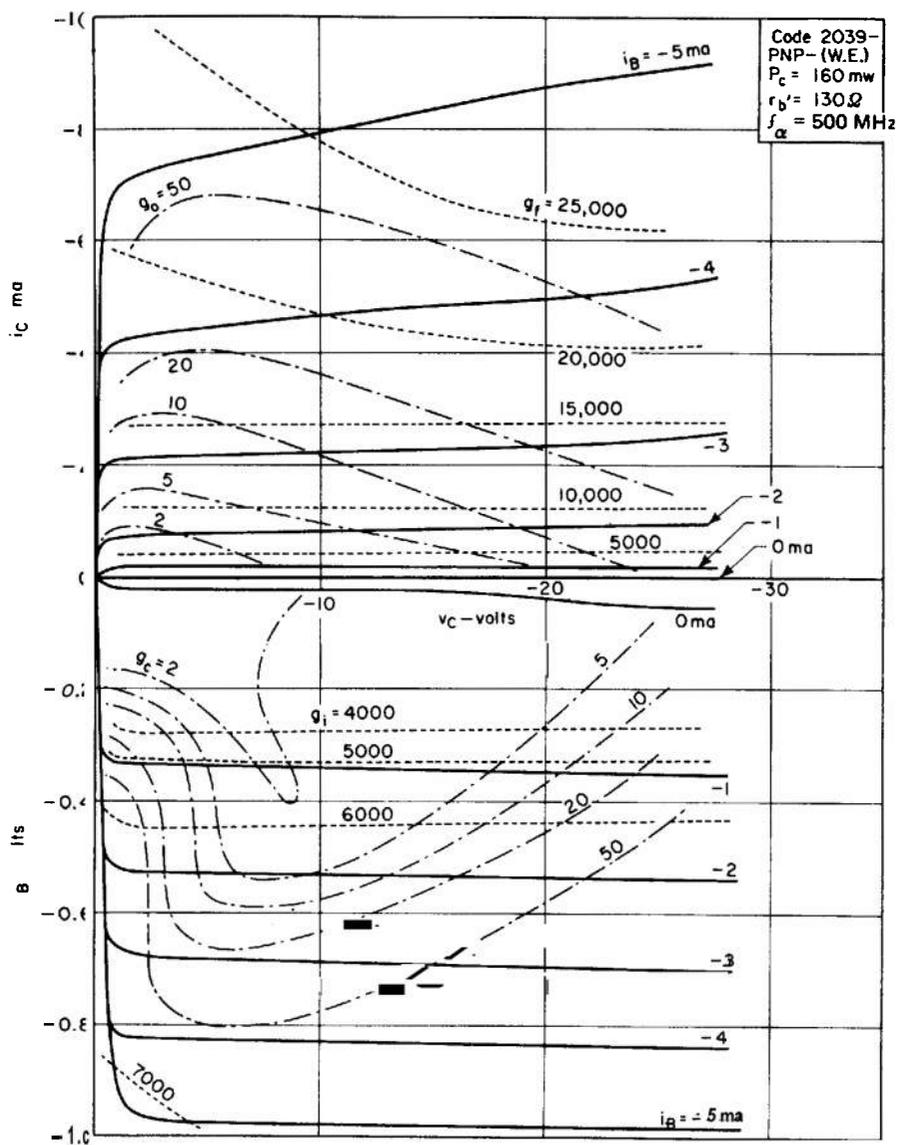


Fig. F-95. Code 2039-PNP-(W.E.)

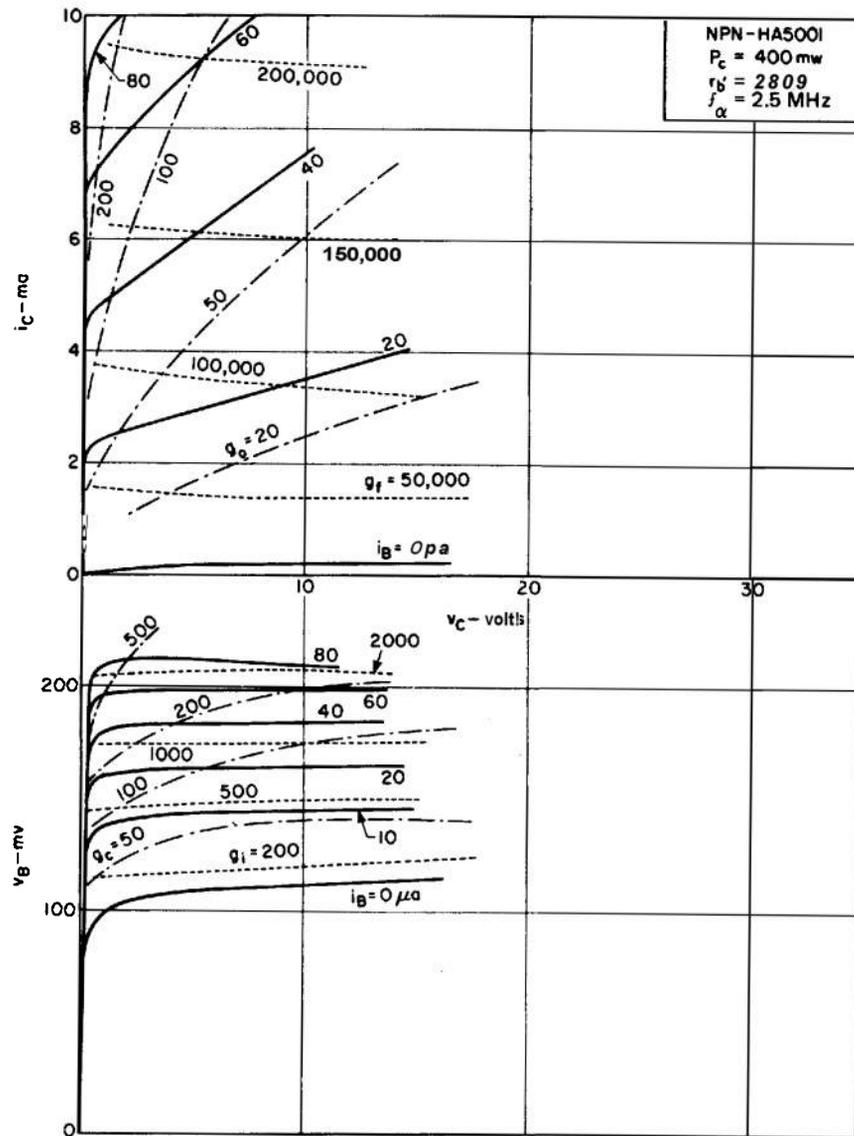


Fig. F-96. NPN-HA5001

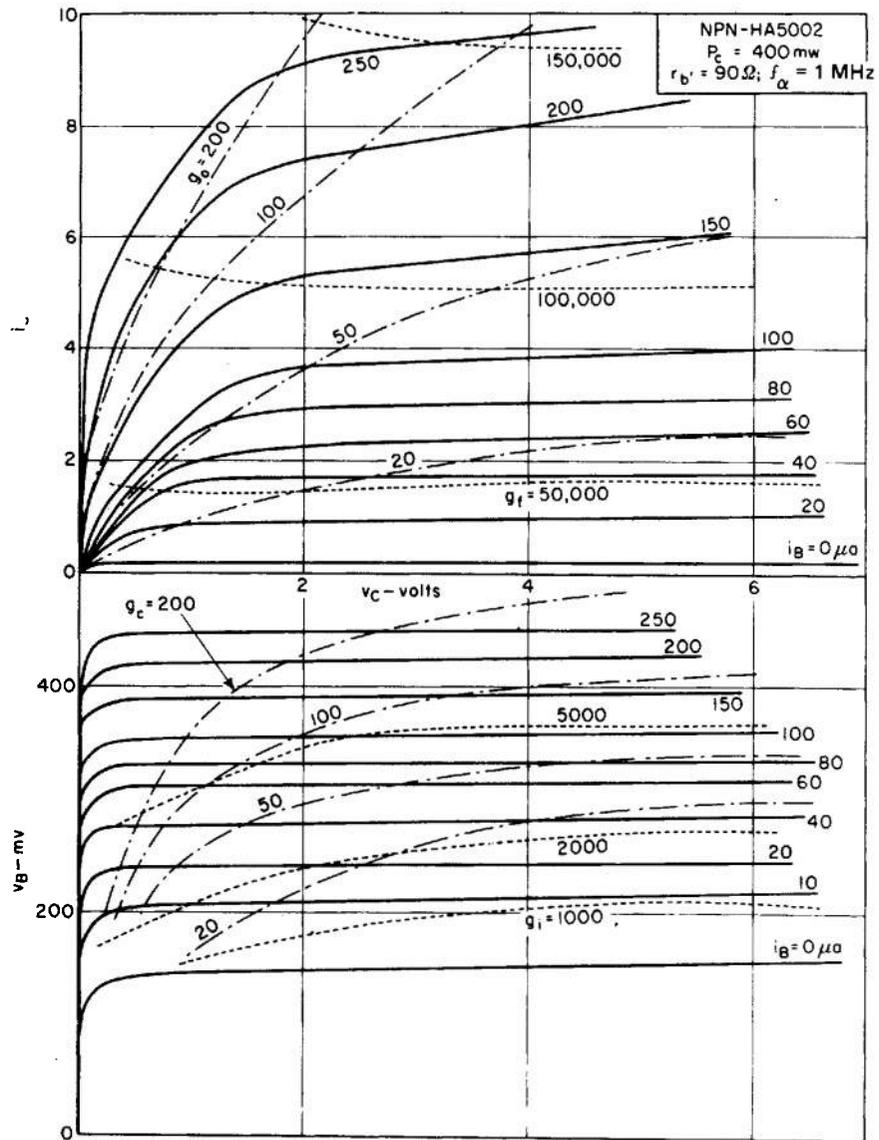


Fig. F-97. NPN-HA5002

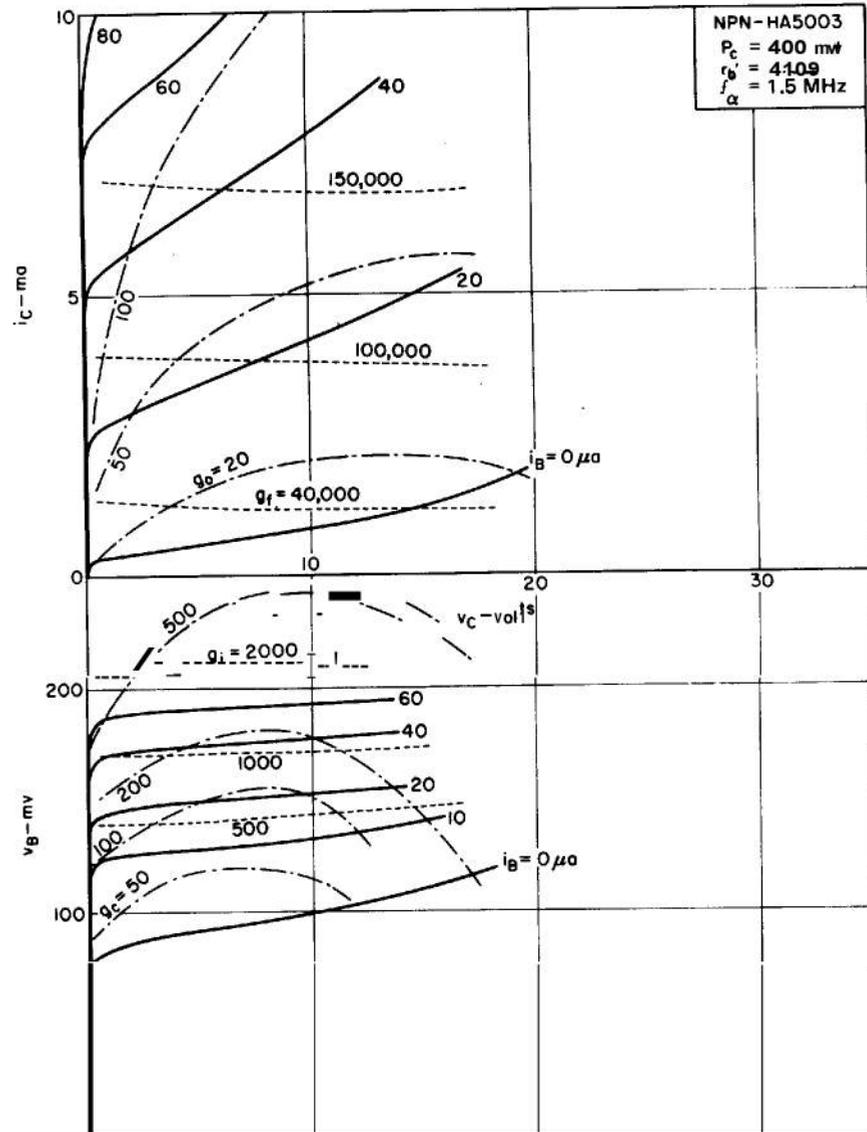


Fig. F-98. NPN-HA5003

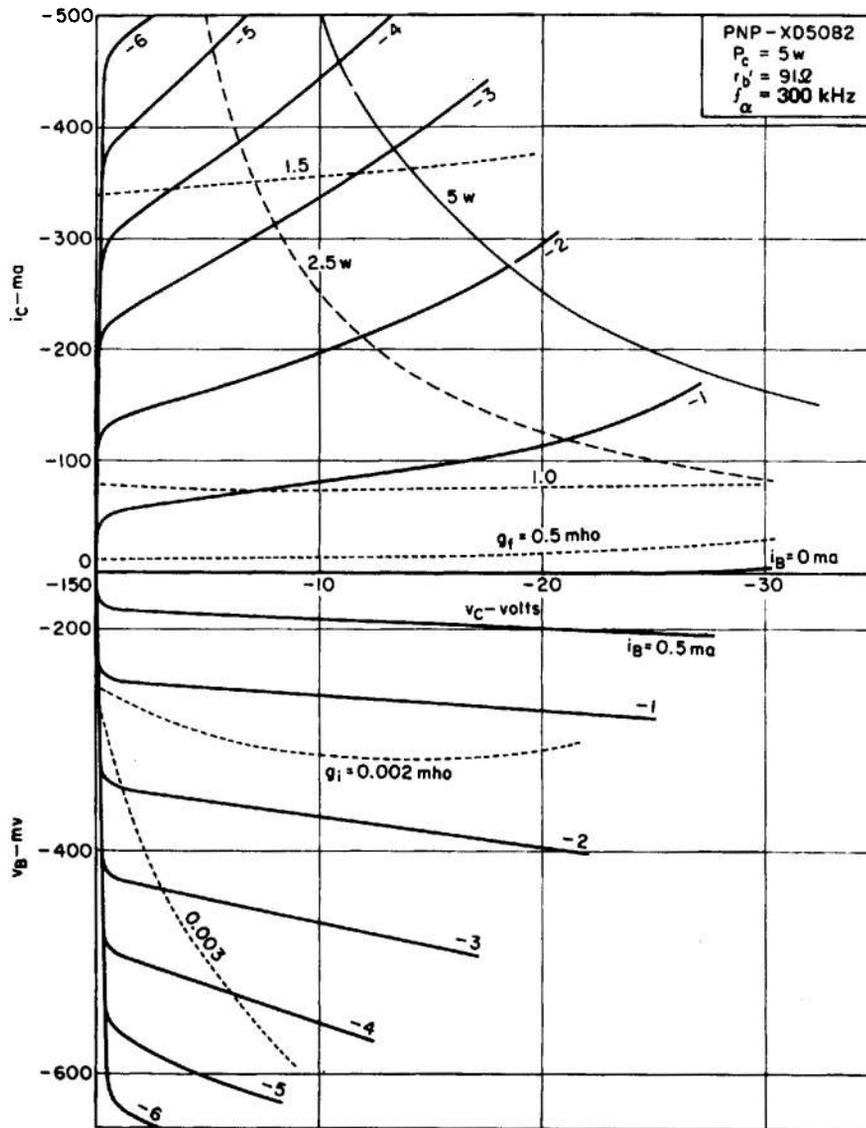


Fig. F-99. PNP-XD5082

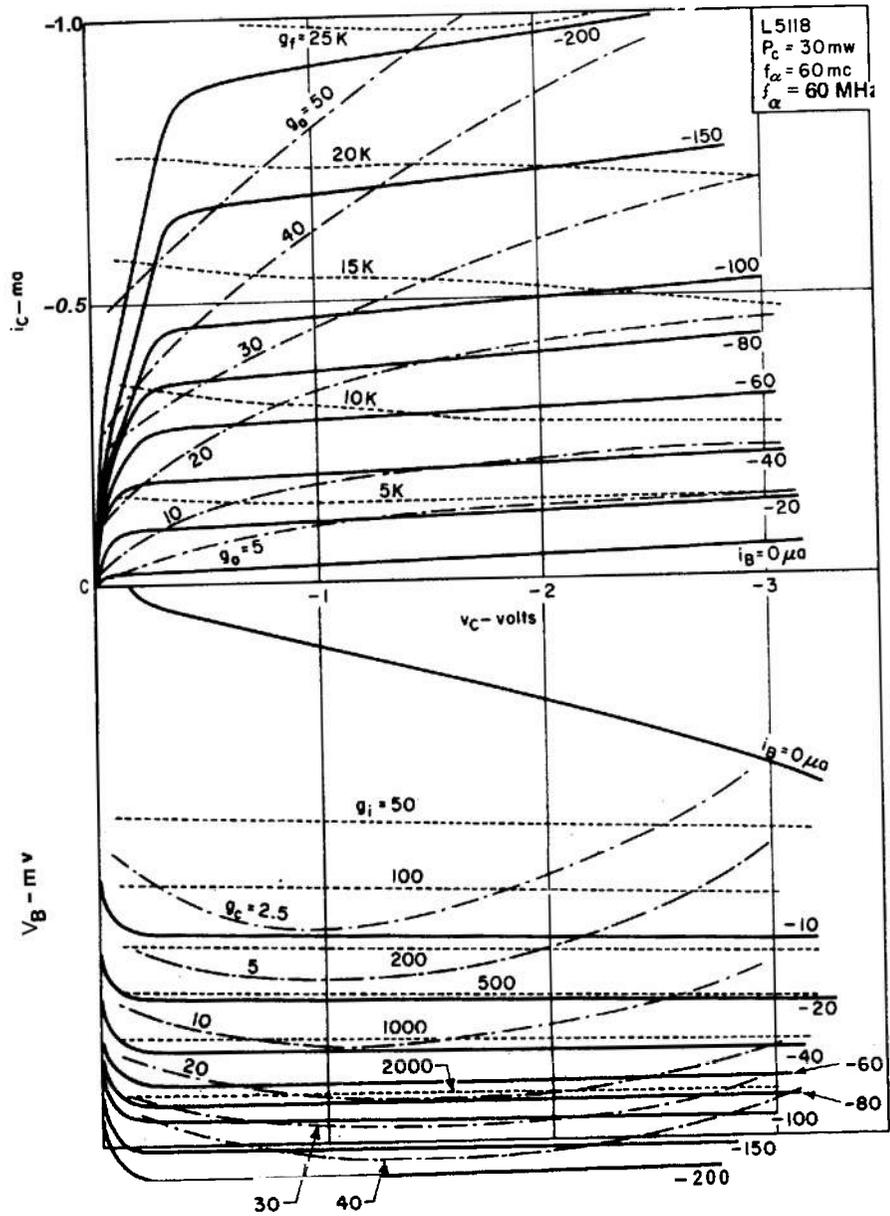


Fig. F-100. W118

APPENDIX G

A CALCULATION NOMOGRAPH FOR TRANSISTOR CIRCUITS

The nomograph, Fig. G-1, for calculation of admittances for transistor circuits is based on the use of a series of "Z" nomographs (Ref. 1). These nomographs have the property that the parallel scales have linear calibrations, yet they can be used to calculate products.

The calculation of the forward admittance of the common-emitter amplifier includes six steps:

- (1) Calculation of the product of g_c and R_L
- (2) Calculation of the product of $(1 + g_c R_L)$ and g_i
- (3) Calculation of the product of R_s and $g_i (1 + g_c R_L)$
- (4) Calculation of the product of g_o and R_L
- (5) Addition of $(1 + g_c R_L)$ and $g_i R_s (1 + g_c R_L)$ to give D
- (6) Division of g_f by D to give Y_f

To obtain product one, locate the value of R_L on line (1) and the value of g_c on line (2). When R_L is given in ohms, then the value of g_c must be given in mhos. Similarly, with R_L in kilohms or megohms, the value of g_c should be expressed in millimhos or micromhos, respectively. The positions of the g_i and R_s scales in respect to lines (1) and (2) add the unity to the value of the product scaled along line (3).

Now, if the value obtained on line (3) is connected by a straight line with the value of g_i on line (4), the product is indicated by the intersection with the transfer line. A second product can be obtained by passing a line from the applicable value of R_s on line (5) through the intersection point on the transfer line on to line (6).

Next, the value of $g_o R_L$ must be found and summed into the total, and unity added to give the value of the denominator, D , on line (10). The value of R_L in ohms, kilohms, or megohms, is located on line (7), and a line drawn through the value of g_o in mhos, millimhos, or micromhos, respectively, on line (8). The product appears on line (9), and plotting a straight line through the appropriate points on lines (6) and (9) and extending to line (10) gives the required value of D . Introduc-

tion of the value of g_f in mhos, millimhos, or micromhos on line (11) and plotting the line from this point to the appropriate point on line (10) gives an intersection on line (12) corresponding to the transfer admittance in the same respective units.

The values of 10^k , 10^{-k} , 10^m or 10^{-m} , and 10^n or 10^{-n} can be used to change the scales consistently to handle values which might be inconvenient in terms of ohms, kilohms, or megohms. If $R_L = 5000$ ohms on line (1), for example, taking the value of $n = 2$ places the datum point at midscale instead of at one end. The range of g_c calibrated on line (2) then is from 50 micromhos to 10 millimhos. Similar conversions may be used on all of the scales.

Although the nomograph has apparently been developed for the circuit in which r_b is neglected, it can be converted to make it useful with intrinsic data including r_b by making the substitutions:

g_i is replaced by g_i'

g_f is replaced by g_f'

R_s is replaced by $(r_b + R_s)$

Then the calculation procedure is as before.

This nomograph may be used for the calculation of the admittances for common-base and common-collector circuits by taking account of the following changes:

Common base

g_f is replaced by the sum $(g_f + g_o)$

The product $(g_f + g_c + g_o)R_s = g_f R_s$ is determined on lines (7), (8), and (9) and added to the value of $g_o R_L$ on line (9)

Common collector

g_f is replaced by $(g_i + g_f)$

The product $\sigma(g)R_s$ is calculated on lines (7), (8), and (9) and added to the value of $g_o R_L$ on line (9). Otherwise, the calculations are identical with those for the common-emitter circuit. The conversion to intrinsic parameters is accomplished in a similar manner to that described above.

If the input admittance is required, lines (1) through (6) may be used for the calculation of the value of the numerator, taking R_s as 100 units and $m = 2$ on line

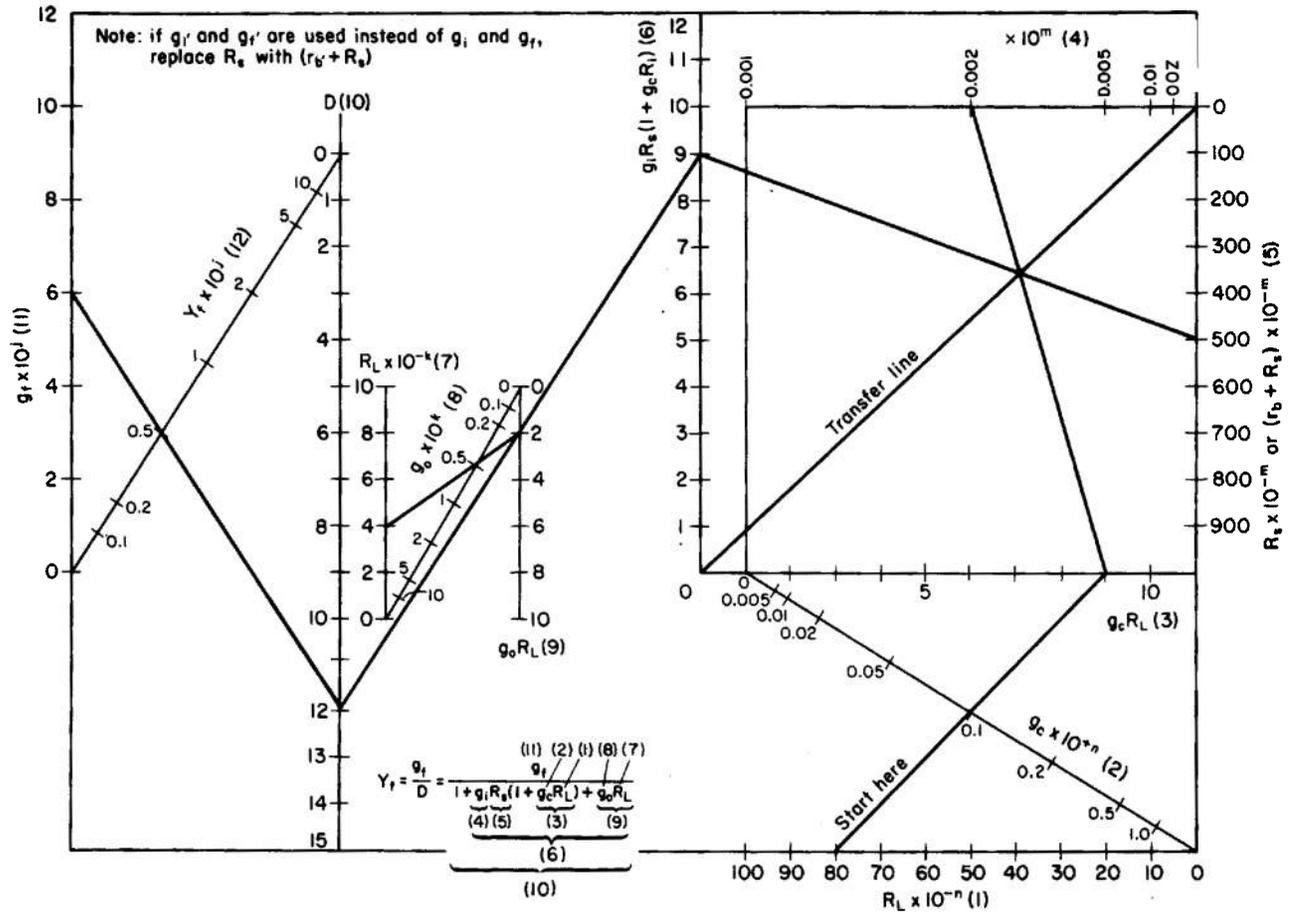


Fig. G-1. Admittance Nomograph

(5). If a value of $m = 0$ cannot be used on line (4), then the value used on line (4) should be included in a multiplying exponential 10^m for line (6). Lines (7) through (10) are used for the calculation of the denominator for the internal admittance for the circuit and lines (1) through (10) for the denominator for the generalized input admittance. The final quotient may be obtained by introducing the value obtained for the numerator on line (11) and the denominator on line (10). The answer appears on line (12).

Calculation of the output admittance uses the scales on lines (1) through (10) for the denominator unless the

value of R_L is zero. The numerator values may be obtained by calculation of $g_c R_s$ on lines (1), (2), and (3) and the use of line (4) for g_r . Once again the value for line (5) is taken unity (nominally 100 with $m = 2$) to give $g_c g_r R_s$ on line (6). The value of g_o may be added to this and the result inserted on line (11). Again, the final value may be read on line (12).

Correction to intrinsic parameters for this equation, and calculation of the input and output admittances for common-base and common-collector configurations follow the patterns already described. They are left as exercises for the reader.

REFERENCE

1. A. S. Levens, *Nomography*, Second Ed., John Wiley & Sons, Inc., New York.

APPENDIX H

INFORMATION ENGINEERING

H-1 GENERAL

Information engineering as an art and a science may be defined as the characterization, evaluation, and study of phenomena based on such factors as order of importance, order of independence, order of stability, order of consistency, and order of repeatability, among others. It involves principles of human engineering in that it is necessary to develop efficient ways of presenting information for assimilation, evaluation, application, and decision making by the user. It also involves information science in that a maximization of useful information content, and the corresponding reduction of information entropy, are key functions. It may involve the theory of graphs and graphics in that multidimensional relations between variables and parameters may be involved. It also can involve the theory of networks and channelization.

The ordering on the basis of importance is simply the determination of the rate of change of an important parameter whose control is desired with respect to other parameters and variables which are known to have influence on the parameters of principal concern. It is in effect the finding of the parameter or variable grouping creating the greatest or the maximum "rate of descent", and the order arrangement within the grouping successively creates substantially lower rates of descent as the more significant parameters are removed.

Clearly, a set of parameters selected for characterization of any device should rank as highly as possible on all of the ordering bases, and, in case of conflict, the bases also should be ordered to display the parameters in their proper relative order of importance in the application at hand. These are the processes and procedures which have been applied in establishing the curve and data formats described in Chapter 3 and elsewhere in this handbook.

The scope of application of these techniques and procedures is actually much broader than might be suspected from the previous discussion. They may be used as the basis for development of the principles which must apply in speed reading and for time-bandwidth compression in areas as far afield as the transmis-

sion of word messages and weather maps. They can also be applied in the development of tagging techniques for the retrieval of important technical information in verbal, tabular, or graphical form.

H-2 ORDER OF IMPORTANCE

Order of importance is commonly ignored as an important design parameter both in engineering and in consumer goods. For example, with the automobile, possibly the two most important functions the driver must be ready to perform with minimum delay are steering and braking. The importance of steering is recognized inasmuch as the steering function is provided through the use of both hands on the steering wheel. The braking function, which can be intermittently significantly more important, however, is not provided for with anywhere near the efficiency or **speed** of reaction as steering. The process of raising the foot, moving the foot, and after locating the foot on the brake pedal, pressing the foot, requires excessive reaction time after the decision to react has been made. As a result, the response time is much longer than justified in relation to the importance of the function. It is essential that the transfer to braking require only a minor change of mode of application of foot pressure compared to the acceleration mode if rapid safety reaction is to be achieved. In no other way can the critical second or more required for application of brakes be recovered. Order of importance in this general sense can be of vital importan—in fact, a life or death matter—and it is of extreme importance in the characterization of devices whose representation must be presented in multidimensional space.

H-3 ORDER OF INDEPENDENCE

The ordering on the basis of mutual independence can be of overriding importance also. Wherever possible, it is vital, and may be critical, to select the characterizing parameters in such a way that interaction can-

not mask the information which is required. A typical example of use of parameters whose interaction seriously restricts their use is the plotting of the transconductance of a triode tube as a function of control-grid bias. Actually, the transconductance can easily be shown to be a single-valued function of plate current, and it is impossible to specify it in a meaningful way in terms of grid voltage. The combination of grid voltage and plate voltage specifies the plate current, and the relation between plate voltage and plate current is one of the extremely unreliable parameters in the triode tube. As a result, the complexity of the specification of transconductance in terms of plate current through grid voltage leads to an almost indeterminate relation—as designers of practical triode circuits soon learn. The specification directly in terms of plate current is in a similar way found to be both effective and convenient.

H-4 ORDER OF STABILITY

The ordering on the basis of stability of parameters, in the organization of data for devices, is probably of equal importance to order of importance and order of independence. This factor is closely related to sensitivity in the sense used in network design in that the higher the stability of the data, the lower the sensitivity tends to be in the network sensitivity sense. A parameter which is directly derivable from basic solid-state relations such as the Ebers-Moll equations for the transistor is, for example, of orders-of-magnitude greater stability than one which is based on small differences of large and poorly-controlled numbers.

The question of using differences of nearly equal numbers is a serious question in active networks since the junction nature of these devices leads to an inherent differencing. Power gain is obtained only as the difference approaches zero. If the characteristic data are selected in such a way as to minimize the dependence on the differencing, reliable designs are possible; otherwise, not.

Stability can also depend on known variables like temperature, as is the case with the Fermi parameter $q/(kT)$. The absolute temperature, of course, only varies by a small percentage for the normal operating range of an electron device, so the effect on stability is quite small. The variation of transistor transadmittance is linear with the Fermi parameter, but only a second order variation exists with respect to minority carrier lifetime. On the other hand, base current is linearly dependent on the reciprocal of lifetime and, as a result, it is almost uncontrolled, making the stability of parameters based on base current very poor.

H-2

The current gain β for a transistor is an excellent example of a parameter whose value is very unstable. It is defined as the rate of change of collector current with respect to change of the highly unstable base current for the device. Derivation of the equation for β from the Ebers-Moll model for the device leads to a relation which apparently is relatively constant. Unfortunately, however, the equations for I_{c1} and I_{e1} are relatively independent of variations in diffusion and drift, lifetime, and diffusion length, whereas the difference between the currents is a linear function of reciprocal lifetime in particular. The effect of the drift field is to increase effective lifetime at small values of current, and the effect of the ionic mass-action law under high-injection conditions is to reduce lifetime very sharply. The device β is roughly proportional to effective lifetime.

H-5 ORDER OF CONSISTENCY AND REPEATABILITY

The ordering on the basis of consistency or repeatability is in some ways similar to ordering on the basis of stability, but at the same time there are distinct differences. Consistency of behavior means that characteristics do not change appreciably under the influence of environmental changes or abnormalities, and that they are relatively independent of the effects of minor variations in construction or processing of the product.

As an example, the amplification factors μ of a group of samples of a given type of tube, say the 12AU7, may all be consistent, roughly 20. At the same time, they may have modest instability of value in that the μ varies with operating point. Yet, the μ may have relatively little importance, in that it gives no indication whatever about the relative power-handling ability of the tube. Yet power-handling ability is one of the most important and critical parameters required in the design of reliable active networks. In fact, the power level above which failure due to dissipation is no longer statistical in nature, but begins to become a deterministic problem, is probably one of the more important, and one of the most consistent and repeatable, parameters for all active devices. It is a function of ambient temperature and, since the thermal properties of the device and its case are rather readily controlled, it of necessity must be consistent from unit to unit when proper production standards are adhered to in the factory.

H-6 EXAMPLES

As examples of effective application of the principles of information engineering to electron tubes, Fig. H-1 presents a typical set of triode plate characteristic curves for the 6BQ7A dual-triode tube, and Fig. H-2 a set of pentode screen characteristic curves for the 6BH6 tube. The basic principles of design of these curves are as described previously and as used in the preparation of the device curves in Appendix F. The use of these curves in the design of circuits is described in detail in Refs. 1 and 2.

Particular note should be given to the use of contours of constant power dissipation and the contours of constant conductance and transconductance on these figures. The conductance contours typically depend on the Fermi parameter $q/(kT)$ and on the conductance

efficiency, κ , in addition to the appropriate value of current (e.g., collector current). It is for this reason that these sets of contours should be used as the basis for design for reliability.

With the pentode tube, the rapid change of plate current with screen voltage is clearly visible in Fig. H-2. The great importance of the variation of plate current with screen voltage as compared with plate voltage is clearly evident from this curve, and the advantages available in minimizing power input through careful selection of screen voltage are likewise plainly evident. Actually, calculations at a series of screen voltages show that there is an optimum screen voltage to use, since power input increases rapidly for screen voltages in excess of optimum, but power output changes little if at all. (With a frequency-multiplier amplifier, the output power actually decreases as screen voltage is raised above the optimum value.)

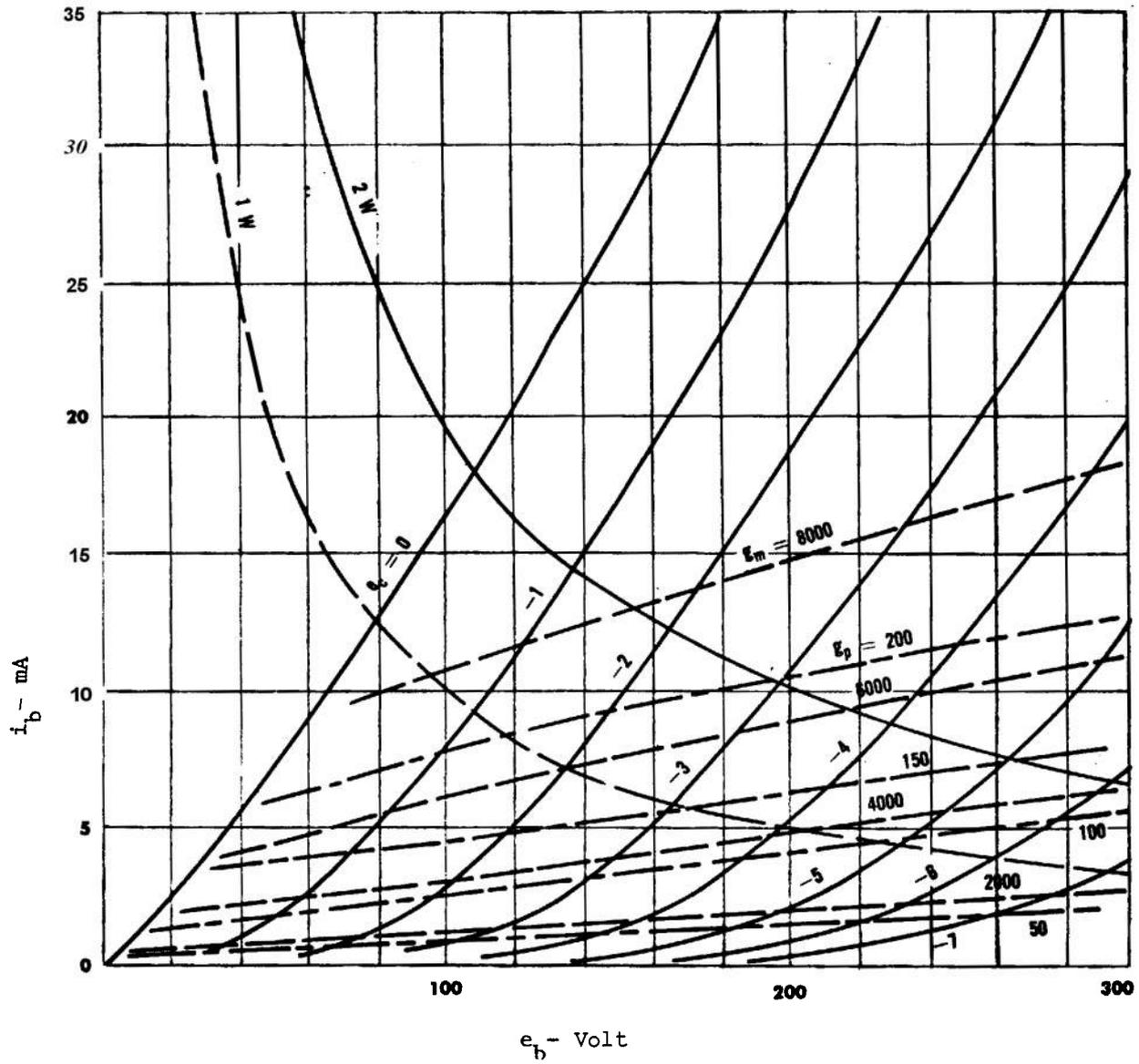


Fig. H-1. Plate Characteristic Curves, Tube 6BQ7A

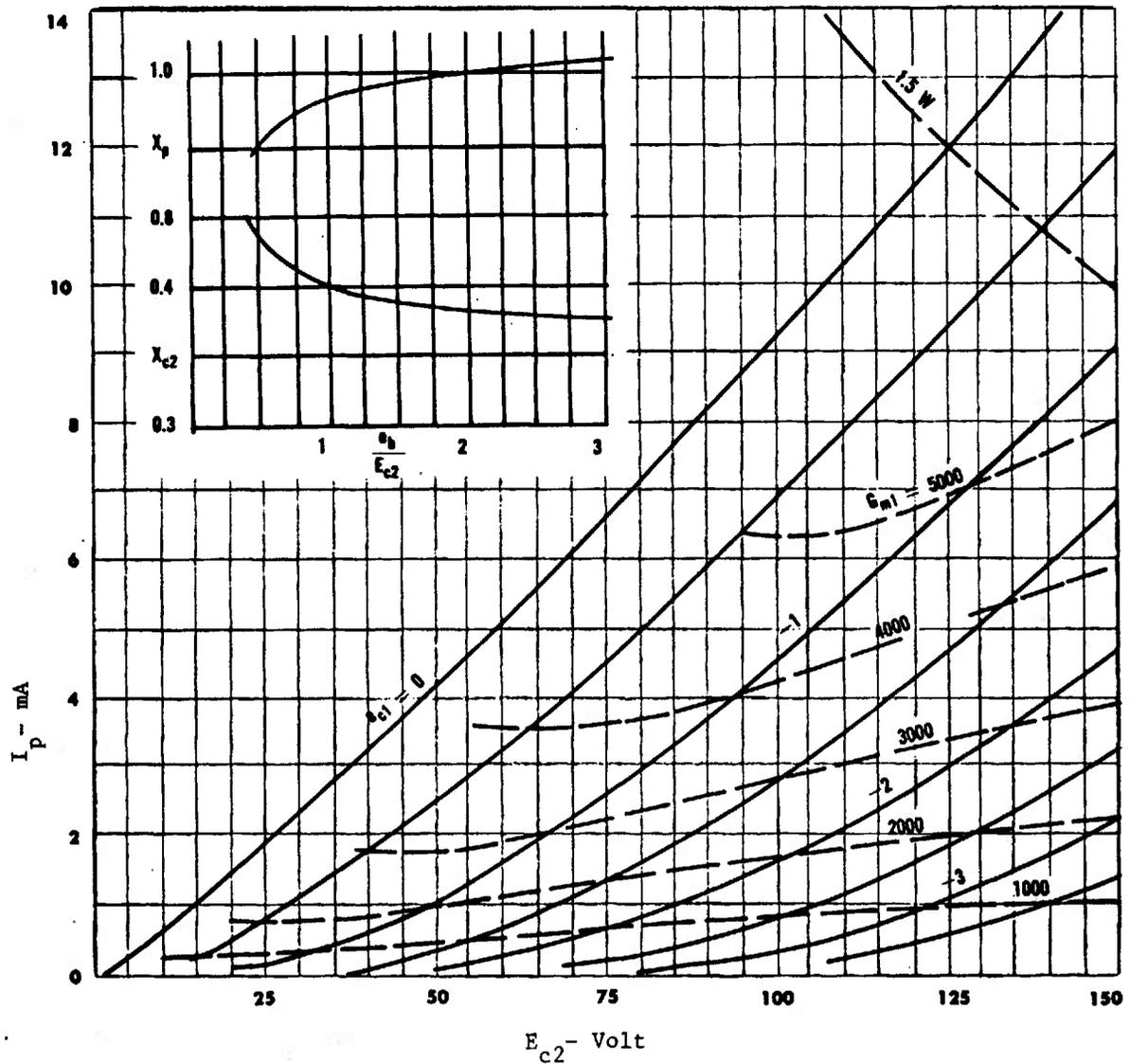


Fig. H-2. Screen Characteristic Curves, Tube 6BH6

REFERENCES

1. K. A. Pullen, Jr., *Conductance Curve Design Manual*; John F. Rider Publishers, New York, 1959.
2. K. A. Pullen, Jr., *Conductance Design of Active Circuits*, John F. Rider Publishers, New York, 1959.

APPENDIX I

THE RELATION OF THE FERMI LIMITATION TO FET DEVICES

The general theory of FET devices has been developed by Shockley and by Dacey and Ross and others, and it covers quite adequately the normal operating range for these devices. Experiment in fact has shown that under the normal operating conditions encountered, the devices do largely respond as specified by the Shockley-Dacey-Ross equations. The basic equations neglect the effect of contact potential (strictly the Fermi level potential) across differently doped zones in the semiconductor device. Correction for this is required, but the correction is easily made.

The equations which Dacey and Ross have developed (based on Shockley) for the transconductance for the field-effect transistor are complex, and they show the transconductance per unit current to be a function of both the gate-to-drain voltage and of the gate-to-source voltage. Both of Shockley's equations and these equations of Dacey and Ross have been verified experimentally in the normal range of operating currents, and, consequently, are completely adequate for normal operating conditions.

If one reduces the level of operating current in these devices to approximately one-thousandth that normally encountered, at least two interesting effects can be noted. The first of these is that rather than potential changes of the order of volts being required to cause a change of drain current by a factor of two-to-one, now a voltage less than 20 mV may be required. (For Metal-Insulator-Semiconductor, or MIS, devices, the voltage may be as much as 40 to 50 mV.) As a matter of fact, this condition of a very small voltage required for the two-to-one change may exist over from three to five orders of magnitude of drain current, and it is completely independent of drain-to-source voltage at the same time!

Clearly, these data indicated that a mode of operation other than the strict Shockley mode must exist. An examination of Shockley's original paper provided a lead in that just after Eq. 3, p. 1366, Shockley has stated that he neglects the effect of the potential jump across the "Debye-length" transition region. If in fact this

potential jump should provide the maximum field rather than be negligible, one might expect a constant voltage increment to be required for a given current change ratio. This new mode of operation can be called either the diffusion or the "Fermi-mode" of operation, since it is controlled by the Fermi parameter $q/(kT)$ with an efficiency (or κ) factor approaching either unity for JFET devices (diode or junction devices) or approximately one-half for MIS devices.

Application of two-dimensional field theory for a channel having varying conductivity is enlightening in that it is readily determined that at the exact center of the symmetric channel, where the flow occurs under the Fermi-mode of operation, the field gradient is a minimum. If, then, the doping and channel conductivity are varied in a manner to lead to conditions for minimum gradient, it is found that the conductivity should be a minimum at the channel center and should increase exponentially in either direction from the center. (Strictly, a distribution based on the cosh or catenary function results.) Under these conditions, the transverse field is a minimum, and such field as exists is axial, just the condition for drift-aided diffusion.

From another point of view, one can note that the increased concentration of dopants will cause the current flow to concentrate in two thin layers adjacent to the depletion region, and a minimum amount of uncontrolled current will flow in the channel center. The result is a high transconductance efficiency.

The possibility of grading the channel doping leads to the possibility of controlling the value of κ , and leads to new and unique possibilities for development of higher-power solid-state devices. Values of κ intermediate to those presently available with FET devices of conventional design and those available with bipolar transistors can lead to RF devices of substantially increased potential power output.

It is possible to determine the value of κ desired for any RF application. The output tuned impedance for any amplifier should be between approximately 20 and 200 ohms for easy and effective matching to a coaxial

transmission line. This means that the supply voltage must be allowed to increase proportional to the desired device current, and, for a constant voltage gain, the value of κ must decrease as an inverse function of output current. For a stage voltage gain of about 100, the allowed transconductance, therefore, is in the range from 0.5 mho to 5 mhos. The corresponding κ -factor is of course given by the equation

$$\kappa = g_m / (39 I_d) \quad (I-1)$$

where the value 39 is the value of the Fermi parameter, 39 mhos per ampere, and where either g_m and I_d are both average values or they may both be peak values. The transconductance g_m is measured in mhos in this equation, and the drain current I_d in amperes.

The power output P_o is related to the power input, which is a function of the relation

$$P_o = \eta I_d^2 Z_L, W \quad (I-2)$$

where η is the stage efficiency and Z_L is the load impedance. Clearly, the output capability P_o is proportional to I_d^2 when the κ can be varied, but it is a function of the equation

$$P_o = \eta I_d \times 10, W \quad (I-3)$$

when the value of κ is fixed at near unity, as is the case with the bipolar transistor.

REFERENCE

1. W. Shockley, "A 'Unipolar' Field-Effect Transistor", Proc. IRE, Nov. 1952, p. 1365.

PROBLEMS

Chapter 1

1. Calculate the value of energy for the ten and ninety percentile points for the Fermi function, $F(E)$. Take Boltzmann's constant as 8.3×10^{-6} V per deg and use room temperature for the calculation.

2. Plot the slope of the Fermi function $F(E)$ as a function of the absolute temperature at the 10%, 50%,

n_i	n_n	n_p	p_n	p_p	polarity
For germanium:					
2.5×10^{13}	10^{16}				
2.5×10^{13}			108		
2.5×10^{13}				5×10^{18}	
For silicon:					
1.5×10^{10}	2×10^{12}				
1.5×10^{10}			108		
Unknown:					
10^{12}			109		

5. If the gap energies of germanium and silicon are 0.78 and 1.2 V, respectively, what are the maximum values of base-to-emitter bias required to offset the gap bias and cause a start of conduction? Discuss the reason why this barrier potential may be as small as 0.1 V with a germanium device.

6. If the minority-carrier transit for a particle across the base region of a given transistor is 0.1 μ sec, and the ratio of the base-width to the mean-free-path is 0.10, what is the effective diffusion time across the base region? What is the approximate radian frequency for the upper noise corner (ω_{n2})? What is the minimum value of beta for the transistor, and what is its probable value?

7. Estimate the value of the collector-series resistance for the 15118 transistor, based on the slope of the collector characteristic curves in the saturation region, Appendix G. Repeat for the 2N1613 and the 903/2N1149 transistors.

Chapter 2

1. Convert sets of static contours such as those

and 90% points. Discuss briefly the significance of the slope.

3. Look up the values for the constants in Eq. 1-5 for both germanium and for silicon, and calculate the resulting values of n_i to be expected, and their rate of change with temperature.

4. Calculate the data which are missing in the following table:

n_i	n_n	n_p	p_n	p_p	polarity
For germanium:					
2.5×10^{13}	10^{16}				
2.5×10^{13}			108		
2.5×10^{13}				5×10^{18}	
For silicon:					
1.5×10^{10}	2×10^{12}				
1.5×10^{10}			108		
Unknown:					
10^{12}			109		

provided on the 2N456 transistor into a coordinated set similar to those presented in Appendix F. Calculate the approximate value of r_c' from the low-voltage curves. (These data have been reproduced from the RCA data sheets for the 2N456 transistor.) For the plotting, assume that the input contours for values of collector voltage greater in magnitude than 1.5 V coincide with the values for 1.5 V.

2. Convert the static curves on the 2N1090 transistor into a coordinated set. Determine the approximate value of r_c' for this transistor. (Attached data have been reproduced from the RCA data sheet for the 2N1090 transistor.)

3. Derive the relations among the H , Y , and Z parameters.

4. Derive the configuration relations among common-emitter, common-base, and common-collector hybrid parameters.

5. Derive the configuration relations for the admittance parameters.

6. Derive the configuration relations for the impedance parameters.

7. Derive the values of the common-emitter conductances from Eqs. 2-16 and 2-17, giving the values of

f_{max}	f_t	f_β	$r_{e\alpha}$	r_b	C_c	$r_b C_c$	α	β
100 MHz					5 pF	0.1 ns		100
	90 MHz		50 MHz	100 ohm	2 pF		0.90	
				50 ohm		0.1 ns	0.90	

where pF = 10^{-12} F and ns = 10^{-9} sec.

9. Derive Eqs. 2-31 through 2-33.

Chapter 3

1. Derive Eq. 3-58.
2. Derive Eq. 3-59.
3. Derive Eq. 3-60.

Chapter 4

1. Derive Eqs. 4-3 and 4-5 by Kirchhoffs laws.
2. Repeat Problem 1 using the topological method of Appendix B.
3. Derive Eqs. 4-7 and 4-8, and the corresponding equations in terms of impedance parameters, and tabulate the substitutions required to convert one to the other. What conclusions can you draw from these relations?
4. Derive Eqs. 4-9, 4-13, 4-14, and 4-19.
5. Derive Eqs. 4-10, 4-15, 4-16, and 4-20.
6. Derive Eqs. 4-22 and 4-23.
7. Derive Eqs. 4-21 and 4-24.
8. Derive Eqs. 4-25 and 4-28 by Kirchhoffs laws.
9. Derive Eqs. 4-26 and 4-27 by Kirchhoffs laws.
10. Repeat Problem 8 using topological methods.
11. Repeat Problem 9 using topological methods.
12. Derive Eqs. 4-32 through 4-34.
13. Derive Eqs. 4-37 through 4-40.
14. Derive Eq. 4-46.

Chapter 5

1. Design an amplifier similar to that in Example 5-1, using a 2N247 transistor, a supply voltage of 5 V, and a load resistance of 1000 ohms. Select the optimum base bias resistance.
2. Repeat the distortion calculations of Problem 5-1, using the static data only in conjunction with the orthogonal polynomial techniques described in Appendix C. Again determine the optimum operating conditions.
3. Design an amplifier using the 2N270 transistor with a supply voltage of 5 V and a load resistance of 100 ohms. Use orthogonal methods to obtain the small-signal input admittance and the forward admittance,

g_{11} , g_{12} , g_{21} , and g_{22} in terms of these equations.

8. Fill in the appropriate vacancies in the table:

and select a suitable operating point.

4. If a transistor amplifier has a supply voltage of 10 V, a static load resistance of 1000 ohms, and a dynamic load resistance of 500 ohms, select the optimum operating conditions assuming that the amplifier is linear. What is the maximum static and maximum dynamic dissipation for the transistor?

5. Design an amplifier using a GT761 transistor, first as a common-emitter amplifier, and then as a common-base amplifier. Tabulate their input admittances and gains with a supply voltage of 5 V and a load resistance of 1000 ohms. Tabulate the power gains for both configurations.

6. Introduce 100 ohms as an emitter-degenerative resistor in the common-emitter amplifier in Problem 5-5. Determine the input admittance and the amplification and distortion for the resulting amplifier, and compare with the undegenerated amplifier.

7. Introduce a shunt feedback network across the amplifier of Problem 5-5. Take the source impedance of the signal source as 1000 ohms, and the feedback admittance as 100 micromhos. Calculate the input admittance, the current and voltage gains and distortion, and compare these results with the results of Problems 5-5 and 5-6.

8. Based on the data tabulated in Problems 5-5 and 5-6, discuss the behavior of cascaded R-C coupled amplifiers in the C-E and C-B configurations. Discuss the physical limitations which develop in the cascaded circuits, and determine how the difficulty can be corrected.

9. In cascading degenerative R-C amplifiers, which of the types discussed in this chapter should be used? Justify your selection.

Chapter 6

1. Determine the stability function per unit of gain for an emitter-degenerative amplifier as a function of base-spreading resistance. The output admittances may be considered negligible if desired. Take $R_{c2} = 0$.

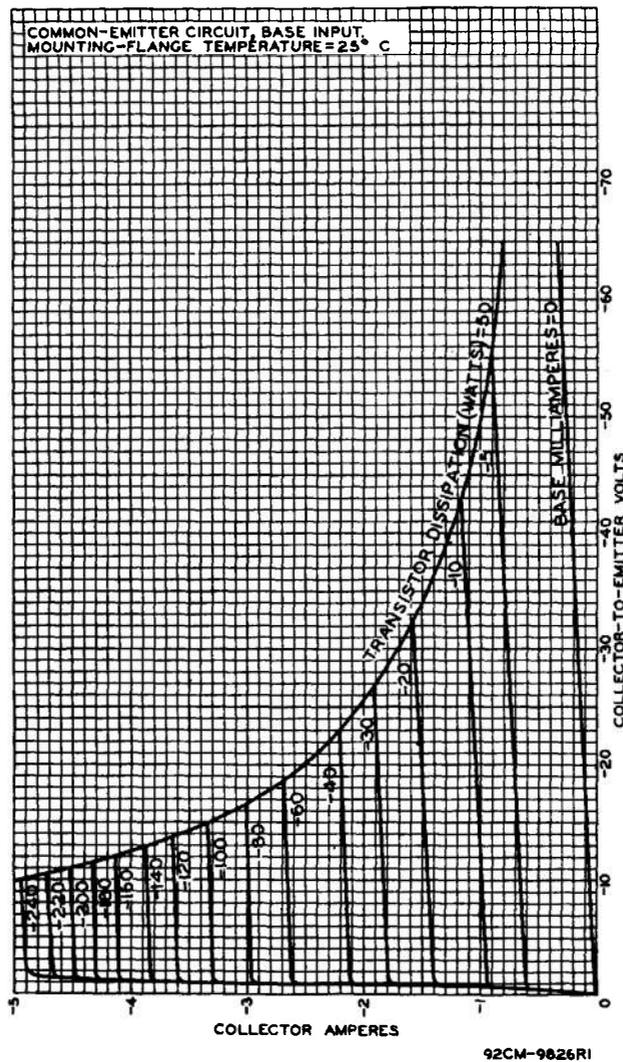
2. Determine the maximum or minimum value of the function of Problem 6-1. Take r_b as the maximizing parameter. Discuss the significance of the result. Would you expect this?

3. What values of C , in Eq. 6-32 should be made available to designers for use in instrument design? Discuss in detail the reasons for your choices.
4. Derive a stability equation for the amplifier of Fig. 6-4.
5. Modify the design of the amplifier in Problem 5-1 to introduce a factor-of-five improvement in the current stabilization. Complete the resulting design.

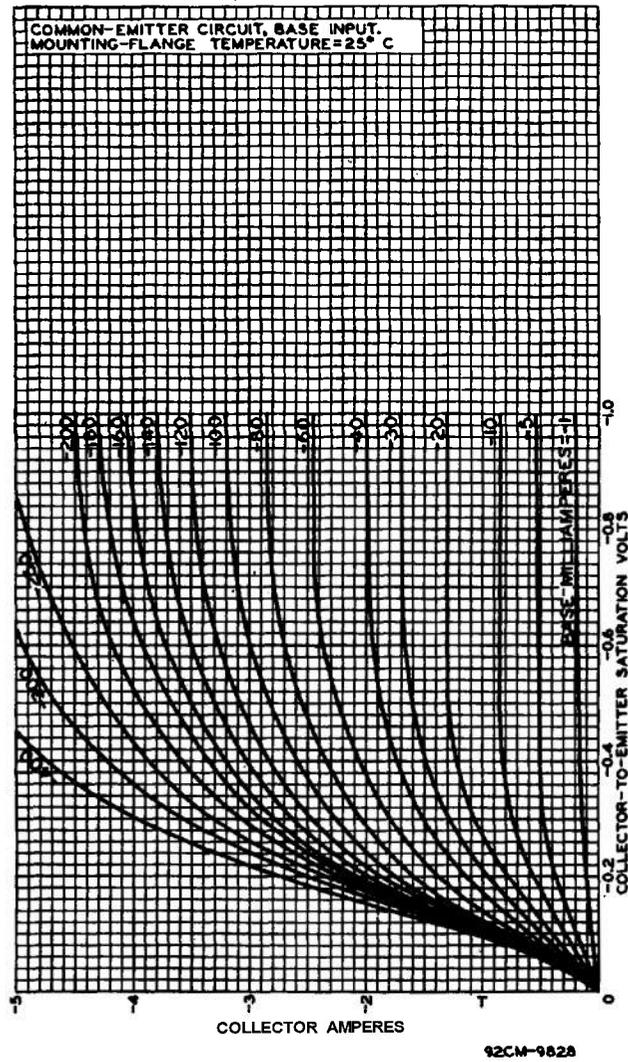
6. Modify Problem 5-2, to increase the current stability by a factor of ten. Complete the corresponding design.

Chapter 7

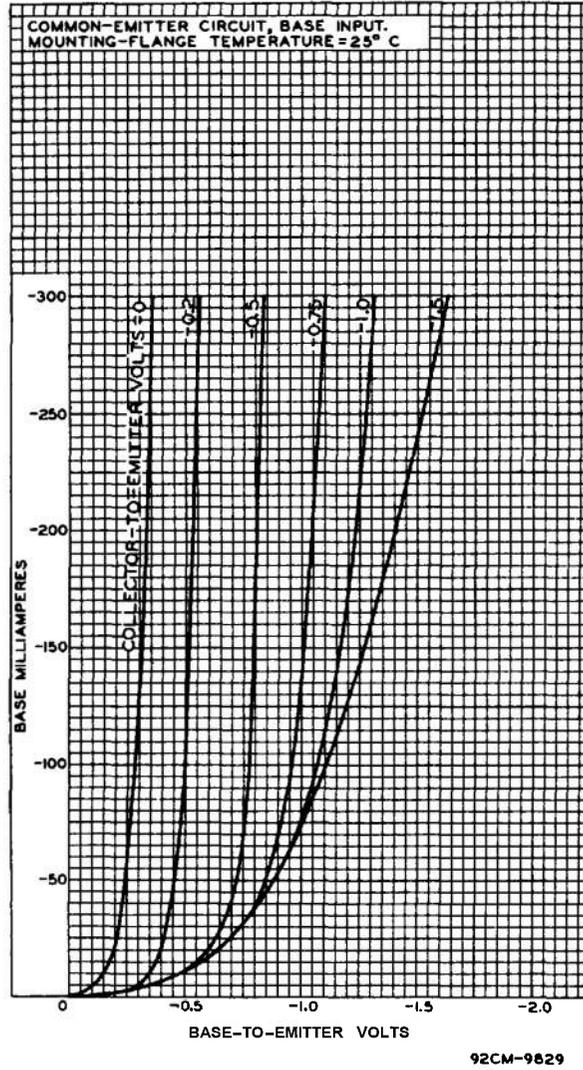
1. Derive Eq. 7-1.
2. Derive Eq. 7-4.



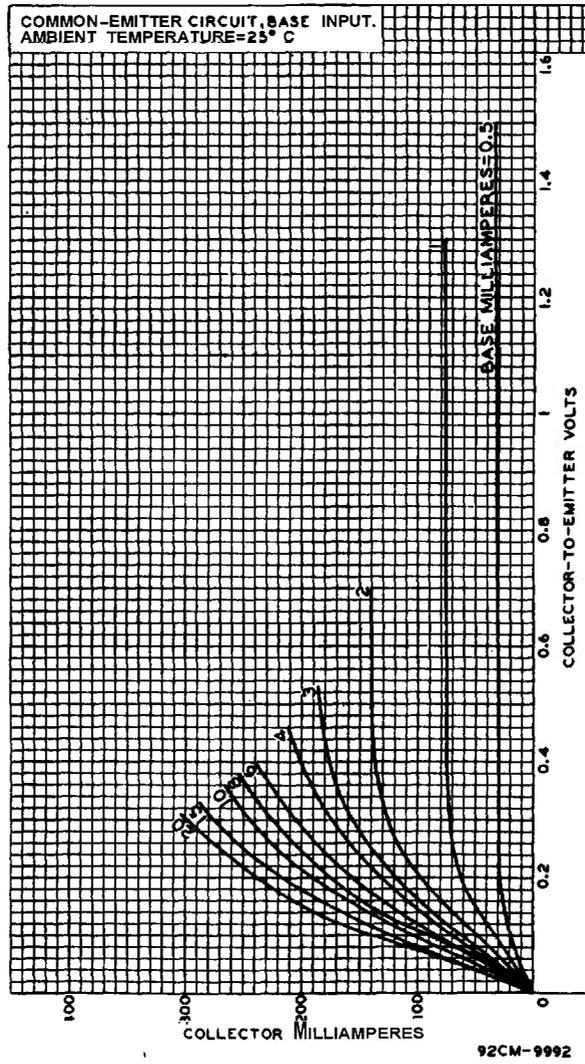
Problem 2-1. Fig. P-1



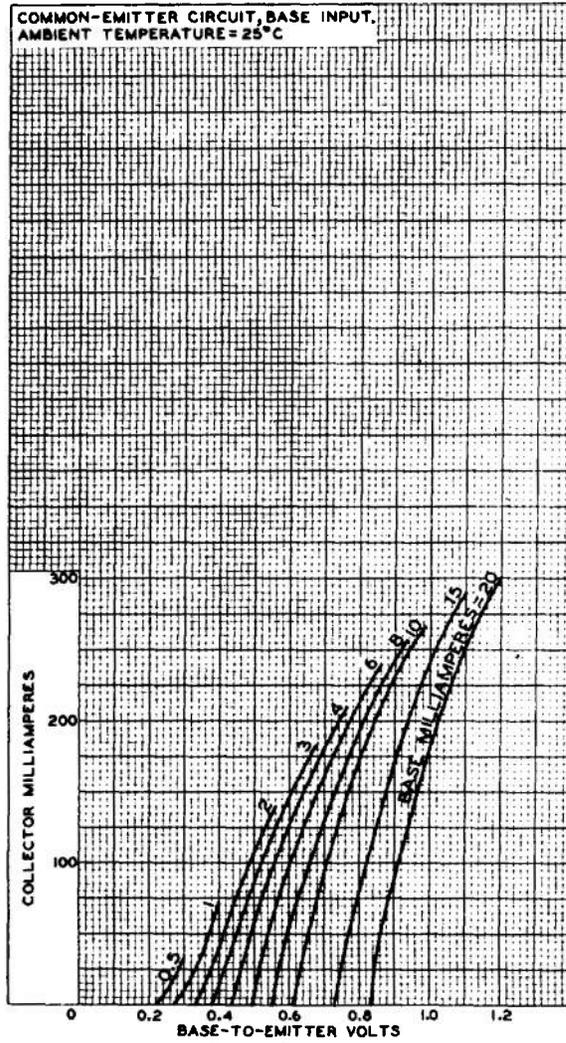
Problem 2-1. Fig. P-2



Problem 2-1. Fig. P-3



Problem 2-1. Fig. P-4



92CM-9990

Problem 21. Fig. P-5

3. Verify the limit-frequency conditions in Eqs. 7-5 through 7-8.
4. Verify Eq. 7-9.
5. Repeat Example 7-1 using the 2N301A transistor. Select your own operating conditions.
6. Repeat Example 7-2 using a 2N270 transistor as a driver and a 2N459 for the output. Use orthogonal methods.
7. Repeat Example 7-4 using a pair of 2N268 transistors.
8. Repeat Example 7-4 using orthogonal methods on a pair of 2N459 transistors.

Chapter 8

1. Derive the equation for amplification of a common-emitter amplifier using a nonzero value for $r_{c'}$. Compare with previous results. Include a separate collector-base capacitance (to the intrinsic base, not the base terminal).
2. Repeat Problem 8-1 for the common-base amplifier.
3. What effect might the presence of $r_{c'}$ have on the apparent value of f_t for a transistor? Derive and discuss the results.
4. Select a transistor having an f_{n2} greater than 50 MHz, and design an amplifier using it for operation at 50 MHz. Let the design parallel that for Example 8-2. Use orthogonal methods for obtaining small-signal data.
5. Design unilateralization networks for the amplifier of Problem 8-4 and for that of Example 8-2.
6. Plot the variation of K with bias current for the amplifiers of Example 8-2 and Problem 8-4, both with and without a shunt input loading impedance of 30 ohms. Take the source impedance as 20 ohms. Design a differential amplifier for providing constant input load, and calculate the effect of the input loading.
7. Select a tunnel diode for use with 50 ohm coaxial cable, and design the components required for using it at 100 MHz.

Chapter 9

1. Derive Eqs. 9-7 and 9-10.
2. Verify Eq. 9-14.
3. Derive Eqs. 9-15 and 9-16.
4. Derive Eq. 9-18.
5. Derive Eq. 9-20.
6. Solve Example 9-1 completely, including Fourier, Legendre, and orthogonal solutions. With the latter, solve for the conditions $(2n + 1) = 11, 15, \text{ and } 19$. Make trapezoidal corrections.

P-8

7. Repeat Problem 9-6 for $y = x^3$ as the basic device relation.

Chapter 10

1. Derive Eqs. 10-1 through 10-3 and Eqs. 10-5 through 10-8.
2. Derive Eqs. 10-10, 10-11, 10-11a, and 10-12.
3. Derive Eqs. 10-14, 10-15, 10-18, 10-18a, 10-18b, and 10-19.
4. Assume that a transistor matching the curves for the 2N247 has a value of $f_{n2} = 100$ MHz, and design a Colpitts oscillator for use at 75 MHz based on it. Determine limit contours and oscillation amplitude.
5. Repeat Problem 10-4 using a Hartley circuit.
6. Design a Colpitts oscillator based on the 2N502 transistor operating at 100 MHz. Use orthogonal techniques.
7. Design a series-mode crystal oscillator for use with a 25 MHz crystal and a 2N1613 transistor. Take the series-resonant resistance of the crystal as 10 ohms, and its Q -factor as 10^6 .
8. Calculate the frequency stability of the oscillator for Problem 10-7 in terms of its probable RMS value for ΔK_{σ} .

Chapter 11

1. Derive Eqs. 11-1 through 11-3.
2. Derive Eqs. 11-4 and 11-5.
3. Derive Eqs. 11-11 through 11-13.
4. Derive Eq. 11-17.
5. Derive Eqs. 11-24 through 11-29.
6. Design the amplifiers and impedance converters required for a forward-transmission, three-stage, phase-shift oscillator. Verify the adequacy of the terminating impedance levels.
7. Repeat Problem 11-6 using a reverse-transmission network.
8. Design the amplifiers required for use with a transistor zero-phase-shift oscillator, and verify the adequacy of the terminating impedance levels.

Chapter 12

1. Derive the values of conversion gain listed in Table 12-1.
2. Derive Eqs. 12-16 and 12-16a from Eq. 12-15.
3. Repeat Example 12-1 using the 2N1613 transistor and orthogonal techniques.
4. Verify the topological derivation of Eqs. 12-17 through 12-20.
5. Establish Eq. 12-32 topologically.
6. Determine the circuit characteristics required of

the tunnel diode that it be usable as an oscillating modulator having reasonably linear behavior. The objective is to obtain an amplified signal by detection of the modulation envelope. Assume a square-law variation of conductance with bias.

7. Discuss the behavior of the circuit of Problem 12-6 with a cube-law variation for the diode conductance. Can a tunnel diode have such a conductance?

8. Establish the limiting conditions which must be applied to Problem 12-6, and see if you can find a way to generalize the above procedures.

Chapter 13

1. Repeat the design of Example 13-1, using the 2N697 transistor and orthogonal methods of determining the small-signal properties. Take $V_{cc} = 10$ V, and select your own load resistance.

2. Repeat Problem 13-1, using the 2N1613 transistor.

3. Repeat Example 13-2 using the 2N1220 transistor as the active device and calculate small-signal values by orthogonal methods. Take $V_{cc} = -12$ V.

4. Repeat Problem 13-3 using the SBDT-10X transistor with a supply of 5 V.

Chapter 14

1. Repeat Example 14-1 for conditions applying to a silicon transistor, i.e., $|V_{bz}| = 400$ mV.

2. Derive Eq. 14-1.

3. Repeat Example 14-2 using the 2N1613 transistor and $|V_{cc}| = |V_{bb}| = 10$ V.

4. Repeat Example 14-3 using the 2N697 transistor with a supply voltage of 8 V. Discuss ways in which the design can be improved.

5. Determine the number of diodes which may be used in a matrix consisting of 1N873A Fairchild diodes. Test conditions for the diodes are:

Maximum forward voltage = 1 V at 150 mA.

Maximum reverse current = 15 μ A at -75 V.

Reverse recovery time = 0.3 μ sec at 30 mA.

Capacitance = 3.5 pF.

Take the barrier potential as 0.4 V, and take the reverse current to be ohmic current.

6. Design a control circuit for a bi-directional binary counter such as is described in this chapter.

7. Design a reset circuit for a decade bi-directional counter based on the described configuration. Include all the sensor and the switching circuits.

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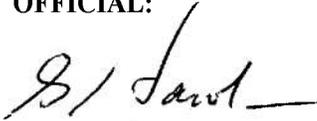
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		445	Subst. Technology Performance
		470	*Nuclear Conversion Guide for Military Applications

*NOTE: REVISION--not available
 **REVISION UNDER REPARATION
 ***OUT OF STOCK