UNCLASSIFIED

AD NUMBER
AD918277
LIMITATION CHANGES
TO: **Approved for public release; distribution is unlimited.**
FROM: **Distribution authorized to U.S. Gov't. agencies only; Test and Evaluation; 03 APR 1974. Other requests shall be referred to Air Force Weapons Lab., Attn: AFWL/ELA, Kirtland AFB, NM 87117.**
AUTHORITY
AFWAL ltr dtd 18 Apr 1975

THIS PAGE IS UNCLASSIFIED

THIS REPORT HAS BEEN DELIMITED
AND CLEARED FOR PUBLIC RELEASE
UNDER DOD DIRECTIVE 5200.20 AND
NO RESTRICTIONS ARE IMPOSED UPON
ITS USE AND DISCLOSURE.

DISTRIBUTION STATEMENT A

APPROVED FOR PUBLIC RELEASE;
DISTRIBUTION UNLIMITED.

AD-918277-L

WL-TR-74-58 c.1

(1)

EMP

ELECTRONIC DESIGN

HANDBOOK

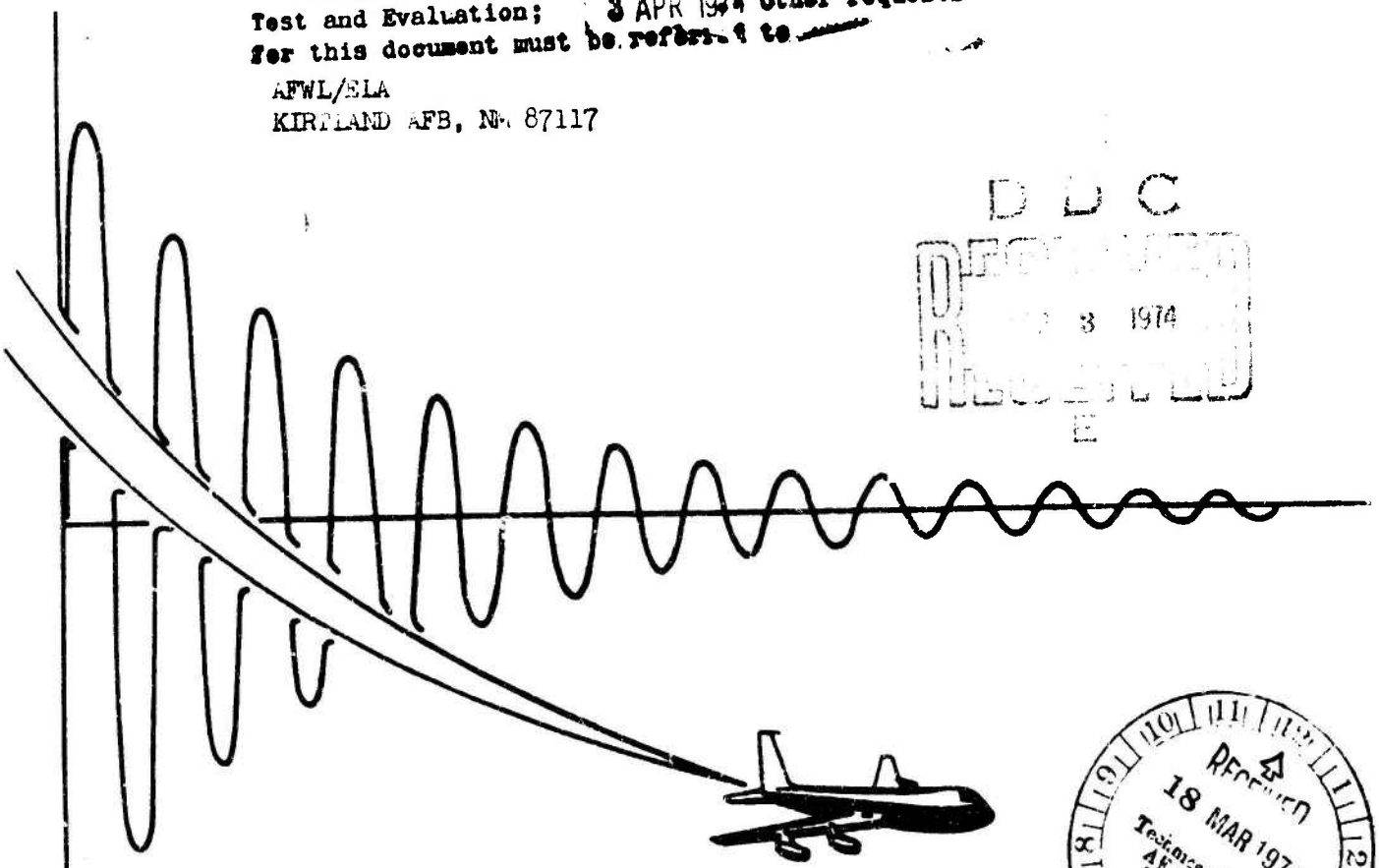
APRIL 1973

LC

Distribution limited to U.S. Gov't. agencies only; Test and Evaluation; 3 APR 1974 Other requests for this document must be referred to

AFWL/ELA
KIRTLAND AFB, NM 87117

DDC
RECEIVED
3 1974
E



RECEIVED
18 MAR 1974
Technical Library
AF Weapons
Laboratory

UNDER CONTRACT: F29601-72-C-0028

BY: THE BOEING COMPANY SEATTLE, WASHINGTON

PREPARED FOR: U.S. AIR FORCE WEAPONS LABORATORY, KAFB

D224-10019-1

AFWL-TR-74-58

EMP

AFWL-TR-74-58

ELECTRONIC DESIGN HANDBOOK

APRIL 1973

PREPARED UNDER CONTRACT NO. F29601-72-C-0028
PROJECT OFFICER CAPT. G. MICHAELIDIS

WORK ORDER 2-9

TASK OFFICER L. G. EICHWALD

BY

THE BOEING COMPANY
SEATTLE, WASHINGTON

AND

BRADDOCK, DUNN AND McDONALD, INC.

ALBUQUERQUE, NEW MEXICO

FOR

U.S. AIR FORCE WEAPONS LABORATORY
KIRTLAND AIR FORCE BASE
ALBUQUERQUE, NEW MEXICO

PREFACE

This handbook provides a state-of-the-art compilation of EMP hardening design information in a format of immediate use to electronic designers. Candidate hardening techniques are identified and their implementation is discussed. Pertinent design data are presented and detailed hardening examples are provided. In many cases the required design data were generated directly for this handbook. The appendix provides a general description of the test program.

The handbook is organized in four main sections and 11 chapters. Section I provides a general introduction and overview for EMP hardened design. Section II treats good design practices for all phases of subsystem design. Section III treats specific hardening techniques for subsystems or circuits known to require EMP hardening. Section IV presents examples of the design of specific hardened circuits.

This handbook has been prepared by Aeronautical Systems EMP Program personnel of The Boeing Company and their subcontractor, Braddock, Dunn and McDonald, Inc., located in the First National Bank Bldg., East, Albuquerque, New Mexico. The Program Manager is J. J. Dicomes and the Technical Director is W. L. Curtis. The principal Investigator for this work order is B. P. Gage. BDM efforts on this program are directed by J. J. Schwarz. The contributors to the volume are: R. M. Brown, D. L. Durgin, B. P. Gage, C. R. Jenkins, G. J. Rimbert, J. J. Schwarz, M. L. Vincent, and J. L. Wells.

TABLE OF CONTENTS

		Page
SECTION I		1-1
CHAPTER 1	INTRODUCTION	1-1
	1. BACKGROUND	1-1
	2. SCOPE	-2
	3. OVERVIEW	-3
	a. General	1-3
	b. Damage	1-4
	c. Upset	1-6
	4. SUMMARY	1-13
SECTION II	DESIGN PRACTICES	II-1
CHAPTER 2	SYSTEM DESIGN	2-1
	1. INTRODUCTION	2-1
	2. ERROR CRITICALITY REDUCTION	2-2
	3. PARAMETER CONSTRAINT ANALYSIS	2-6
CHAPTER 3	HARDENED CIRCUIT DESIGN	3-1
	1. INTRODUCTION	3-1
	2. COMPONENT PARAMETER OPTIMIZATION	3-1
	3. ANOMALOUS STATES	3-4
	a. Unstable Responses	3-5
	b. Stable Responses	3-9
	4. TRANSIENT ISOLATION	3-12
	5. HYBRID TECHNIQUES	3-16
	6. REFERENCES	3-20
CHAPTER 4	COMPONENT RATINGS	4-1
	1. INTRODUCTION	4-1
	2. SEMICONDUCTOR JUNCTION DEVICES	4-1
	3. INTEGRATED CIRCUITS	4-2
	a. Damage	4-2
	b. Upset	4-4
	4. NONSEMICONDUCTOR COMPONENTS	4-11
	5. REFERENCES	4-13
CHAPTER 5	PACKAGING	5-1
	1. INTRODUCTION	5-1
	2. ZONING	5-2
	a. Layout	5-2
	b. Zone Design	5-6
	3. SHIELDING	5-7
	a. Shield Selection	5-7
	b. Structural Integrity	5-8
	c. Penetrations	5-10

TABLE OF CONTENTS (Continued)

		Page
	4. GROUNDING	5-11
	a. Grounding Requirements	5-11
	b. Bonding	5-15
CHAPTER 6	SUPPRESSION DEVICES	6-1
	1. INTRODUCTION	6-1
	2. TPD IDENTIFICATION	6-3
	a. General	6-3
	b. Dielectric Breakdown Devices	6-3
	c. Semiconductor Breakdown Devices	6-7
	d. Nonlinear Resistors	6-10
	e. TPD Combinations	6-12
	3. RESPONSE CHARACTERISTICS	6-14
	a. General	6-14
	b. Standby Parameters	6-15
	c. Protection Parameters	6-17
	d. Failure Parameters	6-27
	4. REFERENCES	6-27
CHAPTER 7	FILTERS	7-1
	1. INTRODUCTION	7-1
	2. FILTER RESPONSE CHARACTERISTICS	7-2
	3. FILTER DISCUSSION	7-3
	a. Discrete R, L, C Filters	7-4
	b. Ferrite Beads	7-5
	c. Filter Pin Connectors	7-6
	d. Active Filters	7-9
	e. Distributed Passive Filters	7-10
	f. Electromechanical Filters	7-11
	4. APPLICATION SUMMARY	7-12
	5. REFERENCES	7-14
SECTION III	HARDENING TECHNIQUES	III-1
SECTION IV	HARDENED DESIGN EXAMPLES	IV-1
CHAPTER 8	DECOUPLING	8-1
	1. INTRODUCTION	8-1
	2. DIFFERENTIAL SIGNALING	8-2
	a. Balanced Cables	8-2
	b. Interface Circuitry	8-4
	3. ELECTRO-OPTICS	8-5
	a. Optical Conductors	8-6
	b. Photon Couplers	8-7

TABLE OF CONTENTS (Concluded)

		Page
	4. OTHER DECOUPLING METHODS	8-8
	5. REFERENCES	8-10
CHAPTER 9	ERROR DETECTION	9-1
	1. INTRODUCTION	9-1
	2. ERROR DETECTING CODES	9-4
	3. ERROR CORRECTING CODES	9-6
	4. SINGLE ERROR CODES	9-7
	5. INTERLEAVING	9-8
	6. HYBRID SYSTEMS	9-10
	a. Detect and Reject System	9-12
	b. Automatic-Repeat-Request (ARQ) System	9-12
	c. Circumvention	9-13
	7. APPLICATION GUIDELINES	9-15
CHAPTER 10	UPSET HARDENING EXAMPLE	10-1
	1. SYSTEM DESCRIPTION	10-1
	2. FAILURE MODES	10-6
	3. HARDENING DESCRIPTION	10-11
	a. Prevention of Complement Errors	10-11
	b. Input Filters	10-12
	c. Time Discrimination	10-17
	d. Complete Hardened Design	10-20
	4. ASSESSMENT OF PERFORMANCE	10-23
	a. Analysis	10-23
	b. Simulation	10-32
	5. REFERENCE	10-36
CHAPTER 11	DAMAGE EXAMPLES	11-1
	1. INTRODUCTION	11-1
	2. INERTIAL ELECTRONICS UNIT	11-2
	3. AN/ARC-109 RADIO	11-4
APPENDIX A	HARDENING GUIDELINES EXPERIMENTAL SUPPORT PROGRAM	A-1

LIST OF ILLUSTRATIONS

Figure		Page
1-1	EMP Interference Test Specifications for B-1 Mission Critical Avionics	1-5
1-2	Examples of Anomalous Circuit Response	1-8
1-3	Voltage-Time Factors Influencing the Selection of an Upset Hardening Technique	1-11
2-1	Example Problem in Functional Layout Based on Susceptibility	2-4
2-2	Performance of Example Doppler Radar Configurations	2-8
2-3	Timing Constraint Example	2-10
2-4	Digital Amplitude Discrimination	2-11
3-1	Component Optimization Example	3-3
3-2	Example of Amplifier Saturation	3-6
3-3	Antisaturation Techniques	3-8
3-4	Illustration of SCR dV/dt Sensitivity	3-10
3-5	Illustration of Trapping States in Digital Counters	3-11
3-6	Transient Buffering Examples	3-14
3-7	Upset Hardening Using Combined Filtering and Limiting	3-17
3-8	Upset Hardening Using Combined Filtering and IC Selection	3-19
4-1	Range of Measured Damage Constant for General Diode Classes	4-3
4-2	Range of Measured Damage Constants for General Transistor Classes	4-3
4-3	Damage Threshold for Integrated Circuits	4-5
4-4	Burnout Power of the Input of Various IC's Versus Time	4-6
4-5	Typical Logic Transfer Function	4-8
4-6	Comparison of Logic Family Upset Threshold	4-12
5-1	Combined Zoning	5-4
5-2	Grounding Technique	5-13
6-1	Typical Gas-Filled Spark Gap Characteristic Curve	6-4
6-2	Single Diode V-I Characteristic Curve	6-8
6-3	V-I Characteristics for Opposed Series Diodes	6-8
6-4	Basic Diode Configurations for Terminal Protection Applications	6-9
6-5	V-I Characteristics of Several Nonlinear TPD's	6-11
6-6	TPD Combination Networks	6-13
6-7	Typical Protection Configuration	6-18
6-8	Actuation Voltage Versus Time for Several 4000-Volt Dielectric Breakdown TPD's	6-20
6-9	Actuation Voltage Versus Time for Several 1000-Volt Dielectric Breakdown TPD's	6-20
6-10	Actuation Voltage Versus Time for Eight Different Types of Lower Voltage Dielectric and Semiconductor TPD's	6-21

LIST OF ILLUSTRATIONS (Continued)

Figure		Page
6-11	V-I Characteristic Curves for Some Zener Diodes, TransZorbs and a 1N4003 Rectifier	6-22
6-12	V-I Characteristic Curves for Some MOV's and Dielectric Breakdown TPD's	6-23
7-1	Impedance Added to a Test Circuit by Typical Ferrite Cores	7-7
8-1	Typical Common Mode Rejection of a Twisted Pair Cable Versus Frequency	8-3
9-1	EMP Interference Model for Error Code Evaluation	9-3
9-2	Burst-Error Detecting Code	9-5
9-3	IBM Tape Format	9-8
9-4	Separate Encode/Interleave Operation	9-9
9-5	Interleave Operation	9-11
10-1	Inertial Electronics Unit Block Diagram	10-2
10-2	Logic Diagram X Accelerometer Counter and Register	10-4
10-3a	Portion of X Accelerometer Counter Circuit	10-7
10-3b	Circuit Hardened to Prevent Erroneous 0,0 Data	10-7
10-4	Data and EMP Interference Signals	10-14
10-5	Line Receiver Input Filters	10-16
10-6	Clock Pulse Generator Operation with 25 kHz Reference	10-19
10-7	Synthesizer for 25 kHz for Accelerometer Counter	10-21
10-8	Spectral Response	10-22
10-9	Line Receiver Response to Common Mode Input	10-25
10-10	Line Receiver Input Voltage from EMP with 49-Conductor Cable	10-28
10-11	Line Receiver Input Voltage from EMP with Twisted Pair Cable	10-29
11-1	IEU Hardening Schematics	11-3
11-2	RC Hardening Test Results	11-5
11-3	Zener Hardening Test Results	11-6
11-4	Sense Amplifier Hardening Schematic	11-8
11-5	Transistor Substitution Test Results	11-10
11-6	Current Limiting Test Results	11-12
A-1	Pulse Generators	A-3
A-2	Test Support Equipment	A-6

LIST OF TABLES

Table		Page
4-1	Comparison Chart of the Major IC Digital Logic Families	4-10
6-1	TPD Parameter Matrix	6-2
6-2	TPD Standby Characteristics	6-16
6-3	TPD Protective Efficiency	6-26
6-4	TPD Failure Parameters	6-28
7-1	Filter Comparison Matrix	7-13
8-1	Photon Coupler Failure Thresholds	8-8
10-1	Specifications Related to Accelerometer Counters	10-5
10-2	State Diagram Showing the Possible Influence of Interference on Received Data	10-9
10-3	State Diagram Showing the Possible Influence of Interference on D_1 and D_2 Data with Modified Circuit	10-13
10-4	0,0 Type Upset Example Twisted Pair Case	10-34
10-5	DISIM Analysis, Results for 10 kHz EMP, Twisted Pair Cable Case	10-35
A-1	Test Summary Matrix	A-8

SECTION I

CHAPTER 1

INTRODUCTION

1. BACKGROUND

The phenomenological and coupling aspects of nuclear Electromagnetic Pulse (EMP) generation, propagation, and interaction are described in considerable detail in numerous published sources. For the purposes of this document, it is sufficient to say that EMP can cause large voltage and current transients that result in anomalous responses in electronic systems. These responses are broadly divided into two effects: damage and upset. Damage is a permanent irreversible degradation of component or system functional capabilities. Upset is a nonpermanent anomalous response which also results in the degradation of system functional capabilities.

In general, active components are more susceptible to EMP degradation than passive components and semiconductors are more susceptible than vacuum tube or electromechanical devices. Susceptibility thresholds also tend to vary directly with system operating levels and inversely with the complexity of the system. Modern avionics systems, with their increased reliance on electronic subsystems and a wider use of the newest technologies in semiconductor and integrated circuit design, present a potentially serious susceptibility to EMP degradation.

Electronic design engineers often encounter, and routinely handle, the transients caused by normal switching functions or other electrical phenomena. The EMP induced transients are generally more severe than those routinely encountered. Still, the EMP interference signal can be treated as simply another system design specification.

A number of techniques have been suggested for the reduction of system susceptibility to EMP degradation. In fact, only a very few techniques have actually been applied to reduce the susceptibility of real systems. Thus, the body of available design experience is limited. As a result, designers are compelled to review current system and circuit design practices for their inherent advantages and disadvantages with respect to EMP degradation. This handbook provides a comprehensive review for designers faced with the task of hardening electronic subsystems to EMP.

2. SCOPE

The purpose of this handbook is to compile the state-of-the-art EMP hardening design information in a format of immediate use to electronic designers. This involves three types of information:

(1) Detailed description of the available EMP hardening techniques and a discussion of their implementation.

(2) Presentation of pertinent design data.

(3) Detailed examples of the application of EMP upset and damage hardening to specific circuits.

This report is based on a review of the most current hardening information. As indicated above, there is a lack of practical design experience available for review. Thus, the initial approach was to review the available references and to consult with designers and EMP analysts who have had relevant experience. This effort resulted in the identification of many of the damage and upset hardening techniques but very few practical evaluations, and very little hard data. As a result, an

experimental effort was conducted to obtain the most essential data. The test results are presented in the text. The experimental effort was not exhaustive, and considerable work remains to be done. In addition, much of the hardening technique identification and most of the evaluation was undertaken through analysis of the current system and circuit design practices. It is possible that some of the practical limitations cannot be discovered by this type of analysis. Therefore, it is anticipated that this document will be revised as the available body of EMP design information expands.

In many cases, the hardening techniques are based on standard design techniques. In these cases, no effort is made to present tutorial design information. Instead, the unique considerations related to EMP damage and upset hardening are discussed and the reader is directed to the references at the end of each chapter for normal design application information.

3. OVERVIEW

a. General

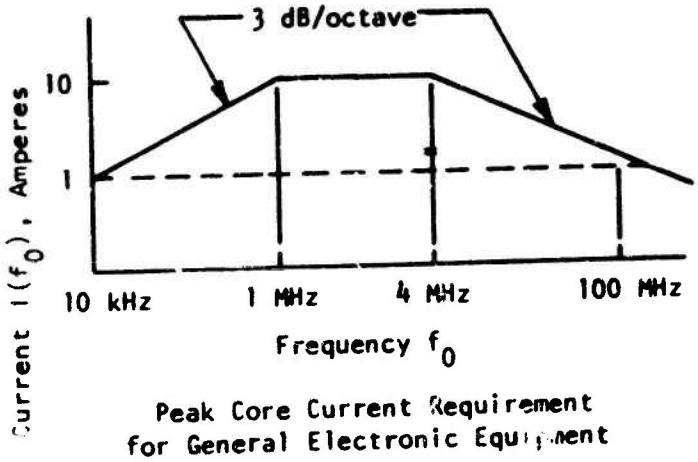
The EMP hardening of subsystems and circuits cannot be pursued independent of other design functions. EMP hardening must be considered as a routine design constraint. This additional design constraint may be conflicting, and the electronic designer's task is to create an optimum design within the defined constraints. For the purposes of this discussion, the constraints can be divided into two categories. The first category includes all non-EMP related constraints. Some of these are: functional requirements, interface levels, reliability, electromagnetic compatibility, lightning, nuclear effects, size, weight, cost, and so on. These will be familiar to most designers, and in addition, are treated in various texts. The second category includes EMP related constraints. These include the system EMP specifications and the subsystem and circuit threshold levels. These subjects are treated in the EMP Susceptibility

Threshold Handbook. Another constraint in the second category which is very real, though not obvious, is the amount of information available to support EMP hardened design. The objective of this handbook is to present the current state-of-the-art EMP hardening design information in a format of immediate use to the electroni design engineer.

It will be obvious to most readers that many of the EMP hardening concepts presented here have a direct impact on other design constraints. Clearly, adding components for EMP hardening increases weight and cost, and generally decreases reliability. Some techniques that improve EMP hardness, actually decrease hardness to other nuclear effects. For example, decreasing gain-bandwidth product for transistors tends to increase EMP hardness but decrease hardness to nuclear radiation. On the other hand, a technique may be beneficial for both EMP hardening and other constraints. For example, adding suppression devices will generally help to meet lightning and electromagnetic compatibility constraints. These examples are not exhaustive and the designer should carefully examine the overall impact of any hardening technique before adopting it.

b. Damage

Damage has been defined as an irreversible degradation of component functional capabilities. In theory, any electronic component is potentially susceptible to EMP caused damage. In fact, some component types are inherently hard to the levels of EMP transients likely to be experienced in aeronautical systems. Figure 1-1 shows the frequency distribution of peak currents for shielded electronic subsystems as defined in the B-1 EMP specifications. The maximum current is 10 amps and the frequency distribution is related to the physical dimensions of the aircraft. For other aeronautical systems employing different hardening philosophies, the maximum currents might be one or two orders of magnitude higher. The maximum voltages are limited to about 10 kV by the insulation



Peak Core Current Requirement
for General Electronic Equipment

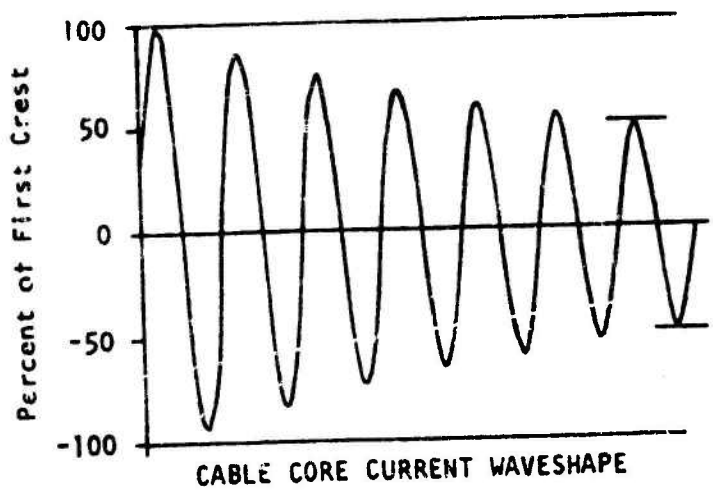


Figure I-1. EMP Interference Test Specifications for B-1 Mission Critical Avionics

breakdown of cables and connectors. Thus, the range of EMP signals that must be considered for EMP hardening is from 1 to 1000 amps with a maximum voltage of perhaps 10 kV, and with durations less than 100 μs. Some rare circuits connected to efficient antennas may experience higher levels, but this range can be considered an extreme worst case for the vast majority.

Given these levels, it can be deduced that in most cases, components such as relays, transformers, tubes, and high power passive components are not susceptible to EMP induced damage. Discrete semiconductors, integrated circuits, and low power passive components are potentially susceptible. The understanding of the damage phenomena in these components is incomplete. However, at present most damage modes are believed to be thermal dependent. The EMP signal heats the component or a localized area (such as a semiconductor junction) until it produces melting or vaporization. This process continues until the component's functional characteristics are permanently altered. In some severe cases, the component may be destroyed completely.

The hardening techniques fall into two groups: (1) use harder components, and (2) limit the energy supplied to the components. The first alternative is attractive but not always feasible. A number of techniques are available for the second alternative. The remaining chapters of this handbook include a detailed treatment of damage hardening techniques.

c. Upset

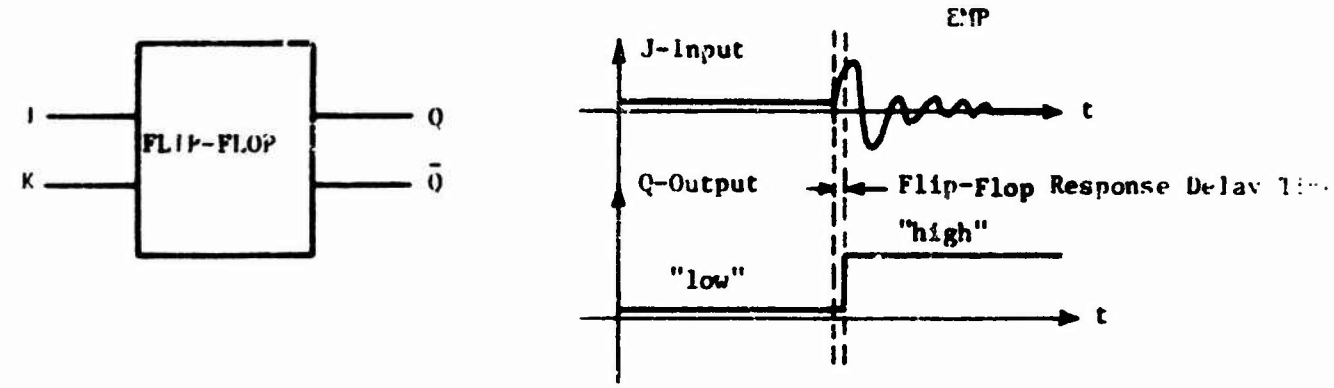
Upset was previously defined as a nonpermanent anomalous response which results in the degradation of system functional capabilities. Thus, an EMP event may cause a variety of transient responses in various subsystems and circuits, but unless a degradation of system capability

results, there is no upset. Given this definition, it can be seen that an individual upset is not uniquely defined. Whether or not an EMP-induced signal produces an upset depends on both electrical parameters such as amplitude and duration, and operational parameters such as circuit or subsystem criticality and mission description.

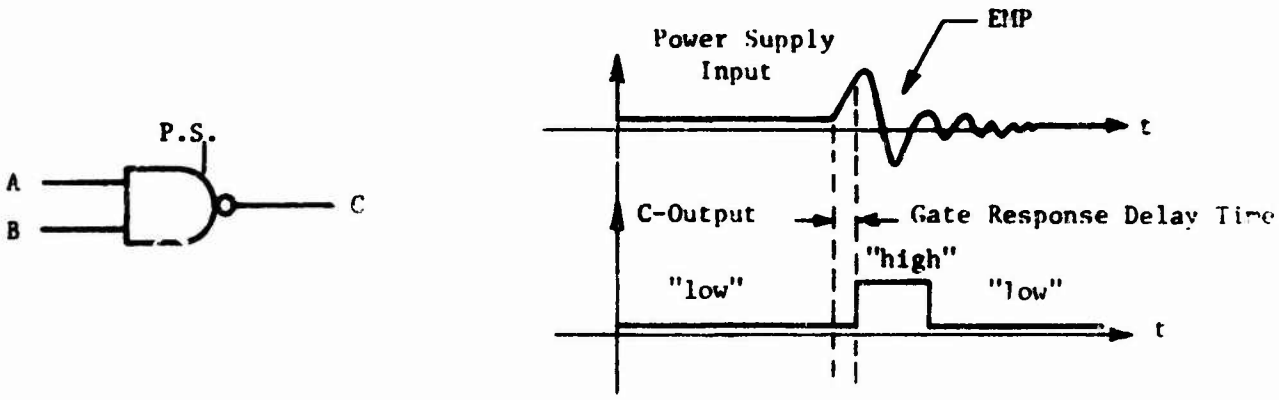
From the above discussion, it may be surmised that the definition of upset is concise and technically correct, but perhaps not particularly helpful in gaining an understanding of upset phenomena. This is a consistent problem in discussing upset. Any attempt to provide general guidelines requires so many qualifications that the complexity precludes understanding. Alternatively, understanding may be gained by studying examples rather than principles.

(1) Upset Mechanisms

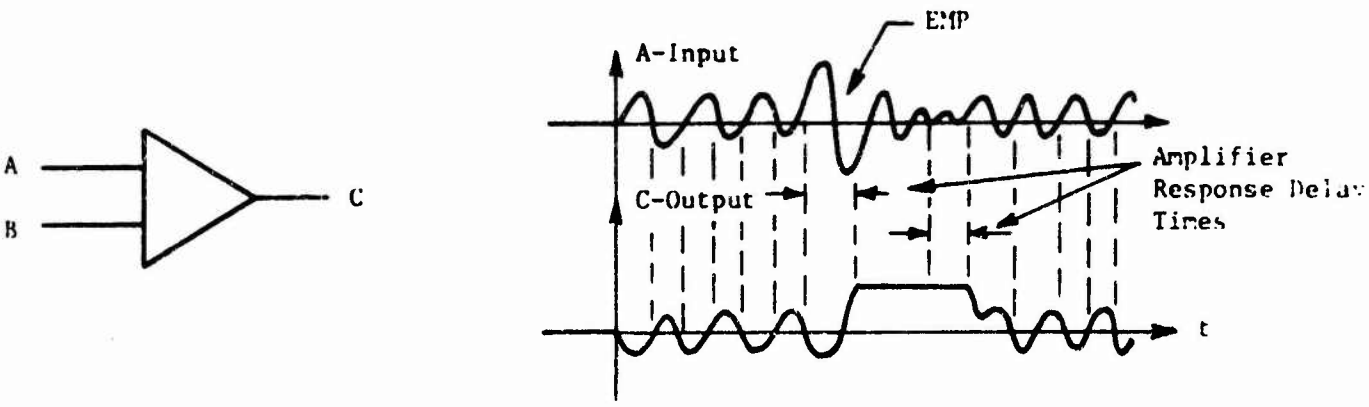
System upset can result from either the generation of erroneous data or the loss of valid data. In general, upset may result from the anomalous response of either analog or digital circuitry. However, in many cases the determination of whether an anomalous response actually constitutes an upset will depend on its timing relative to other system parameters (e.g., Is a clock pulse present? Are the data critical during this portion of the mission?). In these cases, the probability of upset increases with the duration of the anomalous response. Thus, the probability of upset increases as a circuit's ability to "remember" transients increases. Digital circuitry inherently provides a greater memory capability than analog circuitry. Thus, digital circuitry receives more emphasis in discussions of upset. However, in certain cases, especially if latch-up or saturation occurs, analog circuits can exhibit a memory of considerable duration. At any rate, it should be recalled that memory is not always necessary to produce upset, it merely increases the probability. Figure 1-2 presents three examples of anomalous circuit



(a) Flip-Flop Upset



(b) NAND Gate Upset



(c) Amplifier Upset

Figure 1-2. Examples of Anomalous Circuit Response

responses that could produce upset, given an appropriate operational situation. These examples are provided to gain a practical insight into upset mechanisms.

Figure 1-2a illustrates a flip-flop circuit which changes state due to an EMP transient on a trigger input. This is perhaps the classical upset example. Erroneous data have been generated. Unless the flip-flop is reset, it will remain in the changed state permanently. If the data which the flip-flop state represents are critical, the system functional capability will be degraded and upset will have occurred. On the other hand, if the flip-flop is reset before the data are needed (i.e., become critical), the system will not be degraded and upset has not occurred.

Figure 1-2b shows a NAND gate changing its output logic level temporarily due to an EMP transient on the power supply input. If the system is configured to recognize this temporary logic shift as data, then upset may occur. If the system does not recognize the logic shift as data (e.g., if the system responds too slowly), then upset does not occur.

Figure 1-2c shows an amplifier being driven into saturation by an EMP transient superimposed on its signal input. Here, the data channel is interrupted and all valid data are lost as long as the amplifier remains in saturation. If critical data are lost, then the system capability is degraded and upset has occurred. If no data were present, or if the outage time was insufficient to destroy any data, or if the data were not critical; then no degradation, and thus no upset has occurred.

It should be noted that although these examples each postulate the appearance of transient at a specific input, the transients may appear at any combination of terminals. In some cases this "multiport" excitation may result in a lower upset threshold than that obtained for excitation of a single port.

In reviewing these simple examples, the experienced designer will no doubt have conceived a number of circuit or system level hardening techniques. This provides an insight into a significant fact concerning upset hardening. That is, the basis for upset hardening is careful design at both the system and circuit levels using available techniques. This document provides guidelines for selecting the hardening technique that best fits a particular upset problem.

(2) Hardening Factors

This discussion assumes that the EMP threat is defined for the system, subsystem, or circuit of interest in terms of voltage or current waveshapes at the interface level. The system operational parameters are also presumed to be defined, so that the designer can use the relationships between these parameters and the EMP signal to determine the requirement for upset hardening techniques. The technique selected may be required to provide either absolute or relative hardening. An absolute hardening technique completely eliminates the possibility of upset. A relative hardening technique reduces either the probability or the severity of upset. A particular technique may be capable of providing either absolute or relative hardening depending on the operational and EMP parameters involved. In the worst case, absolute EMP hardening of data links can only be provided by nonconducting circuitry. In most practical cases however, one or a combination of the other techniques can achieve satisfactory hardening.

Some of the factors that influence the selection of an upset hardening technique can be illustrated with the aid of Figure 1-3. This figure presents a simplified depiction of the signal line input voltage versus time, associated with various circuit responses. (Of course, the actual voltage-time dependence may be more complicated, but this depiction serves the purpose.) Due to the presence of external damage hardening devices, the maximum signal amplitude that the circuit can experience is

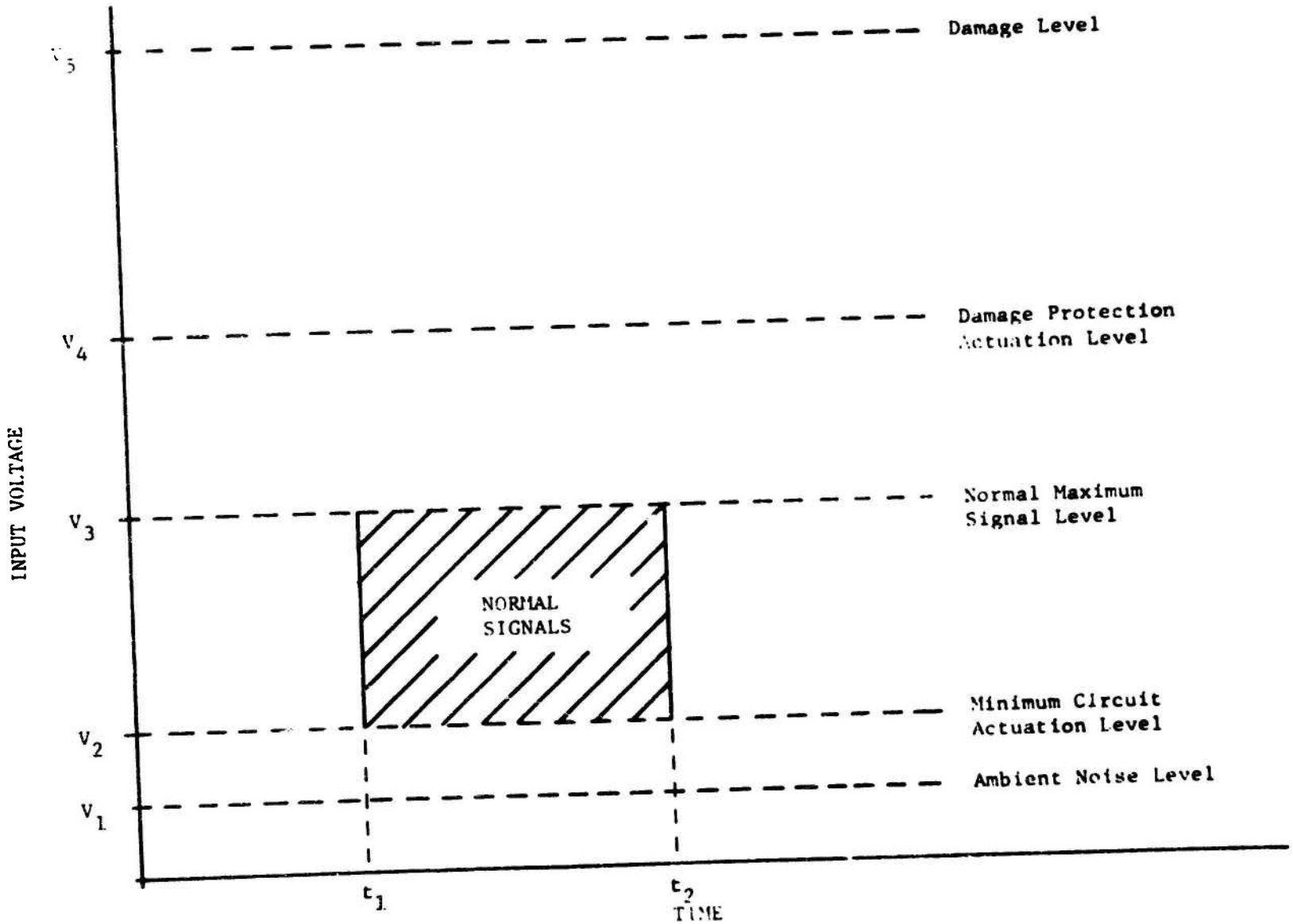


Figure 1-3. Voltage-Time Factors Influencing the Selection of an Upset Hardening Technique

V_4. Signals below V_2 are of no concern because the circuit cannot respond to them. The cross-hatched area represents the amplitude range and the duration range of normal valid data.

The designer now reviews the EMP interface specification as applied to this circuit. If the resultant EMP signal is below V_2, then no hardening is required. If the EMP signal is greater then V_2 but the duration of a single cycle is much less than that of a normal signal, then some type of low pass filtering may be used. If the risetime of the EMP signal is greater than the duration of the normal signal, then high pass filtering is in order. If the EMP signal occurs within the duration of the normal signal and the amplitude is significantly less than V_4, the operating levels may be increased to raise V_2 above the EMP signal. The limitation here is that V_3 must remain less than V_4 unless the damage protection is to be redesigned. An alternative may be to install a balanced line interface which may provide sufficient improvement in shielding to reduce the EMP signal below V_2.

If none of these techniques are feasible and the EMP signal falls in the normal signal range, a second approach is to operate on the data signal itself. One alternative is carrier modulation to move the data signal so that high pass filtering may be employed. Another alternative would be a time discrimination technique which would increase the duration of the data signal so that low pass filtering could be employed. A third general approach is to detect the presence of the EMP signal through the use of error codes. The incorrect data could then be either corrected or rejected.

While this example does not cover all of the possible hardening techniques that could be applied to the circuit, it does indicate the general approach. It should be noted that the second and third approaches involve more complexity than the first. However, their effectiveness is

independent of the amplitude of the EMP signal. Thus, these types of techniques may be preferred where more uncertainty exists in the EMP specification, although even these techniques require some knowledge of the EMP signal duration.

4. SUMMARY

The remainder of this handbook is divided into three sections and 10 chapters. The section divisions are based on the application of the hardening information presented. The chapter divisions are based on subject matter.

The sections are:

- II - DESIGN PRACTICES
- III - HARDENING TECHNIQUES
- IV - HARDENING EXAMPLES

Section II, DESIGN PRACTICES, discusses the specific EMP considerations related to four phases of design common to all subsystems, namely system design, circuit design, component selection and packaging. This section treats good design practices that should be reviewed in the design of any subsystem for which an EMP threat may exist, independent of whether or not a specific vulnerability has been defined. Specific design practices may, however, optimize either upset or damage hardening.

Section III, HARDENING TECHNIQUES, presents techniques that can be employed to hardened specific circuits. This presumes that the requirement for EMP hardening has been otherwise established. The hardening techniques presented include suppression, filtering, decoupling, and error

detection. Error detection can be used only for upset hardening. Filtering and decoupling can be used for both upset and damage hardening. Suppression is most applicable to damage hardening, although in some cases it is quite attractive for upset hardening.

Section IV, HARDENING EXAMPLES, presents detailed examples of the application of upset and damage hardening to specific circuits. The upset hardening example is analyzed theoretically, while the damage hardening analysis is primarily empirical.

SECTION II

DESIGN PRACTICES

Chapters 2 through 5 cover design practices and considerations that play a part in the design of electronic equipment whether EMP requirements are imposed or not. As a rule, these considerations are required in the course of designing electronic equipment to handle normal noise, cross talk, and power surge considerations. The impact of EMP specifications is to cause the designer to view these considerations from an additional point of view. In many cases, EMP specifications create more severe problems than those which exist otherwise and force these considerations to be much more carefully analyzed.

The various design considerations discussed in this section are grouped according to the design phase in which they would normally occur. Thus, considerations that must be addressed during the system design phase are discussed in Chapter 2. Considerations that must be addressed during the design of individual circuits are discussed in Chapter 3. Considerations that relate directly to the selection of components are addressed in Chapter 4, and finally, considerations that relate to the design of the electronic packaging and system mechanical configuration are addressed in Chapter 5.

CHAPTER 2

SYSTEM DESIGN

1. INTRODUCTION

EMP upset in electronic systems results from a combination of two occurrences. First, for upset to occur, EMP induced interference must create erroneous signals or responses at some point within the system. Second, for EMP upset to occur, the induced signal errors or erroneous response must cause the system to perform outside its specifications or to fail to accomplish its mission.

Two approaches to the problem of reducing the impact of EMP induced interference and errors on system performance are discussed in this chapter. These techniques are referred to as error criticality reduction and parameter constraint analysis. In both cases, the techniques address the problem of creating a system that will meet its performance specifications and mission goals in spite of interference. These techniques do not address the problem of preventing interference like techniques such as shielding and high noise immunity interface designs. Also, the techniques do not have any application with regard to the question of damage hardening.

Possible applications of error criticality reduction and parameter constraints should always be examined carefully. These techniques can often do more to prevent serious upset than all of the techniques in Section III combined since they tend to produce a system which refuses to behave in an unreasonable manner.

2. ERROR CRITICALITY REDUCTION

One approach to hardening is to address the problem of error criticality. As a general rule, certain portions of the system are more susceptible to errors resulting from EMP or other interference. If good packaging techniques have been employed, this will be interconnection cabling and interface circuits within a given electronics unit. Often the form of data at the interface of a particular electronic unit can be changed to modify the criticality of the signals that are susceptible to EMP induced errors. Thus, the errors themselves are not prevented but the significance of such errors on the system operation is reduced.

When interface points within a system are selected, an examination of the consequences of errors introduced at the interfaces should be carried out. When it is determined that errors introduced into a particular interface signal will seriously impair the operation of the system, the designer should examine the functional block diagram of the system in an attempt to eliminate the problem. Shifting the interface point so that functional elements are reassigned within the subsystems will produce new interface signals and remove the previous signals from the interface area. Examination of the new interface signals may show that interference does not lead to as much degradation in system performance. In general, errors in data in a form completely replaced by subsequent data sets are less likely to cause severe upset in the system operation than errors in data which represent incremental updates of a parameter and are, therefore, never totally replaced by subsequent data sets. In addition, when interfaces can be chosen so that separate data items are not completely independent, it may be possible to detect errors by comparison of different data items. When a system has redundant data available within it, it is often advantageous to choose interfaces at points where it is most convenient to make use of the redundancy as a check on errors in the signals themselves.

Figure 2-1 illustrates the basic concept of reducing the criticality of errors within a system. The example consists of a doppler radar, ground speed measuring system with a remote solid state display to indicate distance traveled. Two basic operational formats are specified in Figure 2-1.

In Format 1, pulses are generated within the doppler radar system to indicate every one-tenth of a mile traveled. These pulses are transferred over the data line to the solid state display unit. At this point, they are used to update an accumulator which provides a running indication of the total distance traveled. In this example, it is assumed that the data line is the point at which EMP errors are most likely to occur within the system. With this format, EMP induced errors in the data line signal will cause an error in the total distance accumulator. Depending on the nature of the interference, this may cause a total distance indication which is larger or smaller than the actual value. This error will stay in the system and the displayed value, until such time as the total distance value is corrected by some independent means. Thus, EMP induced errors cause permanent upset in this system.

In Format 2, the accumulator which keeps track of the total distance traveled is placed in the doppler radar unit instead of the display unit. The accumulator contents are then serialized and transferred over the data line to a storage register in the display unit. Since it is assumed that the EMP induced errors will occur in the data line, the accumulator value will not be upset by EMP with this format. The value stored in the register within the display unit will be incorrect following EMP induced errors in the data line signal. This situation will last only until the next transfer of the contents of the accumulator in the doppler radar to the register in the display unit. At this time, the error in the display unit will be corrected. Thus, with this format, the upset is of a very temporary nature. If the amount of time between message transfers is small enough, it is possible that this type of short term response will have no impact on operations, and then no upset will occur.

FORMAT 1. THE DOPPLER RADAR GENERATES ONE PULSE FOR EVERY 0.1 MILE TRAVELED. THESE PULSES ARE TRANSFERRED OVER THE DATA LINE TO AN ACCUMULATOR IN THE DISPLAY UNIT WHICH UPDATES A TOTAL DISTANCE COUNT.

FORMAT 2. THE TOTAL DISTANCE ACCUMULATOR IS IN THE DOPPLER RADAR UNIT. THE ACCUMULATOR CONTENTS ARE TRANSFERRED IN SERIAL FORMAT TO A REGISTER IN THE SOLID STATE DISPLAY.

Figure 2-1. Example Problem in Functional Layout Based on Susceptibility

This illustrates the basic technique of choosing interface points and data formats to reduce or eliminate the criticality of EMP induced errors without actually eliminating the errors themselves. It is obvious that this entails other compromises in the design of the equipment. At least one additional register is required in the overall system, as well as additional circuitry for interfacing the signal to a serial format for the data line. In addition, to accomplish updating of the distance display as frequently with Format 2 as is accomplished with Format 1, it is necessary to increase the bit rate on the data line and thus, perhaps increase the severity of EMP induced errors. Nevertheless, the careful selection of data formats and interface points within a system can often reduce the criticality of errors to the point where other compromises required to accomplish this are more than justified.

Another common technique for reducing the duration of upset resulting from EMP interference in digital systems is the use of a master reset or synchronization signal. Many digital systems require synchronized sequencing of events at several points within a system. If the sequencing operations are synchronized only at the beginning of operation, it is possible for interference to upset the synchronization between various sections, thus causing permanent error. A synchronization pulse derived from one of the sequencing operations at some convenient time in the cycle can be used to periodically reset all other sequence operations in the system. As long as all sequencing operations stay synchronized, the master synchronization pulse has no effect on the system's operation. However, if interference causes a loss of synchronization between various sections of the system, the master synchronization pulse will resynchronize all portions of the system the next time it occurs. Thus, the error becomes temporary rather than permanent, and system upset may not occur.

3. PARAMETER CONSTRAINT ANALYSIS

In many systems, it is possible to provide some measure of upset protection by designing equipment to take full benefit of all available information. Signals within a system can generally be related to some parameter which has limitations on its possible behavior. Signals representing the position of an aircraft, a servo motor, or any physical object with a given mass subjected to known types of forces, will have definite limits in the possible acceleration and sometimes in velocity as well. Very large, sudden shifts in the values of such signals can readily be identified as errors because the physical parameter represented cannot change value that rapidly. Signals which represent the status of a system are obviously constrained by the same constraints that apply to the system itself. If a system can go into only some of the available states from a given starting point (only certain sequences are possible), then any change in status indication which does not represent a possible change in the system status can be readily detected as an error. Substantial improvement in the performance of an electronic system can often be realized by designing the system so that it cannot respond to changes in signals which are not realistic. This involves adding circuitry to the interface to bound the interface parameter values. Maximum and minimum values of given parameters can be simulated by limiters. The maximum rate of change in the parameter which the signals represent can be simulated by slewing limits in servos or rate limits in digital equipment. Restrictions on sequences of events or status signals can be incorporated through the use of interlocking logic.

By simulating parameter constraints, it is possible to design a system which simply refuses to respond in an unrealistic manner when signal errors occur. These constraints can often be introduced into the design of equipment with very little cost or complexity. One test to determine whether or not opportunities exist to incorporate such constraints, is to examine the possible data signals which the interference might generate. Then ask the simple question, could a trained observer examining this signal

determine that an error occurred because the data are impossible for the real parameters represented? If it is possible for an observer to detect and reject errors from the data, based on his knowledge of the system and what it represents, then it is also possible to design the equipment to do the same thing. The only question that remains at that point is whether or not the complexity of the equipment required is justified.

Referring to the doppler radar example in Figure 2-1, it can be seen that although Format 2 will reduce the criticality of errors within the system by limiting their influence to a very short period of time, it is still possible to correct many errors which may occur by applying all the information available on the system. Specifically, there are two facts related to this system which could be used in the equipment to detect and correct errors. It is known that the aircraft always accumulates distance. The total distance indication cannot realistically be reduced. In addition, the maximum speed of the aircraft is a known parameter constraint and can be used to eliminate erroneous data that would indicate too rapid a change in total accumulated distance. With Format 2, EMP induced interference is reasonably likely to cause errors in high order digits indicating changes of tens or hundreds of miles between two data sets on the data line. Since this is an impossible rate of travel for the aircraft, the error can be detected and, in many cases, corrected. Logic can be added to the register in the display unit which allows the higher order bits to change only to the next state in sequence. Any data from the data line indicating a value for a high order digit other than the next value in sequence, would be rejected and the previous value in the register would be retained. This technique does not correct all errors, but it does correct many of the EMP induced errors. The improvement in performance resulting from the interface change (Format 2) and the parameter constraint for the doppler radar example is illustrated in Figure 2-2.

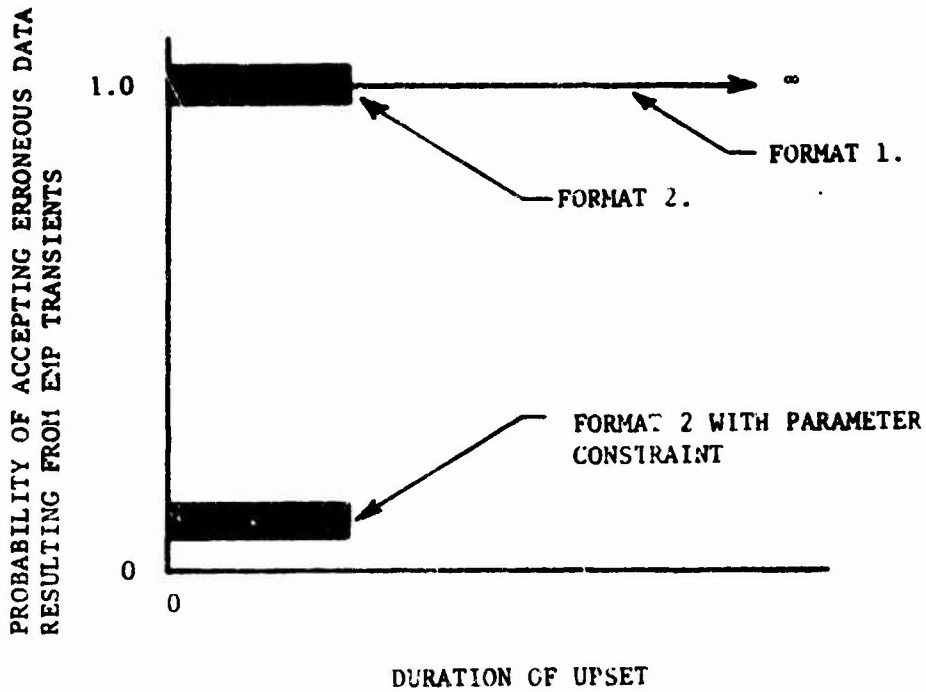
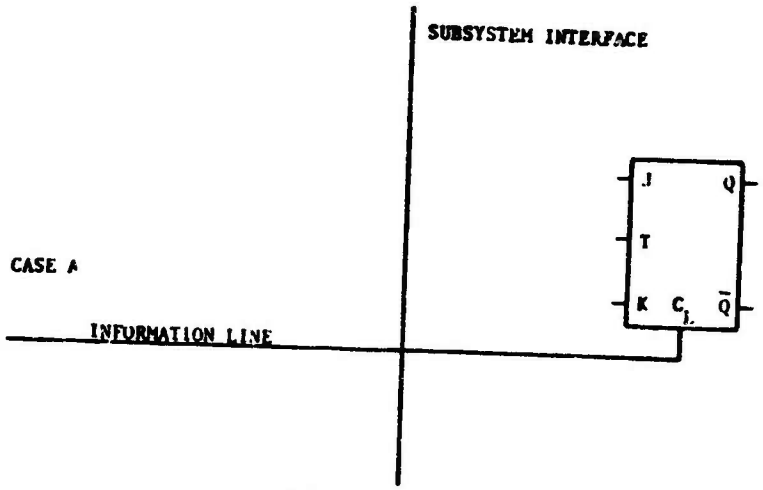


Figure 2-2. Performance of Example Doppler Radar Configurations

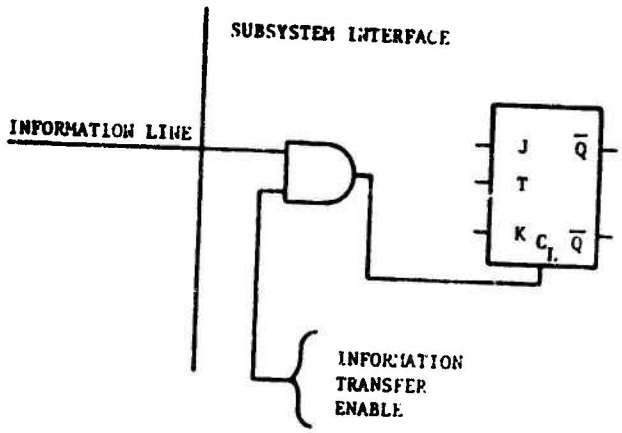
Another type of parameter constraint that can often be useful in reducing the probability of system upset is the timing constraints on data received at a given interface. These timing constraints are imposed by the format of the data transmission source. The parameter constraints that can be used in this case are the duration and synchronization parameters on transmitted data, along with the typical duration of EMP induced transients. In synchronized systems, the fact that EMP induced transients occur at random times in the operation of the system while data transfers do not, can be utilized to reduce the probability of upset.

An example of a situation without the application of parameter constraints is illustrated in Figure 2-3a. Any transient on the information line can clear the flip-flop, if of sufficient amplitude and duration.

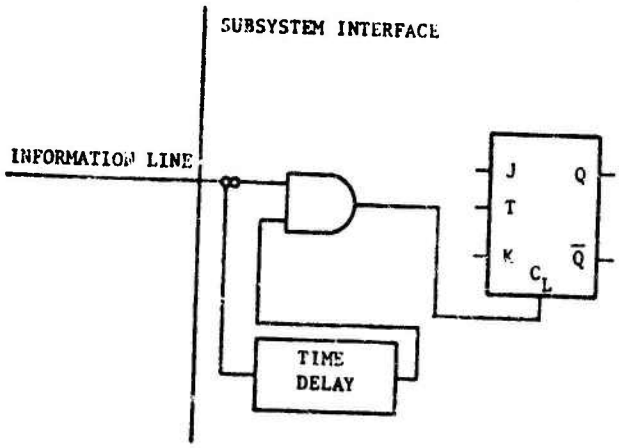
Some reduction in the probability of system upset can be obtained by designing the logic such that information signals normally required to change memory circuit states are gated to occur only at times when such information transfers may take place. The implementation of such a technique is shown in Figure 2-3b. In this case, the information signal is gated by an information transfer enable signal obtained from within the receiving subsystem. This technique is applicable to systems where information transfer is done synchronously.



(a) Unhardened Input



(b) Information Transfer Enable Gating



(c) Fixed Time Duration Gating

Figure 2-3. Timing Constraint Example

Another possibility is to require the information signal to be present for a selected length of time before any logic circuit signal processing can occur. Such a technique is implemented in Figure 2-3c by passing the signal and a delayed version of it through an AND gate before clearing the flip-flop. This technique can be applied to both asynchronous and synchronous data transfer.

A final example of parameter constraint is the use of digital gating functions in conjunction with an amplitude comparator to preclude data transmission when signal amplitudes exceed a predetermined maximum. Such a scheme is illustrated in Figure 2-4. Input signals greater than a preset threshold, which should be slightly larger than the maximum positive 1 voltage level, cause the threshold detector to respond and inhibit the coincidence gate from passing on the false information.

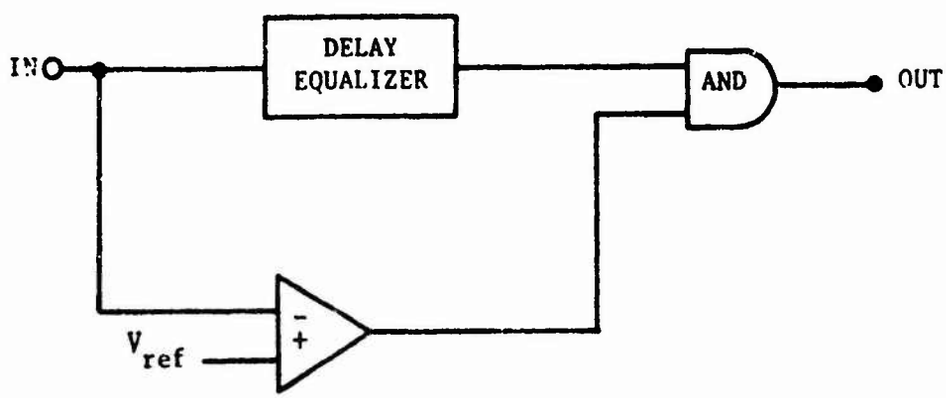


Figure 2-4. Digital Amplitude Discrimination

Basically, the parameter constraint technique depends on a thorough analysis of all parameter constraint information related to the system. This includes an analysis to determine redundant data within the system as well as the value and possible application of information related to the parameters of the system operation, such as the maximum speed of the aircraft in the first example.

CHAPTER 3

HARDENED CIRCUIT DESIGN

1. INTRODUCTION

Circuit design for EMP hardening refers to the reduction of a given circuit's damage or upset susceptibility by one or more of the following techniques:

(1) Optimization of component parameter values to minimize susceptibility.

(2) Internal circuit modifications to minimize susceptibility.

(3) Transient isolation, (i.e., the addition of components or circuits between transient injection points and sensitive circuits).

These techniques are discussed in detail in the remainder of this chapter.

2. COMPONENT PARAMETER OPTIMIZATION

Optimizing component values to reduce circuit damage susceptibility can be an integral part of the circuit design process for new systems. The usefulness of this technique arises from the fact that many of the components included in the functional design of a circuit can tolerate considerable flexibility in specifying component values without affecting circuit performance. For example, assuming compatibility with other circuit design requirements, maximizing the value of series resistors or

shunt capacitors at all interface points (i.e., input, output, and supply) can enhance hardening.

A simple example of circuit hardening by component optimization is shown in Figure 3-1. Figure 3-1a is the schematic of an amplifier circuit whose base resistance (R_B) is to be optimized for maximum protection of the transistor Q_1 base emitter junction. Figure 3-1b shows the effect of varying R_B on the circuit voltage gain and on the damage threshold voltage. It can be seen that substantial improvement in the susceptibility level can be obtained at essentially no loss of gain. This design takes advantage of the fact that the input resistance seen at node A is much smaller when the base-emitter junction is in the breakdown mode (near damage) than it is under small signal conditions. Stated quantitatively,

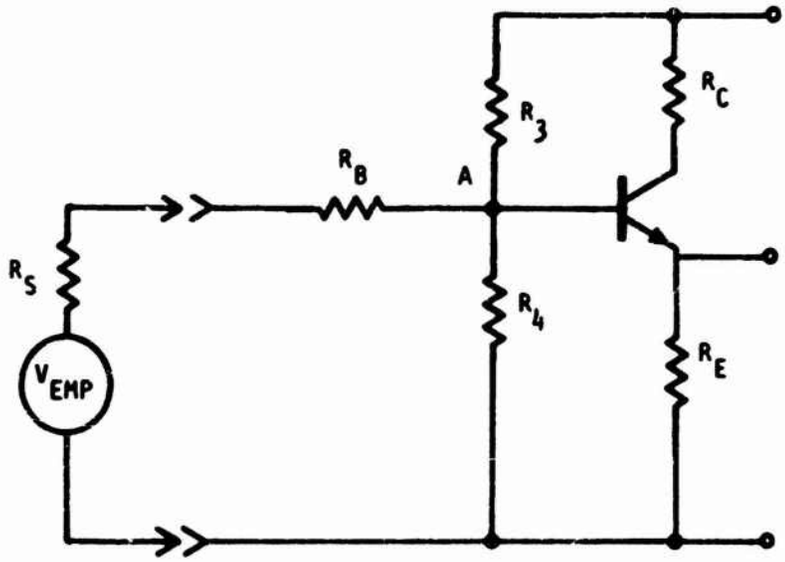
$$R_1 >> R_2$$

where R_1 is the small signal input resistance and R_2 is the breakdown mode input resistance. Assuming breakdown of both the base-emitter and base-collector junctions during the failure transient,

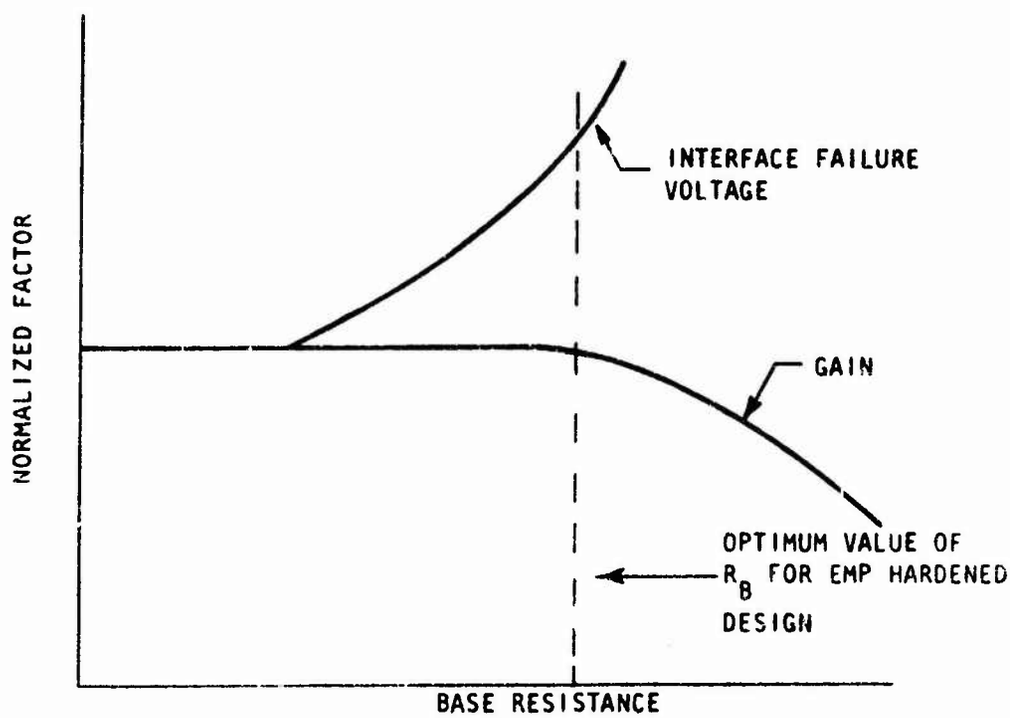
$$R_3 \,||\, R_4 \,||\, (1 + \beta)\, R_E >> R_3 \,||\, R_4 \,||\, R_E \,||\, R_C$$

This result has been demonstrated experimentally, and considerable hardening can be achieved with a minor circuit change. Other circuit constraints that may impose limitations on this technique should also be considered.

It should be noted that this use of increased current limiting as a means of hardening must also take into account the damage threshold of the resistor selected. Some types of precision, low power resistors may be more susceptible to transient damage than the semiconductor being protected.



(a) AMPLIFIER SCHEMATIC



(b) OPTIMIZATION OF BASE RESISTANCE

Figure 3-1. Component Optimization Example

Component or parameter optimization is not limited to passive components but can also be applied to the selection of diodes, transistors, and integrated circuits. To reduce device damage and upset susceptibility, the following parametric optimizing should also be considered:

MAXIMIZE	MINIMIZE
Power Rating	Gain Bandwidth Product
Current Ratings	
Propagation Delay	
Noise Immunity	

Selection of the least susceptible device from a group of functionally similar devices may give a significant increase in EMP hardness in some cases. The discrete hardening example given in Chapter 11 illustrates this approach. For hardening by component selection to be useful, either a device transient response model or data base must be available to allow a comparison of the burnout thresholds of candidate components. A discussion of available models and data is in Chapter 4.

3. ANOMALOUS STATES

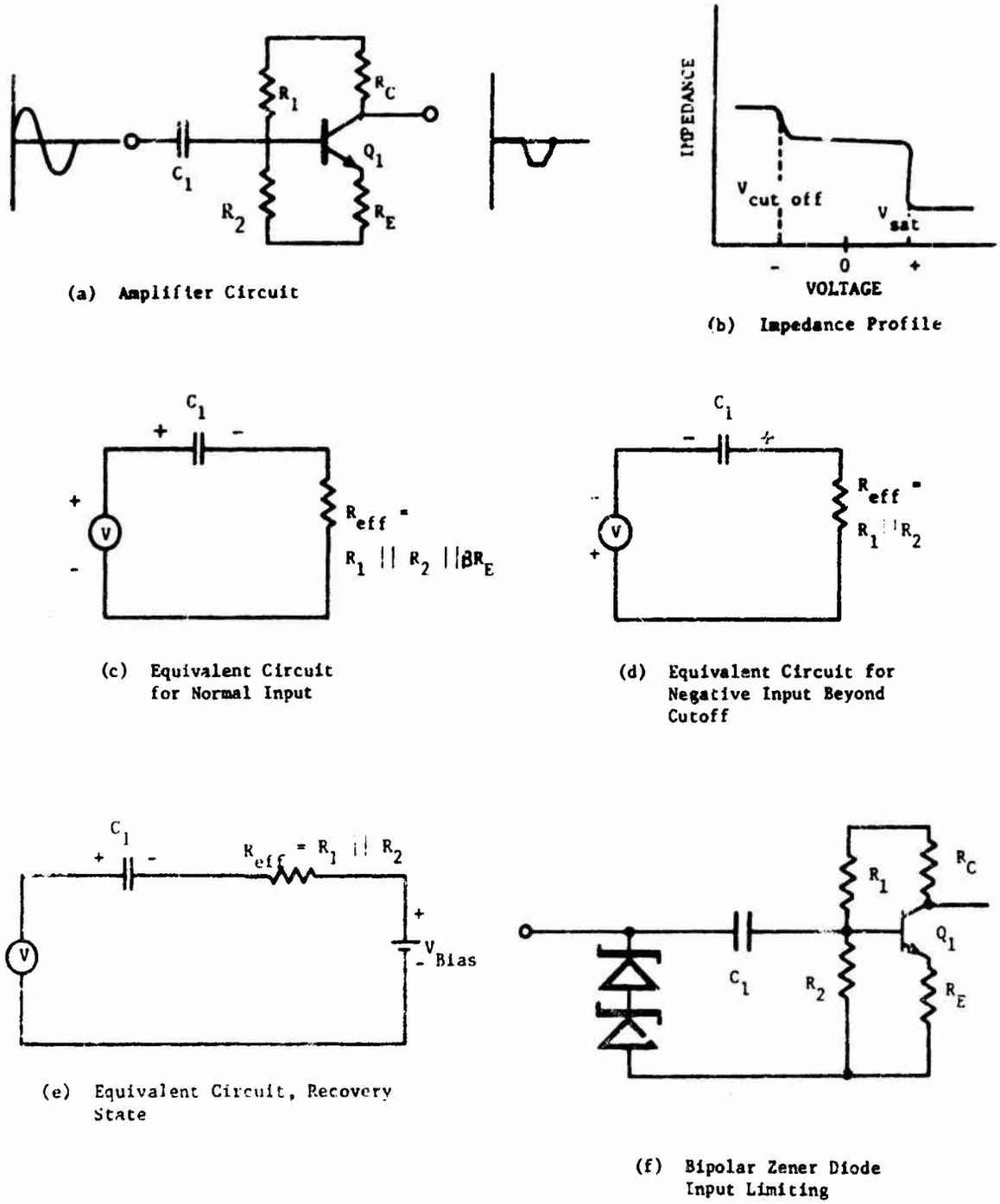
Circuits driven beyond their normal operating range may exhibit extended periods of functional interruption or outage which results in lost or degraded data. Abnormal circuit response may be generally categorized as either unstable states or stable states. Unstable abnormal responses are characterized by an eventual recovery back to a designed operating state. Stable abnormal responses result in a permanent, but correctable, transfer to an abnormal state. These two abnormal responses are discussed in detail in the following paragraphs.

a. Unstable Responses

For the general case of saturation of linear circuits, outage time for the circuit with and without limiting, or other hardening, must be assessed to achieve minimum functional interrupt. Data required for such an analysis include a detailed definition of the EMP interference and of the circuit configuration. Since outage time is a function of transient frequency spectrum, high pass filtering prior to limiting may be necessary to minimize low frequency levels before the limiting operation.

An example of saturation is illustrated in Figure 3-2. The circuit considered is a capacitively coupled common-emitter amplifier. Normal input signals do not drive the amplifier outside of its linear operating range. However, very large signals such as those that might be induced by EMP interference can cause saturation of the amplifier which results in a substantial reduction in the input impedance of the amplifier during the period of saturation. Thus, very large positive input voltages will see a very low input impedance because of saturation, whereas, very large negative input voltages will see a high input impedance because of reverse bias of the base-emitter junction. It is assumed that the negative input voltage does not exceed the emitter-base breakdown rating. The input impedance profile of the overdriven amplifier is shown in Figure 3-2b.

Since the impedance for positive inputs is less than the impedance for negative inputs, more charge will accumulate on the capacitor for the positive half cycle. The capacitor will charge to a dc or average potential much more negative than the normal bias point when subjected to a series of very large positive and negative excursions. Normal circuit operation cannot be resumed until the capacitor, which has been negatively charged with respect to the circuit, as illustrated in Figure 3-2e, dumps its negative charge and charges back up to the



(a) Amplifier Circuit

(b) Impedance Profile

(c) Equivalent Circuit for Normal Input

(d) Equivalent Circuit for Negative Input Beyond Cutoff

(e) Equivalent Circuit, Recovery State

(f) Bipolar Zener Diode Input Limiting

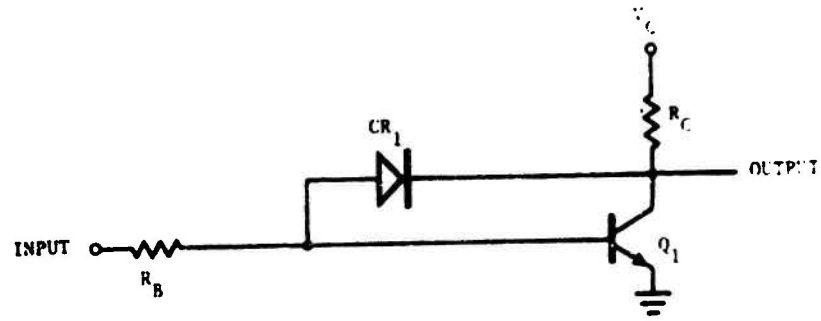
Figure 3-2. Example of Amplifier Saturation

positive bias potential on the base of Q_1. The length of time for this to occur is determined by the time constant $(R_1||R_2)C_1$. This phenomenon can be eliminated if the transistor circuitry is not permitted to exhibit asymmetrical input impedance by being driven into saturation. A hardening technique here would be to limit the input voltage by means of a bipolar clamp as shown in Figure 3-2f. In this case the critical analysis requirement is to examine the circuit state diagram which results from input signals outside the normal operating range and to evaluate circuit recovery characteristics.

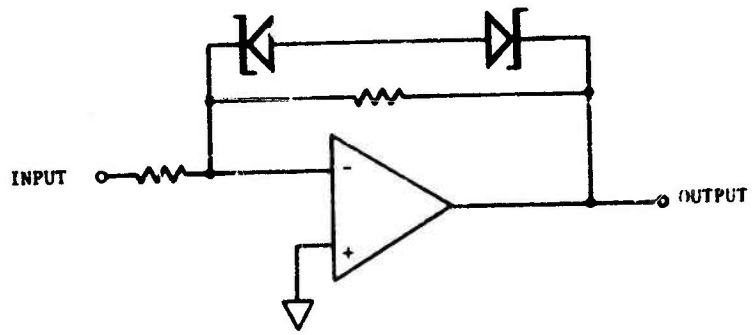
Antisaturation design techniques for analog and digital interface circuits are generally well understood and numerous examples are discussed in References (1) and (2). Figure 3-3 shows several diode techniques used to minimize transistor and operational amplifier saturation problems. Figure 3-3a illustrates a collector-base clamp. This can be achieved for silicon transistors by using a germanium or Schottky barrier diode whose saturation voltage is less than the collector-base saturation voltage. This is the technique used to prevent minority carrier storage delays in Schottky TTL digital integrated logic.

Gain limiting may be applied to operational amplifier circuitry as illustrated in Figure 3-3b. The two Zeners limit the feedback and output voltage in this case. The input or output voltage may also be clamped as illustrated in Figures 3-3c and 3-3d.

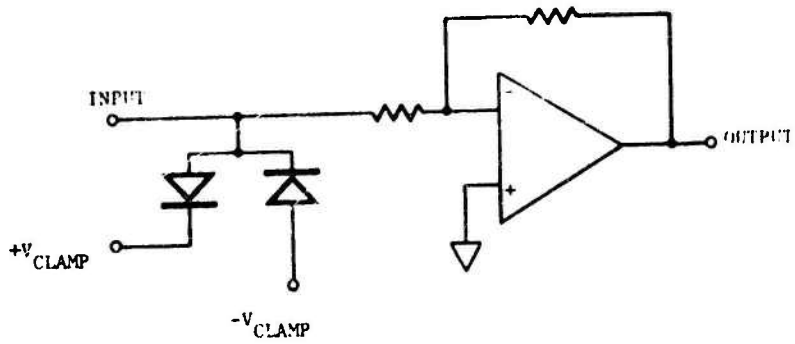
Automatic Gain Control (AGC) is another saturation prevention technique that may be considered to minimize outage time. This technique can be implemented in many ways but consists essentially of varying the gain of an amplifier stage in inverse proportion to the input signal amplitude. The technique, well known and documented in the communication field (Reference (3)), has only limited applicability for EMP hardening and so will not be further discussed in this report.



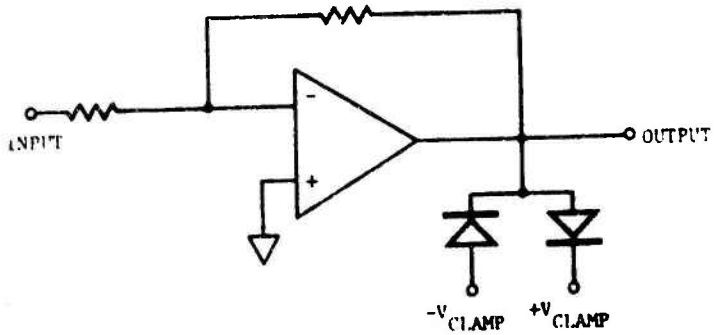
(a) Collector-Base Clamp



(b) Inverting Op-Amp Gain Limiting



(c) Op-Amp Input Clamping



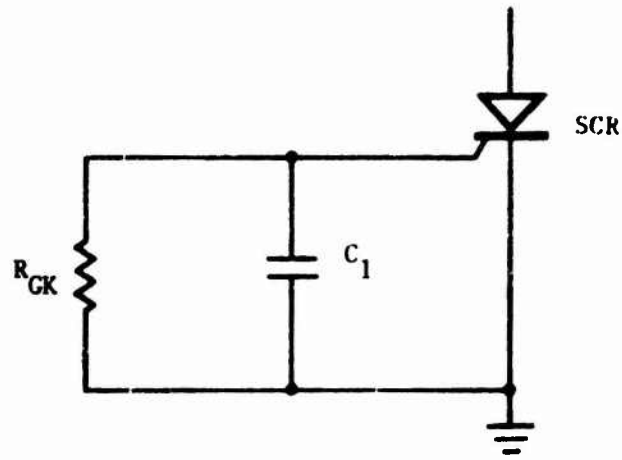
(d) Op-Amp Output Clamping

Figure 3-3. Antisaturation Techniques

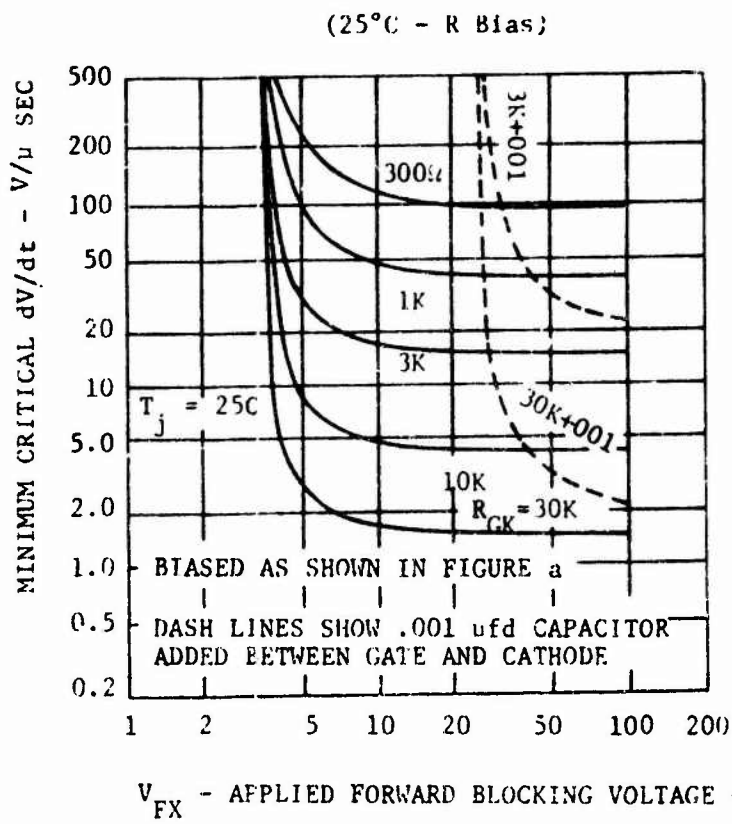
b. Stable Responses

Another abnormal circuit response that must be considered is latch-up. For the purposes of this report, latch-up will be defined as the excursion of a circuit into an undesirable stable state which precludes normal circuit operation. An SCR is an example of a device which is designed to be latched in normal circuit use. However, EMP induced transients can cause latching at an unprogrammed time which may cause system malfunction. The prevention of premature SCR response due to fast rate of rise (dV/dt) anode transients is accomplished by either modifying the gate-cathode bias network, or by adding anode filters (Figure 3-4). As shown in Figure 3-4b, increased bias is necessary the more rapidly that anode voltage is applied to the SCR. Since increased bias increases the total trigger current requirement, overall sensitivity of the circuit is reduced. It is usually desirable to minimize dV/dt effects by providing transient filters which limit the rate of rise of anode voltage. In dc circuits, the power supply filter may accomplish this result. In other cases, simple RC filters can be employed. The load can often be used as the series element in the filter network.

Figure 3-5 illustrates the problem of trapping states in digital counters. The two state diagrams in this figure are for a counter with three flip-flops (or other binary circuits) and thus eight possible states. The configuration of the counter is designed to make use of only six states and thus provides a divide-by-six operation. Normally, the counter will never enter the two remaining unused states. However, under the influence of severe interference, the counter might be forced into one of these two unused states. With the state diagram in Figure 3-5a, the counter will never recover. It will simply switch back and forth between the two non-allowed states. The state diagram in Figure 3-5b does not lead to such problems. If the circuit is induced into one of the nonallowed states, it will sequence back into its normal operating pattern. The counter in this example is a "Johnson" counter. In Figure 3-5b, the Johnson counter

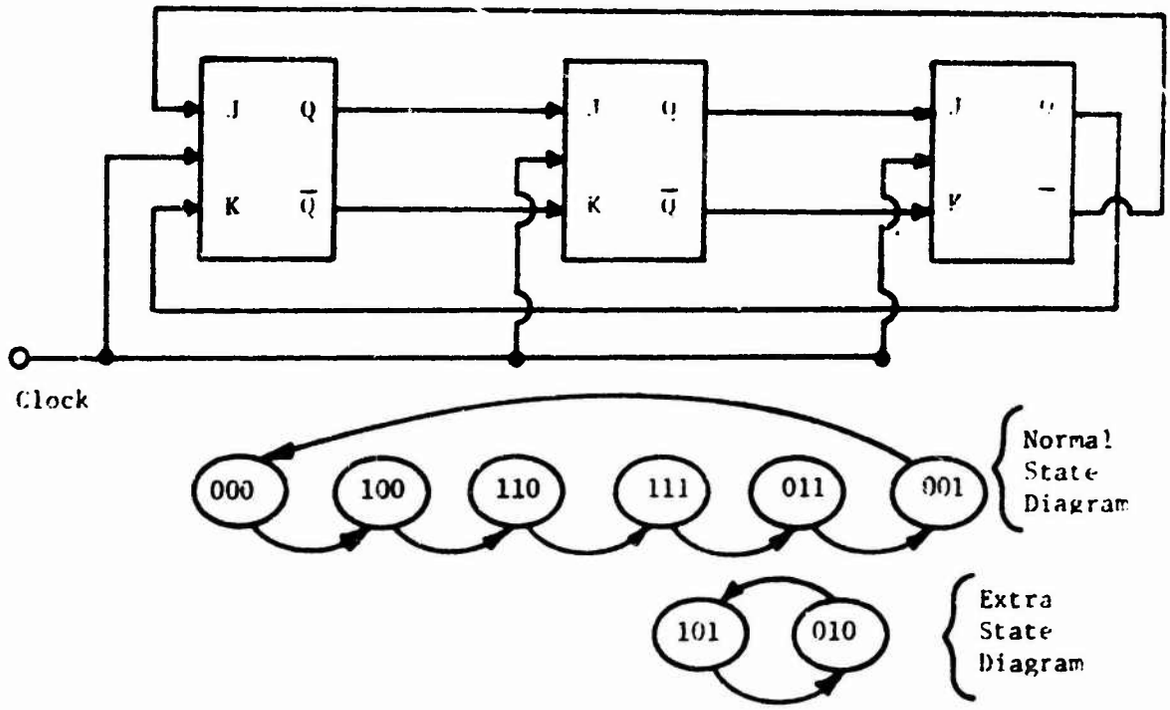


(a) SCR Bias Circuit

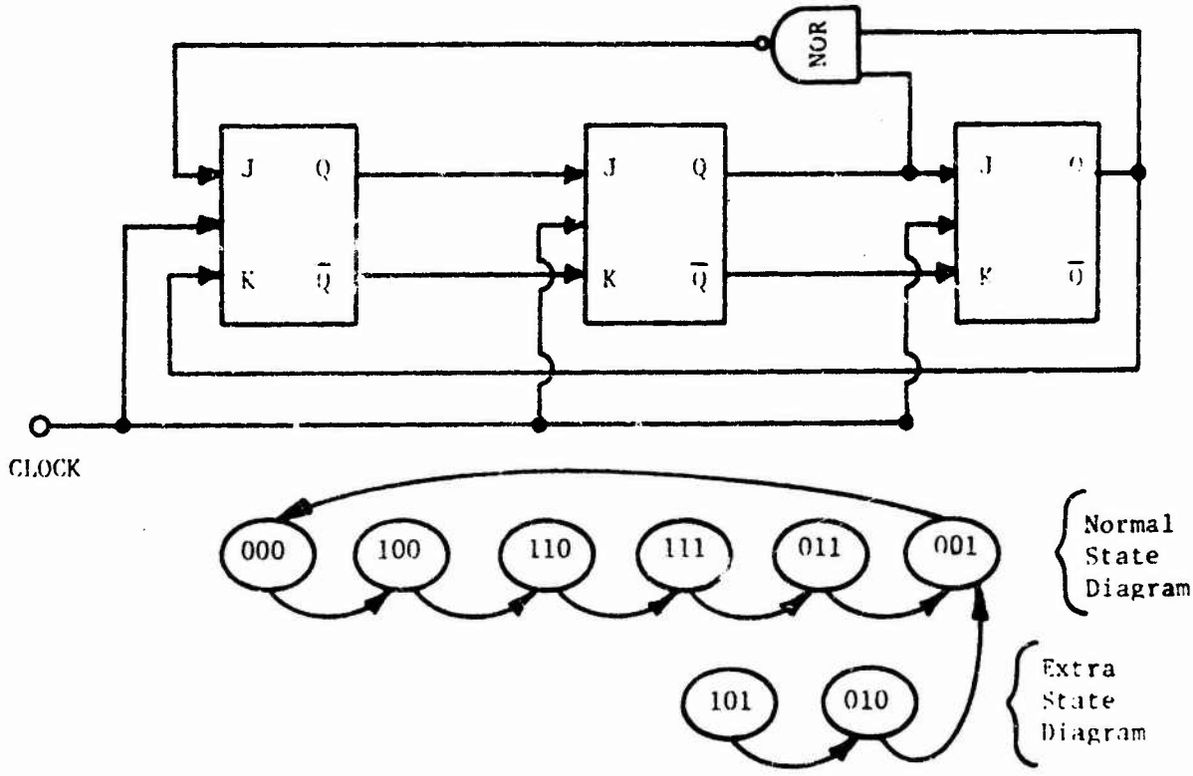


(b) Min. Critical dV/dt as a Function of Gate-Cathode Biasing

Figure 3-4. Illustration of SCR dV/dt Sensitivity



(a) Johnson Counter



(b) Modified Johnson Counter

Figure 3-5. Illustration of Trapping States in Digital Counters

has been modified by the addition of a gate to make the appropriate change in its state diagram. This problem can exist in any counter which does not make use of all of the available states in its normal operation. The problem may occur with ring counters, Johnson counters, or binary counters that use feedback to limit the normally used states. The important factor is the detailed nature of the complete state diagram. States from which recovery cannot be accomplished should always be eliminated.

Another type of latch-up occurs in multistage, negative feedback amplifiers with a saturated input stage. At a critical input voltage, the gain changes polarity and magnitude. In such a situation, the inverting amplifier transfers signal in a noninverting mode at essentially unity gain after saturation. The amplifier system as a whole, however, may still have a reasonably high gain because subsequent stages are not saturated. The net effect is a reversal in polarity and some reduction in gain for the overall multistage amplifier. If such an amplifier is utilized in a gain controlling feedback configuration, the loss of one inversion within the amplifier system changes negative feedback to positive feedback and may in some cases cause latch-up. This is a particularly common problem in integrated circuit operational amplifiers which typically use two differential amplifiers in cascade. Any multistage amplifier, however, can exhibit the same problem regardless of the nature of the individual amplifier stages. The problem may be prevented in two ways: (1) feedback can be restricted to values insufficient to realize > 1 closed loop gain for saturation of the first stage, and/or (2) input signals may be limited to amplitudes insufficient to cause first stage saturation.

4. TRANSIENT ISOLATION

When the protection of integrated circuits or other prepackaged circuits is required, external components such as series resistors or shunt capacitors or external, hardened buffer circuits may be used to

increase circuit damage hardness. This is an alternative to the use of terminal protection devices such as discussed in Chapter 6. In general, this type of design is applicable only where relatively small (hundreds of volts) EMP transients will be incurred.

The protection of power supply lines is relatively easy using general amplitude limiting and/or filtering techniques. For this case, special consideration must be given to the following factors:

(1) Proximity of filters to the circuit.

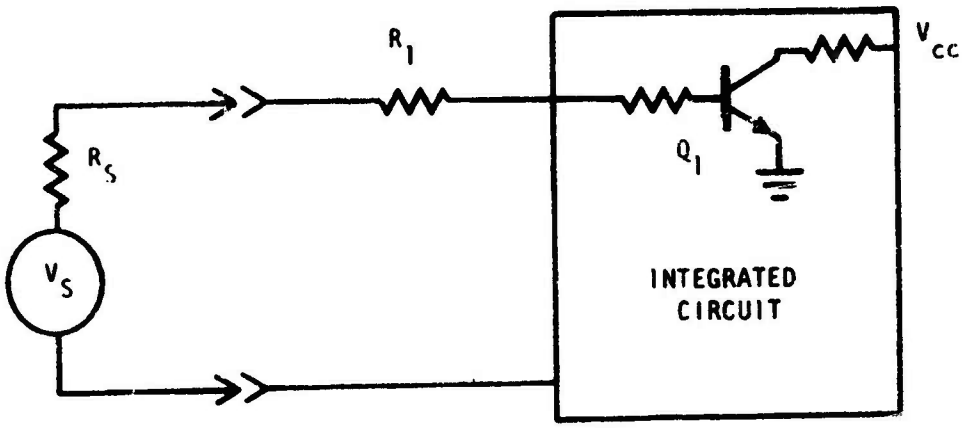
(2) High frequency (fast risetime) response of conventional low pass filters. The response of low pass filters to frequencies considerably above the cutoff frequency may render such filters useless.

The upset hardening of signal output or input ports depends on several factors including the following:

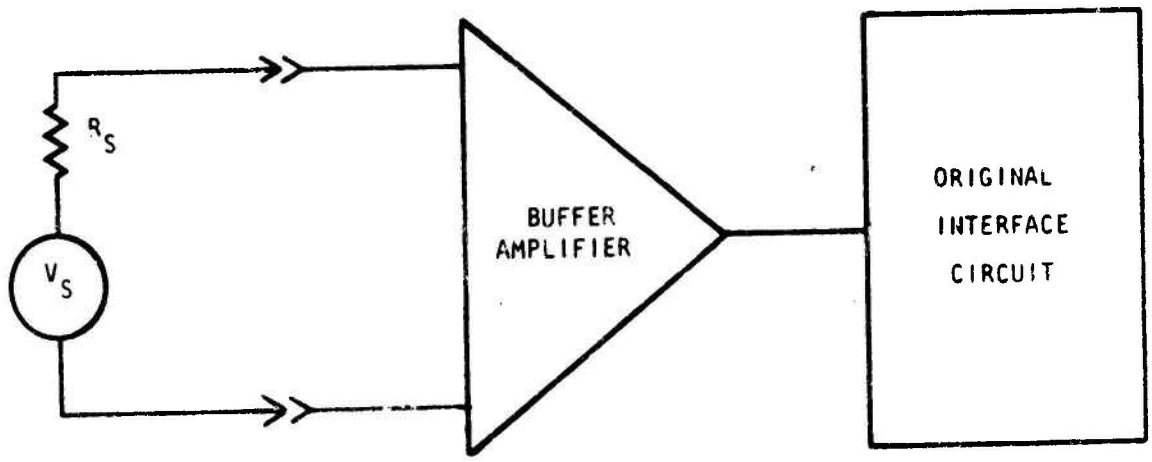
(1) The relationship between the normal signal and the interference signal.

(2) Susceptibility threshold of the port of interest.

When system parameters such as available space, cost, and reliability do not limit the use of additional components or circuits, a significant increase in hardness can be obtained by transient isolation. Two simple examples are shown in Figure 3-6. Figure 3-6a shows an external series resistor, R_1, used to limit current into an RTL inverter. The considerations here are similar to those of the example in Figure 3-1. The value



(a) INPUT CURRENT LIMITING



(b) BUFFER-AMPLIFIER

Figure 3-6. Transient Buffering Examples

of R_1 must be selected such that sufficient base drive is available to saturate Q_1 under worst case conditions (temperature, fan out, etc.). However, considerable reduction of susceptibility may be realized even under those constraints.

Figure 3-6b illustrates the use of a damage hardened buffer-amplifier to absorb or divert transient energy while at the same time altering operational parameters such as voltage gain. Of course the buffer itself must be hard to the anticipated EMF levels. The design of buffer circuits will be familiar to the design engineer and hence, is not discussed in detail.

Amplitude limiting at the interface is a primary hardening technique candidate. Chapter 6 should be consulted for detailed data on suppression device for amplitude limiting. The function of amplitude limiting networks for either damage or upset are essentially the same in that voltages above a specified amplitude are prohibited and excess energy is diverted away from the protected circuit. For upset hardening, incident voltage amplitudes are relatively low (< 100 volts) and the effective interrupt time during limiting can be critical. The subsystem outage specification must be known in order to determine if the limit level required to prevent abnormal circuit operation is compatible. If the outage time exceeds the specified maximum, alternate hardening techniques such as filtering or some hybrid approach may be necessary. If amplitude limiting is satisfactory, the insertion effects of the limiter must be evaluated to assure capatibility with normal circuit function. Limiter capacitance, frequency response, and leakage are primary parameters to consider.

If outage time is critical, time related factors, such as those listed below, should be considered.

(1) Interference duration. For a given limit level, outage time will obviously depend on the duration of the EMP signal.

(2) Circuit recovery time. Circuit outage time in some cases may exceed the incident transient duration due to charge storage.

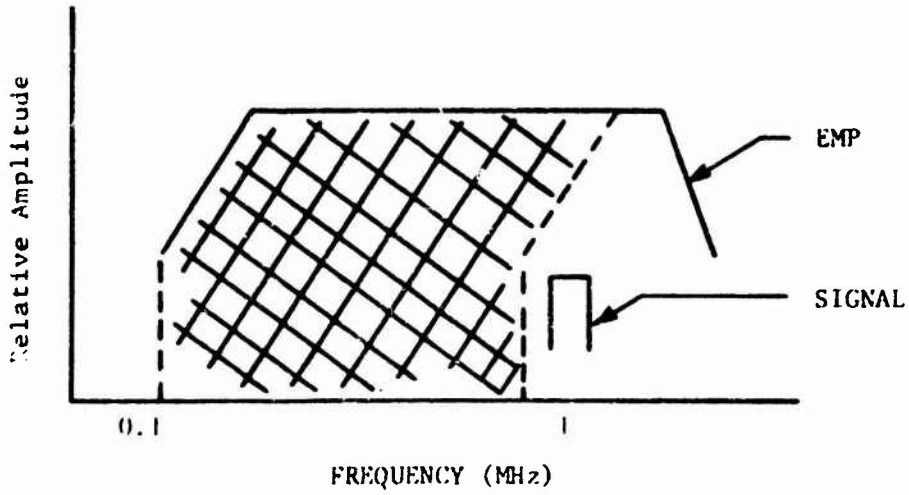
5. HYBRID TECHNIQUES

The subsystem upset hardening techniques mentioned up to this point may be used separately to effect some decrease in upset susceptibility. In many cases they may also be used in combination to enhance their effectiveness. Two examples of combined or hybrid upset hardening techniques will be discussed here.

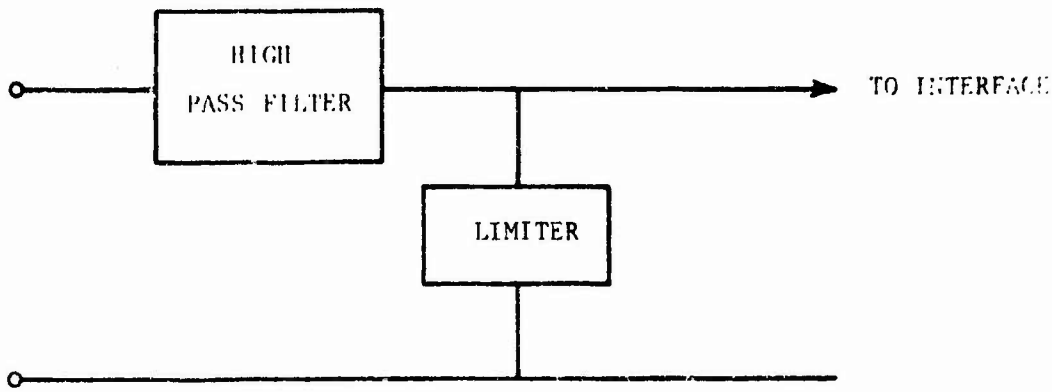
Consider a subsystem interface connected to a circuit that exhibits latch-up or saturation recovery problems when subjected to high amplitude transients. Figure 3-7a shows the signal and predicted EMP interference characteristics at the unhardened interface. The exclusive use of amplitude limiting techniques in this case would cause a long subsystem interruption due to the presence of low frequency EMP components. Although the limiter related outage would be shorter than a latch-up or saturation outage, it is not the minimum that can be achieved.

Since signal frequencies are near the upper end of the EMP spectrum, the use of a high pass filter will eliminate most of the EMP low frequency components as shown by the cross hatched area in Figure 3-7a. The use of a limiter after high pass filtering has been performed will yield the minimum outage period and therefore minimum lost data. This configuration is shown in Figure 3-7b. Any high frequency components generated by the limiting process will be of low amplitude and of no consequence for this case.

The combined use of various types of filters and limiters is an effective solution to many practical upset hardening problems. Given the relationship between the signal and EMP frequencies and amplitudes, the design of such networks is reasonably straightforward. As discussed in



(a) Signal and EMP Characteristics



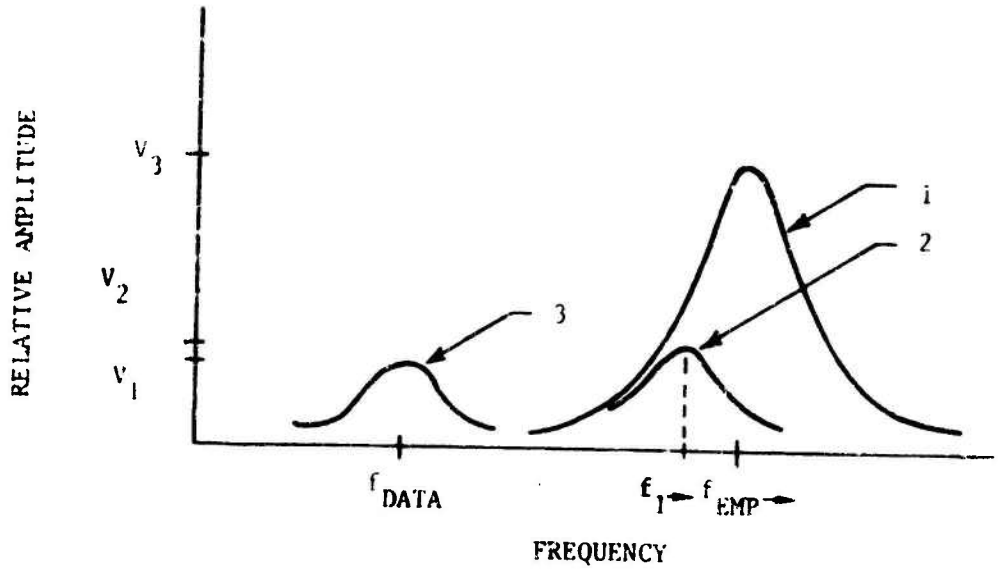
(b) Hybrid Upset Hardening Network

Figure 3-7. Upset Hardening Using Combined Filtering and Limiting

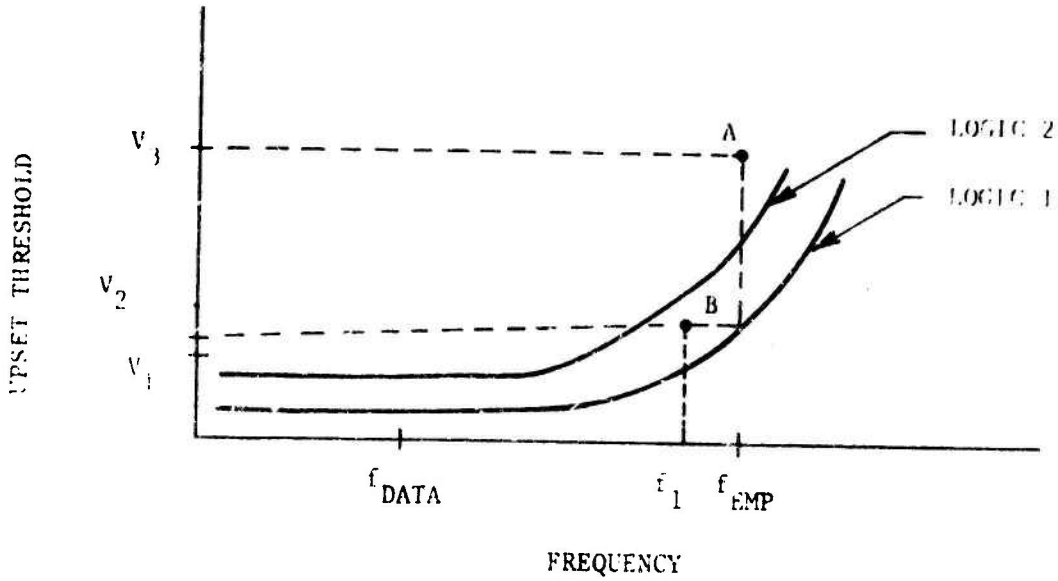
Chapter 6, limiters exhibit unique response to fast risetime pulses and also generate new high frequency components regardless of the frequency of the incident signal. These factors impact limiter/filter hybrid design and must be carefully evaluated.

Another useful combination, or hybrid, upset hardening technique involves combining filtering techniques and IC logic family selection. Given the initial EMP interference spectrum shown by Curve 1 of Figure 3-8a, it is apparent that both of the logic families characterized by Figure 3-8b will be upset (Point A, Figure 3-8b). As is generally the case, the data bit rate is assumed to be lower than the lowest EMP frequency, Curve 3, Figure 3-8b. The use of a low pass filter will shift the EMP frequency spectrum as shown by Curve 2 of Figure 3-8b. The higher noise immunity and lower frequency response of logic type 2 necessitates its selection in order to minimize the probability of upset. Point B of Figure 3-8b is the transient level after filtering. Logic type 2 is also compatible with the normal logic "one" level of V_1. In this case no change in the logic signal level was required because the slower response characteristic of logic type 2 was more important than the increase in noise immunity. However, this will not usually be the case.

The examples of circuit level hardening presented here are intentionally brief due to the impracticality of illustrating even a small cross section of the design problems caused by transient interference. This discussion is designed to expose some of the functional trade-offs related to EMP hardening so that they may be integrated into the design consideration related to the general interference problem.



(a) EMP/Data Frequency Spectra



(b) Logic Upset Level Comparison

Figure 3-8. Upset Hardening Using Combined Filtering and IC Selection

6. REFERENCES

The following references were used in this chapter:

(1) Burr-Brown Research Corporation, "Operational Amplifiers, Design and Applications," The Maple Press Company, 1971, pp. 244-245.

(2) Millman, J., and Taub, H., "Pulse, Digital and Switching Waveforms," McGraw-Hill Book Company, 1965, pp. 297-300.

(3) Texas Instruments Incorporated, "Solid-State Communications, Design of Communications Equipment Using Semiconductors," McGraw-Hill Book Company, 1966, pp. 202-224.

CHAPTER 4

COMPONENT RATINGS

1. INTRODUCTION

The failure threshold of a circuit or subsystem is determined from the failure thresholds of the components that make up that circuit or subsystem. In some cases, the hardness can be improved by simply using harder components as pointed out in Chapter 3. Obviously, this requires an extensive data base of relative component hardness ratings. This chapter discusses the available damage threshold data for the various components used in electronic circuits and subsystems. Specifically three categories of components will be discussed: semiconductor junction devices, integrated circuits, and passive components. The computer code SUPERSAP (Reference (1)) provides an amenable data base for component hardness data.

2. SEMICONDUCTOR JUNCTION DEVICES

Considerable previous work has been performed to investigate semiconductor damage thresholds and to develop models to predict their pulse power burnout characteristics. The most widely used model was developed by Wunsch (Reference (1)). The Wunsch model is based on junction heating and predicts the power required to fail a semiconductor junction as a function of the pulse width. This relation is given as

$$P = Kt^{-1/2}$$

where P is the power required to fail the junction, K is a constant based on junction properties and geometry, and t is the pulse time to failure.

Many of the failure threshold studies concerning semiconductor junction devices have been designed to determine the value of K (damage constant). These damage constants can be stored in tabular form or in a computer for quick retrieval. An extensive list of damage constants for diodes and transistors is given in the EMP Susceptibility Threshold Handbook (Reference {2}).

A summary of the range of damage constants for five general classes of diodes is presented in Figure 4-1 and for five general classes of transistors in Figure 4-2. Note that for both diodes and transistors, the low power, high frequency units are the most susceptible. A microwave diode having a K of 10^{-3} requires only 1 watt of power applied for 1 μsec to cause failure; whereas a silicon reference diode, such as might be used for terminal protection, having a K of 10 would require 10,000 watts applied for 1 μsec to cause failure.

3. INTEGRATED CIRCUITS

a. Damage

There are very little data available on the damage thresholds of integrated circuits. As yet, models analogous to the Wunsch model for junction devices have not been developed to predict the terminal failure thresholds of integrated circuits. While there have been some tentative conclusions drawn concerning the relative hardness of various types of integrated circuits, considerably more research is needed before a useful data base can be constructed.

In general, linear IC's are considered harder than digital IC's. This is due primarily to the larger series input resistors used in linear IC's.

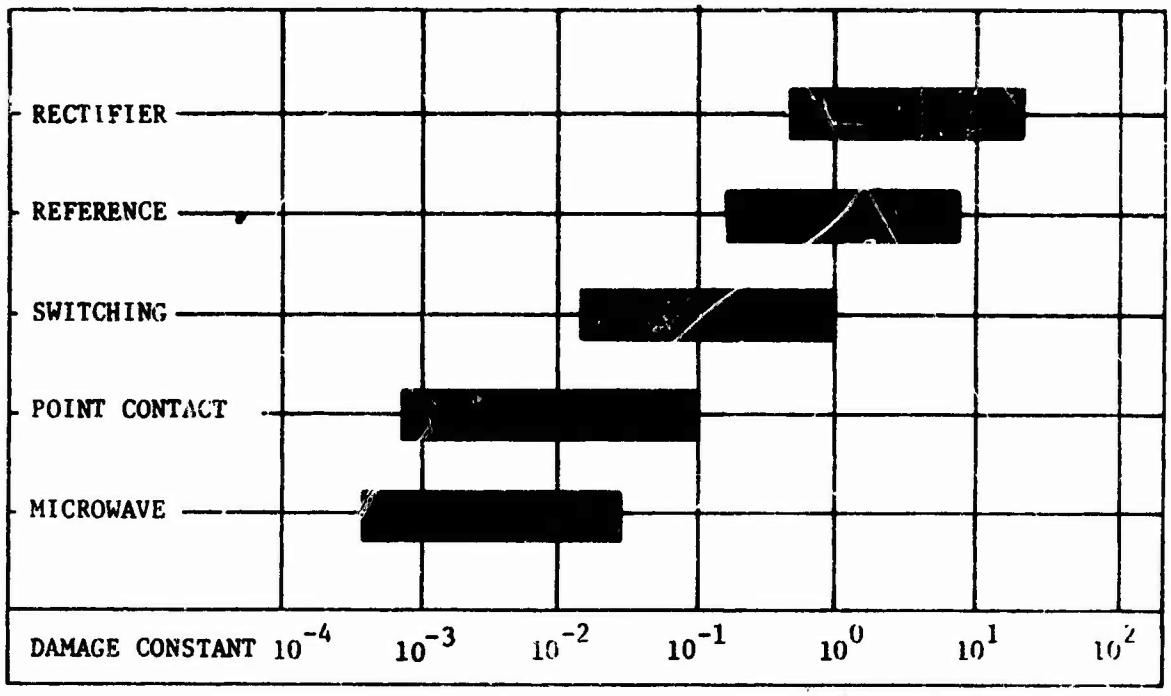


Figure 4-1. Range of Measured Damage Constant for General Diode Classes

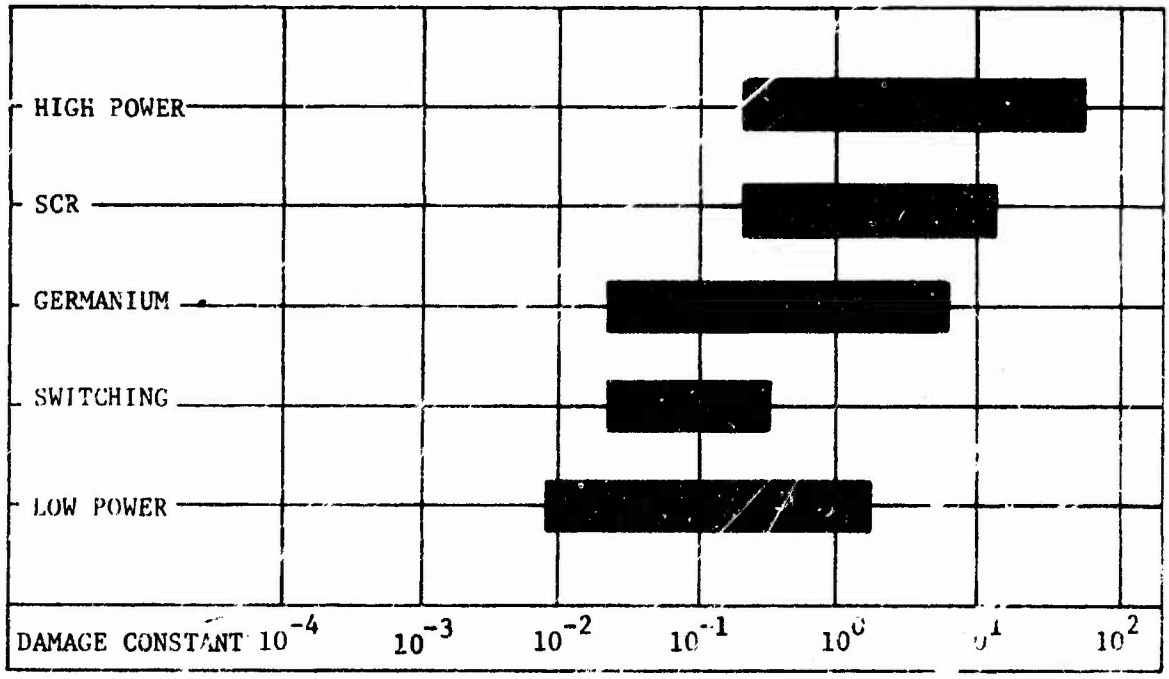


Figure 4-2. Range of Measured Damage Constants for General Transistor Classes

Figure 4-3 is a comparison of the average damage threshold characteristics of a sample of digital and linear integrated circuits presented in (Reference (4)). The number associated with each data point represents the number of devices tested.

There are insufficient data available at this time to draw firm conclusions as to the relative damage hardness of the various digital integrated circuit types (TTL, DTL, RTL, ECL). The average failure thresholds for the input of a number of different digital integrated circuits are shown in Figure 4-4. While these data give no indication of a consistent hardness advantage of one circuit type over another, survey tests have uncovered interesting trends listed below. These data are obtained from the above reference and from the test program described in Appendix A.

(1) Damage threshold for a given functional logic varies with manufacturer.

(2) High noise immunity logic may be more susceptible to burnout than standard logic.

(3) Passive components in integrated circuits are extremely transient sensitive and can determine device damage threshold.

(4) Application of the Wunsch model to junction devices on an integrated circuit chip does not give meaningful results.

b. Upset

Fortunately, the assessment of integrated circuit EMP upset susceptibility can be readily accomplished. A significant amount of

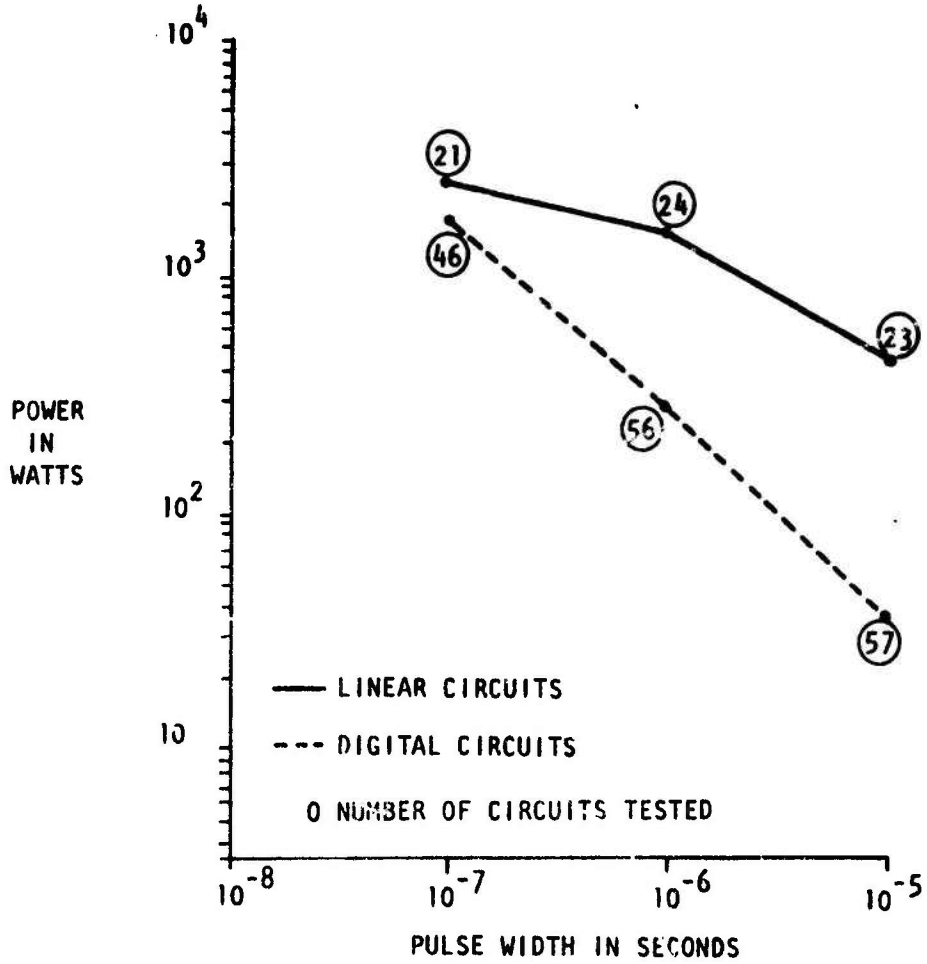


Figure 4-3. Damage Threshold for Integrated Circuits

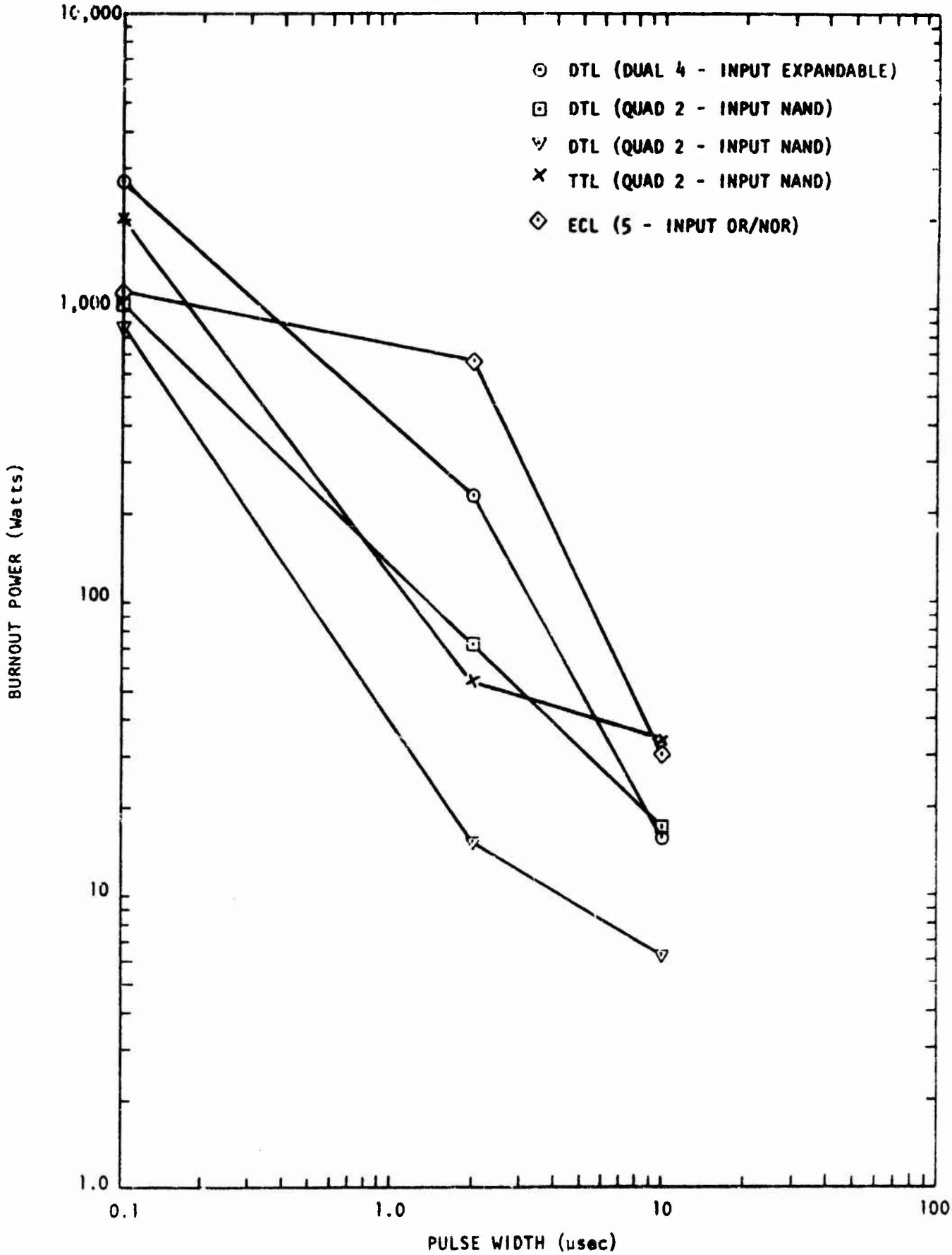
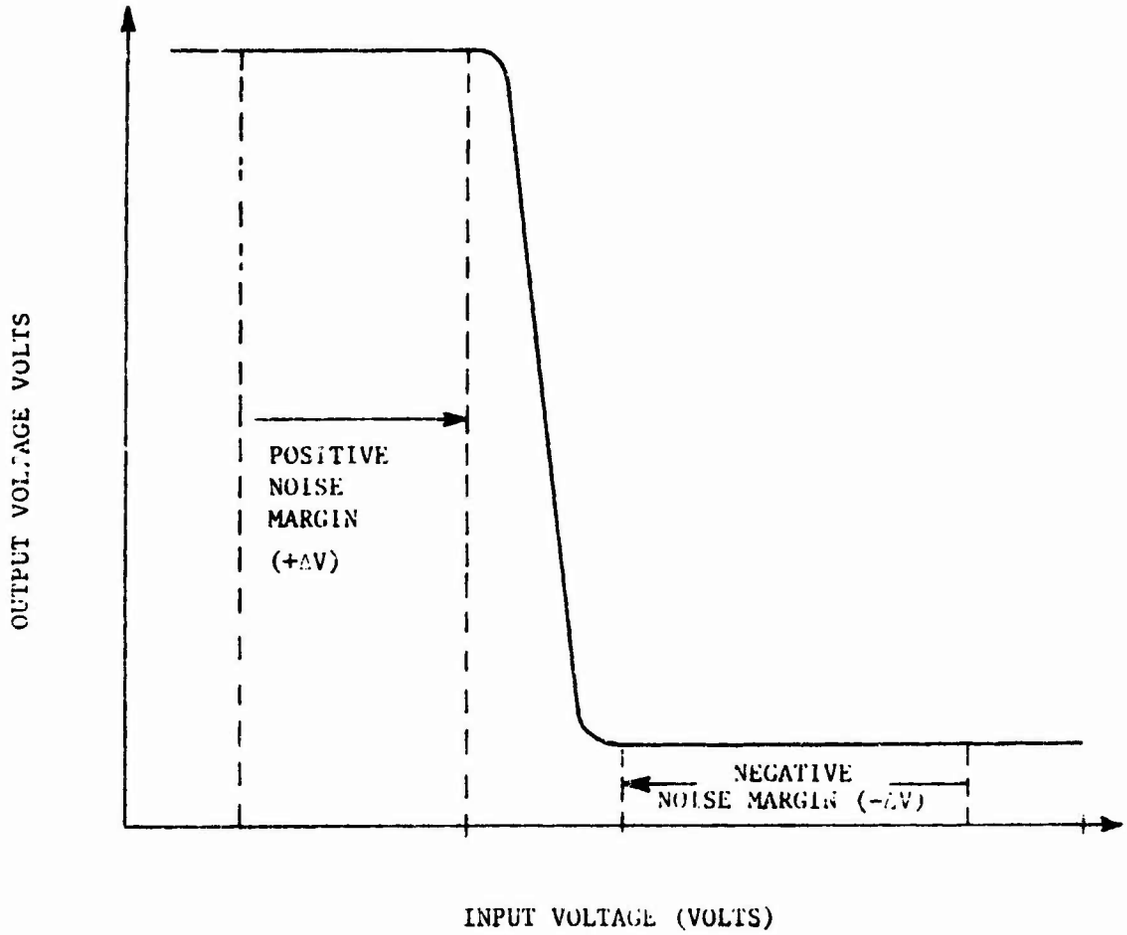


Figure 4-4. Burnout Power of the Input of Various IC's Versus Time

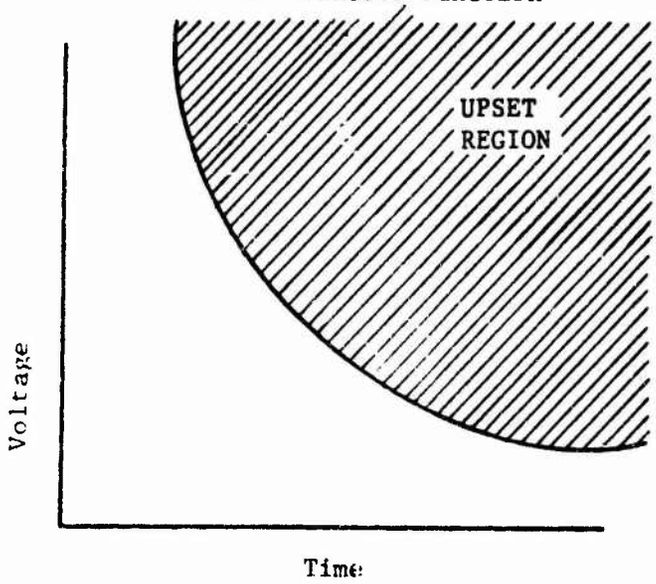
information describing the response of integrated circuits to powerline spikes, input noise, pulses on input terminals that are outside the normal input voltage range, and other unusual signals, is available in product data sheets and design guidelines publications. Hardening by component selection is applicable in cases where either an increase in noise immunity or a decrease in response time (increased propagation delay) will, either independently or in combination with other hardening techniques, reduce the probability of an undesirable response.

Saturating digital circuits can be characterized by active elements which are operated in either their high (1) or low (0) conduction state in order to produce two distinct output levels. The digital circuit output state is controlled by the voltage at the input node of the active switching device which is derived by a logical combination of the input voltages. Figure 4-5a shows a typical logic transfer function and illustrates positive and negative noise margin. Logic upset occurs if the magnitude of the EMP transient is high enough and if the duration of the transient exceeds the circuit's propagation delay time. Figure 4-5b shows the form of an upset characteristic. Increasing either ΔV or t_{pd} reduces upset susceptibility for a given transient (Reference (2)). For well defined EMP interference, maximizing these parameters, consistent with normal operating design specifications, is a valid upset hardening technique. Whether or not subsystem upset occurs depends on the response invoked by the circuit upset and is determined by operational and criticality analyses.

For the characteristic damped sine EMP induced transients, the digital logic circuitry will be most effective if designed so that the positive and negative noise margins are equal. This assumes the input impedance seen by the transient signal is equal for both polarities. Also note that dc voltage noise comparisons are meaningful only if the input impedances of the logic circuits are comparable. Otherwise energy noise immunity must be considered.



a. IC Transfer Function



b. Minimum V-T Characteristic for Upset

Figure 4-5. Typical Logic Transfer Function

Maximizing noise margin and propagation delay requires an evaluation of the following trade-offs:

$$\text{Increased } \Delta V \longrightarrow \begin{cases} \text{Increased } V_{CC} \\ \text{Increased Power Dissipation} \\ \text{Increased Propagation Delay} \end{cases}$$

$$\text{Increased } t_{pd} \longrightarrow \text{Slower Data Rate}$$

Table 4-1 is a general comparison of digital logic families including such design constraints as cost and functional flexibility (References (4) through (6).

EMP induced transient signals generated on system cables are a conducted type of interference which is most critical at the cable/conductor circuit interface. While higher noise margins throughout the system circuitry are desirable, higher noise margins for only the interface circuitry are probably more cost-effective. High noise immunity integrated logic circuits are available which can be used in such an interface hardening scheme. The use of discrete logic circuits can yield higher noise immunity if the size, cost, and reliability penalties are acceptable.

Increased propagation delay time will result in the attenuation of the high frequency content of the EMP induced transients but will lower the permissible bit rate also. EMP transient pulse energy is usually concentrated mainly in the 10 kHz to 100 MHz frequency region for aeronautical systems. If system requirements allow the bit rate to be lower than 10 kHz, then effective EMP upset hardening can be accomplished by using devices with large propagation delays. Some intrinsic filtering is inherent in circuit design due to minority carrier storage and parasitics. The designer should take maximum advantage of this intrinsic

TABLE 4-1

COMPARISON CHART OF THE MAJOR IC DIGITAL LOGIC FAMILIES

Parameters	RTL	Low-Power RTL	DTL	RTL	12-ns TTL	6-ns TTL	4-ns ECL	2-ns ECL	1-ns ECL	P-MOS	CMOS
1. Circuit form	← resistor-transistor →		diode-transistor	diode-Zener transistor	← transistor-transistor →		← emitter-coupled current mode →			p-channel MOS	complementary MOS
2. Positive logic function of basic gate	← NOR →		← NAND →				← OR/NOR →			NAND	NOR or NAND
3. Wired positive logic function	← implied AND (some functions) →		implied AND	implied AND (A-O-I)	← AND-OR-INVERT →		← Implied OR (all functions) →			← none →	
4. Typical high-level Z_{in} Ohms	640	3.6 k	6 k or 2 k	15 k or 1.5 k	70	10	15	6	6	2 k	1.5 k
5. Typical low-level Z_o	R_{sat}	R_{sat}	R_{sat}	R_{sat}	R_{sat}	R_{sat}	15 ohms or 2.7 mA	8 ohms or 6.7 mA	6 ohms or 21 mA	25 k	1.5 k
6. Fanout	5	4	8	10	10	10	25	25 inputs at 50 ohms	10 low-Z inputs or 50 ohms	20	50 or higher
7. Specified Temperature range, °C	-55 to 125 0 to 75 15 to 55	-55 to 125 0 to 75 15 to 55	-55 to 125 0 to 75	-30 to 75	-55 to 125 0 to 70	-55 to 125 0 to 75	-55 to 125 0 to 75	-55 to 125 0 to 75	0 to 75	-55 to 125 0 to 75	-55 to 125
8. Supply voltage	3.0V ± 10% 3.6V ± 10%	3.0V ± 10% 3.6V ± 10%	5.0V ± 10%	15 ± 1 V	5.0V ± 10% 5.0V ± 5%	5.0V ± 10% 5.0V ± 5%	-5.2V + 20% - 10%	-5.2V + 20% -10%	-5.2V ± 10%	-27 ± 2V -13 ± 1V	4.5 to 16V
9. Typical power dissipation per gate	12 mW	2.5 mW	8 mW or 12 mW	55 mW	12 mW	22 mW	40 mW	55 mW plus load	55 mW plus load	0.2 to 10 mW	0.01 mW static 1 mW at 1 MHz
10. Immunity to external noise	nominal	fair	good	excellent	very good	very good	good	good	good	nominal	very good
11. Noise generation	medium	low-medium	medium	medium	medium-high	high	low	low-medium	medium	medium	low-medium
12. Propagation delay per gate, ns	12	27	30	90	12	6	4	2	1	300	70
13. Typical clock rate for flip-flops, MHz	8	2.5	12 to 30	4	15 to 30	30 to 60	60 to 120	200	400	2	5
16. Number of functions; family growth rate	high; growing	high; growing	fairly high; new functions in TTL	nominal; growing	very high; growing	very high; growing	very high; growing	high; growing	high; growing	low; growing	low, growing
15. Cost per function	low	low	low	medium	low	medium	low	medium	high	medium to high	medium to high

filtering. For discrete circuits, one should select active components with large values of junction capacitance, and lower high frequency cutoff parameters, such as F_t. For integrated circuits, the slowest logic types should be chosen which will operate at the maximum required bit rate. Reference (7) presents a graphical illustration of voltage-time upset characteristics of four logic families as shown in Figure 4-6. Curves of the general form shown in this figure apply to most logic families. References (8) and (9) present information further illustrating the voltage-time upset problem.

It should be mentioned at this point that EMP hardening by component selection may decrease component hardness to the effects of neutrons and gamma radiation. The consequences of such EMP hardening measures must therefore be evaluated in the interest of maintaining balanced hardening for systems required to withstand all nuclear weapon effects.

4. NONSEMICONDUCTOR COMPONENTS

EMP induced damage in subsystems has been generally treated as a problem associated exclusively with semiconductor components. While these devices are inherently sensitive to transient overloads, other device types such as resistors and capacitors are also susceptible to degradation or permanent damage at the same voltage or power levels. With the increased use of advanced microelectronic design techniques in aeronautical systems, the population of small, low power, passive components is increased to such an extent that they may in some cases determine a given circuit's damage threshold. Included in the nonsemiconductor category are passive circuit elements such as resistors, capacitors, and inductors along with all types of vacuum tubes and electromechanical devices such as relays, transformers, switches, and electroexplosive devices. At the present time, there is no established data base for nonsemiconductor devices, and likewise there are no accepted failure modes. The limited

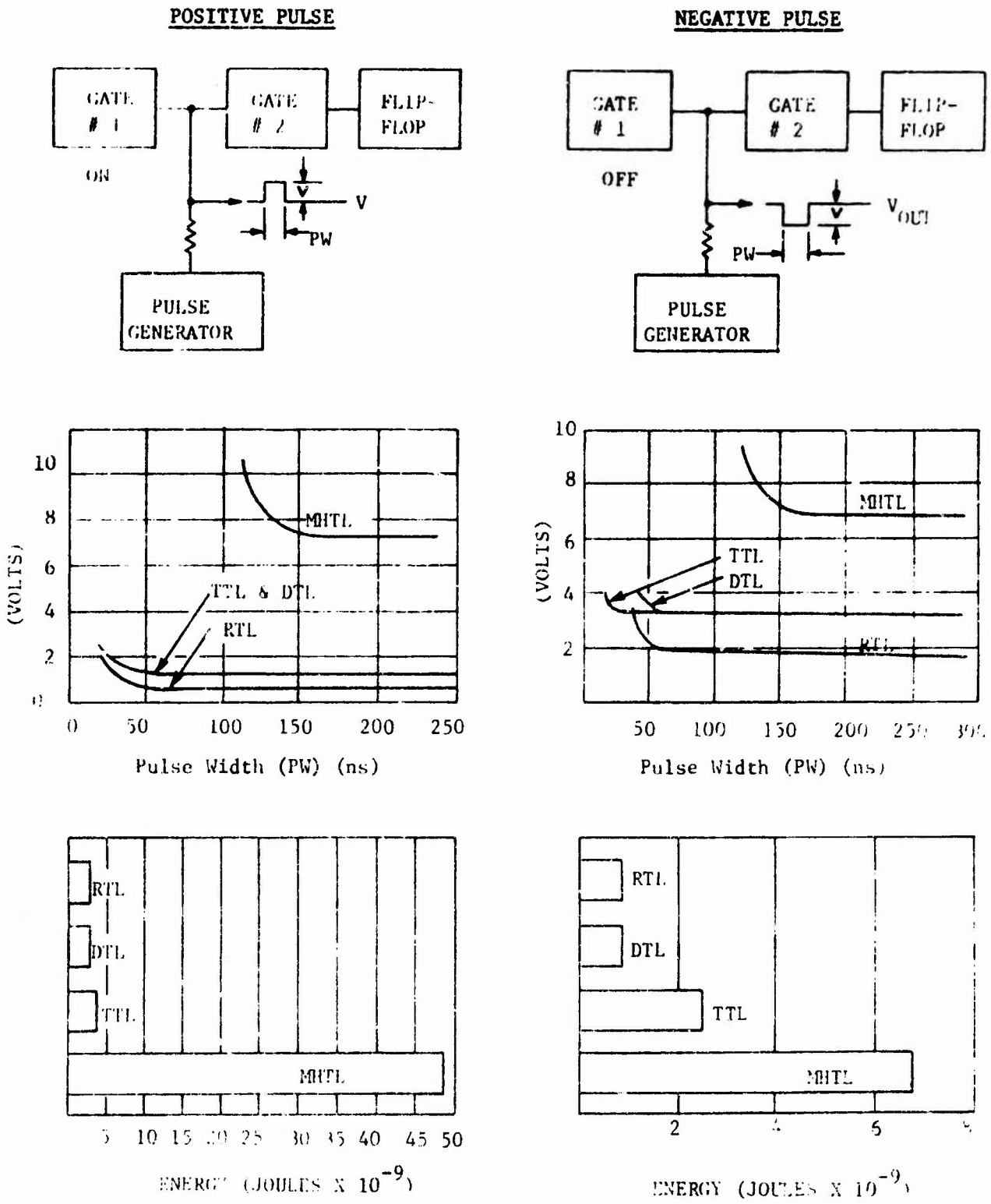


Figure 4-6. Comparison of Logic Family Upset Threshold

test data available show that vacuum tubes, relays, and transformers are, for the most part, insensitive to EMP type signals. Low power metal film resistors and low voltage, polarized tantalum capacitors may suffer degradation or failure when subjected to EMP signals of the same order of magnitude that would damage a medium power semiconductor. Some carbon composition resistors have shown a decrease in resistance during pulse application but recover to nominal value after the pulse. This decrease could affect circuits that use these resistors as series current limiting elements.

Clearly this information is insufficient to support an EMP hardened design. Until sufficient information becomes available, all that can be said is that nonsemiconductor components should not be regarded as hard on an a priori basis. The response at each component to the EMP specification signals should be calculated. Any nonsemiconductors subjected to voltages and currents substantially above their design specifications should be considered potentially susceptible. In these cases, a test program is required to establish the hardness levels of these components.

5. REFERENCES

The following references were used in this chapter:

(1) Boeing Company, The, "SUPERSAP Control Manual," AFWL Contract No. F29601-72-C-0028, Boeing Document No. D224-10020-2, March 1973.

(2) Wunsch, D. C., and R. R. Bell, "Determination of Threshold Failure Levels of Semiconductor Diodes and Transistors Due to Pulse Voltages," IEEE Transactions on Nuclear Science, Vol. NS-15, No. 6, December 1968.

(3) Boeing Company, The, "EMP Susceptibility Threshold Handbook," AFWL Contract No. F29601-72-C-0028, Boeing Document No. D224-10013-1, July 1972.

(4) Smith, J. S., "Pulse Power Testing of Microcircuits," RADC-TR-71-59, Rome Air Development Center, October 1971.

(5) Garrett, Lane S., "Integrated Circuit Digital Logic Families," Part I, kTL, DTL, and HTL Devices," IEEE Spectrum, pp. 46-58, October 1970.

(6) Garrett, Lane S., "Integrated Circuit Digital Logic Families, Part II, TTL Devices," IEEE Spectrum, pp. 63-72, November 1970.

(7) Garrett, Lane S., "Integrated Circuit Digital Logic Families, Part III, ECL and MOS Devices," IEEE Spectrum, pp. 30-42, December 1970.

(8) Motorola Semiconductor Products Inc., "Noise Immunity With High Threshold Logic," Application Note AN298.

(9) Miles, Eugene T., "Schottky TTL versus ECL for High Speed Logic," Computer Design pp. 79-86, October 1972.

(10) Gray, R. M., "An Experimental Investigation of EMP Induced Transient Upset of Integrated Circuits," Sandia Laboratories Document SM-TM-71-0330 June 1971.

CHAPTER 5

PACKAGING

1. INTRODUCTION

The design of an EMP hardened assembly consists not only of choosing the proper components and the optimal protective devices, but also of giving proper consideration to the packaging of the assembly. Without proper packaging, even the most attractive hardening concepts may become useless. It is the purpose of this chapter to present a coherent treatment of the EMP related aspects of assembly packaging. This discussion will be limited to treatment of a single assembly or box. However, in many cases it will be obvious that the same philosophy and rules proposed for single boxes can be applied to an entire system or subsystem. Therefore, although this handbook, and specifically this chapter, are directed toward the design engineer who has a particular specification to meet for a single circuit or subsystem unit, the concepts described here can be considered for application to larger systematic entities.

It should be noted that the discussions presented here are not necessarily original. An adequate packaging design is necessary for any complex system to achieve Electromagnetic Compatibility (EMC). Thus, the concepts discussed here are merely those concepts that have been successfully applied in the past by previous designers for EMC reasons. These concepts have been reviewed for their applicability to the subsystem unit EMP hardening problem and are assembled here into a consistent approach.

Proper EMP hardened package design must consider three areas:

- Zoning
- Shielding
- Grounding

The remainder of this section treats these three topics in detail.

2. ZONING

a. Layout

If EMP hardened packaging is considered as an original design parameter, significant hardening improvements can sometimes be achieved simply by using care in establishing the layout of individual circuits or the relative location of various circuit groups. It is possible to establish zones of protection in which the most sensitive circuits can be isolated from the source of the EMP transients by taking advantage of their electrical or physical isolation. A protective zone is defined here as an identifiable grouping of circuits or components which displays some commonality in the characteristics of concern for an EMP hardened design. The primary characteristics to be considered in establishing zones are circuit function, criticality, operating level, and susceptibility level. The requirements for zoning do not require the introduction of drastically new and different philosophies in the layout of electronic units. For example, circuits are conventionally laid out in a functional manner. That is, input, signal output, and processing and power supply are physically isolated from one another.

The interfacing requirements for an electronic unit generally necessitate points of entry into a system for EMP induced interference. Radio receivers, for instance, require deliberate antennas coupled directly into receiver circuitry. Interfaces to other electronic units require wires in relatively exposed cabling to be connected into circuitry internal to an electronic unit. Openings in electronic chassis are required in many cases for convection or forced-air cooling of circuitry that operates at high power levels. Openings in the shielding or chassis of electronic systems are also required for other purposes such as manual control shafts, access to recessed adjustment potentiometers and capacitors, etc. The purpose of zoning and shielding is to isolate all

circuit elements within an electronic unit from EMP interference of high enough levels to cause upset or damage without compromising functional interface requirements. Additionally, it is necessary to accomplish these goals in a cost-effective manner.

In most systems it is not feasible to group circuits on the basis of susceptibility alone. However, it is possible to first group the circuits according to their function and then construct zones on the basis of component or circuit susceptibility level. Thus, for example, a group of IC flip-flops may be zoned together as a highly susceptible zone and then be protected by a number of discrete buffer circuits which would represent a zone of lower susceptibility. At the same time, a parallel grouping of high susceptibility IC amplifiers might be buffered by similar low susceptibility discrete components. This type of combined zoning is illustrated in Figure 5-1. It should be noted that the components within a zone need not be related. The zone itself may have no functional significance other than its EMP protective role Thus, a relatively hard zone might consist merely of resistors placed in all interface lines to another softer zone. All that is necessary to establish a zone is careful design to assure that it meets its performance specifications. In this case, the specification would merely be a certain isolation between the input and the output together with a tolerable degradation of the interface signal.

There are a number of physical considerations to be addressed when establishing protective zones. These are not necessarily inherent in the concept, but arise from other consideraions such as economics, manufacturing, and reliability. In general, the specifications for zones will include both shielding and interface isolation. Thus, choosing the boundaries of a particular zone must be based on a consideration of its physical realizability. If the zone is to include shielding, then it should not be so small that it creates manufacturing problems. In

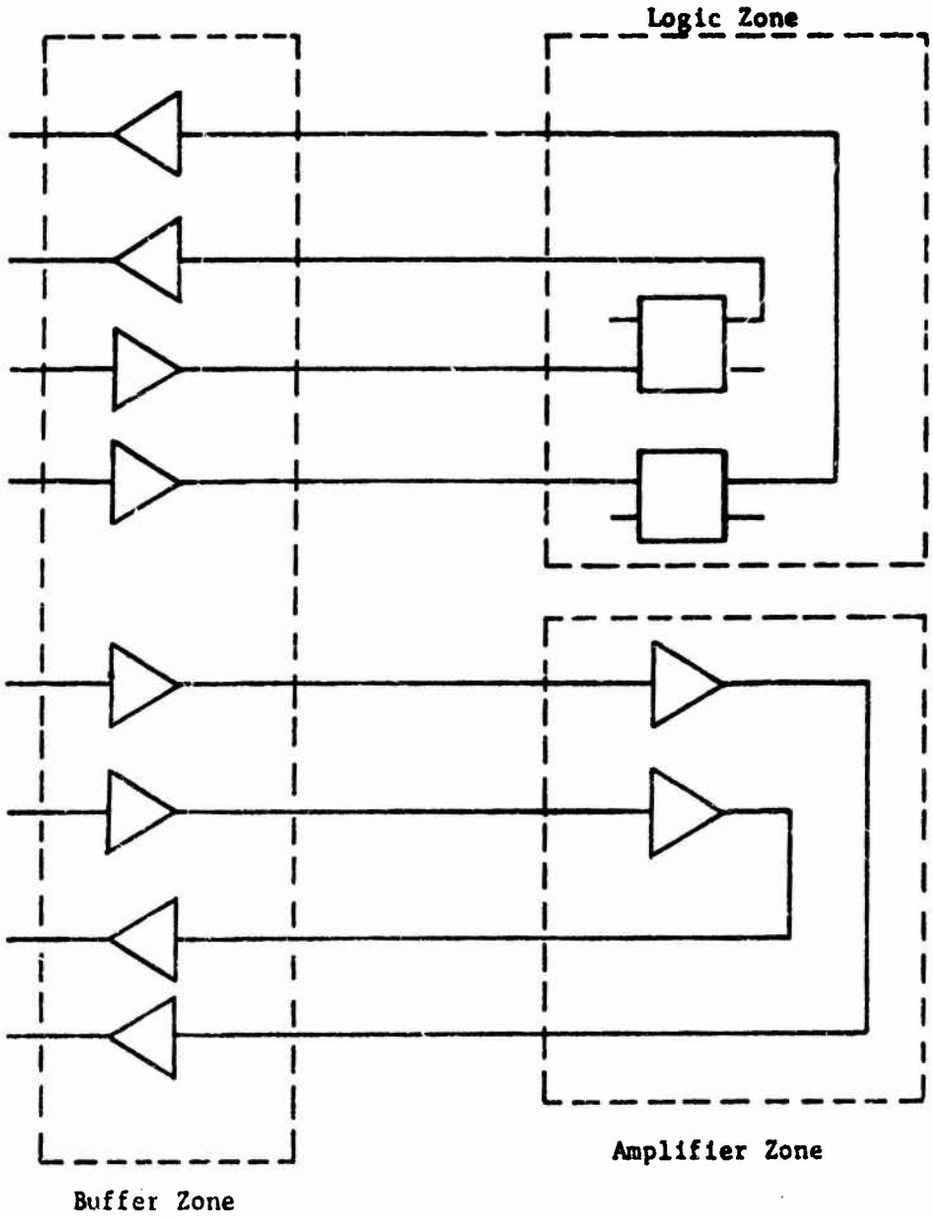


Figure 5-1. Combined Zoning

addition, if there are many zones, they may present a significant weight penality. On the other hand, it is desirable to minimize zone size to eliminate wiring lengths on the order of a wavelength for the EMP or signal frequencies.

The requirement to keep the cost and complexity of system design to a minimum dictates that the number of shielded and isolated zones be held to a minimum consistent with EMP hardening requirements. Although each specific design problem is likely to have its own unusual considerations, there are consistent guidelines to the pattern of zoning which generally apply to almost all electronic equipment.

First, internal signal processing circuits generally involve elements with high criticality and relatively high susceptibility to interference. These portions of the circuitry must generally be contained in one or more well-isolated and shielded zones which isolate these portions from external interfaces that provide entry points for EMP interference. Second, the circuitry directly related with these interfaces constitutes another required set of zones in which EMP interference is at a relatively high level and no highly susceptible circuitry is enclosed. Generally, these zones contain only interface and isolation circuitry such as interface amplifiers, isolation transformers, filters, etc. Zones of this type might also include interfaces such as display meters and manual controls which necessarily involve penetrations in the chassis. The third type of zone normally encountered encloses such elements as power supplies and servo motors. These zones are often established because the high power circuitry involved is itself a source of interference which must be isolated from other portions of the circuitry. This type of high power circuitry is generally immune to EMP interference and often involves interfaces external to the electronic unit and thus it also provides a logical zone for EMP purposes.

b. Zone Design

It is important to achieve an adequate grounding system within a protective zone. The general subject of grounding will be discussed in more detail later on in this chapter. However, any zone should have a single point ground. Each component should have at most one path to this ground. This path should be via the shortest length of wire possible. It is desirable that the ground point be, in actuality, a plane. If the zone has an individual shield, this shield should be bonded to the ground plane. If the zone does not have an individual shield, the ground plane should be bonded to the assembly chassis.

All penetrations of the zonal boundary must be designed to minimize the possibility of their introducing spurious transients into the zone. The most effective isolation techniques require the use of either an isolation transformer with a grounded Faraday Shield or a nonconducting coupling device. Either of these techniques may be used with a differential signaling process. Somewhat less effective, but nonetheless an acceptable method, is to use differential signaling (a differential amplifier and twisted pair cable) for interzone communication. In addition, coaxial connections between zones may be used. This requires a connection between zone shields or grounds which violates the single point ground concept. However, this is easily compensated for by the shielding provided by any reasonably effective coaxial cable shield. It should be noted that only the isolation transformer and the nonconducting coupling technique provide both ground isolation and protection against conducted transients.

It is desirable to have individual zones as autonomous as possible. This implies some sort of power supply regulation within the zone. If other considerations make it more feasible to design a system in which several separate zones are powered from one supply, then it is desirable to have a decoupling network within each zone so that the zone power is independent of EMP-caused transient fluctuations in the power levels. If the zones each have individual shields, then an over-shield should be provided for the powerline between the power supply and the individual zone. If an overall shield is not provided, the power should be provided using a twisted pair. The pair should be dressed down as close as possible to the ground plane throughout its travel.

3. SHIELDING

a. Shield Selection

The purpose of a shield when used as a subsystem assembly EMP hardening technique is to exclude the EMP generated transient fields. To be effective, the shield must have adequate structural integrity and all penetrations must be carefully controlled. It is desirable that each zone of protection have an individual shield. However, in some cases, overall system considerations may require that zones be nested, in which case the chassis or the outer zones may provide shielding for the inner zones.

The structural considerations in designing a shield are similar for all levels of subassembly complexity. That is, the procedures for designing the shield for a large electronics rack or bay are essentially the same as those applied to the shields for a very small circuit grouping. These are shield thickness, shield structural integrity, and shield penetrations. For the frequencies of concern in EMP interactions, any structurally sound metallic material will normally be thick enough to provide protective shielding. Thus, the larger racks and bays that are exposed to potentially

higher level incident fields will likewise require a heavier, thicker chassis for purely mechanical reasons. On the other hand, smaller shields located at the circuit level are exposed in general to much lower fields. At the same time, their remote location precludes any rough handling so that they will normally tend to be much thinner. In general, EMP hardening requires that primary consideration be given to providing shielding at the outermost level of any system, subsystem, or circuit. Of course, shielding is also desirable at the more internal zoning levels. However, the first consideration should always be given to maintaining the shielding integrity of the outer level. This will be most effective from an EMP standpoint and also usually more economical.

b. Structural Integrity

Cans, boxes or other shielding enclosures take many forms. The ideal continuously welded enclosure is almost never used because the equipment it encloses then becomes inaccessible. The real shield is, in almost every case, degraded by the presence of penetrations and various access doors. This gives rise to the necessity to consider the various techniques for maintaining shielding integrity in the presence of these obviously necessary degradations.

The mechanical assembly of a shield must specify clean metal-to-metal mating surfaces. Good contact between the surfaces should be assured by using either a continuous bond or at least using setscrews or rivets at close intervals. The maximum allowable distance between fasteners is 0.1 wavelength for the highest frequency. In preparing the surfaces for bonding, it should be recalled that many metallic oxides, particularly aluminum oxide, are nonconductive. In addition, the finishes commonly applied to metals, such as the iridite or anodizing applied to aluminum or the cadmium plating applied to iron and steel, are less conductive than the metals themselves. Care should be taken to assure that a clean, highly conductive surface exists at each metal-to-metal contact point.

When large openings are necessary for airflow, various forms of screens are used to break the large opening into a series of small openings that act as waveguides below cutoff. To be most effective, the intersections between openings must be fused. Three commonly used devices are honeycomb, perforated metal sheet, and wire mesh screen. Honeycomb is usually the most effective and offers the additional advantages of low resistance to airflow.

To allow for servicing, most shielding equipment has a bolted cover of some kind. Spacing between fasteners must be much closer as the material gets thinner because the surfaces buckle with respect to each other. For maximum EMP shielding protection, gasketing is used to ensure short interval metallic contact. Any of several types of conductive gaskets may be used to close the opening, but it must be thick enough and soft enough to fill in all irregularities. Where covers are to be removed and replaced, the gasket must be capable of return because the irregularity may be displaced with respect to a given set in the gasket. The contact pressure should be high enough to make adequate contact even when there is nonconducting corrosion present. In most cases, any of a number of gasketing materials will electrically satisfy the requirements. However, maintaining EMP shielding in service requires that the design be maintainable. Thus, it is important for the designer to consider mechanical suitability in specifying the overall EMP hardness.

Conductive paints or epoxies can sometimes be used where shielding is not very critical. Their use for EMP shielding is very limited since the amount of shielding that is available is quite small because their volume resistivities are usually on the order of 1000 times higher than copper. Another great disadvantage is that most of the best conductive paints must be baked at over 100 degrees centigrade to get the best electrical characteristics. This is obviously unattractive from the standpoint of the electronic gear contained inside.

c. Penetrations

In most applications, the greatest threat to shield degradation arises from the shield penetrations. These include interface wiring and the controls and meters provided external to the shield volume. Unless these are handled correctly they are likely to totally negate the effects of the shields. Large holes that cannot be screened should be designed as waveguide attenuators. This involves placing a relatively long metal cylinder behind the hole (inside the shield) and properly bonding the cylinder to the shield surface. The cylinder length should be at least three times the diameter of the hole. This waveguide attenuator is also suitable for installing dielectric control shafts. If it is necessary to provide access for a conductive control shaft, it must be connected to the outside of the shield by a gasket.

All unshielded wires that penetrate the shield should have the protection of filters and/or supression devices as discussed in the succeeding sections. These devices must be installed at the penetration point. Care should be taken to assure that the EMP currents shunted to ground by the protective devices do not couple to the equipment inside the shield. This is done by providing a separate shielded zone for the protective devices. This protective zone shield should be bonded to the overall shield at the penetration point.

Care must be taken in terminating the shields of cables that enter the enclosure. Basically, there are two types of shield terminations to be considered here; circumferential terminations and single wire terminations. Either of these types may be carried on into the enclosure to the circuit of interest after being bonded to the enclosure shield itself at the interface point. By far the best technique is to provide a continuous circumferential bond between the cable shield and the outside of the enclosure at

the interface point. This technique should be used for all shields exposed to high level EMP fields. The alternative technique in which the shield enters the enclosure on one pin of a multipin connector is suitable only for internal cable shields enclosed within an overall shield that is circumferentially bonded. In this case, it is permissible to bond the shield into the enclosure with a properly designed ground strap. However, even for internal cable shields it is much more desirable to provide a circumferential bond to the structure. The requirement to bond all cable shields to the outer enclosure at the penetration point is independent of whether they are continued into the enclosure where they must be bonded again to other zones which they penetrate.

4. GROUNDING

a. Grounding Requirements

From an EMP hardening standpoint, the major problems that arise in ground system design are the magnetic field pick-up associated with ground loops and the spurious signals that can be induced in the electronics due to common impedance between separate circuits. The problem of ground loops exhibits itself as EMP currents induced within the ground system itself. These currents can be coupled into the electronics and cause spurious responses or they can exhibit themselves as a voltage difference between two points that are theoretically at the same potential. In any case, the solution is to avoid ground loops by using a single point grounding system. It should be noted that the single point will in most cases be, in actuality, a plane.

The problem of common impedance between isolated systems results in a situation where EMP signals that are induced in one circuit (and which may be tolerable in that circuit) also exhibit themselves in another more susceptible circuit due to the fact that they share the same ground reference.

The solution to common impedance problems lies in proper choice of circuit zones as discussed previously and in providing low impedance ground paths so that the ground currents do not produce significant voltages.

There are a number of different ground plane designs that have been used in various systems, with varied degree of success. A ground plane is an instrument by which an attempt is made to reference a number of electrical units to the same potential to minimize the potential difference between the interface units. The ground plane may be considered as an equal potential plane except that no conductive material exists that has zero impedance. A ground plane can be a flat conductive area, interconnecting wires or tubular conductors to reference enclosures or chassis to essentially the same potential; or, it can be used as a separate reference for all signal circuitry. The dimensions of a ground plane in a system can become critical relative to the wavelengths used in the system or to the wavelength of the EMP generated signals. For this reason, the ground plane must be precisely defined. Many systems never consider the ground as a plane but only as a ground point. However, since all systems components must be connected to this ground point, the connecting network forms the ground plane.

The grounding schemes that have been widely used in various systems are the multipoint uncontrolled ground, the fishbone type ground, and the single point ground. Each of these leads to practical difficulties for complex systems. Any of the references for this section can be consulted for a detailed discussion of these problems. A recommended grounding system is shown in Figure 5-2. This system is based on implementation of the circuit zoning and shielding concepts previously described, and it exhibits some aspects of the multipoint, fishbone, and single point grounding systems. At each level of zoning, a ground plane is provided. This ground plane is connected to the components within the zone using a multipoint grounding system. Care must be taken to ensure that each component finds only one path to the ground plane. The ground plane is also bonded to the

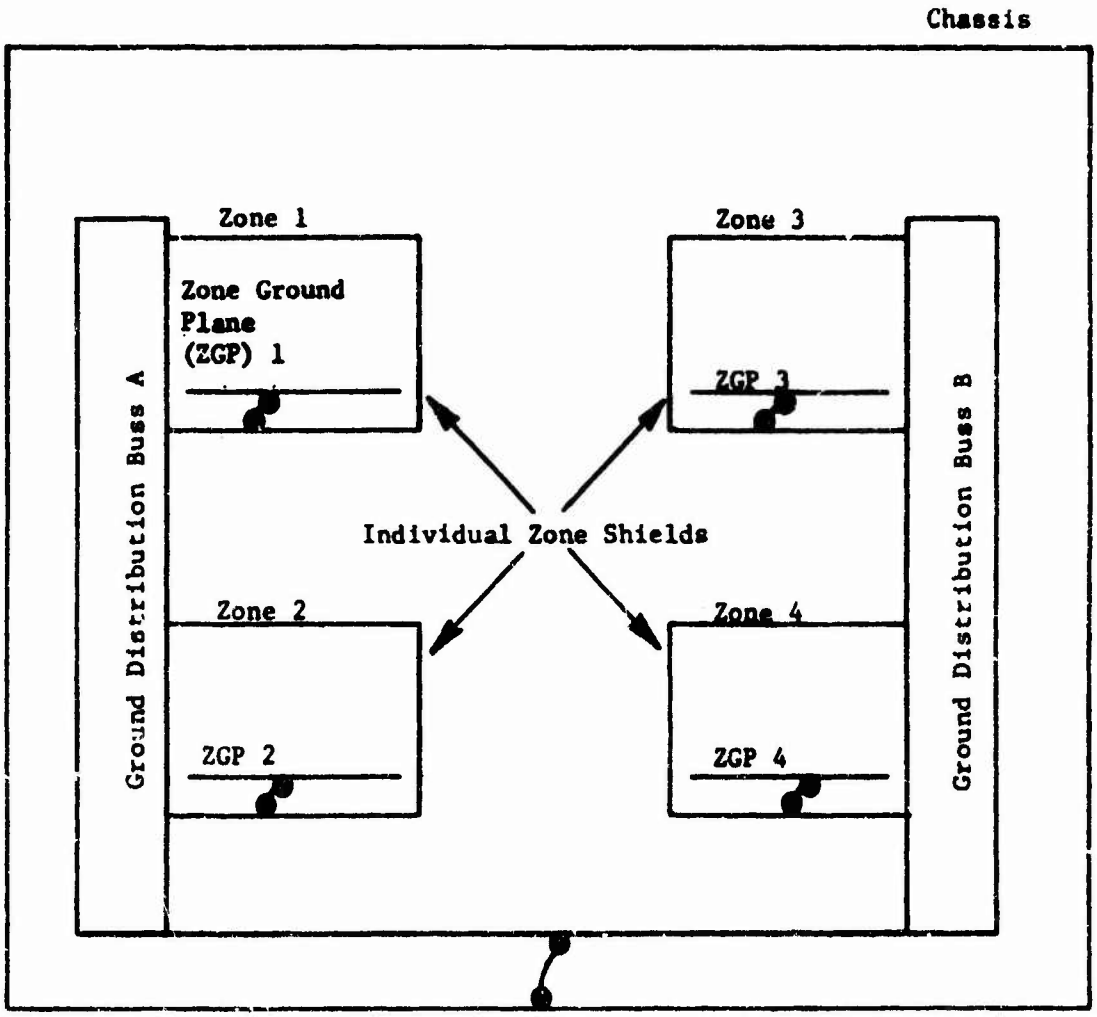


Figure 5-2. Grounding Technique

shield of the zone. Each zone within an overall chassis is then connected to the chassis ground plane. Depending on the complexity of the subsystem being designed, it may be necessary to provide more than one chassis ground plane. For example, in a rack, separate planes may be required for each drawer. At any rate, the chassis ground plane(s) are then bonded to the chassis.

While it is the intent of this chapter to establish guidelines only for individual units up to the chassis level, in considering grounding, one must consider the overall system. If the system being designed consists of a few relatively large chassis units such as electronics racks, these are then bonded to an overall ground plane (usually the floor). If the system consists of a number of smaller plug-in type chassis modules, each of these chassis are bonded to an overall ground plane using a large ground strap. If the system consists of a number of relatively small and widely distributed chassis units, such as might be encountered in a missile, the recommended procedure is to use the shields of the interconnecting cables to provide the ground connections. In this latter case, care must be taken to also provide a parallel path, separate from the signal ground, for power currents. The power system should be grounded to the chassis only at the supply end.

If the subsystem assembly designer has no control over the external ground system, he should use the ground system recommended above with the further provision that all inputs to his chassis should be isolated from the interconnecting cable. This isolation can either take the form of transformers or it may be based on electro-optical coupling or in some cases other decoupling techniques, for example, fluidic logic or dielectrically coupled motor-generator sets.

b. Bonding

The general solution for many of the common impedance problems lies in adequate bonding techniques. If a low impedance path is available throughout the ground plane, then common impedance problems will usually be negligible. However, to merely state that the bond must have low impedance is not sufficient. The dc resistance is not a satisfactory measure of the effectiveness of a bond. Impedance at the EMP frequencies is the key factor. There are only two general techniques for bonding: direct and indirect. Direct bonding is obtained by a direct contact between two metallic members. Indirect bonding is obtained by the use of a jumper between the two members. Direct bonding is always the preferred method but it is limited because it cannot be used except when two members can be joined permanently. Indirect bonding is a substitute when physical constraints make it impractical to use direct bonding.

Direct bonding is implemented by metal-to-metal contact between surfaces. The contact is maintained by a high uniform unit pressure. These direct bonds usually have a low dc resistance as well as a low impedance at EMP frequencies if of the proper configuration. Direct bonding includes both the thermal processes such as welding, brazing, and sweating, and mechanical processes such as the use of clamp fitting rivets or locked threaded devices. Direct metal-to-metal bonding joints that are held together mechanically are subject to deterioration. This deterioration includes oxidation, galvanic corrosion, and electrolysis. There is also the potential problem of migration of metals such as silver, zinc (galvanized iron), and aluminum. It is beyond the scope of this report to consider all of the potential problems and solutions related to bonding. The designer is referred to the references for further discussion.

There are a number of indirect bonding techniques commonly used. It should be recalled that in any case where a jumper is used to join two members, there is a possibility for resonant circuits to be formed at the EMP frequencies. The bonding jumper has an associated resistance, capacitance, and inductance that depend on the jumper material, its geometrical shape and length, and the physical configuration of the members being joined. The choice of an indirect bonding technique then involves design to minimize the effect of these possible resonances in the EMP portion of the spectrum and appropriate mechanical design to assure that the grounding system is not degraded by routine use to the point where the EMP hardening is compromised. Again, it is beyond the scope for this chapter to present a detailed discussion of how to calculate the resonant response of a bonding jumper. These techniques are presented in the references and should be consulted if indirect bonding techniques are being used.

SECTION III

HARDENING TECHNIQUES

Chapters 6 through 9 describe EMP hardening techniques. Many of these techniques create requirements that do not exist in the absence of EMP specifications. Although the techniques are applicable for other types of problems, they are not a necessary part of the design of electronic units. They treat considerations that arise due to specific EMP hardening requirements placed on the design of a specific piece of equipment.

Chapter 6 addresses techniques for suppression of transients resulting from EMP. These techniques are of primary importance in damage hardening. In upset hardening, suppression techniques are sometimes helpful but are also sometimes detrimental. Chapter 7 discusses the application of filtering to the problem of EMP hardening and specifically directs attention to problems in filter design that are of particular importance in EMP hardening. Chapter 8 discusses techniques for decoupling the electronic circuitry from the EMP interference. Both the filtering and decoupling techniques are relatively linear processing techniques and they are therefore useful in both upset and damage hardening. The last chapter in this section, Chapter 9, addresses techniques for error detection and various corrective measures that may be taken in response to the detection of errors. These techniques are of value in upset hardening, but not in damage hardening.

CHAPTER 6

SUPPRESSION DEVICES

1. INTRODUCTION

The electrical transients induced by EMP exhibit unique characteristics which differ considerably from transients associated with other phenomena such as lightning, switching, and circuit malfunctions. However, the suppression techniques developed to handle these transients, though not necessarily the same devices, can be applied for EMP damage protection. The suppression devices used for circuit level EMP protection are referred to as Terminal Protection Devices (TPD).

This chapter is devoted to a discussion of TPD functional parameters and response characteristics. These factors cannot be considered independent of systematic parameters such as cost, size, weight, complexity, reliability, and maintainability. Electrical and environmental compatibility and required protective efficiency must often be achieved within specified limits of one or more of the above systematic parameters. Trade-offs associated with both functional and systematic parameters are within the normal realm of designer responsibility.

The TPD systematic parameters are provided by the manufacturer and will not be treated in detail here. Some cost data are indicated in Table 6-1. Additional systematic parameters for some of the TPD's evaluated here are presented in Reference (8).

Table 6-1 summarizes various design parameters for a sample of TPD's evaluated in the preparation of this chapter, hereafter referred to as the evaluation samples. The identification of the TPD types and the definition of parameters are the subject of the following paragraphs. Table 6-1 is provided as a convenient summary.

TABLE 6-1

TPD PARAMETER MATRIX

DEVICE FAMILY	DEVICE TYPE	SPECIFIED V_{BO} VOLTS	AVERAGE MEASURED V_{BO} VOLTS	SPECIFIED P_{DISS} WATTS	F_{3dB} MHz	MAXIMUM NO FAIL PULSE CURRENT, AMPS	MAXIMUM PULSER OUTPUT NO FAIL ENERGY, JOULES	MINIMUM PULSER OUTPUT ENERGY TO FAIL, JOULES	AVG C_T, pF OR V_A @ T_A=10ns VOLTS	VOLTAGE AT 10 AMPS VOLTS	PROTECTIVE EFFICIENCY α	UNIT PRICE
Transzorbs	1N5555	33	34	1	2.9	357	24.2	26.8	2194 pF	-	8.85	4.50
	1N5558	191	200	1	13	213	.87	.93	489 pF	-	3.15	5.85
	1N5629A	6.5-7.1	6.6	1	.4	880	162	-	14892 pF	9	4.91	4.50
	1N5630A	7.1-7.9	7.7	1	.7	880	162	-	9621 pF	-	6.1	4.50
	1N5644A	28.5-31.5	28.5	1	2.6	430	34.3	37.3	2460 pF	31	2.9	4.50
	1N5648A	40.9-45.2	43.4	1	3.3	235	11.9	13.3	1908 pF	-	8.68	4.50
	ICT-5	6	6.6	1	.4	880	162	-	15062 pF	-	9.1	4.50
	GHV-8	5.4	5.4	1	71.5	880	162	-	89 pF	-	3.48	3.45
	GHV-14	9.4	9.3	1	124.5	880	162	-	51 pF	17	3.58	5.10
Diodes	1N2042-2	6	5.6	10	1.2	400	29.5	30.9	5267 pF	-	105	7.60
	1N2838	100	98	50	6.6	56	.9	1.6	957 pF	-	3.42	5.65
	1N2980	16	15.5	10	2.4	355	25.9	26.8	2683 pF	-	22.6	5.45
	1N2991	36	36.5	10	5.5	205	9.3	11	1159 pF	43	13.9	5.45
	1N3321	24	22	50	1.7	507	52.1	55.7	3683 pF	-	7.3	5.65
	1N3794	16	15.6	1.5	6.6	130	3.6	4.9	968 pF	-	11.5	3.75
	1N3798	24	24.9	1.5	9.5	320	1.4	15.4	669 pF	-	6.13	3.75
	1N4122	36	37.5	.25	47.5	80	.14	.16	134 pF	42	3.64	3.85
	1N5233	6	5.7	.5	11.4	153	.39	.42	557 pF	10	19.7	.67
	1N5359	24	23.3	5	9.9	105	2.3	3.2	640 pF	-	13.9	3.45
	1N5365	36	36.7	5	15.6	293	1.34	1.4	423 pF	-	12.8	4.00
	1N5378	100	89	5	29.4	147	.39	.42	216 pF	-	1.3	2.20
	1N4003 F/R	-	.4/563.4	-	119	680/2.3	91/.04	104/.05	53 pF	7	1060/-	.45
MOV'S	VP130A20	185	202	.85	4.5	827	162	-	1403 pF	300	.26	3.75
	VP150A20	211	225	.85	5.3	847	162	-	1191 pF	-	.31	3.83
	VP510820	720	825	.7	38	647	162	-	167 pF	1250	.02	5.35
	VP510840	720	837	.7	40.6	680	162	-	157 pF	-	.02	6.83
	VP10008160	1410	1400	1.3	33.6	570	162	-	189 pF	-	.006	24.00
Uni-Imps	UBO-.55	550	555	-	2109	880	162	-	.8 kV	23	4.1	25.00
	UBO-1	1000	1125	-	594	890	162	-	1.1 kV	-	2.43	25.00
	UGT-4	4000	4450	-	3975	880	162	-	4.5 kV	-	1.28	30.00
Spark Gaps	CG-75L	75	78	-	6115	880	162	-	.83 kV	17	9.17	1.99
	CG-470L	470	475	-	9830	880	162	-	1.5 kV	22	2.26	1.72
	CG-1000L	1000	1000	-	11564	880	162	-	3.5 kV	-	1.38	1.99
	SB-.55	550	557	-	10144	880	162	-	7.0 kV	53	.05	18.50
	SB-1	1000	1147	-	4051	880	162	-	2.4 kV	-	1.08	18.50
	SB-4	4000	4533	-	8379	880	162	-	7.2 kV	-	.003	18.50
NEON LAMPS	NE-2	110	72	-	13060	880	162	-	4.5 kV	-	.75	.15
	NE-86	55-90	70	-	9493	880	162	-	4.2 kV	-	.35	.35
	NE-51	110	72	-	3457	880	162	-	3.4 kV	230	.61	.38
SURGE ARRESTORS	LA921C-500	500	505	-	1530	880	162	-	1.85 kV	32	.38	23.18
	LA9B1C-1000	1000	1127	-	1519	880	162	-	1.9 kV	-	.5	23.18
	LA9B1C-4000	4000	4400	-	1761	880	162	-	5.8 kV	-	.07	23.18

2. TPD IDENTIFICATION

a. General

The design engineer defines his functional and system requirements and selects or designs a specific protection device for use in his subsystem. In an effort to assist the designer in these tasks, the advantages and limitations of specific terminal protection devices are examined in the following paragraphs.

The generic types of EMP protection devices that have been evaluated here are:

- Dielectric Breakdown Devices
- Semiconductor Breakdown Devices
- Nonlinear Resistors
- Combinations of the Above

This chapter will be devoted to a discussion of the functional characteristics, general physics of operation, general applications and evaluations of candidate device types in each of the above generic categories.

b. Dielectric Breakdown Devices

This device category includes spark gaps (either air or gas filled), neon lamps, surge arrestors, and special dielectric stimulated breakdown devices. The range of functional and system characteristics available in this family is extensive because of the broad product lines available from various manufacturers. Figure 6-1 illustrates the V-I characteristics of a typical gas-filled spark gap.

This curve shows the inherent hysteresis characteristic of gas-filled breakdown devices operated in the arc (high current) region. The curve also illustrates the bipolar nature of these devices which permits the use of a single device for protection from transients of either polarity.

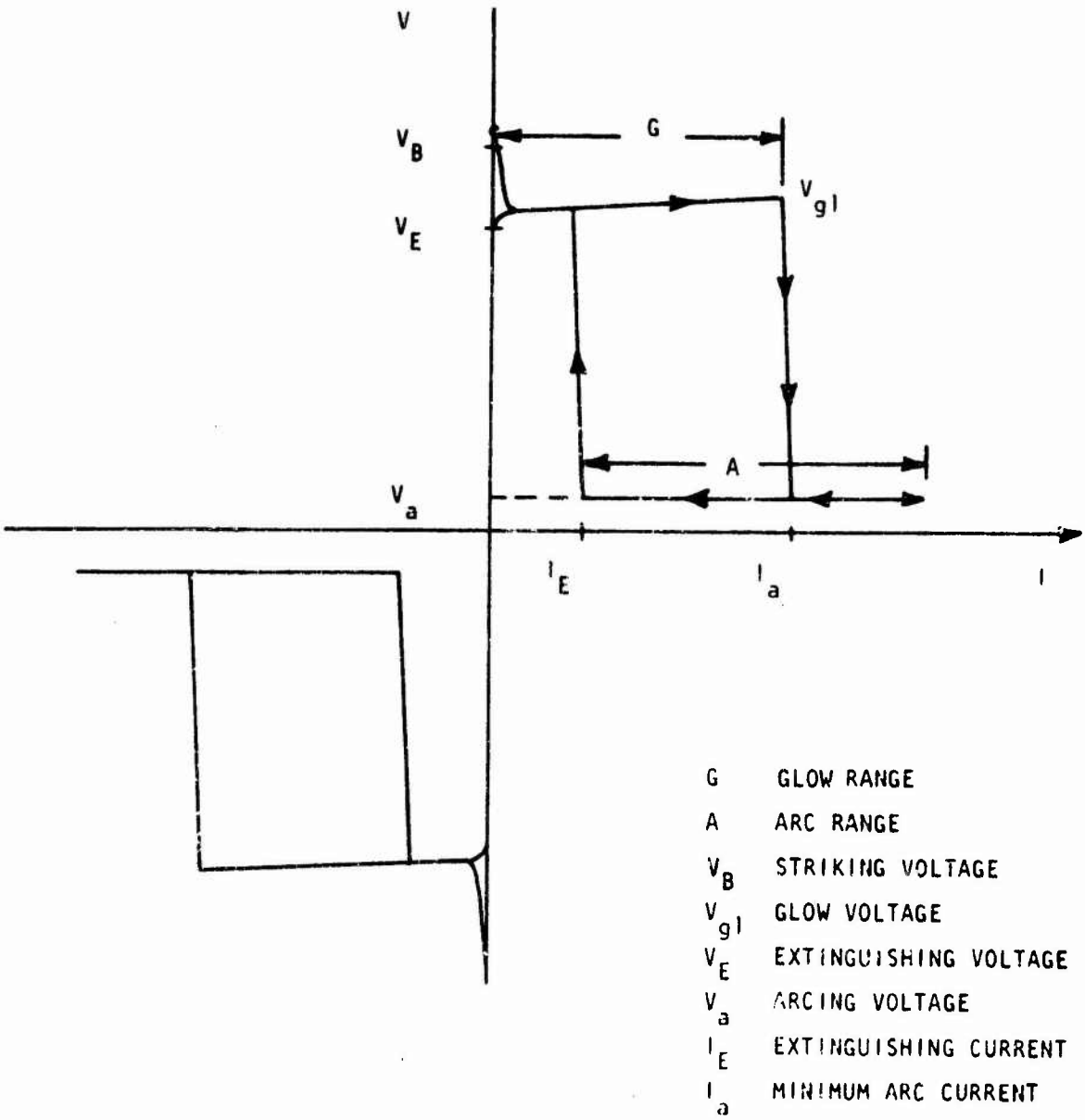


Figure 6-1. Typical Gas-Filled Spark Gap Characteristic Curve

The functional characteristics of dielectric breakdown devices are dependent on design factors including electrode size, shape, and composition, dielectric medium and gap pressure; and external factors such as the applied voltage-time waveshape, and the circuit configuration. A detailed discussion of the operation of dielectric breakdown devices is beyond the scope of this handbook. The reader is directed to consult References (1) and (2) for additional information.

(1) Gas-Filled Gaps and Neon Lamps

Gas-filled spark gaps are commercially available or can be designed and fabricated to meet almost any cost, size, weight, complexity, reliability, or maintainability requirement. This does not imply that optimum system parameters and functional parameters can necessarily be obtained concurrently.

Neon lamps are designed for operation in the glow mode rather than the arc mode. However, they are frequently used for overload protection and have the advantage of being inexpensive.

Five types of spark gaps and neon lamp devices were evaluated experimentally as discussed in Appendix A. These devices were selected to provide a representative cross section of dielectric breakdown devices. The selection was based on common usage and initial estimates of their potential EMP hardening value.

The five types of dielectric breakdown TPD's are:

- Signalite CG Series Spark Gap
- Signalite SB Series Spark Gap
- Signalite Uni-Imp* Spark Gap, UBD series

---

* Signalite Trade Name

- Chicago Miniature Neon Lamps (NE-2, NE-51, NE-86)
- Dale LA9 Series Surge Arrestor

The Signalite CGL series "Comm Gap" is a low voltage surge arrestor with welded leads and miniaturized ceramic construction. The devices designated CG-75L, 470L, and 1000L were evaluated. The CG series spark gaps are principally used in the telecommunications industry. The SB series device is a two-electrode spark gap (dc overvoltage protector) enclosed in a glass envelope. Devices designated SB-.55, 1.0, and 4.0 were used as evaluation samples. The Uni-Imp spark gaps are a special family (Reference (3)) which activate at their specified breakdown voltages for faster risetimes than the other conventional Signalite spark gaps. The UBD-.55, UBD-1.0, and UGT-4.0 Uni-Imps were evaluated.

The Chicago Miniature neon glow lamps are cold-cathode devices with two electrodes separated in a neon-filled envelope. The NE-2, NE-51, and NE-86 lamps were tested.

The Dale LA9 series surge arrestors are spark gaps hermetically sealed in a case with a single-ended flange mounting (Reference (4)). They function as a voltage-sensitive switch using a surge-charged coil in conjunction with a tapered spiral electrode. The arc is initiated between the top of the spiral electrode and a cylindrical electrode. The coil is energized, and produces a magnetic field which causes the arc to rotate down the tapered spiral, lengthening it to the breaking point before excess current is drawn. The spark gap atmosphere is pre-ionized by a radioisotope. Devices designated LA9BIC-500, 1 kV, and 4 kV were used as evaluation samples.

For each device type, at least three samples were evaluated during each parameter measurement. For further information on the spark gaps described above, the reader is directed to consult References (3) and (4).

(2) Dielectric Stimulated Breakdown Devices

The use of a solid dielectric to stimulate arc formation in spark gaps is being used in a new device under development by Sandia Laboratories (Reference (5)). This technique apparently yields lower breakdown and actuation voltages than conventional gas-filled gaps. Since these devices are commercially unavailable they are mentioned here for reference only.

c. Semiconductor Breakdown Devices

This category includes single junction semiconductor devices such as rectifier and Zener diodes. While other semiconductor devices such as PNPN devices and bipolar transistors may have application as surge arrestors, they will not be addressed here because of the limited pertinent data available.

As shown in Figure 6-2, diodes are basically polarized devices which exhibit an avalanche breakdown when the applied voltage in the reverse bias direction exceeds the device's specified breakdown or Zener voltage. Operated in an opposed series configuration (Figure 6-3), diodes can be used as effective suppression devices. Since Zener diodes are designed to operate in the breakdown mode, they usually can perform more effectively than signal diodes as terminal protection devices.

Figure 6-4 shows that rectifier diodes can also be employed as TPD's if connected in either an opposed parallel (OPD) or opposed series (OSD) configuration. This figure also shows bipolar stacking which may be used to reduce total network shunt capacitance. The OPD configuration is limited to use to where the normal operating signal is small (< 0.5 volt). However, due to a diode's high current handling capability in the forward bias direction, the OPD configuration can be very effective in EMP suppression.

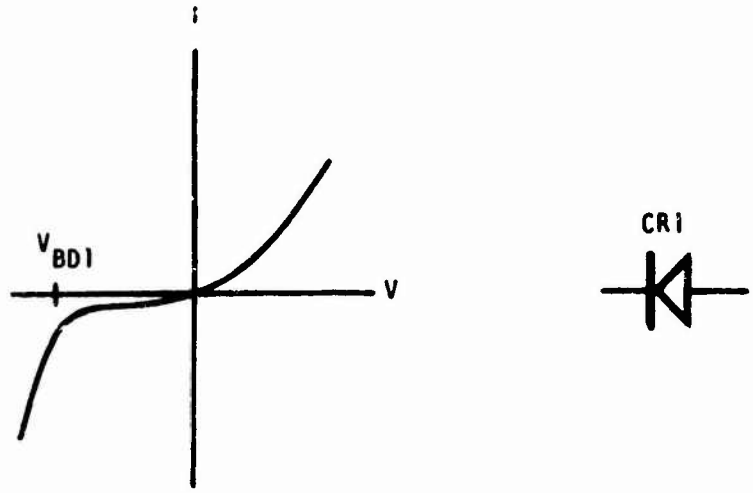


Figure 6-2. Single Diode I Characteristic Curve

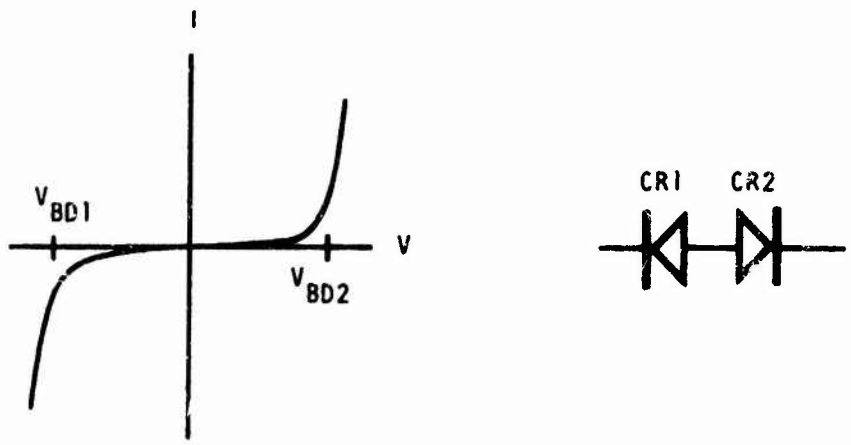


Figure 6-3. V-I Characteristics for Opposed Series Diodes

The selection of specific devices for use in the OSD configuration can make use of the Wunsch pulse power burnout model and associated data base as discussed in Chapter 4.

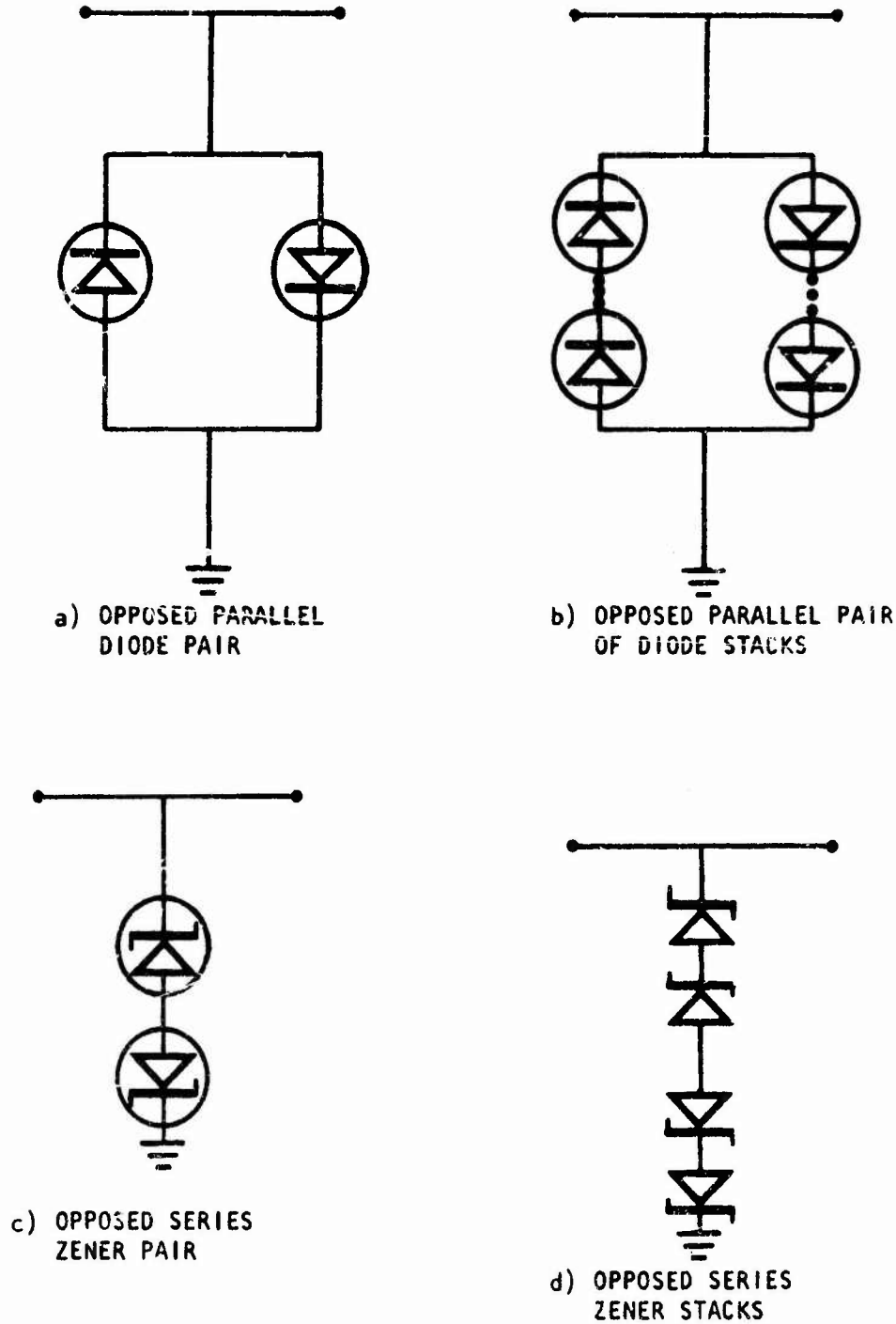


Figure 6-4. Basic Diode Configurations for Terminal Protection Applications

Several types of single junction semiconductor devices were evaluated experimentally as discussed in Appendix A. These devices were selected on a basis of providing various breakdown potentials and power dissipations. The selections were based on common usage and initial estimates of thin protection capability.

Twelve different types of Zener diodes and one signal diode were evaluated. These devices covered breakdown potentials from 6 to 100 volts and power ratings from .5 to 50 watts.

Nine types of TransZorbs* were also used as evaluation samples. The TransZorb is a specially packaged (hermetically sealed glass-to-metal) semiconductor breakdown device developed by General Semiconductor Industries in conjunction with Harry Diamond Laboratory. Four series types of TransZorbs were tested. The 5500 and 5600 series TransZorbs are defined as silicon transient suppressors designed to protect voltage-sensitive components in airborne systems. The GHV series TransZorbs are much lower in shunt capacitance, permitting applications across analog and digital input circuitry with minimum insertion loss. The ICT-5 TransZorb is specially designed for protection of 5 volt IC logic circuits.

At least three samples of each diode type were evaluated during each parameter measurement. Additional TransZorb information can be found in Reference (6).

d. Nonlinear Resistors

This device family includes nonlinear resistors (varistors) whose V-I characteristics can be described by the relationship:

---

* General Semiconductor Trade Name

$$I = KV^N$$

where N and K are device constants dependent on the varistor material.

This general expression also applies to linear resistors and Zener diodes. Some characteristic curves are compared in Figure 6-5 (Reference (7)).

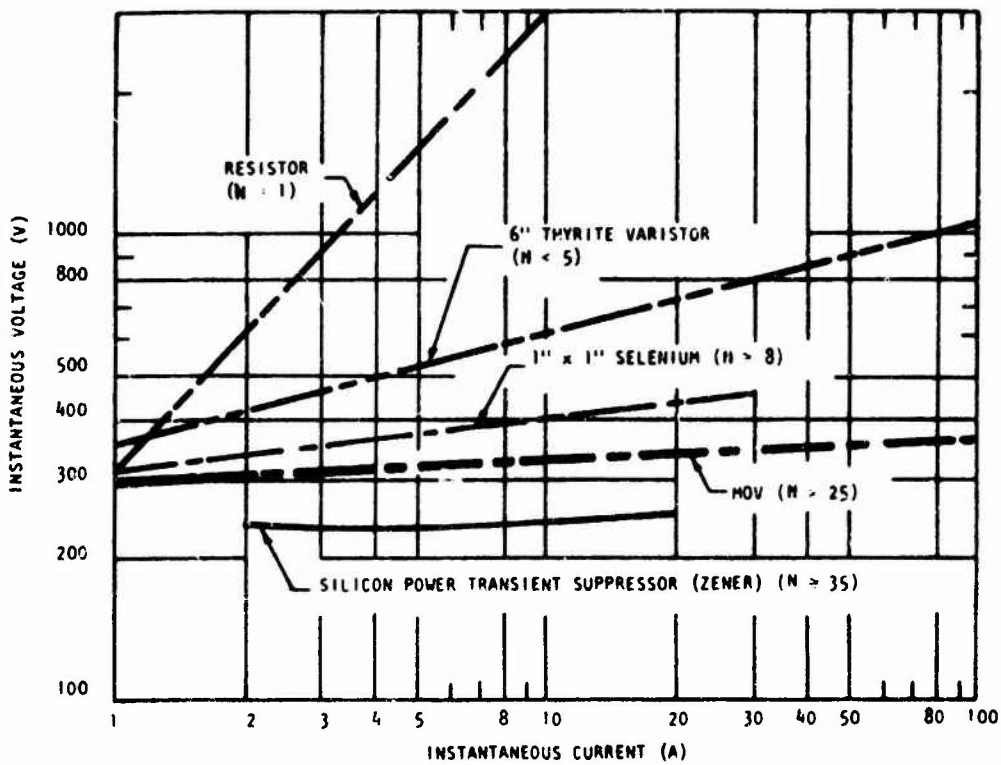


Figure 6-5. V-I Characteristics of Several Nonlinear TPD's

Since varistors constructed of silicon carbide or selenium generally exhibit responses that are too slow for use in EMP problems (Reference (8)), this discussion will concentrate on the metal-oxide varistor developed by General Electric. For slower EMP transient rise-times, varistors constructed of silicon carbide or selenium may be effective and should be considered for such applications. For transients

such as lightning, these latter devices may be superior due to their higher energy handling capabilities.

As in the case of spark gaps, the G.E. MOV* is inherently bipolar. It is a voltage dependent symmetrical resistor having a high degree of nonlinearity and a much higher energy storage and current handling capability than other semiconductor breakdown devices. The metal oxide (primarily ZnO and Bi_2O_3) varistor consists of a polycrystalline ceramic body, encapsulated in epoxy, with wire leads.

Five models of VP series MOV's were evaluated. These devices were selected on the basis of providing different voltage and energy ratings. The evaluation samples included RMS voltage ratings of 130, 150, 510, and 1000 volts and pulse energy ratings of 20, 40, and 160 joules. For additional GE-MOV information, the reader is directed to consult References (7) and (9).

e. TPD Combinations

Improvement in specific TPD functional parameters can be achieved by special design; that is, by combining two or more of the basic generic device types. Reference (10) presents the results of hybrid TPD tests. Examples of potential device combinations are shown in Figure 6-6. In addition, TPD's can be combined with other hardening techniques.

The use of TPD combinations results in improved performance but often results in higher costs, increased complexity, and uncertain reliability. These factors are obviously important considerations in the design engineer's selection of a particular TPD or combination of TPD's. For example, Figure 6-6c shows a combination of Zener and low capacitance

---

* Trademark of the General Electric Company

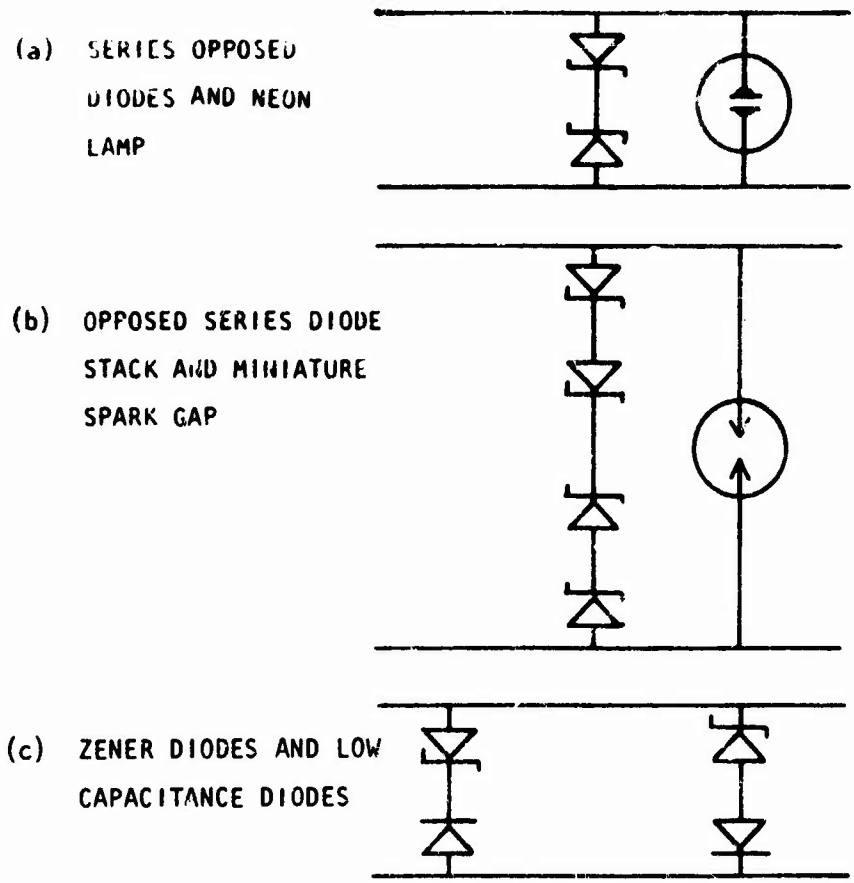


Figure 6-6. TPD Combination Networks

signal diodes. The Zener diodes provide controlled voltage, high current protection, while the diodes impair the insertion characteristics for low level signals.

3. RESPONSE CHARACTERISTICS

a. General

Little detailed data describing the response of TPD's to EMP related transients have been published. While many vendors publish specifications for TPD performance, there is no standardization of parameters and no available response modeling capability. This has resulted in a proliferation of test data that is sometimes conflicting but usually not directly comparable. The approach here has been to define a consistent set of parameters based on EMP hardening requirements and on measurable component parameters. These parameters were then used to evaluate a representative sample of TPD's.

Selection of a TPD for the specific hardening application requires consideration of three TPD characteristics.

- Standby Parameters
- Protection Parameters
- Failure Parameters

The detailed methodology used to determine circuit failure threshold is presented in the EMP Susceptibility Threshold Handbook (Reference (11)). It is assumed here that the designer has determined the failure threshold of the circuit to be protected. Given this information, the problem becomes one of selecting a TPD that does not degrade circuit performance in the standby mode and that produces acceptable transient suppression in the protection mode. The TPD itself must be able to withstand the multiple EMP transients without significant degradation.

b. Standby Parameters

The TPD must not degrade the normal circuit function. This implies careful consideration of the standby parameters of the TPD. Two insertion effects must be considered.

(1) Signal degradation due to shunt capacitance, C_T.

(2) Power loss due to leakage current.

Shunt capacitance is a problem primarily for circuits that carry data at relatively high frequencies. The measurement of shunt capacity for a wide variety of TPD types is presented in References (10) and (12) through (15). Assuming that the shunt capacitance is the controlling parameter, the following equation can be used to determine the cutoff (3 dB) frequency.

$$F_{3dB} = \frac{0.159}{C_T} \frac{R_S + R_L}{R_S R_L}$$

R_S and R_L are respectively the source and load resistances. The shunt capacity has been measured for each TPD evaluation sample as described in Appendix A. Table 6-2 presents these data and also presents the tabulation of cutoff frequencies (F_{3dB}).

For subsystems operating at high signal levels or for subsystems in which power conservation is critical (satellite applications), the leakage current in the standby mode may be important. This parameter is usually specified by the manufacturer and is quite small for almost all TPD types. Dielectric breakdown devices offer particularly low leakage currents.

TABLE 6-2

TPD STANDBY CHARACTERISTICS

DEVICE FAMILY	DEVICE TYPE	SPECIFIED V_{BD} VOLTS	AVERAGE MEASURED V_{BD} VOLTS	SPECIFIED P_{DISS} WATTS	F_{3dB} MHz	AVERAGE C_T pF
Transzorbs	1N5555	33	34	1	2.9	2194
	1N5558	191	200	1	13	489
	1N5629A	6.5-7.1	6.6	1	.4	14892
	1N5630A	7.1-7.9	7.7	1	.7	9621
	1N5644A	28.5-31.5	28.5	1	2.6	2460
	1N5648A	40.9-45.2	43.4	1	3.3	1908
	ICT-5	6	6.6	1	.4	15062
	GHV-8	5.4	5.4	1	71.5	89
	GHV-14	9.4	9.3	1	124.5	51
Diodes	1N2042-2	6	5.6	10	1.2	5267
	1N2838	100	98	50	6.6	957
	1N2980	16	15.5	10	2.4	2683
	1N2991	36	36.5	10	5.5	1159
	1N3321	24	22	50	1.7	3683
	1N3794	16	15.6	1.5	6.6	968
	1N3798	24	24.9	1.5	9.5	669
	1N4122	36	37.5	.25	47.5	134
	1N5233	6	5.7	.5	11.4	557
	1N5359	24	23.3	5	9.9	640
	1N5365	36	36.7	5	15.6	423
	1N5378	100	89	5	29.4	216
	1N4003 F/R	-	.4/563.4	-	119	53
MOV'S	VP130A20	185	202	.85	4.5	1403
	VP150A20	211	225	85	5.3	1191
	VP 510B20	720	825	.7	38	167
	VP510B40	720	837	.7	40.6	157
	VP1000B160	1410	1400	1.3	33.6	189
Uni-Imps	UBD-.55	550	555	-	2109	3
	UBD-1	1000	1125	-	594	10.7
	UGT-4	4000	4450	-	3975	1.6
Spark Gaps	CG-75L	75	78	-	6115	1
	CG-470L	470	475	-	9830	.65
	CG-1000L	1000	1000	-	11564	.55
	SB-.55	550	557	-	10144	.63
	SB-1	1000	1147	-	4051	1.6
	SB-4	4000	4533	-	8379	.76
NEON LAMPS	NE-2	110	72	-	13060	.49
	NE-86	55-90	70	-	9493	.67
	NE-51	110	72	-	3457	1.8
SURGE ARRESTORS	LA9B1C-500	500	505	-	1530	4.2
	LA9B1C-1000	1000	1127	-	1519	4.2
	LA9B1C-4000	4000	4400	-	1761	3.6

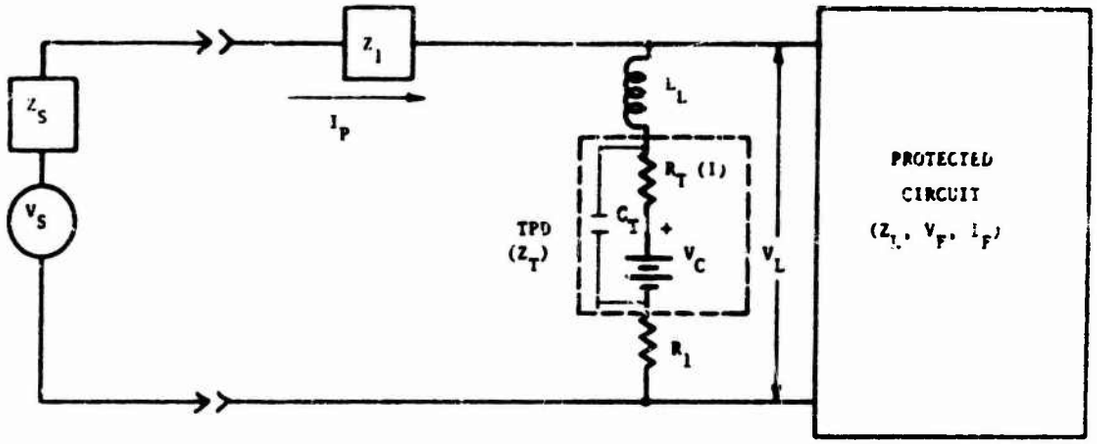
c. Protection Parameters

While the EMP induced transient produced at any given circuit interface may exhibit one of many waveform and amplitude characteristics, the pulse waveform shown in Figure 6-7 will be used for this discussion. This figure details the parameters that must be considered in evaluating the protective capability of a TPD in a specific situation. Note that once the TPD actuates, that is, enters the nonlinear conduction state, the incident waveform is distorted. The discussion presented here will attempt to limit this large number of parameters to a few measurable parameters by which data can be obtained and from which piecewise linear approximations can be derived.

TPD protection mode can be divided into three regions; turn-on, conduction, and turn-off. Estimating piecewise linear representation for each region requires synthesizing equivalent circuits and calculating the resultant input/output relationships. The results will be only approximate, however, they will generally compare with the accuracy of a corresponding susceptibility analysis.

(1) Turn-On

Since EMP presents relatively fast risetimes to the TPD, the normal turn-on characteristics may not be applicable for EMP hardening considerations. The actual voltage at which the TPD goes into conduction may be significantly higher than its rated voltage. This "overshoot" can be related to a number of physical parameters. For dielectric breakdown devices these include such parameters as the statistical delay time of the gap, the gap formative time, the package lead inductance, and the gap capacity. These parameters are all measurable but they are not routinely provided. To provide a quantitative indication for the turn-on characteristics of dielectric breakdown devices, a test was performed to measure actuation voltage as a function of time for varied values of dV/dt. The results of this test



V_S - EMP Transient Source
Z_S - Source Impedance
Z_l - Distributed Line Impedance
L_L - TPD Lead Inductance
$R_T(I)$ - TPD Effective Resistance
V_C - TPD Clamping Voltage
R_l - Discrete Current Limiting Resistor
Z_L - Load Impedance
V_F - Damage Threshold Voltage
I_F - Damage Threshold Current
I_P - EMP Surge Current
V_L - Circuit Input Voltage

C_T - Shunt Capacity
V_A - TPD Actuation Voltage
V_{BD} - TPD Static Breakdown Voltage
V_E - TPD Extinguishing Voltage
V_P - Peak EMP Voltage

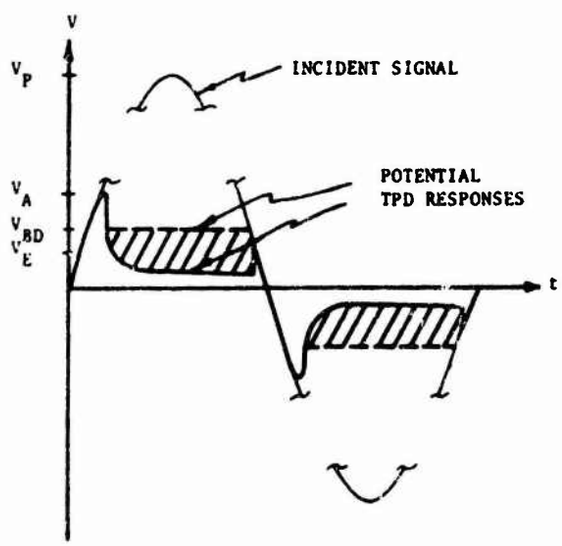


Figure 6-7. Typical Protection Configuration

are shown in Figures 6-8, 6-9, and 6-10. The TPD actuation voltage (V_A) was found to be very dependent on dV/dt with some devices such as the "SB" series gap demonstrating a particularly eratic behavior. This is apparently due to the fact that it is being operated near its mean statistical time.

The turn-on characteristics for semiconductors and non-linear resistors are determined by the device lag time, capacity, and lead inductance. The delay time is quite small for these type devices and does not significantly affect the turn-on chracteristics. Most of the semiconductors and variable resistors evaluated had relatively large capacities, so that the turn-on is determined by the time required to charge the capacity. In these cases the effect of lead inductance is to generate some minor high frequency noise related to the dV/dt of the incident pulse. For the lower capacitance devices, some overshoot attributed to lead inductance effects was observed. It should be noted here that some semiconductors and varistors show an apparent overshoot in specific test situations. However, this is attributed to the discharge of their capacitance into the bulk resistance of the device in the normal conduction mode, and not to any turn-on characteristic.

(2) Conduction

All TPD's present a nonlinear voltage-current (V-I) characteristic in the conduction mode. The evaluation sample was tested to obtain typical V-I relationships as described in Appendix A. The results are shown in Figures 6-11 and 6-12. It should be noted that this current-voltage relation is measured at the time when conduction is well established and the device has settled down to essentially a steady-state condition. The shape of the curves is generally similar, with the exception of the neon lamp. This device presents an unusual V-I characteristic because it is designed to operate in the glow mode rather than in the arc mode, and considerable current is required to force it into the arc mode.

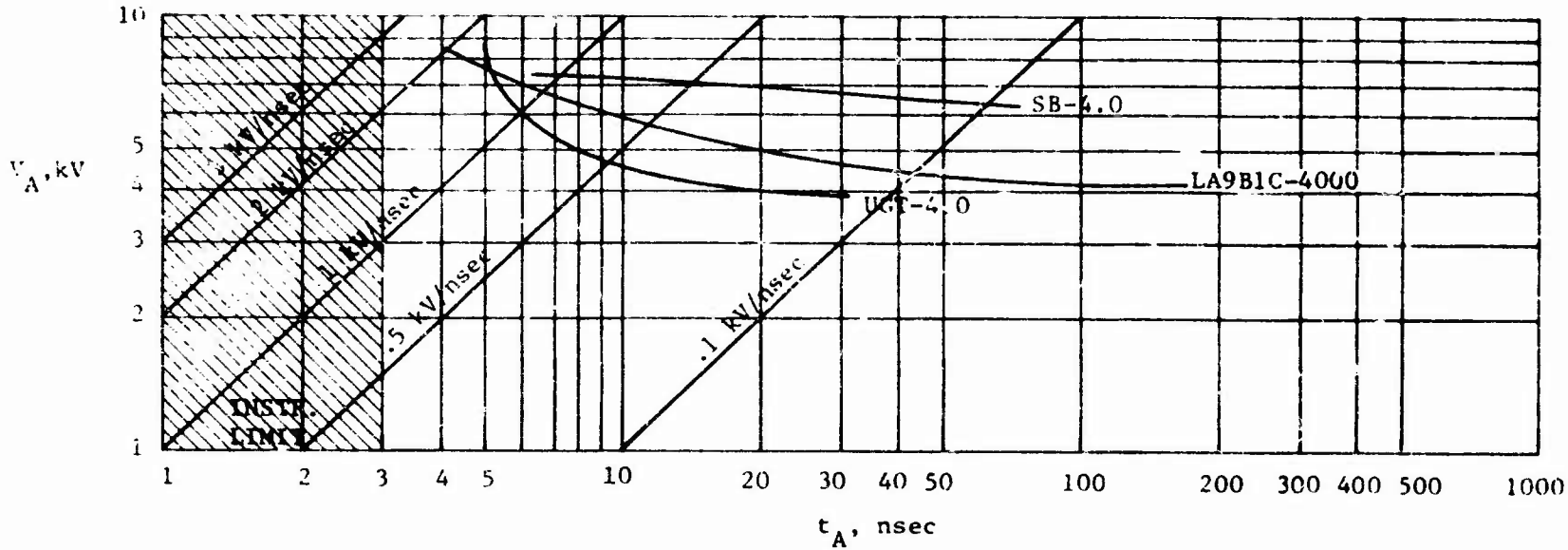


Figure 6-8. Actuation Voltage Versus Time for Several 4000-Volt Dielectric Breakdown TPD's

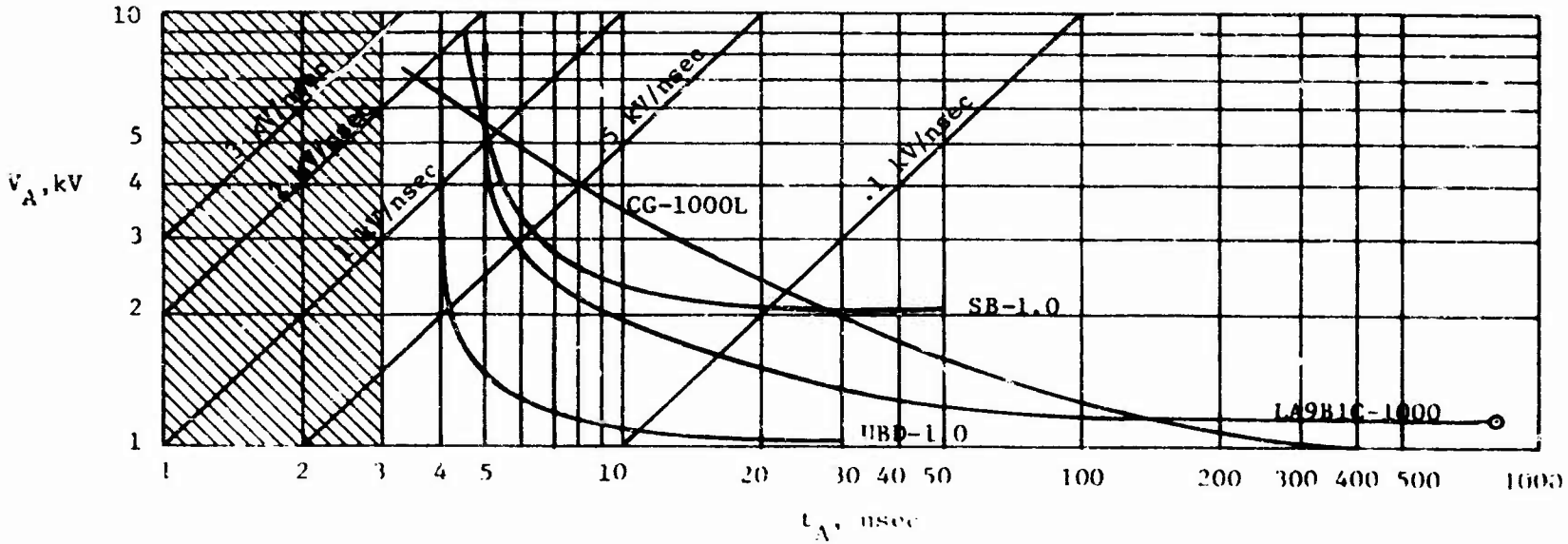


Figure 6-9. Actuation Voltage Versus Time for Several 1000-Volt Dielectric Breakdown TPD's

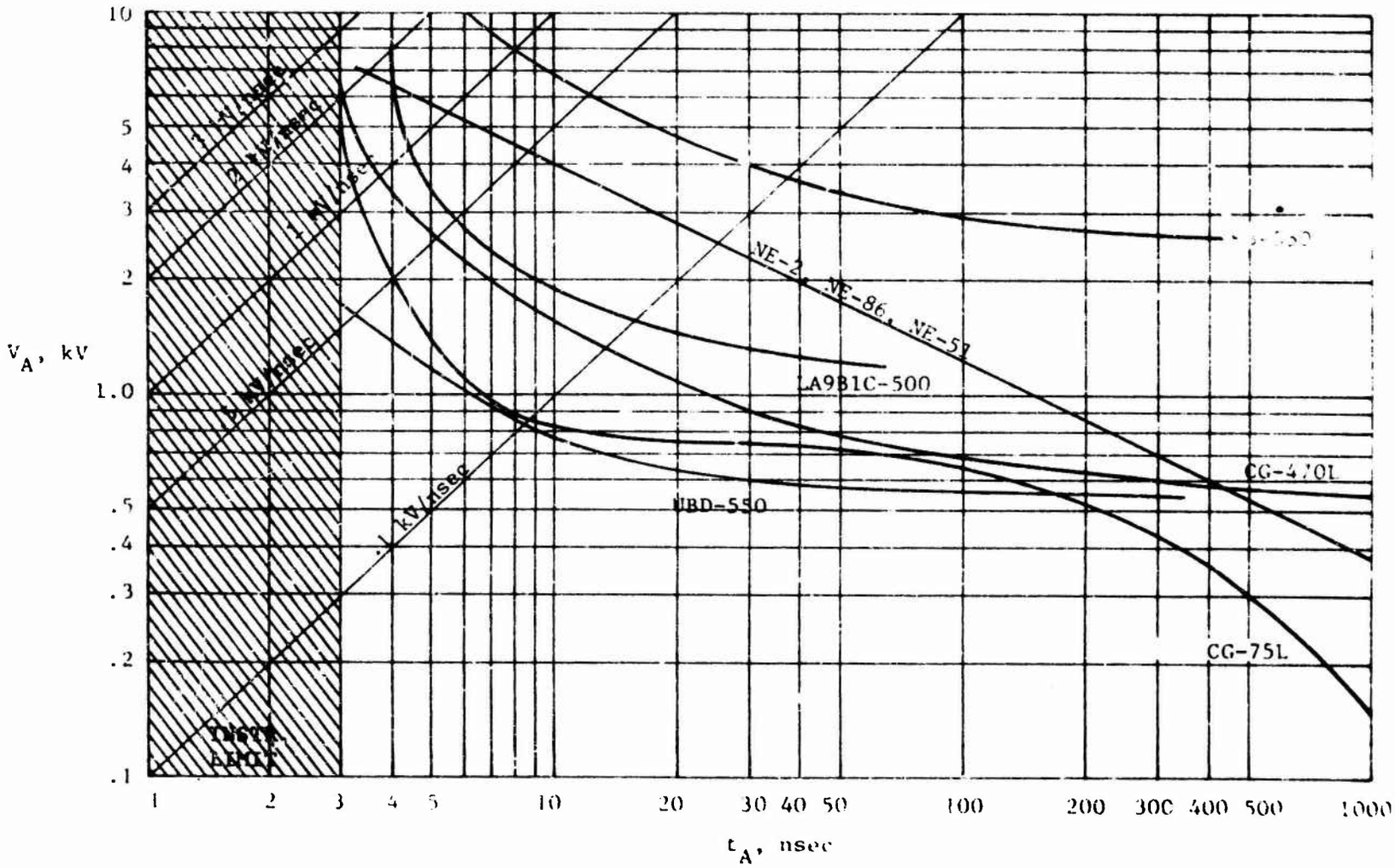


Figure 6-10. Actuation Voltage Versus Time for Eight Different Types of Lower Voltage Dielectric and Semiconductor TPD's

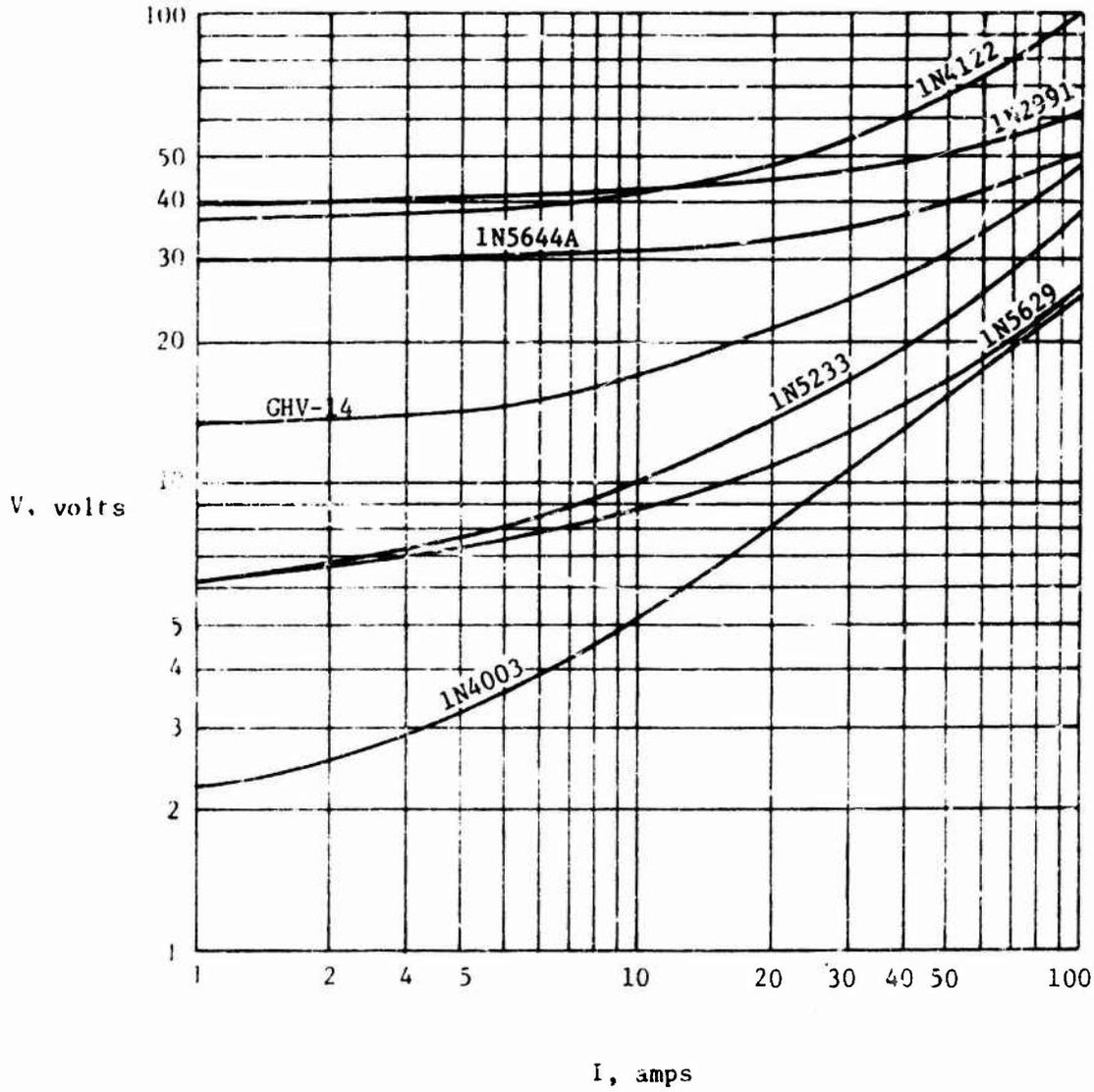


Figure 6-11. V-I Charateristic Curves for Some Zener Diodes, TransZorbs and a 1N4003 Rectifier

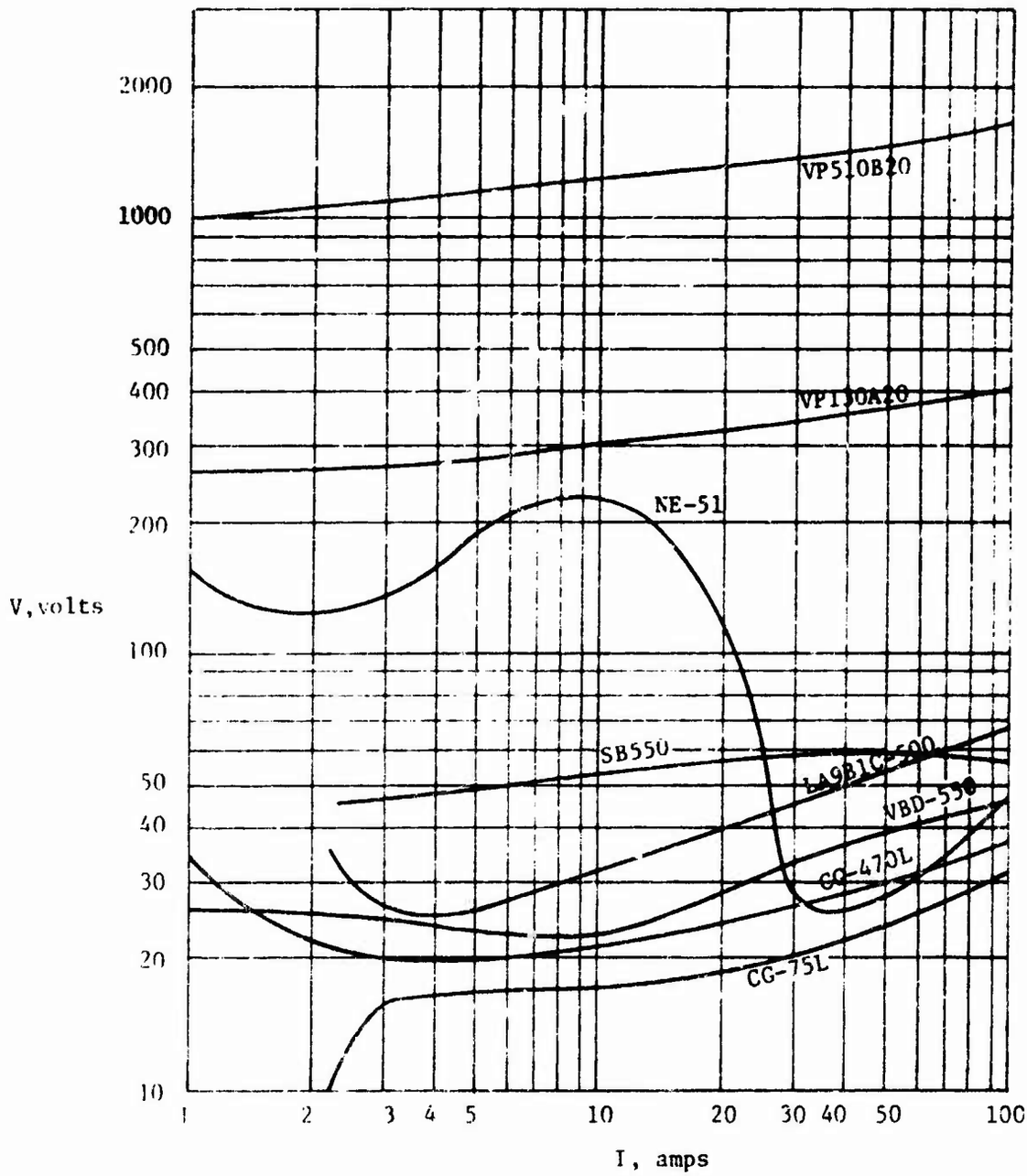


Figure 6-12. V-I Characteristic Curves for Some MOV's and Dielectric Breakdown TPD's

(3) Turn-Off

In some applications, the turn-off characteristics of a TPD can be very important. This is particularly true when a steady-state signal is present on the protected line along with the EMP signal. Either dc or continuous RF signals can maintain some TPD's in the conductive state so that the circuit remains interrupted until the steady-state signal is removed. Another turn-off parameter that must be considered is the inductive surge that some TPD's exhibit as they return to the standby mode. In specific applications, this surge signal could become significant in determining the overall effectiveness of the TPD.

No data are available to evaluate TPD turn-off parameters. Until such data become available, each application of a TPD must be evaluated separately. Since the recovery is necessarily related to some of the same physical parameters that govern turn-on and conduction, it is sometimes possible to infer turn-off characteristics from the turn-on and conduction characteristics. Since the evaluation of TPD turn-off is dependent on circuit configuration, this evaluation must be performed at the circuit or subsystem level.

(4) Protective Efficiency

The preceding paragraphs provide a detailed discussion of response characteristics and provide considerable data. However, it is convenient to postulate a parameter that can be used to evaluate a wide variety of TPD's quantitatively. Clearly if this is to be done, the parameter must be somewhat arbitrary since the different TPD's possess different physical principles of operation and different power and breakdown voltage ratings.

The definition of the protective efficiency parameter, α, is based on the energy delivered to a protected 50 Ω load by a 5 kV, 1 usec rectangular pulse.

Specifically:

$$\alpha = \frac{10^{-3}}{E_L \text{ (joules)}}$$

where E_L is the energy dissipated in the 50 Ω load. The constant in the numerator, one millijoule, normalizes the protective efficiency to a unity Wunsch damage constant for a 1 μs pulse. This definition is arbitrary, but convenient. Table 6-3 presents the measured protected efficiency for the TPD evaluation sample from the test described in Appendix A. The protective efficiency ranges over almost six orders of magnitude. Note that a protective efficiency of one would provide protection with a 20 dB safety factor to a circuit with a damage constant of 0.1 for the given test configuration. In fact, the value of protective efficiency obviously depends to a large extent on the test configuration. A different value of pulse voltage, duration, or of load impedance, would change not only the value obtained for protective efficiency, but the order of relative ratings as well. The real value of the protective efficiency lies in the fact that it provides a quick comparison between various TPD's for a defined set of conditions. It should be noted that the protective efficiency tends to vary inversely with TPD rated breakdown voltage. Thus, the TPD which presents the highest protective efficiency, the 1N4003, is a forward biased signal diode that cannot be used for signal levels above about 100 mV.

Table 6-3 also presents information on TPD turn-on and conduction parameters. The voltage-current characteristic is indicated by presenting the device voltage for a 10 amp pulse. The turn-on parameter is indicated by listing the TPD capacitance for semiconductors and nonlinear resistors, and the actuation voltage at 10 ns for dielectric breakdown devices. These values are provided only for quantitative comparison. The detailed graphical presentations should be reviewed for actual application information.

TABLE 6-3

TPD PROTECTIVE EFFICIENCY

DEVICE FAMILY	DEVICE TYPE	SPECIFIED V_{BD} VOLTS	AVERAGE MEASURED V_{BD} VOLTS	SPECIFIED P_{DISS} WATTS	AVG C_T, pF OR V_A @ T_A=10ns VOLTS	VOLTAGE AT 10 AMPS VOLTS	PROTECTIVE EFFICIENCY α
Transzorbs	1N5555	33	34	1	2194 pF	-	8.85
	1N5558	191	200	1	489 pF	-	3.15
	1N5629A	6.5-7.1	6.6	1	14892 pF	9	4.81
	1N5630A	7.1-7.9	7.7	1	9621 pF	-	6.1
	1N5644A	28.5-31.5	28.5	1	2460 pF	31	2.8
	1N5648A	40.9-45.2	43.4	1	1908 pF	-	8.66
	FCT-5	6	6.6	1	15062 pF	-	9.1
	GHV-8	5.4	5.4	1	89 pF	-	3.48
	GHV-14	9.4	9.3	1	51 pF	17	3.58
Diodes	1N2047-2	6	5.6	10	5267 pF	-	105
	1N2838	100	98	50	957 pF	-	3.42
	1N2980	16	15.5	10	2683 pF	-	22.6
	1N2991	36	36.5	10	1159 pF	43	13.9
	1N3321	24	22	50	3683 pF	-	7.3
	1N3794	16	15.6	1.5	968 pF	-	11.5
	1N3798	24	24.9	1.5	669 pF	-	6.13
	1N4127	36	37.5	.25	134 pF	42	3.64
	1N5233	6	5.7	.5	557 pF	10	19.7
	1N5359	24	23.3	5	640 pF	-	13.9
	1N5365	36	36.7	5	423 pF	-	12.8
	1N5378	100	89	5	216 pF	-	1.3
	1N4003 F/R	-	.4/563.4	-	53 pF	7	1060/-
MOV'S	VP150A20	185	202	.85	1403 pF	300	.26
	VP150A20	211	225	.85	1191 pF	-	.31
	VP510B20	720	825	.7	167 pF	1250	.02
	VP510B40	720	837	.7	157 pF	-	.02
	VP1000B160	1410	1400	1.3	189 pF	-	.006
Uni-Imps	UBD-.55	550	555	-	.8 kV	23	4.1
	UBD-1	1000	1125	-	1.1 kV	-	2.43
	UGT-4	4000	4450	-	4.5 kV	-	1.28
Spark Gaps	CG-75L	75	78	-	.83 kV	17	9.17
	CG-470L	470	475	-	1.5 kV	22	2.26
	CG-1000L	1000	1000	-	3.5 kV	-	1.38
	SB-.55	550	557	-	7.0 kV	53	.05
	SB-1	1000	1147	-	2.4 kV	-	1.08
	SB-4	4000	4533	-	7.2 kV	-	.003
NEON LAMPS	NE-2	110	72	-	4.5 kV	-	.75
	NE-86	55-90	70	-	4.2 kV	-	.35
	NE-51	110	72	-	3.4 kV	230	.61
SURGE ARRESTORS	LA9B1C-500	500	505	-	1.85 kV	32	.38
	LA9B1C-1000	1000	1127	-	1.9 kV	-	.5
	LA9B1C-4000	4000	4400	-	5.8 kV	-	.07

d. Failure Parameters

In addition to providing protection to a specific circuit, the TPD must itself not suffer degradation from the EMP transient. The TPD evaluation sample was tested as described in Appendix A to determine individual device failure characteristics. The results are presented in Table 6-4. This table presents maximum no-fail pulse current, and maximum no-fail pulser energy for all devices; and minimum failure pulser energy for those devices that could be failed using the available equipment. Note that the energy listed represents the total energy stored in the pulse generator and not the energy dissipated by the device. This is important to recognize, since dielectric breakdown devices dissipate very little energy compared to the semiconductor devices and nonlinear resistors.

It can be seen in Table 6-4 that many of the devices could not be failed using the available equipment. The maximum no-fail current was determined primarily by the voltage-current characteristics of the devices themselves rather than by the pulse generator. The maximum pulse applied was 10 kV with an 11 Ω source impedance. One immediate conclusion from Table 6-4 is that the wide variety of TPD's available can provide protection, and at the same time survive worst case EMP currents.

5. REFERENCES

The following references were used in the preparation of this chapter:

(1) Cobine, J. D., Gaseous Conductors, Theory and Engineering Applications, Dover Publications, Inc., 1958, p. 606.

(2) Miller, W. G., Using and Understanding Miniature Neon Lamps, Howard W. Sams and Co., Inc., Indianapolis, Indiana, 1969.

(3) Basarian, A. V., "Gas Discharge Devices for Use in Transient Voltage Protection," Signalite Internal Report, Date Unknown.

TABLE 6-4

TPD FAILURE PARAMETERS

DEVICE FAMILY	DEVICE TYPE	SPECIFIED V_{BD} VOLTS	AVERAGE MEASURED V_{BD} VOLTS	SPECIFIED P_{DISS} WATTS	MAXIMUM NO FAIL PULSE CURRENT, AMPS	MAXIMUM PULSER OUTPUT NO FAIL ENERGY, JOULES	MINIMUM PULSER OUTPUT ENERGY TO FAIL, JOULES
Transzorbs	IN5555	33	34	1	357	24.2	26.8
	IN5558	191	200	1	213	.87	.93
	IN5629A	6.5-7.1	6.6	1	880	162	-
	IN5630A	7.1-7.9	7.7	1	880	162	-
	IN5644A	28.5-31.5	28.5	1	430	34.3	37.3
	IN5648A	40.9-45.2	43.4	1	235	11.9	13.3
	ICT-5	6	6.6	1	880	162	-
	GHV-8	5.4	5.4	1	880	162	-
	GHV-14	9.4	9.3	1	880	162	-
Diodes	IN2642-2	6	5.6	10	400	23.5	30.9
	IN2838	100	98	50	56	.9	1.6
	IN2980	16	15.5	10	355	25.9	26.8
	IN2991	36	36.5	10	205	9.3	11
	IN3321	24	22	50	507	52.1	55.7
	IN3794	16	15.6	1.5	130	3.6	4.9
	IN3798	24	24.9	1.5	320	1.4	15.4
	IN4122	36	37.5	.25	80	.14	.16
	IN5233	6	5.7	.5	153	.39	.42
	IN5359	24	23.3	5	105	2.3	3.2
	IN5365	36	36.7	5	293	1.34	1.4
	IN5378	100	89	5	147	.39	.42
	IN4003 F/R	-	.4/563.4	-	680/2.3	91/.04	104/.05
MOV'S	VP130A20	185	202	.85	827	162	-
	VP150A20	211	225	.85	847	162	-
	VP510B20	720	825	.7	647	162	-
	VP510B40	720	837	.7	680	162	-
	VP1000B160	1410	1400	1.3	570	162.	-
Uni-Imps	UBO-.55	550	555	-	880	162	-
	UBD-1	1000	1125	-	890	162	-
	UGT-4	4000	4450	-	880	162	-
Spark Gaps	CG-75L	75	78	-	880	162	-
	CG-470L	470	475	-	880	162	-
	CG-1000L	1000	1000	-	880	162	-
	SB-.55	550	557	-	880	162	-
	SB-1	1000	1147	-	880	162	-
	SB-4	4000	4533	-	880	162	-
NEON LAMPS	NE-2	110	72	-	880	162	-
	NE-86	55-90	70	-	880	162	-
	NE-51	110	72	-	880	162	-
SURGE ARRESTORS	LA9B1C-500	500	505	-	880	162	-
	LA9B1C-1000	1000	1127	-	880	162	-
	LA9B1C-4000	4000	4400	-	880	162	-

(4) Dale Electronics, Inc., LA9 Series Specification Sheet, Date Unknown.

(5) Cooper, J. A. and Allen, L. J., Lightning Arrestor-Connector Feasibility Study, SC-RR-71 0180, Sandia Laboratories, April 1971.

(6) General Semiconductor Industries, Inc., GHV Surge Suppressor Specification Sheet, dated 1972; ICT-5 Transzorb Specification Sheet, April 1971; Transzorb 1N5500 and 1N5600 Series Specification Sheets.

(7) Golden, F. B. and Fox, R. W., "G.E.-MOV Varistors Voltage Transient Suppressors," General Electric Company Application Note 200.70, December 1971.

(8) Bascou, V. A., et.al., "Final Report on the Evaluation of Surge Protection Devices for EMP Hardening Applications," AFWL Contract No. F29601-72-C-0037, Autonetics Document No. C72-712/201, July 1972.

(9) Harnden, J. D. Jr., et.al., "Metal-Oxide Varistor: A New Way to Suppress Transients," Electronics, October 1972.

(10) Durgin, D. L., Jenkins, C. R., and Rimbert, G. J., "Methods, Devices, and Circuits for EMP Hardening of Army Electronics," Contract No. DAAB07-71-C-0275, BDM/A-119-72-TR, July 1972.

(11) Boeing Company, The, "EMP Susceptibility Threshold Handbook," AFWL Contract No. F29601-72-C-0028, Boeing Document No. D224-10013-1, July 1972.

(12) Singletary, J. B., Cline, R. L., and Hasdal, J. A., "Methods, Devices, and Circuits for the EMP Hardening of Army Electronics," ECOM-0085-1, August 1970.

(13) Singletary, J. B., Cline, R. L., and Hasdal, J. A., "Methods, Devices, and Circuits for the EMP Hardening of Army Electronics," ECOM-0085-2, March 1971.

(14) Singletary, J. B., and Hasdal, J. A., "Methods, Devices, and Circuits for the EMP Hardening of Army Electronics," ECOM-0085-3, June 1971.

(15) Singletary, J. B. and Hasdal, J. A., "Methods, Devices, and Circuits for the EMP Hardening of Army Electronics," ECOM-0085-F, June 1971.

(16) Joslyn Electronic Systems, "The Fast Clamp-Down of Transients in a Radar Modulation," Application Note, October 1969.

(17) Defense Civil Preparedness Agency, "EMP Protection for Emergency Operating Centers," Document No. TR-61A, July 1972.

(18) Siemens Corporation, "Gas Filled Surge Voltage Protectors," Short Form Catalogue and Application Note, Date Unknown.

(19) Winters, R. D. and Gadberry, R. E., "Feasibility Study Into the Use of Transzorb For EMP Suppression," USAMERDC Contract No. DAAK02-71-C-0127, General Semiconductors Industries, Inc., November 1971.

CHAPTER 7

FILTERS

1. INTRODUCTION

In many cases filters can be used to harden circuits and subsystems to EMP transients. Since filters are frequency selective, the normal signal frequencies must be significantly different from the important EMP frequencies, to achieve optimum filter usage. Perhaps this is the greatest restriction in the use of filters for EMP hardening. If this restriction can be met, the filter offers significant advantages. These include low cost for simple filters, and a linear response that allows the normal signal to pass at the same time that EMP transients are being rejected. Thus, the EMP event results in no loss of data.

The use of electrical filters as a means of eliminating out-of-band interference components can be an effective technique for both damage and upset hardening. The bandwidth associated with EMP interferences is often relatively narrow at the subsystem interface level due to the nature of the system response of aeronautical systems. Provided that the EMP interference spectrum is not modified by nonlinear devices, used for damage hardening, the selection of a filter for use with a given subsystem of known operating characteristics is relatively straightforward. If the EMP interference frequency spectrum is altered by some type of nonlinear device, the selection of an effective filter design may be complicated considerably.

The design of filters is routine in electronic design and is well treated in standard texts. Thus, there is no need to discuss the normal design parameters and equations here. This chapter reviews filter design considerations unique to the application of filters to EMP hardening.

In addition, some detail is provided on ferrite beads and filter pin connectors which offer special attraction for EMP hardening.

2. FILTER RESPONSE CHARACTERISTICS

The parameters of interest for EMP hardening design include the normal design parameters plus added parameters to describe nonlinear responses and failure. These parameters are reviewed briefly in the following discussion.

The first consideration in filter design is bandwidth. This includes definition of the pass band and the roll-off in the reject band. The ideal design criteria are to pass the normal signal with no attenuation or phase shift and to totally reject the EMP transient. The practical filter is usually a compromise that trades the cutoff frequency and the roll-off against other design parameters, such as cost. In specifying filters for EMP hardening, it is important to recall the fact that bandwidth and roll-off are dependent on the filter source and load impedances. The EMP response of a subsystem or circuit is often dominated by stray reactances. In these cases, the source and load impedances may vary considerably from the values determined from circuit schematics. As a result, experimental work may be required to define the impedances.

Where large voltages or currents are expected, the designer must consider possible nonlinear filter responses. Two nonlinear parameters will be considered here: arcing voltage and saturation current. Both are undesirable and should be eliminated in the design. All filter elements are susceptible to arcing. Thus it is important to determine the arcing voltage at EMP frequencies. Arcing voltage must be determined both terminal to case (ground) and terminal to terminal. This information is not usually available explicitly and must be deduced from rated working voltage or determined experimentally. It should be noted

that arcing itself is not always detrimental to circuit protection. An arc from filter input to ground may act as a suppression device and protect both the filter and the circuit. However, arcing can cause damage to filter elements or to other unprotected circuits. Filters that use permeable elements to achieve inductive or resistive characteristics are subject to saturation. When saturation occurs, the inductance or resistance decreases rapidly and the filter bandwidth and roll-off are changed. Saturation is dependent on both current and frequency. As in the case of arcing, saturation levels are not generally well specified, and must be evaluated experimentally.

The final filter parameter to be considered is damage. Filter damage is catastrophic both to the filter itself and to the line being protected. If the filter fails as an effective series short, then the circuit is unprotected. If the filter fails as an effective series open, then the circuit is protected but no data can be transmitted. Since most filters are composed of individual components, the information of Chapter 4 should be reviewed as part of any filter design.

3. FILTER DISCUSSION

A wide range of filter types are available in the selection of a filter for EMP hardening. The size, electrical parameters and complexity range from a simple capacitive shunt filter to large multi-section units with matching networks. The advantages and disadvantages of several types will be discussed in this chapter.

The filter types most likely to find practical application for subsystem level hardening are:

- Discrete R, L, C Filters
- Ferrite Beads
- Filter Pin Connectors
- Distributed Passive Filters
- Active Filters
- Electromechanical Filters

a. Discrete R, L, C Filters

The most ubiquitous filter type is the discrete filter composed of individual resistors, inductors, and/or capacitors. They can be either reflective or dissipative filters and have the distinct advantage of general familiarity. They also permit implementation of any of the functional filter characteristics (i.e., high pass, low pass, bandpass, and band reject). With careful attention paid to component selection, they can be designed for use at frequencies beyond 100 MHz. High frequency performance is limited by component and package parasitics such as capacitor lead inductance, turn-to-turn capacitance in inductors and input-to-output coupling capacitance. These tend to cause high frequency resonances and bypass the filter circuitry, thereby reducing high frequency attenuation. These out-of-band responses must be explicitly considered. A filter that nominally exhibits a cutoff at a low frequency may actually have resonant characteristics in the MHz regions that compromise its attenuation. Still, their potential ability to operate to 100 MHz and higher, makes discrete R, L, C filters suitable to the entire EMP frequency spectrum. As with other filters, high signal levels can cause nonlinear effects and/or damage resulting in a change in filter characteristics.

Low pass, high pass, and bandpass reflective filters all have applications in EMP hardening. The choice of which type to use depends on the relation between the normal operating frequency and the EMP

specification frequency. If the highest operating frequency is less than the lowest frequency in the EMP specification, a low pass filter is used, and if the lowest operating frequency is greater than the highest EMP frequency, a high pass filter is used. The bandpass filter may be used in either of the above cases and may also have some application when the operating frequency is in the EMP spectrum. In this latter case, the filter pass band must be quite narrow in order to provide protection. Since the EMP signals consist typically of a broad range of frequencies, limiting the pass band to a narrow range of frequencies can potentially reduce the amount of energy the filter will pass. If substantial EMP energy is contained in the pass band, the filtering will not be effective, and a different hardening method must be used.

The reflective filter is characterized by the fact that signals outside its pass band are reflected and must eventually be dissipated elsewhere in the system. With this type of filter, it is possible to produce signals at the load which are larger with the filter in place than without it. This can be caused either by the return of secondary reflections from other unmatched line terminations or by the filter elements forming a resonant circuit with the source impedance. In this respect, the dissipative filter is preferred since most of the EMP energy is absorbed by the filter.

b. Ferrite Beads

The ferrite bead is receiving widespread application for RF noise suppression in modern circuit design. The term "ferrite" is applied to a wide range of ceramic ferromagnetic materials. Generally, they are crystalline structures in which a divalent metallic ion (such as iron, manganese, cobalt, nickel, copper, cadmium, zinc, or magnesium) is joined with iron oxide. The relative permeability, dielectric constant, and conductivity can be varied over a wide range to meet design requirements. When used for electromagnetic noise suppression, small cores or beads

are placed around a conductor to form a one-turn choke. A principal advantage of the ferrite beads arises from the characteristics of the complex permeability. For some applications, the resistive impedance added by the ferrite bead exceeds the inductive impedance and still presents a frequency selective suppression.

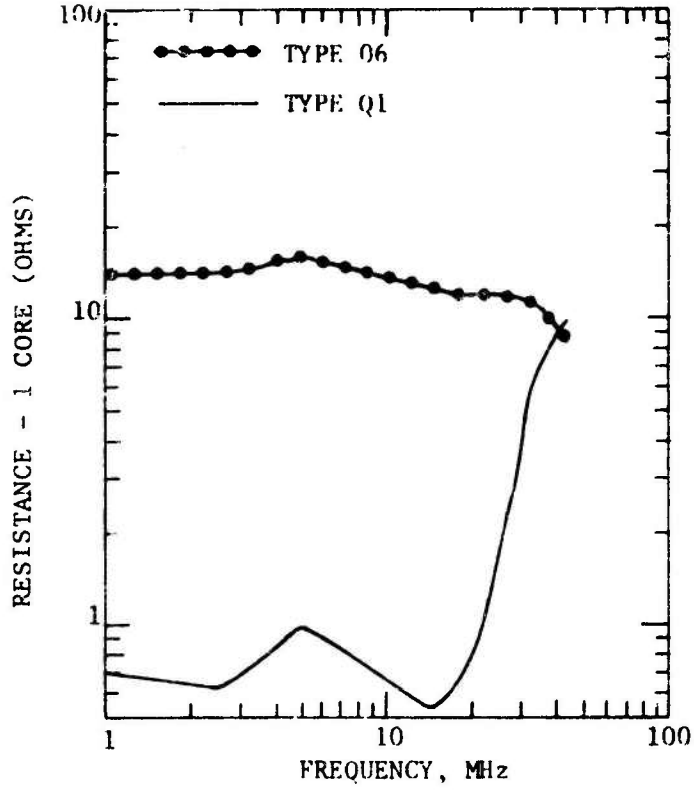
The small size and low cost of ferrite beads is a particularly attractive design feature. However, the small size also makes the beads susceptible to saturation at relatively low currents. Typical saturation currents are on the order of one amp for a one turn configuration.

The resistance and inductive reactance added to a circuit by one core was investigated in Reference (1). Some typical results are shown in Figure 7-1 for two types of ferrite beads manufactured by Indiana General. The availability of different frequency dependence characteristics is clearly shown.

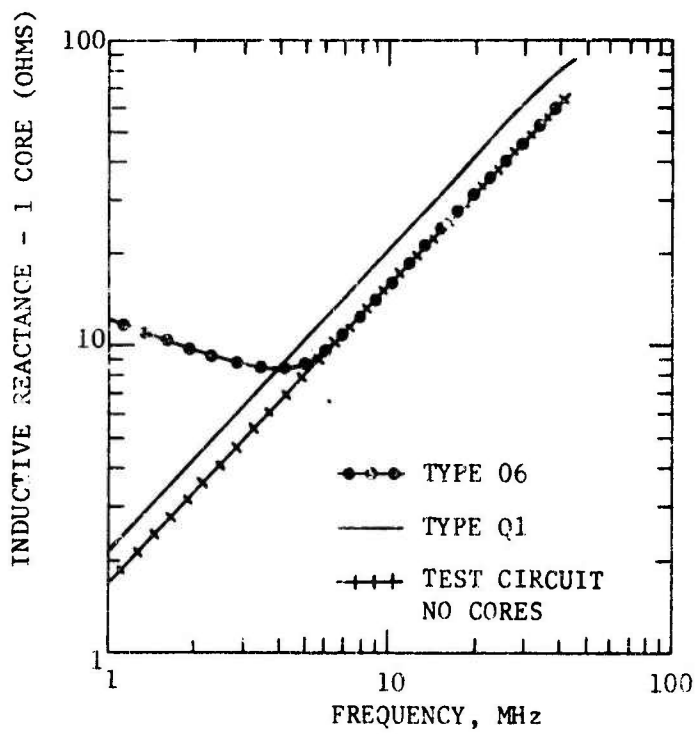
It is possible to obtain larger values of resistance and inductive reactance by increasing the number of beads. However, care must be exercised since the added inductance may combine with stay circuit capacitance to generate spurious resonances that compromise the filter.

c. Filter Pin Connectors

The filter pin connector consists of multiple low pass filters integrated into an interface connector shell. Thus, its use at interfaces where a connector is required anyway, can result in savings in cost, weight, and complexity. In addition, since the filter is installed at the interface, the rejected signals never enter the protected volume. As a result, the requirements for shielding and isolation inside the protected volume can sometimes be relaxed with further cost and weight savings.



(a) Resistance



(b) Inductive Reactance

Figure 7-1. Impedance Added to a Test Circuit by Typical Ferrite Cores

Filter pin connectors are commercially available from a number of vendors in a number of configurations including: π, half-π and single feedthrough capacitor. All except the single feedthrough capacitor use ferrites to obtain a dissipative characteristic.

Since little data have been published on the use of filter pin connectors for EMP hardening, the test described in Appendix A was performed. Two types of Cannon filter pin connectors were evaluated. The DEJ-9TP is a π section with a rated 2 MHz cutoff frequency. The DEJ-9LP is a special low frequency model with a rated cutoff of 100 kHz. The test results confirmed the rated cutoff frequency. However, the π filter presented a nominal roll-off of 60 dB/decade while the low frequency model had 20 dB/decade roll-off. This difference is apparently attributable to the method used to obtain the larger values of capacitance and inductance required for the 100 kHz cut-off. At any rate, the result is that for frequencies in the higher portion of the EMP spectrum (approaching 100 MHz) the π section provides greater attenuation.

The tests also evaluated the two filter pin connectors for nonlinear characteristics. Pulses of 100 ns and 1 μs duration and up to 5 kV were injected and the output monitored. Both filters performed as predicted by their frequency characteristics up to the point where arcing occurred. The arcing occurred pin-to-case as follows:

		100 ns	1 μs
DEJ-9TP	(π section)	2 kV	1.1 kV
DEJ-9LP	(low frequency)	> 5 kV	1.2 kV

No degradation in normal frequency characteristics occurred in either connector. The saturation characteristics were not investigated.

d. Active Filters

While not generally recommended for EMP damage protection, active filters may be useful in some specific applications. Active filters are based upon the performance of one of four basically different active circuits or devices when used in conjunction with passive frequency discrimination elements. These four circuits include: the negative impedance converter (NIC), the operational amplifier, the gyrator, and the phase-locked loop. They are currently receiving much attention in the literature due to the declining price of commercially available monolithic and hybrid active circuits making them cost competitive with other filter types (Reference (6)). These filters, with the exception of the very special purpose phase-locked loop, are limited in frequency by the phase shift of the active network to approximately a few hundred kHz. Sufficient interference signal amplitudes at frequencies above this limit, as in the case for EMP, may cause erratic behavior including possible oscillations and should be investigated prior to any design implementation. Reference (6) gives a good overview of active filter characteristics.

An operational amplifier filter such as Burr-Brown's modular active filters uses feedback to achieve a filtering response that features extremely high rejection of out-of-band signals. The discrete RC input section provides both protection and dissipation while the gain of the op-amp results in zero attenuation in the passband. However, in most design applications, the operational amplifier is itself a semiconductor device, and thus has an inherent EMP susceptibility. Thus, an active filter should not be selected as a protective device unless other circuit design considerations require its presence.

The design of an active filter must include a susceptibility analysis of the amplifier itself to compare its threshold to the threat

specification. It may be necessary to add other protective devices (filters or suppression devices) to protect the active filter. Thus, unless they are required for other purposes, the use of active filters for EMP protection can lead to an unnecessary increase in system complexity.

e. Distributed Passive Filters

Coaxial filters are distributed passive filters that utilize short sections of high impedance or low impedance transmission line to simulate series inductance and shunt capacitance respectively. All of the functional filter characteristics may be implemented with coaxial filters. Coaxial filters can provide cutoff frequencies in the 10 MHz to 1000 MHz range with stop band attenuations free of spurious resonances above five times the cutoff frequency. Both reflective and absorptive filters may be realized.

A special type of distributed filter is the quarter-wave shunt which can provide effective EMP protection to narrow band systems operating in and beyond the UHF region. The shunt is a coaxial cable, a quarter wavelength long at the operating frequency. It is connected in shunt to pass the signal frequency and appear as a short circuit to essentially all other frequencies. Thus, the shunt functions as a band-pass filter. For an EMP transient arriving at the line-shunt junction, the shunt appears initially as merely a parallel transmission line. The shorting action does not affect the transmission of the pulse into the protected circuit until the pulse travels to the short, is reflected, and returns to the junction. This travel time is the effective risetime for the shunt as a protective device. As an example, for a 300 MHz signal, the effective risetime is 1.5 nsec, and it varies inversely with operating frequency.

All distributed filters have the advantage of being relatively immune to EMP caused damage. Excess voltage may cause the coaxial line elements to arc, however this would not cause damage unless a power source was available to deliver more energy.

f. Electromechanical Filters

Monolithic crystal and ceramic filters are electromechanical circuits which utilize the piezoelectric effect to transform electrical energy to mechanical energy and then utilize the mechanical resonance properties of the crystal or ceramic to achieve frequency selectivity. These filters are basically bandpass circuits, but low and high pass functions can be achieved by the addition of passive elements. The useful frequency range of monolithic crystal filters (5-150 MHz) puts them into the interference spectrum of EMP. However, they are highly selective (high Q) filters with bandwidths of from .001 to .2 percent of their center frequency. Ceramic filters also operate in the EMP interference spectrum (0.1 to 10 MHz) and have slightly larger bandwidths than the crystal filters. Both crystal and ceramic filters suffer from stop band resonances which reduce their high frequency attenuation. These are due to overtones of their fundamental vibrational mode and to the excitation of other vibrational modes. The dynamic signal range of these filters is 40-80 dB and depends on the proximity to spurious overtones.

Mechanical filters generally utilize a mechanical resonator with electromechanical transducers at the input and output to achieve electrical filter properties. Like crystal and ceramic filters, mechanical filters are essentially bandpass devices and additional circuitry must be added to effect a low or high pass filter. The frequency range of mechanical filters is from .1 Hz to 50 kHz. Mechanical filters are not as susceptible to high frequency stop band resonances as are monolithic crystals or ceramic filters. The dynamic signal range of these filters is 60-80 dB.

No data have been found on the response of electromechanical filters to EMP signals.

4. APPLICATION SUMMARY

The successful application of a filter to a particular circuit for EMP hardening requires a detailed specification of the threat amplitude and frequency spectrum and the source and load impedances. In addition, the damage threshold of the components to be protected must also be known. From the known failure threshold of the circuit or subsystem and the threat definition, the required insertion loss characteristics of the filter are determined. The required type of filter can then be selected and the component values needed can be calculated. It is also possible to match the characteristics of the filter to a prepackaged unit available from many filter manufacturers or to the characteristics of available filter pin connectors or ferrite cores.

Regardless of the method used to obtain a filter with the proper frequency response characteristics, consideration must be given to the filter's response to high amplitude EMP signals. Table 7-1 summarizes the use of various filters and indicates some of the additional factors that must be considered when these filters are used for EMP hardening.

Considerably more information is needed concerning the response of filters to high amplitude, short duration signals. Until a library of this information is developed, each designer must perform the necessary tests and analyses to assure that his filter design is truly effective for EMP damage protection.

TABLE 7-1

FILTER COMPARISON MATRIX

FILTER CLASS	FILTER TYPE *	USEFUL FREQUENCY RANGE (Hz)	SIGNIFICANT ADVANTAGES	SIGNIFICANT DISADVANTAGES
Discrete R, L, C	1, 2, 3, 4	to 10^8	• Versatile • Low Cost	• Large for Low Frequency • Low Q
Ferrite Beads	1	10^6 - 10^8	• Versatile • Dissipative with Low Pass Band Loss	• Spurious Resonances • Saturation
Filter Connector	1	10^4 - 10^9	• Design Integration Simplicity • Dissipative	• Spurious Resonances • Saturation
Coaxial	1, 2, 3, 4	10^7 - 10^9	• High Frequency Use • Low Parasitics	• Large Size
Crystal	3, 4	$5x10^6$ - $1.5x10^8$	• High Q • Small Size	• Spurious Resonances • High Cost
Ceramic	3	10^5 - 10^7	• High Q • Small Size	• Spurious Resonances • Not IC Compatible
Mechanical	3, 4	.1 - $2x10^4$	• High Q	• Limited Range • Not IC Compatible • High Insertion Loss
Active	1, 2, 3, 4	to 10^5	• Small Size • Gain Provision	• Power Requirement • Limited Range • Damage Susceptibility

* 1 - Low Pass 3 - Bandpass

2 - High Pass 4 - Band Reject

5. REFERENCES

The following references were used in the preparation of this chapter:

(1) Schwarz, J. J., "ARES F/G Instrumentation Study, Phase I Results," BDM Memorandum, 15 October 1971.

(2) Rome Air Development Center, "Interference Notebook, Volume 1," RADC-TR-66-1, June 1966.

(3) Rome Air Development Center, "Interference Notebook, Volume 2," RADC-TR-66-1, August 1969.

(4) Moschytz, George S., "Inductorless Filters, A Survey, Part I, Electromechanical Filters," IEEE Spectrum, pp. 30-36, August 1970.

(5) Moschytz, George S., "Inductorless Filters, A Survey, Part II, Linear Active and Digital Filters," IEEE Spectrum, pp. 63-75 September 1970.

(6) Mattera, Lucinda, "Active Filters Get More of the Action," Electronics, pp. 104-109 June 19, 1972.

(7) International Telephone and Telegraph Corp., "Reference Data for Radio Engineers," Fourth Edition, September 1956.

CHAPTER 8

DECOUPLING

1. INTRODUCTION

In some applications, the protection provided by filtering techniques is not sufficient. In these cases, there are a number of circuit isolation techniques that are capable of providing considerably more attenuation between input and output. This attenuation is generally gained at the expense of bandwidth, weight, cost, or circuit complexity. The most common isolation technique is differential coupling. Another technique that is becoming more readily available is electro-optical coupling. In addition, there are other techniques that, while apparently attractive, have not been applied to any significant extent for EMP hardening. These include a number of mechanical, fluidic, and acoustical coupling techniques.

The entire EMP problem is intrinsically involved with coupling. The EMP free field outside an aeronautical system must be prevented as much as practicable from coupling to the sensitive electronic circuits in typical airborne equipment. Through various coupling mechanisms, the fields outside an aeronautical system eventually manifest themselves as cable currents. Conducted cable transients can be reduced by using information transmission mechanisms other than conducted electrical energy. The two most common nonelectrical conduction means of such information transfer are microwave dielectric waveguide and optical light pipes. These devices operate on identical principles, but have been described by their most common name for convenience. (Reference (1))

2. DIFFERENTIAL SIGNALING

In many cases, subsystem hardening can be improved by using balanced signal techniques for some or all of the interfaces. This improvement derives from the fact that EMP signals are usually induced on cables in the common mode. The balanced configuration uses two-line communication to establish a separate signal mode isolated from the reference ground. Since internal signaling is usually referenced to ground, interface circuitry must be added to reject the common mode and to convert the signal mode from balanced to unbalanced so that it can be used by the internal circuitry. Thus, two changes are required to implement balanced interface configuration. One change involves the cabling, the other involves the interface circuitry. As a rule, the use of a properly designed balanced interface configuration can provide a hardness improvement of about 20 dB relative to a similar unbalanced configuration.

a. Balanced Cables

A balanced interface configuration often utilizes the twisted pair cabling. Ideally, the twisted pair experiences only common mode interference coupling. In the balanced signal mode, the twisting serves to minimize the coupling by cancelling the magnetic field coupling and equalizing the electric field coupling. In the real case, the pair is not completely balanced, so that some signal mode interference coupling is present. However, the signal mode will always be less than the common mode and thus effective shielding (common mode rejection) is obtained.

Tests described in Appendix A, were conducted on a sample twisted pair shielded cable, Alpha No. 1267/18V, to obtain typical common mode rejection (CMR) data.

The common mode rejection or gain in shielding effectiveness is expressed as

$$CMR = 20 \log \frac{I_a - I_b}{I_a}$$

where I_a and I_b are the currents in the individual wires. Figure 8-1 is a plot of the test results, CMR versus frequency. This graph shows that the common mode rejection varies inversely with frequency. There is a nominal improvement of 40 dB in the 1 to 100 kHz region, and a 20 dB improvement in the 1 to 10 MHz region.

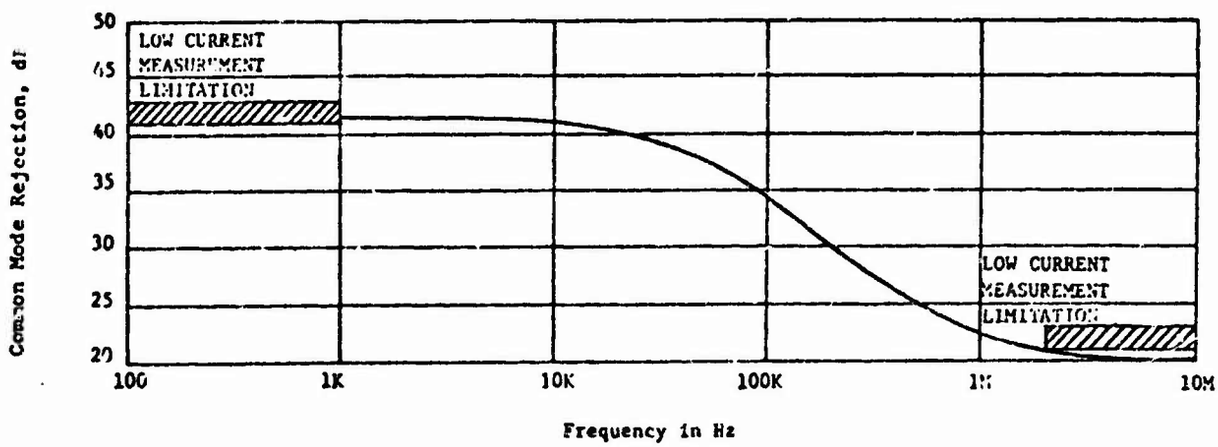


Figure 8-1. Typical Common Mode Rejection of a Twisted Pair Cable Versus Frequency

The twisted pair evaluated here has a signal mode characteristic impedance of about 200 ohms. In spectral applications, such as those in which lower impedances are required, twinax (balanced coaxial) cable can be employed for differential signalling. Twinax can be expected to be somewhat less effective in terms of common mode rejection at the lower frequencies, since it is not twisted.

b. Interface Circuitry

In order to take advantage of the improved shielding offered by the balanced cabling, interface circuitry must be provided to reject the common mode and convert the signal mode from balanced to unbalanced. This common mode rejection can be accomplished either passively or actively.

The passive method employs a differential transformer, designed specifically for wideband application. Since differential transformers use magnetic cores, it is important to consider saturation effects in EMP applications. Two possible drawbacks of these devices are their appreciable weight and bulkiness.

There are two techniques often used to improve the differential signalling performance of a differential transformer; one is the use of shielding and the other is the use of tuning. When used in a balanced cabling system, the use of a Faraday shield between the primary and secondary windings provides excellent attenuation of common mode signals. Given the initial transformer investment, the tuned transformer offers some inherent advantages. In this case, the transient response of the tuned circuit should be analyzed to determine the possibility of damage to the tuning capacitors.

The problems to be considered in specifying a differential transformer include voltage insulation and core saturation. Actually, core saturation tends to aid in EMP protection since it reduces the coupling efficiency. However, careful design is necessary to take advantage of this saturation since it is a nonlinear function of both time (or frequency) and amplitude. Similarly, arcing can be a mixed blessing. Arcing to ground may be advantageous since it can behave like a suppression device. Arcing between primary and secondary on the other hand, completely destroys the effectiveness of the transformer for passive rejection of common mode

signals. In either case, arcing can have serious side effects such as damage to insulation or even damage to other components.

The active approach uses a differential amplifier to make the balanced to unbalanced conversion. Differential amplifiers with a common mode rejection of 40 dB at 50 MHz (Reference (2)) have been fabricated and it is possible to trade off one of these parameters at the expense of the other (i.e., CMR versus bandwidth). When using differential amplifiers, it is important to specify the CMR, the bandwidth, and the maximum common mode voltage. This latter parameter is related to the damage threshold of the active device. Unless otherwise protected, integrated circuit differential amplifiers are limited to common mode voltages of about 20 volts.

3. ELECTRO-OPTICS

Optical systems utilizing nonconducting transmission systems are becoming more practical for use in aeronautical systems and present some potential advantages in EMP hardening. In both cases, this is due to improved excitation and detection systems as well as adequate transmission systems. In the case of optical transmission, the mode which appears the most feasible is the use of fiber optics with light emitting diodes (LED) and photodiode detectors (PD) as the optical/electrical transducers. Either plastic or glass fiber optics can be used, each having their individual and unique advantages. Entries and exits at unit housings can be via small (e.g., waveguide beyond cutoff) diameter holes. The electrical/optical conversions should be made within the unit housings in order to protect the semiconductor transducers.

a. Optical Conductors

As a one-to-one substitution for electrical conducted signals, light pipes may not always be cost effective or otherwise desirable at the present time. Usually one of three different multiplexing methods would be used. Traditional multiplexing refers to both time division and frequency division methods. The other techniques are: Wavelength Division Multiplexing (WDM) and Space Division Multiplexing (SDM). (Reference (3))

WDM involves the transmission of data using light of different wavelengths. The various wavelengths are generated by different LED's and are sorted at the receiver by photodetectors tuned to the various wavelengths. The number of channels is essentially a function of the number of wavelengths available, the LED and PD spectral widths, and the ability to optically couple the individual wavelengths into the fiber.

SDM involves the coding of various signals by means of their spatial location at the entrance and the exit of the fiber optics bundle. This technique requires the use of a coherent fiber optic bundle and a special fiber optic connector arrangement. The number of channels that can be multiplexed on a given bundle is primarily a function of the channel spot size at the fiber entrance, length of the fiber bundle, and cross coupling between the individual fibers.

The best approach is to consider the use of fiber optic links when the system is being designed and take full advantage of the high data rate capability. High light pipe attenuation, up to now a problem in long line light transmission, has recently undergone some technology break-throughs. Attenuation has been lowered from the range of about 4 dB/meter to better than .02 dB/meter. The low cost mass production of these low

attenuation pipes has not been achieved. However, for the short cable lengths in aeronautical systems even the higher attenuation pipes may be acceptable. Line of sight transmission is also possible with higher attenuation.

b. Photon Couplers

In the last 10 to 15 years, there has been a significant increase in electronic design activity and an intensified search for improved isolation methods. With the advent of photon couplers on the electronics market, it was realized that there may be a substitute for an isolation transformer. Photon couplers offer the following distinct advantages over other coupling methods.

- No Inductance
- Minimum Capacitance Between Input and Output
- Good Frequency Response
- No Saturation or Hysteresis Problems
- No Degenerative Feedback

Photon couplers normally consist of a light emitting device emitting EM radiation through a transparent dielectric medium towards a light sensitive sensor.

Tests were conducted, as described in Appendix A, to determine the pulse power failure thresholds of two Texas Instruments photon couplers (optically coupled isolators). These devices consisted of a diode input and a phototransistor output. The TIL 107 coupler is a 4-lead, hermetically sealed device in a glass-metal package. The TIL 112 coupler is a 6-lead device, having access to the base, encapsulated in plastic.

Table 8-1 lists the maximum no fail power and the minimum power to fail for one microsecond pulses applied to the diode and transistor sections of two types of photon couplers. When pulsed from input to output, these devices exhibited a voltage mode of failure. The current is essentially zero up to the failure point. The maximum no-fail incident pulse voltage for the two devices was 3.5 kV, indicating that their isolation resistance values are extremely high.

TABLE 8-1

PHOTON COUPLER FAILURE THRESHOLDS

DEVICE	MAXIMUM NO FAIL POWER, W	MINIMUM POWER TO FAIL, W
TIL 112 Diode	881	1183
TIL 112 Transistor	677	915
TIL 107 Diode	627	831
TIL 107 Transistor	566	1333

4. OTHER DECOUPLING METHODS

Frequency translation is an effective hardening technique for cases where the normal signal is within the interference frequency spectrum. Subsystem to subsystem information transmission may be accomplished by modulation of a high frequency carrier and the transmission of the carrier by electrical conduction. In this manner, the signal may be placed at a frequency outside the EMP spectrum so that EMP interference coupling is inefficient. This technique also allows effective filtering techniques to be implemented. Such an approach requires the addition of modulation and demodulation circuitry to the system, but in the case of systems with a small number of information exchange lines or when used in conjunction with a multiplexing approach, this may be an acceptable trade-off.

Another nonconducting information processing subsystem uses fluidic devices which are commercially available for implementation in digital processing and control systems. Applications include a wide range of sensing, logic, amplification, and control functions. These applications take advantage of a fluidic system's ability to function solely by employing the fluid dynamic phenomena associated with a flowing stream of gas or liquid, without relying on the use of moving parts or electrical components.

Functions available include all of the basic digital logic functions, gates, flip-flops, and single shots, and some combinations of these such as counters, encoders, and shift registers. Analog functions such as operational amplifiers are also available. However, where an electronic or electromechanical system is already doing a job satisfactorily, it is seldom prudent to replace that system with a fluidic system.

Although fluidic technology offers some advantages over electronic technology such as simplicity, ruggedness, and immunity to radiation effects; the slow frequency response of the components inherently limits information transmission to frequencies below 1 kHz. This is a very severe restriction for most airborne information processing applications typically handled by electronic systems. Their low electrical noise susceptibility and high reliability make fluidics very effective for EMP hardening where they can be used. Because of their extreme frequency limitation they will not be discussed further in this handbook. Reference (4) is a comprehensive survey of fluidic technology and applications.

6. REFERENCES

The following references were used in the preparation of this chapter:

(1) International Business Machines Inc., "Light Interface Technology," IBM Report No. 71-928-007, September 1971.

(2) Brown, R. M., "Differential Amplifier BDM Model BDA-101 Final Report," DNA Contract DASA-01-71-D-0036-0021, Braddock, Dunn and McDonald, Inc., February 1973.

(3) Doellner, Leonard, "The Optically Linked Missile," Paper, presented 1972 Electro-Optics Conference, New York, 13-14 September 1972.

(4) Weathers, T. M., "NASA Contributions to Fluidic Systems," Contract No. NASW-2173, Computer Sciences Corporation, 1972.

CHAPTER 9

ERROR DETECTION

1. INTRODUCTION

Data coding schemes can provide two useful functions in reducing errors in a system subjected to EMP. It is possible to make use of coding for the detection of errors within data. Once the errors are detected, a variety of techniques can be used to prevent undesired system response to the data errors. In some systems, provisions are made for requesting retransmission of the data when an error is detected. In other systems, the data errors are ignored on the assumption that small amounts of lost data do not significantly impair the operation of the system.

It is also possible to use coding techniques to correct data errors. This requires more elaborate codes than those designed for error detection, but eliminates the need for transmission from the data receiver back to the data source in order to request retransmission of data in systems that are significantly degraded by lost information.

Coding techniques for eliminating errors due to EMP interference must be chosen to take the best advantage of the characteristics of EMP. There are basically two important characteristics of EMP interference that have a serious impact on the selection of coding techniques. First, EMP may affect all interconnections simultaneously and second, EMP causes severe interference for a short period of time with no interference outside of this period.

EMP interference is possible on all interconnections within electronic systems, simultaneously. It is unlikely that codes employing multiple line, parallel, simultaneous transmission can offer an advantage. A

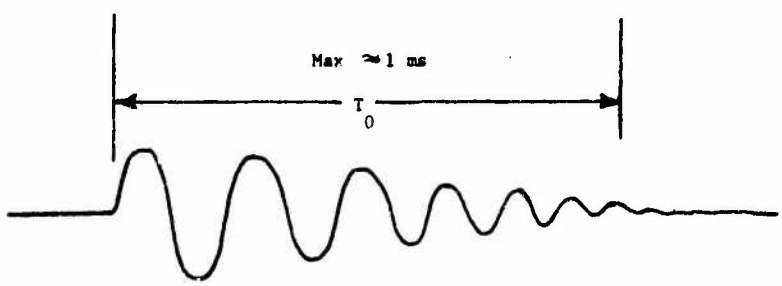
16-bit data word transmitted in parallel format can be completely blanked out by EMP. However, a 16-bit word transmitted in serial format at about 10 kbps is unlikely to have more than one to five bits destroyed from EMP interference. Thus, the techniques for providing parity checks, and for error coding in general, should take advantage of the benefits to be derived by spreading out the bits within a single message, including its check bits, over a period of time. When parallel transmission of data words is required because of other constraints on the system design, such as cost and size of equipment, it is useful to provide parity check information in a separate word transmitted at a different time than the data word. Longitudinal parity checks are a good example of this technique.

Another factor to consider is the nature of the interference in a serial transmission. Again, because of the short time duration and high intensity of EMP interference, it is likely that bit errors in a serial transmission will be grouped together in a short time burst. This is a significantly different type of interference than random error probability interference sources, which are generally encountered in digital transmission systems. Thus, it requires special types of error detection and error correction codings. The coding techniques most useful for this type of interference are generally referred to as burst-error-detecting, and burst-error-correcting codes.

The problem of EMP interference can be narrowed down to a more specific case, even within the general area of burst error coding. Burst error codes are designed to handle the general form of the classical bursty channel. The classical bursty channel is a communication channel subject to bursts of interference with a maximum duration of T_0 and a minimum separation between bursts of T_1 (Reference (1)). The effectiveness of various codes and the selection of optimum codes are heavily dependent on the ratio, T_0/T_1. This ratio essentially dictates the maximum percentage of transmitted information which may be destroyed by interference. In addition, the actual value of T_0 and T_1 have a bearing on the code structure which

will be most beneficial. In the case of EMP interference, the interference bursts are seldom likely to be longer than one millisecond. In addition, since EMP results from nuclear explosion, it is unlikely that the separation between bursts will be nearly as short as the period of a burst, although any system has its own scenario specifications. This gives a small value for T_0/T_1.

Under these circumstances, it is reasonable to treat the special case of a single isolated interference burst (see Figure 9-1) in the selection and evaluation of coding techniques. This means that the total percentage of data destroyed by EMP interference is very low. In other words, when burst interference occurs, the length of time following it, during which redundant information can be received and used to correct or detect the errors which have occurred, is relatively long. As a general rule in this class of problems, the percentage of redundant information transmitted, and the length of time over which such information must be received in order to accomplish detection or correction of errors, is limited primarily by constraints on equipment complexity rather than the potential reception of another interference burst.



1. A single isolated noise burst of maximum duration ≈ 1 ms.
2. Simultaneous interference with all susceptible electronics in a system.
3. Interference levels substantially greater than signals.

Figure 9-1. EMP Interference Model for Error Code Evaluation

The remainder of this section will include primarily a discussion of some of the simpler forms and requirements of burst-error codes. In addition, particular attention will be given to the special case of burst-error-codes which are single-error-codes. For convenience, a definition of a burst-error group within a defined data word is given:

> A burst-error of length, D, is defined as a collection of bits whose first and last bit are incorrect, and which includes all incorrect bits in the data word (Reference (2)). It is neither necessary nor assumed that all bits within the burst are incorrect.

2. ERROR DETECTING CODES

With the definition of an error burst, it is possible to state precisely the parity check or error coding requirements to detect burst-errors within a data word.

> Theorem: For detecting all burst-errors of length, D or less with a linear code of length N, D parity-check symbols are necessary and sufficient (Reference (2)).

This is an extremely powerful theorem for determining parity check requirements in transmissions subjected to EMP interference. Because of the short time duration of EMP interference, it is usually possible to establish a maximum time duration for an error burst resulting from EMP interference. Using this maximum duration for interference of a given data set or line, and the transmission format (such as bit rate), it is possible to determine the maximum number of bits that can be in error as a result of EMP interference.

As an example, assume that the expected maximum duration for EMP interference on a given serial transmission line is 40 μsec and the bit rate is 100 kbps. For this example, a data word of 16 bits, not including parity check bits, will be assumed. The data bits and parity bits required are shown in an array in Figure 9-2. This array illustrates the format of the parity check procedure. In actual transmission, the sequence is to transmit the bits in the first column sequentially, then the bits in the second column, and so forth. The parity check bits establish parity tests on each row of the array. Thus, the first parity check symbol detects parity errors in the group of bits which include the first, fifth, ninth, thirteenth, and seventeenth data bits. Since the burst error cannot include more than four bits, and no two of these bits are in the same group of four, it is not possible for more than one bit to be wrong in a given row. Thus, the parity check symbol will always detect the error.

X_1	X_5	X_9	X_{13}	P_{17}
X_2	X_6	X_{10}	X_{14}	P_{18}
X_3	X_7	X_{11}	X_{15}	P_{19}
X_4	X_8	X_{12}	X_{16}	P_{20}

X = Data Bit
P = Row Parity Bit

Subscripts identify serial transmission sequence.

Figure 9-2. Burst-Error Detecting Code

It should be noted that if parity check symbols were arranged in the standard format of one parity check symbol for each sequential group of four bits, it would be possible for more than one bit to be wrong in each parity check group. In this case, those errors including an even number of bit errors associated with one parity check would not be detected. It is also useful to note that this detection system depends only on the fact that all errors are confined within a group of four bits or less in sequence. Therefore, this parity check system would detect all errors under a serial transmission format as described above and would also check all parity bit errors if the transmission format was four-bit parallel words transmitted once every 40 μsecs. Thus, a combination of parallel groups transmitted with a given time separation and with the parity check configuration shown, can also utilize this technique.

3. ERROR CORRECTING CODES

The situation is complicated somewhat with error correcting codes. A concise statement of necessary and sufficient conditions for correction of any number of errors within an arbitrary code has not been determined. Several theorems give expressions for a minimum, or necessary, set of conditions. The necessary and sufficient conditions for some specific types of codes with a specific number of errors have also been derived (Reference (2)). Some specific examples of this type of coding which are fairly readily implemented, are given in the following paragraph.

To correct all burst errors of length D or less in a data set of N bits where $N > D$, it is sufficient to send each message three times with sufficient parity checks on each message (in accordance with the procedure previously described) to detect all burst errors. With the conditions stated, it is not possible for EMP or burst interference of length D, to cause errors in more than two out of the three transmissions of the same data set. Any data set with errors will be detected by the parity checks. Thus, the equipment receives and accepts only those data sets

which do not indicate parity error, and it is assured that every message will be received at least once without error. Another similar procedure, which involves fewer bits to accomplish error correcting transmission, but may require slightly more complex decoding equipment, is to send the data set three times without parity check bits. Since the length of the burst error is never longer than one message length, each individual bit within the message will be correctly received at least two out of the three times. Thus, the three transmissions of a given data set must be stored and then compared, bit by bit. For each bit, at least two of the three transmissions will be correct, and a majority rule procedure can always determine the correct value for the bit. Neither of the procedures mentioned accomplish error correction with the minimum possible number of bits, but they both represent realistic approaches which can be implemented in a relatively straightforward manner.

4. SINGLE ERROR CODES

With low bit rates, the burst error often reduces to a single bit error. In those cases where EMP interference is shorter than one bit period and can therefore interfere with only a single bit in a data set, single error correcting and single error detecting codes can be used. Since many data links are designed to work in a random error environment with a very low probability of error, they are generally subjected to only single errors within a given data word. As a result, extensive work has been done on single error detection and correction codes. Most of the codes currently in use are of this type. The technique of using one parity bit to establish either odd or even parity on a given data word (of any length), will detect any single bit error. The IBM tape format which includes word parity and longitudinal parity checks as shown in Figure 9-3, is capable of correcting any single bit error and detecting any double bit error. Any single bit error in this format will cause one row parity error and one column parity error. The bit located at the intersection of the error column and error row is the bit in error. Since the specific bit in error can be determined, it is possible to correct this bit error and correctly receive the message.

X	X	X	X	P
X	X	X	X	P
X	X	X	X	P
X	X	X	X	P
X	X	X	X	P
X	X	X	X	P
p	p	p	p	P_p

X = Data Bit
P = Row Parity Bit
p = Column Parity Bit
P_p = Row and Columnar Parity Bit

Figure 9-3. IBM Tape Format

5. INTERLEAVING

One of the most popular techniques for handling burst errors is interleaving. This is a technique by which the information to be transmitted is rearranged in time order prior to transmission, and then reordered back into the original format (deinterleaved) after reception. The purpose of the technique is to take the burst of errors which occurs and spread them out into a series of individual isolated errors in the format following the deinterleaving process. This changes the nature of the interference from a burst error group to a series of isolated bit errors which can, in many cases, be more readily handled with simpler encoding and decoding equipment. The ability to take the burst of errors and spread them out into a series of isolated bit errors is dependent on the fact that there will be a long period of good reception following a burst of errors. The

interleaving operation is a type of coding, but its purpose is to change the nature of the error distribution rather than to detect or correct errors. This technique can then be combined with error detection or correction codes.

Figure 9-4 shows a functional diagram of a system based on error coding combined with an independent interleaving operation. As a general rule, the added complexity required to accomplish interleaving is more than justified by the reduced requirements on the error detecting or correcting techniques. In fact, most burst error codes which do not utilize a separate interleaving and deinterleaving process actually combine interleaving with the introduction of redundant data (coding) in a single operation. This can be seen by examining such codes and noting the fact that burst error codes generally provide information based, to some extent, on a particular data bit which is scattered over a long segment of the information transmission format.

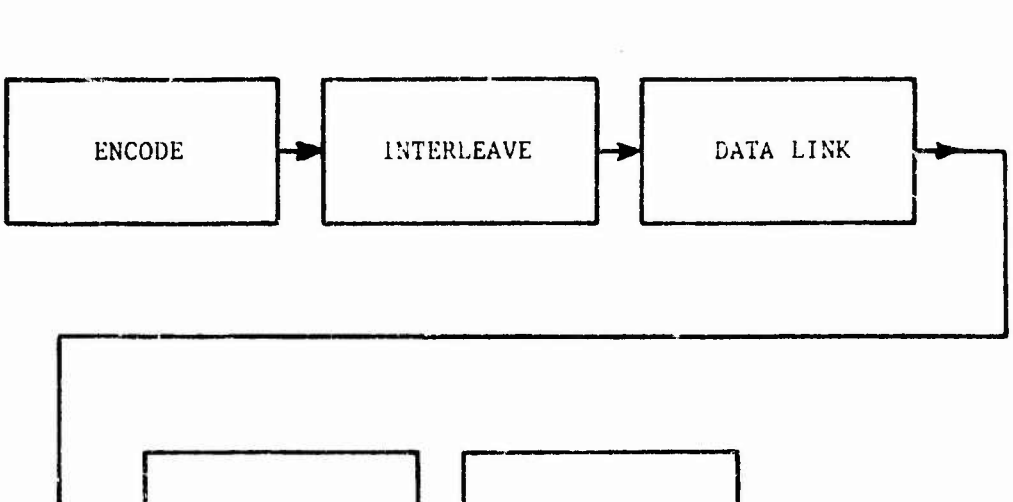


Figure 9-4. Separate Encode/Interleave Operation

With respect to interleaving as a separate operation to be combined with various coding techniques, two specific methods are discussed. The first is best illustrated by the "longitudinal parity check" technique. These codes do not involve the interleaving or reordering of the actual data bits. What is done is the generation of parity check bits from an interleaved set of the data bits. In the standard IBM tape format, for instance (see Figure 9-3), parallel words are transmitted without any interleaving or reordering, but the longitudinal parity check bits are applied to a given bit in each of a set of words. Thus, a given longitudinal parity bit is applied to an interleaved portion of the data, such as the second bit of every word in a 100-word block. This has most commonly found application in single parity bit error detecting codes, but is equally applicable to error correcting codes. Polynomial codes (Reference (3)) involving the generation of several parity bits which allow error correcting can also be applied to such a set of interleaved data bits.

The second form of interleaving employs the encoding of data in its original format and the subsequent interleaving of both data and check bits (Reference (1)). A diagram of this technique is shown in Figure 9-5. As an example, if the bit stream from the encoder represents data encoded in a convolutional* code with a constraint length of two, the resulting distribution of errors in the data entering the decoder can be entirely corrected. On the other hand, if the interleaving operations were not carried out, the convolutional code with a constraint length of two could not correct a burst of four adjacent errors.

6. HYBRID SYSTEMS

Techniques for detecting interference or the resulting errors obviously are of no value by themselves. In all cases, detection techniques must be combined with some planned response on the part of the

---

*See References (1) and (2) for discussion of convolutional coding.

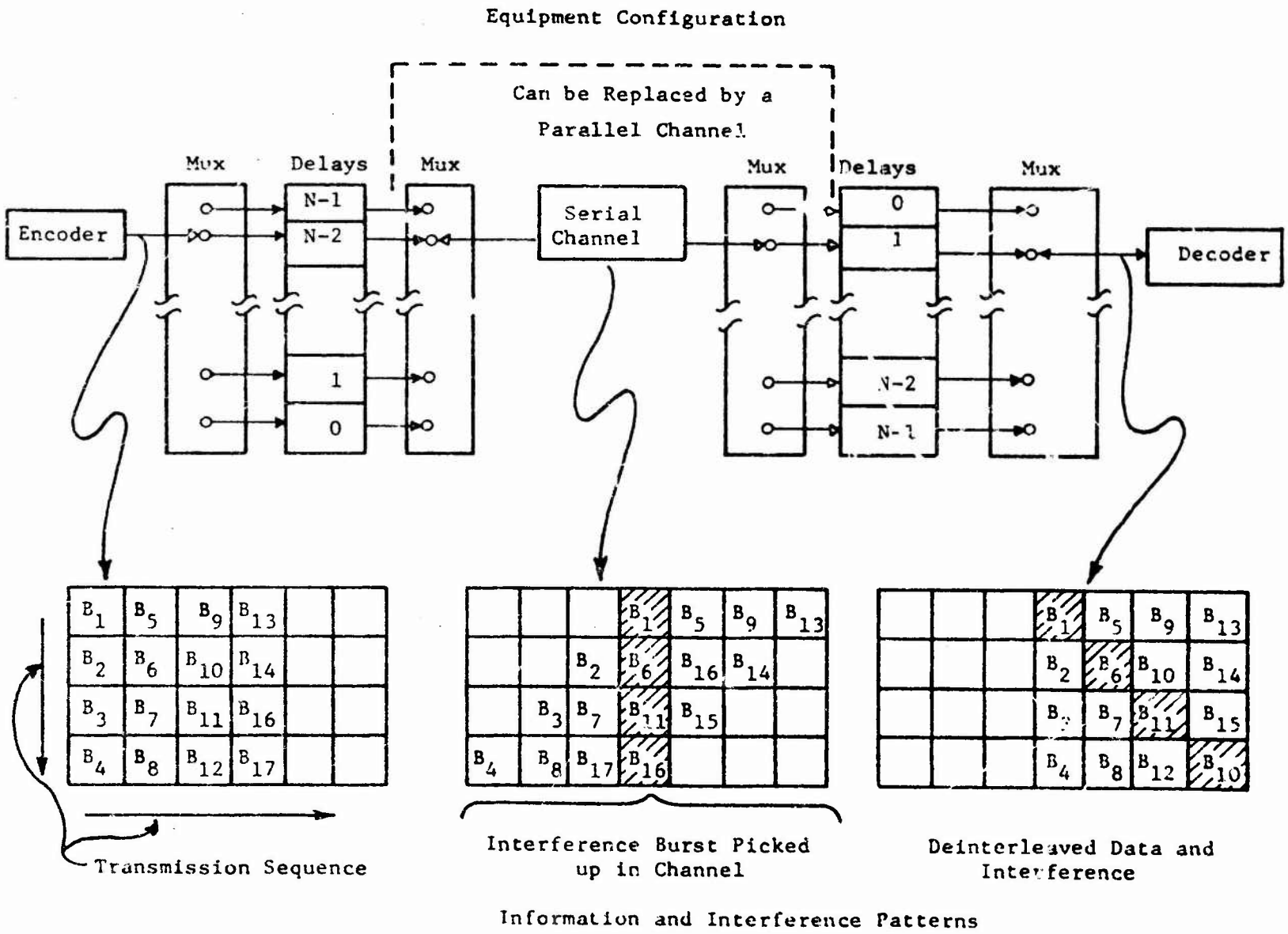


Figure 9-5. Interleave Operation

system. In fact, the only reason for supplying error or interference detection equipment is to identify those occasions when the system should change its mode of operation in some manner in order to minimize the detrimental impact of the interference or errors. A wide variety of detection/response combinations can be designed into systems. The choice is dependent on the functional requirements and design of the specific equipment in question. Several of the more common techniques are discussed here.

a. Detect and Reject System

The simplest type of detection/response technique is the detect and reject system used quite commonly in both digital and analog data. For this technique, some type of error detection is provided on a single data link. The equipment receiving the data is designed to ignore any data set accompanied by an error indication from the error detector. This technique is very straightforward and can be applied to a wide variety of data types utilizing an equally wide variety of error and interference detection techniques. This method is of value in systems that suffer degradation from erroneous data, but do not suffer serious degradation from lost data. As long as it is possible for a system to operate satisfactorily without receiving all the data transmitted, erroneous data can be ignored.

b. Automatic-Repeat-Request (ARQ) System

The ARQ System requires error detecting techniques such as coding in digital signals and amplitude discrimination in analog signals (see Chapter 3), to determine when errors or interference have occurred. Following this, a request for retransmission of the data must be generated by the receiving equipment and transmitted to the source equipment via a return transmission link. When this occurs, the source equipment must retransmit the data set.

In actual practice, many ARQ systems are dramatically superior to any error correcting code system in that they have much higher data throughput and are substantially error free (Reference (3)). This is accomplished at the cost of some compromise in system design requirements. First, the ARQ System requires a return link for request signals. Second, in order for data to be retransmitted when a request is issued, it is necessary to provide some form of memory for storing the data long enough to determine if a repeat request will arrive. Finally, the repeat data requested arrives with some time delay compared with the normal sequence of data transmission. In some cases, added complexity in the receiving equipment is required to accommodate data which do not arrive in a fixed time sequence. The ARQ System can be extremely useful and efficient in systems which do not require serious compromise in the design goals and equipment complexity in order to provide the required return link, data source memory capability, and receiver capability to handle data out of time sequence. This technique can be applied to digital data and to many types of analog data, such as the output from multiplexed, analog sample-and-hold equipment.

c. Circumvention

The term "circumvention" applies to hardening techniques which depend on the detection of the EMP event to initiate some preplanned system response. This response includes rejecting the data which are being transmitted during the EMP event, and either awaiting the next data transmission, requesting immediate retransmission, or recycling stored pre-event data. Previous circumvention applications have used the recycling approach (Reference (4)).

The advantages of circumvention arise from the fact that when an EMP event occurs, it is likely to interfere with almost all data flow between equipment units simultaneously. Circumvention has been employed with computer systems where the sheer volume of data inputs makes any attempt to

correct all of the data subjected to EMP interference very complicated. The number of inputs to a computer and the resulting volume of data that must be handled makes circumvention seem attractive in many cases.

Another advantage is that circumvention techniques may also be applied to nuclear radiation hardening. Here, there is a probability that a nuclear event will generate erroneous data not only at the interface, but within the subsystems as well. This situation handicaps other error detection techniques. If the stored data are not affected by the nuclear environments, (as might be the case with a disc memory), then valid, but perhaps outdated, data are immediately available. Thus, whereas in some cases circumvention may not be the most attractive technique from the standpoint of EMP upset hardening, if it is to be included in the system design for radiation hardening, then this may warrant its application for EMP hardening as well.

The major disadvantage associated with circumvention is involved with detecting the EMP event. Two detection techniques have been used previously. One involves the use of an external antenna to measure the EMP field. The other uses a current probe to detect EMP induced currents on cables entering the package to be protected. If the fields are detected, then the problem is to determine at what level to initiate the circumvention response. Of course, the transfer function between the antenna and the interface circuitry can be measured and used to determine the initiation level. However, the transfer function can vary with either planned or unplanned changes in system configuration, and thus, may not be reliable. If instead of determining the transfer function, the initiation level is merely set very low, circumvention may be initiated for EMP events of insufficient magnitude to generate erroneous data; or even by electromagnetic interference.

If the cable current is detected, choosing the initiation level is still a problem. It must be chosen to allow normal data to pass and yet detect the EMP currents. If the sensor is placed outside the cable shield, sufficient difference between the signal and EMP currents exists to allow

effective detection. However, the cable shield transfer function must now be considered. Again, unless this transfer function can be closely controlled, it may vary. If the sensor is placed inside the cable shield the transfer function is eliminated. However, in this location the sensor cannot discriminate between normal signals and EMP transients of the same magnitude.

Another possibility might be to keep track of errors in a large number of signal lines to a given unit. For example, with a computer employing a great number of input data lines from several sources, it might be possible to utilize error detecting on all of the individual data lines. Whenever the total number of errors for all input data within a given length of time, reached a specified value, it might be assumed that the data set, as a whole during that time frame, was sufficiently degraded to be essentially useless. Based on this decision, some form of circumvention such as recycling the last good data set or merely ignoring one complete group of data for a given time frame, could be employed rather than attempting to make decisions about the usefulness of each individual data item from the various sources. Circumvention based on this type of detection would have the advantage that the decision concerning the quality of the data would be based on actual errors within the data, and not on some attempt to correlate an external field to the probability of serious degradation in the data.

7. APPLICATION GUIDELINES

A variety of system upset hardening techniques have been presented in this chapter. The problem that faces the designer is one of determining which of the available techniques are useful and necessary in a specific application. What follows is a set of general guidelines to assist in this determination.

(1) If small amounts of erroneous data do not have the significant detrimental influence on system operation, it is obvious that there is no justification to employ any code.

(2) In systems that cannot tolerate erroneous data, but do not suffer significant degradation from lost data, error detecting codes combined with some procedure for rejecting erroneous data should be employed since they are sufficient and generally less complex than error correcting codes.

(3) In complex systems (such as a computer interfaced to many other units) requiring error detection, but not correction, circumvention may be a better alternative than separate handling of each signal interface.

(4) In systems that cannot tolerate erroneous data or lost data without significant degradation, either error correcting codes or an ARQ technique must be employed.

(5) ARQ systems are useful when throughput and minimum uncorrected errors are more important design goals than reduced complexity.

(6) Error correcting codes should be utilized in preference to ARQ systems when minimum system complexity is an important design goal. This is particularly true if minimum complexity at the data source end of a link is of primary importance since error correcting codes have their most serious impact on equipment complexity at the decoder.

(7) Interleaving is an especially attractive approach for modification of existing equipment which already has its own error detecting and error correcting code system designed for random probability errors, or when it is desirable to work with a particular standardized coding and decoding system to take advantage of existing equipment designs or standardized formats.

(8) Interleaving is of no value when the data rates and error burst durations are such that the problem is essentially a single error problem.

8. REFERENCES

The following references were used in the preparation of this chapter:

(1) Tarney, G. David, Jr., "Burst-Correcting Codes for the Classic Bursty Channel," IEEE Transactions and Communications Technology, Vol. Com-19, No. 5, October 1971, pp. 772-780.

(2) Peterson, W. Wesley, Error Correcting Codes, Cambridge, Massachusetts The M.I.T. Press, 1968.

(3) Liccards, Michael A., "Polynomial Error Detecting Codes and Their Implementation," Computer Design, September 1971, pp. 53-59.

(4) Electromagnetic Handbook for Missiles and Aircraft in Flight, Albuquerque, New Mexico, Sandia Laboratories, September 1972, pp. 357-358.

SECTION IV

HARDENED DESIGN EXAMPLES

This section includes Chapters 10 and 11 and provides examples to illustrate the application of the techniques described in this handbook. Both upset and damage hardening examples are presented. The examples represent realistic hardening design requirements and are taken from equipment which is required in airborne applications and have not previously undergone EMP hardening design by analysis. In addition, they represent equipment which is, in fact, mission critical to some extent. Examples are presented to show EMP consideration only. These hardening techniques treat EMP specification and functional requirements in detail. However, only peripheral attention is given to other system parameters such as cost and weight and no attention is given to other nuclear effects such as TREES. As a result, they should not be construed as recommendations for the actual subsystem considered.

CHAPTER 10

UPSET HARDENING EXAMPLE

1. SYSTEM DESCRIPTION

The circuit selected as an example of upset hardening is taken from the Inertial Electronics Unit (IEU). This unit receives signals from a set of inertial sensors in an Inertial Measurement Unit (IMU). The inertial data received by the IEU are transferred to an on-board computer for purposes of inertial navigation. A small amount of preprocessing of the inertial sensor data is carried out within the IEU. Some subsidiary functions, such as driving cockpit displays, are also carried out. The IEU is utilized in the B-52 aircraft as a part of the SRAM support equipment. In this application, it interfaces between the IMU and the computer associated with SRAM missile guidance and firing. The IEU is currently being modified for use in the B-1 aircraft. In this application, it will serve as a portion of the navigation system for the B-1 itself.

A block diagram of the IEU is shown in Figure 10-1. The circuitry for the hardening example is taken from the accelerometer counter section. Accelerometer sensors measure acceleration, the second derivative of position information. In order to convert these data to position information required for aircraft navigation, it is necessary to carry out two integration steps on the accelerometer data. The first integration is carried out within the Inertial Electronics Unit. Pulses representing 0.1 ft/sec velocity increments are received from the IMU and accumulated in the accelerometer counter section. This accumulated velocity change is transferred out on request. When a transfer takes place, the accumulated velocity counter is reset to zero and begins accumulating changes in

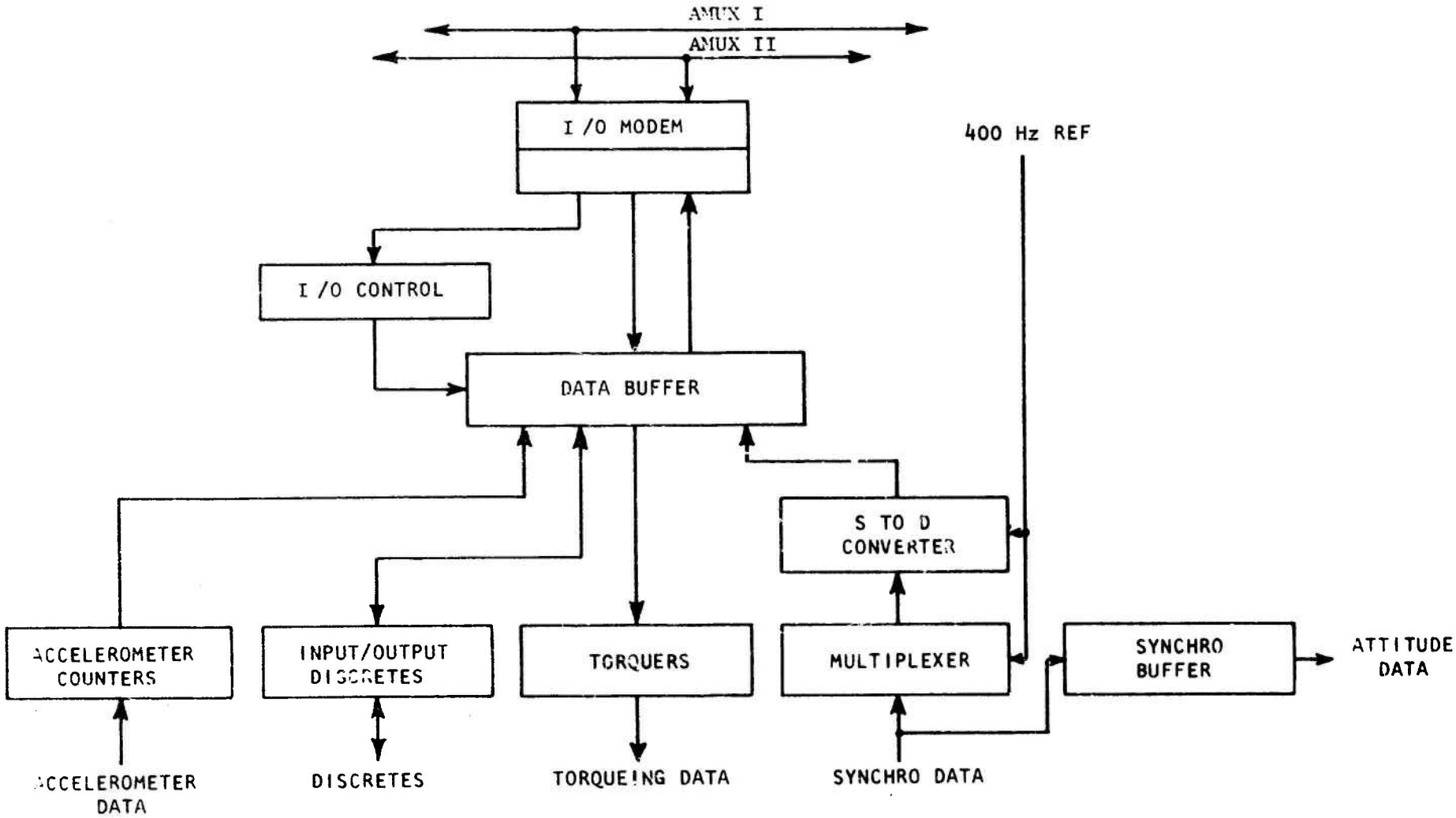


Figure 10-1. Inertial Electronics Unit Block Diagram

velocity again. By the very nature of integrated data, it is obvious that an error in the accumulation of velocity increments will cause a permanent error in the velocity value utilized from that time on. This will cause an ever increasing position error. For this reason, integrated data of this type are particularly susceptible to upset since a momentary error in the operation of the accumulator renders the final position data erroneous from that time on unless the position and velocity figures are reset by some completely independent means. As a general rule, the only adequate means of resetting the velocity and position data to the accuracy specifications of the inertial system is to land the aircraft and set these parameters while the aircraft is stationary at a known location on the ground. The specific portion of the IEU selected for the upset example is the accelerometer counter which is shown along with some related circuitry in the logic diagram for the X Accelerometer Counter and Register card (see Figure 10-2).

The X Accelerometer Counter and Register card contains the X velocity counter for accumulating the input velocity increments and the shift register required to transfer the accumulated X velocity to other portions of the IEU when requested by the computer. In addition, this card contains some control logic utilized both for the X Accelerometer Counter and Register and for the Y and Z accelerometer counters and registers contained on another circuit card. Since the control logic required for the circuitry for all three axes of accelerometer data is contained on this circuit card, the card will be utilized throughout this analysis. Changes to the control logic will impact the circuitry for all three axes of accelerometer data. Changes to the circuitry uniquely associated with the X accelerometer data can be applied identically to the circuitry for the Y and Z accelerometer data.

Table 10-1 gives a summary of the functional specifications of the IMU and IEU that are specifically related to the operation of the accelerometer counters. These specifications determine the constraints

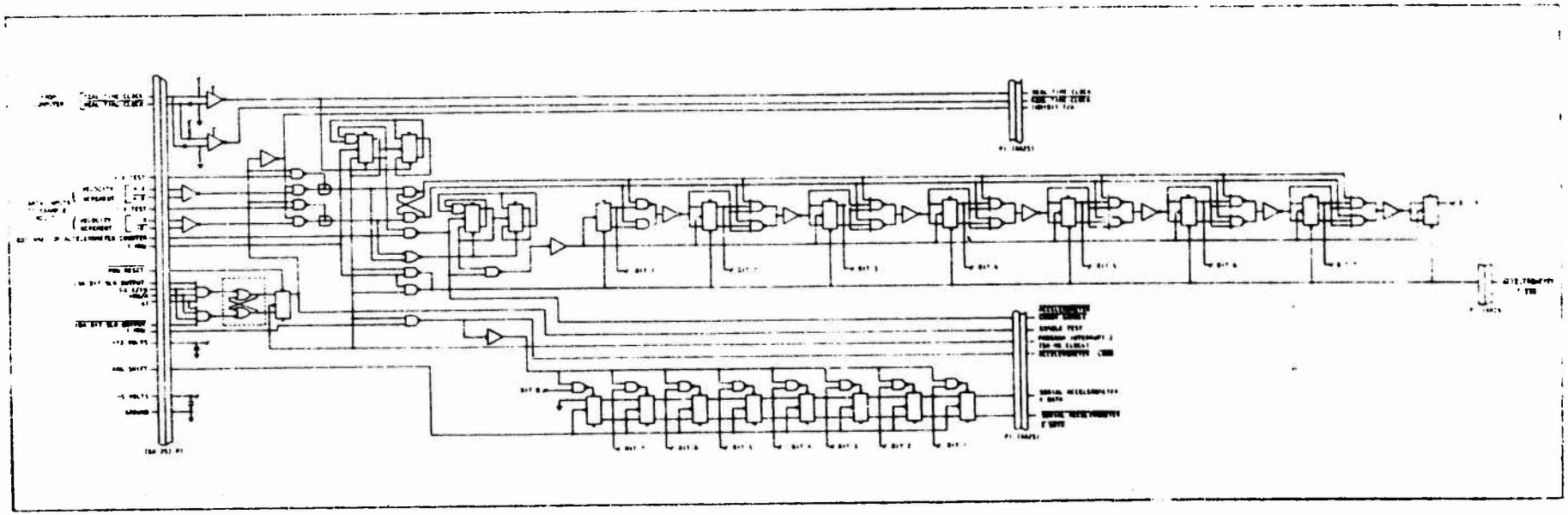


Figure 10-2. Logic Diagram X Accelerometer Counter and Register

TABLE 10-1

SPECIFICATIONS RELATED TO ACCELEROMETER COUNTERS

Velocity Increment Signals	
Active state pulse width	= 100 to 200 μs
Max pulse rate	= 2.6 K pps
each pulse	= 0.1 ft/sec velocity increment
Velocity Increment Signal Source Characteristics	
Source impedance (each side of twisted pair)	= 100 Ω
With a 510 Ω load on each side:	
high level	= 3.7 V ± 1 V
low level	= 0 V ± 1 V
IEU Specifications	
Max error rate	= 1 pulse/min = (0.1 ft/sec)/min
Minimum frame length (before integration and clear by computer)	= 62.5 ms
Line Receiver Circuit	
Maximum differential input required to establish desired output	= 0.5 V

under which hardening design changes must be accomplished. The changes to the design of the equipment must accommodate the requirements to operate with velocity increment signal pulses as narrow as 100 microseconds at repetition rates from zero to 2.6 K pps. The source characteristics specified for the velocity increments signals provide signal level specifications for load impedances as low as 510 ohms. Although it may be possible to load the signal sources down more than this, there is no guaranteed signal level specification for lower load impedances and thus the 510 ohm load has been taken at a minimum permissible dc load. Transient loading at lower impedances than 510 ohms must be analyzed to determine the impact of risetime of the velocity increment signals. The allowed drift rate or error rate is one pulse per minute for the IEU operation and this is primarily caused by quantization errors.

2. FAILURE MODES

The only signal lines to this circuit card which originate outside the IEU are the velocity increment inputs. These signals are routed through the aircraft cabling and thus exposed to EMP. Since these represent interface circuits, they are of primary concern in the EMP susceptibility analysis. It is assumed in this example that good packaging design has been implemented (see Chapter 5). Good packaging and grounding design is necessary to justify the assumption that the only point of entry for EMP interference to the accelerometer counters is in fact the interface for the velocity increment signals. Since this example is concerned primarily with upset, the problems of damage hardening the line receivers is not discussed. Some techniques for damage hardening the line receivers are examined extensively in the damage hardening examples in Chapter 11. The first step in analyzing this problem is to trace the consequences of erroneous data received at the velocity increment inputs. For convenience in the analysis, the signals at pin ten and pin four of E22 will be discussed (see Figure 10-3a).

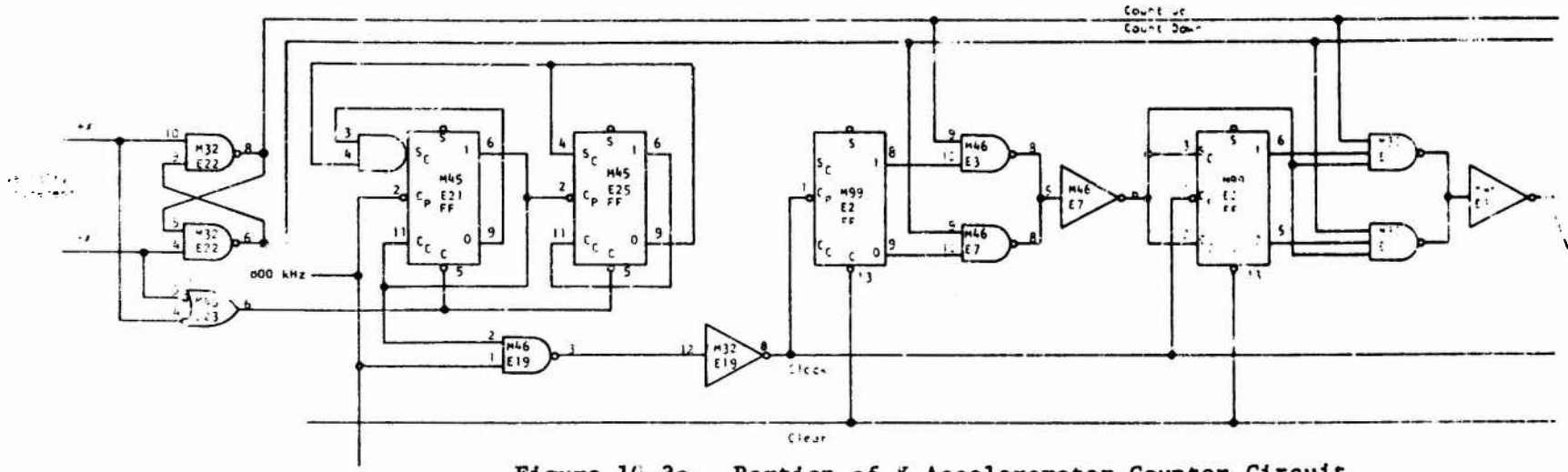
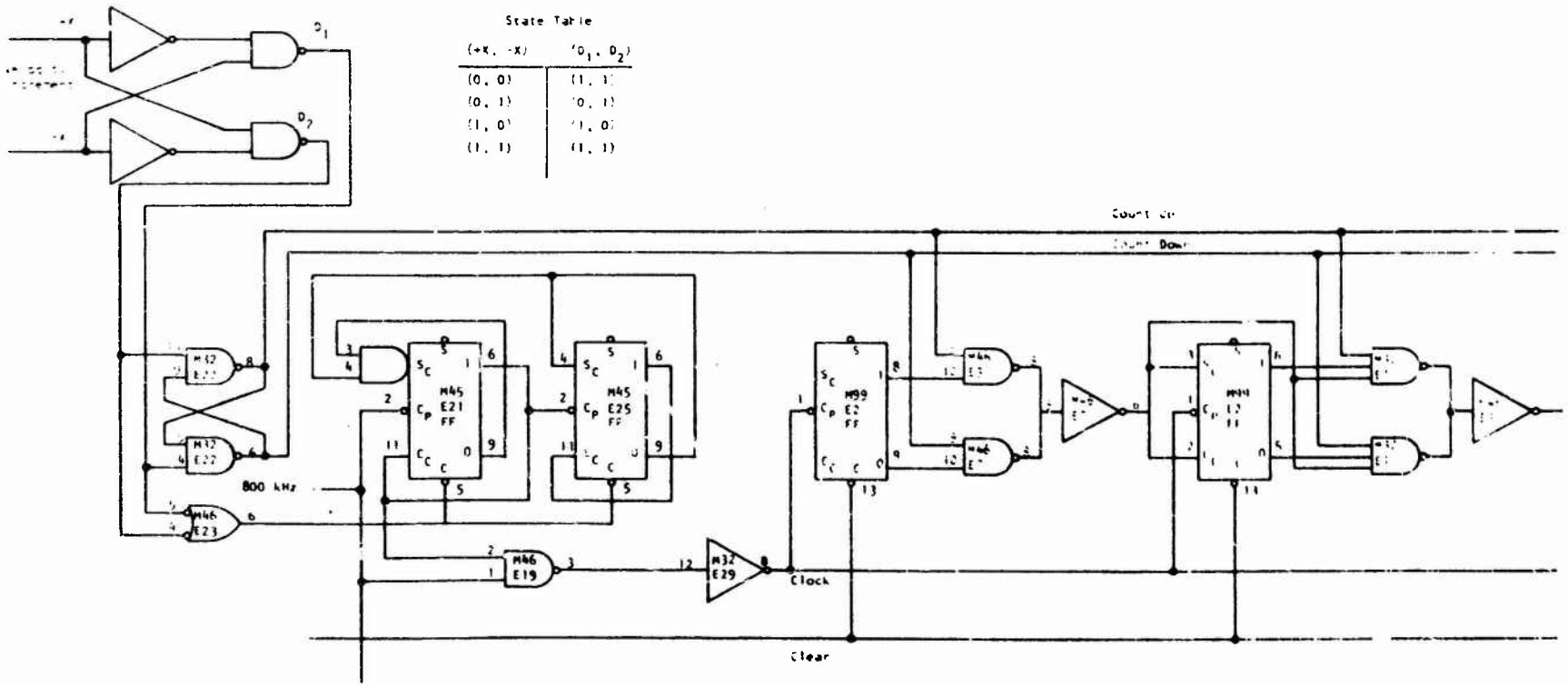


Figure 10-3a. Portion of X Accelerometer Counter Circuit



State Table

(+X, -X)	(D_1, D_2)
(0, 0)	(1, 1)
(0, 1)	(0, 1)
(1, 0)	(1, 0)
(1, 1)	(1, 1)

Figure 10-3b. Circuit Hardened to Prevent Erroneous 0,0 Data

These represent the velocity increment signals whenever the IEU is in the normal mode of operation (not in test mode). Table 10-2 shows the velocity increment signals that may be received and the possible result of interference on these signals. All combinations of a "1" or a "0," resulting from interference on the +X and -X signals are considered. The velocity increment signals are normally 1,1 whenever no velocity increment is indicated. A zero pulse on the +X signal indicates an increase of 0.1 feet/second in velocity. A zero pulse on the -X signal indicates a decrease of 0.1 feet/second velocity. Simultaneous zeros on both the +X and -X signals cannot occur since this would represent a simultaneous increase and decrease in velocity and the IMU will not produce these signals when operating normally. Thus, there are three possible velocity increment signal states as shown in Table 10-2. The possible erroneous data resulting from interference are also shown in this table. For each of the three possible signals, there are three possible erroneous data sets that may be received when EMP interference occurs.

The consequences of the erroneous 0,0 state (Class I errors) which may occur with any of the three signal inputs will be examined first. It should be noted that a zero state on either the +X or -X line will remove the clear signal from flip-flops E21 and E25. When this clear signal is released, these flip-flops will produce a single clock pulse for the X accelerometer counter synchronized with the 800 kHz input. When a 0,0 state is present in the velocity increment signals, the countup and countdown signals will both be logic one, and a clock pulse for the accelerometer counter will be produced. It can be seen in Figure 10-3a that simultaneous one states on countup and countdown lines will enable gates E3, pin 8 and E7, pin 8. Since there must be a one state on either the one or zero output of flip-flop E2, pins 8 and 9 the S_C and C_C inputs (E2, pins 3 and 2) to the next flip-flop will be at a one state. The same situation will occur on

TABLE 10-2

STATE DIAGRAM SHOWING THE POSSIBLE INFLUENCE OF INTERFERENCE ON RECEIVED DATA

	TRANSMITTED SIGNAL	RECEIVED SIGNAL + INTERFERENCE							
	+X,-X	0,0	1,1	0,1	1,0	+X,0	+X,1	1,-X	0,-X
No Change	1,1	0,0	~~-1,1-~~	0,1	1,0	1,0	~~-1,1-~~	~~-1,1-~~	0,1
+0.1 Ft/Sec.	0,1	0,0	1,1	~~-0,1-~~	1,0	0,0	~~-0,1-~~	1,1	~~-0,1-~~
-0.1 Ft/Sec.	1,0	0,0	1,1	0,1	~~-1,0-~~	~~1,0--~~	1,1	~~-1,0-~~	0,0
Not allowed	0,0								

THESE ENTRIES SHOW THE RESULTING STATES OF THE DATA

NOTE: Correct entries have been crossed out showing the remaining erroneous entries.

the inputs to all of the remaining flip-flops in the X accelerometer counter. Thus, the clock signal will cause this counter to complement the value it has accumulated up to this point. Since this is an 8 bit counter and a one's complement occurs, the new value could be wrong by as much as 255. This represents a velocity error of 25.5 feet/second or about 18 miles per hour. It is obvious that if the computer accepts these data for updating its X velocity value, the indicated position of the aircraft will drift farther and farther from the actual position at a constant rate. This will continue until the velocity value stored in the computer is corrected by some independent determination of velocity. This obviously represents a very serious EMP upset mode and essentially renders the inertial navigation useless until it can be reinitialized.

The next group of errors (Class II errors) to be considered includes those cases where a 1,0 or a 0,1 is received when the actual signal is 1,1. In these cases, an erroneous negative or positive velocity increment will be counted. This causes permanent upset of the accumulated X velocity value. In this case however, the error may be rather small. Each erroneous count causes an error of 0.1 feet/second. The total error resulting from a burst of EMP interference depends upon the algebraic sum of all erroneous counts introduced by a burst of interference. (Further analysis is made elsewhere.)

The third upset case (Class III errors) includes all remaining interference errors. These are the cases where a signal indicating a plus or minus velocity increment results in data indicating either no velocity increment (1,1) or a velocity increment of the opposite polarity to that indicated by the actual signal as originally transmitted. This case causes accumulated velocity errors of 0.1 or 0.2 foot/second for every erroneous data set and again the total error depends on a summation of all the erroneous data sets produced by a given EMP burst of interference.

3. HARDENING DESCRIPTION

Based on the results of the examinations of failure modes for the accelerometer counters, two basic requirements for the hardening design can be established. First it is necessary to completely eliminate the possibility of complementing the accelerometer counter as a result of a 0,0 data set. The errors resulting from this type of upset can be so large that even a small probability of occurrence cannot be tolerated. The second requirement is to reduce the probability of the remaining types of errors (single count and double count errors) to the point where their total contribution to velocity error is significantly smaller than the one pulse per minute error specification for the IEU. It is obviously desirable, but not necessary, to completely eliminate this type of error. Because of the damped sinusoid nature of the EMP interference, it is reasonable to expect that a single EMP interference burst may induce a series of these errors. As a result, any technique which simply blanks normal operation for the entire period of the EMP interference is not likely to produce satisfactory results. Therefore, techniques such as circumvention or the use of input suppression devices (which might be useful for damage hardening), have been avoided in favor of techniques which will allow normal operation to some extent during the actual period of time when EMP interference is present.

a. Prevention of Complement Errors

The first task in upset hardening of this equipment will be the prevention of those cases where a 0,0 data set is received. This is the most serious case since it can cause a very large velocity error resulting from a single erroneous data set. In this case, the technique of parameter constraint analysis will be utilized because a 0,0 data set indicates a simultaneous increase and decrease in velocity which is obviously unrealistic. Since a 0,0 data set cannot possibly be a real signal, the circuitry can be modified to prevent any response at all

to the reception of such a data set. Figure 10-3b shows a modification to the logic circuitry to prevent response to a 0,0 data set. The signal lines to E22, pins 10 and 4 and to E23, pins 4 and 5 have a set of two inverters and two gates inserted as shown in Figure 10-3b. The state table shows how the data have been modified by the additional gates and inverters. The only change in the data is that when a 0,0 is received it will produce a 1,1 result. This result will prevent any change in the state of the remaining circuits. The countup and countdown signals will remain unchanged and no clock pulse to the accumulator will result; therefore, accumulator count will remain unchanged. This completely eliminates the possibility of ever complementing the value of the X accelerometer counter, because a 0,0 state on the D_1, D_2 signals is not possible. An examination of the additional gate and inverter configuration will also show that no timing races exist which might create a momentary 0,0 state.

b. Input filters

Table 10-3 shows the relationship between the states marked D_1 and D_2 with given signal inputs and with signals subjected to interference. All erroneous data sets now represent data which could be real [(1,1), (0,1), (1,0)] and they can therefore not be rejected by inspection of their value. The next alternative considered is to prevent reception of the interference.

The velocity increment signals are zero state pulses on the +X or -X lines respectively. Their duration is between 100 and 200 microseconds and the maximum pulse rate is 2.6 K pps. Figure 10-4 shows a maximum acceleration velocity increment signal, the form of a typical EMP interference signal, and the EMP frequency range. The EMP interference information is taken from the B-1 specification and is likely to be similar to the form of EMP specifications applied to

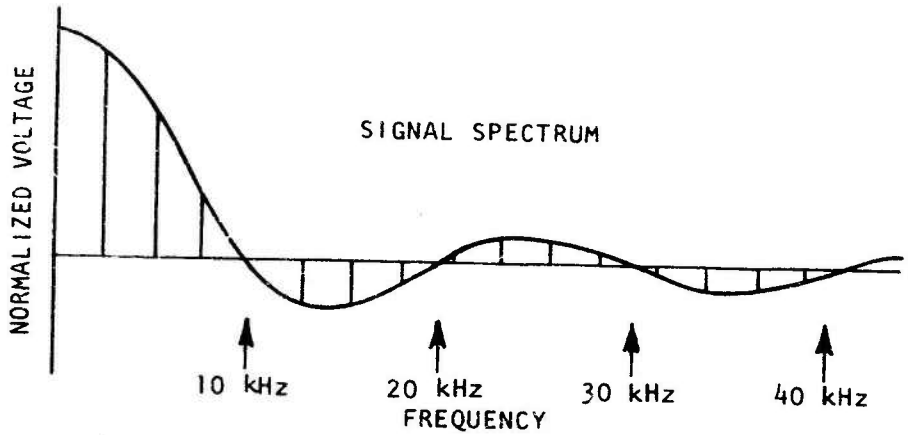
TABLE 10-3

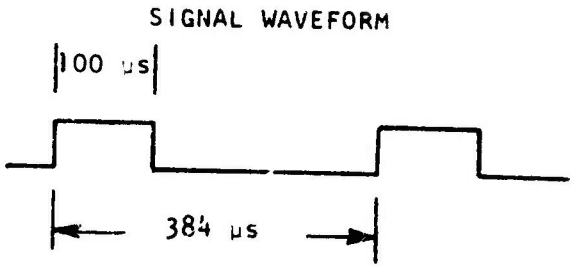
STATE DIAGRAM SHOWING THE POSSIBLE INFLUENCE OF INTERFERENCE ON D_1, AND D_2 DATA WITH MODIFIED CIRCUIT

	TRANSMITTED SIGNAL	RECEIVED SIGNAL + INTERFERENCE							
	+X,-X	0,0	1,1	0,1	1,0	+X,0	+X,1	1,-X	0,-X
		CLASS II ERRORS							
No Change	1,1	~~1,1~~	~~1,1~~	0,1	1,0	1,0	~~1,1~~	~~1,1~~	0,1
+0.1 Ft/Sec.	0,1	1,1	1,1	~~0,1~~	1,0	1,1	~~0,1~~	1,1	~~0,1~~
-0.1 Ft/Sec.	1,0	1,1	1,1	0,1	~~1,0~~	~~1,0~~	1,1	~~1,0~~	1,1
Not Allowed	0,0	CLASS III ERRORS							

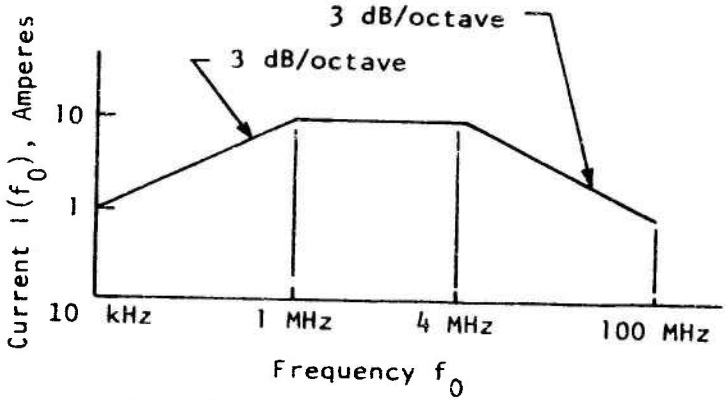
THESE ENTRIES SHOW THE RESULTING STATES OF D_1 AND D_2

NOTE: Correct entries have been crossed out showing the remaining erroneous entries.

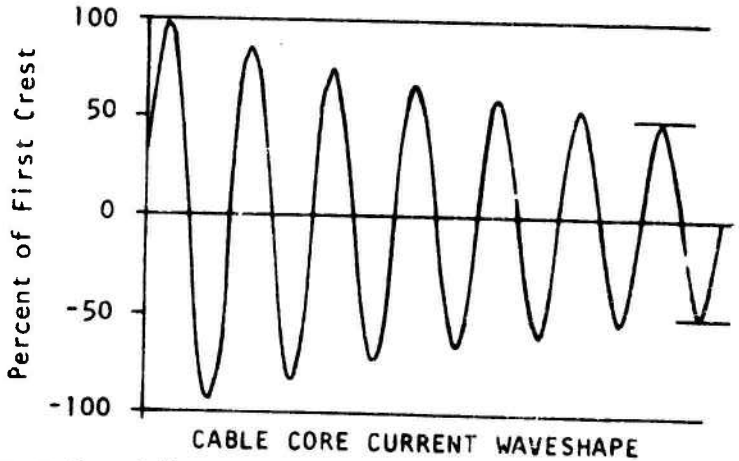




(a) 2.6 K pps Velocity Increment Signal



Peak Core Current Requirement
for General Electronic Equipment



(b) EMP Interference Test Specifications for
B-1 Mission Critical Avionics

Figure 10-4. Data and EMP Interference Signals

other equipment in the future. It is evident from the velocity increment spectrum that most of the signal energy falls at or below about 16 kHz, whereas the specified EMP spectrum falls between 10 kHz and 100 MHz. The conclusion from this is that a major portion of the EMP interference energy may be rejected through the use of filters without seriously degrading the signal. Thus, input filters are recommended for the velocity increment signals. These filters will substantially reduce the probability that interference will result in erroneous received data, but will not totally eliminate the problem.

The filter design selected is shown in Figure 10-5. Filter pin connectors were rejected as a possibility because of the very low cutoff frequency required. At such low cutoff frequencies, the available filter pin connectors give marginal saturation and spectral response characteristics for this application. The filter selected was a simple RC filter. This appears to be adequate for the purpose, and cost-effective. More complex filters could be adopted with better results, but they would result in significantly greater cost. The RC filter has a cutoff frequency of 8.2 kHz. The 100 microsecond minimum pulse width for the velocity increment signals is approximately five times the duration of the filter time constant. Thus, there is sufficient time to establish the logic levels between transitions of the velocity increment signal. Some degradation in risetime does occur but this does not impair the performance of the system in any way. In addition to the RC filter, a 510-ohm load to ground is included. This accomplishes two results. First, since the specified EMP signal is a constant current source, 510 ohms shunts a significant portion of the interference signal to ground without loading down the source signal to an unreasonable degree. In addition, the 510 ohms provides a closer match to the twisted pair line impedance (≈ 200 ohms) and, thus, reduces spectral peaks due to ringing of an improperly terminated transmission line. This reduces the maximum voltages that occur at line resonances. It would obviously be best to terminate the transmission line

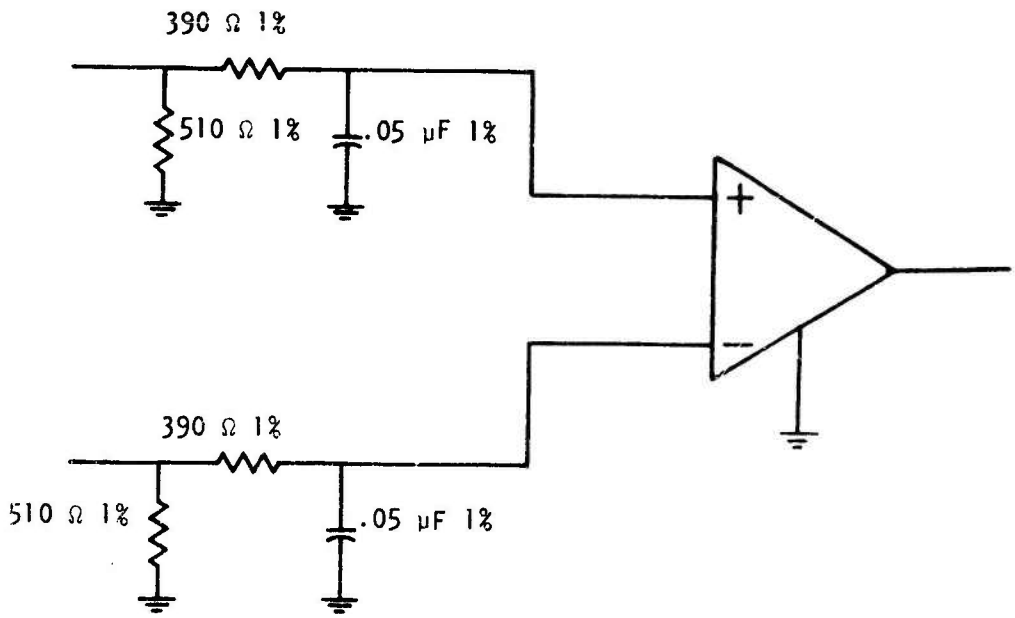


Figure 10-5. Line Receiver Input Filters

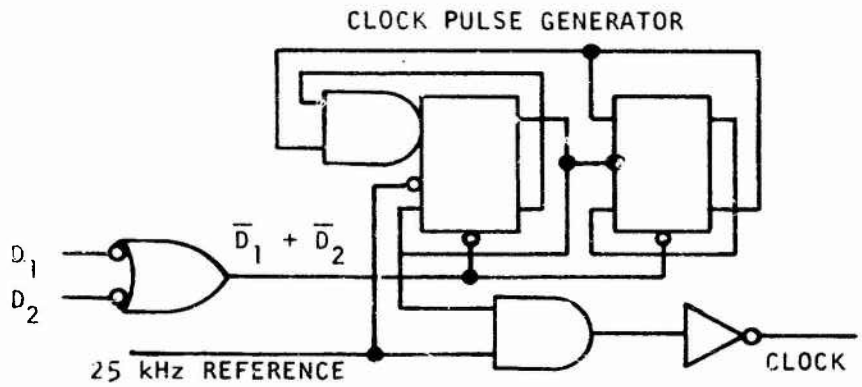
in its characteristic impedance to eliminate resonances almost completely. In this case, however, the specifications of the signal source constrain the load to a minimum of 510 ohms on each line of the twisted pair and thus this value was selected.

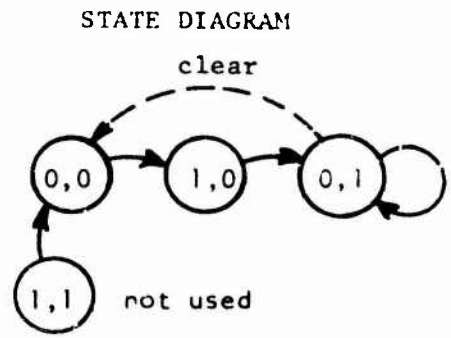
c. Time Discrimination

One other possibility for reducing the probability of erroneous received data as a result of EMP interference is available. The maximum pulse rate for velocity increment signals is 2.6 K pps. This corresponds to the maximum acceleration on any axis that the inertial navigation equipment is designed to accommodate. It is obvious however, that during the major portion of any flight, the acceleration will be substantially lower than this value and the resulting velocity increment pulse rate will also be substantially lower. With the pulse width of 100 or 200 microseconds, it is obvious that for a majority of the time, a 1,1 signal will be present. Suppose it were possible to detect all cases of interference and always produce a 1,1 signal on D_1 and D_2. In this case, interference would never cause erroneous results when a 1,1 signal was present, but would always cause erroneous results when a velocity increment pulse was present during EMP interference. Since the signal is a 1,1 the majority of the time, this would substantially reduce the overall probability of error resulting from EMP interference. No way has been found to detect EMP interference in all cases; however, a method has been found to detect EMP interference in a majority of cases. Since the signal pulses representing velocity increments are between 100 and 200 microseconds in duration, it is possible to reject pulses of 0 state on either the +X or -X signal line when their duration is shorter than 100 microseconds. If all pulses shorter than about 100 microseconds duration are rejected, then the majority of interference pulses will be rejected. However, when interference causes a real signal velocity

increment pulse to be eliminated or shortened in duration (by summing with a short duration interference pulse of the opposite polarity) then these signal pulses will be interpreted incorrectly whereas they might have been correctly interpreted if short pulses had not been ignored. Thus, this technique will reduce the probability of erroneous data from interference during a 1,1 signal state at the expense of increasing the probability of erroneous data due to interference during a 0,1 or a 1,0 signal state. The net result, however, is an overall reduction in the probability of error resulting from EMP interference.

The EMP damped sinusoid waveform may produce a series of errors in one burst, (particularly at the lower end of the EMP spectrum), and the majority of these will occur during a 1,1 signal state. Thus, the total number of errors resulting from one burst from EMP interference will be reduced by rejecting short zero state pulses on the signal lines. Figure 10-6 shows how a modification to the existing circuitry will accomplish this rejection of short pulses. The state diagram of the circuitry utilizing flip-flops E21 and E25 shows that a clock pulse to increment the X accelerometer counter will occur only if the zero state data signal is present for some minimum period of time. This minimum is at least as long as the zero state of the reference for the accelerometer counter and may be as long as one cycle of the reference state for the counter plus the duration of the zero state of the reference for the accelerometer counter. Selection of an appropriate reference frequency and duty cycle for the reference for the accelerometer counter can accomplish the rejection of all pulses shorter than a given time duration. If the reference for the accelerometer counter is in a zero state for the major portion of its cycle, then the duration required on a zero state signal in order to accomplish the creation of a clock pulse for the accelerometer counter will vary, between essentially one and two periods of the reference for the accelerometer counter, depending on the timing of the reference and the velocity increment zero state pulse. Without revision of the





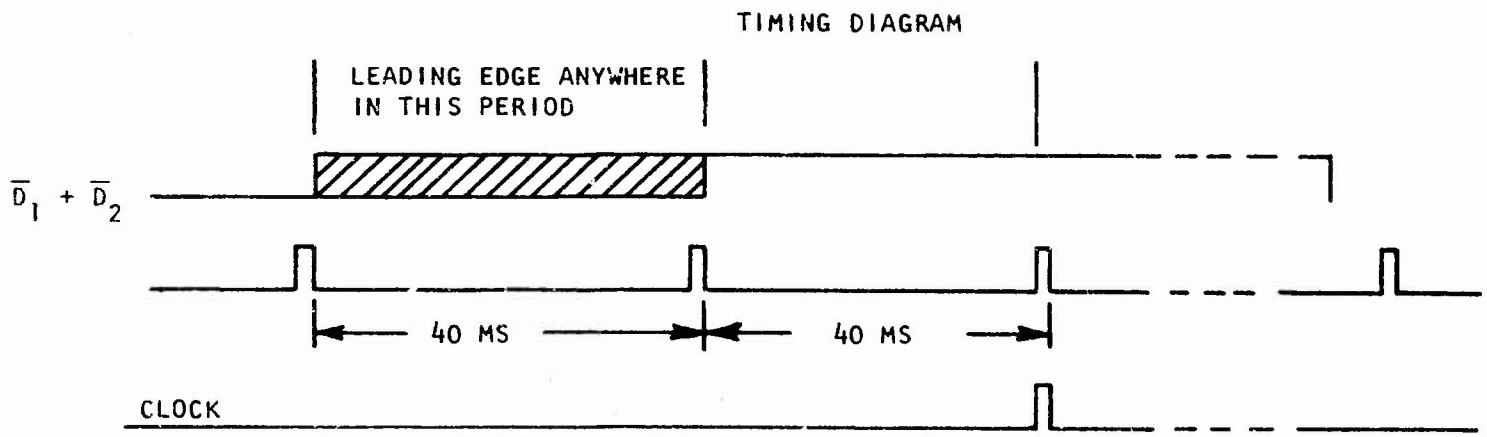


Figure 10-6. Clock Pulse Generator Operation with 25 kHz Reference

synthesizing circuitry within the IEU, 800 kHz and 100 kHz reference signals are available. Figure 10-7 shows additional circuitry which can be utilized to provide a 25 kHz reference for the accelerometer counter with a very low duty cycle. With this signal utilized as a reference for the accelerometer counter, pulses will be rejected if their duration is less than 40 to 80 microseconds depending on the time relationship between the reference and the zero state velocity increment signal pulses. Since normal velocity increment pulses have a minimum duration of 100 microseconds, they will not be rejected.

d. Complete Hardened Design

At this point, the combination of all techniques to reduce the probability of upset resulting from EMP interference of the Class 2 and Class 3 types is considered. First, the existing line driver, line receiver interface utilizing twisted pair lines can be expected to reject pick-up of EMP interference in accordance with the spectral response shown in Figure 10-8. Second, low pass filtering through the use of RC filters can be expected to reject EMP interference in accordance with the spectral response shown in Figure 10-8. The decay time of the damped sinusoid EMP interference is long enough to treat it as a pure sine wave for interface analysis. It is important to note that at the low frequency end of the EMP spectrum where low pass filtering cannot substantially reduce the interference, the attenuation of interference resulting from the use of twisted pair cabling is at a maximum. Thus, the filter and twisted pair techniques complement each other very well. Errors which remain in spite of these two techniques have a reduced overall probability of causing upset by the requirement for 40 to 80 microseconds pulse durations even though the probability of Class III errors is somewhat increased. The combination of these three techniques can be expected to reduce the probability of upset to an extremely low and, therefore, acceptable figure In addition, the combination of all hardening

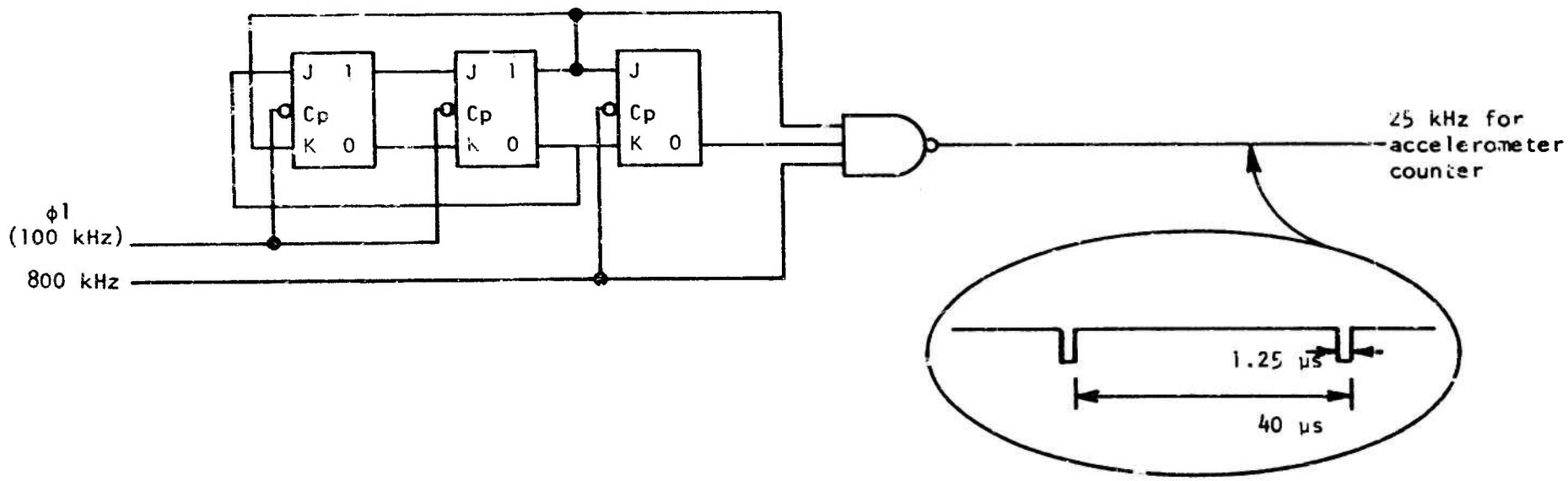


Figure 10-7. Synthesizer for 25 kHz for Accelerometer Counter

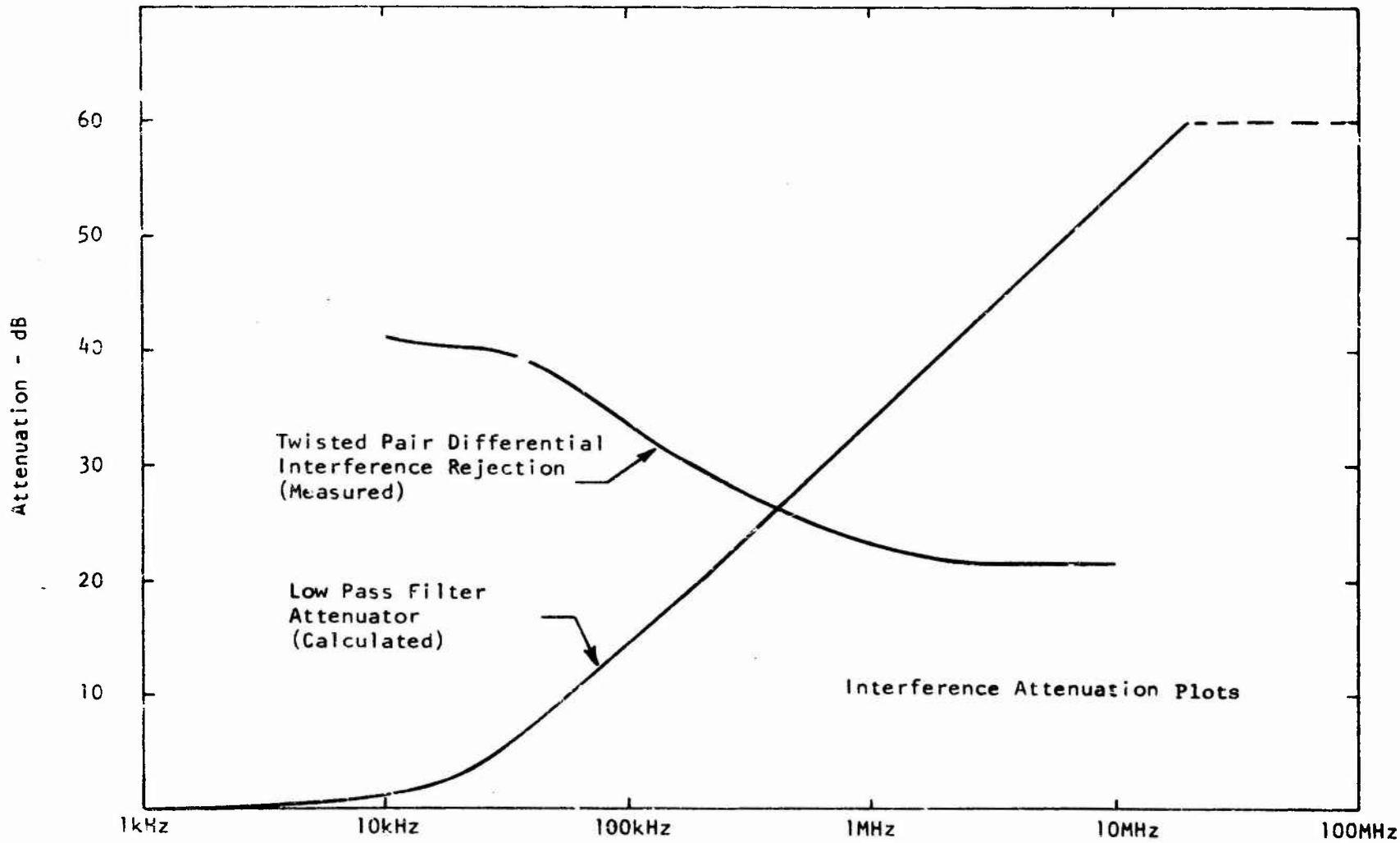


Figure 10-8. Spectral Response

techniques employed in this example will assure that upset, if it does occur, produces relatively small accumulated velocity errors.

4. ASSESSMENT OF PERFORMANCE

The performance of hardening design can be determined either by test or analysis or a combination of the two. In this example, the actual equipment being considered was not available for test; therefore, the assessment of the performance of the hardening procedures was carried out entirely by analytical methods and by computer simulation. Although this example is primarily to illustrate upset hardening, it is obvious that a complete hardening program must consider both upset and damage and the results of the damage hardening examples are referenced simply to show that the hardening techniques employed in this example are sufficient to prevent damage as well as upset.

a. Analysis

It should first be noted from the hardening description previously discussed that the problem created by 0.0 data sets is completely eliminated by the modification shown in Figure 10-3b. Simple logic analysis clearly illustrates this point.

The remaining problems are to determine the performance of the combination of input filtering, the use of twisted pair differential data lines, and the application of time discrimination illustrated in Figure 10-6. In the actual circuit as configured for the B-1 application, the velocity increment signals are contained in a multiconductor cable with a large number of conductors. The analysis was carried out in two ways to illustrate the range of the EMP problem of this type that might be encountered. First, analysis was performed assuming a 45-conductor cable with a random selection of loads on the various lines.

The actual cable in question contains slightly more than 49 conductors, but this was the largest number of conductors for which parameters could be determined conveniently using GEOPRM1 (Reference (1)). This furnishes an example very close to the real situation with the current cabling configuration proposed for the B-1 application. By contrast, analysis was also carried out based on the assumption that each velocity increment twisted pair signal line was in fact a separate cable. This is essentially a worst case since all of the cable core current is now applied to a single twisted pair.

Before examining the impact of interference signals on the performance of the hardened system, it is necessary to determine the thresholds at which the line receiver will be induced to an erroneous output state. The source specifications are shown in Table 10-1. From these specifications, it can be seen that when the differential signal lines are loaded with 510 ohms, there is a minimum differential signal of 1.7 volts and a typical differential signal of 3.7 volts. The maximum differential input threshold to assure a desired state in the line receiver is 0.5 volt. Thus, if differential interference alone is to create an erroneous state in the line receiver, the differential signal must be at least 1.2 volts. The typical differential interference required to create an erroneous state will be about 3.7 volts. Figure 10-9 shows that common mode voltage can induce an erroneous zero state output of the line receiver under some conditions, but can never induce an erroneous one state.

If it is assumed that the worst case conditions of line driver signal levels, line receiver input thresholds, and differential interference of about 0.7 volt peak are present, then the differential signal drive will be about 0.5 volt. Under these conditions, the common mode voltage of about 16 volts (or 25 dB above one volt) is necessary to create an erroneous zero state output. This common mode voltage is taken as the worst case common mode susceptibility. With typical conditions and about

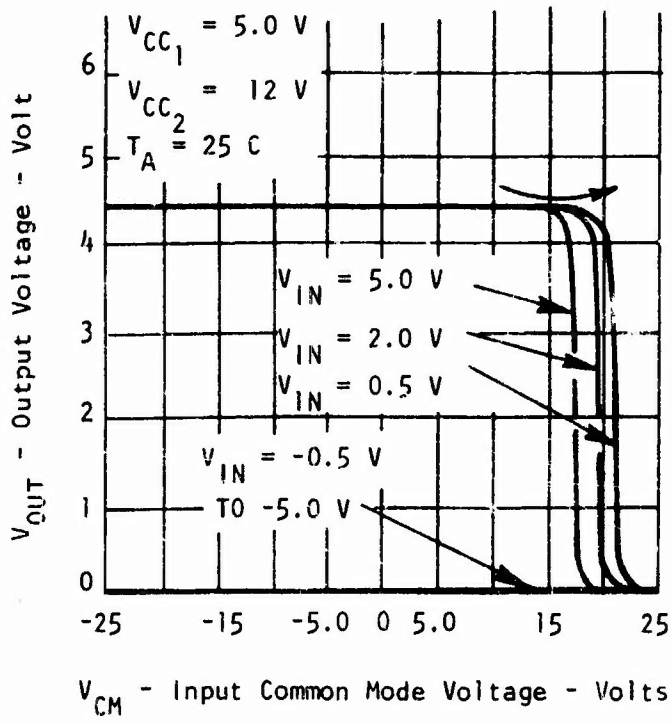


Figure 10-9. Line Receiver Response to Common Mode Input

1.2 volts differential interference, the common mode voltage required to create an erroneous zero state output is about 20 volts or 26 dB. These conditions are assumed to represent the worst case and typical thresholds for erroneous response in the line receiver. The purpose of the input filters is to reduce the common mode and differential interference signal below these values over as much of the EMP interference spectrum as possible.

The next step in the analysis is to determine the actual voltages present at the inputs to the line receivers when the cable is driven with the B-1 specification EMP signals. This determination of voltage was carried out using the TRAFFIC (Reference (2)) cable analysis program.

Using the program GEOPRM1, (Reference (1)) twisted pair parameters, L, C, M, and R per unit length parameters were generated. The individual wires are AWG #20 with an insulation covering that has an effective relative dielectric constant of 2.9. The 32-foot twisted pair was laid on the ground plane.

In the second case, the cable bundle was composed of 49 AWG #20 conductors with an insulation covering that has an effective relative dielectric constant of 2.9. The cable is 32 feet long and suspended two inches above the around plane with no external or internal shields. The individual wires are laid somewhat randomly in the cable so their relative position varies with the transverse axis. The per-unit length parameters were again generated from the geometric physical parameters by GEOPRM1.

Both cables were analyzed over the B-1 specification frequency range (10 kHz to 100 MHz) using TRAFFIC. Random individual conductor resistive loads, ranging from 1 ohm to 10 K ohms, were used as cable terminations for both the input and the output. The individual conductors used for determining the voltage levels at the example circuit input were

chosen so they had a 100-ohm termination at the source to match the velocity increment signal source impedance specification. These same conductors were evaluated for terminations at the load end representing unhardened conditions and hardened conditions. The hardened conditions include a shunt resistor and filter. This was done for both the twisted pair and 49-conductor bundle. The terminations at the source end of the cables were tied to a common point at the top of the current source. This technique assures a fixed common mode current at all frequencies. All TRAFFIC output was obtained using a one amp common mode current source.

The results of the TRAFFIC Cable Analysis utilizing a one amp current source were then modified to reflect the variation in current source as a function of frequency as shown in Figure 10-4b. Finally, the typical common mode rejection twisted pair lines presented in Chapter 8 and repeated in Figure 10-8 were utilized to determine the differential mode voltage that would result from the filtered common mode voltage. All of these results are shown in Figures 10-10 and 10-11.

Figure 10-10 shows the results of the TRAFFIC analysis of the signal lines when contained in a 49-conductor cable. The unfiltered voltage curve shows the voltage applied to the input of the line receiver circuit when no filtering is applied to the signal line. It is obvious that the common mode signal exceeds 24 dB or 16 volts throughout that portion of the spectrum above 150 kHz. Thus, in that region, erroneous data will result from the EMP interference and upset will occur if no hardening measures are taken. The filtered input curve shows the voltage on the input terminal of the line receiver when the hardening filter is utilized. In this case, the entire spectrum produces input voltages below -5 dB or .56 volt. Thus, the common mode voltage is well below the value at which upset can be induced in the line receiver by excessive common mode voltage.

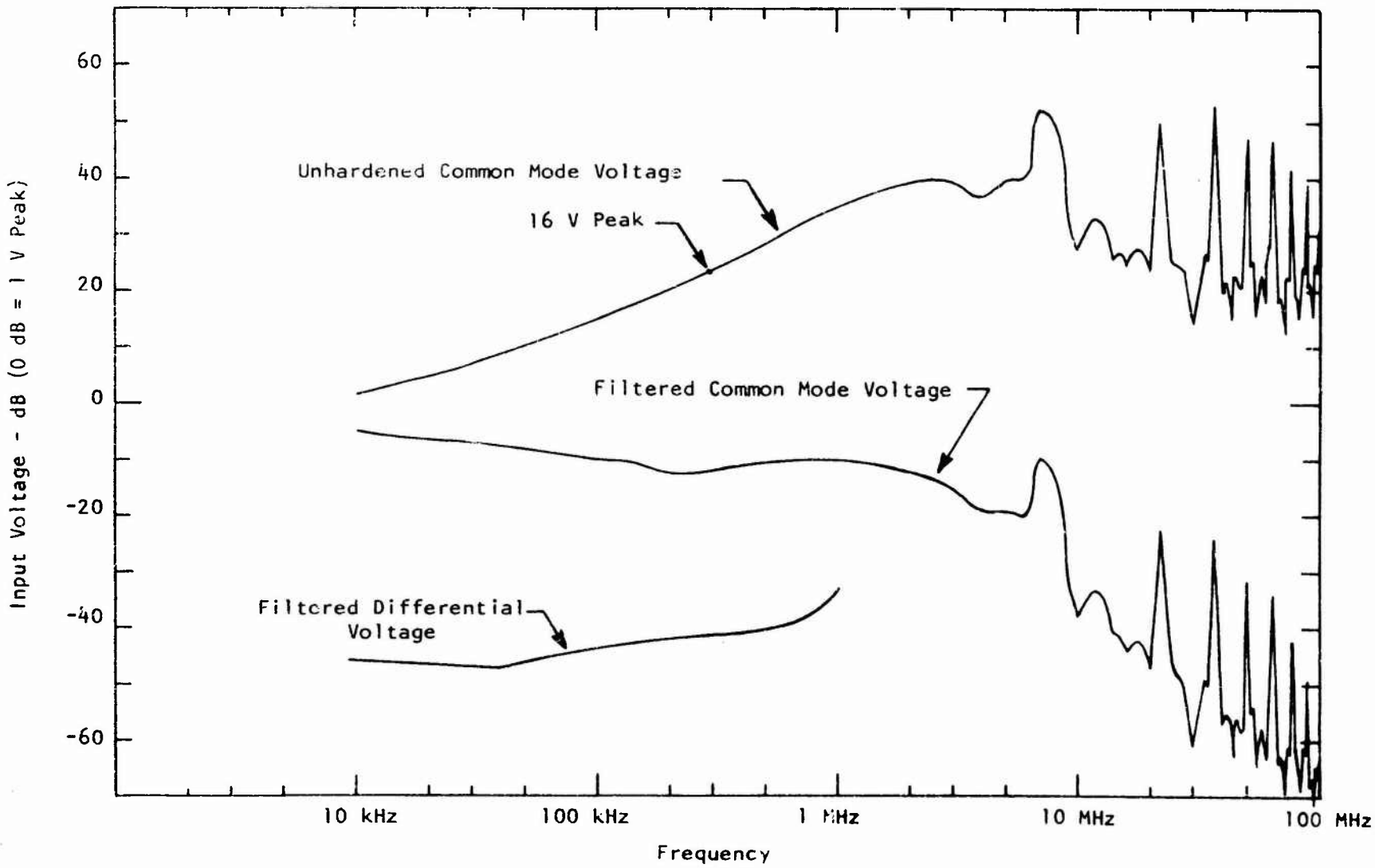


Figure 10-10. Line Receiver Input Voltage from EMP with 49-Conductor Cable

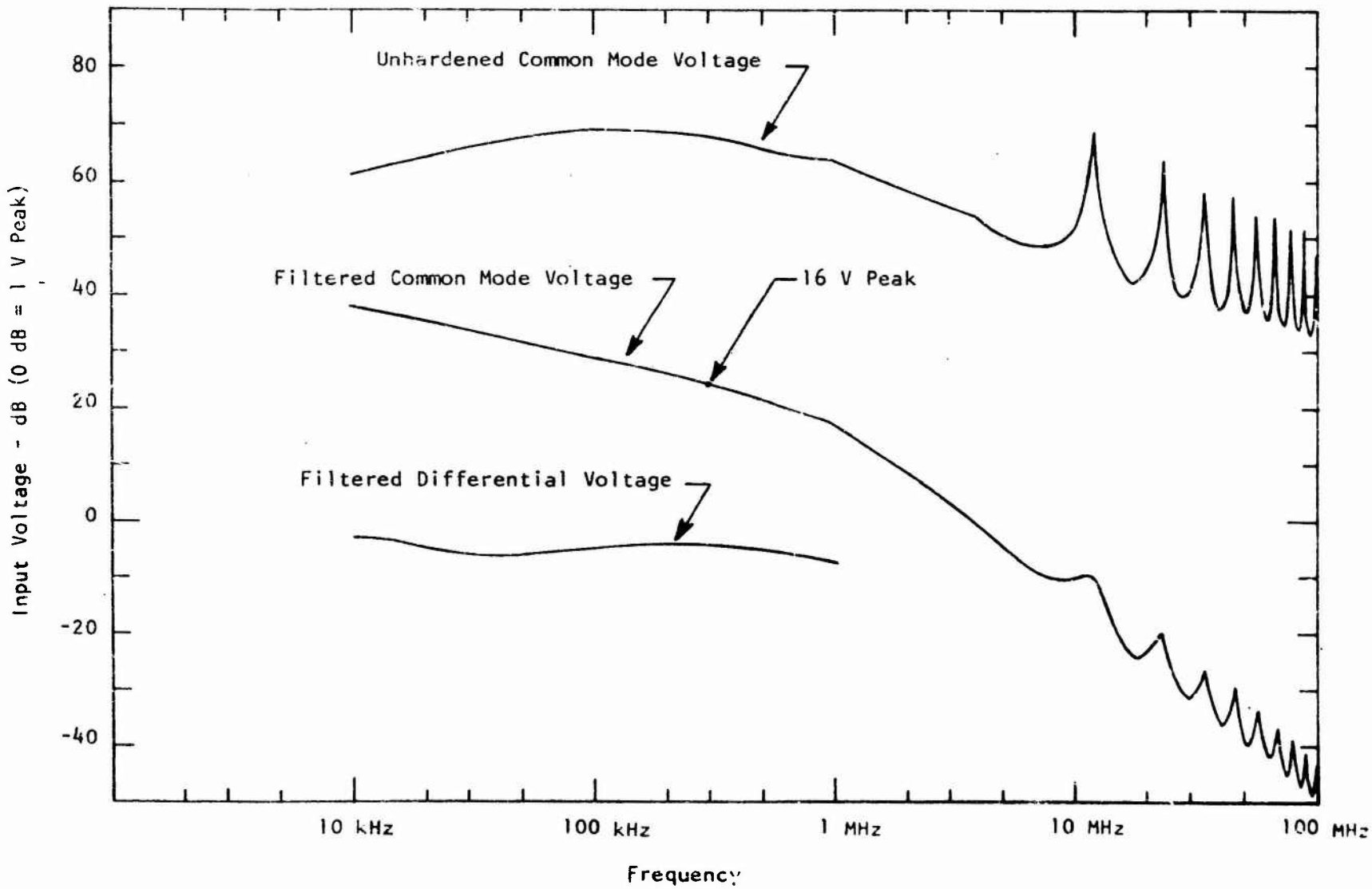


Figure 10-11. Line Receiver Input Voltage from EMP with Twisted Pair Cable

The third curve in Figure 10-10 shows the differential voltage that will occur on the twisted pair in the presence of the filtered common mode voltage. The differential voltage actually results from coupling imbalances in the twisted pair prior to filtering, but it has been assumed that these differential voltages are reduced by the filters to the same extent that the common mode voltages are reduced by the filters. This obviously assumes well-balanced and matched filters which of course is the reason for having specified one percent tolerance components in these filters. The graph shows that the differential voltages are well below the differential signal voltages and therefore will not induce erroneous data in the line receiver. These results show that the filters applied to the velocity increment signals are sufficient to completely eliminate any possibility of erroneous data when these velocity increment signal lines are contained in the 49-conductor cable.

The time discrimination hardening (see Figure 10-6) is somewhat superfluous in this case but it represents a small modification to the circuitry which provides some extra assurance. It will be seen that in the case of the twisted pair in a cable by itself, this becomes an important factor.

Figure 10-11 shows the results of the analysis of a cable which consists entirely of a single velocity increment twisted pair data line. In this case, the unhardened voltage on the input of the line receiver is great enough to provide some risk of damage to the line receiver. When filtering is applied, the voltage input to the line receiver is reduced to the point where damage is no longer a potential problem. The differential signal is less than one-volt peak throughout the spectrum and thus will not cause errors in the received data. The common mode voltage received with filtered inputs exceeds 24 dB or 16 volts in that portion of the EMP spectrum between 10 and 300 kHz. Thus, in this range, erroneous zero states can be induced by excessive common mode voltage and upset may occur. In this situation the hardening design recommended

does not totally eliminate the possibility of upset. It is obvious that complex and expensive filters could be applied to completely prevent upset by reducing the common mode voltage below 16 volts throughout the spectrum. The portion of the spectrum where upset could occur extends only from 10 kHz to 400 kHz.

Figure 10-9 shows that common mode voltages as high as 20 volts would be required to produce upset in cases where the differential signal voltage is between two and four volts. This is the most likely circumstance since only a combination of worst case signal drive voltages and differential interference of the correct polarity can reduce the total differential signal to as low as one volt. Therefore, in most cases it will be necessary to have common mode voltages of about 20 volts or slightly greater to induce erroneous zero states. This reduces the susceptibile portion of the spectrum to the range of 10 to 200 kHz or less. Within this portion of the spectrum, an erroneous zero state on one or both signal lines will not upset the operation of the circuitry if the signals present are 1,1. This results from the fact that the EMP waveform will produce pulses too short to pass the time discrimination test. If a 1,0 or 0,1 data set is present, only one of the two signal lines can be upset by an erroneous zero since the other is in a zero state already. This further reduces the probability of errors in the data. Finally, if errors do occur in the data, they are likely to result in very small net velocity errors. In fact, it is unlikely that more than a single 0.1 foot per second velocity error will result since the only type of error that can occur is the substitution of a 1,1 data set for a 0,1 or 1,0 velocity increment. These are generally spread far enough apart in time that only one will be in error as a result of EMP interference.

The analysis of performance using a cable containing only the twisted pair velocity increment data lines illustrates an important point in the determination of upset in a system. It is critical to realistically assess what constitutes upset in a system. In this case, it has been

assumed that it is possible for EMP to induce errors which would not exist in the absence of EMP interference. However, it is assumed that this does not constitute upset which would be cause for demanding improvements in the design, such as more complex filters. This assumption is based on the fact that the probability of the upset that may occur is very small and the nature of the upset is such that in a realistic threat environment, the errors resulting from upset would be small enough that they would not cause the system to perform outside its normal designed tolerances. In other words, a few 0.1 foot per second errors induced by EMP in normal performance of an aircraft mission will be smaller than accumulated velocity errors resulting from the 1 pulse/minute IEU error specification.

b. Simulation

Simulation of the accelerometer counter operation with and without the design changes to harden this circuit against EMP upset was accomplished using the DISIM language (Reference (3)). DISIM is a computer program designed for simulating the operation of the digital circuits. In addition, it has the capability for including FORTRAN statements which can be utilized to simulate analog operations within a digital system. A DISIM program was formulated to model the operation of the accelerometer counter circuitry. The damped sinusoid EMP interference shown in Figure 10-4 was modeled using FORTRAN statements. The results of the previously discussed TRAFFIC analysis were used to determine both differential and common mode EMP interference inputs. The line receivers in the accelerometer counter circuitry were modeled to simulate their normal behavior and their response to common mode signals.

Table 10-4 shows the test conditions and results of an analysis of the unhardened accelerometer counter circuitry. This simulation was conducted to illustrate the type of upset resulting from a 0,0 data set. During this run EMP interference was induced near the end of a time frame (between computer interrogations of the IEU) so that a reasonably large

count would be accumulated to illustrate the severity of this problem. It can be seen in Table 10-4 that the counter accumulated a count of 16 prior to the EMP interference and then complemented this count as a result of this interference. One more count occurred prior to the end of the frame. The total error in this case is -3.4 feet per second. It should be noted that all of the computer simulation runs were carried out with a very short time frame to minimize the computer time. At the maximum rate of 2.6 K pps for velocity increment data, the frame was only long enough to allow 17 counts. If the full 62.5 milloseconds had been allowed for time frames, the velocity errors resulting from this type of upset could be substantially larger than the error created in this example. The test runs following this were all conducted with the added circuitry to prevent 0,0 data sets from causing this type of upset. Several variations of the circuitry were tested with exactly the same EMP and the complement upset did not occur again.

Table 10-5 shows a summary of the results of six more DISIM runs. All of these DISIM runs were conducted with 10 kHz interference at the voltage predicted by the TRAFFIC analysis for a twisted pair cable. Analysis for the 49 conductor cable was not included because in all cases the interference voltage would be substantially lower and therefore represent a less severe case. Two situations were examined in these runs. First, the maximum allowed data rate of 2.6 K pps was simulated and second, the case where no velocity increment pulses are received were simulated. As stated previously, the hardened design is based on the assumption that the frequency of occurrence of velocity increment pulses on the average is very low. Thus the 2.6 K pps represents a worst case since the hardening design actually sacrificed the performance during the velocity increment pulses to some extent in order to improve performance in the absense of velocity increment pulses at the time of EMP interference. In addition, it should be noted that the choice of 10 kHz and the twisted pair voltage level also represent a worst case EMP interference because they provide the highest voltage and because this represents

TABLE 10-4

0,0 TYPE UPSET EXAMPLE

TWISTED PAIR CASE

- EMP Parameters

EMP peak voltage	1,250 V
EMP frequency	10 kHz
+X data	2.6 K pps
-X data	0

- Hardening — None

- Upset — Complemented 00001000 to produce 11110111

  Missed one normal count

- True accumulated velocity — 1.7
- IEU Output — -1.7

- Error — -3.4 ft/sec

TABLE 10-5

DISIM ANALYSIS, RESULTS FOR 10 kHz EMP, TWISTED PAIR CABLE CASE

EMP PEAK VOLTAGE (VOLTS)	EMP FREQUENCY kHz	+X DATA K pps	-X DATA K pps	HARDENING	TRUE ACCUMULATED VELOCITY (ft/sec)	IEU OUTPUT (ft/sec)	ERROR (ft/sec)
1250	10	2.6	0	0,0 prevention	1.7	2.1	0.4
1250	10	2.6	0	0,0 prevention input filters	1.7	1.9	0.2
1250	10	2.6	0	0,0 prevention 40 μs clock	1.7	1 8	0.1
1250	10	2.6	0	0,0 prevention 40 μs clock input filters	1.7	1.9	0.2
1250	10	0	0	0,0 prevention	0.0	-0.6	-0.6
1250	10	0	0	0,0 prevention 40 μs clock input filters	0.0	0.0	0.0

the lowest frequency in the specification. Low frequencies are a worst case because they are most likely to create upset in spite of the filter and time discrimination hardening techniques.

The first four runs show that the input filters and the 40 microsecond clock utilized for time discrimination, both individually and in combination, result in some improvement in the total error. The improvement in this case is not dramatic, but if the assumption that the velocity increment pulses are infrequent on an average is valid, then this is not an alarming result. In the last two runs where no velocity increment pulses were present on the data line, the error reduction was quite dramatic. With no input filters or time discrimination the total error of -0.6 feet per second was induced by a single 10 kHz EMP interference burst. With the input filters and the 40 microsecond clock for time discrimination there were no errors. The magnitude of the errors at the maximum velocity increment rate and at zero velocity increment rate with the hardened circuit verifies the conclusion that although the hardening does not totally prevent errors for the twisted pair case, the total error as a result of EMP interference is small enough that it does not represent a significant contribution when compared with the error that can accumulate from the one pulse per minute error specification for the IMU.

5. REFERENCES

The following references were used in this chapter:

(1) Vincent, M. L., "Parameter for Aircraft Cables," AFWL Contract No. F29601-72-C-0028, Boeing Document No. D224-10015-1, January 1973.

(2) Hanrahan, et. al., "TRAFFIC Program Description," AFWL Contract No. F04701-69-C-0153, Boeing Document No. D2-19334-2, December 1970.

(3) Pritchard, E. K., "DISIM Extended" Naval Ordnance Lab. Document No. NOLTR-71-66, NTIS Document No. AD 730 441, July 1971.

CHAPTER 11

DAMAGE EXAMPLES

1. INTRODUCTION

This chapter presents examples of the application of damage hardening techniques to two circuits. To maximize the benefit to the reader, both a discrete circuit and an integrated circuit are discussed, and the effects of different types of EMP interface specifications (specs) are shown. The analysis is primarily empirical, with manual circuit analysis used to establish test levels and verify results. The circuits to be discussed are the accelerometer data line receiver for the Inertial Electronic Unit (IEU) as used on the B-1 and the B-52/SCRAM, and the Receiver-Transmitter Control sense amplifiers for the AN/ARC 109 UHF radio, also used on the B-1.

Each circuit has been tested to failure for the defined EMP interface specifications. Two interface specs were used, the first is the B-1 cable current specification. Both circuits are used on the B-1, so this choice is reasonable. The B-1 spec is a relatively high Q damped sinusoidal, constant current source with an amplitude of one amp at 10 kHz and 10 amps from 1 MHz to 4 MHz. The exact waveforms and the distribution of the peak current with resonant frequency are discussed in Chapter 10 (see Figure 10-4). The other interface specification is a hypothetical constant voltage source with the same waveshape and frequency distribution as the B-1 spec, and an amplitude of 100 volts at 10 kHz and 1 kV at 1 MHz. Since both of these specs are damped sinusoids, it was necessary to convert the waveform to an equivalent rectangular pulse to accommodate the available pulse generators. This conversion is given in the EMP Susceptibility Threshold Handbook or:

$$\tau = \frac{1}{5f}$$

where f is the resonant frequency, and τ is the rectangular pulse width.

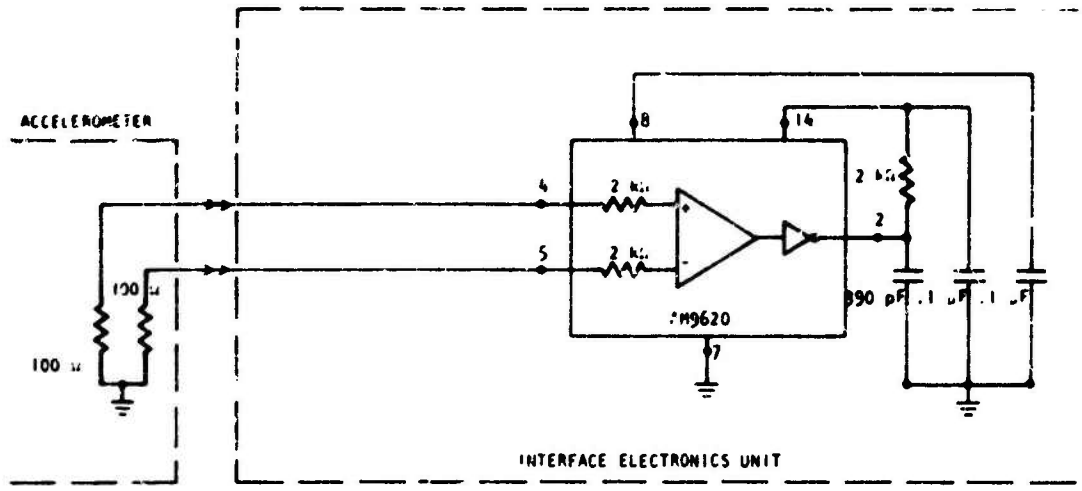
The damage mechanisms are assumed to be thermal and of the Wunsch model form. Thus, the worst case maximizes the amplitude and duration of the input pulse. The worst case test frequencies have been selected as 1 MHz and 100 kHz. The corresponding rectangular pulse durations are 200 ns and 2 μs respectively. All testing used these two pulse widths.

Both interface specifications roll off in amplitude above 4 MHz. Since the damage mechanism is assumed to be thermal, it is obvious that the higher frequencies present a lesser threat to the circuits. Thus, frequencies above 4 MHz are not considered in this chapter.

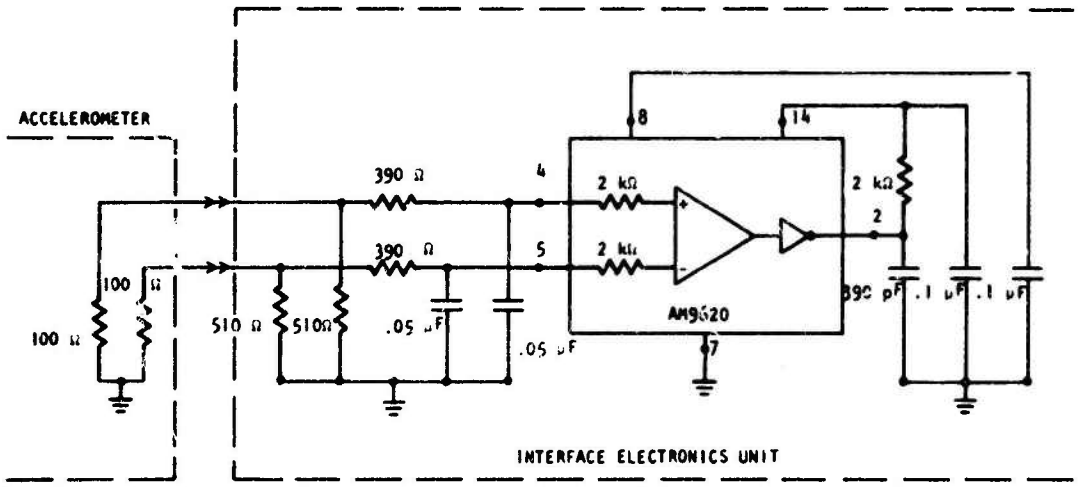
2. INERTIAL ELECTRONICS UNIT

The accelerometer input to the IEU is discussed in detail in the upset hardening example of Chapter 10. A few significant points are repeated here. The interface schematic is shown in Figure 11-1a. The IEU line receiver is a differential amplifier which receives pulses from the accelerometer at a maximum bit rate of 2.6 K pps, with a pulse duration of 100 μs to 200 μs. The pulses are transmitted in signal mode from a 100 ohm source, with nominal logic states of 0 V and 3.7 V. The maximum differential input threshold to assure a desired state is 0.5 volts. The line receiver itself is an American Microcircuits AM 9620 Dual Differential Line Receiver. The input impedance is at least 2 kΩ. Failure is defined as having occurred when the IC fails to switch with the rated differential input.

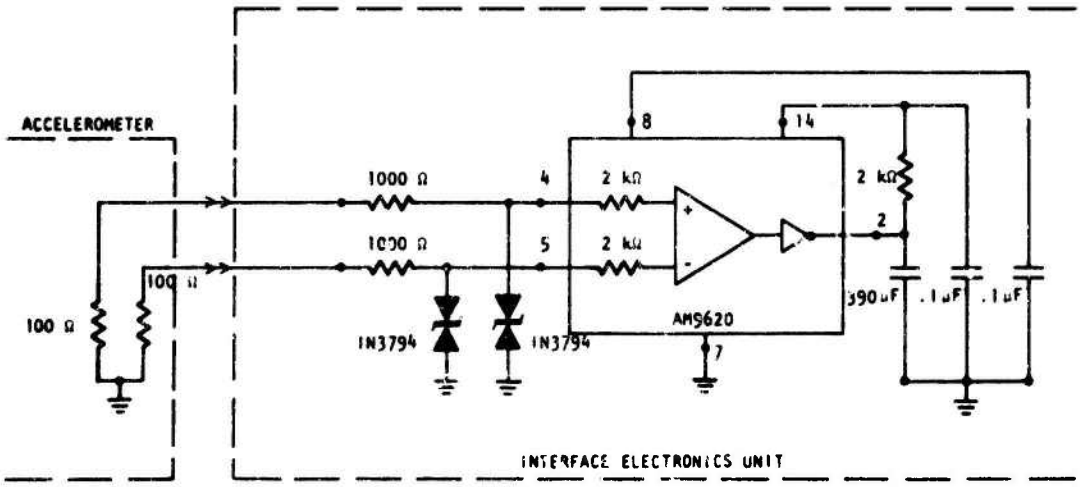
The first hardening example will use the B-1 cable current spec. The hardening technique is the RC filter discussed in Chapter 10. This filter was developed for upset protection, but it will also provide damage hardening. Figure 11-1b shows the RC filter installed at the IEU interface.



11-1 (a) unhardened Circuit



11-1 (b) RC Filter Hardening



11-1 (c) Zener Hardening

Figure 11-1. IEU Hardening Schematics

The line receiver was pulsed to failure at 200 ns and 2 μs. Both positive and negative pulses were injected at the interface between the signal input (pins 4 and 5) and ground (pin 7). Then the filter was installed and the test was repeated. The test results are shown in Figure 11-2. The data plotted are actually the maximum no fail point tested. The differences between positive and negative polarity were not significant. Figure 11-2 also shows the calculated interface signals at the IEU input for the B-1 cable current spec, with and without the RC filter installed. The current generator is assumed to be connected in series between the source end resistors in the accelerometer and ground, and the cable is assumed to be electrically short. It is seen that without the filter, the spec signal exceeds the threshold and damage will occur. With the filter installed, the threshold exceeds the spec signal by almost 20 dB for all frequencies.

The second damage example uses an EMP interface spec consisting of a constant voltage source in series with the source end resistor in the accelerometer and ground. The hardening technique uses a discrete resistor and Zener diodes to limit current to the circuit as shown in Figure 11-1c. The 1 kΩ resistor is chosen to limit current without interferring with normal circuit operation. The Zener voltage, 16 volts, is compatible with the rated maximum common mode voltage rating of the IC. The calculated IEU interface signals and the measured damage thresholds are presented in Figure 11-3. Again, the differences between positive and negative polarity were not significant.

The circuit is seen to be vulnerable to the spec signal in the unhardened case while it has a 6 dB safety margin in the hardened case. The failure in the hardened case occurred when the resistor (1/4 watt carbon) arced. A greater safety margin could undoubtedly be achieved by selecting a more suitable resistor.

3. AN/ARC-109 RADIO

The AN/ARC-109 is a UHF radio. It consists of two boxes, a receiver-transmitter, and a controller. The controller provides remote frequency

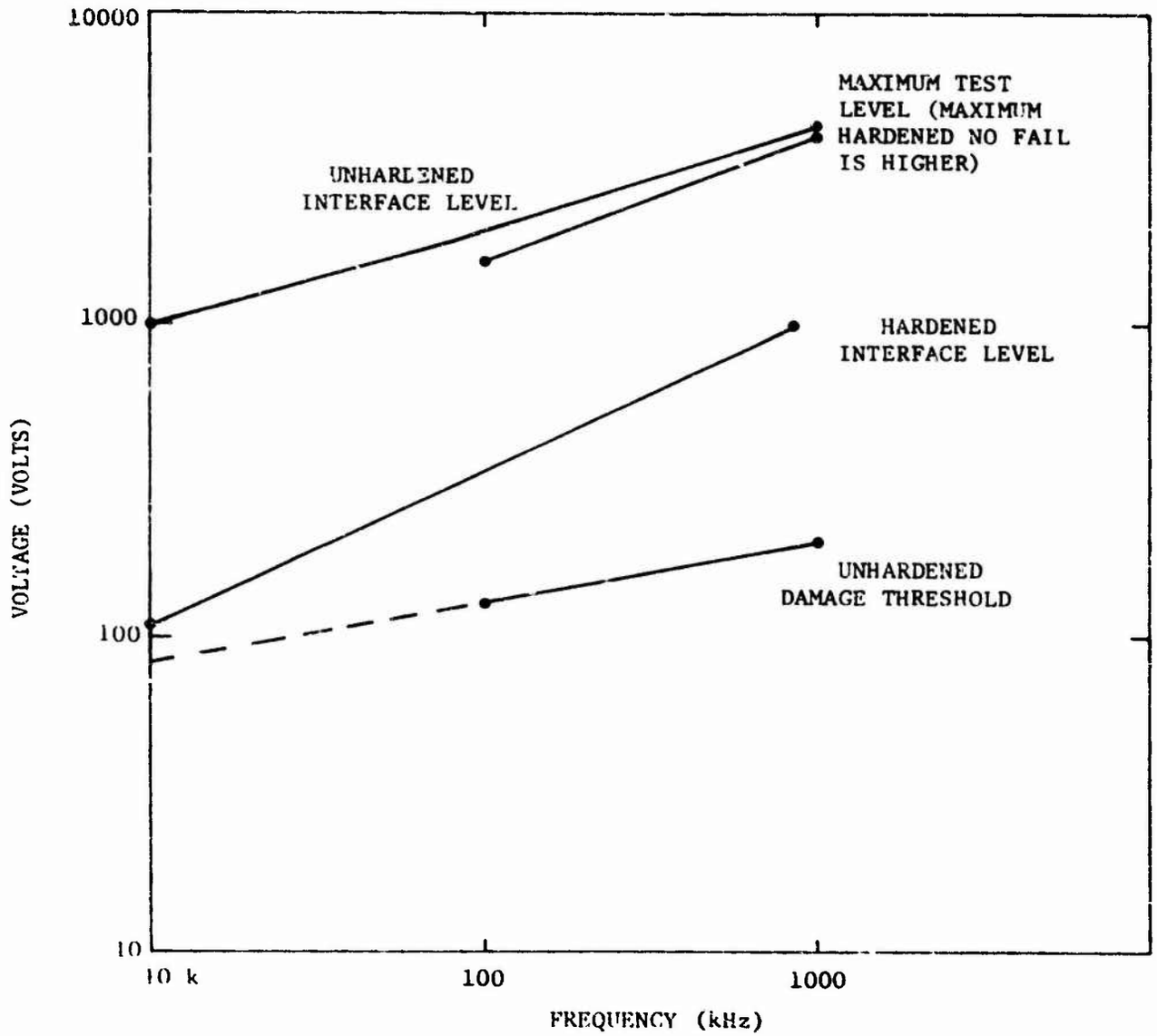


Figure 11-2. RC Hardening Test Results

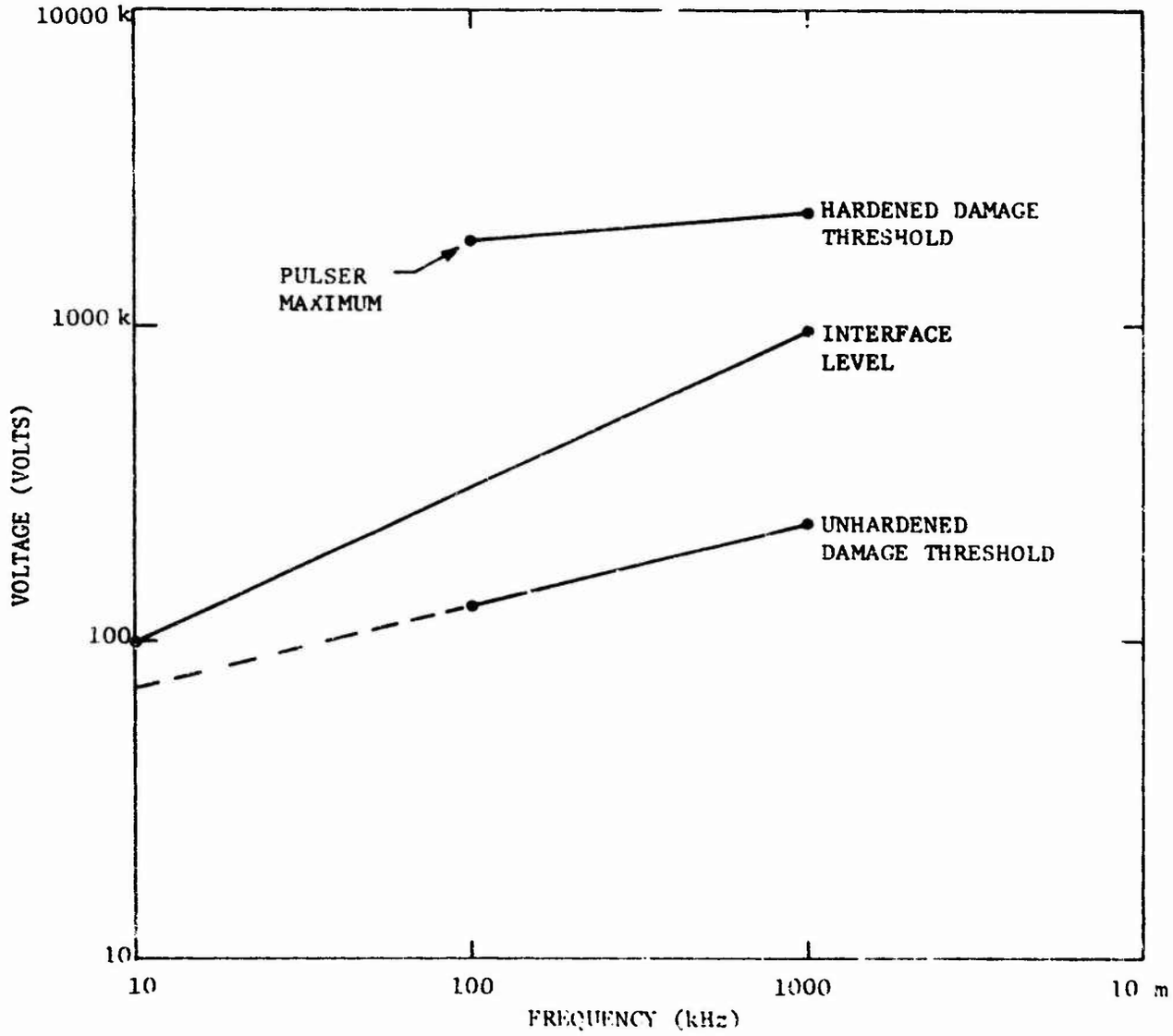
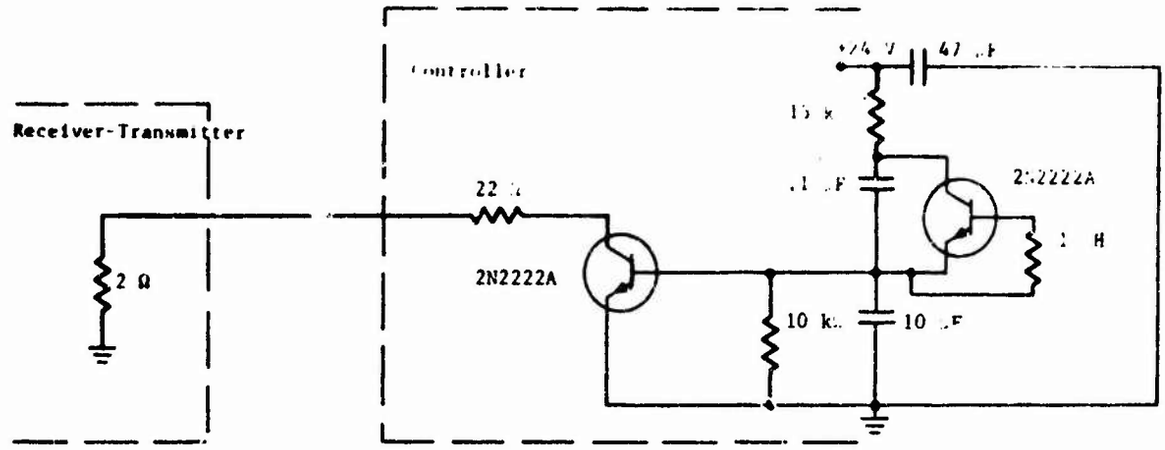


Figure 11-3. Zener Hardening Test Results

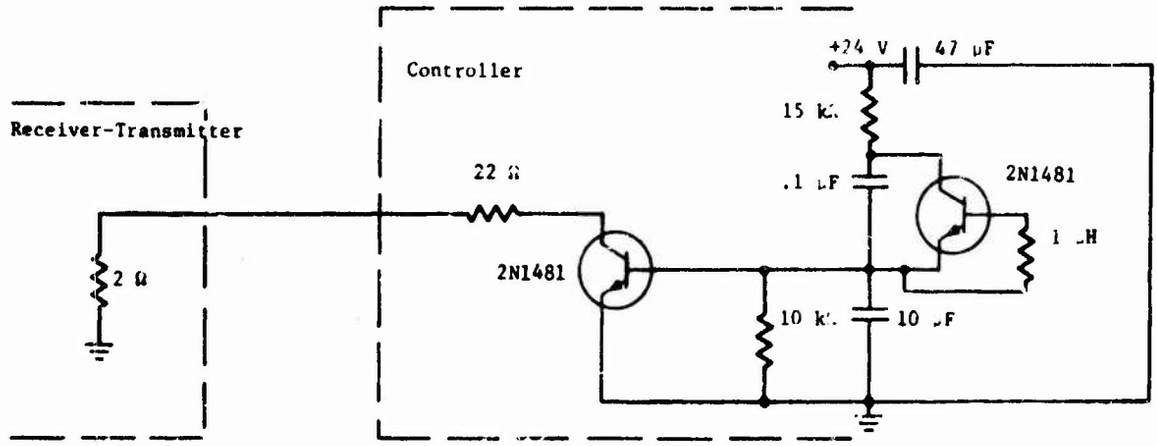
selection commands to the receiver-transmitter in binary coded decimal (BCD) format. The circuit selected for this example is the controller sense amplifier. The sense amplifier (one for each of 14 bits) transfers data from the memory core in the controller to the BCD comparator in the receiver-transmitter. The input to the sense amplifier from the core is a 5 kHz, 1.5 volt pulse. The output is a high or low switch for a 32 Vdc reference from the comparator. The sense amplifier interface schematic is shown in Figure 11-4a. Failure is defined as having occurred when the sense amplifier output does not switch from 0 V to 17.8 V, for the specified input pulse.

The sense amplifier was analyzed to determine its damage threshold. These results are used to guide and verify the test results. The failure threshold is seen to be critically dependent on the characteristics of the 2N2222A transistors. Their rated collector-base reverse breakdown is given in the Susceptibility Threshold Handbook as 75 V. However, tests showed that for currents over 100 ma the junction goes into second breakdown with a voltage of about 30 V. The Handbook gives a damage constant of 0.1 for the emitter-base junction. Applying this constant to the collector-base for a 2 μs pulse yields about 80 V (2.3 amps), for the circuit damage threshold to positive pulses. This should be quite conservative, since the collector-base junction is generally harder than the emitter-base junction. The negative damage threshold depends on the 2N2222A bulk resistance. Assuming a bulk resistance of 1 ohm, the circuit input damage threshold is 184 volts (8 amps). This threshold should also be conservative.

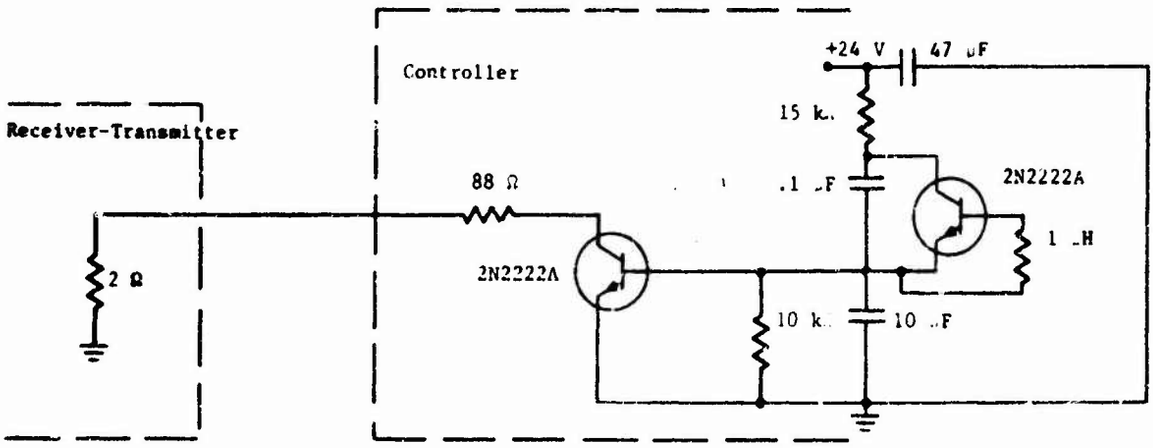
The first hardening example involves simply substituting a harder transistor for the 2N2222A. The 2N1481 was selected since it has similar switching characteristics and a listed damage constant of 2.2. The circuit configuration is shown in Figure 11-4b. A static check of the collector-base reverse breakdown voltage showed similar second breakdown characteristics to the 2N2222A. Thus, an improvement of about 26 dB is expected in



11-4 (a). Unhardened Circuit



11-4 (b). Substitution Hardening



11-4 (c). Resistive Limiting

Figure 11-4. Sense Amplifier Hardening Schematic

circuit damage threshold to positive pulses. An improvement of about 13 dB is expected in the negative threshold (again assuming 1 ohm for bulk resistance) since the threshold varies with the square of the current for a forward biased junction.

Both the hardened and the unhardened circuits were pulse tested to failure at the interface. The maximum no-fail voltage results are presented in Figure 11-5 which also shows the calculated interface voltage level for the B-1 bulk current spec. The constant current source is assumed to be between the source end resistor in the receiver-transmitter and ground. No schematic was available on the comparator. An equivalent load impedance of 2 ohms is postulated for these examples. Note that the interface voltage level frequency distribution is distorted by the nonlinear termination presented by the transistor. The asymptotic value is determined by the measured reverse breakdown voltage. Both the interface specification voltage and the threshold voltage are dependent on signal polarity. Since the specification is a damped sinusoid having both polarities, curves are required for each polarity. The dashed lines represent extrapolation outside the range of the test equipment.

The experimental results are seen to be in general agreement with the analysis presented above for the unhardened circuit. However, the failure threshold follows a linear frequency relationship rather than the $f^{1/2}$ suggested in the Susceptibility Threshold Handbook. The reason for this is not apparent; however, the same slope will be used to extrapolate other results outside the test range. Note that the hardened circuit could only be failed with the positive polarity 100 kHz (2 μs) pulse. In this case, the hardness improvement is about 14 dB which is somewhat less than predicted. The exact improvement in the other cases cannot be determined. However, it is clear that the circuit has been hardened.

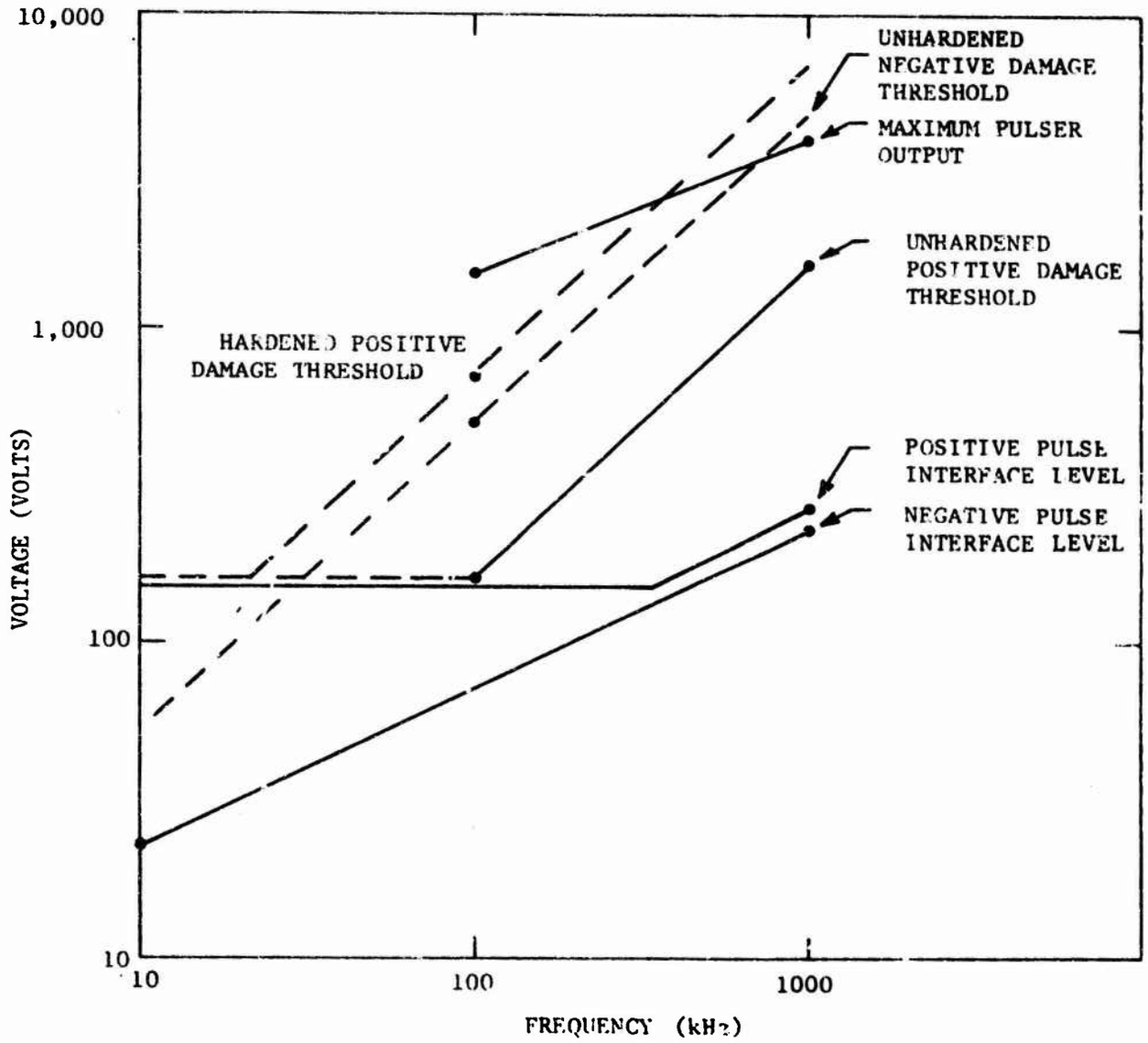


Figure 11-5. Transistor Substitution Test Results

The second hardening example uses the constant voltage source interface specification. The hardening technique involves increasing the size of the 22 ohm collector resistor to limit the current. Normally the maximum value of resistance consistent with the comparator load requirement would be chosen. In this case, it is assumed that a value of 88 ohms can be used, since the information required for the analysis is not available. This should increase the circuit damage threshold by 12 dB for both positive and negative polarities.

The hardened and unhardened circuits were pulse tested to failure and the test results are shown in Figure 11-6. The calculated interface voltage level is also shown. The thresholds shown are for maximum no-fail voltage. A number of sample circuits were tested at each pulse width and polarity. It was found that unless care was exercised in resistor installation, voltages in excess of 2 kV could cause arcing across the resistor and resulting failure of the transistor. In most cases, however, the resistors withstood the maximum pulser voltage of up to 4 kV. In these cases the only circuit failure occurred with the positive polarity 100 kHz (2 μs) pulse. The measured hardening improvement of 11 dB for this case agrees well with the predicted improvement. The exact hardening provided for the negative polarity cannot be determined but obviously the threshold was increased. Note that the extrapolated damage threshold for the positive polarity cannot drop below the measured breakdown voltage of about 150 V.

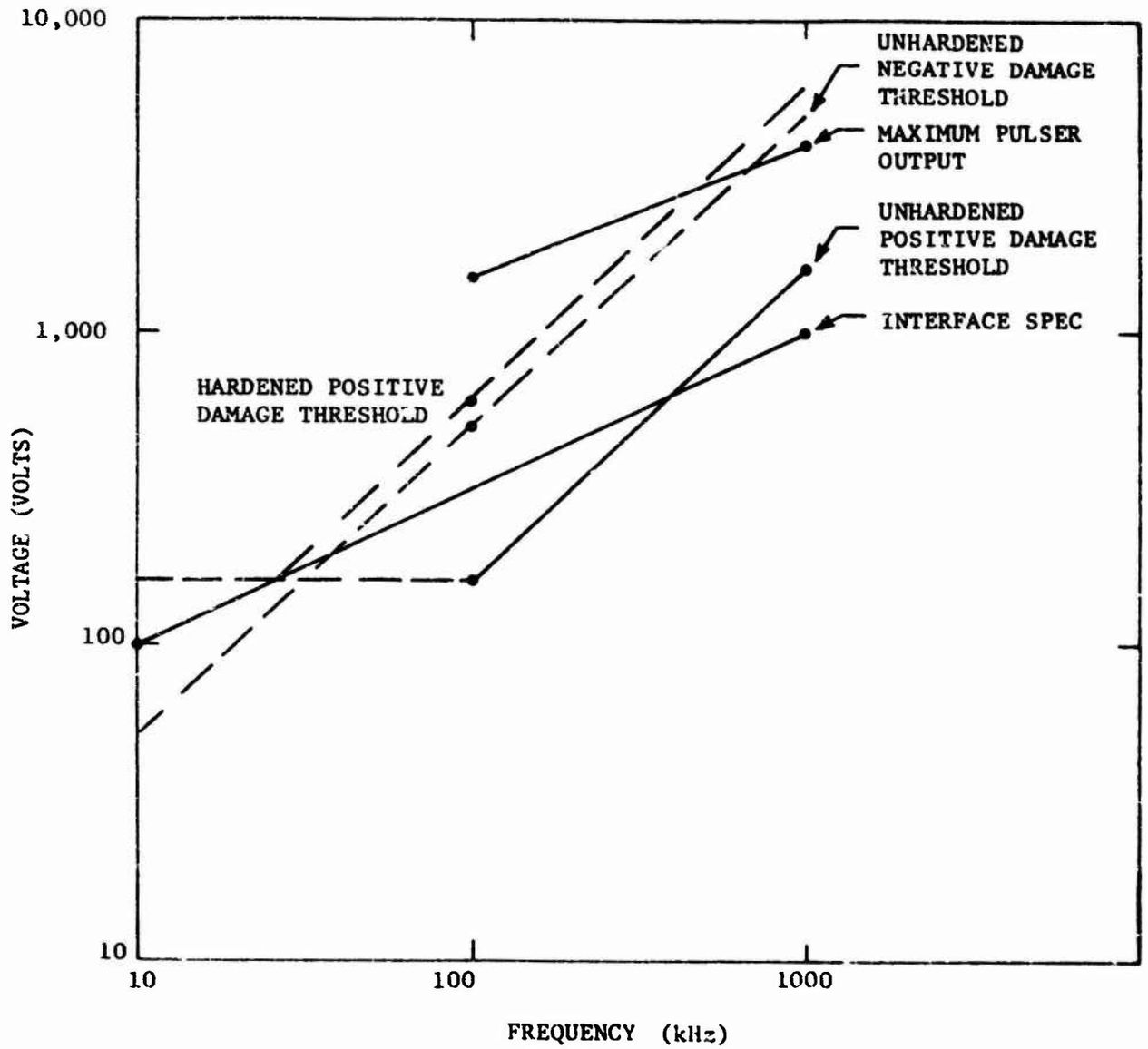


Figure 11-6. Current imiting Test Results

APPENDIX A

HARDENING GUIDELINES
EXPERIMENTAL SUPPORT PROGRAM

1. SCOPE

The formulation of subsystem hardening guidelines presented in this report required a parallel experimental program designed to investigate or verify the unique response of electronic components and circuits to simulated EMP transients. Testing was necessary to supplement available data in the following two general areas:

- Static and dynamic characteristics of candidate protective devices and networks
- Assessment of component and circuit damage thresholds in various hardened and unhardened configurations

Since potential transient suppression devices such as spark gaps, diodes, varistors and neon lamps are not normally subjected to pulse tests representative of an EMP environment, extensive testing of these devices was necessary. Static and dynamic parameters germane to the selection of a suppression device for a given circuit hardening application were evaluated and presented in matrix form in Chapter 6.

The large signal response of filter pin connectors and photon couplers was measured on an exploratory basis to determine degradation and failure tendencies of these devices.

The common mode rejection of a sample twisted pair cable was measured to obtain a typical frequency distribution for this parameter.

The damage thresholds of a few digital integrated circuits was experimentally determined to verify similar work done using different transient characteristics.

Finally, circuit injection tests were performed to demonstrate the damage hardening achieved by the various protection methods described in these hardening guidelines.

While the results of the above tests are integrated into the appropriate sections of the text, a description of the test facility and methodology may be valuable to the reader and is thereby presented in the following paragraphs.

2. FACILITY

All testing was performed at the BDM R&D Laboratory in Albuquerque, New Mexico. In addition to conventional instrumentation required to measure key device parameters such as breakdown voltage, capacitance, or frequency response as in the case of filter pin connectors, unique EMP transient simulation equipment was required. Figure A-1 shows the three custom pulse generators used during this program.

The SN/SPG-200 pulse generator is the large console at the left of Figure A-1 and is designed to produce fast risetime, medium energy, rectangular pulses for component and circuit response testings. This pulser delivers rectangular pulses up to 10 kV with risetimes typically on the order of 1 to 2 nanoseconds and pulse widths variable from 10 to 1000 nanoseconds in 10 nanosecond increments. Its output is continuously variable from 5 volts to 10 kV. The pulser has an output impedance of 50 ohms, and current and voltage probes are built into the pulser. Special circuitry has been added to suppress the late-time

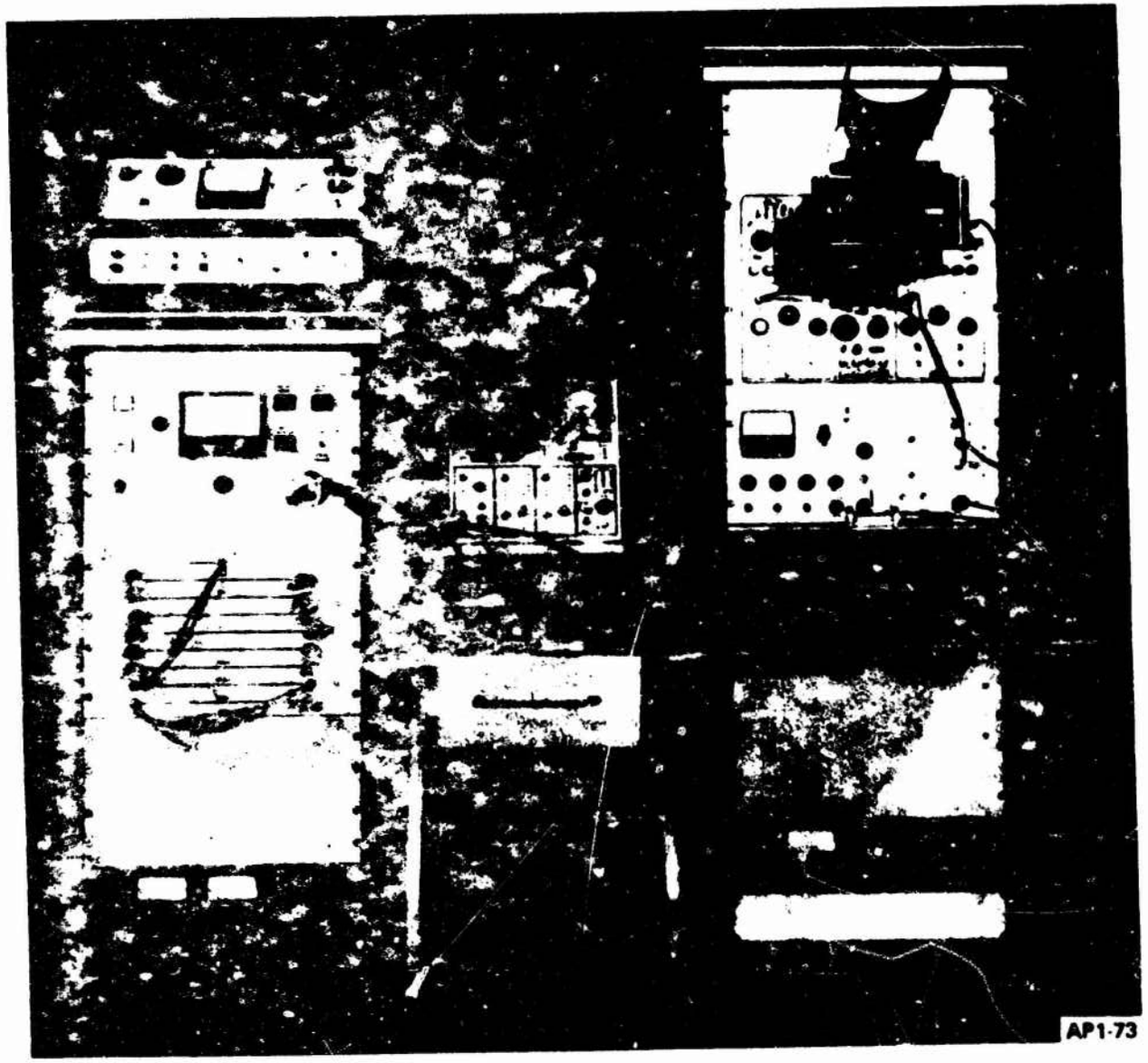


Figure A-1. Pulse Generators

reflections often associated with transmission line pulsers. This is particularly important when testing sensitive, polarized components (such as diodes) whose failure threshold in one direction differs from their failure threshold in the other direction. The SN/SPG-200 can deliver a maximum of about 2 megawatts to a matched load, and has a total energy storage of 2 joules. Particular attention was also given in the design of this pulser to optimize its operational characteristics. Thus, it presents excellent repeatability at any given pulse width, or amplitude, and changes in pulse width or amplitude can be made on the front panel in a matter of a few minutes. For the TPD actuation voltage tests a delay line was added to the SN/SPG-200 to provide available risetime.

The HEP-100 pulse generator is the large console at the right of Figure A-1. It is designed to deliver high energy double exponential pulses for the failure testing of components with damage thresholds beyond the capability of the SN/SPG-200 pulser. The HEP-100 pulse generator can deliver up to 1000 amperes at 10 kV. Nominal risetime is 20 nanoseconds and the decay time is determined by the load impedance. For a 50 ohm load, the decay time to the 1/e value is about 200 microseconds. The HEP-100 pulser has a maximum power output of 5 megawatts to a matched load. Its total energy storage is 162 joules. Attention has been given to optimization of the operational features of this pulser, including very good repeatability and readily changeable pulse amplitudes. Current and voltage probes are included in the pulser design, and a Tektronix Type 556 oscilloscope is built into the pulser chassis. Thus, for many tests, no external instrumentation is required.

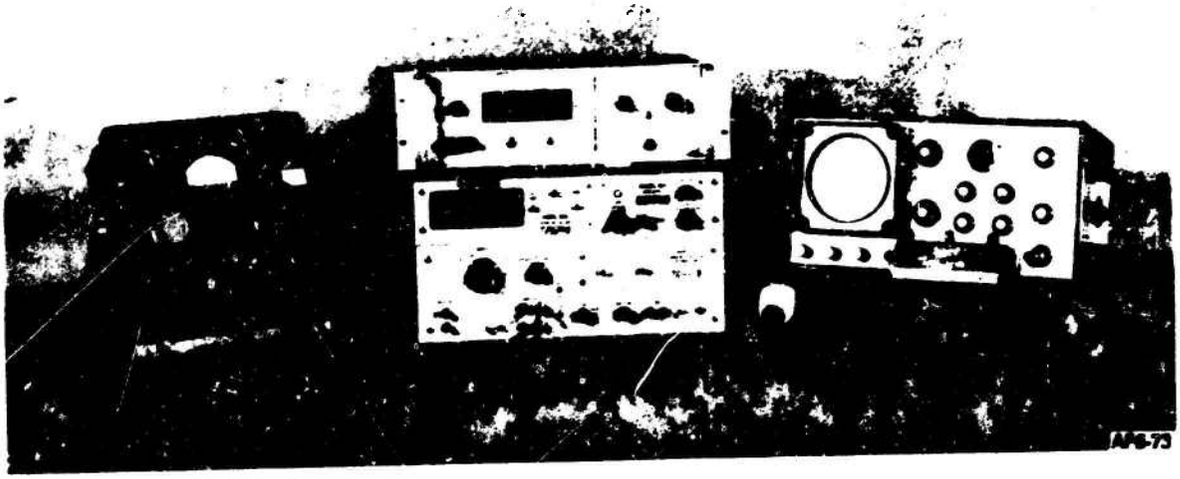
The PEG-101 pulse generator is the small unit on top of the SN/SPG-200 and is designed to produce rectangular pulses with a 20 nanosecond risetime variable duration (100 nsec to 20 μsec) and variable amplitude (25 to 2500 volts). It has a minimum output impedance of 25 ohms and a maximum current of 100 amps. For the TPD actuation voltage tests an RC network was added to the output of the PEG-101 to provide variable risetimes.

Data recording was accomplished through the use of oscilloscopes, and their associated cameras, combined with voltage and current probes. In addition to the HEP-100's Tektronix 556 scope, the Tektronix 454A and 7904 oscilloscopes, (shown in Figure A-1) with 2.3 nanosecond and 0.8 nanosecond risetimes, respectively, were used for transient measurements thoughout the test program. Oscillographic data was reduced either manually or using a Hewlett-Packard 9100 calculator and digitizing system such as shown in Figure A-2. Figure A-2 also shows the equipment used to measure static parameters. This includes a Fairchild curve tracer, and Boonton and General Radio reactance bridges.

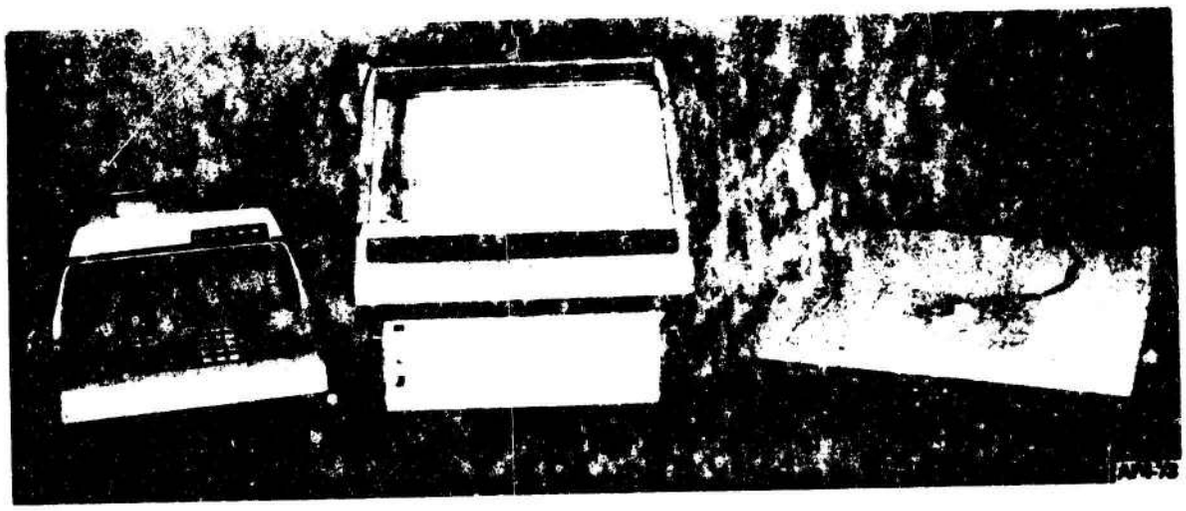
3. METHODOLOGY

The component and circuit testing performed during this program can be summarized under two major categories: response testing and failure testing. Response testing consists of several non-destructive measurements that define the device or network response to the frequencies and waveforms typical of an EMP Environment. Response tests include such specific measurements as:

- Actuation Voltage (V_A)
- Protective Efficiency (α)
- Insertion Loss (C_T or $_{3db}$)
- V-I Characteristics
- Frequency Response (FR)
- Static Tests (V_{BD})



(a) Static Instrumentation



(b) Data Reduction Equipment

Figure A-2. Test Support Equipment

Some of the above tests were performed in conjunction with the step-stress failure testing to determine the functional condition of the unit under test, i.e., as a means of observing parameter degradation.

Failure testing consisted of step stress pulse testing of candidate devices or networks and intermediate "state of health" static tests to determine at which pulse level failure occurred. All components and circuits were tested to either failure or to the maximum pulse level obtainable from the equipment described previously.

Table A-1 summarizes the test program related to the formulation of subsystem EMP hardening guidelines. A detailed description of test configurations and procedures is beyond the scope of this report.

UNCLASSIFIED

Security Classification

DOCUMENT CONTROL DATA - R & D

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1. ORIGINATING ACTIVITY (Corporate author) The Boeing Company Seattle, Washington	2a. REPORT SECURITY CLASSIFICATION UNCLASSIFIED 2b. GROUP N/A

3. REPORT TITLE

EMP ELECTRONIC DESIGN HANDBOOK

4. DESCRIPTIVE NOTES (Type of report and inclusive dates)

Final

5. AUTHOR(S) (First name, middle initial, last name)

Byron P. Gage

6. REPORT DATE April 1973	7a. TOTAL NO. OF PAGES 212	7b. NO. OF REFS 30
8a. CONTRACT OR GRANT NO. F29601-72-C-0028 b. PROJECT NO. c. Work Order 2-9 d.	9a. ORIGINATOR'S REPORT NUMBER(S) D224-10019-1 9b. OTHER REPORT NO(S) (Any other numbers that may be assigned this report) N/A	

10. DISTRIBUTION STATEMENT

Statement [redacted]. [redacted] B
Controlling DoD Office - U. S. Air Force Weapons Laboratory (ELA)

11. SUPPLEMENTARY NOTES	12. SPONSORING MILITARY ACTIVITY U. S. Air Force Weapons Laboratory Kirtland Air Force Base Albuquerque, New Mexico 87117

13. ABSTRACT

This handbook provides a state-of-the-art compilation of EMP hardening design information in a format of immediate use to electronic designers. Candidate hardening techniques are identified and their implementation is discussed. Pertinent design data are presented and detailed hardening examples are provided. In many cases the required design data were generated directly for this handbook. The appendix provides a general description of the test program.

The handbook is organized in four main sections and 11 chapters. Section I provides a general introduction and overview for EMP hardened design. Section II treats good design practices for all phases of subsystem design. Section III treats specific hardening techniques for subsystems or circuits known to require EMP hardening. Section IV presents examples of the design of specific hardened circuits.

DD FORM 1 NOV 65 1473

Security Classification

14 KEY WORDS	LINK A ROLE	LINK A WT	LINK B ROLE	LINK B WT	LINK C ROLE	LINK C WT
EMP						
EMP Hardening Design Information						
EMP Hardening Techniques						

TABLE A-1 TEST SUMMARY MATRIX

TEST SUBJECT	TEST							
	V_{BD}	C_T	α	V_A	FR	VI	Other * Operational	Failure
Spark Gaps	X	X	X	X		X		X
Neon Lamps	X	X	X	X		X		X
Transzorbs	X	X	X		X	X		X
Zener Diodes	X	X	X		X	X		X
Surge Arrestors	X	X	X	X		X		X
Rectifier Diode	X	X	X			X		X
Varistors	X	X	X		X	X		X
Filter Pin Connectors	X				X			X
Photon Couplers	X						X	X
Integrated Circuits							X	X
Twisted Pair					X		X	
Demonstration Circuits							X	X

* Refers to special functional tests such as I.C. or circuit check out.