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VOLUME I

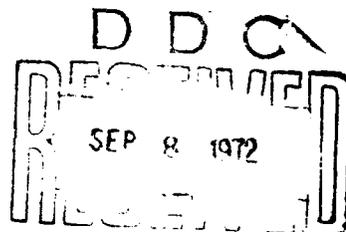
PRODUCTION ENGINEERING MEASURE
SOLID ENCAPSULATED SEMICONDUCTOR DEVICES

Contract DAAB05-70-C-3109

FINAL REPORT
JUNE 1972

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225 South 18th Street, Phila., Pa. 19103.

Prepared for
Department of the Army
United States Army Electronics Command
225 South 18th Street
Philadelphia, Pennsylvania 19103

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PURPOSE

This is the final technical report on the United States Army Electronics Command Contract DAAB05-70-C-3109 from 23 March, 1970 to 23 March, 1972. This contract with the General Electric Company, Semiconductor Products Department, Electronics Park, Syracuse, New York was initiated by the Electronics Command as a Production Engineering Measure for achieving reliable Solid Encapsulated Semiconductor Devices.

The purpose of this program was to develop and optimize production capability for the manufacture of small signal solid encapsulated transistors capable of performing to military specifications. An NPN (GE type 32DXR5318) and a PNP (GE type 34EXR1853) small signal transistor in a TO-18 lead configuration, currently in high volume production, were used as vehicles for this program.

Specifically this program has had the following objectives:

- Improve the capability of solid encapsulated transistors to meet the performance requirements of military application environments,
- Assess the capability of the devices to meet the requirements of MIL-S-19500 and additional Group B tests which include:

Moisture Resistance with Bias Test,
High Temperature Reverse Bias Life (non-operating),
Steady State Operating Life for 1,000 hours.

- Perform a sound statistical and engineering test program design to assess and demonstrate, with confidence, the desired reliability levels of solid encapsulated transistors under accelerated stress conditions.

- Assure that the quality and reliability of the product meet the requirements of applicable military specifications,
- Establish production planning to meet the estimated military needs for a period of two years after the completion of the solid encapsulated semiconductors (100,000 units per month operating one 8-hour shift, five days a week).

The work performed on this contract was under the direction of Mr. David Biser of the United States Army Electronics Command, 225 South 18th Street, Philadelphia, Pennsylvania. The report was submitted 6 June, 1972.

Mr. David K. Hartman was the program manager for this contract and the technical project manager was Erwin A. Herr. The contributions to this effort, and to the preparation of this report, were B. L. Bair, R. L. Clark, S. F. Daniluk, A. Fox, A. D. Hammon, C. O. Hull, A. Poe, J. H. Racette, R. E. Smith, and J. F. Wholey. In addition to the above key contributors, there were many people over the course of the two years both from the engineering and manufacturing function that became involved in the program. The contributions of the following from engineering should be acknowledged: J. H. Affleck, H. Brandhorst, J. R. Canon, E. G. Carson, S. I. Gabrail, R. V. Hillery, H. H. Hosack, R. E. Hysell, E. H. Lederer, L. F. Leinweber, C. E. Logan, A. M. Intrator, H. Johnston, L. A. Rivera, R. J. Shanahan, P. N. Sherman, T. Shepelavy, L. C. Smith, J. W. Sprague, and H. W. Wawrousek. The following manufacturing people who made contributions to the program include A. Blank, R. M. Hughes, D. H. Lapray, R. B. Moses, G. J. Nicholas and D. E. Shaughnessy. Further acknowledgments are to be made to B. Corrie of IC², Dr. J. F. Schenck of the Electronics Laboratory and to the Corporate Research and Development Center in Schenectady for analytical work.

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ABSTRACT

This is the final documentary report of the Production Engineering Measure (PEM) program for improving the reliability and performance of solid encapsulated semiconductor devices to meet the rigorous requirements of military application environments. A small signal NPN transistor (GE type D32D) and a small signal PNP transistor (GE type D34E) were the vehicles used. Basic changes in the semiconductor structure were made on these devices to enhance the performance of the products and to improve the capability of solid encapsulated transistors. The semiconductor topological structure was based on the application of a clean thermal oxide, a pyrolytic silicon nitride barrier over the oxide, refractory metalization and a glass coating over the entire structure except at contact windows for the emitter and base regions. The refractory metalization system was a platinum silicide/molybdenum/gold laminar structure that was capable of withstanding the high temperatures associated with the glassivation process. This system, through proper processing, provided good ohmic contacts to both the N and P regions of the transistors. As result of these features, device stability was enhanced by preventing the migration of contaminating ions, such as sodium, to the silicon surface. The glassivation prevented metalization corrosion and in addition provided complete chip passivation. As a result, a chip is now available that is compatible with hermetic, plastic and hybrid packaging.

During the course of this program, over 10,000 transistors were fabricated for evaluation and test purposes to assess product performance. The contract units in every case were compared to control structures manufactured at the same time and in the same system where possible. A sound statistical and engineering test program was designed and implemented based on step-stress, bias moisture resistance, high temperature reverse bias life, and steady state operating life tests. As a result of the extensive test program, it was conclusively proved that a superior product has been achieved that was capable of meeting the severe military requirements. As an additional benefit, a transistor evolved that was capable of handling significantly more power.

SECTION I

INTRODUCTION

1. POTENTIAL PROBLEMS IN PLASTIC ENCAPSULATED SEMICONDUCTORS

The area that has been of the greatest concern for plastic encapsulated devices has been the potential degradation of the device when it is subjected to humidity. The mechanisms that could result involve the transmission of water vapor through the plastic or along the device leads. If this occurs in the presence of contaminants, it is possible that ionic conduction could occur external to the pellet surface or on the pellet surface. The presence of contaminants could also result in silicon surface inversion or channeling. The electrical indicators of this type of change include increases in the collector to base leakage current, shifts in the small signal current gain and shifts in the collector to base breakdown voltage. The presence of humidity could result in corrosion of the pellet metalization, internal leads, the internal bonds (intermetallics) and the external leads.

Additional problem areas could include the mismatch of the thermal coefficient of expansion of the several materials, changes in the mechanical strength and the flammability resistance of the encapsulating material. Some of the plastics which have been suggested for encapsulants have been limited to operation or storage at temperatures below 150°C. This is a limitation for the usual military specification, but several epoxies and silicones have been tested and are presently being evaluated at temperatures in excess of 150°C.

2. ADVANTAGES OF PLASTIC ENCAPSULATION

The solid encapsulated device has a high capability to withstand mechanical stress. In addition, high volume assembly methods based on solid encapsulation technology allow automated production techniques which greatly minimize human variability factors. These concepts are being used for manufacturing commercial transistors and have resulted in a significant reduction

of manufacturing defects. The solid encapsulant also provides good thermal transfer, since there is contact to the entire surface of the pellet and the internal leads. Such complete contact increases the current handling capability of the device because of the improved thermal conductivity of the solid encapsulant over the internal gas environment which is standard in metal enclosed transistors. The solid encapsulation also provides complete mechanical support of the internal components and eliminates possible problems with loose particles.

3. TECHNIQUES FOR OVERCOMING LIMITATIONS AND ENHANCING ADVANTAGES OF PLASTIC ENCAPSULATION

An existing, high volume production facility with automated processes has been used to accomplish the objectives of this program. This approach provided volume and cost advantages and used processes with well developed levels of control.

Existing chip designs were modified in order to manufacture a sealed junction device with a protective silicon nitride layer, a high temperature refractory contact system and glassivation. Thus, a major part of the work effort of this program was devoted to forming and optimizing the required device structure.

The silicon nitride layer was used to reduce or eliminate surface inversion due to the migration of contaminants through the silicon dioxide passivation layer. The high temperature refractory metalization system, based on platinum silicide/molybdenum/gold was used to minimize corrosion and to provide a stable high temperature system that was more tolerant of higher operating temperatures without affecting the device performance, such as those induced by power surges or peak operating conditions. Further the system was designed such that it was compatible with high temperature processing.

Even with the use of a silicon nitride barrier layer, it is possible to induce a surface charge that creates channels from ionic contamination accumulated

during exposure to humidity and temperature conditions. An additional barrier to this ionic or moisture penetration to the metalization and chip surface is provided by a glassivation layer overcoating the entire chip structure.

Thus the General Electric Company approach to higher reliability solid encapsulated semiconductor structures was based on the application of a clean thermal oxide, a pyrolytic silicon nitride barrier and a glass coating. The platinum silicide/molybdenum/gold metalization system was a high temperature refractory contact system compatible with the glassivation process, which also provided good ohmic contacts to both N and P regions. This system provided a chip which eliminated metal phase transformations by the use of a gold to gold contact system, and that could be used in hermetic, plastic or hybrid applications.

The test vehicles used on this program included a small signal NPN transistor and a PNP transistor with a TO-18 lead configuration. Both of these devices are standard planar epitaxial passivated structures. The fabrication process used on this new design included several additions to the standard planar passivated chip process.

A sound statistical and engineering test program design was used to evaluate and demonstrate, with confidence, the desired reliability levels of solid encapsulated transistors under accelerated stress conditions. These devices were evaluated using temperature and power step-stress, combination and sequential stressing such as thermal shock and humidity cycling tests. Steam pressure, boiling water and extended temperature-humidity life tests were also performed. Both the new structures and proper control devices, derived from the same replicated production lots, were subjected to the different stress cells in a random and balanced manner to assure statistically valid and reproducible results.

A family of small signal solid encapsulated transistors was designed and fabricated and tests have shown that they are able to perform to military specifications. The following significant results have been obtained on the program:

- Demonstration of a superior chip passivation seal,
- Extension of the operating temperature range to 175°C,
- Extension of the power dissipation range from 360 mW to 600 mW ratings,
- Demonstration of resistance to water vapor and temperature,
- Demonstration of parameter stability after accelerated testing,
- Demonstration that both NPN and PNP type transistors with the new passivation seal met the requirements of MIL-S-19500E, with Amendment 1 and Special Notes 21, 22 and 23 of the contract. These special notes required additional 1000 hour tests including:
 - Moisture Resistance with Bias,
 - High Temperature Reverse Bias Life (non-operating),
 - Steady State Operating Life.

SECTION II

WAFER AND CHIP PROCESSING

1. CHIP DESIGN

In order to concentrate the contract effort on consolidating and optimizing the metalization and passivation technology, it was decided to start with two existing General Electric transistor designs used to produce a complementary chip pair. The existing design, with silicon dioxide passivation and aluminum metalization is referred to as the control device or structure. The devices with silicon dioxide, silicon nitride, refractory metalization and glassivation are referred to as the contract structures.

The surface geometry for the contract structures is shown in Figures 1 and 2 and the diffused cross sections for the control NPN and contract structures are shown schematically in Figure 3. The principal device dimensions are indicated in Table I. The final surface configuration of the NPN and PNP chips differ only in the field relief electrode just outside the collector base junction of the PNP structure. This is a standard industry precaution against surface inversion of the P-type collector.

Assembled plastic encapsulated devices made from the above chips are used as general purpose, medium current amplifiers and switches up to collector currents of about 500 milliamperes.

2. MATERIAL

Specifications for the epitaxial wafers used in the contract study are given in Table II. At the start of the program a sufficient quantity of NN^+ and PP^+ wafers were procured and measured to serve as a uniform bank for future experimental and pilot line inputs. One and one-half inch diameter wafers were used for the bank because of the greater confidence at that time (early 1970)

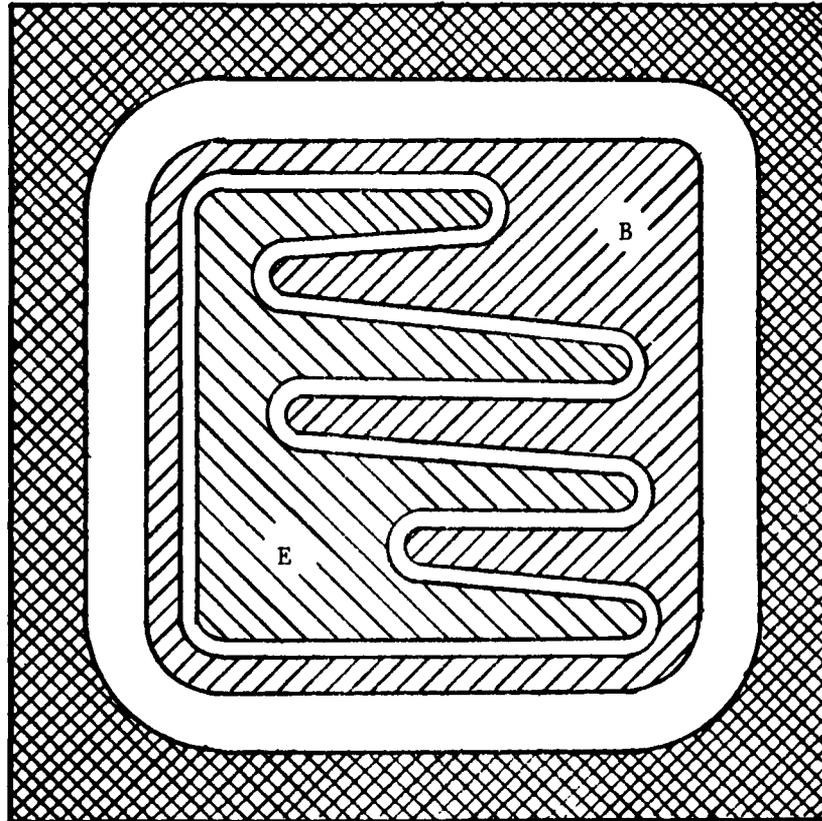
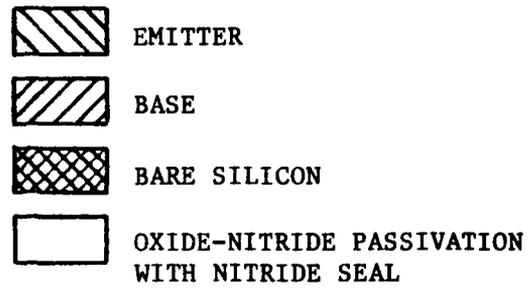


Figure 1 NPN Chip Geometry

-  EMITTER
-  BASE
-  BARE SILICON
-  OXIDE-NITRIDE PASSIVATION
WITH NITRIDE SEAL
-  FIELD RELIEF ELECTRODE

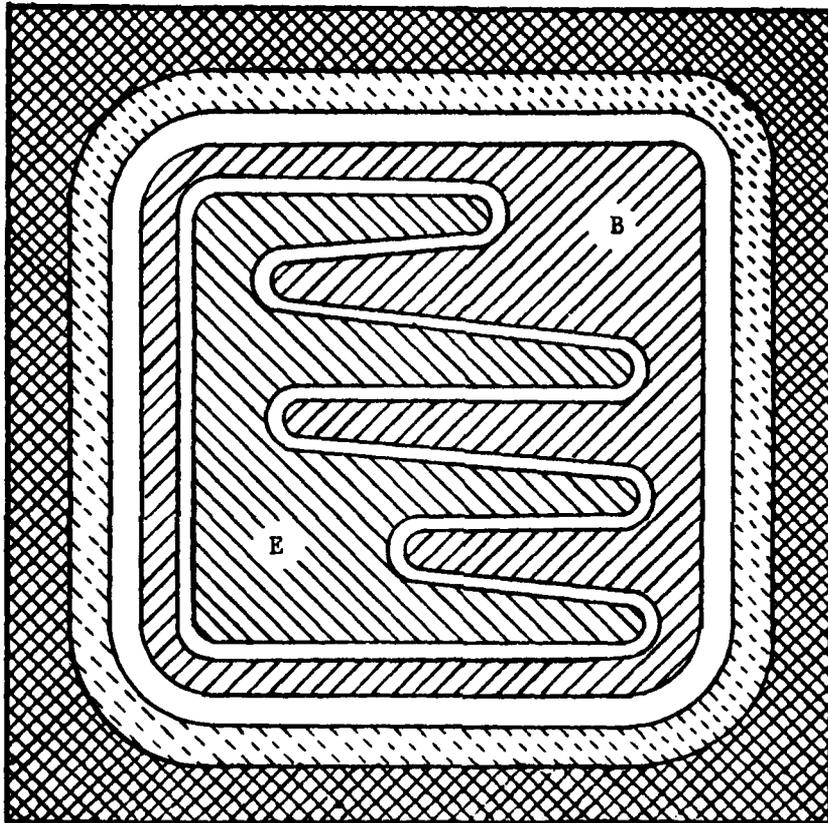


Figure 2 PNP Chip Geometry

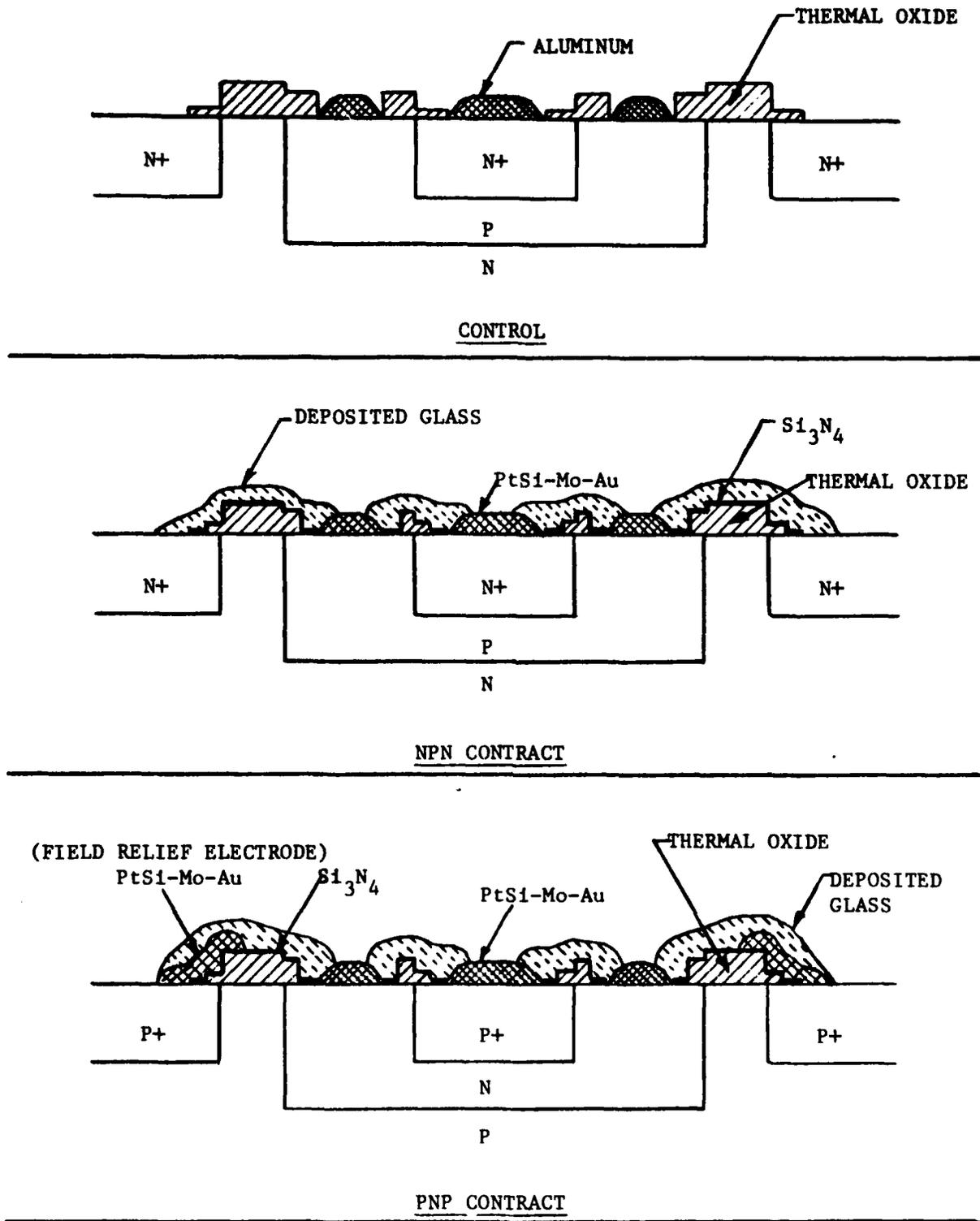


Figure 3 Device Cross Sections

TABLE I CHIP DIMENSIONS

SIDE	MILS	24
TOTAL AREA	MILS ²	576
BASE AREA (ACTIVE)	MILS ²	270
EMITTER AREA (ACTIVE)	MILS ²	113
EMITTER-BASE PERIMETER	MILS	97

TABLE II EPITAXIAL WAFER SPECIFICATIONS

CHIP	NPN	PNP
TYPE	NN ⁺	PP ⁺
SUBSTRATE DOPANT	ANTIMONY	BORON
SUBSTRATE THICKNESS (MILS)	11.5 - 12.5	11.5 - 12.5
SUBSTRATE RESISTIVITY (OHM-CM)	0.005-0.016	0.008-0.016
EPITAXIAL LAYER DOPANT	PHOSPHORUS	BORON
EPITAXIAL LAYER RESISTIVITY (OHM-CM)	3.5-7	3-6
EPITAXIAL LAYER THICKNESS (MICRONS)	16.2-23.8	16-20

in the material uniformity. However, all equipment used on the program has two inch diameter capability and all the processes have been run successfully on the larger diameter material.

Epitaxial processing of NN^+ wafers utilized the standard silicon tetrachloride decomposition above $1000^{\circ}C$ in the presence of phosphine. The PP^+ wafers were purchased from an outside vendor and then inspected and measured for surface perfection, layer thickness, and resistivity in the same manner as that used for in-house material.

One problem arose affecting some of the PP^+ wafers used for the pilot line. The layer resistivities looked normal based on dC/dV measurements using shallow diodes diffused into a sample of wafers pulled from the bank. When completed structures were made on pilot line lots, many of the wafers were found to have unexpectedly high BV_{CEO} values at wafer probe. This later resulted in high $V_{CE(sat)}$ values on the finished devices. It was discovered that a narrow region of high resistivity material existed deep within the epitaxial layer, and that the dC/dV test failed to disclose its presence because the shallow diode reached avalanche before the depletion layer spread into the "epitaxial spike" region. Automated spreading resistance measuring equipment has since been acquired and determination of the complete epitaxial profile is now a routine practice.

3. DIFFUSION

The standard process sequence for the NPN control chip was adopted, and manufacturing equipment, operated by shop personnel, was used for all the diffusion and oxidation steps during the engineering pilot line phase. The collector junction passivation consisted of approximately one micron of thermally grown silicon dioxide. A base predeposition step using boron was followed by a conventional dry-wet drive cycle to achieve the desired junction depth and to passivate the base with fresh oxide. The emitter diffusion sequence was similar with a phosphorus predeposition followed by a variable dry drive to adjust current gain, and a fixed steam oxidation step to passivate the emitter. The control was uniformly good on NPN lots with no serious problems being evident.

The PNP diffusion cycle is essentially analogous to that for the NPN device with the obvious switch in concentrations to a heavy emitter doping range for the boron and a correspondingly lower level for the phosphorus. Because this lighter phosphorus surface concentration does not produce a good ohmic contact in conjunction with the standard aluminum metalization, a shallow, high concentration, phosphorus layer is diffused into the base contact area following an extra photoresist step which is performed after emitter oxidation. At the start of the contract it was not certain if the final refractory metalization system would require this added diffusion step but it was decided to keep it in the cycle pending the final structure definition. The PNP diffusion control, as measured by lot-to-lot current gain variations, was not as tight as for the NPN counterpart. This contributed to an overall control problem involving the fluctuations in PNP current gain level with subsequent metalization and passivation steps. The corrective steps taken are discussed in Section II.8.

4. SILICON NITRIDE DEPOSITION

An established manufacturing silicon nitride process was used to provide the passivation layer and barrier on the device structure. The silicon nitride layer is deposited in either a fully automated stainless steel reactor or a large barrel reactor by the pyrolysis of silane and ammonia. This process has now been fully optimized for the particular chip structure, has been evaluated in a preliminary fashion and has found to produce more reliable units than the control units which represent the existing manufacturing process.

The pyrolytic reactor (shown in Figure 4), used in the initial phase, is a water cooled stainless steel apparatus with separate heater and reaction chambers, incorporating vertical gas impingement on the substrate wafers. The flow to each of the gas ports is separately balanced to achieve maximum uniformity, and a rotation mechanism is provided to achieve the maximum degree of wafer to wafer

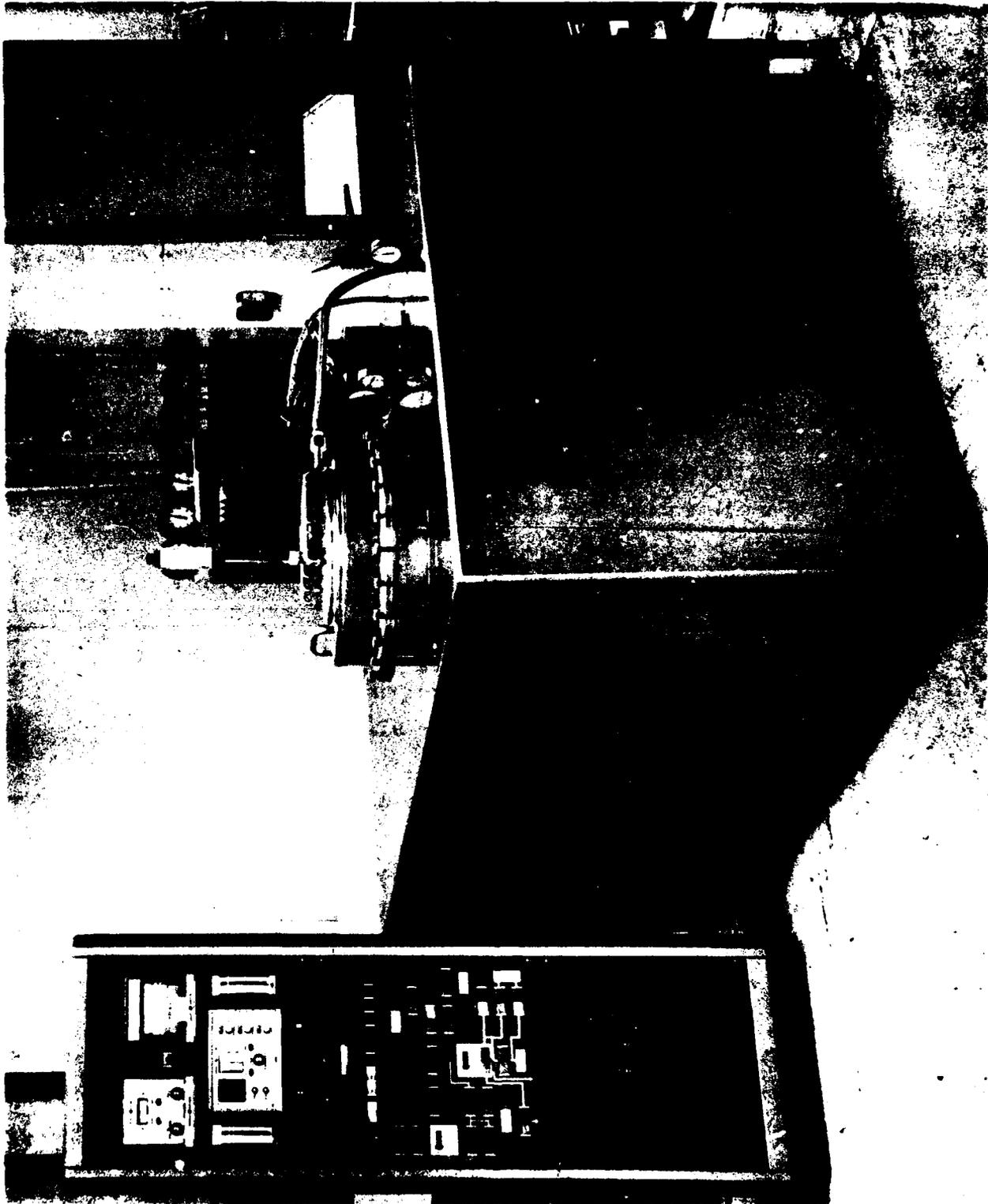


Figure 4 Pyrolytic Reactor System

layer uniformity during the deposition process. The barrel reactor (Figure 5) used for nitride deposition from the third quarter through the final phase, has a capability of handling 45 wafers per run. This reactor employs vertical gas impingement on the wafers from a central gas distribution inlet tube. Rotation of the barrel during silicon nitride deposition assures maximum uniformity of layer thickness and composition. The source gases for the reactors and the controls are established so that it is possible to deposit either silicon nitride or silicon dioxide without removing the wafers from the system. The control system for the stainless steel reactor is shown in Figure 6.

The deposition of silicon nitride, followed by a pyrolytic silicon dioxide overlay deposition, is accomplished in about one hour. The major events that occur during the cycle are:

- Vacuum; the chambers and gas manifold are evacuated to one micron pressure,
- Back-fill and Purge: the chambers are back-filled with nitrogen to atmospheric pressure and allowed to purge,
- Power; temperature is increased to the nitride deposition set point,
- Deposition: reactant gases are introduced to the chamber for the silicon nitride deposition,
- Purge: nitrogen flush and temperature change,
- Deposition; reactant gases are introduced for the silicon dioxide deposition,
- Purge and cooling.

The substrate wafers are loaded onto a clean quartz plate in a laminar flow hood. Twenty wafers two inches in diameter can be accommodated per run with the stainless steel manufacturing reactor system. At least two small diameter silicon wafers (N-type, about five ohm-cm) are also loaded on the plate so that measurements of the films can be made for process control and lot characterization.

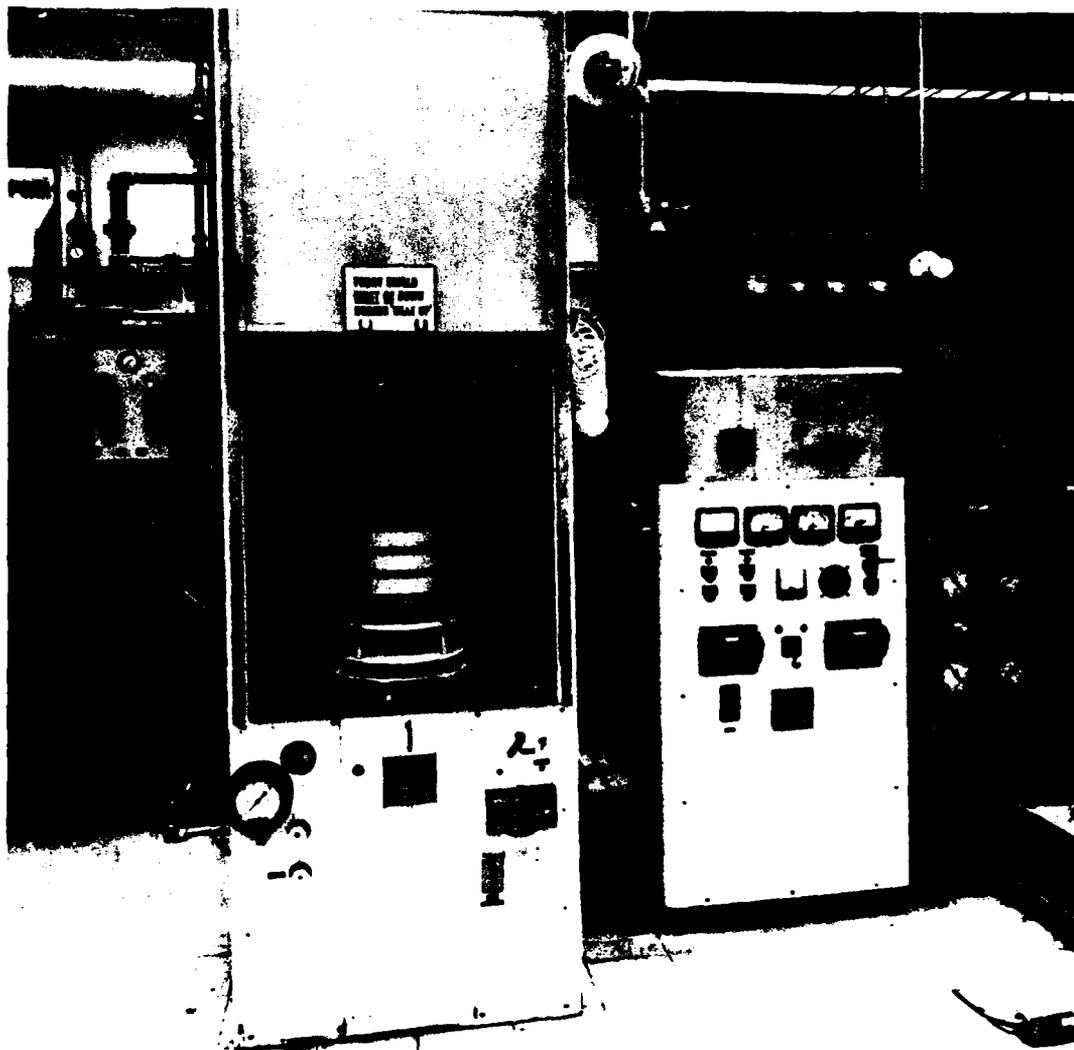


Figure 5 Barrel Reactor

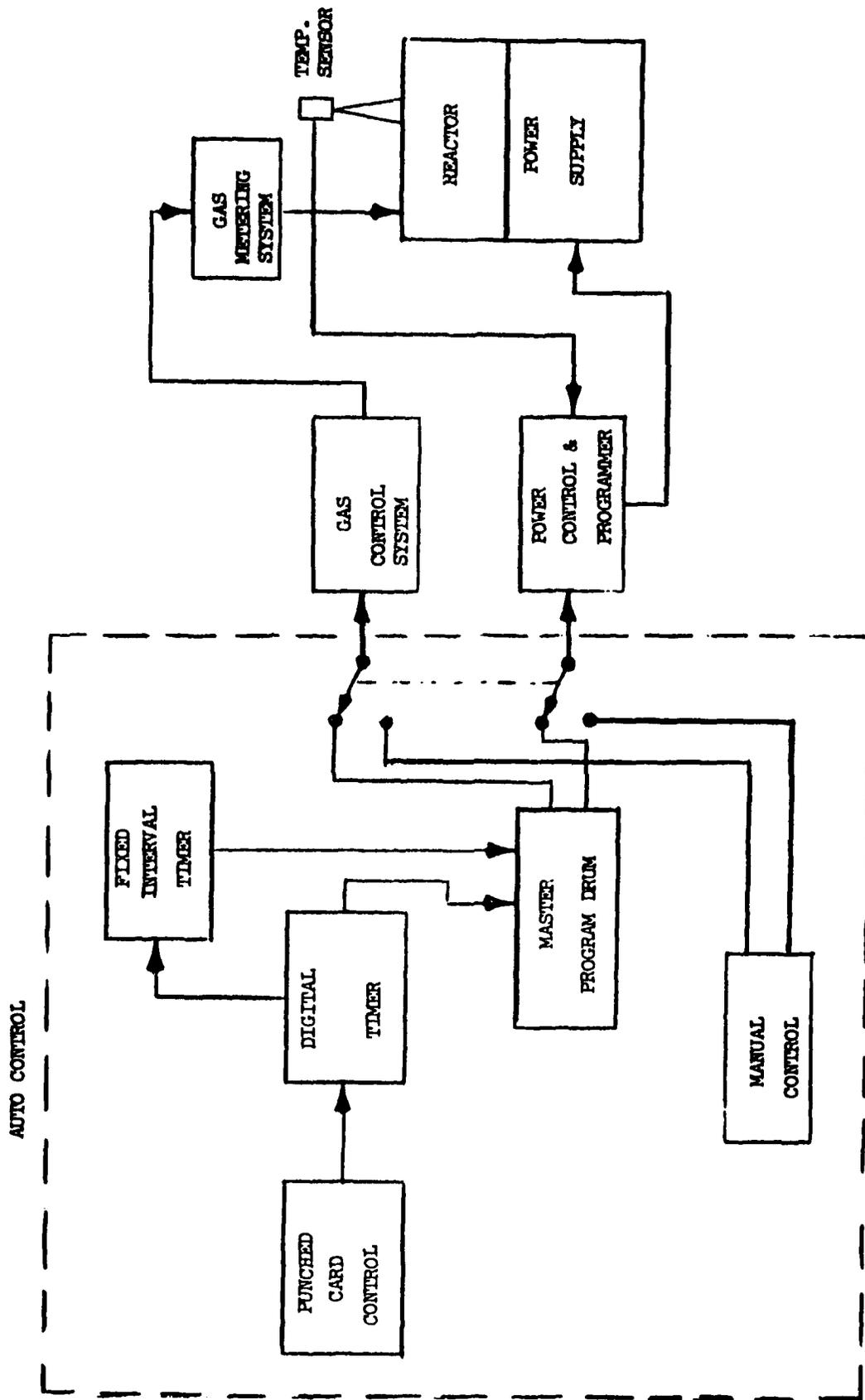
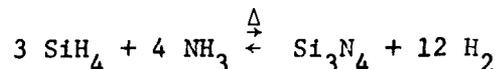


Figure 6 Pyrolytic Reactor Control System

The reaction of silane and ammonia is thermally activated and occurs, for practical purposes, between 750° and 1100°C. It is characterized by the equation:



Helium was used as the carrier gas during the first quarter of the program. A process change was made in the second quarter to substitute argon for helium as the carrier gas for the nitride deposition cycle to achieve manufacturing economies. Process control measurements of the properties of the deposited silicon nitride film revealed no detectable changes as a result of the change in inert carrier gas. During the fifth quarter, substitution of hydrogen for the argon carrier gas during heat-up and silicon nitride deposition was evaluated. Superior h_{FE} stability was obtained by using hydrogen as the carrier gas when depositing silicon nitride on NPN wafers. The life tests on NPN devices have confirmed the beta stability realized with the use of hydrogen. This modification was then adopted as the standard process for both NPN and PNP product types.

The thickness of the silicon nitride film is routinely determined by a spectrophotometer in the visible ultraviolet range. The integrity is monitored with a mild oxide etch, performed on a sampling basis for each deposition run. This test is capable of making the presence of pinholes in the nitride film very obvious, or conversely of increasing the certainty of the absence of pinholes.

An additional evaluation of the nitride was made by measuring the capacitance-voltage, CV, characteristics. The structure measured consisted of 1,000 Å of thermal oxide on N-type silicon wafers with 1,000 Å of deposited silicon nitride. The wafers were first metalized with electron beam evaporated aluminum, then annealed, and then capacitance-voltage curves were generated. The results, indicating a clean nitride, were V_{FB} (flat band voltage) ranging (pre-stressed) from 4.7 to 5.0 volts and ΔV_{FB} about 0.1 to 0.2 volts.

During the third quarter of the program it was determined that the nitride layer could be etched using standard photoresist patterning without the added step of a top oxide mask. Therefore, this oxide was omitted from lots processed through silicon nitride deposition after January 1, 1971.

5. METALIZATION

A large percentage of the problems associated with producing high yield and high reliability devices has been shown to be directly attributable to the metalization system used. The most widely accepted metal for both discrete devices and integrated circuits is aluminum. In high temperature processing, however, this system has inherent limitations because of the low melting points of aluminum and the aluminum-silicon eutectic. In addition, there are the well known reliability problems associated with the chemical activity and corrosion rate of aluminum, electromigration under high current conditions, and the well documented formation of gold-aluminum intermetallic compounds on gold wire bonds.

Several investigators have discussed the problem of selecting an appropriate metalization system for high temperature silicon contacts. The general conclusion has been that the only alternative to aluminum is a laminated system with gold as the uppermost level. The selection of the metalization system must take into account overall cost factors, available techniques for metal deposition, ease of processing, and the compatibility of the metal system with further device processing.

Prior to the start of this contract, several groups within the General Electric Company had explored high temperature, high reliability metalization systems in connection with internal device requirements. From this previous work, several available approaches were selected for further evaluation, and one primary system was selected to be optimized for the device structure pertinent to this contract. The system initially chosen to offer the best combination of properties consisted of platinum silicide followed by titanium, molybdenum, and gold. This metal system provides good ohmic contact to both emitter and

base regions of the transistors by virtue of the platinum silicide layer, a good bonding surface through the outer gold layer, and a high temperature processing capability with a coherent molybdenum barrier layer between the platinum silicide and gold. The titanium layer was initially included to reduce any oxide which might be present on the silicide, as well as to getter any contaminants present. However, it was found that the titanium was not necessary to obtain good contacts when platinum silicide was used, and it was subsequently eliminated.

The metal deposition for the NPN devices has been performed in a multi-target sputtering system located in the Integrated Circuits Center at Electronics Park. The process consisted of first depositing about 400 Å of platinum on pre-cleaned wafers, then sintering to obtain platinum silicide. The unreacted platinum over the oxidized regions of the wafer was removed with an aqua regia etch. The molybdenum and gold films were then sputtered sequentially without breaking vacuum. The thickness of each of these layers is about 5000 Å. The metalized wafers were then photoresist patterned and etched to remove unwanted metalized regions using the appropriate etches for each of the deposited metal films. During this etch cycle care must be taken to prevent undercutting of the molybdenum. If this occurs, the subsequent heat treatments are likely to cause the overhanging gold region to drop down onto the exposed silicide. This results in eutectic formation and destruction of the device.

During the production phase of the NPN device program it became apparent that it would be difficult and quite expensive to scale up the multi-target sputtering system for a large volume manufacturing capacity. In addition, the partial alloying of some metal pads had occurred on random wafers during the glassivation heat treatment after metalization. In response to these problems, further evaluation was carried out on molybdenum and gold deposition in a high volume electron beam evaporator. The system used consists of a Veeco diffusion pump module, a Temescal multi-hearth electron gun and target assembly, and a Temescal electron gun power supply. This system is capable of processing twenty-one wafers two inches in diameter per cycle. It was found that heating the substrates during the molybdenum deposition and then allowing them to cool before depositing the gold produced devices of equal quality to the sputtered metal process, but with significantly improved resistance to alloying during glassivation. This

resulted in the replacement of the sputtering process with the electron beam process as the standard for the molybdenum and gold deposition. All of the PNP devices used in this contract were produced with the electron beam metal. Material produced with this final process has been found to be consistently capable of withstanding the glassivation temperature without alloying.

A major portion of the metalization process optimization effort on this contract has been concerned with the formation of the platinum silicide layer. In the initial stages of the contract considerable difficulty was found in consistently producing uniform and complete silicide formation. After investigating several possible causes for the problem, it was determined that the wafer cleaning process used for conventional contacts was not adequate for the forming of platinum silicide. New cleaning procedures consisting of treatment in a strong oxidizing solution to remove any organic residues on the wafer, followed by a final dip etch in an HF solution to remove any oxide remaining in the contact windows, yielded consistent and reproducible silicides.

Even after consistent sintering of the platinum was achieved, several anomalies were noted in the platinum silicide. The appearance of these anomalies depended upon platinum thickness, deposition conditions, and the platinum etch cycle. Examples of the most critical features observed are shown in Figure 7. The edge of a silicided contact window after the excess platinum has been removed is visible and, in this case, small dendritic structures may be observed which extend up from the contact area and overlap the nitride layer at the edge of the contact. These small protuberances extend above the normal platinum silicide surface and provide a channel for gold diffusion through the molybdenum layer, with subsequent formation of the gold silicon eutetic during glassivation. The appearance of these structures seems to be dependent upon both platinum thickness and the sintering cycle. However, the particular control parameters used in the final process were found to minimize this problem.



Figure 7 Contact Window Edge Defects and Overetch Effects

The effects of overetching a silicided wafer in aqua regia also are shown in Figure 7. Here, small scallop shaped etch pits formed at the edges of the contact area. If further etching is performed, these pits will continue to grow until the entire silicide layer is removed. Use of a thin platinum layer and minimizing the etch time in the final process has eliminated this problem.

In conclusion, the platinum silicide-molybdenum-gold metalization optimized on this contract has been found to be a high volume, highly reproducible system which is compatible with high temperature device passivation techniques. Further, it is chemically more insensitive than aluminum to corrosive conditions.

6. GLASSIVATION

A glassivation process was developed which had the inherent properties of being a good barrier to alkali ion migration and moisture. Also it exhibited good adhesive properties to the contact metal. As a good "rule of thumb", the farther the junction is from the epoxy encapsulation the better the junction will be passivated. In practice, however, there are several trade-offs that must be considered since an extremely thick passivation film is not practical to achieve. Therefore, some thickness for this passivation layer had to be chosen which would be compatible with all the processes involved. At first, the selected number was to be about three microns of the glass passivating layer.

Depositing a layer this thick presented a problem as to which method of deposition would be best. The three basic processes commonly used in the semiconductor industry today are: chemical vapor deposition, sedimentation, and sputtering. Chemical vapor deposition offers the advantages of a clean and low temperature process. However, deposition times are considerably longer at these temperatures for the thickness required and only silox type glasses may be deposited with ease. The silox type of glasses have not proved to be good barriers since they tend to be fairly porous. Also, the long deposition cycle seems to irreversibly degrade the devices. Glass sputtering was also non-acceptable because of the extremely long deposition times, which would run on the order of a day for the required thickness.

This left sedimentation as a viable process. Sedimentation was thought to be ideal since it allowed many different glasses to be investigated. Deposition time was not a problem since the process depends only on the time it takes to centrifuge particles out of solution onto the wafer substrate, and on the size and capacity of the centrifuge system.

In selecting the type of glass to be used, it was necessary to remember that the most important property is the ability to act as a barrier to alkali ions and moisture. Therefore, the first type of glasses evaluated were the lead borosilicates since they exhibit the most desirable barrier properties. Also, the coefficient of expansion was a near match for the device material. The first lead borosilicate tried was a proprietary glass previously used for other applications in the General Electric Company. It was believed to have excellent barrier properties and ease of deposition. However, it was found that the firing temperature was so high that gold alloying was unavoidable. Also, the glass exhibited severe cracking and was difficult to etch. After some consideration of other candidates, it was decided to try the Innotech 550 type lead borosilicate glass. Since the adoption of Innotech 550, the glassivation process by sedimentation has been generally successful and controllable. However, adherence to the gold pads can be a problem and attempts have been made to get a glass which will not be in stress when it is in contact with a gold surface. This is a difficult problem to overcome since the coefficient of expansion of gold is 143×10^{-7} per degree centigrade whereas most lead borosilicates are in the $50-70 \times 10^{-7}$ range. A glass does exist which has a range from $120-125 \times 10^{-7}$ but no samples have yet become available for experimentation.

To develop a consistent and easy sedimentation process, a solvent system is required as the suspension medium. The most important property is the dielectric constant of the solvent system. In other work it has been found that solvents with dielectric constants higher than the glass being used are necessary in order to obtain films which adhere uniformly. Since Innotech 550 glass has a dielectric constant of 15, a mixture of acetone and methanol with a dielectric constant of 26 was used for the suspending medium. When the dielectric constant is less than the glass, the glass particles tend to agglomerate and settle out of solution permanently. When the dielectric constant is too high (>30) there is a tendency

for the glass particles to swirl with any solvent current, thus producing stresses of uneven glass on the wafer.

Once the glass had been compacted down to the substrate by the sedimentation process, it had to be fused to form a continuous, pinhole-free film. It was found that the ambient was of considerable importance when trying to achieve a good pinhole-free film during firing and that the minimum time allowable for fusing should be employed. A pure oxygen ambient yielded the best results at 560°C and the total firing time was less than 15 minutes. However, pure oxygen had corrosive effects on the exposed molybdenum and was deemed to be harmful to the device. A mixture of oxygen and nitrogen (simulating air) was tried and found to be corrosive but not nearly as much as the pure oxygen. This corrosion is probably enhanced by the solvent system employed. Therefore, steps had to be taken to correct this problem of which one alternative was to change the metalization and another was to attempt to try to seal the contact before the sedimentation process. Attempts with other metalization systems did not yield satisfactory results. Sealing of the contacts was then tried by the use of a silox glass layer. Results after firing with the sealing glass confirmed the fact that it stopped the corrosion of the molybdenum.

Obtaining a continuous glass film seemed to be a problem until good control of the particle size, glass purity, and solvent purity was attained. The most frequent fault found was pinholing, and occasionally the aforementioned swirling occurred. The swirling seemed to be a direct result of a questionable solvent, methanol in particular. Certain lots of methanol seemed to upset the sedimentation process, so extensive analyses of these problem lots of methanol were performed. All properties seemed very good with the exception of the ultraviolet absorption edge profile. The interpretation of this was not attempted but unidentified contamination in the ppm range remains a possibility. Particle size control was very important in controlling thickness and pinholes. Many different centrifuging times and speeds were explored to attain a consistent particle size and therefore a good, smooth continuous glass film. The relatively thick film, originally thought to be needed, turned out to be bad from a particle size consideration since large particles resulted in bumpy glass and pinholes occurred more frequently thus making photoprocessing and etching very difficult. Also, the barrier

effectiveness was not as good because of these inherent defects in the thicker films. Therefore, the suspension solution was made from reagent grade acetone and glass by mixing one gram of glass to every six ml. of acetone and centrifuging at 100g's for 20 minutes. This solution was calibrated each time that it was mixed to be sure that the particle size upon sedimentation yielded a film about 1.2 microns thick after being diluted a proper amount (1:1) with methanol and centrifuged at 1600g's for 10 minutes. The calibration was necessary to be sure that different glass lots had the same particle size and purity.

After the process optimization was completed for laying down and firing a consistent glass, the film had to be photoprocessed and etched in order to provide a contact area for the leads. The thicker glass (3 microns) proved to be difficult to control in etching and in holding the resolution, probably because of the large crystallite size after firing and the unevenness of the film. Therefore, it was decided to use a thinner glass (approximately 1.5 microns) which would still preserve the good barrier properties and provide ease of etching. Also, it was necessary to find a good etchant for the lead borosilicate glass, since normal buffered hydrofluoric acid etchants failed to work. The etchant used was "P" etch which is a dilute mixture of hydrofluoric acid, nitric acid, and water. This etch yielded consistent results and no problems were encountered, thus making a good routine production process. The final process settled on is:

- Deposition of about 600 \AA of silox glass to seal the molybdenum,
- Application of the glass suspension solution and centrifuging at 1600g's for 10 minutes,
- Firing at 560 $^{\circ}$ C for 8 minutes (Film thickness about 1.2 microns; Ambient - Synthetic dry air),
- Application of a second glass suspension solution and centrifuging at 1600g's for 10 minutes (total film thickness about 1.6 microns),
- Firing at 560 $^{\circ}$ C for 5 minutes (Ambient - Synthetic dry air).

With the second glass application, any pinholes in the first were covered up and it was felt that the film had much superior integrity compared to a single coat film. The system presently used is capable of doing six two-inch wafers every half hour. New centrifuge cups capable of quadrupling the output have been made and tested.

7. PHOTOLITHOGRAPHY

The masking demands required by the topography of the contract vehicles (0.25 mils minimum tolerance) were well within the capabilities of both the Engineering and Manufacturing photoresist facilities. Therefore, standard processes, equipment, and control procedures were adequate.

Silicon nitride etching was performed with boiling orthophosphoric acid using a reflux condenser to maintain a fixed composition. The etch time for a wafer lot was based on the nitride layer thickness and the etch rate of a control wafer from the same nitride deposition run. A constant over etch time was applied to assure complete removal of the final invisible traces of the nitride film from all contact windows. The absence of film was further verified by a sample electrical check.

For patterning the molybdenum-gold contact areas, a commercial cyanide base gold stripper and an in-house mixture containing phosphoric and nitric acids were sequentially employed. The final photoresist step is used to define the bonding pad areas and requires etching through the 1.5 to 2 microns of glass and the thin silox layer separating the glass from the metalization. An early problem of undercutting the glass with buffered HF was solved by changing to "P" etch. Buffered HF was then used for the silox layer only. By this procedure undercutting troubles were avoided and traces of glass left by the "P" etch were completely removed as the undercoating of silox dissolved.

8. PILOT LINE

A. NPN Devices

The material processing plan for the contract called for a steady flow of material at the input rate of one wafer lot every other week starting during the second quarter of 1970. Lot sizes were generally 20 wafers but sometimes were increased to 30 or 35 to provide extra material for process optimization experiments. With each lot a group of control wafers was run with the same

oxidation and diffusion processing but with standard silicon dioxide passivation and aluminum metalization. Also, the newer processes were added progressively such that chips were produced with the basic structure plus silicon nitride only, as well as with nitride and refractory metalization but no glassivation. Starting in June 1970, the full passivation and refractory metal sequence became standard practice.

During the course of the pilot operation it was noted that wafers with nitride seal passivation did not change in h_{FE} under the low temperature bake cycles which have been previously reported to be effective in adjusting the h_{FE} distribution. In the early phase of the program, h_{FE} was found to drop substantially during the heat-up cycle just prior to nitride deposition. This degradation effect was eliminated by changing the ambient used in the nitride process from an inert gas (helium or argon) to hydrogen whenever refractory metalization was to be used. When aluminum metalization was used in conjunction with nitride (as it was in several early pilot runs) beta lowering due to the nitride cycle in helium or argon was capable of being corrected by subsequent sintering or baking.

B. PNP Devices

During the second half of 1970, PNP pilot lots were started through the cycle at the rate of 4 lots per quarter to identify any unanticipated difference from the NPN structure. Starting with the first quarter of 1971, PNP lot inputs were increased to the rate of one every two weeks.

With the experience gained from the substantial number of NPN lots run before starting the PNP, the main process conditions were well defined for the nitride, refractory metalization, and glassivation operations. However, the availability of an electron beam evaporation system with substrate heating sufficient for molybdenum deposition prompted a shift from sputtered molybdenum-gold to the electron beam evaporation system because of the higher volume per run capability and the avoidance of gold alloying troubles which occurred sporadically when the metals were sputtered.

The principal problem of the PNP pilot line activity was h_{FE} control. The beta levels have been somewhat variable after diffusion and each step of the subsequent passivation and metalization processes caused wider beta fluctuations than had been the case for the NPN structure. Following the nitride deposition and its associated photoresist step, the betas were extremely high, with excellent low current beta holdup because of the hydrogen ambient in the nitride reactor which reduced the surface state density. Little change was observed during the platinum deposition but degradation occurred at the platinum silicide sintering step.

Some recovery of beta generally was seen during the molybdenum gold and silox depositions, but final distributions peaking near the center of the prime range were difficult to obtain. This problem still exists and is being investigated from the points of view of recovery bakes that are effective in the presence of a nitride seal. Process modifications are being assessed to reduce the severity of beta degradation during metalization.

9. CONCLUSIONS

Reviewing the results obtained from the overall NPN-PNP pilot phase of the contract leads to the following observations:

- The new passivation and metalization processes are reproducible and manufacturable. In all cases, feasibility has been demonstrated in equipment capable of run sizes compatible with volume production at reasonable cost.
- Although electrical yields in wafer form were not a prime consideration of the contract, they were constantly monitored and found to be equivalent to the respective NPN and PNP product lines having standard aluminum metalization and silicon dioxide passivation.

- The nitride process is well defined and reproducible. The transfer of the technology to volume production may present some difficulties with pinholes or attack from phosphorus glass until the process is well debugged.

- Adherence between the glass and the gold is still not completely optimized. As a result, some cracking and chipping can occur in the vicinity of the bond areas. A flash of molybdenum or tungsten between the glass and the gold is being investigated to avoid this difficulty.

- Since platinum deposition is the only process which requires sputtering equipment, and since the platinum sintering step degrades beta, a study should be made to see if the platinum silicide can be eliminated.

SECTION III

DEVICE ASSEMBLY PROCESSING

The device assembly, encapsulation and testing was done with automated facilities for mounting, bonding and casting of transistors. The overall assembly flow is shown in Figure 8 and the many inspection points are indicated on the flow chart. This mechanized transistor production facility was previously developed, with the aid of a ribbon concept of manufacturing, to avoid piece by piece handling. In this approach, which has been in production since 1962, pellets are mounted on a kovar ribbon and then pass through several automated steps in the manufacturing cycle to where the ribbon is cut apart into individual devices. This approach solved many orientation and parts handling problems, has resulted in high assembly yields, and has improved the reliability of the devices through elimination of some of the human variability factors.

The various steps in the assembly process are described in some detail in the following paragraphs, along with some specific process assembly optimization checks which were made to compare the interaction of the improved performance pellet to the standard one in the assembly system.

1. RIBBON PREPARATION

The ribbon is gold plated kovar foil which is prepared for pellet bonding with the dimple and preform machine. This equipment takes a plain strip from the spool at the left, draws it through forming and welding stations, and rewinds it on the spool at the right as illustrated in the assembly (ASM) flow chart of Figure 9. At the forming station a die is used to make a dimple in the strip at regular intervals. This dimple is then used as an indexing guide in the other equipments. Gold-antimony solder preforms are welded at a suitable position between the dimples. The preforms, which are used later in the pellet bonding process, are sheared from gold foil drawn from another spool at the welding station.

ASSEMBLY PROCESSING FLOW CHART

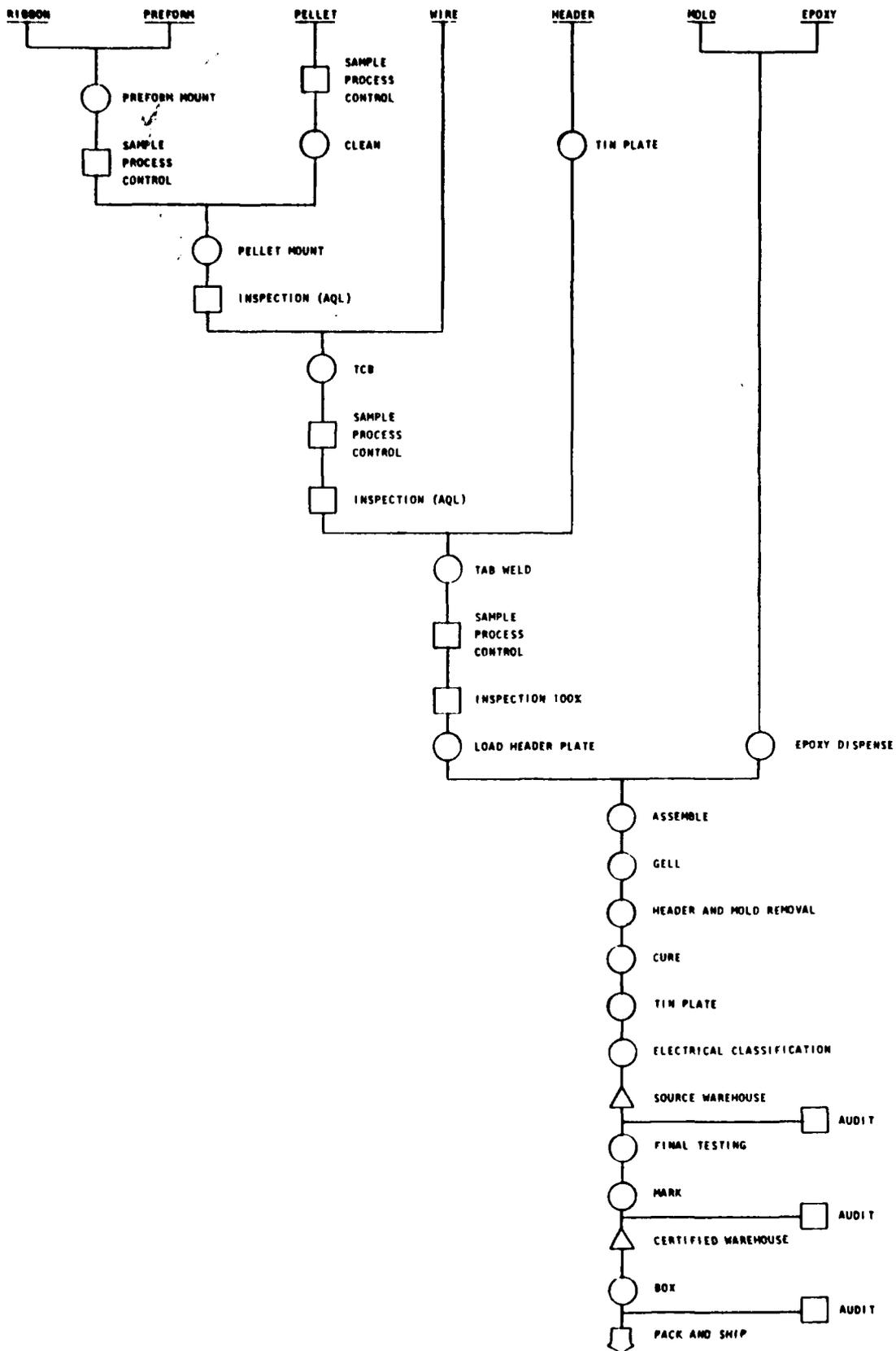


Figure 8 Assembly Processing Flow Chart

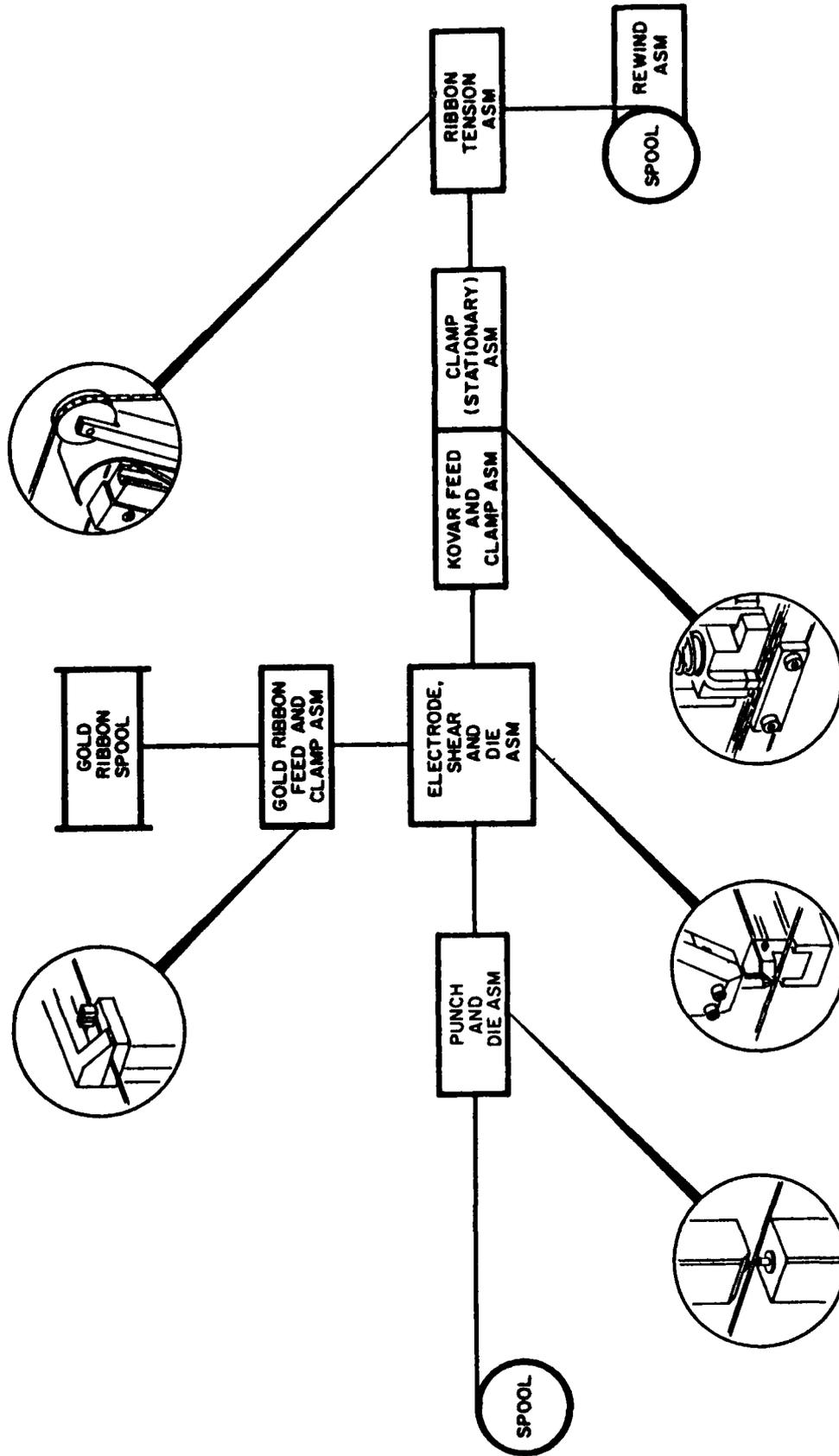


Figure 9 Kovar Ribbon Flow Diagram

2. PELLETT MOUNT

The overall process flow is illustrated in Figure 10. The dimpled ribbon, with preforms attached, is drawn off the spool and indexed so that each preform is stopped momentarily in front of the machine operator. The chips, loaded on a freely movable stage are observed through a stereoscopic microscope. The stage is positioned to align one chip at a time with the alignment reticle in the microscope. A vacuum pick-up needle, moving at the indexing rhythm, picks up the aligned chip and places it on the preform, on the strip. During this process the strip has been heated to raise the preform temperature to the level required to form a silicon-gold eutectic bond of the silicon pellet and gold preform to the kovar ribbon. Then the strip moves on, the temperature is reduced to set the bond, and the strip is spirally wound on a magnetic drum.

3. LEAD WIRE ATTACHMENT

At the third machine, the strip is fed from the magnetic drum through the fixture and back on the drum with the wire connections having been made to the chips as shown in the flow chart of Figure 11. As each chip comes into position on the bonding fixture, the machine draws gold wire off a spool and grasps the wire with two tweezers. The wire is cut so that each tweezer holds the proper small length of wire. A wedge shaped thermocompression bonding tool is used to bond each wire in turn to the proper bonding pad on the chip.

4. COMPLETION OF ASSEMBLY

The final process steps (before encapsulation) involve shearing of the kovar ribbon and attachment of the device subassembly to the external leads. This is performed in the sequence shown in the flow diagram of Figure 12. The equipment used is the tab weld machine which draws the ribbon from the magnetic drum, welds it to the collector lead, shears the strip and passes the header on to the wire to post bonders. The bonders automatically form the gold leads against the base and emitter external leads and bond them. The machine is then used to load the headers into a slotted fixture.

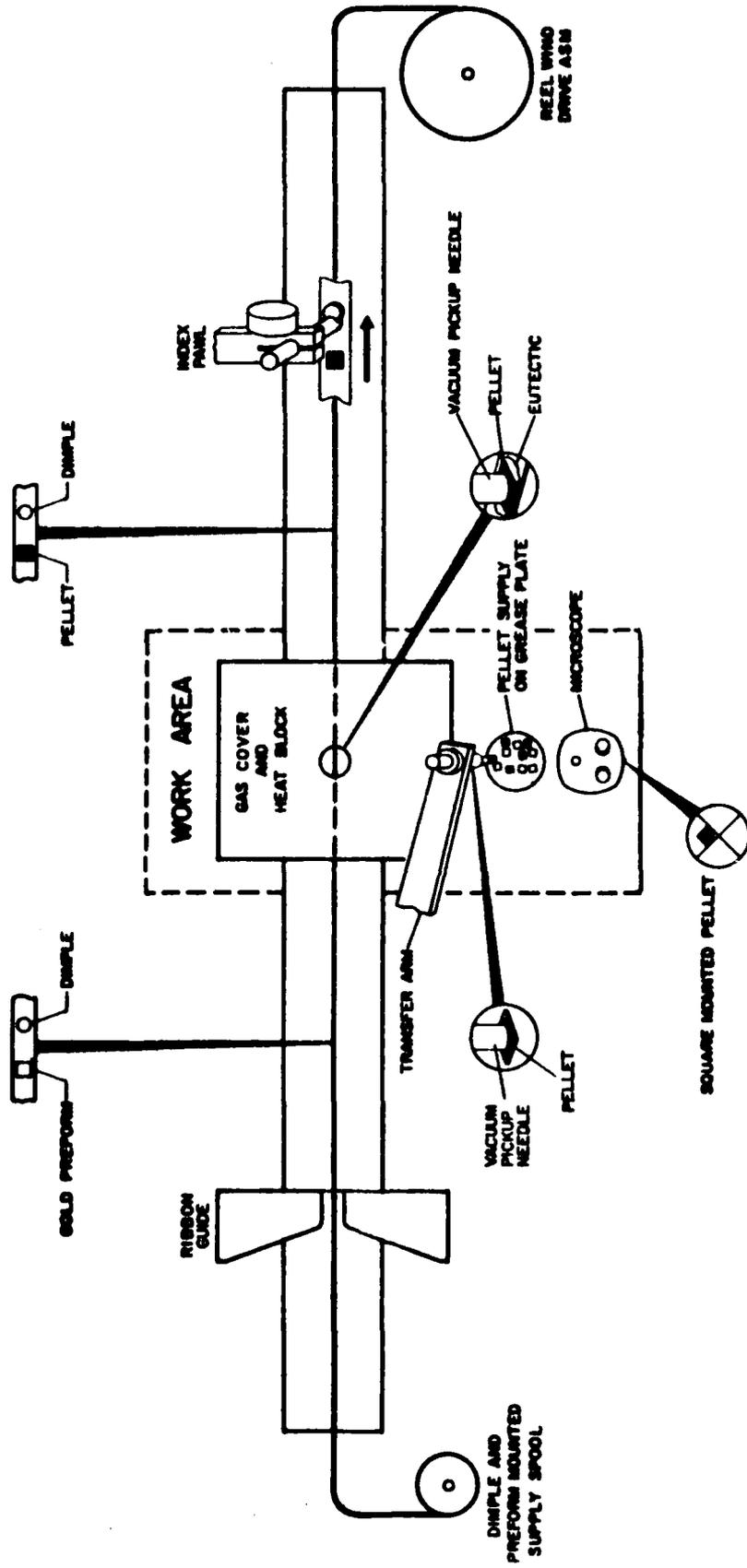


Figure 10 Pellet Mount Block Diagram

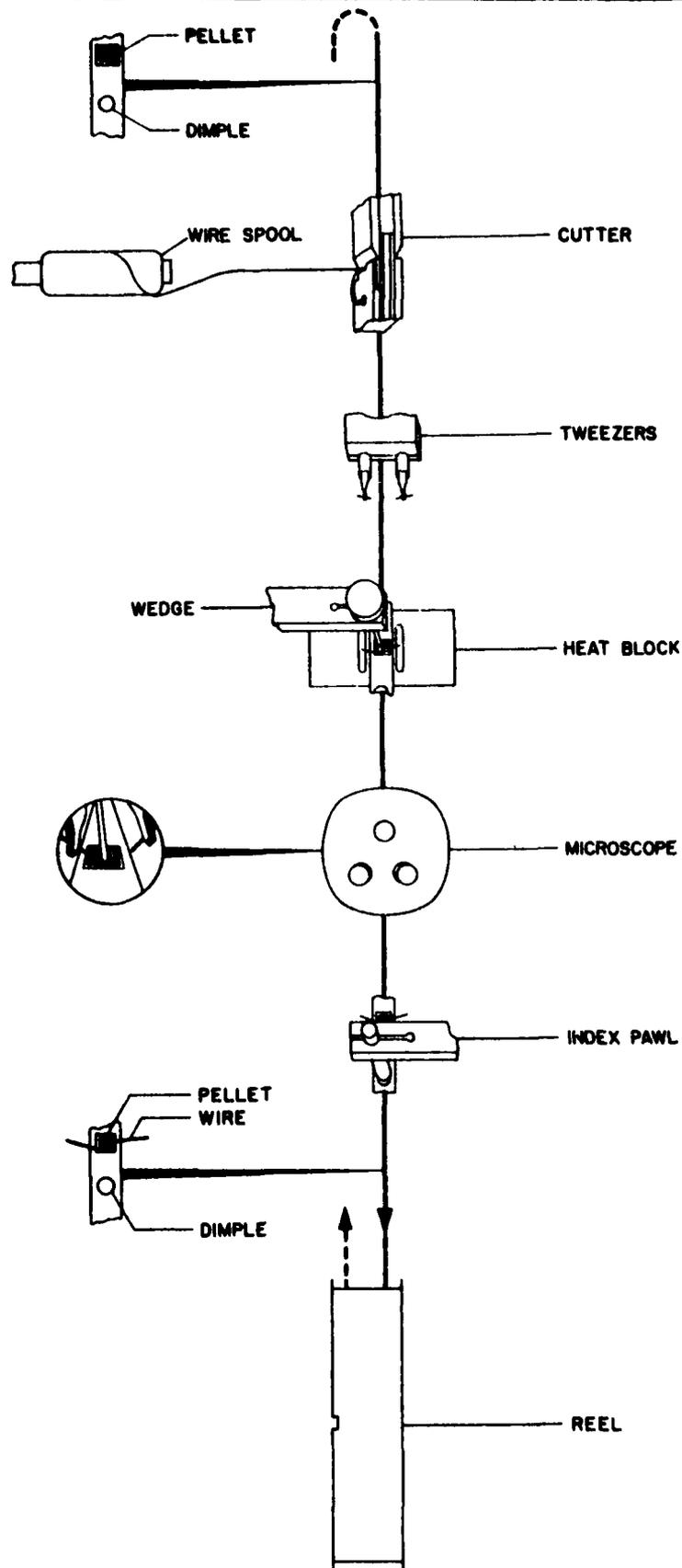


Figure 11 TCB Machine Flow Diagram

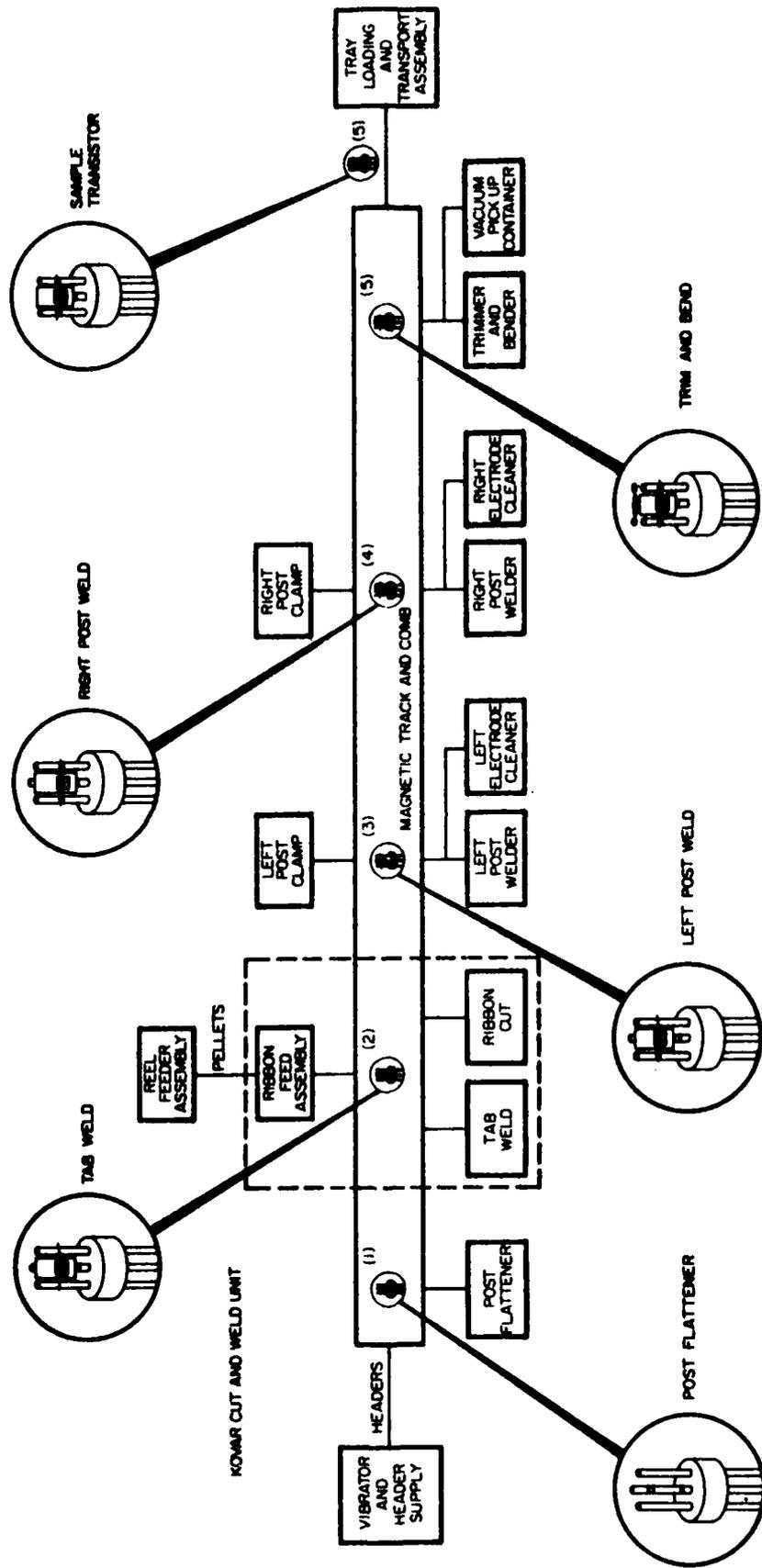


Figure 12 Tab Weld Machine Flow Diagram

In addition to the welding operations, a series of flattening, shearing and trimming steps are performed. When the assembled header has completed processing through the tab welder, it is a complete transistor assembly, ready for testing and final epoxy encapsulation.

The tab welder is completely automatic. Once in operation, an operator, or attendant, is needed merely to observe for malfunction and to keep material supplied to the machine.

3. ENCAPSULATION

For encapsulation, the devices are inserted, upside down, in D-shaped cavities filled with epoxy, with the flat side of the D behind the chip. The flat side is used for orientation during finishing and testing, and during placement in circuit boards.

The proprietary composition of the epoxy is rigidly controlled by incoming inspection. An infrared spectrophotometer is used to measure organic ingredients of the epoxy. Regular samples of epoxy are measured and analyzed. When infrared radiation is passed through an organic compound, certain wavelengths are absorbed and others transmitted. The infrared spectrophotometer passes infrared radiation through the sample, then measures the amount transmitted at each wavelength. From this information a spectrogram is drawn which accurately "fingerprints" the molecules in the sample. These infrared spectra are then used as the basis for both qualitative and quantitative analysis. The exact position of the absorption bands in a spectrum indicates the chemical composition and structure of the sample being analyzed. The depth of the band is a measure of the amount of sample present and can be used in determining characteristic absorption bands in the infrared range. Measurement of the organic ingredients of the epoxy and acceptance only of material which meets standard criteria assures homogeneity of the epoxy encapsulant.

Atomic absorption spectrophotometry is an analytical method used for analysis of precise amounts of the major components in a material. A solution containing some of the element of interest is sprayed into a flame where the droplets are dried and volatilized. Once this occurs the components are broken down into clouds of neutral atoms. A light beam, from a hollow cathode lamp with the cathode constructed of the same element being measured, is passed through this flame and the neutral atom absorbs the same wavelength of light it would emit if it were excited. The quantity of light absorbed is a function of the concentration of the element of interest in the original solution. This instrument is used to measure and control the amounts of key components in the epoxy encapsulant.

6. FINAL TEST

After encapsulation, transistors are tested and classified automatically. The leads are slid between three pairs of copper plates, which form the test contacts; thus avoiding the necessity of inserting the leads into test sockets. The automatic loading equipment is shown in Figure 13. This equipment operates with an external test set such as the Attribute Test Set shown in Figure 14. The Electronically Programmed Attribute Test Set (E-Pat) shown in Figure 14, in conjunction with appropriate peripheral equipment, is one such automatic system for testing and classifying semiconductors. A built-in core memory provides storage of up to 20,480 bits of testing and classifying instructions with a capacity for providing up to 256 individual tests organized into routines of up to 64 tests per routine.

7. BOND STRENGTH

There was some initial concern about the strength of the wire bonds on the standard assembly process since it was optimized using gold wire and aluminum bonding pads, not the refractory metal contact system. Samples of the refractory metal contact system were processed on the regular assembly tooling for a comparison to the regular aluminum contacts. The criteria used included:



Figure 13 Loader Segregator

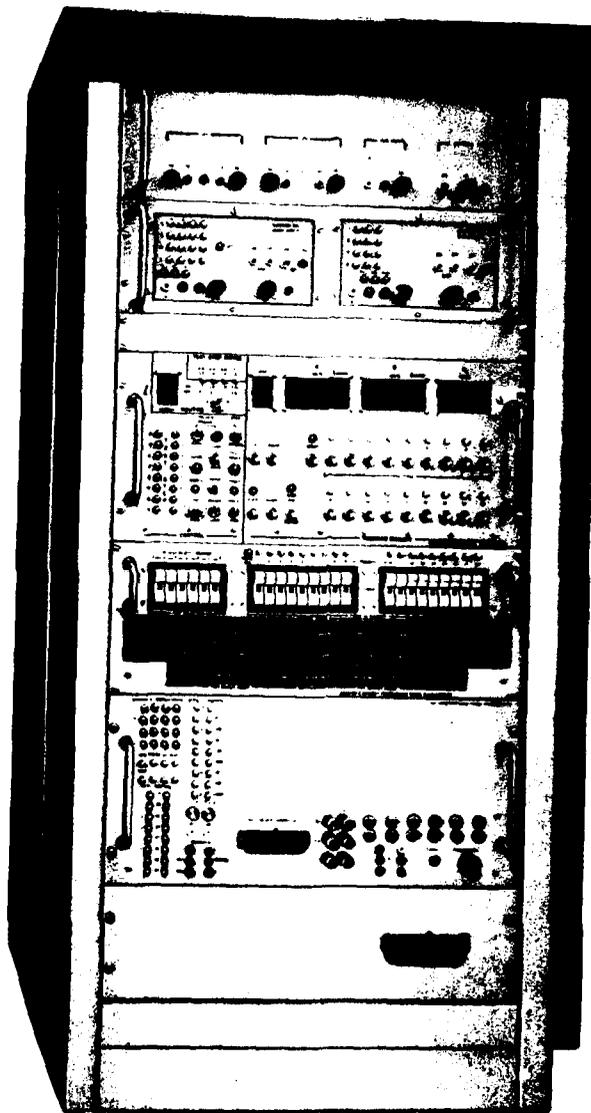


Figure 14 Attribute Test Set

- Bond strength (both pull and peel strengths),
- Bond deformation,
- Drop shock,
- Centrifuge,
- Steam atmosphere.

The refractory metal system was slightly superior to the aluminum system as illustrated in the comparison on pull strength shown below.

Bond Strength in Grams
(1.5 mil gold wire, 50 gram wedge pressure)

	Production Aluminum System			Refractory Metal System		
	Max.	Median	Min	Max.	Median	Min
Emitter	12	7	3	13	11.5	10
Base	8	6	3	13	10	6

In general, the breaking point of this refractory metal system was the gold wire, rather than the bond, which indicates excellent bond strength.

For a check on optimization of wedge force, pellet samples from two wafer lots were mounted on T0-18 headers. Both of the lots were processed with the full silicon nitride layer, refractory metalization and glassivation. Gold lead wires, 1.5 mils in diameter, were thermocompression bonded to the pellets and then bond strength measurements were made. The median bond breaking values observed were:

PULL TEST

(Force parallel to surface) - grams to break

Lot	Wedge Weights (gm)		
	30	50	70
1012	11	9.5	11.5
1014	9.0	8.5	9.0

PEEL TEST

(Force normal to surface) - grams to break

Lot	Wedge Weights (gm)		
	30	50	70
1012	10	7.5	9.0
1014	9.5	9.5	8.0

In addition, stress tests were conducted with 40 bonds tested for each stress test. There were no bond failures after any of the tests.

The stress tests were:

- Boiling water for 24 hours, no header caps,
- Drop shock, 5 blows in each of 6 planes, 1500 g, 0.5 msec,
- Centrifuge, 20,000 g in each of 6 planes,
- Centrifuge, 50,000 g in each of 6 planes.

8. INSPECTION

The transistors are subjected to inspections and numerous sampling tests by the Quality Control organization, as indicated in Figure 8. All chips are tested and inspected before they are bonded. After lead bonding an inspector examines the strips to detect misplaced or missing wires, missing chips, or inadequate bonding. Before encapsulation, the header assemblies are checked for similar defects, as well as for chip or header damage, and for shorted or open leads. The machine and manual processes are monitored by periodic checks on such conditions as weld strength, weld positions, and preform-to-chip bonding.

SECTION IV

EVALUATION PROGRAM

The comprehensive evaluation test program used for this contract was statistically designed to establish uniform standards for military qualification of plastic encapsulated semiconductors. The program results provided the necessary performance data to develop lot qualification procedures. These procedures can be used to modify the present MIL-S-19500 requirements which are adequate for hermetic units but not for plastic encapsulated units. The stress procedures involved step-stress, combination and sequential stresses, extended stress-in-time testing to 7500 hours, data analysis and failure analysis. The stresses were applied to the completed contract structures and the control structures, in accordance with the terms of the contract. In addition, some of the stresses were applied to partial structures. That is, devices with only the silicon nitride barrier added were stressed, as well as devices with the nitride and the refractory metalization. The evaluation program can be divided into four parts, each of which will be discussed separately.

1. PRELIMINARY STEP-STRESS AND SPECIAL TESTS

The preliminary step-stress and special tests portion of the program, shown in Figure 15, was referred to as the Phase I tests and was designed to obtain a rapid response survey of the stress space. These tests were applied to the partial structures as well as to the completed contract and control devices. The purpose of the step-stresses was to:

- Provide proper candidates for failure analyses by inducing and identifying the failure modes and mechanisms, and determine the acceleration with both the stress and stress level
- Establish the threshold and ultimate capability of the plastic structures,
- Determine effective stress screening and critical parameter response,

PHASE I COMPREHENSIVE STEP STRESS AND SPECIAL TESTS FOR RAPID RESPONSE SURVEY

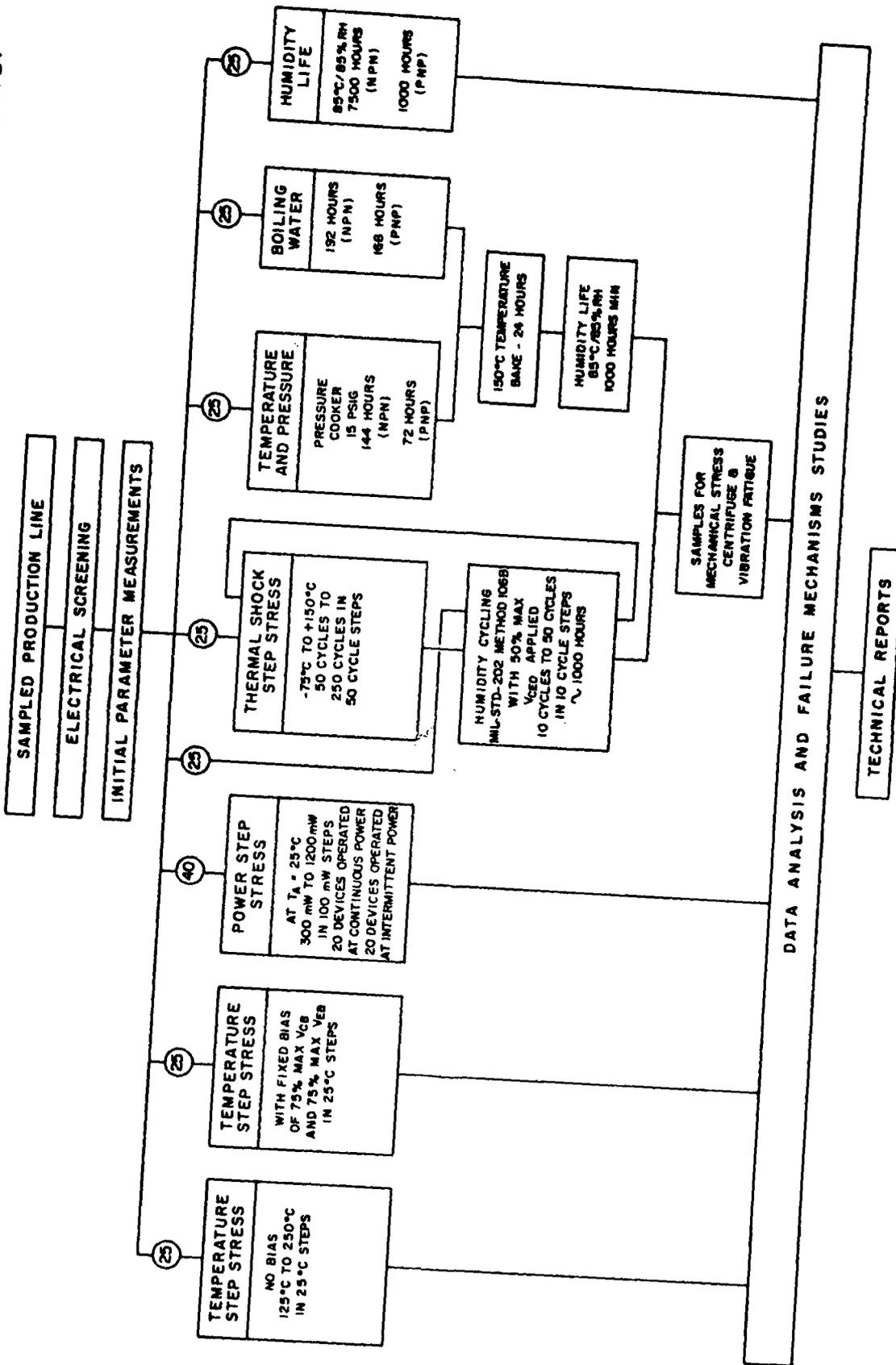


Figure 15 Phase I Test Plan

- Determine any necessary modifications for the Phase II test program.

2. LONG TERM PERFORMANCE CAPABILITY

Phase II of the stress program is outlined in Figure 16. The assigned stress cell numbers and details are shown in Figure 22. The program was designed to establish the overall reliability of plastic encapsulated semiconductors under the variety of accelerated environmental, thermal and operating stresses found in military applications. Random samples of devices for the stress cells were selected from several production lots so that lot to lot performance could be assessed. The Lot Qualification tests shown in the illustration will be discussed in the next two subsections of this section of the report. It should also be noted that the length of the program precluded the running of the Phase II tests for the PNP devices.

The stresses were utilized to assess such things as the effect of the silicon nitride deposition in retarding ion migration resulting in inversion layers at high temperatures; the effect of the glass over oxide and metal interconnections making the chip surface impervious to moisture or other contaminations as well as to reduce pellet handling damage such as scratches and cracked areas. Also, the glassivation was assessed for elimination, or significant reduction of the failure modes of corrosion and surface damage.

Results from the accelerated thermal shock test afforded an evaluation of thermal matching and the capability of materials in the system structure to withstand temperature extremes. To assure that the mechanical integrity of the devices were not affected by the moisture, environmental and operating tests, a randomly selected sample from these tests was subjected to accelerated centrifuge and/or vibration stressing. These tests could detect any possible induced mechanical degradation.

PHASE II LONG TERM PERFORMANCE PRODUCTION CAPABILITY

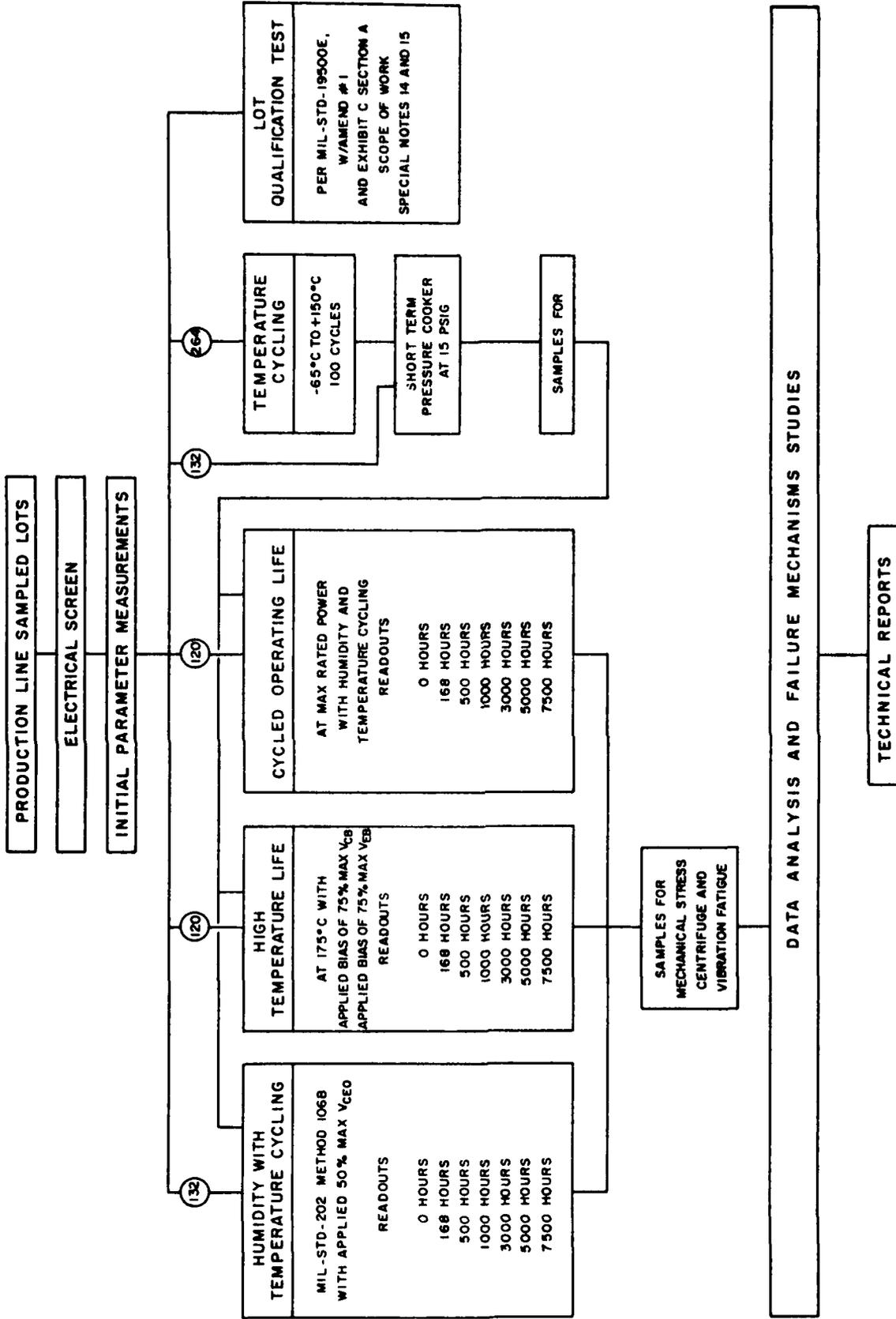


Figure 16 Phase II Test Plan

3. FIRST ARTICLE INSPECTION

The First Article Inspection specifications were generated in accordance with MIL-S-19500 and Special Notes 21, 22 and 23 of the contract and were then approved by USAECOM. The specification for the NPN devices is shown in Figure 17, and the one for the PNP devices in Figure 18. These specifications include Group A, B and C tests and were conducted basically in the manner of device qualification tests. Summaries of the results are included in the next section of the report.

4. LOT ACCEPTANCE

The output of the pilot production line for each of the device types was sampled and lot acceptance tests were conducted on each before shipment of the 2000 sample devices. These tests used the First Article Inspection specifications for the applicable Group A and B tests. The summaries of the results are included in the next section of this report.

(PROPOSED)
 SPECIFICATION, FIRST ARTICLE INSPECTION
 SEMICONDUCTOR DEVICE, TRANSISTOR, PNP, SILICON, SWITCHING

1. SCOPE

- 1.1 Scope. This specification covers the detail requirements for plastic encapsulated silicon, planar, epitaxial, passivated switching transistor.
- 1.2 Physical dimensions. See figure 1.
- 1.3 Maximum ratings.

Type	$P \frac{1}{\text{Free Air}}$ @ 25°C	V_{CBO}	V_{EBO}	V_{CEO}	I_C	T_{stg} and $T_{stg} \text{ w/Rev. Bias}$	T_J
	<u>mW</u>	<u>Vdc</u>	<u>Vdc</u>	<u>Vdc</u>	<u>mAdc</u>	<u>°C</u>	<u>°C</u>
34EXR1853	600	-40	-5	-40	750	-65 to +175	175

1/ Derate 4.0m W/C for $T_A > 25^\circ\text{C}$

Figure 17 NPN Specification (Continued)

1.4 Primary electrical characteristics.

Type	h_{FE} $V_{CE}=10V$ $I_C=10mA$	h_{fe} $V_{CE}=10V$ $I_E=1mA$	$V_{CE(sat)}$ $I_C=150mA$ $I_B=15mA$	C_{cb} $V_{CB}=10V$ $f=1MHz$	t_d	t_r	t_s	t_f	$R_{\theta JA}$
			<u>Vdc</u>	<u>PF</u>	<u>ns</u>	<u>ns</u>	<u>ns</u>	<u>ns</u>	<u>°C/mW</u>
32DXR5318	100 to 300	65 to 450	0.20	10	12	25	350	130	0.25

2. **APPLICABLE DOCUMENTS**

2.1 The following documents, of the issue in effect on date of invitation for bids or request for proposal, form a part of the specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-S-19500-Semiconductor Devices, General Specification for.

STANDARDS

MILITARY

MIL-STD-750 - Test Methods for Semiconductor Devices.

MIL-STD-202 - Test Methods for Electronic and Electrical Component Parts.

3. **REQUIREMENTS**

3.1 General. Requirements shall be in accordance with MIL-S-19500, and as specified herein.

3.2 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-S-19500.

Figure 17 NPN Specification (Continued)

3.3 Design and construction. Transistor shall be of the design, construction, and physical dimensions shown in figure 1.

3.4 Performance characteristics. Performance characteristics shall be as specified in tables I, II, and III.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection shall be in accordance with MIL-S-19500, and as specified herein.

4.2 Quality conformance inspection. Quality conformance inspection shall consist of groups A, B, and C inspections.

4.2.1 Group A inspection. Group A inspection shall consist of the examinations and tests specified in table I.

4.2.2 Group B inspection. Group B inspection shall consist of the examinations and tests specified in table II.

4.2.3 Group C inspection. Group C inspection shall consist of the examinations and tests specified in table III.

4.3 Methods of examination and test. Methods of examination and test shall be as specified in tables I, II and III.

Figure 17 NPN Specification (Continued)

TABLE I. Group A Inspection

Examination or test	MIL-STD-750		L T P D	Symbol	LIMITS		Unit
	Method	Details			Min	Max	
<u>Subgroup 1</u>							
Visual and mechanical examination	2071	See note 1	10	---	---	---	---
<u>Subgroup 2</u>							
Breakdown voltage, collector to emitter	3011	Bias cond.D; $I_C=10mA^*$	5	BV_{CEO}	40	---	Vdc
Breakdown voltage, collector to base	3001	Bias cond.D; $I_C=100\mu A$		BV_{CBO}	40	---	Vdc
Breakdown voltage, emitter to base	3026	Bias cond.D; $I_E=100\mu A$		BV_{EBO}	5	---	Vdc
Collector to base cutoff current	3036	Bias cond.D; $V_{CB}=30V$		I_{CBO}	---	0.01	μA_{dc}
Emitter to base cutoff current	3061	Bias cond.D; $V_{EB}=4V$		I_{EBO}	---	0.01	μA_{dc}

* Pulse Test P.W. \leq 300 μs , Duty Cycle \leq 2%

Figure 17 NPN Specification (Continued)

TABLE I. Group A inspection - (Cont'd)

Examination or Test	MIL-STD-750		L T P D	Symbol	LIMITS		
	Method	Details			Min	Max	Unit
Subgroup 2 - Cont'd							
Forward-current transfer ratio	3076	$V_{CE}=1V^*$ $I_C=10mA$		h_{FE}	100	300	---
		$V_{CE}=2V^*$ $I_C=150mA$			90		
		$V_{CE}=2V^*$ $I_C=300mA$			60		
		$V_{CE}=5V^*$ $I_C=500mA$			40		
Collector to emitter voltage (saturated)	3071	$I_C=150mA^*$ $I_B=15mA$		$V_{CE(sat)}$	---	0.20	Vdc
		$I_C=300mA^*$ $I_B=30mA$				0.25	Vdc
Base emitter voltage (saturated)	3066	Test cond. A $I_C=150mA^*$ $I_B=15mA$		$V_{BE(sat)}$	0.70	0.92	Vdc
		$I_C=300mA^*$ $I_B=30mA$			0.80	1.00	Vdc
Small-signal short-circuit forward-current transfer ratio	3026	$V_{CB}=10V$ $I_E=1mA$ $f=1kHz$		h_{fe}	65	450	---

* Pulse Test P.W. $\leq 300 \mu s$, Duty Cycle $\leq 2\%$

Figure 17 NPN Specification (Continued)

TABLE I. Group A inspection - (Cont'd)

Examination or Test	MIL-STD-750		L T P D	Symbol	LIMITS		
	Method	Details			Min	Max	Unit
<u>Subgroup 3</u>			10				
Emitter-Base Capacitance	3241	Test Method A $V_{EB}=0.5V$ $f=1MHz$ $I_C=0$ 1/16" from seating plane		$C_{eb(dir)}$		50	pF
Collector-Base Capacitance	3241	Test Method A $V_{CB}=10V$ $f=1MHz$ $I_E=0$ 1/16" from seating plane		$C_{cb(dir)}$		10	pF
<u>Subgroup 4</u>			10				
Noise Figure	3246	$V_{CE}=5V$ $I_E=-100\mu A$ $R_g=5k\Omega$ $f=10Hz$ to 10kHz $BW=15.7kHz$		NF		6	dB
Gain-Bandwidth Product	3261	$V_{CE}=10V$ $I_E=-10mA$ $f=30MHz$		f_T	105	335	MHz

* Pulse Test P.W. $\leq 300 \mu s$, Duty Cycle $\leq 2\%$

Figure 17 NPN Specification (Continued)

TABLE I. Group A inspection - (Cont'd)

Examination or Test	MIL-STD-750		L T P D	Symbol	LIMITS		
	Method	Details			Min	Max	Unit
<u>Subgroup 5</u>			15				
Switching delay time	3251	See Figure 2		t_d	---	12	ns
Switching rise time	3251	$I_C=150mA$ $I_{B1}=15mA$		t_r	---	25	ns
Switching storage time	3251	See Figure 3		t_s	---	350	ns
Switching fall time	3251	$I_C=150mA$ $I_{B1}=I_{B2}=15mA$		t_f	---	130	ns

Note 1

VISUAL EXAMINATION

Inspect for the following criteria.

REJECTION CRITERIA

- Holes or voids in the encapsulant greater than 1/32 inch deep or wide
- Chips which touch any lead or the circle formed by the three leads
- Any lead which crosses over or under another
- More than one sharp bend along any lead
- Stain, ink or epoxy encircling a lead or greater than two lead diameters
- Flash on the round part of the body greater than 1/32 inch or any protrusion which causes the device to be larger than the outline drawing dimensions
- Flash down the leads more than 1/16 inch
- Exposure of the internal lead bends which are a part of the device design.

Figure 17 NPN Specification (Continued)

TABLE II. Group B inspection

Examination or Test	MIL-STD-750		L T P D	Symbol	LIMITS		
	Method	Details			Min	Max	Unit
<u>Subgroup 1</u>							
Physical dimensions	2066	See figure 1	10	---	---	---	---
<u>Subgroup 2</u>							
Solderability	2026	Omit aging	10	---	---	---	---
Thermal shock (temperature cycling)	1051	Test cond. Method 107 MIL-STD-202 except -65 to 150°C 10 min.Min. at each Temp. extreme 5 min. Max. at 25°C 50 Cycles		---	---	---	---
End points:							
Collector to base cutoff current	3036	Bias cond. D; V _{CB} =30V		I _{CBO}	---	0.03	μAdc
Emitter to base cutoff current	3061	Bias cond. D; V _{EB} =4V		I _{EBO}	---	0.03	μAdc
Forward-current transfer ratio	3076	I _C =150mA* V _{CE} =2V		h _{FE}	-25	+25	% of initial reading
<u>Subgroup 3</u>							
Terminal strength (lead fatigue) End points (same as Subgroup 2)	2036	Test cond. E	10	---	---	---	---
<u>Subgroup 4</u>							
High-temperature life (nonoperating) (Reference Note 22 in Contract DAAB05-70-C-3109)	1031	T _{stg} =175°C V _{CB} =30V V _{EB} =4V 1000 Hours cool with bias applied	λ= 10	---	---	---	---

* Pulse Test P.W. <300 μs, Duty Cycle ≤ 2%

Figure 17 NPN Specification (Continued)

TABLE II. Group B-inspection (Cont'd)

Examination or test	MIL-STD-750		L T P D	Symbol	LIMITS		
	Method	Details			Min	Max	Unit
<u>Subgroup 4 (Cont'd)</u>							
End points:		Readout within 8 hours after units reach room ambient					
Collector to base cutoff current	3036	Bias condition D; $V_{CB} = 30V$		I_{CBO}	---	30	nA
Emitter to base cutoff current	3061	Bias cond. D; $V_{EB} = 4V$		I_{EBO}	---	30	nA
Forward current transfer ratio	3076	$I_C = 150mA^*$ $V_{CE} = 2V$		h_{FE}	-25	+25	% of initial reading
Collector-emitter saturation voltage	3071	$I_C = 150mA^*$ $I_B = 15mA$		$V_{CE(sat)}$		0.30	V
<u>Subgroup 5</u>							
Steady state operation life	1026	Bias condition $V_{CB} = 20V$ $I_E = 30mA$ 1000 hours	$\lambda =$ 7	---	---	---	---
End points:		(Same as Subgroup 4)					
<u>Subgroup 6</u>							
Moisture resistance (Reference Note 22 in Contract DAAB05-70-C-3109)	1021	Test condition MIL-STD-202 Method 106B omit initial conditioning and Step 7B $V_{CE} = 20V$, 1000 Hrs	$\lambda =$ 10				
End points:		Read within 24 hours.					
		(Same as Subgroup 4)					

*Pulse Test P.W. $\leq 300 \mu s$, Duty Cycle $\leq 2\%$

Figure 17 NPN Specification (Continued)

TABLE III. Group C inspection

Examination or Test	MIL-STD-750		L T P D	Symbol	LIMITS		
	Method	Details			Min	Max	Unit
<u>Subgroup 1</u>							
Salt Atmosphere	1041		15				
End points: (Same as Group B Subgroup 4) plus							
Base-emitter saturation voltage	3066	Test Cond. A $I_C = 150\text{mA}^*$ $I_B = 15\text{mA}$		$V_{BE}(\text{sat})$	1.0		V
<u>Subgroup 2</u>							
Flammability (external flame)		Method 111 MIL-STD-202	20				
End points:		Self-extinguishing within 10 sec.					
<u>Subgroup 3</u>							
Pressure Cooker ** (water)		Pressure 15 psig 24 Hours	20				
End points:							
Collector to base cutoff current	3036	Bias Cond. D; $V_{CB} = 30\text{V}$		I_{CBO}	---	0.10	μA
Emitter to base cutoff current	3061	Bias Cond. D; $V_{EB} = 4\text{V}$		I_{EBO}	---	0.10	μA
Forward-current transfer ratio	3076	$I_C = 150\text{mA}^*$ $V_{CE} = 2\text{V}$		h_{FE}	-25	+25	% of initial reading

*Pulse Test P.W. $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$

Figure 17 NPN Specification (Continued)

TABLE III. Group C inspection (Cont'd)

Examination or Test	MIL-STD-750		L T P D	Symbol	LIMITS		
	Method	Details			Min	Max	Unit
<u>Subgroup 3 (Cont'd)</u>							
Collector-emitter saturation voltage	3071	$I_C=150 \text{ mA}^*$ $I_B=15 \text{ mA}$		$V_{CE}(\text{sat})$		0.30	V
Base-emitter saturation voltage	3066	$I_C=150 \text{ mA}^*$ $I_B=15 \text{ mA}$		$V_{BE}(\text{sat})$		1.0	V
<u>Subgroup 4</u>							
Thermal Shock (Temperature cycling)	1051	Same as Group B Thermal Shock Test except 200 cycles	10				

* Pulse Test P.W. $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$

** Submit devices to steam pressure chamber at 15 psig for 24 hours. Remove devices from chamber and dry off any external moisture at room temperature. Measure the specified electrical parameters within 4 to 8 hours after removal from the steam chamber. The devices shall meet the specified electrical end points.

5. PREPARATION FOR DELIVERY

5.1 Preparation for delivery shall conform to MIL-S-19500.

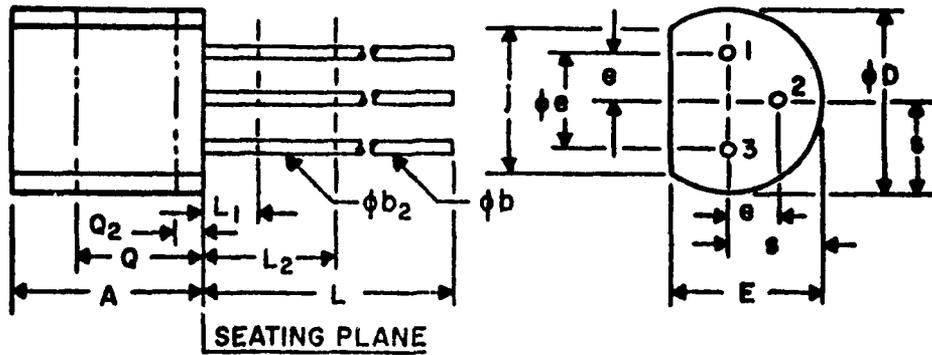
6. NOTES

6.1 Notes. The notes specified in MIL-S-19500 are applicable to this specification.

Figure 17 NPN Specification (Continued)

OUTLINE

Figure



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	.170	.210	4.32	5.33	
φ _b	.016	.021	.407	.533	1, 3
φ _{b2}	.016	.019	.407	.482	3
φ _D	.175	.205	4.45	5.20	2
E	.125	.165	3.18	4.19	2
φ _e	.095	.105	2.42	2.66	
e	.045	.055	1.15	1.39	
J	.135	.170	3.43	4.31	2
L	.500		12.70		1, 3
L ₁		.050		1.27	3
L ₂	.250		6.35		3
Q	.115		2.93		2
Q ₂		.030		.76	2
ϑ	.080	.110	2.04	2.79	

NOTES:

1. THREE LEADS
2. CONTOUR OF PACKAGE UNCONTROLLED OUTSIDE THE ZONE BETWEEN Q₂ AND Q.
3. (THREE LEADS) φ_{b2} APPLIES BETWEEN L₁ AND L₂. φ_b APPLIES BETWEEN L₂ AND .5"(12.70 MM) FROM SEATING PLANE. DIAMETER IS UNCONTROLLED IN L₁ AND BEYOND .5"(12.70 MM) FROM SEATING PLANE.

Figure 17 NPN Specification (Continued)

Figure 2

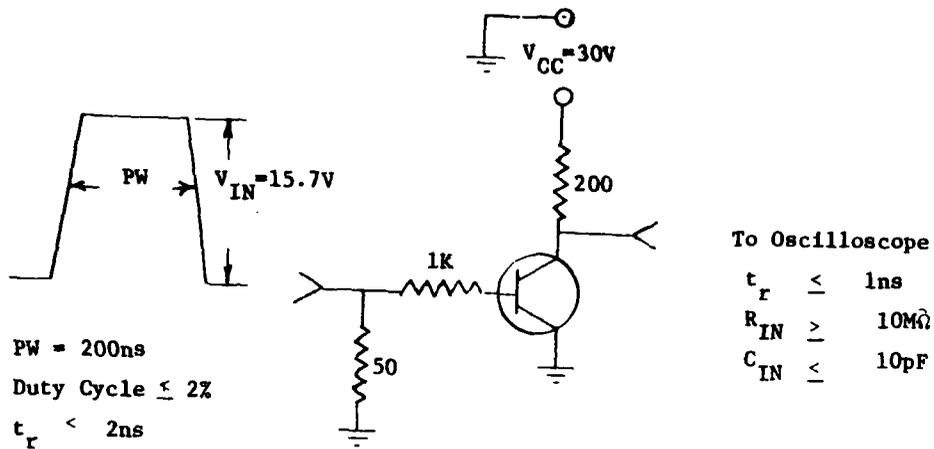


Figure 3

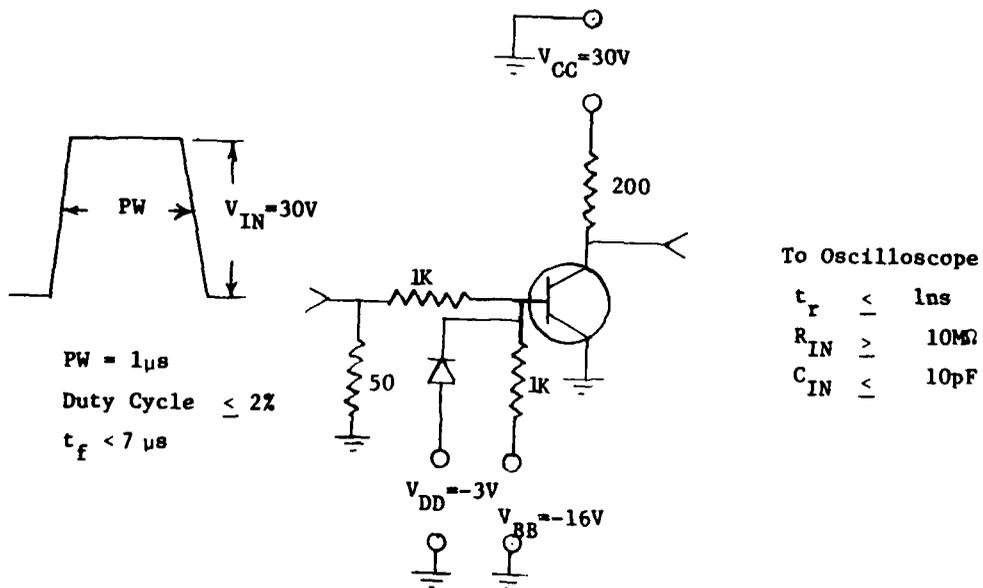


Figure 17 NPN Specification (Concluded)

(PROPOSED)

SPECIFICATION, FIRST ARTICLE INSPECTION
SEMICONDUCTOR DEVICE, TRANSISTOR, NPN, SILICON, SWITCHING

1. SCOPE

1.1 Scope. This specification covers the detail requirements for plastic encapsulated silicon, planar, epitaxial, passivated switching transistor.

1.2 Physical dimensions. See figure 1.

1.3 Maximum ratings.

Type	P <u>1/</u> Free Air @ 25°C mW	V _{CBO} Vdc	V _{EBO} Vdc	V _{CEO} Vdc	I _C mAdc	T _{stg} and T _{stg} w/Rev.Bias °C	T _J °C
32DXR5318	600	40	5	40	800	-65 to 175	175

1/ Derate 4.0 mW/C for T_A > 25°C

Figure 18 PNP Specification (Continued)

1.4 Primary electrical characteristics,

Type	h_{FE} $V_{CE} = -10V$ $I_C = -10mA$	h_{fe} $V_{CE} = -10V$ $I_E = 1mA$	$V_{CE(sat)}$ $I_C = -150mA$ $I_B = -15mA$	C_{cb} $V_{CB} = -10V$ $f = 1MHz$	t_d	t_r	t_s	t_f	$R_{\theta JA}$
34EXR1853	100 to 300	90 to 450	<u>Vdc</u> 0.40	<u>pF</u> 15	<u>ns</u> 10	<u>ns</u> 35	<u>ns</u> 375	<u>ns</u> 130	<u>°C/mW</u> 0.25

2. **APPLICABLE DOCUMENTS**

2.1 The following documents, of the issue in effect on date of invitation for bids or request for proposal, form a part of the specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-S-19500-Semiconductor Devices, General Specification for.

STANDARDS

MILITARY

MIL-STD-750 - Test Methods for Semiconductor Devices.

MIL-STD-202 - Test Methods for Electronic and Electrical Component Parts.

3. **REQUIREMENTS**

3.1 General. Requirements shall be in accordance with MIL-S-19500, and as specified herein.

3.2 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-S-19500.

Figure 18 PNP Specification (Continued)

3.3 Design and construction. Transistor shall be of the design, construction and physical dimensions shown in figure 1.

3.4 Performance characteristics. Performance characteristics shall be as specified in tables I, II, and III.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection shall be in accordance with MIL-S-19500, and as specified herein.

4.2 Quality conformance inspection. Quality conformance inspection shall consist of groups A, B, and C inspections.

4.2.1 Group A inspection. Group A inspection shall consist of the examinations and tests specified in table I.

4.2.2 Group B inspection. Group B inspection shall consist of the examinations and tests specified in table II.

4.2.3 Group C inspection. Group C inspection shall consist of the examinations and tests specified in table III.

4.3 Methods of examination and test. Methods of examination and test shall be as specified in tables I, II and III.

Figure 18 PNP Specification (Continued)

TABLE I. Group A Inspection

Examination or test	MIL-STD-750		L T P D	Symbol	LIMITS		
	Method	Details			Min	Max	Unit
<u>Subgroup 1</u>							
Visual and mechanical examination	2071	See note 1	10	---	---	---	---
<u>Subgroup 2</u>							
Breakdown voltage, collector to emitter	3011	Bias cond.D; $I_C = -10\text{mA}^*$	5	BV_{CEO}	-40	---	Vdc
Breakdown voltage, collector to base	3001	Bias cond.D; $I_C = -100\mu\text{A}$		BV_{CBO}	-40	---	Vdc
Breakdown voltage, emitter to base	3026	Bias cond.D; $I_E = -100\mu\text{A}$		BV_{EBO}	-5	---	Vdc
Collector to base cutoff current	3036	Bias cond.D; $V_{CB} = -30\text{V}$		I_{CBO}	---	0.01	μAdc
Emitter to base cutoff current	3061	Bias cond.D; $V_{EB} = -4\text{V}$		I_{EBO}	---	0.01	μAdc

* Pulse Test P.W. $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$

Figure 18 PNP Specification (Continued)

TABLE I. Group A Inspection (Cont'd)

Examination or test	MIL-STD-750		L T P D	Symbol	LIMITS						
	Method	Details			Min	Max	Unit				
Subgroup 2 - Cont'd											
Forward-current transfer ratio	3076	$V_{CE} = -1V^*$		h_{FE}	100	300	---				
		$I_C = -10mA$									
		$V_{CE} = -2V^*$									
		$I_C = -150mA$									
Collector to emitter voltage (saturated)	3071	$V_{CE} = -3V^*$		$V_{CE(sat)}$	---	-0.50	Vdc				
		$I_C = -300mA$									
		$V_{CE} = -5V^*$						50	---	-0.60	Vdc
		$I_C = -500mA$									
Base emitter voltage (saturated)	3066	$I_C = -150mA^*$		$V_{BE(sat)}$	-0.60	-0.90	Vdc				
		$I_B = -15mA$									
		Test cond. A									
Small-signal short circuit forward-current transfer ratio	3026	$V_{CB} = -10V$		h_{fe}	90	450	---				
		$I_E = -1mA$									
		$f = 1kHz$									

* Pulse Test P.W. $\leq 300 \mu s$. Duty Cycle $\leq 2\%$

Figure 18 PNP Specification (Continued)

TABLE I. Group A Inspection (Cont'd)

Examination or test	MIL-STD-750		L T P D	Symbol	LIMITS		
	Method	Details			Min	Max	Unit
<u>Subgroup 3</u>			10				
Emitter-Base Capacitance	3241	Test Method A $V_{EB} = -0.5V$ $f = 1MHz$ $I_C = 0$ 1/16" from seating plane		$C_{eb(dir)}$		45	pF
Collector-Base Capacitance	3241	Test Method A $V_{CB} = -10V$ $f = 1MHz$ $I_E = 0$ 1/16" from seating plane		$C_{cb(dir)}$		15	pF
<u>Subgroup 4</u>			10				
Noise Figure	3246	$V_{CE} = -5V$ $I_E = -100\mu A$ $R_s = 5k\Omega$ $f = 10Hz$ to 10kHz BW=15.7kHz		NF		6	dB
Gain-Bandwidth Product	3261	$V_{CE} = -10V$ $I_E = -10mA$ $f = 30MHz$		f_T	75	250	MHz

* Pulse Test P.W. $\leq 300 \mu s$, Duty Cycle $\leq 2\%$

Figure 18 PNP Specification (Continued)

TABLE I. Group Inspection (Cont'd)

Examination or Test	MIL-STD-750		L T P D	Symbol	LIMITS		
	Method	Details			Min	Max	Unit
<u>Subgroup 5</u>			15				
Switching delay time	3251	See Figure 2		t_d	---	10	ns
Switching rise time	3251	$I_C = -150\text{mA}$ $I_{B1} = -15\text{mA}$		t_r	---	35	ns
Switching storage time	3251	See Figure 3		t_s	---	375	ns
Switching fall time	3251	$I_C = -150\text{mA}$ $I_{B1} = -I_{B2} = -15\text{mA}$		t_f	---	130	ns

Note 1

VISUAL EXAMINATION

Inspect for the following criteria.

REJECTION CRITERIA

- Holes or voids in the encapsulant greater than 1/32 inch deep or wide
- Chips which touch any lead or the circle formed by the three leads
- Any lead which crosses over or under another
- More than one sharp bend along any lead
- Stain, ink or epoxy encircling a lead or greater than two lead diameters
- Flash on the round part of the body greater than 1/32 inch or any protrusion which causes the device to be larger than the outline drawing dimensions
- Flash down the leads more than 1/16 inch
- Exposure of the internal lead bends which are a part of the device design.

Figure 18 PNP Specification (Continued)

TABLE II. Group B Inspection

Examination or Test	MIL-STD-750		L T P D	Symbol	LIMITS		
	Method	Details			Min	Max	Unit
<u>Subgroup 1</u>							
Physical dimensions	2066	See figure 1	10	---	---	---	---
<u>Subgroup 2</u>							
Solderability	2026	Omit aging	10	---	---	---	---
Thermal shock (temperature cycling)	1051	Test cond. Method 107 MIL-STD-202 except -65 to 150°C 10 min. Min. at each Temp.extreme 5 min. Max at 25°C 50 Cycles		---	---	---	---
End points:							
Collector to base cutoff current	3036	Bias cond. D; $V_{CB} = -30V$		I_{CBO}	---	-0.03	μA_{dc}
Emitter to base cutoff current	3061	Bias cond. D; $V_{EB} = -4V$		I_{EBO}	---	-0.03	μA_{dc}
Forward-current transfer ratio	3076	$I_C = -150 \text{ mA}^*$ $V_{CE} = -2V$		h_{FE}	-25	+25	% of initial reading
<u>Subgroup 3</u>							
Terminal strength (lead fatigue) End points (same as subgroup 2)	2036	Test cond. E	10	---	---	---	---
<u>Subgroup 4</u>							
High-temperature life (nonoperating) (Reference Note 22 in Contract DAAB05-70-C-3109)	1031	$T_{stg} = 175^\circ C$ $V_{CB} = -30V$ $V_{EB} = -4V$ 1000 Hours cool with bias applied	$\lambda =$ 10	---	---	---	---

* Pulse Test P.W. $\leq 300 \mu s$, Duty Cycle $\leq 2\%$

Figure 18 PNP Specification (Continued)

TABLE II. Group B Inspection (Cont'd)

Examination or test	MIL-STD-750		L T P D	Symbol	LIMITS		
	Method	Details			Min	Max	Unit
Subgroup 4 (Cont'd)							
End points:		Readout within 8 hours after units reach room ambient					
Collector to base cutoff current	3036	Bias condition D; $V_{CB} = -30V$		I_{CBO}	---	30	nA
Emitter to base cutoff current	3061	Bias cond. D; $V_{EB} = -4V$		I_{EBO}	---	30	nA
Forward current transfer ratio	3076	$I_C = -150mA^*$ $V_{CE} = -2V$		h_{FE}	-25	+25	% of initial reading
Collector-emitter saturation voltage	3071	$I_C = -150mA^*$ $I_B = -15mA$		$V_{CE(sat)}$		-0.50	V
Subgroup 5							
Steady state operation life	1026	Bias condition $V_{CB} = -20V$ $I_E = -30mA$ 1000 hours	$\lambda =$ 7	---	---	---	---
End points: (same as Subgroup 4)							
Subgroup 6							
Moisture resistance (Reference Note 22 in Contract DAAB05-70-C-3109)	1021	Test condition MIL-STD-202 Method 106B omit initial conditioning and Step 7E $V_{CE} = -20V$, 1000 Hrs.	$\lambda =$ 10				
End points: (Same as Subgroup 4)		Read within 24 hours.					

* Pulse Test P.W. < 300 μs , Duty Cycle $\leq 2\%$

Figure 18 PNP Specification (Continued)

TABLE III. Group C Inspection

Examination or Test	MIL-STD-750		L T P D	Symbol	LIMITS		
	Method	Details			Min	Max	Unit
<u>Subgroup 1</u>							
Salt Atmosphere	1041		15				
End Points: (Same as Group B Subgroup 4) plus							
Base-emitter saturation voltage	3066	Test Cond. A $I_C = -150$ $I_B = -15mA$		$V_{BE(sat)}$		-1.0	v
<u>Subgroup 2</u>							
Flammability (external flame)		Method 111 MIL-STD-202	20				
End points:		Self-extinguishing within 10 sec.					
<u>Subgroup 3</u>							
Pressure Cooker** (water)		Pressure 15 psig 24 Hours	20				
End points:							
Collector to base cutoff current	3036	Bias Cond. D; $V_{CB} = -30V$		I_{CBO}	---	-0.10	μA
Emitter to base cutoff current	3061	Bias Cond. D; $V_{EB} = -4 V$		I_{EBO}	---	-0.10	μA
Forward-current transfer ratio	3076	$I_C = -150mA^*$ $V_{CE} = -2V$		h_{FE}	-25	+25	% of initial

* Pulse Test P.W. $\leq 300 \mu s$, Duty Cycle $\leq 2\%$

Figure 18 PNP Specification (Continued)

TABLE III. Group C Inspection (Cont'd)

Examination or Test	MIL-STD-750		L T P D	Symbol	LIMITS		
	Method	Details			Min	Max	Unit
<u>Subgroup 3</u> (Cont'd)							
Collector-emitter saturation voltage	3071	$I_C = -150\text{mA}^*$ $I_B = -15\text{mA}$		$V_{CE(\text{sat})}$		-0.50	V
Base-emitter saturation voltage	3066	$I_C = -150\text{mA}^*$ $I_B = -15\text{mA}$		$V_{BE(\text{sat})}$		-1.0	V
<u>Subgroup 4</u>							
Thermal Shock (Temperature cycling)	1051	Same as Group B Thermal Shock Test except 200 cycles	10				

* Pulse Test P.W. $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$

** Submit devices to steam pressure chamber at 15 psig for 24 hours. Remove devices from chamber and dry off any external moisture at room temperature. Measure the specified electrical parameters within 4 to 8 hours after removal from the steam chamber. The devices shall meet the specified electrical end points.

5. PREPARATION FOR DELIVERY

5.1 Preparation for delivery shall conform to MIL-S-19500.

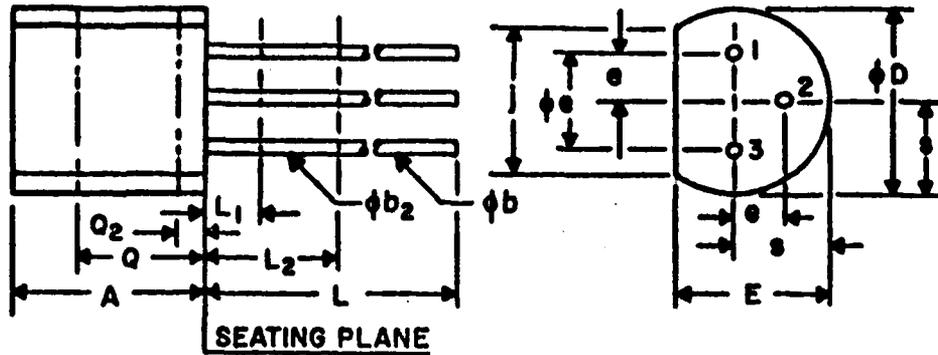
6. NOTES

6.1 Notes. The notes specified in MIL-S-19500 are applicable to this specification.

Figure 18 PNP Specification (Continued)

OUTLINE

Figure 1



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	.170	.210	4.32	5.33	
ϕ_b	.016	.021	.407	.533	1, 3
ϕ_{b_2}	.016	.019	.407	.482	3
ϕ_D	.175	.205	4.45	5.20	2
E	.125	.165	3.18	4.19	2
ϕ_e	.095	.105	2.42	2.66	
e	.045	.055	1.15	1.39	
J	.135	.170	3.43	4.31	2
L	.500		12.70		1, 3
L_1		.050		1.27	3
L_2	.250		6.35		3
Q	.115		2.93		2
Q_2		.030		.76	2
S	.080	.110	2.04	2.79	

NOTES:

1. THREE LEADS
2. CONTOUR OF PACKAGE UNCONTROLLED OUTSIDE THE ZONE BETWEEN Q_2 AND Q.
3. (THREE LEADS) ϕ_{b_2} APPLIES BETWEEN L_1 AND L_2 . ϕ_b APPLIES BETWEEN L_2 AND .5" (12.70 MM) FROM SEATING PLANE. DIAMETER IS UNCONTROLLED IN L_1 AND BEYOND .5" (12.70 MM) FROM SEATING PLANE.

Figure 18 PNP Specification (Continued)

Figure 2

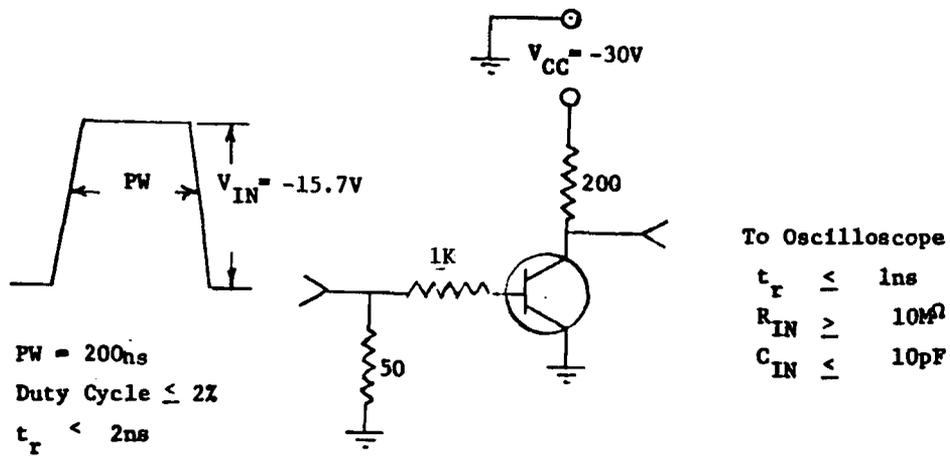


Figure 3

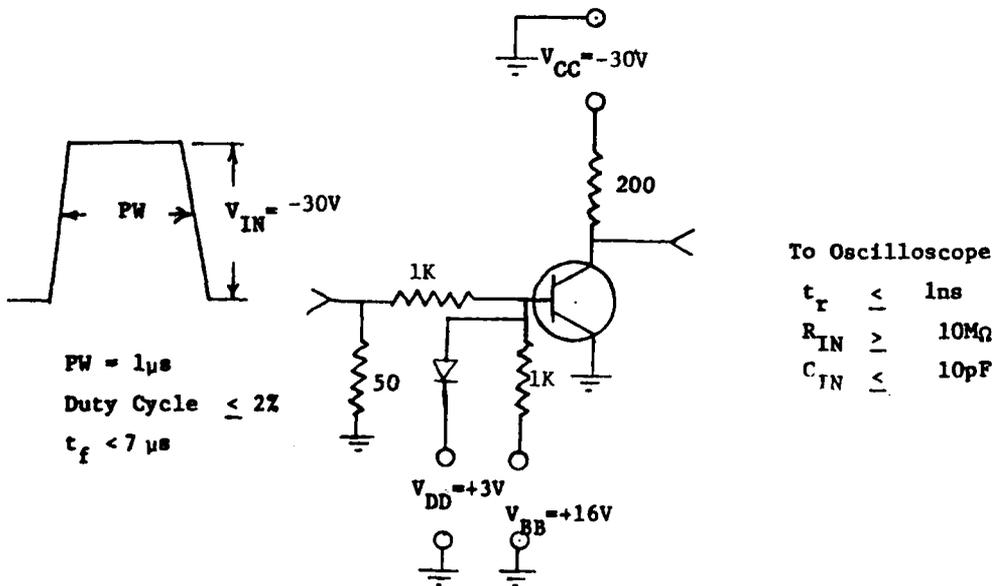


Figure 18 PNP Specification (Concluded)

SECTION V

RESULTS FROM THE EVALUATION PROGRAM

1. GENERAL

This section contains the results of a comprehensive evaluation test program, based on sound statistical and engineering design principles which have demonstrated with confidence the reliability performance of solid encapsulated transistors under accelerated stress conditions. The program results provide performance data for plastic devices which can be utilized for setting uniform standards and military lot qualification procedures.

The emphasis of the stress program has been on ascertaining the resistance capability of both NPN and PNP plastic encapsulated sealed chip structures to moisture environments under electrical bias and temperature cycling conditions. These devices were evaluated using temperature and power step-stressing, as well as combination and sequential stressing such as thermal shock and humidity cycling tests. Steam pressure, boiling water and extended temperature-humidity life tests with bias were also performed. Extended stress-in-time tests for an accumulated 7,500 hours were also conducted for replicate production lots. The stress-in-time tests were performed under conditions of temperature-humidity cycling, with bias and with operating power. In addition, a high temperature stress with simultaneously applied reverse bias to the collector base and emitter base junctions were performed. The new structures, along with proper control units derived from the same replicated production lots, were subjected to the different stress cells in a random and balanced manner to assure statistically valid and reproducible results.

2. PROGRAM DESIGN

The Phase I comprehensive stress program, the Phase II long term stress-in-time tests and the supplementary stressing and evaluation tests are delineated in Figure 19 through 23. This program represented an investment of over 8 million unit hours of stressing; with 62% of this delegated to the contract structure evaluation and the remaining portion of the control units.

The Phase I comprehensive step-stress and special test program conducted for representative NPN and PNP production samples allowed a thorough response evaluation of the stress space. Results from these stresses established the threshold levels and ultimate capabilities of the plastic structures, provided estimates for the acceleration of response of the stress with stress level, allowed a valid and rapid comparison of contract and control device performance and provided needed information concerning effective stress screening and critical parameter response.

The long term, Phase II test program results established the overall reliability of the plastic packaged transistors under a variety of accelerated environmental, thermal and operating stresses, simultaneously applied. Devices assigned here were sampled from several production lots so that the repeatability and uniformity of performance could be demonstrated. Such continual lot-to-lot demonstration of homogeneity in stress results is indicative of a controlled process. The electrical parameters monitored before and after test were those most sensitive to the effects of moisture, surface contamination, intermittency and resistance change in the lead bond-metalization system.

To assure that the mechanical integrity of the solid encapsulated devices was not affected by accelerated moisture, environmental and operating stress under long time exposures, random samples, upon completion of such stressing, were subjected to drop shock, centrifuge and vibration fatigue.

In addition, and as a part of the Phase II testing, military lot qualification type tests (to MIL-S-19500) were performed on both the NPN and PNP devices.

3. TEST RESULTS

In the discussion of the test results, the program vehicles, consisting of a completely sealed chip structure with silicon dioxide and silicon nitride barrier, refractory metalization and glass seal are referred to as the contract devices. Units derived from the standard planar passivated chip process are referred to as the control devices. Both chip types were assembled and encapsulated in a solid monoplactic epoxy package.

The stability performance for the contract structures was significantly superior to the control devices after the Phase I accelerated temperature and power step-stressing. Refer to Figure 19 for the deliniation of these stress cells. Shown in Figures 24 and 25 are the dc current gain stability contrasts between the contract and control devices for NPN and PNP, respectively, after temperature step-stress with bias. The improved stability of the contract structure is strongly evident above the 150°C temperature stress level. At the lower stress levels, both structures exhibited excellent stability.

Contained in Figures 26 and 27 are examples of the computer output of multi-parameter statistical summaries contrasting contract and control device stability. These were obtained after each scheduled readout. Shown in these figures are the results for the NPN and PNP, respectively after the 200°C temperature step with applied bias. The information presented includes percentiles of the electrical parameter change from initial conditions as well as the failure counts. Thus for example, in the NPN summary in Figure 26, it can be seen that there was a median low current (I_B at 0.1 mA) change in dc gain of 5% for the contract samples compared to a -95% downward shift for the control device samples.

Figures 28 and 29 are used to show the dc current gain stability contrasts between contract and control devices for NPN and PNP, respectively, after each step of the power step-stressing. Again, superior gain stability is noted for the contract devices. Figures 30 and 31 contain examples of the computerized multi-parameter statistical summaries after power step-stressing for NPN and PNP devices, respectively. Thus, contained in Figure 30 are NPN stability contrasts between contract and control samples after the 1 watt power step reflecting the striking superiority achieved with the contract structures. Similarly, Figure 31 contains the PNP contrasts after the 800 mW step of the power step-stress. Below these levels, both contract and control devices exhibited excellent parameter stability. Shown in Figure 32 are the cumulative failure count summaries contrasting the contract with the control samples for the temperature step-stress and power step-stress cells of Phase I. At the 250°C temperature step and 1200 mW power step, instability in the dc gain was evident in both structures. However, the superiority of the contract structures was still clearly evident from other monitored electrical parameter indicators such as collector and base saturation voltage, $V_{CE(sat)}$ and $V_{BE(sat)}$. The computerized stability summaries for the NPN samples after the final steps of power step-stress (1200 mW) and temperature step-stress (250°C) with bias are shown in Figures 33 and 34, respectively. For the power step results, the saturation voltages are stable for the contract devices while the control units show hundreds of percent shift upward. For the temperature with bias results, the collector saturation voltage change for the contract device ranges $\pm 4\%$ compared to a range from +7 to +123% for the control samples.

The results after 7500 cumulative hours of Phase II long term performance under environmental, thermal and electrical stressing continued to indicate the superior reliability achieved with the contract devices. The three long term test conditions of the NPN Phase II Program and the pre-condition stress cells are identified and described in Figure 22.

Significantly superior parameter stability was obtained for the contract units on temperature-humidity cycling with operating power and temperature with applied bias stresses. Plotted in Figures 35 and 36 are the cumulative distributions of large current h_{FE} percent change, contrasting the contract and control structures for these stress cells. These are plotted for the three replicate production lots combined and the superiority of the contract structure stability is clearly evident. No statistically significant difference in performance between the contract and control devices was obtained after 7500 hours of temperature humidity cycling with bias, where both device types exhibited excellent parameter stability. Reflecting these results are the cumulative failure summaries contained in Figures 37 through 39, where each of the three stress-in-time stress cells are summarized. The failure criteria shown are consistent with those found in the First Article Inspection Specification. The failure criteria used for the computerized electrical parameter stability summaries include additional definitions of failure. Significantly fewer failures were obtained for the contract structures on the temperature-humidity cycling with power and on the temperature with reverse bias stress, which reinforce the Phase I results mentioned previously. The detailed computer output summaries of the 7500 hour results for each of these stress cells, for each replicate production lot, are shown in Figures 40 to 48. These are summarized by comparing the contract and control sample performance for each diffusion lot source demonstrating the lot-to-lot homogeneity in response to stress.

In accordance with the Phase II program plan, samples derived from the same replicate lots were preconditioned prior to the long term stressing described above. This preconditioning consisted of 100 cycles of temperature cycling from -65°C to 150°C and/or 107 hours of pressure cooker stress at 15 psig followed with a 150°C recovery bake. The pre-stress screening with pressure cooker proved to be too harsh for both an efficient and effective 100% screen. For those samples having the pressure cooker stress screening, significantly greater degradation for both device types was obtained after the subsequent stressing of temperature-humidity cycling with operating power and temperature with reverse bias, compared to the non-preconditioned devices.

4. SUMMARY OF RESULTS

A summary of the highlights of the test results includes:

- Contract NPN structures have repeatedly demonstrated a significant increase in device capability at high operating temperatures (175°C to 225°C) and high power dissipation levels,
- Similar results have been demonstrated with PNP structures,
- Superior long term performance of the contract over the control devices has been demonstrated under operating environmental stressing,
- Both control and contract units have demonstrated excellent device capability to withstand accelerated temperature-humidity-vapor pressure stressing, but the contract devices show a consistent trend toward decreased leakage degradation and increased chip resistance under accelerated vapor pressure conditions demonstrating superior package-device passivation,
- A short term pressure cooker stress screen would not be recommended on a 100% but only on a lot sample basis for evaluation of lot capability.

PHASE I - COMPREHENSIVE STEP-STRESS AND SPECIAL TEST
NPN AND PNP/CONTRACT AND CONTROL STRUCTURES
25 PER STRESS PER TYPE

I ACCELERATED ELECTRICAL-THERMAL STRESSING

A. TEMPERATURE STEP-STRESS, 150°C TO 250°C (IN 25°C STEPS)
72 HOURS PER STEP

1. WITHOUT BIAS
2. WITH BIAS, $V_{CB} = 30V$, $V_{EB} = 4V$

B. POWER STEP-STRESS, 500mW TO 800mW (IN 100mW STEPS)
EXTENDED TO 1200mW

1. CONTINUOUS OPERATING LIFE
2. INTERMITTENT LIFE 50 MINUTES ON/ 10 MINUTES OFF

Figure 19 Phase I Accelerated Electrical - Thermal Stresses

PHASE I - COMPREHENSIVE STEP-STRESS AND SPECIAL TEST
NPN AND PNP/CONTRACT AND CONTROL STRUCTURES
25 PER STRESS PER TYPE

II ACCELERATED ENVIRONMENTAL STRESSING

- A. TEMPERATURE CYCLING, -65°C TO 150°C , AIR-TO-AIR
EXTENDED TO 400 CYCLES
- B. 1.THERMAL SHOCK, -75°C TO 150°C , 250 CYCLES,
LIQUID-TO-LIQUID, RAPID TRANSFER
FOLLOWED WITH TEMPERATURE-HUMIDITY CYCLING,
 2°C TO 65°C , WITH BIAS OF V_{CEO} OF 20V,
50 CYCLES (1200 HOURS)
2.SAME STRESSING AS ABOVE WITH THE SEQUENCE REVERSED
- C. HUMIDITY LIFE, $85^{\circ}\text{C}/85\%$ RH
7500 ACCUMULATED HOURS (NPN)
1000 ACCUMULATED HOURS (PNP)
- D. 1.PRESSURE COOKER, 15 PSIG (121°C) 72 TO 144 HOURS
2.BOILING WATER, 168 TO 200 HOURS
3.THE DEVICES FROM THE ABOVE STRESSES SUBMITTED TO
24 HOURS OF 150°C RECOVERY BAKE AND SUBJECTED TO
1000 HOURS OF HUMIDITY LIFE, $85^{\circ}\text{C}/85\%$ RH.

Figure 20 Phase I Accelerated Environmental Stresses

PHASE I - COMPREHENSIVE STEP-STRESSES AND SPECIAL TEST
NPN AND PNP/CONTRACT AND CONTROL STRUCTURES
25 PER STRESS PER TYPE

III MECHANICAL

RANDOM SAMPLES FROM II B, C, D
SUBJECTED TO 1500G DROP SHOCK (Z_2 PLANE, 5 DROPS)
20G VIBRATION (Z_2 PLANE, 32 HOURS)
20KG CENTRIFUGE (Z_2 PLANE, 1 MINUTE)

Figure 21 Phase I Mechanical Stresses

PHASE II - LONG TERM (7500 HOURS)
THERMAL-ELECTRICAL-ENVIRONMENTAL STRESSES-IN-TIME
REPRESENTING THREE PRODUCTION LOTS

STRESS CELL 1:

TEMPERATURE-HUMIDITY CYCLING, 25°C TO 65°C
WITH APPLIED BIAS OF V_{CE0} OF 20V
132 CONTRACT
68 CONTROL SAMPLE SIZE

STRESS CELL 2:

TEMPERATURE STRESS WITH APPLIED BIAS OF $V_{CB} = 30V$
 $V_{EB} = 4V$ at 175°C
120 CONTRACT
60 CONTROL SAMPLE SIZE

STRESS CELL 3:

TEMPERATURE-HUMIDITY CYCLING, 25°C TO 65°C
WITH OPERATING POWER OF 360mW
($V_{CB} = 20V$)
120 CONTRACT
60 CONTROL SAMPLE SIZE

PRE-CONDITION SAMPLES DERIVED FROM THE SAME SOURCE LOTS WERE ALSO
SUBJECTED TO THE ABOVE STRESSES. PRE-CONDITIONED STRESS CELLS INCLUDE

STRESS CELL 4: 100 CYCLES OF TEMPERATURE CYCLING (-65°C TO 100°C,
AIR-TO-AIR) FOLLOWED WITH 107 HOURS OF PRESSURE COOKER
STRESS AT 15 PSIG.

264 CONTRACT
136 CONTROL SAMPLE SIZE

STRESS CELL 5: 107 HOURS OF PRESSURE COOKER STRESS AT 15 PSIG.

132 CONTRACT
68 CONTROL SAMPLE SIZE

Figure 22 Phase II Long Term Stresses

ADDITIONAL TESTING AND EVALUATION

- A. LONG TERM (5000 HOURS) HUMIDITY LIFE, 85°C/85% RH,
WITH BIAS (NPN CONTRACT AND CONTROL STRUCTURES)

- B. SUPERHEATED STEAM PRESSURE TEST (DRY STEAM) AT
35 PSIG APPLIED FOR 312 HOURS (NPN CONTRACT AND
CONTROL STRUCTURES)

- C. SUBJECTION TO 572 HOURS OF SALT ATMOSPHERE
(NPN CONTRACT AND CONTROL STRUCTURES)

Figure 23 Additional Stresses

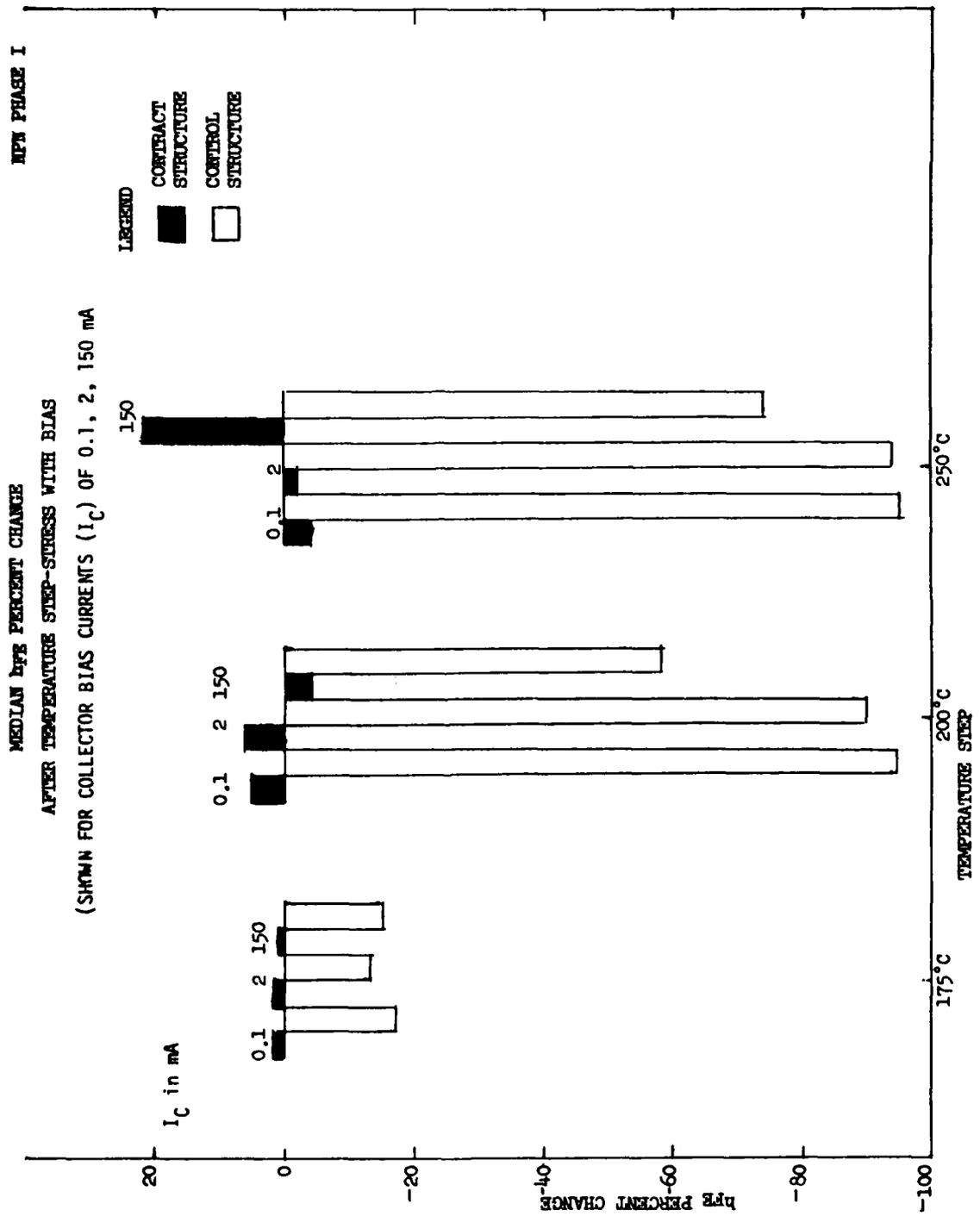


Figure 24 NPN h_{FE} Percent Change After Temperature Step-Stress With Bias

PNP PHASE I

MEDIAN h_{FE} PERCENT CHANGE
 AFTER TEMPERATURE STEP-STRESS WITH BIAS
 (SHOWN FOR COLLECTOR BIAS CURRENTS (I_C) OF 0.1, 2, 150 mA)

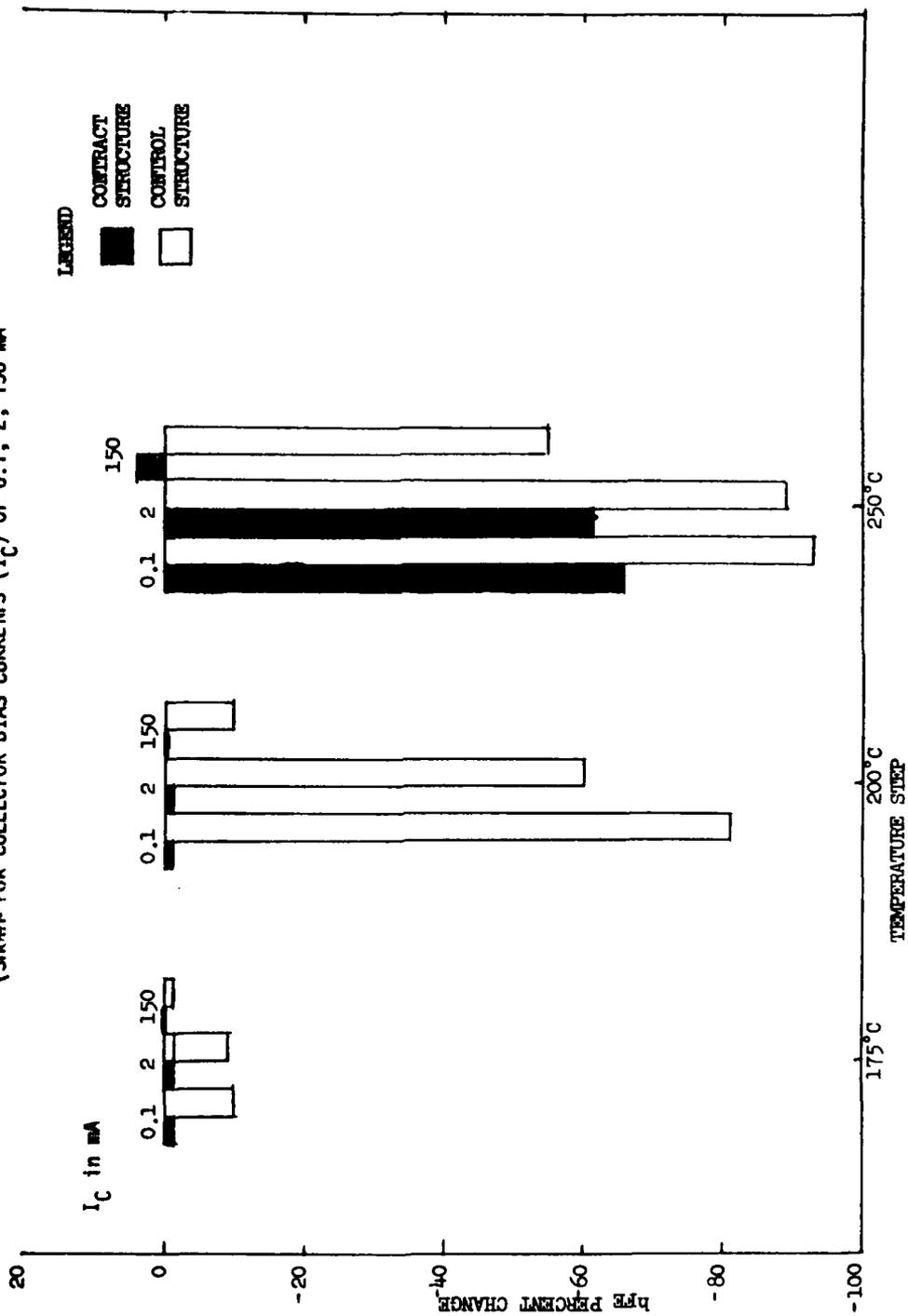


Figure 25 PNP h_{FE} Percent Change After Temperature Step-Stress With Bias

COMPUTERIZED STABILITY SUMMARY STATISTICS

NPN
LOT 1014

AFTER THIRD STEP (200°C) OF TEMPERATURE STEP-STRESS WITH APPLIED BIAS
of $V_{CB} = 30$ V, $V_{EB} = 4$ V (72 hours per step)

DEFINITION OF PARAMETERS

- PAR 1 Arithmetic Change of ICBO @ 30 V in nA
- PAR 2 " " of IEBO @ 4 V in nA
- PAR 3 Percent Change (values shown x 100) of hFE @ .1 mA, 2 V
- PAR 4 " " " of hFE @ 2 mA, 2 V
- PAR 5 " " " of hFE @ 150 mA, 2 V
- PAR 6 " " " of VCE(SAT) @ 150 mA, 15 mA
- PAR 7 Arithmetic Change of VBE(SAT) @ 150 mA, 15 mA in V

FAILURE DEFINITIONS: ICBO and IEBO in excess of 100 nA
hFE values exceeding $\pm 30\%$
VCE(SAT) exceeding $\pm 25\%$
VBE(SAT) exceeding change of ± 0.1 V

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER LOT SAMPLE 25

TOTAL NO. FAILURES 2

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	-0.38	-0.298	-0.14225	-0.1035	-0.0205	0.1995	25499.9
2	-10.262	-6.0185	-4.1885	-2.7455	-2.09525	-1.0305	1044.7
3	-0.84	-0.3975	0.0325	0.052	0.05875	0.0695	0.079
4	-0.752	-0.306	0.044	0.0575	0.063	0.0685	0.083
5	-0.117	-0.09	-0.074	-0.0415	-0.02675	0.018	0.034
6	-0.048	-0.0395	-0.03475	-0.0275	-0.02125	-0.0115	-0.01
7	-0.008	-0.007	-0.006	-0.0055	-0.004	-0.002	-0.001

CONTROL GROUP WITHOUT GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER LOT SAMPLE 25

TOTAL NO. FAILURES 25

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	-0.034	0.214	1.13775	2.616	4.27475	31.93	508.768
2	-0.376	-0.34	-0.1535	0.3485	1.7575	6.627	40.938
3	-0.955	-0.954	-0.9505	-0.946	-0.9385	-0.9345	-0.922
4	-0.944	-0.937	-0.92675	-0.8995	-0.86125	-0.824	-0.804
5	-0.671	-0.6495	-0.6135	-0.577	-0.51875	-0.4695	-0.321
6	-0.999	-0.0215	-0.00975	0	0.013	0.014	0.028
7	-0.006	-0.0055	-0.005	-0.004	-0.00325	-0.002	-0.001

Figure 26 NPN Summary Statistics After 200°C Temperature Step-Stress With Bias

COMPUTERIZED STABILITY SUMMARY STATISTICS

LOT 7010
Phase I-PNP

AFTER 200°C OF TEMPERATURE STEP-STRESS WITH APPLIED BIAS
of VCB = 30V, VEB = 4V (72 hours per step)

DEFINITION OF PARAMETERS

- PAR 1 Arithmetic Change of ICBO @ 30 V in nA
- PAR 2 " " of IEBO @ 4 V in nA
- PAR 3 Percent Change (values shown x 100) of hFE @ .1 mA, 2 V
- PAR 4 " " " of hFE @ 2 mA, 2 V
- PAR 5 " " " of hFE @ 150 mA, 2 V
- PAR 6 " " " of VCE(SAT) @ 150 mA, 15 mA
- PAR 7 Arithmetic Change of VBE(SAT) @ 150 mA, 15 mA in V

FAILURE DEFINITIONS: ICBO or IEBO in excess of 100 nA
hFE values exceeding ±30%
VCE(SAT) exceeding ±25%
VBE(SAT) exceeding change of ±0.1 V

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER LOT SAMPLE 25

TOTAL NO. FAILURES 8

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.181	0.223	0.25	0.326	1.583	486506.	998999.
2	0	0	0.004	0.003	0.028	0.479	2.86
3	-0.828	-0.695	-0.046	-0.012	0.011	0.045	0.078
4	-0.772	-0.698	-0.035	-0.014	-0.001	0.02	0.048
5	-0.07	-0.069	-0.045	0.001	0.059	0.097	0.315
6	-0.132	-0.027	0.018	0.056	0.201	0.452	0.534
7	-0.009	-0.008	-0.007	-0.006	-0.004	-0.004	-0.003

CONTROL GROUP WITHOUT GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER LOT SAMPLE 25

TOTAL NO. FAILURES 21

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.106	0.109	0.123	0.162	0.549	0.909	1.85
2	0.003	0.005	0.008	0.013	0.018	0.106	2.15
3	-0.917	-0.913	-0.86	-0.812	-0.621	-0.192	0.005
4	-0.782	-0.773	-0.659	-0.6	-0.406	-0.16	0
5	-0.274	-0.249	-0.158	-0.103	-0.064	0.002	0.049
6	-0.047	-0.034	0.007	0.074	0.224	0.307	0.474
7	-0.007	-0.006	-0.005	-0.004	-0.003	-0.003	-0.003

Figure 27 PNP Summary Statistics After 200°C Temperature Step-Stress With Bias

NPN PHASE I

MEDIAN h_{FE} PERCENT CHANGE
AFTER POWER STEP-STRESS

(SHOWN FOR COLLECTOR BIAS CURRENT'S (I_C) OF 0.1, 2, 150 mA)

LEGEND
 ■ CONTRACT STRUCTURE
 □ CONTROL STRUCTURE

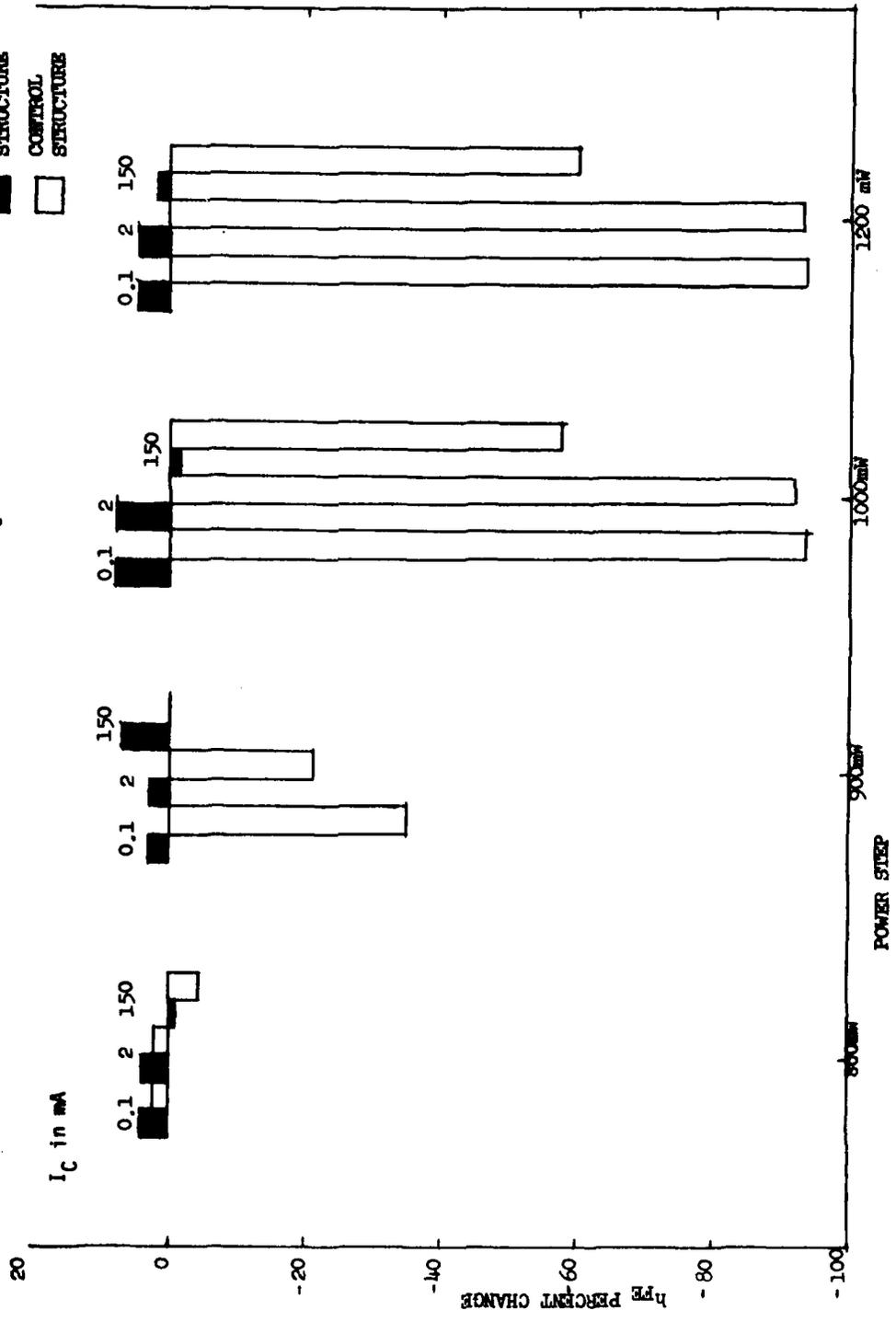


Figure 28 NPN h_{FE} Percent Change After Power Step-Stress

PMP PHASE I

MEDIAN h_{FE} PERCENT CHANGE
AFTER POWER STEP-STRESS

(SHOWN FOR COLLECTOR BIAS CURRENTS (I_C) OF 0.1, 2, 150 mA)

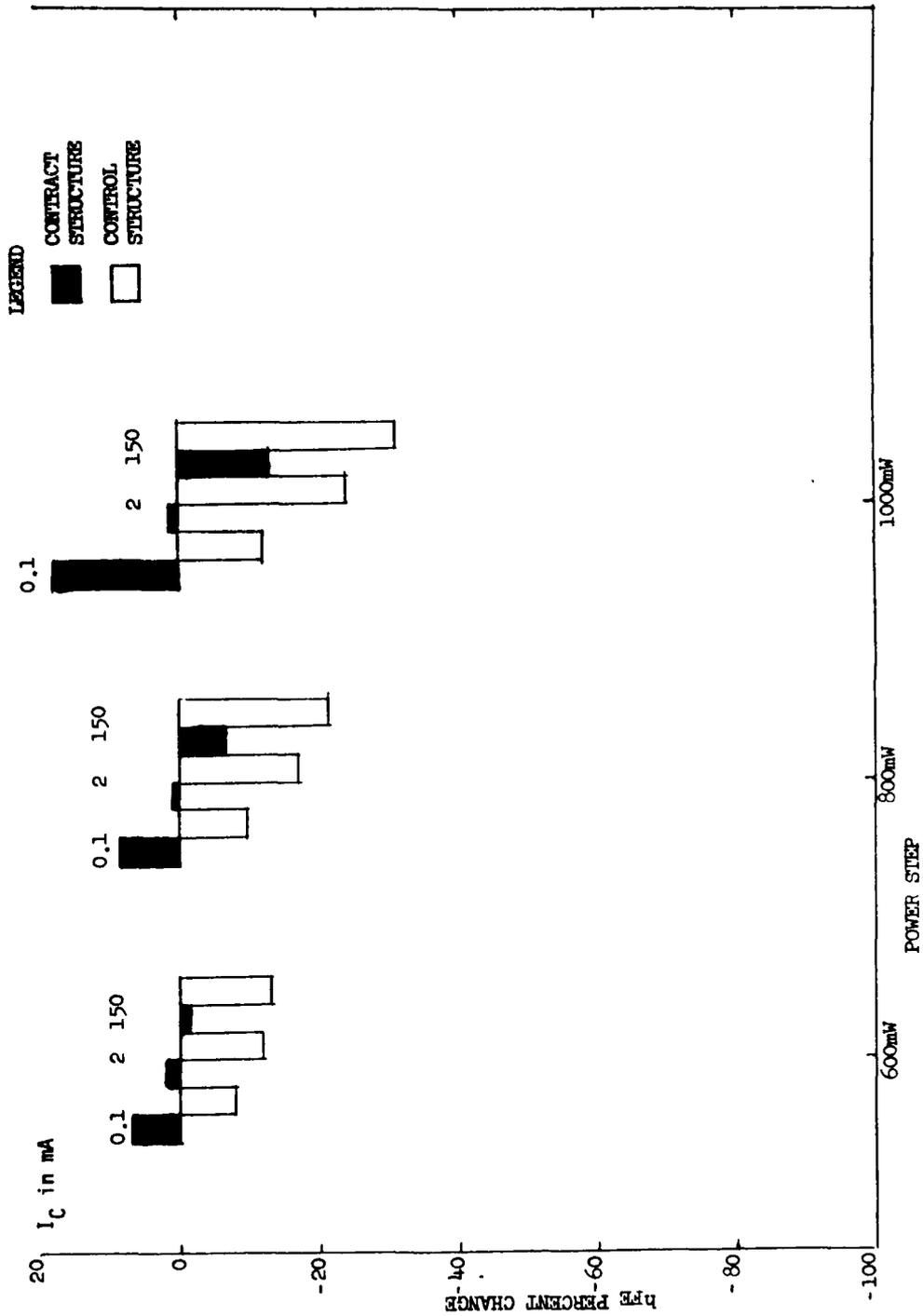


Figure 29 PNP h_{FE} Percent Change After Power Step-Stress

COMPUTERIZED STABILITY SUMMARY STATISTICS

AFTER 1000 mW STEP OF EXTENDED POWER STEP-STRESS (72 hours per step)

NPN
LOT 1014

DEFINITION OF PARAMETERS

- PAR 1 Arithmetic Change of ICBO @ 30 V in nA
- PAR 2 " " of IEBO @ 4 V in nA
- PAR 3 Percent Change (values shown x 100) of hFE @ .1 mA, 2 V
- PAR 4 " " " of hFE @ 2 mA, 2 V
- PAR 5 " " " of hFE @ 150 mA, 2 V
- PAR 6 " " " of VCE(SAT) @ 150 mA, 15 mA
- PAR 7 Arithmetic Change of VBE(SAT) @ 150 mA, 15 mA in V

FAILURE DEFINITIONS: ICBO and IEBO in excess of 100 nA
 hFE values exceeding $\pm 30\%$
 VCE(SAT) exceeding $\pm 25\%$
 VBE(SAT) exceeding change of ± 0.1 V

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 40

TOTAL NO. FAILURES 7

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	-0.84	-0.072	-0.023	0.014	0.041	0.11	2499.7
2	-2.6	-0.72	-0.159	0.06	0.3	1.2	65.958
3	-0.825	-0.004	0.047	0.082	0.173	0.272	0.333
4	-0.79	0.024	0.051	0.081	0.142	0.242	1.537
5	-0.313	-0.082	-0.071	-0.019	0.055	0.113	0.188
6	-0.105	-0.085	-0.072	-0.067	-0.058	-0.048	-0.041
7	-0.01	-0.01	-0.009	-0.008	-0.006	-0.006	-0.004

CONTROL GROUP WITHOUT

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 40

TOTAL NO. FAILURES 40

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.021	0.127	1.638	12.1	33.88	74.62	208.729
2	0.06	0.6	3.183	9.978	58.815	152.822	3540.72
3	-0.954	-0.951	-0.949	-0.941	-0.934	-0.911	-0.568
4	-0.942	-0.939	-0.934	-0.924	-0.912	-0.797	-0.347
5	-0.839	-0.784	-0.692	-0.585	-0.491	-0.414	-0.178
6	-0.059	-0.053	-0.04	-0.026	-0.013	0	0.013
7	-0.012	-0.011	-0.01	-0.009	-0.006	-0.005	-0.002

Figure 30 NPN Summary Statistics After Power Step-Stress

COMPUTERIZED STABILITY SUMMARY STATISTICS

LOT 7010
Phase I-PNP

AFTER 800 mW STEP OF CONTINUOUS POWER STEP-STRESS (72 hours per Step)

DEFINITION OF PARAMETERS

- PAR 1 Arithmetic Change of ICBO @ 30 V in nA
- PAR 2 " " of IEBO @ 4 V in nA
- PAR 3 Percent Change (values shown x 100) of hFE @ .1 mA, 2 V
- PAR 4 " " " of hFE @ 2 mA, 2 V
- PAR 5 " " " of hFE @ 150 mA, 2 V
- PAR 6 " " " of VCE(SAT) @ 150 mA, 15 mA
- PAR 7 Arithmetic Change of VBE(SAT) @ 150 mA, 15 mA in V

FAILURE DEFINITIONS: ICBO or IEBO in excess of 100 nA
 hFE values exceeding $\pm 30\%$
 VCE(SAT) exceeding $\pm 25\%$
 VBE(SAT) exceeding change of ± 0.1 V

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 20

TOTAL NO. FAILURES 5

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.113	0.162	0.237	0.26	0.474	0.683	1.19
2	0.002	0.003	0.006	0.009	0.014	0.099	4.01
3	-0.014	-0.006	0.013	0.092	0.135	0.198	0.203
4	-0.06	-0.044	-0.029	0.014	0.042	0.108	0.118
5	-0.16	-0.11	-0.091	-0.074	-0.046	-0.036	0.012
6	0	0.005	0.019	0.052	0.191	0.369	0.715
7	-0.006	-0.004	-0.003	-0.002	-0.001	0	0

CONTROL GROUP WITHOUT

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 20

TOTAL NO. FAILURES 7

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.079	0.082	0.106	0.299	0.454	1.48	3.24
2	0	0.01	0.012	0.016	0.018	0.021	0.544
3	-0.177	-0.153	-0.125	-0.105	-0.051	-0.036	-0.014
4	-0.243	-0.222	-0.201	-0.174	-0.137	-0.118	-0.104
5	-0.31	-0.298	-0.257	-0.226	-0.183	-0.162	-0.127
6	0.007	0.027	0.06	0.153	0.485	0.782	0.961
7	-0.006	-0.006	-0.005	-0.004	-0.002	-0.002	0.009

Figure 31 PNP Summary Statistics After Power Step-Stress

CUMULATIVE FAILURE* SUMMARY
 AFTER ACCELERATED STEP-STRESS IN TEMPERATURE AND POWER
 (NPN AND PNP PHASE I)

DEVICE TYPE	SAMPLE SIZE	TEMPERATURE STEP-STRESS WITH BIAS		
		175°C	200°C	250°C
NPN CONTRACT	25	0	2	9
NPN CONTROL	25	2	25	25
PNP CONTRACT	25	6	8	21
PNP CONTROL	25	6	21	24

	SAMPLE SIZE	TEMPERATURE STEP-STRESS W/O BIAS		
		200°C	225°C	250°C
NPN CONTRACT	25	0	0	18
NPN CONTROL	25	0	0	20
PNP CONTRACT	25	0	2	25
PNP CONTROL	25	3	5	25

	SAMPLE SIZE	POWER STEP-STRESS			
		800mW	900mW	1000mW	1200mW
NPN CONTRACT	40	1	1	7	35
NPN CONTROL	40	0	22	40	40
PNP CONTRACT	25	5	-	5	17
PNP CONTROL	25	7	-	14	20

*FAILURE CRITERIA: I_{CBO} OR $I_{EBO} > 100nA$, $\Delta h_{FE} > \pm 30\%$,
 $\Delta V_{CE(sat)} \geq 25\%$, $\Delta V_{BE(sat)} > 0.1V$

Figure 32 Cumulative Failure Count Summary After Temperature and Power Step-Stresses

COMPUTERIZED STABILITY SUMMARY STATISTICS

AFTER 1200 mW STEP OF EXTENDED POWER STEP-STRESS (72 hours per step)

NPN
LOT 1014

DEFINITION OF PARAMETERS

- PAR 1 Arithmetic Change of I_{CBO} @ 30 V in nA
- PAR 2 " " of I_{EBO} @ 4 V in nA
- PAR 3 Percent Change (values shown x 100) of hFE @ .1 mA, 2 V
- PAR 4 " " " of hFE @ 2 mA, 2 V
- PAR 5 " " " of hFE @ 150 mA, 2 V
- PAR 6 " " " of VCE(SAT) @ 150 mA, 15 mA
- PAR 7 Arithmetic Change of VBE(SAT) @ 150 mA, 15 mA in V

FAILURE DEFINITIONS: I_{CBO} and I_{EBO} in excess of 100 nA
 hFE values exceeding $\pm 30\%$
 VCE(SAT) exceeding $\pm 25\%$
 VBE(SAT) exceeding change of ± 0.1 V

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER LOT SAMPLE 40

TOTAL NO. FAILURES 35

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	-0.263	-0.162	-0.055	-0.006	0.073	0.138	11597.4
2	-4.21	-1.24	-0.68	-0.214	0.2	3	288989
3	-0.834	-0.783	-0.768	0.052	0.423	0.71	13
4	-0.843	-0.787	-0.765	0.047	0.361	0.556	0.592
5	-0.689	-0.569	-0.367	0.016	0.462	0.59	0.75
6	-0.053	-0.047	-0.035	-0.019	0.01	0.033	0.043
7	-0.007	-0.004	-0.003	-0.002	0	0.001	0.002

CONTROL GROUP WITHOUT GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER LOT SAMPLE 40

TOTAL NO. FAILURES 40

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	-0.144	0.018	0.292	1.62	5.64	30.666	5550.3
2	-0.093	0.318	1.216	7.03	30.534	83.851	285.645
3	-0.955	-0.952	-0.949	-0.944	-0.938	-0.934	-0.921
4	-0.946	-0.944	-0.939	-0.932	-0.918	-0.862	-0.793
5	-0.754	-0.714	-0.66	-0.605	-0.491	-0.375	0
6	0.073	0.135	0.912	1.373	2.133	2.577	11.974
7	-0.002	0.018	0.089	0.121	0.188	0.19	0.191

Figure 33 NPN Summary Statistics After Final Power Step-Stress

COMPUTERIZED STABILITY SUMMARY STATISTICS

AFTER FINAL STEP (250°C) OF TEMPERATURE STEP-STRESS WITH APPLIED BIAS
of $V_{CB} = 30$ V, $V_{EB} = 4$ V (72 hours per step)

NPN
LOT 1014

DEFINITION OF PARAMETERS

- PAR 1 Arithmetic Change of I_{CBO} @ 30 V in nA
- PAR 2 " " of I_{EBO} @ 4 V in nA
- PAR 3 Percent Change (values shown x 100) of h_{FE} @ .1 mA, 2 V
- PAR 4 " " " of h_{FE} @ 2 mA, 2 V
- PAR 5 " " " of h_{FE} @ 150 mA, 2 V
- PAR 6 " " " of $V_{CE(SAT)}$ @ 150 mA, 15 mA
- PAR 7 Arithmetic Change of $V_{BE(SAT)}$ @ 150 mA, 15 mA in V

FAILURE DEFINITIONS: I_{CBO} and I_{EBO} in excess of 100 nA
 h_{FE} values exceeding $\pm 30\%$
 $V_{CE(SAT)}$ exceeding $\pm 25\%$
 $V_{BE(SAT)}$ exceeding change of ± 0.1 V

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 25

TOTAL NO. FAILURES 9

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	-0.209	-0.147	-0.03675	0.0405	0.08575	0.133	0.939
2	-0.13	0.17	0.2475	0.44	0.8925	4.21	6916.03
3	-0.748	-0.5185	-0.2355	-0.043	0.07025	0.153	0.292
4	-0.754	-0.3885	-0.147	-0.0185	0.0795	0.1455	0.252
5	-0.099	-0.0375	0.09975	0.2275	0.25975	0.378	1.157
6	-0.041	-0.0055	0.011	0.012	0.023	0.0355	0.04
7	-0.003	-0.002	0	0	0.001	0.002	0.003

CONTROL GROUP WITHOUT

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 25

TOTAL NO. FAILURES 25

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.036	0.231	5.734	28.932	92.616	186.204	870000.
2	-0.225	0.7335	3.2905	15.8915	44.193	78.914	6659.49
3	-0.955	-0.954	-0.9505	-0.9475	-0.94225	-0.935	-0.934
4	-0.947	-0.9455	-0.943	-0.9385	-0.93125	-0.927	-0.923
5	-0.977	-0.821	-0.783	-0.74	-0.7015	-0.647	-0.62
6	0.072	0.08	0.11325	0.119	0.1375	0.2595	12.32
7	9.99995E-4	0.001	0.002	0.005	0.016	0.028	0.191

Figure 34 NPN Summary Statistics After Final Temperature Step-Stress With Bias

NPN PHASE II

DISTRIBUTION OF h_{FE} PERCENT CHANGE
 AFTER 7500 HOURS OF TEMPERATURE-HUMIDITY CYCLING WITH OPERATING POWER

$h_{FE} @ V_{CE} = 2V, I_C = 150 \text{ mA}$

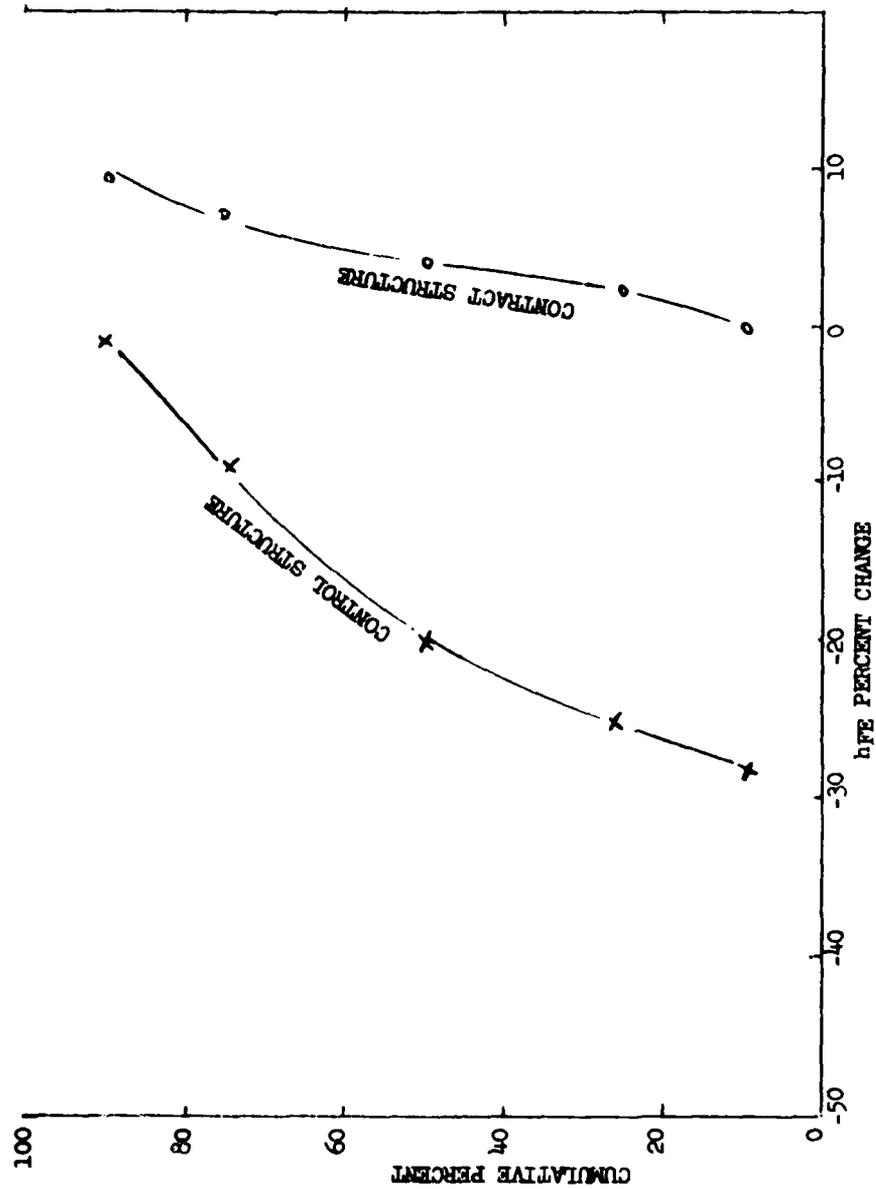


Figure 35 NPN h_{FE} Percent Change After 7500 Hours of Temperature and Humidity Cycling With Operating Power

NPN PHASE II

DISTRIBUTION OF h_{FE} PERCENT CHANGE

AFTER 7500 HOURS OF TEMPERATURE STRESS WITH APPLIED BIAS

h_{FE} @ $V_{CE} = 2V, I_C = 150 \text{ mA}$

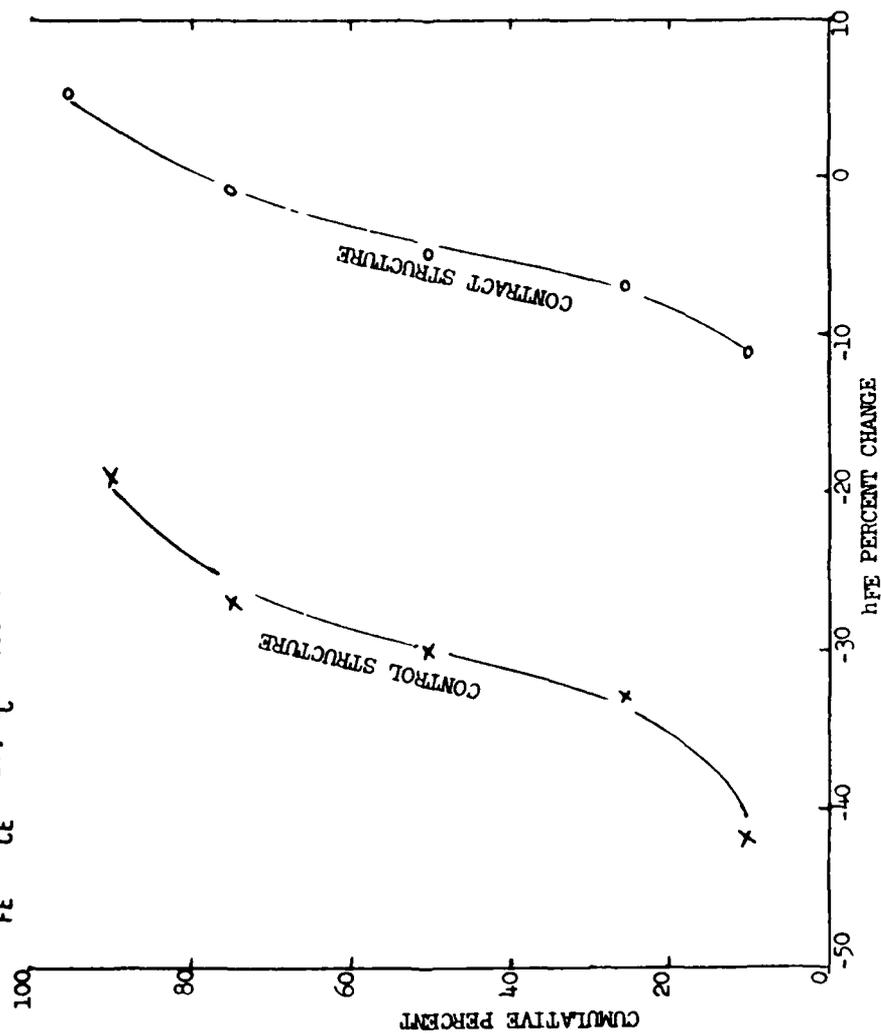


Figure 36 NPN h_{FE} Percent Change After 7500 Hours of Temperature Stress With Bias

CUMULATIVE FAILURE SUMMARY

(FAILURE CRITERIA CONSISTENT WITH THE SPECIFICATION IN FIRST ARTICLE INSPECTION)*

AFTER TEMPERATURE - HUMIDITY CYCLING (MIL-STD-202, METHOD 106B) WITH BIAS OF $V_{CE0} = 20V$

STRESS CELL 1 NON-PRECONDITIONED

<u>DEVICE</u>	<u>SAMPLE SIZE</u>	<u>CUMULATIVE HOURS OF STRESS</u>					
		<u>168</u>	<u>500</u>	<u>1000</u>	<u>2700</u>	<u>5000</u>	<u>7500</u>
D32D(CONTRACT)	132	0	1 (1%)	1 (1%)	1 (1%)	1 (1%)	1 (1%)
D32D(CONTROL)	68	0	2 (3%)	2 (3%)	2 (3%)	2 (2%)	2 (2%)

* FAILURE CRITERIA: I_{CDO} OR $I_{EBO} > 30nA$, Δh_{FE} @ 150mA, $2V > \pm 25\%$, $V_{CE(sat)} > 0.5V$

Figure 37 NPN Cumulative Failure Summary After 7500 Hours of Temperature-Humidity Cycling With Bias.

CUMULATIVE FAILURE SUMMARY

(FAILURE CRITERIA CONSISTENT WITH THE SPECIFICATION IN FIRST ARTICLE INSPECTION)*

AFTER 175°C TEMPERATURE WITH APPLIED BIAS OF $V_{CB} = 30V$, $V_{EB} = 4V$

STRESS CELL 2 NON-PRECONDITIONED

DEVICE	SAMPLE SIZE	CUMULATIVE HOURS OF STRESS					
		168	500	1000	2700	5000	7500
D32D (CONTRACT)	120	1 (1%)	2 (2%)	2 (2%)	2 (2%)	7 (6%)	20 (17%)
D32D (CONTROL)	60	2 (3%)	45 (75%)	54 (90%)	54 (90%)	58 (97%)	60 (100%)

*FAILURE CRITERIA: I_{CBO} OR $I_{EBO} > 30nA$, Δh_{FE} @ 150mA, $2V > \pm 25\%$, $V_{CE(sat)} > 0.5V$

Figure 38 NPN Cumulative Failure Summary After 7500 Hours of Temperature With Bias

CUMULATIVE FAILURE SUMMARY

(FAILURE CRITERIA CONSISTENT WITH THE SPECIFICATION IN FIRST ARTICLE INSPECTION)*

AFTER TEMPERATURE - HUMIDITY CYCLING (MIL-STD-202, METHOD 106B) WITH OPERATING POWER OF 360mW

STRESS CELL 3 NON-PRECONDITIONED

DEVICE	SAMPLE SIZE	CUMULATIVE HOURS OF STRESS					
		168	500	1000	2700	5000	7500
D32D(CONTRACT)	120	0	0	1 (1%)	1 (1%)	1 (1%)	2 (2%)
D32D(CONTROL)	60	0	3 (5%)	6 (10%)	10 (17%)	18 (30%)	18 (30%)

* FAILURE CRITERIA: I_{CBO} OR $I_{E30} > 30nA$, Δh_{FE} @ 150mA, $2V > \pm 25\%$, $V_{CE(sat)} > 0.5V$

Figure 39 NPN Cumulative Failure Summary After 7500 Hours of Temperature-Humidity Cycling With Operating Power

COMPUTERIZED STABILITY SUMMARY STATISTICS

NPN LOT 1014

Phase II

AFTER 7500 HOURS OF TEMPERATURE AND HUMIDITY CYCLING (MIL-STD-202, METHOD 106B)

WITH APPLIED BIAS OF $V_{CBO} = 20V$ (STRESS CELL 1 NON-PRECONDITIONED)

DEFINITION OF PARAMETERS

- PAR 1 Arithmetic Change of I_{CBO} @ 30 V in nA
- PAR 2 " " of I_{EBO} @ 4 V in nA
- PAR 3 Percent Change (values shown x 100) of h_{FE} @ .1 mA, 2 V
- PAR 4 " " " of h_{FE} @ 2 mA, 2 V
- PAR 5 " " " of h_{FE} @ 150 mA, 2 V
- PAR 6 " " " of $V_{CE(SAT)}$ @ 150 mA, 15 mA
- PAR 7 Arithmetic Change of $V_{BE(SAT)}$ @ 150 mA, 15 mA in V

FAILURE DEFINITIONS: I_{CBO} or I_{EBO} in excess of 100 nA
 h_{FE} values exceeding $\pm 30\%$
 $V_{CE(SAT)}$ exceeding $\pm 25\%$
 $V_{BE(SAT)}$ exceeding change of ± 0.1 V

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 44

TOTAL NO. FAILURES 10							
PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.148	0.167	0.185	0.211	0.24	0.283	0.401
2	0.004	1.56	2.04	2.91	5.68	7.624	24.9
3	-0.067	-0.047	-0.032	-0.017	0	0.011	0.033
4	-0.061	-0.041	-0.023	-0.011	0.011	0.041	0.167
5	-0.052	-0.039	0.013	0.036	0.067	0.097	0.114
6	-0.032	0	0	0.01	0.021	0.065	0.24
7	-0.006	-0.004	-0.002	0.001	0.005	0.006	0.014

CONTROL GROUP WITHOUT

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 23

TOTAL NO. FAILURES 0							
PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.161	0.174	0.189	0.228	0.293	0.324	0.626
2	0.246	0.259	0.466	0.985	1.63	6.642	9.9
3	-0.179	-0.074	-0.052	-0.033	-0.019	-0.009	0
4	-0.114	-0.053	-0.049	-0.031	-0.016	-0.002	0.079
5	-0.091	-0.066	-0.004	0.043	0.068	0.126	0.194
6	-0.013	-0.009	0	0.027	0.049	0.106	0.13
7	-0.006	-0.005	-0.004	-0.003	0.005	0.008	0.054

Figure 40 NPN Summary Statistics, 7500 Hours, Temperature-Humidity Cycling With Bias, Lot 1014

COMPUTERIZED STABILITY SUMMARY STATISTICS

NPN LOT 1021

Phase II

AFTER 7500 HOURS OF TEMPERATURE AND HUMIDITY CYCLING (MIL-STD-202, METHOD 106B)
WITH APPLIED BIAS OF $V_{CE0} = 20V$ (STRESS CELL 1 NON-PRECONDITIONED)

DEFINITION OF PARAMETERS

- PAR 1 Arithmetic Change of I_{CBO} @ 30 V in nA
- PAR 2 " " of I_{EBO} @ 4 V in nA
- PAR 3 Percent Change (values shown x 100) of hFE @ .1 mA, 2 V
- PAR 4 " " " of hFE @ 2 mA, 2 V
- PAR 5 " " " of hFE @ 150 mA, 2 V
- PAR 6 " " " of $V_{CE}(SAT)$ @ 150 mA, 15 mA
- PAR 7 Arithmetic Change of $V_{BE}(SAT)$ @ 150 mA, 15 mA in V

FAILURE DEFINITIONS: I_{CBO} or I_{EBO} in excess of 100 nA
hFE values exceeding $\pm 30\%$
 $V_{CE}(SAT)$ exceeding $\pm 25\%$
 $V_{BE}(SAT)$ exceeding change of ± 0.1 V

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 44

TOTAL NO. FAILURES 1

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.254	0.277	0.294	0.319	0.352	0.406	2089.71
2	0.455	0.624	1.04	1.57	2.72	4.112	7.28
3	-0.1	-0.028	-0.02	-0.01	0	0.007	0.02
4	-0.051	-0.029	-0.022	-0.011	-0.005	0.003	0.129
5	-0.046	-0.038	0	0.029	0.057	0.073	0.099
6	-0.012	-0.011	-0.011	0	0.024	0.059	0.195
7	-0.006	-0.005	-0.004	-0.004	-0.003	0.003	0.006

CONTROL GROUP WITHOUT

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 22

TOTAL NO. FAILURES 0

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.015	0.095	0.133	0.147	0.186	0.229	0.267
2	0.231	0.239	0.356	0.603	0.734	1.326	2.5
3	-0.086	-0.073	-0.059	-0.037	-0.025	-0.015	-0.014
4	-0.062	-0.059	-0.042	-0.029	-0.013	-0.01	0.016
5	-0.026	0.026	0.032	0.067	0.095	0.124	0.138
6	-0.014	-0.01	0	0.013	0.043	0.099	0.205
7	-0.005	-0.005	-0.004	-0.002	0	0.004	0.034

Figure 41 NPN Summary Statistics, 7500 Hours, Temperature-Humidity Cycling With Bias, Lot 1021

COMPUTERIZED STABILITY SUMMARY STATISTICS

NPN LOT 1022
Phase II

AFTER 7500 HOURS OF TEMPERATURE AND HUMIDITY CYCLING (MIL-STD-202, METHOD 106B)
AFTER APPLIED BIAS OF V_{CE0} = 20V (STRESS CELL 1 NON-PRECONDITIONED)

DEFINITION OF PARAMETERS

- PAR 1 Arithmetic Change of I_{CBO} @ 30 V in nA
- PAR 2 " " of I_{EBO} @ 4 V in nA
- PAR 3 Percent Change (values shown x 100) of h_{FE} @ .1 mA, 2 V
- PAR 4 " " " of h_{FE} @ 2 mA, 2 V
- PAR 5 " " " of h_{FE} @ 150 mA, 2 V
- PAR 6 " " " of V_{CE(SAT)} @ 150 mA, 15 mA
- PAR 7 Arithmetic Change of V_{BE(SAT)} @ 150 mA, 15 mA in V

FAILURE DEFINITIONS: I_{CBO} or I_{EBO} in excess of 100 nA
h_{FE} values exceeding ±30%
V_{CE(SAT)} exceeding ±25%
V_{BE(SAT)} exceeding change of ±0.1 V

CLASSIFICATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 44

TOTAL NO. FAILURES 0							
PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.164	0.246	0.266	0.287	0.331	0.445	1.41
2	0.581	1.082	1.49	2.15	4.01	7.062	11.3
3	-0.017	-0.005	0.006	0.019	0.031	0.036	0.055
4	-0.015	-0.007	0	0.015	0.024	0.03	0.05
5	-0.009	0.004	0.021	0.04	0.063	0.081	0.146
6	-0.025	-0.014	-0.011	0.011	0.027	0.053	0.065
7	-0.008	-0.007	-0.006	-0.006	-0.003	0	0.02

CONTROL GROUP WITHOUT

CLASSIFICATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 23

TOTAL NO. FAILURES 0							
PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.126	0.129	0.14	0.159	0.207	0.253	0.369
2	0.237	0.256	0.326	0.424	0.582	0.885	1.99
3	-0.041	-0.04	-0.032	-0.023	-0.018	-0.011	-0.01
4	-0.038	-0.03	-0.02	-0.01	-0.006	0	0
5	-0.021	0	0.02	0.045	0.066	0.087	0.115
6	-0.013	0	0	0.014	0.041	0.055	0.129
7	-0.006	-0.006	-0.005	-0.004	-0.003	0.002	0.003

Figure 42 NPN Summary Statistics, 7500 Hours, Temperature-Humidity Cycling With Bias, Lot 1022

COMPUTERIZED STABILITY SUMMARY STATISTICS

NPN LOT 1014
Phase II

AFTER 7500 HOURS OF 175°C TEMPERATURE

WITH APPLIED BIAS OF VCB = 30V, VEB = 4V (STRESS CELL 2 NON-PRECONDITIONED)

DEFINITION OF PARAMETERS

- PAR 1 Arithmetic Change of ICBO @ 30 V in nA
- PAR 2 " " of IEBO @ 4 V in nA
- PAR 3 Percent Change (values shown x 100) of hFE @ .1 mA, 2 V
- PAR 4 " " " of hFE @ 2 mA, 2 V
- PAR 5 " " " of hFE @ 150 mA, 2 V
- PAR 6 " " " of VCE(SAT) @ 150 mA, 15 mA
- PAR 7 Arithmetic Change of VBE(SAT) @ 150 mA, 15 mA in V

FAILURE DEFINITIONS: ICBO or IEBO in excess of 100 nA

hFE values exceeding ±30%

VCE(SAT) exceeding ±25%

VBE(SAT) exceeding change of ±0.1 V

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 40

TOTAL NO. FAILURES 39

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PTCL	MAX VAL
1	0.107	0.118	0.145	0.188	0.261	0.343	493
2	1.09	1.53	2.11	3.88	7.8	11.3	136.61
3	-0.506	-0.074	-0.054	-0.034	0.024	0.079	16.375
4	-0.211	-0.048	-0.031	-0.017	0.021	0.083	0.186
5	-0.118	-0.107	-0.071	-0.053	-0.01	0.047	0.068
6	0.204	0.519	0.811	1.061	2.49	4.669	9.091
7	0.002	0.004	0.005	0.006	0.007	0.007	0.019

CONTROL GROUP WITHOUT

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 20

TOTAL NO. FAILURES 20

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PTCL	MAX VAL
1	0.09	0.112	0.134	0.155	0.205	0.278	0.39
2	0.218	0.24	0.372	0.503	0.797	1.14	2.82
3	-0.353	-0.346	-0.329	-0.296	-0.25	-0.109	0.095
4	-0.389	-0.387	-0.358	-0.31	-0.212	-0.161	0.017
5	-0.486	-0.441	-0.333	-0.303	-0.268	-0.19	-0.042
6	1.903	2.945	3.883	6.039	9.513	11.216	13.07
7	-0.014	0.003	0.005	0.007	0.009	0.011	0.049

Figure 43 NPN Summary Statistics, 7500 Hours, Temperature With Bias, Lot 1014

COMPUTERIZED STABILITY SUMMARY STATISTICS

NPN LOT 1021
Phase II

AFTER 7500 HOURS OF 175°C TEMPERATURE

WITH APPLIED BIAS OF $V_{CB} = 30V$, $V_{EB} = 4V$ (STRESS CELL 2 NON-PRECONDITIONED)

DEFINITION OF PARAMETERS

- PAR 1 Arithmetic Change of I_{CBO} @ 30 V in nA
- PAR 2 " " of I_{EBO} @ 4 V in nA
- PAR 3 Percent Change (values shown x 100) of h_{FE} @ .1 mA, 2 V
- PAR 4 " " " of h_{FE} @ 2 mA, 2 V
- PAR 5 " " " of h_{FE} @ 150 mA, 2 V
- PAR 6 " " " of $V_{CE(SAT)}$ @ 150 mA, 15 mA
- PAR 7 Arithmetic Change of $V_{BE(SAT)}$ @ 150 mA, 15 mA in V

FAILURE DEFINITIONS: I_{CBO} or I_{EBO} in excess of 100 nA

h_{FE} values exceeding $\pm 30\%$

$V_{CE(SAT)}$ exceeding $\pm 25\%$

$V_{BE(SAT)}$ exceeding change of $\pm 0.1 V$

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 40

TOTAL NO. FAILURES 39

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.213	0.223	0.247	0.285	0.343	0.381	2.75
2	0.718	0.96	1.13	1.0	2.52	3.94	8.8
3	-0.074	-0.053	-0.042	-0.023	-0.014	-0.008	0.03
4	-0.112	-0.09	-0.074	-0.042	-0.023	-0.017	0.046
5	-0.217	-0.184	-0.145	-0.109	-0.076	-0.048	0
6	0.247	0.326	0.43	0.831	1.393	2.605	5.702
7	0	0.002	0.004	0.004	0.005	0.006	0.023

CONTROL GROUP WITHOUT

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 20

TOTAL NO. FAILURES 20

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.075	0.093	0.115	0.162	0.232	0.381	1.53
2	0.366	0.38	0.406	0.497	0.644	0.597	0.308
3	-0.926	-0.875	-0.607	-0.394	-0.22	-0.183	-0.036
4	-0.764	-0.536	-0.453	-0.372	-0.263	-0.181	-0.091
5	-0.486	-0.465	-0.393	-0.362	-0.309	-0.228	-0.115
6	2.36	2.974	4.056	9.382	17.304	10.567	10.006
7	0.003	0.003	0.005	0.007	0.009	0.01	0.013

Figure 44 NPN Summary Statistics, 7500 Hours, Temperature With Bias, Lot 1021

COMPUTERIZED STABILITY SUMMARY STATISTICS

NPN LOT 1022
Phase II

AFTER 7500 HOURS OF 175°C TEMPERATURE

WITH APPLIED BIAS OF VCB = 30V, VEB = 4V (STRESS CELL 2 NON-PRECONDITIONED)

DEFINITION OF PARAMETERS

- PAR 1 Arithmetic Change of ICBO @ 30 V in nA
- PAR 2 " " of IEBO @ 4 V in nA
- PAR 3 Percent Change (values shown x 100) of hFE @ .1 mA, 2 V
- PAR 4 " " " of hFE @ 2 mA, 2 V
- PAR 5 " " " of hFE @ 150 mA, 2 V
- PAR 6 " " " of VCE(SAT) @ 150 mA, 15 mA
- PAR 7 Arithmetic Change of VBE(SAT) @ 150 mA, 15 mA in V

FAILURE DEFINITIONS: ICBO or IEBO in excess of 100 nA
hFE values exceeding ±30%
VCE(SAT) exceeding ±25%
VBE(SAT) exceeding change of ±0.1 V

CLASSIFICATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 40

TOTAL NO. FAILURES 32

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.188	0.199	0.216	0.285	0.363	0.51	999000.
2	0.007	0.763	1.14	2.02	3.24	6.15	54.5
3	-0.678	-0.471	-0.095	-0.021	0.019	0.051	331
OVERFLOW IN 3030							
4	-0.482	-0.275	-0.06	-0.012	0.019	0.051	1.70141E+35
5	-0.196	-0.095	-0.067	-0.032	-0.01	0.029	97
6	-0.125	0.084	0.202	1.431	7.341	10.17	11.432
7	-0.006	0.003	0.004	0.005	0.006	0.007	0.188

CONTROL GROUP WITHOUT

CLASSIFICATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 20

TOTAL NO. FAILURES 20

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.071	0.079	0.11	0.351	317.825	14699.9	27399.8
2	0.095	0.27	0.363	0.489	0.598	0.7	1.43
3	-0.856	-0.749	-0.63	-0.386	-0.176	0.008	6.833
4	-0.579	-0.531	-0.398	-0.349	-0.154	0.007	0.161
5	-0.395	-0.376	-0.322	-0.291	-0.247	-0.189	-0.072
6	-0.014	1.69	3.128	11.487	12.429	13.478	13.691
7	-0.005	0.013	0.047	0.134	0.181	0.196	0.197

Figure 45 NPN Summary Statistics, 7500 Hours, Temperature With Bias, Lot 1022

COMPUTERIZED STABILITY SUMMARY STATISTICS

NPN LOT 1014
Phase II

AFTER 7500 HOURS OF TEMPERATURE AND HUMIDITY CYCLING (MIL-STD-202, METHOD 106B)
WITH OPERATING POWER OF 360 mW (STRESS CELL 3 NON-PRECONDITIONED)

DEFINITION OF PARAMETERS

- PAR 1 Arithmetic Change of ICBO @ 30 V in nA
- PAR 2 " " of IEBO @ 4 V in nA
- PAR 3 Percent Change (values shown x 100) of hFE @ .1 mA, 2 V
- PAR 4 " " " of hFE @ 2 mA, 2 V
- PAR 5 " " " of hFE @ 150 mA, 2 V
- PAR 6 " " " of VCE(SAT) @ 150 mA, 15 mA
- PAR 7 Arithmetic Change of VBE(SAT) @ 150 mA, 15 mA in V

FAILURE DEFINITIONS: ICBO or IEBO in excess of 100 nA
hFE values exceeding ±30%
VCE(SAT) exceeding ±25%
VBE(SAT) exceeding change of ±0.1 V

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER LOT SAMPLE 40

TOTAL NO. FAILURES 4

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.145	0.172	0.192	0.206	0.232	0.276	0.798
2	0.495	0.941	1.81	3.35	5.67	8.99	36.8
3	-0.366	-0.133	-0.019	-0.004	0.013	0.063	0.197
4	-0.338	-0.029	-0.018	0	0.013	0.056	0.171
5	-0.373	0	0.025	0.041	0.067	0.088	0.179
6	-0.019	0	0.01	0.031	0.052	0.1	0.495
7	-0.007	-0.004	-0.004	-0.003	-0.003	-0.002	-0.001

CONTROL GROUP WITHOUT
GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER LOT SAMPLE 20

TOTAL NO. FAILURES 10

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.187	0.196	0.243	0.368	0.419	0.764	8.18
2	0.08	0.279	0.334	0.377	0.481	0.987	1.25
3	-0.491	-0.412	-0.327	-0.259	-0.031	0.066	0.145
4	-0.472	-0.387	-0.345	-0.276	-0.09	-0.015	0.087
5	-0.397	-0.283	-0.259	-0.206	-0.092	-0.012	0.121
6	0.036	0.05	0.056	0.081	0.105	0.133	0.23
7	-0.005	-0.005	-0.004	-0.004	-0.003	-0.002	0.003

Figure 46 NPN Summary Statistics, 7500 Hours, Temperature-Humidity Cycling, With Operating Power, Lot 1014

NPN LOT 1021
Phase II

COMPUTERIZED STABILITY SUMMARY STATISTICS

AFTER 7500 HOURS OF TEMPERATURE AND HUMIDITY CYCLING (MIL-STD-202, METHOD 106B)
WITH OPERATING POWER OF 360 mW (STRESS CELL 3 NON-PRECONDITIONED)

DEFINITION OF PARAMETERS

- PAR 1 Arithmetic Change of ICBO @ 30 V in nA
- PAR 2 " " of IEBO @ 4 V in nA
- PAR 3 Percent Change (values shown x 100) of hFE @ .1 mA, 2 V
- PAR 4 " " " of hFE @ 2 mA, 2 V
- PAR 5 " " " of hFE @ 150 mA, 2 V
- PAR 6 " " " of VCE(SAT) @ 150 mA, 15 mA
- PAR 7 Arithmetic Change of VBE(SAT) @ 150 mA, 15 mA in V

FAILURE DEFINITIONS: ICBO or IEBO in excess of 100 nA
hFE values exceeding $\pm 30\%$
VCE(SAT) exceeding $\pm 25\%$
VBE(SAT) exceeding change of ± 0.1 V

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 40

TOTAL NO. FAILURES 0

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.246	0.272	0.292	0.31	0.333	0.373	12.6
2	0.679	0.822	0.956	1.33	1.68	2.86	5.06
3	-0.073	-0.056	-0.042	-0.024	-0.013	0	0.014
4	-0.096	-0.069	-0.056	-0.032	-0.016	-0.006	0.008
5	-0.11	-0.082	-0.048	-0.02	0.015	0.032	0.042
6	-0.024	0	0.011	0.013	0.035	0.077	0.209
7	-0.007	-0.005	-0.005	-0.004	-0.004	-0.003	-0.002

CONTROL GROUP WITHOUT

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 20

TOTAL NO. FAILURES 4

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.109	0.124	0.134	0.169	0.356	0.65	37.3
2	0.226	0.284	0.338	0.478	0.635	0.749	1.12
3	-0.41	-0.262	-0.195	-0.16	-0.085	-0.074	-0.035
4	-0.395	-0.289	-0.239	-0.221	-0.139	-0.102	-0.082
5	-0.333	-0.321	-0.261	-0.204	-0.1	-0.075	-0.02
6	0.013	0.014	0.047	0.055	0.074	0.167	0.265
7	-0.007	-0.006	-0.005	-0.005	-0.004	-0.003	-0.002

Figure 47 NPN Summary Statistics, 7500 Hours, Temperature-Humidity Cycling, With Operating Power, Lot 1021

COMPUTERIZED STABILITY SUMMARY STATISTICS

NPN LOT 1022

Phase II

AFTER 7500 HOURS OF TEMPERATURE AND HUMIDITY CYCLING (MIL-STD-202, METHOD 106B)

WITH OPERATING POWER OF 360 mW (STRESS CELL 3 NON-PRECONDITIONED)

DEFINITION OF PARAMETERS

- PAR 1 Arithmetic Change of ICBO @ 30 V in nA
- PAR 2 " " of IEBO @ 4 V in nA
- PAR 3 Percent Change (values shown x 100) of hFE @ .1 mA, 2 V
- PAR 4 " " " of hFE @ 2 mA, 2 V
- PAR 5 " " " of hFE @ 150 mA, 2 V
- PAR 6 " " " of VCE(SAT) @ 150 mA, 15 mA
- PAR 7 Arithmetic Change of VBE(SAT) @ 150 mA, 15 mA in V

FAILURE DEFINITIONS: ICBO or IEBO in excess of 100 nA

hFE values exceeding ±30%

VCE(SAT) exceeding ±25%

VBE(SAT) exceeding change of ±0.1 V

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 40

TOTAL NO. FAILURES 1

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.207	0.232	0.239	0.25	0.312	0.367	17.9
2	0.442	0.73	1.05	1.55	2.51	3.33	17.6
3	-0.047	-0.019	0	0.028	0.05	0.07	0.106
4	-0.016	-0.008	0.008	0.024	0.046	0.065	0.083
5	-0.04	-0.01	0.011	0.03	0.055	0.068	0.098
6	-0.023	-0.013	0	0	0.014	0.027	0.372
7	-0.009	-0.007	-0.006	-0.006	-0.004	-0.004	0.004

CONTROL GROUP WITHOUT

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 20

TOTAL NO. FAILURES 3

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.113	0.12	0.187	0.258	1.64	3.25	397.779
2	0.26	0.262	0.317	0.397	0.518	0.685	1.34
3	-0.442	-0.07	-0.044	-0.01	0.056	0.095	0.202
4	-0.317	-0.106	-0.074	-0.057	0.019	0.049	0.153
5	-0.171	-0.121	-0.089	-0.035	0.018	0.042	0.164
6	-0.012	0.011	0.027	0.069	0.11	0.131	0.165
7	-0.009	-0.008	-0.007	-0.007	-0.005	-0.001	0

Figure 48 NPN Summary Statistics, 7500 Hours, Temperature-Humidity Cycling, With Operating Power, Lot 1022

PERCENTAGE FAILURES*

AFTER PRECONDITION STRESSING FAILURE CRITERIA

CONSISTENT WITH THE SPECIFICATION IN FIRST ARTICLE GROUP C INSPECTION

DEVICE: D32D NPN TRANSISTOR - PHASE II (Lots 1014, 1021 and 1022)

DEVICE TYPE	SAMPLE SIZE	PRECONDITION STRESS CELL ⁴			CELL ⁵	
		100 CYCLES TEMPERATURE CYCLING	107 HOURS PRESSURE COOKER (15PSIG)	SAMPLE SIZE	107 HOURS PRESSURE COOKER (15PSIG)	
CONTRACT	264	0	30 (11%)	132	9 (7%)	
CONTROL	136	0	57 (42%)	68	16 (24%)	

*FAILURE CRITERIA: I_{CBO} or $I_{EBO} > 100\mu A$, Δh_{FE} @150mA, 2V $> \pm 25\%$

Figure 49 NPN Stress Screen Failure Summaries

COMPUTERIZED STABILITY SUMMARY STATISTICS

AFTER 96 HOURS OF PRESSURE COOKER STRESS @ 15 PSIG (=121°C)

NPN
LOT 1014

DEFINITION OF PARAMETERS

- PAR 1 Arithmetic Change of ICBO @ 30 V in nA
- PAR 2 " " of IEBO @ 4 V in nA
- PAR 3 Percent Change (values shown x 100) of hFE @ .1 mA, 2 V
- PAR 4 " " " of hFE @ 2 mA, 2 V
- PAR 5 " " " of hFE @ 150 mA, 2 V
- PAR 6 " " " of VCE(SAT) @ 150 mA, 15 mA
- PAR 7 Arithmetic Change of VBE(SAT) @ 150 mA, 15 mA in V

FAILURE DEFINITIONS: ICBO and IEBO in excess of 100 nA
 hFE values exceeding ±30%
 VCE(SAT) exceeding ±25%
 VBE(SAT) exceeding change of ±0.1 V

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 25

TOTAL NO. FAILURES 7

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	-0.204	-0.0425	0.03325	0.169	110.06	1394.67	3728
2	-0.02	0	0.05	0.215	0.8925	22.6885	199.6
3	-0.038	-0.031	0.00525	0.0335	0.04625	0.0575	0.094
4	-0.025	-0.0015	0.00875	0.033	0.051	0.0535	0.099
5	-0.014	0.019	0.033	0.0725	0.09875	0.126	0.164
6	0	0	0.01	0.011	0.01875	0.023	0.044
7	-0.002	-0.0015	9.99995E-4	0.002	0.002	0.0035	0.004

CONTROL GROUP WITHOUT

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 25

TOTAL NO. FAILURES 16

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	-0.181	0.193	11.777	107.773	328.403	809.640	1709.65
2	-0.014	0.0385	0.07475	1.1215	116.679	686.883	1189.56
3	-0.093	-0.0465	0	0.018	0.021	0.0395	0.043
4	0	0	0	0.0155	0.018	0.0325	0.038
5	-0.074	-0.042	0	0.044	0.1415	0.2915	16
6	0.013	0.0135	0.02625	0.038	0.052	0.0715	0.2
7	-0.003	-0.002	-9.99999E-4	0	9.99999E-4	0.0015	0.015

Figure 50 NPN Summary Statistics After Pressure Cooker Stress

CUMULATIVE FAILURE SUMMARY AFTER ACCELERATED PRESSURE
COOKER STRESS @ 15 PSIG (121°C)

DEVICE: D32D NPN TRANSISTOR WITH GLASSIVATION, REFRACTORY
METAL AND SILICON NITRIDE BARRIER

FAILURE CRITERIA: I_{CBO} AND I_{EBO} 100nA
 $\Delta h_{FE} > \pm 30\%$
 $\Delta V_{CE(sat)} \pm 25\%$
 $\Delta V_{BE(sat)} 0.1V$

<u>DEVICE</u>	<u>SAMPLE SIZE</u>	<u>72 HOURS</u>	<u>96 HOURS</u>	<u>144 HOURS</u>
D32D (CONTRACT)	25	1	7	14
D32D (CONTROL)	25	0	16	16

Figure 51 NPN Cumulative Failure Count Summary After Pressure Cooker Stress

COMPUTERIZED STABILITY SUMMARY STATISTICS

NPN LOT 1014

AFTER 250 CYCLES OF THERMAL SHOCK STRESS (-75°C to +150°C, Fluid to Fluid, 5 minutes at temperature extremes, 15 second maximum transfer time).

DEFINITION OF PARAMETERS

- PAR 1 Arithmetic Change of I_{CBO} @ 30 V in nA
- PAR 2 " " of I_{EBO} @ 4 V in nA
- PAR 3 Percent Change (values shown x 100) of h_{FE} @ .1 mA, 2 V
- PAR 4 " " " of h_{FE} @ 2 mA, 2 V
- PAR 5 " " " of h_{FE} @ 150 mA, 2 V
- PAR 6 " " " of $V_{CE}(SAT)$ @ 150 mA, 15 mA
- PAR 7 Arithmetic Change of $V_{BE}(SAT)$ @ 150 mA, 15 mA in V

FAILURE DEFINITIONS: I_{CBO} and I_{EBO} in excess of 100 nA
 h_{FE} values exceeding $\pm 30\%$
 $V_{CE}(SAT)$ exceeding $\pm 25\%$
 $V_{BE}(SAT)$ exceeding change of ± 0.1 V

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER LOT SAMPLE 25

TOTAL NO. FAILURES 1

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	-0.045	-0.036	0.02775	0.2485	0.0675	0.1055	0.210
2	-0.4	-0.169	0.0725	0.12	2.16	0.21	0.3
3	-0.006	0	0.006	0.0175	0.02625	0.037	0.051
4	0	0	0.006	0.013	0.019	0.03	0.04
5	-0.044	-0.023	-0.01475	0	0.02275	0.2305	0.028
6	0	0	0.011	0.011	0.02175	0.032	0.005
7	-0.004	-0.003	-0.002	-0.0015	0	0.001	0.055

CONTROL GROUP WITHOUT GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER LOT SAMPLE 25

TOTAL NO. FAILURES 0

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	-0.305	-0.095	0.02875	0.0345	0.042	0.0865	0.167
2	-0.015	0.005	0.0135	0.035	0.06275	0.080	0.14
3	0	0	0.004	0.019	0.031	0.0515	0.063
4	0	0	0.01425	0.023	0.03175	0.0365	0.047
5	-0.043	-0.037	-0.02325	0	0.04375	0.07	0.111
6	0	0	0.013	0.013	0.01375	0.027	0.030
7	-0.005	-0.004	-0.003	-0.003	-0.002	-0.00075E-4	0

Figure 52 NPN Summary Statistics After Thermal Shock Stress

COMPUTERIZED STABILITY SUMMARY STATISTICS

NPN
LOT 1014

AFTER 30 CYCLES OF HUMIDITY CYCLING (MIL-STD-202, Method 106B)
WITH APPLIED BIAS, V_{CEO} = 20 V

DEFINITION OF PARAMETERS

- PAR 1 Arithmetic Change of I_{CEO} @ 30 V in nA
- PAR 2 " " of I_{EBO} @ 4 V in nA
- PAR 3 Percent Change (values shown x 100) of h_{FE} @ .1 mA, 2 V
- PAR 4 " " " of h_{FE} @ 2 mA, 2 V
- PAR 5 " " " of h_{FE} @ 150 mA, 2 V
- PAR 6 " " " of V_{CE(SAT)} @ 150 mA, 15 mA
- PAR 7 Arithmetic Change of V_{BE(SAT)} @ 150 mA, 15 mA in V

FAILURE DEFINITIONS: I_{CEO} and I_{EBO} in excess of 100 nA
h_{FE} values exceeding ±30%
V_{CE(SAT)} exceeding ±25%
V_{BE(SAT)} exceeding change of ±0.1 V

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER LOT SAMPLE 25

TOTAL NO. FAILURES @							
PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	-0.137	-0.043	-0.01425	0.0295	0.067	0.6645	26.25
2	-0.14	0.15	0.2	0.25	0.3075	0.465	1.3
3	0.02	0.0255	0.03025	0.0445	0.048	0.050	0.067
4	0.02	0.0205	0.02725	0.037	0.04175	0.0465	0.049
5	-0.014	-0.007	0.01925	0.027	0.03075	0.042	0.05
6	-0.01	0	0	0	0.011	0.011	0.212
7	-0.005	-0.005	-0.00475	-0.004	-0.003	-0.003	-0.002

CONTROL GROUP WITHOUT
GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER LOT SAMPLE 25

TOTAL NO. FAILURES @							
PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	-0.135	-0.041	-0.00975	0.0145	0.04375	0.103	4.2
2	-0.055	-0.0085	0.00025	0.021	0.03675	0.1205	4.041
3	0	0	0.004	0.031	0.036	0.0455	0.066
4	0	0	0.01425	0.018	0.02875	0.0335	0.044
5	-0.1	-0.07	-0.03775	-0.031	0	0.0145	0.180
6	0	0	0	0	0.012	0.013	0.013
7	-0.005	-0.0045	-0.004	-0.003	-0.002	-0.001	0.021

Figure 53 NPN Summary Statistics After Humidity Cycling With Bias

COMPUTERIZED STABILITY SUMMARY STATISTICS

LOT 7010
Phase I-PNP

AFTER 400 CYCLES OF TEMPERATURE CYCLING (air-to-air, -65°C to +150°C)

DEFINITION OF PARAMETERS

- PAR 1 Arithmetic Change of ICBO @ 30 V in nA
- PAR 2 " " of IEBO @ 4 V in nA
- PAR 3 Percent Change (values shown x 100) of hFE @ .1 mA, 2 V
- PAR 4 " " " of hFE @ 2 mA, 2 V
- PAR 5 " " " of hFE @ 150 mA, 2 V
- PAR 6 " " " of VCE(SAT) @ 150 mA, 15 mA
- PAR 7 Arithmetic Change of VBE(SAT) @ 150 mA, 15 mA in V

FAILURE DEFINITIONS: ICBO or IEBO in excess of 100 nA
 hFE values exceeding ±30%
 VCE(SAT) exceeding ±25%
 VBE(SAT) exceeding change of ±0.1 V

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 25

TOTAL NO. FAILURES 0

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.125	0.151	0.255	0.448	1.22	4.29	7.87
2	0	0	0.006	0.029	0.252	2.59	4.17
3	-0.015	-0.005	0.004	0.009	0.03	0.05	0.102
4	-0.005	0.001	0.007	0.01	0.018	0.028	0.048
5	-0.052	-0.039	-0.019	0.003	0.06	0.086	0.109
6	-0.056	-0.045	-0.036	-0.022	-0.006	0.011	0.024
7	-0.006	-0.005	-0.005	-0.005	-0.004	-0.004	-0.003

CONTROL GROUP WITHOUT

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 25

TOTAL NO. FAILURES 0

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.071	0.099	0.099	0.123	0.363	0.547	1.02
2	0.002	0.005	0.008	0.011	0.014	0.019	0.18
3	-0.061	-0.051	-0.03	-0.022	-0.014	-0.005	0.09
4	-0.039	-0.034	-0.019	-0.014	-0.009	-0.003	0
5	-0.092	-0.067	-0.033	0.019	0.043	0.065	0.095
6	-0.058	-0.043	-0.034	-0.019	0	0.018	0.032
7	-0.008	-0.006	-0.005	-0.005	-0.004	-0.004	-0.004

Figure 54 PNP Summary Statistics After Temperature Cycling Stress

COMPUTERIZED STABILITY SUMMARY STATISTICS
 AFTER 30 CYCLES OF TEMPERATURE - HUMIDITY CYCLING
 MIL-STD-202, METHOD 106B
 WITH APPLIED BIAS OF $V_{CEO} = 20V$

LOT 7010
 Phase I-PNP

DEFINITION OF PARAMETERS

- PAR 1 Arithmetic Change of I_{CBO} @ 30 V in nA
 PAR 2 " " of I_{EBO} @ 4 V in nA
 PAR 3 Percent Change (values shown x 100) of h_{FE} @ .1 mA, 2 V
 PAR 4 " " " of h_{FE} @ 2 mA, 2 V
 PAR 5 " " " of h_{FE} @ 150 mA, 2 V
 PAR 6 " " " of $V_{CE(SAT)}$ @ 150 mA, 15 mA
 PAR 7 Arithmetic Change of $V_{BE(SAT)}$ @ 150 mA, 15 mA in V

FAILURE DEFINITIONS: I_{CBO} or I_{EBO} in excess of 100 nA
 h_{FE} values exceeding $\pm 30\%$
 $V_{CE(SAT)}$ exceeding $\pm 25\%$
 $V_{BE(SAT)}$ exceeding change of ± 0.1 V

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER LOT SAMPLE 25

TOTAL NO. FAILURES 0

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PTCL	MAX VAL
1	0.17	0.214	0.339	0.533	0.728	1.56	5.22
2	0.001	0.003	0.007	0.018	2.933	7.615	44.7
3	-0.118	-0.085	-0.03	-0.015	-0.005	0.029	0.037
4	-0.047	-0.037	-0.023	-0.011	-0.007	0.018	0.027
5	-0.097	-0.08	-0.07	-0.05	-0.041	-0.015	0.005
6	-0.114	-0.109	-0.029	-0.023	-0.011	-0.007	0
7	-0.028	-0.012	-0.007	-0.005	-0.005	-0.004	-0.004

CONTROL GROUP WITHOUT

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER LOT SAMPLE 25

TOTAL NO. FAILURES 0

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PTCL	MAX VAL
1	0.089	0.094	0.104	0.168	0.431	2.03	16.1
2	0	0.002	0.006	0.052	0.222	0.565	2.35
3	-0.035	-0.026	0	0.013	0.018	0.033	0.041
4	-0.074	-0.041	-0.023	-0.012	-0.009	0	0.009
5	-0.214	-0.15	-0.112	-0.09	-0.067	-0.047	-0.008
6	-0.049	-0.043	-0.038	-0.031	-0.025	-0.016	0.125
7	-0.008	-0.008	-0.008	-0.005	-0.005	-0.005	-0.001

Figure 55 PNP Summary Statistics After Humidity Cycling With Bias

COMPUTERIZED STABILITY SUMMARY STATISTICS

NPN LOT 1014
PHASE I

AFTER 7500 HOURS OF HUMIDITY LIFE (85°C - 85% RH)

DEFINITION OF PARAMETERS

- PAR 1 Arithmetic Change of ICBO @ 30 V in nA
- PAR 2 " " of IEBO @ 4 V in nA
- PAR 3 Percent Change (values shown x 100) of hFE @ .1 mA, 2 V
- PAR 4 " " " of hFE @ 2 mA, 2 V
- PAR 5 " " " of hFE @ 150 mA, 2 V
- PAR 6 " " " of VCE(SAT) @ 150 mA, 15 mA
- PAR 7 Arithmetic Change of VBE(SAT) @ 150 mA, 15 mA in V

FAILURE DEFINITIONS: ICBO or IEBO in excess of 100 nA
hFE values exceeding ±30%
VCE(SAT) exceeding ±25%
VBE(SAT) exceeding change of ±0.1 V

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 25

TOTAL NO. FAILURES III

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.132	0.145	0.168	0.251	0.313	0.378	0.772
2	1.63	2.175	2.395	5.7	10.655	13.8	32.7
3	-0.18	-0.039	0.014	0.061	0.136	0.232	0.408
4	-0.175	-0.02	0.029	0.077	0.161	0.245	0.422
5	-0.244	-0.077	-0.048	-0.006	0.09	0.13	0.18
6	-0.045	-0.041	-0.011	0	0.06	0.098	0.179
7	0	0.001	0.003	0.004	0.008	0.014	0.033

CONTROL GROUP WITHOUT

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 25

TOTAL NO. FAILURES 2

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.026	0.123	0.138	0.194	0.281	7.36	4668.19
2	0.315	0.362	0.639	1.995	3.483	4.65	34
3	-0.018	0.059	0.137	0.165	0.212	0.247	0.259
4	-0.381	-0.024	0.111	0.13	0.151	0.189	0.228
5	-0.293	-0.238	-0.21	-0.174	-0.094	-0.071	-0.036
6	-0.064	-0.021	-0.01	0.007	0.037	0.066	0.159
7	-0.002	-0.001	0	0.002	0.006	0.007	0.008

Figure 56 NPN Summary Statistics After 7500 Hours, Humidity Life

COMPUTERIZED STABILITY SUMMARY STATISTICS

LOT 7010
Phase I-PRP

AFTER 1000 HOURS OF HUMIDITY LIFE (85°C - 85% RH)

DEFINITION OF PARAMETERS

PAR 1 Arithmetic Change of ICBO @ 30 V in nA
 PAR 2 " " of IEBO @ 4 V in nA
 PAR 3 Percent Change (values shown x 100) of hFE @ .1 mA, 2 V
 PAR 4 " " " of hFE @ 2 mA, 2 V
 PAR 5 " " " of hFE @ 150 mA, 2 V
 PAR 6 " " " of VCE(SAT) @ 150 mA, 15 mA
 PAR 7 Arithmetic Change of VBE(SAT) @ 150 mA, 15 mA in V

FAILURE DEFINITIONS: ICBO or IEBO in excess of 100 nA
 hFE values exceeding ±30%
 VCE(SAT) exceeding ±25%
 VBE(SAT) exceeding change of ±0.1 V

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 25

TOTAL NO. FAILURES 4

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.215	0.229	0.298	0.472	0.951	1.925	12
2	0.031	0.048	0.067	0.087	0.166	1.223	147.995
3	-0.103	-0.097	-0.085	-0.072	-0.044	-0.023	0.067
4	-0.031	-0.019	-0.013	0	0.016	0.032	0.049
5	-0.081	-0.063	-0.051	-0.039	-0.021	-0.01	0.005
6	0.005	0.022	0.038	0.033	0.157	0.199	0.404
7	-0.007	-0.007	-0.007	-0.006	-0.004	-0.003	0.019

CONTROL GROUP WITHOUT

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 25

TOTAL NO. FAILURES 19

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.511	0.856	2.667	5.29	19.25	27.6	52298.2
2	0.81	1.87	4.07	7.715	13.325	22.5	34.2
3	-0.496	-0.495	-0.471	-0.339	-0.274	-0.256	-0.235
4	-0.275	-0.27	-0.254	-0.171	-0.123	-0.109	-0.102
5	-0.224	-0.143	-0.122	-0.092	-0.071	-0.05	-0.041
6	-0.319	0.008	0.043	0.126	0.204	0.251	0.279
7	-0.009	-0.009	-0.008	-0.008	-0.007	-0.007	0.015

Figure 57 PNP Summary Statistics After 7500 Hours, Humidity Life

COMPUTERIZED STABILITY SUMMARY STATISTICS
 AFTER 5000 HOURS OF HUMIDITY LIFE (85°C - 85% RH)
 WITH APPLIED BIAS OF V_{CE0} = 20V

LOT 1014
 NPN

DEFINITION OF PARAMETERS

- PAR 1 Arithmetic Change of I_{CBO} @ 30 V in nA
- PAR 2 " " of I_{EBO} @ 4 V in nA
- PAR 3 Percent Change (values shown x 100) of h_{FE} @ .1 mA, 2 V
- PAR 4 " " " of h_{FE} @ 2 mA, 2 V
- PAR 5 " " " of h_{FE} @ 150 mA, 2 V
- PAR 6 " " " of V_{CE}(SAT) @ 150 mA, 15 mA
- PAR 7 Arithmetic Change of V_{BE}(SAT) @ 150 mA, 15 mA in V

FAILURE DEFINITIONS: I_{CBO} or I_{EBO} in excess of 100 nA
 h_{FE} values exceeding ±30%
 V_{CE}(SAT) exceeding ±25%
 V_{BE}(SAT) exceeding change of ±0.1 V

CLASSIFICATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 20

TOTAL NO. FAILURES 3

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.005	0.09	0.125	0.163	0.234	26.1	48099.9
2	0.96	1.43	2.65	3.52	6.84	14.3	16.5
3	0.032	0.04	0.05	0.113	0.140	0.24	0.252
4	0.042	0.042	0.063	0.119	0.149	0.228	0.239
5	-0.173	-0.172	-0.111	-0.073	-0.044	0.014	0.023
6	-0.062	-0.057	-0.048	-0.034	0.024	0.149	1.048
7	-0.006	0	0.004	0.005	0.007	0.022	0.023

CONTROL GROUP WITHOUT

CLASSIFICATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 10

TOTAL NO. FAILURES 2

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.068	0.063	0.084	0.117	0.125	0.136	0.139
2	0.227	0.227	0.269	0.419	0.537	0.564	2.65
3	0.092	0.092	0.104	0.123	0.133	0.143	0.157
4	0.07	0.07	0.072	0.075	0.101	0.154	0.172
5	-0.409	-0.409	-0.283	-0.232	-0.203	-0.155	-0.071
6	-0.041	-0.041	-0.034	-0.014	0.116	0.233	7.026
7	0.002	0.002	0.002	0.004	0.005	0.018	0.073

Figure 58 NPN Summary Statistics After 5000 Hours, Humidity Life With Bias, Lot 1014

COMPUTERIZED STABILITY SUMMARY STATISTICS

LOT 1021

AFTER 5000 HOURS OF HUMIDITY LIFE (85°C - 85% RH)

NPN

WITH APPLIED BIAS OF $V_{CBO} = 20V$

DEFINITION OF PARAMETERS

- PAR 1 Arithmetic Change of I_{CBO} @ 30 V in nA
- PAR 2 " " of I_{EBO} @ 4 V in nA
- PAR 3 Percent Change (values shown x 100) of h_{FE} @ .1 mA, 2 V
- PAR 4 " " " of h_{FE} @ 2 mA, 2 V
- PAR 5 " " " of h_{FE} @ 150 mA, 2 V
- PAR 6 " " " of $V_{CE(SAT)}$ @ 150 mA, 15 mA
- PAR 7 Arithmetic Change of $V_{BE(SAT)}$ @ 150 mA, 15 mA in V

FAILURE DEFINITIONS: I_{CBO} or I_{EBO} in excess of 100 nA
 h_{FE} values exceeding $\pm 30\%$
 $V_{CE(SAT)}$ exceeding $\pm 25\%$
 $V_{BE(SAT)}$ exceeding change of $\pm 0.1 V$

CLASSIFICATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 15

TOTAL NO. FAILURES 1

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.075	0.126	0.191	0.29	0.324	0.373	543000.
2	0.412	0.706	1.23	1.94	3.73	6.445	8.49
3	0.004	0.306	0.021	0.026	0.047	0.1	0.849
4	0.007	0.014	0.028	0.032	0.042	0.067	0.075
5	-0.236	-0.213	-0.154	-0.115	-0.093	-0.055	-0.049
6	-0.069	-0.059	-0.037	-0.03	-0.019	0.158	0.172
7	-0.001	-0.001	0.003	0.003	0.004	0.017	0.018

CONTROL GROUP WITHOUT

CLASSIFICATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 10

TOTAL NO. FAILURES 12

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.036	0.036	0.049	0.069	0.105	0.164	0.25
2	0.267	0.267	0.356	0.631	0.862	0.916	1.01
3	0.083	0.083	0.088	0.099	0.115	0.117	0.123
4	0.056	0.056	0.064	0.076	0.096	0.123	0.138
5	-0.375	-0.375	-0.307	-0.229	-0.203	-0.2	-0.118
6	-0.061	-0.061	-0.053	-0.043	-0.026	-0.012	0.145
7	0.002	0.002	0.001	0.004	0.004	0.005	0.005

Figure 59 NPN Summary Statistics After 5000 Hours, Humidity Life With Bias, Lot 1021

COMPUTERIZED STABILITY SUMMARY STATISTICS

LOT 1022
NPN

AFTER 5000 HOURS OF HUMIDITY LIFE (85°C - 85% RH)

WITH APPLIED BIAS OF $V_{CBO} = 20V$

DEFINITION OF PARAMETERS

- PAR 1 Arithmetic Change of I_{CBO} @ 30 V in nA
- PAR 2 " " of I_{EBO} @ 4 V in nA
- PAR 3 Percent Change (values shown x 100) of h_{FE} @ .1 mA, 2 V
- PAR 4 " " " of h_{FE} @ 2 mA, 2 V
- PAR 5 " " " of h_{FE} @ 150 mA, 2 V
- PAR 6 " " " of $V_{CE(SAT)}$ @ 150 mA, 15 mA
- PAR 7 Arithmetic Change of $V_{BE(SAT)}$ @ 150 mA, 15 mA in V

FAILURE DEFINITIONS: I_{CBO} or I_{EBO} in excess of 100 nA
 h_{FE} values exceeding $\pm 30\%$
 $V_{CE(SAT)}$ exceeding $\pm 25\%$
 $V_{BE(SAT)}$ exceeding change of $\pm 0.1 V$

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 15

TOTAL NO. FAILURES OF

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.145	0.158	0.213	0.269	0.349	1.18	29.7
2	0.122	0.467	0.939	1.63	2.502	6.09	17
3	-0.024	-0.003	0.028	0.041	0.053	0.061	0.069
4	0	0.012	0.035	0.05	0.063	0.069	0.146
5	-0.141	+0.136	-0.124	-0.097	-0.062	-0.01	0.033
6	-0.077	-0.064	-0.036	-0.033	-0.02	0	0.129
7	-0.003	-0.003	-0.002	0.001	0.003	0.004	0.004

CONTROL GROUP WITHOUT

GLASSIVATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER

LOT SAMPLE 10

TOTAL NO. FAILURES OF

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.086	0.086	0.11	0.268	0.376	0.4	0.532
2	0.349	0.349	0.823	1.37	2.495	4.04	859.39
3	0.079	0.079	0.09	0.093	0.126	0.157	0.169
4	0.059	0.059	0.076	0.092	0.119	0.135	0.137
5	-0.219	-0.219	-0.195	-0.106	-0.045	-0.029	-0.013
6	-0.043	-0.043	-0.04	-0.026	-0.014	-0.013	0.096
7	-0.006	-0.006	-0.005	-0.002	-0.002	-0.001	-0.001

Figure 60 NPN Summary Statistics After 5000 Hours, Humidity Life With Bias, Lot 1022

COMPUTERIZED STABILITY SUMMARY STATISTICS
 AFTER 572 HOURS OF SALT ATMOSPHERE
 ACCORDING TO MIL-STD-750, METHOD 1041.1

NPN TRANSISTOR
 LOTS 1014 & 1022

DEFINITION OF PARAMETERS

- PAR 1 Arithmetic Change of ICBO @ 30 V in nA
- PAR 2 " " of IEBO @ 4 V in nA
- PAR 3 Percent Change (values shown x 100) of hFE @ .1 mA, 2 V
- PAR 4 " " " of hFE @ 2 mA, 2 V
- PAR 5 " " " of hFE @ 150 mA, 2 V
- PAR 6 " " " of VCE(SAT) @ 150 mA, 15 mA
- PAR 7 Arithmetic Change of VBE(SAT) @ 150 mA, 15 mA in V

FAILURE DEFINITIONS: ICBO or IEBO in excess of 100 nA
 hFE values exceeding $\pm 30\%$
 VCE(SAT) exceeding $\pm 25\%$
 VBE(SAT) exceeding change of ± 0.1 V

CLASSIFICATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER LOT SAMPLE 30

TOTAL NO. FAILURES 10

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.13	0.14	0.174	0.219	0.287	0.332	0.518
2	0.228	0.671	1.335	2	3.605	8.8	34.2
3	-0.058	-0.049	-0.033	-0.018	-0.006	0.006	0.010
4	-0.045	-0.041	-0.022	-0.012	0	0.01	0.016
5	-0.143	-0.069	0.005	0.039	0.07	0.094	0.154
6	-0.02	0	0.055	0.067	0.082	0.134	0.188
7	-0.001	0.003	0.005	0.006	0.007	0.014	0.032

CONTROL GROUP WITHOUT
 CLASSIFICATION, REFRACTORY METAL WITH SILICON NITRIDE BARRIER LOT SAMPLE 30

TOTAL NO. FAILURES 12

PAR	LOW VAL	10 PCTL	25 PCTL	50 PCTL	75 PCTL	90 PCTL	MAX VAL
1	0.062	0.084	0.111	0.15	0.22	0.363	0.87
2	0.233	0.263	0.381	0.53	0.708	0.853	2.19
3	-0.056	-0.038	-0.036	-0.024	-0.018	0	0.005
4	-0.032	-0.031	-0.021	-0.018	-0.014	0	0.02
5	-0.337	-0.026	0.011	0.061	0.113	0.219	0.344
6	0.014	0.056	0.066	0.069	0.085	0.153	0.346
7	0.001	0.004	0.006	0.007	0.008	0.008	0.021

Figure 61 NPN Summary Statistics After Salt Atmosphere Stress

DEVICE PARAMETER RESPONSE

AFTER 312 HOURS OF EXPOSURE TO SUPERHEATED STEAM @ 35 PSIG - 20 NPN DEVICES PER TYPE

MEASURED PARAMETER	DEVICE TYPE	INITIAL MEAN VALUE	MEAN VALUE AFTER STRESS	CHANGE
V _{CE(sat)}	CONTRACT	84 mV	160 mV	1.9X
@ 150mA, 15mA	CONTROL	72 mV	570 mV	7.9X
V _{BE(sat)}	CONTRACT	806 mV	817 mV	1%
@ 150mA, 15mA	CONTROL	804 mV	1080 mV	34%

Figure 62 NPN Response After Superheated Steam Stress

ABSTRACT OF RESULTS OF TESTS					
PLANT NAME AND ADDRESS General Electric Company Semiconductor Products Dept. Bldg. 7., Electronics Park Syracuse, New York 13201		SPECIFICATION NUMBER MIL-S-19500E		TEST REPORT NUMBER 32DIR5318 - Lot 7122	
		AMENDMENT NUMBER 3		TEST REPORT DATE June 1971	
		DETAIL SPECIFICATION NUMBER First Article: Contract No. DAAB05-70-C-3109 Item 0003AB		PRODUCT	
TEST or GROUP	PAR. No.	No. TESTED	No. PASSED	No. FAILED	REMARKS
Group A					
Subgroup 1		614	595	19	
Subgroup 2		595	595	0	
Subgroup 3		595	595	0	
Subgroup 4		595	574	21	NF above max. limit
Subgroup 5		595	595	0	
Group B					
Subgroup 1		38	37	1	ϕ_e and e_1 below min. limit
Subgroup 2		52	52	0	
Subgroup 3		38	38	0	
Subgroup 4		52	51	1	IGBO end point reject
Subgroup 5		75	75	0	
Subgroup 6		52	52	0	
Group C					
Subgroup 1		25	25	0	
Subgroup 2		11	11	0	
Subgroup 3		18	18	0	
Subgroup 4		52	52	0	
					Observed MTPD/Lambda values and applicable acceptance numbers are outlined under "Sampling Procedure" included in the test description portion of this report.

DESC FORM 38F

Figure 63 NPN First Article Inspection, Summary Results (MIL-S-19500) (Continued)

Sampling Procedure

Sample sizes and acceptance criteria were observed in accordance with first article inspection levels of L/TPD or Lambda as follows:

<u>Group</u>	<u>Subgroup</u>	<u>L/TPD</u>	<u>Sample Size</u>	<u>Rejects Allowed</u>
A	1	10	614	50
A	2	5	595	22
A	3	10	595	49
A	4	10	595	49
A	5	15	595	78
B	1	10	38	1
B	2	10	52	2
B	3	10	38	1
B	4	10 (Lambda)	52	2
B	5	7 (Lambda)	75	2
B	6	10 (Lambda)	52	2
C	1	15	25	1
C	2	20	11	0
C	3	20	18	1
C	4	10	52	2

The quantity of units tested at Group A was sufficient to satisfy the subgroup sampling requirements prescribed for Groups B and C, and also the submission requirement of 100 additional units per Item 0003AB.

Figure 63 NPN First Article Inspection, Summary Results (MIL-S-19500) (Concluded)

ABSTRACT OF RESULTS OF TESTS					
PLANT NAME AND ADDRESS General Electric Company Semiconductor Products Dept., Bldg.7, Electronics Park Syracuse, New York 13201		SPECIFICATION NUMBER MIL-S-19500E		TEST REPORT NUMBER 34EXR1853 Lot 7205	
		AMENDMENT NUMBER 3		TEST REPORT DATE February 1972	
		DETAIL SPECIFICATION NUMBER First Article: Contract No. DAAB05-70-C-3109 Item 0003AA		PRODUCT	
TEST or GROUP	PAR. No.	No. TESTED	No. PASSED	No. FAILED	REMARKS
Group A					
Subgroup 1		519	513	0	
Subgroup 2		513	512	1 *	
Subgroup 3		513	513	0	
Subgroup 4		513	494	19 *	NF above max. limit
Subgroup 5		513	512	1 *	
					*Unit No.230 represented in each subgroup
Group B					
Subgroup 1		38	38	0	
Subgroup 2		52	52	0	
Subgroup 3		52	52	0	
Subgroup 4		65	63	2	ICBO and hfg shift
Subgroup 5		75	74	1	hfg shift
Subgroup 6		52	51	1	ICBO
Group C					
Subgroup 1		25	25	0	
Subgroup 2		11	11	0	
Subgroup 3		25	25	0	
Subgroup 4		52	52	0	
					Observed I_{MPD}/λ values and applicable acceptance numbers are outlined under "Sampling Procedure" included in the test description portion of this report.

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Figure 64 PNP First Article Inspection, Summary Results (MIL-S-19500) (Continued)

Sampling Procedure

Sample sizes and acceptance criteria were observed in accordance with first article inspection levels of LTPD or Lambda as follows:

<u>Group</u>	<u>Subgroup</u>	<u>LTPD</u>	<u>Sample Size</u>	<u>Rejects Allowed</u>
A	1	10	519	42
A	2	5	513	18
A	3	10	513	41
A	4	10	513	41
A	5	15	513	50
B	1	10	38	1
B	2	10	52	2
B	3	10	52	2
B	4	10 (Lambda)	65	3
B	5	7 (Lambda)	75	2
B	6	10 (Lambda)	52	2
C	1	15	25	1
C	2	20	11	0
C	3	20	25	2
C	4	10	52	2

The quantity of units tested at Group A was sufficient to satisfy the subgroup sampling requirements prescribed for Groups B and C, and also the submission requirement of 100 additional units per Item 0003AA.

Figure 64 PNP First Article Inspection, Summary Results (MIL-S-19500) (Concluded)

MILITARY LOT ACCEPTANCE TEST SUMMARY

PROPOSED

DETAIL SPECIFICATION: MIL-S-19500/
 GENERAL SPECIFICATION/AMEND.: MIL-S-19500B/3
 MIL DESIGNATION: 32DXR5318
 LOT NUMBER/DATE CODE: 7152
 LOT SIZE: 705
 COMPLETION DATE: 12-17-71

TEST GROUP	SUB GROUP	SAMPLING PLAN	SAMPLES TESTED	FAILURES ALLOWED	ACTUAL FAILURES	REMARKS
A	1	LTPD 10	52	2	1	
A	2	LTPD 5	105	2	0	
A	3	LTPD 10	52	2	0	
A	4	LTPD 10	52	2	0	
A	5	LTPD 15	34	2	0	
B	1	LTPD 10	38	1	2	See Note 1
B	2	LTPD 15	52	4	0	
B	3	LTPD 10	38	1	1	#2, hfg shift
B	4	Lambda 10	52	2	2	See Note 2
B	5	LTPD 7	75	2	0	1000 hours
B	6	LTPD 10	51	1	1	See Note 3

NOTES:

1. One of the 38 devices is .001" out of specification on only one dimension due to a slight misalignment in the mold. Corrective action has been taken to eliminate this in normal production.
2. Unit 44, IEBO end point reject. Unit 52, hfg shift rejects. 1000 hours.
3. Unit 48 was initial ICBO reject. Observed sample size and failures allowed reduced by one. Unit 11, IEBO end point reject.

GENERAL ELECTRIC SEMICONDUCTOR PRODUCTS DEPT. RELIABILITY PROGRAMS	NAME:	TITLE:	DATE:
	W.A. Whiteman	Reliability Specialist Q & RA	1-3-72

Figure 65 NPN Pilot Line Acceptance Test, Summary Results (MIL-S-19500)

MILITARY LOT ACCEPTANCE TEST SUMMARY

PROPOSED

DETAIL SPECIFICATION: MIL-S-19500/
 GENERAL SPECIFICATION/AMEND.: MIL-S-19500E/3
 MIL DESIGNATION: 34EXR1853
 LOT NUMBER/DATE CODE: 7219
 LOT SIZE: 1710
 COMPLETION DATE: 4-14-72

TEST GROUP	SUB GROUP	SAMPLING PLAN	SAMPLES TESTED	FAILURES ALLOWED	ACTUAL FAILURES	REMARKS
A	1	LTPD 10	356	28	0	
A	2	LTPD 5	356	12	3	
A	3	LTPD 10	356	28	0	
A	4	LTPD 10	356	28	2	
A	5	LTPD 15	356	43	0	
B	1	LTPD 10	38	1	1	
B	2	LTPD 10	38	1	0	
B	3	LTPD 10	22	0	0	
B	4	Lambda 10	65	3	0	1000 hrs.
B	5	Lambda 7	94	3	2	1000 hrs. bFE min. shift.
B	6	Lambda 10	52	2	0	1000 hrs.

NOTES:

GENERAL ELECTRIC SEMICONDUCTOR PRODUCTS DEPT. RELIABILITY PROGRAMS	NAME:	TITLE:	DATE:
	<i>W.A. Whiteman</i> W.A. Whiteman	Reliability Spec. Reliability Assurance	4-18-72

Figure 66 PNP Pilot Line Acceptance Test, Summary Results (MIL-S-19500)

SECTION VI

CONCLUSIONS AND RECOMMENDATIONS

The objectives of this program have been met. It was demonstrated that modifications could be made to the conventional planar passivated epitaxial structure that would enhance product performance and extend the capability of small signal NPN and PNP solid encapsulated transistors. Further it was demonstrated that these same transistors were capable of meeting the exacting performance requirements of military tests and application environments. A sound statistical and engineering test program was designed and implemented based on step-stress, bias moisture resistance, high temperature reverse bias life, and steady state operating life tests. Special emphasis in the test program was directed towards evaluating the devices under combinations of elevated temperature, humidity, steam pressure, operating power, temperature cycling and thermal shock. The purpose of these tests was to determine the short term stress margins above the normal maximum ratings as well as the long term (up to 7500 hour) endurance of the devices under humidity, temperature and operating life tests.

As a result of the Phase I Comprehensive Step-Stress and Special Test Program, the following can be concluded for the NPN and PNP contract devices:

- The contract devices were superior to the control devices on the high temperature step-stress with and without electrical bias up through 225°C.
- The contract devices were superior to the control devices on the operating power step-stress up through 1000 mW.
- The contract and control devices were similar on temperature cycling out to 400 cycles of -65 to +150°C with no catastrophic failures obtained.

- The contract devices were superior to the control devices after more than 100 hours of pressure cooker at 15 psig for the NPN devices and comparable for the PNP devices after 72 hours of pressure cooker.
- The contract devices were superior to the control devices on the 85°C, 85% RH environmental test out to 1000 hours. The NPN devices were stressed for 7,500 hours at 85°C, 85% RH which resulted in one out of twenty-five contract and two out of twenty-five control degradation failures.

The results from the long term performance test of Phase II of the test program on NPN devices demonstrated that:

- The contract devices were superior to the control devices under the 7,500 hour environmental tests of humidity with temperature cycling (MIL-STD-202 Method 106B) with applied power, and both device types demonstrated excellent performance under this environmental test with electrical bias.
- The contract devices were superior to the control devices under the 7,500 hour high temperature (175°C) with reverse bias tests.

The devices which received the precondition stress of pressure cooker at 15 psig had a higher failure rate during subsequent long term testing, demonstrating that this stress is destructive, and therefore, would not be recommended as a one hundred percent stress screen for reliability improvement.

Both NPN and PNP program devices were subjected to and passed MIL-S-19500E Group A, B and C test conditions.

In summary, the following significant results have been obtained on this program:

- Demonstration of a superior chip passivation seal,

- Extension of the operating temperature range to 175°C,
- Extension of the power dissipation range from 360 mW to 600 mW ratings,
- Demonstration of resistance to water vapor and temperature,
- Demonstration of parameter stability after accelerated testing,
- Demonstration that both NPN and PNP type transistors with the new passivation seal are capable of passing MIL-S-19500E Group B and C operating and environmental test conditions.

There is a continuing need to upgrade and increase product performance, even beyond what has been accomplished on this program. It is recommended that:

- Improved and higher temperature metalization systems be explored and implemented into the planar products. The system developed on this contract can be cost reduced and simplified and there have been some recent developments that indicate that this system can be further improved,
- A more effective glass to metal system should be explored. Thicker glass films with high integrity should be the objectives in future programs,
- There is need for higher temperature solid encapsulants. Theoretically, the devices can perform up to 250°C and the solid encapsulants should be capable of performing beyond this limit for extended periods of time,
- New and effective tests for detecting possible failure modes need to be developed and evaluated with the idea of obtaining superior products that meet the exacting military environmental tests.

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13. ABSTRACT This is the final documentary report of a Production Engineering Measure program for improving the reliability and performance of solid encapsulated semiconductor devices to meet the rigorous requirements of military application environments. Small signal NPN and PNP transistors were the vehicles used. Basic changes in the semiconductor structure were made on these devices to enhance the performance of the products and to improve the capability of solid encapsulated transistors. The topological structure was based on a clean thermal oxide, a pyrolytic silicon nitride barrier, refractory metalization and a glass coating over the entire structure. The refractory metalization system was a platinum silicide/molybdenum/gold laminar structure that was capable of withstanding the high temperatures associated with the glassivation process. This system provided good ohmic contacts to both the N and P regions of the transistors. As result of these features, device stability was enhanced by preventing the migration of contaminating ions to the silicon surface. The glassivation prevented metalization corrosion and in addition provided complete chip passivation. Over 10,000 transistors were fabricated for evaluation and test purposes to assess product performance. The contract units in every case were compared to control structures manufactured at the same time and in the same system where possible. A sound statistical test program was designed and implemented based on step-stress, bias moisture resistance, high temperature reverse bias life, and steady state operating life tests. It was conclusively proved that a superior product has been achieved that was capable of meeting the severe military requirements.		

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14	KEY WORDS	LINK A		LINK B		LINK C	
		ROLE	WT	ROLE	WT	ROLE	WT
	NPN Transistor PNP Transistor Silicon Nitride Barrier Refractory Metal Contact System Glassivation Reliability Improvement Plastic Encapsulation Solid Encapsulation						

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