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RADC-TR- 66-775
Final Report

FABRICATION AND TESTING OF 5000 WORD CRYOGENIC ASSOCIATIVE PROCESSOR

J. Paul Pritchard, Jr.
Texas Instruments Incorporated

TECHNICAL REPORT NO. RADC-TR- 66-775
February 1967

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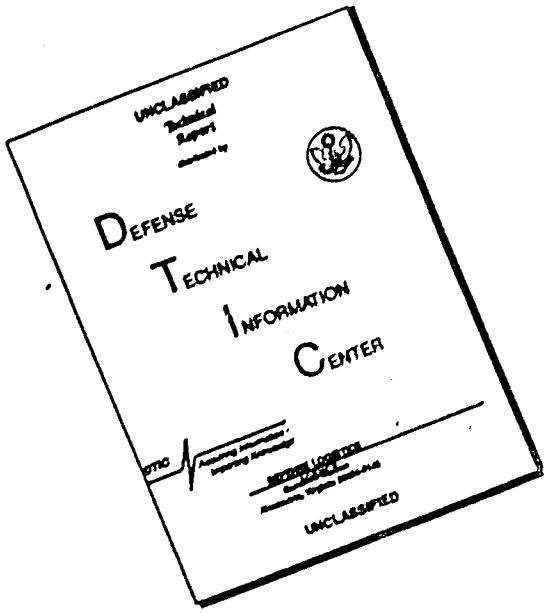

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FOREWORD

This report was prepared by Texas Instruments Incorporated, Dallas, Texas, under contract AF 30(602)-3737, Project 5581, Task 558108. The secondary report number is 08-66-143. This is the final report for contract AF 30(602)-3737 and covers the period 10 May 1965 through 10 October 1966. The RADC project engineer was Mr. James Previte (EMIIO).

At Texas Instruments the contract effort was carried out principally in the Advanced Components Research Laboratory, a part of the Central Research Laboratories. Dr. J. Paul Pritchard, Jr., was program manager. Principal contributors to the work reported here were Mr. Joe T. Pierce, Mr. B. G. Slay, Mr. A. D. Stephenson, Jr. and Mr. L. D. Wald.

This document contains information embargoed from release to Sino-Soviet Bloc Countries by AFR 400-10, "Strategic Trade Control Program."

This report has been reviewed and is approved.

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ABSTRACT

This engineering research program, undertaken to construct a 5000 word cryogenic associative data processor, achieved its intermediate objectives concerning identification and solution of technical limitations for large capacity array fabrication, interconnection, data linkage, and packaging. Successful methods for fabricating 2.0 inch x 2.25 inch arrays having 40-word, 2000-cell (11,000 cryotrons) capacities resulted in seven operable arrays by the end of the program. Between 126 and 144 such arrays would provide the 5000 word objective. Fault-tolerant system operation permits use of arrays containing failed word(s). Array interconnection via superconducting, flexible, strip transmission line in pressure-actuated contact with thin film array contacts was successfully used throughout the contract, as were preferred data linkage means. Design concepts for packaging the multiple-array system were accomplished, and the interface electronic functions to permit on-line operation with a Univac 1218(M) computer were specified. Because solution of array fabrication problems consumed most of the contract period, fabrication of the full complement of arrays was not possible. An engineering development program is recommended for construction of the 5000 word cryogenic associative processor.

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SECTION I
INTRODUCTION

The data processing objective of this program has been an experimental model of a 5000-word cryogenic associative processor which could be used in conjunction with a Univac 1218-M computer installation at RADC.* A 50-bit fixed word length was selected for the application. Basic operational capabilities include:

(1) variable field masking of search and write operations;

(2) selective write with respect to one or more words simultaneously and in bit-parallel;

(3) destructive and nondestructive read in bit-parallel;

(4) explicit "1"-"0" read of multiple words for algorithmic convenience, in bit-parallel;

(5) bit-parallel search for equality;

(6) logical connective operation between scratch-pad and history registers for Lewin algorithm search with respect to magnitude, extremum, between limits, and nearest value;

(7) write with respect to a marker bit in conjunction with read operations; and

(8) insensitivity to presence of failed words through fault-tolerant operating mode.

The technological objectives of this program have been to determine:

(1) the adequacy of existing technology to accomplish a large capacity cryogenic associative processor;

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* The original contract specification of CDC 16048 computer compatibility was changed by RADC in the course of the contract.

(2) the origin and severity of any technological limitations encountered;

(3) performance characteristics of cryotron circuitry at prototype complexity required by economic considerations; and, if totally successful,

(4) usefulness of associative processing by programmer utilization and evaluation of the assembled processor.

The cryogenic and room-temperature equipment functions were organized to facilitate performance evaluation of the cryogenic subsystem for the experimental model. The computer, therefore, serves as an exerciser under variable rather than fixed program control. In fact, the cryogenic portion of the experimental model is unaffected by the choice of controlling computer.

An 11,000-cryotron array, 2.0 inch x 2.25 inch and containing 40 words of 50 bits each and associated word control circuitry, is the desired unit of array manufacture. An assemblage of at least 126 such arrays provides the 5000-word processor objective; 117 data and control signal paths thread through all words in the cryogenic arrays. Arrays are interconnected by 117-conductor flexible strip transmission line; superconductive contact is made by pressure actuation at all low-temperature junctions.

The first operable, large area array was achieved in the fifteenth program month after solutions had been found for an unanticipated number of technological problems. The problems stemmed primarily from an inadequate state of the art in preparation and use of sets of large area photomasks, and from a film rupture phenomenon undetected in small capacity array fabrication. In the final two months of the program four arrays were made operable for fault-tolerant processor use with 50-bit word length, and three other arrays for at least 45-bit word length. Five others were structurally acceptable, but had depressed critical currents as a result of thin Sn layers.

Array interconnection, data linkage, and 300°K signal conditioning were provided without major technical difficulty, except for pulse read-out from

the cryogenic circuitry. Late in the program, a balanced-bridge read scheme was used successfully in limited experiments.

The design concepts for assembly, packaging, and signal conditioning for on-line computer use of the 5000-word processor are generally described, but final design and construction have been deferred.

SECTION II

CRYOGENIC ASSOCIATIVE MEMORY (CAM) FUNCTION

A. General Information

The experimental model of the cryogenic associative data processor (ADP) is intended primarily as a means of establishing feasibility of this new technology. A processor capacity of 5000 words (250,000 bits) was determined by both projected economic considerations of the technology and the storage desires of potential users if an operational system should result from the program. It has been estimated that cryotron associative memories must have a minimum capacity of 10^6 bits to absorb the base cost of liquid helium refrigeration. From the alternative, or user's viewpoint, an associative processor represents a unique tool whose potential worth can best be established through experience with prototype hardware of large storage capacity. It is believed that the results obtained from this program should relate directly to systems of potentially practical capacity on both counts.

The following material describes the specific organization and logic design of the cryotron circuitry. The available algorithmic means for accomplishing varied complex searches, and the manner in which the cryogenic ADP will be related to the Univac 1218-M with respect to flow of control and data signals, are treated in Section IV.E. The TI-ADP will be electronically compatible with the switching interface between the 1218-M and a search memory unit being supplied to RADC by the Goodyear Corporation. This compatibility, however, does not extend to the 1218-M software required at the machine language level.

Figure 1 shows the relationship of the ADP to the Univac 1218-M when operation of the cryogenic ADP is intended. The signal conditioning interface of the ADP will be electronically identical to that of the Goodyear associative memory unit with respect to both number of I/O paths and signal characteristics. (Note that this does not imply identical usage of these I/O paths.)

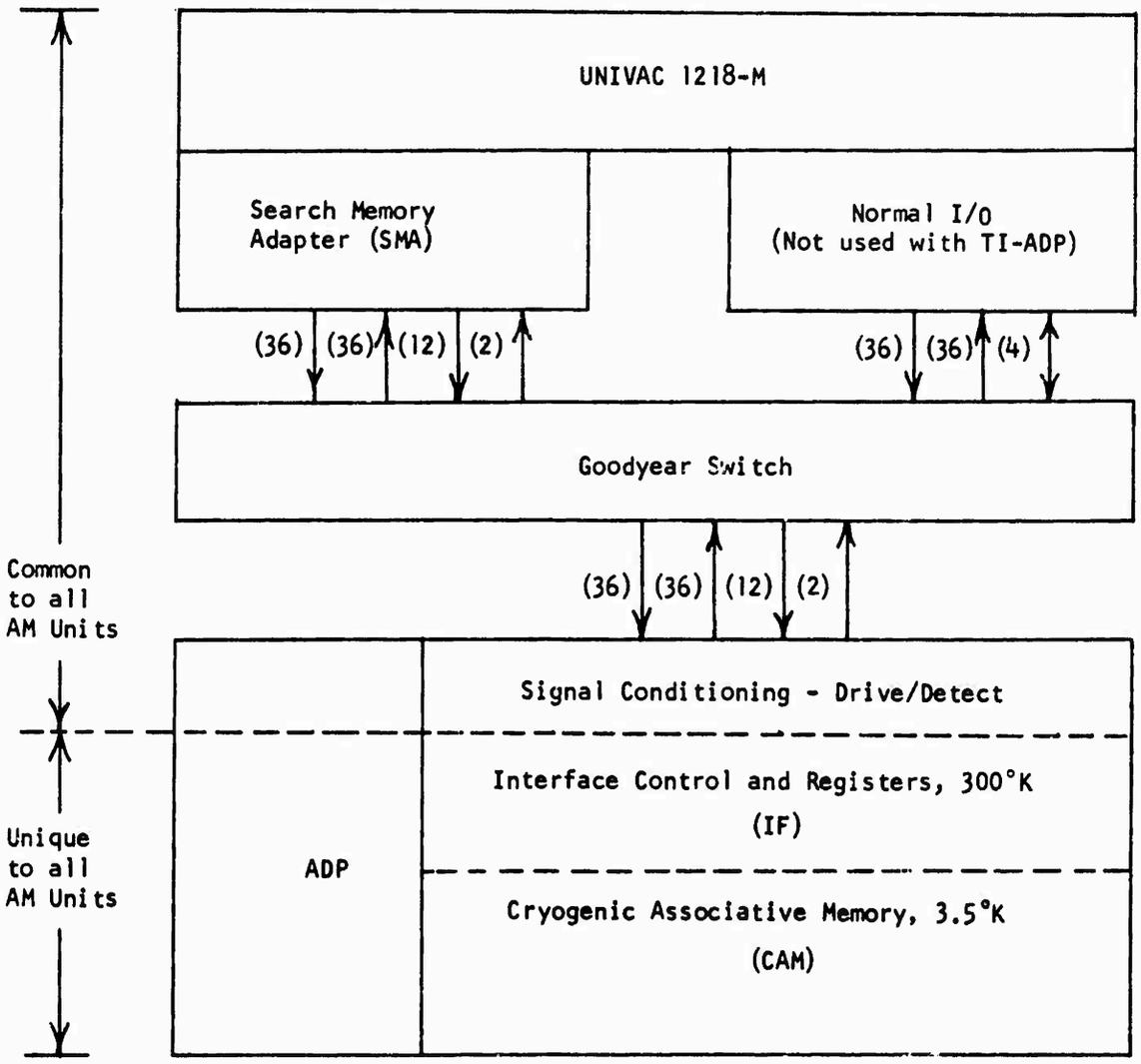


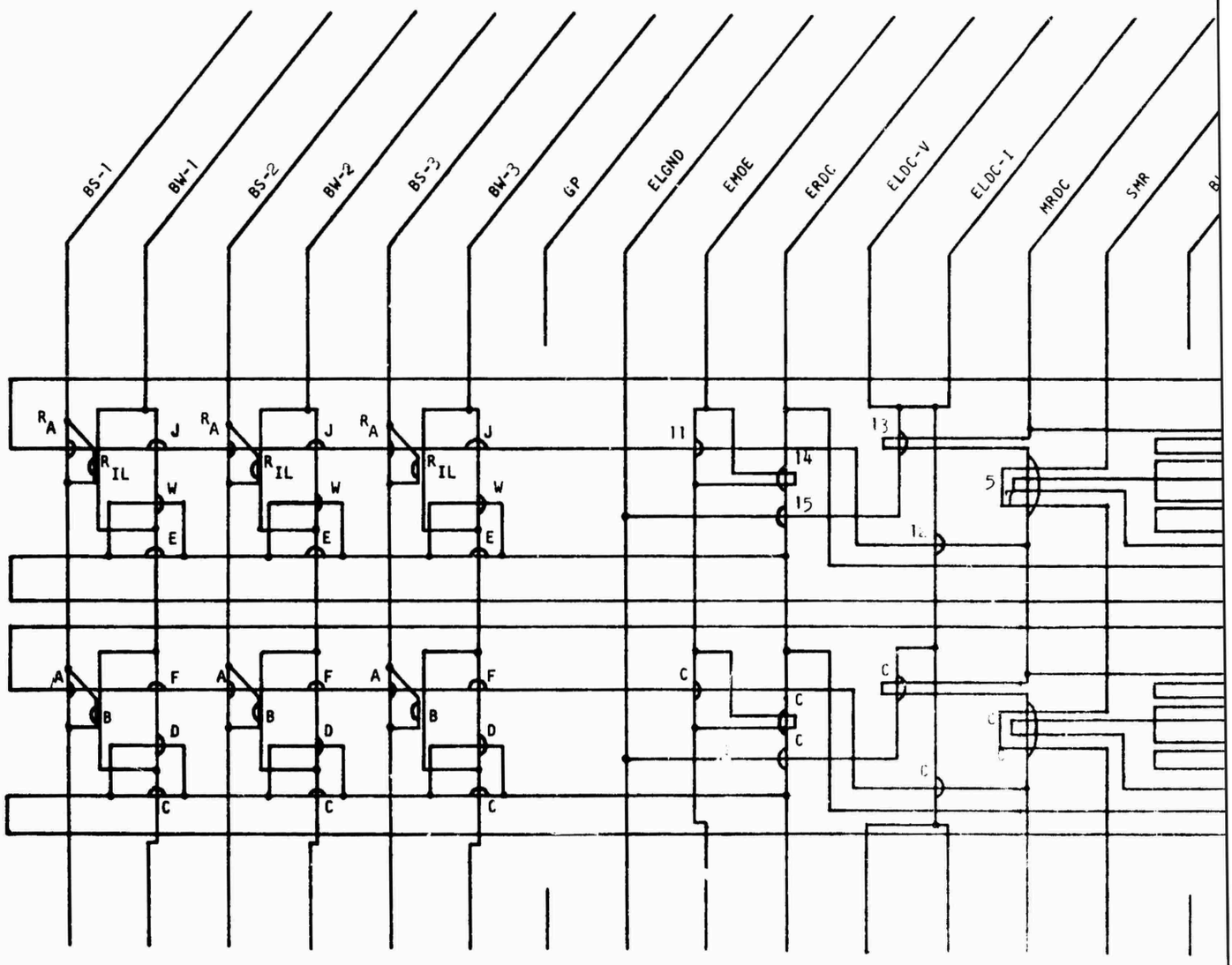
Figure 1 ADP relationship to Univac 1218-M via Goodyear Switch

The subsystems unique to the ADP are the Interface Control and Registers (IF) and the Cryogenic Associative Memory (CAM). The IF consists of suitably coupled registers to manipulate mask, argument, and instruction data; CAM instruction decoder, controller, and clock; and CAM drivers and sense amplifiers. The CAM consists of the cryotron, word-organized associative cells and word control circuitry, all maintained at a temperature of 3.5°K in a liquid helium bath.

The CAM subsystem contains the devices whose feasibility is under study, and it will become apparent that the IF organization effectively replaces CAM tester and exerciser equipment by the 1218-M computer. Subroutines provided for the 1218-M will generate the microinstructions and IF register contents directly meaningful to the CAM. This will permit maximum access to the CAM for device test and evaluation purposes. Although this approach will be suboptimum with respect to data processing rate under any given set of algorithms for associative search, a variety of search capabilities and algorithms may be evaluated by providing appropriate 1218-M subroutines. An optimum IF organization can be determined from experience with the software controlled simulations, as can the operational characteristics of subsequently proposed hardware.

B. Description of CAM Operation

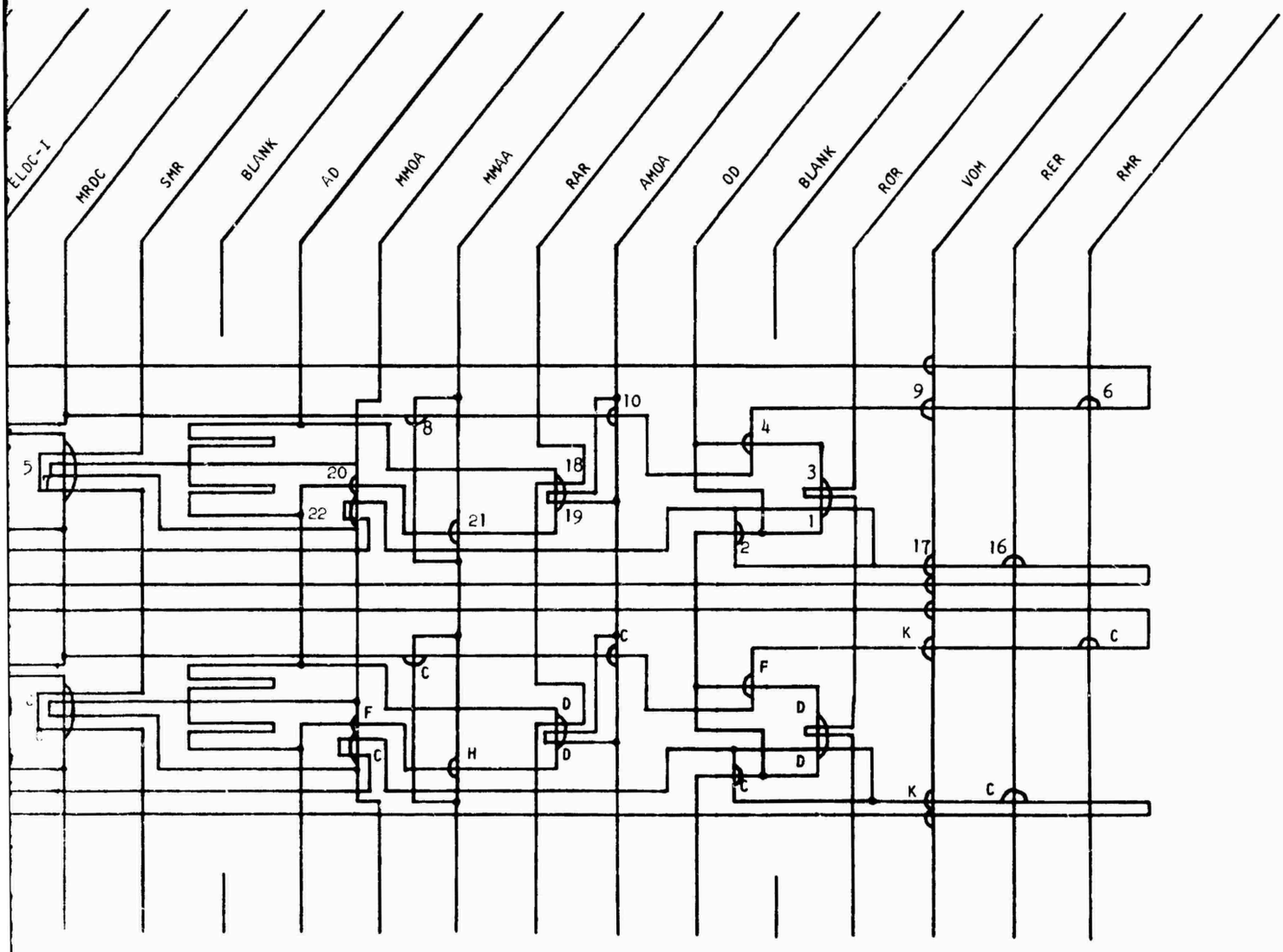
The CAM consists of 5000 words of 50 associative storage cells each. The cells are word-organized, i.e., they may be linearly selected to enable read, write, and search operations by word. The control circuitry is formed simultaneously with the cells and interconnections of the multiple layer, thin film cryotron circuitry. Each word consists of 50 associative storage cells, a Match Register (MR) flip-flop, an Enable Register (ER) flip-flop, an Occupancy Register (OR) cell (binary), an Action Register (AR) cell (ternary), an Enable Ladder (EL) "rung", and suitable control means to produce the desired interactions. Data input (50) and output (50) paths thread all words in memory in bit-parallel, as also the control means with respect to word control circuitry (17). These 117 paths are externally driven or sensed by electronic provisions at room temperature. Figure 2 is a diagram of the cryotron circuitry for two words of three bits each with appended word control circuitry. The controlled



$w_c \times w_g$ - Type Cryotron

(A) 1.5 x 1.5 MIL CFC
(B) 2.5 x 1.5 MIL IN LINE
(C) 1.5 x 7.0 MIL CFC
(D) 1.5 x 11.0 MIL CFC
(F) 2.0 x 7.0 MIL CFC
(H) 1.0 x 7.0 MIL CFC
(K) 1.5 x 2.0 MIL CFC

Figure 2 [illegible]



circuitry for CAM
words of three bits each

2

gate of a crossed film cryotron (CFC) is represented as a semicircle tangent to its series path. Only those lines which intersect a semicircle exert control on gate resistance. The gate type labeled R_{IL} is an in-line cryotron controlled by the storage loop branch shown paralleling its gate. The gates have been assigned an alphanumeric reference in the upper word of Figure 2; in the lower word they are assigned an alphabetical character to describe their crossing ratio (gain characteristic), as shown in key of Figure 2.

C. Microinstruction Complement for CAM Operation

The Cryogenic Associative Memory (CAM) may be controlled for test, exercise, or prototype operation by specification of Mask and Argument data in the 50-bit C and M registers, and a 12-bit operation code in the IFI register of the IF (see Section IV.E). The CAM operation code will hereafter be referred to as the microinstruction.

In brief, the CAM reflects a "wired-in" capability to selectively write and read (DRO/NDRO) 50-bit words which are selected by appropriate associative search procedures. Word occupancy is determined by the storage state (vacant/occupied) of an additional cell within each word's Word Control Circuitry (WCC). Equality search is parallel-by-word and is determined only for the bit positions designated as unmasked in the M register, and for these it is relative to the state of the corresponding C register bit positions. The WCC of each word contains both a Match Register (MR) flip-flop and an Enable Register (ER) flip-flop. The MR flip-flop is set to the Match (M) condition in words to be searched, then reset to $\overline{M}$ in words which are mismatched; i.e., a word is potentially matched until proven mismatched. The M state of an MR flip-flop also enables read-out from its word. The ER flip-flop enables only writing in its word; within the word, only those cells for which a BW current drive is imposed are affected with respect to storage state, and thus the selective write feature.

The MR flip-flops effectively constitute a scratch-pad register. Complementing these are ternary Action Register (AR) cells, one for each word within the WCC circuitry. The AR effectively retains the past history of

sequences of equality searches. Its state may influence or be influenced by the MR through a variety of logical connectives, effective also within the WCC circuitry of each word. The three possible states for an AR cell are A, $\overline{A}$, and Ø (Null). An alternative use of the AR provides fault-tolerant operation, as described in Section IV.B.

An Enable Ladder (EL) is included within the WCC circuitry to permit initial loading of the CAM. The ability to sequentially activate words in memory is the only hardware provision for distinguishing between words on other than a stored data basis. Although the ladder seemingly provides a convenient means of identifying "first empty word" when fresh data is to be entered, its time constants make such use generally unattractive. The EL is preferred as a sequencing mode for initial loading of unique addresses to be allocated to serviceable words in memory. Thereafter, "first empty word" is algorithmically determined.

One cycle time of the CAM is required to accomplish the specified CAM microinstruction. Within this cycle time up to six clock phases are executed; the precise number is determined by the particular microinstruction specified.

The microinstruction conveys the control information necessary to specify:

(1) method of identifying initial search set of words,

(2) occupancy status constraint to be imposed with respect to search execution,

(3) an input/output operation with respect to search-identified words,

(4) method of conditionally effecting the search-history record for words.

The microinstruction is executed in the time sequence implied by the order of control information stated above. In terms of the cryogenic registers involved, the above statements affect:

(1) one of eight ways in which the MR flip-flops (scratch-pad) can be initially set to M state,

(2) one of four occupancy states which must apply to permit the M state to exist after search with respect to mask-argument data specification,

(3) one of sixteen input/output variations,

(4) one of eight ways in which the AR ternary cell (search history for word) is to be conditioned as a result of the final state of the MR flip-flop in each word.

Table I summarizes the microinstruction complement and the pulse sequences to the CAM occasioned for each.

D. Extended Search Capability

The variety of search criteria is extended to include Magnitude ($\gtrless$), Between Limits, Extrema (max./min.), and Nearest (>,<) by sequential interrogation of the associative memory under appropriate algorithmic control. Bit serial algorithms require the least modification of Mask and Argument Registers during search, but they require a maximum of memory accesses. Conversely, the bit-parallel algorithms require variability of Mask and Argument Registers during search, but minimum memory accesses.

The ADP will receive algorithmic control from software subroutines stored in the Univac 1218-M; therefore, minimum complexity will be required in the interface electronics. This will necessarily reduce the efficiency of system use because of the increased time spent in transmitting data and control information between 1218-M and ADP. The disadvantage will be offset by increased flexibility in evaluation of alternative usage of the ADP through 1218-M subroutine modification rather than expensive interface hardware modification.

TABLE I

CAM MICROINSTRUCTION COMPLEMENT AND PULSE TIMING DIAGRAMS

Note: A 12-bit microinstruction is provided to the Interface (IF) of the ADP for CAM control. The 12 bits consist of an α-aspect (b.p. P,Q,1,2) to specify input/output operations, a β-aspect (b.p. 3,4) to define searched-word status, a γ-aspect (b.p. 5,6,7) to define initial search set, and a δ-aspect (b.p. 8,9,10) to define recording of search results in history register.

TABLE I

α - Aspect

Operation:	Bits P Q 1 2	Phase	Pulses Required φ22	φ23
ALL	* † - -	EMOE/ELP	W_1/W_9	
		MES	D_4 W_8	
		RER		W_5
No I/O Action	* - 0 0		No additional pulses	
Write	* - 0 1	BW, OD(Occ.)		W_4
		MMOAOE		W_5
NDRO	* † 1 0	RMR2	W_1	
		BSD(1/0)	W_3	W_3 OS_3
		BR(1/0)S	D_3 W_8 OS_3	D_3 W_8
		MMOAOE	W_1	W_5
		RMR1	W_1	
DRO	* † 1 1		Superimpose NDRO Sequence	
		OD(V-		W_4

* Note: If P = 0, EMOE of width W_1 occurs; if P = 1, ELP of width W_9 occurs.

† Note: If Q = 0, BSDO (neg.) and BROS will occur; if Q = 1, BRD1 (pos.) and BR1S.

Note: MES and BR(1/0)S are strobes relative to IF sense amplifiers.

TABLE I (continued)

F - Aspect

Operation:	Bits 3 4	Pulses Required Phase
No Search	0 0	No Pulses - Skip to φ_{22} if applicable
Search $\{\overline{M}_i \cdot BW_i\}$ for Vac.	0 1	BW, OD (Vac.)
Search $\{\overline{M}_i \cdot BW_i\}$ for Occ.	1 0	BW, OD (Occ.)
Search $\{\overline{M}_i \cdot BW_i\}$ independent of Occupancy Bit	1 1	BW

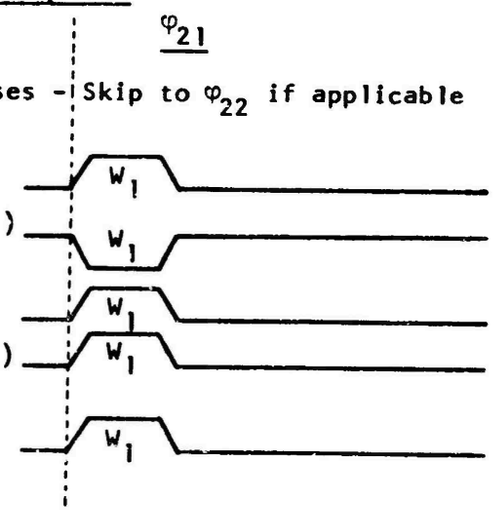


TABLE I (continued)

γ - Aspect

Operation:	Bits 5 6 7	Pulses Required Phase	φ_{11}	φ_{12}
$MR_o = MR$ (Leave MR as is)	0 0 0	No pulses - skip to φ_{21} if applicable		
$MR_o = 1$ (Set to M in all words)	0 0 1	SMR	W_1	Skip φ_{12}
$MR_o = AR(A)$ (Set to M for AR(A) words)	0 1 0	SMR	W_1	
		AD(A)		W_2
		MMAA		D_1 W_1
$MR_o = AR(\bar{A})$ (Set to M for $AR(\bar{A})$ words)	0 1 1	SMR	W_1	
		$AD(\bar{A})$		W_2
		MMAA		D_1 W_1
$MR_o = MR + AR(\bar{A})$ (Accumulate $AR(\bar{A})$ words to MR)	1 0 0	AD(A)	Skip φ_{11}	W_2
		MMOAOE		D_1 W_1
$MR_o = MR + AR(A)$ (Accumulate AR(A) words to MR)	1 0 1	$AD(\bar{A})$	Skip φ_{11}	W_2
		MMOAOE		D_1 W_1
$MR_o = MR \cdot AR(A)$ (Edit M to AR(A) words)	1 1 0	AD(A)	Skip φ_{11}	W_2
		MMAA		D_1 W_1
$MR_o = MR \cdot AR(\bar{A})$ (Edit M to $AR(\bar{A})$ words)	1 1 1	$AD(\bar{A})$	Skip φ_{11}	W_2
		MMAA		D_1 W_1

TABLE I (continued)

δ - Aspect

Operation:	Bits 8 9 10	Pulses Required Phase	φ_{23}	φ_{24}
$AR_F = AR$ (Leave AR as is)	0 0 0	No pulses - μ-instruction complete		execution
$AR_F = AR \cdot \overline{MR}$ (Edit $AR(A/\overline{A})$ by M state words)	0 0 1	AAOM	Skip φ_{23}	W_6
$AR(A)_F = AR(A) + MR$ (Accumulate M words to AR(A))	0 1 0	AD(A) AAOM	Skip φ_{23}	W_7 W_6
$AR(\overline{A})_F = AR(\overline{A}) + MR$ (Accumulate M words to $AR(\overline{A})$)	0 1 1	$AD(\overline{A})$ AAOM	Skip φ_{23}	W_7 W_6
$AR_F = 0$ (Set AR to Null state in all words)	1 0 0	RAR	W_5	Skip φ_{24}
* $AR_F = 0$ (Same as (100))	1 0 1	RAR AAOM	W_5	 W_6
$AR_F(A) = MR$ (Clears $AR(\overline{A})$, sets AR(A) for M words)	1 1 0	RAR AD(A) AAOM	W_5	 W_7 W_6
$AR_F(\overline{A}) = MR$ (Clears AR(A), sets $AR(\overline{A})$ for M words)	1 1 1	RAR $AD(\overline{A})$ AAOM	W_5	 W_7 W_6

* Unused code structured for convenience of exerciser logic.

E. CAM Circuit Operation

The following sections describe the operation of the major CAM circuit functions and methods of influencing their interactions.

1. Associative Cell

Figure 3 illustrates the associative storage and match circuitry for each cell. Storage is accomplished by producing a circulating current within the loop containing the W cryotron gate. The binary state of the argument to be written is conveyed as the polarity of the Bit Write (BW) drive current. Presence of this BW current affects the storage state only if the Enable (EN) line is active; thus, BW current controls gate E, which can divert EN current to control gate W. When EN and BW currents are released in that order, a fraction of BW current is trapped in the loop. If EN current is present in the absence of BW current, the cell's storage state is unaffected, and a selective write capability is provided.

The J cryotron appears serially in the Match (M) branch of a flip-flop spanning all cells of a word. If a mismatch of stored and interrogation states exists, the Exclusive Or is true and gate J is to be switched resistive, thereby causing reset of the M line current for the word. The interrogation state is expressed also as the polarity of the BW current drive during search time. Observe that if a match exists, stored and interrogation currents cancel in the J cryotron control, and conversely for a mismatch. Since stored current is continuously present, the J cryotron is designed to switch only in the case of a mismatch and not otherwise.

Read-out of the stored state is accomplished by coincidence of M current and Bit Sense (BS) drive current of a state corresponding to the stored data state. The result is that cryotron gates R_a and R_{IL} are simultaneously resistive, thus producing a voltage on the BS line. The M line, therefore, serves as a Read Enable line for word selection, and the stored state is inferred from the presence or absence of a voltage on the BS line in the presence of a known polarity of BS current.

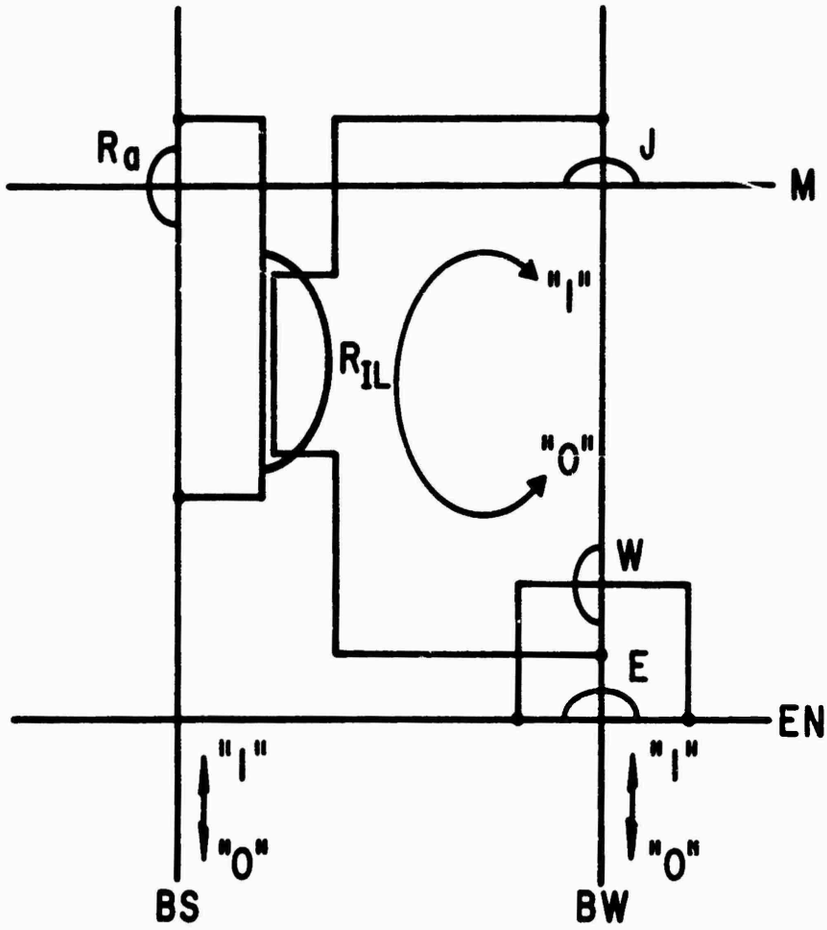


Figure 3 Associative cell circuitry (see Figure 2 for memory context)

2. Match Register

The Match Register (MR) is a serial arrangement of flip-flops, one for each word in memory (see Figure 4). The match status of a word before and after each search is indicated by the state of its MR flip-flop; thus, if a word is matched, MRDC current is diverted through the M path at this word, and conversely through path $\overline{M}$ if the word is mismatched. Supercurrent trapping in a MR flip-flop is not an intended mode of operation in the current ADP design.

The entire MR may be conditioned by memory controls Set MR (SMR) and Reset MR (RMR), all MR flip-flops terminating in the M or $\overline{M}$ conducting state, respectively.

A given MR flip-flop may be set to the M state only if the logical OR condition is satisfied with respect to the Action Register (AR), or with respect to the Enable Register (ER) in this word.

A given MR flip-flop may be reset to the $\overline{M}$ state by its associated word if:

(1) the Exclusive Or of stored and interrogated data is true at one or more storage sites in this word;

(2) the Exclusive Or of Occupancy Register (OR) states, stored and interrogated, is true in this word;

(3) the logical AND condition is not satisfied with respect to the AR.

A given MR flip-flop in its M state:

(1) enables read-out from storage sites in this word,

(2) enables modification of AR storage state,

(3) controls Enable Ladder (EL) current distribution in this word,

(4) enables setting of the Enable Register (ER) flip-flop for this word,

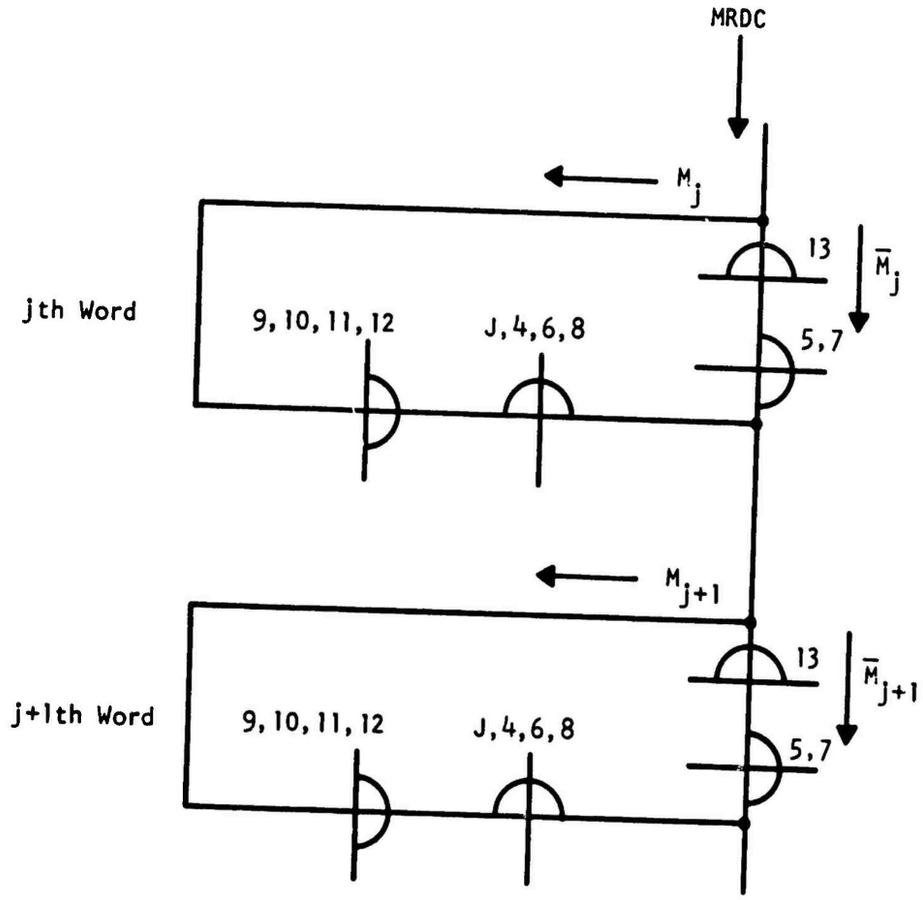


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Figure 4 Match Register relationship to cell and word control circuitry for two words. See Figure 2 for identification of alphanumerically designated cryotrons.

(5) controls a series gate in the Voltage On Match (VOM) line for the memory.

A given flip-flop in the $\overline{M}$ state controls only the EL current distribution in this word.

3. Enable Register

The Enable Register (ER) is a serial arrangement of flip-flops, one for each word in memory (see Figure 5). The primary function of the ER is to enable writing with respect to word storage sites and the OR in words in which the ERDC current has been diverted through the EN path. Supercurrent trapping in an ER flip-flop is not an intended mode of operation in the current ADP design.

The entire ER may be reset to $\overline{EN}$ state by memory control Reset ER (RER).

A given ER flip-flop may be set to the EN state by:

(1) Presence of the M state current at this word necessary to divert the memory control current EMOE (when present) through a high inductance path which controls cryotron 14. The inductive split is such that cryotron 14 is not switched resistive in a word for which the $\overline{M}$ state is true.

(2) Presence of current in the EL crossover branch for this word, thus switching cryotron 15 resistive. This provision is used only for initial word address assignment.

A given ER flip-flop in the EN state controls a series gate in the VOM line for the memory.

The EN branch of a given ER flip-flop is locally subjected to switching action at the storage sites and OR cell in the act of writing. However, each such switched gate is shunted by a superconducting path at its storage or OR site. In the worst case of all storage sites and the OR cell being simultaneously written into, the inductance of the ER flip-flop retards significant degradation of the EN current in normal operation.

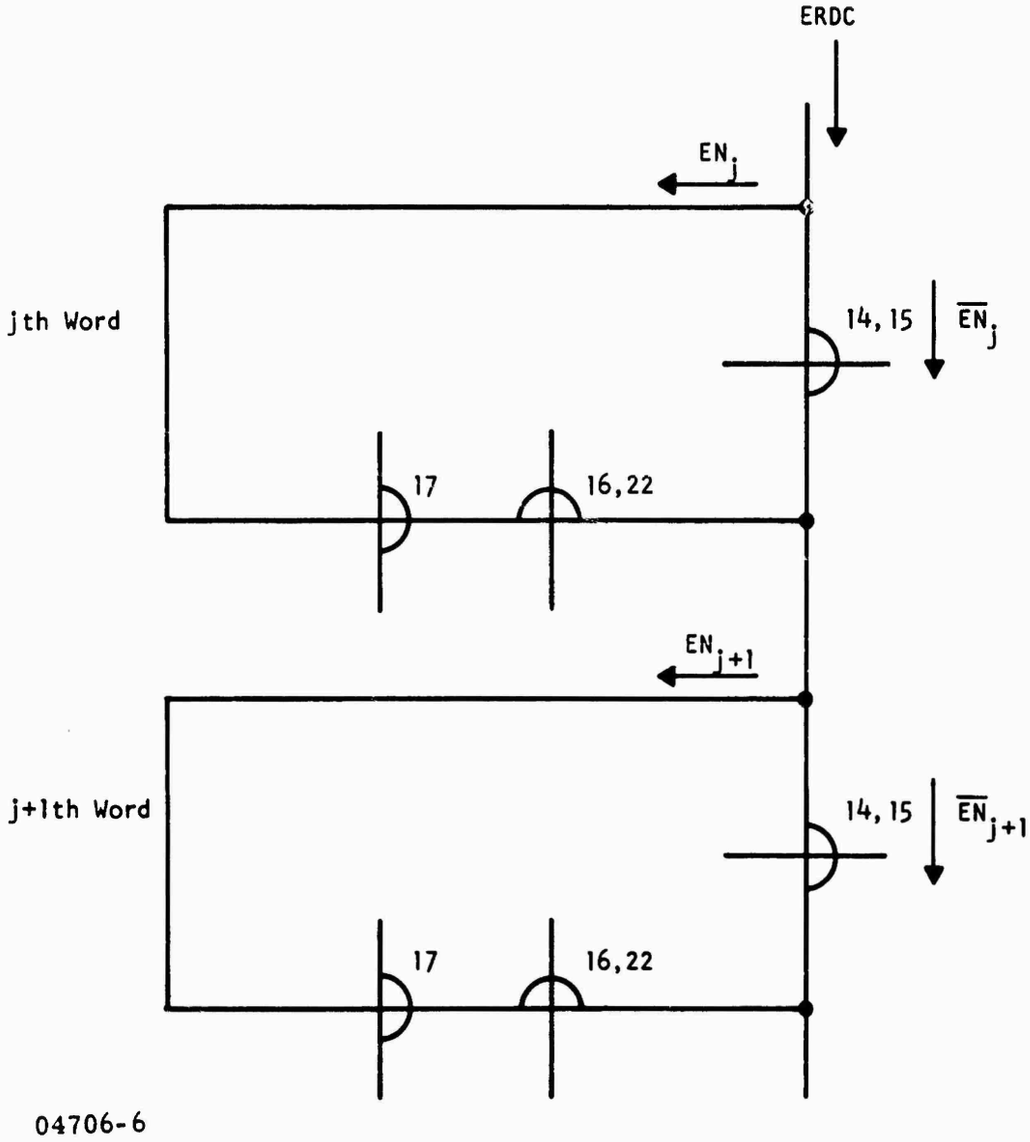

Figure 5 Enable Register flip-flop interactions with cell and word control circuitry (see Figure 2) for two words

4. Occupancy Register

The Occupancy Register (OR) is a serial arrangement of persistent current storage cells, one for each word in memory (see Figure 6). The occupancy status of each word is indicated by the direction in which persistent current circulates in the OR cell of its Word Control Circuit (WCC). A third cell state, the Null state (Ø), corresponds to absence of a persistent cell current; however, no functional use of this state is made in the current ADP design.

The entire OR may be cleared to the empty state by activating memory control Reset OR (ROR) alone. However, it is normally used in conjunction with the OR Drive (OD) to simultaneously set all words to Vacant (Vac) or Occupied (Occ). OD current of appropriate polarity and ROR current may be applied simultaneously, then released in the sequence ROR, then OD, to accomplish the latter purpose.

A given OR cell may be written into by coincidence of current in the EN line of its word and OD current of suitable polarity. The EN current must be turned off (diverted to $\overline{EN}$) before OD current is turned off, to affect storage in the cell. The superconductive shunt across the gate of cryotron 2 is of high inductance such that EN current diverted through the control of cryotron 1 is not sufficient to switch cryotron gate 1 resistive in the absence of ORD current.

A given OR cell may cause reset of the MR loop in its word when the Exclusive OR of stored and interrogated (OD activated in proper polarity) states is true. Thus, cryotron 4 is designed with a control current threshold of greater than one unit of stored current, but less than two units. Note that the critical gate current of cryotron 3 must exceed twice the stored current level.

5. Action Register

The Action Register (AR) is a serial arrangement of persistent current storage cells, one for each word in memory (see Figure 7). Full advantage of the ternary capabilities of this cell is exercised in the logical control of

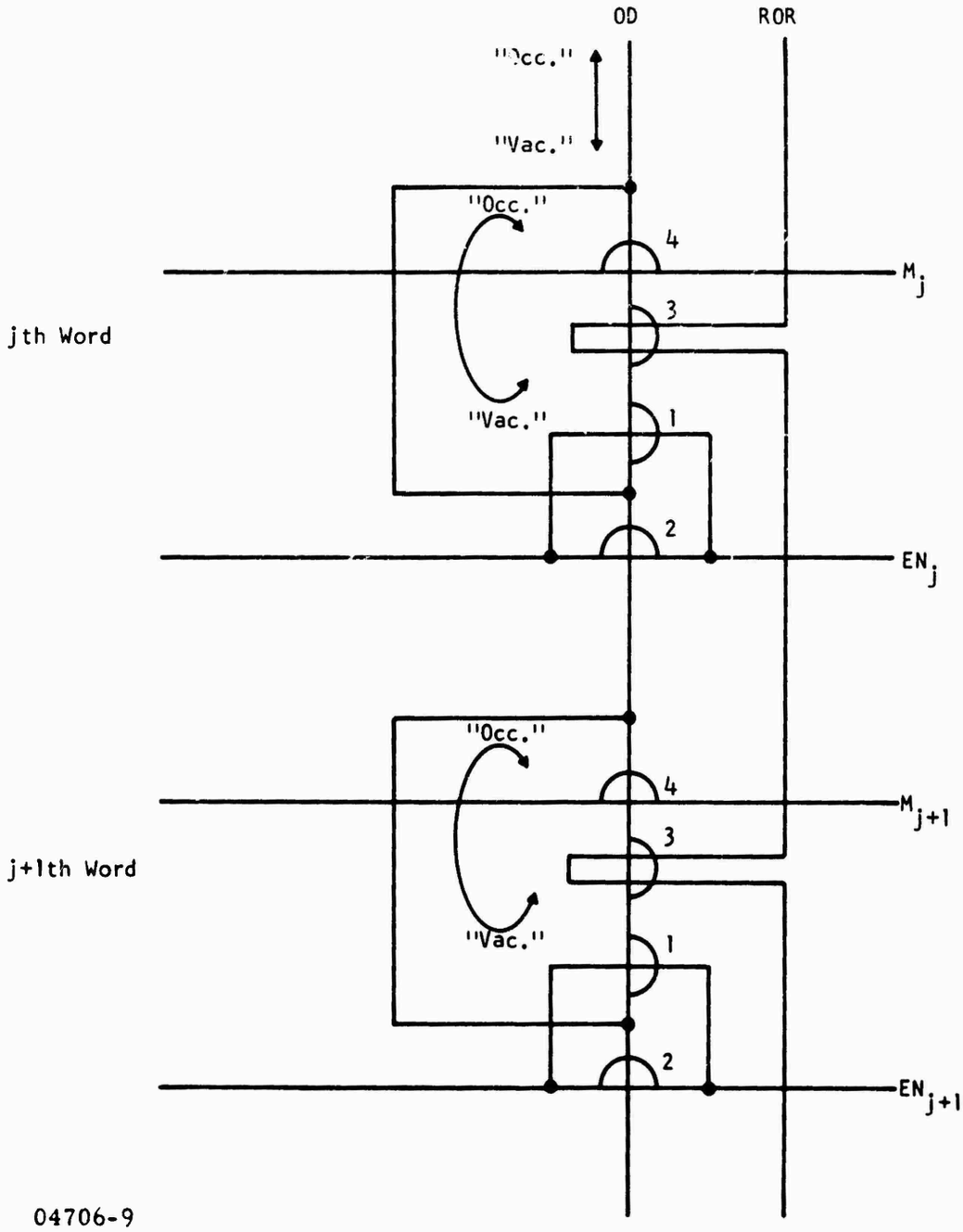

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Figure 6 Occupancy Register cell interactions with word control circuitry (see Figure 2) for two words

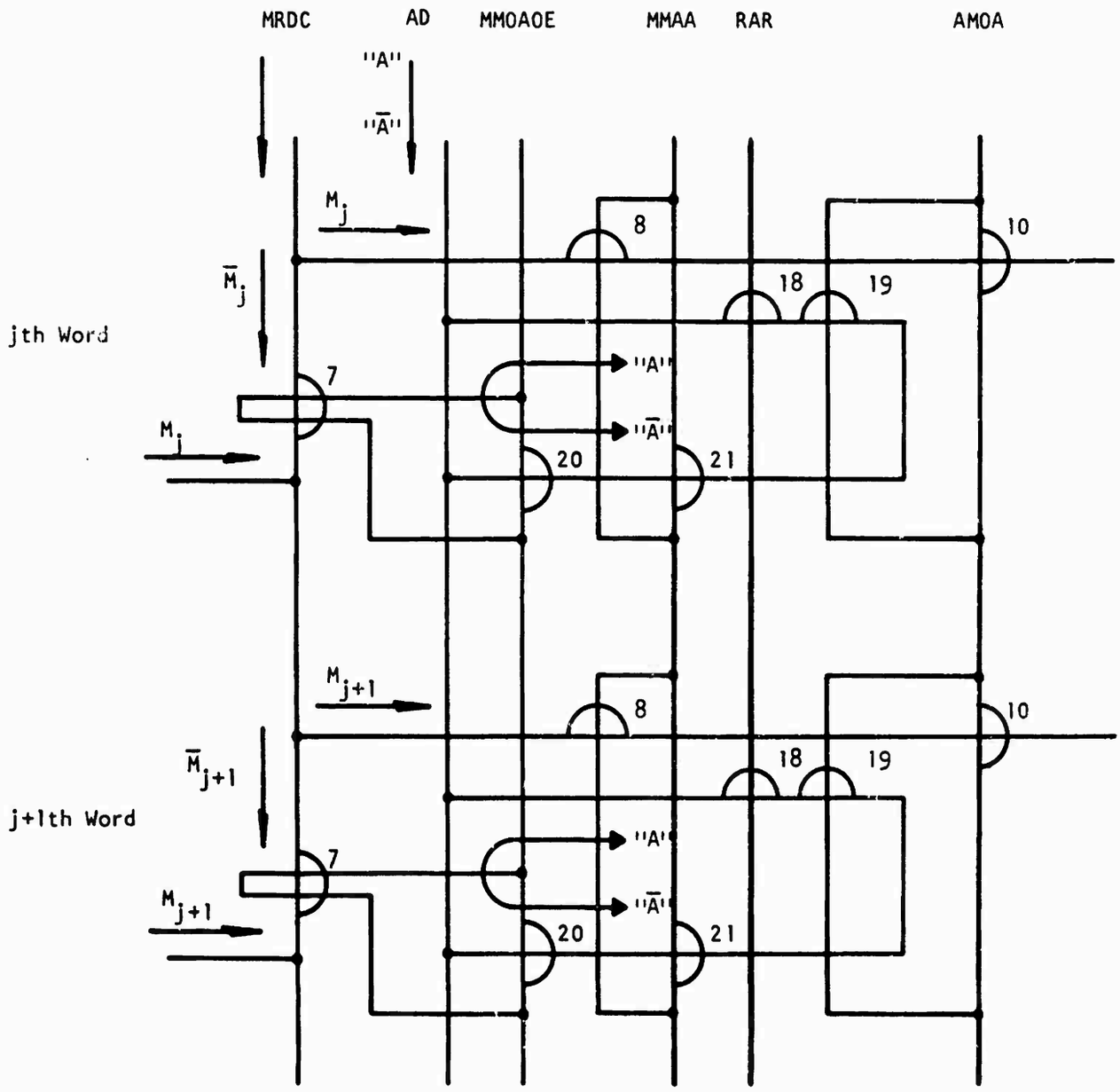

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Figure 7 Action Register interactions with word control circuitry (see Figure 2) for two words

the memory. One representative use of this ternary capability arises in the serial retrieval of a multiplicity of previously identified words. Words which are not to be retrieved are denoted by absence of stored current in their AR cell. Those which are to be retrieved, but have not yet been, are denoted by presence of loop current of polarity corresponding to $\bar{A}$, and those which have already been retrieved are denoted by presence of loop current of opposite polarity corresponding to A. The AR and MR registers influence each other's states through a number of memory controls which permit various logical connectives, thus permitting generalized set partitioning of memory.

The AR may be reset to the Null (Ø) state (absence of stored current) by memory control Reset AR (RAR) in parallel by word. If the AR Drive (AD) is simultaneously activated, and the RAR turned off before the AD, the A or $\bar{A}$ state (determined by polarity of AD) may be stored in the AR in parallel by word.

A given cell of the AR may assume the storage state implied by the polarity of the applied AD current when the memory control AMOA is active and the MR flip-flop in this word is in the M state. The original cell state is preserved if $\bar{M}$ is true, since the cryotron 18 control is shunted by the low inductance path containing the cryotron 10 gate. The AMOA control must be turned off before the AD drive is deactivated to insure proper storage action.

A given MR flip-flop may be set to the M state under the combined action of memory controls AD and MMOA, and the existing state of the AR cell in this word. The Not Exclusive Or between stored and interrogated states of an AR cell, if true, enables the MMOA current to be diverted to the high inductance cryotron 7 control. MMOA current is otherwise passed through the cryotron 20 gate. Only the A and $\bar{A}$ states of the AR cell are applicable to this operation in the present ADP design. For this operation a reversed assignment of AD polarity is used to express the interrogation state with respect to that used at the time of writing into the AR. Current must be deactivated first in MMOA, then in AD.

A given MR flip-flop may be reset to the $\bar{M}$ state under the combined action of memory controls AD and MMAA, and the existing state of the word's AR cell.

The $\overline{\text{Exclusive Or}}$ between stored and interrogated states of an AR cell, if true, prevents diversion of switching MMAA current to the high inductance, cryotron 8 control. Switching MMAA current is otherwise shunted to the cryotron 8 control. This operation is applicable to the A, $\overline{A}$, and Ø states of the AR cell. AD polarity is assigned identically for interrogation and for writing for this operation. Current must first be deactivated in MMAA, then in AD.

6. Enable Ladder

The Enable Ladder (EL) comprises two parallel paths (rails) passing (ideally) through all words in memory and has a crossover (rung) at each word in its extent. Current is assumed to enter the memory on only one of the parallel paths, the ELDC, and will be uniquely diverted to the alternate parallel path, ELGND, at the first word whose crossover presents the only non-resistive path for ELDC current (see Figure 2). The MR flip-flops condition the current distribution between ELDC and crossover paths at each word to preclude a reverse crossing from ELGND to ELDC; therefore, either one or none of the crossovers is a current carrier for a given MR state. Thus, the first (in the sense of a directed ELDC current flow) of an arbitrary number of words for which the M state is true may be uniquely selected and enabled for writing into by presence of current in its EL-crossover. The ladder is effectively "stepped" to the next M state word by resetting the former MR flip-flop to the $\overline{M}$ state. Although the ladder is logically well suited to sequentially identify individual words of a multiple word set, its time constants may be prohibitive for other than address loading purposes in which the steps are always between adjacent words. In summary:

(1) Either the ELDC extension or crossover at each word is maintained superconductive under control of the associated MR flip-flop. Thus, if M is true at a given word, the ELDC extension is resistive and the crossover superconducting, and conversely for the $\overline{M}$ state.

(2) When current enters an M state word on the ELDC extension and passes through the crossover path, the ER is set to the EN state in that word only. Selective writing is therefore possible, sequentially by word, for purposes of initially loading address information and establishing OR.

the memory. One representative use of this ternary capability arises in the serial retrieval of a multiplicity of previously identified words. Words which are not to be retrieved are denoted by absence of stored current in their AR cell. Those which are to be retrieved, but have not yet been, are denoted by presence of loop current of polarity corresponding to $\bar{A}$, and those which have already been retrieved are denoted by presence of loop current of opposite polarity corresponding to A. The AR and MR registers influence each other's states through a number of memory controls which permit various logical connectives, thus permitting generalized set partitioning of memory.

The AR may be reset to the Null (Ø) state (absence of stored current) by memory control Reset AR (RAR) in parallel by word. If the AR Drive (AD) is simultaneously activated, and the RAR turned off before the AD, the A or $\bar{A}$ state (determined by polarity of AD) may be stored in the AR in parallel by word.

A given cell of the AR may assume the storage state implied by the polarity of the applied AD current when the memory control AMOA is active and the MR flip-flop in this word is in the M state. The original cell state is preserved if $\bar{M}$ is true, since the cryotron 18 control is shunted by the low inductance path containing the cryotron 10 gate. The AMOA control must be turned off before the AD drive is deactivated to insure proper storage action.

A given MR flip-flop may be set to the M state under the combined action of memory controls AD and MMOA, and the existing state of the AR cell in this word. The Not Exclusive Or between stored and interrogated states of an AR cell, if true, enables the MMOA current to be diverted to the high inductance cryotron 7 control. MMOA current is otherwise passed through the cryotron 20 gate. Only the A and $\bar{A}$ states of the AR cell are applicable to this operation in the present ADP design. For this operation a reversed assignment of AD polarity is used to express the interrogation state with respect to that used at the time of writing into the AR. Current must be deactivated first in MMOA, then in AD.

A given MR flip-flop may be reset to the $\bar{M}$ state under the combined action of memory controls AD and MMAA, and the existing state of the word's AR cell.

For multiple array operation, as in the ADP, the ladder functions as a twin-rail, or ring counter circuit only through a single array, as illustrated in Figure 8. The ERDC supply may be distributed through all arrays or only to one at a time under control of an array selector function in the ADP interface. Since the EL operation may influence array operation only through its ability to enable ER flip-flops, its effectiveness can be restricted by selectively supplying ER current only to a specific array. Alternatively, when all arrays have ERDC supplied, then stepping of the EL circuits sets ER to EN in the next M state word in all arrays.

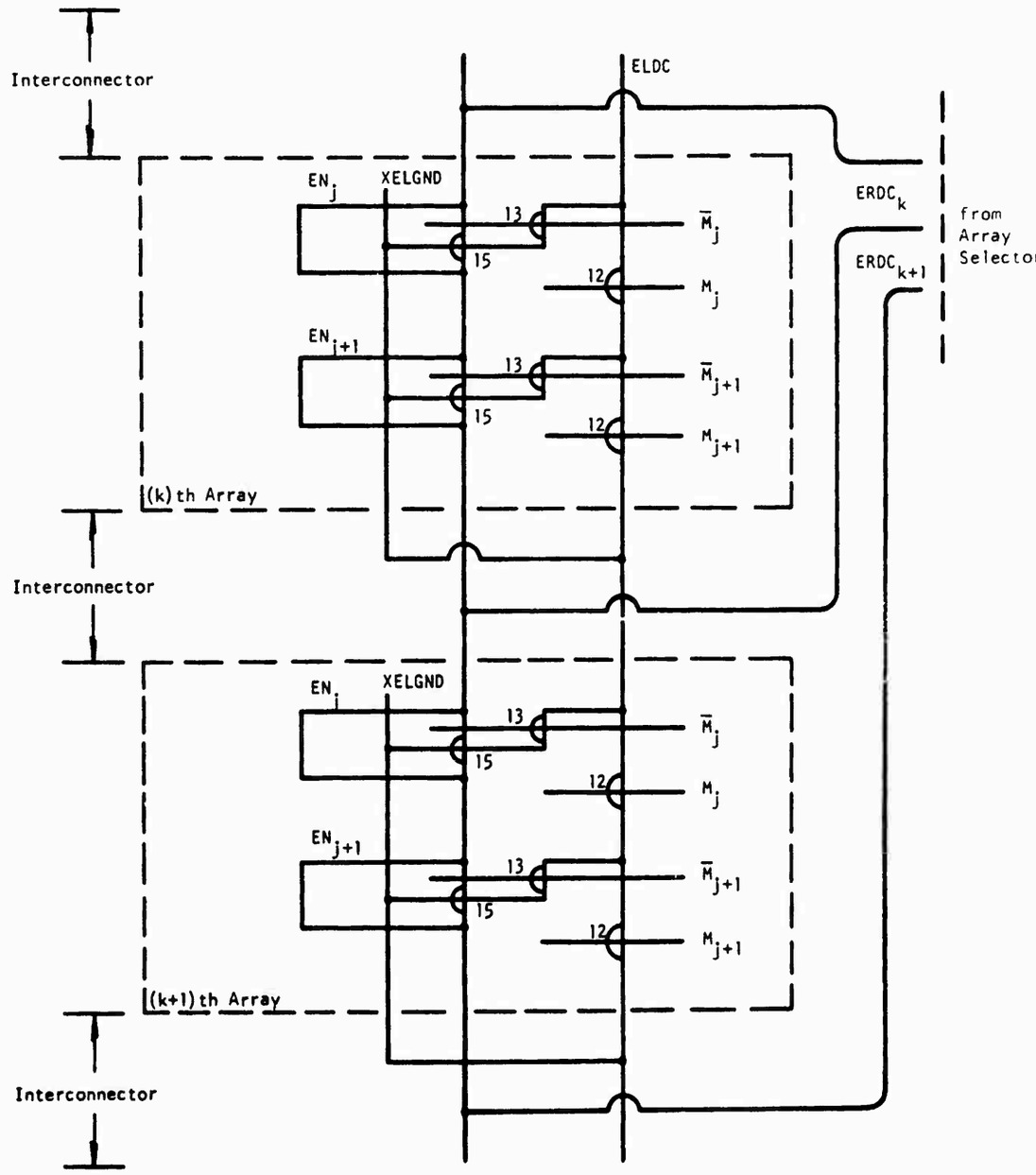


Figure 8 Enable Ladder relationship to ER and MR. Note that effectiveness of EL can be limited by selecting ERDC to only one array at a time.

SECTION III

CRYOGENIC ASSOCIATIVE MEMORY (CAM) TECHNOLOGY

A. General Information

Table II summarizes the preferred distribution of computing elements among units of manufacture, and methods of combining these elements for construction of the cryogenic portion of the 5000-word ADP. The 2.0 inch x 2.25 inch array (TIAP) containing 2000 cells and associated word control circuitry evolved as a compromise between a desire to minimize the number of arrays required and the state of the art in array fabrication. As noted in Table II, 126 serially interconnected TIAP arrays form a minimum package for the 5000-word ADP. Since fault-tolerance by word is anticipated, up to 144 arrays might actually be required to meet the capacity desired.

We encountered greater difficulty than anticipated in identifying and solving fabrication problems of the large area TIAP arrays for the final ADP configuration. Table III summarizes events under the contract. Note that fabrication difficulties were resolved in mid-program for an array size containing 20 words of 25 bits each; however, this was not a sufficient capacity for the end objective. Seven TIAP units, appropriately short-free and continuous, and possessing desired critical current levels for operation, were obtained in the final two months of the contract.

Supporting capabilities necessary for assembly and operation of the TIAP arrays in the ADP objective were advanced as required by progress in array fabrication. Interconnection by means of pressure-actuated contacts between etched superconductive strip transmission lines (117-conductor) and thin film lands of the arrays has been used successfully throughout the program for device test and operation. Practical approaches to efficient packaging of the intended 126 arrays have been studied. Data linkage means between room- and low-temperature circuitry were successfully developed and used throughout the program. Driver and sense amplifier designs have been in continuous use and have been developed into economical form.

TABLE II

TECHNOLOGY FOR 5000-WORD CRYOGENIC ADP

Array Characteristics:

(a) Capacity: 40 words of 50 bits each

(b) Active elements: 11,000

(c) Substrate: 2 inch x 2.25 inch glass

(d) Contacts: 120 on each of two opposing edges

Array Interconnection via Flexible Strip Transmission Line (Superconducting) in Pressure Contact with Array Contacts: 0.007-inch wide lines on 0.014-inch centers.

System Characteristics:

(a) 126 to 144 arrays serially interconnected

(b) Data link via 476 twisted pair, #38 gauge wire

(c) Cylindrical, immersed package; 10-inch diameter x 16-inch height

(d) Operating temperature 3.5°K ± 0.01°K

(e) Thermal load at 3.5°K of 1 to 2 watts.

TABLE III

PROGRESS HISTORY TOWARD 5000-WORD ASSOCIATIVE DATA PROCESSOR (ADP)

Program Month	Major Events
1	Preliminary design for ADP.
2	
3	Cell design confirmed via dc test of 4-cell arrays, 9-layer.
4	Feasibility of read-out concept tentatively established.
5	Word design confirmed via dc test of 2-word, 4-cell arrays, 9-layer.
6	Excessive shorting encountered with 30-word, 750-cell arrays, 9-layer. * Improved reliability of redesigned pressure actuators established.
7	Redesign for 7-layer structure at reduced cell density.
8	* Line-width control problem solved. * Nondestructive short removal enhanced at liquid helium.
9	* First operable 20-word, 500-cell array tested via dc exercise. Multisubstrate deposition facility design complete.
10	5 additional 20-word arrays dc operative; one array perfect!
11	Programmable pulse exerciser completed (3-month delay). * Pulsed operation of ADP design confirmed except for read-noise problem.
12	Film rupture phenomena identified in 80-word, 4000-cell arrays. * T. Queen discovers selective Pb-vs-Sn etchant, thus 6-layer structures.
13	* Photomask-pinholing problem solved; Electromask is supplier. 40-word, 2000-cell array (TIAP) specified for ADP.
14	* Read-noise problem solved in experimental configuration. 1218-M interface electronics specified, construction deferred.
15	* Film rupture problem solved. * First operative TIAP arrays (2) acquired in trial production.
16	* Intralayer shorting identified; problem solved by mask twinning. Two additional TIAP arrays completed.
17	* Seven additional TIAP arrays completed.

* Major technology breakthroughs.

Subsequent parts of this section of the report will describe the design approach, preferred construction means, and difficulties overcome during the program for each item of the CAM assembly.

B. Circuit Design and Photomask Specification

1. Film Layout from Circuit Function

The line drawing of Figure 2 reflects the cryotron organization and design for associative storage and word control circuit (WCC) functions adopted in the 40-word, 2000-cell TIAP arrays. The functional design stemmed from precontract effort and required only minor modifications in experimental development. Translation from functional design to actual thin film circuitry requires joint consideration of numerous factors. For example:

(1) Choice of a 0.0015-inch minimum line width (within the storage cell)

(a) was consistent with known capabilities in photoetch technique over multiple square inch areas, and

(b) resulted in an over-all circuit layout which made maximum use of the array area while mating exactly to an external contact land pattern of 0.007-inch wide lines on 0.014-inch centers, a proven interconnection configuration.

(2) Selection of gate and control line widths followed directly from

(a) consideration of the function of each cryotron,

(b) previously measured I_g vs I_c characteristics for a variety of cryotron crossing ratios, and

(c) preselection of 250 mA as the nominal drive current levels, except for Bit Sense (BS) and VOM drive current amplitudes of 90 mA.

(3) Judicious placement, and selection of width and length of inductive shunts on controlled gates to provide:

(a) 65% current trapping levels for storage, occupancy, and action register cells, and

(b) minimum ratio of 3:1 for shunt-to-gate inductance in singly controlled, non-storage loops.

(4) Lead routing is otherwise specified to:

(a) minimize the number of material layers required,

(b) minimize the number of passive crossings, and

(c) maximize packing density.

Figure 9 shows the desired film structure for the storage cell only, excluding the ground plane and return paths labeled Match (M) and Enable (EN) to their respective register circuitry in the appended WCC film structure on the array. A 9-layer structure was used in the initial arrays constructed for breadboard adjustment of circuit operation. Figure 10 is a photograph of a 4-cell array first constructed and operated. The third generation design was selected for subsequent efforts; the cell module is 0.028-inch wide by 0.030-inch high. Figure 11 shows the 2-word, 4-cell array next constructed and modified through two generations to provide satisfactory operation of cells and the complete WCC circuit functions. The circuit layout has been modified only slightly in subsequent arrays to accommodate to the reduced layering desired for fabrication ease. In the TIAP array, the cell is 0.040-inch high by 0.028-inch wide, as before, but the increased height is the result only of relocating the M and EN returns in the post-ground plane metal layers.

2. Photomask Preparation

The mechanics of photomask specification and preparation are of paramount importance to successful array fabrication. The preferred methods now used are described below in terms of the 6-layer TIAP array utilizing a selective etchant for lead (Pb) in the presence of tin (Sn). The Pb ground plane and its insulating layer are masked either by stencil or by photomasks of non-critical geometry, depending on the process used to form those layers.

Four photomasks of critically controlled geometry form the set which defines the interconnected cryotron film structure. The functions of the masks are as follows:

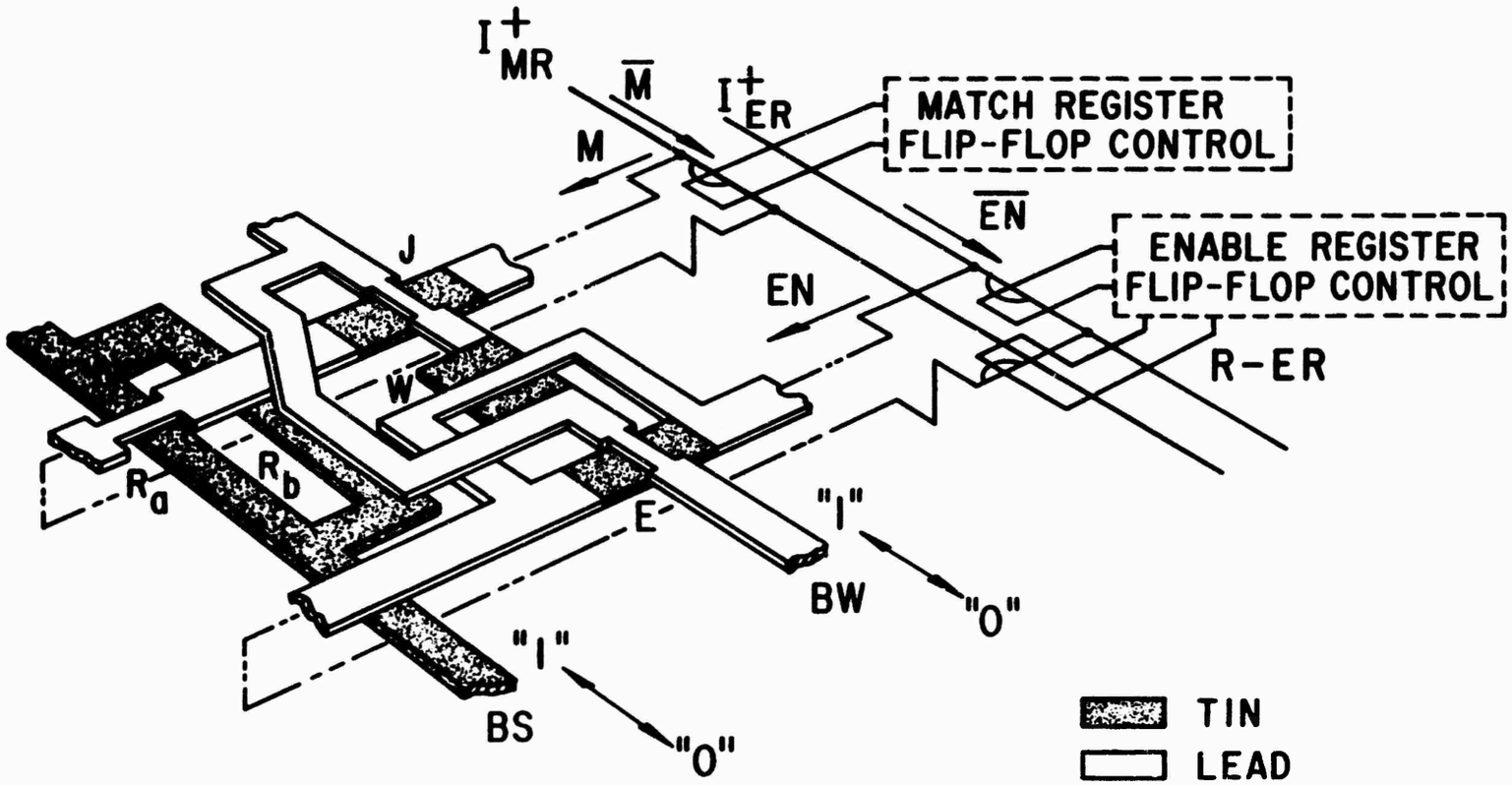


Figure 9 Thin film cryotron structure for single associative cell, excluding ground plane, underlying register returns (shown in dotted line form), and obvious insulation layers

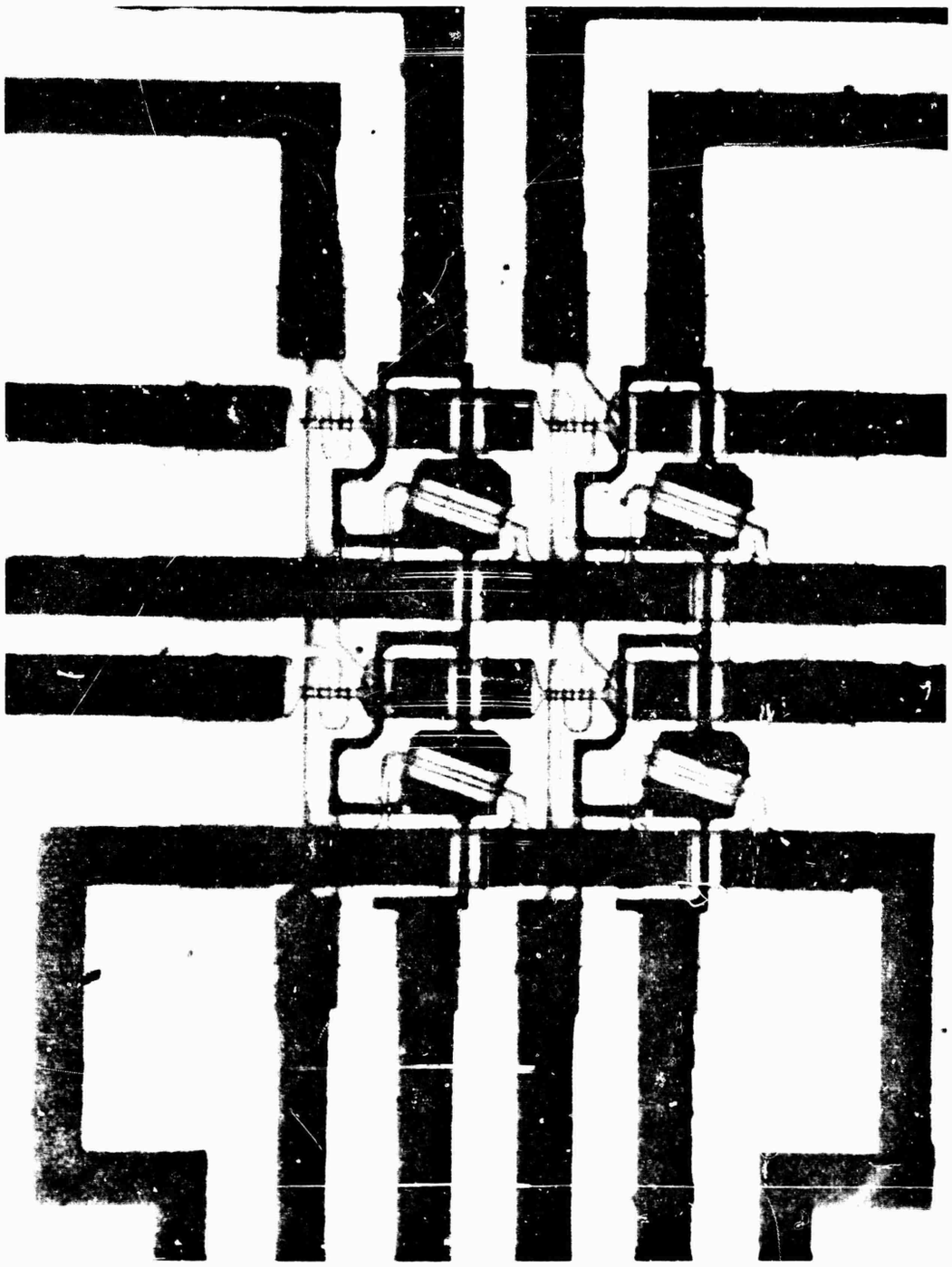


Figure 10 Four-cell array of associative storage sites used to experimentally determine final cell design. Circuit area is 0.056 inch x 0.060 inch.

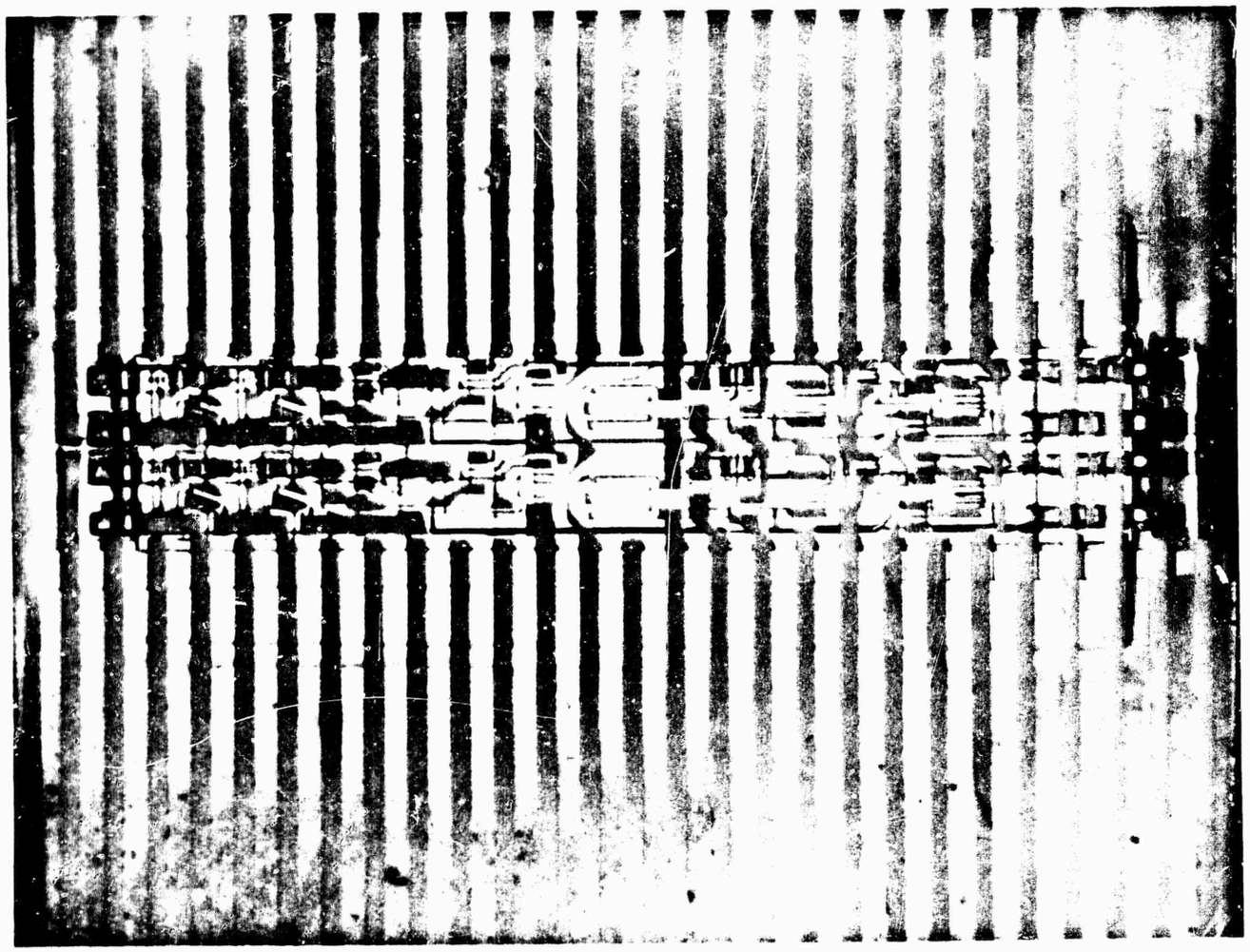


Figure 11 Two-word, 4-cell array of associative process words used to determine final word design. Circuit area is 0.3 inch x 0.060 inch.

(1) Mask #32 defines regions of metal which are to remain after the Pb on Sn bilayer is etched.

(2) Mask #31 defines regions where Pb is to be retained over Sn following a selective etch for Pb.

(3) Mask #42 defines regions of insulation to be retained or, conversely, opens contact points and etch-through windows (to subsequently remove shorting bars) to the underlying metal.

(4) Mask #50 defines regions of Pb which are to remain to form control lines and remaining interconnection structure following etch. (Note that the etchant has access to shorting filaments in prior metal layer.)

A scale layout is made of representative circuit functions (storage cell, WCC, register flip-flop closures, and lands form basic functional elements for step-and-repeat generation of the total array pattern) in appropriate modular relationship to each other. The parts are segmented and allocated to the metal layers, and appropriate openings are assigned in the intervening insulation. A coordinate description of each segment or opening is prepared, with applicable layer and functional element designated. This information is keypunched and computer-processed (IBM-7044), then translated and presented on a control tape for automatic plotting or cutting of individual or composite mask patterns for an array of arbitrary step-and-repeat composition. At present, we use a Calcomp plot of both individual and composite masks at 200X final size for inspection purposes.

The photomask vendor, Electromask Corp. of Van Nuys, California, is then provided 200X plots of the masks for the individual functional elements. These are overlaid with a laminated plastic peel coat, one layer of which is opaque in the ultraviolet. The conventional cut-and-strip procedure is performed for at least one of each of the functional elements in the array. This artwork is photographically reduced 10X in transfer to a photographic plate. This plate serves as the reticle in step-and-repeat generation of the master plate for each mask. The master plate is projection-printed at 2X reduction at each step of its generation.

The 10X master plate is carefully inspected for light pinholes and/or broken line segments in the desired opaque regions. At 10X, photographic retouching is practical; excess opaque material can be tolerated when mask twinning is employed, but it is undesirable. Then the working copies of photomasks for array fabrication are projection-printed from the master plates at 10X reduction.

The importance of certain critical features of this method was not recognized at the start of this program, and these features have caused major retardation of process development for large area arrays. Chronologically, they were identified and resolved as follows:

(1) Interlayer registry of film segments in the array must be maintained within design tolerance (0.0001 inch) over the entire array. Step composition of the multiple functional elements was possible over areas upwards of 1.2 inch x 1.2 inch at the start of the program, consistent with general semiconductor industry requirements. Electromask Corp. was among the first to remove the limiting characteristics in mechanical means employed for step composition, however, and provided acceptably registered mask sets by the fifth program month for a 30-word, 750-cell array (9-layer film structure then used). Subsequent developments in the step-composition art eliminated this as a factor of concern for arrays up to 4 inches x 4 inches.

(2) Opaque emulsions on photographic master plates or working photomasks are thin films subject to pinhole damage. The resultant light leakage creates corresponding pinholes in photoetched metal and insulation patterns. Early step composition methods involved contact- rather than projection-printing of both master plates and working photomasks. Pinholes were caused principally by surface irregularities of the contacted plates or included "dust" between the plates. Worst of all, the master plate was at final size and could not be repaired by retouch techniques. The complete step composition process is now done by projection-printing at 10X to allow retouch of the few inevitable pinholes in large area plate coatings. Working photomasks are also projection-printed and

subjected to critical inspection before and during use. The benefits of this development were not available until the thirteenth program month.

(3) Master plates (10X) and working photomasks are subject to degradation through "aging" and repeated use; in particular, they may increase their opaque character locally through:

(a) retouch procedures applied to pinholes in master plates, which are transferred to photomask copies,

(b) "dust" accumulation on master plates and stored photomasks,

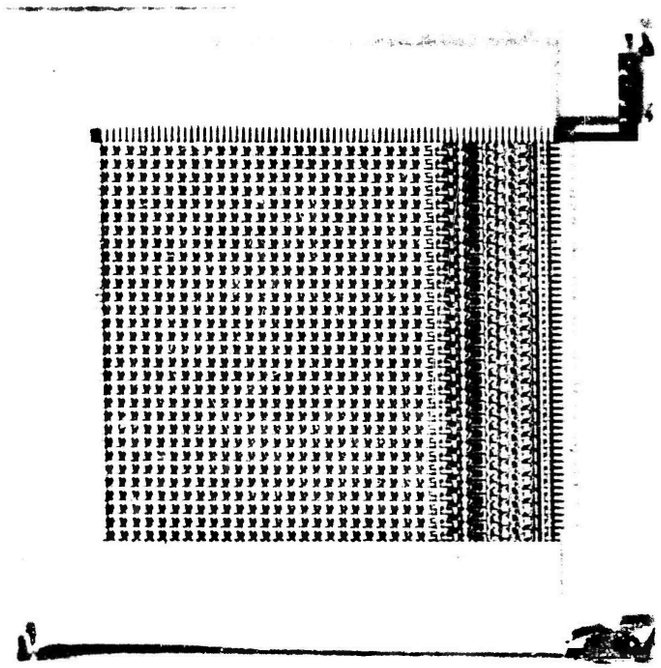
(c) contaminant adhesion to used photomasks. The result, not identified until the sixteenth program month, can be intralayer metal shorts which cannot be nondestructively cleared. The most practical solution is independent preparation of two master plates for each mask pattern. Copies of each are used separately to double-expose the metal etch photoresist before the etch is accomplished.

C. Array Fabrication

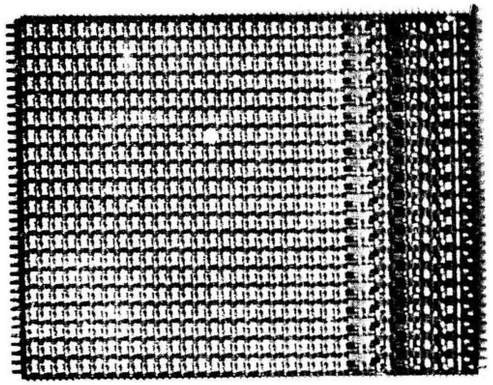
1. Background

The 2.0 inch x 2.25 inch TIAP (40-word, 2000-cell array) evolved as the final unit of production following a succession of problem identification and solution cycles encountered with arrays larger than those used to determine circuit design. A 30-word, 750-cell array, shown in Figure 12(a), was the first array of intermediate size attempted for mid-program evaluation of total cryogenic technology. The return paths for EN and M (see Figure 9) were situated beneath and insulated from the ground plane of this 9-layer structure to minimize word height, 0.030 inch at that time. The level of shorting experienced between ground plane and cryotron structure was attributed (erroneously, as now known) to the large number of processing steps necessary to complete the structure.

The array design was accordingly altered to require only a 7-layer structure by reassigning register return paths, formerly beneath the ground plane,



(a) 9-layer array of 30-word, 750-cell capacity: 1.0 inch x 0.9 inch circuit area.



(b) 7-layer array of 20-word, 500-cell capacity: 1.0 inch x 0.8 inch circuit area.

Figure 12 Intermediate-sized arrays produced in the course of large area array fabrication development

to a subsequent metal layer. This increased word height 33%, to 0.040 inch. Figure 12(b) shows the 20-word, 500-cell array which resulted, In all, six of the 500-cell arrays were successfully fabricated by the tenth month of the contract. These arrays were pulse operated to evaluate circuit performance.

The initial program objective was a 9-layer, 2 inch x 4 inch array containing 100 words of 50 bits each. We obtained a mask set for a 7-layer structure of 80-word, 4000-cell capacity and attempted to construct ten arrays. Without exception, one segment in the middle of each array exhibited gross film rupture as the multiple-layer structure developed. The major contributor to short circuit formation was thereby identified and subsequently removed, as evidenced by circuits obtained in the twelfth program month. Concurrent developments included (1) a redefinition of final array size to the 2 inch x 2.25 inch TIAP of 2000-cell capacity, as shown in Figure 13; (2) independent development of a selective etch for Pb in the presence of Sn, and thus the 6-layer array; (3) development by Electromask Corp. of an accurate step composition method of preparing photomasks using only projection printing means. By incorporating these results in the fabrication process immediately, we were able to fabricate two TIAP arrays in which we could remove shorts so that unfailed words were accessible and operable. One remaining fabrication problem was intralayer shorts resulting from photomask degradation during operation. Double exposure through independently prepared masks eliminated this form of structural failure.

Three trial production lots of TIAP arrays were made, and from these we have obtained 7 arrays which are capable of fault-tolerant operation. The following subsection describes the preferred process now used and the nature and solution of the fabrication problems which retarded completion of the end program objective.

2. Laboratory-Scale Fabrication Methods

Thin-film fabrication techniques for cryotrons have been substantially advanced in this program to permit laboratory-scale production of operable, large-capacity arrays. The TIAP array shown in Figure 13 provides 2000 cells

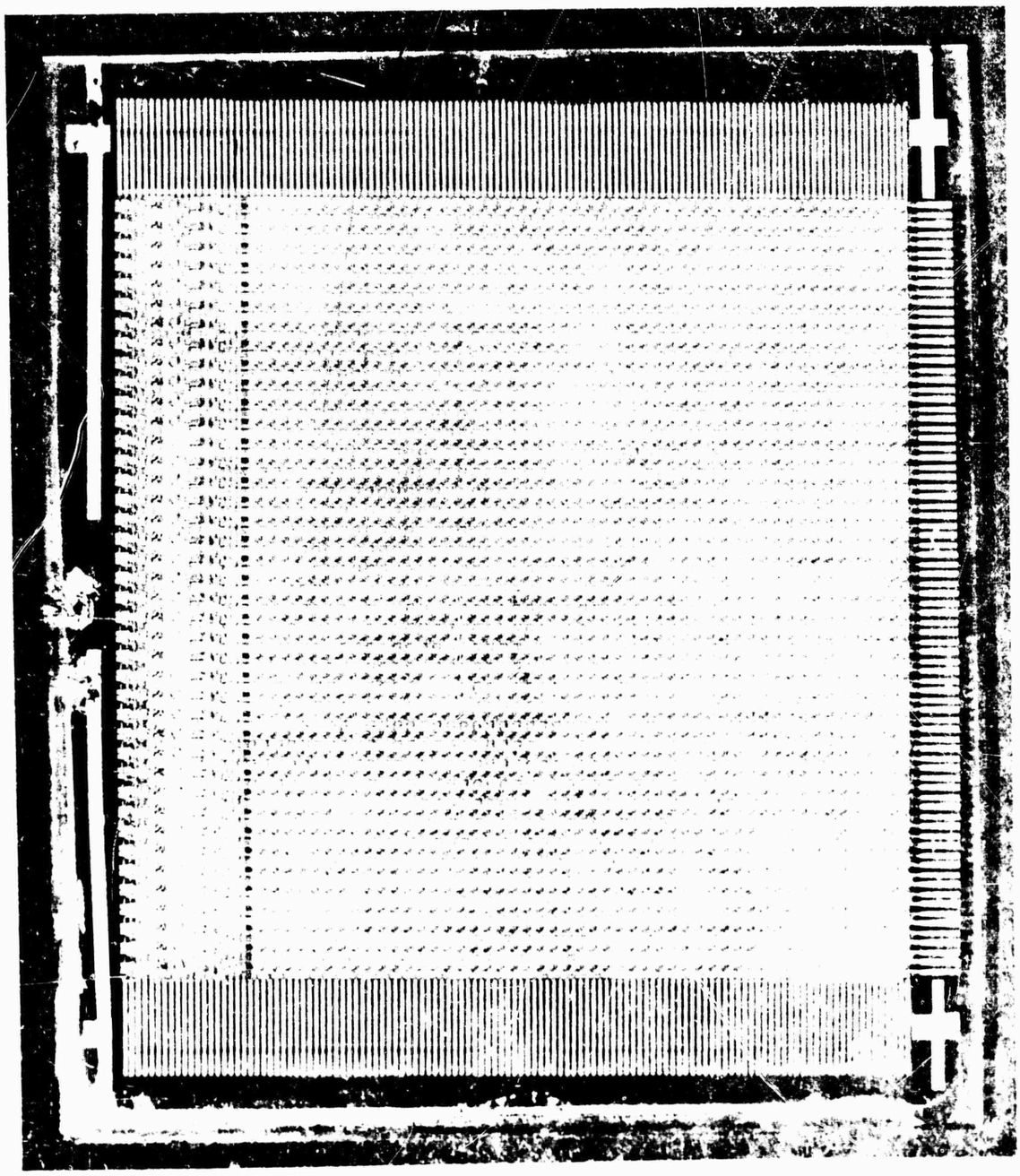


Figure 13 6-layer TIAP containi[illegible]
each. Array size is [illegible]
circuit area is 1.[illegible]

and associated word control circuitry through appropriate control and interconnection of 11,000 active gates. Figure 14 illustrates the simplified construction which resulted in the now standard 6-layer structural format. The substantial reduction in major material processing steps was achieved principally by introducing a reliable method for selective etch of Pb in the presence of Sn, insulation, and photoresist materials.

Depositing the first four material layers means, in effect, constructing a large area capacitor; the ground plane serves as one plate, the Pb-Sn combination (before fine patterning) the other. The "capacitor" character is exploited by providing an exposed ground plane tab (see Figure 15) at one edge of the array. This tab is masked during deposition of the Pb-Sn combination. Shorts through the ground plane insulation can be readily detected and cleared, and the surface quality of the potential array can be visually inspected. Since little material or labor has been invested in the array at this point, samples which are marginal in any sense are discarded.

The short-free specimens are now subjected to the following process steps:

(1) double exposure and development of a photoresist coat with independently prepared mask specimens to define regions where Pb and/or Sn are to be retained;

(2) etch removal of undesired Pb and Sn, removal of resist residue, and recoat;

(3) double exposure and development with twin masks to expose gate regions only; i.e., regions where only Sn is desired in a series path;

(4) etch removal of Pb only, removal of etch residue, and recoat;

(5) double exposure and development with twin masks to provide openings for subsequent interlayer contact and shorting-filament removal, resist polymerization, and recoat;

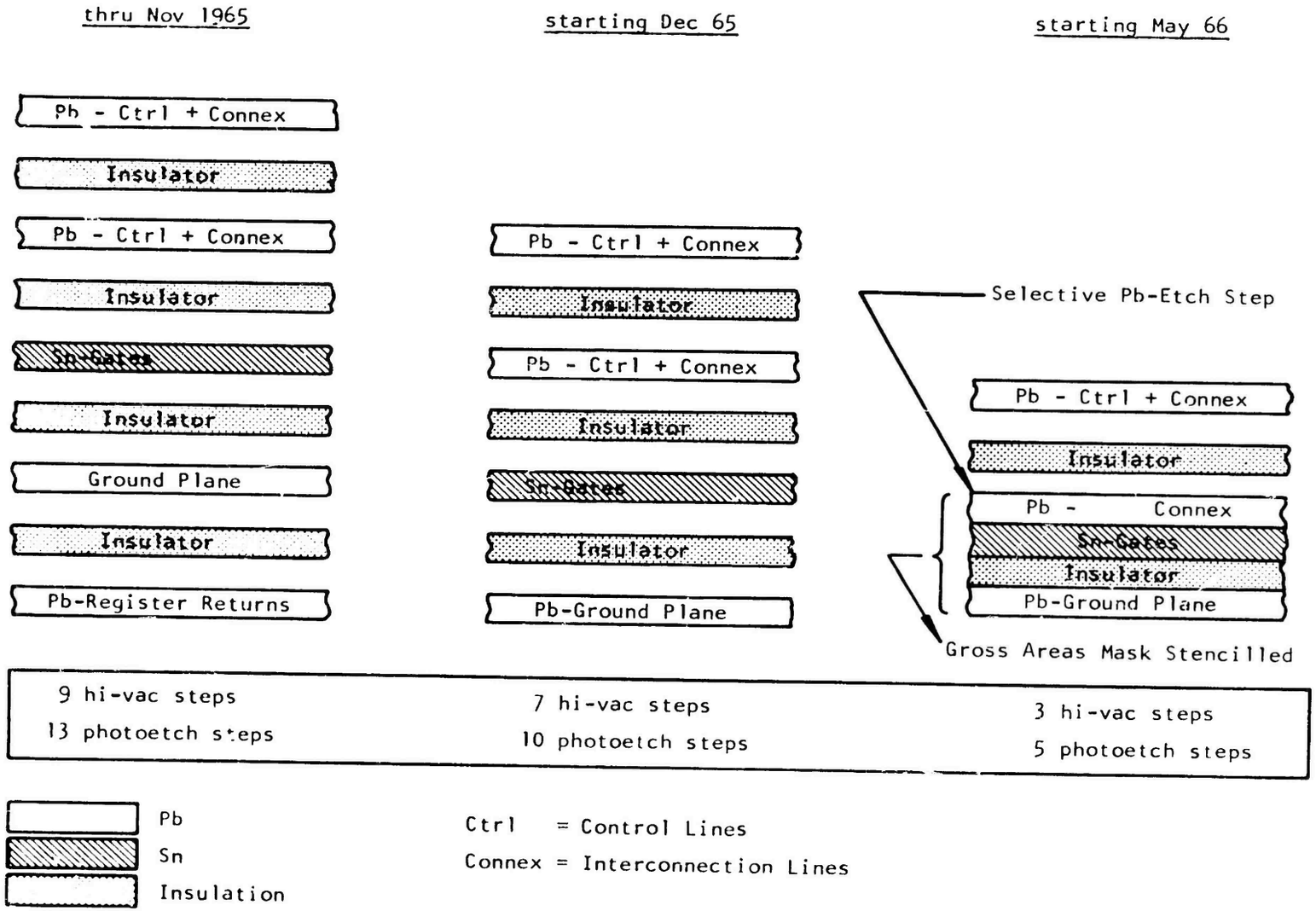


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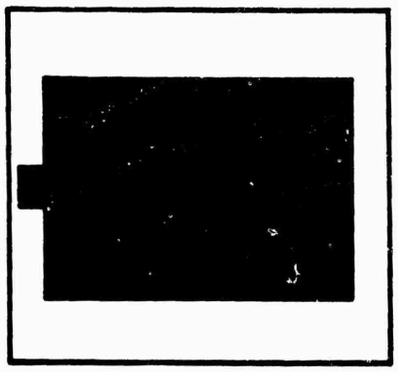
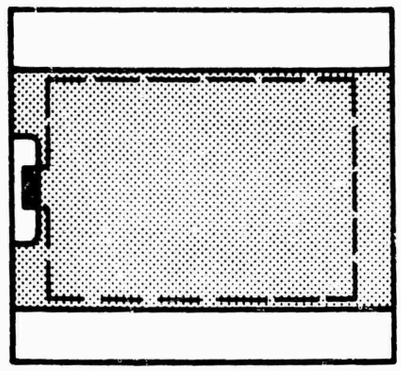
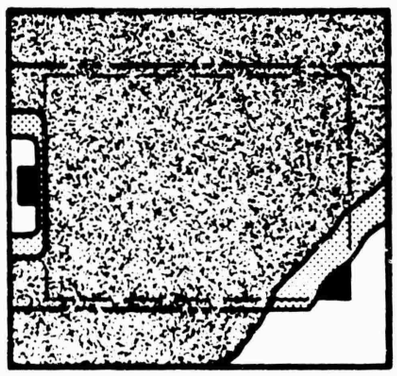
Figure 14 Evolutionary simplification to "6-layer" cryotron thin film fabrication



(a) Pb-Ground Plane



(b) Ground Plane Insulated



(c) Pb-Sn Combination
Added to Complete "Capacitor"

Figure 15 Stepwise construction of array through first four material layers. The "capacitor" formed is readily checked for shorts through ground plane insulation.

(6) double exposure and development with insulation patterns as in (5) above, but vacuum-depositing the last Pb layer following insulator polymerization;

(7) double exposure and development of a photoresist coat with twin masks to define regions where Pb is to be retained to form control lines, and completion of interconnection structure; in particular, shorting filaments in the previous metal layer are etched away;

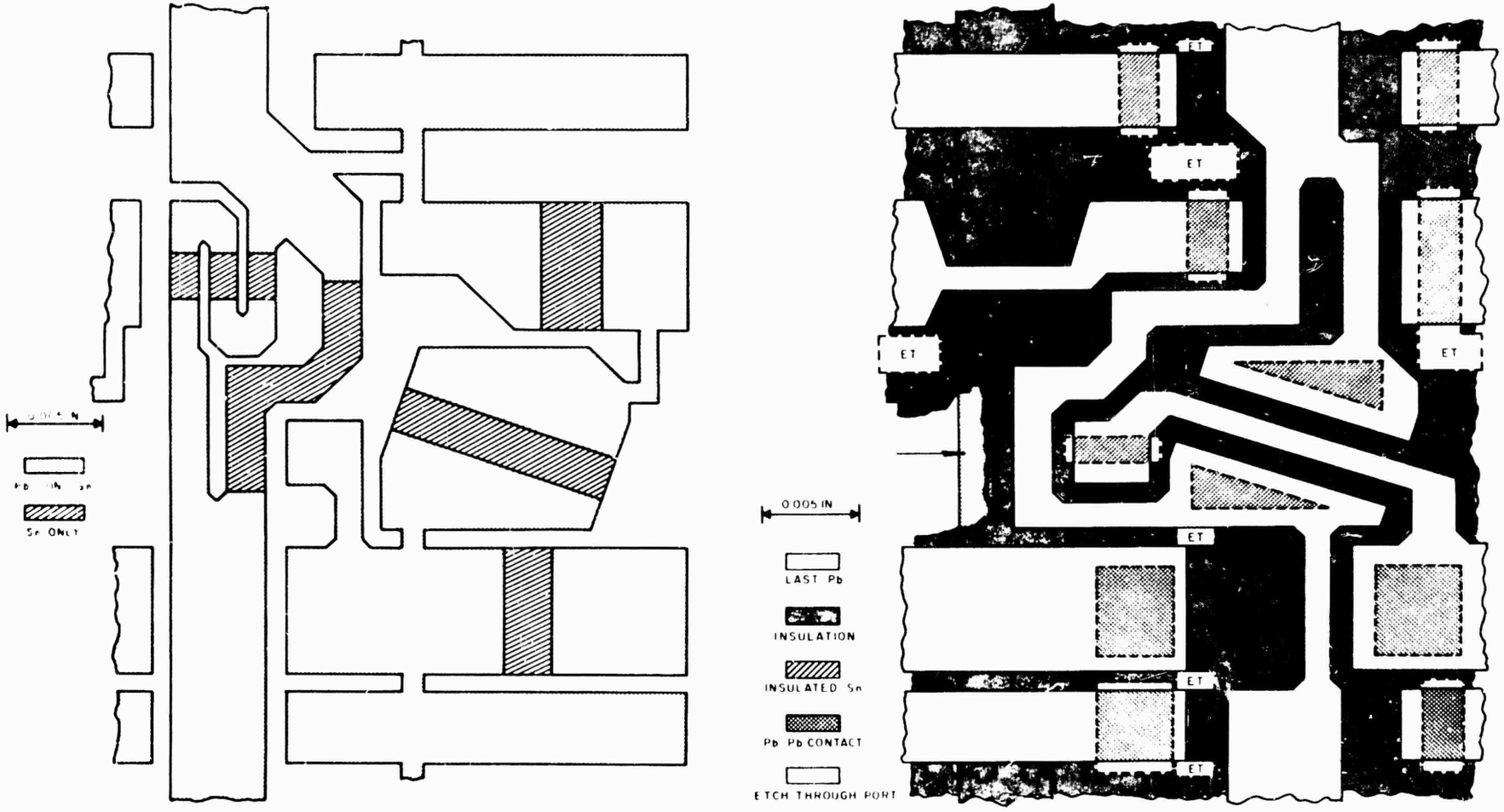
(8) etch removal of undesired Pb, and resist removal complete the array construction.

Figure 16 illustrates the situation following steps (4) and (8) for a single associative cell.

Double exposure of a positive photoresist with twin (separately prepared) copies of each photomask pattern reduces the probability of intralayer shorts caused by light-blocking flaws in individual photomasks. Such flaws occur when dust is randomly trapped between mask and array in a given exposure act, and when intended transparent regions of the photomask are abraded through use and cleaning operations. Preferably, twin masks are copies printed from independently prepared and retouched master plates, since the latter are also subject to light-blocking flaws.

Shorting bars are included in the pattern for the Pb-Sn combination layer to overcome the major cause of interlayer short circuits experienced with large area arrays through the fourteenth program month. This shorting had been attributed principally to insulation voids caused by ambient "dust" in the critical wet steps of insulator application. For the 7-layer, 500-cell arrays the short-clearing procedures permitted successful completion of a low yield of arrays. The locations of shorts were uncorrelated between arrays and seemingly randomly distributed over any given array.

When the 7-layer, 4000-cell arrays were attempted, at an area increase of 8X, the number of interlayer shorts among all layers increased markedly, and the shorts were concentrated in the center of the 2 inch x 4 inch arrays.



(a) after selective etch of Pb in composite Pb-on-Sn layers

(b) after etch of last Pb layer

Figure 16 Resulting structure of a single associative storage cell following major process steps. Starting point is assumed to be unpatterned Pb-on-Sn layers over an insulated ground plane on glass substrate.

Inspection under transmitted light showed that large segments of film layers down through the ground plane were literally "exploded" away from the substrate surface. The models explaining interlayer shorts on the basis of ambient "dust" conditions did not fit this observation. The intensive review of all process steps and conditions occasioned a measurement of potential drop between an insulated ground plane film and the metal fittings of the vacuum chamber during a metal deposition step. A large potential was observed to develop during the glow discharge step which precedes all metal depositions to improve film adhesion. A series of experiments indicated that both high-energy electrons and ions were incident on the surface of the substrate. The stopping power of the insulator was sufficient to inhibit penetration of ions to the underlying metal film, but not high-energy electrons. Thus, a net negative charge was suspected to be accumulating in the insulated metal film layer. When the net voltage between metal film and discharge exceeded the breakdown potential of the insulator, a localized "explosion" of metal film and overlying insulation accompanied the arc produced. The interlayer shorts experienced, then, were the result of contact between freshly deposited metal and underlying metal edges left exposed at the perimeter of a film rupture point.

The successful solution was to provide a high-conductance path from insulated metal film structure to the discharge region, thus inhibiting harmful electron charge accumulation. In the TIAP arrays this flow path takes the form of shorting bars defined between all metal segments in the Pb-Sn combination layer, including the contact lands. The lands are also bussed together, and at the time of glow discharge prior to final Pb deposition, the ground plane tab and the common point of the Pb-Sn layer are shorted to the metal fittings of the vacuum systems employed. The final insulation layer pattern was appropriately modified to define etch-through openings to permit these shorting filaments to be removed when the last Pb layer is etched.

When this problem was identified and remedied, TIAP arrays were produced with an average of 30 shorts between the two patterned metal layers. Short clearing at liquid helium temperature yielded unshorted, operable arrays, but generally at the expense of an average of 3 of 50 bit lines. The identification and correction of intralayer shorting mechanisms now makes possible

arrays with an average of 10 shorts before clearing. These shorts can be removed without loss of bit lines, in most cases.

Problems related to structuring of short-free, appropriately continuous multilayer arrays are therefore neither of a fundamental nature nor impractical in their solution for the material system and process employed. Laboratory-scale fabrication of arrays is now an accomplished fact.

3. Fabrication Equipment

Figure 17 shows one of two vacuum systems used to deposit metal film. This equipment can rapidly achieve 10^{-7} Torr preparatory to deposition of Pb and/or Sn in the 10^{-6} Torr range. Figure 18 shows one of the two mask alignment and photoetch installations used in the program. The wet steps of the process are conducted in laminar flow hoods such as the one at the left of Figure 18.

This equipment was originally intended only for experimental fabrication to assess multilayer construction methods at each new level of complexity. Preferred methods, relating to thin film deposition, were to be incorporated in two multiple array fabricators for the pseudo-production of the 126-144 arrays required for the ADP. Figure 19 shows one of two such units developed in a program peripheral to the ADP effort. The unit shown accommodates eight arrays for simultaneous construction of the first four layers of the TIAP structure in a single vacuum cycle. Mask stencils are used to limit the extent of the ground plane and its insulation, as previously described. No TIAP arrays were completed using these multiple array fabricators before the program expired. Should the ADP objective be pursued, specialization of the multiple array fabricators for ADP construction will be completed.

4. TIAP Fabrication Results

Although arrays of 20-word, 500-cell capacity were successfully fabricated in mid-program, the process then in use reflected neither the selective etch method nor the preventive means subsequently introduced for short circuit elimination. A low yield of useful samples was obtained by extensive application

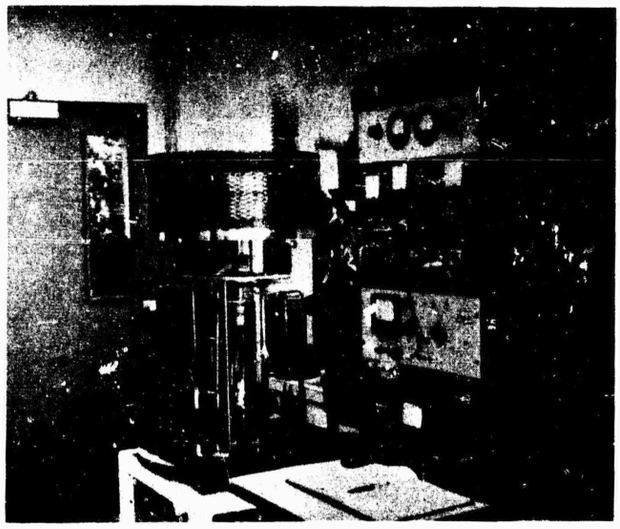


Figure 17 One of two laboratory vacuum systems used for thin film deposition

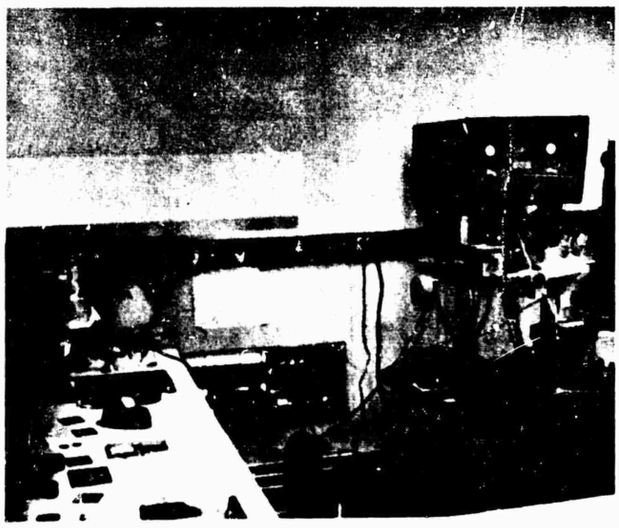


Figure 18 One of two photoetch stations employed in program. Wet steps of photoresist application, development, and etch are conducted in the laminar flow bench on the left. Mask alignment and exposure steps are conducted on unit at right.

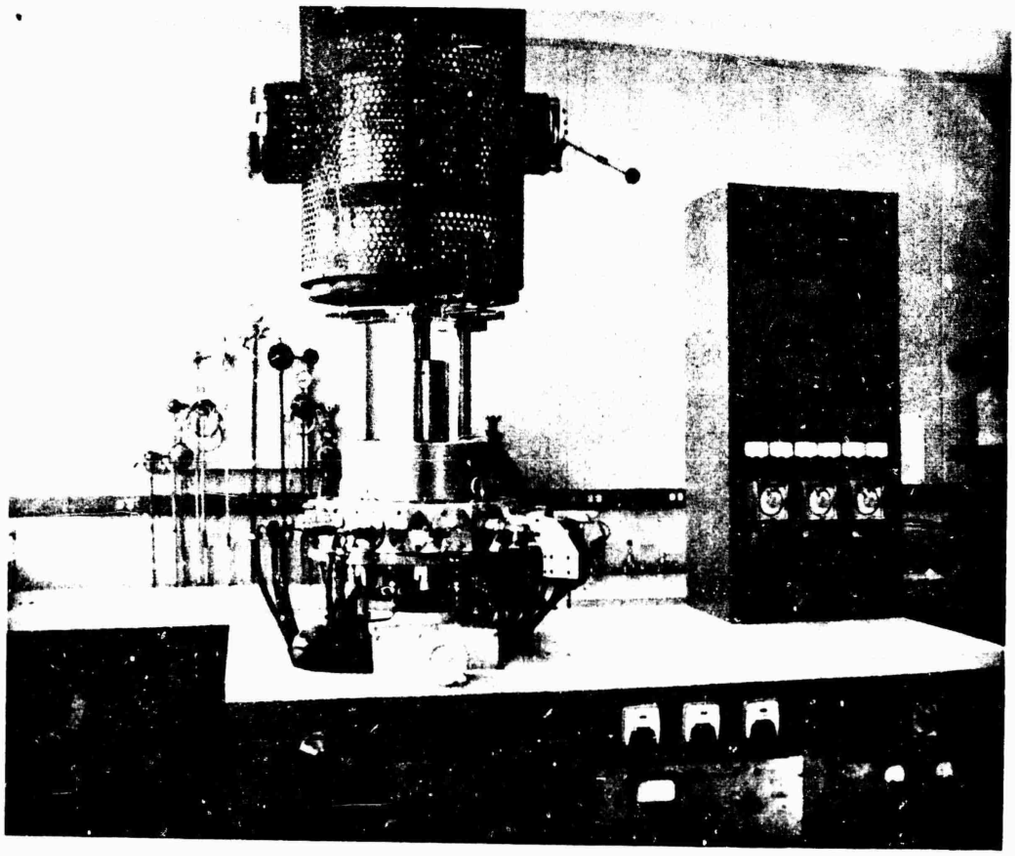


Figure 19 Multisubstrate, vacuum deposition equipment being developed for pseudo-production usage

of short clearing methods at 3.5°K. The experience obtained is therefore not relevant to the process now in use for 6-layer structures.

Fifty-nine TIAP (40-word, 2000-cell) arrays were initiated in the final two-and-a-half months of the program, after receipt of a photomask set incorporating internal shorting bars designed to prohibit film rupture during a pre-deposition glow discharge step (for film adhesion). Previous experience with TIAP arrays had resulted in no useful samples, even after extensive short clearing. In all cases, vital through-signal paths were themselves open-circuited before all shorts had been removed.

The 59 arrays reviewed here represent three trial fabrication lots, each designed to verify the solution of a particular problem and to provide qualitative information concerning array yield.

The first lot consisted of 15 arrays. The 6-layer process was modified only with respect to use of the mask set inhibiting film rupture (intralayer shorting was not yet identified). The vacuum deposition units were thoroughly cleaned just prior to processing of this lot. Of the 15 arrays initiated, three were aborted before or just following large area deposition of the Pb-on-Sn combination layer. The remaining 12 were completed and subjected to 300°K and 3.5°K test. Arrays are tested at 300°K to assess number and location of shorts, as well as the resistance associated with each primary path. Except for the first and third arrays of the lot (#95 and #97), an average of 30 shorts was noted for each array before short clearing. This corresponds to 30 out of a possible total of 10^5 shorting sites per array. Array #95 had 10 shorts, while #97 had 15. In no instance were there short circuits to the ground plane.

Arrays #95 and #97 were operable after 3.5°K short clearing. In each case, one short was left uncleared after the capacitor discharge voltage had been increased to the safe maximum of 45 volts. (Beyond this level, destructive dielectric breakdown is frequently experienced.) In array #95 no critical through-signal paths were lost. In #97 five bits were rendered inoperable because of BW or BS open circuit. Since no word control circuitry was

open-circuited, these arrays were structurally acceptable for 50-bit and 45-bit operation, respectively.

Analytical methods have been developed to pinpoint the location of shorts in the array based on the 300°K test data. Microscopic examination of the locale of shorts which could not be nondestructively cleared from this first lot clearly indicated the presence of excess metallization in one or another etched metal layer. These intralayer shorts could be attributed only to an error associated with preparation or use of the patterning photomask. However, the shorting sites were predominantly nonrepetitive among arrays made with the same working photomasks. (Observation of a repeating short site among arrays is a direct indication of a photomask flaw incurred during mask preparation.) Once the shorting was identified as intralayer and the result of light interference caused by inclusion of opaque particles between mask and array during the exposure act, it was determined that double exposure with independently prepared mask specimens was an apparent solution.

A second lot of 15 arrays was then initiated using double exposure for each photoetched material layer. Other than this change, the process was identical to that used for the first lot of arrays. To accelerate matters, the vacuum equipment was not cleaned prior to initiation.

Only seven of the 15 arrays initiated were processed to completion beyond the large area Pb-on-Sn combination layer. Not unexpectedly, the failure modes associated with the aborted units were characteristic of a degrading vacuum environment as a result of inadequate cleanup. The number of shorts in each array before clearing ranged from 2 to 10; all shorts were removed with low-voltage capacitor discharge (6 volts). Of the seven units, four had no open signal paths. The other three arrays had one, two, and seven open bit lines, respectively.

The critical current levels in arrays from these two lots were lower than desired because the film thickness monitoring equipment was miscalibrated after the cleanup preceding the first lot (not discovered until both lots were completed). The Sn layer, in particular, was 25% thinner than desired; however, operation was possible with six of the seven arrays completed.

Use of arrays with failed devices is feasible under fault-tolerant operating capabilities of an associative processor. (This is discussed more fully in Section IV.B.) Failure modes not accommodated by these fault-tolerant operating techniques include:

(1) short circuits as determined by array contact measurement;

(2) open circuit of a through-signal path, particularly a word control signal path;

(3) insufficient critical current levels in through-signal paths due to thin metal.

The third, and final, lot of arrays undertaken before the end of the program represented experiments designed to increase both the level and the reproducibility of critical current in Sn film structure. Only nine of the 29 arrays initiated were suitable for processing beyond deposition of the Pb-on-Sn layers. The vacuum systems were subjected to partial cleanup, but this was not sufficient to completely restore reliable execution of vacuum steps.

Of the nine arrays completed and tested, only three resulted in potentially operable units after short clearing. Two arrays were unshorted but had an open bit line; the third retained one short, but no open lines. Although this lot was relatively unproductive of useful arrays, the level and reproducibility of critical surface current density of Sn was reestablished. The desired critical gate current is 45 mA per 0.001 inch. Less than 35 mA per mil is too little for designed circuit operation; there is no practical upper limit on this parameter.

Thus, of the 59 arrays initiated, four were rendered operable for a 50-bit word length, five for 49-bit word length, and three for at least 45-bit word length. Critical current levels, although lower than desired because of the thin Sn film, allowed seven of these arrays to be operated in the intended associative processing modes.

In summary, short circuit failure problems which had prevented proper structuring of large area TIAP arrays have been identified and eliminated. The corrective methods used have not adversely affected superconductive properties of the Pb and Sn circuitry, including interlayer contacts. Modest yield can be achieved using laboratory-scale techniques. When proper cleanup practices are routinely used for the vacuum equipment, yield will improve significantly above the 10% level experienced during the accelerated experimental fabrication of the final program months.

Fault-tolerance is a desirable, if not a mandatory, operational quality in circuit design and structural apportionment if realistic yields of large area arrays are to result. Contamination sources in processing ambients must be minimized to reduce the excessive number of aborted arrays experienced in this program; however, total elimination of these effects is an impractical objective.

D. Support Functions

1. General

Array fabrication has necessarily commanded most of the technical attention in cryotron research and development programs. Given the means of producing the arrays, however, we still must solve the problems of interconnecting and packaging, signal processing, and cooling. The following subsections describe the means, either developed and proved, or projected, for accomplishing these support functions for the 5000-word ADP. Preferred pulse current driver and sense amplifier designs are presented.

Figure 20 illustrates the relationship of the several component assemblies which will comprise the cryogenic package and data link for the 5000-word ADP. The arrays are assumed to be grouped six to a tray, with a total of 24 trays providing the associative storage capacity desired. Signal flow is along 117 parallel paths strung through all words in the processor. Flexible strip transmission line, photoetched from doubly Pb-clad Mylar laminate, serves for interconnection between arrays and trays, and to the low temperature junction box. Arrays are superconductively contacted by pressure actuation.

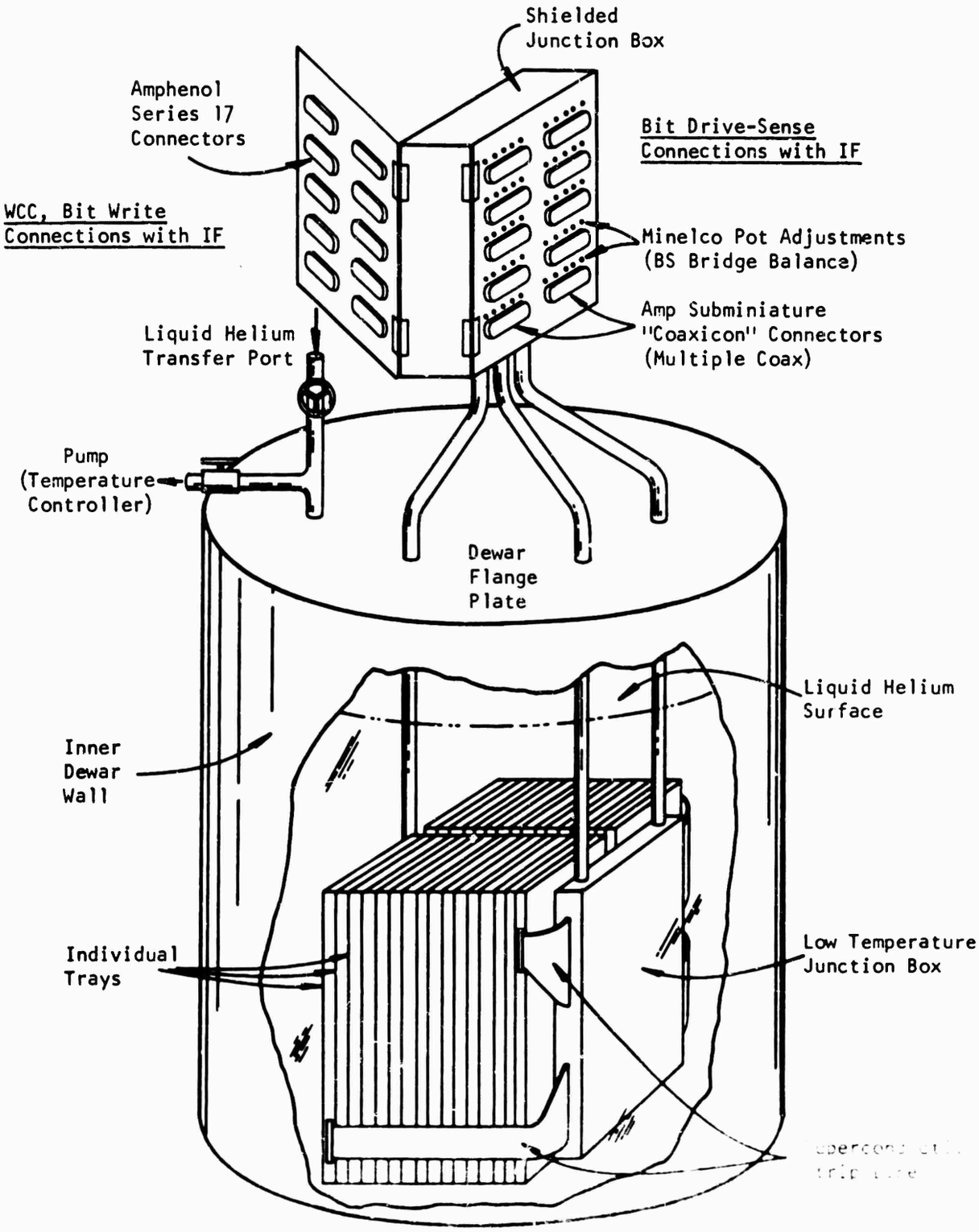


Figure 23. Major

The low-temperature junction box provides the means for transition between the multiconductor stripline and the twisted pairs which form the transmission medium to the 300°K junction box. The three thin-walled stainless steel pipes serve as low thermal-conductance supporting means for the low-temperature components, and as shielded conduit for separately channeled classes of input and output signals. The flange plate serves as a vacuum seal on the liquid helium dewar with suitable ports for passage of transmission line, and replenishment and temperature control means for the liquid helium coolant.

The 300°K junction box provides a shielded chamber in which the transition from twisted pair to external cabling forms (to the ADP interface) is accomplished. The transition is not a simple transmission medium adaptation in the case of the Bit Sense lines, but requires incorporation of adjustable potentiometers.

Open cycle cooling was to be provided by the contractor if an operable ADP unit resulted, but the difficulties still being experienced with array fabrication in mid-program made it necessary to defer the recommendation for procurement. Considerations which would govern selection of equipment are briefly mentioned in the following paragraph.

The low-temperature package requires a minimum cylinder diameter of 10 inches and a minimum head of 15 inches of liquid helium for complete immersion of the package. (This head measurement excludes the depth of the hemispherical bottom of conventional dewars.) The oversupply of liquid helium required for extended operation and the surface to flange-plate separation will strongly depend on the nature of thermal insulation around the dewar walls. The choice between direct replenishment to the working chamber or isothermal transfer from an associated reservoir will similarly affect vertical dimensions of the operating dewar.

2. Interconnection at 3.5°K

Superconductive transmission is required for 117 signal paths which thread through all arrays in the low-temperature package. Although no current switching loops extend between array boundaries, minimizing inductance through use

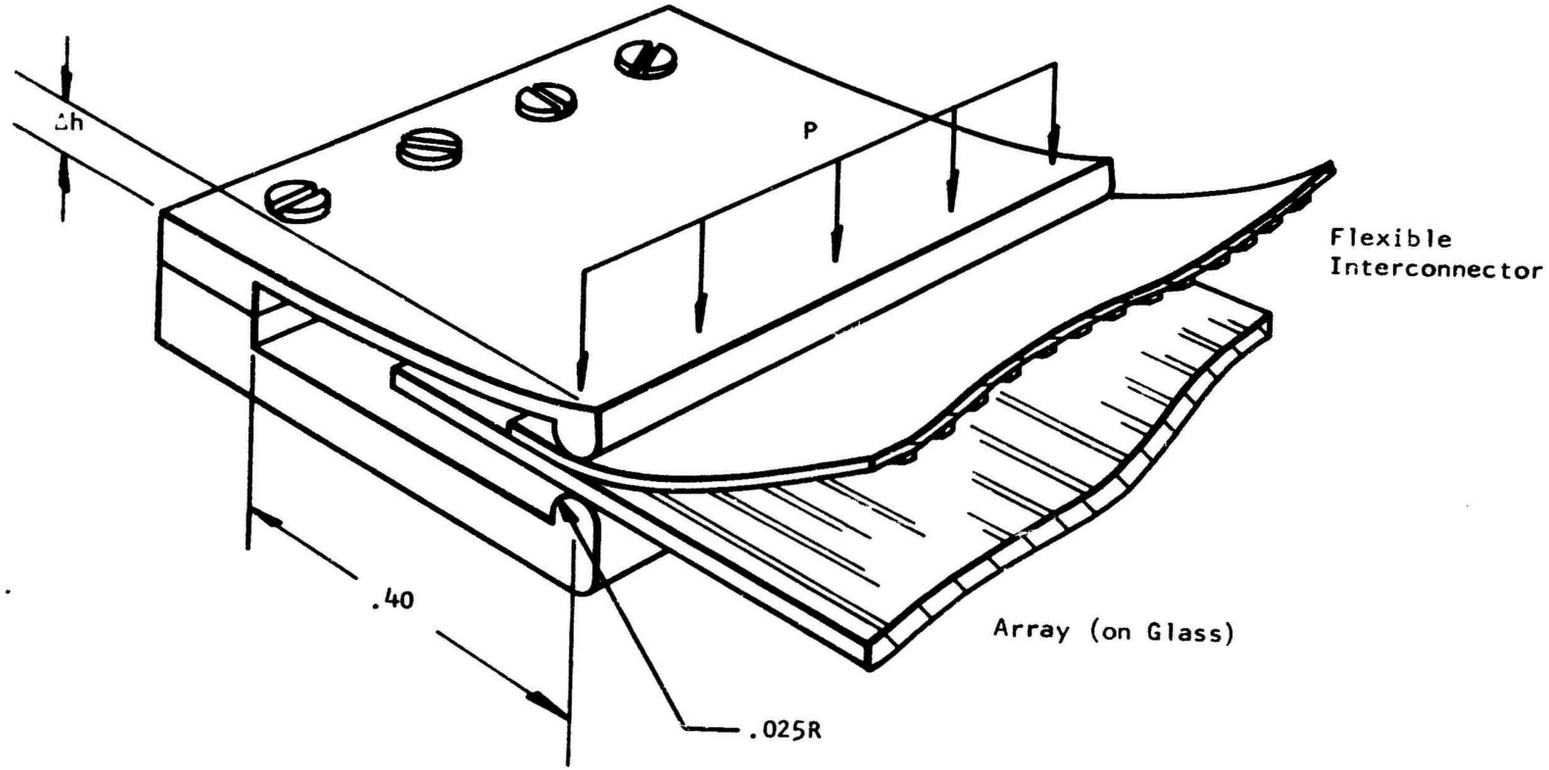
of diamagnetic stripline configurations minimizes crosstalk between closely spaced signal paths.

The 117-conductor stripline is formed from a laminate comprising 0.0008-inch thick Pb bonded to both sides of 0.005-inch thick Mylar. The Pb layer on one side is kept intact as the shield plane, and the reverse side is photoetched to the desired connector pattern. Where interconnector ends are to be mated with thin film lands (2.0 μm thick) on the arrays, connector line widths must be identically formed to 0.007 inch width on 0.014 inch centers. Conventional photomask preparation methods are used to define all connector patterns to be described. Dilute nitric acid is a satisfactory etchant if residues are prevented from accumulating by frequent water-spray rinses during the etch operations.

Figure 21 illustrates the clamp design used successfully throughout this program to actuate superconductive pressure contact between flexible connectors and arrays produced on glass substrates. The spring-loaded beam provides ample pressure to ensure superconductive contact by surface oxide breakthrough at all contact points. Contacting loads are uniformly distributed in this configuration to prevent bending moments in the glass substrate.

Since this clamp design was introduced, more than 400 arrays have been individually tested and operated with no glass substrate breakage and no instance of nonsuperconductive contact. More than 100 associative processor arrays have been subjected to two or more connect-disconnect cycles for repeated low-temperature test and operation without evidence of contact degradation. With careful handling at the time of alignment of connector and array lands, up to five reliable connect-disconnect cycles are practical before the 2 μm-thick lands of the arrays require rebuilding (redeposition and photoetch is practical).

Experience with multiple arrays was limited because of the relative scarcity of operable specimens until late in the program. However, one pair of 20-word, 500-cell arrays was successfully interconnected and operated during the tenth program month. Superconductive contact was also reliably



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P = 28#/inch
Δh = .025 inch (max.)
Beryllium Copper Alloy 25 - Condition 1/2 hard/Spec QQC-533

Figure 21 Clamp design

obtained across a 100-line span through four interconnected substrates containing prototype lands and through-signal paths. This experiment involved eight clamped contacts in series.

These observations, though not the result of a controlled experiment, tend to support optimism for use of this interconnection means in the final ADP assembly.

The following description of projected interconnection and modular assembly practice will require reference to Figure 20 for clarity. Figure 22 shows four TIAP arrays interconnected to form a tray module (6 TIAPs would ultimately form a tray) which would be vertically positioned in the test dewar as a unit in a multiple-tray, or stack module. The use of U-shaped array interconnectors minimizes the likelihood of gaseous helium accumulating over critical superconducting circuit regions. The free connectors associated with end arrays in the tray would then be pressure-contacted to corresponding free ends of adjacent trays in a stack, thus threading signal flow throughout the assemblage of arrays.

Two additional connector types are required to join the four free connectors of the assembled stacks. The first, shown in Figure 23, can be considered to interconnect the outgoing signal paths of one stack to the incoming signal paths of the other stack. This will be referred to as the midpoint junction in all signal processor paths. It provides expanded contacts for auxiliary twisted-pair-to-stripline junctions required at the midpoint of all Bit Sense (BS) lines and the RMR control line to permit the balanced-bridge-read described elsewhere in this report. A second connector, shown in Figure 24, completes the ring of interconnection for the two stacks and provides expanded contacts for twisted-pair-to-stripline junctions for all end-point data and control paths. The junctions between twisted-pair and expanded contacts on these connectors may be made either by direct soldering of leads or through quick-disconnect pressure contact with a circuit board to which the twisted pairs are permanently soldered from the reverse side. Both methods have been used successfully; however, the latter is preferred for its quick-disconnect feature.

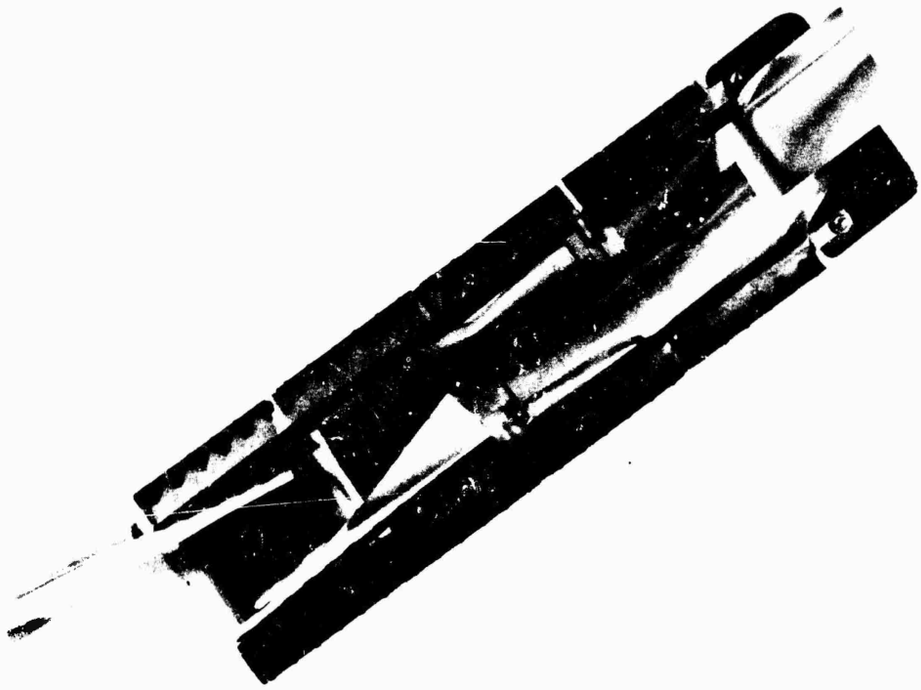


Figure 22 Representative tray module consisting of interconnected TIAP arrays

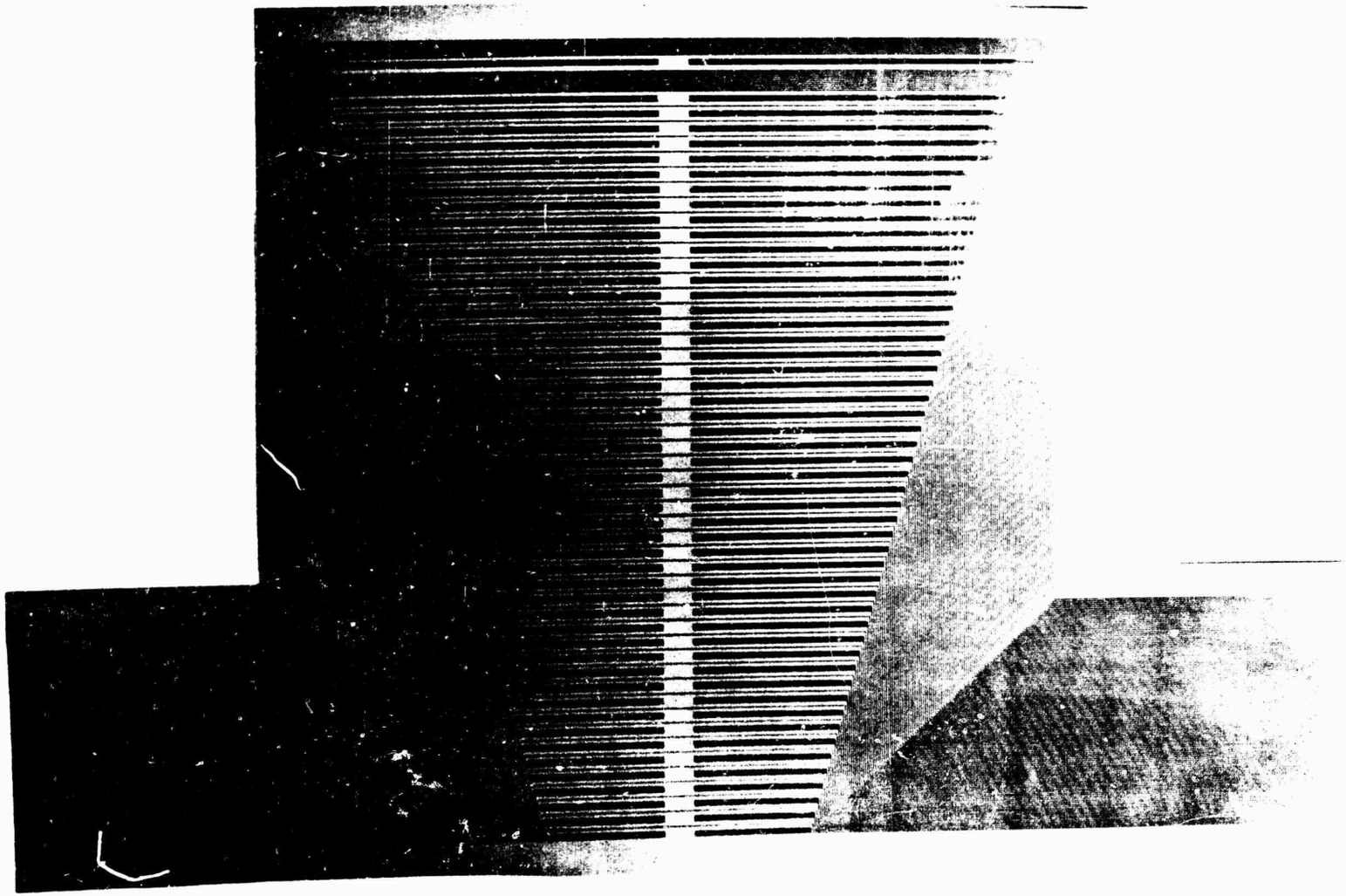


Figure 23 Midpoint junction connector in cryogenic assembly

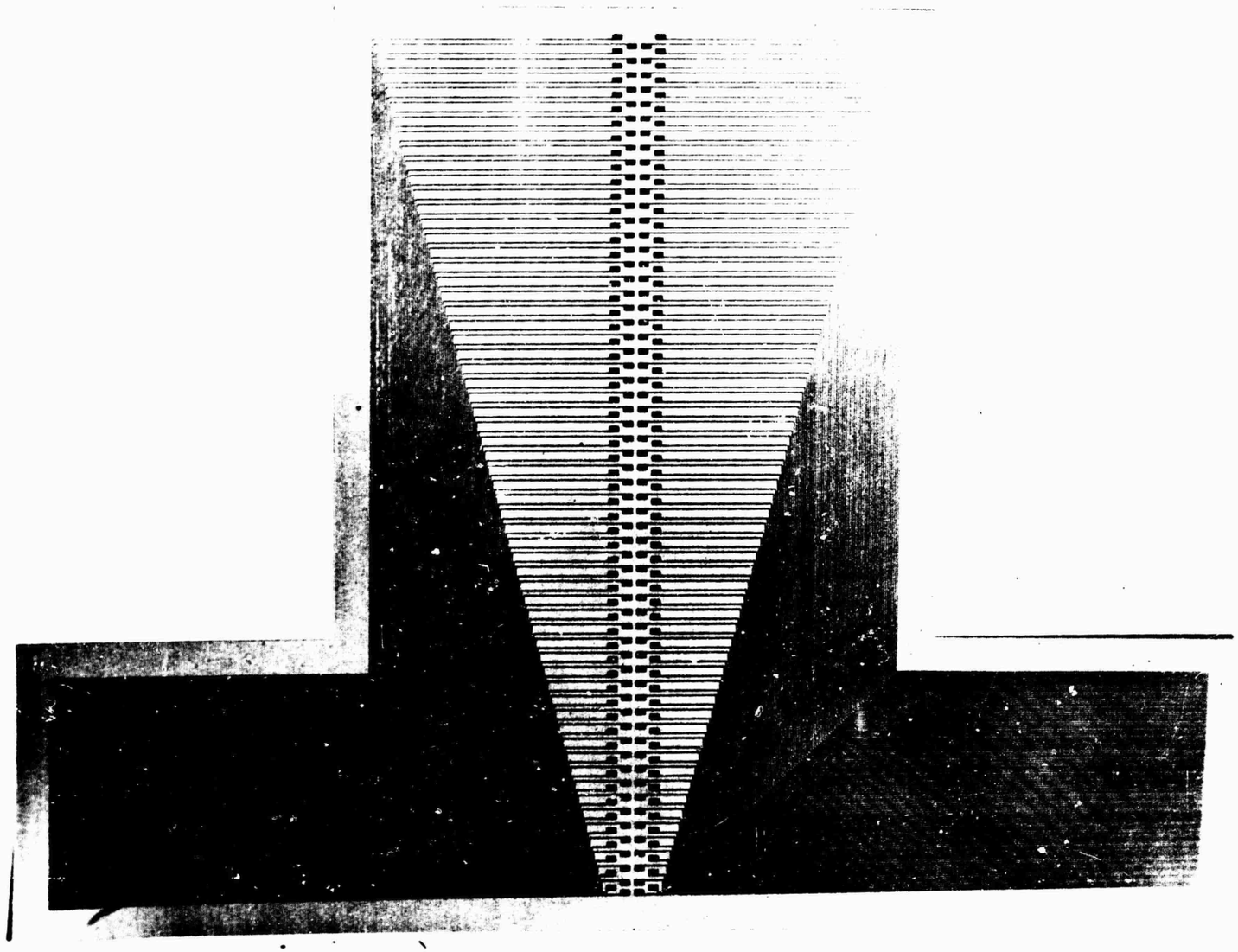


Figure 24 Endpoint junction connector in cryogenic assembly

The foregoing discussion of a projected means of modular assembly of arrays is presently only a design concept; however, its construction incorporates no electrical or mechanical capabilities which have not been successfully demonstrated in this program. The reliability of the more than 300 clamp contacts for interconnection of 117 signal paths must remain suspect until proved in practice. The existence and severity of thermal gradients and/or localized thermal transients are similarly questions which cannot be answered at this time.

Preliminary calculations of module dimensions are:

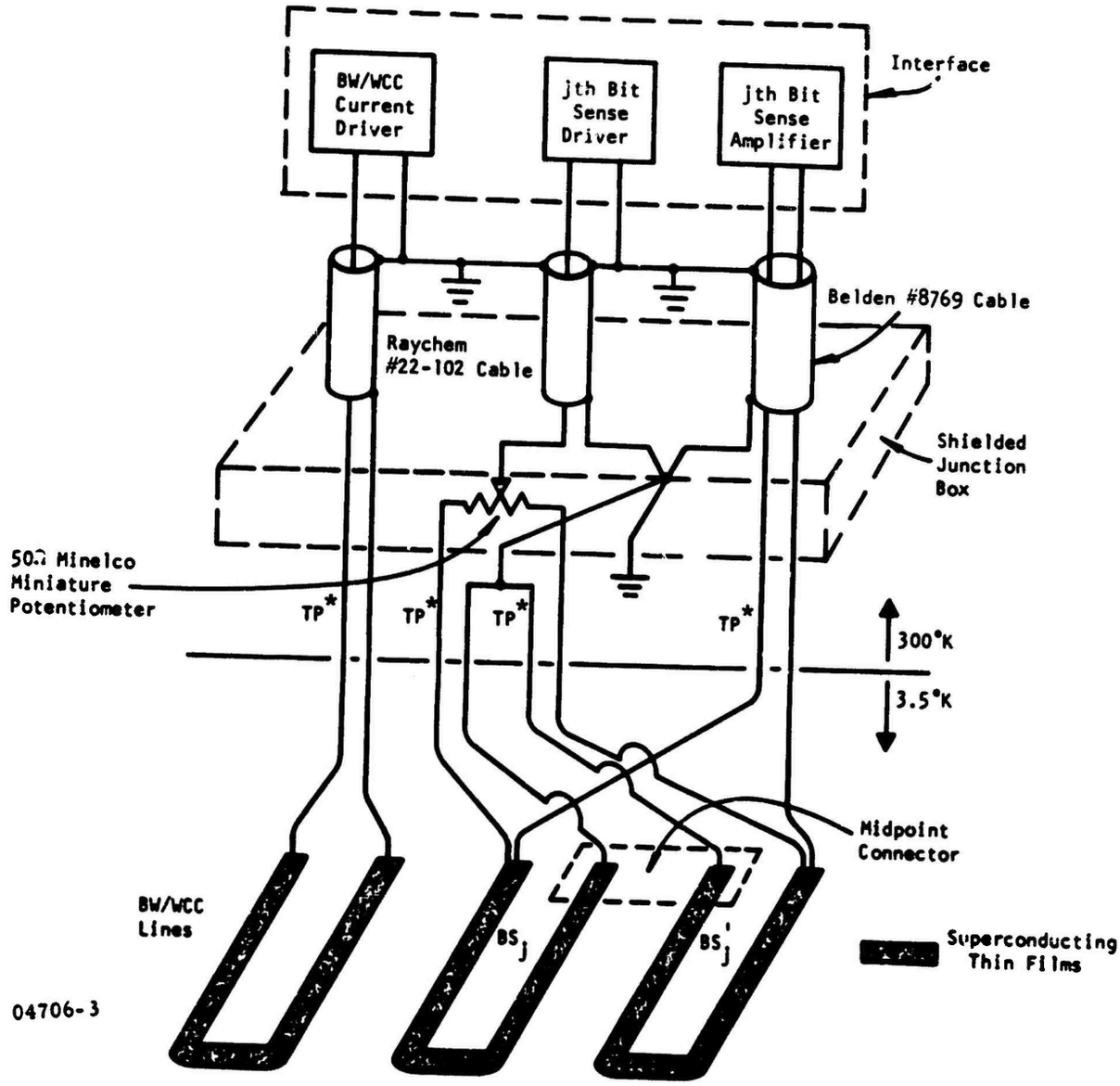
(1)	Tray (6 TIAP arrays):	3.5 inch x 0.5 inch x 13 inch high
(2)	Stack (12 trays):	3.5 inch x 7 inch x 13 inch high
(3)	Junction Box:	4 inch x 1 inch x 13 inch high

Thus, the complete assemblage for immersion in liquid helium would occupy a solid cylinder 10 inches in diameter and 13 inches high.

3. Data Link

Figure 25 shows representative electrical connections between 300°K electronics and superconducting film circuitry which must be accommodated in the data link structure. The simplest type of connections are those for Bit Write (BW) lines and control circuitry functions. These are straightforward out-and-back paths in an unbalanced transmission line configuration. Grounding practice shown for these and all other data link signal path types were experimentally determined to yield a minimum ground loop noise configuration for the particular installation used for test and operation.

The read scheme shown in Figure 25 is required to accommodate the split memory, balanced-bridge configuration developed in this program to decouple the sense amplifiers from noise due to the bit sense drive pulse which activates cryotron read-out. In effect, the cryogenic processor is divided into two halves with respect to its word capacity during read operations. For example, BS_j represents the superconducting read path for the jth bit of words 1 through N/2, and BS_j' the jth-bit read path for the balance of words of an



* TP implies twisted pairs of #38 Nylclad Wire (10 turns/inch)

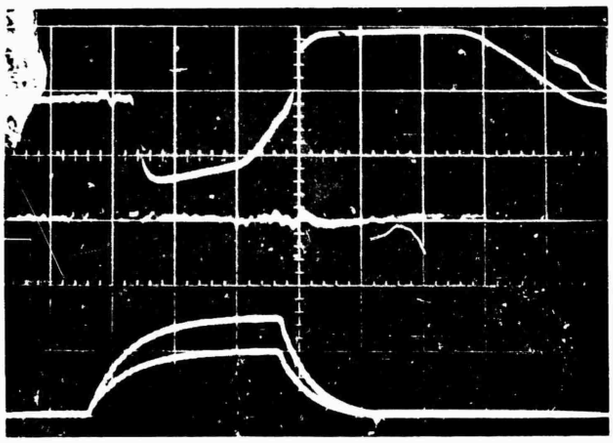
Figure 25 Representative electrical connections relating room-temperature drive and detect functions to cryogenic circuitry

N-word processor. These two paths are predominantly inductive and are necessarily symmetrical in structure and electrical properties. BS_j and BS_j' form adjacent inductive legs of the impedance bridge. The other legs are the resistances to either side of the tap of the 50-ohm balance potentiometer situated in the 300°K junction box. Read-out is potentially enabled then for words related to either BS_j or BS_j', but not both, simultaneously. The voltage output signal (nominally 500 μV) which occurs if a resistance (nominally 5 mΩ) is restored in the enabled BS leg appears as a substantial imbalance at the output terminals of the bridge, situated across both legs of the BS line. Conversely, the Bit Sense Driver (BSD) pulse and incidental noise associated with its line are effectively self-cancelling with respect to the voltage output terminals. The 5 mΩ restored resistance is a negligible factor to the impedance balance of the bridge because of the very large intrinsic resistance and inductance of the four bridge legs.

Figure 26 shows the response of the sense amplifier output for two BSD amplitudes, one just insufficient to cause resistance restoration, the other corresponding to 50% overdrive. The overshoot of the sense amplifier following BSD pulse termination was caused by the use of a decoupling transformer situated at low temperature and wound to provide 3X voltage amplification.

The marked improvement in both general noise sensitivity and signal-to-noise ratio during read operation is apparent when contrasted to the results obtained when voltage output and BSD lines share common endpoint terminals of BS, treated as a single line. This was the early program design concept, intended to achieve noise suppression of BSD pulse activity through frequency discrimination properties of the sense amplifier. Figure 27 shows the response of this direct-drive read-out configuration only for a 5% overdrive condition. The sense amplifier output is initially saturated to both polarities by feed-through of the BSD pulse; the read-out is the unstable response that follows. This configuration is obviously impractical because of the signal instability, minimal overdrive permissible, and time delay required for signal acquisition.

Figures 28 and 29 are representative of construction practices for the 3.5°K and 300°K junction boxes of the data link. The unit shown is the one

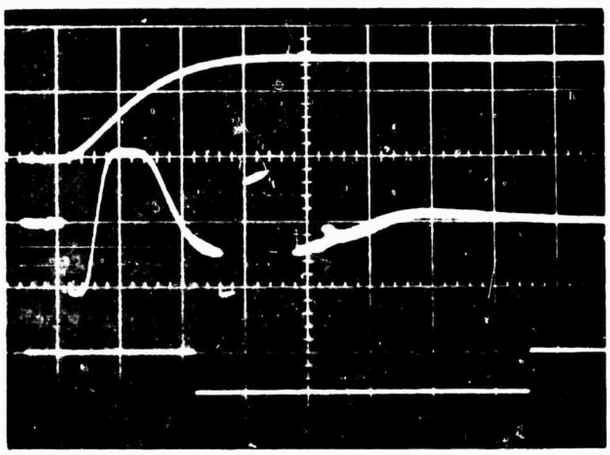


Sense Amplifier - Gate Switched
(2.0 V/cm)

Sense Amplifier - Gate Not Switched
(0.5 V/cm)

Bit Sense Drive
(200 mA/cm, 0.4 μsec/cm)

Figure 26 Bridge read-out test results



Bit Sense Drive Current
(2 V/cm, 4 μsec/cm)

Sense Amplifier Output
(2 V/cm, 4 μsec/cm)
(C_{in} = 0.02 μF, R_{FB} = 5.6 kΩ

Read Strobe (2 V/cm, 4 μsec/cm)

Figure 27 Direct read-out test results

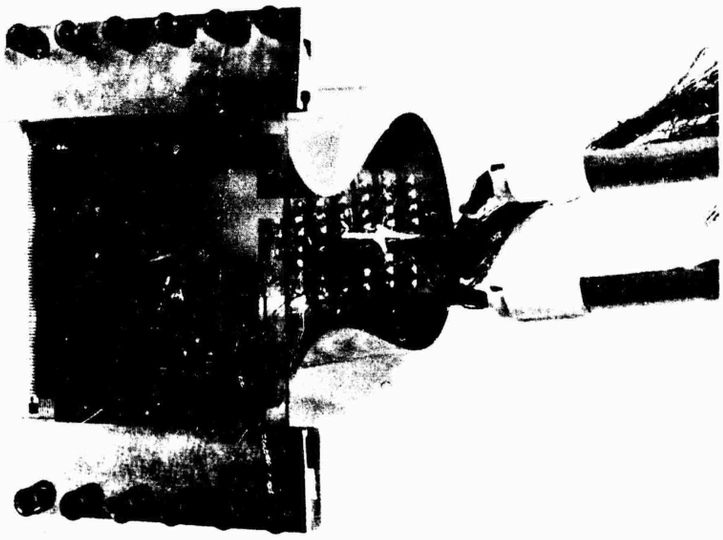


Figure 28 3.5°K junction between twisted pairs and superconductive transmission line for single array test and operation. For multiple array operation, the assembly would be rigidly affixed to pipes for support.

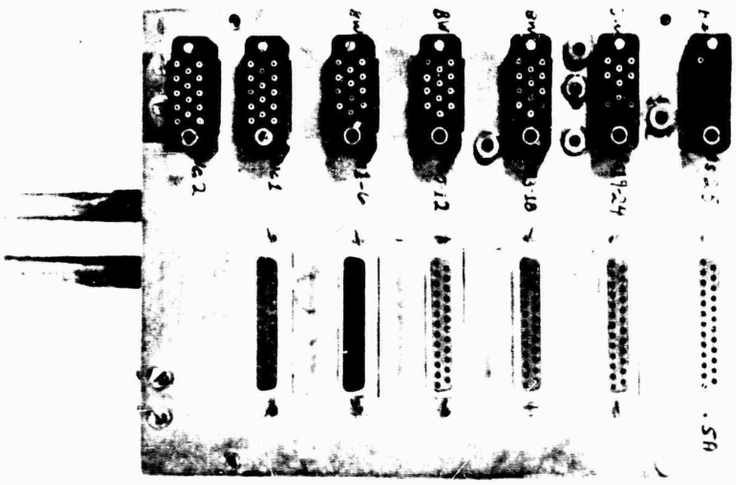


Figure 29 300°K junction between twisted pairs and cabling to exerciser (not shown). Note that five-bit sense lines have been adapted for balanced-bridge read, evidenced by presence of balance potentiometers.

used for pulse test and operation of the 25-bit word length arrays, first operated in the tenth program month. The unit actually accommodates signal processing of any 25 bits of word length of the established associative processor design, since word control functions are independent of word length and number of words present. This unit has therefore been used also for final design evaluation of the concept with TIAP arrays (50-bit word length). If the ADP program were continued, a data link for TIAP word length, of the form suggested in Figure 20, would be constructed. Additional details of preferred construction practice include:

(1) use of thin-walled, stainless steel pipe to enclose twisted pairs between 300°K and 3.5°K junction boxes, and support of suspended array assemblage;

(2) distribution of twisted pairs among three pipes according to signal transmission function, i.e., one for BSD inputs, one for outputs to sense amplifiers, and the balance to a third pipe;

(3) continued use of RTV #210 potting material as a vacuum seal at the 300°K entry of twisted pairs to their respective pipes;

(4) distribution of connectors and miniature potentiometers between two hinged faces of the 300°K junction and shield box to facilitate access;

(5) enclosure of 3.5°K junction between twisted pairs and respective strip transmission lines, principally for protection in handling.

It is felt that the present data link design concept is sound. Subsequent engineering design would be necessary principally to improve structural characteristics.

4. Pulse Current Drivers

The pulse drivers were designed to generate a large fast-rise current pulse into a low-impedance line. Since the application was developmental, provisions were included for full range amplitude adjustment, control of rise and fall times, and monitoring of the output current waveform. Two types of drivers were developed. The first has a bipolar output and two inputs for

enabling the respective output polarities. The second is monopolar with a single enable input and is essentially half of the bipolar driver.

The final bipolar circuit (Figure 30) comprises two pulse power amplifiers driving into the same load. Essentially, the circuitry above the dashed line in the figure generates the positive output current, while that below the dashed line generates negative output current. A monopolar driver is merely the portion below the line. Each half of the bipolar can be further divided functionally into a low-level processing section (Q_1, Q_3, Q_5 or Q_2, Q_4, Q_6) and a power driver section (Q_7, Q_9 or Q_8, Q_{10}).

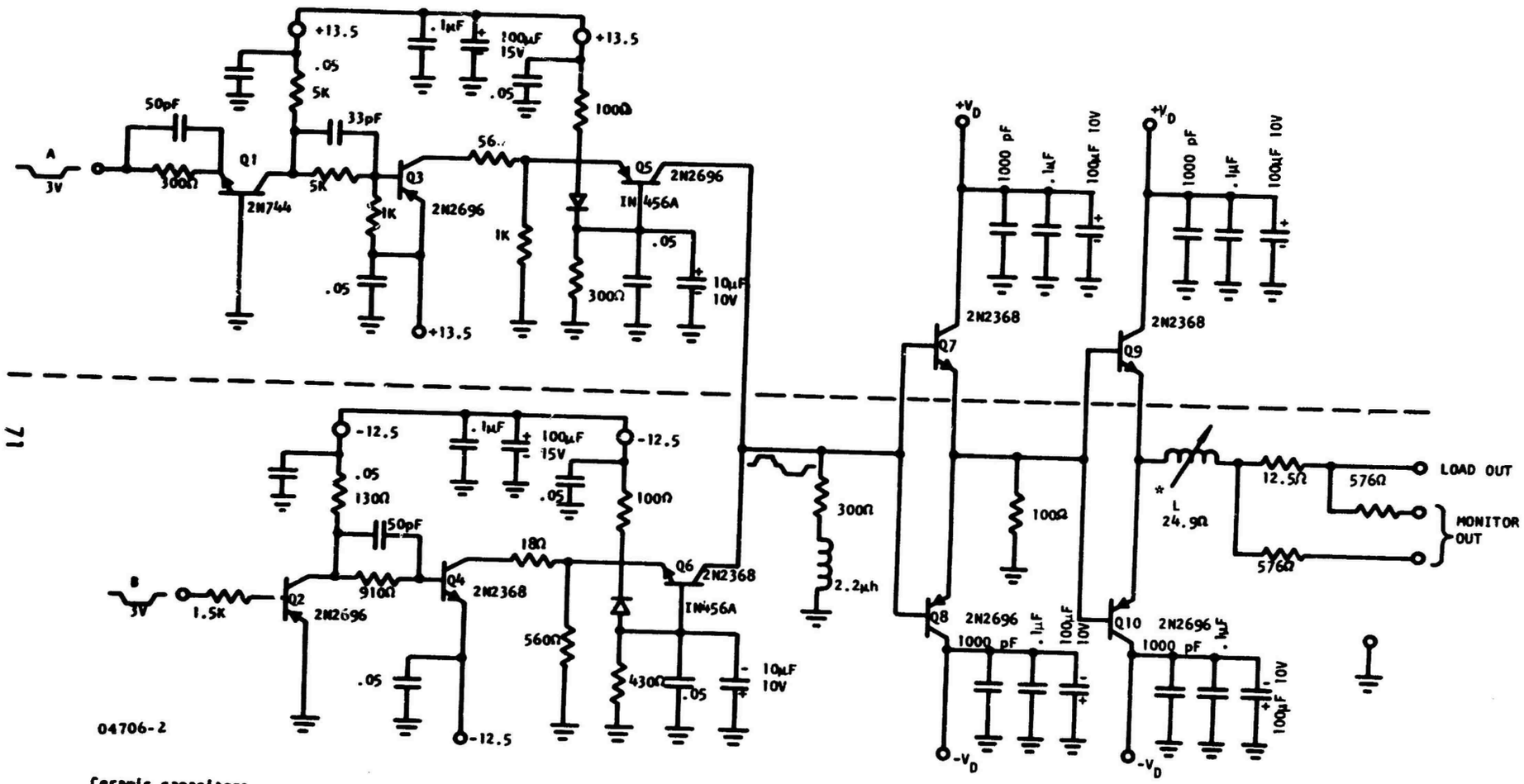
The function of the low-level section is to voltage-amplify the input signal by about 4, improve rise and fall time, invert and level shift if necessary, and present a high output impedance to the power section over the full dynamic range of the output. The relatively high collector-base breakdown voltages of transistors Q_5 and Q_6 permit these common base stages to exhibit a high output impedance over the full signal swing of about 22 V.

The power driver section is simply a pair of complementary emitter followers to provide current gain, further waveshaping, and a low output impedance. The amplitude of the pulse load current is dependent on the value of V_D and thus may be externally programmed. Rise and fall times are readily adjusted from the lower limit set by the driver transistors to an upper limit governed only by the maximum allowable size and resistance of the series inductor in the output line. The series resistor in the output lead matches the drive cable impedance when the driver is on, limits short circuit current, and provides a means of current monitoring. The current monitor voltage can be sensed remotely with two 50-Ω terminated cables from the monitor terminals.

The measured performance of this circuit with a negative 3-volt input pulse is typically:

Output pulse amplitude, variable from 0-4 volts into 12-Ω cable;

Output rise and fall time, variable from 10 nsec to 5 μsec using a maximum inductance of 100 μH;



Ceramic capacitors.
All resistors 1/4 W and in ohms unless noted (K = 1000).
* Inductance to be selected for rise and fall time.
Bipolar Current Driver (BCD).
For monopolar, use circuitry below dashed line only.

Figure 30 Current pulse driver schematic

Negligible pulse sag with 500 μsec width;

Duty cycle (per polarity), 30%;

Maximum steady-state input turn-on current, 10 mA.

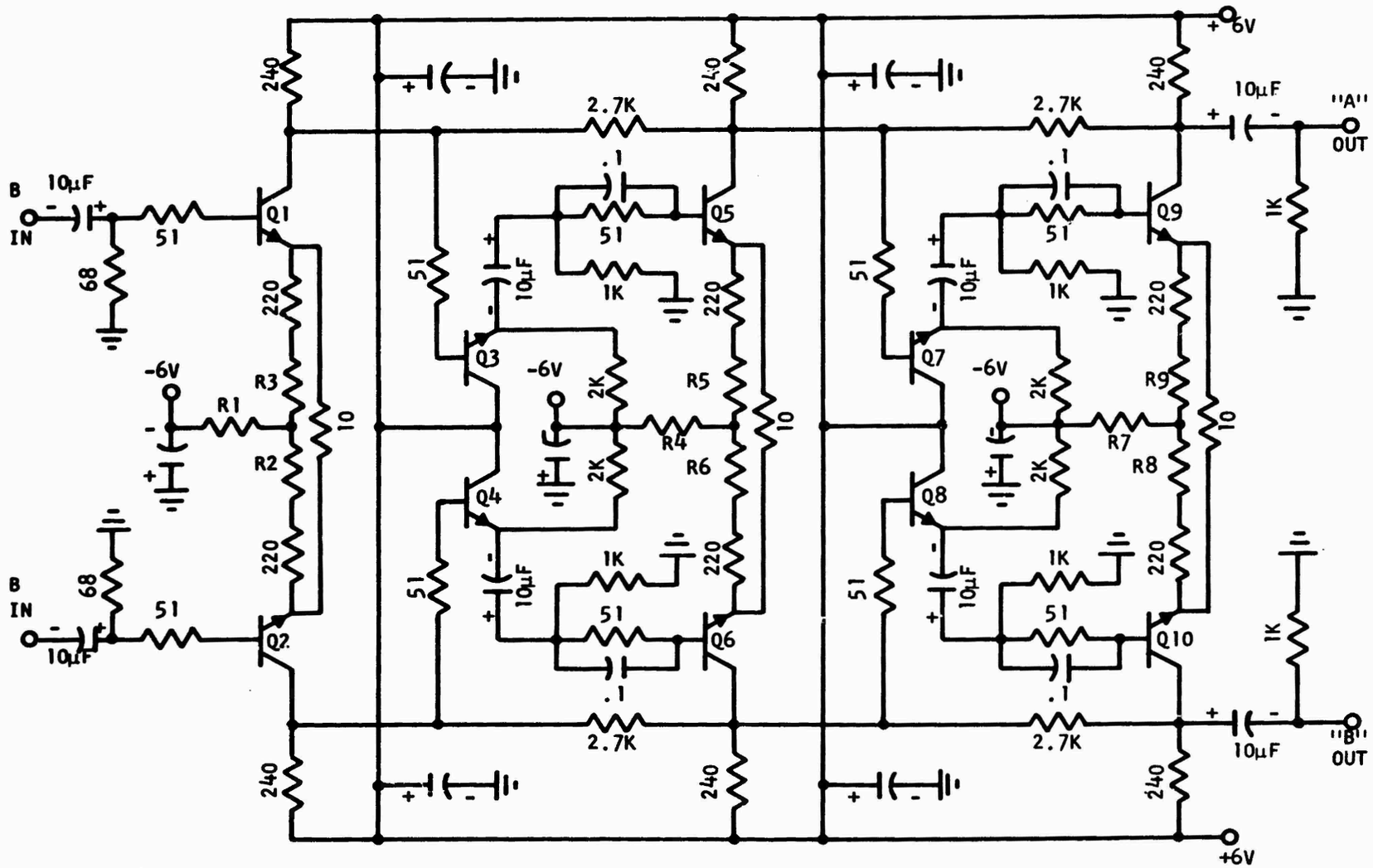
5. Sense Amplifiers

The sense amplifiers are of a generic design class commonly used in memory systems. They may be characterized as wide-band, high-gain, low-level, low-noise feedback, differential pulse amplifiers.

The circuit, shown in Figure 31, is basically a series of balanced stages. Each stage comprises a balanced common emitter (CE) pair, providing voltage gain and driving an emitter follower (EF) pair for low drive impedance into the next stage. Negative feedback to lower noise, increase bandwidth, and improve stability is provided between the outputs of each CE pair to the inputs of the succeeding EF pair.

A number of features make this amplifier particularly suitable for use with the ADP. The input impedance is chosen to approximately match the memory output transmission line. The amplifier output impedance, about 240Ω, is low enough to drive nearby logic; an additional EF pair can be used to drive long cables.

Amplifiers of this type are often direct-coupled to avoid differentiating signal and noise and thereby increasing read cycle time. Unfortunately, this advantage is offset by time and temperature stability problems and by greatly increased dependence of performance upon transistor and other component parameters. The compromise chosen for the ADP amplifiers is RC-coupling between EF outputs and CE inputs using very large (10 μF) capacitors. The resulting low-frequency response is sufficient to avoid differentiating any signal or noise voltages which occur in this application, and a marked independence of operation on time, temperature, or component parameters has been observed. The low output impedance of the EF pairs permits driving the distributed shunt-to-ground capacitance of the coupling capacitors without apparent rise and fall time degradation.



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Note: R1 through R9 are experimentally adjusted to obtain correct bias point.

Figure 31 ADP sense amplifier

Typical operating results with the circuit of Figure 31 using 2N2368 transistors for Q_1-Q_{10} include the following:

Gain, 1000

Random noise level, referred to input, less than 50 μV

Saturation input signal level, 2 mV

Rise and fall times, 15 nsec

Pulse lengthening distortion, 10%

Overshoot and undershoot, less than 5%

Maximum duty cycle with pulse width 500 nsec or less, 50%

Maximum duty cycle with 2 μsec pulse width, 33%.

Except as noted, all the above measurements were made with an input pulse having a rise time of 1 nsec, a width of 100 nsec, and an amplitude of 1 mV, transmitted through a simulated read data link.

SECTION IV
ARRAY TEST AND OPERATION

A. General

Four distinct test and operation activities can be identified for cryogenic arrays taken singly or in multiple array assemblies:

(1) resistance measurements at 300°K to determine the structural character of a freshly fabricated array;

(2) short clearing and critical current assessment at 3.5°K, combined with parallel-by-word exercise of word control circuitry to ensure operability of fault-tolerance control circuitry;

(3) pulse mode exercise of all array circuitry at 3.5°K, either to determine acceptance of a given array for operational use or to explore limits of operability of specimens to determine acceptance criteria;

(4) pulse mode operation of arrays and subassemblies under prototype computer control for programmer evaluation or use.

Test equipment for the first three activities has been provided and used extensively; however, the interface required to permit controlled operation by a Univac 1218-M was deferred pending solution of array fabrication problems which existed until late in the program.

Part IV.B of this report will describe fault-tolerance characteristics of the design and its relationship to most prevalent failure modes. Subsequent subsections will discuss test activities, equipment, and results.

B. Fault-Tolerant Operation

The near term probability of achieving perfection in large area arrays containing high density and count of devices is extremely low, whether in cryogenic or in other technology. To increase useful array yield, therefore,

one must find methods of desensitizing the function of the array to the presence of some failed devices.

This fault-tolerance is a practical attribute for cryotron circuitry in associatively organized data processing applications. The cryogenic associative memory (CAM) function, as described in Section II, does not explicitly recognize the existence of the preferred fault-tolerant operating mode which has evolved from experience with large area arrays. This was not an oversight but an intentional omission because we did not know what dominant failure modes would be encountered.

The following observations are made specifically with respect to the ADP organization selected in this program.

(1) There is no occasion for direct interaction of logic, control, and memory functions between physically adjacent words in an associative processor.

(2) Through-signal paths of the array must remain superconductively continuous, since they pass serially through all arrays of the CAM.

(3) Line-to-line or line-to-ground plane shorts may not be tolerated relative to the through-signal paths.

(4) No word of the CAM can be effective with respect to write, search, or read operations if the M state of its Match Register (MR) flip-flop is permanently inhibited.

Coupled with these observations concerning organization and constraints for operation are the following factors relating to large area cryotron array fabrication and the dominant failure modes as identified in this program.

(5) Insulation is provided by redundant layers applied and patterned with separate photomasks to statistically minimize shorts caused by randomly occurring pinholes in photomask emulsions and thin film insulators.

(6) Photomask masters are photographically retouched to eliminate emulsion pinholes (light leaks) at the risk of introducing superfluous opaque material.

(7) Redundant exposure and development methods are used for separately prepared photomasks to statistically remove the effect of superfluous opaque regions in photoetch patterning.

(8) Any short circuit can be removed by capacitive discharge, as measured from the array contacts.

(9) Short circuit removal does not destroy desired thin film structure when there is no high conductance intra- or interlayer shorting; fabrication methods now practiced minimize the occurrence of such shorts.

(10) Open circuits due to fabrication are extremely infrequent; their occurrence incidental to short circuit removal has been minimized, as noted in item (9).

The preventive and corrective means cited above for array fabrication [items (5)-(10)] in effect limit the short circuits that occur to a class that can be nondestructively removed. Thus, only open circuit fault conditions must be tolerated. Further, the yield acceptance criterion of item (3) is met by removing all short circuits in the arrays. An open circuit in a through-signal path would constitute a catastrophic failure, as in item (2), but this is not a serious yield-loss factor in practice.

Items (1) and (4) remain to be considered, but these are statements of fact for the CAM design. Thus, yield improvement through operational fault-tolerance hinges on the ability to sense the presence of a device failure and to permanently inhibit the M state of the associated word's MR flip-flop in subsequent processor operations.

The basis for fault-tolerant operation is recognition of not only the "Occupied" and "Vacant" states, but also the "Failed" state as an associated, meaningful word status. In addition to satisfying the Match criterion with

respect to a Mask-Argument specification, words must also Match with respect to occupancy status in the present circuit design. This requirement is implemented by an additional storage cell contained in the word control circuit (WCC) segment, which can reset a word's MR flip-flop to the $\overline{M}$ state if the appropriate occupancy status is not present. Because the cryotron storage cell has an inherent ternary capability, the three-state description of word status can be accommodated with a single cell as before. The Action Register (AR) of the present CAM design is one method of incorporating fault-tolerant control in CAM operation and is so used in TIAP test and operation. The A or $\overline{A}$ current circulation states are associated with "Occupied" and "Vacant" states, respectively. The Null state (no trapped current in the AR cell) is associated with the "Failed" state.

A brief, parallel-by-word exercise of the CAM circuit functions identifies words containing failed elements for all functions except Read. Words containing failed Read circuitry can be identified only by serial-by-word exercise in conjunction with Ladder Load operation of the CAM.

The parallel-by-word exercise results in an A state, circulating current in the AR cells of operable words. After subsequent Ladder Load and Read tests, both the A and $\overline{A}$ states are used to signify unfailed word status, since they are both current circulation states, differing only in sense. These states are appropriately associated with unfailed word Occupancy or Vacancy. The Set MR (SMR) function of the design discussed in Section II is replaced in all operations by MMOAOE and the appropriate choice of AD(A) OR AD($\overline{A}$) to set to M state only occupied or vacant words in memory. This automatically excludes failed words whose AR cell is in the Null or non-storage state.

The nature of the failed-word identification exercise will be described more fully in the subsections concerning structural and functional test procedures and equipment.

C. Structural Test

Arrays of several thousand active elements each pose a challenging test and characterization problem from the standpoint of test equipment complexity

and minimum cost procedures. In the case of the CAM function, the unit array must be properly responsive to 2^{10} unique commands with respect to a 50-bit data word length. The translation of commands to appropriate control pulse sequences suggests the presence of a stored program computer for efficient test purposes; 50 driver-detector pairs are similarly indicated. In view of these factors and the not inconsequential cost of providing the liquid helium ambient, a hierarchical test concept has evolved, as outlined in Section IV.A. This subsection will deal specifically with the first two levels of test cited. These essentially assess the structural propriety of an array.

Room-temperature resistance measurements are the least expensive and time consuming to make. They also provide an immediate indication of the quality of an array. An apparatus for these measurements consists of a suitable cable and selector switches to permit 4-wire resistance measurements between any of the 117 pairs of contacts to the array. The freshly completed array is pressure-contacted to the cable connectors and the resistance measurements recorded for array contacts selected as follows:

(1) top (of array)-to-bottom for each line
(2) top-to-top by adjacent contact pairs
(3) bottom-to-bottom by adjacent contact pairs
(4) top of all lines to top of ERDC and MRDC
(5) bottom of all lines to bottom of ERDC and MRDC.

Item (1) not only qualifies continuity of vital through-signal paths, but also provides a coarse check of adequacy and uniformity of metal film depositions. Items (2)-(5) characterize the number of short circuits in the array and may be used to compute location of each within the array when the number of shorts is nominally less than 50, as is now the case. The presence of high conductance short circuit filaments is readily detected.

The criteria for continuing an array to subsequent low-temperature acceptance test are:

(1) continuity of all through-signal paths

(2) acceptable through-signal path resistances and variances (compared to established values) for each type of line

(3) less than 50 (nominal) shorts whose minimum resistance is established from experience.

Item (3) is subject to adjustment in accordance with the state of process development and economics of test. Although short circuits are presently cleared only at 3.5°K ambients, limited experiments with arrays produced in the seventeenth program month suggest that nondestructive short clearing may also be done at room temperature, since only low conductance shorts are present.

An array which passes the room-temperature tests is next taken into the liquid helium bath for the second level of test activity. The purpose of this test is to clear all short circuit paths and recheck through-signal path continuity, then assess functional operation of all cryotron circuitry except that for Read operations. The 4-wire measurement and selector switch configuration for room-temperature test is again used; however, appropriate power supplies, meters, and switching provisions must be accommodated to perform the parallel-by-word cryotron circuit operations.

The first operation performed is capacitive discharge clearing of all short circuits. This is presently done by reference to the previously prepared short circuit "map" for the array. The most recent experience indicates that a 1 μF capacitor charged to 6 volts is adequate to clear most of the shorts encountered; however, past experience indicates that a 22-volt charge is rarely destructive to desired film structure. The lower capacitor charge is used initially with each short circuit path and is increased as necessary to remove the short.

When all short circuits have been removed, each through-signal path is strobed with the minimum acceptable current for which it must remain superconducting. Typically, BS lines and the VOM line must have critical currents in excess of 100 mA; BW lines and all others must carry at least 300 mA. These

measurements also assure that continuity has not been lost in a through-signal path due to short clearing.

The array is next subjected to a brief sequence of level-logic operations which directly assess the quality of the cryotron circuitry for fault-tolerant CAM operation, as described in the previous subsection. The CAM function described in Section II is amenable to fault-tolerant operation through use of the Action Register (AR) as the ternary word status cell. The A and $\overline{A}$ states are associated with Occupancy and Vacancy status, respectively, and correspond to oppositely circulating stored currents. The Null state of an AR cell is associated with "Failed" status and corresponds to absence of stored current within the cell.

In this use of the CAM function design, fault-tolerance hinges on the ability to inhibit the M state in a failed word's Match Register (MR) flip-flop. Therefore, it is critical that the $\overline{M}$ path of all MR flip-flops be structurally and superconductively proper. This can be ascertained by providing current (250 mA) to the Reset MR (RMR) control while monitoring voltage with respect to the MRDC (250 mA) or VOM (15 mA) line. If no voltage appears, the test has been passed. (The RMR control is a through-signal path, and therefore its continuity has been established.) A similar check for validity of $\overline{EN}$ paths in all Enable Register (ER) flip-flops is made by providing current (250 mA) to the Reset ER (RER) control while monitoring voltage with respect to the ERDC (250 mA) or VOM (15 mA) line. No voltage should appear.

Table IV lists one sequence of level-logic exercise which can then be performed to determine the existence of operable words in the array. By creating the M state in unfailed words, the number of operable words can be inferred from the analog voltage appearing across the VOM line. The sequence of operations indicated have the effect of logically AND-ing the registers of the Word Control Circuitry under all possible control combinations, then extending the AND-ing to cell storage and search operations of the data cells as well. The AR cells of words which are failed for any reason will be in their Null state; unfailed words are marked by the A state cells of the AR.

TABLE IV

REPRESENTATIVE PARALLEL-BY-WORD EXERCISE OF CAM CIRCUITRY TO DETERMINE AND RECORD THE PRESENCE OF FAILED WORD(S) AS THE NON-CONDUCTING STATE OF SUCH WORD(S)' AR CELL.

Unfailed words are assigned either the A or $\bar{A}$ stored current sense of their AR cells.

	Step Number and Description	CAM Lines Involved
1.	AR is set to A state	AD(A) with RAR
2.	Set MR to AR(A)	AD($\bar{A}$) with MMOAOE
3.	Set ER to MR	EMOE
4.	Reset AR	RAR
5.	Reset MR	RMR
6.	Set MR to ER	MMOAOE
7.	Reset ER	RER
8.	Set AR(A) to MR	AD(A) with AMOA
9.	MR set to AND of MR, AR($\bar{A}$)	AD($\bar{A}$) with MMAA
10.	Reset AR for M state true	AMOA
11.	Set MR to AR(A)	AD($\bar{A}$) with MMOAOE
12.	OR set "Occupied"	OD(Occ.) with ROR, MMOAOE
13.	Search for OR(Vacant)	OD(Vac.)
14.	Reset AR for M state true	AMOA

Note: AR(A) now identifies unfailed words with respect to all WCC functions exclusive of Ladder Load (ELDC, ELGND).

15.	Set MR to AR(A)	AD($\bar{A}$) with MMOAOE
16.	Write "1" in cells, "Occupied" in OR	{BW_i(1)}, OD(Occ.) with EMOE, MMOAOE, RER
17.	Bit-parallel search on "1", "Occupied"	{BW_i(1)}, OD(Occ.)
18.	Set AR(A) to MR	AD(A) with AMOA
19.	Bit-serial search "0"	BW_i(0)
20.	Reset AR for M state true	AMOA
21.	Set MR to AR(A)	AD($\bar{A}$) with MMOAOE
	Repeat for all 50 BW_i	
169.	Search "Vacant"	OD(Vac.)
170.	Reset AR for M state true	AMOA

Note: AR(A) now identifies unfailed words with respect to all CAM functions except Ladder Load (ELDC, ELGND) and Read ({BS_i}); the exceptions are investigated for potential failure in the course of serial-by-word Ladder Load operation for entry of unique "addresses".

The test apparatus for the liquid helium activity includes all capabilities required for the room-temperature test activity. However, separate facilities were constructed in support of this program for these two activities. The facility for liquid helium test provides toggle switch control of the fault-tolerant capabilities of an array with respect to WCC functions, but the unit has switch control only for simultaneous test of six-bit lines. The entire 50-bit word length can be investigated, however, in six-bit groups by stepping of room-temperature connectors. There was not enough time in the contract following proven solution of TIAP array fabrication problems to complete construction of an automatic tester which would sequentially execute and print results of both room- and low-temperature test activities. Such a unit will be mandatory for efficient test of arrays in pseudo-production efforts.

In the time frame of this program, TIAP arrays were only separately tested through the 3.5°K structural activity. Considerations of invested time and liquid helium consumption for each cool-down cycle make multiple array testing desirable, if practical. A tray of six arrays, interconnected prototypically for operation, could be simultaneously immersed, short-cleared, and tested for fault-tolerant operation. If through-signal paths are rarely open-circuited due to short clearing, this would be acceptable. Otherwise, loss of such a path in one array would prevent complete test of the other arrays. Late program experience, however, tends to minimize that point of concern.

A preferred approach to multiple array test includes specially patterned interconnectors which would permit individual distribution of ERDC and MRDC currents to the separate arrays; all other signal paths would thread through the arrays as usual. In this way, the test operations and results could be restricted to the particular array under test without ambiguity.

Several hundred arrays have been subjected to both room- and low-temperature tests for structural characterization and/or test in the course of the program. Only the TIAP arrays have been tested to assess fault-tolerant operation characteristics and, in particular, only those completed after the major short circuit causes in the fabrication process were removed. The results with respect to short clearing, retention of through-signal path continuity, and adequacy of critical current levels were cited previously.

Six TIAP arrays had unfailed Word Control Circuit (WCC) structure for at least 35 of the potential 40-word array capacity. Bit storage and search capability were not exhaustively tested during the program so that we could examine the structural attributes of as many different arrays produced as possible. However, a partial check of propriety was made for one 6-bit field of array #126, and greater than 35 words were found to be unfailed.

D. Functional Test

The level-logic exercise of an array at liquid helium temperatures is, in a sense, a test of its operating characteristics. However, acceptance is not completely determined until all CAM functions, including Read operations, have been performed under prototype pulsed control and transmission conditions. Thus pulse mode exercise or test is a necessary activity before an array is committed to an operational system such as the projected 5000-word ADP.

An associative memory exerciser, designed and under construction before initiation of this contract, was suitably modified to support initial pulse characterization, exercise, and test requirements for experimental development of the CAM. The exerciser in its present rack-mounted form appears on the left in Figure 32. In the center is a conventional open-cycle dewar system used for all liquid helium test and operation in this program. The 300°K junction box of the data link is shown extending above the dewar. Conventional cabling and connectors form the link between exerciser and 300°K junction box.

The exerciser can repetitively execute an 18-step program based on up to 12 microinstruction statements entered in the plugboard programming matrix. A statement consists of a 12-bit data mask and argument specification in conjunction with a 10-bit microinstruction. Although the exerciser is limited to simultaneous operation of 12-bit data fields, the connectors at the 300°K junction box permit arbitrary assignment of the twelve active bit lines from the exerciser to any two groups of six bit lines of the cryotron array.

The exerciser is capable of automatic operation for clock rates up to 600 kHz, push-button execution by statement, or push-button execution by

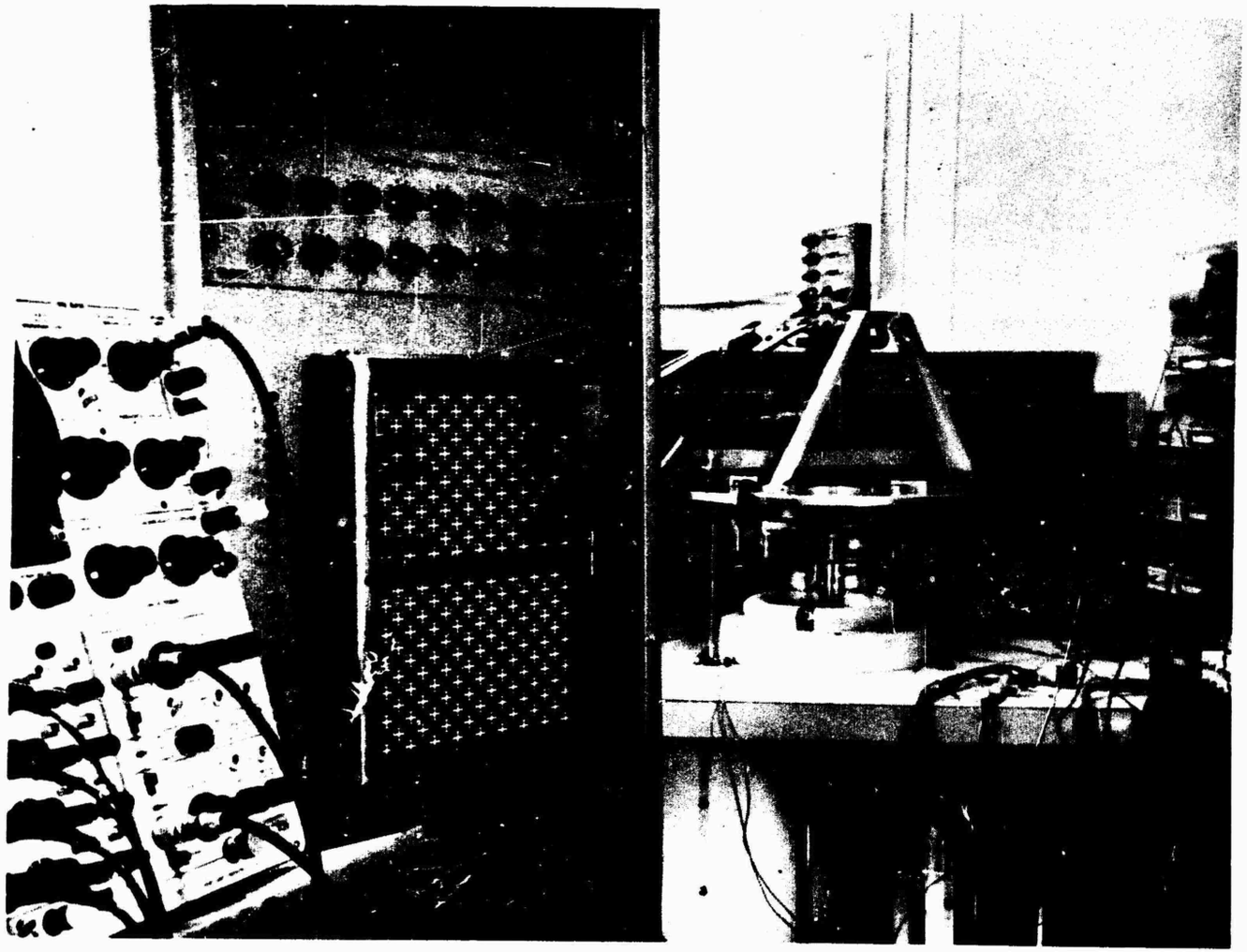

Figure 32 Photograph of test station with exerciser and dewar

microinstruction phase. Up to eight pulse widths and three pulse delay parameters may be independently specified, ranging in time from 1 msec to 1.6 μsec. Individual amplitude controls are provided for all categories of CAM drive pulses. Current driver and sense amplifier boards are compatible in form and merged with standard Digital Equipment Corporation logic modules in panels within the rack.

An indicator register is provided to display the output of the sense amplifiers. Individual adjustments are available to establish the threshold for noise discrimination at the sense amplifier outputs. Input current pulses may be sampled for presentation by a multiple-channel oscilloscope for any pulse input function under selector switch control. Monitoring is accomplished without significant current driver loading.

This unit was used initially to evaluate pulse controlled performance of the CAM circuitry in the 20-word, 500-cell arrays successfully built and operated in mid-program. It has also been used to successfully operate CAM circuitry in the TIAP arrays in the seventeenth program month. The principal interim use of the exerciser has been to experimentally evaluate alternative read-out methods, early forms of which reflected intolerable noise susceptibility as a result of driver-to-sense amplifier coupling.

Except for CAM Read operations, no significant difference was detected between the performance of CAM operations under level logic (multisecond width) or pulsed logic (2 μsec width) control. Nor was any significant difference detected as a function of clock rate in the range from essentially zero to 200 kHz. Experimentally determined amplitudes for the several classes of input current function varied for the 7-layer structure of the 20-word, 500-cell arrays and the 6-layer structure of the 40-word, 2000-cell arrays, but this variation was expected because of changes in thin film segment disposition relative to the shield plane.

No interference effects have been observed up to 200 kHz between the parallel input current pulse lines or their associated cryotron circuitry.

The Match Register (MR) and Enable Register (ER) flip-flops have the largest time constants and therefore will determine cycle time limitations of the design. Pulse measurements of the current diversion time of these flip-flops could not be detected at the 1.6 μsec minimum width ability of the exerciser for the 20-word, 500-cell arrays. Similar measurements for the flip-flops of the 40-word, 2000-cell TIAP array indicated a current diversion time limitation of less than 2.5 μsec. Since the TIAP flip-flops have double the inductance of the smaller arrays, this result is not surprising.

E. ADP Operation under Computer Control

An operational system which would place the cryogenic associative memory (CAM) under program control by a Univac 1218-M has been identified through the design concept phase. Final design and construction of the required interface equipment for this purpose has been deferred, however, pending a decision to proceed toward the 5000-word ADP objective. A description of the design concept and representative 1218-M programming for an address load routine follow.

1. ADP Organization

The ADP will operate through the 1218-M search memory adapter via the Goodyear switching unit (SUN), as shown in Figure 33. The ADP consists of three major sections: (1) a room-temperature interface (IF) with register storage and control capabilities; (2) a cryoelectronic associative memory (CAM) consisting of 126 TIAP arrays; and (3) a control and display (C&D) unit with off-line program control capability.

The interface receives and interprets data and instructions from the 1218-M, generates the control signals necessary to operate the CAM, and buffers read-out data from the CAM to the 1218-M.

In normal operation the ADP is under 1218-M control. The two IF sections involved in this type of operation (Figure 34) are the IF register unit and the TIAP controller unit. The interface has five registers. The three 36-bit registers are: (1) the "comparand data" (CD) register which holds the argument for a data search operation; (2) the "mask data" (MD) register which holds

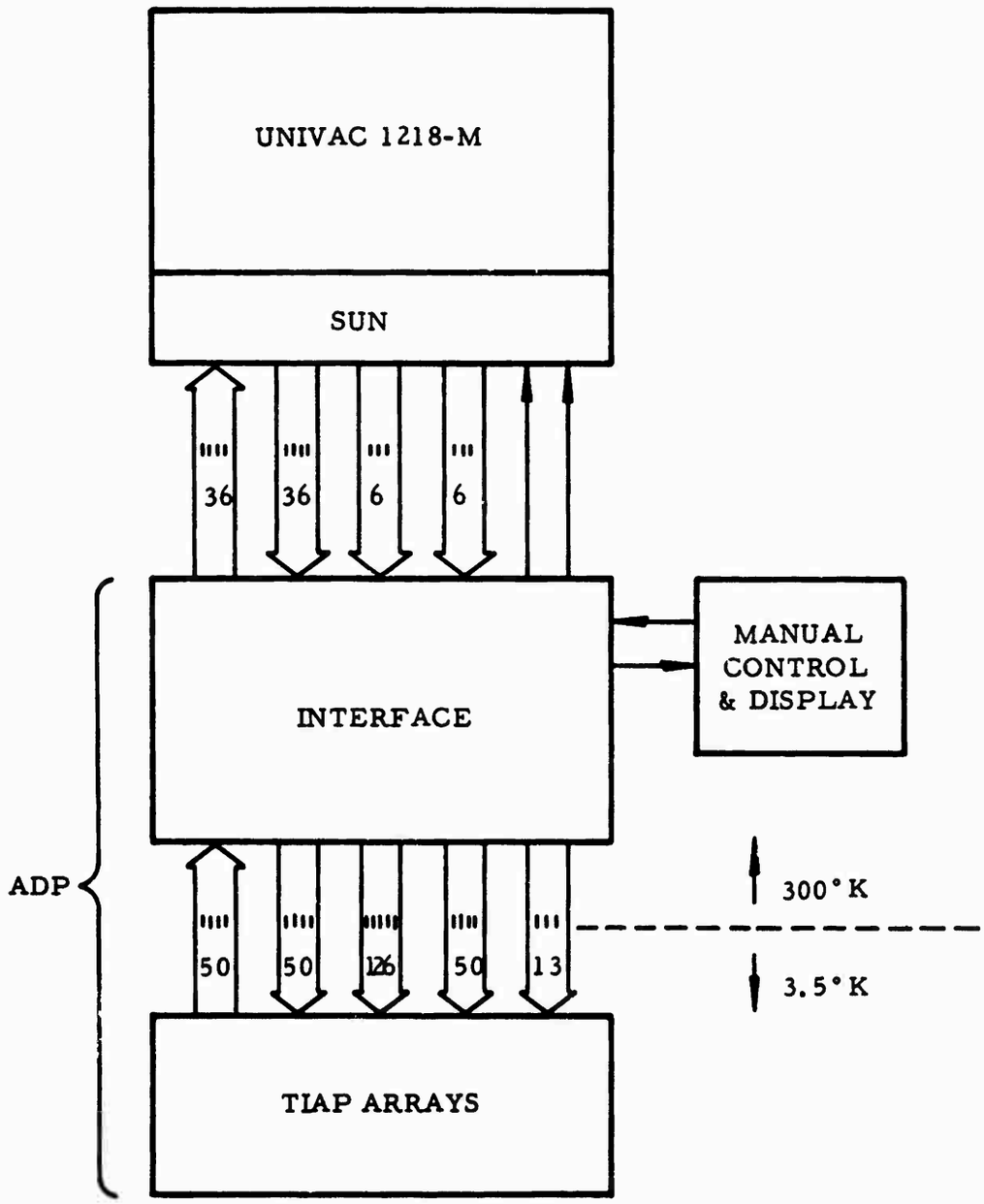

Figure 33 ADP organization

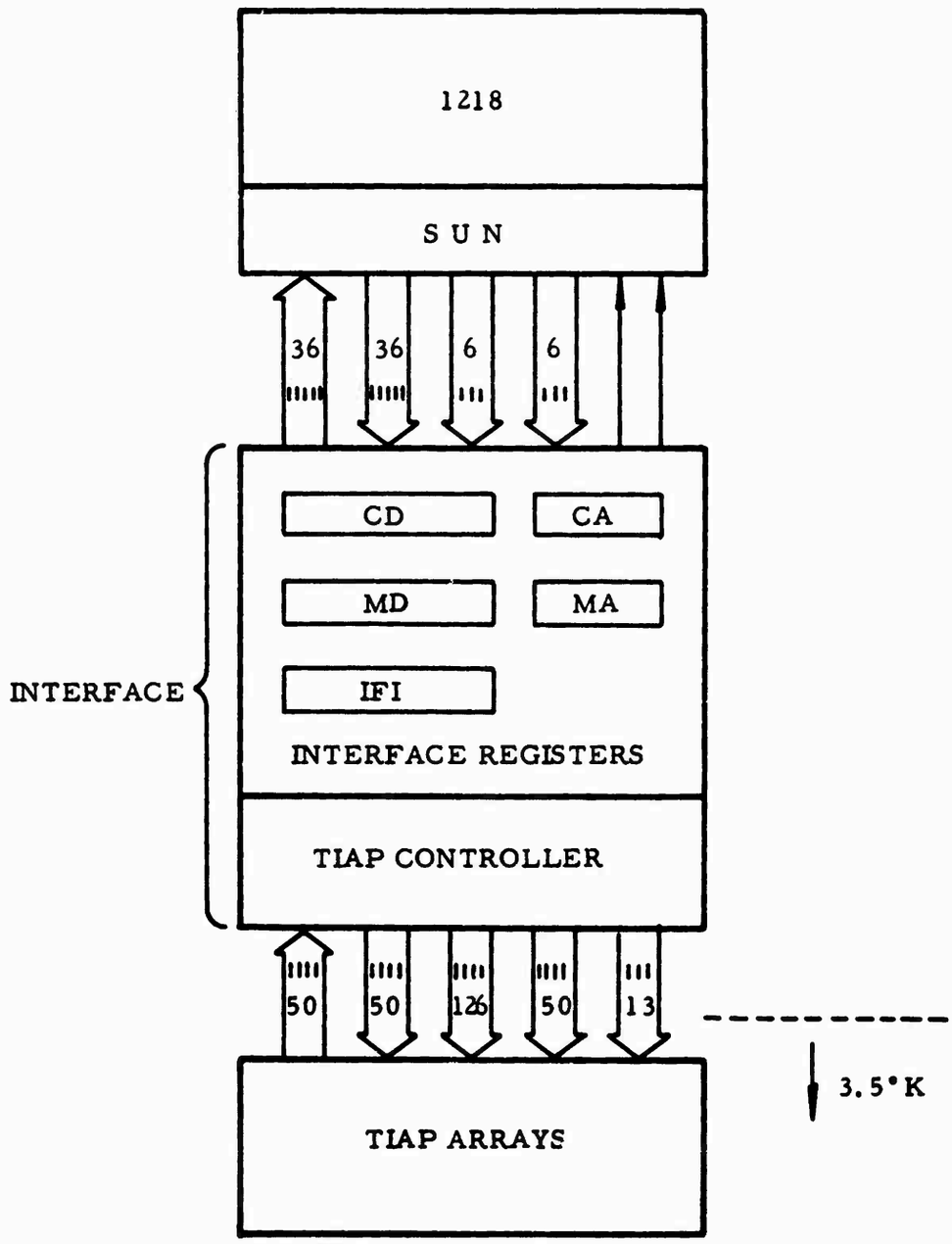

Figure 34 Interface organization

the data search mask; (3) the "interface instruction" (IFI) register which holds the current 12-bit CAM microinstruction and several variables which relate to the internal operation of the interface. The "comparand address" (CA) and "mask address" (MA) registers are each 14 bits long. The CAM word length is 50 bits, with the right-hand 14 available for storing a unique address in each of the 5000 CAM words. In the CAM, the MD and MA and the CD and CA registers combine to form two 50-bit registers, one for mask and one for argument.

When a 1218-M instruction requiring CAM operation is executed, the TIAP controller section decodes the IFI register microinstruction and generates the drive pulses necessary for its execution. If the microinstruction requires CAM read-out, the output word is stored in the interface C register.

The microinstructions, as well as the mask and argument data, are transmitted from the 1218-M to the interface as they are needed in program execution. They are treated as program constants in the 1218-M programming.

2. <u>1218-M - ADP Instructions</u>

The three 1218-M instructions which affect the ADP are $(5000)_8$, $(5003)_8$, and $(5004)_8$. Only 5003 causes actual operation of the CAM; 5000 and 5004 are concerned with data transfer between the 1218-M and the IF registers. As these are Format 2 instructions, each has a 6-bit subfunction specification. The instructions are discussed below.

a. Load Interface (LIF) - 5000

This instruction accomplishes (a) loading the ADP registers from the 1218-M accumulator, or (b) interregister transfer, depending on the subfunction specification. The IF register to be loaded or read into the CD register is also specified in the subfunction code. This is shown in Table V. The 1218-M does not recognize the "BUSY" or "SKIP" status for a 5000 instruction. Thus, the ADP does not tie up the 1218-M or cause a program skip on the LIF instruction.

TABLE V

1218-M - ADP INSTRUCTIONS

Function	Subfunction Binary $y_1y_2y_3z_1z_2z_3$	Data Transfer	Description
5000_8 (LIF)	- - 0 0 0 1	[A] → [CD]	Load CD
LOAD INTERFACE	- - 0 0 1 0	[A] → [MD]	Load MD
	- - 0 0 1 1	[AL, 13-0] → [CA]	Load CA
	- - 0 1 0 0	[AL, 13-0] → [MA]	Load MA
	- - 0 1 0 1	[AL] → [IFI, 1-18]	Load IFI
	- - 1 0 1 0	[MD] → [CD]	Transfer MD
	- - 1 0 1 1	[CA] → [CD, 5-18]	Transfer CA
	- - 1 1 0 0	[MA] → [CD, 5-18]	Transfer MA
	- - 1 1 0 1	[IFI] → [CD]	Transfer IFI
	"BUSY" and "SKIP" ignored by 1218		
5004_8 (RIF)	- - - - - -	[CD] → [A]	Read CD
READ INTERFACE	"BUSY" and "SKIP" not activated		
5003_8 (EAP)	- - - 0 0 0	No Load	No Load from A
EXECUTE ASSOCIATIVE PROCESSOR	- - - 0 0 1	[A] → [CD]	Load CD
	- - - 0 1 0	[A] → [MD]	Load MD
	- - - 0 1 1	[AL, 13-0] → [CA]	Load CA
	- - - 1 0 0	[AL, 13-0] → [MA]	Load MA
	- - - 1 0 1	[AL] → [IFI, 1-18]	Load IFI
	- - 0 - - -		Full Word (50-bit) Operation
	- - 1 - - -		Address (14-bit) Operation
	- 0 - - - -		ERDC to All Arrays
	- 1 - - - -		ERPA to Array No. [CA, 1-8]
	0 - - - - -		"SKIP" Not Allowed
	1 - - - - -		"SKIP" If There Are Matched Words
	"BUSY" raised throughout execution. "SKIP" raised before "BUSY" lowered if y_1 = 1 and matched words exist.		

b. Read Interface (RIF) - 5004

This instruction causes the CD register in the interface to be read into the 1218-M accumulator. No subfunction code is supplied. The "BUSY" and "SKIP" lines are not raised on a 5004 because it is a simple interface readout.

In both the preceding 1218-M instructions the TIAP controller section of the interface and the CAM remain inactive.

c. Execute Associative Processor (EAP) - 5003

This instruction causes an optional transfer of data from the 1218-M accumulator, followed by execution of the microinstruction in the IFI register. The Z digit of the subfunction code specifies which IF register, if any, will be loaded from the 1218-M. The three bits of the Y subfunction digit offer the programmer three options as to the manner in which the microinstruction is executed. The Y_3 bit specifies whether full word (50-bit) or address-only (14-bit) CAM operation is desired. The Y_2 bit specifies whether all 126 TIAP arrays will be enabled, or just one specified array. These two options are useful when loading unique addresses into each word of cryogenic memory and may afford unexplored potential to the inquisitive programmer. The Y_1 bit specifies whether or not the 1218-M program Skip option is to be exercised if "matched" words are found in CAM.

Since the 5003 instruction requires operation of the CAM, the 1218-M must be stopped by raising the "BUSY" line until the microinstruction has been executed. If the Skip option is allowed and matched words are found, the "SKIP" line is raised before the "BUSY" line is lowered. Then the next 1218-M program instruction in sequence is skipped. Table V summarizes the three instructions. Table VI gives a sample 1218-M - ADP program. Its function is to load unique addresses into the memory words of the ADP upon initial cool-down of the CAM or as an option to "new user" operation.

3. Off-Line ADP Operation

For preliminary test and evaluation it will be desirable to operate the ADP before a 1218-M is available. This can be accomplished by the off-line manual control and display (C&D) unit shown with the ADP in Figure 35.

TABLE VI

ADP ADDRESS LOAD SUBROUTINE

LOC	INSTRUCTION	ACTION	DESCRIPTION
P00	XXXXXX	None	Main Program Return Address
*P01	500400	(CD) → A	Read CD [# Arrays | # Words]
P02	504506	L.S. AU-6	Left Shift AU 6 bits
P03	46 K00	(AU) → K00	Store No. Arrays in K00
P04	717776	(AL) - 1 → AL	Decrement AL
P05	44 K01	(AL) → K01	Store No. Words per Array in K01
P06	703010	$(3010)_8$ → AL	Enter Microinstruction $(3010)_8$
P07	500305	(AL) → IFI	Load IFI, DRO All Words
P10	700000	0 → AL	Clear AL
P11	500004	(AL) → MA	Clear MA
P12	700110	$(0110)_8$ → AL	Enter Microinstruction $(0110)_8$
P13	500355	(AL) → IFI	Adr-only, SKIP OK, Match All Vacant Words
P14	30 K02	Ind.Ret.Jp. to (K02)	Fault Exit
P15	707777	$(7...7)_8$ → AL	Set AL
P16	500004	(AL) → MA	Set MA
P17	705000	$(5000)_8$ → AL	Enter Microinstruction $(5000)_8$
P20	500005	(AL) → IFI	Load IFI
P21	12 K01	(K01) → AL	Load AL with No. Words per Array
P22	500353	(AL) → CA	Adr-only, All Arrays, SKIP OK, Write Address
P23	30 K02	Jump to (K02)	Fault Exit
P24	57 K01	(K01)-1 → K01	SKIP if (K01)=0, Loop Exit
P25	34 P10	Jump to P10	Loop Return
P26	700377	$(0377)_8$ → AL	Enter Array Address Mask
P27	504606	$(037700)_8$ → AL	Left Shift AL 6 bits
P30	500004	(AL) → MA	Load Array Address Mask
P31	701210	$(1210)_8$ → AL	Enter Microinstruction 1210
P32	500005	(AL) → IFI	Load IFI
P33	12 K00	(K00) → AL	Load Shifted Array Number
P34	717773	(AL)-$(100)_8$→AL	Decrement AL by $(100)_8$
P35	67 P40	Jump if (AL)<0	Loop Exit
P36	500373	(AL) → CA	Adr-only, SKIP OK, Sing. Array, Write Array Address
P37	30 K02	Jump to (K02)	Fault Exit
P40	34 P33	Jump to P34	Loop Return
P41	40 K01	0 → K01	Clear K01 (K01 should already be clear)
P42	10 K01	(K01) → AU	Clear AU
P43	12 K01	(K01) → AL	Clear AL
P44	500002	(A) → MD	Clear MD
P45	500004	(AL) → MA	Clear MA
P46	703110	$(3110)_8$ → AL	Enter Microinstruction $(3110)_8$
P47	500315	(AL) → IFI	Adr-only, No SKIP, All Arrays, Adr. Words "Vac."
P50	55 P00	Jump to (P00)	Return to Main Program

TABLE VI
(Continued)

K00	XXXXXX
K01	XXXXXX
K02	Address of Fault Subroutine

* It is assumed that the operator has entered the number of arrays and the number of words per array into the upper and lower halves, respectively, of the CD register via the ADP Control and Display unit.

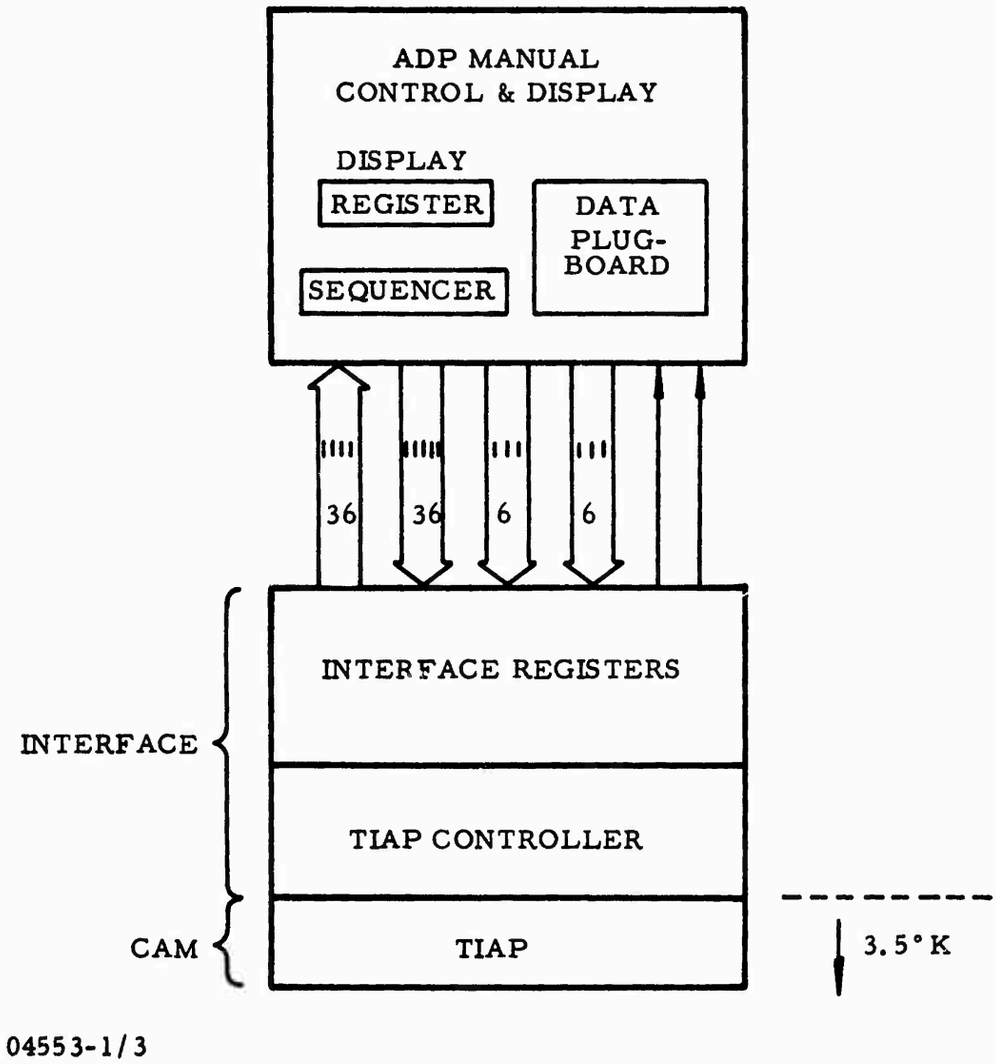

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Figure 35 ADP manual control and display

The entire ADP can be exercised off-line by the ADP C&D unit. Like the TIAP exerciser now in operation, it has a plugboard, a sequencer, and a display register. The plugboard supplies the ADP with the data it would normally receive from the 1218-M accumulator register. The sequencer allows execution of short 1218-M instruction sequences, while the result of each ADP output function is displayed in the C&D register. Thus, ADP operation may be simulated in free-running form, by instruction steps, or by IF clock phase steps when under C&D unit control.

SECTION V
CONCLUSIONS AND RECOMMENDATIONS

Section I of this report cited a progression of four objectives for this engineering research program which, if completely successful, would yield a 5000-word cryogenic ADP. The 5000-word cryogenic ADP was not achieved during the course of the contract; however, its technological feasibility has been established, and technical limitations have been overcome. Associative processor operations have been satisfactorily conducted in large capacity cryotron arrays. Fault-tolerant operation has been demonstrated which permits reliable use of arrays, a vast majority of whose included cryotron circuitry is appropriately operative.

Laboratory-scale array fabrication methods now provide fault-tolerant arrays with approximately 10% of the substrates initiated. More than half the arrays attempted in pseudo-production were lost because the laboratory vacuum systems are not designed for continuous use with minimum maintenance. As a result, residual gas pressures and film thickness reproducibility were not adequately controlled. Poorly adhered and/or overly thick films etch improperly; films that are too thin have inadequate critical current characteristics. Such failures can be detected in-process, and arrays with these failures were immediately aborted.

Short circuit formation posed the most serious problem in large area array fabrication. Since the two basic contributors to interlayer and intralayer shorting have been identified and removed, fewer than 30 shorts are now encountered in completed arrays, i.e., 30 of a possible 10^5 shorting sites. In most arrays these shorts can be nondestructively cleared in 3.5°K test. This residual shorting level is attributed to dust particles which interfere with the conformal application of photoresist. The problem can be largely eliminated by conducting process steps in a laminar flow clean room.

Dynamic fault-tolerant operation of this associatively organized and controlled processor permits maximum utilization of completed arrays.

In summary, a complete and proven technology exists for fabrication of operable cryotron arrays at prototype density and device count for economically favorable applications.

Interconnection solely by means of multiple conductor, superconductive strip transmission line in pressure-actuated contact with thin film array contacts has been used without failure for all low-temperature test activities in this program and in related programs within Texas Instruments. Several design concepts for packaging interconnected arrays have been considered. Engineering development remains to be done but involves only minimum risk effort. The immersed package of 126-144 interconnected arrays for the 5000-word ADP would clear a 10-inch diameter cylinder 15 inches high.

The preferred construction practices for data link provisions, including room- and low-temperature junctions for the multiplicity of parallel signal paths, have been successfully demonstrated in test and operation throughout the program. Interface current drivers and sense amplifiers have similarly been used successfully throughout the program. The circuitry and component specification further reflects substantial cost reduction for these highly replicated functions.

Read-out from the cryotron circuitry posed severe noise susceptibility problems throughout much of the program. A balanced-bridge, split-memory mode was conceived and evaluated in late program months. This mode was operated successfully in an experimental configuration, but there was not time enough to evaluate this configuration for prototype multiple-bit operation before the end of the contract. Further engineering research will be necessary to verify its feasibility.

The basic cryotron circuit design and layout developed in this program provide the desired functions reliably. Certain minor changes have been identified in the course of operation which might improve the operating tolerances of the design.

Although not an explicit task under this program, specific thermal control problems in a practical open-cycle liquid helium cooling system have been

preliminarily reviewed. The principal questions were related to existence and magnitude of thermal gradients in the densely packed bath. Both vertical and radial gradients may exist independent of the thermal load generated internally by cryotron switching and thermal conduction along the data link and supporting structure. It is not certain that these questions have received adequate attention, particularly with regard to remedial actions for design and operation of the cooler. It is not believed, however, that these constitute prohibitive limitations to technology development.

A subsequent engineering program of a developmental rather than a research nature is recommended for construction of a cryogenic ADP of 5000-word capacity. This effort would entail additional research, principally to verify feasibility of the balanced-bridge read scheme or to replace this scheme. Engineering development of test equipment, fixtures, and structural members for packaging in the pseudo-production situation of making, testing, and operating 126 to 144 arrays would represent a major portion of program effort. This number of arrays would be most reliably and efficiently fabricated following detailed study and implementation of process control methods. A significant portion of program effort would concern constructing an operational interface unit for a computer-controlled installation. As previously noted, a corollary study to quantitatively identify and compensate thermal gradients within the open-cycle cooler is recommended.

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This engineering research program, undertaken to construct a 5000 word cryogenic associative data processor, achieved its intermediate objectives concerning identification and solution of technical limitations for large capacity array fabrication, interconnection, data linkage, and packaging. Successful methods for fabricating 2.0 inch x 2.25 inch arrays having 40-word, 2000-cell (11,000 cryotrons) capacities resulted in seven operable arrays by the end of the program. Between 126 and 144 such arrays would provide the 5000 word objective. Fault-tolerant system operation permits use of arrays containing failed word(s). Array interconnection via superconducting, flexible, strip transmission line in pressure-actuated contact with thin film array contacts was successfully used throughout the contract, as were preferred data linkage means. Design concepts for packaging the multiple-array system were accomplished, and the interface electronic functions to permit on-line operation with a Univac 1218(M) computer were specified. Because solution of array fabrication problems consumed most of the contract period, fabrication of the full complement of arrays was not possible. An engineering development program is recommended for construction of the 5000 word cryogenic associative processor.

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