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RESIDUAL SAW DAMAGE IN SILICON WAFERS AND ITS INFLUENCE ON MOS CAPACITANCE RELAXATION

INTERNATIONAL BUSINESS MACHINES CORP.

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DAMAGE PROFILES IN SILICON AND THEIR IMPACT ON DEVICE RELIABILITY

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LIST OF INVESTIGATORS

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RESIDUAL SAW DAMAGE IN SILICON WAFERS AND ITS INFLUENCE ON MOS CAPACITANCE RELAXATION

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SUMMARY

Residual saw damage in silicon surfaces and its influence on MOS capacitance relaxation is discussed. Experiments are conducted to gain information on the influence of silicon process parameters on MOS capacitance relaxation. Process parameters investigated include: crystal slicing, wafer cleaning and wafer polishing. The main results of this investigation include evidence about saw damage in the silicon surface and its variation with different slicing and polishing procedures. It is also found that the amount of saw damage is larger in wafers cut from the tail-end relative to wafers cut from the seed-part of the crystal. Based on the results obtained, recommendations are made about future activities of the contract work.

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RESIDUAL SAW DAMAGE IN SILICON WAFERS AND ITS INFLUENCE ON MOS CAPACITANCE RELAXATION

1. Introduction

It is the purpose of this contract work to examine the behavior of crystal defects in silicon and their impact on semiconductor device reliability. In Technical Report No. 1 we have shown that crystal defects in the surface of MOS capacitors influence MOS capacitance relaxation.[1] It was shown that the time behavior of the deep depletion capacitance relaxation is strongly influenced by residual mechanical saw damage which is sometimes present in standard silicon slices. Using transmission electron microscopy the residual saw damage was identified as microsplits of the silicon lattice. Microsplits were shown to vary considerably in density and size across a wafer surface and large differences in microsplit density were found for different wafers.

The measurements reported here concentrate on saw damage in silicon surfaces and its influence on MOS storage time. Standard 2 1/4 inch silicon wafers were obtained from different sources. Consequently, control of wafer production could not be exerted. All silicon wafers as-received were quality inspected before processing and appeared flawless to the naked eye or under optical microscopic inspection. A wide variation in silicon surface quality was

observed. Wafers showing scratches or any other surface degradation as revealed by standard quality inspection were not used for the experiments reported here.

The evaluation of silicon wafers in terms of microsplits is difficult and time consuming. It requires the classification of silicon into "good" or "bad" through electrical measurements followed by transmission electron microscopy work. The silicon classification is achieved through MOS processing of the silicon and subsequent measurement of storage time of every capacitor on the wafer for every wafer processed. This approach relies on a continuous electron microscopy evaluation of good and bad devices and recognition of pathological features in the silicon typical for bad devices only. To recognize such features in the transmission microscope the procedure is as follows. First, the bad silicon area is localized on the silicon surface through a storage time measurement of the MOS capacitor. After the measurement the MOS capacitor is separated from the rest of the wafer. For the electron microscopy work the metal as well as the oxide are stripped off the device and subsequently the device chip is chemically thinned by a jet-etching technique until an area is obtained thin enough to transmit the 200KeV electrons. This area is normally the thin area around a small hole. The jet etching is fairly well controlled and

the thin area is normally obtained more or less in the middle of the chip. However, the useful area for transmission electron microscopy is approximately only 1% of the total 60 mil diameter device area. Accordingly, one needs a fairly high defect number per cm^2 ($\sim 10^6$) to see one defect in the useful area at a magnification of 10,000 to 20,000 times. This condition is fortunately fulfilled. After investigating 200 bad devices and 60 good devices it can be stated that we never had a bad device free of microsplits and that we never saw a single microsplit in a good device. This does not mean that a good device is completely free of defects but it is obviously safe to claim that the number of defects (if any) in a good device must be considerably lower than $10^6/cm^2$. The number of defects in a bad device is at least $10^6/cm^2$.

Another problem to consider is the problem of contamination of the bulk silicon during device processing. Contamination can easily be picked up during wafer polishing, wafer cleaning or during oxidation. But here we are confident that electron microscopy can reveal silicon bulk contamination which normally leads to precipitation effects in the silicon. Contamination can also have a strong influence on MOS storage time.

The results presented in this report are a continuation of the work reported in Technical Report No. 1 and first summarize our electrical measurement technique and then discuss the influence of silicon process parameters on MOS storage time.

2. Experimental

The time behavior of the deep depletion capacitance relaxation is readily measured[2,3] when an MOS capacitor is pulsed from accumulation into deep depletion by applying a voltage step of correct polarity to its gate to deplete majority carriers from the semiconductor surface. Thus a negative step is applied for n-type material and a positive step is applied for p-type material. Initially, a large depletion region forms in the silicon. As minority carriers are generated in the depletion region they are swept to the silicon-silicon dioxide interface where they accumulate in an inversion layer. The majority carriers generated flow to the edge of the depletion region where some of them neutralize the ionized impurity sites and thus reduce the width of the depletion region. Consequently, the width of the depletion region relaxes as the inversion layer forms until equilibrium is reached. The relaxation time is typically 5-8 orders of magnitude greater than the minority carrier generation-lifetime and is conveniently and accurately measured. This can be achieved by measuring either the MOS capacitance as a function of time or the external current as a function of time. Both effects are a consequence of the change in the depletion width region. Our work is based on measurements of the MOS capacitance as a function of time and with the help of such measurements MOS

devices are classified as "good" or "bad". Subsequently good and bad devices are examined and analysed for structural differences in the silicon lattice.

2.1 Fabrication of MOS Capacitors

The 2 1/4 inch diameter silicon wafers used in the preparation of MOS capacitors were normally sliced from Czochralski grown, p-type crystals of <100> orientation boron doped to a resistivity of 2 ohm-cm. The wafers used for device fabrication have a mechanically-chemically polished surface. The silicon slices are processed to contain 36 circular MOS devices. Each device is 60 mils in diameter. Before oxidation the wafers are carefully cleaned using NH_4 - H_2O_2, HCl - H_2O_2 and HF solutions. A 5000 Ångstrom thick oxide is grown at 1000°C using a dry-wet-dry oxidation cycle. Aluminum metallurgy is used. After metalization the wafers are annealed. A photograph of a finished wafer is shown in Fig. 1 and a schematic cross-sectional view of a single finished device is given in Fig. 2.

2.2 Electrical Apparatus

A schematic diagram of the electrical setup used to measure capacitance vs. voltage curves as well as MOS storage time curve is shown in Fig. 3. Accordingly, the MOS capacitor is connected to a Boonton capacitance meter. The capacitance output is amplified

by a variable gain amplifier and fed into the y-axis of an x-y recorder. The x-axis of the recorder is connected to a bias supply.

C-V curve plotting is done at a frequency of 1MHz and at a scanning rate less than 0.1 volt/second. For the measurement a voltage ramp is applied to the sample and to the x-axis of the recorder. The output of the Boonton capacitance meter is fed to the y-axis of the x-y recorder. The bridge sensitivity is better than 1% and its transient time is 40μsec.

For the storage time measurement the x-axis of the recorder is set to a function time of 5 sec/inch. The output of the capacitance meter is again fed to the x-y recorder. At the start of the measurement the MOS capacitor is switched into its accumulation regime. Then the recorder is started and the MOS capacitor is switched into deep depletion. The x-y recorder plots the relaxation of the MOS capacitor from deep depletion vs. the function time.

The information obtained from this measurement is the high frequency capacitance versus the time it takes to read a predetermined capacitance change after the device is pulsed into deep depletion such that the interface potential equals 10 volts. This time can also be printed out or entered via a special interface unit into an IBM Magnetic Card Selectric Typewriter.

For the actual measurements the devices are contacted by a K & S stepping probe with a platinum probe point in a dark box. C-t traces are made of all devices on a wafer. A device is classified as good for leakage currents less than 0.02 pA/mil^2 area.

2.3 Data Collection for MOS Storage Time Measurements

A study of the influence of process parameters on MOS storage time calls for a large number of measurements. A single wafer contains 36 MOS devices and the storage time is measured for every device on the wafer as described in section 2.2. For the purpose of statistical evaluations the mean yield of good devices/wafer for many wafers processed under different conditions must be available. Therefore, a computer program was introduced for data handling. The program (APL) stores the data of each wafer and prints out the results either of one wafer or of one wafer lot based on statistical calculations. The MOS storage time can be entered into the APL program in the following ways:

- Manual with the typewriter.
- Manual on magnetic card and from there into the program.
- Automatic via the interface unit into the MCST. From there on a routine basis into the program.

The number of devices can vary for every wafer.

The program calculates from this data:

- Consecutive wafer numbers.
- Mean yield.
- Mean current.
- Standard deviation of current.

All this data is stored as on-line within a matrix. If desired the list of all wafers or only part of it can be printed out. Together with this data the storage times of all devices are stored in the program.

There are two forms of output available. The first one is a list or partial list of all wafers measured until now. The second one prints out all data for one or more wafers or for a specific lot number. The program searches for the entered wafer or lot number and prints a list. Together with the list a histogram is plotted where the y-axis is the number of capacitors and the logarithmic x-axis the current. The output is usable for direct reproduction on foils, slides, etc. as needed for presentations. Examples are shown in Figs. 4 and 5.

2.4 Measurements

Preliminary experiments consisted in processing silicon wafers as-received from different sources. All wafers were processed under identical conditions and large variations (0% to 100%) in good capacitors/wafer were noted. Transmission electron microscopy

studies were made on numerous good and bad devices. Microsplits were found in bad devices only. Considerable differences in microsplit size for different wafers were also noted. Examples are shown in Figs. 6. After processing and testing of approximately 300 different silicon wafers several general observations were made which can be summarized as follows:

A. The number of good capacitors/wafer seems to depend on the saw damage introduced by the crystal slicing technique. Crystals that are mounted in the horizontal position and thus are cut by a blade in the vertical position seem to give many more good devices per wafer than crystals mounted in a vertical position and thus are cut by a horizontally mounted blade. Crystal slices are therefore classified as H wafers when obtained from crystals mounted horizontally for slicing and correspondingly are named V-wafers when obtained from crystals mounted vertically for slicing.

B. A reasonable number of good capacitors/wafer is obtained for V-crystals if they are treated before oxidation for approximately 7.5 minutes with HF. If the HF treatment is eliminated V-crystals give a very low number of good capacitors/wafer (0% - 10%).

C. The stock removal rate of the copper polishing process has a large influence on the number of good capacitors/wafer of V-crystals. The slower polishing rates give more good capacitors/wafer.

D. The wafer position in the crystal also seems influential on the number of good capacitors/wafer. Wafers cut from the seed-end give consistently better results than wafers cut from the tail-end. This is found true for H- and V-crystals.

E. Wafers cut from Czochralski crystals give better results than wafers cut from float zone crystals.

Based on such general observations more detailed experiments were performed. Each conclusion was tested separately and the results are reported in the following.

2.4.1 H-wafers versus V-wafers

The two different modes of silicon crystal slicing as practiced in industry are shown schematically in Figs. 7 a,b. Two different Czochralski crystals were obtained and sliced by two different vendors as pictured in Figs. 7a and 7b. Care was taken to maintain knowledge of the position of each slice in the crystal after slicing. The silicon wafers were received as-sliced and copper polished by us. After polishing, the crystals were processed as described in section 2.1. The results are summarized in Tables I and II.

Table I

H-wafers, slices copper polished	
Crystal Part	Average of Good Capacitors/Wafer (%)
Seed (A)	92.5
Middle (B)	86.3
Tail (C)	37.8
A,B,C Average:	72.2%

Table II

V-wafers, slices copper polished	
Crystal Part	Average of Good Capacitors/wafer (%)
Seed (A)	76.6
Middle (B)	39.6
Tail (C)	25.7
A,B,C Average:	47.3

Accordingly, we find a substantially higher average of good devices/wafer for H-wafers (72.2%) as compared to V-crystals (47.3%). This difference is even more apparent when the wafer position in

the crystal is taken into account. H-wafers show consistently large numbers of good capacitors/wafer approaching 100% for seed and middle part contrary to V-wafers where the number of good capacitors drops below 50% for cuts starting at the middle section of the crystal.

2.4.2 Prolonged HF Treatment

Another interesting difference between H- and V-wafers relates to the 7.5 minute HF treatment introduced as a cleaning step before processing. If this time is reduced to 10 seconds V-wafers have practically no good capacitors/wafer, contrary to H-wafers which maintain good yield independent of the HF cleaning step.

Yield results comparing the 10 second and the 7.5 minute HF cleaning for V-wafers are summarized in Table III.

Table III

V-wafer	
Average of Good Capacitors/Wafer (%) (10 Sec.)	Average of Good Capacitors/Wafer (%) (7.5 Min.)
0.82	31.4

Based on 75 processed wafers which consistently showed good yield after 7.5 minutes HF cleaning the prolonged HF treatment

was introduced as the standard cleaning procedure for all our experiments in this investigation.

2.4.3 Different Polishing Parameters

Experiments were conducted to assess the influence, if any, of the chemically-mechanically polishing process on the capacitance relaxation time. The two polishing techniques investigated are the Syton and the copper polishing methods.[4,5] The Syton process uses a solution of Syton HT to 1 part of D.I. water. The pH value of the polishing solution is approximately 11 to 12 and is adjusted through diluted NaOH. The polishing rate is constant and slow (approximately 0.7 to 0.8 mil/hour).

The copper polishing rate is greatly affected by wheel temperature and acidity of the polishing solution and can be set slow (1-2 mil/hour) or fast (12 mil/hour). The copper polishing solution consists of 120gm $Cu(NO_3)_2 \cdot 3H_2O$; 1140cc D.I. water; 12cc conc. HNO_3; and 300cc NH_4F (40%). Details on both polishing techniques are found in refs. 4 and 5. Horizontally sliced wafers were used for this experiment. No significant difference was found between the two polishing techniques. The data are presented in Tables IV and V.

Table IV

Crystal	Process	Average of Good Capacitors/Wafer (%)
No control of wafer position	SiO_2 (Syton)	72.1

Table V

Crystal	Process	Average of Good Capacitors/Wafer (%)
Seed (A)	Copper (slow)	92.5
Middle (B)	Copper (slow)	86.3
Tail (C)	Copper (slow)	54.5
Average:	77.8%	

Another experiment compared the influence of fast and slow copper polishing on storage time yield of MOS capacitors. Vertical sliced wafers were processed for this experiment. The fast polishing process was adjusted to remove 12 mil/hour and the slow process removed 1 mil/hour. The results are compiled in Table VI.

Table VI

Copper Polish Removal Rate	Average of Good Capacitors/Wafer (%)
12 mil/hour	15.3
1 mil/hour	37.5

Transmission electron microscopy of bad devices after fast and slow copper polishing reveals interesting differences in the defect size. Representative examples are shown in Figs. 10 a,b. The microsplits are considerably larger in the fast polished wafer. This indicates clearly that the slow polish is much more effective in damage removal than a fast polishing action. This is also confirmed through the good agreement of Syton and copper (slow) polishing results. If both techniques have approximately the same stock removal rate of 1 mil/hour they seem to give identical results.

2.4.4 Wafer Position Dependency

It is well known that crystal properties of wafers cut from Czochralski grown crystals can vary relative to the position of the wafer in the bulk crystal. Such variations are caused through a non-uniform impurity distribution in the crystal, which in turn results from the asymmetry of the furnace heat output present in all crystal growth systems. It is the result of such an asymmetry that thermal and rotational axes in the furnace do not coincide. Under such conditions the instantaneous microscopic growth rate of the crystal at any point at the crystal/melt interface undergoes sinusoidal fluctuations with time. Such fluctuations lead to similar changes in the impurity and/or point defect state of the crystal. Well known examples of such variations are the seed to tail dependency of resistivity, the seed to tail dependency of the oxygen content, the carbon content, and the content of other impurities in Czochralski silicon crystal. Since the fracture strength of single crystal silicon depends critically on its perfection (impurity clusters, point defect clusters, etc.) it is not surprising to find differences in residual saw damage in wafers cut from different locations down the growth axis. Likewise it must be anticipated that the amount of saw damage relates also to the slicing technique.

We have found that such differences are particularly pronounced in V-wafers but are also present in H-wafers. The results are summarized in Tables I and II and were confirmed by a separate experiment. In this experiment an additional crystal was first pulled by the Czochralski technique, sliced in the V-position and finally copper polished. The position identity was registered for every single wafer in the crystal. Subsequently, slices representative of seed, middle and tail section were MOS processed and finally the yield of good devices was measured for every wafer processed. A steady decrease in yield from seed to tail was apparent. To confirm these results another crystal was mounted in the reversed position with the tail-end in the front and the seed-end in the back to insure that the position dependency is a crystal property and not a result of crystal mounting and slicing. Similar results for the standard mounted crystal were obtained for the reversed mounted crystal.

Oxygen measurements were performed on crystal slices located adjacent to the MOS processed slices.

The oxygen measurements showed also a decrease of the oxygen concentration from seed to tail. Such measurements are summarized in Table VII. The seed to tail oxygen decrease in large diameter Czochralski crystals, as shown in Table VII, was confirmed for different crystals.

Table VII

Wafer Position Dependency for <100>			
No.	O_2 (ppm)	Resistivity ohm-cm	Average of Good Capacitors/Wafer (%)
12	24.5	2.21	70
72	27.6	2.15	
120	26.6	2.11	50
179	21.5	2.06	
208	20.9	2.02	
271	17.1	1.93	10

2.4.5 Czochralski Versus Float Zone Crystal

One of the major differences between Czochralski silicon and float zone silicon is the higher oxygen content in the Czochralski silicon crystals. The oxygen content in Czochralski crystal is generally between 10^{17} to 10^{18} oxygen atoms/cm^3. In float zone silicon the oxygen content is below 10^{16} oxygen atoms/cm^3. Up to date only a limited number of float zone crystals were MOS processed. The float zone wafers were obtained from different sources. The yield obtained from float zone wafers is relatively low. Float zone measurements for 10 different crystal slices obtained from the different crystals averaged approximately 5%.

3. Discussion and Recommendations

One of the main results of this investigation indicates that residual saw damage related to different equipment and slicing conditions as encountered in the semiconductor industry can have a strong influence on silicon surface perfection. Our results are typical for crystals obtained from two different vendors, which happen to use different techniques, and obviously cannot be generalized. However, it is well known that ID diamond cutting of silicon can lead to large variations in saw damage, depending on the quality of the saw as a vibration sink.* Horizontal saws

* A major damage mechanism during ID slicing of silicon wafers was previously shown to be related to out-of-plane flexural vibrations of the membranelike ID-blade which produce, in turn, oscillating stresses in the wafer being cut and thus create microcracks in the wafer surface.[6]

seem to be more successful in damping blade variations during cutting and also seem to be better in smoothing out variations in the cutting rate.

At any rate, it seems to be clear that ID diamond slicing of silicon crystals into thin wafers is more complicated than previously thought. Any progress of slicing to larger diameter silicon wafers will be difficult to achieve if minimal surface damage is the requirement. Such difficulties should not be underestimated. They are compounded through large variations in silicon crystal quality. The role of standard silicon contaminants, such as oxygen and carbon, and their influence on the flexure strength of silicon, is not understood. As a matter of fact, this subject has never been investigated and, consequently, data are not available.

The trend of the semiconductor industry to larger and larger diameter crystals is also clear. Detailed investigations reported on ID saw damage in silicon[6] indicate clearly that slicing of 3 or 4 inch Si crystals into thin, perfect wafers could be very difficult or even impossible to achieve without new ideas and concepts, resulting in the conception of new devices that can minimize saw blade vibrations during slicing, and are also able to smooth out variations in the cutting rate.

Another result of this investigation is the wafer position dependency, which indicates that the seed part of a silicon crystal can be less susceptible to saw damage than the tail end. The only difference we find between the seed and the tail end of a Czochralski crystal is the variation in oxygen concentration. Therefore one might speculate that finally oxygen is doing something beneficial to silicon. The influence of oxygen on the mechanical properties of single crystal silicon was reported ten years ago as the upper and lower yield point dependency of silicon on oxygen concentration.[7] That oxygen makes silicon more resistant to crack propagation seems to be tentatively confirmed by the few measurements reported here on float zone crystals. However, we feel more measurements on float zone material are needed to confirm this point. Further research on the influence of crystal growing parameters on the flexure strength of silicon is recommended in this context.

The effect of the HF cleaning step on MOS storage time results observed for V-crystals indicates that "clean splits" can heal during device processing. Obviously, smaller splits will have a better chance for "perfect closing" because their opposing fracture faces are less likely to be completely disengaged. It is also less likely for smaller splits to contain dislodged silicon pieces between their fracture faces. Small splits in silicon crystals and their healing capability have

been actively researched.[8] These investigations seem to indicate that mechanically damaged surfaces (damaged on an atomic level) can be substantially improved by proper chemical treatment. Therefore we recommend that a better understanding of the healing of microsplits should also be an area of future investigations.

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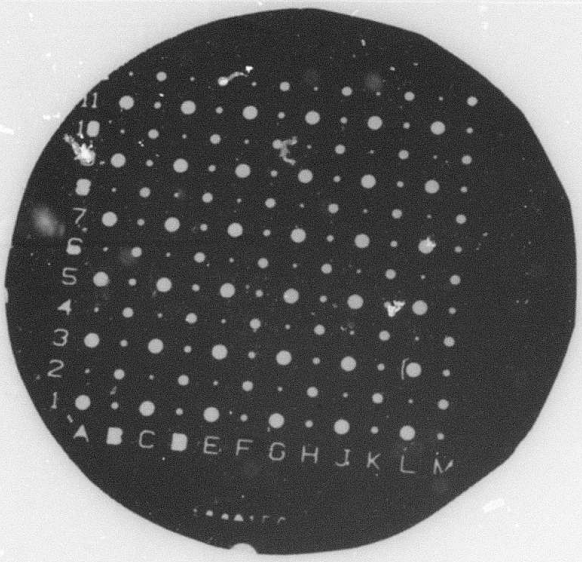


Fig. 1. Photomicrograph of finished wafer.

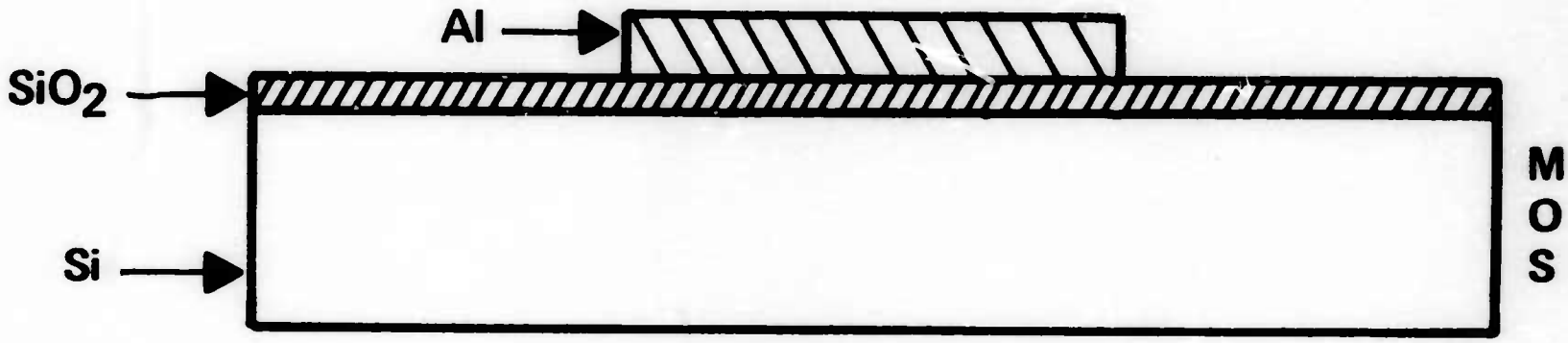


Fig. 2. Cross-sectional view of single finished device.

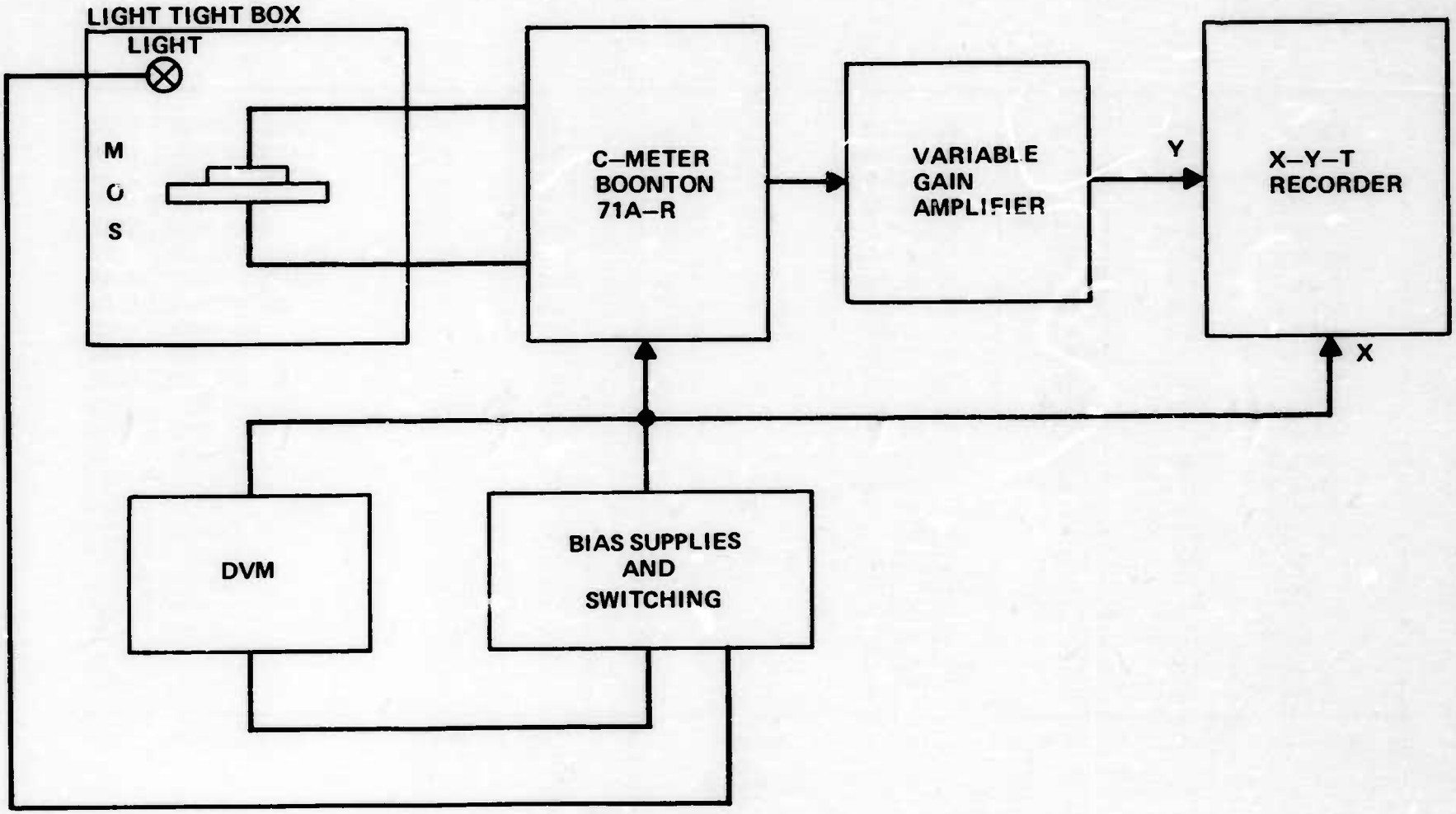


Fig. 3. Schematic diagram of electrical setup.

MOS STORAGE TIME LIST

DEPT. 267
04/30/73

LOT	DESCRIPTION	VEN	RES	COX	ΔAVFB	DATE	NO.	YIELD	CUR NA	STDEV
3072	FZ115 15–16	X	1.1	138		04/25/73	1	2.78	10.8353	4.513
3015	2806 HHH	Y	12.6	134		04/25/73	2	16.67	3.3312	2.251
3016	XXXX2 162	X	2.4	132	3.5	04/25/73	3	43.33	4.0897	4.003
3041	7068 9	X	2.4	140		04/25/73	4	7.41	8.7522	4.012
3016	XXXX2 6	X	2.2	131		04/25/73	5	69.44	1.7997	2.843
3014	7068 241	X	2.2	140	29.8	04/25/73	6	7.69	8.8872	3.770
3016	XXXX2 195	X	1.8	131	1.3	04/25/73	7	30.00	4.9609	4.289
4172	20509 SLOW32	X	2.1	140		04/25/73	8	0.00	11.5970	1.268
4173	20509 FAST13	X	2.4	140		04/25/73	9	3.23	6.9343	3.814
3011	2806 KC	Y	12.6	132		04/25/73	10	100.00	0.1335	0.040
3011	2806 KC	Y	12.6	136		04/25/73	11	58.33	1.7743	2.596
4241	2806 MIX KC	Y	2.3	139		04/25/73	12	25.00	4.6754	3.274
3016	XXXX2 76	X	2.2	128	21.5	04/27/73	13	50.00	4.6431	6.675
3014	7068 31	X	2.2	131		04/27/73	14	43.75	3.6401	4.310
3014	7068 190	X	2.2	140	6.0	04/27/73	15	0.00	7.2604	2.716
3016	XXXX2 147	X	2.3	129	17.2	04/27/73	16	38.24	3.7275	3.786
4172	20509 SLOW20	X	2.3	136		04/27/73	17	0.00	7.5477	3.132
4172	20509 SLOW10	X	2.4	134		04/27/73	18	0.00	6.5295	2.507
3015	2806 HHH	Y	14.6	124		04/27/73	19	75.00	0.9095	1.644
3011	2806 KC XVI	Y	12.6	135		04/27/73	20	50.00	2.0788	2.650
3011	2806 KC XVII	Y	12.6	131		04/27/73	21	50.00	2.3681	2.765
3011	2806 KCXVIII	Y	13.3	128		04/27/73	22	39.39	2.3709	2.339
3011	2806 KC XIX	Y	12.1	129		04/27/73	23	50.00	1.7303	2.245

Fig. 4. Example of computer printout data — storage time list.

MOS STORAGE TIME DATA

DEPT. 267
04/30/73

LOT NUMBER	3011
LOT DESCRIPTION	2806 KC
VENDOR	Y
NUMBER OF DOTS	213
MEAN YIELD	57.955
MEAN CURRENT IN NA	1.7338
STD.DEV.OF CURRENT	2.40395
MAX CURRENT	9.65231
MIN CURRENT	0.120729

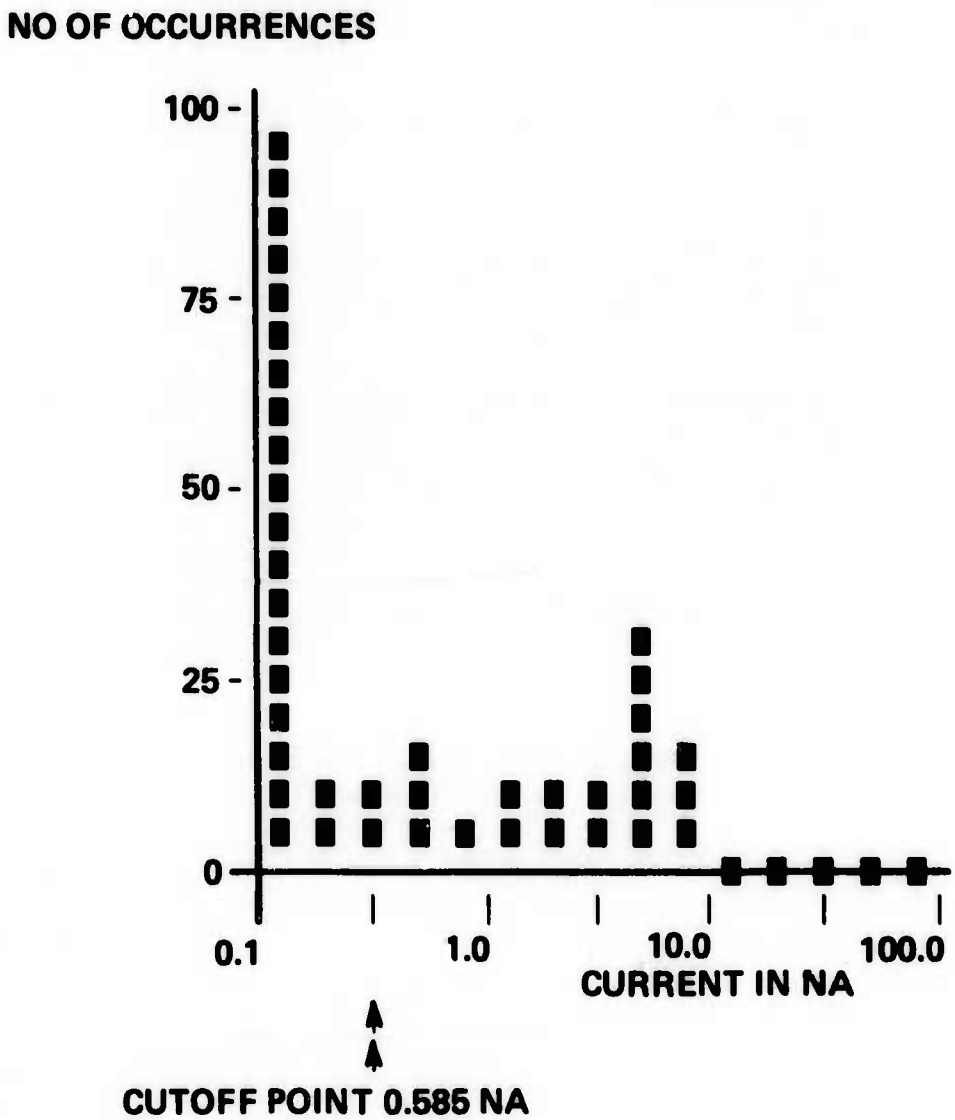


Fig. 5. Example of computer printout — histogram.

Fig. 6a. Example of microsplit configuration as found in "bad" devi ces.

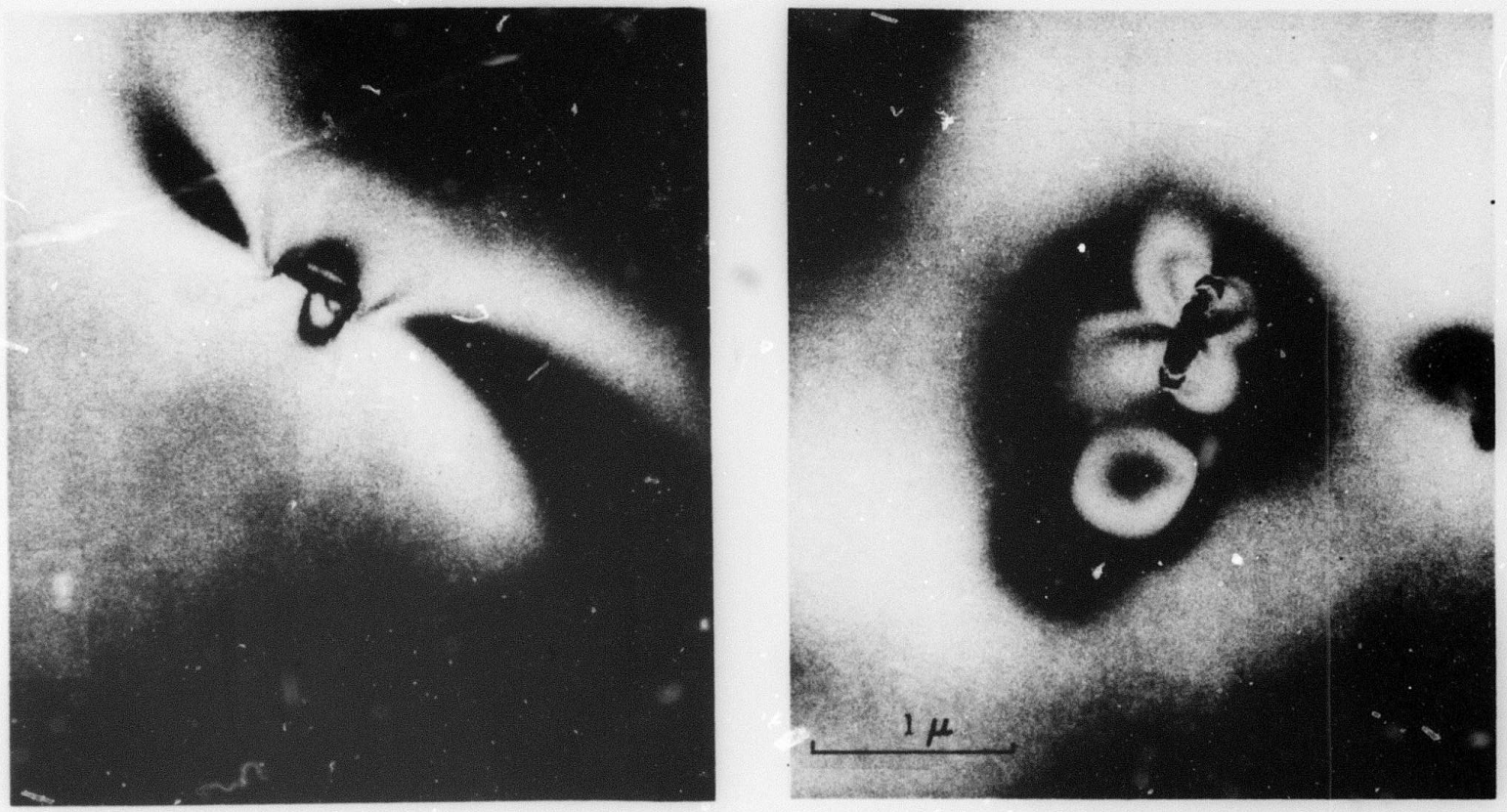


Fig. 6b. Examples of microsplit configurations as found in "bad" devices.

Fig. 6c. Examples of microsplit configurations as found in "bad" devices.

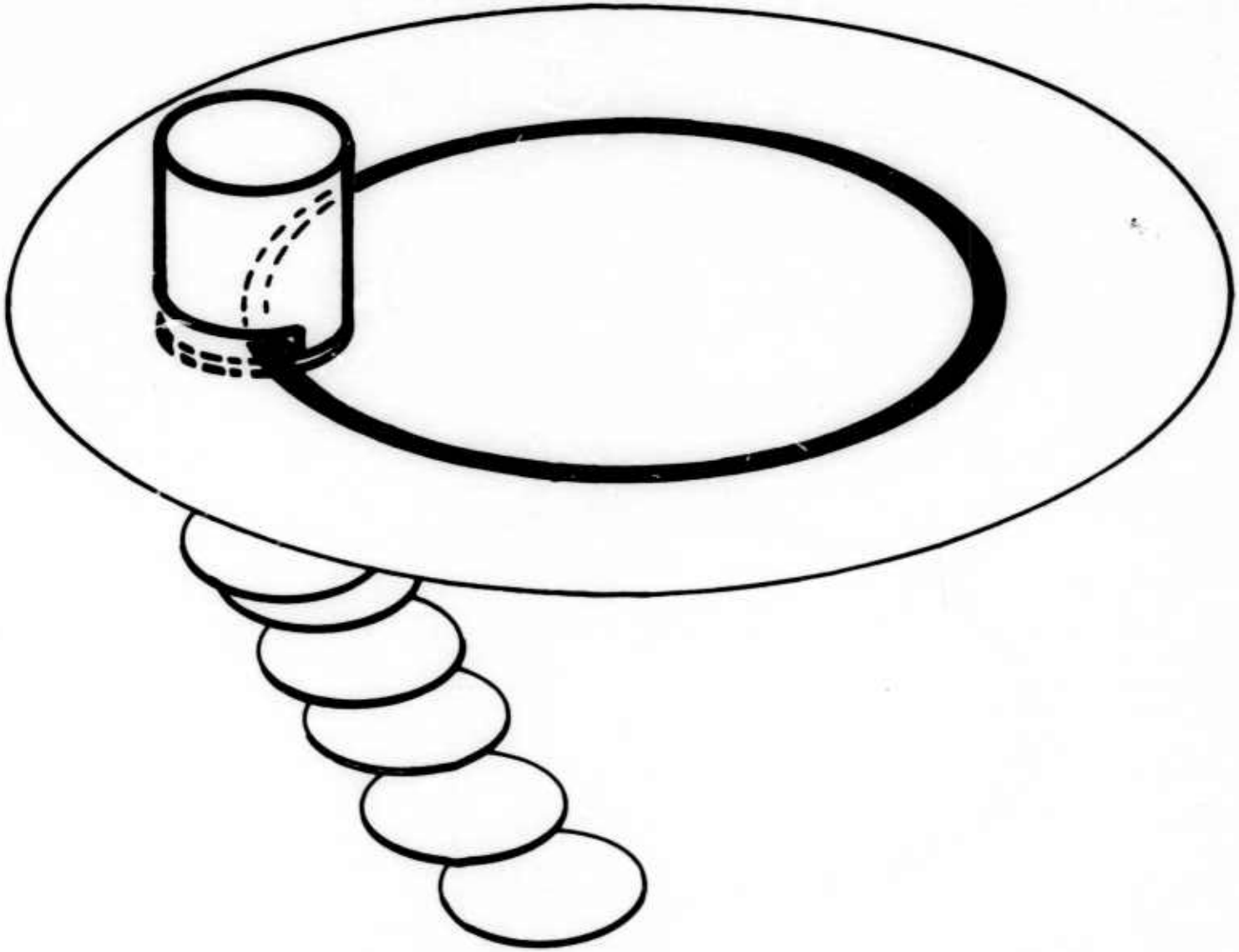


Fig. 7a. Different modes of crystal slicing techniques — horizontal slicing.

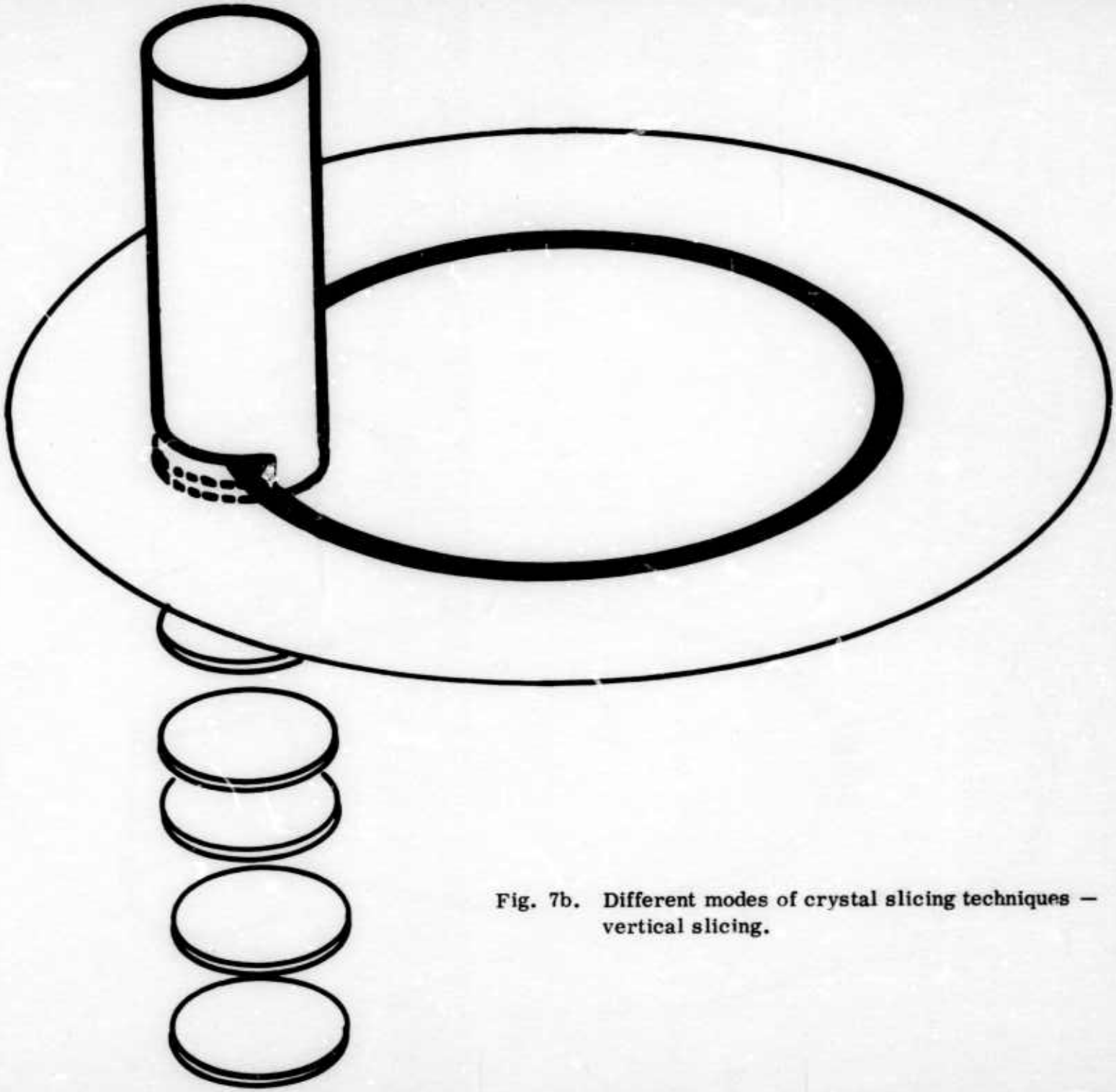
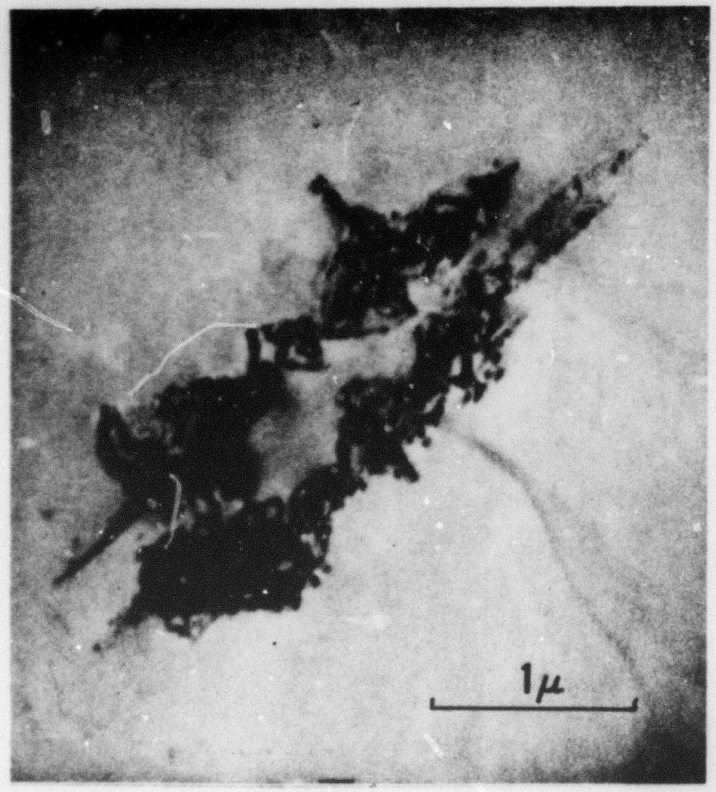


Fig. 7b. Different modes of crystal slicing techniques — vertical slicing.



6865

6946

Fig. 8a. Examples of microsplits as seen in the TEM. Typical for fast polishing.

7838

7752

Fig. 8b. Examples of microsplits as seen in the TEM. Typical for slow polishing.