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An Investigation of Thin Single-Crystal Silicon Films on Insulator/Polycrystalline-Silicon Substrates

Fairchild Camera and Instrument Corp.

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AN INVESTIGATION OF THIN SINGLE-CRYSTAL SILICON FILMS ON INSULATOR/POLYCRYSTALLINE-SILICON SUBSTRATES

FINAL TECHNICAL REPORT

February 1973

Prepared by

Theodore I. Kamins

Fairchild Camera and Instrument Corp.
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Mountain View, California 94040

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Hall measurements of p-type films indicated mobilities close to the bulk values while the mobilities observed in n-type films were probably influenced by the presence of an accumulation layer near the bottom surface of the film. Minority-carrier lifetimes of the order of 10 μsec have been found by injection of carriers across junctions and by generation near the surfaces of deep-depletion MOS structures. To first order the diffusion characteristics of both boron and phosphorus are similar in the thin films and in bulk wafers as is the oxidation rate. Lattice parameter measurements indicated that the stress is probably at least a factor of 40 less in the electrochemically etched films than in silicon-on-sapphire films.

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by Theodore I. Kamins

High-quality, thin silicon films suitable for bipolar, as well as MOS, devices can be reproducibly fabricated using this technique. This structure, therefore, provides an attractive alternative to the silicon-on-sapphire system and is preferable because of the superior quality of the silicon film formed, the ease of subsequent device fabrication, and the compatibility with well-defined, conventional silicon technology. Further research efforts can be most productively devoted to gaining understanding of and control over the Si/SiO_2 interface beneath the thin silicon film.

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I. INTRODUCTION

This report summarizes the results of a nine-month, research-and-development study of the material properties of thin, single-crystal silicon films supported by insulator/polycrystalline-silicon substrates. To fabricate this structure a lightly doped silicon film is epitaxially grown on a heavily doped, n-type, single-crystal silicon wafer. The structure is then covered with an insulator (e.g., silicon dioxide), and a thick layer of polycrystalline-silicon is deposited over the entire wafer. The heavily doped, single-crystal substrate is then removed by an electrochemical-etching process which terminates at the epi/substrate interface, leaving a thin, uniform, single-crystal silicon film on an insulating layer on top of the semi-insulating polycrystalline silicon. In this manner, a film of high-quality, single-crystal silicon can be fabricated on a substrate which is essentially insulating. The oxide film has the usual insulating properties of thermally grown silicon dioxide, and the resistivity of the polycrystalline support is about 10^5 - 10^6 Ω-cm.

For the last decade, the semiconductor industry has been dominated by silicon technology. In present-day silicon Planar technology, devices are fabricated only in the top few microns of the silicon wafer, and integrated circuits are formed by connecting various devices together with metallization on top of the silicon wafer. The rest of the silicon simply serves as a supporting substrate. Although the complexity of integrated circuits has increased enormously, the basic concept of utilizing only the top few microns of the silicon wafer has remained unchanged for the past ten years.

Silicon technology is presently encountering significant limitations, however. For example, integration of the component devices into a circuit is often constrained by the fact that all devices are fabricated from the same surface. Cell size is often limited by the requirement that all metallization be on the top side. Circuit performance is usually limited by parasitic capacitances to the substrate materials. Preliminary investigation indicates that all of these limitations can be reduced by use of the structure containing high-quality, silicon films

a few microns thick on a dielectric substrate, which is the subject of this report. The development of this materials system has broad and far-reaching implications. It represents a fundamental change in the concept of silicon technology; i.e., devices and interconnections may be placed on both sides of the thin film, thus allowing greater flexibility in the integration of circuits and functions and achieving size reduction. Furthermore, performance will be significantly improved since the parasitic capacitances can be drastically reduced by using a dielectric substrate.

The program discussed in this report represents an effort to refine and study the fabrication processes and the materials properties of the thin silicon film on dielectric substrate in order to achieve the necessary understanding and control of this structure so that it may serve as the basis of a major advance in silicon technology. The approach taken during this study involved an interaction of the process development and the materials investigation. First, considerable effort was devoted to developing reproducible processes for the fabrication of these thin films, and methods were developed to evaluate their quality. The causes of the defects occurring in the films were investigated, and continuing efforts were made to minimize their occurrence. Since device properties are sometimes the most sensitive indicators of material quality, large-area bipolar transistors were fabricated to investigate the quality of the thin films and their suitability for complex bipolar integrated circuitry. Fabrication of these devices also allowed the evaluation of process variations and insured that the materials study was directed toward properties which are relevant to the applications for this technology.

After reasonable film quality had been obtained, the properties of the films were investigated in more detail. The majority-carrier mobility and minority-carrier lifetime were studied. Diffusion of dopant impurity atoms into the films and oxidation of the films were considered, and the stress in the thin films was investigated. Throughout these investigations, the properties of the thin films were compared to those in bulk, single-crystal wafers so that any differences could be seen. In the case of the stress measurements, results from the electrochemically etched thin films were compared to those from silicon-on-sapphire films.

2. SUBSTRATE FABRICATION

2.1 Introduction

The basic technique for fabricating the composite substrate will be discussed in this section. This basic structure is shown in Fig. 2.1 and is composed of the thin single-crystal silicon film on an insulating layer on top of a polycrystalline-silicon mechanical support.

The thin film is obtained in the following manner. A highly doped, n-type, single-crystal silicon wafer is cleaned and placed in an epitaxial reactor, where about 3 μm of silicon is removed by vapor etching. A lightly doped epitaxial film of silicon is then grown on the heavily doped substrate. This film is generally formed by the thermal decomposition of silane at approximately 1040°C in order to obtain an abrupt change in dopant concentration at the epi/substrate interface. This sharp interface is necessary in order to achieve a well-defined endpoint for the electrochemical-etching process. Since the epitaxial film becomes the single-crystal film in which devices are fabricated, its thickness and resistivity are chosen to be suitable for the desired device. Thicknesses of 1-10 μm have been used while the resistivity was normally about 5 Ω-cm. After the epitaxial film is formed, it is covered with an insulator, such as thermally grown silicon dioxide.

The deposition of a thick layer of polycrystalline silicon on the insulator then follows. Since this layer serves as the mechanical support for the thin film of single-crystal silicon, it should have adequate mechanical strength. Layers about 250 μm thick are generally used. In order to avoid severe impurity redistribution at the epi/substrate interface, the polycrystalline silicon is deposited at a relatively low temperature by using either silane or dichlorosilane. The latter gas is generally used because of the more uniform deposition obtained.

After the thick polycrystalline support film is deposited, the original, heavily doped silicon substrate is removed by electrochemical etching. After some chemical or mechanical thinning the wafer is inserted into the electrochemical-etch bath, which contains a 6-7% hydro-

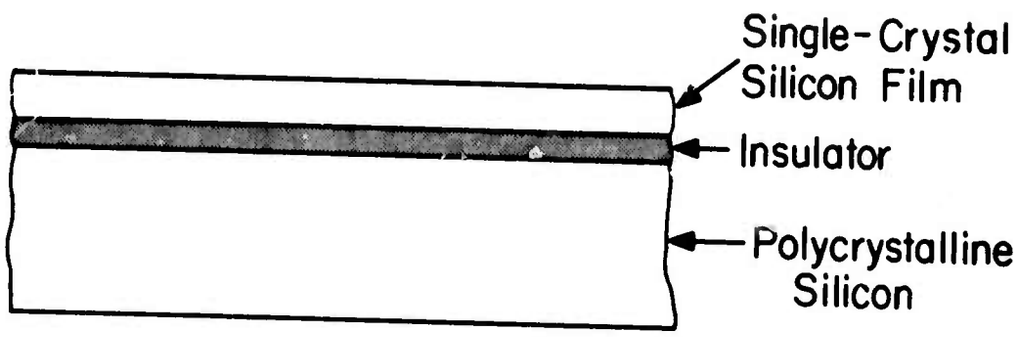

Fig. 2.1. Cross section of composite substrate.

fluoric-acid electrolyte. The remainder of the heavily doped silicon is removed, leaving the lightly doped, epitaxially deposited, silicon film on top of an insulating layer on a semi-insulating, polycrystalline-silicon support.

Since the wafer often shows some staining during the last stages of the electrochemical-etching process, approximately 0.5 μm of silicon is generally removed by vapor etching at 1200°C in order to provide a good quality surface for subsequent device fabrication. Although the physical position of the end-point of the electrochemical etch is well defined, the dopant concentration at the end-point is not as clear. Therefore, the removal of a small amount of silicon by vapor etching also insures a more uniform and controllable surface dopant concentration. In this manner a thin, smooth silicon film of uniform thickness on an insulator/polycrystalline-silicon support is obtained.

Each step of the fabrication process will be discussed in some detail in this section with further comments on some critical steps and a discussion of the film quality in the following section.

2.2 Starting Wafer

Although the starting wafer used in the fabrication of the thin films is completely removed during the electrochemical-etching process, its quality and resistivity strongly influence the quality of the thin film formed. The electrochemical etch rate of silicon depends strongly on the resistivity of the material being etched (1). In order to maximize the difference in etch rate between the substrate and the epitaxial layer which becomes the thin silicon film, the difference in resistivity must be maximized. In particular, the etch rate of the substrate should be maximum, and hence its resistivity should be minimum. The lowest resistivity which can be conventionally obtained with antimony-doped silicon is about 0.005 Ω-cm while a resistivity of about 0.0015 Ω-cm can be achieved with arsenic. Consequently, arsenic-doped wafers with a nominal resistivity of 0.0015-0.0025 Ω-cm were used as starting substrates throughout this investigation. In addition, the diffusivity of arsenic in silicon at 1100°C is about 20% less than that of antimony; consequently, less diffusion of the substrate dopant into the epitaxial

film will occur during the deposition of the polycrystalline-silicon support layer when arsenic-doped wafers are used.

Previous investigations (2) have shown that the removal of n^+ silicon proceeds more uniformly than the removal of p^+ silicon. Although a recent study (3) indicates that p^+ silicon can also be removed uniformly by the proper choice of electrolyte, n^+ substrates were used throughout this investigation.

The quality of the starting wafer is probably more important than its exact resistivity in determining the quality of the final thin film formed. Dislocations in the starting wafer, especially, are seriously detrimental since they will propagate into the epitaxial film. During electrochemical etching these dislocations will be sites of rapid hole generation and, consequently, will etch more rapidly than the remainder of the film. Since the film is quite thin, the etch channel thus formed may extend completely through the film.

In an effort to understand the influence of the starting wafer on the defect formation which occurs during electrochemical etching, it was necessary to evaluate the heavily doped starting wafers. The evaluation of this type of wafer is not trivial since normal dislocation etches, such as Sirtl etch, do not reliably reveal dislocations in n^+ material. Consequently, epitaxial films were grown on the wafers to be studied. Arsenic doped, 0.0015-0.0025 Ω-cm, (111)-oriented silicon wafers with both low dislocation density and high dislocation density were initially investigated.

After the starting wafers were cleaned, they were inserted into the reactor and heated to approximately 1250°C (corrected temperature) for a 5-minute vapor etch which removed about 3 μm of silicon. The reactor was then cooled to 1035°C for the deposition of the silicon film from a silane source. In the present experiment some wafers were subjected to the vapor-etch cycle only while a 10 μm-thick, 7 Ω-cm, p-type epitaxial film was grown on others. The wafers were then chemically etched for 30 seconds in a 1:1 solution of Sirtl etch and concentrated hydrofluoric acid to reveal dislocations.

Well-defined etch pits were seen on the epitaxial films. These

etch pits were triangular and relatively uniform in size. Their density in the high-dislocation-density silicon was of the order of 10^5 cm^{-2}, which is about the expected dislocation density in this material. The density of etch pits in the low-dislocation-density wafer was several orders of magnitude less, probably about 100 cm^{-2}. Other defects, such as small circular pits, probably due to compositional nonuniformities, were sometimes seen. No etch pits were seen on either the high-dislocation-density or low-dislocation-density wafers which were only vapor etched, confirming the unreliability of dislocation etches on n^+ material. The high-dislocation-density wafer which had been vapor etched and then Sirtl etched also showed circular banding, probably characteristic of oxygen segregation. Further etching on the low-dislocation-density wafer revealed similar, but much weaker, banding. After the growth of the 10 μm-thick epitaxial film and Sirtl etching, no circular banding was visible on either type of wafer after a two-minute Sirtl etch, indicating that the oxygen did not propagate into the film.

In order to investigate the influence of the dislocation density in the starting substrate on the defect formation during electrochemical etching, silicon films approximately 1.5–2 μm-thick were formed on both low- and high-dislocation-density starting wafers. After the electrochemical etching, the films were examined under the dark-field microscope. The density of defects in the film formed on the high-dislocation-density substrate was about 2 X 10^5 cm^{-2}, while that on the low-dislocation-density material was several orders of magnitude lower, in good agreement with the dislocation density in the starting wafers. When there is a high density of defects in the electrochemically etched film from dislocations in the starting wafer, the 6-fold symmetry characteristic of dislocations in (111)-oriented material is especially apparent (Fig. 2.2). In one case, this characteristic 6-fold defect pattern was seen on films fabricated on nominally low-dislocation-density starting wafers. The defects were traced to defective wafers and subsequently to a crystal which was pulled from the melt too rapidly. Because of the demonstrated importance of the dislocation density, starting wafers with a dislocation density of less than 500 cm^{-2} were specified.

X-ray topographs of a high-quality, low-dislocation-density wafer revealed some surface damage. By removing 10 μm from each surface of

Fig. 2.2. Dark-field photomicrograph showing 6-fold symmetry of defects in poor-quality electrochemically etched film (142X).

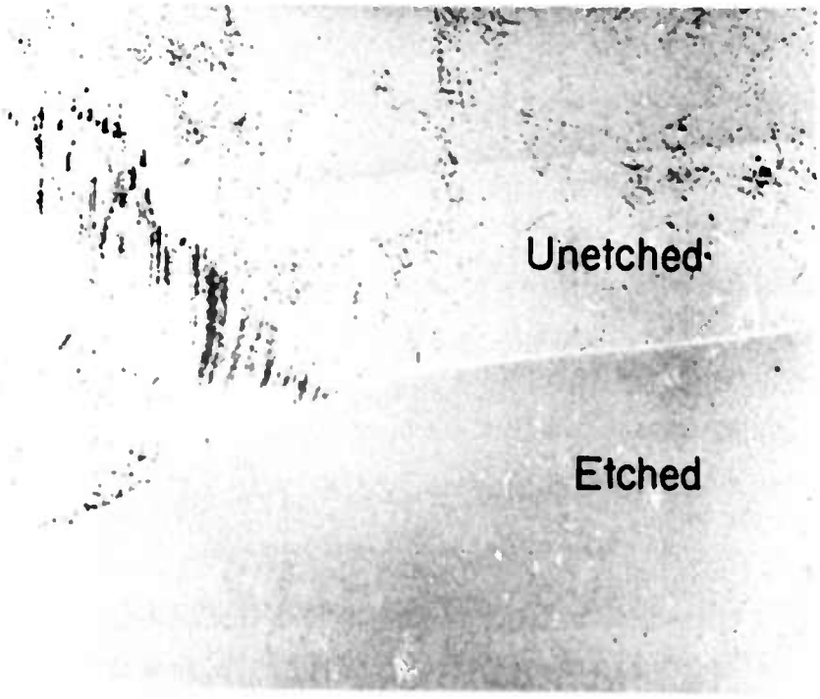

Fig. 2.3. [$2\bar{2}0$] topograph in region of backside etch (3X).

the wafer (in different areas) and repeating the topographs, the damage was shown to be limited to the back of the wafer (Fig. 2.3). This result indicates the importance of removing sufficient material from the back of the wafer during its fabrication since residual damage may propagate into the bulk of the wafer during subsequent heat treatments.

One additional anomaly was observed on epitaxial films deposited on wafers from one ingot. The resistivity of p-type films grown on these wafers was consistently observed to be lower than the resistivity of films simultaneously grown on other nominally similar wafers as well as on wafers of different resistivity or substrate orientation. The effect of wafer placement in the reactor has been eliminated as a possible cause of the behavior. This anomaly has not been investigated in detail, but it is tentatively attributed to the presence of a fast diffusing impurity in the questionable ingot.

One of the primary difficulties experienced throughout this investigation was obtaining an adequate supply of starting wafers. Very few suppliers will fabricate arsenic-doped substrates, especially with the low resistivity and dislocation density specified in the current study. In addition, the undercapacity of the silicon industry during a portion of this study became apparent as the delivery time changed from 4 weeks to 3 months. For high-volume production utilizing this technique, a greater number of suppliers must become available.

2.3 Epitaxial Deposition

Before the wafers were inserted into the reactor, they were cleaned with the following sequence of chemicals:

3 H_2SO_4 : 1 H_2O_2	:	5 min
DI water rinse	:	5 min
Aqua Regia	:	3 min
DI water rinse	:	5 min
10:1 DI water:HF dip	:	30 sec
DI water rinse	:	3 min
Isopropyl Alchol Dry	:	3 min

After cleaning, the wafers were loaded into the epitaxial reactor. A

conventional, R-F heated, horizontal epitaxial reactor* was used. The wafers were heated to 1250°C (corrected temperature) in a hydrogen carrier gas and etched for 5 minutes in HBr in order to remove about 3 μm of silicon from the wafer surface. The temperature was then lowered to about 1040°C, and the epitaxial film was grown, generally from silane at a rate of about 0.5 μm/min. In order to investigate the possibility of using dichlorosilane rather than silane, one series of epitaxial films was grown from dichlorosilane.

During deposition the dopant impurities were added to the gas stream from phosphine or diborane in order to obtain the desired type and resistivity epitaxial layer. Both n-type and p-type films of about 5 Ω-cm have generally been used. In some cases, however, no dopant was added to the epitaxial film during deposition. The effect of the different dopant concentrations will be discussed in Sec. 3.4.3.

After removing the wafer from the reactor, the thickness was measured by infrared spectrometry. For the thicker films, the curves of Albert and Combs (4) were used while the thinner films were evaluated with a nomogram constructed for the particular substrates used from the data of Schumann (5).

This nomogram is shown in Fig. 2.4 for substrate dopant concentrations of 3 and 5 X 10^{19} cm^{-3}. In this manner films as thin as 1 μm could be easily evaluated. The meaning of the absolute thickness determined for such a thin film is not clear since the epi/substrate interface extends over an appreciable fraction of the film thickness. However, this method of thickness evaluation provides a rapid, and nondestructive indication of the relative thickness of various samples and allows the reproducibility of the process to be easily determined.

The quality of the epitaxial films was evaluated by Sirtl etching, and few defects were found when low-dislocation starting wafers were used. In particular, very few stacking faults were seen ($\lesssim 1$ cm^{-2}).

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* Applied Materials Technology AMH-620

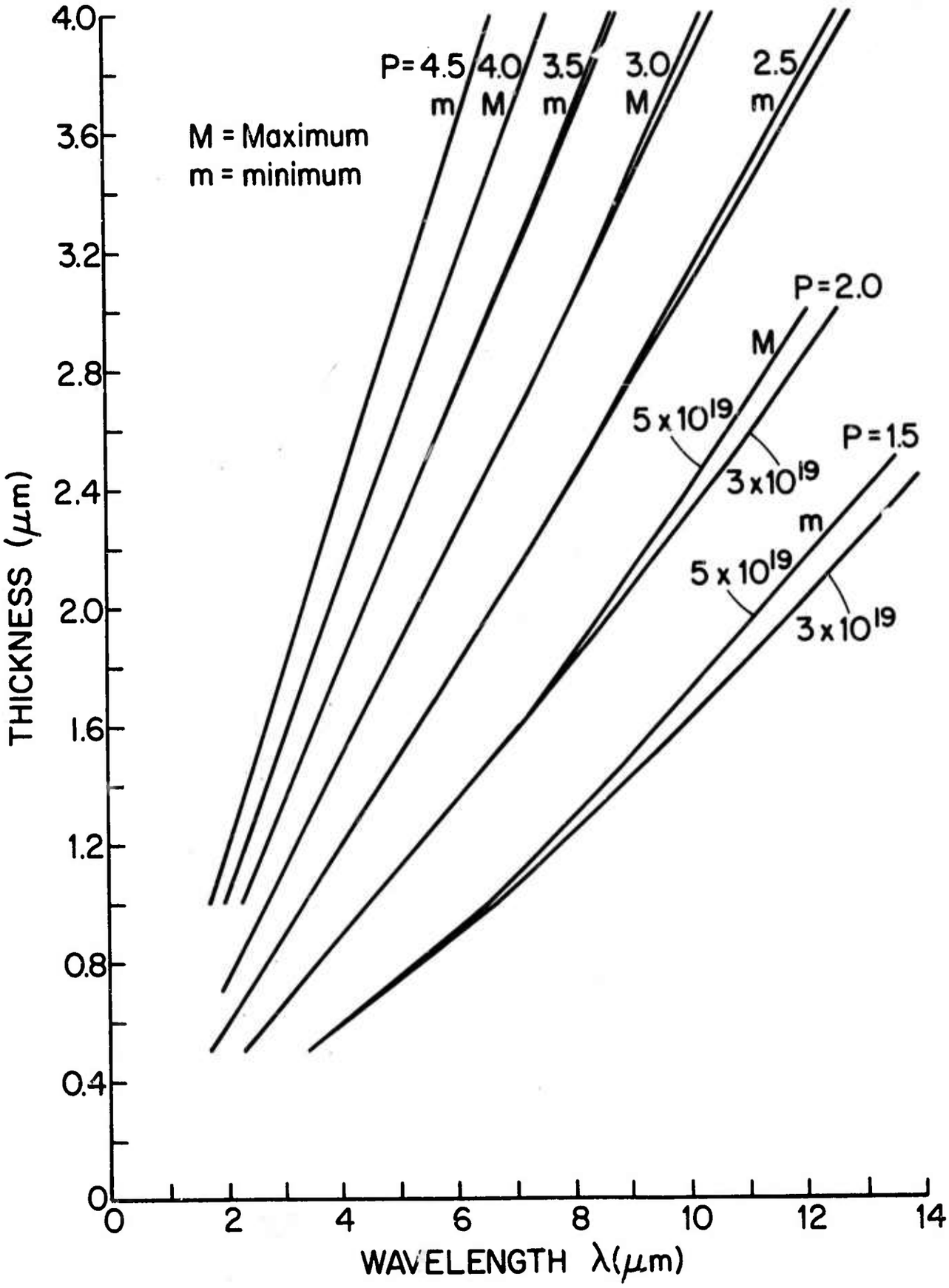

Fig. 2.4. Nomogram for infrared reflectance determination of epitaxial film thickness for 3 and 5 X 10^{19} cm^{-3} n^+ substrate.

The thinnest films fabricated indicated a thickness of about 1.7 μm after the initial epitaxial deposition.

2.4 Oxidation

Although previous experiments indicated that several different insulating layers or combinations of layers could be used, most of the composite substrates fabricated during this study employed a layer of thermally grown SiO_2 about 0.3 μm thick for simplicity of processing. This layer was formed primarily in a steam ambient at 920°C after initial purging in dry N_2 and then dry O_2. The short, dry O_2 cycle may be especially important in preventing dislocation formation in (100)-oriented wafers (6). Oxidation times of 75 minutes and 105 minutes were generally used for (111) and (100)-oriented silicon, respectively, in order to obtain approximately the same oxide thickness on wafers of the two different orientations. Conventional diffusion furnaces were used for the oxidations. The $\sqrt{Dt}$ during the oxidation was much less than that experienced during the subsequent polycrystalline-silicon deposition so the oxidation did not contribute significantly to the redistribution of impurities at the epi/substrate interface.

2.5 Polycrystalline-Silicon Deposition

After the layer of insulating SiO_2 is formed on the wafer, a thick layer of polycrystalline silicon is deposited. Since this layer becomes the mechanical support for the thin, single-crystal silicon film, its thickness is typically about 250 μm. A deposition rate of approximately 4 μm/min is generally used so that the entire film is deposited in one hour. In early experiments both silane and dichlorosilane were investigated as source gases, and the latter gas was found to be more suitable for this application for two reasons: First, the surface of the thick layer was smoother when dichlorosilane was used. Second, markedly less silicon was deposited on the quartz reaction chamber with dichlorosilane at the high deposition rate used to form this thick layer.

With either silane or dichlorosilane the deposition was started directly on the clean SiO_2 surface of the wafer. No nucleating layer,

such as must be used with silicon tetrachloride, was needed in the temperature range of interest. At temperatures below about 900°C, however, a nucleating layer may be necessary when dichlorosilane is used, but none is needed with silane at any temperature at which the pyrolysis reaction proceeds.

The temperature used for the deposition represents a compromise between two competing limitations. First, a low deposition temperature is desired so that minimum impurity redistribution occurs at the epi/substrate interface and a well-defined end-point for the electrochemical-etching process is retained. A low deposition temperature also minimizes deposition on the walls of the quartz reaction chamber. Significant deposition on the walls can increase the heat reflected back to the silicon wafer and change the temperature in an uncontrolled manner, leading to nonuniform and nonreproducible film thicknesses and impurity redistribution. On the other hand, the quality of the deposited polycrystalline-silicon film has been found to increase with increasing temperature.

The degradation often observed at low temperatures has been related to the presence of trace quantities of active gases, such as oxygen, in the deposition chamber. With a given quantity of residual oxygen in the reaction chamber, the quality of the polycrystalline film decreases rapidly with decreasing temperature. Therefore, a lower bound on the useful temperature range is set by the amount of residual oxygen in the system. In addition, the temperature must be high enough to remain in the mass-transfer-limited region of deposition in order to retain control over the thickness of the deposited film. However, in presently available reactor systems, the limitation imposed by oxygen contamination is more severe. The effect of oxygen will be discussed in more detail in Sec. 3.2.

Since the lower temperature that can be used is strongly dependent on the tightness of the reactor system, the importance of minimizing leaks cannot be overemphasized. Frequent leak checking was employed as a routine precaution, and the system was immediately leak checked whenever the film quality began to degrade. In the latter case, the film degradation could almost invariably be traced to a leak in the plumbing.

The system was checked by pressuring with helium and using a mass-spectrometer leak detector on the outside of the system. While evacuating the system and using helium on the outside is a somewhat more sensitive technique, a reactor cannot usually be evacuated because of check values in the plumbing system. The use of a mass-spectrometer detector is mandatory. Leak detecting liquids which form bubbles at leaks are completely inadequate in finding the size of leak which can degrade the polycrystalline-silicon films. One particularly troublesome location in the reactor was the end-plate which sealed the loading port of the reactor during the deposition.

After the reactor and associated plumbing were made as leak free as possible, a temperature of about 1100°C (corrected temperature) was determined to be optimum. The impurity redistribution expected during the deposition is indicated in Fig. 2.5. As the amount of redistribution increases, the thickness of the film remaining after electrochemical etching decreases and becomes less reproducible. However, as the quality of the polycrystalline-silicon film increases, less defects are induced in the single-crystal wafer during the polycrystalline deposition, and the quality of the electrochemically etched film increases. Therefore, the deposition of the thick layer of polycrystalline-silicon demands minimization of the presence of oxygen in the system and then operation at the minimum temperature possible, consistent with the remaining trace quantities of oxygen in the system.

During the early stages of the investigation, the wafers were placed on a standard, flat, silicon-carbide-coated, graphite susceptor in the reactor. During the deposition, however, the polycrystalline-silicon deposited around the edges of each wafer as well as on its exposed surface. Since the deposited film was about the same thickness as the original wafer, the wafer often became firmly attached to the susceptor and could not be removed after the deposition. Therefore, a susceptor was obtained with grooves cut into the surface before it was coated with silicon carbide (Fig. 2.6). A groove was located at the periphery of each wafer so that the wafer sat on a pedestal with its edges extending slightly over the groove. In this manner the wafer could not become attached to the susceptor. This system does have the

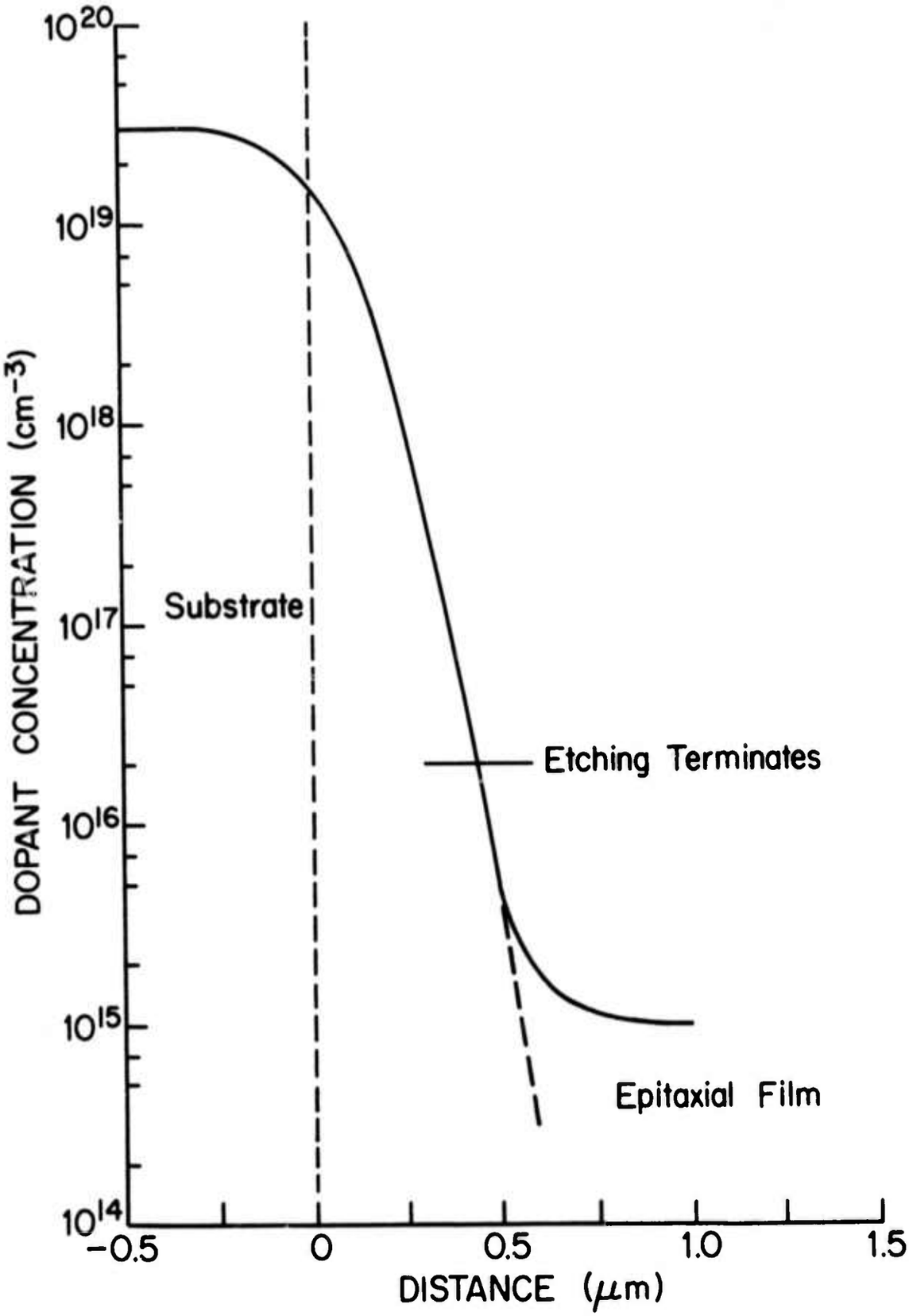

Fig. 2.5. Impurity redistribution at epi/substrate interface during deposition of polycrystalline silicon.

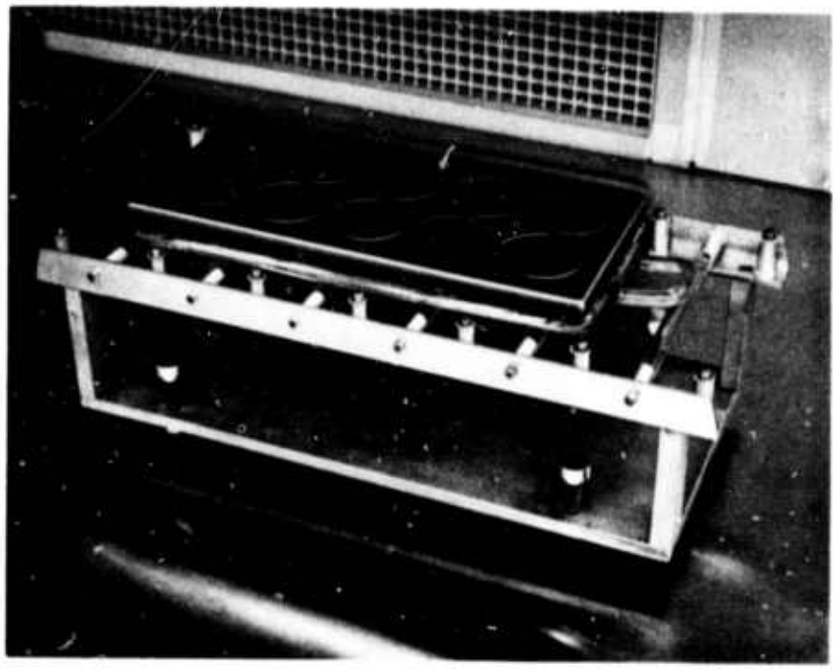

Fig. 2.6. Photograph of susceptor used for deposition of thick polycrystalline-silicon films, showing grooves cut into surface; note that the wafer edges extend slightly over the grooves to prevent adhesion.

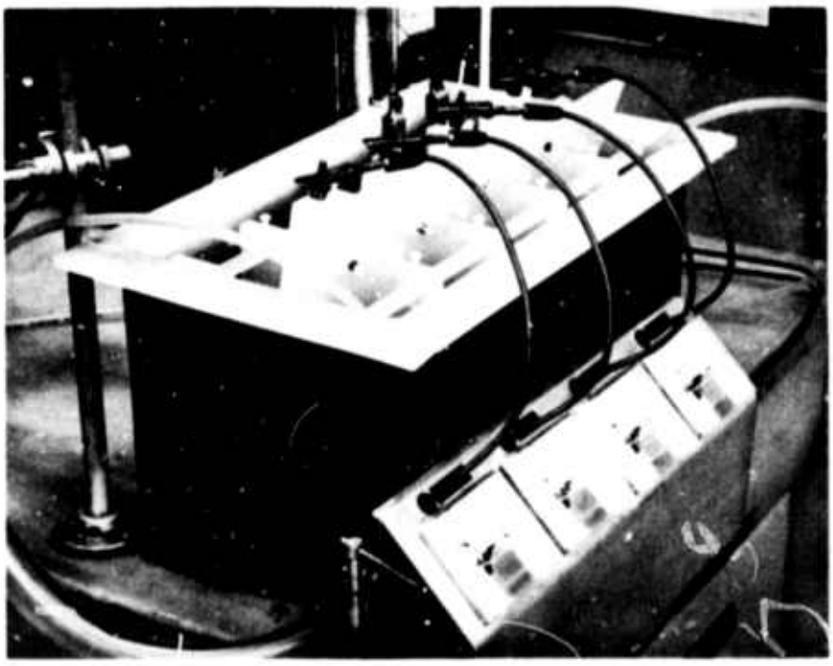

Fig. 2.7. Photograph of 4-wafer, electrochemical-etch bath, showing fixtures and individual ammeters to monitor completion of etching.

disadvantage that the wafer diameter cannot be changed significantly without fabricating a new susceptor since the pedestal diameter must be only slightly smaller than the wafer diameter. The diameter of the wafers used in the current study was specified as 2 ± 1/8" and no difficulties were encountered with variations in the diameter of the wafers.

2.6 Preparation for Electrochemical Etching

After the thick film of polycrystalline silicon was deposited, the wafer was prepared for electrochemical etching. During the previous step polycrystalline silicon was deposited on the edges of the wafer as well as on the back surface. Since this undoped polycrystalline silicon would not be removed during the electrochemical etch, the edge of each wafer was ground on a belt sander to remove this deposit. If the polycrystalline silicon were not removed from the edge of the wafer, a ledge would be left after electrochemical etching, and a photo-mask could not be brought into contact with the wafer.

The back surface of the wafer was then cleaned, and in some cases a portion of the thickness of the heavily doped, single-crystal silicon was removed either by chemical etching or by mechanical lapping. In order to reduce the electrochemical-etching time, the wafer should be thinned as much as possible before it is inserted into the etch bath. Lapping to a thickness of about 350 μm was found to be optimum when the polycrystalline-silicon film was about 250 μm thick. If the wafer was lapped to 300 μm, the thickness of the remaining, single-crystal substrate was often too nonuniform to etch properly. Mechanical lapping was found to be more satisfactory than chemical etching since chemical etching generally proceeded more rapidly near the edge of the wafer and left the single-crystal silicon thinner in the region where electrical contact was made during electrochemical etching. This area could then etch through before the thicker material was removed from the center of the wafer, preventing complete removal of the silicon substrate. In most cases the wafer was not substantially thinned before being inserted into the electrochemical-etch bath in order to simplify the process, although the etch time was longer.

In all cases, however, it was necessary to remove at least 10-15 μm of silicon from the back surface of the wafer. During the vapor etch

before the growth of the initial epitaxial film, silicon is transferred from the susceptor to the back of the silicon wafer. Since this silicon is intrinsic, it will not etch in the electrochemical etch and must be removed before the wafer is inserted into the etch bath. This small amount of silicon removal does not cause appreciable rounding of the wafer.

In some cases, especially when extensive evaluation of the wafer was to be performed after electrochemical etching, the wafer was mounted on a glass slide so that it could be handled more readily. This step is generally not necessary since the polycrystalline silicon can be exposed to the electrolyte in the electrochemical-etch bath without deleterious effects.

2.7 Electrochemical Etching

Once the wafer is prepared, it is inserted into the electrochemical-etch bath. Since this electrochemical-etching process is crucial to the preparation of the thin silicon films, it will be discussed in some detail. The etch bath and etching procedure will be described here while the results of etching experiments will be discussed in Secs. 3.3-3.7.

The basic electrochemical cell is similar to that conventionally used. The positive terminal of the power supply is connected to the periphery of the wafer to be etched; the negative side is connected to a graphite counter-electrode; and a dilute HF electrolyte (generally 6-7% HF) is used. However, the approach employed in this case to insure complete removal of the single-crystal substrate differs from the technique previously reported (7). If the substrate is completely etched near the electrical contact area, little current can flow to the unetched portions of the wafer, and little further etching will take place. Therefore, care must be taken to ensure that the silicon farthest from the contact area is etched before the area near the contact. In the previous case (7), the wafer was gradually lowered into the electrolyte. In the present case, however, the geometry of the etch bath was chosen to ensure that the etching proceeded most rapidly at the areas furthest from the contact. The wafer could thus be immersed

fully at the start of the etch cycle, reducing the complexity of the experimental apparatus. The simplicity thus afforded is more compatible with large volume production.

The influence of the etch-bath geometry can be seen by considering the division of the applied voltage into three components: the voltage dropped in the electrolyte, that appearing across the silicon/electrolyte interface at the surface of the sample being etched, and the IR voltage drop in the wafer itself. This latter component will be more significant further from the contact area. Consequently, if the voltage drop in the electrolyte is uniform across the wafer surface, the interface potential will be greater and the etching will proceed more rapidly near the contact. In the present case the geometry was adjusted so that the voltage drop in the liquid was reduced near the area of the wafer farthest from the contact to overcompensate for the additional IR drop in the wafer. In this manner the interface potential was maximum farthest from the contact area, and the etching proceeded most rapidly there. This was accomplished by inserting the wafer into the etch bath at an angle so that the bottom of the wafer was nearer the cathode than was the top of the wafer, where the contact was located. In addition, nonconducting partitions were placed in the etch bath between adjacent wafers in order to confine the field lines in the electrolyte so that the edges of the wafer did not etch much more rapidly than the center. These partitions also minimized interaction between adjacent wafers. In earlier experiments without the partitions, the etching was found to progress differently if one, two, or three wafers were simultaneously etched. Photographs of the etch bath are shown in Figs. 2.7 and 2.8.

Also unlike previous investigations, the etching was found to proceed most satisfactorily if the electrolyte was agitated so that fresh solution was constantly impinging on the wafer surface. If no agitation was employed, the solution near the wafer surface could become depleted and a stain film would form.

The wafer was first positioned in a spring-loaded clip (Fig. 2.9) so that a platinum wire was in contact with the wafer along the length of the wafer flat. The clip was then inserted into the etch bath until the top of the solution was at the level of the platinum wire. The

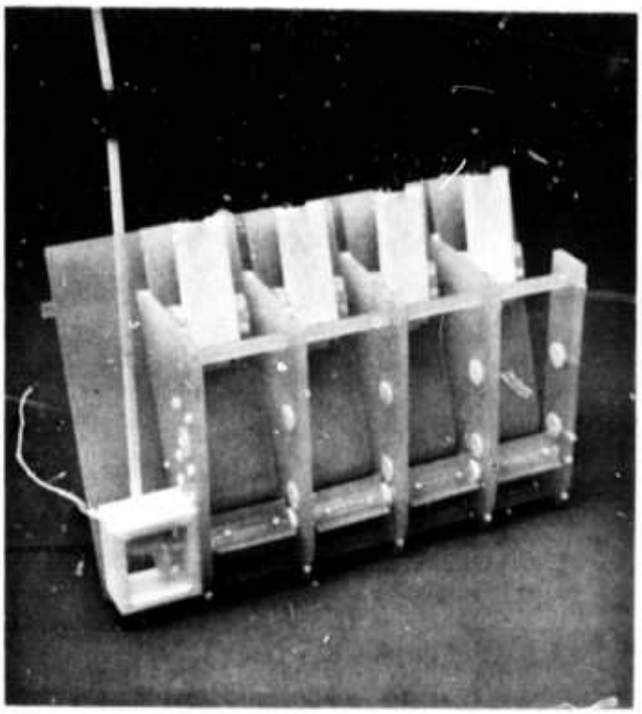

Fig. 2.8. Photograph of fixtures from 4-wafer etch bath showing partitions between compartments and method of agitation of solution (near bottom).

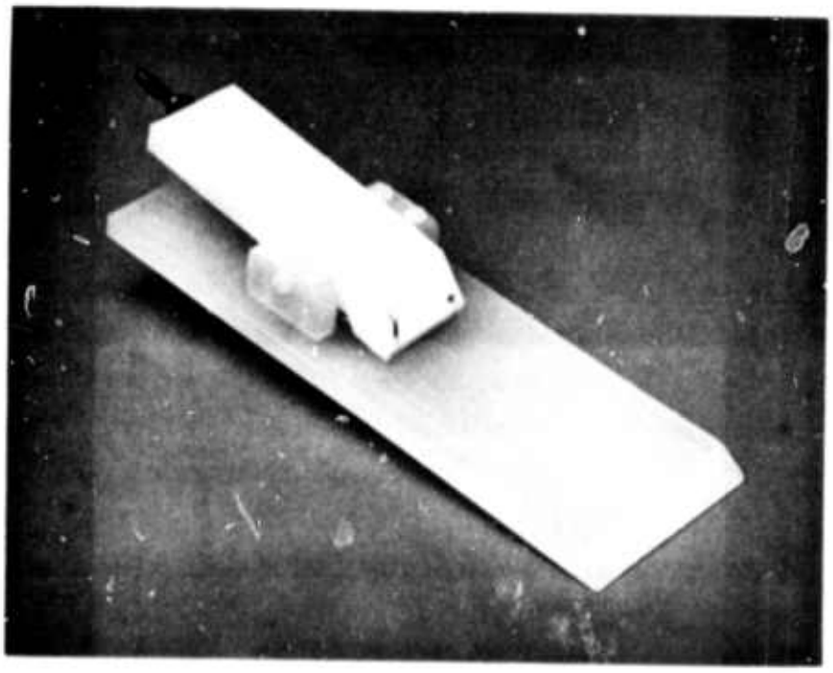

Fig. 2.9. Photograph of clip which holds wafer and provides electrical contact in the etch bath; wafer is held against large backing plate and electrical connection is made by platinum wire running under lighter-colored section.

fixturing in the etch bath ensured that the wafer was always held at the same angle. The etch bath and fixtures were fabricated from polyethylene, teflon and nylon, which were not severely attacked by the dilute HF electrolyte used.

The current was supplied by a constant-voltage, regulated power supply, generally with about 10 V applied. The current was monitored on a 0-3 A DC ammeter individually for each wafer. The current was initially about 2.5-2.8 Amps and decreased as the etching proceeded. The termination of etching could be determined fairly easily by observing the current decrease. When several wafers were etched simultaneously, more than 75 watts could be dissipated, with a significant increase in the temperature of the electrolyte. Therefore, the solution was cooled with water running through polyvinyl-chloride tubing inserted into the etch bath. The cooling was found to be more important for (100)-oriented wafers than for (111)-oriented wafers.

Since the IR drop, and hence the amount of compensation required to ensure more rapid etching farthest from the contact area, depended on the resistivity of the substrate, fairly close control was required on the substrate resistivity. Substrates of significantly different resistivity could not be etched under the same conditions once the angle was fixed. Substrates of higher resistivity required lower initial currents in order to obtain the same degree of compensation. As the initial current decreased, the etch rate, of course, decreased also.

After the etching was completed, the wafer was immersed in aqua regia for ten minutes in order to remove loosely adherent particles left on the surface as well as any metallic contaminants from the etch bath. These particles were probably amorphous silicon. The area to which the contact was made during the electrochemical etching was then removed by conventional scribing.

2.8 Surface Layer Removal

In order to remove a possible residual layer with different impurity concentration from the surface of the film as well as to obtain a better quality surface for further device processing, the wafer was generally vapor etched. The vapor etching was performed in the epitaxial

reactor at a temperature of 1200°C (corrected). About 0.5-1 μm of silicon was generally removed from the wafer surface. The vapor etching provided close control over the final film thickness and allowed films thinner than otherwise possible to be obtained. The heating and cooling rate during this operation was found to influence the deformation of the wafer; rapid cooling, especially, was found to increase the convex curvature of the substrate (as viewed from the thin-film side).

Vapor etching was particularly suitable for (111)-oriented material, which was uniformly removed by the HBr etching gas used in these experiments. However, (100)-oriented material was not removed uniformly, but was attacked perferentially at defects on the film surface so that these defects were accentuated during the vapor-etch cycle. Consequently, (100)-material was generally thinned by oxidizing the film and then stripping the oxide. The oxide was generally grown at 1100°C in a steam ambient after initial purging of the oxidation furnace in dry N_2 and then in dry O_2. The insertion and removal rate were found to be important since the wafers could warp severely if improperly handled. The wafers generally became less convex or even concave after this treatment. This reversal of the curvature is consistent with the behavior observed in other investigations (8). Removal of the surface layer by chemical etching was also attempted, but the thickness control available, as well as the surface quality after chemical etching, was found to be less satisfactory than the other techniques investigated.

2.9 Device Fabrication and Die Separation

After the surface layer was removed by either vapor etching or oxidizing and stripping, the thin film was ready for device fabrication. Conventional, silicon device processing was employed, with the exception that the wafers were inserted into and removed from high-temperature (1100°C or higher) furnaces slowly. After device processing, the wafers were diced into individual chips. Although conventional scribing techniques were generally acceptable as long as the wafer was thinned before scribing, other die separation techniques were considered since it was initially felt that conventional scribing would be difficult in the polycrystalline material, which lacks definite cleavage

planes.

Since the polycrystalline silicon deposited from dichlorosilane under the conditions employed in this study contains primarily {110}-texture (9), an anisotropic KOH etch was used in order to obtain a greater rate of vertical etching than lateral etching. In this manner the amount of material lost during die separation was minimized, and circuit density could be maximized. A silicon nitride film was deposited on the polycrystalline-silicon side of the wafer to be separated, and this nitride layer was defined with a mask of the same size as the integrated circuit chip. The wafer was then placed in a warm (about 70°C) solution of KOH (about 40%) until the polycrystalline silicon was etched. This technique left well-defined, nearly vertical edges on the polycrystalline-silicon chips as seen in Fig. 2.10. The vertical structure of the polycrystalline silicon itself is readily apparent in this figure.

Two difficulties were encountered with this process, however. First, the silicon nitride used to mask the etching did not always maintain its integrity for the complete etch time. The variable chemical resistance is probably related to variations in the structure of the silicon-nitride films obtained. Second, the face of the wafer must be protected during the etching in order to prevent attack of the completed integrated circuits. This is most easily acomplished by waxing the wafer face down onto an inert carrier. No wax suitable for use at the etch temperature has yet been located. Consequently, further development of this process is necessary although the results to date appear to be quite promising.

Commercially available laser-scribing equipment* was used for the laser-scribing experiments. Figure 2.11 shows a cross section of a 1-mil deep cut made by the laser in the silicon film/oxide/polycrystalline-silicon structure. This depth produced a high yield of good dice, but a deeper cut may be optimum.

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* from Electroglas Inc., Menlo Park, CA.

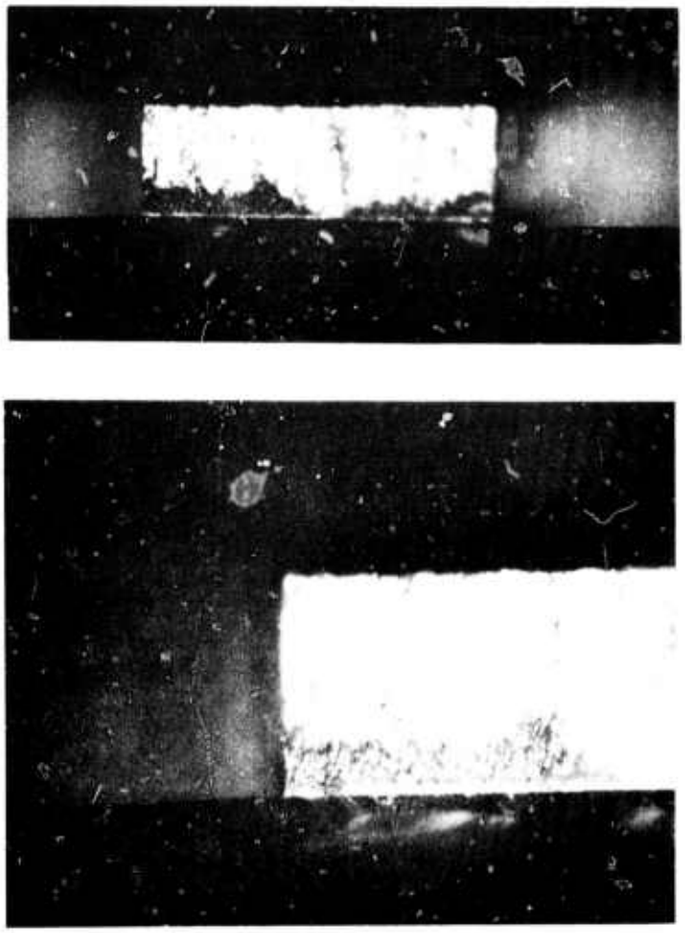

Fig. 2.10. Side view of polycrystalline-silicon island formed by etching with KOH, showing vertical edges; (a) 71X, (b) 142X.

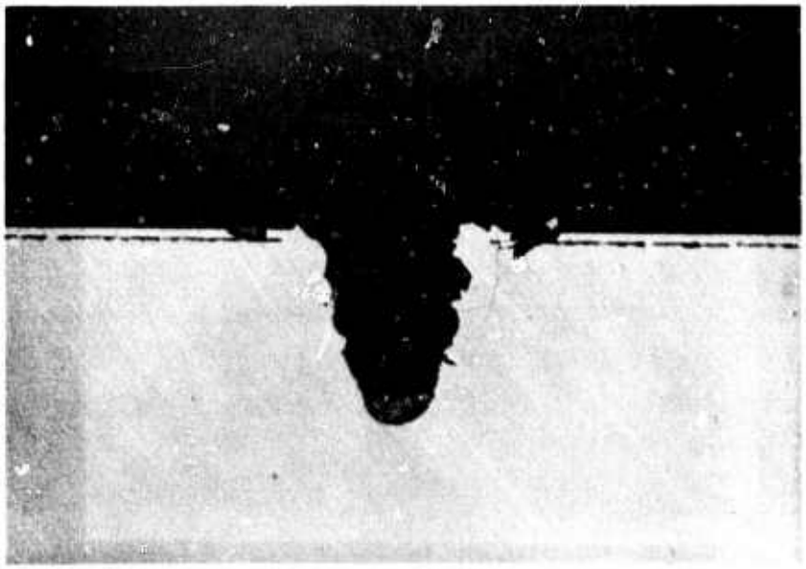

Fig. 2.11. Cross section of laser cut 1 mil deep in silicon film/oxide/polycrystalline-silicon structure.

After die separation the chips are handled in the conventional manner. They may be mounted on headers and bonded by any of the standard techniques. Electrical testing of the device then follows. It should be noted, however, that the electrically active portions of the die are isolated from the polycrystalline-silicon substrate so that the header is not automatically in electrical contact with the back of the film. If contact to the film is necessary, it must be made from the top of the die.

2.10 Summary

In this section each step in the process of obtaining a thin, high-quality silicon film on an insulator/polycrystalline-silicon support has been described. The major steps in the fabrication sequence include epitaxial growth of a thin silicon layer, oxidation, polycrystalline-silicon deposition, electrochemical etching, and vapor etching. The deposition of the polycrystalline silicon and the electrochemical etching are the critical steps in the overall fabrication process and will be discussed in more detail in the following section.

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3. FILM QUALITY AND DISCUSSION OF SUBSTRATE FABRICATION

3.1 Introduction

The basic steps in the fabrication process were described in Sec. 2. These steps were generally followed during the course of this study in order to fabricate wafers for investigation of the material properties of the films. However, several subsidiary experiments related to critical steps in the fabrication sequence were performed in order to gain an understanding of some of the processes and to optimize the total fabrication process.

The two most critical steps are the deposition of the polycrystalline-silicon film and the electrochemical removal of the initial n^+ starting wafer. Aspects of both these processes are discussed. In particular, the results of an investigation of the degradation occurring during the polycrystalline-silicon deposition are described in Sec. 3.2 while the electrochemical-etching procedure used in this study is compared to that of previous studies in Sec. 3.3.

Section 3.4 contains a description of the techniques used to evaluate the film quality so that the effect of process variables could be investigated; the influence of several of these variations is also discussed in Sec. 3.4. The following sections describe the effect of a different substrate crystal orientation, the thickness control possible, and the residual surface layer left after electrochemical etching. The final section indicates that the quality of the films fabricated is comparable to that required for reasonable yield of large-area, bipolar integrated circuitry.

3.2 Degradation Occurring During Polycrystalline-Silicon Deposition

3.2.1 Occurrence of degradation

Severe degradation, generally involving plastic deformation, has occasionally been observed during the deposition of the thick polycrystalline-silicon layers. This degradation is especially damaging in thicker layers and has been encountered whether the silicon was deposited from silane, dichlorosilane, or silicon tetrachloride. The deformation occurs <u>during</u> the deposition, while the entire system is at constant temperature, <u>not</u> during the cooling cycle. Therefore, the degradation

cannot be attributed to differences in the thermal coefficients of expansion between the various material in the sturcture and must be due to stresses built into the growing layer of polycrystalline silicon. When the degradation is seen, the wafer may become severely warped with a marked change in the structure of the polycrystalline silicon near the edge of the wafer.

Since the incidence of degradation is sporadic, it cannot be attributed to an intrinsic property of the materials system under investigation but is probably related to the presence of contaminant atoms in the gas stream in the reactor during the deposition. Evidence for this hypothesis can be cited:

1. When a cylinder of silane which was rejected for epitaxial deposition was used to deposit polycrystalline silicon,severe warping was encountered. This cylinder could not be used for epi because of its very low intrinsic resistivity, indicating the presence of unwanted impurity atoms in the silane. No significant deformation was encountered during polycrystalline-silicon depositions before or after the degraded deposition when good quality silane was used.

2. Severe warping has also been seen when the end-plate of the reaction chamber did not seat properly because of build-up of residue on the face of the plate. After the plate was cleaned so that air did not enter the reaction chamber, no degradation was observed. Therefore, some gaseous constituent of air can cause significant deformation; some other gases probably can also.

3. When a small piece of teflon tape prevented proper seating of a nitrogen value, severe warping was seen. In this case colored regions, probably related to the formation of some silicon nitride, as well as cracking of the wafers, were seen. The quantity of nitrogen entering the main hydrogen gas steam was unknown, but was probably quite significant since a test run with about 40 ppm nitrogen intentionally introduced into the hydrogen/dichlorosilane gas flow did not show any degradation.

4. Small amounts of deformation are often reduced by eliminating any small leaks in the reactor.

If we assume that the degradation is related to a gaseous contaminant entering the reaction chamber, further observations indicate that

the contaminant must interact with the structure of the polycrystalline silicon:

1. Even when slight deformation is observed during the deposition of thick polycrystalline silicon, good quality epitaxial films can be grown in the same reactor immediately following.

2. When severe deformation is observed during the deposition of thick polycrystalline silicon, the sense of warping is opposite for simultaneously deposited epitaxial layers. The polycrystalline film is concave upward while the epitaxial layer is convex upward, and the warping of epitaxial layer is generally less severe.

The sense of the warping in epitaxial films is reasonable since the inclusion of contaminant atoms in interstitial positions would lead to compressive stresses and convex curvature. The mechanism of deformation in the polycrystalline-silicon films must be significantly different and may involve the grain boundaries in the polycrystalline material. One possibility would be the inclusion of contaminant atoms at grain boundaries and the subsequent migration of these impurities out of the film, leaving voids which then collapse causing tensile stress.

Controlled experiments have indicated that the degradation is not related to the type of wafer used. No difference in the severity of degradation attributable to the type of wafer used was seen with heavily arsenic-doped wafers with both high and low-dislocation-densities or with lightly boron-doped wafers. The degradation is not related to the presence of the silicon dioxide layer beneath the depositing film since polycrystalline-silicon nucleated on a thin layer of low-temperature, silane polycrystalline-silicon deposited directly on single-crystal silicon shows similar amounts of deformation.

The effect of temperature is significant however. Appreciably less degradation is seen at higher deposition temperatures with the same magnitude of contamination. When only small amounts of degradation occur, the severity is strongly dependent on the location of the wafer on the susceptor. The first wafers, which are somewhat cooler than subsequent wafers, always exhibit the maximum amount of deformation. Similarly, larger-diameter wafers, whose edges extend over the pedestals

on the susceptor and are, consequently, cooler, are more susceptible to degradation. Since the increase in film quality with increasing deposition temperature has been seen in different reactors and with different silicon-containing gases, it is the most significant clue to the nature of the degradation mechanism. As the temperature increases, contaminant atoms absorbed on the surface of the growing film may desorb more readily, minimizing the incidence of plastic deformation. The observed temperature dependence is consistent with the strong effect of temperature on the influence of gaseous contaminants on epitaxial deposition found by Shepherd (1).

A related explanation may be developed from the arguments of Klokholm and Berry (2). They argue that tensile stress results from internal rearrangement of deposited atoms behind the growing surface of the film. The necessity for internal rearrangement may be related to the ease of surface diffusion of the depositing silicon atoms. A small quantity of adsorbed impurity atoms may severely impede the surface diffusion of deposited silicon atoms. The silicon atoms will then continue to rearrange after they have been covered by subsequently arriving atoms, resulting in the incorporation of a highly stressed layer in the depositing film. The bending moment will be proportional to the product of the stress and the film thickness and will become more significant in thicker films. When the bending force exceeds the yield strength of the single-crystal substrate at the deposition temperature, plastic deformation will occur. As the deposition temperature increases, the yield strength of the substrate will probably decrease, but this decrease must be less rapid than the decrease in the bending force. The bending force will decrease because of the increased desorption of the impurity atoms and the increased rate of surface diffusion at higher temperatures. The influence of the rate of deposition of the silicon layer will be more complicated. At lower rates, the surface silicon atoms will have a longer time to rearrange before being buried by subsequently arriving silicon atoms, but the ratio of impurity to silicon atoms may be higher so more may be adsorbed to inhibit surface diffusion.

3.2.2 Oxygen-induced degradation

In order to determine the type of impurity which could cause the degradation, experiments were conducted in which controlled amounts of either nitrogen or oxygen were added to the hydrogen/dichlorosilane gas stream. The addition of about 30 ppm of nitrogen (2.0 cc/min N_2 in the main flow of 67 l/min H_2 and 1.3 l/min SiH_2Cl_2) did not induce any degradation while the addition of about 12 ppm of oxygen caused some degradation in the polycrystalline films.

Further depositions in which 20 and 44 ppm of oxygen were added to the main gas stream showed moderate and severe degradation, respectively. Photomicrographs of the moderately and severely degraded polycrystalline films (2827F and 2830F, respectively) together with photomicrographs of the high-quality film (2831F) are shown in Figs. 3.1, 3.2 and 3.3. The position of the wafer on the susceptor was the same in each case. The successive pictures from each wafer show (a) the center of the wafer, and positions approximately, (b) 1/4 inch from the outer edge, (c) 1/8 inch from the outer edge, and (d) close to the outer edge. All micrographs were taken at 280X magnification with 1/10 second exposure; they were all taken within one hour so the variation due to changes in the photography is minimum.

The control wafer (2831F) shows a large-grained structure near the center of the wafer with a gradual decrease in grain size toward the edge of the wafer. This decrease is probably due to the outer edge of the wafer being cooler than the center because of the pedestal on which the wafer sits. The moderately degraded wafer (2827F) shows the same large-grained structure as the control wafer near the center of the wafer with a decrease in grain size toward the edge of the wafer. Immediately adjacent to the edge, however, a markedly different structure is seen. As the wafer deforms during the deposition, it lifts from the susceptor and becomes cooler. Therefore, the different structure may be related to a markedly lower temperature on this part of the wafer.

The severely degraded wafer (2830F) again shows the same large-grained structure near the center of the wafer, but the grain size diminishes rapidly toward the edge of the wafer. (Compare positions (d) of the control wafer and (b) of 2830F). Continued degradation is seen at

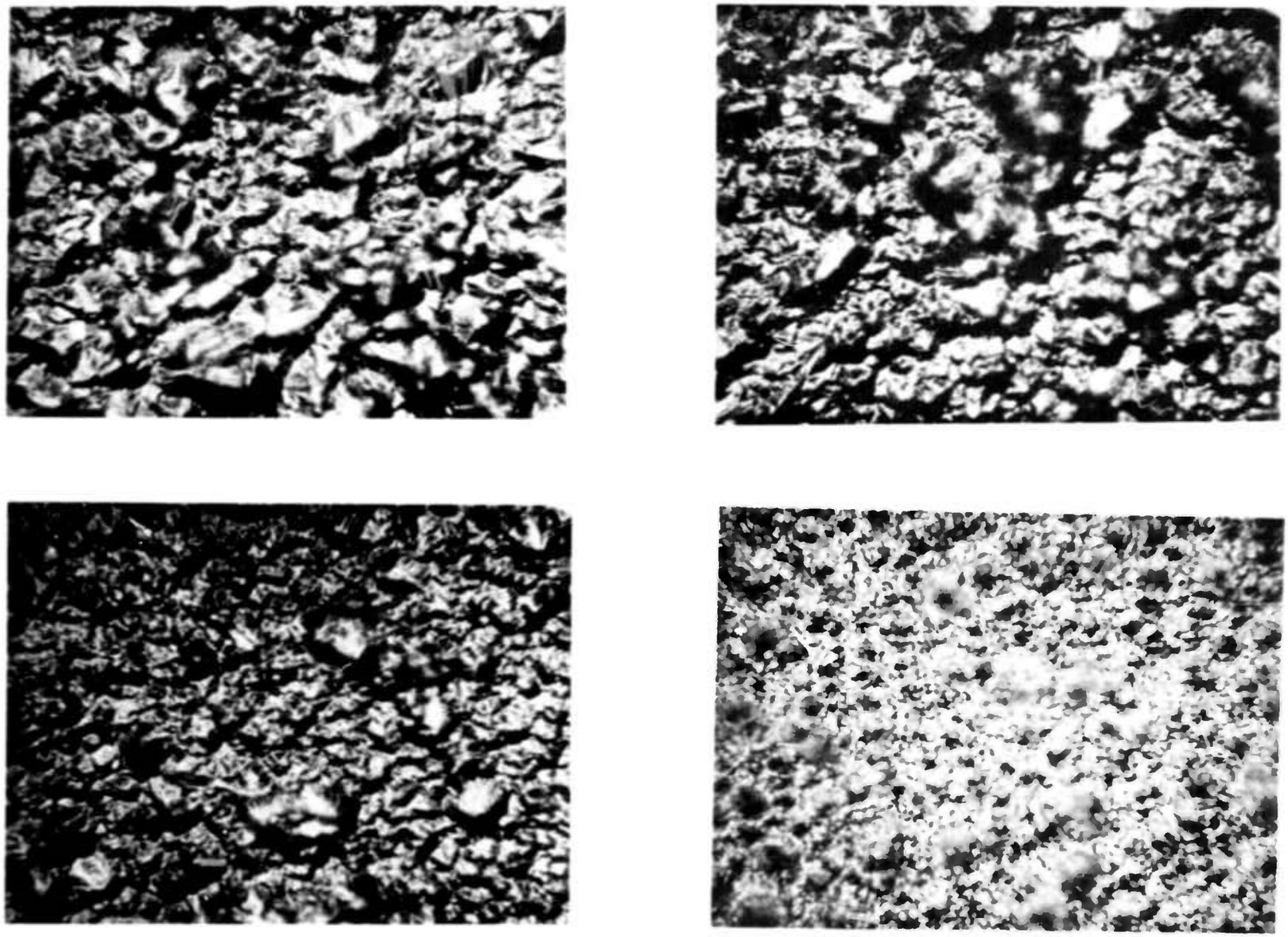

Fig. 3.1. Photomicrographs of moderately degraded polycrystalline-silicon film deposited with $[O_2]/[H_2]$ = 20 ppm; (a) center of wafer, (b) 1/4 inch from edge, (c) 1/8 inch from edge, (d) near edge (280X).

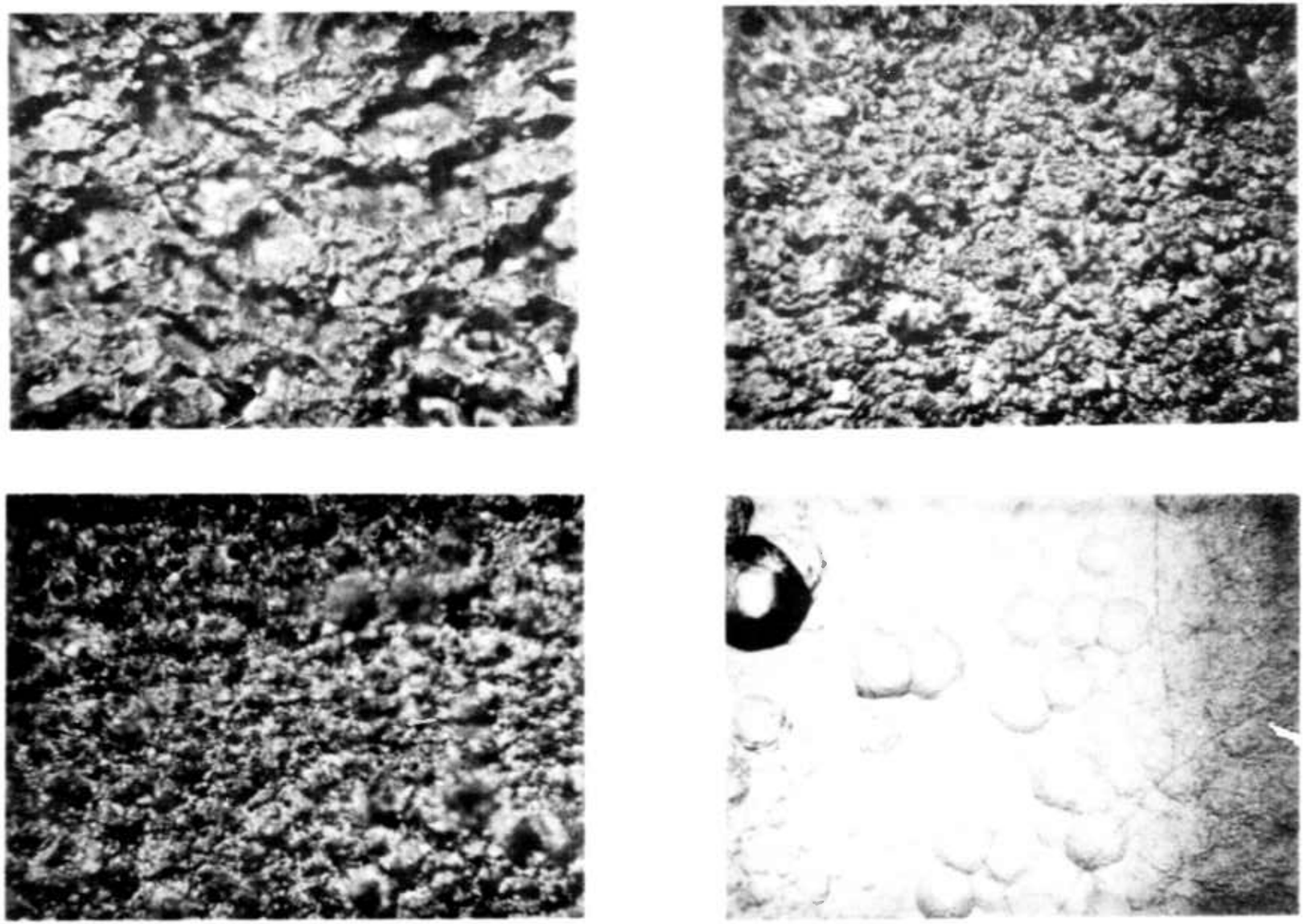

Fig. 3.2. Photomicrographs of severely degraded polycrystalline-silicon film deposited with $[O_2]/[H_2]$ = 44 ppm; (a) center of wafer, (b) 1/4 inch from edge, (c) 1/8 inch from edge, (d) near edge (280X).

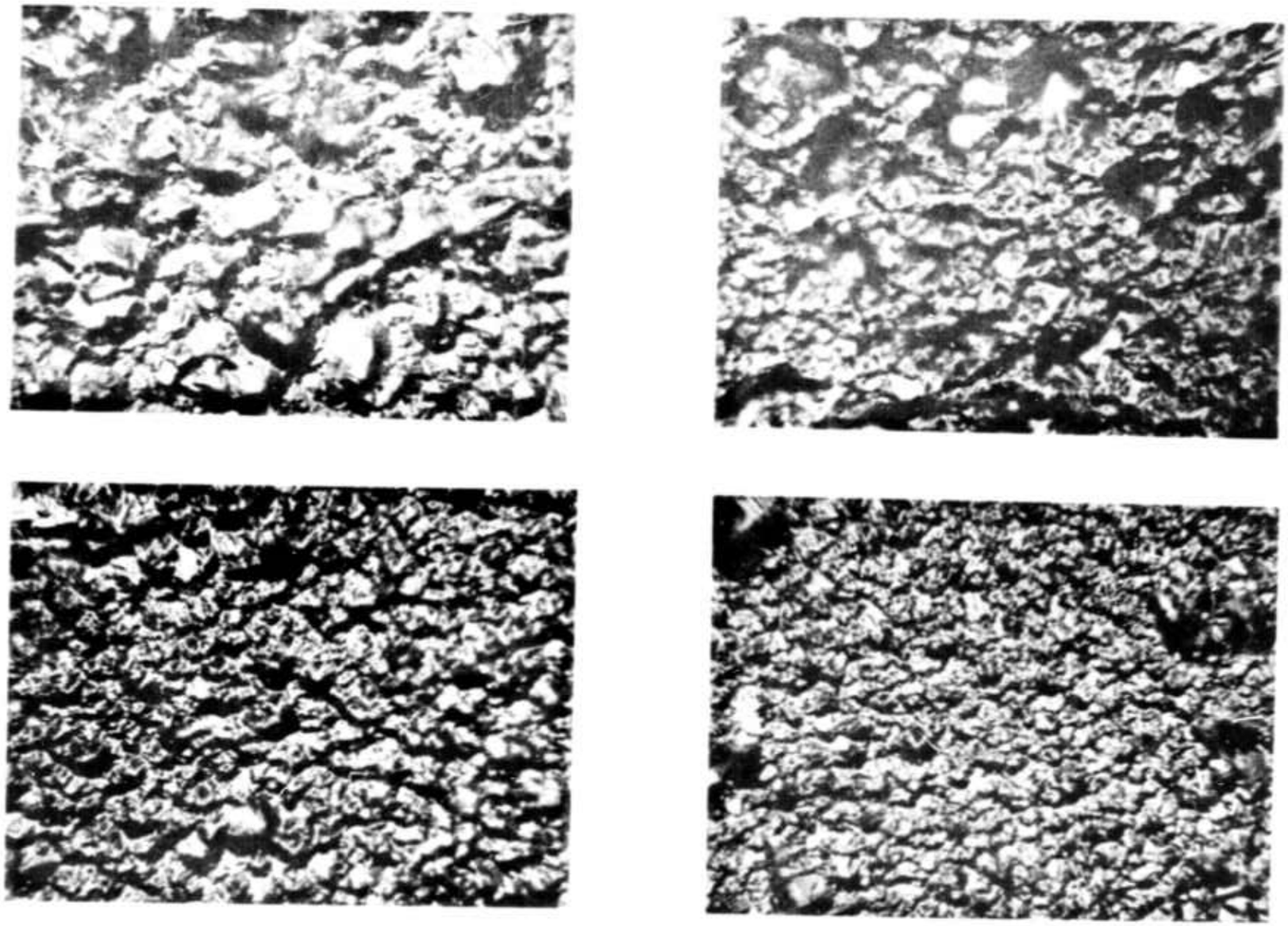

Fig. 3.3. Photomicrographs of high-quality polycrystalline-silicon film with no oxygen added during deposition; (a) center of wafer, (b) 1/4 inch from edge, (c) 1/8 inch from edge, (d) near edge (280X).

position (c) (compare to position (d) of 2827F). Near the edge of the wafer, the structure appears to change completely. The faceted structure disappears and is replaced by a mound-like structure. Cracks are also seen in the silicon, probably indicating the inclusion of appreciable quantities of oxygen into the structure. The film is also much thinner near the edge than at the center, probably because of the lower temperature near the edge.

In order to determine the relative importance of the deposition rate and the oxygen-to-silicon ratio in the deposition chamber, a further series of depositions was formed. The normal deposition rate of 4 μm/min was used for two depositions while the deposition rate was reduced by a factor of two for the other three depositions. The two control runs (3126 and 3131) produced films of good quality.

The same oxygen concentration (18 ppm) was used for runs 3127 and 3129 although the deposition rate was halved for the second run so that the oxygen-to-silicon ratio was doubled. The quality of the deposited films was markedly better for the first run, indicating that the oxygen-to-silicon ratio is more significant that is the oxygen partial pressure in the deposition chamber. The oxygen flow rate was halved in the next run so that a similar oxygen-to-silicon ratio was used in runs 3127 and 3130 although the deposition rate of run 3130 was only half that of run 3127. The film quality of the run deposited at the lower rate was noticeably better than that of the run deposited at the rapid rate. Although the deposited film was about 10% thinner in run 3130, the better film quality observed probably indicates that the deposition rate, as well as the oxygen-to-silicon ratio,is important in determining the film quality.

These results are consistent with the possible models proposed to explain the film degradation. As the oxygen-to-silicon ratio increases, more oxygen is included in the film,causing more significant degradation. As the deposition rate decreases, however, two mechanisms may be active to decrease the film degradation for a constant oxygen-to-silicon ratio. First, the adsorbed oxygen atoms will be near the surface of the film for a longer period of time before they are buried by subsequently arriving atoms,and they will have a greater probability of desorbing from

the film. A second argument is probably much more significant in the present case. We have assumed that the tensile stress in the film results from the internal rearrangement of deposited atoms behind the growing surface of the film (2). The need for this internal rearrangement occurs since surface diffusion of the depositing silicon atoms which normally leads to rearrangement is severely impeded by the adsorbed oxygen atoms. As the deposition rate decreases, a longer time is available for the surface silicon atoms to migrate along the surface and reach a stable position even though the same number of oxygen atoms are present on the surface. Consequently, less rearrangement will have to occur after the silicon atoms are buried by subsequently arriving atoms. Less stress will arise, and less plastic deformation will occur.

3.2.3 Neutron activation analysis

In order to determine if oxygen is actually included in thick polycrystalline-silicon films when they are degraded during the deposition, several wafers were subjected to neutron activation analysis*. Wafers from depositions to which oxygen was purposely introduced into the gas stream were sent along with control wafers. Four wafers from each of runs 2827, 2830 and 2831 (shown in Fig. 3.1, 3.2 and 3.3) were prepared by etching off the single-crystal substrate and the intermediate oxide layer. The four samples from each run were than combined in one vial so that a total sample mass of approximately 3 g was available for each analysis. The most severely degraded samples weighed less than the others since the deposited films were much thinner near the edges of these wafers. This analysis indicated the presence of approximately 100 ppm oxygen in the control sample, 140 ppm in the lightly contaminated sample, and 370 ppm in the heavily contaminated sample. These values show that oxygen is included into the structure of the degraded polycrystalline-silicon films during the deposition.

Although the oxygen concentration increased monotonically with increasing degradation, the increase does not appear to be linear.

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* Analysis performed by Gulf Radiation Technology (San Diego, CA.).

Possibly, some of this discrepancy is due to the experimental errors introduced in the sample preparation and the flowmeter calibration. However, the amount of degradation does not appear to be a linear function of the oxygen addition either, indicating that the degradation process accelerates once it starts. Once the edges of the wafers start lifting from the susceptor and cooling, increasing quantities of oxygen are probably included into the film. The probable presence of approximately 100 ppm oxygen in the control sample, to which no oxygen was intentionally introduced, is especially disturbing. Although some of this oxygen may have been introduced when the sample was prepared for analysis, a significant fraction may have been included in the film, indicating that potentially detrimental quantities of oxygen may be present in the reactor under the best conditions.

In these experiments the deleterious effect of a small concentration of oxygen in the reaction chamber was demonstrated. Consequently, the importance of eliminating small quantities of oxygen entering the system from leaks or contaminated gases is apparent.

3.3 Characteristics of Electrochemical-Etching Process

3.3.1 Etching of n^+ silicon

In order to gain some insight into the electrochemical-etching process and to compare the etching behavior observed in the present case with results of other investigations (3,4,5,6), some brief studies were conducted with bare (111)-oriented, 0.002 Ω-cm, n-type substrates. The potential across the silicon/electrolyte interface was first determined as a function of the applied voltage. The applied voltage can be divided into three primary components: the voltage drop in the electrolyte, the potential across the silicon/electrolyte interface, and the IR voltage drop in the silicon wafer. Since a low-resistivity wafer with an initial thickness of 260 μm was used in these experiments, the IR drop in the wafer was probably only a few tenths of a volt in the worst case and will be neglected. The remaining two components were separated by varying the spacing between the wafer and the cathode with the wafer held vertically and assuming a linear relationship of the form

$$V_{appl} = V_\ell + V_i = J(\rho_\ell d + R_b), \qquad [3.1]$$

where d is the spacing, ρ_ℓ is the resistivity of the electrolyte, and R_b (Ω-cm ^{2}) is an equivalent contact resistance at the silicon/electrolyte interface. The current was measured for spacings of 1, 2, 3, 4 and 5 inches and applied voltages of 7, 9 and 12 V. The electrolyte was agitated during these tests. Reasonable agreement with a linear relationship was found with ρ_ℓ = 1.6 Ω-cm and R_b = 50 Ω-cm^2. Some deviation was observed at higher voltages and smaller spacings where the IR drop in the wafer would be expected to be important. Figure 3.4 shows the measured current density as a function of the calculated value of the interface potential $V_i = V_{appl} - J\rho_\ell d$, indicating a linear relationship over most of the range tested. In order to compare these results with published results, similar measurements were taken without agitation. Figure 3.5 (a) shows the current density measured as a function of the applied voltage for spacings of 2, 3 and 5 inches. When the voltage drop in the electrolyte is subtracted so that the current density is plotted as a function of the interface potential, the three curves become superposed as shown in Fig. 3.5 (b). When these curves are compared to Fig. 4 of Ref. 3, good agreement is found, with the relative maximum occurring at about the same value of current density. From this agreement we may conclude that the present apparatus functions similarly to that employed in other investigations when no agitation is used. However, different mechanisms appear to be important with and without agitation at an interface potential of approximately 7 V (6).

In order to gain some understanding of the etch-mechanism involved, the valence of the dissolving silicon was determined by considering the integral of the current-vs.-time curve as a wafer was etched under the normal conditions (with agitation). Approximately 7600 Coulombs of charge was supplied to the cell during the etch (after subtracting the leakage current), corresponding to 4.8 X 10^{22} electrons. The wafer being etched contained roughly 2.6 X 10^{22} atoms, so we may conclude that the silicon dissolves in divalent form, rather than in tetravalent form under these etch conditions (6).

3.3.2 Etching of p-type silicon

In order to determine the behavior of p-type silicon in the

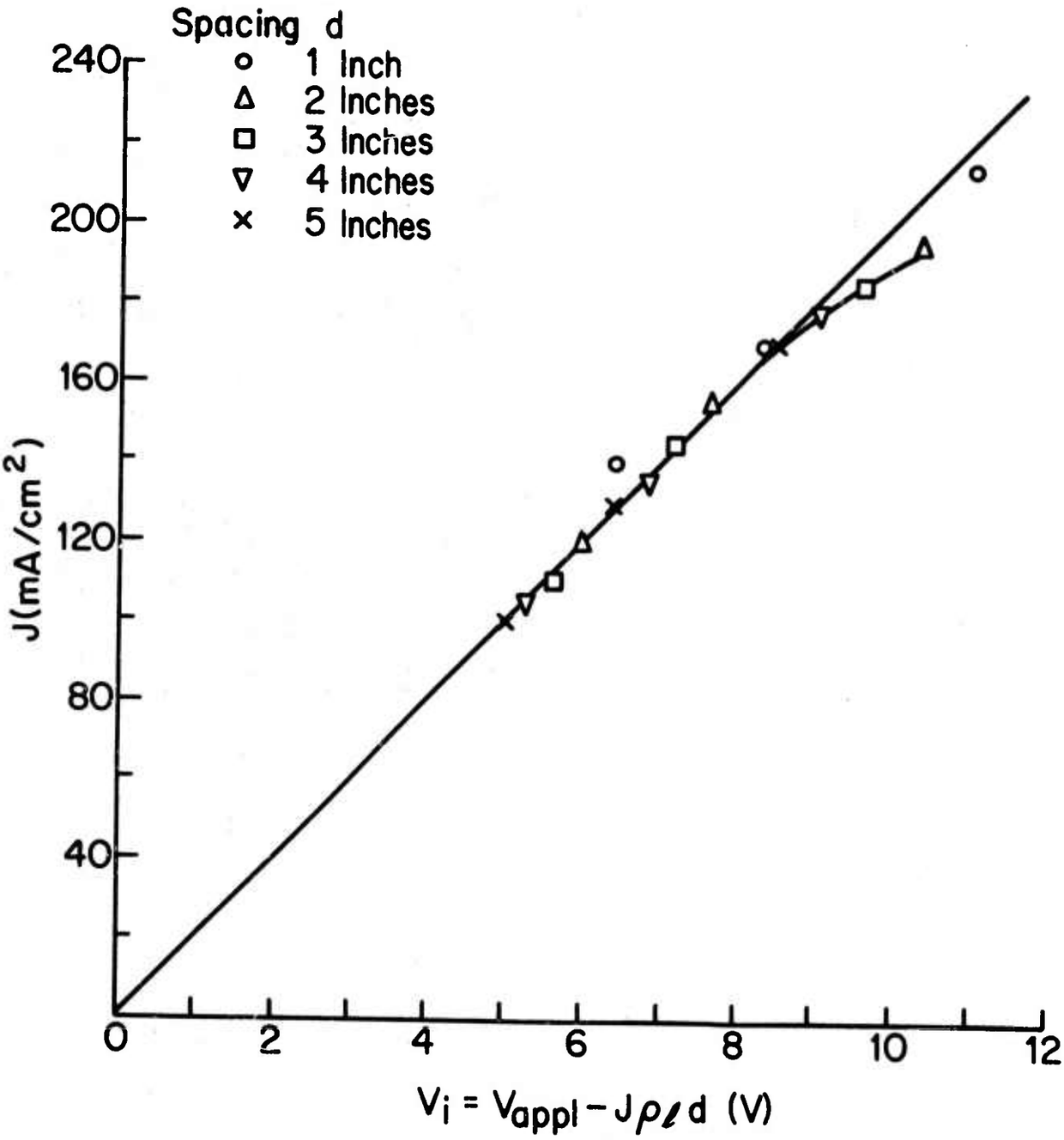
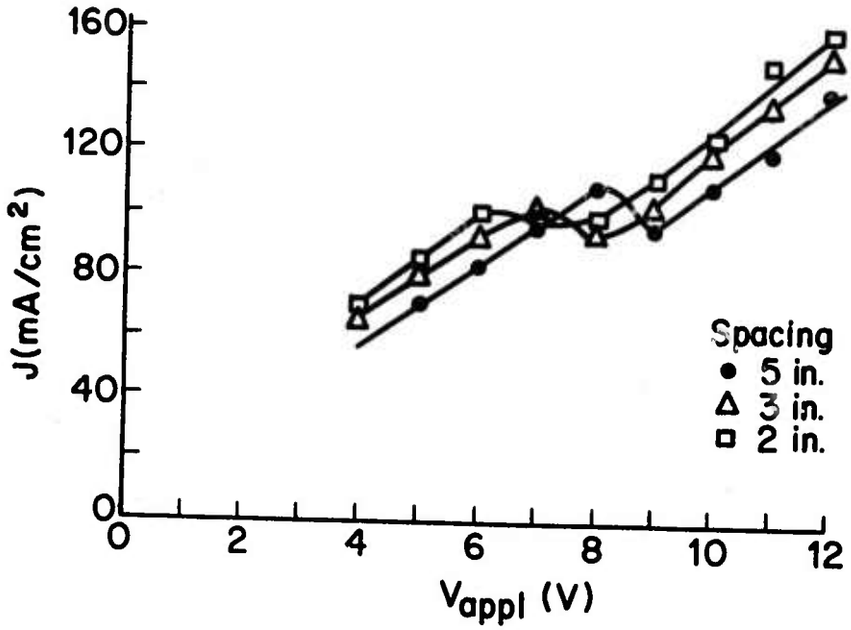
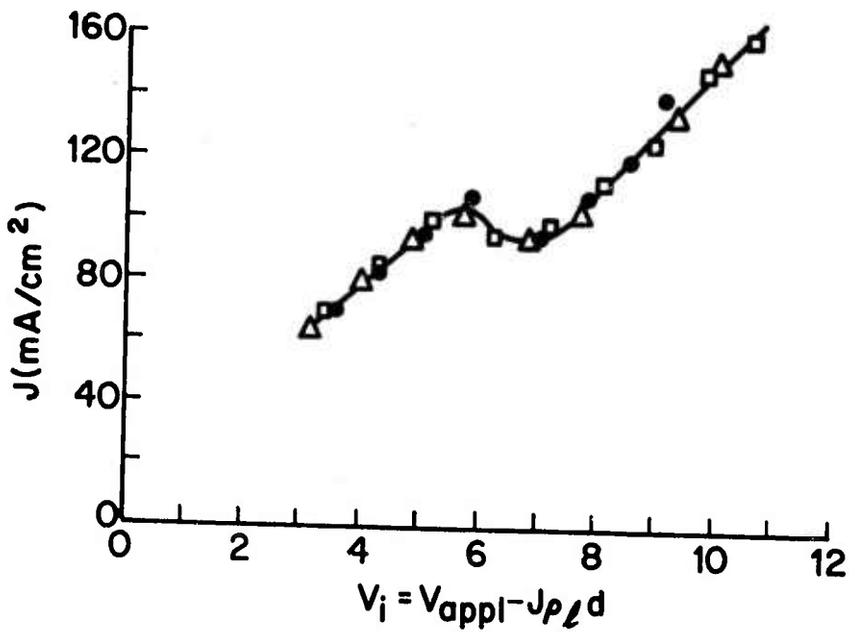


Fig. 3.4. Current density as a function of interface potential (with agitation).



(a)

Fig. 3.5 (a). Current density as a function of applied voltage (without agitation).



(b)

Fig. 3.5 (b). Current density as a function of interface potential (without agitation).

electrochemical-etch bath, samples of various resistivities were prepared. The resistivities of these p-type wafers varied from 0.0023 Ω-cm to 110 Ω-cm. Most of the face of each wafer was protected with a vapor-deposited oxide, and a small region (1/8 - 1/4 inch) near the flat was doped with a 1020°C BBr_3 predeposition so that good contact could be made to the wafer. The oxide was stripped,and the back of the wafer was covered with aluminum and alloyed to ensure that series resistance within the wafer did not affect the results.

The wafer was secured in the clip and immersed in the electrochemical-etch bath so that the electrolyte did not come into contact with the platinum clip. The current was observed at a constant voltage of 10 V after the wafer had been immersed for three minutes, and the wafer was examined for indications of stain formation. In all cases the current was found to be approximately 100 ma/cm^2 when the platinum clip contacted the boron diffused region of the wafer. No stain was formed on the wafer at this high current density. Several wafers were immersed for five minutes without agitation with the same results.

On the lightly doped wafers, a low current (of the order of 1-10 ma/cm^2) was observed if the platinum clip contacted the lightly doped wafer itself rather than the heavily doped, diffused region. In these cases, a stain film was formed, and the surface usually became rough. The stain film could be removed by moving the clip back to the diffused region so that a higher current again flowed, but the rough surface was not easily evened out. In one case, a thin stain film formed and could not be dissolved in HF (5 min) and only slowly in aqua regia (10 min). In other cases thicker,yellow stain films formed.

These results are in agreement with statements in the literature which report that p-type silicon etches in the electrochemical-etch bath regardless of its resistivity (7). They also indicate the importance of making good contact to the wafer so that the necessary current may flow to allow the wafer to etch and to prevent stain formation.

3.4 Process-Related Effects On Film Quality

3.4.1 Introduction

During the course of this study, the effects of various changes in the fabrication conditions on the quality of the thin silicon films were investigated. The thickness, type, and resistivity of the epitaxial film, the quality of the starting wafer, and the effect of defects induced during the polycrystalline-silicon deposition, were among the parameters investigated.

3.4.2 Defect formation and evaluation of film quality

Two primary methods were used to evaluate the quality of the films. Defects in the films after electrochemical etching were directly observed in the dark-field microscope, and the characteristics of shallow bipolar transistors fabricated in the films were examined.

During this investigation it was found that the major type of defects in the thin films appeared to be channels in the silicon formed during the electrochemical etching (8, 9). These channels probably occur at locations with high hole generation rates as discussed by Meek (10). In very thin films of the order of 1 or 2 μm thick, these channels can easily extend completely through the thin film and intersect the underlying oxide. If the channel is large enough,the HF electrolyte can then start attacking the oxide laterally, thus widening the defect.

The most direct method of examining the defect was to observe the film after electrochemical etching under the dark-field microscope. Light can easily penetrate the very thin film and be reflected back into the microscope. If the defect extends under the silicon film due to etching of the underlying oxide, its size can easily be large enough to be revealed in an optical microscope although the actual channel in the silicon may be too small to observe optically. In very defective films in which the channeling was severe, the channel, as well as the surrounding region from which the oxide was removed, was clearly seen (Fig. 3.6) although generally only the different appearance due to the oxide removal was readily apparent. More detailed investigation of the defects was performed by Sirtl etching defective films and observing the widening of the channels in the silicon film with continued etching. SEM observation of these defects was also consistent with the interpretation presented above.

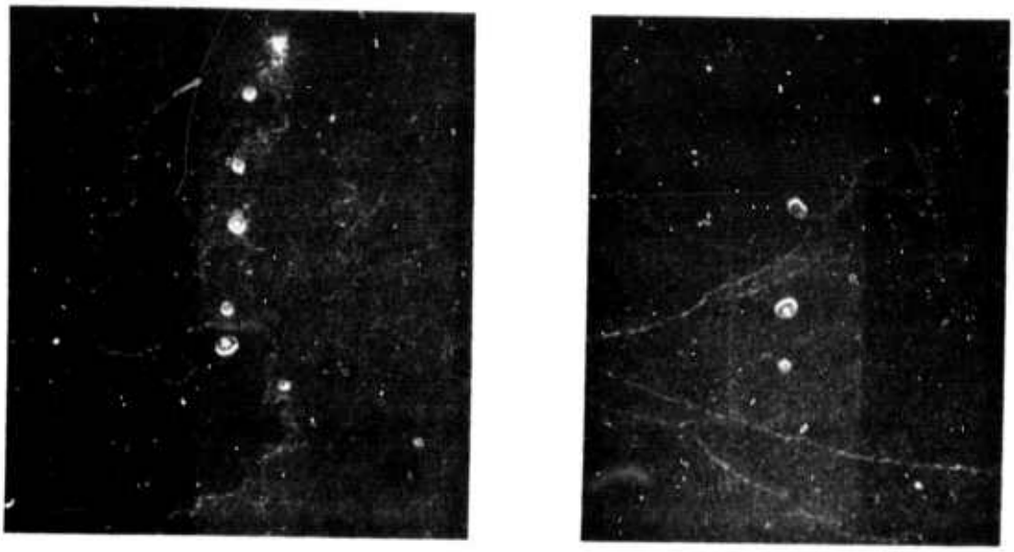


Fig. 3.6. Dark-field photomicrographs showing defects with central channels surrounded by larger defective areas on severely degraded wafer (560X).

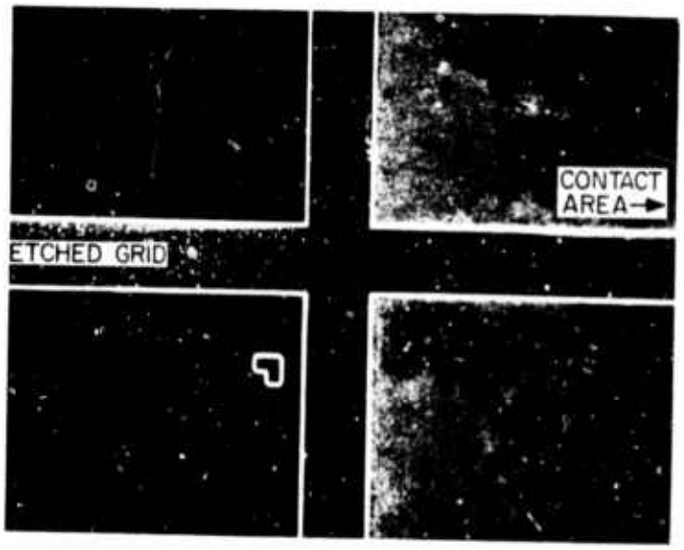


Fig. 3.7. Dark-field micrograph of wafer with etched grid showing higher film quality on portion of silicon island which was etched last (71X).

Further investigation of the defects and their effect on device behavior was determined by fabricating large-area bipolar transistors in the thin films and observing the emitter-to-collector leakage current. Good correlation has been found between the incidence of leakage current and the presence of defects observed under the dark-field microscope after electrochemical etching. Therefore, observation of the defects under the microscope provides a rapid and meaningful means of evaluating the quality of the films formed by electrochemical etching.

3.4.3 Epitaxial film variations

In order to determine the optimum characteristics of the initial epitaxial film, the influence of the type and resistivity on the quality of the electrochemically etched film was examined. The effect of the dopant conductivity type was investigated first. Both p-type and n-type films about 2 μm thick with similar resistivity were deposited on the standard n^+ substrates and then processed in the normal manner. The films were examined after electrochemical etching, and it was found that the quality of the p-type films was consistently higher than that of the n-type films. Extensive channeling was frequently observed in the n-type films under the dark-field microscope. The incidence of channeling was markedly less in p-type films. These results are consistent with those reported by others (4). Therefore, for applications in which the conductivity type of the film is not important, p-type films should be used. In the case of bipolar circuitry, in which the film is subjected to a heavy,n-type predeposition and then covered with another epitaxial layer of silicon, the film formed by electrochemical etching may be of either conductivity type, and the use of p-type films has been found to improve the device yield markedly.

The effect of the dopant concentration in p-type films was also investigated. One series of films was fabricated with a dopant concentration of about 3×10^{15} cm^{-3} while no dopant was intentionally introduced into another series. The undoped films averaged approximately 5% thicker than the doped films. The wafers were oxidized, and a thick layer of polycrystalline silicon was deposited. The locations of the doped and undoped films during the polycrystalline-silicon deposition were selected to preclude variations in the quality of the polycrystalline

film from influencing the results. After the wafers were prepared for electrochemical etching, they were etched two at a time with the position of the doped and undoped films interchanged in successive batches to eliminate the effect of location in the electrochemical-etch bath on the quality of the film. After the wafers were etched, they were examined both macroscopically and microscopically under the dark-field microscope. Little variation in quality was found, with the thicker films generally being of better quality than the thinner ones.

As indicated above, the thickness of the film was more critical in determining the film quality than was the dopant concentration in the initial epitaxial film. Epitaxial films which indicated a thickness less than about 1.8 - 1.9 μm by the infrared reflectance technique discussed in Sec. 2.3 generally were found to be highly defective after electrochemical etching. Consequently, a lower limit of 2.0 μm was arbitrarily set on the acceptable epitaxial film thickness. An epitaxial layer of this thickness will produce a silicon film about 1.5 μm thick after electrochemical etching. This 0.5 μm difference was reasonably reproducible and is in good agreement with the loss expected from interdiffusion at the epi/substrate interface if it is assumed that the electrochemical etching stops at a concentration of 2×10^{16} as suggested in Ref. (4). This interdiffusion occurs primarily during the deposition of the polycrystalline-silicon film (Fig. 2.5). The uncertainty in the meaning of the measurement of the initial epitaxial film may also contribute significantly to the 0.5 μm difference.

In most cases the initial epitaxial film was deposited by the pyrolysis of silane. In one case, however, dichlorosilane was used in order to investigate its suitability for use in this process. Five ohm-cm, p-type epitaxial films about 2 μm thick were deposited on the standard substrates at a rate of 0.75 μm/min. Similar epitaxial films were deposited from silane for comparison purposes. The silane epitaxial films were 2-3% thinner than the dichlorosilane films on the average. After the films were oxidized, the polycrystalline silicon was deposited with the wafers suitably located to eliminate the influence of possible wafer-to-wafer variations in the quality of the

polycrystalline silicon. The wafers were electrochemically etched in pairs with the position of successive sets of wafers interchanged. When the wafers were examined, no apparent difference in the quality of the silane and dichlorosilane wafers could be found. The only general trend observed was the better quality of the thicker films. From this experiment it is concluded that dichlorosilane should be suitable for the deposition of the initial epitaxial layer. Silane epitaxial films were used in all the remaining experiments discussed in this section.

3.4.4 Process-induced dislocations

The effect of dislocations in the starting material has already been discussed in Sec. 2.2, where it was indicated that dislocations in the initial substrate lead to the characteristic defect which can be observed under the microscope and which causes device failure. However, substantial numbers of defects can also be generated by process-induced defects occurring at various steps in the fabrication sequence before electrochemical etching. The most serious degradation can occur during the deposition of the thick layer of polycrystalline silicon. As has been discussed in Secs. 2.5 and 3.2, serious plastic deformation can occur during this deposition. The deformation causes large numbers of dislocations to be generated in the single-crystal wafer and leads to the formation of etch channels during the electrochemical etching. Whenever severe plastic deformation was observed after polycrystalline-silicon deposition, large numbers of defects were observed after electrochemical etching, and a high incidence of emitter-to-collector leakage was found after transistor fabrication. For this reason the deposition of high-quality films of polycrystalline silicon is essential to the successful fabrication of the thin silicon films. In addition, severe warping of the wafer will cause difficulty in alignment of the photomasks during successive photomasking operations. Since the substrate is fairly flexible, however, some warping can be tolerated.

A recent report (11) indicates that dislocations can be generated during the steam oxidation of a (100)-oriented wafer unless a thin layer of oxide is first grown in dry O_2. Therefore, an initial dry O_2 cycle was included in the oxidation of the initial epitaxial

films to prevent the possible introduction of dislocations during this step.

3.4.5 Process variations

In an attempt to reduce the pitting occurring during electrochemical etching, several variations in the processing sequence were attempted. One variation will be discussed here. Since the defect density appeared to increase as the wafer was immersed in the electrochemical-etch bath for longer times, it was felt that the defect density could be reduced by electrically isolating portions of the film shortly after they were completely etched. In order to test this hypothesis, epitaxial films were oxidized and then covered with an additional layer of vapor-deposited oxide. The oxides were removed from a square grid of lines with spacings of either 40 or 75 mils, corresponding to the scribe-line spacing of various devices. A heavy phosphorus diffusion was added to the exposed silicon lines, and then the wafer was covered with more vapor-deposited oxide before the polycrystalline silicon was deposited. During the electrochemical etching, the heavily doped regions of the thin film, as well as the n^+ substrate, were removed, leaving squares of thin silicon corresponding to the size of an individual die on the underlying insulator.

Wafers fabricated in this manner were examined under the dark-field microscope. It was found that n-type films exhibited a much lower defect density in the portion of an individual island from which the substrate was etched last; i.e., the area nearest the electrical contact to the wafer (Fig. 3.7). Higher defect densities were observed in the portion of the island which was exposed first. On the other hand, p-type films, which are generally of better quality than n-type films, did not show a marked variation across an individual island. Bipolar transistors were also fabricated in thin films formed by this process, with 9 transistors in each 75 mil square island. The n-type films showed markedly better yield in the portion of the island closest to the electrical contact while no significant variation was observed in the p-type films. From these results we may conclude that the quality of n-type films may be substantially improved by the addition of heavily doped grids after the epitaxial film is formed while the improvement in p-type films is only marginal.

In addition, since the defect density was not suppressed over the entire area of an island on n-type films, the defects must be generated within a few minutes of the removal of the substrate from a region. Few further defects will probably form after the highly conducting n^+ substrate is several tenths of an inch away even if no grid is used. Defects initially present, however, may become enlarged with continued immersion in the etch bath due to attack of the underlying SiO_2 through a small etch channel.

In another experiment an attempt was made to add a heavily doped subcollector region to the structure before electrochemical etching in order to avoid the deposition of a second epitaxial layer after the film was electrochemically etched. An n^+ antimony predeposition was added after an initial n-type epitaxial film was grown but before the polycrystalline-silicon layer was deposited. The n-type impurities were added either over the entire wafer or restricted to the die areas by a masking oxide. In either case, a large number of etch channels penetrated the lightly doped epitaxial film during the electrochemical etch. The defect density increased with decreasing thickness of the epitaxial film and produced films of unacceptable quality if the thickness was less than about 8 μm. Since very thin films could not be achieved, this method of adding a buried subcollector to the structure was not investigated further.

3.5 (100)-Oriented Films

Although most of the films fabricated during this study had (111)-orientation, a limited number of (100)-films were investigated. During processing these films generally behaved similarly to the (111)-films with several minor exceptions. During electrochemical etching, the number of defects formed over most of the wafer was similar or perhaps somewhat lower than that formed in (111)-films; however, the degradation near the wafer periphery was markedly greater for the (100)-material. The cause of this difference is not known.

The electrochemical-etch conditions had been optimized for (111)-oriented material before any (100)-films were etched, and it was found that the latter required a slightly lower current density for compensation

at the fixed angle. Consequently, heating of the electrolyte during the etching was especially detrimental for this orientation material, and the temperature was generally kept several degrees lower for (100)-material than for (111)-material. A more significant difference was the preferential attack of defects in the (100)-films during vapor etching already discussed in Sec. 2.8. No other significant variations were observed between the two orientations of silicon although only limited experience with the (100)-films is available.

3.6 Thickness Variations

The thicknesses of many wafers were measured at various stages in the fabrication process, and it was generally found that the thickness variation between wafers or within a wafer could be attributed to nonuniformities in the deposition of the epitaxial film or nonuniform interdiffusion at the epi/substrate interface rather than nonuniformities in the electrochemical etching. The wafer-to-wafer nonuniformity of the initial epitaxial film should be less than ± 5% for a properly profiled epitaxial reactor. For a film nominally 2 μm thick, the thickness should vary from 1.9 to 2.1 μm at most. Variations of this magnitude or less were generally observed except when the reactor configuration had been changed to accommodate other experiments. The variation within a wafer should be of the same magnitude. In some cases, however, the side of one row of wafers nearest the edge of the susceptor was found to be somewhat thin. This difference is attributed to the nature of the gas flow in the reactor, especially when the susceptor was not centered within the cross section of the quartz reaction chamber.

During deposition of the polycrystalline-silicon layer, significant outdiffusion may occur. If the wafer temperature during this deposition increases significantly above the nominal temperature of 1100°C, appreciably more interdiffusion may occur, and the film thickness after electrochemical etching will be less than the nominal value. Although the reactor may be accurately profiled (entire susceptor within ± 5°C) temperature variations may occur during a deposition. If the cooling of the walls of the reaction chamber is inadequate, appreciable amounts

of silicon may be deposited on the quartz above the wafers. As the quartz is coated, more heat is reflected back onto the wafer surface and its temperature increases, causing excessive interdiffusion and, consequently, a thinner final film. If the polycrystalline-silicon deposition was well controlled, however, the difference in thickness between the initial epitaxial film and the final electrochemically etched film was generally within ± 0.1 μm of the nominal change. For example, the initial thickness of a series of films from two epitaxial depositions with nominal film thickness of 2.1 μm varied from 2.02 to 2.19 μm with less variation within each run. After electrochemical etching the thickness varied from 1.37 to 1.62 μm or ± 9% from the nominal thickness of 1.5 μm. Better thickness control should be possible if large numbers of wafers are processed so that the equipment can continually be optimized.

3.7 Residual Surface Layer

When p-type films are formed by electrochemical etching, a residual n-type layer is usually left on the surface since the etching terminates at an n-type dopant concentration of about 2×10^{16} (4). This n-type layer is expected to be wider in cases where more interdiffusion has occurred at the epi/substrate interface.

In order to investigate this behavior further, measurements were taken on a sample initially about 8 μm thick. After the electrochemical etch, an n-type layer about 1.4 μm thick was observed by grooving and staining. The sample tested n-type with a hot-point probe and indicated a V/I of about 2500 Ω with a four-point probe at a current of 0.1 mA. Portions of the wafer were subjected to vapor etching for 1, 2, 3 and 4 minutes (~0.55 μm/min). After grooving and staining, the first two samples still indicated n-type surface layers while the last two did not. These results were consistent with hot-point probe measurements. Presumably this unstained region corresponded to the n-type layer plus a portion of the depletion region, which should have been about 1 μm thick, so that the actual n-type region was less than about 1 μm thick. Although this value is slightly greater than expected,it is not unreasonable if the etching stops at a donor concentration of about 2×10^{16} cm^{-3} and interdiffusion is considered.

3.8 Shallow Bipolar Transistors

In order to evaluate the quality of the electrochemically etched films for use in bipolar integrated circuits, shallow bipolar transistors were fabricated in many films (12). After the film was electrochemically etched and vapor etched, it was subjected to an antimony predeposition cycle at 1250°C. This heavily doped film served as the buried subcollector in the transistor structure and reduced the collector series resistance. When the buried subcollector was not used, the collector-base depletion region could extend to the bottom of the film. In this case the gain was sharply reduced as the effective area of the device decreased to the peripheral area only. After the n^+ predeposition, an n-type epitaxial layer of about 0.5 Ω-cm resistivity was grown on the thin film. This layer was generally about 1.4 μm thick while the initial film was about 0.6 μm thick after vapor etching so that the total structure was about 2.0 μm thick. In some cases the Isoplanar process was applied to this structure in order to provide lateral isolation between devices. When only an evaluation of the film quality was desired, the outdiffusion of the buried layer during the Isoplanar oxidation was simulated, but the entire Isoplanar process was not used in order to reduce the processing time and obtain more rapid feedback for further process optimization. Diffusion of the shallow base and emitter regions followed, and the transistors were then metallized and alloyed.

In order to examine as much of the area of the film as possible, large-area bipolar transistors were used. Each transistor had an emitter area of 4.5 mil^2. The center-to-center spacing was 25 mils so that 9 transistors were located on a 75 mil X 75 mil area, roughly the size of typical MSI circuits currently in production. The total emitter area of 9 transistors was 43 mil^2, about twice the total emitter area of a typical MSI circuit. Thus, examination of these transistors provided a realistic indication of the quality of the film and its applicability to MSI bipolar circuitry.

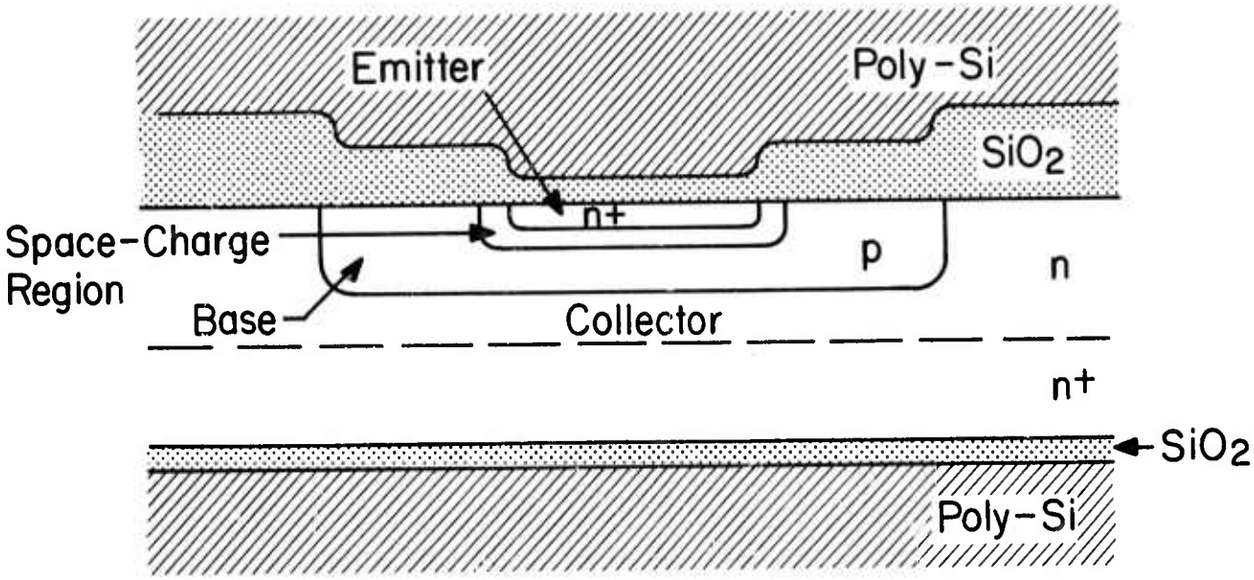
Since a defect in the electrochemically etched film and in the subsequently grown epitaxial film will lead to a region in which impurities will rapidly diffuse, the dominant failure mode of the transistors was expected to be emitter-to-collector leakage (I_{CEO}). This leakage

was expected wherever a defect passed through the active emitter area so that the n-type emitter impurities could diffuse rapidly through the p-type base and approach the n-type collector. This failure mode is especially important in the narrow-base transistors used in this evaluation. A cross section of the transistor is shown in Fig. 3.8. The cross section was obtained by a method partially developed during this investigation (13). The active base region is seen to be about 0.5 μm thick.

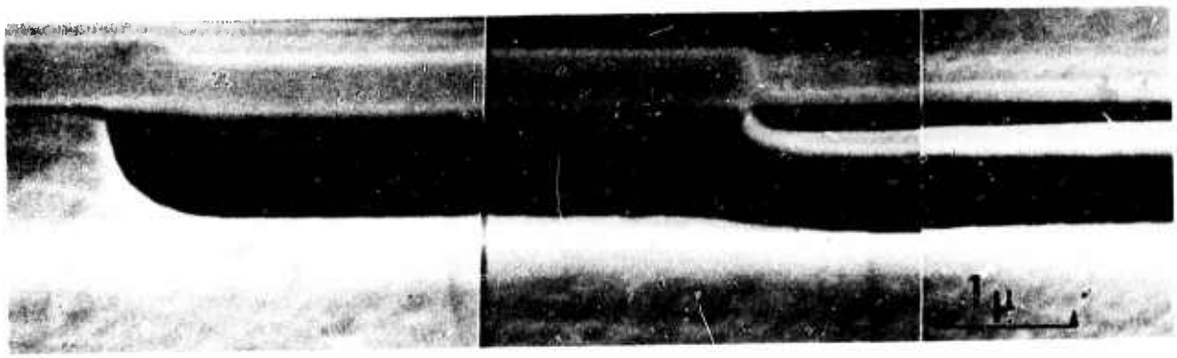
The transistors were tested on a curve tracer. A 4.5 mil^2-emitter device was considered to be acceptable if the collector characteristics appeared normal on the curve tracer and the leakage (I_{CEO}) was less than 1 μA at a collector-to-emitter voltage of 5 V. Yield maps were plotted to indicate the variation of the film quality across the wafer. The quality of the films was highly variable with a good wafer showing 88 percent yield over a 0.8 X 0.9 inch area and lower yield in the regions near the periphery which were etched first. Devices fabricated in bulk control wafers showed characteristics similar to those in the thin-film wafers, indicating that no basic anomalies are occurring in the thin films. The results obtained from the yield studies indicate that, with some further expected improvement in the film quality, reasonable yields of MSI circuitry can be obtained with this type of structure.

3.9 Summary

In this section the quality of the film which is obtained by electrochemical etching and the critical steps of the fabrication process have been discussed. In particular, the importance of eliminating trace quantities of oxygen during the deposition of the polycrystalline-silicon film was emphasized. The methods of evaluating the film quality were described along with the effects of several variations in the epitaxial deposition and the other processing steps. The effect of a different substrate crystal orientation, the thickness control possible, and the residual surface layer left after electrochemical etching were then discussed. Finally, the yield of shallow bipolar transistors fabricated in the thin films indicated that the film quality is comparable to that required for reasonable yield of large-area, bipolar integrated circuitry.



(a)



(b)

Fig. 3.8. Cross section of high-frequency npn transistor formed in thin film of single-crystal silicon; (a) representation of device structure; (b) composite SEM micrograph of left half section of transistor.

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4. MAJORITY-CARRIER MOBILITY

4.1 Introduction

Throughout this investigation of the properties of thin silicon films, emphasis has been placed on comparing their properties with those of bulk silicon wafers and identifying any differences which would appreciably affect device behavior. Since the characteristics of most semiconductor devices are significantly influenced by the majority-carrier mobility, Hall-mobility experiments were conducted. Both n and p-type films of several thicknesses were investigated. A dopant concentration of about 10^{15} cm^{-3} was generally selected since this concentration is typical of that in wafers used for many semiconductor devices and is compatible with the electrochemical-etching process.

4.2 Experimental Method

4.2.1 Sample preparation

The thin-film wafers were fabricated by the process described in Sec. 2. First, a lightly doped epitaxial film of the appropriate conductivity type was grown on a heavily doped, (111)-oriented, n-type wafer using silane epitaxy. Either diborane or phosphine was used as the dopant source. The wafer was then oxidized at 920°C primarily in a steam ambient in order to grow an oxide about 0.25 - 0.30 μm thick. Polycrystalline silicon was deposited from dichlorosilane to a thickness of about 250 μm. The wafer was electrochemically etched, usually at a cell voltage of about 10 V and a starting current of 2.5 - 2.8 A. In order to provide a well-defined dopant concentration at the top surface, each wafer was then vapor etched. By varying the etch time, films of different thickness were obtained from the same epitaxial deposition.

The thickness of each film was measured with an infrared spectrometer at several points in the fabrication process. The thickness of Hall samples from various locations on the wafer probably did not differ by more than about 10 percent from the value measured in the center of the wafer.

The cloverleaf, van der Pauw-Hall samples were then fabricated in

the thin film using conventional silicon technology. A vapor-deposited oxide was first formed on the silicon film surface and photomasked to open windows where the device contact areas would be located. Dopant atoms were diffused into these areas to insure good electrical contact during device testing. A 1020°C BBr_3 predeposition which produced a sheet resistivity of about 30 Ω/sq was used for the p-type films, and a 1070°C $POCl_3$ predeposition which produced a sheet resistivity of about 3 Ω/sq was used for the n-type films. After the boron or phosphorus glass was removed from the contact areas, the wafer was covered with a thick layer of aluminum. The complete Hall pattern was then defined in the metal by photomasking, and the exposed oxide and silicon film were etched until the underlying oxide was clean. A second photomasking step was used to remove the metal from all except the contact areas of the Hall pattern. After annealing at 450°C in a hydrogen/nitrogen ambient, the samples were mechanically thinned to 180 μm and separated into individual dice by conventional scribing techniques. Each die was 0.25 inch on a side.

As a basis for comparison, Hall samples were also fabricated on epitaxial control wafers. During each epitaxial deposition, substrates of opposite conductivity type were placed in the reactor along with the n^+ substrates for electrochemical etching. Hall samples were fabricated in these epitaxial films at the same time as in the corresponding thin films. These control samples allowed determination of differences between the electrochemically etched films and silicon layers which had not been electrochemically etched. They also served as a check on the experimental technique by allowing comparison to published mobility values.

4.2.2 van der Pauw-Hall measurements

The van der Pauw geometry (1) was used for these Hall measurements because of its convenience and sensitivity. This technique employs a cloverleaf sample with four contacts near its outer rim rather than the more conventional, rectangular bridge sample. The resistivity is first found by forcing a current I_s through two adjacent contacts and observing the voltage V_ρ produced at the other two contacts, in a manner similar to the square four-point-probe array (2). The presence of any asymmetry in the sample is determined and minimized by applying the current and

measuring the voltage in two perpendicular directions and by reversing the polarity of the applied voltage. The resistivity is then found from the formula

$$\rho = (\pi d/\ln 2)\ (\overline{V}_\rho/I_s), \qquad [4.1]$$

where d is the thickness of the sample and $\overline{V}_\rho$ is the average of the four values of voltage found. If appreciable asymmetry is observed, a correction factor given by van der Pauw can be employed, but its use was not necessary in the present experiments.

The Hall voltage V_H is then observed by applying a current I_s between two diagonally opposite contacts and observing the change in voltage between the other two contacts when a magnetic field is applied. A permanent magnet with a field of 4.1 kilogauss was used in these experiments. The direction of the magnetic field was reversed, and the current was applied in two perpendicular directions in order to minimize measurement errors. The Hall mobility is then given by the formula

$$\mu_H = \frac{\overline{V}_H\ d}{B\ I_s\ \rho}\ . \qquad [4.2]$$

By combining Eqs. [4.1] and [4.2], the mobility can be expressed as

$$\mu_H = (\ln 2/\pi)\ (\overline{V}_H/\overline{V}_\rho\ B), \qquad [4.3]$$

in which the sample thickness does not explicitly appear, allowing more ready comparison of different samples.

The voltages and currents were measured with Hewlett-Packard 425A microvolt-ammeters. In all cases the input impedance of the ammeter was much less than that of the sample, but in some cases the 1 MΩ input impedance of the voltmeter was not sufficiently large compared to the sample impedance to be neglected, and the data was corrected for the meter impedance as necessary. This correction was only significant for the most lightly doped samples, and primarily affected the carrier concentration rather than the mobility.

All samples were measured at two different current levels in order to preclude any nonlinearities. The two current levels generally differed by a factor of two and were chosen so that the voltage V_ρ was in

the range 10-50 mV. At least four samples from each wafer were generally tested with the median values reported.

A more significant difficulty with the interpretation of the experimental data arises from the difference between the Hall mobility and the drift mobility. This ratio can be expressed as $\mu_H/\mu_D = \tau^2/(\bar{\tau})^2$ (3), where τ is the mean time between randomizing collisions and is related to the particular scattering mechanisms involved. At a dopant concentration of approximately 10^{15} cm^{-3}, the mobility in bulk silicon is primarily determined by lattice scattering although some influence of ionized impurity scattering can be seen, especially in n-type samples.

Nakanuma (4) has investigated the ratio of the Hall mobility to the drift mobility in phosphorus-doped, silicon epitaxial layers and found the ratio to be approximately 1.2 for a dopant concentration of about 10^{15} cm^{-3}. This value was used for the reduction of the data from n-type films in the present experiments. Less extensive data is available for boron-doped samples as a function of dopant concentration, but Messier and Flores (5) have found the ratio to be 0.84 in lightly doped samples at room temperature. Since the mobility is primarily determined by lattice scattering at 10^{15} cm^{-3}, this value was used to reduce the data from the p-type films in these experiments. When these ratios were applied to the epitaxial control wafers processed and measured with the thin films, values of drift mobility close to published values were obtained, indicating that these ratios are reasonable.

4.3 Experimental Results and Discussion

4.3.1 P-type samples

Two series of p-type films were fabricated and thinned to varying thickness after initial experimental difficulties with the early samples had been overcome. Each series of samples was fabricated from a set of wafers on which the initial epitaxial film was deposited at the same time. The thickness of the epitaxial films on the first series (2980) ranged from 9.3-10.0 μm as measured by the uncorrected infrared interference technique (6). After electrochemical etching the films were 8.8-9.5 μm thick. This 0.5 μm difference is consistent with the amount which should be lost due to impurity interdiffusion at the epi/substrate

interface for the particular processing conditions employed, assuming that the etching stops at a donor concentration of about 2×10^{16} as indicated by Theunissen, et. al., (7). The wafers were then thinned by vapor etching at a temperature of 1200°C and a rate of about 0.5 μm/min to final thicknesses ranging from 4.6 to 7.7 μm.

The results of the Hall measurements are indicated in Table 4.1. The drift mobility found in the two epitaxial films (2980A and B) averaged 408 cm^2/V-sec, while the average of the drift mobility in the thin films (2980C-I) was about 393 cm^2/V-sec, a difference of only 4 percent. Within the series of thin films, the mobility decreased approximately 3 percent as the thickness decreased 40 percent. This small difference is probably not significant.

A marked variation in the indicated carrier concentration was seen in this series of films, however. The dopant concentration in the thin films appeared to be about twice as great as that in the epitaxial films. However, a difference of almost a factor of two was seen even after the initial epitaxial deposition. This difference was related to the different substrates used for the films which were to be subsequently electrochemically etched and those which were not to be etched. Subsequent investigation indicated that the difference cannot be attributed solely to the placement of the wafers in the reactor during the epitaxial deposition. (The wafers nearest the front of the reactor generally have a higher dopant concentration than do those near the exhaust end of the reactor.) The reason for the difference in dopant concentration due to the different substrate is not obvious. The films to be electrochemically etched were deposited on (111)-oriented, arsenic-doped wafers with a resistivity of 0.0015-0.0025 Ω-cm ($N_D \approx 3 \times 10^{19}$ cm^{-3}) while the control wafers were antimony doped with an impurity concentration of about 3×10^{18} cm^{-3}. Because of the close match between the radius of arsenic and silicon, the lattice constant of the arsenic-doped wafers is not expected to deviate significantly from that of intrinsic silicon while the antimony doped wafers should have a lattice constant about 8×10^{-5} Å larger than that of pure silicon. This difference is probably not large enough to affect the dopant concentration in the silicon

TABLE 4.1

Hall Mobility Data--Thin Silicon Films

Type	Run	Wafer	t (μm)	μ_H (cm^2/V-sec)	μ_D (cm^2/V-sec)	n or p(HALL) (10^{15} cm^{-3})	n or p(V/I) (10^{15} cm^{-3})	Spread of Mobility Data (%)
p	2980	A	epi	345	411	3.0	2.8*	2
		B	epi	340	405	2.6	2.8	3
		C	7.7	334	398	5.7	4.8	2
		E	6.7	330	393	4.9	4.8	2
		G	6.2	333	396	6.4	4.6	2
		I	4.6	324	386	5.4	4.4	2
							*from similarly doped epi run	
p	3064	A	epi	344	409	0.99	1.1	
		E	7.5	333	396	1.4	2.0	
		H	5.3	333	396	1.0	1.0	
		J	4.1	332	395	0.98	0.9	
p	2862	A	7.2	346	412	0.78	4 min vapor etch	
		C	8.5	339	403	0.69	1 min vapor etch	
n	2990	B	epi	1492	1245	2.1	1.4	1
		C	8.5	970	809	2.6		4
		E	7.4	1038	865	1.6		8
		I	7.0	1038	865	1.3		2
		G	6.1	958	798	1.2		1
		K	4.7	874	728	1.9		3
n	2951	A	epi	1436	1196	1.4	1.2	
		C	5.6	902	752	2.0		
n	2859	C	1.03	810	----	$N_s \sim 1 \times 10^{11}/cm^2$	1 min vapor etch	
n	2782	F	1.62	956	796	$N_s \sim 3 \times 10^{11}/cm^2$	no vapor etch	

films appreciably, however. The standard substrates and those for the control wafers also varied in dislocation density. The arsenic doped wafers had a very low dislocation density (<500 cm^{-2}) while no special care was taken to obtain low-dislocation-density wafers for the controls.

In order to investigate the source of this anomaly further, several test runs were carried out in which a different test substrate was placed between two of the standard substrates in the reactor gas stream, and epitaxial films were simultaneously deposited on all three substrates. In all cases the resistivity of the epitaxial films on both of the standard substrates was markedly less than the resistivity of the film on the test substrate which was located between the two standard substrates. Thus, the effect of wafer placement may definitely be eliminated. The results of the experiments are shown in Table 4.2. From these results, we can see that the anomaly appears to be associated only with the standard substrates and cannot be attributed to the dopant species (arsenic or antimony) or the effect of dislocation density (<500 cm^{-2} or 10^5 cm^{-2}) and that the effect of substrate orientation [(111) or (100)] is also not significant. The possibility of a fast diffusing contaminant in the ingot from which the standard substrates were cut does remain, however. A further experiment compared standard substrates cut from the present ingot to one from a previous ingot. The epitaxial film grown on the older wafer did not show the anomalously low resistivity. This point should be investigated further. However, it is not especially relevant to the present investigation since a similar difference between the thin films and the control samples was seen after the initial epitaxial deposition and in the Hall measurements.

The mobility of 408 cm^2/V-sec observed in the epitaxial films is somewhat lower than the published value of 450 cm^2/V-sec at 3 X 10^{15} cm^{-3} (8). The slightly lower value of mobility seen in the thin-film samples may be related to the somewhat higher dopant concentration in these films than in the epitaxial control samples.

Another series of p-type samples (3064) was less heavily doped than the first set, but of approximately the same thickness, varying from 4.1 to 7.5 μm after the vapor etch. The data for these samples are also indicated in Table 4.1. The mobility in the thin films was

TABLE 4.2

Comparison of Resistivity of Epitaxial Films on Various Substrates

Substrate				Epitaxial Resistivity (Ω-cm)		
Dopant	Orientation	Resistivity (Ω-cm)	Dislocation Density (cm^{-2})	Standard Substrate A	Test Substrate B	Standard Substrate C
As	111	.0015-.0025	10^5	2.5	5.1	2.4
As	100	.0015-.0025	<500	2.6	4.9	2.6
Sb	111	.005 -.013	10^4	2.9	3.9	2.6

again about 4 percent less than that in the epitaxial control sample, and little difference was seen between the thin-film samples of varying thickness. The carrier concentration behaved similarly to that observed in the first series of p-type samples. The indicated carrier concentration in the epitaxial film (front of reactor) was less than that of the nearby thin-film samples, with the carrier concentration among the thin-film samples decreasing toward the exhaust end of the reactor. The carrier concentration indicated by a V/I measurement of the initial epitaxial layer is also shown in Table 4.1; reasonable agreement was found with the Hall data. The results of the initial four-point-probe measurements on lightly doped samples of this nature are somewhat unreliable, however. The mobility in the epitaxial film was again only slightly lower than would be expected from published values. However, the good agreement between the two series of samples indicates that the mobility is not being limited by the formation of the thin films or influenced by erratic process variations.

4.3.2 N-type samples

The results observed on the n-type samples differed markedly from the results on the p-type samples. While the mobilities observed on the thin-film and control wafers were almost identical for the p-type samples, these mobilities differed markedly for the n-type samples, as seen in Table 4.1. While the mobility in the epitaxial control samples was reasonably close to the published value of mobility, the values in the thin-film samples were markedly lower. This difference was seen in two different sets of samples fabricated at widely separated times. For the set of samples vapor etched to different thicknesses (2990), a lower median mobility was observed for the thinner samples. These differences in mobility appear to be appreciably greater than the scatter in the data and are probably significant. They will be discussed in detail in Sec. 4.4.

4.3.3 Thinner samples

Brief experiments on some thinner samples provided further insight into the structure under consideration. Hall samples were prepared on two wafers which had initial lightly doped, p-type epitaxial layers about 2 μm thick. One sample (2859C) was vapor etched for one

minute after electrochemical etching while the other (2782F) was not further thinned after electrochemical etching. The van der Pauw samples were then fabricated on both wafers as described previously. Both samples indicated n-type conduction even though the deposited epitaxial layers were p-type. The n-type conduction can be attributed to a thin, n-type surface layer which is left on the top surface of the electrochemically etched film. The sample which had not been vapor etched showed a Hall mobility of about 956 $cm^2/V\text{-}sec$ similar to that seen in the n-type samples, while the vapor-etched sample showed a somewhat lower mobility.

We can calculate the amount of n-type impurity left on each wafer from a two-layer model. The indicated Hall mobility will be an average of the mobility of the n-type surface layer and the p-type film weighted by the conductance of each region.

$$\mu = \frac{\mu_n g_n - \mu_p g_p}{g_n + g_p} = \frac{\mu_n^2 N_s - \mu_p^2 pt}{\mu_n N_s + \mu_p pt}, \qquad [4.4]$$

where N_s is the net number of donor atoms (cm^{-2}) left in the surface layer, p is the dopant concentration (cm^{-3}) in the p-type layer and t is the thickness of the p-type layer.

By using reasonable values in Eq. [4.4] for the unetched film, the first term in both the numerator and denominator can be seen to dominate the expression, and the mobility measured is similar to the mobility of the carriers in the surface channel. From the measured conductance the net number of donor atoms in the surface layer of the unetched film is then found to be about 3×10^{11} cm^{-2}. This value is reasonable assuming that the etching terminates at a dopant concentration of about 2×10^{16} cm^{-3} and the residual n-type layer is a few tenths of a micron thick. Much of this residual layer is removed by the vapor etch, but a weak n-type surface layer still may remain although it was not found on all similar samples. From Eq. [4.4] the residual donor concentration is found to be about 1×10^{11} cm^{-2} in the surface layer after the one-minute vapor etch.

4.4 Discussion

The major observation from the Hall measurements on the thin silicon films is that the majority carrier mobility in n-type samples is considerably less than that in similarly doped bulk samples while the mobility in p-type films is approximately the same as in bulk wafers. This striking difference must be discussed in some detail.

Two possible explanations for the reduction in the observed electron mobility will be discussed in this section. First, we will consider the different behavior of n-type and p-type films in the electrochemical etch and attempt to relate the mobility reduction to the formation of etch-channels in the n-type films during electrochemical etching. These voids and the surrounding space charge regions will reduce the conducting area of the n-type films and would cause the observed mobility to be less that the microscopic film mobility. The second model considers the effect of an accumulation layer near the bottom surface of the thin film. If the carriers have a reduced mobility in this conducting channel, the observed mobility will again be reduced below the microscopic mobility of carriers in the bulk of the film.

It has been observed that a high density of etch channels may occur during the etching of n-type films while few are formed when etching p-type films (9). These channels will form nonconducting, cylindrical voids in the samples with their axes along major crystallographic directions. Although these voids appear during the electrochemical etch, they are accentuated during the subsequent vapor etch which is used to thin the samples to the desired thickness for the Hall measurements. Since up to 5 μm of silicon was removed from the Hall samples during the vapor etch, considerable enlargement of the voids may have occurred.

In order to consider the effect of these voids on the mobility and carrier concentration, we will first consider the simple model of Juretschke, Landauer and Swanson (10) and then the more detailed treatment of Wolfe, Stillman and Rossi (11) for the case of the van der Pauw geometry. For the case of nonconducting cylinders parallel to the magnetic field and perpendicular to the applied electric field, Juretschke, et. al., find that the measured Hall coefficient, and hence the apparent carrier density, equals that of the conducting portions of the film

while the measured conductivity and mobility are less than those of the conducting portions of the film. In particular, the measured mobility $\bar{\mu}$ is given by

$$\bar{\mu} = \mu_o \frac{1 - \varepsilon}{1 + \varepsilon} , \qquad [4.5]$$

where ε is the fraction of missing conductive material, μ_o is the mobility in the conducting regions, and the cylinders are assumed to be far enough apart to be noninteracting. For cylinders which have a component perpendicular to the direction of the magnetic field, the measured carrier density, conductivity and mobility are all reduced below the corresponding quantities in the conducting material. If we assume that the majority of the cylinders lie in a direction parallel to the magnetic field and that the average measured mobility is about 66 percent of the single-crystal mobility, we find that the voids and surrounding nonconducting space charge regions comprise about 20 percent of the material. This value is, of course, approximate since not all the voids are perpendicular to the film plane and the van der Pauw geometry is sensitive to voids in the central region.

A more detailed treatment of a different conductivity region in a van der Pauw sample has been given by Wolfe, et. al. (11). For the case of a nonconducting inhomogeneity at the center of a van der Pauw sample, their Eqs. [A-5] and [A-6] for the apparent resistivity and Hall coefficient simplify to

$$\bar{\rho} = \frac{1}{\sigma_o \ln 2} \sum_{n=1}^{\infty} \frac{1 + 4\varepsilon^n + \varepsilon^{2n}}{1 - \varepsilon^{2n}} \frac{(-1)^{n+1}}{n} , \qquad [4.6]$$

and

$$\bar{R} = \frac{\mu_o}{\sigma_o} \frac{4}{\pi} \sum_{n=1}^{\infty} \frac{(-1)^{n+1}}{2n+1} = \frac{\mu_o}{\sigma_o} , \qquad [4.7]$$

and the measured mobility becomes

$$\bar{\mu} = \mu_o \ln 2 \left[\sum_{n=1}^{\infty} \frac{(-1)^{n+1}}{n} \left(\frac{1 + 4\varepsilon^n + \varepsilon^{2n}}{1 - \varepsilon^{2n}} \right) \right]^{-1} , \qquad [4.8]$$

where ε is again the fraction of voids. The approximation $\mu B << 1$ has been used since $\mu B < 0.126 \times 0.41 = 0.052$ for all samples tested. This

model also assumes that the cylindrical voids are parallel to the magnetic field and again leads to the conclusion that the measured carrier density is equal to the carrier density in the conducting regions while the measured mobility is less than the mobility in the conducting regions. In this case, the fraction of voids is found to be about 10 percent if the measured mobility is again assumed to be 66 percent of the bulk value.

If the mobility is reduced by voids related to channels formed during electrochemical etching, two trends in the data should be generally observable. First, the density of channels should vary across the wafer with the areas of the wafer which were completely etched first showing the most channels and, consequently, the lowest mobility. There should be a large spread in the mobility data between samples since no care was taken to determine the position on the wafer of each sample. Examining the data, we find that the mobility values for the n-type samples show only slightly more spread than do those of the p-type samples, in which channeling is not as prevalent.

The second trend which should be observable is a variation of the mobility with thickness. Each series of n-type samples was formed by growing epitaxial layers on several substrates to the same thickness and then depositing polycrystalline silicon and electrochemically etching the wafers. At this point the films were all approximately the same thickness. Each film was then vapor etched for a different length of time so that a different final film thickness was achieved. It is expected that during the vapor etching the channels were also etched and widened so that the thinnest film, which had been vapor etched for the longest time, had the widest nonconducting, cylindrical channel regions. Consequently, the thinnest film should have the lowest mobility. In agreement with this expected behavior, the mobility was generally found to decrease as the n-type films became thinner. This trend was not observed in p-type films, in which the formation of etch channels is generally not as significant.

The low mobility observed in the n-type thin films may be explained by an alternative model also. The presence of an accumulation layer near the bottom surface of the silicon film may cause the observed

mobility to be lower than the mobility in the bulk of the film if appreciable conduction occurs in the accumulation layer and if the mobility of carriers is less in the accumulation layer than in the remainder of the film. Both of these assumptions are probably fulfilled in the present case. Accumulation layers are generally formed on n-type surfaces, especially during steam oxidation (12), and the mobility of electrons in surface channels is generally found to be about half of that in bulk silicon (13).

In the presence of a conducting surface layer, the observed mobility would be the average of the mobility in each of the two regions weighted by the respective conductances g of the bulk of the film and the underlying accumulation layer

$$\bar{\mu} = \frac{\mu_f\, g_f + \mu_s\, g_s}{g_f + g_s} = \frac{\mu_f^{\,2}\, n_f t + \mu_s^{\,2}\, N_s}{\mu_f\, n_f t + \mu_s N_s} \quad , \qquad [4.9]$$

where the subscripts f and s refer to the bulk of the film and the underlying surface layer, respectively, n_f is the carrier concentration (cm^{-3}) in the film, and N_s is the induced carrier density (cm^{-2}) in the surface layer. Figure 4.1 shows the effect of various values of carrier density in the film and in the surface channel as a function of the film thickness computed using values of Hall mobility of 1500 cm^2/V-sec and 800 cm^2/V-sec for the thin film and the surface layer, respectively. We find that the observed mobility does, indeed, decrease as the film becomes thinner since a greater fraction of the conductance is then carried in the surface layer where the carriers have lower mobility. The data available from the present experiments do not allow accurate computation of the mobilities in the two regions, however, because of their limited scope and the possible nonuniformity of dopant concentration from wafer to wafer. The general trends observed in Table 4.1, however, do indicate that a conducting surface layer near the bottom of the film can explain the data and is an alternative model to the presence of voids discussed above.

It should be noted that the conducting channel must be near the bottom surface, rather than the top surface, of the thin film since similar surface conditions should prevail at the upper surfaces of both

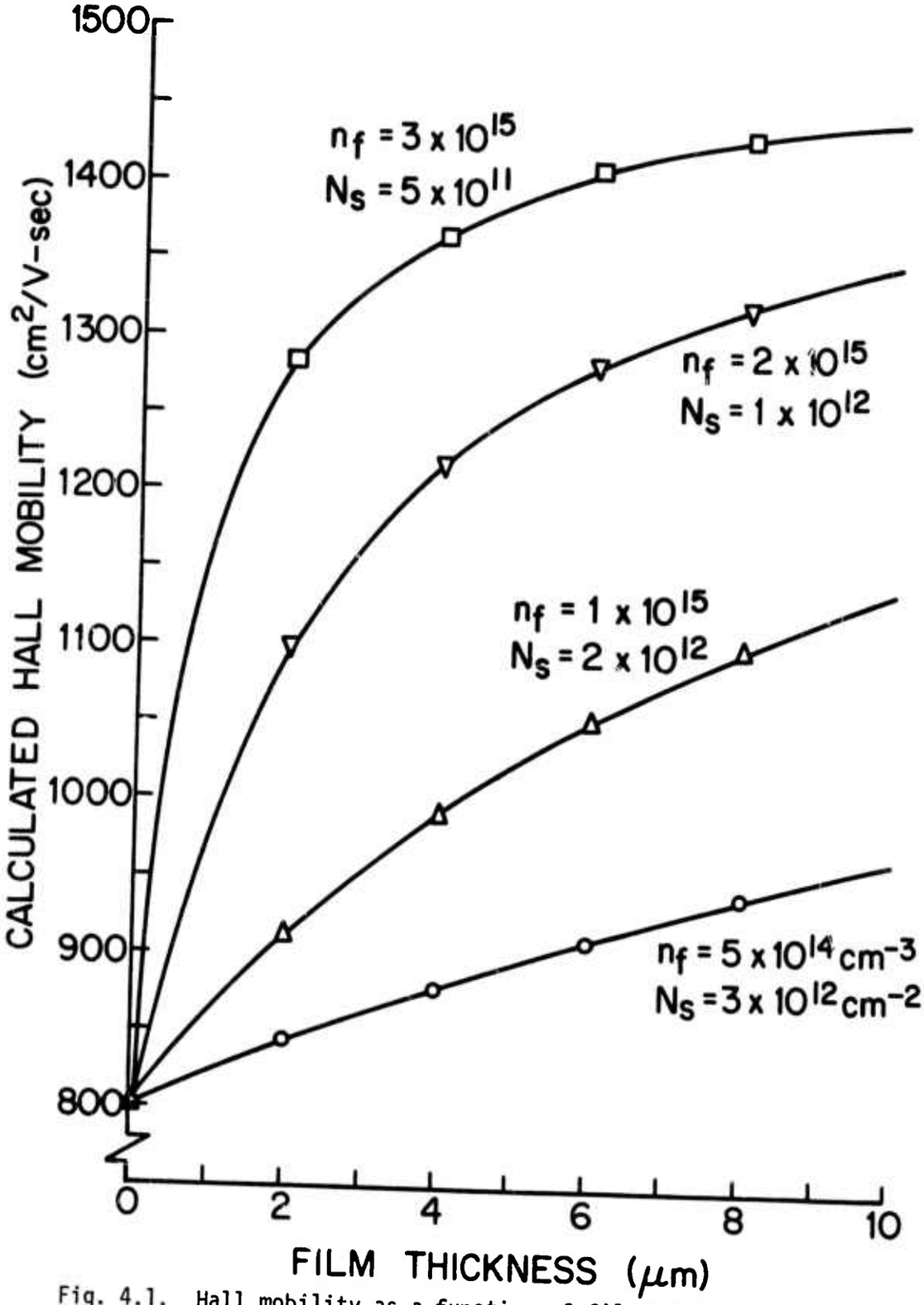

Fig. 4.1. Hall mobility as a function of film thickness calculated for an n-type film with an accumulation layer at the bottom surface for several values of film doping, n_f, and surface charge, N_s (μ_{Hf} = 1500 cm^2/V-sec, μ_{Hs} = 800 cm^2/V-sec).

the thin-film samples and the control wafers.

The presence of the conducting surface layer is also consistent with the limited scatter seen in the mobility data from the n-type samples. The last column of Table 4.1 indicates the range in which half of the eight data points from each sample fell. If the mobility were limited by voids, marked scatter would be expected from sample to sample depending on the location of the sample on the wafer since the void density should vary strongly across the wafer. Since the scatter in the data from the n-type samples is only slightly greater than that in the p-type samples, the surface-layer model may explain the data more adequately than the void model.

We can also see that the effect of the surface layer would only be observed on the n-type samples since the bottom of the p-type samples would be expected to be depleted or even inverted. In the case of a depletion region, few carriers would be near the surface, and the average mobility would not be reduced appreciably below the value in the film away from the surface. In the case of an inversion layer, a p-n junction would separate the film and the conducting channel, and the conductance of such a channel would not influence the mobility observed in the p-type film.

Thus, although we cannot differentiate between the two models to explain the low values of observed mobility on n-type samples, the bulk of the arguments tend to support a model in which an appreciable fraction of the conduction occurs in an accumulation layer near the bottom surface of the thin film.

The influence of surface scattering on the measured mobility should also be briefly mentioned. Following the treatment by Many, et. al. (14), we find that surface scattering will become important only when a significant number of carriers are within a few mean free paths of the semiconductor surface. If no significant accumulation layers exist at the surfaces of the samples, as in the case of p-type films, then surface scattering will be important only if the film thickness is comparable to the mean free path. The mean free path can be computed from

Eq. [8.7] of Many (14)

$$\lambda = \mu_b \sqrt{m^* kT/2\pi q^2} \lesssim 110 \text{ Å} \qquad [4.10]$$

for silicon at 300°K. Since the computed value of 110 Å is much less than the thickness of any of the films under consideration here, we may neglect surface scattering as a mechanism limiting the carrier mobility in the thin, p-type silicon films.

4.5 Summary

The results of Hall mobility measurements on the thin silicon films formed by electrochemical etching have been reported in this section. Measurements were taken on both p-type and n-type samples of varying thicknesses with about 10^{15} cm^{-3} dopant atoms. The mobilities observed in the thin-film and control samples were almost identical for the p-type films. However, the mobilities measured in the n-type films differed markedly from those in the control samples. This behavior may be caused by either voids in the film or by an accumulation layer with lower carrier mobility at the bottom surface of the n-type thin film. Discussion in Sec. 4.4, as well as measurements on MOS structures to be discussed in Sec. 5.4.4, suggests that the latter explanation is probably relevant in the case of the thin films. Measurements on very thin samples indicated that an n-type surface layer was left on p-type samples immediately after electrochemical etching. These results suggest that the characteristics of semiconductor devices fabricated in the thin films formed by electrochemical etching will not be degraded by reduced majority-carrier mobilities.

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5. MINORITY-CARRIER LIFETIME

5.1 Introduction

The minority-carrier lifetime is probably second only to the majority-carrier mobility as the material property which determines device performance. While this parameter plays a secondary role in majority-carrier devices, such as MOS transistors, it dominates the behavior of devices which rely on minority-carrier motion for their operation, such as bipolar transistors and charge-coupled devices.

In bipolar transistors the lifetime must be significantly greater than the transit time of carriers across the base region in order to obtain a high-gain device. If the transit time is greater than the lifetime, most of the carriers injected from the emitter into the base will recombine before reaching the collector, and the gain of the transistor will decrease. For present-day bipolar transistors,which operate in the megahertz region, the lifetime must be of the order of a microsecond to prevent gain degradation. Even in very high-frequency devices,in which the lifetime is purposely reduced in order to minimize minority-charge storage and improve the switching time, a much longer lifetime is initially desirable so that it can be reduced in a controlled manner.

In the charge-coupled structure, a deep depletion region is formed under a layer of insulating silicon dioxide, and minority carriers may be injected into this potential well. In order to obtain useful device operation, these injected carriers must move through several stages of the structure before a significant number of additional minority carriers are thermally generated. For a lower frequency of operation of the order of 1 kilohertz, the generation time of these additional minority carriers must be of the order of 10 to 100 msec. For the lightly doped substrates generally used in charge-coupled structures, the minority-carrier lifetime must, therefore, be at least 10 μsec, while much greater values are desirable for low-frequency and image-sensing applications.

In addition to its direct impact on device performance, the minority-carrier lifetime is generally accepted as a direct measure of the quality of the material being investigated since it is significantly reduced by material defects such as dislocations. For these reasons the minority-carrier lifetime was studied in both n-type and p-type, thin silicon films formed by the electrochemical-etching process.

5.2 Experimental Approach

Two types of structures are generally used to measure minority-carrier lifetime. P-n junction diodes and bipolar transistors can be directly studied in order to find the lifetime if it is short enough to dominate the characteristics of these devices. If it is relatively long, however, the effects of the lifetime are obscured by other limitations in the structure, and only a lower limit on the lifetime can be ascertained. In this case more significant information can generally be obtained by observing the time required to generate an inversion layer in an MOS structure. The time required to form the inversion layer can then be related to the minority-carrier lifetime. One possible discrepancy between the two types of measurements, however, is a potentially significant difference in the parameter measured (1). In the case of junction devices, the time required for injected carriers to recombine is generally measured while MOS structures generally indicate the time required for the generation of minority carriers. With the usual assumption that the most effective generation and recombination centers are located at the center of the forbidden energy gap, these two parameters are generally similar. However, they may differ significantly if the centers are displaced appreciably from midgap.

5.3 Junction Structures

5.3.1 P-n junctions

In p-n junctions the recombination of carriers injected across the junction is generally investigated in order to determine the lifetime. If the lifetime is short or the space-charge region into which carriers are injected is long, recombination within the space-charge

region may be observed. If recombination occurs within this depletion region, the current will be given by

$$J_{rec} = \frac{1}{2} q \frac{n_i}{\tau_0} W \exp (q|V_F|/2kT) \qquad [5.1]$$

where W is the width of the depletion region and V_F is the forward voltage applied across the junction. At room temperature the current will change by a factor of ten for every additional 120 mV applied across the junction. On the other hand, if the injected carriers traverse the space-charge region and recombine in the neutral region, the current will change by a factor of ten for every 60 mV change in applied voltage. The lifetime may also be found from neutral-region recombination provided that the device dimensions are much longer than the diffusion length, $L = \sqrt{D\tau_0}$, of the injected minority carriers. For short lifetimes and wide depletion regions, the lifetime may also be obtained from the generation observed in the depletion region.

During the initial stages of this investigation, the characteristics of junction diodes were studied. These junctions were fabricated by adding p^+ diffusions to n-type epitaxial films which were deposited on the electrochemically etched films. Before the epitaxial film was deposited, a heavy,n-type diffusion was added to the electrochemically etched film to reduce series resistance. The lifetime of carriers injected into the space-charge region at the p-n junction was observed in these experiments. Space-charge-region recombination was seen in some junctions, especially at low current levels. In most of the junctions, however, a current change close to the ideal 60 mV per decade, characteristic of neutral-region recombination,was seen. Even in most cases, where space-charge-region recombination was seen at lower current levels, the current exhibited a 60 mV per decade slope at higher currents. Generally, the few junctions which exhibited space-charge-region recombination were located in areas of the wafer with higher defect densities. Therefore, the reduced lifetime was attributed to isolated

defects in the film rather than to the basic properties of the film itself. Lifetimes ranging from 2 nsec to 2 μsec were found in the defective junctions by using Eq. [5.1]. The reverse characteristics of these devices also indicated similar lifetimes.

Most of the junctions, however, indicated neutral-region recombination over the entire current range studied (100 pA - 3 mA), and only a lower limit on the lifetime of several microseconds could be ascertained. For this lower limit the corresponding diffusion length is approximately 50 μm, much greater than the thickness of the films under consideration. Therefore, no value of hole lifetime could be obtained from these measurements since most of the injected carriers could diffuse through the film to the back of the device, rather than recombining in the film itself.

5.3.2 Bipolar transistors

During an investigation of the quality of the films fabricated by electrochemical etching, many large-area, npn bipolar transistors were fabricated in thin films which had a total thickness of about 2 μm [Fig. 3.8(a)]. Measurement of the current-voltage characteristics of these transistors allowed a determination of the lifetime of carriers injected into the emitter-base space charge region.

The base and collector currents were measured as a function of the emitter-base voltage, and no discernible differences between the transistors fabricated in the thin films and those fabricated in bulk control wafers were seen. Figure 5.1 shows the base and collector currents and the reciprocal of the common-emitter current gain, h_{FE}, plotted as functions of the emitter-base voltage at room temperature for a typical transistor. At low values of V_{EB}, the reciprocal of h_{FE} approaches a relation of the form exp $(-qV_{EB}/2kT)$, indicative of recombination in the space-charge region at the emitter-base junction. The reciprocal of the current gain may be written as (3)

$$\frac{1}{h_{FE}} = \frac{1}{2}\left(\frac{W_B}{L_{nB}}\right)^2 + \frac{Q_B}{D_{nB}}\,\frac{D_{pE}}{Q_E} + \frac{Q_B}{qD_{nB}}\,\frac{W_{EB}/\tau_o}{2n_i\,\exp(qV_{EB}/2kT)}. \qquad [5.2]$$

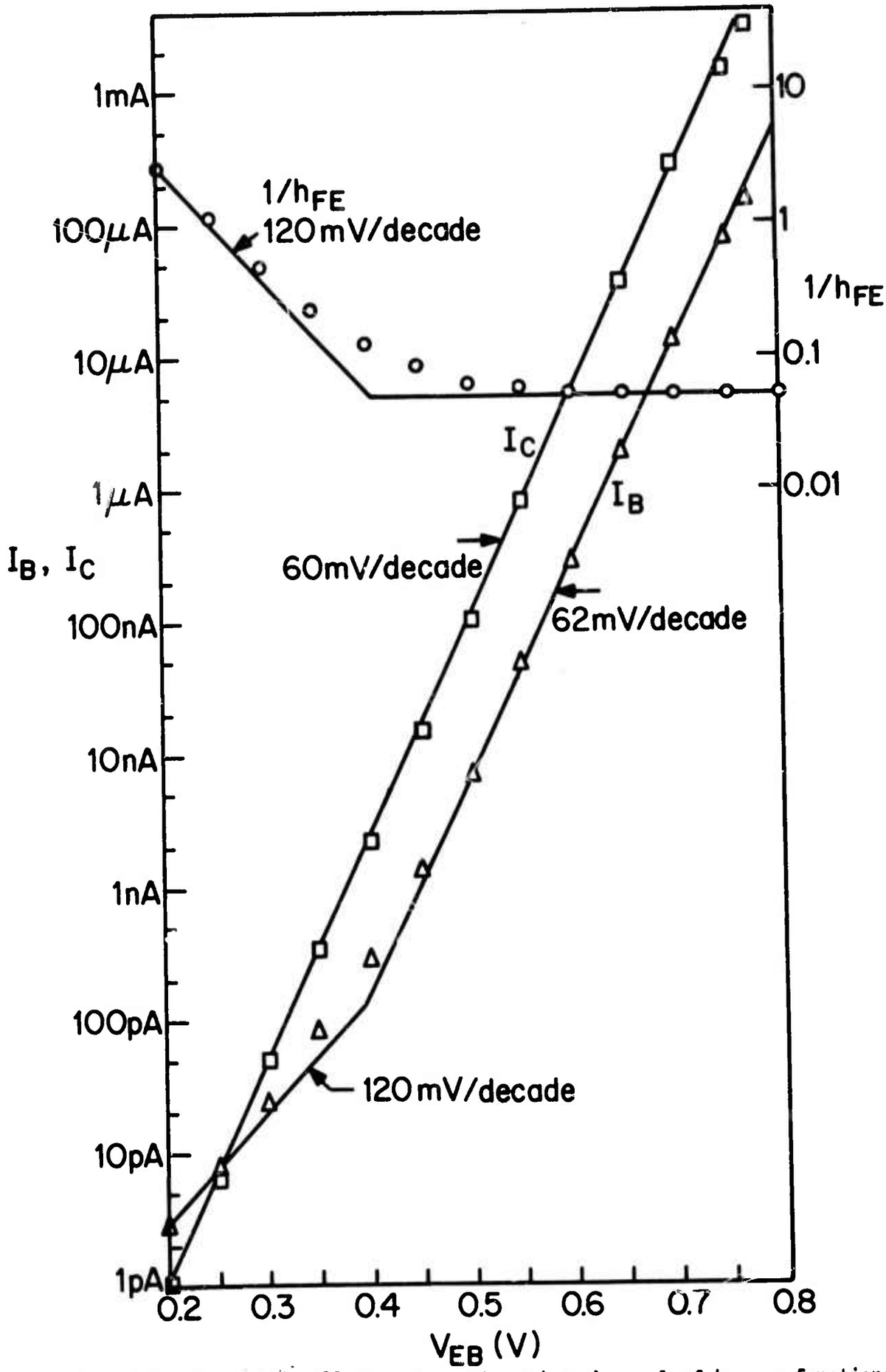

Fig. 5.1. Base and collector currents and reciprocal of h_{FE} as functions of emitter-base voltage for shallow bipolar transistor at room temperature.

The three terms in this expression describe recombination within the neutral base region, injection into the emitter, and recombination within the emitter-base space charge region, respectively. Since only the latter term is a strong function of applied bias and follows the form $\exp(-qV_{EB}/2kT)$ observed, we may attribute the current gain falloff at low currents to recombination in the emitter-base space charge region and calculate an approximate value of the lifetime. For the transistor used in this experiment, Q_B/qD_{nB} was calculated from the collector characteristics to be about 2×10^{12} sec/cm^4. From cross sections of these devices [Fig. 3.8(b)], the width of the emitter-base space charge region was found to be 0.24 μm. Using these values in Eq. [5.2], we find the lifetime of carriers injected into the space-charge region to be about 12 μsec, consistent with the lower bound for the lifetime found from the p-n junctions fabricated much earlier in the study.

Although this analysis neglects surface recombination, surface recombination is probably not significant here since the depleted surface area is much smaller than the junction area in this large transistor. From the calculated carrier lifetime, the diffusion length is found to be about 130 μm while the base width is about 0.8 μm. Consequently, recombination in the neutral base region is negligible, and the high-current gain is determined by the second term in Eq. [5.2]--injection into the emitter.

Thus, from the characteristics of bipolar transistors fabricated in epitaxial layers grown on the thin silicon films, the carrier lifetime was found to be of the order of 10 μsec, consistent with the lower bound of several microseconds found from the earlier p-n junction measurements. From these results we may conclude that the lifetime is long enough so that the characteristics of bipolar transistors fabricated in the thin films will not be limited by low lifetimes.

These results, however, apply to the epitaxial film grown on the electrochemically etched film rather than to the electrochemically etched film itself. However, we would not expect the epitaxial film to show significantly longer lifetimes than the material on which it is fabricated. In order to measure the lifetime in the electrochemically

formed films more directly, the majority of the lifetime experiments conducted during the present study involved generation of minority carriers in the nonequilibrium, depletion region of MOS structures.

5.4 Deep-Depletion MOS Structure

5.4.1 Theory of operation

The basic, deep-depletion structure used in these experiments is shown in Fig. 5.2. The source and drain diffusions are of the same conductivity type as the film under the gate so current can flow from source to drain through the undepleted portion of the film. As the gate voltage is changed to repel mobile carriers from the channel of the device, a depletion region is formed; the width of the conducting channel is constricted; and the current observed is reduced. At large enough gate voltages, an inversion layer of conductivity type opposite to the film type will be formed under the gate, and the depletion region will no longer widen with increasing gate voltage. Then, the width of the conducting channel beneath the depletion layer will no longer change, and the observed current will also remain constant. However, a significant time will pass before minority carriers can be generated to form the inversion layer. If the gate voltage is changed rapidly, the depletion region will initially be wider than its equilibrium value. Consequently, the conducting channel will be narrower, and the observed current will be less than its equilibrium value during the time while the inversion layer is forming.

The formation time of the inversion layer may be related to the minority-carrier generation rate in the depletion region (4). The charge induced in the semiconductor, Q_s, must be the sum of the charge in the inversion layer and that in the depletion region in order to preserve electrical neutrality:

$$Q_s = Q_p + q\, N_D\, x_d, \qquad [5.3]$$

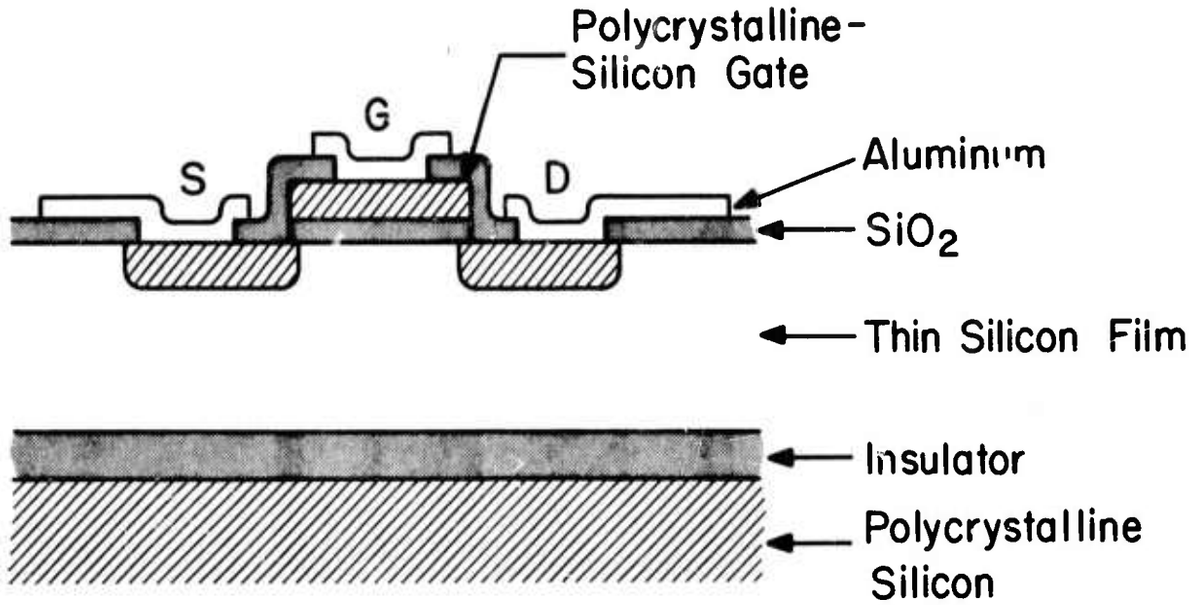

Fig. 5.2. Cross section of deep-depletion MOS transistor fabricated in thin silicon film. Source, drain and gate diffusions are of the same conductivity type as the thin film.

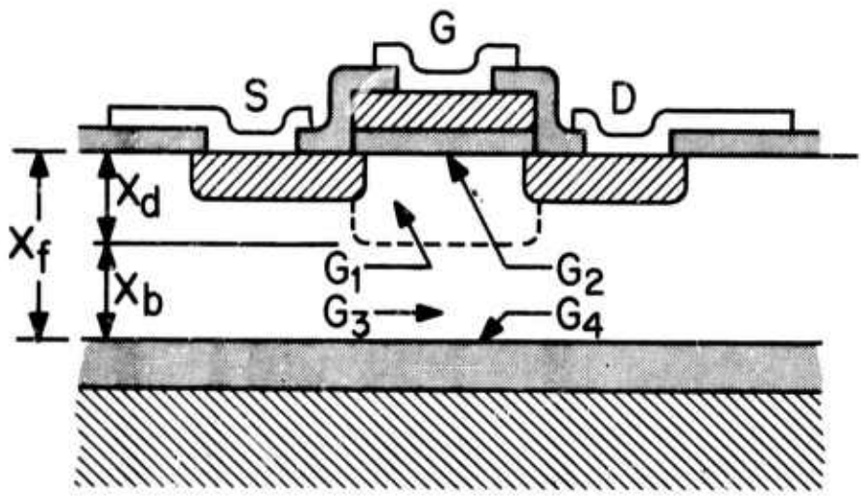

Fig. 5.3. Deep-depletion MOS structure showing regions of minority-carrier generation.

where x_d is the depletion-region width at any time after the application of the gate voltage, and an n-type semiconductor is assumed. The generation rate of minority carriers (holes in this case) is given by

$$\frac{dQ_p}{dt} = Uq(x_d - x_{de}), \qquad [5.4]$$

where U is the generation rate within the depletion region and x_{de} is the width of the equilibrium depletion-region. Since Q_s is approximately constant

$$\frac{dQ_p}{dt} = -q\, N_D \frac{dx_d}{dt} = Uq(x_d - x_{de}). \qquad [5.5]$$

The time response of the depletion-region width is then found to be of the form

$$x_d - x_{de} = x_o \exp\,(-Ut/N_D), \qquad [5.6]$$

and the time constant t_f associated with the formation of the depletion region is $t_f = N_D/U$. Since the mobile carrier concentrations are very small in the depletion region, $U = n_i/\tau_o$ where τ_o is now the minority-carrier <u>generation</u> lifetime. The lifetime can then be expressed in terms of the formation time of the inversion layer as

$$\tau_o = t_f \frac{n_i}{N_D}. \qquad [5.7]$$

Since the width of the conducting channel varies with the same time constant as the depletion layer, the lifetime can be found from the time response of the source-drain conductance and Eq. [5.7].

This straightforward analysis assumes that most of the minority carriers are generated within the depletion region. However, several competing generation mechanisms may also contribute carriers to the inversion layer. Each of these must be briefly discussed in order to determine if they are significant in the present case and preclude the application of Eq. [5.7] to determine the minority-carrier lifetime.

First, we can briefly consider the effect of illumination. If light is incident on the sample and the film is thin enough so that the minority carriers are generated uniformly throughout the film, the charge in the inversion layer will approach its equilibrium value linearly with time; the depletion layer width will decrease linearly; and the conduction in the channel will increase linearly with time (5). This behavior has been observed in the thin-film structures under consideration here. The generation rate increased, and hence the time for formation of the equilibrium charge distribution decreased with increasing light intensity, as expected.

If the sample is not illuminated, however, the carriers must be thermally generated at various regions in the structure (6). The net generation rate in the depletion region can be written as $G_1 = n_i (x_d - x_{de})/\tau_o$. In the particular structure indicated in Fig. 5.3, we can identify three major generation mechanisms in addition to generation in the depletion region. First, thermal surface generation may occur at the top Si/SiO_2 interface. Since this silicon surface will be initially depleted of carriers if the depleting gate-voltage pulse is applied to an initially accumulated surface, the generation rate may be significant. This rate may be written

$$G_2 = n_i s_o, \qquad [5.8]$$

where s_0 is the surface generation velocity at the depleted surface. Once an appreciable number of minority carriers are generated, however, this surface will be shielded from the space-charge region and the generation rate there will decrease. Similarly, if an inversion layer initially exists at the surface before the gate voltage is changed to induce further inversion, the generation rate at this surface will be less than if the surface were initially accumulated. Thus, if the response times are similar when the structure is pulsed from accumulation and from inversion, we can conclude that generation at this surface does not dominate the response.

Schroder and Nathanson (7) also indicate that the interpretation of the observed decay characteristics may be influenced by lateral spreading of the depletion region as well as by its increase in depth. In the present case, however, the depletion region is surrounded on both sides by the heavily doped source and drain regions so that little lateral spreading of the depletion region is expected.

Two other regions which may contribute significantly to the generation are the neutral portion of the film, x_b, beneath the space-charge region and the neutral Si/SiO_2 interface at the bottom surface of the thin film. Carriers generated in these regions will influence the observed behavior only if they are formed within a diffusion length of the edge of the depletion region. Since the thickness of the film is much less than the diffusion length, however, this condition is fulfilled for all the structures considered in this investigation. Since generation and diffusion are involved, these two generation rates are coupled and are given by (6)

$$G_{3,4} = \frac{n_i^2}{N_D} \frac{D_p}{L_p} \frac{s_o' L_p/x_b + D_p/L_p}{s_o' + D_p/x_b} , \qquad [5.9]$$

where s_0' is the surface generation velocity at the bottom Si/SiO_2 interface.

For small values of s_o' the ratio of generation in the depletion region to the contributions from the neutral region and underlying Si/SiO_2 interface becomes

$$\frac{G_1}{G_{3,4}} = \frac{(x_d - x_{de})\, N_D}{x_b\, n_i} . \qquad [5.10]$$

For reasonable values of the variables ($N_D \approx 10^{15}$ cm^{-3} and $x_b \approx 10^{-4}$ cm), this ratio is of the order of 10^5, and $G_{3,4}$ may be neglected. For large values of s_o', the ratio becomes

$$\frac{G_1}{G_{3,4}} = \frac{(x_d - x_{de})\, x_b\, N_D}{D_p\, \tau_o\, n_i} . \qquad [5.11]$$

In most cases this ratio is also larger than unity, but in some cases $G_{3,4}$ may become comparable to G_1. The influence of $G_{3,4}$ must, therefore, be considered again after the experimental data are presented.

If the depletion region does reach the bottom surface of the silicon film, the generation rate G_5 due to this Si/SiO_2 interface will be $n_i s_o$ --the same form as for generation at the top Si/SiO_2 interface. The magnitude of the surface generation velocity at the bottom surface, however, is unknown since the influence of the hydrogen anneal on the surface states at this underlying interface has not been investigated. A large value is not at all unlikely so that this component may exceed the generation rate in the bulk of the depletion region. If, however, the depletion region extends to the bottom of the silicon film, the source-drain conductance would be very low while the film was completely depleted and then would increase as the depletion region became narrower than the thickness of the film. The markedly different time response would allow this case to be easily differentiated from the previous case. The decay time measured after the conducting channel started to form would probably still be related to the generation in the

bulk of the depletion region and at the top Si/SiO_2 interface. Information about the surface generation velocity at the bottom interface may be extracted from the time required before any conduction is seen in the film; i.e., the time required for a conducting channel to start forming.

5.4.2 Sample fabrication and experimental measurements

Films of both conductivity types were formed by electrochemical etching in the manner described previously (Section 2). They were then thinned to several different thicknesses by vapor etching for varying times so that the effect of film thickness could be investigated. Deep-depletion MOS structures were subsequently fabricated. The samples were first oxidized at 1200°C in a dry O_2 ambient to form a 0.14 μm-thick gate oxide, which was then covered with about 0.8 μm of polycrystalline silicon to serve as the gate electrode. These layers were then defined by photomasking using a circular pattern to eliminate peripheral leakage paths. The source, drain, and gate regions were doped with phosphorus for the n-channel devices and boron for the p-channel devices. Either a 960°C PBr_3 predeposition which produced a sheet resistivity of about 10 Ω/sq or a BCl_3 predeposition which produced a sheet resistivity of about 30 Ω/sq was used. After removing the boron or phosphorus glass, the structure was covered with about 1 μm of vapor-deposited oxide. The p-channel devices were then gettered by a 30 min, 1070°C $POCl_3$ heat cycle while the n-channel devices were only subjected to a 15 min, 1000°C dry-nitrogen heat treatment to densify the vapor-deposited oxide. The additional gettering cycle was omitted from the n-channel devices in order to prevent excessive diffusion of the impurities in the source and drain regions. The only gettering on these phosphorus-doped films occurred during the 960°C phosphorus predeposition. Contact cuts were then opened on both types of devices, and they were metallized with electron-gun evaporated aluminum. After the electrodes were defined, the wafers were annealed at 450°C in a 25% hydrogen/75% nitrogen ambient for 30 minutes.

For comparison purposes control samples were fabricated on epitaxial films grown at the same time as the films which were subjected to the electrochemical-etching cycle.

The samples were first tested on a curve tracer to ensure that the devices behaved as MOS transistors and,in some cases,to learn about the location of the flatband voltage. Then the devices were tested as indicated in Fig. 5.4. The voltage across the transistor was observed on a storage oscilloscope since the formation time of the inversion layer was usually of the order of a few tenths of a second to about one minute.

5.4.3 Transient response

The minority-carrier lifetimes observed in the films will be reported and briefly discussed in this section; then other observations made on the deep-depletion structures will be described. The DC characteristics of the devices will be compared to the calculated device characteristics in the following section.

The lifetimes calculated from the observed decay time of the current transient are summarized in Table 5.1. These calculations were performed assuming that only generation in the depletion region was of importance. Each value is the average of several measurements taken on each wafer. In some cases, markedly lower values of decay time were observed at various locations on the wafer, especially near the edges of the wafer where the film tended to be degraded. As can be seen from Table 5.1, the lifetimes in the p-type films appeared to be higher than those observed in the n-type films. While the electron lifetimes in the p-type films were in the range 11-25 μsec, the hole lifetimes in the n-type films ranged from 2-11 μsec. Part of this difference may be related to the stronger gettering treatment given to the p-type samples. Within each series of films, no consistent change in lifetime with varying thickness was observed. This behavior is not unreasonable if we assume that generation at the underlying Si/SiO_2 interface does not contribute significantly to the minority-carrier generation rate. In only one case (2769B) did the depletion region extend completely through the thin film. This wafer will be discussed in more detail below.

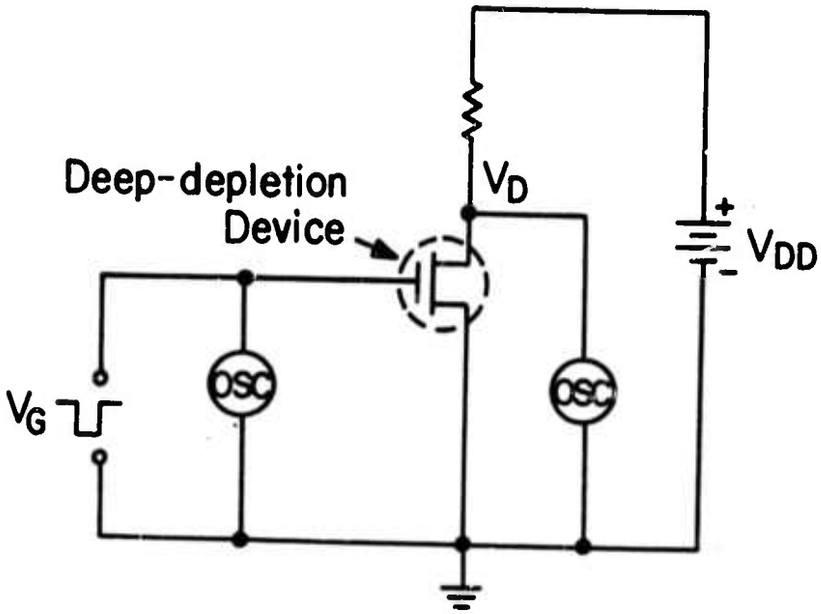

Fig. 5.4. Test circuit for lifetime measurements on n-type thin films. Polarity of battery and pulse generator were reversed for p-type films.

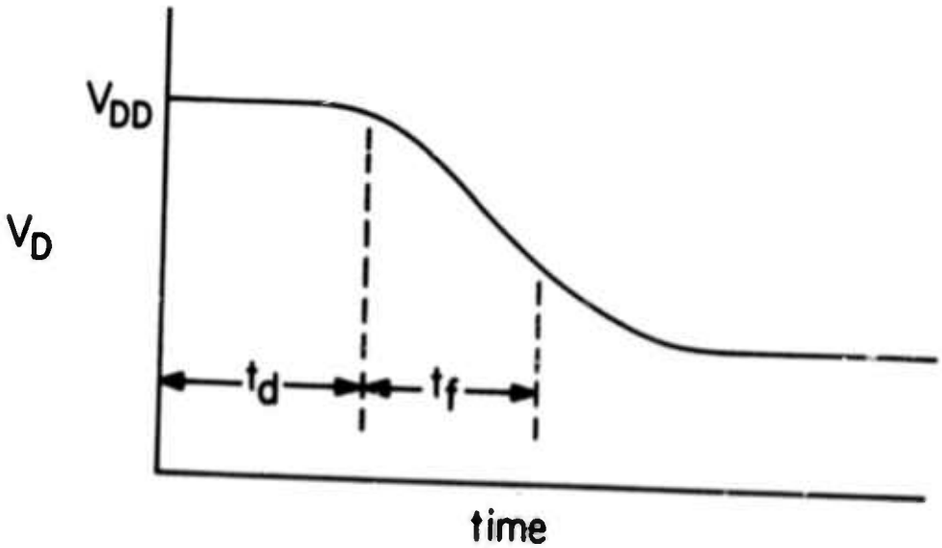

Fig 5.5. Time response of thin film which was completely depleted by gate-voltage pulse.

TABLE 5.1

Lifetime Data--Thin Silicon Films

Run	Wafer	Type	Doping ($10^{15}cm^{-3}$)	t (μm)	t_f (sec)		τ_o (μsec)		Device Run No.
3003	B	p	2.4	EPI	19		119		119
	C		4.1	9.1	3.0		11		119
	G		3.9	7.6	6.3		24		119
	I		3.8	5.5	6.7		26		119
2948	A	p	1.5	EPI	13		130		117
	E		2.1	4.5	2.3		16		117
2979	A	n	1.3	EPI	50		580		115
	B			EPI	40		460		116
					Acc.	Inv.	Acc.	Inv.	
	C			7.0	0.28	0.34	3.2	3.9	115
	E			5.9	0.77	0.97	8.9	11	116
	I			5.3	0.20	0.28	2.3	3.2	115
	G			4.4	0.44	0.52	5.1	6.0	116
	K			3.4	0.20	0.28	2.3	3.2	115
2769	B	n	∿2	∿1	∿2.5		∿19		105

Although the lifetimes in the p-type films were greater than those in the n-type films, the lifetimes in the p-type control wafers were less than those in the n-type control wafers.

The p-type control samples consisted of boron-doped epitaxial films deposited on antimony-doped wafers while the n-type control samples had phosphorus-doped epitaxial films deposited on boron-doped substrates. In both cases, however, the lifetimes in the control samples were several times as long as those in the thin films and may have been controlled by generation in other regions than the depletion region. The possibility of surface generation in these control samples cannot be ruled out. Even if the generation in the control samples was dominated by the upper Si/SiO_2 interface, the significantly longer response time seen in the control samples indicates that surface generation is not the dominant mechanism controlling the response of the thin films. The marked difference between the n-type thin films and the control wafers is especially striking.

In most cases little difference was observed whether the sample was pulsed into deep depletion from accumulation or from inversion. Data are shown for both initial conditions for one set of samples. The small differences seen are probably not significant. These results again indicate that the top Si/SiO_2 interface does not contribute significantly to the observed carrier generation in the thin films.

In order to investigate the source of the carrier generation in more detail, we can apply the analysis of Sec. 5.4.1 to the present results.

One of the n-type films investigated (2769B) was thin enough that the depletion region could extend completely through the film when the MOS transistor was pulsed into deep depletion. The initial n-type epitaxial film on this wafer was about 2.3 μm thick. After the electrochemical etch the film was about 1.8 μm thick, and the final film was about one micron thick after the vapor etch. The phosphorus dopant concentration in a similarly doped epitaxial film deposited on a boron-doped wafer was of the order of 2×10^{15} cm^{-3}.

The time response of the current observed on Wafer 2769B is indicated schematically in Fig. 5.5. During the time t_d the entire film is depleted, and no current can flow from source to drain. After sufficient minority carriers enter the inversion layer, the depletion region starts narrowing, and current is observed. The depletion region then continues narrowing, approaching its equilibrium value with a time constant t_f. Curve-tracer measurements taken with the device strongly illuminated indicated that the onset of strong inversion occurred at a threshold gate voltage $V_T = -4.5$ V. The flatband voltage can then be calculated to be -3.0 V from the dopant concentration and the relation (8)

$$V_T - V_{FB} \simeq 2\,\phi_F - Q_B/C_{ox} = -0.62\text{ V} - 0.85\text{ V} = -1.5\text{ V}, \quad [5.12]$$

and the maximum width of the equilibrium depletion region is found to be 0.68 μm from the relation (9)

$$x_{d\,max} = [4\epsilon_s\,\phi_F/q\,N_D]^{1/2} \quad [5.13]$$

The nonequilibrium depletion region width is calculated from the expression*

$$x_d = \frac{\epsilon_s\,t_{ox}}{\epsilon_{ox}}\left\{\left[1 + \frac{2\,\epsilon_{ox}^2}{t_{ox}^2\,\epsilon_s\,q\,N_D}\,|V_G - V_{FB}|\right]^{1/2} - 1\right\} \quad [5.14]$$

$$= 0.42\left\{\left[1 + 3.68\,|V_G - V_{FB}|\right]^{1/2} - 1\right\}\ \mu\text{m},$$

* Derived in Sec. 5.4.4.

using 0.14 μm for the thickness of the gate oxide. The delay time t_d for a typical device on this wafer was found to be zero at a gate voltage of about -6.0 V and to increase as the magnitude of the gate voltage increased. The depletion layer width corresponding to the onset of complete film depletion is then calculated to be 1.04 μm from Eq. [5.14].

When a -15.8 V gate-voltage pulse was applied to this device, a delay time of about 0.8 sec was observed before any source-drain conduction could be observed. If the film were thick enough, the depletion region corresponding to this -15.8 V gate voltage would be about 2.50 μm. Since the film is thinner than this value, however, the charge corresponding to the additional 1.46 μm thickness must be generated before a conducting channel can form. This charge is given by

$$\frac{\Delta Q}{q} = N_D \, \Delta x_d = 2.92 \times 10^{11} \text{ cm}^{-2} = G \;\; t_d, \qquad [5.15]$$

where Δx_d is the difference between the depletion region width corresponding to -15.8 V and that corresponding to -6.0 V. If generation at the top Si/SiO_2 interface is neglected, the generation rate G corresponds to the generation rate in the depleted film and that at the exposed Si/SiO_2 interface beneath the film.

$$G = G_1 + G_5 = \frac{n_i}{\tau_o} (x_f - x_{de}) + n_i s_o', \qquad [5.16]$$

where x_f is the film thickness. Using Eq. [5.16] in Eq. [5.15], we find that

$$s_o' + (x_f - x_{de})/\tau_o = \Delta Q / n_i t_d = 24.3 \text{ cm/sec.} \qquad [5.17]$$

After the conducting channel started to form, the current was observed to approach its final value with a time constant t_f of about 2.5 sec. If this decay time is attributed to generation in the depletion region only, the corresponding lifetime is found from Eq. [5.7] to be 18.7 μsec. If the generation rate $G_{3,4}$ at the bottom interface and in the neutral region is still significant even after the interface is shielded, this value of 18.7 μsec is a lower bound on the lifetime in the film. Using 18.7 μsec for the lifetime, however, we find the value of surface recombination velocity at the bottom Si/SiO_2 interface to be $s_o' = 24 - 8 = 16$ cm/sec. Since the second term is small, the assumption that $G_{3,4}$ is negligible does not seriously affect the calculated value of s_o'.

Although this number for s_o' is reasonable, its value is somewhat uncertain since some of the parameters used are not accurately known. It does indicate, however, that the surface recombination velocity at the back surface is not abnormally large and should not seriously degrade device performance, especially if it can be further reduced by additional annealing treatments. This wafer was subjected to one additional processing step during the film fabrication, however. After growth of the initial epitaxial film, the wafer was oxidized in the normal manner. This thermally grown oxide was then covered by a layer of vapor-deposited oxide, masked, and subjected to a phosphorus predeposition. The phosphorus glass was removed by a dilute HF etch, and the wafer was covered with more vapor-deposited oxide before the thick film of polycrystalline silicon was subsequently deposited. The effect of this additional treatment on the surface recombination velocity is unknown but may not be especially important since the wafer was subjected to many subsequent, high-temperature heat cycles in various ambients.

The value of s_o' found from Wafer 2769B can be used to estimate the importance of the generation mechanism $G_{3,4}$ in the thicker films. Using reasonable numbers, we find that $G_{3,4}$ is of the order of 10^7 or less while G_1 is of the order of 10^{10} or greater so that the neglect of $G_{3,4}$ is certainly justified for the thicker films and even for the thinner film over most of the decay time.

Since comparison with the epitaxial control samples shows that G_2 may be neglected and the arguments above indicate that $G_{3,4}$ is not significant, we may conclude that generation within the depletion region dominates the observed increase of the source-drain conductance in the electrochemically etched thin films. Consequently, the values of lifetime computed for these electrochemically etched films should be an accurate indication of the minority-carrier generation lifetime.

5.4.4 DC characteristics of deep-depletion devices

The source-drain characteristics of the deep-depletion MOS transistors fabricated in the thin films were briefly examined and compared to those of devices fabricated in the epitaxial control wafers to identify any major differences. The devices were measured in the dark on a curve tracer with a small applied drain voltage in order to keep the device in the linear region and, therefore, simplify the analysis. In the linear region the drain current is given by

$$I_D = \frac{Z}{L} \mu Q V_D, \qquad [5.18]$$

where Q is the mobile charge in the conducting channel. For an n-type semiconductor

$$Q = -q N_D x_f + \Delta Q, \qquad [5.19]$$

where the first term represents the mobile charge for flatband conditions and ΔQ is the charge induced by the gate voltage. When the device is biased to create an accumulation region, the gate voltage induces carriers close to the Si/SiO_2 interface so that ΔQ is given by $\Delta Q = -C_{ox} (V_G - V_{FB})$, and the drain current becomes

$$I_D = -\frac{Z}{L} V_D \left[\mu_B q N_D x_f + \mu_{FE} C_{ox} (V_G - V_{FB})\right], \qquad [5.20]$$

where μ_B is the mobility of the carriers away from the surface of the film and μ_{FE} is the mobility of the induced carriers close to the silicon surface.

When the device is biased to deplete the surface, the conducting channel will narrow, and the current will decrease. The number of carriers removed from the channel by the applied gate voltage can be found by considering the widening of the depletion region as the applied gate voltage is increased in magnitude. The applied gate voltage appears partially across the gate oxide and partially across the depletion region induced in the semiconductor:

$$-(V_G - V_{FB}) = E_{ox} t_{ox} + \phi_s, \qquad [5.21]$$

where the semiconductor surface potential ϕ_s is related to the depletion-region width through the relation

$$\phi_s = q N_D x_d^2 / 2\varepsilon_s. \qquad [5.22]$$

The electric field in the oxide is related to the depletion-region width by the constancy of the normal component of the displacement and by Gauss' law:

$$\varepsilon_{ox} E_{ox} = \varepsilon_s E_s = q N_D x_d, \qquad [5.23]$$

where we have assumed that no minority carriers will be generated during the time that the device is tested; i.e., deep-depletion conditions prevail. Equations [5.21], [5.22], and [5.23] may be combined to produce an expression relating the gate voltage and the depletion-region width:

$$-(V_G - V_{FB}) = \frac{q\, N_D\, x_d\, t_{ox}}{\varepsilon_{ox}} + \frac{q\, N_D\, x_d^{\,2}}{2\, \varepsilon_s}. \qquad [5.24]$$

Solving this expression for the depletion-region width, we find

$$x_d = \frac{\varepsilon_s\, t_{ox}}{\varepsilon_{ox}} \left\{ \left[1 - \frac{2\varepsilon_{ox}^{\,2}}{t_{ox}^{\,2}\, \varepsilon_s\, q\, N_D} (V_G - V_{FB}) \right]^{1/2} - 1 \right\}. \qquad [5.25]$$

The mobile charge which is repelled from the conducting channel is then given by

$$-\Delta Q = -q\, N_D\, x_d = -\frac{q\, N_D\, t_{ox}\, \varepsilon_s}{\varepsilon_{ox}} \left\{ \left[1 - \frac{2\varepsilon_{ox}^{\,2}}{q\, N_D\, \varepsilon_s\, t_{ox}^{\,2}} (V_G - V_{FB}) \right]^{1/2} - 1 \right\}, \qquad [5.26]$$

and the drain current is given by

$$I_D = \frac{Z}{L} \mu_B\, V_D\, [-q\, N_D\, x_f + \Delta Q]. \qquad [5.27]$$

From Eqs. [5.26] and [5.27] we see that the reduction in the magnitude of the current will vary approximately as $V_G^{1/2}$ at large gate voltages.

In order to compare the expected device behavior with that observed, some knowledge of the flatband voltage is necessary. Under

strong illumination, minority carriers can be generated rapidly, and an inversion layer will form. Once the inversion layer has formed, the current will no longer decrease in magnitude with additional applied gate voltage. Consequently, the onset of inversion may be easily observed from the curve-tracer measurements. This threshold voltage may then be related to the flatband voltage through the relation (8)

$$V_{FB} = V_T - 2\phi_F + Q_B/C_{ox}. \qquad [5.28]$$

The drain current was observed on a curve tracer in the dark at a low drain voltage as the gate voltage was varied. The sweep time of the curve tracer was less than the formation time of the inversion layer for most of the devices tested so the devices were observed in the deep-depletion region, and the observed characteristics may be compared to those expected from Eqs. [5.20], [5.26], and [5.27]. Figure 5.6 shows the I_D - V_G characteristics for devices fabricated in a series of n-type films (2979) of various thicknesses. The average inversion voltage was found to be -5.3 V so that the flatband voltage was V_{FB} = -5.3 + 0.59 + 0.70 = -4.0 V. These measurements were taken with the polycrystalline-silicon substrate grounded to the source electrode.

From Fig. 5.6 we see that the change in drain current with applied gate voltage was generally similar for the electrochemically etched films and the control samples. However, for the larger depleting voltages, the change in drain current was slightly less in the thin films than in the control samples. This difference was more pronounced in the thinner films and may be explained by noting that the depletion layer may occupy a significant fraction of the film thickness in the thinner films. In this case the underlying surface will start to affect the device behavior. An accumulation layer near this bottom interface, especially, would cause the conducting channel to be harder to deplete.

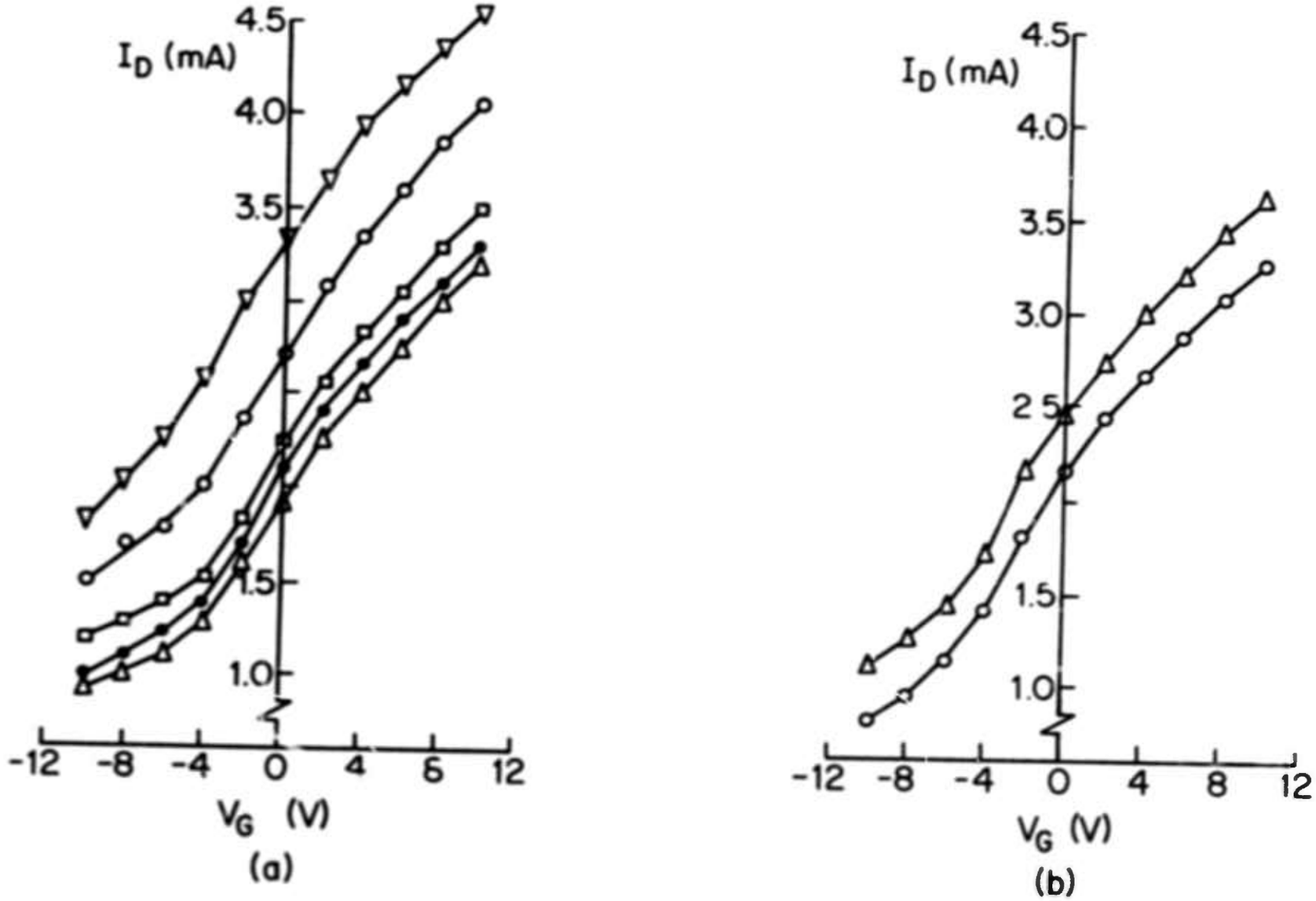

Fig. 5.6. Drain current as a function of gate voltage for deep-depletion MOS transistors fabricated in n-type films with V_D = 0.5 V and substrate grounded; (a) electrochemically etched films of several thicknesses; (b) epitaxial control films on single-crystal wafers.

Figure 5.7 shows the I_D - V_G characteristics observed on Wafer 2979G when the gate voltage was applied to either the gate electrode or the polycrystalline-silicon substrate with the other electrode grounded or when the gate voltage was applied simultaneously to both electrodes. The latter curve indicates that the entire film can be depleted of mobile carriers.

From these measurements we may conclude that the deep-depletion MOS structure fabricated in the thin film generally behaves as expected from theoretical considerations but that some differences may begin to appear as the depletion layer approaches the bottom of the film.

5.5 Summary

The results of minority-carrier-lifetime studies in the thin silicon films formed by electrochemical etching have been reported in this section. Values of the lifetime have been determined both by injection of carriers across p-n junctions and by generation near the surfaces of MOS structures. Injection of carriers across p-n junctions indicated a lower bound on the lifetime of a few microseconds while injection of carriers into the emitter-base junction of bipolar transistors indicated lifetimes of the order of 10 μsec. More detailed investigation of deep-depletion MOS structures also revealed lifetimes of the order of 10 μsec. While the values for electrons were somewhat higher than those for holes in the MOS structures, the devices in which the electron lifetimes were measured were more strongly gettered. Further gettering may increase the lifetimes to somewhat higher values. Measurement of the DC characteristics of the deep-depletion devices fabricated in the thin films indicated few differences from those fabricated in the control wafers, at least until the depletion region approached the bottom of the silicon film. In particular, the mobility of electrons appeared to be similar in the thin films and in the control samples, suggesting that the Hall measurements on the n-type films (Sec. 4.3.2) were influenced by surface accumulation layers rather than by voids in the films.

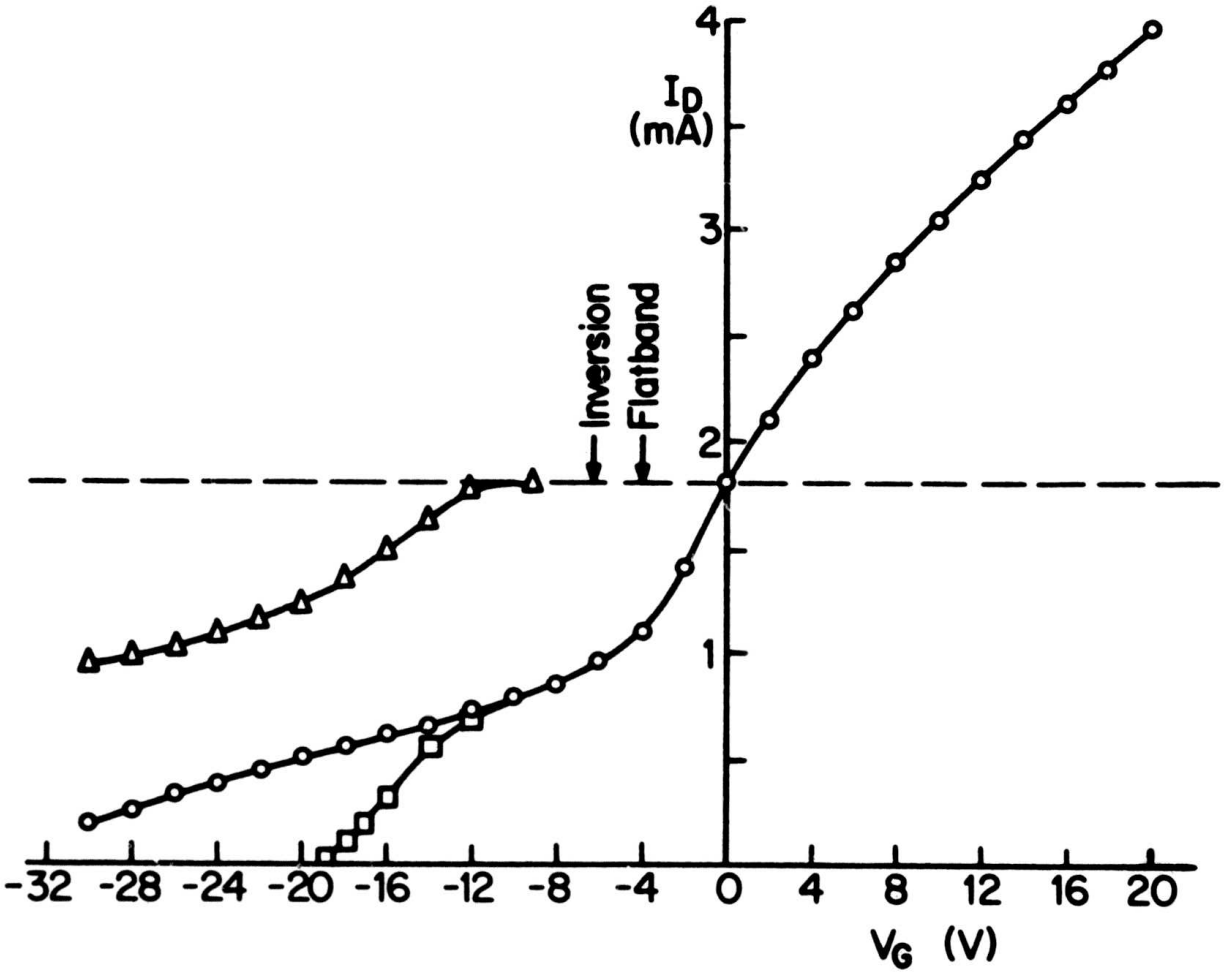

Fig. 5.7. Drain current as a function of gate voltage for deep-depletion MOS transistor fabricated in 4.4 μm-thick, n-type, electrochemically etched film with V_D = 0.5 V; ○ gate voltage on gate electrode, substrate grounded; △ gate voltage on substrate, gate electrode grounded; □ gate voltage on both gate electrode and substrate.

The lifetimes found in this investigation have significant implications for the devices which can be constructed in the films. The lifetimes have been found to be long enough so that the characteristics of junction devices will not be degraded. In particular, high-quality bipolar transistors can be fabricated in the thin films formed by electrochemical etching. This is to be contrasted to the situation for the alternative silicon-on-sapphire system. Lifetimes of about 10 nsec are the maximum which can be achieved in these heteroepitaxial films, even after many years of effort (10,11,12). Therefore, the fabrication of bipolar transistors in silicon-on-sapphire films is difficult, and high-quality bipolar transistors cannot be obtained. Low values of lifetime in the silicon-on-sapphire films also degrade the characteristics of p-n junctions, such as the source and drain junctions in MOS circuitry. No difficulty has been experienced obtaining hard p-n junctions in the films formed by electrochemical etching. The markedly higher lifetime in the present system is one of its major advantages over the silicon-on-sapphire system.

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6. DIFFUSION INTO THIN SINGLE-CRYSTAL SILICON FILMS

6.1 Introduction

A series of experiments was conducted in order to determine if the diffusion of dopant impurities into the thin films formed by electrochemical etching differs from that in bulk wafers. Both boron and phosphorus were considered. Because of the single-crystal nature of these films, no gross differences were expected, although some small differences could be caused by stress in the films. In order to isolate differences in diffusion from other effects, vapor-deposited, doped oxides were used as the diffusion sources. The use of these doped oxides allowed direct comparison of diffusions into the thin films and into bulk control wafers since the amount of dopant which enters the silicon from the doped oxide is primarily controlled by diffusion in the oxide while the diffusion depth is controlled by the diffusivity of the dopant in the silicon (1).

6.2 Experimental Method

Impurities were diffused into (111)-oriented silicon films and into (111)-oriented bulk control wafers doped to approximately the same concentration as the films. After the films were formed by electrochemical etching, about 2 μm was removed from each sample by vapor etching in order to avoid possible effects of a surface region with a different dopant concentration than the remainder of the film. The doped oxides were deposited by oxidation of silane and either diborane or phosphine at a substrate temperature of approximately 400°C. Silicon films approximately 6-7 μm thick were used, and the diffusions were performed in a dry nitrogen ambient. Each thin-film sample was placed in the diffusion furnace between two similarly doped control samples of approximately the same size. A diffusion temperature of 1100°C was generally used since diffusion at this temperature has been found to be more reproducible than diffusion at lower temperatures (2).

Surface concentrations of the dopant atoms were calculated by reference to previous work on diffusion from boron-doped oxides (1) and phosphorus-doped oxides (3). The boron-doped oxide contained about 5% B_2O_3 or 2×10^{21} cm^{-3} boron atoms, which should produce a surface concentration of about 5×10^{19} cm^{-3} boron atoms in the silicon. The

phosphorus-doped oxide contained about 10% P_2O_5 or 2×10^{21} phosphorus atoms so that the surface concentration in the silicon was about 8×10^{19} cm^{-3}.

The diffusion times were chosen so that the conductance and junction depth of the diffused layer could be plotted as functions of the square root of the diffusion time for both the single-crystal films and the control samples. As discussed by Barry and Olofsen (1), this method of presentation allows ready calculation of the diffusivity of the dopant impurity in the films and in the contol samples.

After diffusion the sheet resistivity was measured with a four-point probe in several spots on each sample. Junction depths were measured by optical interferometric techniques after delineation by grooving and staining with a nitric-hydroflouric acid solution (70% HNO_3: 49% HF: H_2O = 0.1: 50:50 by volume).

6.3 Experimental Results

The I/V measured after the boron and phosphorus diffusions into n-type and p-type samples, respectively, are shown in Figs. 6.1 and 6.2 as functions of the square root of the diffusion time. In both cases the data fit a linear relationship fairly well although the agreement is better for the phosphorus diffusion into p-type samples than for boron in n-type samples. The deviation from a linear relationship seen in the latter case may be similar to that seen by Barry and Olofsen at high boron surface concentrations ($C_s > 10^{20}/cm^3$). Figures 6.3 and 6.4 are plots of the I/V for the thin films as functions of the average I/V seen in the bulk wafers diffused at the same time. In both cases the data points lie above a line with unity slope, indicating a reasonably consistent tendency for somewhat higher I/V in the thin films than in the bulk wafers. This behavior was not always seen. In some cases the value in the thin film was the same as that in the bulk wafer, but in no case was the value in the thin film less than that in the bulk wafer. The dashed lines in Figs. 6.3 and 6.4 indicate that the I/V was approximately 10 percent higher in the thin films for the boron diffusions and about 6 percent higher for the phosphorus diffusions.

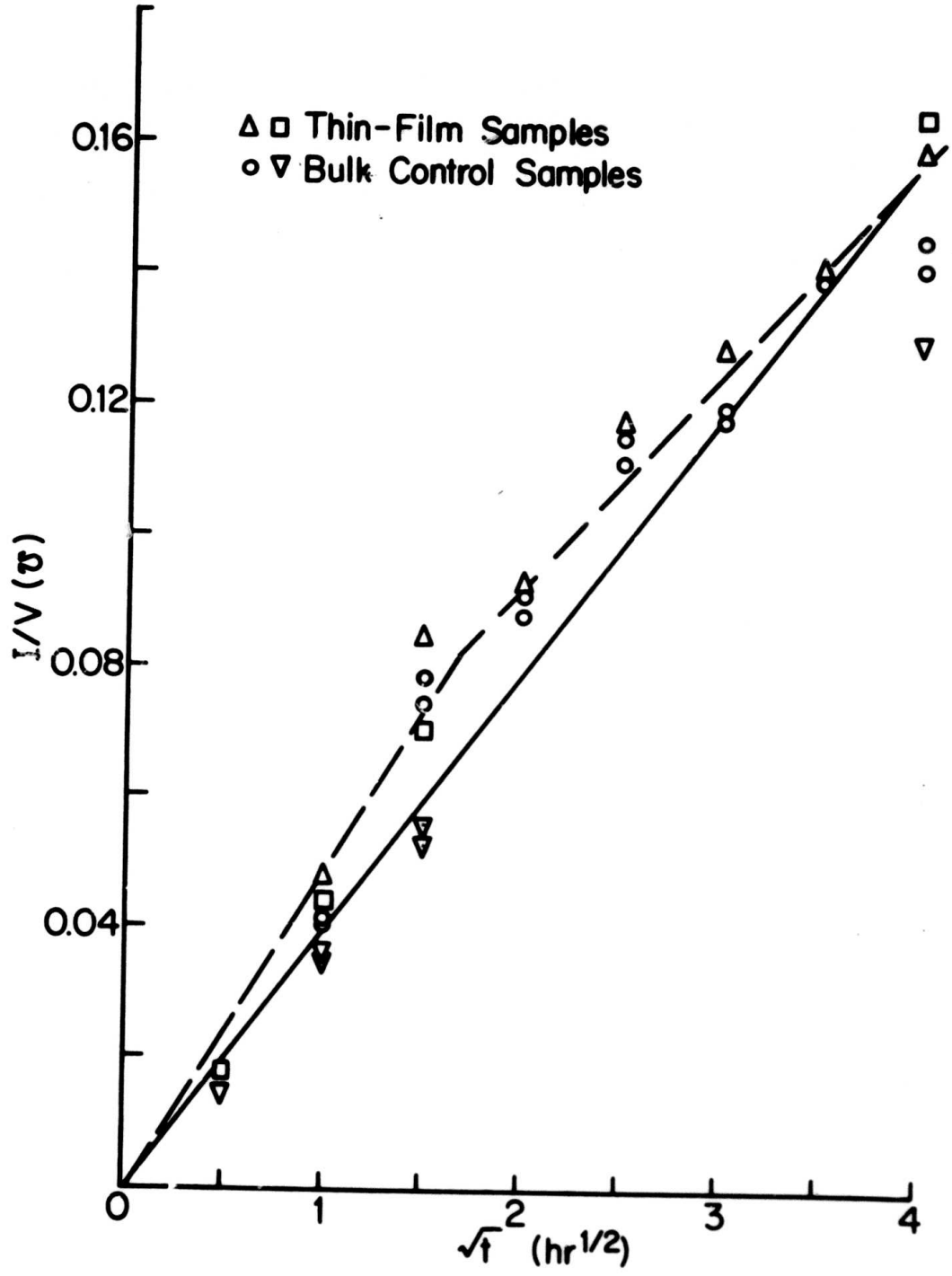

Fig. 6.1. I/V after boron diffusion into n-type sample as a function of square root of diffusion time.

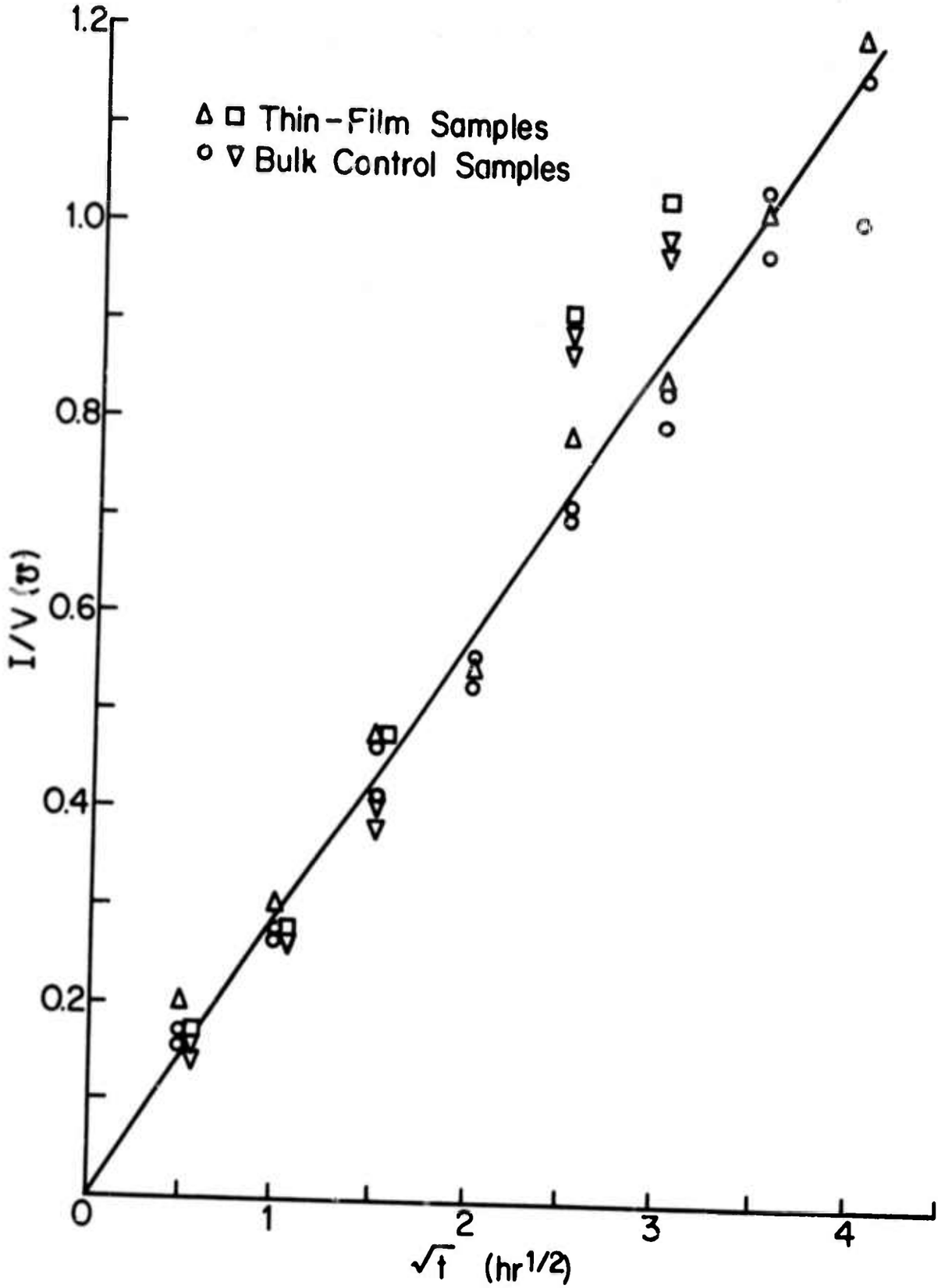

Fig. 6.2. I/V after phosphorus diffusion into p-type sample as a function of square root of diffusion time.

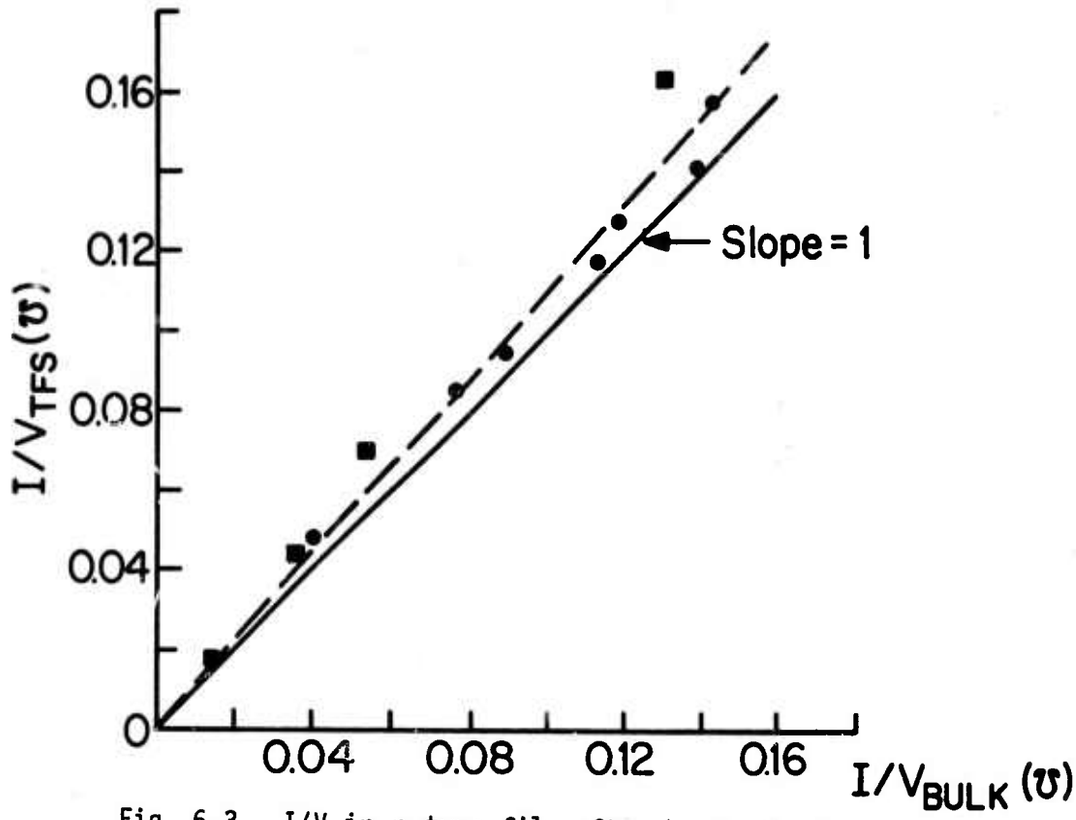

Fig. 6.3. I/V in n-type film after boron diffusion as a function of I/V in corresponding bulk wafer.

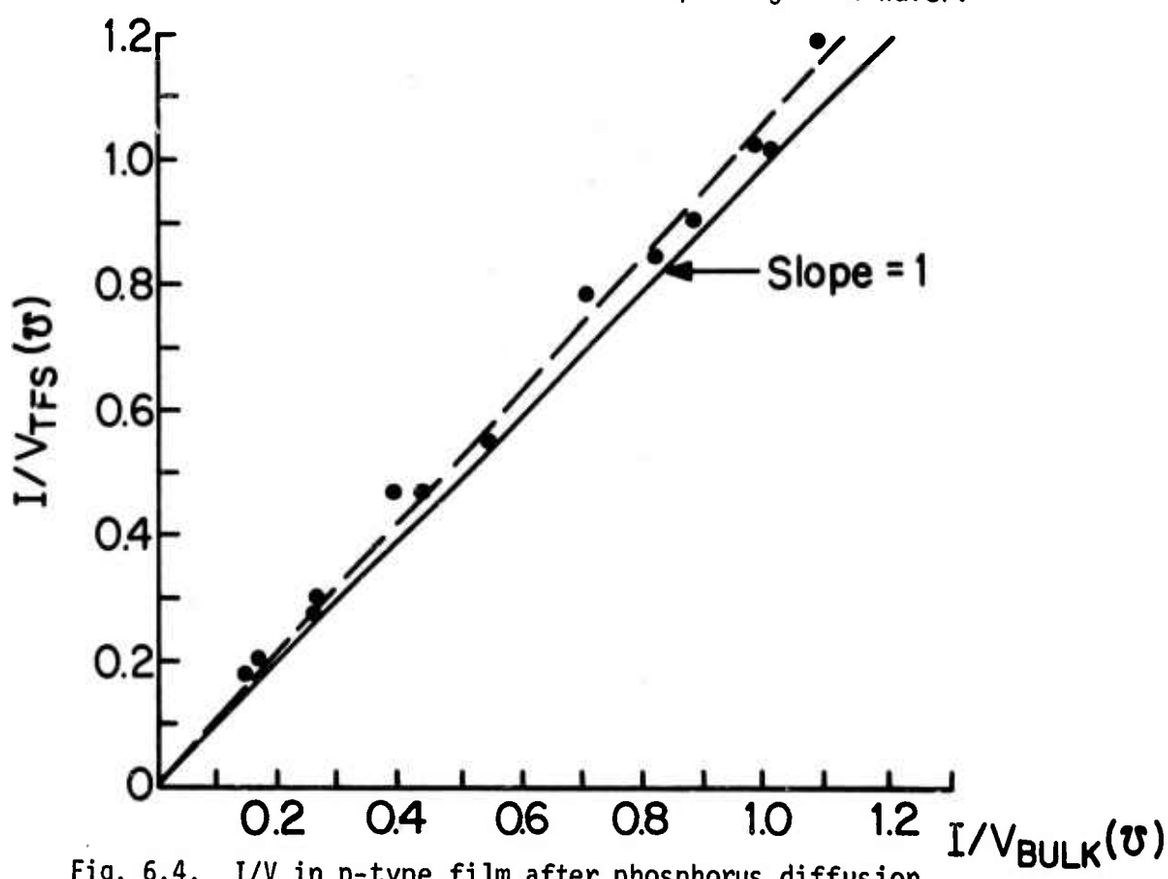

Fig. 6.4. I/V in p-type film after phosphorus diffusion as a function of I/V in corresponding bulk wafer.

The measured values of junction depth were also plotted as functions of the square root of the diffusion time with reasonable fit to a linear relationship. Sharp, well-defined junctions were obtained in the case of phosphorus diffusions into p-type films while some difficulty was encountered obtaining sharp stain lines on some of the n-type films after boron diffusion. The data are only shown for series of samples which exhibited well-defined junctions [Figs. 6.5 and 6.6].

Plots of the junction depths in the thin films as functions of those in the bulk wafers are shown in Figs. 6.7 and 6.8. In both cases the junction depths are the same in the thin films and in the bulk wafers for shallower diffusions ($x_j < 4$ μm). For the longer phosphorus diffusions, however, the junction depth in the thin films becomes appreciably less than that in the bulk wafers. This trend was seen in three separate sets of diffusions and is probably not a statistical error. The dashed line in Fig. 6.8 indicates that the diffusion depths are approximately 8 percent less in the thin films than in the bulk control wafers.

6.4 Discussion

The data obtained from these experiments may be interpreted on the basis of the theory developed by Barry and Olofsen (1), which relates the diffusivity D, and the segregation coefficient, m, of the dopant in the silicon to the measured quantities, I/V and x_j. These relationships are expressed in the most useful form in Eqs. [20], [23] and [28] of Ref. (1) and are repeated below:

$$I/V = 8.15 \times 10^{-23}\, \bar{\mu}\, C_s \sqrt{D_2 t}\,, \qquad [6.1]$$

$$\sqrt{D_2} = \frac{d(x_j)/d(\sqrt{t})}{2 \arg \operatorname{erfc} (C_b/C_s)}\,, \qquad [6.2]$$

and

$$m = \left[\frac{C_o}{C_s} - \sqrt{D_2/D_1}\right]^{-1}\,, \qquad [6.3]$$

where $\bar{\mu}$ is the mean mobility of carriers in the diffused layer, C_o is the dopant concentration in the oxide, C_s is the surface dopant concen-

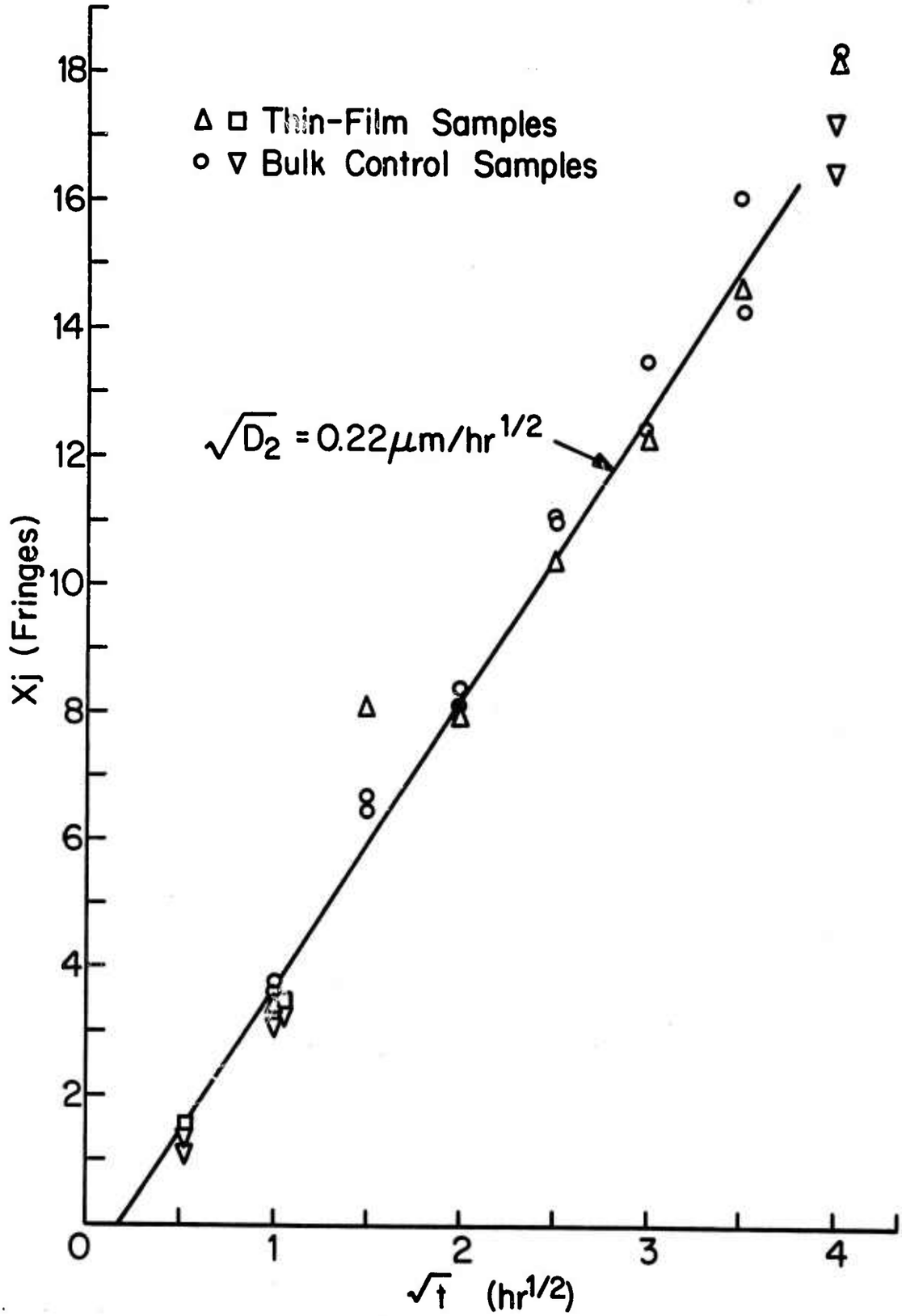

Fig. 6.5. Junction depth after boron diffusion into n-type samples as a function of square root of diffusion time (1 fringe = 2950 Å).

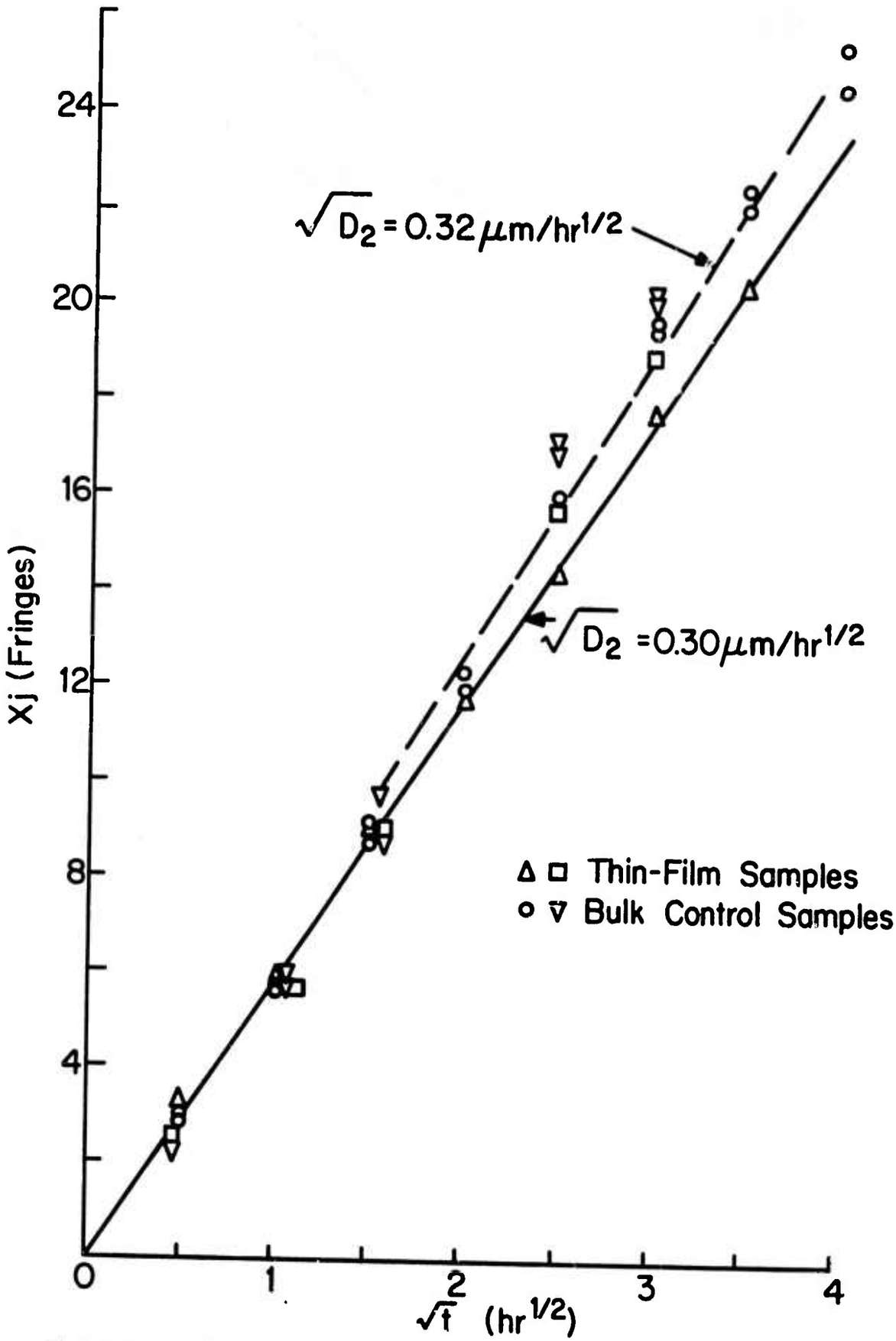

Fig. 6.6. Junction depth after phosphorus diffusion into p-type samples as a function of square root of diffusion time (1 fringe = 2950 Å).

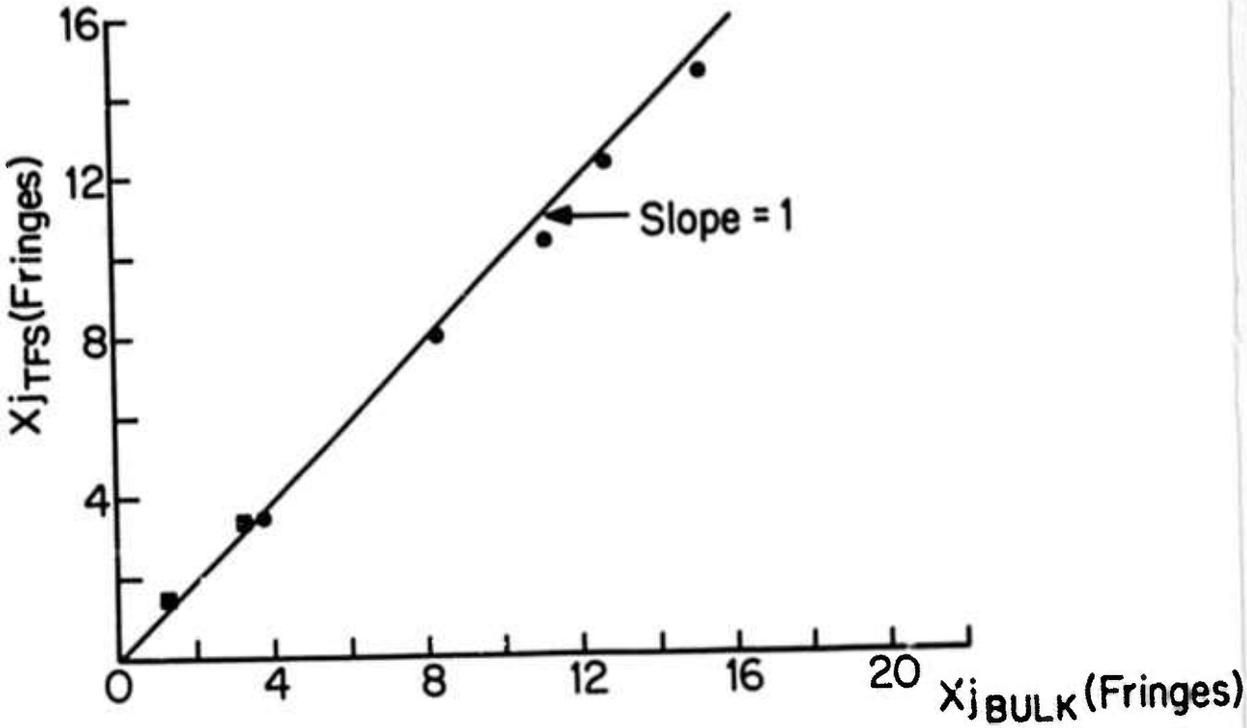

Fig. 6.7. Junction depth in n-type film after boron diffusion as a function of junction depth in corresponding bulk wafer. (1 fringe = 2950 Å).

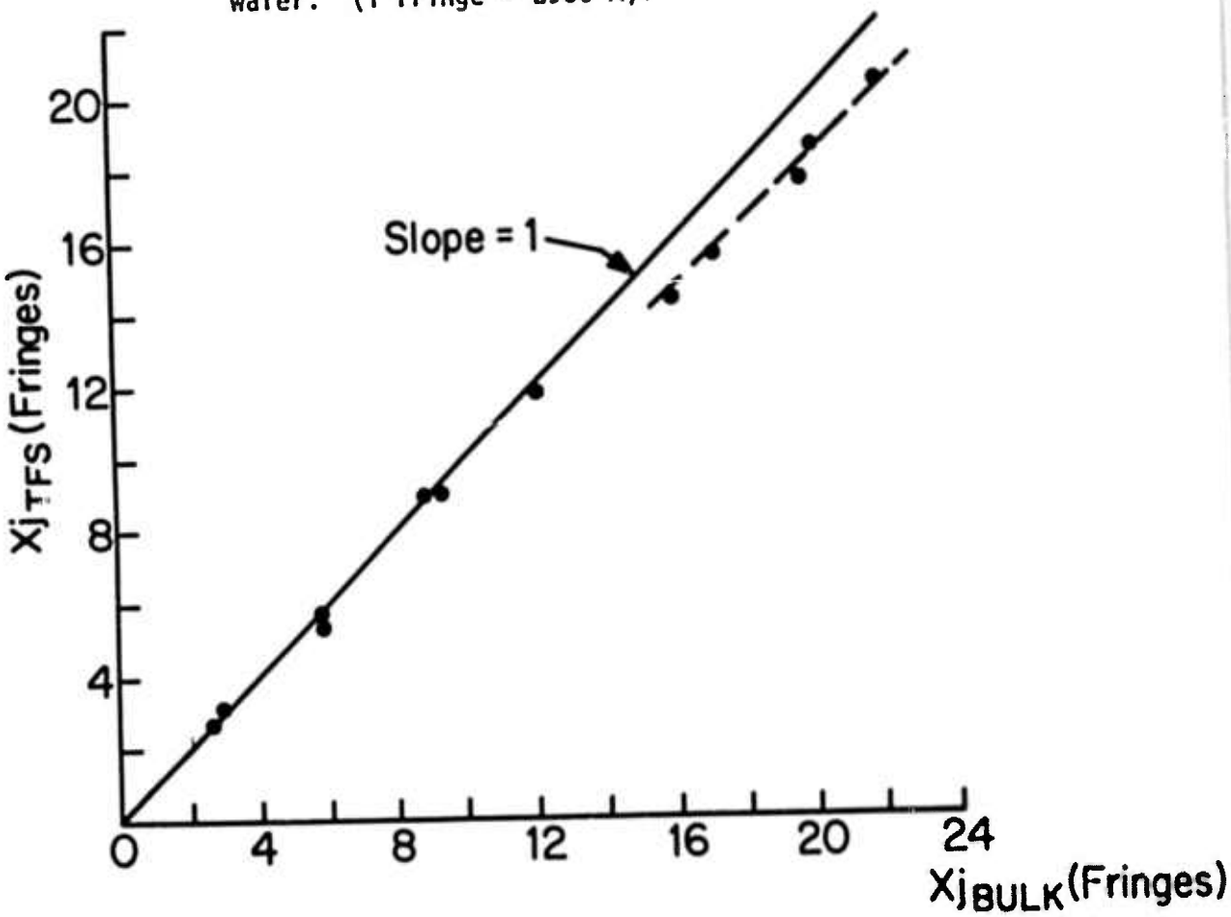

Fig. 6.8. Junction depth in p-type film after phosphorus diffusion as a function of junction depth in corresponding bulk wafer. (1 fringe = 2950 Å).

tration in the silicon, C_b is the background dopant concentration in the silicon, D_1 and D_2 are the diffusivities of the dopant in the oxide and in the silicon, respectively, and m is the segregation coefficient. From Eq. [6.2] and Figs. 6.7 and 6.8, we see that the diffusivities of both phosphorus and boron are the same in the thin film and in the bulk wafers, at least for the shallower diffusions. From Figs. 6.5 and 6.6, $\sqrt{D_2}$ is calculated to be 0.22 $\mu m/hr^{1/2}$ for the boron diffusions and 0.30 $\mu m/hr^{1/2}$ for the shallower phosphorus diffusions, in good agreement with the values obtained by Barry and Olofsen (1) and by Barry (3) under similar conditions. For the deeper phosphorus diffusions, $\sqrt{D_2}$ is best approximated to be 0.32 $\mu m/hr^{1/2}$ in the bulk wafers and 0.30 $\mu m/hr^{1/2}$ in the thin films.

The differences seen in the I/V can be related to the material properties through Eq. [6.1]. These differences must arise from either a greater mobility or a higher surface concentration in the thin films. A higher surface concentration would, in turn, be related to a larger value of the segregation coefficient through Eq. [6.3].

A change in the average value of the mobility might arise from stress effects in the thin films. For current flow parallel to the surface of a (111)-oriented silicon sample (4)

$$\frac{\Delta\rho}{\rho} = \sigma_f \frac{2\pi_{11} + 4\pi_{12} + \pi_{44}}{3} , \qquad [6.4]$$

where ρ is the sample resistivity, σ_f is the stress ($\sigma_f > 0$ for tension), and the π_{ij}'s are the piezoresistance coefficients. In diffused layers, it has been shown (5) that $\pi_{12} \simeq -1/2\ \pi_{11}$ so that $\Delta\rho/\rho \simeq (\pi_{44}/3)\ \sigma_f$. At room temperature, π_{44} for a p-type diffused layer with a surface concentration of 5×10^{19} cm^{-3} in (111)-oriented silicon is about 90×10^{-12} cm^2/dyne while that for an n-type diffused layer is about -12×10^{-12} cm^2/dyne (6). Therefore, the resistivity change should be in the opposite direction and markedly less in n-type diffused layers than in p-type diffused layers. The experimental behavior indicates that the change in sheet resistivity is about the same for both n-type and p-type diffused layers. In addition, stress measurements (Sec. 8) indicate an upper bound of about 5×10^8 dynes/cm^2 on the stress in the thin

films. Consequently, the maximum change in resistivity should be less than about 1.5% in the boron diffused layers in the n-type films and less than about 0.2% in the phosphorus diffused layers in the p-type films. The observed changes are greater than these upper limits; therefore, the differences in I/V between the thin films and the bulk wafers are probably not due solely to straightforward stress effects on the resistivity of the material.

The alternative explanation, a change in the value of the segregation coefficient m, and hence a change in the surface concentration, is therefore more probable. From Eq. [6.1] the change in C_s is proportional to the change in I/V so that a 10% difference in the I/V between the thin film samples and the bulk control wafers would correspond to a 10% difference in C_s. Differentiating Eq. [6.3], we obtain

$$\frac{\Delta m}{m} = m \frac{C_o}{C_s} \frac{\Delta C_s}{C_s} . \qquad [6.5].$$

For the boron diffusions at 1100°C, $C_o/C_s = 40$ and $m \simeq 0.2$ so that a 10% increase in I/V would correspond to an 80% increase in m. Since values of m reported in the literature vary widely, a difference of this magnitude is not improbable. Further measurements on vapor etched and on mechanically polished bulk samples after phosphorus diffusion from doped oxides did not indicate any significant differences, however, so the difference in m between the thin films and the bulk samples cannot be related solely to the vapor-etch treatment given the electrochemically etched films.

Two possible causes of the shallower diffusion depths measured in the thin-film samples than in bulk wafers after the longer phosphorus diffusions should be considered. First, the effect of the lower boundary on the diffusion will be discussed. Since the phosphorus atoms only have a finite thickness of silicon into which to diffuse, the boundary condition of the diffusion equation will be different than that usually encountered. Since the impurities cannot diffuse deep into the silicon as in the bulk wafers, they will eventually start to pile up near the bottom interface, and the impurity gradient will decrease. The

remainder of the diffusing impurities will see a reduced driving force for diffusion so that the diffusion will proceed at a slower rate when the junction approaches the bottom surface of the silicon film. In the case of the thin films, the observed deviation from the behavior in the bulk samples became obvious at a junction depth of about 4.5 μm, which corresponded to $\sqrt{Dt} \approx 0.85$ μm. At a depth of 6 μm an erfc distribution would indicate a concentration of $7 \times 10^{-7}\ C_s = 6 \times 10^{13}\ cm^{-3}$ for a surface concentration of $8 \times 10^{19}\ cm^{-3}$. The quantity of impurities penetrating beyond 6 μm should be only $1.4 \times 10^{9}/cm^{2}$. This small number indicates that little diffusing impurity has reached the back of a 6 μm-thick film when the anomaly begins to appear, so that the driving force of the diffusion should not be appreciably changed.

The second and more likely cause of the anomaly is related to differences in the properties of the silicon film near the bottom surface, including the possibility of a stressed layer near the Si/SiO_2 interface. The precipitation of impurities on dislocations near the bottom of the silicon film is also possible.

6.5 Conclusion

From these measurements we may conclude that, to first order, the diffusion characteristics of dopant impurities are similar in the thin films and in bulk wafers. Possible second-order effects include slightly higher sheet conductivities in the thin films than in bulk control wafers and slightly shallower diffusion of phosphorus into p-type thin films than into bulk control wafers.

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7. OXIDATION OF THIN SINGLE-CRYSTAL SILICON FILMS

In order to find any difference in the oxidation rate of the thin films from that of bulk silicon wafers, films were oxidized together with bulk control wafers. Oxidation conditions which were strongly influenced by the surface reaction rate were generally used rather than conditions controlled by the diffusion of oxygen through the already formed oxide since any differences caused by the thin-film structure would be most easily observed in the former case. Wafers were oxidized at 920°C in both dry oxygen and steam* ambients. More consistent results were obtained in the former case since dry oxidation is generally easier to control than is steam oxidation. In all cases lightly doped samples 6-7 μm thick were used. The thin-film sample was placed in the oxidation furnace between two similarly doped bulk control samples of approximately the same size. The wafers were allowed to heat in dry nitrogen for five minutes before the oxidizing species was introduced into the oxidation furnace, and a five minute post-purge in dry nitrogen was also used. After the oxidations were completed, the oxide thickness was measured with an ellipsometer at the center of each sample. Thin-film samples which were not oxidized were also measured with the ellipsometer to confirm that the light (λ = 6328 Å) did not penetrate through the silicon film to the underlying oxide layer and invalidate the results of the ellipsometer measurements. Readings taken on these unoxidized samples indicated an oxide thickness of about 10 Å, confirming that the measurements on the thin films were valid.

The oxide thicknesses and oxidation times are summarized in Table 7.1 along with the percentage deviation of the oxide thickness on the thin film from the average of those on the two control samples oxidized at the same time. In most cases the oxide thickness deviation was less than one percent, indicating that the oxidation rate of the thin-film

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* Oxygen bubbled through 97°C water.

TABLE 7.1

OXIDATION OF THIN SILICON FILMS

RUN	AMBIENT	TIME (HRS)	BULK SAMPLES			THIN-FILM SAMPLE	DIFFERENCE	
			#1 (Å)	#3 (Å)	AVG. (Å)	(Å)	(Å)	%
D30	DRY O_2	2.0	570	575	573	570	3	0.5
D31	"	4.0	885	860	873	870	3	0.3
D32	"	8.0	1375	1420	1398	1365	33	2.4
D3	STEAM	0.25	905	905	905	910	5	0.6
D4	"	0.50	1620	1630	1625	1625	0	0
D5	"	1.0	2560	2620	2590	2570	20	0.8
D6	"	2.0	4170	4205	4188	4152	36	0.9
D37	"	2.0	4020	4070	4045	4035	10	0.2
D7	"	4.0	6320	6340	6330	6175	155	2.5
D38	"	4.0	6200	6325	6260	6215	45	0.7

samples does not differ to any noticeable degree from the oxidation rate of bulk silicon wafers. For comparison, the oxidation rate of (100)-oriented, single-crystal silicon will differ from that of (111)-oriented, single-crystal silicon by more than 30 percent under oxidation conditions similar to those used in the present experiments.

8. STRESS IN THIN SILICON FILMS

8.1 Introduction

An indication of the magnitude of the stress in the thin silicon films is necessary in order to determine if the properties of devices subsequently fabricated in these films will be significantly degraded by the residual stress. In order to obtain a measure of this stress, the lattice parameter of the film has been measured by X-ray diffraction. A significant amount of stress should cause the lattice parameter to depart markedly from that of bulk silicon.

8.2 Experimental Method

A General Electric XRD-5 diffractometer was used, generally with Mo radiation. This relatively hard radiation was employed so that many X-ray peaks could be observed, and the lattice parameter could be determined more accurately. The angles 2 θ corresponding to several of the peaks were determined for the $K_{\alpha 1}$, $K_{\alpha 2}$ and K_{β} lines by averaging the values at half the peak intensity. The angles 2 θ varied from about 35° for the (333) K_{β} peak to about 130° for the (888) K_{α} peak for (111)-oriented samples. Values of the apparent lattice parameter were calculated for each of the peaks from the formula

$$a_o = \frac{\lambda\sqrt{h^2 + k^2 + \ell^2}}{2 \sin \theta} , \qquad [8.1]$$

and plotted versus a Nelson-Riley function (1):

$$\frac{1}{2} \left(\frac{\cos^2\theta}{\sin \theta} + \frac{\cos^2\theta}{\theta}\right) . \qquad [8.2]$$

The zero-intercept of the least-squares fit to this plot then yielded the corrected lattice parameter. The use of this intercept minimizes the instrumental and other experimental errors (1). A typical set of data is shown in Fig. 8.1.

In order to indicate the accuracy of the technique, lightly and heavily doped, bulk silicon wafers were measured in addition to the thin

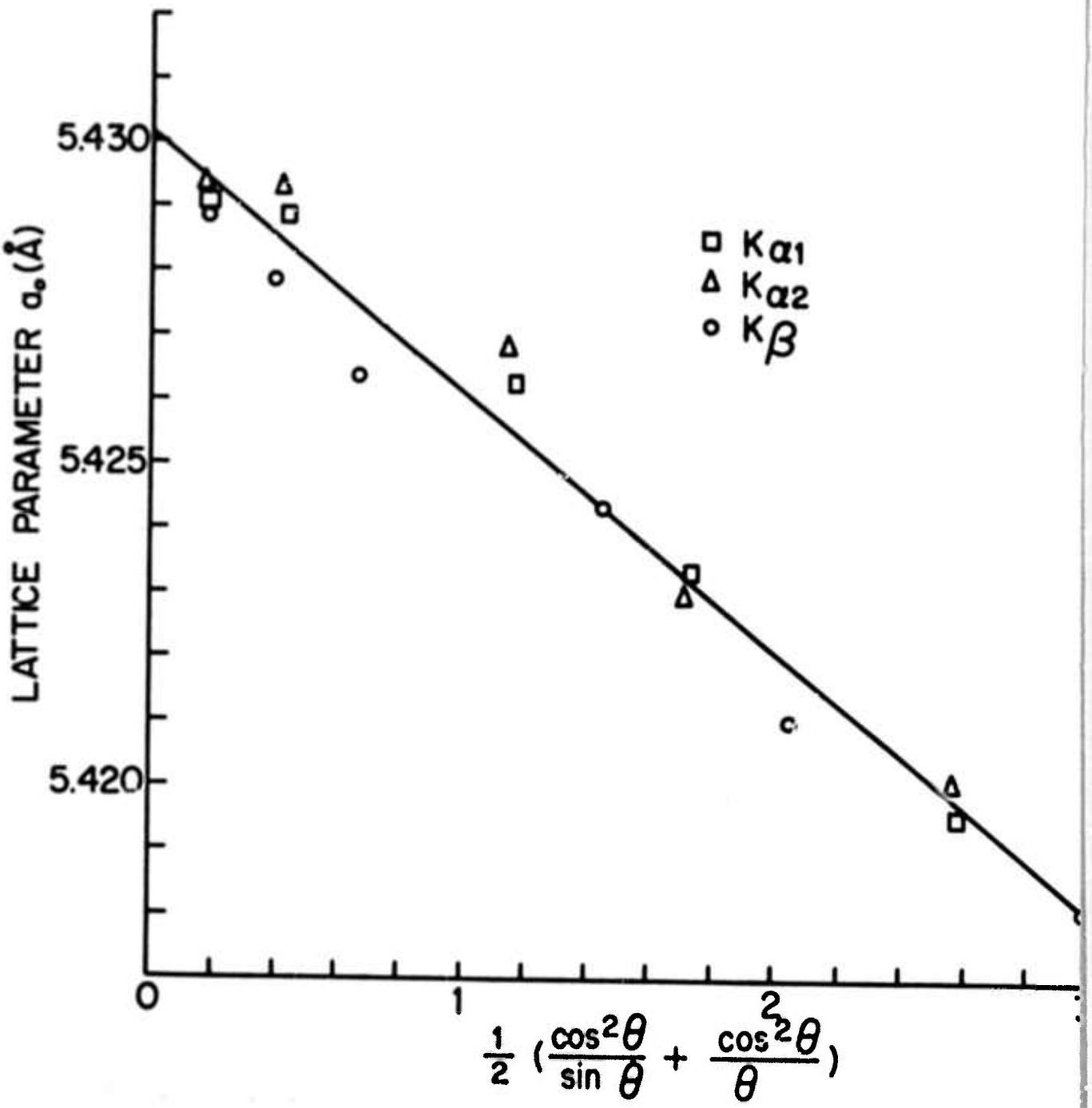

Fig. 8.1. Plot of lattice parameter vs. Nelson-Riley function for p^+ bulk wafer (sample 7); Mo radiation.

films. Commercially prepared silicon films deposited on sapphire substrates were also examined for comparison purposes.

8.3 Experimental Results

The experimentally determined value of the lattice parameter is indicated in Table 8.1 for each of the samples measured. Samples 7, 8 and 10 are bulk, single-crystal wafers with (111)-orientation. The heavily doped samples (7 and 8) were about 260 μm thick while the lightly doped sample was a 3 mm-thick slice of high-quality LOPEX silicon from Texas Instruments. The value of 5.4308 Å measured on the LOPEX crystal is close to the published value of 5.4307 Å (2) for the lattice parameter of lightly doped silicon. (The change in lattice parameter due to the 5×10^{15} cm^{-3} boron atoms in this sample should be about 6×10^{-8} Å and would not be detected by the measurements.) Subsequent data will be compared to the value 5.4308 Å found in this experiment in order to minimize errors due to instrumental and procedural differences between the present study and published investigations.

The value of lattice parameter found for the heavily arsenic-doped n^+ sample was identical to that found for the LOPEX crystal. Since the radii of silicon and arsenic match very closely (2) a dopant concentration of 3×10^{19} cm^{-3} arsenic atoms in a silicon crystal should produce a change in lattice parameter of less than 10^{-5} Å, which could not be resolved in the present experiment. The lattice parameter in the heavily boron-doped wafer was found to be 0.0007 Å (0.01%) less than that of the lightly doped crystal. This change agrees in direction and magnitude with the 0.0009 Å change expected from contraction coefficient $\beta = \frac{\Delta a_o/a_o}{N_A}$ of 2.3×10^{-24} cm^3/atom found by Cohen (3). Thus, values of the lattice parameter found on the bulk samples produced confidence in the experimental technique and indicated that changes of 0.0002-0.0003 Å or greater in the experimentally determined lattice parameter would probably be significant.

Thin-film samples formed by the electrochemical-etching technique were measured after various treatments. Sample 9 was measured after the electrochemical-etching process was completed while sample 15 was tested

TABLE 8.1

Lattice Parameter From Least-Squares Fit and Calculated Stress

Sample	Description	Lattice Parameter (Å)	Strain	Stress (dynes/cm^2)
7	Bulk p^+ 7 X 10^{19} boron	5.4301		
8	Bulk n^+ 3 X 10^{19} arsenic	5.4308		
9	Film after electrochemical etch	5.4311	6 X 10^{-5}	3 X 10^8
10	Bulk LOPEX 5 X 10^{15} boron	5.4308		
11	Poly-Si 1100°C SiH_2Cl_2	5.4295		
13	SOS (Fe-rad) Sapphire	3.4807		
	Silicon 1 X 10^{15} phos.	5.450	3.5 X 10^{-3}	2.2 X 10^{10}
14	SOS (Mo-rad) Sapphire	3.4810		
	Silicon 1 X 10^{15} phos.	5.445	2.6 X 10^{-3}	1.6 X 10^{10}
15	Film after vapor etch	5.4314	1.1 X 10^{-4}	7 X 10^8
16	Film after added epi	5.4310	4 X 10^{-5}	2 X 10^8

after a subsequent vapor-etch cycle, which is often used to thin the film and produce a better surface for subsequent device processing. Sample 16 consisted of a composite film formed by growing a 1.4 μm thick, 0.5 Ω-cm, phosphorus-doped epitaxial film on the electrochemically etched thin film (∿0.8 μm) which was subjected to a 1250°C antimony predeposition after vapor etching. All electrochemically etched films tested had (111)-orientation. The results on these samples (Table 8.1) indicate that the lattice parameter is not appreciably different from that found in the bulk control wafers. The differences of 0.0003, 0.0006 and 0.0002 Å found in the three samples are only slightly greater than the resolution of the technique, so these values can probably only be used as an upper limit on the difference in lattice parameter between the thin films and the bulk control wafers.

The lattice parameter of a polycrystalline-silicon layer of the type used to support the thin film was also measured. Since the polycrystalline-silicon film has little (111)-texture (4), X-ray peaks resulting from the dominant (110)-texture were observed. The angles 2 θ varied from 21° for the (220) K_β peak to 137° for the (10.10.0) K_α peak. The extrapolated lattice parameter was found to be 5.4295 Å, somewhat smaller than that of single-crystal silicon, but in good agreement with the value of 5.4295 Å found earlier (4) in thinner polycrystalline-silicon films deposited primarily from silane rather than dichlorosilane.

In order to compare the thin films formed by electrochemical etching with the alternate silicon-on-sapphire system, a 0.9 μm-thick silicon film deposited on $(1\bar{1}02)$-oriented sapphire was measured. This silicon film was oriented with its (100) plane parallel to the substrate. Consequently, only a few silicon peaks could be obtained from the weak (400) and (800) reflections, and a least squares fit to this limited data could not be performed. Therefore, the lattice parameter of the sapphire substrate was measured from the many, easily observed sapphire peaks. The slope of the a_0-vs-Nelson-Riley curve was multiplied by the ratio of the lattice parameters of silicon and sapphire and was used to extrapolate the measured silicon points to obtain the intercept. These measurements were performed with the softer Fe radiation as well as with the Mo radiation used in the other experiments in order to increase

the 2 θ angle of the (400) peak. The two measurements (13 and 14 in Table 8.1) indicated values of 3.4807 and 3.4810 Å for the (012)-plane spacing in sapphire for the Fe and Mo radiations, respectively, in reasonable agreement with the published value of 3.479 Å (5).

By the technique described above the extrapolated lattice parameters of the silicon film were found to be 5.450 and 5.445 Å for the Fe and Mo radiation, respectively. The latter value is thought to be more accurate since the slope of the curve corresponding to this measurement was almost zero while that corresponding to the measurement using Fe radiation was fairly steep. Therefore, the uncertainty in the technique used to reduce the data may have caused considerable error in the final result in the first experiment. In either case, however, the difference in lattice parameter of the silicon film from that of bulk silicon is of the magnitude of 0.015 Å or 0.3%--at least an order of magnitude greater than that observed in the electrochemically etched thin films.

From these measurements we see that the lattice parameter in the electrochemically etched thin films scarcely deviates from its value in bulk silicon while the lattice parameter in silicon films deposited on sapphire wafers is at least an order of magnitude greater.

8.4 Calculation of Stress and Discussion

From these values of the lattice parameter, we can calculate the magnitude of the stress existing in the thin films. The strain in each of the films is just the deviation in lattice parameter divided by the lattice parameter. These values are summarized in Table 8.1. This strain is, however, the strain normal to the film plane since the X-ray measurements determined the lattice parameter normal to the film plane. In order to find the strain in the film plane, which is the quantity of greater interest, the values of strain in Table 8.1 must be divided by Poisson's ratio, which is taken to be -0.3 for these calculations. The strain can then be related to the stress by multiplying by the elastic constant for silicon $Y = 1.9 \times 10^{12}$ dynes/cm^2 (6, 7). The values of stress computed in this manner are indicated in the last column in Table 8.1. In all cases the stress in the silicon film is compressive.

The values of stress found for the silicon-on-sapphire films can be compared to values from the literature. Dumin (8) found the stress

in the silicon film to be about 5 X 10^9 dynes/cm^2 from measurements of the radius of curvature of the composite silicon-on-sapphire wafer. Ang and Manasevit (9) reported stresses of 6-9 X 10^9 dynes/cm^2 from measurements of the deflection of a sapphire beam after deposition of the silicon film. By radius of curvature measurements, Schlotterer (10) has found the stress in the silicon films deposited on spinel substrates to be about 9 X 10^9 dynes/cm^2. These published values of stress are about a factor of 2 or 3 lower than those found in the present experiments. While the different experimental technique used may lead to somewhat different results, the order of magnitude of the stress found is the same in all cases. It should be noted that the data can be brought into good agreement if Poisson's ratio is not used in calculating the stress in the films in the present experiment.

The results found in this experiment for the electrochemically etched thin films and the silicon-on-sapphire films can be directly compared, however. We find that the stress in the electrochemically etched films is about a factor of 40 less than the stress in the silicon-on-sapphire films. This difference may influence the behavior of devices constructed in the thin films quite significantly. For example, Schlotterer (10) indicates that the mobility in (100)-oriented, n-type silicon films under a compressive stress of 8 X 10^9 dynes/cm^2 will be about a factor of 1.6 less than that in unstressed silicon. This mobility change may seriously affect device behavior. The much smaller stress in the electrochemically etched films will not significantly affect the mobility, and hence the device performance should not be noticeably degraded.

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9. REPORT SUMMARY AND RECOMMENDATIONS

9.1 Introduction

This report has described the results of a research-and-development study of the material properties of thin, single-crystal silicon films supported by insulator/polycrystalline-silicon substrates. To fabricate this structure a lightly doped silicon film is epitaxially grown on a heavily doped, n-type, single-crystal silicon wafer. The structure is then covered with an insulator (e.g., silicon dioxide), and a thick layer of polycrystalline-silicon is deposited over the entire wafer. The heavily doped, single-crystal substrate is then removed by an electrochemical-etching process which terminates at the epi/substrate interface, leaving a thin, uniform, single-crystal silicon film on an insulating layer on top of the semi-insulating polycrystalline silicon. In this manner, a film of high-quality, single-crystal silicon can be fabricated on a substrate which is essentially insulating. The oxide film has the usual insulating properties of thermally grown silicon dioxide, and the resistivity of the polycrystalline support is about 10^5-10^6 Ω-cm. The high differential etch rate of the substrate and the lightly doped epitaxial film in the electrochemical etch is crucial to this process.

9.2 Process Optimization

During this study very significant progress has been made toward achieving a useful substrate system, and reproducibility has been demonstrated. The film quality has been found to be limited by isolated defects formed during electrochemical etching rather than by the basic properties of the film. An investigation of these defects and their minimization were among the major goals of this study. Consideration of each step in the fabrication process has led to a great reduction in the defect density. In particular, it was found that dislocations initially present in the heavily doped substrate wafer or induced by subsequent processing will cause rapid etching during the electrochemical process and will lead to defects in the thin film. The major source of process-induced dislocations was found to be degradation occurring during

the deposition of the thick,polycrystalline-silicon film. This degradation was shown to be related to trace quantities of oxygen in the reactor.

The effect of the dopant type in the epitaxial film has been investigated, and it was found that lightly doped, p-type films are of better quality than similarly doped, n-type films after electrochemical etching. Both silane and dichlorosilane were found to be suitable sources for the deposition of the initial epitaxial film. The thickness of the film was found to be important in determining its quality; films thinner than about 1.3 μm after electrochemical-etching, but before subsequent thinning, were often found to be highly defective. Films thinner than 0.5 μm could be obtained by vapor etching high-quality films formed by electrochemical etching. The behavior of (100)-oriented silicon was generally similar to that of the (111)-silicon which was used in most of the experiments.

In order to evaluate the quality of the material obtained, the films were directly examined under the dark-field microscope, and shallow bipolar transistors, which are quite sensitive to material defects, were also fabricated in the electrochemically etched films. As the study progressed, the characteristics of the transistors and the yield both improved. Comparison of the characteristics of transistors fabricated in 2 μm-thick silicon films with those formed in bulk wafers revealed no differences, indicative of the high film quality. The quality of the films is comparable to that required for reasonable yield of large-area, bipolar integrated circuitry.

9.3 Film Properties

Hall mobility measurements were taken on both p-type and n-type films of varying thicknesses with about 10^{15} cm^{-3} dopant atoms. The mobilities observed in the thin-film and control samples were almost identical for the p-type films. However, the mobilities measured in the n-type films differed markedly from those in the control samples. This behavior is probably caused by an accumulation layer with lower carrier mobility at the bottom surface of the n-type film. Measurements on very thin samples indicated that an n-type surface layer was

left on p-type samples immediately after electrochemical etching. The Hall mobility results suggest that the characteristics of semiconductor devices fabricated in the thin films formed by electrochemical etching will not be degraded by reduced majority-carrier mobilities.

Values of the minority-carrier lifetimes have been determined both by injection of carriers across p-n junctions and by generation near the surfaces of MOS structures. Injection of carriers across p-n junctions indicated a lower bound on the lifetime of a few microseconds while injection across the emitter-base junction of bipolar transistors indicated lifetimes of the order of 10 μsec. More detailed investigation of deep-depletion MOS structures also revealed lifetimes of the order of 10 μsec. Further gettering may increase the lifetimes to somewhat higher values. Measurement of the DC characteristics of the deep-depletion devices fabricated in the thin films indicated few differences from those fabricated in the control wafers, at least until the depletion region approached the bottom of the silicon film.

The lifetimes found in this investigation have significant implications for the devices which can be constructed in the films. The lifetimes have been found to be long enough so that the characteristics of junction devices will not be degraded. In particular, high-quality bipolar transistors can be fabricated in the thin films formed by electrochemical etching. This is to be contrasted to the situation for the alternative silicon-on-sapphire system, in which lifetimes of about 10 nsec are the maximum which can be achieved, even after many years of effort. Therefore, the fabrication of bipolar transistors in silicon-on-sapphire films is difficult. Low values of lifetime in the silicon-on-sapphire films also degrade the characteristics of p-n junctions, such as the source and drain junctions in MOS circuitry. The markedly higher lifetime in the present system is one of its major advantages over the silicon-on-sapphire system.

The diffusion of dopant impurities into the thin films has also been investigated. To first order, the diffusion characteristics of both boron and phosphorus are similar in the thin films and in bulk

wafers. Possible second-order effects include slightly higher sheet conductivities in the thin films than in bulk control wafers and slightly shallower diffusion of phosphorus into p-type films than into bulk control wafers. The oxidation rate of the thin-film samples did not differ to any noticeable degree from the oxidation rate of bulk silicon wafers in either a dry O_2 or a steam ambient.

An indication of the stress in the electrochemically etched thin films was obtained by measuring the lattice parameter. An upper bound on the stress in the films at various stages of the fabrication process was in the 10^8 dynes/cm^2 range. This upper bound is about a factor of 40 less than the stress in a silicon-on-sapphire film which was also measured in the present study. While the large stress in silicon-on-sapphire films may markedly degrade device performance, the much smaller stress in the electrochemically etched films should not significantly affect device characteristics.

9.4 Device Implications

The results of this study indicate that high-quality, thin silicon films can be reproducibly fabricated with material properties which will allow a wide variety of devices to be constructed in the films. High-quality bipolar, as well as MOS devices, may be fabricated for use in a wide range of applications. The parasitic capacitances between elements of such circuits will be greatly reduced, and dielectric isolation can be achieved. This system, therefore, can provide an alternative to the silicon-on-sapphire system and is preferable because of the superior quality of the silicon film formed, the ease of subsequent device fabrication, and the compatibility with conventional, well-developed silicon technology. In addition, a large increase in component density can be achieved when compared to conventional dielectrically isolated integrated circuits. The thin film also offers the possibility of novel structures which cannot be obtained with conventional techniques. For example, conducting interconnections between elements of an integrated circuit may be placed on both sides of the film, allowing significant area reduction and design flexibility, as well as improving the device characteristics.

9.5 Directions for Further Research

The minority-carrier lifetime and the film quality had to be investigated before this system was applied to dielectrically isolated, bipolar integrated circuitry--its first use. Application to other types of devices, as well as to more critical bipolar circuitry, will necessitate additional understanding of the electrochemically etched films. The results of the present study indicate that the behavior of the thin films can easily be dominated by the surface properties at both sides of the film. While the Si/SiO_2 interface at the upper surface is relatively well understood, the properties of the underlying Si/SiO_2 interface are almost completely unknown. Since the films may be very thin, this back surface can influence the electrical behavior throughout the entire thickness of lightly doped films. Although the heavily doped subcollector region in the bipolar transistor structure ensured that the active regions of the device were shielded from the underlying Si/SiO_2 interface, other devices will be strongly influenced by this interface. Therefore, the most productive research efforts can now be devoted to gaining understanding of and control over the properties of this underlying Si/SiO_2 interface. In particular, the surface states and surface recombination velocity should be investigated, and the effectiveness of annealing should be considered. Some additional effort should also be devoted to further improvement of the film quality by continuing optimization of the processing techniques.

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