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DAMAGE PROFILES IN SILICON AND THEIR IMPACT ON DEVICE RELIABILITY

Guenter H. Schwuttke

International Business Machines Corporation

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DAMAGE PROFILES IN SILICON and THEIR IMPACT ON DEVICE RELIABILITY

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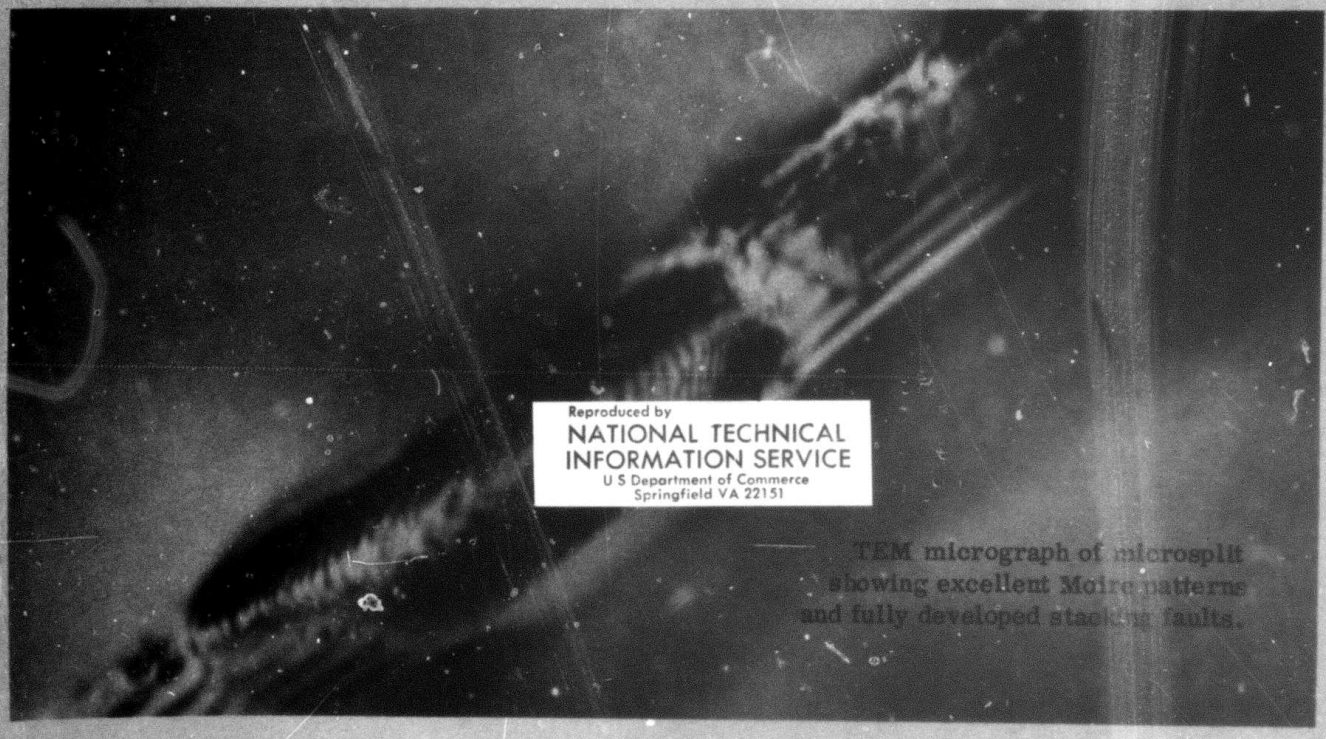

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TEM micrograph of microsplit showing excellent Moire patterns and fully developed stacking faults.

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Standard silicon wafers are shown to frequently contain residual mechanical saw damage in the surface. The damage is identified through transmission electron microscopy (TEM) as microsplits of the silicon lattice. Microsplits are not detectable by standard inspection, screening or etching techniques. Microsplit dimensions range from 0.1 to 10 μm. The density of the splits can vary from zero to $10^6/cm^2$ or even higher. Microsplits are shown to cause loss of storage time in MOS capacitors.

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LIST OF INVESTIGATORS

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The project is supervised by Dr. G. H. Schwuttke, principal investigator. The following persons contributed to the work in the report:

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The views and conclusions in this document are those of the author and should not be interpreted as necessarily representing the official policies, either expressed or implied, of the Advanced Research Projects Agency or the U.S. Government.

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MICROSPLITS IN SILICON SURFACES
and THEIR INFLUENCE ON MOS STORAGE TIME

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SUMMARY

Standard silicon wafers are shown to frequently contain residual mechanical saw damage in the surface. The damage is identified through TEM analysis as microsplits of the silicon lattice. Microsplits are not detectable by standard inspection, screening or etching techniques. Microsplit dimensions range from 0.1μm to 10μm. The density of the splits can vary from zero to $10^6/cm^2$ or even higher. Microsplits are shown to cause loss of storage time in MOS capacitors.

MICROSPLITS IN SILICON SURFACES and THEIR INFLUENCE ON MOS STORAGE TIME

1. INTRODUCTION

Dynamic storage techniques are revolutionizing the approach to high density low power monolithic memory design. The principle of this new technique is to store minority carriers (or their absence) in a spatially defined depletion region (potential well) at the surface of a homogeneous semiconductor and subsequently to move this charge about the surface by moving the potential minimum.[1] The storage and manipulation of charge is achieved at the $Si-SiO_2$ interface of a MOS capacitor. Charge transfer to a closely adjacent capacitor on the same substrate is done by appropriate manipulation of electrode potentials. Examples of possible applications are as shift register, as an imaging device, as a display device and in performing logic.

Such new applications place radically different and previously never realized stringent requirements on silicon material quality. Requirements of leakage currents of less than 10^{-13}A per device have been indicated. This compares to the material requirements to be met for the Picturephone®.[2]

The major concern for charge storage devices is the time required for an undesired formation of an inversion layer in the storage

condenser. If this time is greater than 10^{-3} sec., a satisfactory operation can be expected and only nominal amounts of regeneration of information will be required.

The formation of an inversion layer can be followed conveniently through a measurement of the storage time T of a MOS capacitor. In the storage time measurement a MOS capacitor is pulsed from accumulation into deep depletion by a voltage step while the high-frequency capacitance is measured versus time. This technique has been used by many workers to characterize the effective minority carrier lifetime of bulk silicon.[3-6] The relationship for storage time, or time for inversion as worked out by Heiman[4] is: $T=2\tau N_a/N_i$ (τ = effective minority carrier lifetime, N_a = substrate doping density, N_i = intrinsic carrier density). Since for silicon $N_i = 1.4 \times 10^{10} cm^{-3}$, T can be greater than τ by many orders of magnitude. Storage times of the order of many seconds have been achieved.[2,4,7] Large variations in storage time and its dependency on crystal quality and process parameters have been reported.[8] No exact information relating storage time to crystal perfection is presently available. This paper reports investigations undertaken to identify crystal defects and failure mechanisms that destroy the storage time of MOS capacitors.

2. EXPERIMENTAL

The storage time was determined from the transient response of a depletion - capacitance structure.[4] To facilitate such measurements and to evaluate local variations in storage time on silicon wafers, standard 2 1/4 inch diameter silicon slices of (100) orientation, p-type and of 2 ohm-cm resistivity were processed to contain 36 circular MOS devices (60 mil dia.) per wafer. A 5000Å thick oxide was grown at 1000°C using a dry-wet-dry (15 minutes - 90 minutes - 30 minutes) oxidation cycle. Aluminum metallurgy was used. After metalization the wafers were annealed in forming-gas at 400°C for 30 minutes. For the deep depletion measurements the devices were contacted by a K & S stepping probe with a platinum probe point in a dark box. C-t traces were made of all devices on a wafer. A copy of a typical data sheet for a wafer giving 100% yield is shown in Fig. 1a and a copy of a data sheet of a wafer giving zero yield is shown in Fig. 1b. The trace of a single C-t curve corresponding to a good device is shown magnified in Fig. 1c and for a bad device in Fig. 1d. A device was classified as good for leakage currents less than 0.02 pA/mil^2 area.

Based on the storage time measurements bad devices were selected for structural analysis of their active substrate area. The defect state in the active device area was investigated through

high-voltage transmission electron microscopy (TEM) supplemented by scanning electron microscopy, light microscopy and etching techniques. For the TEM analysis the Al metallurgy and the device oxide was stripped and thus the native substrate area under the MOS device was made available for detailed investigations. Subsequently, the device area was chemically thinned down from the back until it was transparent to the 200 KeV electrons. The native substrate area (front) was not damaged during the specimen preparation process. The sample thickness for TEM analysis was 1μm or less. Scanning electron microscopy and light microscopy were made after etching the front (active device area) of the native substrate area for 10 seconds with Sirtl etch. Similar measurements were performed on good devices for comparison.

3. RESULTS OF STRUCTURAL INVESTIGATIONS

The following is a survey of defects found in devices that yield a C-t response curve as shown in Fig.1d. The average density of defects found in such devices is approximately 10^4 defects/cm^2.

3.1 Transmission Electron Microscopy (TEM)

TEM analysis revealed the presence of linear defects in crystallographic orientation (110 directions). The defect length varies considerably. The length covers a range from several

microns down to only 0.1μm. A simple line defect of approximately 10μm in length is shown in Fig. 2a. Note the shape of the line: very thin ends, thicker in the center and sometimes additional dot contrast in the center. The dot contrast could indicate contamination. The TEM of Fig. 2a was recorded using multi-beam diffraction (kinematical diffraction), therefore, stress effects caused by the defects in the lattice are not displayed. A two beam (dynamical case) recording of a similar defect is shown in Fig. 2b. Most striking are the stress contours (white on the left side and black on the right side of the defect). During tilting extinction contours are generated primarily at the ends of the line defect and sweep across the micrograph during tilting. The extinction contours never cross the defect line. This indicates a clear physical separation of the crystal along and parallel to the defect line. The black/white beat contrast along the ends of the line indicates that the black contrast lines slopes down from the ends towards the middle of the line.

Small linear defects are displayed in the micrographs of Fig. 3. Noteworthy are the strong stress contours displayed by such small defects. The length of the defects is approximately 0.3μm. Both defects show strong Moire contrast indicative of a clear lattice separation along the short defect line.

A set of line defects, each line approximately 1μm long, is shown in Fig. 4. The defects are oriented along <110> directions and penetrate each other at 90 degrees. Both line defects show Moire contrast and are surrounded by a highly stressed lattice. A short (0.2μm) and a long (8μm) defect are contrasted in Figs. 5a, b. Again both defects are visible due to Moire contrast. The long defect shows well developed rotation Moire contrast at the ends. Again, stress concentrations are confined to the ends of the fault.

An interesting series of micrographs is displayed in Figs. 6a, b. Evidently, the shear stresses displayed in the preceding micrographs at the fault ends are large enough in this case to generate stacking faults. Figure 6a shows the birth of a stacking fault due to stress relief at one end of the linear defect while Fig. 6b shows well developed stacking faults at both ends of the defect.

A beautiful example of stress relief through stacking fault generation is shown in Fig. 7. One can see two linear defects producing excellent Moire patterns and complete stress relief through fully developed stacking faults.

Defects of higher complexity can occur and can be abundant. Two

examples are shown in Figs. 8a, b. Both micrographs show groups of linear faults interacting and producing complicated defect patterns.

3.2 Scanning Electron Microscopy and Chemical Etching Results

Sirtl etching was applied to the device surface after stripping the Al and the SiO_2. Occasionally etching was successful in delineating the linear faults. Most of the time the etch patterns did not reveal a clear-cut difference between a good and a bad device. Etching depends very much on the fault size and seems to work quite well for faults in the micron size. An example is shown in Fig. 9 which pictures the silicon surface of a bad device after stripping and Sirtl etching. Linear defects are clearly visible in <110> directions. Scanning electron micrographs of such defects are given in Figs. 10a, b. Figure 10a shows a longitudinal view of the defect. The defect looks like an open cut or split in the lattice and supplements the transmission electron micrograph information. A fault like the one displayed in Fig. 10a obviously must introduce high stresses into the lattice, particularly at the fault ends. Such lattice splits have a tendency to close in order to minimize their elastic tip stresses. Most of the time more or less complete closure takes place in agreement with the observation of Moire patterns in the transmission electron

micrographs. A cross-sectional view of two microsplits after etching is shown in the SEM photomicrograph of Fig. 10b. The cross-sections show that such faults penetrate to different depths and are not confined to cleavage planes. This observation supports partial split experiments made on germanium.[9]

4. DISCUSSION

Based on the data presented in section 3 the linear defects that cause loss of storage time in MOS capacitors are analysed as microsplits or microcracks of the silicon lattice. The density of such microsplits can vary considerably from wafer to wafer from zero to $10^6/cm^2$. This type of surface damage must obviously be associated with the slicing process of silicon. Modern wafering techniques in semiconductor manufacturing rely completely on high-speed cutting using diamond coated inside-diameter (ID) blades. A standard rotational blade speed is 50 revolutions per second and a 2 1/4 inch diameter silicon crystal can be sliced in 60 seconds. Realizing the hardness and brittleness of silicon crystals, large volume oriented manufacturing slicing of silicon is truly an astounding process but has hardly any concern for silicon perfection.

Relatively little work has been reported on the nature and extent of saw damage to semiconductor crystals as a result of

high speed slicing. The work that has been reported is somewhat contradictory because the crystals were not specified sufficiently and slicing was done under conditions that cannot be compared readily. Accordingly, the depth of damage as reported varies from a few microns to about 100μm.[10] In these investigations, the definition of damage is based on the visibility of certain etch features on the wafer surface that disappear with prolonged etching time. Such investigations of saw damage are unaware of the fact that damage may persist in a silicon slice even after etch polishing.

Excellent data on ID-sawing damage to germanium and silicon are reported by R. L. Meek and M. C. Huffstutler, Jr., for a range of sawing parameters.[11] They find well defined damage layers in silicon after ID slicing. The damage layers extend at least 50μm into the bulk crystal. Based on vibration studies made while actually slicing they conclude that out of plane vibrations of the sawing blade and periodic abrasive contact of the blade with the crystal due to the non-circularity of the blade center-hole are important damage mechanisms during slicing. In addition, they conclude that stresses set up in the wafer due to high-frequency vibrations of the slice being cut, may lead to fatigue cracking. This mechanism is a well known failure source in metal crystals but fatigue and fracture of homopolar crystals has received very little attention.

Detailed investigations on the mechanical properties of single crystals of silicon are reported by Sylwestrowicz.[12] This investigator postulated in 1961 that silicon crystals must contain a high density of small cracks in the surface after slicing and that etch polishing does not remove such cracks. He postulates that microcracks are responsible for low fracture stresses observed in most silicon samples. Almost theoretical yield strength was observed in some samples thought to be free of such surface cracks.

Generally it is assumed that today's advanced chemical-mechanical polishing techniques as used in semiconductor manufacturing produce a damage-free wafer surface. Our investigations show that this is not necessarily so and thus confirm Sylwestrowicz's hypothesis.[12] On the other hand it has also become clear that silicon wafers can be produced damage-free, as defined by a 100% yield as shown in Fig. 1a.

A final remark about the electronic properties of fracture interfaces in crystals. Fracture interfaces in crystals are well known to influence electronic properties in semiconductor crystals. Electronic properties of small internal splits in silicon have been studied extensively, and microsplits in the silicon surface have been shown to cause extra surface states, i.e., energy levels within the forbidden energy gap of the silicon.[9,13,14]

Therefore, a question comes up: How is it possible that such a severe type of surface damage as discussed here could pass through the semiconductor industry unnoticed for such a long time? One might take this as an indicator that dynamic storage techniques are not only revolutionizing memory design but also silicon materials technology.

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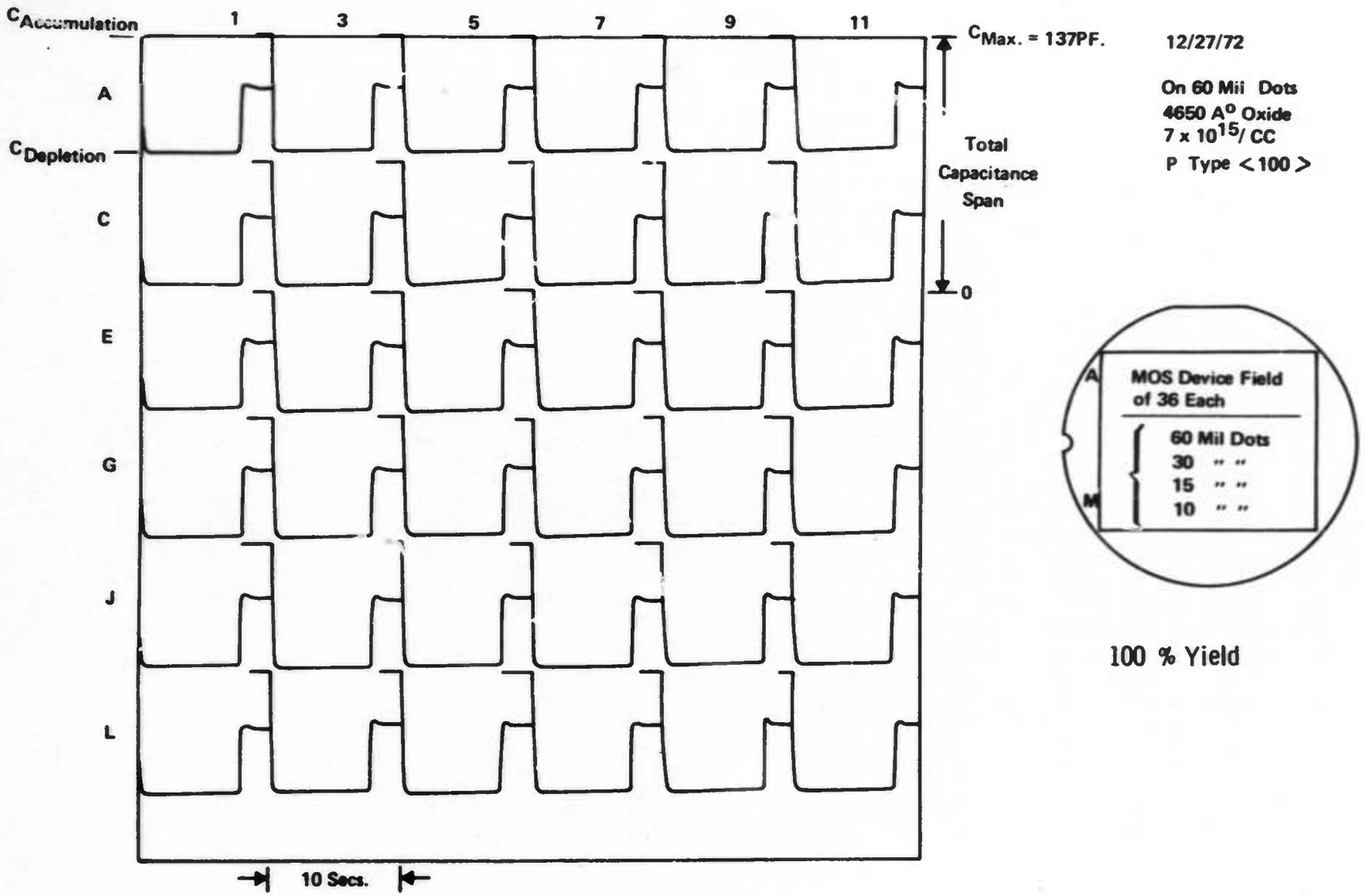

Fig. 1a. Storage time map of silicon wafer with 36 MOS capacitors. All devices good.

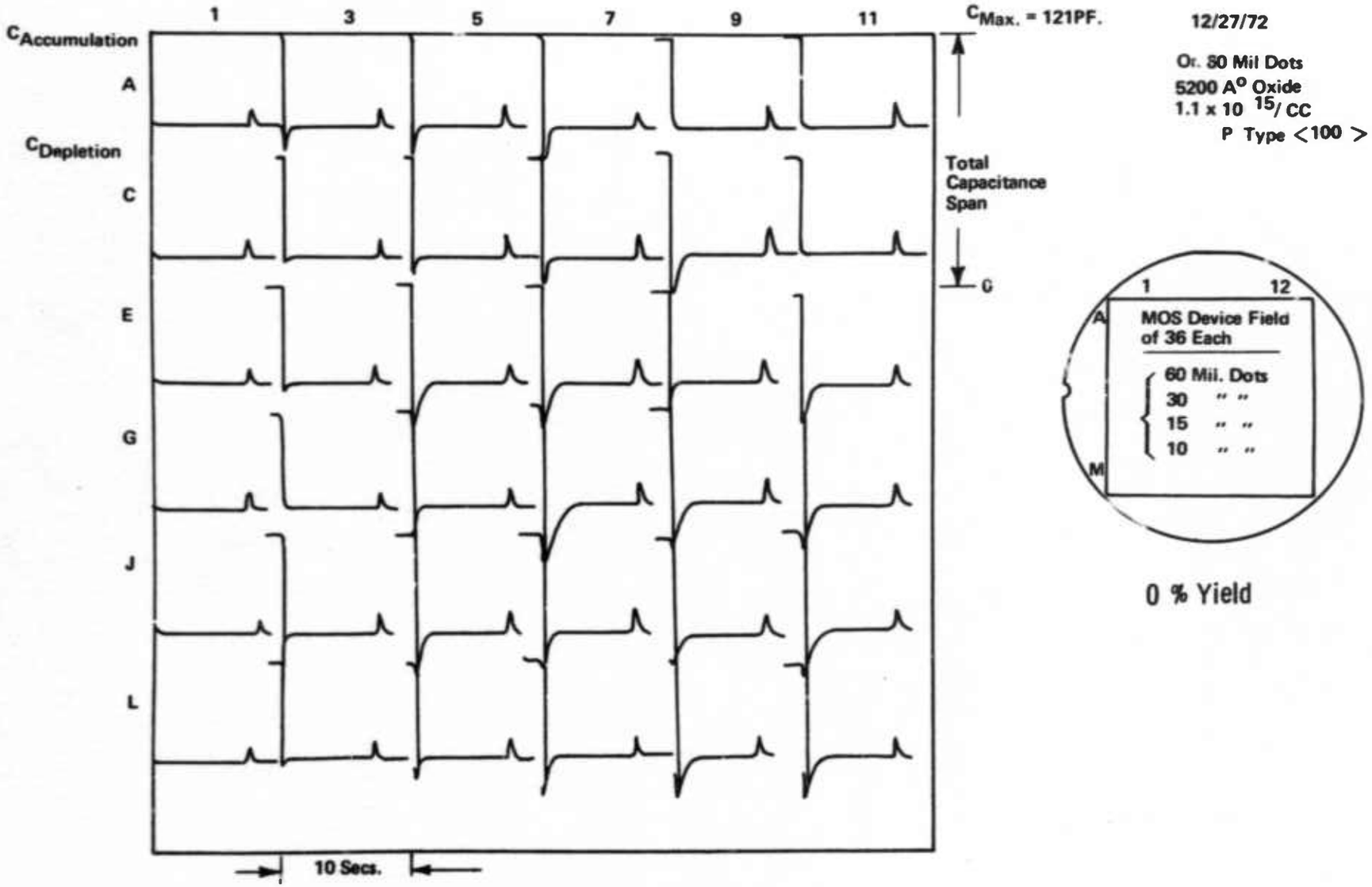

Fig. 1b. Storage time map of silicon wafer with 36 MOS capacitors. All devices bad.

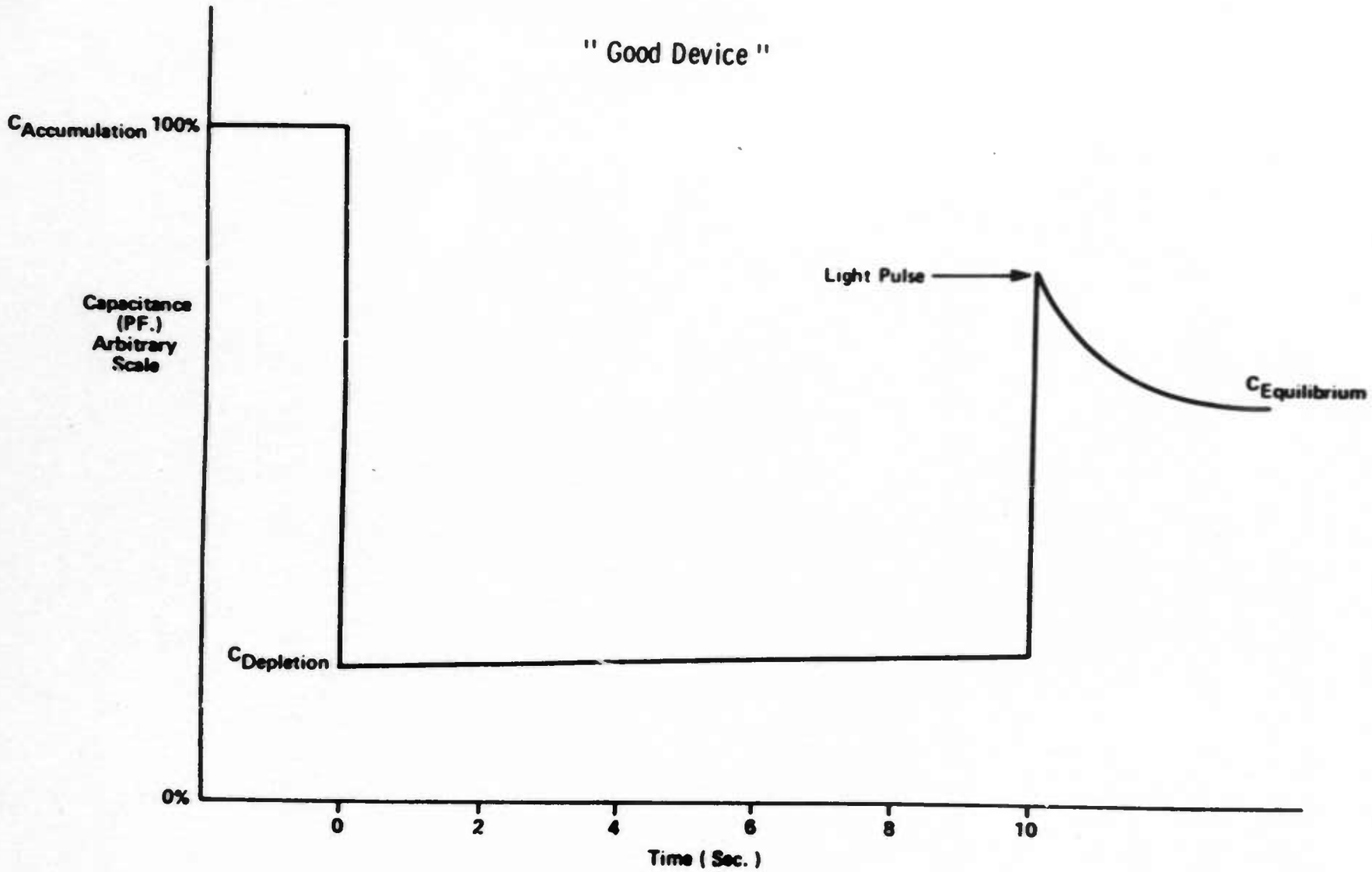

Fig. 1c. Single C-t curve of good device.

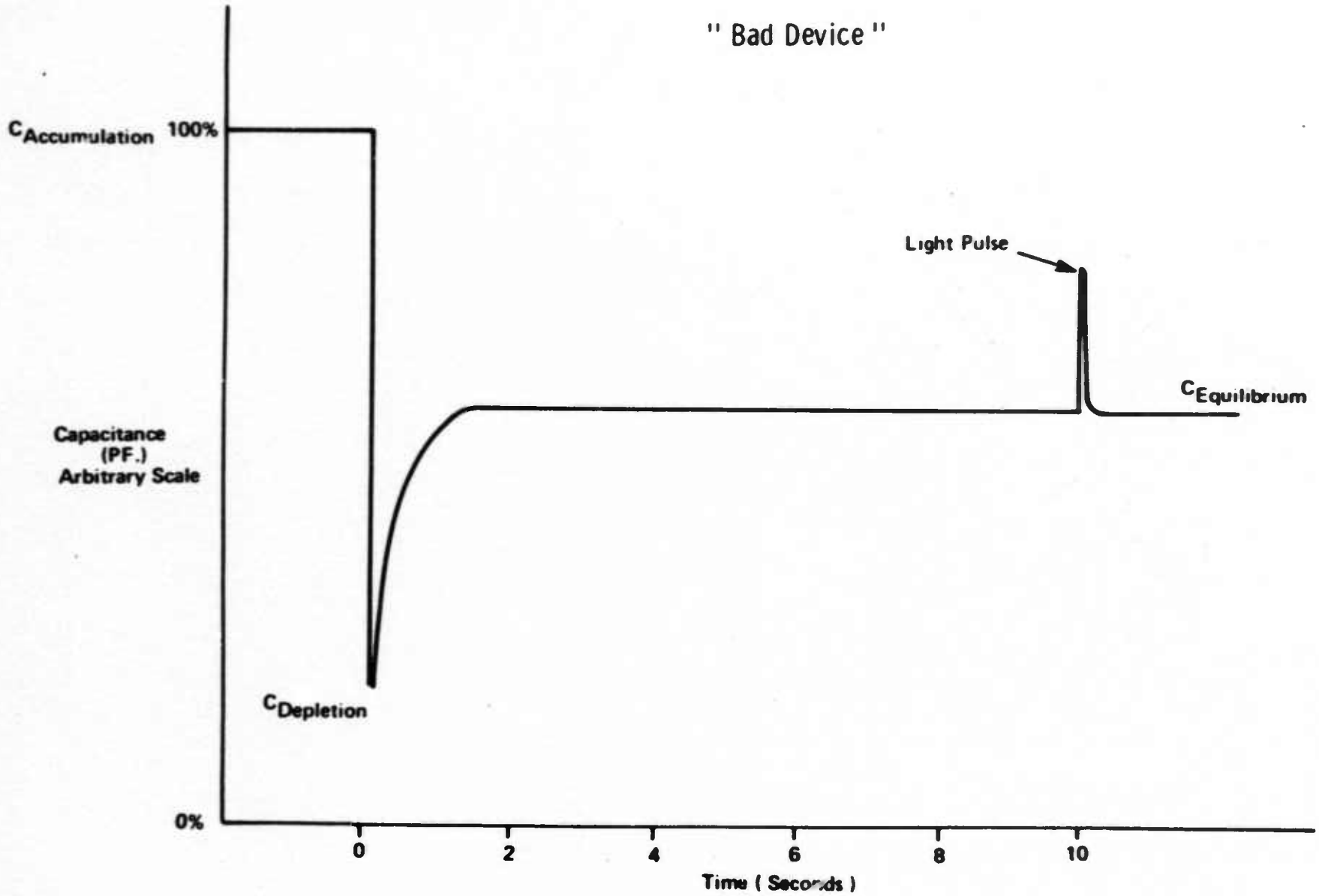

Fig. 1d. Single C-t curve of bad device.

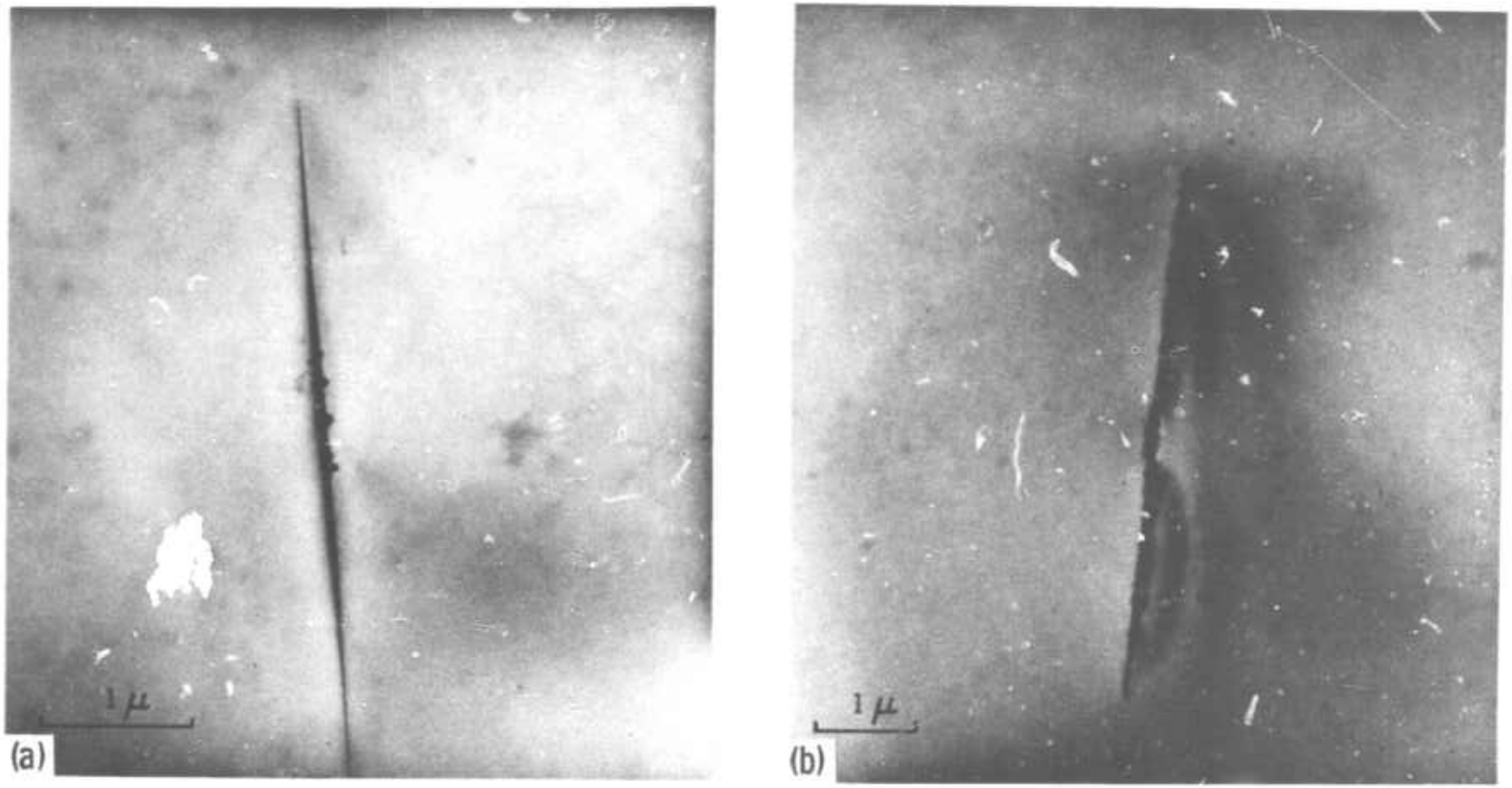

Fig. 2. TEM micrographs of 8μm-long split in lattice. (a) Multibeam recording. (b) Two-beam recording revealing stress effects in lattice.

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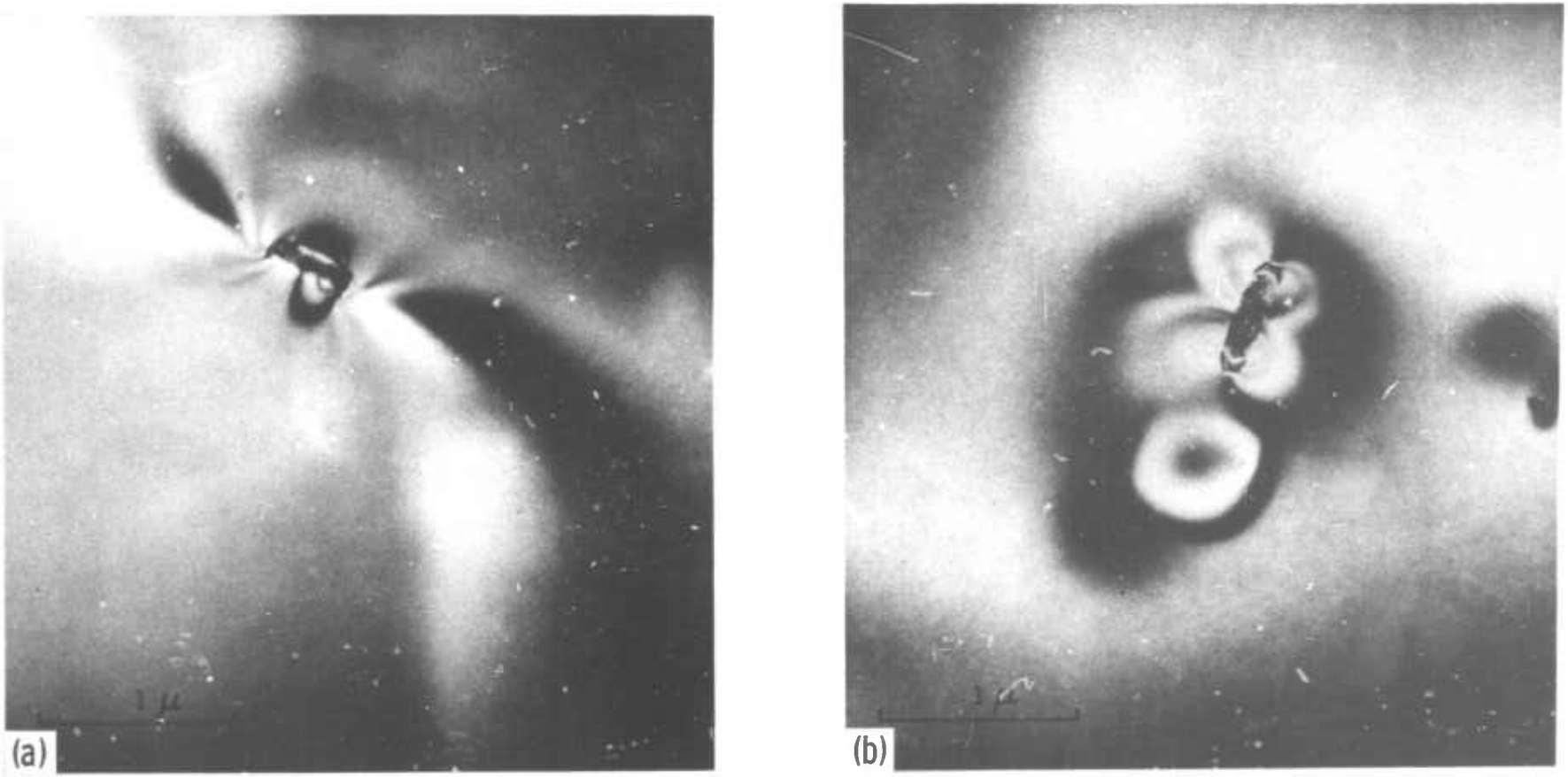


Fig. 3. TEM micrographs of 0.3μm-long microsplit. (a) Note strong stress contours emerging from the ends. (b) Associated four-fold stress contours.

Fig. 4. TEM micrograph of composite microsplit. Two splits penetrate each other at right angles.

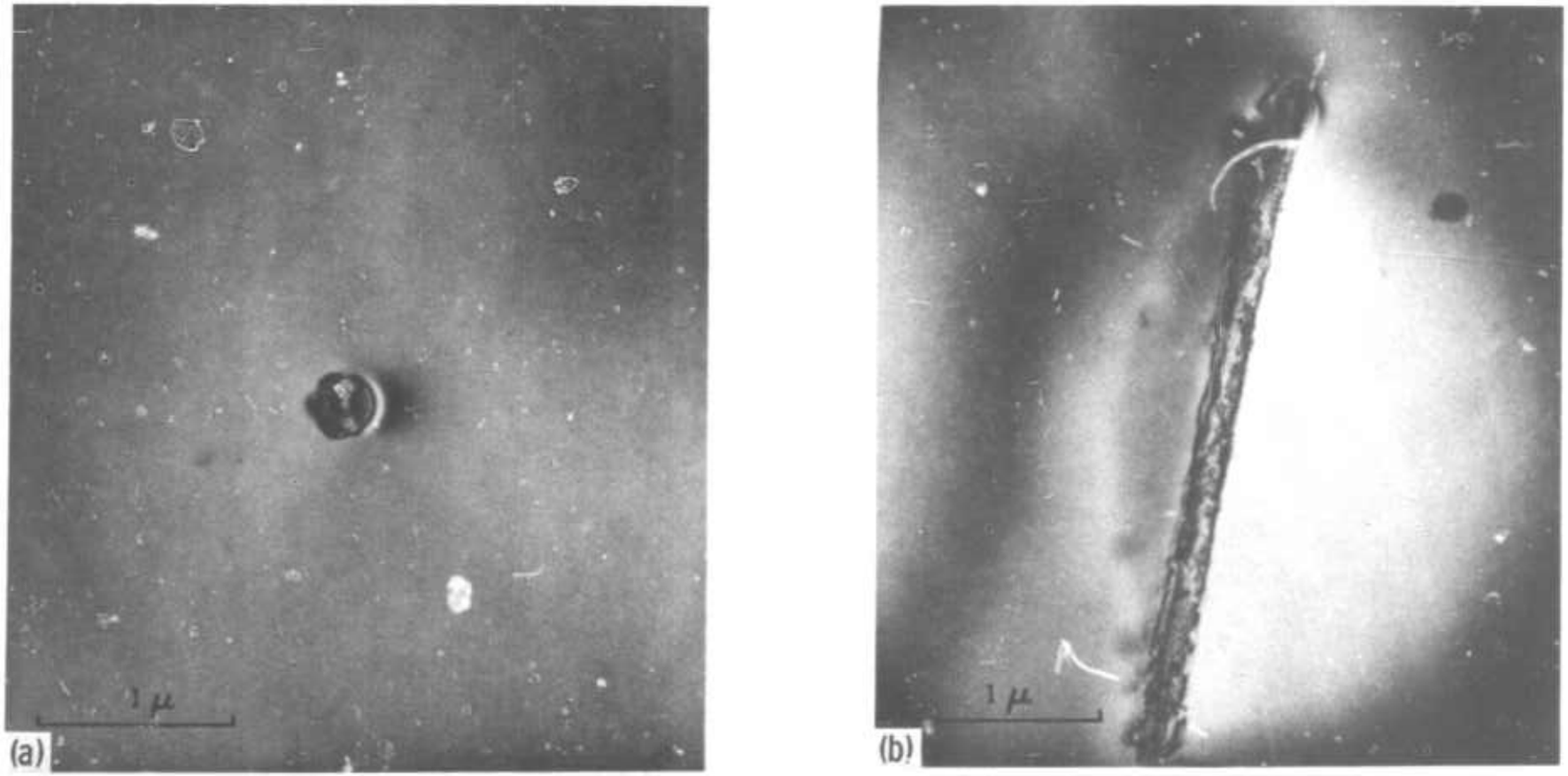


Fig. 5. TEM micrographs. (a) 0.1μm microsplit. (b) 10μm-long split. Note Moire patterns, well developed at the ends.

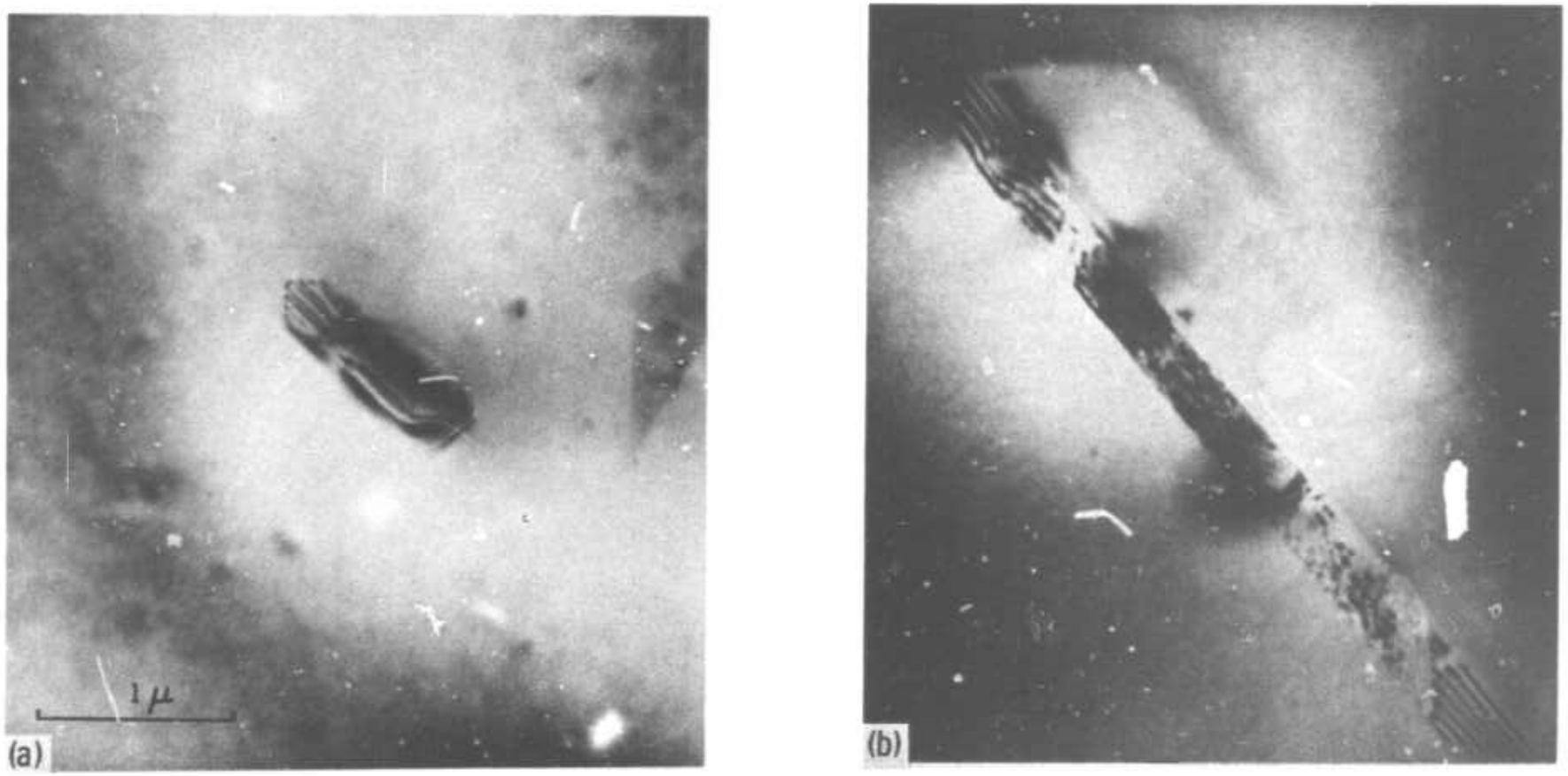


Fig. 6. TEM micrographs of microsplit. (a) Birth of stacking fault at one end. (b) Stacking faults at both ends.

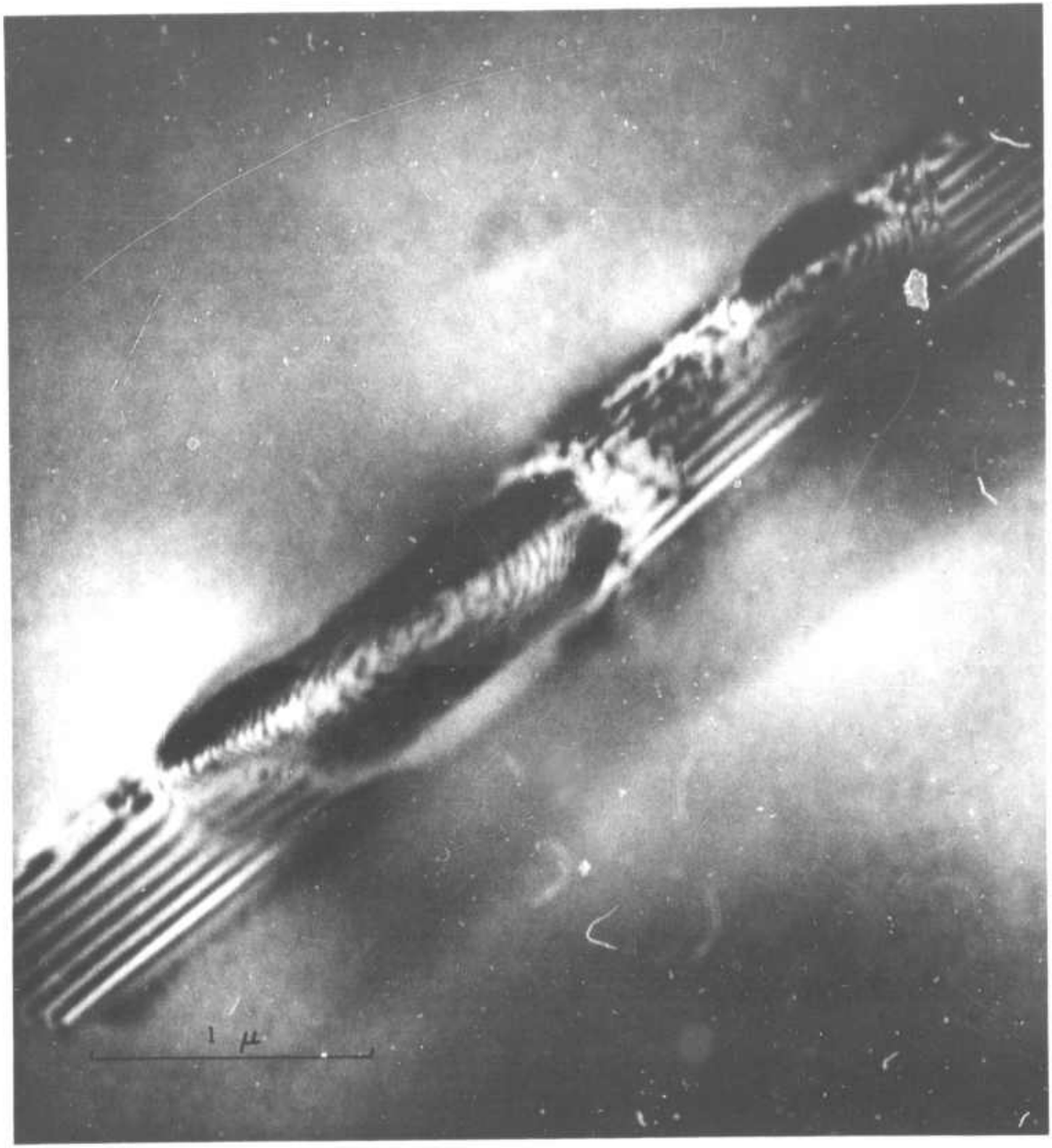


Fig. 7. TEM micrograph of microsplit showing excellent Moire patterns and fully developed stacking faults.

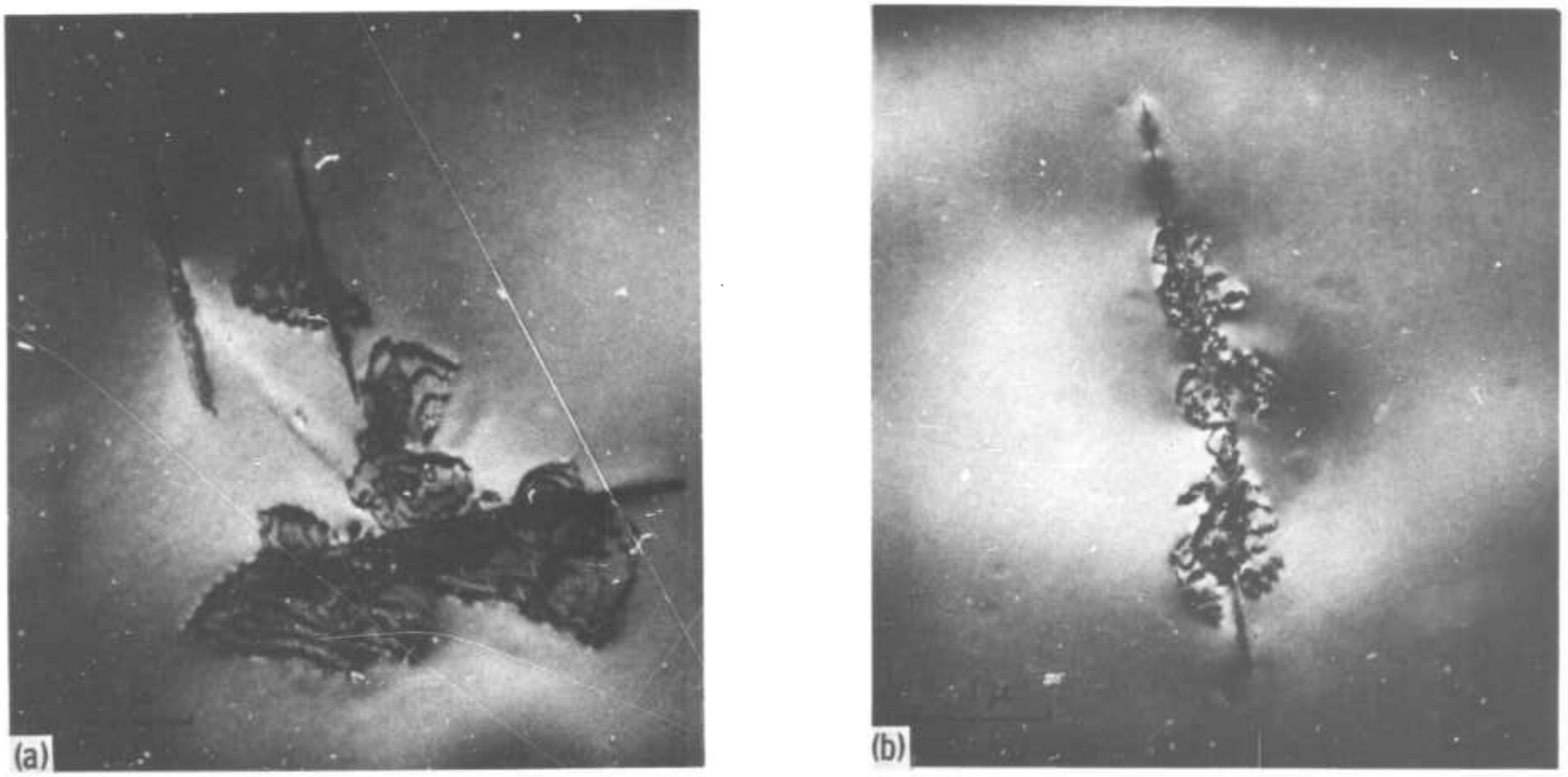


Fig. 8. TEM micrographs of group of splits. (a) Single splits in perpendicular orientation. (b) Single splits in parallel orientation.

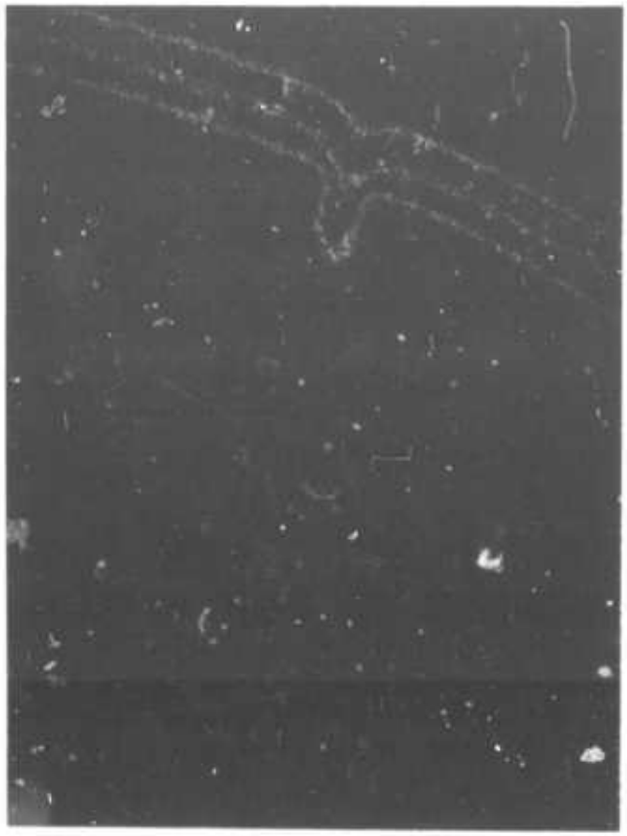
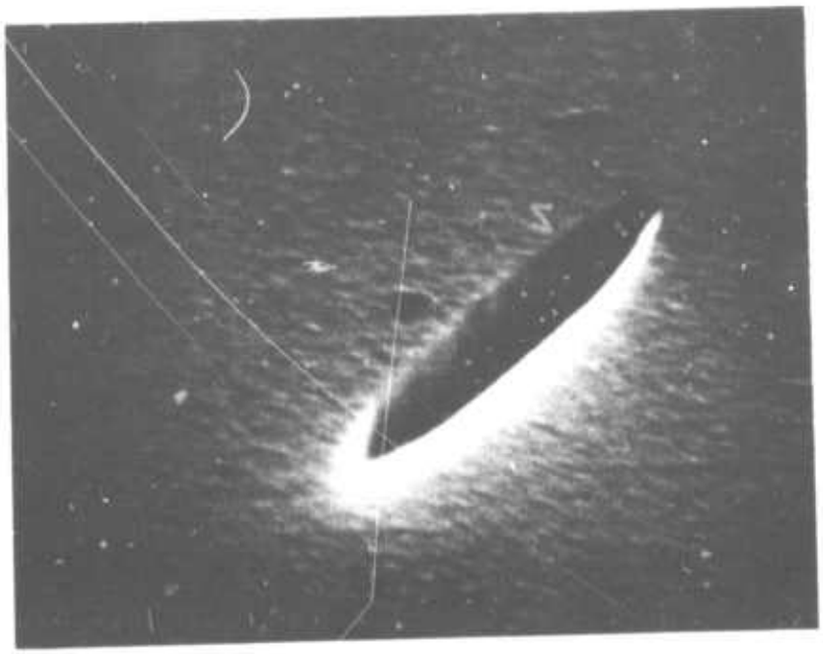
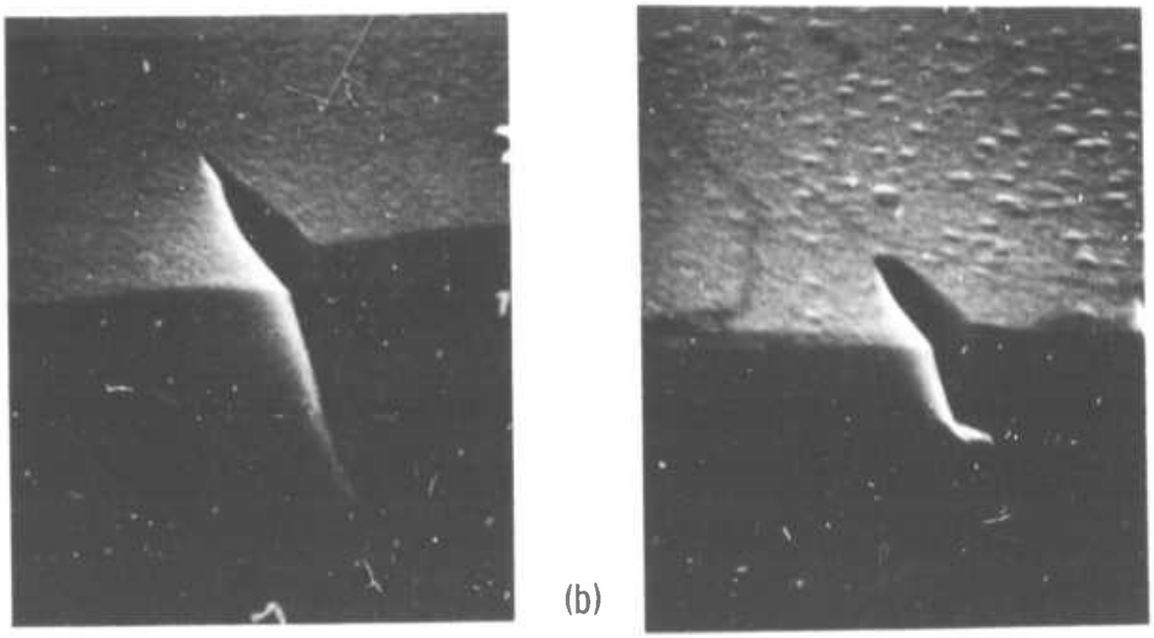


Fig. 9. Optical micrograph of bad device after stripping and Sirtl etching. Note linear defects in ⟨110⟩ orientation.



(a)



(b)

Fig. 10. SEM micrographs of split. (a) From etch figures corresponding to Fig. 9. (b) Cross section of two different splits.

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