AD-753 413

SIMPLIFIED MODELING OF INTEGRATED CIRCUITS FOR RADIATION PERFORMANCE PREDICTION

J. R. Greenbaum

General Electric Company

Prepared for:

Defense Nuclear Agency
Air Force Weapons Laboratory

November 1972

DISTRIBUTED BY:

NTIS

National Technical Information Service
U. S. DEPARTMENT OF COMMERCE
5285 Port Royal Road, Springfield Va. 22151

AD753413

AFWL-TR-72-42

AFWL-TR-
72-42

SIMPLIFIED MODELING OF INTEGRATED CIRCUITS FOR RADIATION PERFORMANCE PREDICTION

J. R. Greenbaum

General Electric Company

TECHNICAL REPORT NO. AFWL-TR-72-42

November 1972

DDC
RECEIVED
JAN 2 1973
E

AIR FORCE WEAPONS LABORATORY
Air Force Systems Command
Kirtland Air Force Base
New Mexico

Reproduced by
NATIONAL TECHNICAL
INFORMATION SERVICE
U S Department of Commerce
Springfield VA 22151

Approved for public release; distribution unlimited.

AFWL-TR-72-42

AIR FORCE WEAPONS LABORATORY
Air Force Systems Command
Kirtland Air Force Base
New Mexico 87117

ACCESSION for
NTIS
DDC
UNANNOUNCED
JUSTIFICATION
BY
DISTRIBUTION/AVAILABILITY CODES
A

When US Government drawings, specifications, or other data are used for any purpose other than a definitely related Government procurement operation, the Government thereby incurs no responsibility nor any obligation whatsoever, and the fact that the Government may have formulated, furnished, or in any way supplied the said drawings, specifications, or other data, is not to be regarded by implication or otherwise, as in any manner licensing the holder or any other person or corporation, or conveying any rights or permission to manufacture, use, or sell any patented invention that may in any way be related thereto.

DO NOT RETURN THIS COPY. RETAIN OR DESTROY.

UNCLASSIFIED

Security Classification

DOCUMENT CONTROL DATA - R & D

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1. ORIGINATING ACTIVITY *(Corporate author)* General Electric Company Court Street Plant Syracuse, New York 13201	2a. REPORT SECURITY CLASSIFICATION UNCLASSIFIED 2b. GROUP

3. REPORT TITLE

SIMPLIFIED MODELING OF INTEGRATED CIRCUITS FOR RADIATION PERFORMANCE PREDICTION

4. DESCRIPTIVE NOTES *(Type of report and inclusive dates)*

February 1971 through February 1972

5. AUTHOR(S) *(First name, middle initial, last name)*

J. R. Greenbaum

6. REPORT DATE November 1972	7a. TOTAL NO. OF PAGES 272	7b. NO. OF REFS ---
8a. CONTRACT OR GRANT NO. F29601-71-C-0049 b. PROJECT NO. 5710 c. Subtask TB027 d.	9a. ORIGINATOR'S REPORT NUMBER(S) AFWL-TR-72-42 9b. OTHER REPORT NO(S) *(Any other numbers that may be assigned this report)*	

10. DISTRIBUTION STATEMENT

Approved for public release; distribution unlimited.

11. SUPPLEMENTARY NOTES	12. SPONSORING MILITARY ACTIVITY AFWL (ELT) Kirtland AFB, NM 87117

13. ABSTRACT

(Distribution Limitation Statement A)

This report describes a simple method for developing computer models for digital and analog integrated circuits. The models are capable of allowing computer prediction of both normal performance and performance when the devices are exposed to gamma and neutron radiation environments. Device models have been developed for two NAND gates, two flip-flops, one four-bit Shift Register, a Monostable Multivibrator, an AND-OR-INVERTER, and two operational amplifiers. All models are demonstrated to agree with observed laboratory performance for conditions of pulsed gamma radiation of 3×10^{10} rads (Si)/Second. Neutron fluence levels of 1.2×10^{14} neutrons per square centimeter, as well as non-radiation conditions. The "black box" technique is employed for model development. The model descriptions were developed for use with the SCEPTRE circuit analysis program.

DD FORM 1 NOV 65 1473

UNCLASSIFIED

Security Classification

UNCLASSIFIED
Security Classification

14. KEY WORDS	LINK A ROLE	LINK A WT	LINK B ROLE	LINK B WT	LINK C ROLE	LINK C WT
Modeling						
Integrated circuits						
Computer aided circuit analysis						
SCEPTRE						

UNCLASSIFIED
Security Classification

AFWL-TR-72-42

SIMPLIFIED MODELING OF INTEGRATED CIRCUITS FOR RADIATION PERFORMANCE PREDICTION

J. R. Greenbaum

General Electric Company

TECHNICAL REPORT NO. AFWL-TR-72-42

Approved for public release; distribution unlimited.

ic

FOREWORD

This report was prepared by the General Electric Company, Syracuse, New York, under Contract F29601-71-C-0049. The research was performed under Program Element 61102H, Project 5710, Subtask TB027, and was funded by the Defense Nuclear Agency (DNA).

Inclusive dates of research were February 1971 through February 1972. The report was submitted 16 October 1972 by the Air Force Weapons Laboratory Project Officer, Captain Robert J. Horen (ELT).

This technical report has been reviewed and is approved.

ROBERT J. HOREN
Captain, USAF
Project Officer

CARL F. PORTER
Lt Colonel, USAF
Chief, Transient Radiation
Effects Branch

CARL F DAVIS
Colonel, USAF
Chief, Electronics Division

ABSTRACT

This report describes a simple method for developing computer models for digital and analog integrated circuits. The models are capable of allowing computer prediction of both normal performance and performance when the devices are exposed to gamma and neutron radiation environments.

Device models have been developed for two NAND gates, two flip-flops, one four-bit Shift Register, a Monostable Multivibrator, an AND-OR-INVERTER, and two operational amplifiers. All models are demonstrated to agree with observed laboratory performance for conditions of pulsed gamma radiation of 3×10^{10} rads (Si)/Second. Neutron fluence levels of 1.2×10^{14} neutrons per square centimeter, as well as non-radiation conditions.

The "black box" technique is employed for model development. The model descriptions were developed for use with the SCEPTRE circuit analysis program.

(Distribution Limitation Statement A)

TABLE OF CONTENTS

Section	Title	Page
I	INTRODUCTION	1
II	TEXAS INSTRUMENTS RSN54L00 NAND GATE	3
III	FAIRCHILD 9704 FOUR-INPUT NAND GATES	21
IV	FAIRCHILD 9774-D FLIP-FLOP	35
V	TEXAS INSTRUMENTS RSN54L72 FLIP-FLOP	59
VI	FAIRCHILD 9780 SHIFT REGISTER	97
VII	TEXAS INSTRUMENTS RSN54L122 MONOSTABLE MULTIVIBRATOR	127
VIII	TEXAS INSTRUMENTS RSN54L57 AND-OR INVERT GATE	155
IX	HARRIS HA 2700 OPERATIONAL AMPLIFIER	169
X	FAIRCHILD μAMP A744	185
APPENDIXES		
I	INTRODUCTION TO INDIVIDUAL DEVICE TESTS	197
II	RSN54L00 NAND GATE	203
III	FAIRCHILD 9704 FOUR-INPUT NAND GATES	208
IV	FAIRCHILD 9774-D FLIP-FLOP	211
V	RSN54L72 FLIP-FLOP	220
VI	FAIRCHILD 9780 SHIFT REGISTER	227
VII	RSN54L122	234
VIII	RSN54L57	244
IX	HA-2700	251
X	FAIRCHILD μAMP A744	257

LIST OF ILLUSTRATIONS

Figure	Title	Page
II-1	Logic Representation and Schematic Diagram	5
II-2	Gate Propagation Delay Times	5
II-3	RSN54L00 Model	6
II-4	Computer Model Description	7
II-5	Model Subprogram	7
II-6	Test Circuit	8
II-7	Test Circuit — Computer Description	8
II-8	Input Signal	9
II-9	Output Response	9
II-10	Simulated Gamma Radiation Pulse	12
II-11	Output Response to Gamma Radiation	12
II-12	Simulated Gamma Radiation Pulse	13
II-13	Response to Gamma Radiation	13
II-14	Response to Gamma Radiation	14
II-15	Response to Gamma Radiation	14
II-16	Gamma Radiation — Test Circuit Description	15
II-17	Neutron Radiation — Circuit Transfer Function	17
II-18	Model Description With Neutron Effects	18
II-19	Neutron Radiation — Test Circuit Description	18
II-20	Response to Neutron Radiation	19
II-21	Response to Neutron and Gamma Radiation	20
III-1	Logic Representation and Electrical Schematic	22
III-2	Gate Propagation Delay Times	22
III-3	Computer Model	24
III-4	Computer Model Description	25
III-5	Model Subprogram	25
III-6	Test Circuit	27
III-7	Test Circuit — Computer Description	27
III-8	Input Signal	28
III-9	Output Response	28
III-10	Simulated Gamma Radiation Pulse	29
III-11	1 Response to Gamma Radiation	29
III-12	0 Response to Gamma Radiation	30
III-13	Gamma Test Circuit Description	30
III-14	Neutron Radiation — Circuit Transfer Function	32
III-15	Model Description With Neutron Effects	33
III-16	Neutron Radiation Test Circuit Description	33
III-17	Response to Neutron Radiation	34
IV-1	Schematic — 9774	36
IV-2	Logic Representation	36
IV-3	Flip-Flop Switching Times	38
IV-4	PRESET/CLEAR Propagation Delay Times	38
IV-5	D Flip-Flop Model	40
IV-6	Computer Model Description	41
IV-7	Model Subprogram	41
IV-8	Test Circuits	43
IV-9	Test Circuit Description for SET and RESET	44

LIST OF ILLUSTRATIONS (Continued)

Figure	Title	Page
IV-10	SET Input Signal	45
IV-11	RESET Input Signal	45
IV-12	Q-Output	46
IV-13	Q-Output	46
IV-14	Test Circuit Description for CLOCK and SIGNAL	47
IV-15	CLOCK Input Signal	48
IV-16	Input Signal	48
IV-17	Q-Output	49
IV-18	Q-Output	49
IV-19	Computer Model Description With Gamma Effects	51
IV-20	Gamma Radiation - Test Circuit Description	51
IV-21	Simulated Gamma - Signal Timing Conditions	52
IV-22	Q-Response for Condition 11	52
IV-23	Q-Response for Condition 11	53
IV-24	Clock Input Signal for Gamma Radiation Simulations	53
IV-25	Q-Response for Conditions 8 and 10	55
IV-26	Q-Response for Conditions 8 and 10	55
IV-27	Neutron Radiation - Circuit Transfer Function	56
IV-28	Model Description With Neutron Effects	57
IV-29	Neutron Radiation - Test Circuit Description	57
IV-30	Q-Response to Neutron Radiation	58
IV-31	Q-Response to Neutron Radiation	58
V-1	Schematic RSN54L72 Master-Slave Flip-Flop	60
V-2	Functional Logic Representation	61
V-3	Logic Diagram	64
V-4	RSN54L72 Device Model #1	64
V-5	Clock Timing	65
V-6	Q Output Without Radiation	65
V-7	Q Output With Radiation	66
V-8	Q Output Without Radiation	66
V-9	Q Output With Radiation	67
V-10	Computer Description - Model #1	68
V-11	Model Subprogram	69
V-12	Test Circuit - Computer Description	70
V-13	Computer Model #2	72
V-14	Computer Description - Model #2	73
V-15	Model Subprogram	73
V-16	Test Circuit	76
V-17	Test Circuit Description for SET and RESET Inputs	77
V-18	CLOCK Input Signal	77
V-19	SET Input Signal	78
V-20	RESET Input Signal	78
V-21	Q-Response	79
V-22	Q-Response	79
V-23	Test Circuit Description for J-K Inputs	80
V-24	CLOCK Input Signal	80
V-25	J-Input Signal	81
V-26	K-Input Signal	81

LIST OF ILLUSTRATIONS (Continued)

Figure	Title	Page
V-27	Q-Response	82
V-28	$\bar{Q}$-Response	82
V-29	CLOCK Signal	83
V-30	Q-Response	83
V-31	$\bar{Q}$-Response	84
V-32	Model Description With Gamma Effects	86
V-33	Q-Response for Condition 5	86
V-34	$\bar{Q}$-Response for Condition 5	87
V-35	Q-Response for Condition 2	87
V-36	$\bar{Q}$-Response for Condition 2	88
V-37	Q-Response for Condition 1	88
V-38	$\bar{Q}$-Response for Condition 1	89
V-39	Gamma - Test Circuit Description	89
V-40	Q-Response for Condition 3	90
V-41	$\bar{Q}$-Response for Condition 3	90
V-42	Neutron Radiation - Circuit Transfer Function	91
V-43	Computer Model Description With Neutron Effects	93
V-44	Model Subprogram With Neutron Effects	93
V-45	Neutron Radiation - Test Circuit Description	94
V-46	Output FNVT - Neutron Effects Subroutine	94
V-47	Q-Response to Neutron Radiation	95
V-48	$\bar{Q}$-Response to Neutron Radiation	96
VI-1	Logic Diagram	99
VI-2	Schematic Diagram of Integrated AND and NOR Gates	100
VI-3	SCEPTRE Model of 9780 Device	102
VI-4	Computer Model Description	103
VI-5	Model Subprogram	103
VI-6	Subfunction Logic Diagram	104
VI-7	Shift Register Test Circuit	106
VI-8	Test Circuit Description - CLOCK Trigger	107
VI-9	RESET Input Signal	107
VI-10	CLOCK Input Signal	108
VI-11	Q_0 - Output	108
VI-12	Q_1 - Output	109
VI-13	Q_2 - Output	109
VI-14	Q_3 - Output	110
VI-15	$\bar{Q}_3$ - Output	111
VI-16	Test Circuit Description - Input Trigger	111
VI-17	RESET Input Signal	112
VI-18	J - Input Signal	112
VI-19	K - Input Signal	113
VI-20	Q_0 - Output	113
VI-21	Q_1 - Output	114
VI-22	Q_2 - Output	114

LIST OF ILLUSTRATIONS (Continued)

Figure	Title	Page
VI-23	Q_3 - Output	115
VI-24	$\overline{Q}_3$ - Output	115
VI-25	Gamma Radiation Test Circuit Description	117
VI-26	Q_0 - Response to Gamma Radiation	118
VI-27	Q_1 - Response to Gamma Radiation	118
VI-28	Q_2 - Response to Gamma Radiation	119
VI-29	Q_3 - Response to Gamma Radiation	119
VI-30	$\overline{Q}_3$ - Response to Gamma Radiation	120
VI-31	Computer Model Description With Both Gamma and Neutron Effects	120
VI-32	Neutron Radiation Test Circuit Description	122
VI-33	Q_0 - Response to Neutron Radiation	123
VI-34	Q_1 - Response to Neutron Radiation	123
VI-35	Q_2 - Response to Neutron Radiation	124
VI-36	Q_3 - Response to Neutron Radiation	125
VI-37	$\overline{Q}_3$ - Response to Neutron Radiation	126
VII-1	Schematic RSN54L122 One-Shot	128
VII-2	Logic Diagram	129
VII-3	Model RSN54L122	131
VII-4	Computer Model Description	132
VII-5	Model Subprogram	133
VII-6	Test Circuit	134
VII-7	Test Circuit Description - Leading Edge Trigger	135
VII-8	RESET Input Signal	136
VII-9	B1 Input Signal	136
VII-10	Q - Output	137
VII-11	$\overline{Q}$ - Output	137
VII-12	Test Circuit Description - Falling Edge Trigger	138
VII-13	A1 Input Signal	139
VII-14	Q - Output	139
VII-15	$\overline{Q}$ - Output	140
VII-16	Test Circuit - With External Timing Components	141
VII-17	Test Circuit Description	142
VII-18	A1 Input Signal	143
VII-19	Q - Output	143
VII-20	$\overline{Q}$ - Output	144
VII-21	Test Circuit Description	145
VII-22	B1 Input Signal	146
VII-23	Q - Output	146
VII-24	$\overline{Q}$ - Output	147
VII-25	Computer Model Description With Gamma Effects	148
VII-26	Gamma Test Circuit Description	148
VII-27	B1 Input Signal	149

LIST OF ILLUSTRATIONS (Continued)

Figure	Title	Page
VII-28	Q - Response to Gamma Radiation	150
VII-29	$\overline{Q}$ - Response to Gamma Radiation	150
VII-30	Neutron Radiation - Circuit Transfer Function	151
VII-31	Computer Model Description With Neutron Effects	152
VII-32	Neutron Test Circuit Description	153
VII-33	Q - Response to Neutron Radiation	154
VII-34	$\overline{Q}$ - Response to Neutron Radiation	154
VIII-1	Logic Diagram	155
VIII-2	Schematic RSN54L57	155
VIII-3	Computer Model	157
VIII-4	Computer Model Description	158
VIII-5	Model Subprogram	159
VIII-6	Test Circuit	160
VIII-7	Test Circuit Description	161
VIII-8	A Input Signal	161
VIII-9	D Input Signal	162
VIII-10	Device Response	162
VIII-11	1 Response to Gamma Radiation	163
VIII-12	0 Response to Gamma Radiation	164
VIII-13	Gamma Radiation Test Circuit Description	165
VIII-14	Neutron Radiation - Circuit Transfer Function	166
VIII-15	Neutron Radiation Test Circuit Description	167
VIII-16	Device Response to Neutron Radiation	168
IX-1	Published Electrical Characteristics	169
IX-2	HA 2700 Model - Linear Model	170
IX-3	Open Loop Gain - Bode Plot	171
IX-4	Computer Description - Linear Model	172
IX-5	Close Loop Gain - 0 dB - Bode Plot	173
IX-6	HA 2700 Model - Non-Linear Model	174
IX-7	Computer Description - Non-Linear Model	174
IX-8	Model Subprogram	175
IX-9	Test Circuit and Computer Description	176
IX-10	Input Signal	177
IX-11	Output Response	177
IX-12	Observed Device Response	178
IX-13	Output Response to Gamma Radiation	179
IX-14	Gamma Function Subprogram	180
IX-15	Model Description With Gamma Effects	181
IX-16	Gamma Radiation - Test Circuit Description	181
IX-17	Model Description With Neutron Effects	183
IX-18	Neutron Radiation - Test Circuit Description	183
IX-19	Response to Neutron Radiation	184
X-1	μA744 Schematic	185
X-2	Op-Amp Frequency Response	186
X-3	μA744 Linear Model	186
X-4	Open Loop Gain - Bode Plot	187

LIST OF ILLUSTRATIONS (Continued)

Figure	Title	Page
X-5	Computer Description - Linear Model	187
X-6	μA744 Non-Linear Model	188
X-7	Computer Description - Non-Linear Model	188
X-8	Input Signal	189
X-9	Output Response	189
X-10	Test Circuit and Computer Description	190
X-11	Model Description With Gamma Effects	191
X-12	Output Response to Gamma Radiation	192
X-13	Effect of Neutron Irradiation on Open-Loop Voltage Gain	193
X-14	Model Description With Neutron Effects	194
X-15	Neutron Radiation - Test Circuit Description	195
X-16	Response to Neutron Radiation	196

LIST OF TABLES

Table	Title	Page
II-1	Truth Table	4
II-2	Electrical Characteristics	4
III-1	Electrical Characteristics	21
IV-1	Truth Table	35
IV-2	Electrical Characteristics	37
V-1	Truth Table	62
V-2	Electrical Characteristics	62
V-3	Delay Times	84
VI-1	Truth Table	98
VI-2	Electrical Characteristics for 9780 Device	101
VI-3	Switching Characteristics for 9780	106
VI-4	Computer Time Delays	116
VII-1	Truth Table	129
VII-2	Electrical Characteristics	130
VIII-1	Electrical Characteristics	156

SECTION I

INTRODUCTION

The program described in this report had as its objective the development of simplified models for linear and digital integrated circuits which would be suitable for use with the SCEPTRE computer program. These models were designed to account for normal electrical performance as well as performance in an environment of ionizing and/or neutron radiation. Techniques were established to derive models capable of representing both the radiation effects and the first order transient response of the microcircuits as system components.

Acceptable computer models have long been available for individual transistors and diodes. Although reasonably complex, these models require a relatively small amount of computer time and are practical for general usage. On the other hand, the existing method of modeling integrated circuits has provided models which are so complex as to be impractical for most applications. This method uses the same procedures employed for the transistor, and thus requires a detailed description of each semiconductor junction. The Fairchild 9774-D Flip-Flop, for example, requires data for 54 transistor junctions and four diode junctions, requiring computer evaluation of approximately 200 complex relationships. In short, the existing method of modeling integrated circuits has two major shortcomings:

1) Computer/circuit analysis program limitations generally preclude simultaneous analyses of two or more integrated circuit functions.

2) Existing computer mathematical techniques require excessive Central Processor Unit (CPU) computer time for large circuits, making this approach uneconomical.

The Air Force Weapons Laboratory was fully cognizant of these two deficiencies when it specified its requirements for the development of simplified models for integrated circuits.

The models which have been developed meet the objectives toward which the program was directed. These models are simply described; they are easily used with the computer program (SCEPTRE), and they account for both normal electrical performance and performance in an ionizing and neutron radiation environment. Exact computer duplication of observed laboratory results has not been attempted. It is felt that the computer output results obtained are sufficiently in agreement with the observed measurements and that more precise matching would be a mechanical process which would be both time consuming and uneconomical. However, all of the device models can be used as described, to predict circuit performance with reasonable assurance that the analysis results will represent normal results.

Several approaches were used in the development of the many devices that have been modeled. This diversity of modeling procedure was deliberate. It represents an effort to evaluate whether any single approach might prove to be more desirable, more efficient, or more economical. To this end, the model descriptions reflect three alternative approaches: (1) use of expressions for certain device behavior effects rather than the use of subprograms or functions; (2) inclusion of radiation effects in the model description rather than in the overall circuit description; (3) combinations of the first two alternatives. Early evaluation indicates no single alternative or combination to be superior.

As a consequence of attempting several modeling approaches, none of the model descriptions is in its simplest form. It is felt that CPU analysis time can be reduced with some small additional effort such as reducing the number of elements in the description, using the expression format in place of some of the equations and subprograms, and generally evaluating the manner in which each device was modeled.

This report includes an introductory appendix (Appendix I) as well as a separate appendix for each of the devices modeled. Appendix I provides information concerning all of the devices, such as typical radiation test circuit schematics, photographs of the test installation, a listing of the number of integration steps required by the various models, etc.

Each appendix for a specific device contains a flow chart of the subprograms associated with that device, as well as the radiation test results of a single "representative" sample of the device type.

Due to the manner of configuring the device models, a "computational delay" statement will sometimes be printed. In most instances, the diagnostic is associated with the output impedance resistor, which has a small value; thus this condition does not result in an error of any consequence and may be ignored. Also, due to an idiosyncrasy of the GE 635, a diagnostic statement occurs that is associated with an output step size (XSTPSZ) request. This also should be ignored since the request is honored. Unfortunately, however, due to this condition, the step size is not available for use in the subprograms as an equation argument. Therefore, in the HA2700 operational amplifier subprogram it was necessary to simulate this condition.

SECTION II

TEXAS INSTRUMENTS RSN54L00 NAND GATE

This integrated circuit is a quad, two input positive logic NAND gate. The circuit behaves in such a manner that when the signal on both the inputs is at a logic 1 level, the output is a logic 0. For all other input signal conditions, the output is at a logic 1 level. The truth table describing this behavior is shown in Table II-1.

The logic representation for the quad and the schematic diagram of each of the four gates, is shown in Figure II-1. The electrical characteristics of the device, as defined by the manufacturer, are shown in Table II-2.

The voltage wave forms describing the device behavior and delay characteristics are shown in Figure II-2.

A. MODEL DEVELOPMENT

The computer model that has been developed to duplicate observed performance is shown in Figure II-3 and its computer description in Figure II-4. The subprogram which establishes the logic output signal level and the delay characteristics is shown in Figure II-5. It will be noted in Figure II-5 that provision is made to include the effects of output impedance variation in the model, since this information was available. However, the results of function FR2, which represents a rough approximation of the impedance changes, has not been included in the final model.

The signal input impedances, JA and JB, are represented as zero valued current sources. In SCEPTRE, this implies that the input signal terminals A and B have infinite impedance (although the gates have measurable and varying impedance values which depend upon the applied signal level). This, as a first order approximation, will provide reasonably accurate results. For greater accuracy, the current sources JA and JB should be modeled as "tabled" functions of current versus applied voltages in SCEPTRE. This method will provide a realistic device input impedance representation.

As indicated on Figure II-3 and described on Figure II-4, the voltage associated with the dependent source E1 is determined by the function FN2. This function establishes the value of E1 voltage in accordance with the truth table (Table II-1). As shown in Figure II-5, if either of the input signals is less than or equal to 0.8 volt, then E1 is set equal to 3.1 volts which represents a logic 1.

When both of the input signals are equal to or greater than 1.9 volts, the value of E1 is established as 0.3 volt which represents a logic 0.

If neither of these conditions exists, then E1 is determined to be 3.1 volts minus the absolute value of the smaller of the two applied signals. (The values associated with the function FN2 have been obtained either from published data, Table II-2, or from laboratory tests.)

TABLE II-1.

TRUTH TABLE

INPUT		OUTPUT
1	2	
0	0	1
1	0	1
0	1	1
1	1	0

TABLE II-2.

ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range, unless otherwise noted)

PARAMETER		TEST CONDITIONS*	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = Min. $V_{out(0)}$ = 0.3V	1.9			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{CC} = Min. $V_{out(1)}$ = 2.4V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = Min. V_{in} = 0.8V I_{load} 100 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = Min. V_{in} = 1.9V I_{sink} 2 mA			0.3	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = Max. V_{in} = 0.3V			-0.18	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = Max. V_{in} = 2.4V			10	μA
		V_{CC} = Max. V_{in} 5.5V			100	μA
I_{OS}	Short circuit output current	V_{CC} = Max. V_{in} = 0 V_{out} = 0	-1		-15	mA
$I_{CC(0)}$	Logical 0 level supply current (each gate)	V_{CC} = 5V V_{in} = 5 V			0.46	mA
$I_{CC(1)}$	Logical 1 level supply current (each gate)	V_{CC} = 5V V_{in} 0			0.18	mA
tpd0	Propagation delay time to logical 0 level	C_1 - 50 pF. V_{CC} = 5V, T_A = 25°C			60	ns
tpd1	Propagation delay time to logical 1 level	C_1 = 50 pF. V_{CC} = 5V, T_A = 25°C			60	ns

*For conditions shown as Min. or Max. use Min = 4.5V, Max. - 5.5V

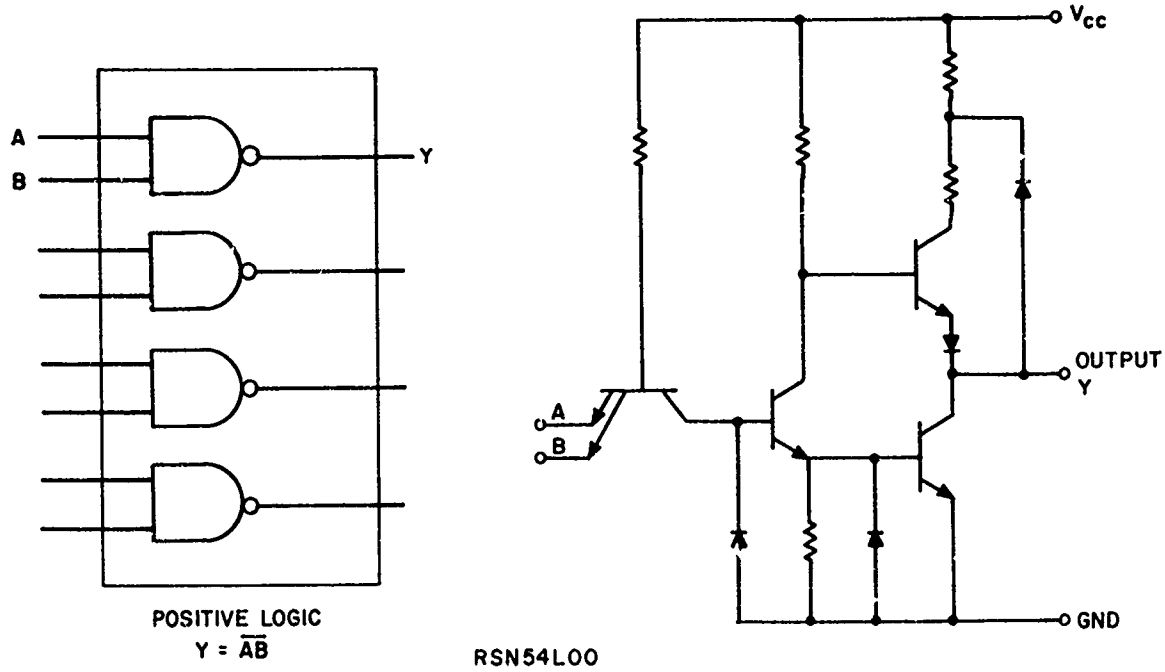


Figure II-1. Logic Representation and Schematic Diagram

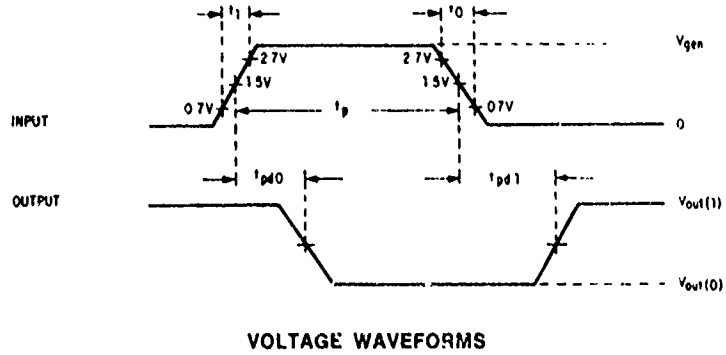


Figure II-2. Gate Propagation Delay Times

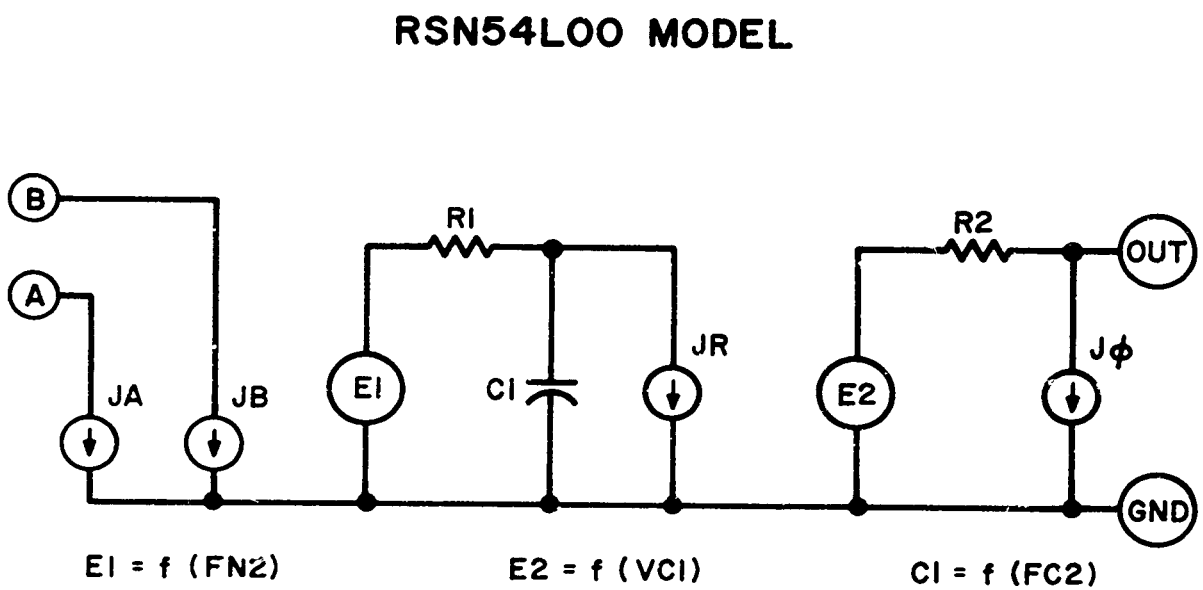


Figure II-3. RSN54L00 Model

```
MODEL LOU(A-B-OUT-GND)
2 INPUT NAND GATE
A = INPUT A
B = INPUT B
J GREENBAUM 5-13-71
ELEMENTS
JA,A-GND=0.
JB,B-GND=6.
JO,OUT-GND=0.
C1,GND-1=FN2(VJA,VJB,0.8,3.1,1.9,0.3)
R1,1-2=100.
C1,2-GND=FC2(E1,E2,550.E-12,300.E-12)
JR,2-GND=0.
E2,GND-3=X1(VC1)
R2,3-OUT=30.
FUNCTIONS
TABLE 1
-0..0..1..0..
OUTPUTS
VJA,VJB
E1,E2,VC1,VJO,C1,PLOT
```

Figure II-4. Computer Model Description

```
0102T 02   05-19-71   12.455        QUAD 2 INPUT NAND GATE LEVEL SELECT

                                          5-6-71

      CFN2              QUAD 2 INPUT NAND GATE LEVEL SELECT
      C                 5-6-71
                  FUNCTION FN2(A,B,C,D,E,F)
      C           A=VJA  B=VJB  C=0.8
      C           D=3.1  E=1.9  F=0.3
                  IF(A .LE. C .OR. B .LE. C) GO TO 4
                  IF(A .GE. E .AND. B .GE. F) GO TO 5
                  FN2=D-AMIN1(A,B)
                  RETURN
        4         FN2 = D
                  RETURN
        5         FN2 = F
                  RETURN
      C
      CFC2                CAPACITOR SELECTION
                  ENTRY FC2(A,B,C,D)
      C           A=E1   B=E2   C=550PF   D=300PF
                  G=C
                  IF(A .LE. B)G=D
                  FN2 = G
                  RETURN
      C
      CFR2                RESISTOR SELECTION
                  ENTRY FR2(A,B,C,D)
      C           A=30   B=613   C=VC1   D=TABLE 1
      C           FOR 0, R=30   FOR 1, R=613   FOR RAD, R=F(INPT)
                  R=B
                  IF(C .LT. .5)R=A
                  FN2 =R
      C
                  RETURN
                  END

   23533 WORDS OF MEMORY USED BY THIS COMPILATION
```

Figure II-5. Model Subprogram

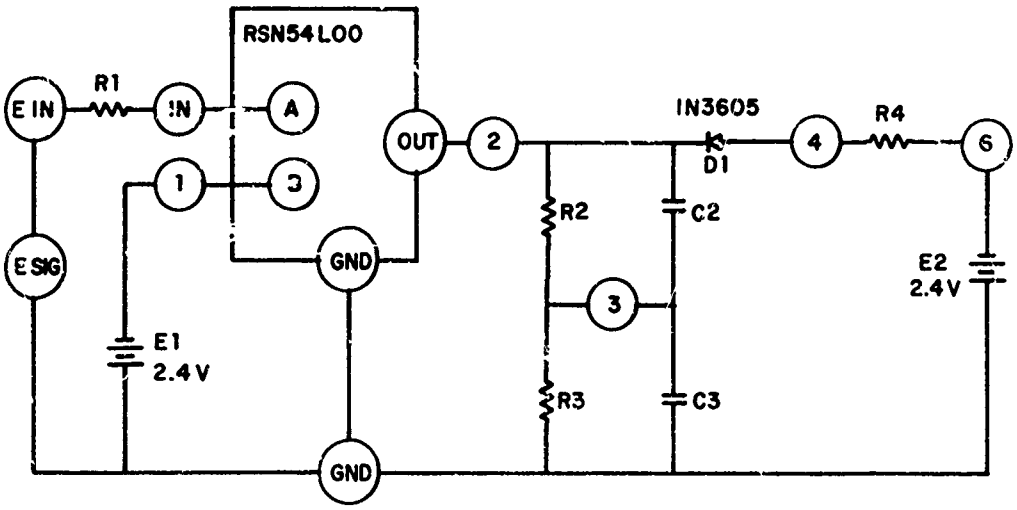


Figure II-6. Test Circuit

```
TEST CIRCUIT FOR RSN54L00 2 INPUT NAND GATE
RAD MODEL AND AFWL CIRCUIT
STORED AS R54L00\###
ELEMENTS
NA,IN-1-2-GND=MODEL L00 (CHANGE JR=P1)
R2,2-3=4300.
C2,2-3=2.6E-12
R3,3-GND=750
C3,3-GND=15.E-12
D1,2-4=MODEL 1N3605 (PERM)
R4,4-5=800.
R5,6-5=1.
E2,GND-6=2.4
ESIG,GND-FIN=01(.3,3.,0.,19.E-9,331.E-9,19.E-9,750.E-9,1.,TIME)
R1,FIN-IN = 50.
E1,GND-1=2.4
DEFINED PARAMETERS
P1=02(TABLE 3(VCINA),TABLE 2(TIME))
FUNCTIONS
TABLE 3=0.,-.5, .3,-.5, 1.0,1., 2.4,1.1, 3.,1.2, 5.,1.2
TABLE 2 = 0.,0.
 800.E-9,0.
 815.E-9,0.
 825.E-9,0.
 840.E-9,0.
 990.E-9,0.
01(A,B,C,D,E,F,G,H,Y)=(FGEN(A,B,C,D,E,F,G,H,Y))
02(A,B)=(A*B)
RUN CONTROLS
STOP TIME = 999.E-9
MAXIMUM PRINT POINTS = 300
OUTPUTS
ESIG,JRNA(IPP),PLOT
VR2,VCUD1,PLOT
RERUN DESCRIPTION(1)
```

Figure II-7. Test Circuit — Computer Description

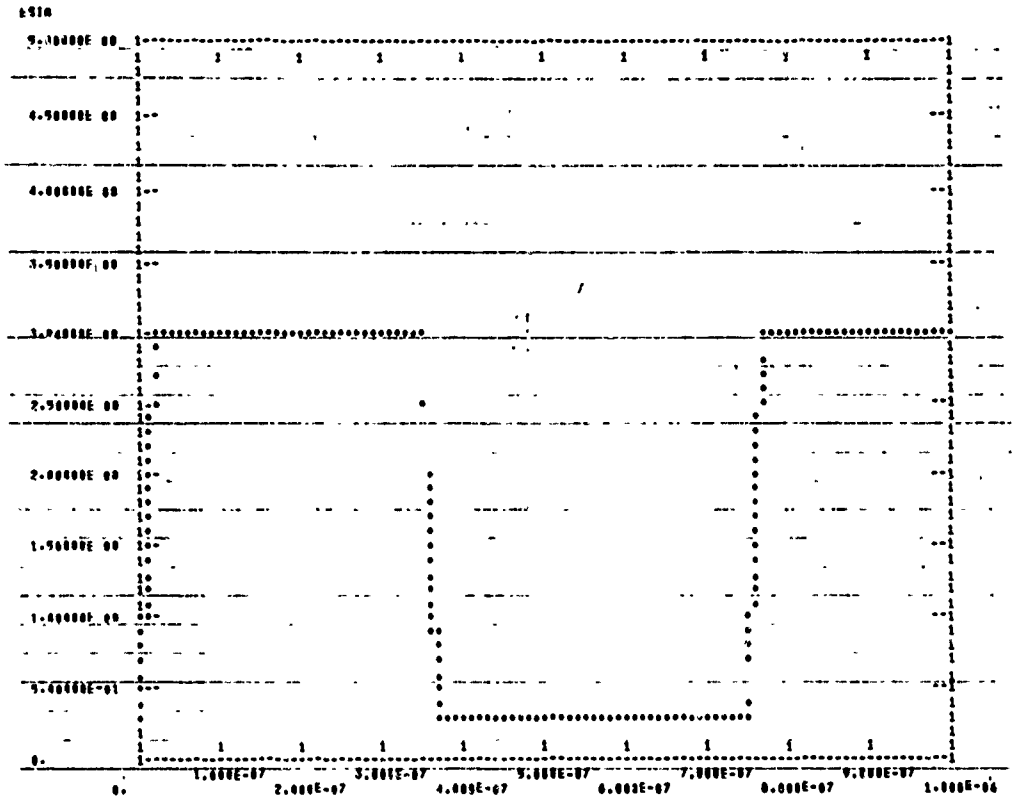


Figure II-8. Input Signal

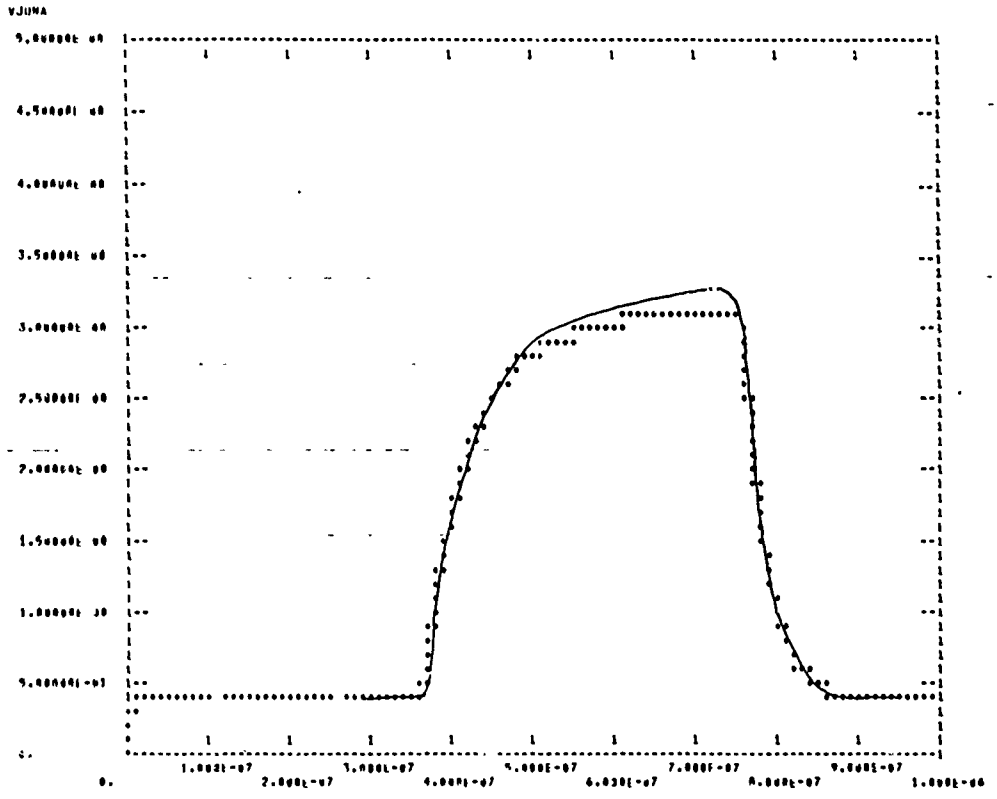


Figure II-9. Output Response

Although the device manufacturer indicates on Table II-2 that the switching delay times for either positive or negative going outputs signals will be no greater than 60 nanoseconds, laboratory test measurements on many units indicate not only that both delays are shorter than this worst case value, but that they are different from each other. Therefore, the delay times t_{pd0} and t_{pd1} are established in the model by the time constant R1 - C1. This time constant is changed by varying the value of C1 depending upon whether a logic 1 or 0 is required as an output signal.

The value of C1 is determined by means of subprogram FC2. Thus, C1 is set to 550 picofarads unless E1 is less than or equal to E2. When this latter condition occurs, C1 assumes the value of 300 picofarads. Since the output voltage E2 is equal to the voltage across the capacitor C1 (JR, a zero valued current source required by SCEPTRE for dc circuit evaluation conditions, is in parallel with C1), a relationship between the input signal levels and the output voltage is readily established. JR is also used as a source of gamma radiation injection in the model, when required. The FORTRAN flow charts associated with these two functions are shown in Appendix II-A.

The output impedance of the device is fixed at 30 ohms. Although this is not an accurate impedance representation for all voltage and load conditions, it provides first order accuracy of output signal level.

The zero valued current source, JO, is a dummy element to permit monitoring the device output signal under varying conditions.

The four terminals required for normal usage of the gate are defined on Figure II-3 as A for the "A" input signal, B for the "B" input signal, OUT for the output signal, and GND as the ground connection.

B. MODEL VERIFICATION

To demonstrate the validity of the model, the circuit shown in Figure II-6 was described to the computer. This circuit, which is one of several standards for laboratory measurement, allows for easy variation of load (fanout) as well as simple impedance matching for monitoring equipment. For the particular tests conducted, an oscilloscope was connected between node 3 and ground. The topological description of the circuit for the SCEPTRE circuit analysis program, is shown in Figure II-7.

The results of the computer analysis of the model are presented in Figures II-8 and II-9. Figure II-8 shows the timing for one of input signals as it varies between the logic 1 and 0 levels. The truth table (Table II-1) indicates that the output should be a logic 1 during the time when the signal is at a 0 level and vice versa. Figure II-9 indicates the model response to the described signal condition. The solid line drawn on the computer printout in Figure II-9 gives the observed results of the laboratory measurements for the same operating conditions.

C. RADIATION EFFECTS

1. GAMMA RADIATION

Exposing the device to a nuclear radiation environment may affect normal performance by causing the output signal level to vary. When exposed to pulsed

gamma radiation at dose rate levels of approximately 3 x 10^{+10} rads (Si)/second, the performance is only momentarily affected. Extensive testing was done by the General Electric Company. The test report with photographic recording of the results is included in Appendix II-B.

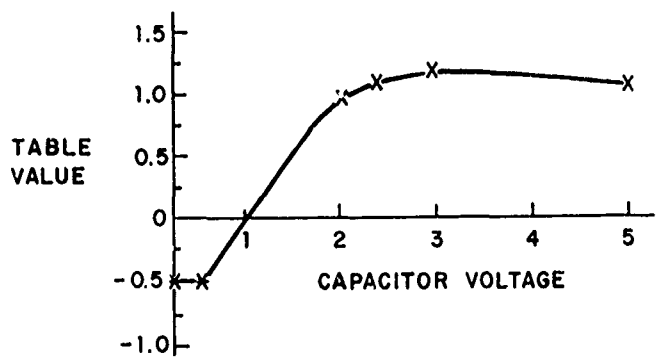
When a gamma radiation pulse simulation is caused to occur at about 0.720 microsecond (Figure II-10), the output response of the device is momentarily reduced. Figure II-11 shows both the observed and computer response to the radiation pulse.

When the time of simulated radiation is changed to occur at about 0.410 microsecond (Figure II-12), the device behavior is also momentarily reduced. Figure II-13 shows both the observed and computer response to the radiation pulse. Figure II-14 shows another radiation pulse response, with both the observed and computed results presented. The time of occurrence of the radiation pulse is such that the gate output is in the process of returning to a 0 level; consequently the return is hastened.

When the radiation pulse is caused to occur when the gate output is at a 0 level, the normal reaction is for the output level to increase slightly. Figure II-15 shows both the observed and computer results.

The method for simulating the transient effects induced by the pulsed ionizing gamma radiation is to change the value of JR in Figure II-4. As shown on Figure II-16, JR in device NA is redefined as a function of the voltage across capacitor C1 and a signal that is time dependent and represented by Table 2 of Figure II-16; this change is identified as P1. By changing the time entries in this table (as shown in the rerun descriptions), the radiation simulation is caused to occur whenever desired. For rerun No. 1 on Figure II-16, the ionizing pulse simulation occurs between 755 and 795 nanoseconds. Rerun No. 2 simulates the radiation pulse between 390 and 430 nanoseconds; rerun No. 3, the radiation pulse between 760 and 800 nanoseconds.

P1 also references Table 3, which defines the behavior of the device where it is subjected to gamma radiation. It relates the voltage across the capacitor C1 to the observed device response; this relationship was obtained as a result of laboratory testing. Since the output signal is equal to the voltage existing across the capacitor, the desired computer results can be obtained using this voltage instead of E2. The following sketch graphically depicts Table 3 relationships.



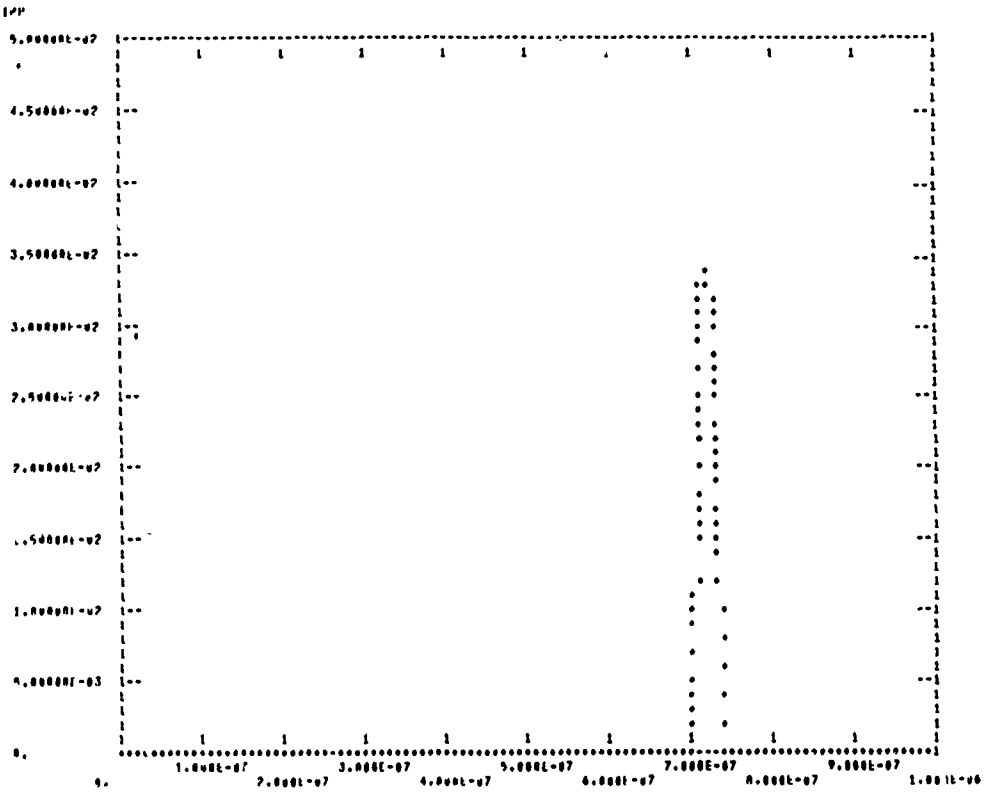


Figure II-10. Simulated Gamma Radiation Pulse

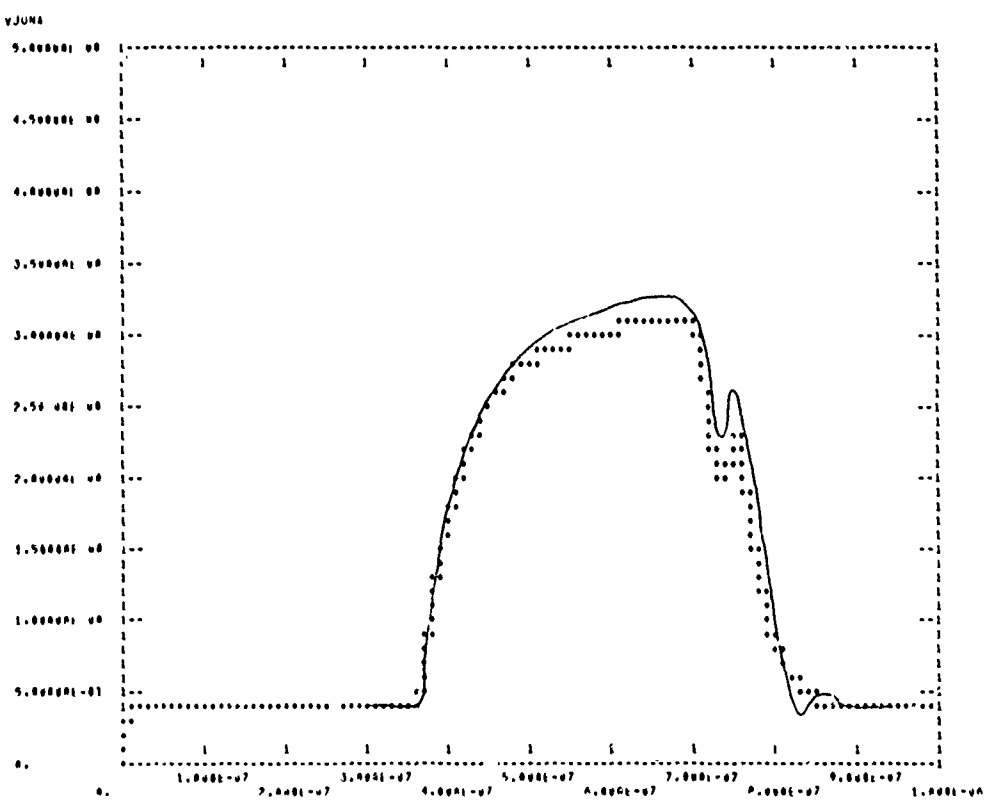


Figure II-11. Output Response to Gamma Radiation

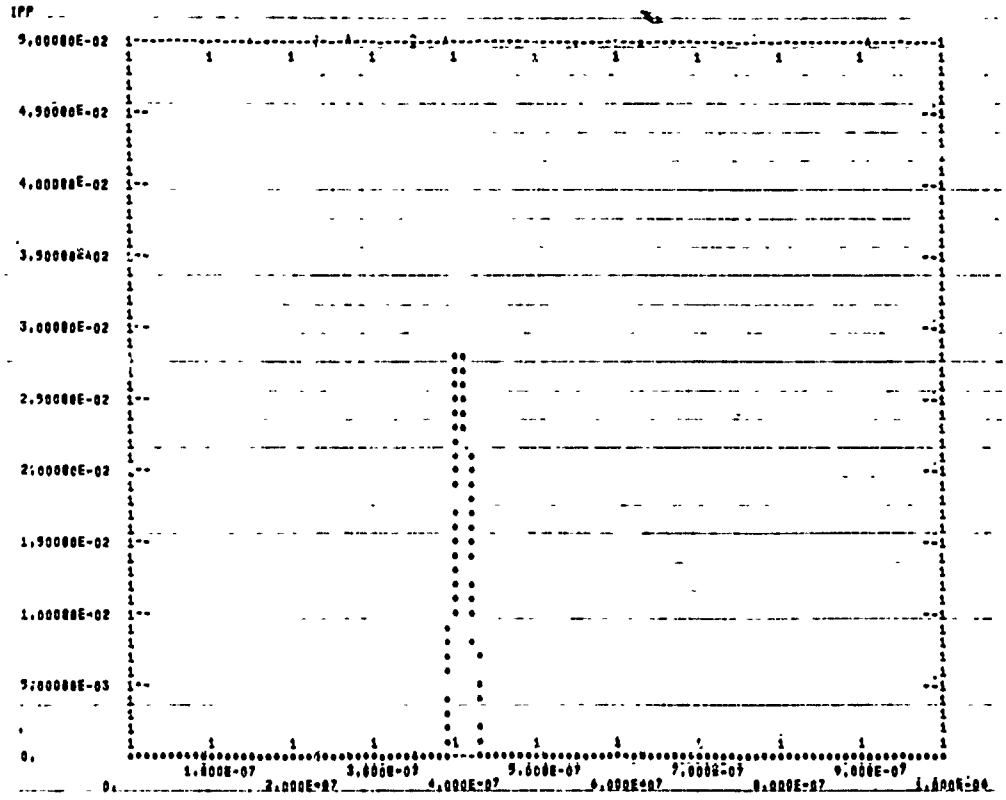


Figure II-12. Simulated Gamma Radiation Pulse

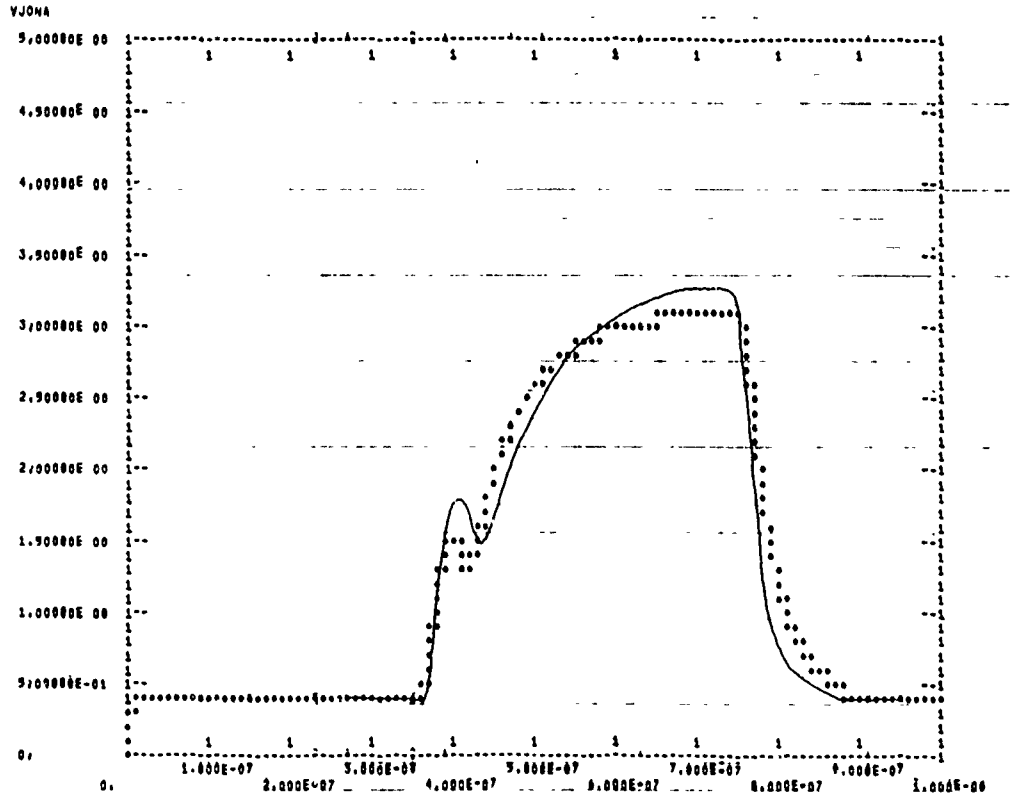


Figure II-13. Response to Gamma Radiation

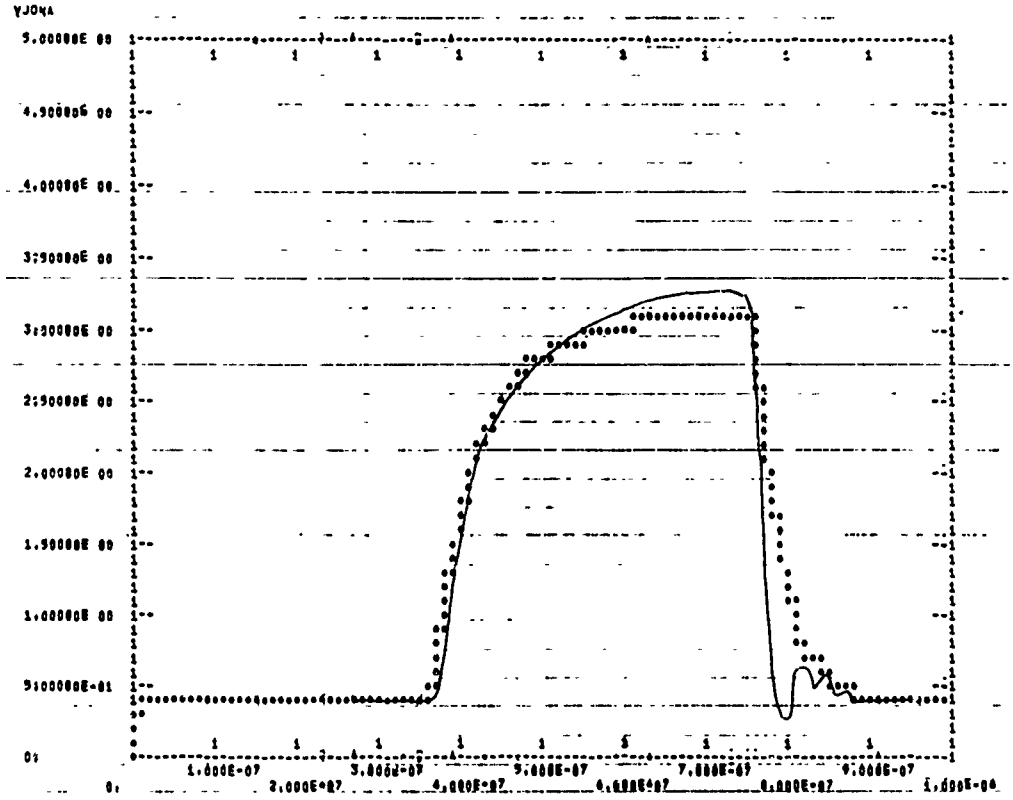


Figure II-14. Response to Gamma Radiation

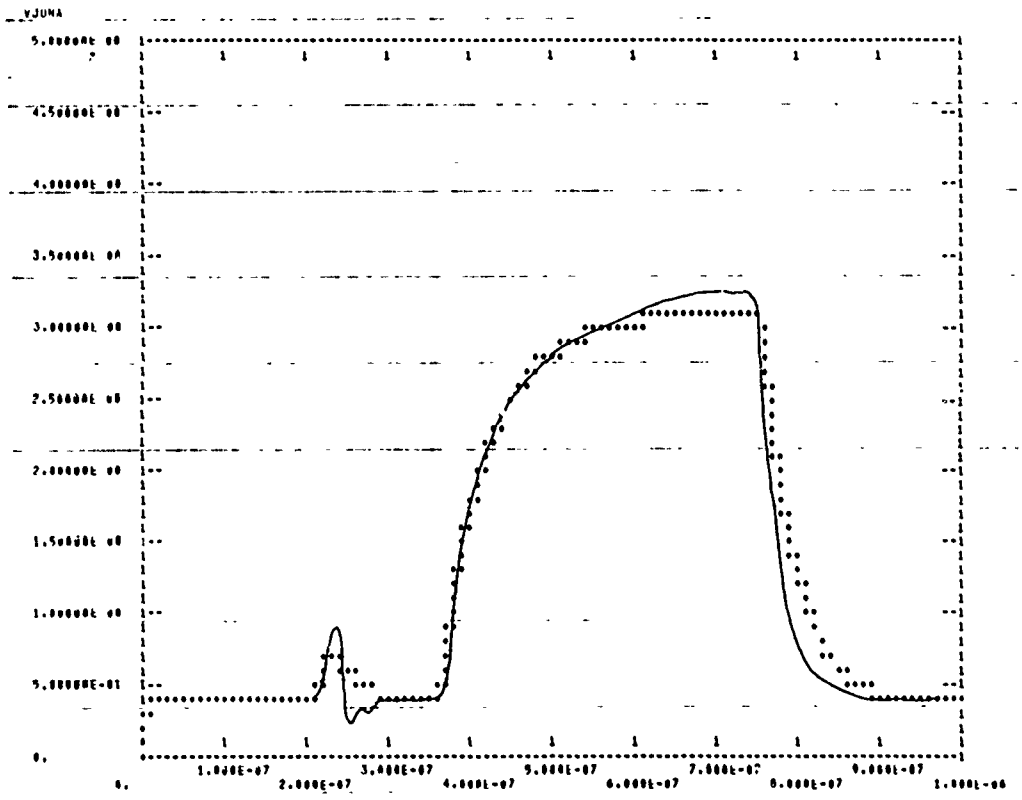


Figure II-15. Response to Gamma Radiation

```
TEST CIRCUIT FOR RSN54L00 2 INPUT NAND GATE
KAU MODEL AND AFWL CIRCUIT
STORED AS R54L00$###
ELEMENTS
NA,IN-1-2-GND=MODEL L00 (CHANGE JR=P1)
R2,2-3=4300.
C2,2-3=2.6E-12
R3,3-GND=750
C3,3-GND=15.E-12
D1,2-4=MODEL 1N3005 (PERM)
R4,4-5=800.
R5,6-5=1.
E2,GND-6=2.4
ESIG,GND-EIN=01(.3,3.,0.,1V.E-9,331.E-9,19.E-9,750.E-9,1.,TIME)
R1,EIN-IN = 50.
E1,GND-1=2.4
DEFINED PARAMETERS
P1=02(TABLE 3(VC1NA),TABLE 2(TIME))
FUNCTIONS
TABLE 3=0.,-.5,.3,-.5,2.,1.,2.4,1.1,3.,1.2,5.,1.2
TABLE 2 = 0.,0.
0.,0.
200.E-9,0.
 215.E-9,0.03
 225.E-9,0.03
240.E-9,0.
500.E-9,0.
01(A,B,C,D,E,F,G,H,Y)=(FGEN(A,B,C,D,E,F,G,H,Y))
02(A,B)=(A*B)
RUN CONTROLS
STOP TIME = 999.E-9
MAXIMUM PRINT POINTS = 300
OUTPUTS
ESIG,JRNA(IPP),VR3,VR5,PLOT
VR2,VCUD1,PLOT
P1,PLOT
RERUN DESCRIPTION(1)

THE TERM 'VR1 ' WILL CAUSE A COMPUTATIONAL DELAY.

FUNCTIONS
TABLE 2 = 0.,0.
755.E-9,0.
 770.E-9,0.03
 780.E-9,0.03
795.E-9,0.
999.E-9,0.
RERUN DESCRIPTION(1)
FUNCTIONS
TABLE 2 = 0.,0.
 390.E-9,0.
 405.E-9,0.03
 415.E-9,0.03
 430.E-9,0.
999.E-9,0.
RERUN DESCRIPTION (1)
FUNCTIONS
TABLE 2 = 0.,0.
 760.E-9,0.
 775.E-9,0.03
 785.E-9,0.03
 800.E-9,0.
 999.E-9,0.
END

SYSTEM NOW ENTERING SIMULATION
```

Figure II-16. Gamma Radiation — Test Circuit Description

After selecting the proper value from the tabled entries (as represented by the sketch), equation Q2 causes it to be multiplied by the value determined from Table 2. Thus except for that interval when the gamma pulse occurs, Table 2 is equal to zero; therefore no change occurs in the current source value.

The figures indicate excellent agreement between the computed results and the laboratory observations.

2. NEUTRON RADIATION

When the device is exposed to neutron radiation conditions, its performance may be degraded either temporarily or permanently. The degree of the degradation as well as the device recovery time, for those conditions which permit recovery, depends upon the exposure level.

Exposure of test circuits to fluence levels of 1.2×10^{14} results in an output level reduction of approximately 0.4 volt, when the signal is at a 1 level. The results were observed by the Air Force Weapons Laboratory when they tested these devices and are reported in Reference 1.* Figure II-17 presents the circuit transfer function degradation observed during these tests, for various fluence levels. For condition 4, which represents the fluence level 1.2×10^{14}, the output signal level drops from about 3.1 volts to approximately 2.7 volts.

The method for incorporating this response change into the model is shown on Figure II-18. The value of the output voltage, E2, is changed from a simple dependency on the voltage across capacitor, C1, to a dependency upon both the capacitor voltage and the fluence level, P1. In this instance, the radiation effects reduce the value of the voltage across C1 by 0.4 volt for all values of voltage.

The computer description to produce an analysis of the device in the test circuit configuration is shown in Figure II-19. The computer provides analyses for both neutron fluence effects and the compounding of fluence and gamma radiation conditions. The results of the analyses are shown in Figures II-20 and II-21, respectively. In each output it can be seen that the positive signal level is reduced from that observed in Figures II-9 and II-11, which represents normal circuit performance.

This method of including fluence effects represents a gross approximation of curve 4 of Figure II-17. A more sophisticated representation would be to describe curve 4 mathematically and allow P1 to represent the resulting equation. However, the present model does demonstrate a satisfactory procedure for incorporating these conditions into the device model description.

---

* R. J. Olson, D. R. Alexander, R. J. Antinone, "Radiation Response Study of New Radiation-Hardened Low Power TTL Series", IEEE Transactions on Nuclear Science, Vol. N. S. 18-No. 6, pp 243-249, December 1971

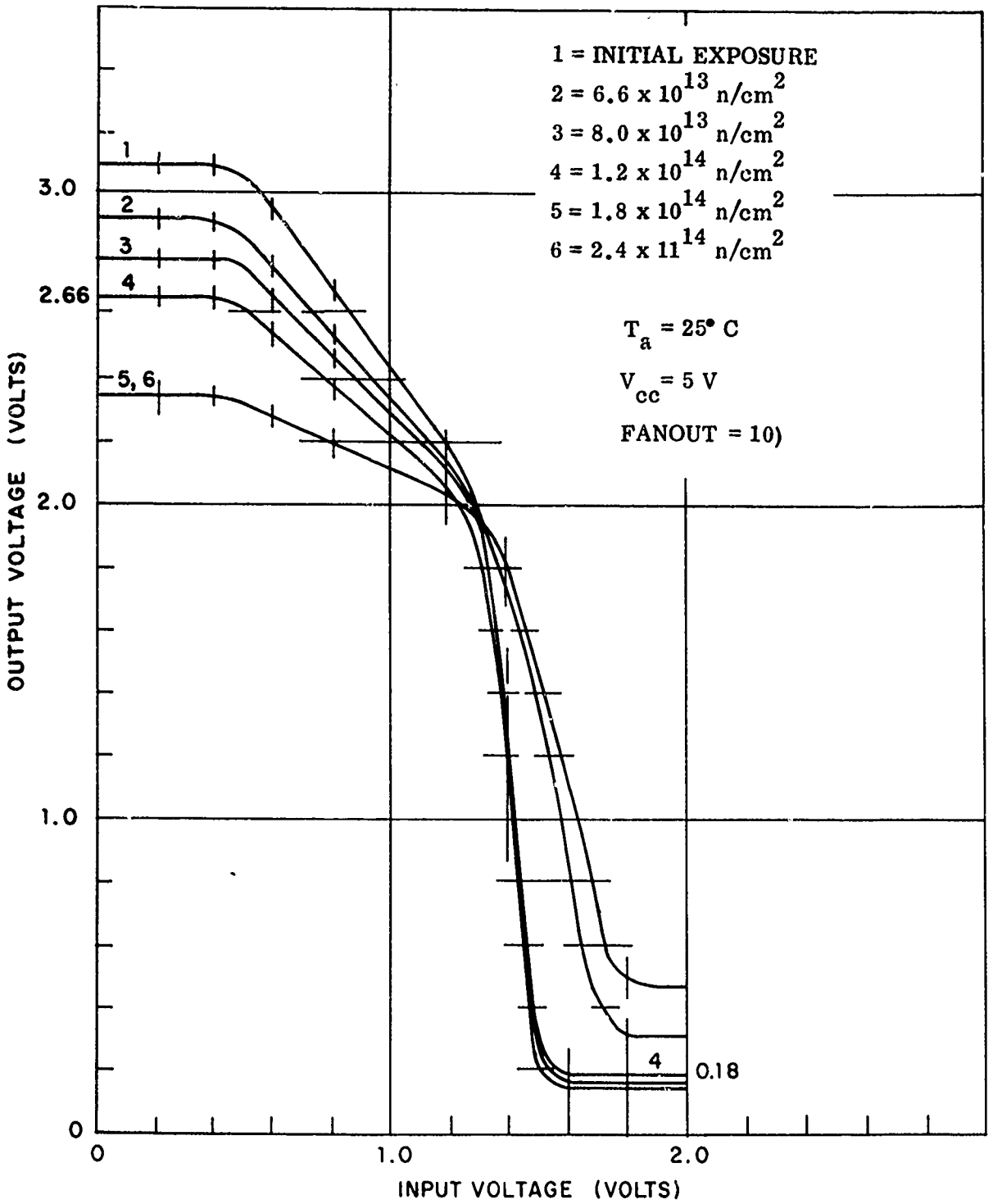


Figure II-17. Neutron Radiation — Circuit Transfer Function

```
MODEL L00(A-B-OUT-GND)
2 INPUT NAND GATE
A = INPUT A
B = INPUT B
REVISED MODEL 11-2-71 TO INCLUDE NVT BEHAVIOR
NEUTRON EFFECTS AT 1.2E14 N/CM*2 LEVEL
ELEMENTS
JA,A-GND=0.
JB,B-GND=0.
JO,OUT-GND=0.
E1,GND-1=FN2(VJA,VJB,0.8,3.1,1.9,6.3)
R1,1-2=100.
C1,2-GND=FC2(E1,E2,550.E-12,300.E-12)
JR,2-GND=0.
E2,GND-3=X1(VC1 + P1)
R2,3-OUT=30.
DEFINED PARAMETERS
P1=-.4
FUNCTIONS
TABLE 1 = 0.,0.,1.,0.
OUTPUTS
VJA,VJB
E1,E2,VC1,VJO,C1,PLOT
```

Figure II-18. Model Description With Neutron Effects

```
TEST CIRCUIT FOR RSN54L00 2 INPUT NAND GATE
NAD MODEL AND AFWL CIRCUIT
STORED AS R54L00S###
ELEMENTS
NA,IN-1-2-GND=MODEL L00 (CHANGE JR=P1)
R2,2-3=4300.
C2,2-3=2.6E-12
R3,3-GND=750.
C3,3-GND=15.E-12
D1,2-4=MODEL 1N3605 (PERM)
R4,4-5=800.
R5,6-5=1.
E2,GND-6=2.4
ESIG,GND-EIN=Q1(.3,3.,0.,19.E-9,331.E-9,19.E-9,750.E-9,1.,TIME)
R1,EIN-IN = 50.
E1,GND-1=2.4
DEFINED PARAMETERS
P1=Q2(TABLE 3(VC1NA),TABLE 2(TIME))
FUNCTIONS
TABLE 3=0.,-.5, .3,-.5, 1.0,1., 2.4,1.1, 3.,1.2, 5.,1.2
TABLE 2 = 0.,0.
 800.E-9,0.
 815.E-9,0.
 825.E-9,0.
 840.E-9,0.
 990.E-9,0.
Q1(A,B,C,D,E,F,G,H,Y)=(FGEN(A,B,C,D,E,F,G,H,Y))
Q2(A,B)=(A*B)
RUN CONTROLS
STOP TIME = 999.E-9
MAXIMUM PRINT POINTS = 200
OUTPUTS
ESIG,JRNA(IPP),PLOT
VR2,VCDD1,PLOT
RERUN DESCRIPTION(1)

THE TERM 'VR1 ' WILL CAUSE A COMPUTATIONAL DELAY.

FUNCTIONS
TABLE 2 = 0.,0.
 700.E-9,0.
 715.E-9,0.03
 725.E-9,0.03
 740.E-9,0.
999.E-9,0.
END

SYSTEM NOW ENTERING SIMULATION
```

Figure II-19. Neutron Radiation — Test Circuit Description

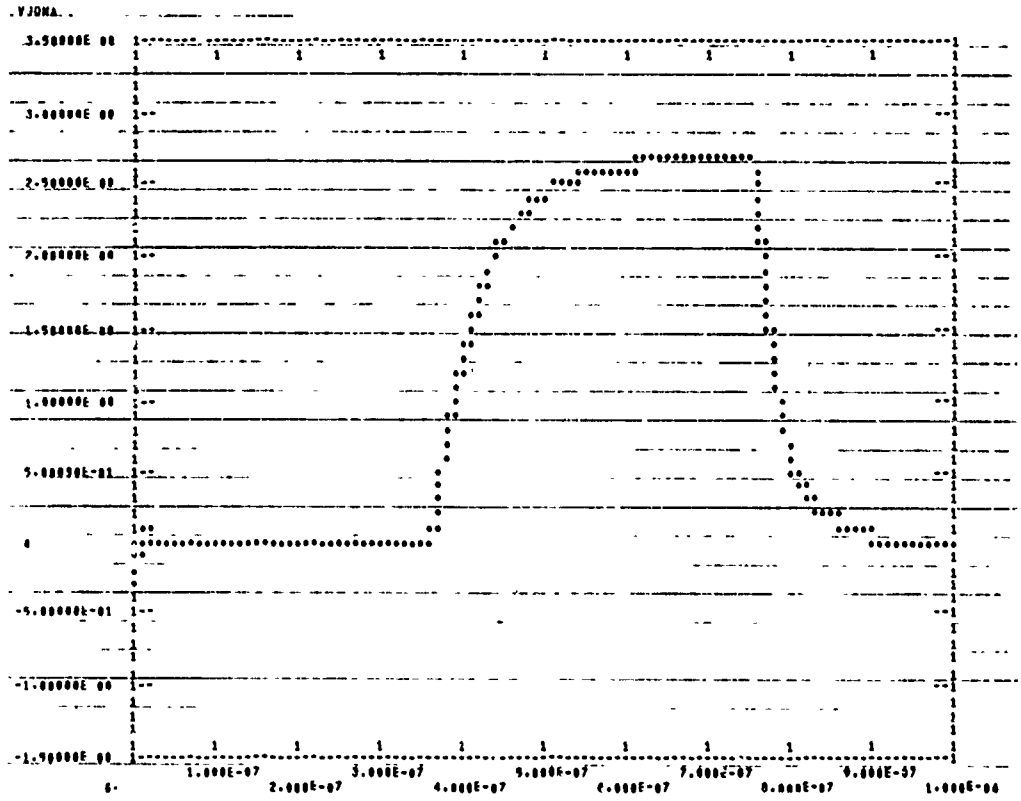


Figure II-20. Response to Neutron Radiation

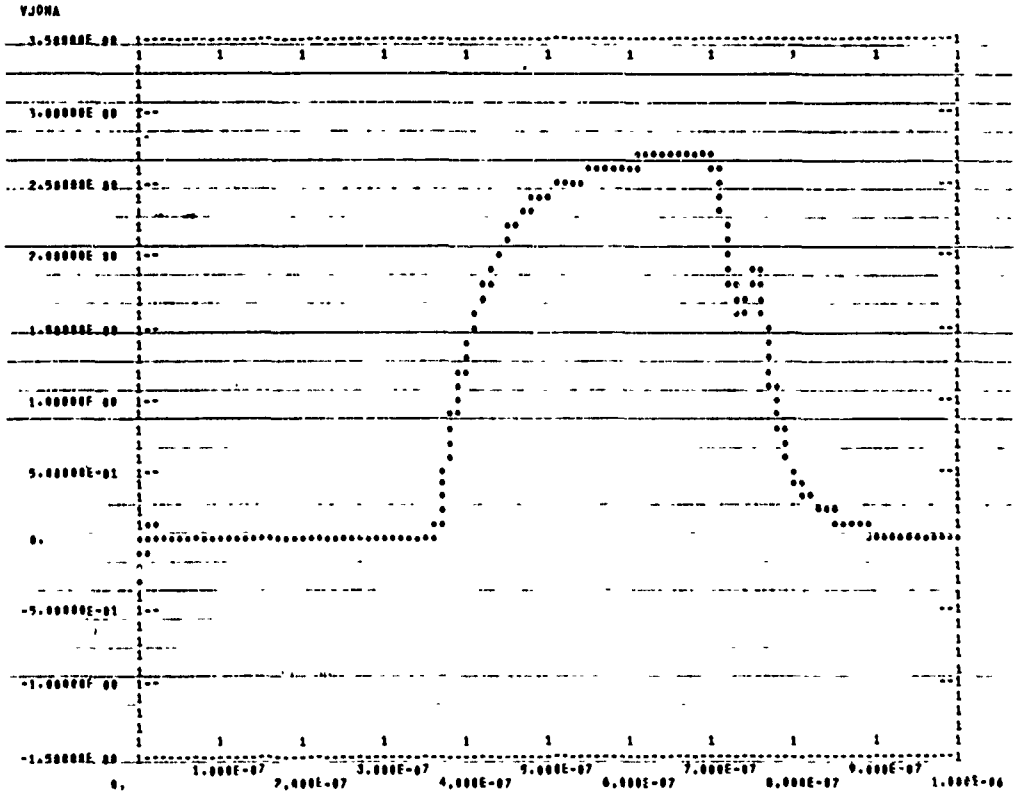


Figure II-21. Response to Neutron and Gamma Radiation

SECTION III

FAIRCHILD 9704 FOUR-INPUT NAND GATES

This integrated circuit is a four-input NAND gate. The circuit behaves in such a manner that when the signal on all of the inputs is at a logic 1 level, the output is at a logic 0. For all other input signal conditions, the output is at a logic 1 level.

The logic representation for the gate and the schematic diagram of the circuit are shown on Figure III-1. The electrical characteristics as defined by the manufacturer are shown in Table III-1. The voltage wave forms describing the device behavior and delay characteristics are shown in Figure III-2.

TABLE III-1.

ELECTRICAL CHARACTERISTICS
(Over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, V_{in} = 0.8 V max, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA (max)			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
		V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	54	−20		−55	mA
			74	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current/gate	V_{CC} = MAX, V_{in} = 5 V			3	5.5	mA
$I_{CC(1)}$	Logical 1 level supply current/gate	V_{CC} = MAX, V_{in} = 0			1	2	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level		C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level		C_L = 15 pF, R_L = 400 Ω		12	22	ns

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions for the applicable device type
‡All typical values are at V_{CC} = 5 V, T_A = 25°C
§Not more than one output should be shorted at a time

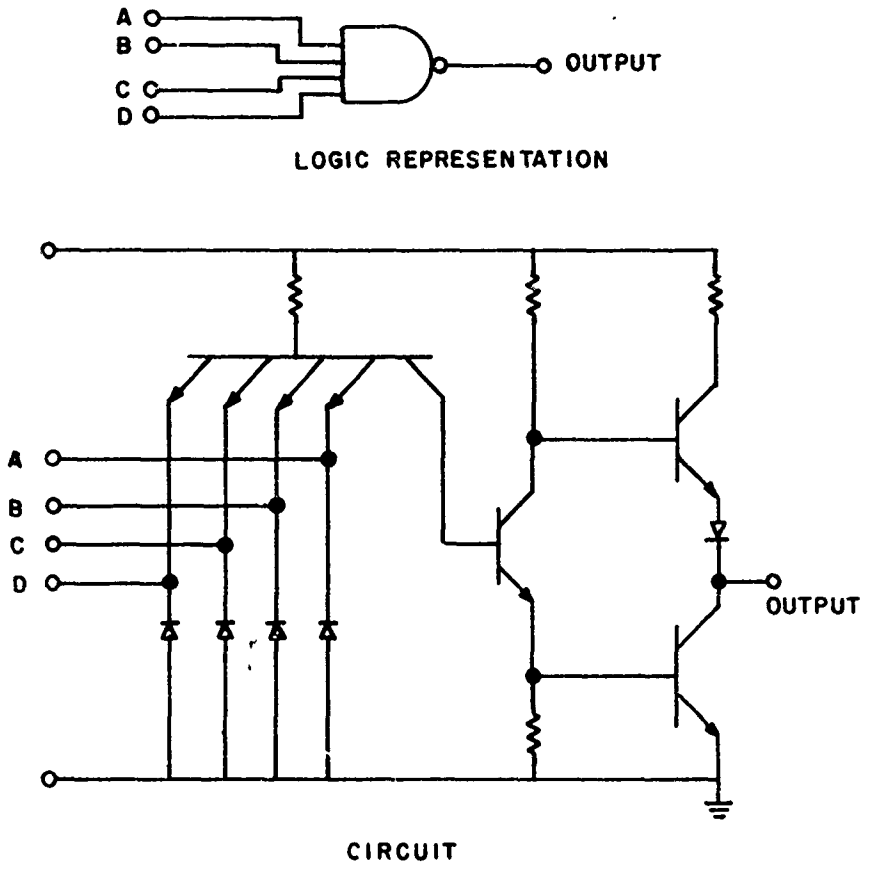


Figure III-1. Logic Representation and Electrical Schematic

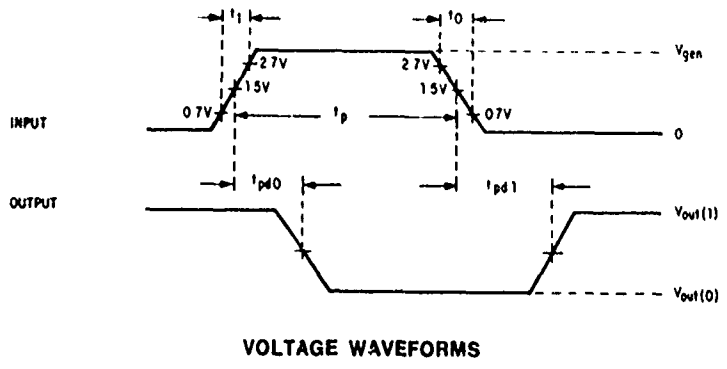


Figure III-2. Gate Propagation Delay Times

A. MODEL DEVELOPMENT

The computer model that has been developed to duplicate observed performance is shown in Figure III-3 and the model computer description in Figure III-4. The subprogram which establishes the logic output signal level, the delay characteristics, and the radiation response behavior is shown in Figure III-5. The FORTRAN flow charts associated with these three functions are included in Appendix III-A.

The signal input impedances, JA, JB, JC and JD, are represented as zero valued current sources. In SCEPTRE, this implies that the input signal terminals A through D have infinite impedance (although the gates have measurable and varying impedance values which depend upon the applied signal level). This, as a first order approximation, will provide reasonably accurate results. For greater accuracy, the current sources JA through JD should be modeled in SCEPTRE as "tabled" functions of current versus applied voltages; this method will provide a realistic device input impedance representation.

As indicated on Figure III-3 and described on Figure III-4, the voltage associated with the dependent source E1 is determined by the function FN4. This function establishes the value of E1 voltage in accordance with the truth table. As shown in Figure III-5, if any of the input signals is less than or equal to 0.8 volt, then E1 is set equal to 3.3 volts which represents a logic 1.

When all of the input signals are equal to or greater than 2.0 volts, the value of E1 is established as 0.4 volt which represents a logic 0.

If neither of these conditions exists, then E1 is determined to be 3.3 volts minus the absolute value of the smallest of the applied signals. (The values associated with the function FN4 have been obtained either from published data, Table III-1, or from laboratory tests.)

The device manufacturer indicates on Table III-1 that the switching delay times t_{pd1} for positive going output signals will be between 8 and 15 nanoseconds; for negative going t_{pd0} output signals, 12 to 22 nanoseconds. The required delay times, t_{pd0} and t_{pd1}, are established in the model by the time constant R1 - C1. This time constant is changed by varying the value of C1 depending upon whether a logic 1 or 0 is required as an output signal.

The value of C1 is determined by means of subprogram FC4. Thus, C1 is set to 60 picofarads, 150 picofarads, or 200 picofarads depending upon the voltage relationships between E1, E2 and VC1 and whether the output is rising, falling, or a constant. Since the output voltage E2 is equal to the voltage across the capacitor, C1, a relationship between the input signal levels and the output voltage is readily established.

JR is used as a source of gamma radiation injection in the model, when required.

The output impedance of the device is fixed at 25 ohms. Although this is not an accurate impedance representation for all voltage and load conditions, it provides first order accuracy of output signal level. To duplicate actual impedance variations, the value of resistor R2 would be made variable and a function of the load voltage and currents.

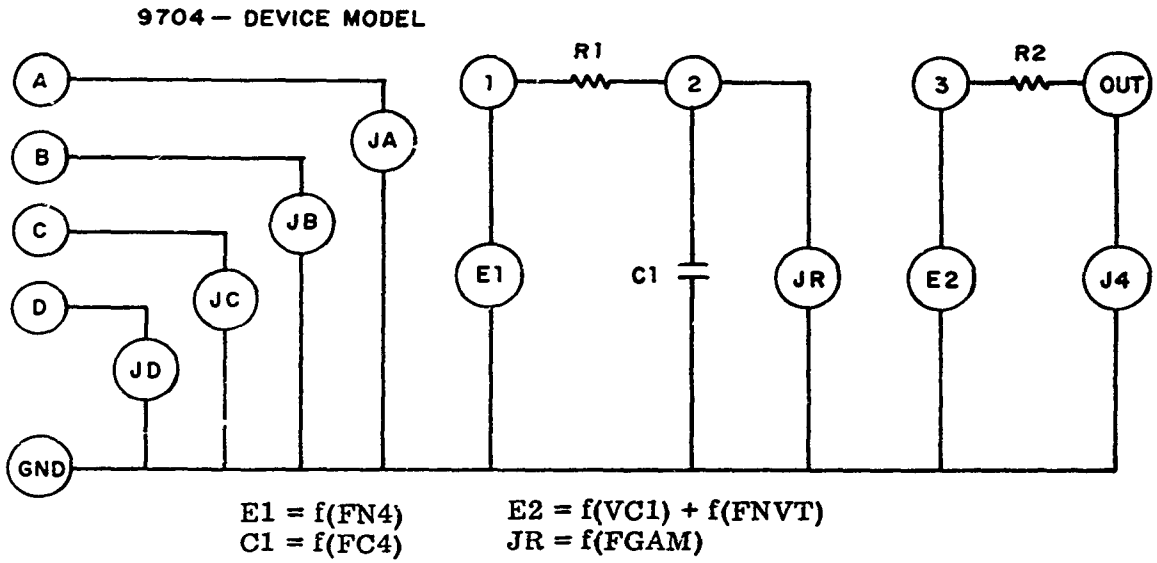


Figure III-3. Computer Model

```
MODEL 9704 (A=B=C=D=OUT=GND)
4 INPUT NAND GATE
A = INPUT A
B = INPUT B
C = INPUT C
D = INPUT D
ELEMENTS
JA,A=GND=0,
JB,B=GND=0,
JC,C=GND=0,
JD,D=GND=0,
E1,GND=1=FN4(VJA,VJB,VJC,VJD,0,0,3,3,2,0,0,4)
R1,1=2=100,
C1,2=GND=FC4(E1,E2,200,E=12,1=0,E=12,VC1,60,E=12)
JR,2=GND=0,
E2,GND=3=X1(VC1)
R2,3=0,T=25,
J4,OUT=GND=0,
OUTPUTS
VJA,VJB,VJC,VJD
E1,E2,VR2,C1,VC1,PLOT
VJ4,PLOT
```

Figure III-4. Computer Model Description

```
                    4 INPUT NAND GATE  LEVEL SELECT
                      A  B = VJB  C = VJC  D = VJD
      CFN4          4 INPUT NAND GATE  LEVEL SELECT
      C     X = VJA  B = VJB  C = VJC  D = VJD
      C     E = 0.6  F = 3.3  G = 2.0  H = 0.4
            FUNCTION FN4(A,B,C,D,E,F,G,H)
            IF(A.LE.E .OR. B.LE.E .OR. C.LE.E .OR. D.LE.E)GO TO 4
            IF(A.GE.G .AND. B.GE.G .AND. C.GE.G .AND. D.GE.G) GO TO 5
            FN4 = F=AMIN1(A,B,C,D)
            RETURN
        4   FN4 = F
            RETURN
        5   FN4 = H
            RETURN
      CFC4          CAPACITOR SELECTION
            ENTRY FC4(A,B,C,D,E,F)
      C     A = E1  B = E2  C = 200,E=12  D =1.0H=12  E=VC1  F=60E=12
            Q=D
            IF(A .GE.B) Q = C
            IF(E .GE. 3.) Q=F
            FN4 = Q
            RETURN
            ENTRY FGAM(A)
      C     GAMMA PERFORMANCE OF GATE
            IF(A.LT.1.0)GO TO 100
            G=A
            GO TO 200
      100   G=-3.
      200   FN4=G
      1000  RETURN
            ENTRY FNVT(A,B,C)
      C     NEUTRON BEHAVIOR OF GATE
            IF(A .LE. 2.)GO TO 500
            X=-H
            FN4=X
            GO TO 1100
      500   Y=C
            FN4=Y
      1100  RETURN
            END
  23598 WORDS OF MEMORY USED BY THIS COMPILATION
```

Figure III-5. Model Subprogram

The zero valued current source, J4, is a dummy element to permit monitoring the device output signal under varying conditions.

The six terminals required for normal usage of the gate are defined on Figure III-3 as A for the "A" input signal, B for the "B" input signal, C for the "C" input signal, D for the "D" input signal, OUT for the output signal and GND as the ground connection.

B MODEL VERIFICATION

To demonstrate the validity of the model, the circuit shown in Figure III-6 was described to the computer. This circuit, which is one of several standards for laboratory measurement, allows for easy variation of load (fanout) as well as simple impedance matching for monitoring equipment. For the particular tests conducted, an oscilloscope was connected between node 3 and ground. The topological description of the circuit for the SCEPTRE circuit analysis program, is shown in Figure III-7.

The results of the computer analysis of the model are presented in Figures III-8 and III-9. Figure III-8 shows the timing for one of the input signals as it varies between the logic 1 and 0 levels, when the other inputs are maintained at a 1 level. The truth table indicates that the output should be a logic 1 during the time when the signal is at a "0" level and vice versa. Figure III-9 indicates the proper model response to the described signal condition. The rise time, t_{pd1}, is about 15 nanoseconds; the fall time, t_{pd0}, about 13 nanoseconds.

C. RADIATION EFFECTS

1. GAMMA RADIATION

Exposing the device to a nuclear radiation environment may affect normal performance by causing the output signal level to vary. When exposed to pulsed ionizing rays (gamma radiation) at dose rate levels of approximately $3 \times 10^{+10}$ rads (Si)/second, the performance is only momentarily affected. Extensive testing was done by the Air Force Weapons Laboratory. The results of these tests were used to obtain the simulated radiation performance.

When a gamma radiation pulse simulation is caused to occur at about 520 nanoseconds (Figure III-10), the output response of the device is momentarily reduced. Figure III-11 shows the computer response to the radiation pulse. The solid line drawn on the figure is the observed laboratory result.

When the radiation pulse is caused to occur when the gate output is at a 0 level, the normal reaction of the output level is to increase. Figure III-12 shows both the observed and computer results.

The method for simulating the transient effects induced by the pulsed ionizing gamma radiation is to change the form of JR in Figure III-4. As shown on Figure III-13, JR in device NA is redefined as a function of the voltage across capacitor C1 and a signal that is time dependent and represented by Table 2 of Figure III-13; this change is identified as P1. By changing the time entries in this table, the radiation simulation is caused to occur whenever desired. Table 3 of Figure III-13 defines the radiation behavior of the device as a function of the voltage across the capacitor, C1.

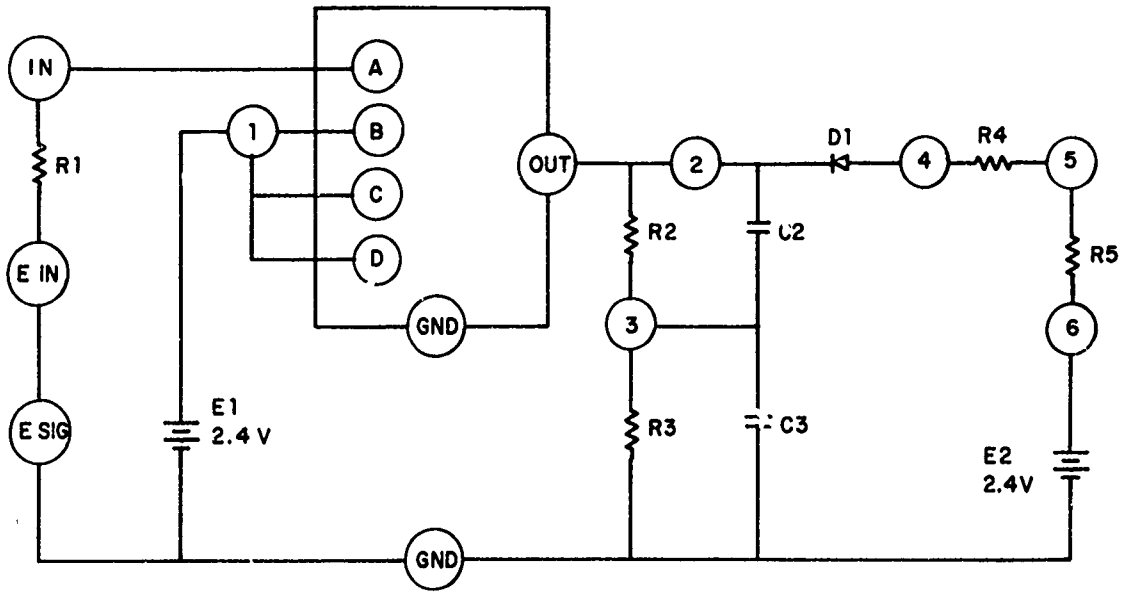


Figure III-6. Test Circuit

```
TEST CIRCUIT FOR 9704 4 INPUT NAND GATE
RAD MODEL AND AFWL CIRCUIT
STORED AS R9704$###
ELEMENTS
NA,IN-1-1-1-2-GND=MODEL 9704
R2,2-3=4300.
C2,2-3=2.6E-12
R3,3-GND=750.
C3,3-GND=15.E-12
D1,2-4=MODEL 1N3605 (PERM)
R4,4-5=800.
R5,6-5=1.
E2,GND-6=2.4
ESIG,GND-EIN=Q1(.3,3.,0.,19.E-19,331.E-9,19.E-9,750.E-9,1.,TIME)
R1,EIN-IN = 50.
E1,GND-1=2.4
FUNCTIONS
Q1(A,B,C,D,E,F,G,H,Y)=(FGEN(A,B,C,D,E,F,G,H,Y))
RUN CONTROLS
STOP TIME = 9 , E-9
 MAXIMUM PRINT POINTS = 100
OUTPUTS
ESIG,VR3,PLOT
END
```

Figure III-7. Test Circuit — Computer Description

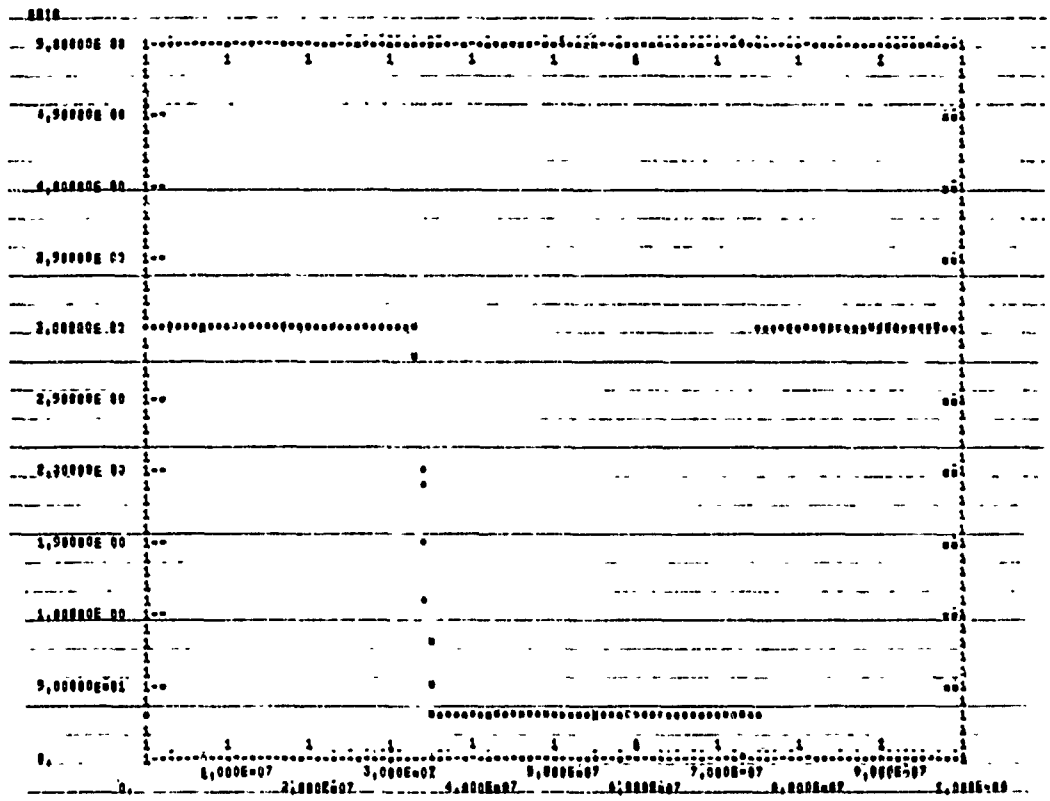


Figure III-8. Input Signal

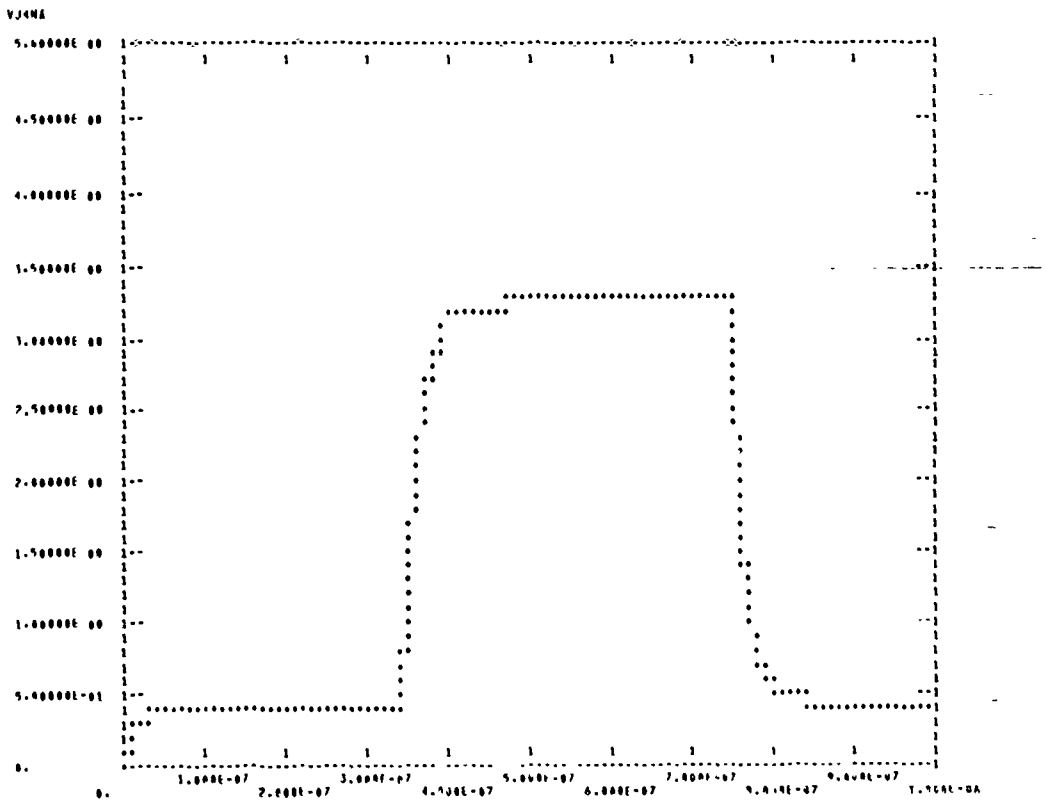


Figure III-9. Output Response

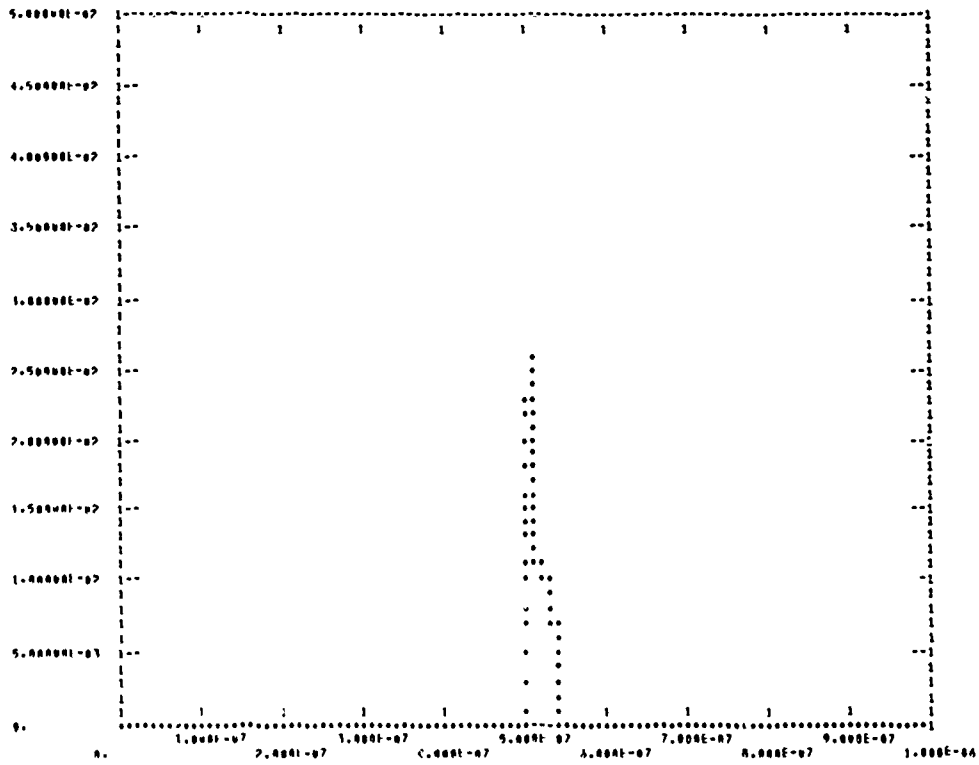


Figure III-10. Simulated Gamma Radiation Pulse

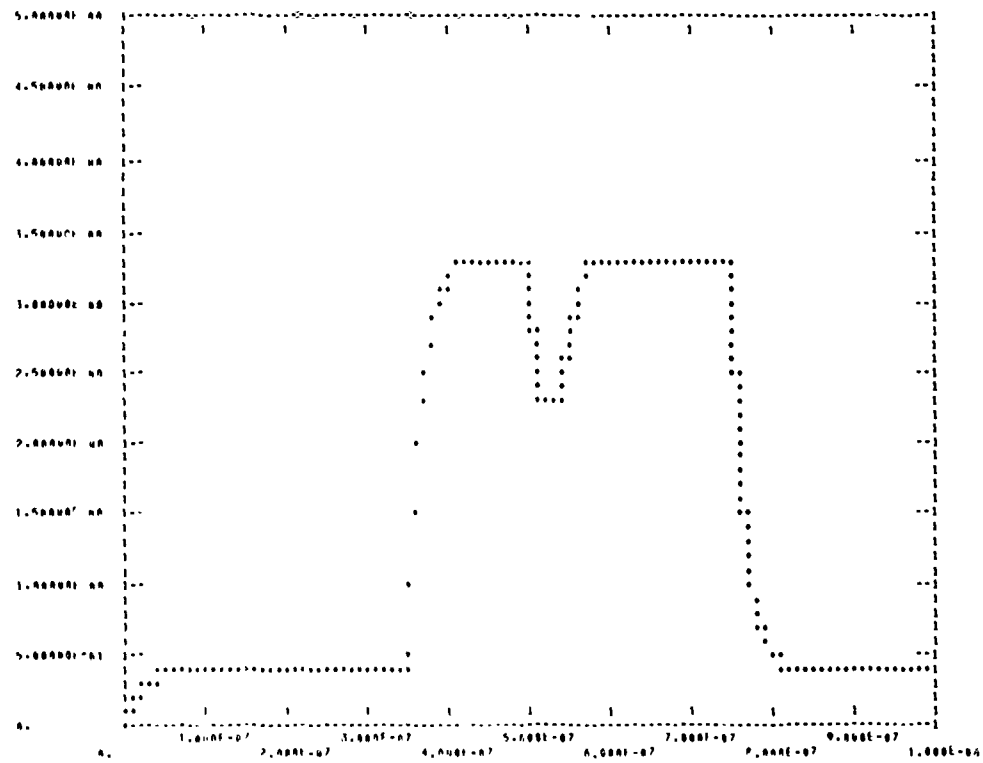


Figure III-11. 1 Response to Gamma Radiation

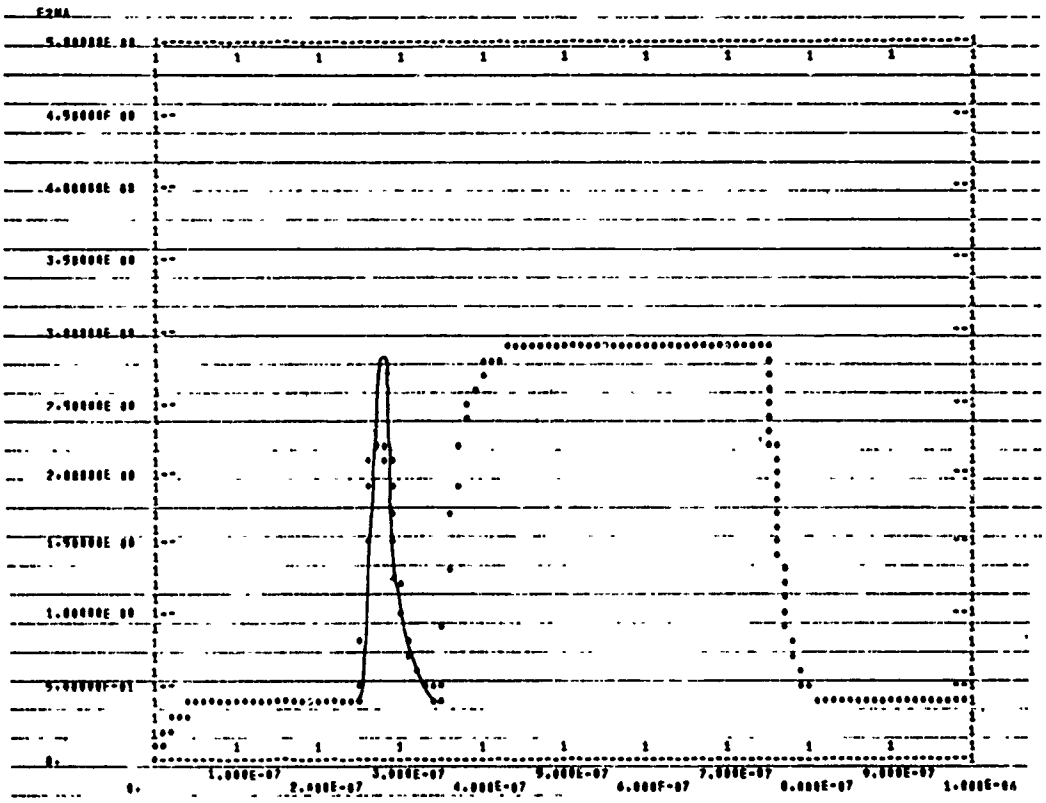


Figure III-12. 0 Response to Gamma Radiation

```
TEST CIRCUIT FOR 9704 4 INPUT NAND GATE
RAD MODEL AND AFWL CIRCUIT
STORED AS R9704S###
ELEMENTS
NA,IN=1-1=1-2=GND;MODEL 9704(CHANGE JR=P1)
R2,2=3=4300,
C2,2=3=2,6E-12
R3,3=GND=750,
C3,3=GND=15,E=12
D1,2=4=MODEL IN3605 (PERM)
R4,4=5=800,
R5,6=5=1,
E2,GND=6=2,4
ESIG,GND=EIN=Q1(,8,3,90,,19,E-19,331,E=9,19,E=9,750,E=9,0,,TIME)
R1,EIN=IN = 50,
E1,GND=1=2,4
DEFINED PARAMETERS
 P1=Q2(TABLE 3(P2),TABLE 2(TIME))
 P2=FGAM(VC1NA)
FUNCTIONS
TABLE 3 = -3,,-3,, 1,8,-3,, 2,4,1,1, 4,,5,
TABLE 2 = 0,,0,
 500,E=9,0,
 515,E=9,0,035
 525,E=9,0,035
 540,E=9,0,
 999,E=9,0,
Q1(A,B,C,D,E,F,G,H,Y)=(FGEN(A,B,C,D,E,F,G,H,Y))
Q2(A,B)=(A*B)
RUN CONTROLS
STOP TIME = 999,E=9
 MAXIMUM PRINT POINTS = 100
OUTPUTS
ESIG,VRNA(IPP),PLOT
 P1,P2,VR5,PLOT
END
```

Figure III-13. Gamma Test Circuit Description

2. NEUTRON RADIATION

When the device is exposed to neutron radiation conditions, the performance may be degraded either temporarily or permanently. The degree of the degradation, as well as the device recovery time for those conditions which permit recovery, depends upon the exposure level.

Exposure of test circuits of fluence levels of 1.2×10^{14} results in an output level reduction of approximately 0.4 volt, when the signal is at a 1 level. The results were observed by the Air Force Weapons Laboratory when they tested similar devices and are reported in Reference 1.* Figure III-14 presents the circuit transfer function degradation for various fluence levels, as observed during these tests. For condition 4, which represents the fluence level of 1.2×10^{14}, the output signal level drops from about 3.1 volts to approximately 2.7 volts.

The method for incorporating this reponse change into the model is shown on Figure III-15. The value of the output voltage, E2, is changed from a simple dependency on the voltage across capacitor C1, to a dependency upon both the capacitor voltage and the fluence level, P4.

The computer description to produce an analysis of the device in the test circuit configuration is shown in Figure III-16. To cause the neutron effects to be included in the analysis, the value of P4 is changed from zero, as stored in the model, to a dependency on function FNVT. This is accomplished through the "change" statement included in the NA callout on the figure. In this instance, the radiation effects reduce the value of the voltage across C1 by 0.4 volt when the output signal is at a 1 level and increase the voltage by 0.2 volt when the output is at a 0 level. The results of the analysis are shown in Figure III-17. In each output it can be seen that the 1 signal level is reduced from the 3.3 volts observed in Figure III-9 to 2.9 volts, and the 0 signal level is increased from 0.4 volt to 0.6 volt.

This method of including fluence effects represents an approximation of the results shown in curve 4 of Figure III-14. A more sophisticated and accurate representation would be to mathematically describe curve 4 and allow P1 to represent the resultant equation. However, the present model does demonstrate a satisfactory procedure for incorporating these conditions into the device model description.

---

*Ibid. page 16

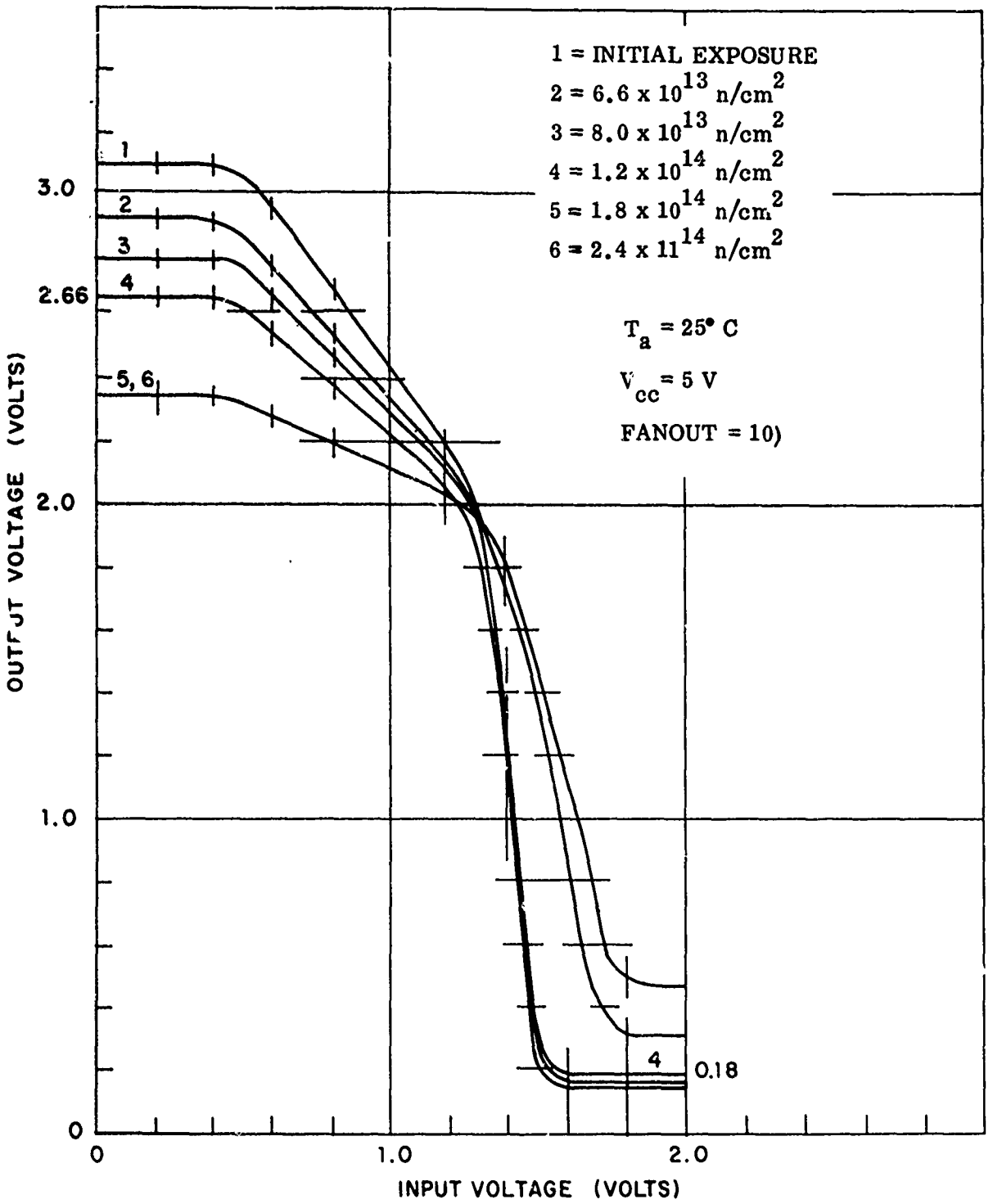


Figure III-14. Neutron Radiation — Circuit Transfer Function

```
MODEL 9704 (A-B-C-D-OUT-GND)
4 INPUT NAND GATE
A = INPUT A
B = INPUT B
C = INPUT C
D = INPUT D
ELEMENTS
JA,A=GND=0,
JB,B=GND=0,
JC,C=GND=0,
JD,D=GND=0,
E1,GND=1=FN4(VJA,VJB,VJC,VJD,0,8,3,3,2,0,0,4)
R1,1=2=100,
C1,2=GND=FC4(E1,E2,200,E=12,150,E=12,VC1,40,E=12)
JR,2=GND=0,
E2,GND=3=X1(VC1=P4)
R2,3=OUT=25,
J4,OUT=GND=0,
DEFINED PARAMETERS
P4=0,
OUTPUTS
VJA,VJB,VJC,VJD
E1,E2,VR2,C1,VC1,PLOT
VJ4,PLOT
```

Figure III-15. Model Description With Neutron Effects

```
TEST CIRCUIT FOR 9704 4 INPUT NAND GATE
RAD MODEL AND AFWL CIRCUIT
STORED AS R97045##
NEUTRON BEHAVIOR TEST
ELEMENTS
NA,IN=1=3-4=2=GND=MODEL 9704(CHANGE P4=P3)
R2,2=3=4300,
C2,2=3=2.6E=12
R3,3=GND=750,
C3,3=GND=15,E=12
D1,2=4=MODEL 1N3605 (PERM)
R4,4=5=800,
R5,6=5=1,
E2,GND=6=2,4
ESIG,GND=EIN=01(,3,3,70,,19,E=19,331,E=9,19,E=9,750,E=9,1,,TIME)
R1,EIN=IN = 50,
E5,GND=3=2,4
E6,GND=4=2,4
E1,GND=1=2,4
DEFINED PARAMETERS
P1=Q2(TABLE 3(P2),TABLE 2(TIME))
P2=FGAM(VC1NA)
P3=FNVT(VC1NA,0,4,0,2)
FUNCTIONS
TABLE 3 = -3,,-3,, 1,8,-3,, 2,4,1,1, 4,,5,
TABLE 2 = 0,,0,
500,E=9,0,
515,E=9,0,035
525,E=9,0,035
540,E=9,0,
999,E=9,0,
Q1(A,B,C,D,E,F,G,H,Y)=(FGEN(A,B,C,D,E,F,G,H,Y))
Q2(A,B)=(A*B)
RUN CONTROLS
STOP TIME = 999,E=9
MAXIMUM PRINT POINTS = 100
OUTPUTS
ESIG,JRNA(IPP),PLOT
P3,VR3,PLOT
END

THE TERM *VR1   ! WILL CAUSE A COMPUTATIONAL DELAY.
```

Figure III-16. Neutron Radiation Test Circuit Description

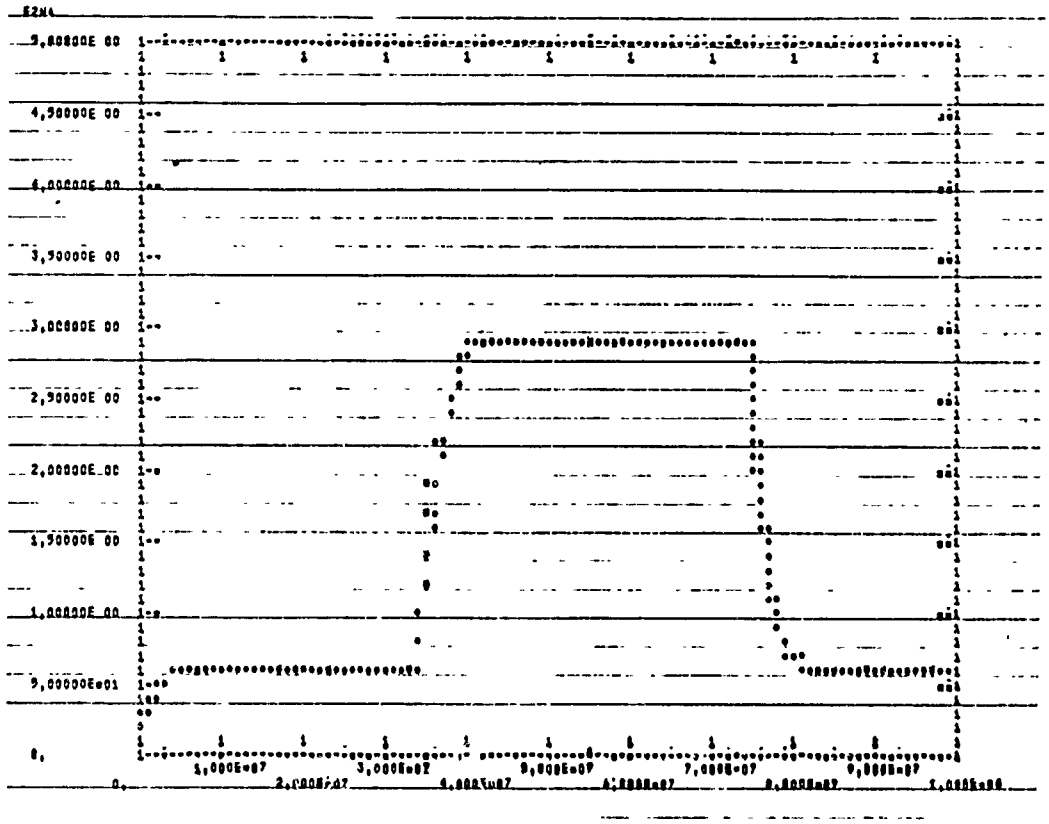


Figure III-17. Output Response to Neutron Radiation

SECTION IV

FAIRCHILD 9774-D FLIP-FLOP

This integrated circuit is a monolithic, edge-triggered flip-flop which accepts independent clear and preset (reset and set) inputs, as well as a clock and "D" data (signal) input. Outputs are provided as complementary Q and $\overline{Q}$ signals. Input information is transferred to the outputs on the positive going edge of the clock pulse.

Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After this clock threshold has been reached, any change in the data input (D) is locked out until the next clock pulse.

The schematic diagram of the integrated circuit is shown in Figure IV-1. A simplified functional logic representation of the flip-flop is shown in Figure IV-2 and is represented as six NAND gates.

The truth table which establishes the input-output relationships for the device is shown in Table IV-1 for the condition when the clear and preset signal levels are high, as a logic 1 level. Under these conditions, the clear and preset do not affect the device performance.

TABLE IV-1

TRUTH TABLE

t_n	t_{n+1}	
Input	Input	Output
D	Q	$\overline{Q}$
0	0	1
1	1	0

t_n = bit time before clock pulse

t_{n+1} = bit time after clock pulse

The electrical characteristics of the device as defined by the manufacturer, are shown in Table IV-2.

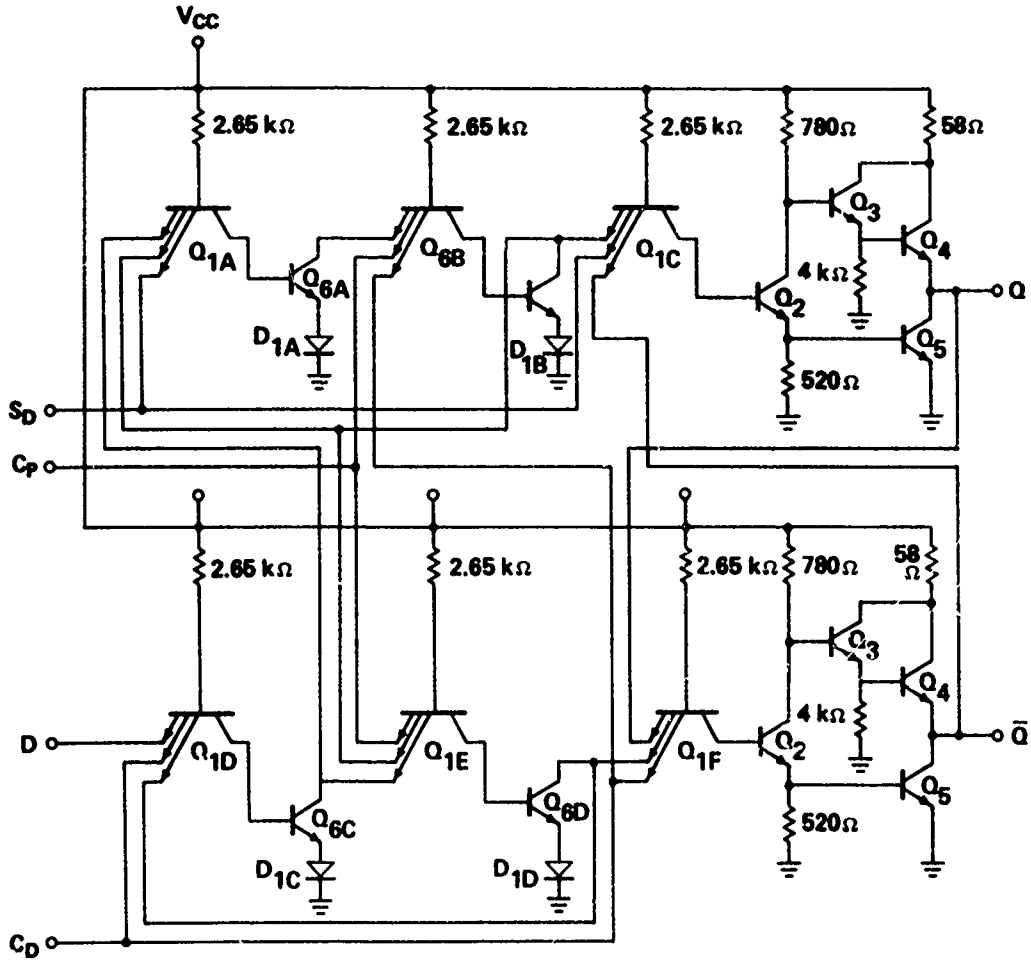


Figure IV-1. Schematic — 9774

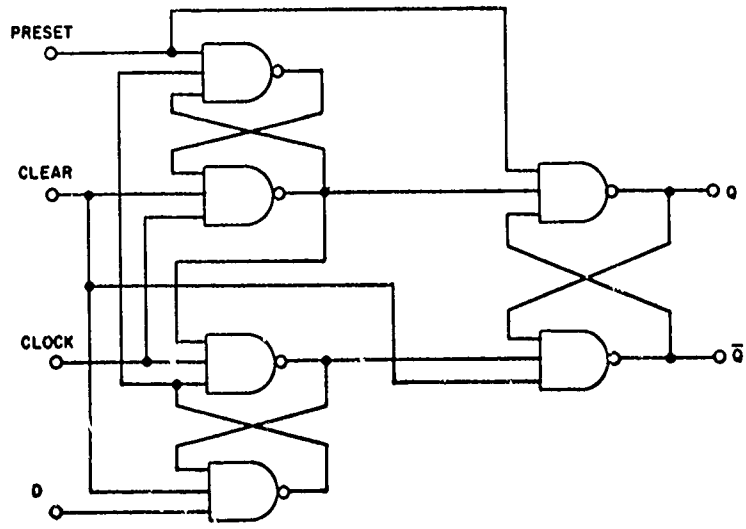


Figure IV-2. Logic Representation

TABLE IV-2.

ELECTRICAL CHARACTERISTICS
(Over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at preset or D	V_{CC} = MAX,	V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	V_{CC} = MAX,	V_{in} = 0.4 V				−3.2	mA
$I_{in(1)}$	Logical 1 level input current at D	V_{CC} = MAX,	V_{in} = 2.4 V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clock	V_{CC} = MAX,	V_{in} = 2.4 V				80	μA
		V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at clear	V_{CC} = MAX,	V_{in} = 2.4 V				120	μA
		V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX,	V_{in} = 0	5474	−20		−57	mA
				7474	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 5 V			17	30	mA

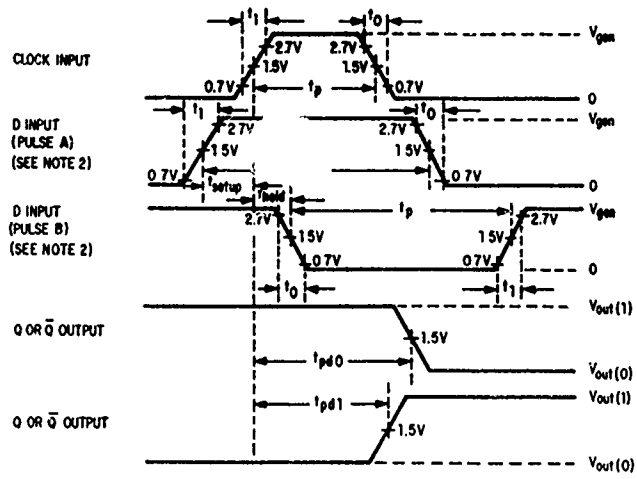
†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions for the applicable device type
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency		C_L = 15 pF, R_L = 400 Ω	15	25		MHz
t_{setup}	Minimum input setup time		C_L = 15 pF, R_L = 400 Ω		15	20	ns
t_{hold}	Minimum input hold time		C_L = 15 pF, R_L = 400 Ω		2	5	ns
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output		C_L = 15 pF, R_L = 400 Ω			25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output		C_L = 15 pF, R_L = 400 Ω			40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output		C_L = 15 pF, R_L = 400 Ω	10	14	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output		C_L = 15 pF, R_L = 400 Ω	10	20	40	ns

POSITIVE LOGIC. Low input to preset sets Q to logical 1 Low input to clear sets Q to logical 0 Preset and clear are independent of clock

The dynamic performance characteristics of the integrated circuit are shown in Figures IV-3 and IV-4. Figure IV-3 defines the time delay relationships that must exist when the clock and D signals (per Table IV-1) are effective. Figure IV-4 describes the effects of applying the clear and preset signals. The stipulated delay times, t_{pd1} and t_{pd0}, for the output response to an applied signal are given in Table IV-2.

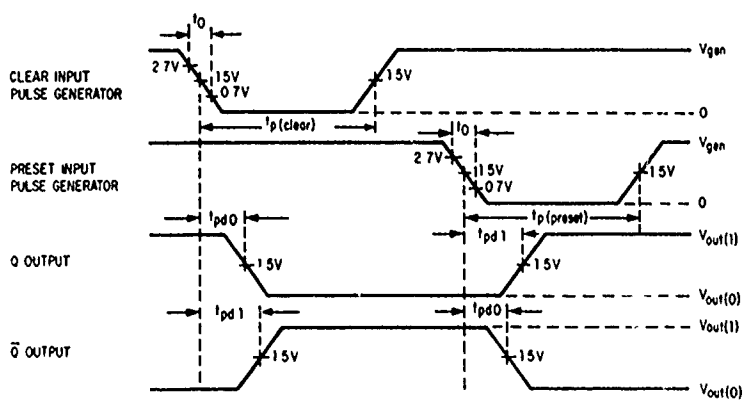


VOLTAGE WAVEFORMS

NOTES 1 Clock input pulse has the following characteristics. V_{gen} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, t_p = 30 ns, and PRR = 1 MHz.

2. D input (pulse A) has the following characteristics: V_{gen} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, t_{setup} = 20 ns, t_p = 60 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics. V_{gen} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, t_{hold} = 5 ns, t_p = 60 ns, and PRR is 50% of the clock PRR

Figure IV-3. Flip-Flop Switching Times



VOLTAGE WAVEFORMS

NOTE: 1. Clear and preset inputs of the 9774 dominate regardless of the state of clock or D inputs.

Figure IV-4. PRESET/CLEAR Propagation Delay Times

A. MODEL DEVELOPMENT

The computer model that has been developed to duplicate observed (and/or manufacturer published) performance is shown in Figure IV-5. The clock (CK), preset (SET), clear (RS) and D (D) voltages are defined as the input signals. The required response delays, as indicated in Table IV-2, are controlled by the time constants R1 - C1 and R2 - C2, for Q and $\overline{Q}$ (QB) respectively. The computer model description is shown in Figure IV-6; the subprograms that establish the proper logic output signal levels, the delay characteristics, and the radiation response behavior are shown in Figure IV-7.

The signal input impedances, JCK, JS, JRS, and JD, are represented as zero valued current sources. In SCEPTRE, this implies that the input signal terminals, CK, SET, RS and D, have infinite impedance (although the gates have measurable and varying impedance values which depend upon the applied signal level). This, as a first order approximation, will provide reasonably accurate results. For greater accuracy, the current sources should be modeled as "tabled" functions of current versus applied voltages in SCEPTRE. This method will provide a realistic device input impedance representation.

As indicated on Figure IV-6, the voltage associated with the dependent source E1 is determined by the function FEI. This function establishes the value of E1 voltage in accordance with the truth table of Table IV-1. As shown in Figure IV-7 which describes the function, if either the set or reset input signals are a logic 0, they override all other signal conditions and establish the value of E1 to be a logic 1 for a 0 SET input or a logic 0 for a RESET input. All other normal device performance conditions are controlled by the function. A flow diagram for this function is shown in Appendix IV-A.

To assure that the device triggers on the leading (positive going) edge of the clock pulse, the function FEI monitors the clock signal. When the clock signal voltage is less than or equal to the preceding observation, the value associated with E1 is maintained constant. When the clock signal voltage is measured to be greater than the preceding value, it is tested to determine whether it is greater than a 0 value of 0.8 volt and less than a 1 value of 2.0 volts, since the device manufacturer indicates that the clock pulse is effective only in this range of values. When the clock level is within this range, the signal at the D input terminal is transferred to the output stage of the model. If the clock voltage is not between these values, no change is permitted to the previously set voltage of E1.

When the clock voltage is established as a positive going signal and is determined to be within the prescribed range, the subprogram evaluates the voltage level of the input signal D. Then, in accordance with the truth table, if the input signal is a 1, E1 is set equal to 3.0 volts. If the input signal is a 0, E1 is set equal to 0.1 volt.

The voltage across C1, and JR1 which is in parallel with it, is determined by the voltage E1. In turn, the output voltage, Q, is directly related to the voltage across JR1 through E3.

$\overline{Q}$ is defined as the complement of Q; therefore E2, which establishes the signal level for QB in the model, is computed to be 3.1 volts minus the value of the voltage across E1. Thus when E1 is set to 3.0 volts or a logic 1 by the function FEI, E2 is equal to 0.1 volt, a logic 0. When E1 is set to 0.1 volt, E2 is then 3.0 volts or a

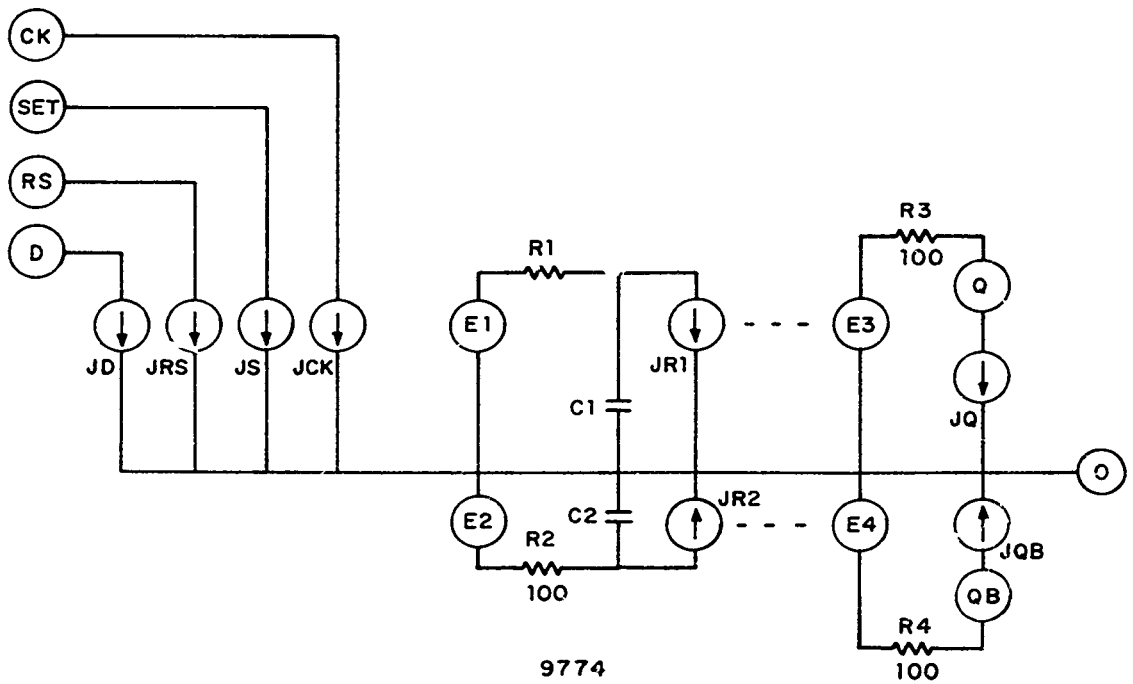


Figure IV-5. D Flip-Flop Model

```
MODEL 9774(CK-D-SET-RS-Q-QB-0)
      DUAL D FLIPFLOP
         VERSION 3
 ELEMENTS
 JCK,CK-0=0
 JS,SET-0=0
 JRS,RS-0=0
 JD,D-0=0
 JQ,Q-0=0
 JQB,QB-0=0
 E1,0-1=FEI(VJS,VJRS,VJCK,VJD,TIME)
 R1,1-2=100.
 C1,2-0=FKC(E1,VC1)
 JR1,2-0=Q1(T1(VJR1),T2)
 E2,0-3=X1(3.1-E1)
 R2,3-4=100.
 C2,4-0=FKC(E2,VC2)
 JR2,4-0=Q1(T1(VJR2),T2)
 E3,0-5=X2(VJR1)
 R3,5-9=100.
 E4,0-6=X3(VJR2)
 R4,6-QB=100.
FUNCTIONS
Q1(A,B)=(A*B)
T1=
 0,0.
 1,9,0,
 2,9,0,
 3,0.
 OUTPUTS
 VJQ,VJQB,VC1,VC2,E1,E2,E3,E4,C1,C2,PLOT
```

Figure IV-6. Computer Model Description

```
CFD                D NAND GATE
      FUNCTION FEI(VSET,VRESET,VCLOCK,VDRIVE,TIME)
C-----------------------------------------------------------------
C     VSET=VOLTAGE AT SET INPUT
C     VRESET=VOLTAGE AT RESET INPUT
C     VCLOCK=VOLTAGE AT CLOCK INPUT
C     VDRIVE=VOLTAGE AT D=INPUT
C     XCLOCK=VOLTAGE AT CLOCK INPUT DURING LAST COMPUTATION
C     XGEN=VOLTAGE AT GATE(E1) DURING LAST COMPUTATION
C-----------------------------------------------------------------
      IF(TIME .LE. 0.) XCLOCK = VCLOCK
      IF(TIME .LE. 0.) XGEN = 3.0
      IF (VSET.LE.1.2) GO TO 1
      IF (VRESET.LE.1.2) GO TO 2
      GO TO 3
    3 IF (TIME.LE.0.) XGEN=3.0
      IF(VCLOCK .LE. XCLOCK) GO TO 9
      IF (VCLOCK.GE.0.8.AND.VCLOCK.LE.2.0) GO TO 4
    9 FEI=XGEN
      GO TO 10
    4 IF(VDRIVE.GE.1.5) FEI=3.0
      IF(VDRIVE .LT. 1.5) FEI = 0.1
      GO TO 10
    1 FEI=3.0
      GO TO 10
    2 FEI=0.1
   10 XCLOCK=VCLOCK
      XGEN=FEI
      RETURN
      ENTRY FKC(VGEN,VCAP)
C-----------------------------------------------------------------
C     TO EVALUATE THE OUTPUT CAPACITOR VALUE
C      VGEN=VOLTAGE ACROSS GENERATOR(GATE)
C      VCAP=VOLTAGE ACROSS CAPACITOR
C-----------------------------------------------------------------
      IF(VGEN .GE. VCAP) FEI = 300.E-12
      IF(VGEN .LT. VCAP)FEI=250.E-12
      RETURN
      ENTRY FNVT(A,B,C)
C      NEUTRON BEHAVIOR OF CIRCUIT
      IF(A - 1.5) 40,50,60
   40 Y=C
      GO TO 150
   50 Y=0.1
      GO TO 150
   70 Y=0.05
      GO TO 150
   60 IF(A .LE. 2.) GO TO 70
      IF(A .LT. 2.3) GO TO 80
      IF(A .LT. 2.5) GO TO 100
      IF(A .LT. 2.7) GO TO 90
      IF(A .LT. 2.8) GO TO 110
      Y=-B
      GO TO 150
   80 Y=-0.05
      GO TO 150
   90 Y=-0.15
      GO TO 150
  100 Y=-0.1
      GO TO 150
  110 Y=-0.25
  150 FEI=Y
      RETURN
      END
```

Figure IV-7. Model Subprogram

logic 1. In an analogous manner to the Q signal, QB is directly related to the voltage across C2 (JR2) through E4.

The time delays associated with the various controlling signals, as defined by the manufacturer, are given in Table IV-2. To obtain these delays, the time constants R1 - C1 and R2 - C2 are used. Since the time delay, t_{pd1}, associated with an increase in the value of Q and $\overline{Q}$ is different from that associated with a decrease in the signal levels, t_{pd0}, the values of C1 and C2 are changed. This is accomplished by means of the function subprogram, FKC. This subprogram sets the values of C1 and C2 equal to 300 picofarads if voltage sources E1 or E2, respectively, are greater than, or equal to, the Q voltage levels. If these voltage sources are less than the Q voltages, C1 and C2 are set to 250 picofarads.

The output impedance associated with Q and QB is fixed at 100 ohms. Although this is not an accurate impedance representation for all voltage and load conditions, it provides first order accuracy of output signal level. To duplicate actual impedance variations, the value of resistor R2 would be made variable and a function of the load voltage and currents.

The zero valued current sources, JQ and JQB, are dummy elements to permit computer monitoring of the output signals under varying performance conditions.

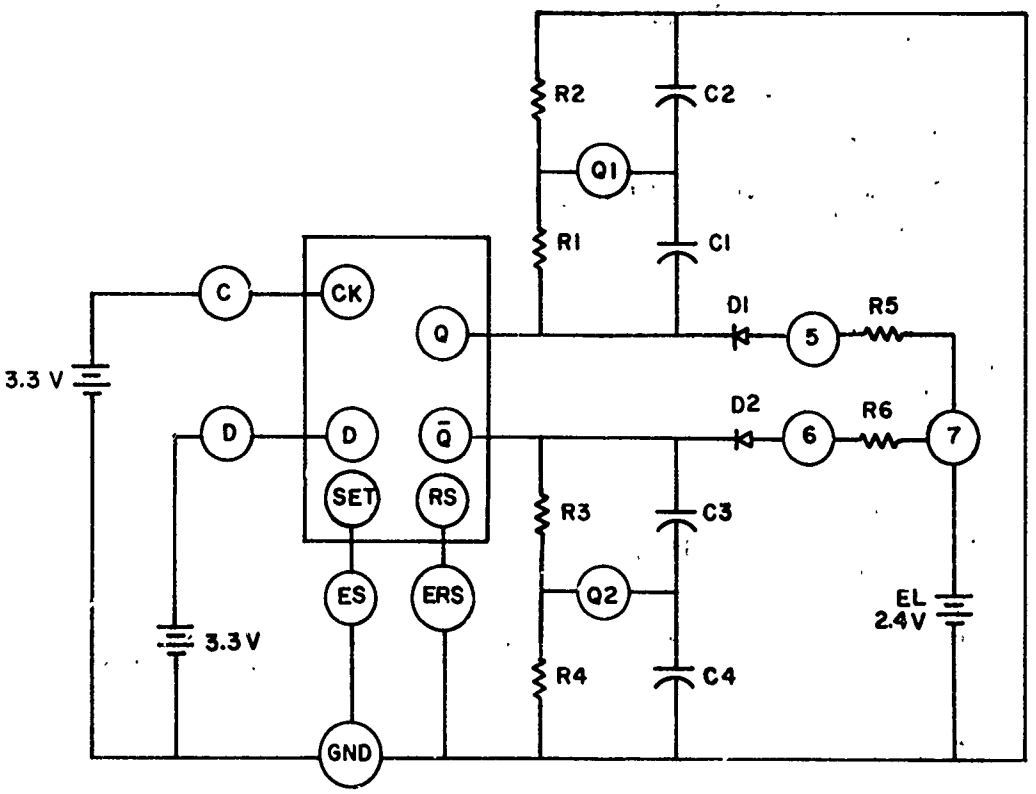
The seven terminals required for normal computer use of the circuit are defined on Figure IV-5 as CK for the clock input signal, SET and RS for the set and reset signals respectively, D for the signal input, Q and QB for the outputs and 0 for the ground connection.

B. MODEL VERIFICATION

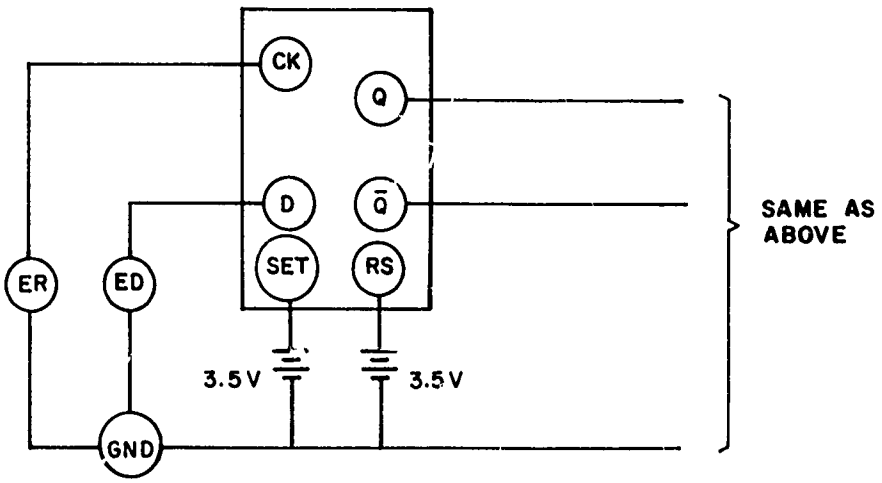
To demonstrate the validity of the model, the circuit shown in Figure IV-8 was described to the computer. Figure IV-8(A) is used to demonstrate the preset and clear functions. To demonstrate the clock and D input signal functions, the circuit shown in Figure IV-8(B) was used. The topological description for the SCEPTRE circuit analysis program for Figure IV-8(A) is shown in Figure IV-9.

The results of the computer analysis of this circuit are shown in Figures IV-10 through IV-13. Figures IV-10 and IV-11 indicate the set and reset input signals. Figures IV-12 and IV-13 show the circuit response to these input signals; Figure IV-12 shows the Q output, and Figure IV-13, the $\overline{Q}$ output. Comparing the time relationships between Figures IV-10 and IV-12, it is observed that when the RESET goes to a 0 level, the Q signal is forced to a 0 and remains there. Only when the SET voltage is reduced to a 0 is the Q signal caused to return to a 1 level (Figure IV-11).

Figures IV-14 through IV-18 present the same information for the Figure IV-8(B) circuit which tests the circuit response to the clock and D input signals. Figure IV-14 describes the circuit topology as input to the computer; Figure IV-15 shows the clock input, Figure IV-16 the signal input, Figure IV-17 the circuit response at the Q output terminal, and Figure IV-18 the $\overline{Q}$ output terminal response. Drawn on Figure IV-17 and Figure IV-18 are the results observed in the laboratory. The t_{pd1} time (i.e., the time delay from the clock signal reaching 1.5 volts and the Q signal falling to 1.5 volts) is 14 nanoseconds. The manufacturer specifies 14 nanoseconds as typical.



Test Circuit for Set and Reset "D" Flip-Flop - 9744



Test Circuit for Clock and "D"

Figure IV-8. Test Circuits

```
        9774 SWITCHING TIME TEST
         AFWL CIRCUIT
           TEST FOR SET AND RESET
ELEMENTS
 ES,GND-S=T1
 ERS,GND-RS=T3
EC,GND-C=3.3
ED,GND-D=3.3
F1,C-D-S-RS-Q-QB-GND=MODEL 9774
R1,Q-Q1=4300
C1,Q-Q1=2.E-12
R2,Q1-GND=750.
C2,Q1-GND=11.5E-12
D1,Q-5=MODEL 1N3605 (PERM)
R5,5-7=800
EL,GND-7=2.4
R3,QB-Q2=4300
C3,QB-Q2=2.E-12
R4,Q2-GND=750.
C4,Q2-GND=11.5E-12
D2,QB-6=MODEL 1N3605 (PERM)
R6,6-7=800
 FUNCTIONS
T1=0,3.5,250.E-9,3.5,259.E-9,0.,300.E-9,0.,309.E-9,3.5
T3=0,3.5,100.E-9,3.5,109.E-9,0.,150.E-9,0.,159.E-9,3.5
 T2F1=
 0,0
 10.E-9,10
 20.E-9,10
 30.E-9,0
 200.E-9,0
 210.E-9,10
 220.E-9,10
 230.E-9,0
 280.E-9,0
 290.E-9,10
 300.E-9,10
 310.E-9,0
 650.E-9,0
 660.E-9,10
 670.E-9,10
 680.E-9,0
 1000.E-9,0
 1010E-9,100
 1020E-9,100
 1030.E-9,0
OUTPUTS
 ES(SET),ERS(RESET),PLOT
XSTPSZ,PLOT
RUNCONTROLS
START TIME = -50.E-9
MAXIMUM PRINT POINTS = 100
COMPUTER TIME LIMIT = 5.5
STOP TIME = 350.E-9
END
```

Figure IV-9. Test Circuit Description for SET and RESET

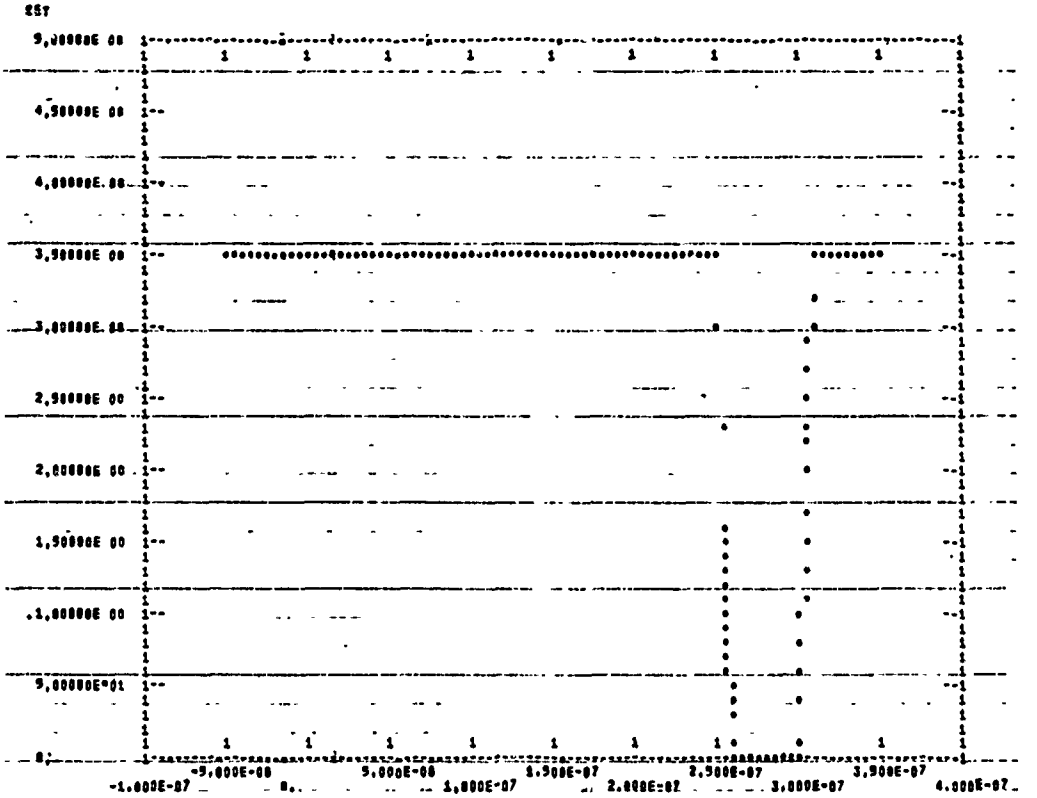


Figure IV-10. SET Input Signal

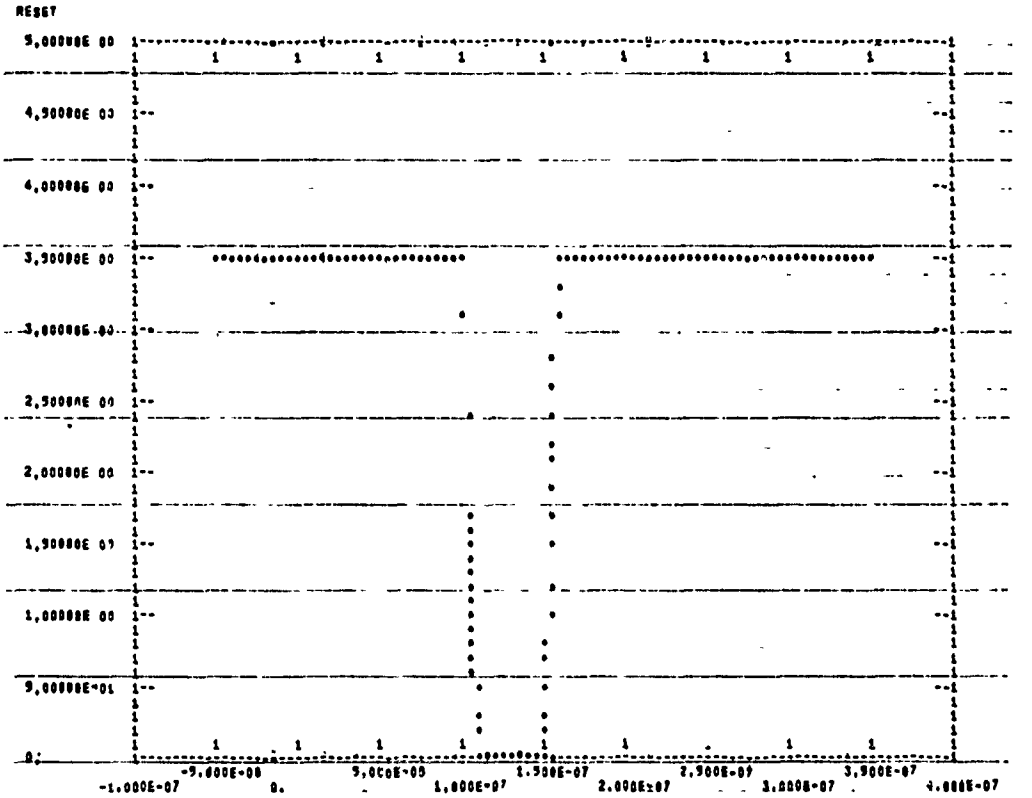


Figure IV-11. RESET Input Signal

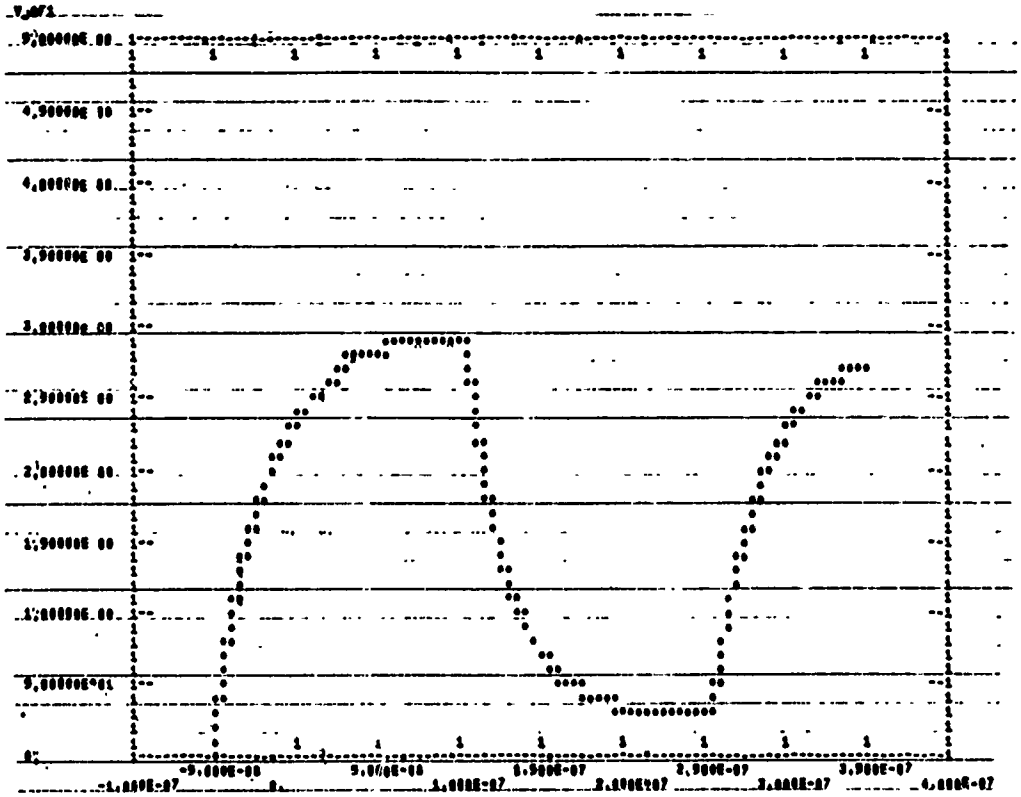


Figure IV-12. Q-Output

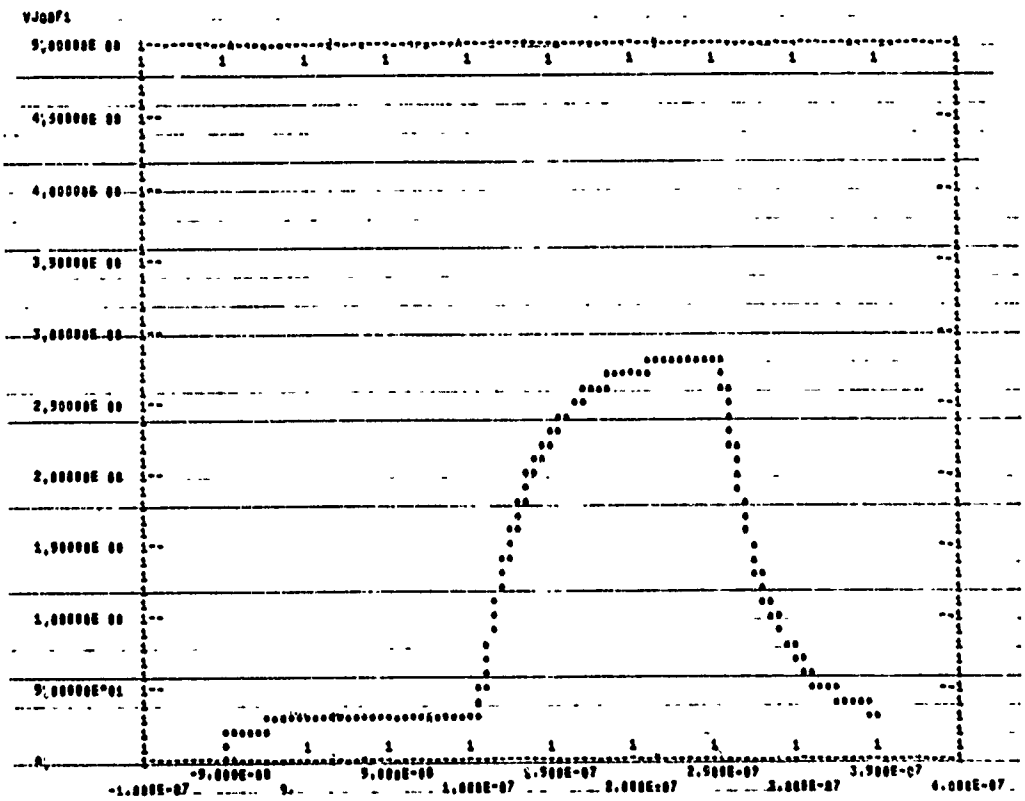


Figure IV-13. $\overline{Q}$-Output

```
        9774 SWITCHING TIME TEST
         AFWL CIRCUIT
         TEST FOR CLOCK AND SIGNAL
ELEMENTS
ES,GND-S=3.5
ERS,GND-RS=3.5
EC,GND-C=Q1(0,3.5,0.,18.E-9,20.E-9,9.E-9,100.E-9,6,TIME)
ED,GND-D=T5
F1,C-D-S-RS-Q-QB-GND=MODEL 9774
R1,Q-Q1=4300
C1,Q-Q1=2.E-12
R2,Q1-GND=750.
C2,Q1-GND=11.5E-12
D1,Q-5=MODEL 1N3605 (PERM)
R5,5-7=800
EL,GND-7=2.4
R3,QB-Q2=4300
C3,QB-Q2=2.E-12
R4,Q2-GND=750.
C4,Q2-GND=11.5E-12
D2,QB-6=MODEL 1N3605 (PERM)
R6,6-7=800
 FUNCTIONS
T5=0,3.5,61.E-9,3.5,70.E-9,0.,170.E-9,0.,188.E-9,3.5,250.E-9,3.5
 T2F1=
 0,0
 10.E-9,10
 20.E-9,10
 30.E-9,0
 200.E-9,0
 210.E-9,10
 220.E-9,10
 230.E-9,0
 280.E-9,0
 290.E-9,10
 300.E-9,10
 310.E-9,0
 650.E-9,0
 660.E-9,10
 670.E-9,10
 680.E-9,0
 1000.E-9,0
 1010E-9,100
 1020E-9,100
 1030.E-9,0
FUNCTIONS
Q1(A,B,C,D,E,F,G,H,Y)=(FGEN(A,B,C,D,E,F,G,H,Y))
OUTPUTS
EC(CLOCK),ED(SIG),PLOT
XSTPSZ,PLOT
RUNCONTROLS
MAXIMUM PRINT POINTS = 100
COMPUTER TIME LIMIT = 5.5
STOP TIME = 499.E-9
END
```

Figure IV-14. Test Circuit Description for CLOCK and SIGNAL

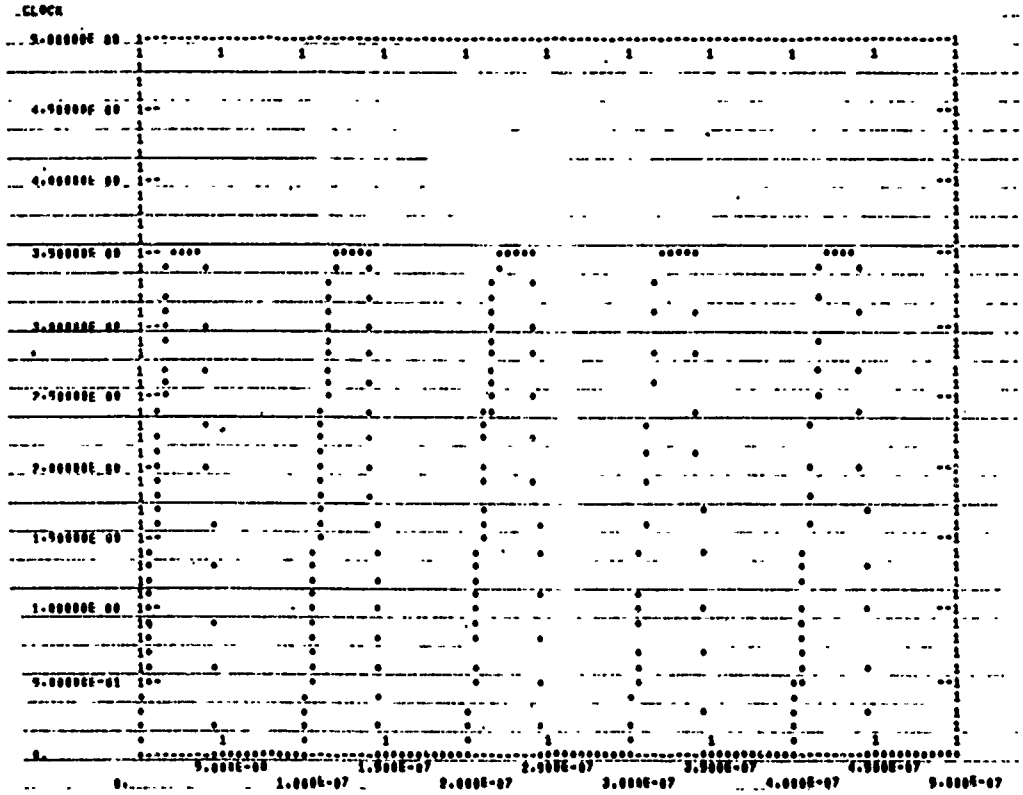


Figure IV-15. CLOCK Input Signal

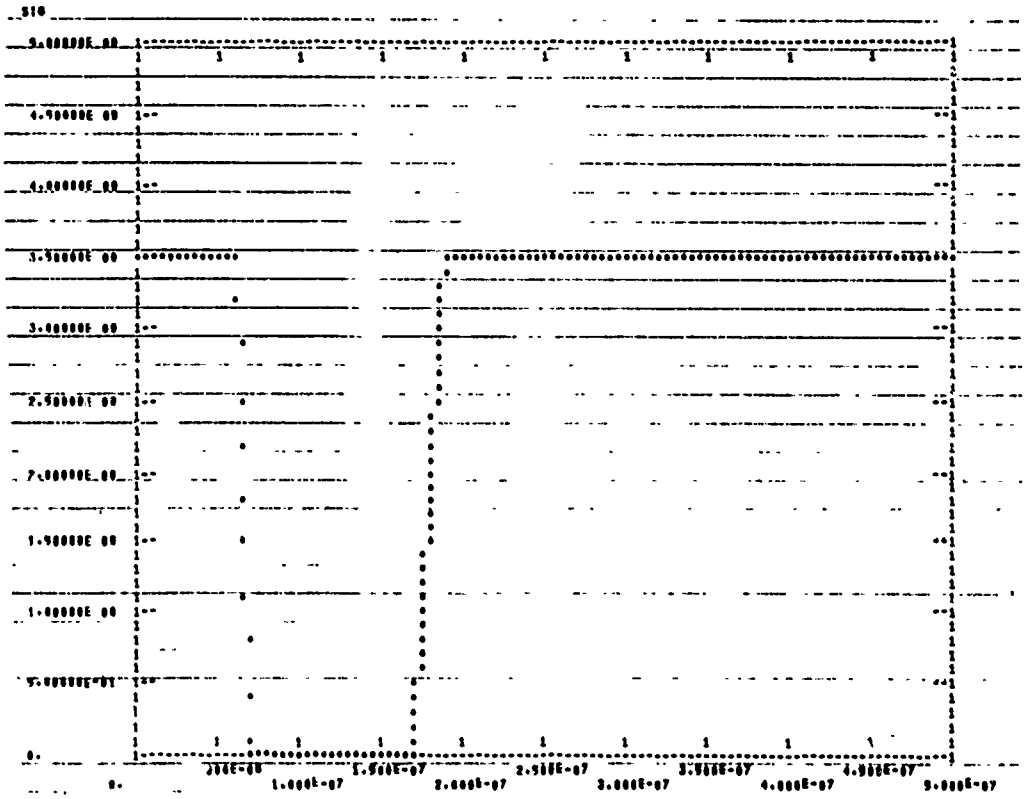


Figure IV-16. Input Signal

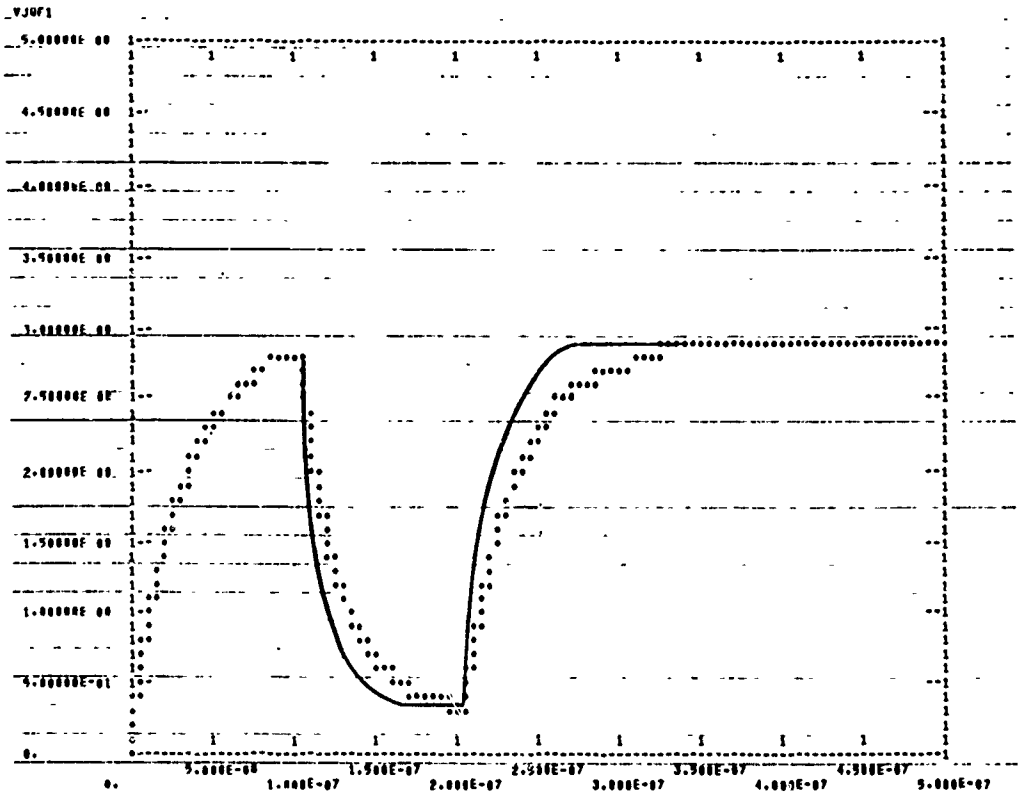


Figure IV-17. Q-Output

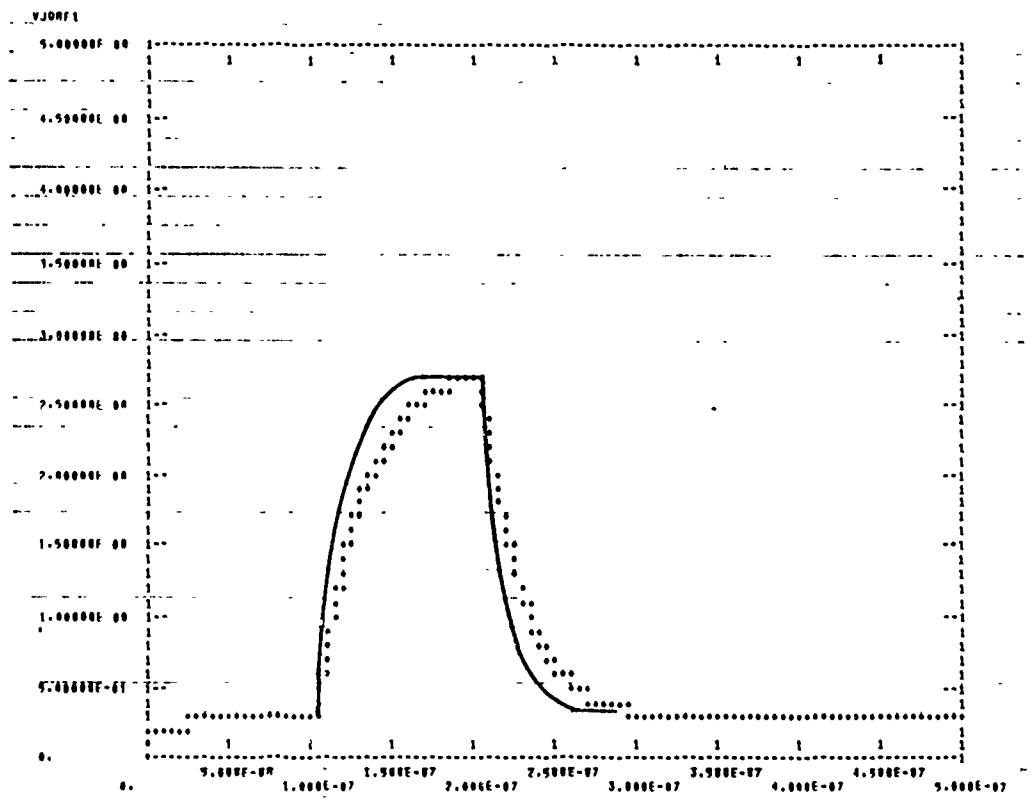


Figure IV-18. $\overline{Q}$-Output

It should be noted that the first 80 to 85 nanoseconds on Figure IV-17 and IV-18 represent an initializing condition; i.e., the time required for the circuit/devices to establish a quiescent performance condition. The positive initializing time required on Figure IV-12 is somewhat reduced since the computer is started at 50 nanoseconds before the analysis is started (t = -50 nanoseconds). However, normal circuit/device performance is demonstrated to exist after this condition is reached.

C. RADIATION EFFECTS

1. GAMMA RADIATION

Exposing the device to a nuclear radiation environment may affect normal performance by causing the Q and $\overline{Q}$ signal levels to vary. When exposed to pulsed gamma radiation at dose rate levels of approximately $3 \times 10^{+10}$ rads (Si)/second, the performance is only temporarily affected. Extensive testing was done by the General Electric Company on four devices (each containing two 9774 circuits). The test report with photographic recording of the results is included in Appendix IV-B.

Although no attempt was made to duplicate all of the radiation exposure conditions, several "typical" conditions were selected. These are identified as condition 8, 10 and 11.

To appropriately include the radiation effects it was necessary to modify the device model. This was accomplished by changing the entries for Table T1 in the model description (Figure IV-6), to reflect the response of the circuit to the radiation in such a manner as to agree with the observed results. Consequently, the listing was changed to indicate a value of -1 when the voltage across JR1 and/or JR2 is 0 volts, a value of -0.5 when the voltage is 1 volt, a value of +0.5 when the voltage is 2 volts, and a value of +1.5 when the voltage is 3 volts. Figure IV-19 shows the manner in which this was accomplished.

For condition 11, the radiation effect in the computer is caused to occur when the time equals 250 nanoseconds. The gamma ray pulse is 30 nanoseconds wide and is described in Table 2F1 (T2F1) on Figure IV-20. Condition 11 requires that the preset and clear be set "high", and the clock and data be set "low", which results in the Q being high and $\overline{Q}$ low. These conditions exist at 250 nanoseconds, at which time the radiation effects are simulated.

Figure IV-21 indicates the relative signal levels versus time for the three simulated conditions. Since the preset and clear signals are maintained at a constant, non-interfering level for all test conditions, they are not shown on this figure.

The result of this application of simulated radiation is shown in Figures IV-22 and IV-23 for Q and $\overline{Q}$ respectively. Drawn on the computer printouts are the results observed during the actual tests. The varying clock pulse is shown on Figure IV-24.

Condition 10 test requirements are that the clock be "low" and the data "high" while Q is "low" and $\overline{Q}$ is "high". These conditions exist at 660 nanoseconds, at which time the radiation effects are simulated.

Condition 8 test requirements are that the clock and data are "high" while Q is "high" and $\overline{Q}$ is "low". These conditions exist at 935 nanoseconds, at which time the radiation effects are simulated.

```
MODEL 9774(CK-D-SET-RS-Q-QB-G)
        DUAL D FLIPFLOP
            VERSION 3
 ELEMENTS
  JCK,CK-D=0
  JS,SET-D=0
  JRS,RS-D=0
  JD,D-D=0
  JQ,Q-D=0
  JQB,QB-D=0
  E1,D-1=FF1(VJS,VJRS,VJCK,VJD,TIME)
  R1,1-2=100.
  C1,2-D=FKC(E1,VC1)
  JR1,2-D=Q1(T1(VJR1),T2)
  E2,D-3=X1(3.1-F1)
  R2,3-4=100.
  C2,4-D=FKC(E2,VC2)
  JR2,4-D=Q1(T1(VJR2),T2)
  E3,D-5=X2(VJR1)
  R3,5-D=100.
  E4,D-6=X3(VJR2)
  R4,6-QB=100.
 FUNCTIONS
 Q1(A,B)=(A,B)
  T1=
  0.,-1.
  1.,-.5
  2.,.5
  3.,1.5
 OUTPUTS
  VJQ,VJQB,VC1,VC2,E1,E2,E3,E4,C1,C2,PLOT
  VJR1,VJR2,PLOT
```

Figure IV-19. Computer Model Description With Gamma Effects

```
      TPP TESTS 9774 D FLIPFLOP
        AFWL CIRCUIT
 TEST CONDITIONS II AND 7
 ELEMENTS
  ES,GND-S = T11
 FRS,GND-RS=3.5
 EC,GND-C=Q1(0,3.5,0.,18.E-9,173.E-9,9.E-9,400.E-9,6,TIME)
  ED,GND-D=T5
 E1,C-D-S-RS-Q-QB-GND=MODEL 9774
 R1,D-Q1=430
 C1,D-Q1=2.E-12
 R2,Q1-GND=750.
 C2,Q1-GND=11.5E-12
 D1,D-5=MODEL 1N3605 (PERM)
 R5,5-7=800
 EL,GND-Z=2.4
 R3,QB-Q2=4300
 C3,QB-Q2=2.E-12
 R4,Q2-GND=750.
 C4,Q2-GND=11.5E-12
 D2,QB-6=MODEL 1N3605 (PERM)
 R6,6-7=800
  FUNCTIONS
 T5=0,3.5,225.E-9,3.5,234.E-9,0.,620.E-9,0.,638.E-9,3.5,995.E-9,3.5
  T11 = 0.,0.,0.,3.5
  T2F1=
  0,0
  235.E-9,0.
  235.E-9,.5
  250.E-9,1.
  265.E-9,.5
  265.E-9,0.
  2000.E-9,0.
 Q1(A,B,C,D,E,F,G,H,Y)=(FGEN(A,B,C,D,E,F,G,H,Y))
 OUTPUTS
 EC(CLOCK),PLOT
  ES(SET),PLOT
 XS(PSZ),PLOT
 RUNCONTROLS
  MAXIMUM PRINT POINTS - 150
 COMPUTER TIME LIMIT = 5.5
  STOP TIME = 990.E-9

 END
```

Figure IV-20. Gamma Radiation - Test Circuit Description

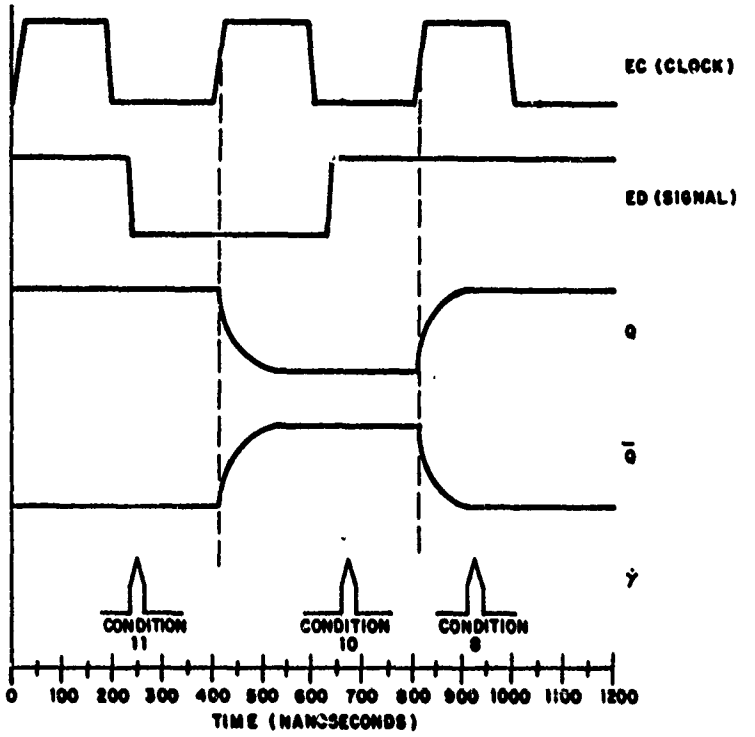


Figure IV-21. Simulated Gamma - Signal Timing Conditions

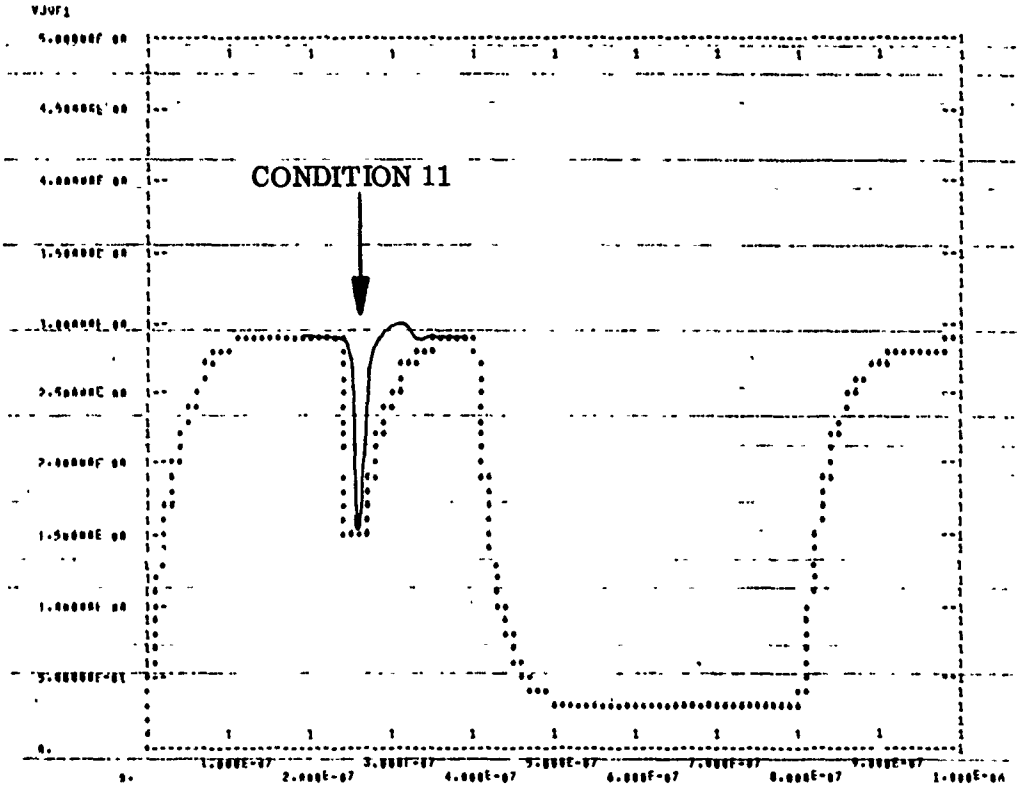


Figure IV-22. Q-Response for Condition 11

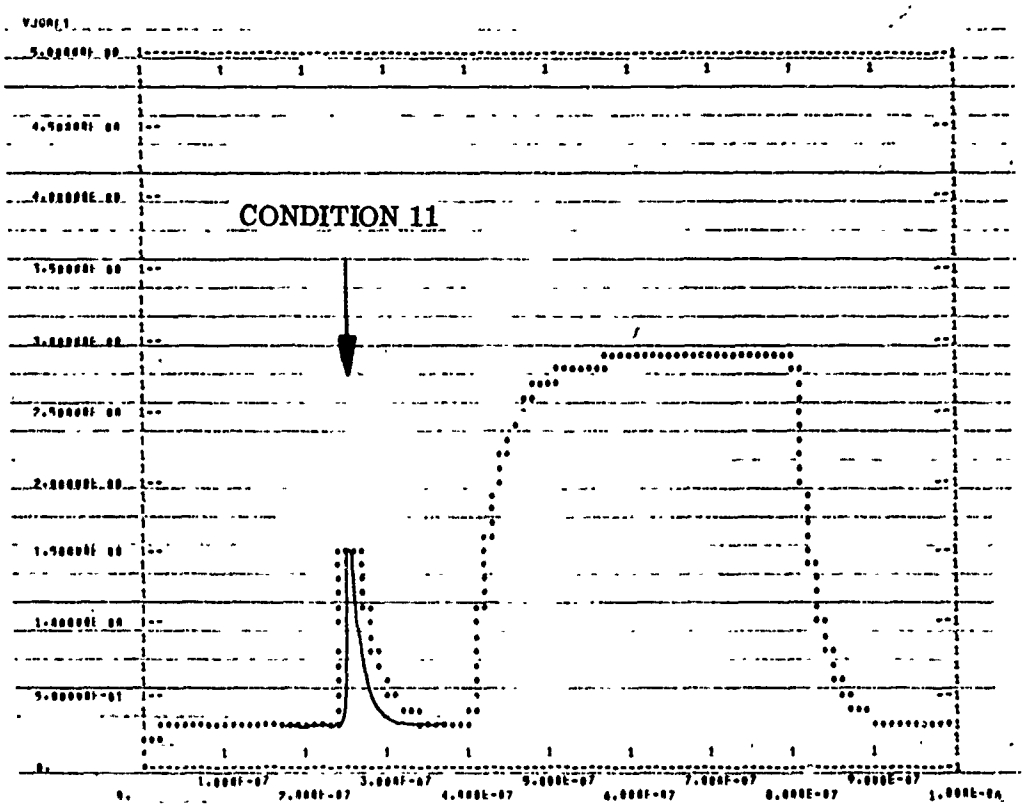


Figure IV-23. $\overline{Q}$-Response for Condition 11

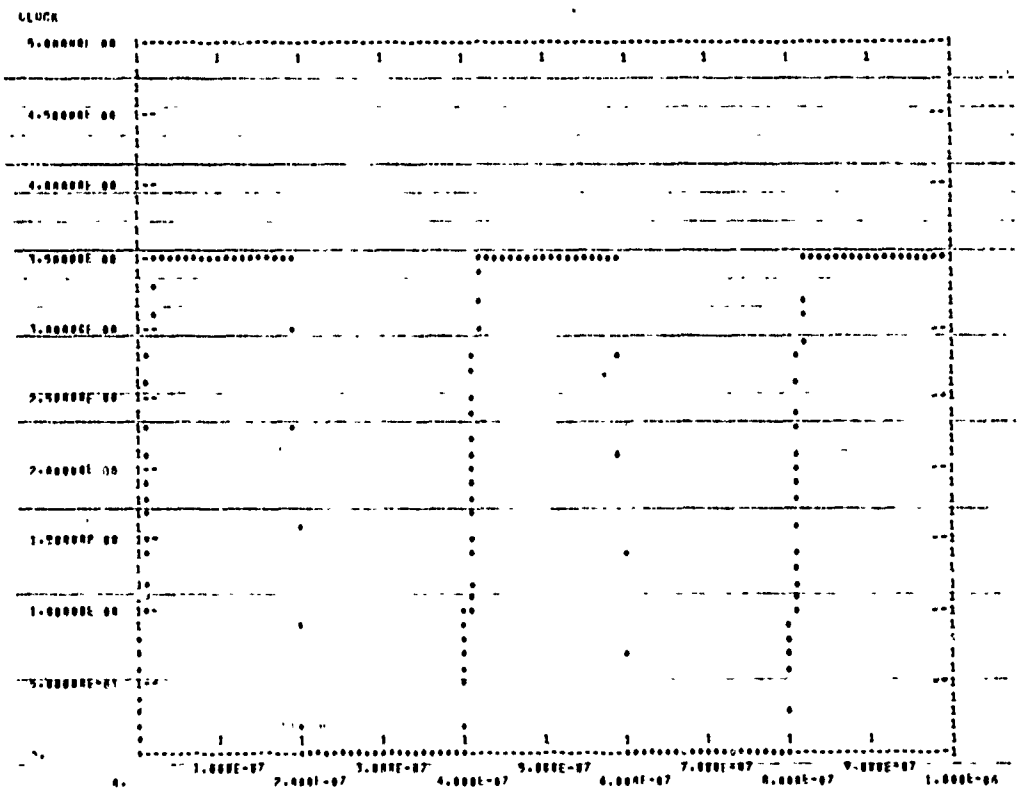


Figure IV-24. Clock Input Signal for Gamma Radiation Simulations

The results of the simulated radiation injection for both of these test conditions are shown on Figures IV-25 and IV-26 for Q and $\overline{Q}$ respectively. Drawn on the computer printouts are the results observed during actual tests.

The figures indicate excellent agreement between the computed results and the laboratory test observations.

2. NEUTRON RADIATION

When the device is exposed to neutron radiation conditions, its performance may be degraded either temporarily or permanently. The degree of the degradation, as well as the device recovery time for those conditions which permit recovery, depends upon the exposure level.

Exposure of test circuits to fluence levels of 1.2×10^{14} results in an output level reduction of approximately 0.4 volt, when the output signal is at a 1 level. When the output signal is at a 0 level, the voltage is increased by about 0.2 volt. These results were observed by the Air Force Weapons Laboratory when they exposed these devices and are reported in Reference 1*.

Figure IV-27 presents the circuit transfer degradation observed during these tests, for various fluence levels. For curve 4, which represents the test condition 4, the output signal level drops from about 3.1 volts to approximately 2.7 volts and rises from about 0.4 volt to approximately 0.6 volt.

The method for incorporating this response change into the model is shown in Figure IV-28. The value of voltage sources E3 and E4, and thus the output voltage EQ and EQB, are changed from a simple dependency on the voltage across sources JR1 and JR2, respectively, to a dependency upon both the voltage across the source and the fluence level, the fluence being defined as P2. This change in dependency is accomplished by use of an additional subroutine, FNVT.

The subroutine FNVT is shown on Figure IV-7; the computer circuit description to produce the analysis in Figure IV-29. The inclusion of the neutron exposure effects is accomplished by redefining P1 and P2, in the model callout, to be P5 and P6 respectively. P5 and P6 establish the values for FNVT and thus modify the values of E3 and E4 in the device model.

The effect of the subroutine FNVT is seen in Figures IV-30 and IV-31, for Q and $\overline{Q}$ respectively. In Figure IV-30, the 1 level voltage is reduced from about 2.9 volts (Figure IV-12) to approximately 2.5 volts and the 0 signal has been increased from about 0.2 volt to 0.4 volt. These results agree with the observed laboratory data.

This method of including fluence effects represents an approximation of the results shown in curve 4 of Figure IV-27. A more sophisticated and accurate representation would be to mathematically describe curve 4 and allow P5 and P6 to represent the resultant equation. However, the present model does demonstrate a satisfactory procedure for incorporating these conditions into the device model description.

---

* ibid. page 16

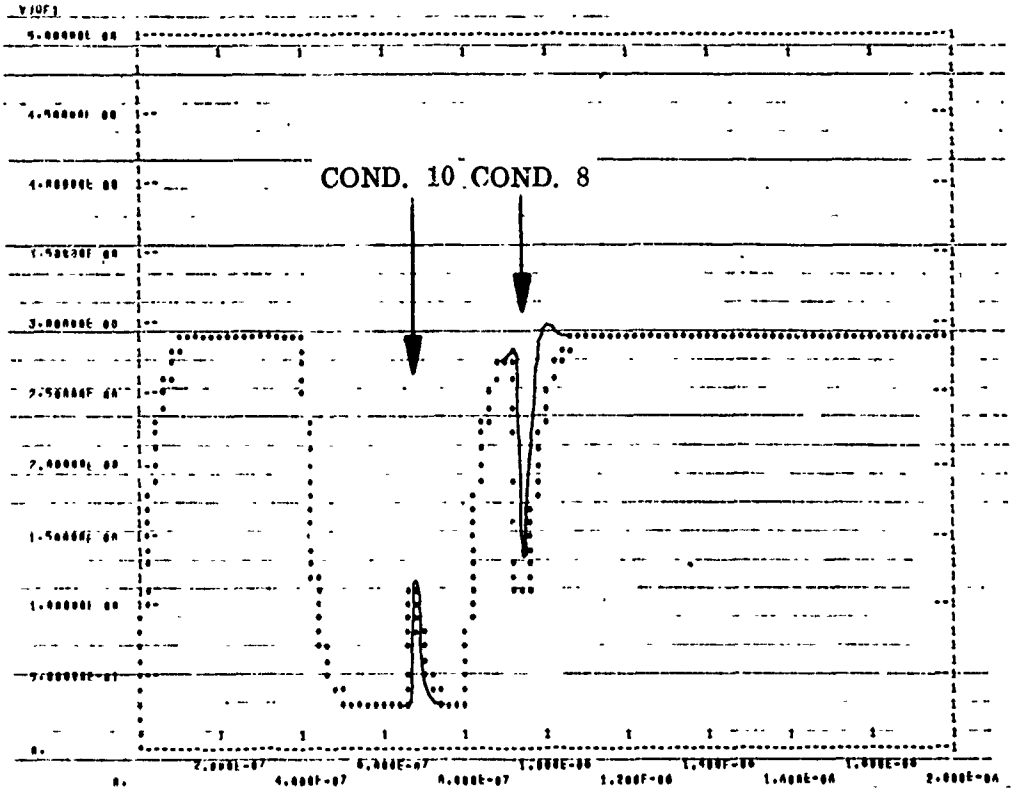


Figure IV-25. Q-Response for Conditions 8 and 10

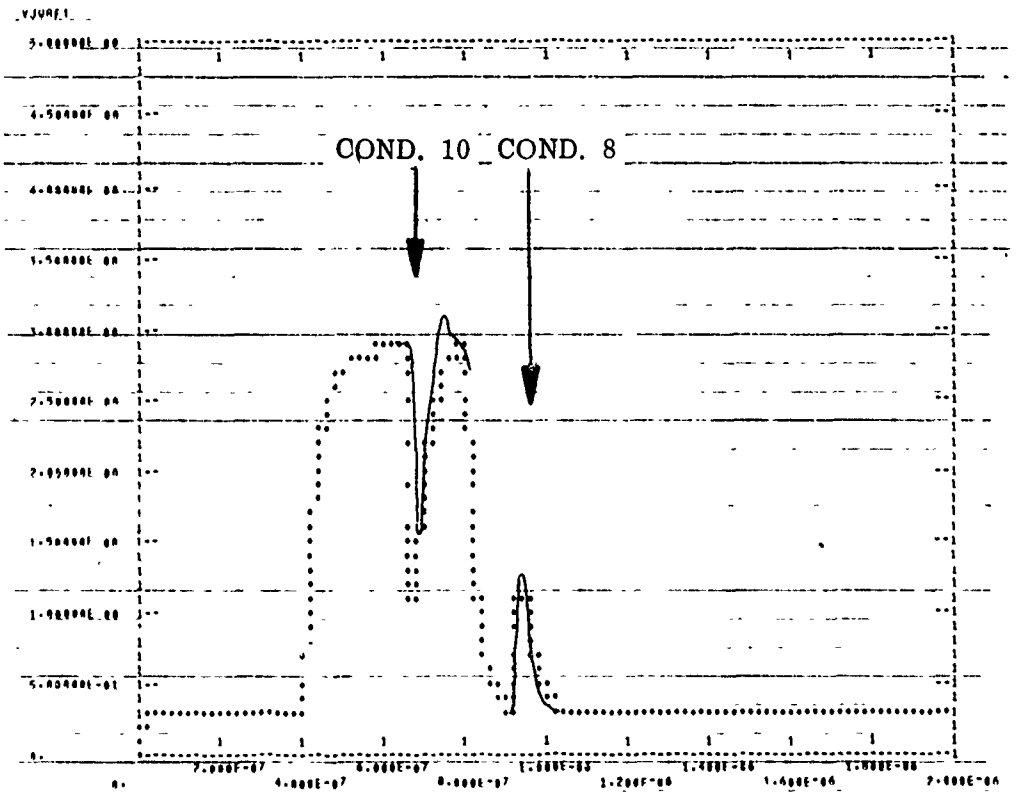


Figure IV-26. $\overline{Q}$-Response for Conditions 8 and 10

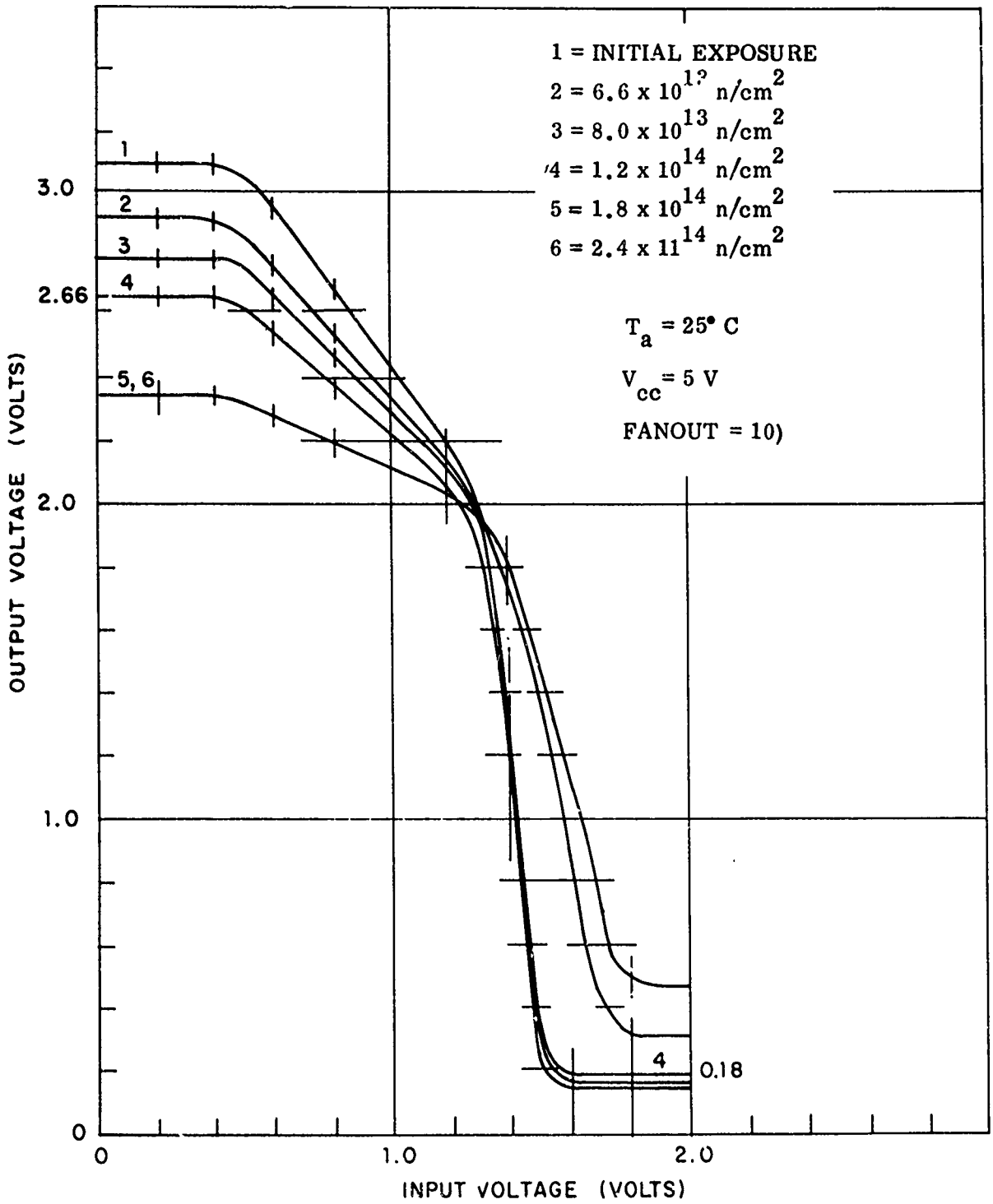


Figure IV-27. Neutron Radiation - Circuit Transfer Function

```
MODEL 9774(CK=D-SET-RS-Q-QB=0)
      DUAL D FLIPFLOP
        VERSION 3
ELEMENTS
JCK,CK-0=0
JS,SET-0=0
JRS,RS-0=0
JD,D=0=0
JQ,Q=0=0
JQB,QB=0=0
E1,0=1=FBI(VJS,VJRS,VJCK,VJD,TIME)
R1,1=2=100.
C1,2=0=FKC(E1,VC1)
JR1,2,0=Q1(T1(VJR1),T2)
E2,0=3=X1(3,1=E1)
R2,3=4=100.
C2,4=0=FKC(E2,VC2)
JR2,4-0=Q1(T1(VJR2),T2)
E3,0=5=X2(VJR1+P1)
R3,5=0=100.
E4,0=6=X3(VJR2+P2)
R4,6=QB=100.
FUNCTIONS
Q1(A,B)=(A*B)
T1=0,,0,
T2=0,,0,
DEFINED PARAMETERS
P1=0,
P2=0,
OUTPUTS
VJQ,VJQB,E3,E4,PLOT
```

Figure IV-28. Model Description With Neutron Effects

```
        9774 SWITCHING TIME TEST
         AFWL CIRCUIT
         TEST FOR CLOCK AND SIGNAL
ELEMENTS
 ES,GND=S=3,5
 ERS,GND-RS=3,9
 EC,GND=C=Q1(0,3,5;0,;18,E-9,20,E-9,9,E-9,100,E-9,8,TIME)
 ED,GND=D=T5
  F1;C=D=S=RS=Q=QB=GND=MODEL 9774(CHANGE P1=P5,P2=P6)
 R1,Q=Q1=4300
 C1,Q=Q1=2,E-12
 R2,Q1=GND=750,
 C2,Q1=GND=11,5E-12
 D1,Q=5=MODEL 1N3605 (PERM)
 R5,5=7=800
 EL,GND=7=2,4
 R3,Q3=Q2=4300
 C3,Q3=Q2=2,E-12
 R4,Q2=GND=750,
 C4,Q2=GND=11,5E-12
 D2,Q3=6=MODEL 1N3605 (PERM)
 R6,6=7=800
  FUNCTIONS
 T5=0,3,5,61,E-9,3;5,70,E-9,0,;170,E-9;0,;188;E-9,8,5,250,E-9,4,5
 Q1(A,B,C,D,E,F,G,H,Y)=(FGEN(A,B,C,D,E,F,G,H,Y))
  DEFINED PARAMETERS
  P5=FNVT(VC1F1,0,4,0,2)
  P6=FNVT(VC2F1,0,4,0,2)
 OUTPUTS
 EC(CLOCK),ED(SIG),PLOT
 XS,PSZ,PLOT
 RUNCONTROLS
 MAXIMUM PRINT POINTS = 100
 COMPUTER TIME LIMIT = 5,5
 STOP TIME = 499,E-9
 END
```

Figure IV-29. Neutron Radiation - Test Circuit Description

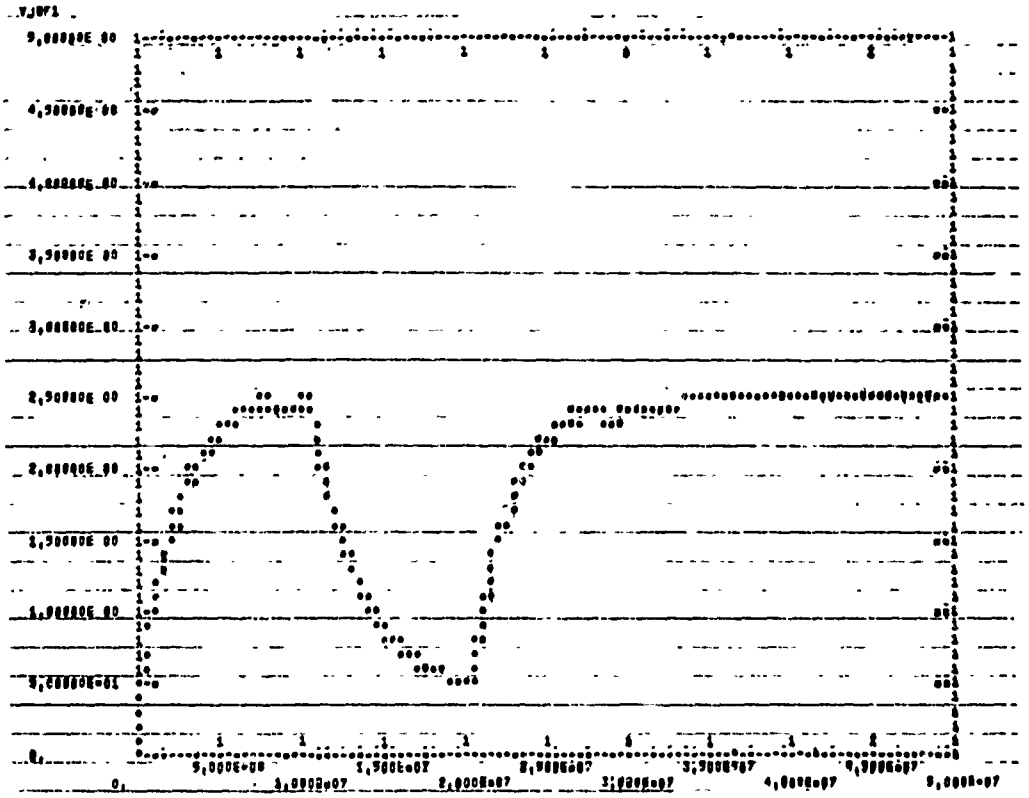


Figure IV-30. Q-Response to Neutron Radiation

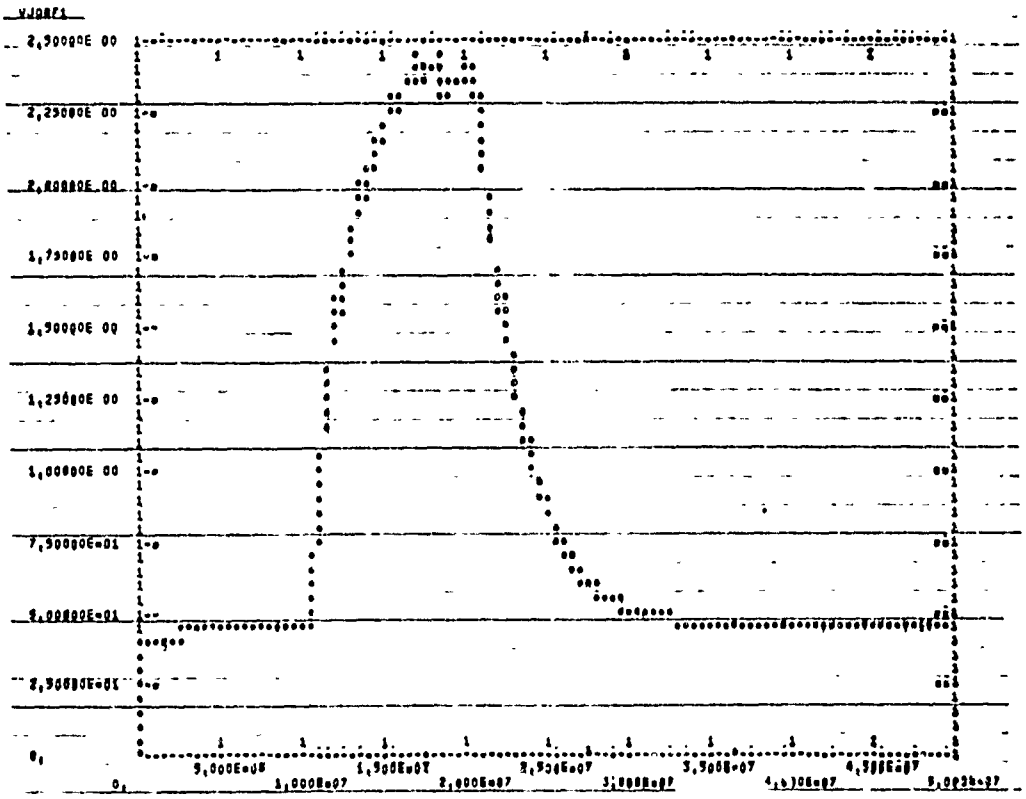


Figure IV-31. $\overline{Q}$-Response to Neutron Radiation

SECTION V

TEXAS INSTRUMENTS RSN54L72 FLIP-FLOP

The RSN54L72 flip-flop operates on the basis of the master-slave principle in which the output changes state on the negative going edge of the clock pulse. The device features multiple J and K inputs with direct PRESET (S_D) and CLEAR (R_D) capability for asynchronous operation, and complementary Q and $\overline{Q}$ outputs. Logic information present on the J and K inputs, plus information fed back from the Q and $\overline{Q}$ outputs, sets the master section. The sequence of operation for this device is as follows:

1) With the clock input at a logic 0 level, the master section is isolated from the slave section by transfer gates.

2) As soon as the clock pulse rises and reaches the clock input threshold level of 1.5 volts, logic information present on the J and K inputs is entered into the master section.

3) With the clock at a logic 1 level, the master section remains isolated from the slave. As the clock pulse begins to fall, the input NAND gates become disabled and the transfer gates are turned on.

4) As soon as the clock pulse falls to the threshold level (approximately 1.5 volts), the logic information present at the output of the master section is transferred to the slave, which controls the output.

As long as the logic information on the J and K inputs remains stable, the flip-flop will respond in accordance to the truth table whenever the clock makes a 1 to 0 transition. Because the flip-flop operates on dc levels rather than dynamic signal changes, no maximum rise and fall times are imposed on the clock or J and K waveforms.

The asynchronous PRESET (S_D) and CLEAR (R_D) inputs may be applied at any time and will override the effect of the clock input pulse. The S_D and R_D are active when in a low (logic 0) state.

The schematic diagram of the integrated circuit is shown in Figure V-1. The functional logic representation is shown in Figure V-2 and is represented by eight NAND and four NOR gates.

The truth table for the device as described by the manufacturer is shown in Table V-1 for the condition when the PRESET (S_D) and CLEAR (R_D) signal levels are high (at 1 level).

The electrical characteristics of the device defined by the manufacturer are shown in Table V-2.

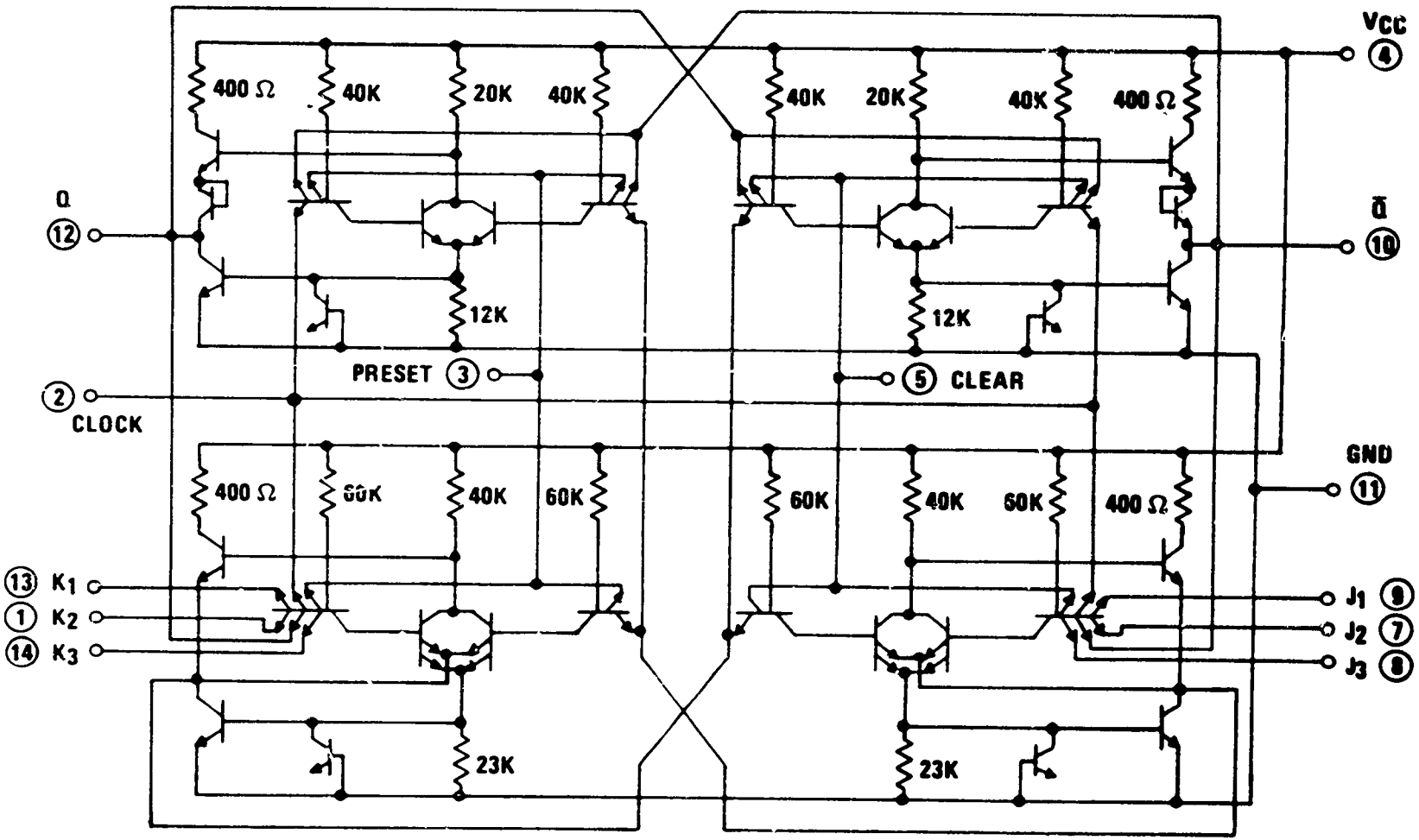
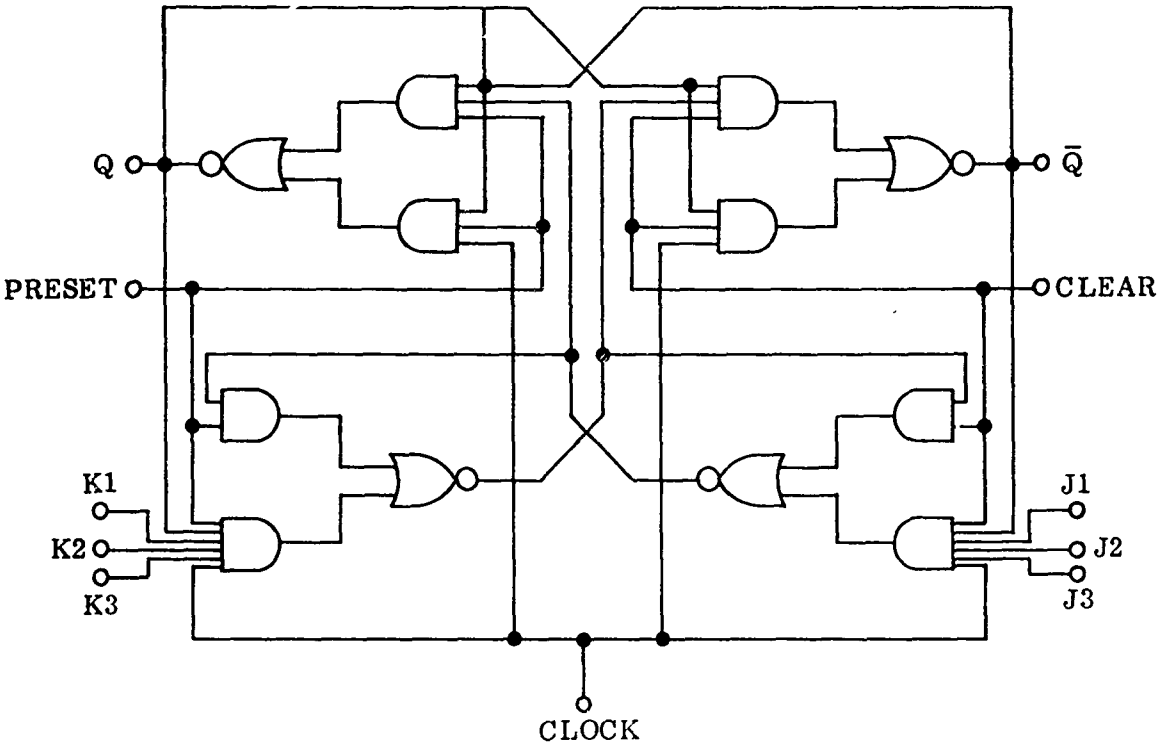
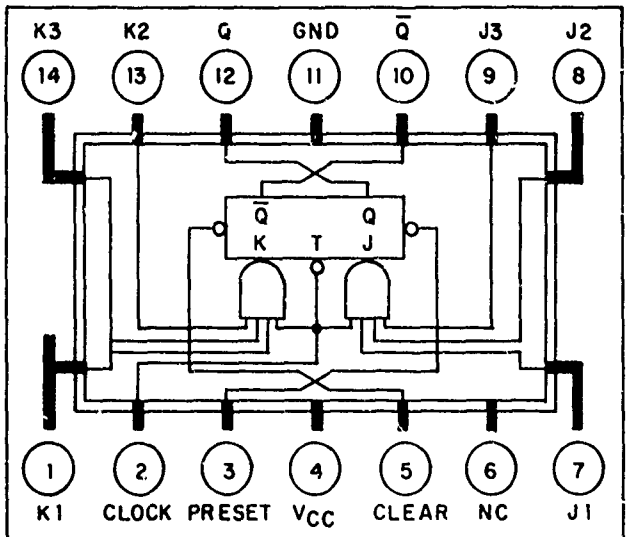


Figure V-1. Schematic RSN54L72 Master-Slave Flip-Flop



H FLAT PACKAGE (TOP VIEW)



POSITIVE LOGIC:
LOW INPUT TO PRESET SETS Q TO HIGH LEVEL
LOW INPUT TO CLEAR RESETS Q TO LOW LEVEL
PRESET AND CLEAR ARE INDEPENDENT OF CLOCK

NC - NO INTERNAL CONNECTION

Figure V-2. Functional Logic Representation

TABLE V-1.
TRUTH TABLE

INPUTS AT t_n		OUTPUTS AT t_{n+1}	
J	K	Q	$\bar{Q}$
L	L	Q_n	$\bar{Q}_n$
L	H	L	H
H	L	H	L
H	H	$\bar{Q}_n$	Q_n

J = J1 · J2 · J3

K = K1 · K2 · K3

t_n = bit time before clock pulse

t_{n+1} = bit time after clock pulse

Q_n = level of output Q at t_n

$\bar{Q}_n$ = complement of Q_n or level of output $\bar{Q}$ at t_n

TABLE V-2.
ELECTRICAL CHARACTERISTICS
(Over recommended operating free-air temperature range, unless otherwise noted)

PARAMETER		TEST CONDITIONS*	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = Min.	1.9			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = Min.			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = Min I_{load} = 100 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = Min I_{sink} = 2 mA			0.3	V
$I_{in(0)}$	Logical 0 level input current	V_{CC} = Max V_{in} = 0.3V			-0.18	mA
$I_{in(0)}$	Logical 0 level input current at preset, clear, or clock	V_{CC} = Max. V_{in} = 0.3V			-0.40	mA
$I_{in(1)}$	Logical level input current	V_{CC} = Max. V_{in} = 2.4V			10	μA
		V_{CC} = Max. V_{in} = 5.5V			100	μA
$I_{in(1)}$	Logical 1 level input current at preset or clear	V_{CC} = Max. V_{in} = 2.4V			20	μA
		V_{CC} = Max. V_{in} = 5.5V			200	μA
$I_{in(1)}$	Logical 1 level current into the clock input	V_{CC} = Max. V_{in} = 2.4V			20	μA
		V_{CC} = Max. V_{in} = 5.5V			200	μA
I_{OS}	Short-circuit output current	V_{CC} = Max.	-1		-15	mA
I_{CC}	Supply current	V_{CC} = 5V $V_{in(clock)}$ = 0			14	mA
f_{clock}	Maximum clock frequency	C_1 = 50 pF V_{CC} = 5V, T_A = 25°C		3		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	C_1 = 50 pF V_{CC} = 5V, T_A = 25°C			75	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	C_1 = 50 pF V_{CC} = 5V, T_A = 25°C			150	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_1 = 50 pF V_{CC} = 5V, T_A = 25°C	10		75	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_1 = 50 pF V_{CC} = 5V, T_A = 25°C	10		150	ns

*For conditions shown as Min. or Max. use Min. = 4.5V, Max. = 5.5V

A. MODEL DEVELOPMENT

1. MODEL 1

Two models were developed for the RSN54L72 flip-flop. The initial modeling approach was to simplify the logic, as represented in Figure V-2, by eliminating the NOR functions. These functions would be included in the model by means of several FORTRAN statements. The revised and simplified logic diagram to perform the flip-flop function is shown in Figure V-3 and consists of eight interconnected NAND gates. Each input and output terminal required to interface with the outside world is represented in SCEPTRE by a zero valued current source as shown in Figure V-4. The general black-box model representation is also shown in this figure.

Figure V-4 is the SCEPTRE model for Figure V-3. It shows the representation for the two input NAND stages (E1 and E2) which respond primarily to external signals, the intermediate stages (E3 through E6) which represent the master-slave relationships, and the output gates (E7 and E9). This model uses two variations of the basic 2 input NAND gate, a three input version, and a six input version. The voltage sources E8 and E10 are included to provide decoupling of any load effects on the model outputs, Q and $\overline{Q}$, and also to allow for incorporation of the neutron effect in the model.

The operation of each stage is as follows: (references are to Figure V-11)

- If any of the inputs is less than 0.8 volt, the voltage generator (E) is set at 3 volts. This is achieved through statement 90.
- If all of the inputs are greater than 1.9 volts, the voltage generator is set at 0 1 volt. This is achieved by statement 110.
- For intermediate values of input, the lowest input voltage controls the value of the voltage generator. This is achieved by statement 130.
- To control the delay between the time the clock signal falls to 1.5 volts and the circuit reaches the same level, it is necessary to provide a time delay circuit. This is achieved by means of the resistor-capacitor (R-C) network present in each gate circuit. Since the rise and fall times are different, the value of the capacitor is changed. The capacitor is set at one of the two values depending upon whether the output signal level is rising or falling. This is achieved by statement 290.

The current generator is used in each gate because each of the gates may be in a different state. A load circuit, for demonstrating proper device performance, is applied to both the Q and $\overline{Q}$ terminals (as shown in Figure V-16).

The clock timing is shown in Figure V-5; the Q output without radiation, in Figure V-6; with arbitrarily injected radiation, in Figure V-7. Figure V-8 shows the $\overline{Q}$ output without radiation; Figure V-9 shows the output with arbitrarily injected radiation. In both Figures V-7 and V-9, the radiation injection is intended to demonstrate the ability of the model to accept the gamma pulse and not to simulate any expected performance.

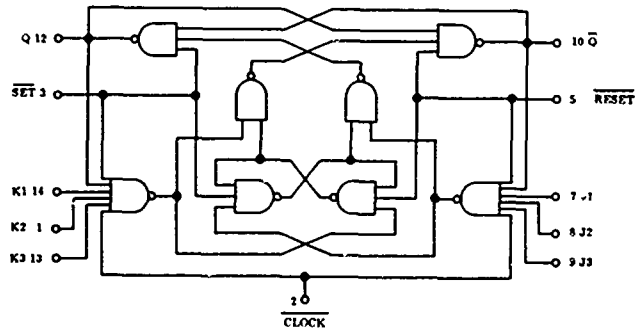


Figure V-3. Logic Diagram

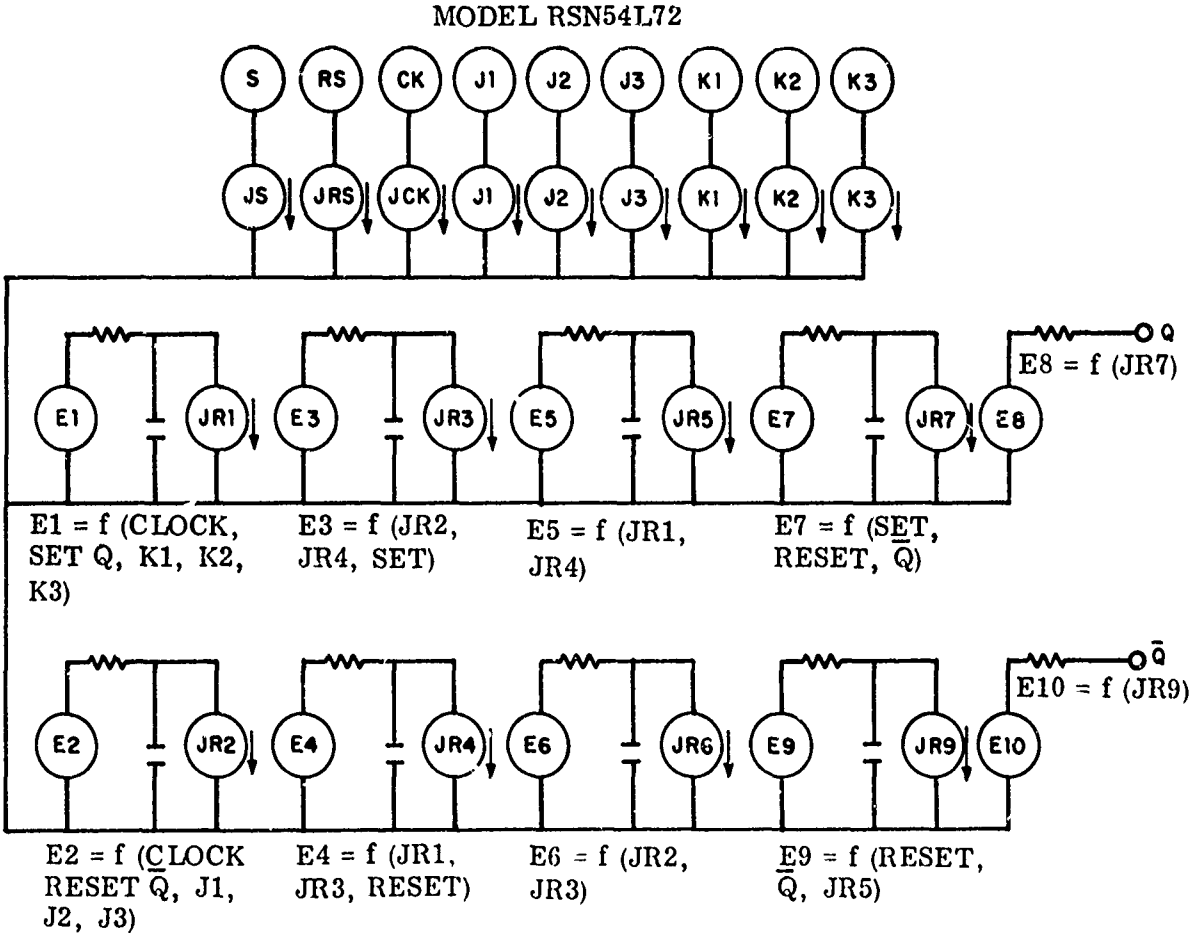


Figure V-4. RSN54L72 Device Model #1

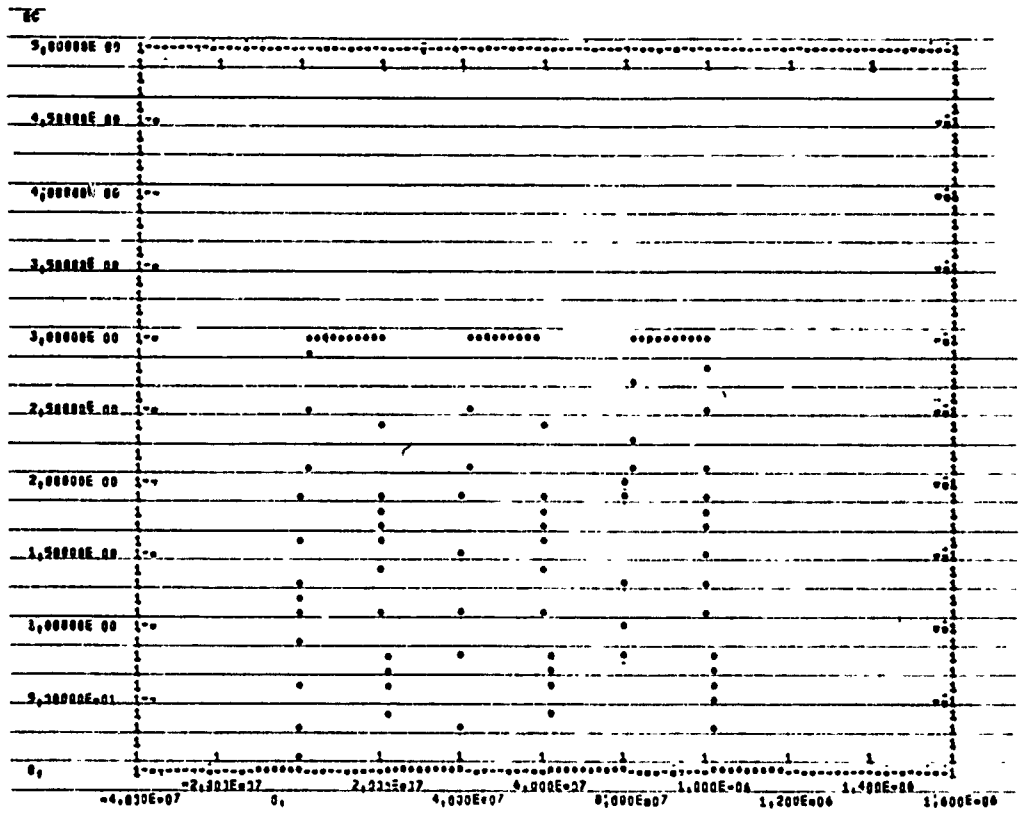


Figure V-5. Clock Timing

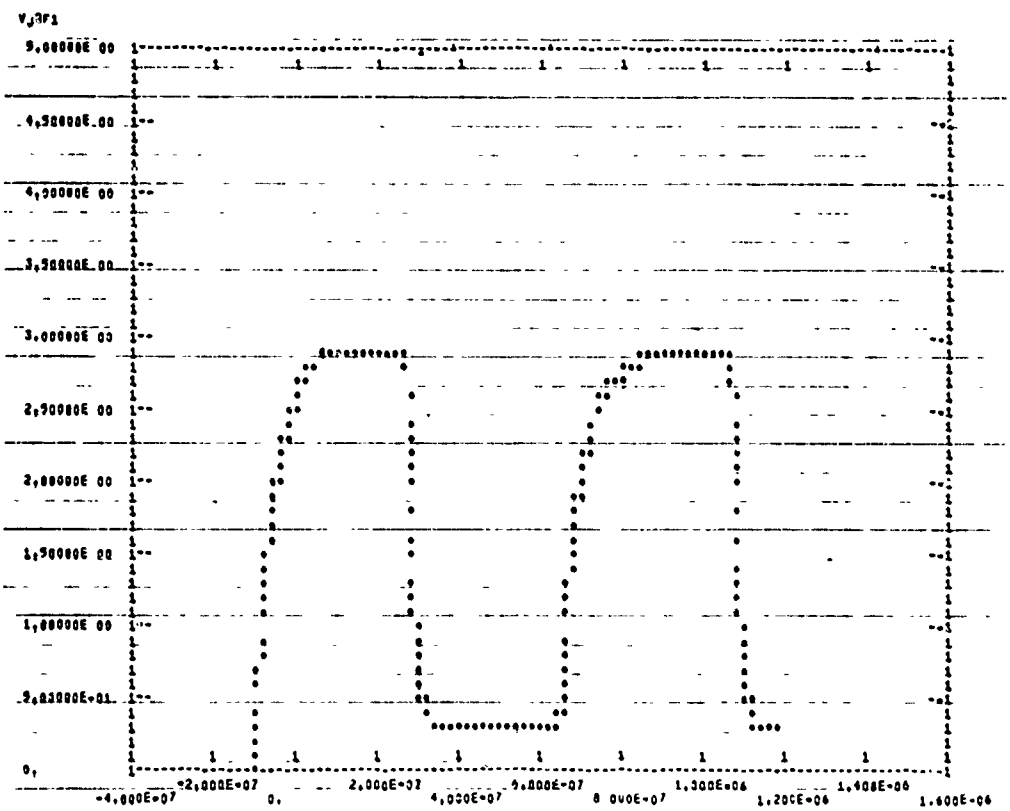


Figure V-6. Q Output Without Radiation

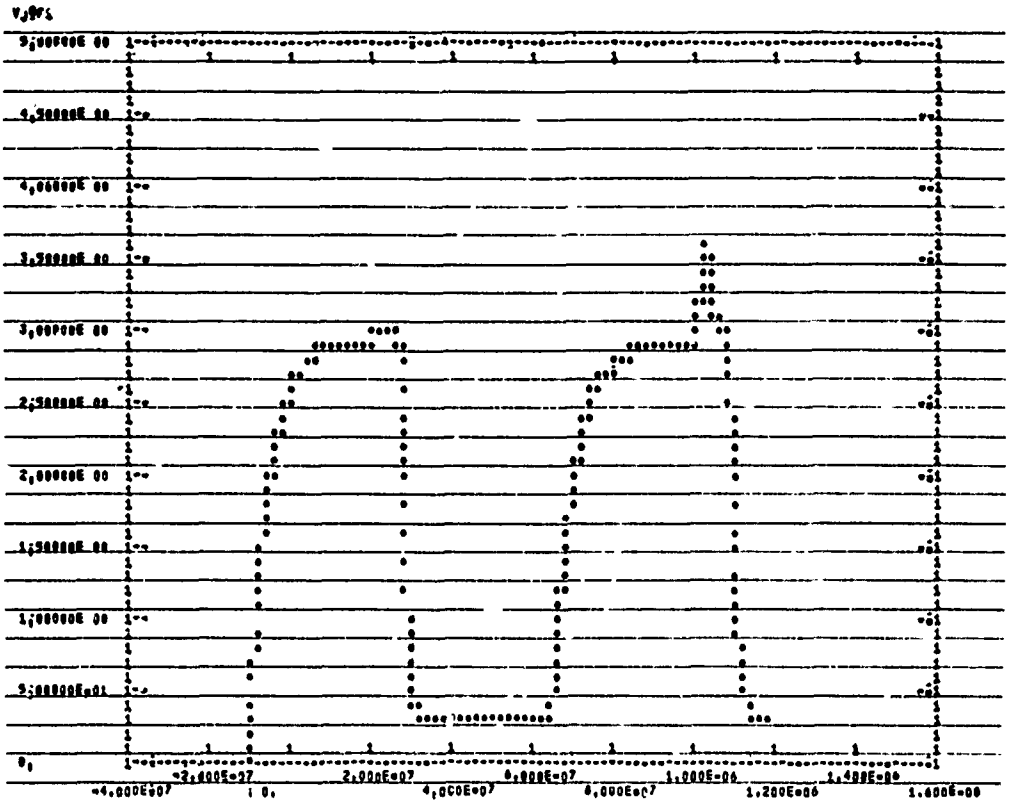


Figure V-7. Q Output With Radiation

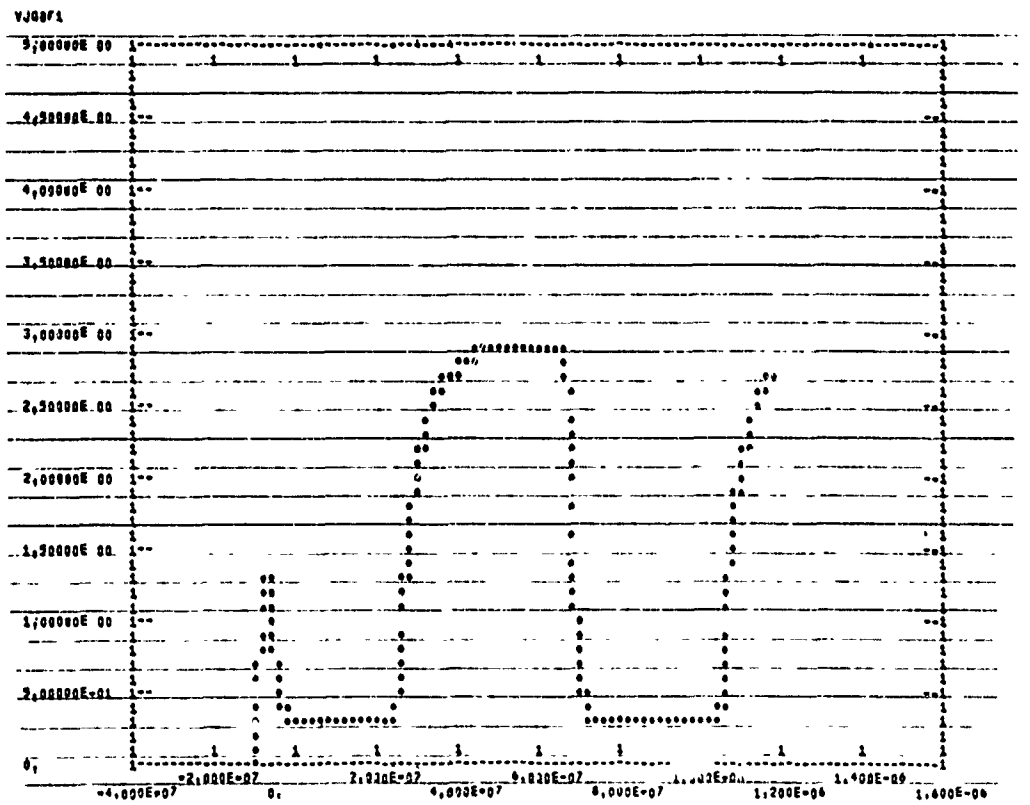


Figure V-8. $\overline{Q}$ Output Without Radiation

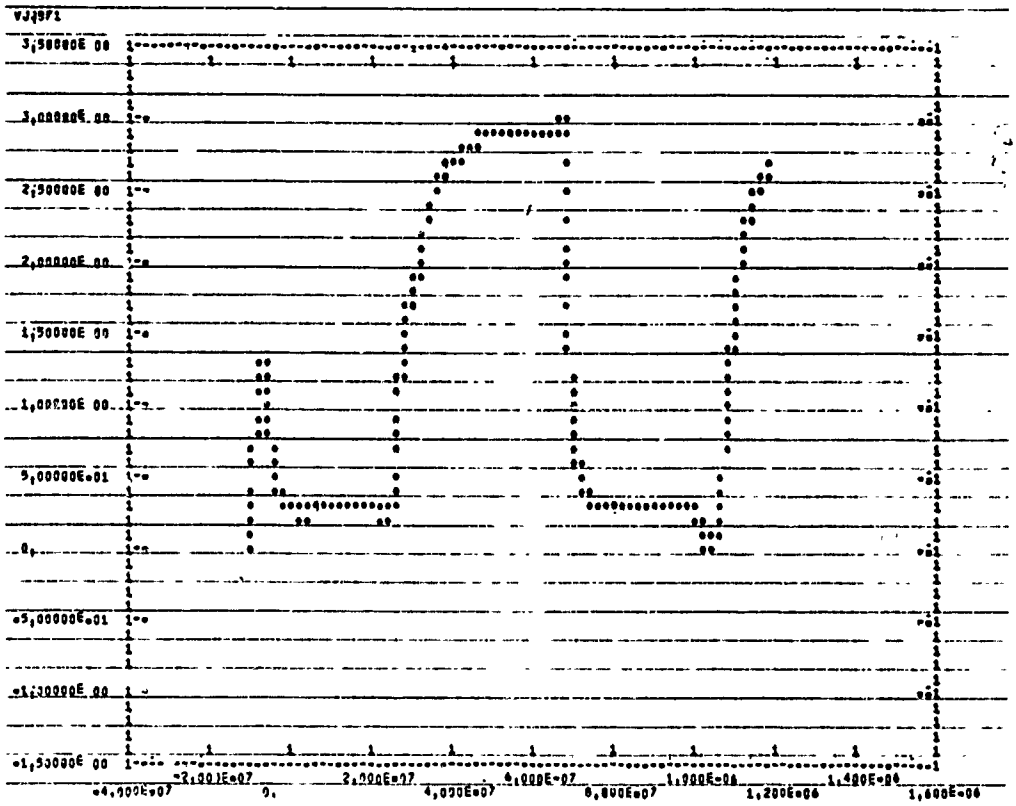


Figure V-9. $\overline{Q}$ Output With Radiation

The SCEPTRE description of the J-K flip-flop model is shown in Figure V-10. Table T1 of this figure is an arbitrary table to be used to demonstrate the response of the model to a gamma impulse radiation.

The function subprogram used in the calculation of the transfer function for the NAND gates and the variable delay time is shown in Figure V-11.

The circuit description used in SCEPTRE for the gamma radiation effects evaluation is shown in Figure V-12. Table T2F1 of this figure describes the time when the arbitrary radiation is caused to occur.

```
70  MODEL DESCRIPTION
80  MODEL RSN54L72  (CK-K1-K2-K3-SET-RS-J1-J2-J3-Q-QB-0)
90        J K FLIPFLOP
100 ELEMENTS
110 JCK,CK-0=0
120 JK1,K1-0=0
130 JK2,K2-0=0
140 JK3,K3-0=0
150 JS,SET-0=0
160 JRS,RS-0=0
170 J1,J1-0=0
180 J2,J2-0=0
190 J3,J3-0=0
200 JQ,Q-0=0
210 JQB,QB-0=0
220 E1,0-1=FE6(VJCK,VJK1,VJK2,VJK3,VJS,VJQ,.8,3.,1.9,.1,2.7)
230 R1,1-2=100
240 C1,2-0=FKC(E1,VC1,450E-12,180.E-12)
250 JR1,2-0=Q1(T1(VJR1),T2)
260 E2,0-3=FE6(VJCK,VJ1,VJ2,VJ3,VJRS,VJQB,.8,3.,1.9,.1,2.7)
270 R2,3-4=100
280 C2,4-0=FKC(E2,VC2,450E-12,180.E-12)
290 JR2,4-0=Q1(T1(VJR2),T2)
300 E3,0-5=FE3(VJR2,VJS,VJR4,1.2,3.,1.5,.1,2.7)
310 R3,5-6=100
320 C3,6-0=FKC(E3,VC3,430.E-12,150.E-12)
330 JR3,6-0=Q1(T1(VJR3),T2)
340 E4,0-7=FE3(VJR1,VJRS,VJR3,1.2,3.,1.5,.1,2.7)
350 R4,7-8=100
360 C4,8-0=FKC(E4,VC4,430.E-12,150.E-12)
370 JR4,8-0=Q1(T1(VJR4),T2)
380 E5,0-9=FE2(VJR1,VJR4,1.2,3.,1.5,.1,2.7)
390 R5,9-10=100
400 C5,10-0=FKC(E5,VC5,430.E-12,150.E-12)
410 JR5,10-0=Q1(T1(VJR5),T2)
420 E6,0-11=FE2(VJR2,VJR3,1.2,3.,1.5,.1,2.7)
430 R6,11-12=100
440 C6,12-0=FKC(E6,VC6,430.E-12,150.E-12)
450 JR6,12-0=Q1(T1(VJR6),T2)
460 E7,0-13=FE3(VJS,VJR6,VJQB,1.2,3.,1.5,.1,2.7)
470 R7,13-14=100
480 C7,14-0=FKC(E7,VC7,430.E-12,150.E-12)
490 JR7,14-0=Q1(T1(VJR7),T2)
500 E8,0-15=X1(VJR7)
510 R8,15-Q=100
520 E9,0-16=FE3(VJRS,VJR5,VJQ,1.2,3.,1.5,.1,2.7)
530 R9,16-17=100
540 C9,17-0=FKC(E9,VC9,430.E-12,150.E-12)
550 JR9,17-0=Q1(T1(VJR9),T2)
560 E10,0-18=X2(VJR9)
570 R10,18-QB=100
580FUNCTIONS
590Q1(A,B)=(A*B)
600T1=
610 0,.0001
620 1.9,.001
630 2.9,0
640 3.,-.0001
650 OUTPUTS
660VJQ,VJQB,JR1,VC1,JR2,VC2,JR3,VC3,JR4,VC4,JR5,VC5,PLOT
670JR6,VC6,JR7,VC7,JR9,VC9,VJS,VJRS,PLOT
```

Figure V-10. Computer Description - Model #1

```
 OLD DESIGN/FE6,R
READY
*LIST

10$S, N
20$:IDENT:150349-433-2536
30$:USERID:CIRCUIT$ANALYSIS
40$       FORTRAN
50$:PRMFL:B*,R/W,S,DESIGN/BJK
60$:REMOTE:P*,IQ
70CFJK          J-K NAND GATE
80        FUNCTION FE6(A,B,C,D,E,F,G,H,P,Q,Y)
90        IF(A.LE.G .OR. B.LE.G .OR. C.LE.G .OR. D.LE.G
100      *  .OR. E.LE.G .OR. F.LE.G) GO TO 4
110        IF(A.GE.P .AND. B.GE.P .AND. C.GE.P .AND.
120      *  D.GE.P .AND. E.GE.P .AND. F.GE.P) GO TO 5
130        FE6=Y-AMIN1(A,B,C,D,E,F)
140        RETURN
150 4      FE6=H
160        RETURN
170 5      FE6=Q
180        RETURN
190        ENTRY FE2(A,B,G,H,P,Q,Y)
200        IF(A.LE.G .OR. B.LE.G) GO TO 4
210        IF(A.GE.P .AND. B.GE.P) GO TO 5
220        FE6=Y-AMIN1(A,B)
230        RETURN
240        ENTRY FE3(A,B,C,G,H,P,Q,Y)
250        IF(A.LE.G .OR. B.LE.G .OR. C.LE.G) GO TO 4
260        IF(A.GE.P .AND. B.GE.P .AND. C.GE.P) GO TO 5
270        FE6=Y-AMIN1(A,B,C)
280        RETURN
290        ENTRY FKC(A,B,C,D)
300        X=C
310        IF(A.GE.B)X=D
320        FE6=X
330        RETURN
340        END
350$:ENDJOB

READY
```

Figure V-11. Model Subprogram

```
680CIRCUIT DESCRIPTION
690  RSN54L72   SWITCHING TIME TEST
700ELEMENTS
710F1,C-K-K-K-S-RS-J-J-J-Q-QB-0=MODEL RSN54L72
720ES,0-S=T1
730ERS,0-RS=2.4
740EC,0-C=FGEN(0,3,0,15E-9,185.E-9,15E-9,400.E-9,100,TIME)
750EK,0-K=FGEN(3,3,-15.E-9,15E-9,200.E-9,15E-9,800.E-9,100,TIME)
760EJ,0-J=FGEN(3,3,-15.E-9,15E-9,200.E-9,15E-9,1600.E-9,100,TIME)
770R1,Q-Q1=4300
780C1,Q-Q1=2.E-12
790R2,Q1-0=750
800C2,Q1-0=11.5E-12
810D1,Q-5=MODEL 1N3605 (PERM)
820R5,5-7=800
830EL,0-7=2.4
840R3,QB-Q2=4300
850C3,QB-Q2=2.E-12
860R4,Q2-0=750
870C4,Q2-0=11.5E-12
880D2,QB-6=MODEL 1N3605 (PERM)
890R6,6-7=800
900 FUNCTIONS
910 T1=-50.E-9,0,-50.E-9,2.4
920T2F1=
930 0,0
940 10.E-9,10
950 20.E-9,10
960 30.E-9,0
970 200.E-9,0
980 210.E-9,10
990 220.E-9,10
1000 230.E-9,0
1010 280.E-9,0
1020 290.E-9,10
1030 300.E-9,10
1040 310.E-9.0
1050 650.E-9,0
1060 660.E-9,10
1070 670.E-9,10
1080 680.E-9,0
1090 1000.E-9,0
1100 1010E-9,100
1110 1020E-9,100
1120 1030.E-9,0
1130OUTPUTS
1140EC,EJ,EK,PLOT
1150VC2,VC4,IR5,IR6,PLOT
1160XSTPSZ,PLOT
1170RUNCONTROLS
1180START TIME=-100.E-9
1190MAXIMUM PRINT POINTS = 1000
1200COMPUTER TIME LIMIT = 5.5
1210STOP TIME=1200.E-9
1220END
```

Figure V-12. Test Circuit - Computer Description

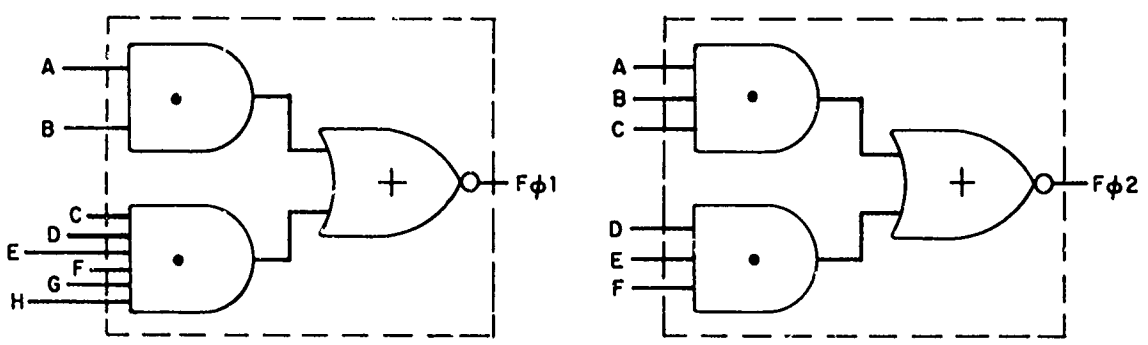
2. MODEL 2

Although this first model performed satisfactorily, a second model was developed. There were two reasons for developing this second model. First, the existing model appeared to be too large and complex. Second, when the first model was used as an integral part of the shift-register circuit model (which in essence is four J-K flip-flop circuits connected in cascade), the resultant device model was too large to have practical application

The computer model that has been developed to duplicate observed performance is shown in Figure V-13. The model description is shown in Figure V-14 and the subprogram which establishes the logic output signal levels and delay characteristics is in Figure V-15.

The signal input impedances JS, JRS, JCK, J1, J2, J3, JK1, JK2 and JK3 are represented as zero valued current sources. In SCEPTRE, this implies that the input signal terminals S, RS, CK, J1, J2, J3, K1, J2 and K3 have infinite impedance (although the gates have measurable and varying impedance values which depend upon the applied signal level). This, as a first order approximation, will provide reasonably accurate results. For greater accuracy, the current sources should be modeled as "tabled" functions of current versus applied voltage in SCEPTRE. This method will provide a realistic device input impedance representation.

As indicated on Figure V-13, and described on Figure V-14, the voltages associated with dependent sources E1 and E2 are determined by the functions FØ1 and FØ2. The functions are an implementation of the logic as indicated on the following sketches.



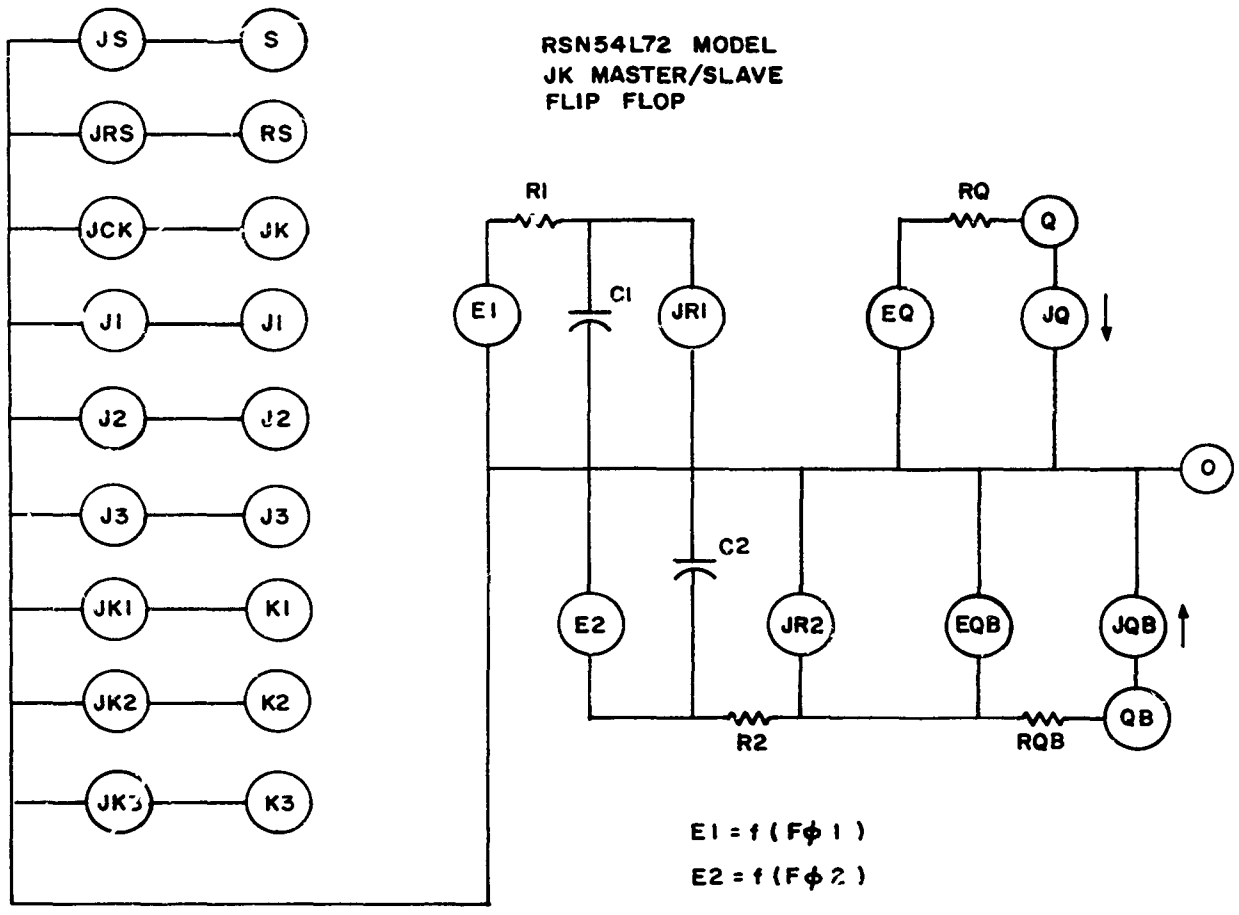


Figure V-13. Computer Model #2

```
      MODEL RSN54L72 (S-RS-CK-J1-J2-J3-K1-K2-K3-Q-QH-GND)
      ELEMENTS
JS,S-GND=0.
JRS,RS-GND=0.
JCK,CK-GND=0.
J1,J1-GND=0.
J2,J2-GND=0.
J3,J3-GND=0.
JK1,K1-GND=0.
JK2,K2-GND=0.
JK3,K3-GND=0.
F1,GND-A=P02
R1,A-B=100.
C1,B-GND=FCAP(E1,VC1)
JK1,B-GND=Q1(TABLE 1(VC1),F1)
FQ,GND-C=X1(VJR1)
RQ,C-Q=100.
JQ,Q-GND=0.
E2,GND-D=P04
R2,D-E=100.
C2,E-GND=FCAP(E2,VC2)
JK2,E-GND = Q1(TABLE 1(VC2),P1)
FQR,GND-F=X2(VJR2)
RQR,F-QH=100.
JQR,QH-GND=0.
      DEFINED PARAMETERS
P1=0.
P01=F01(P03,VJRS,VJ1,VJ2,VJ3,VJQR,VJRS,VJCK)
P02=F02(VJQS,P01,VJS,VJQR,VJS,VJCK)
P03=F01(P01,VJS,VJK1,VJK2,VJK3,VJQ,VJS,VJCK)
P04=F02(VJQ,P03,VJRS,VJQ,VJRS,VJCK)
      FUNCTIONS
Q1(A,B) = (A*B)
TABLE 1 = 0.,-2.,  1.,-1.,  2.,0.,  3.,2.
TABLE 2 = 0.,0., 5000.E-9,0.
      OUTPUTS
E1,E2,VJQ,VJQR,PLOT
```

Figure V-14. Computer Description - Model #2

```
A132T 02  10-12-71   14.204

      1        *FG1
      2                FUNCTION F01(A,B,C,D,E,F,G,H)
      3        *       SUBPROGRAM FOR JK FLIP FLOP
      4        *       WAM 9-21-71
      5        ***********************************************************
      6                X=1.5
      7                NPART1=1
      8                IF(A.GE.X.AND.B.GE.X) NPART1=2
      9                NPART2=1
     10                IF(C.GE.X.AND.D.GE.X.AND.E.GE.X) NPART2=2
     11                NPART3=1
     12                IF(F.GE.X.AND.G.GE.X.AND.H.GE.X) NPART3=2
     13                NPART4=1
     14                IF(NPART2.EQ.2.AND.NPART3.EQ.2) NPART4=2
     15                F01=0.1
     16                IF(NPART1.EQ.1.AND.NPART4.EQ.1) F01=3.0
     17                RETURN
     18                ENTRY F02(A,B,C,D,E,F)
     19                X=1.5
     20                F01=0.1
     21                NPART1=1
     22                IF(A.GE.X.AND.B.GE.X.AND.C.GE.X) NPART1=2
     23                NPART2=1
     24                IF(D.GE.X.AND.E.GE.X.AND.F.GE.X) NPART2=2
     25                IF(NPART1.EQ.1.AND.NPART2.EQ.1) F01=3.0
     26                RETURN
     27                ENTRY FCAP(A,B)
     28                F01 = 600.E-12
     29                IF(A  GE. B) F01 = 475.E-12
     30                RETURN
     31                END

      23541 WORDS OF MEMORY USED BY THIS COMPILATION
```

Figure V-15. Model Subprogram

These complex relationships are entered into the model description as functions, thereby allowing the use of the simple model shown in Figure V-13. This figure schematically presents how the functions are included in the model, while Figure V-14 indicates the method for inclusion in a SCEPTRE listing.

The functions FØ1 and FØ2 are connected to form the master and slave gate respectively as shown in Figure V-2. Defined parameters PØ1 and PØ3 are the output signals of the master gates, while defined parameters PØ2 and PØ4 are the output signals of the slave gates. The output signals from the gates are saved as defined parameters to avoid confusion if multiple J-K flip-flops are called for under "circuit description", as well as for use in the latching function. The logic levels are 1 for signals greater than or equal to 1.5 volts and 0 for signals less than 1.5 volts.

The RSN54L72 triggers on the negative edge of the clock pulse. The model senses the level of the clock signal and transfers input information in two steps. As the clock signal rises above 1.5 volts, the signals at the inputs are transferred to defined parameters PØ1 and PØ3 as determined by the logic in function FØ1. This represents the master section of the flip-flop. When the clock signal falls below 1.5 volts, the defined parameters PØ1 and PØ3 are transferred to defined parameters PØ2 and PØ4 as determined by the logic in function FØ2. This represents the slave section of the flip-flop. Thus the signals enter the master section during a high clock and are transferred to the slave section during a low clock which occurs during a high-to-low transition of the clock (negative edge).

Although the device manufacturer indicates (Table V-2) that the switching delay times for either positive or negative going output signals will be no greater than 150 nanoseconds, laboratory test measurements on many units indicate not only that both delays are shorter than this worst case value, but that they are different from each other. Therefore, the delay times t_{pd1} and t_{pd0} are established in the model by the time constant R1 - C1 and R2 - C2. These time constants are changed by varying the value of C1 or C3 depending upon whether a logic 1 or 0 is required as an output signal.

The value of C1 and C2 is determined by means of subprogram FCAP. Thus, C1 is set to 600 picofarads unless E1 is greater than, or equal to, VCI (voltage across C1). When this latter condition occurs, C1 assumes the value of 475 picofarads. C2 is determined in a similar manner. Since the output voltages EQ and EQB are equal to the voltage across the capacitors C1 and C2 respectively (JR1 and JR2 are zero valued current sources, required by SCEPTRE for dc circuit evaluation condition, and are in parallel with C1 and C2 respectively), a relationship between the input signal levels and the output voltages is readily established. JR1 and JR2 are also used as a source of gamma radiation injection in the model, when required. The FORTRAN flow charts associated with these two functions as well as the radiation response are shown in Appendix V-A.

The output impedances of the device (RQ and RQB) are fixed at 100 ohms. Although this value is not an accurate impedance representation for all voltage and load conditions, it provides first order accuracy of output signal level. To duplicate actual impedance variations, the value of resistors RQ and RQB would be made variable and a function of the load voltage and currents.

The zero valued current sources, JQ and JQB, are dummy elements to permit monitoring the device output signal under varying conditions.

The model listing as described to the computer is shown in Figure V-14. A comparison between this figure and Figure V-10 indicates the greater simplification achieved in the model description size. The former requires 56 entries and three subprograms to describe its behavior; the latter, 35 statements and 1 subprogram. The subprogram which established the E1 and E2 signal levels, as well as the capacitance value for the delay characteristics, is shown in Figure V-15.

B. MODEL VERIFICATION

The test circuit used earlier, and shown in Figure V-16, was described to the computer. The topological description for the SCEPTRE circuit analysis program to demonstrate the performance of the preset and clear functions is shown in Figure V-17. The results of the computer analysis of the circuit are shown in Figures V-18 through V-22. Figure V-18 shows the clock pulse. Figures V-19 and V-20 indicate the SET and RESET input signals. Figure V-21 and V-22 show the circuit response to these input signals; Figure V-21 shows the Q output and Figure V-22 the $\overline{Q}$ output. It is evident that from the results that the preset and clear are independent of the clock and override the J and K inputs.

The topological description for the SCEPTRE circuit analysis program to verify the J and K input control is shown in Figure V-23. The inputs are shown in Figures V-24 through V-26; clock in Figure V-24, J in Figure V-25, and K in Figure V-26. Figures V-27 and V-28 indicate the circuit response to these signals and represent the outputs Q and $\overline{Q}$ respectively. It is evident that the flip-flop model is triggering on the negative slope of the clock and in accordance with the truth table.

The model rise and fall times were verified as shown in Figures V-29 through V-31. The manufacturer defines delay time, t_{pd1}, as the delay between the clock signal reaching 1.5 volts and the Q signal rising to 1.5 volts and the delay time, t_{pd0}, as the delay between the clocking falling to 1.5 volts and the Q signal falling to 1.5 volts. The same definition holds for the Q signal. The results are shown in Table V-3, and compare favorably with the manufacturer's data in Table V-2.

C. RADIATION EFFECTS

1. GAMMA RADIATION

Exposing the device to a nuclear radiation environment may affect normal performance by causing the output signal level to vary. When exposed to pulsed ionizing rays (gamma radiation) at dose rate levels of approximately 3×10^{10} rads (Si)/second, the performance is only temporarily affected. Extensive radiation testing was done by the General Electric Company; the test report with photographic recording of the results is included in Appendix V-B.

If a gamma radiation pulse simulation is caused to occur when the device output is at a 1 level, the output response is momentarily reduced. If a radiation pulse simulation is caused to occur when the device output level is in a 0 state, the output response is momentarily increased.

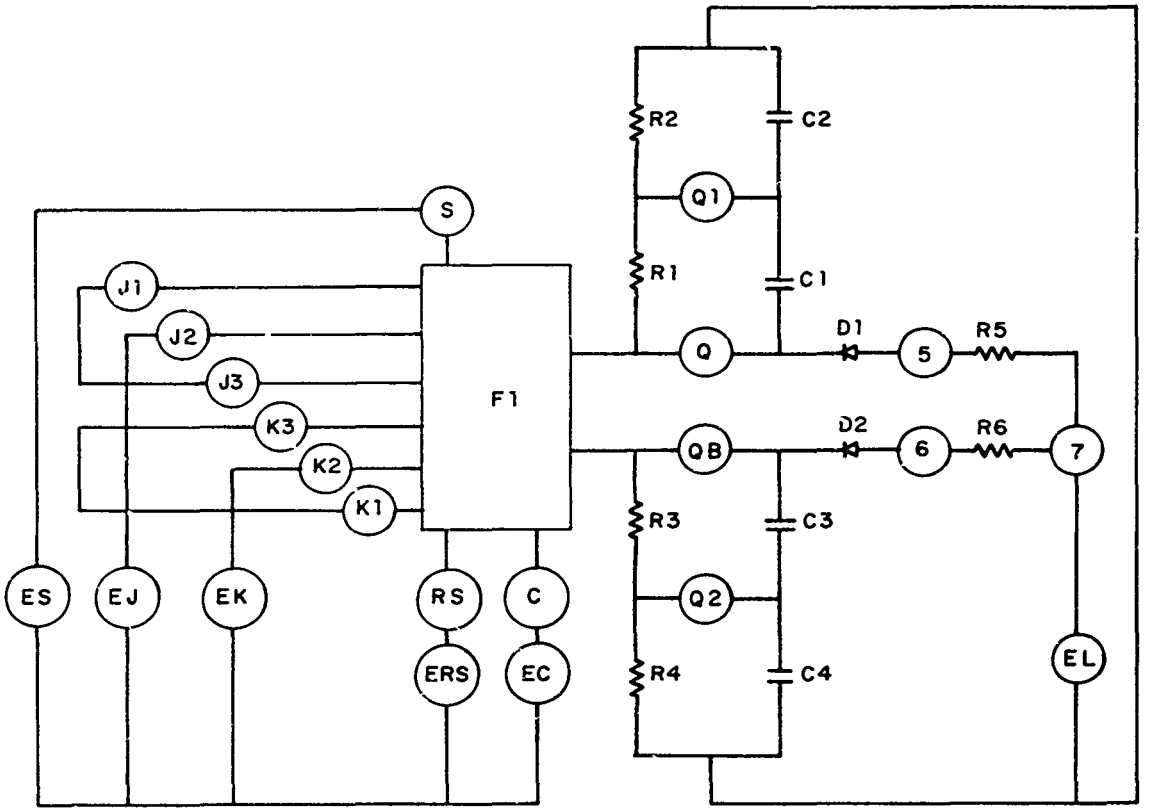


Figure V-16. Test Circuit

```
      RSN54L72 SWITCHING TIME T191
      SAVED UNDER RSN54L72  9-21-71
      ELEMENTS
F1,S-RS-C-J-J-J-K-K-K-Q-QB-Q=MODEL RSN54L72
ES,0-S=T1
ERS,0-RS=T2
EC,0-C=FGEN(0.,3.,0.,15.E-9,200.E-9,15.E-9,400.E-9,100.,TIME)
EJ,0-J=T3
EK,0-K=T4
R1,Q-Q1=4300.
C1,Q-Q1=2.E-12
R2,Q1-0=750.
C2,Q1-0=11.5E-12
D1,Q-5=MODEL 1N3605 (PERM)
R5,5-7=800.
EL,0-7=2.4
R3,QB-Q2=4300.
C3,QB-Q2=2.E-12
R4,Q2-0=750.
C4,Q2-0=11.5E-12
D2,QB-6=MODEL 1N3605 (PERM)
R6,6-7=900.
      FUNCTIONS
T1=0.,.1,8.85E-7,.1,9.E-7,3.,1.5E-6,3.,1.515E-6,.1,1.7E-6,.1,
1.715E-6,3.
T2=0.,3.,1700.E-9,3.,1715.E-9,.1,2800.E-9,.1,2815.E-9,3.
T3=0.,3.,5000.E-9,3.
T4=0.,3.,5000.E-9,3.
      OUTPUTS
EC,EJ,EK,PLOT
ES,ERS,PLOT
      RUN CONTROLS
START TIME =0.
MAXIMUM PRINT POINTS = 200
COMPUTER TIME LIMIT = 5.5
STOP TIME = 5000.E-9
END
```

Figure V-17. Test Circuit Description for SET and RESET Inputs

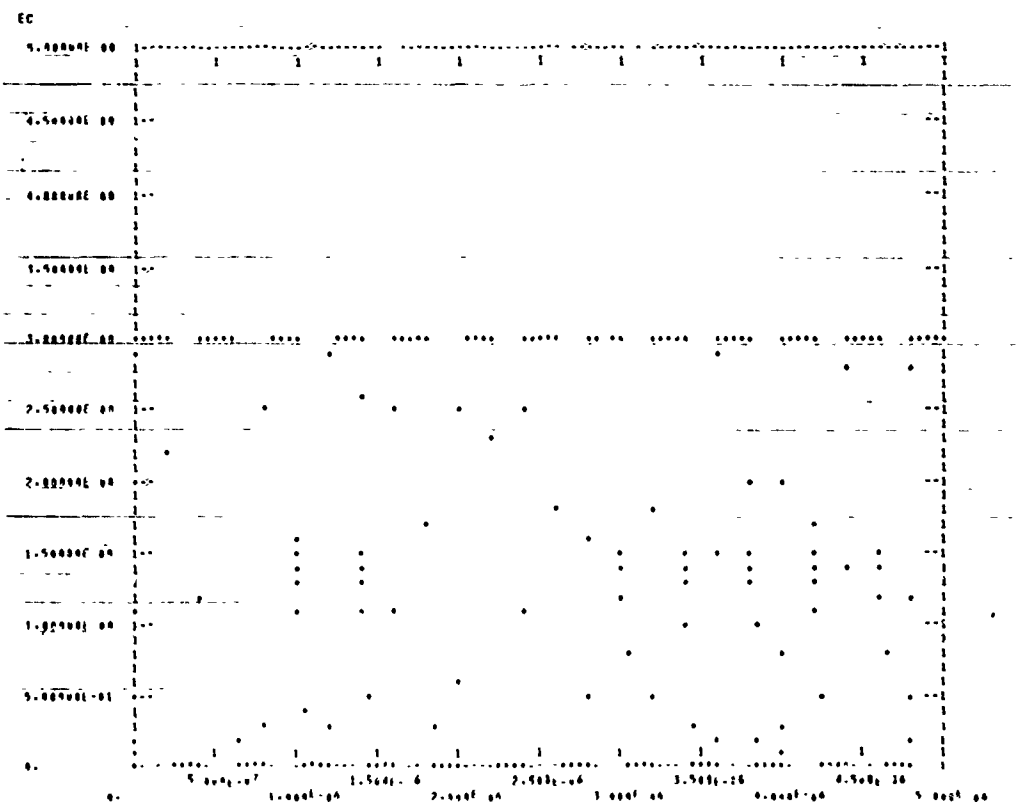


Figure V-18. CLOCK Input Signal

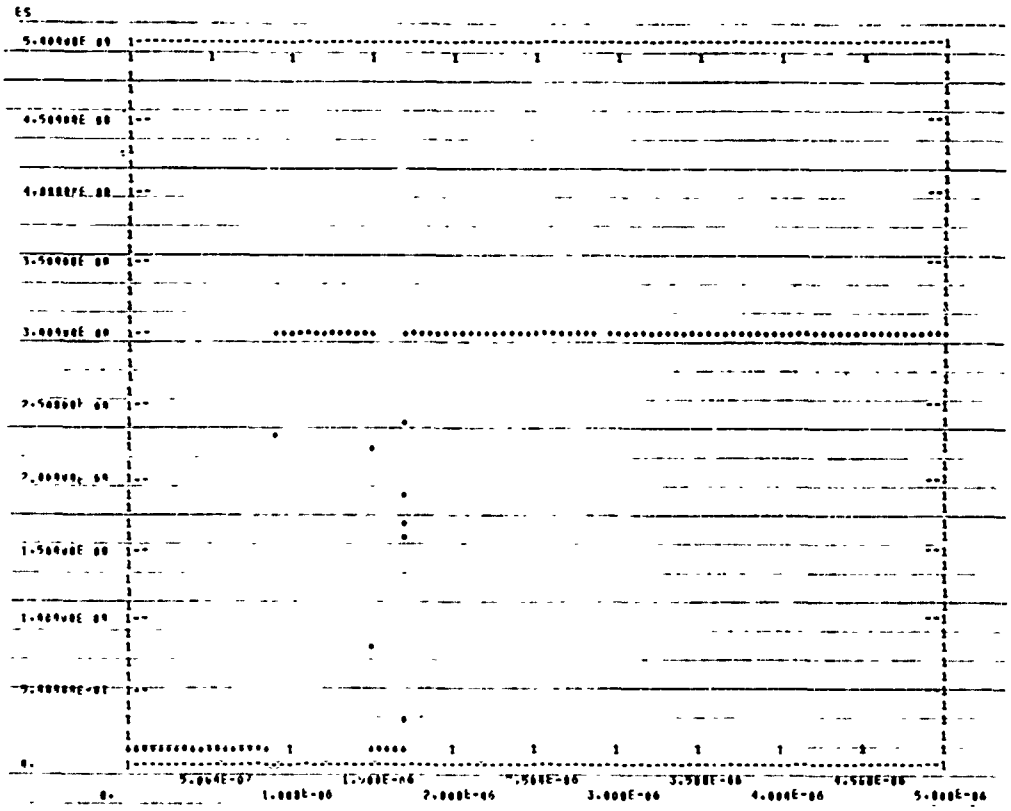


Figure V-19. SET Input Signal

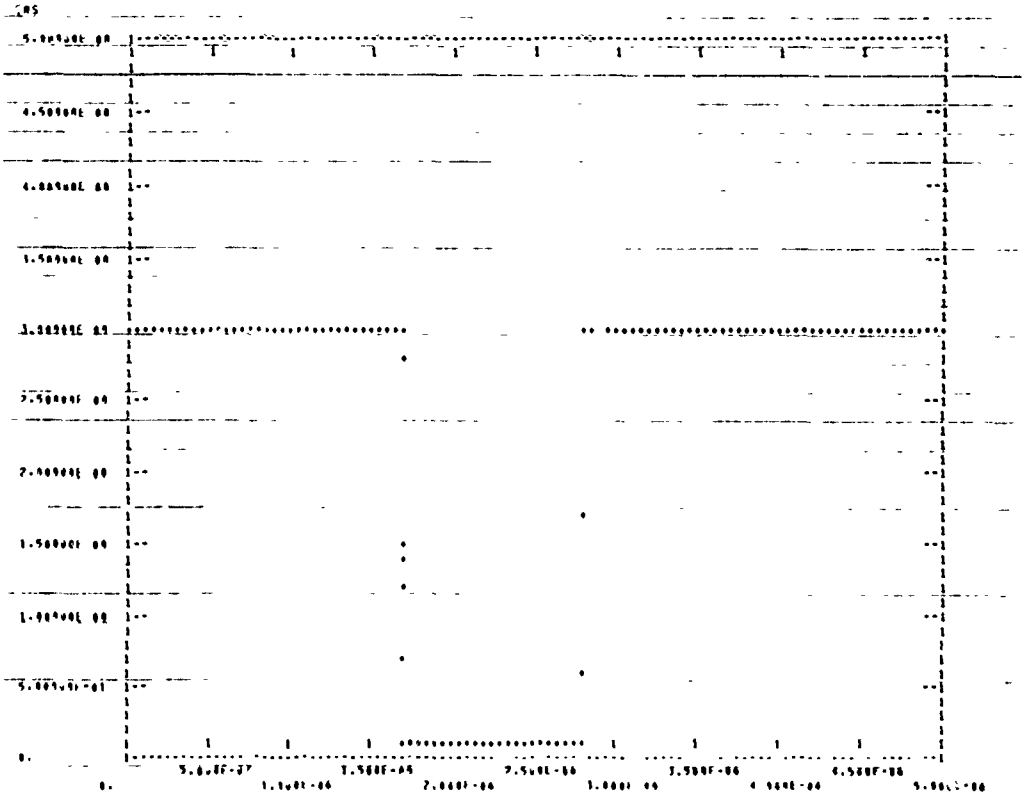


Figure V-20. RESET Input Signal

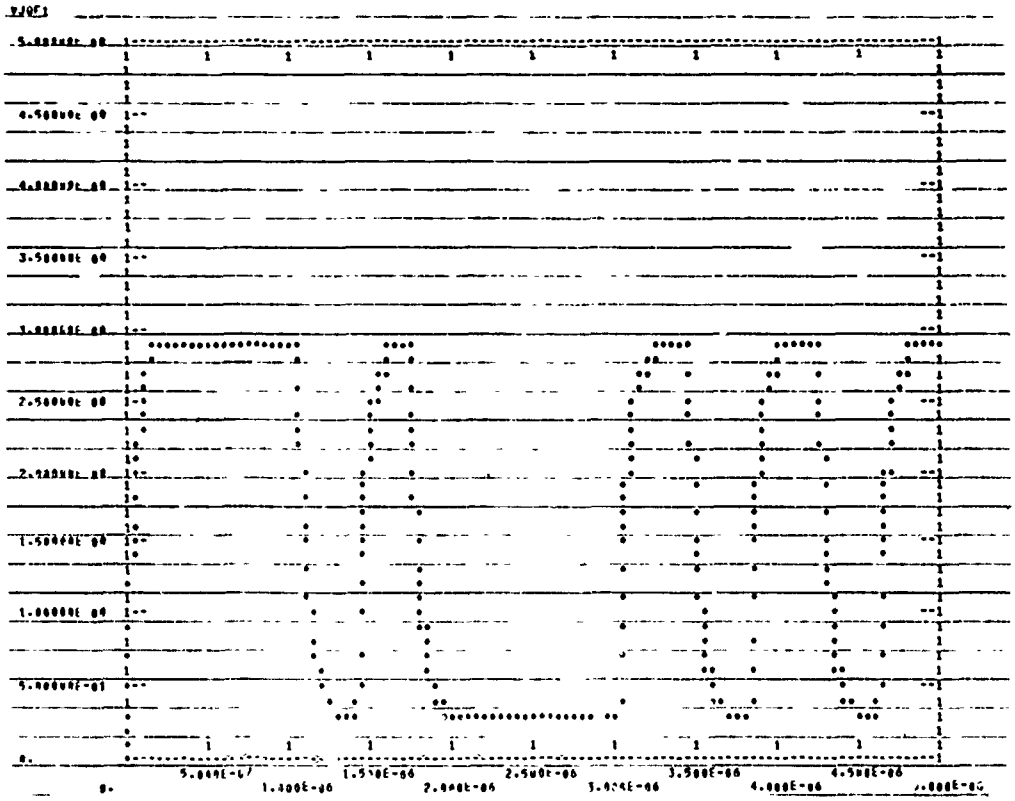


Figure V-21. Q-Response

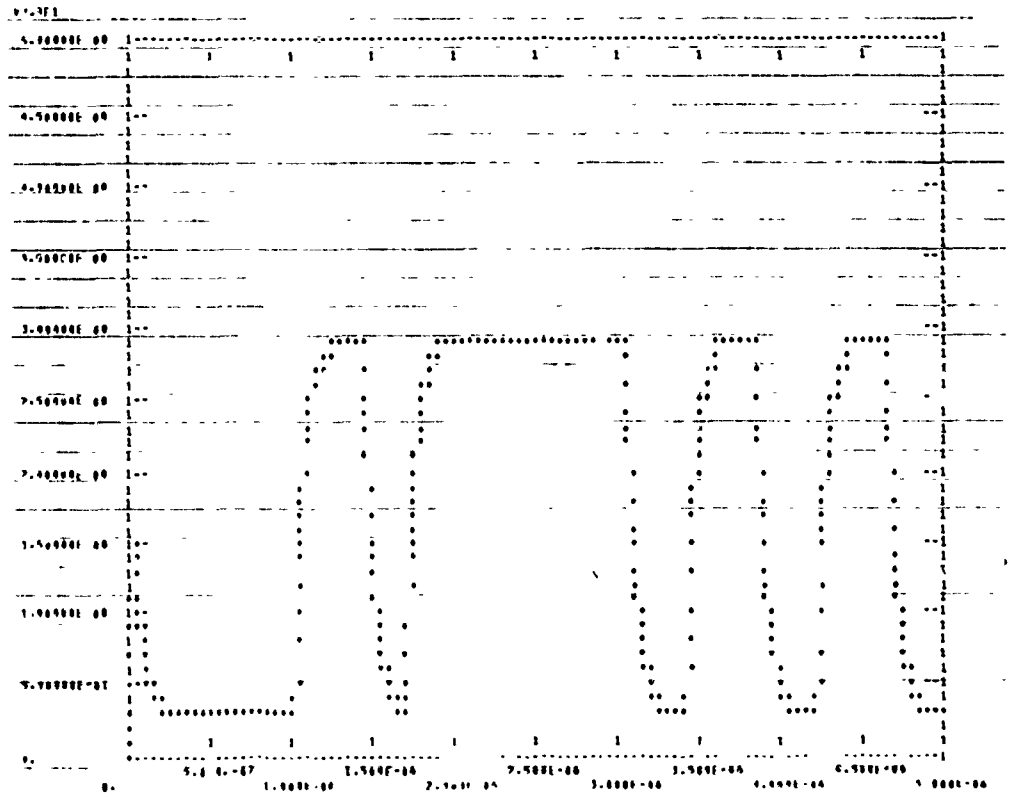


Figure V-22. $\bar{Q}$-Response

```
        RSN54L72 SWITCHING TIME TEST
        SAVED UNDER FILE WANDJ1 9-21-71
        ELEMENTS
F1,S-RS-C-J-J-J-K-K-Q-QB-B=MODEL RSN54L72
ES,B-S=2.4
ERS,B-RS=T1
EC,A-C=FGEN(PC1,PC2,PC3,PC4,PC5,PC6,PC7,PC8,TIME)
EK,A-K=FGEN(PK1,PK2,PK3,PK4,PK5,PK6,PK7,PK8,TIME)
EJ,6-J=FGEN(PJ1,PJ2,PJ3,PJ4,PJ5,PJ6,PJ7,PJ8,TIME)
R1,0-01=4300.
C1,0-01=2.E-12
R2,01-0=750.
C2,01-0=11.5E-12
D1,0-5=MODEL 1N3685 (PERM)
R5,5-7=800.
EL,B-7=2.4
R3,08-02=4300.
C3,08-02=2.E-12
R4,02-0=750.
C4,02-0=11.5E-12
D2,09-6=MODEL 1N3685 (PERM)
R6,6-7=900.
        DEFINED PARAMETERS
PC1=0.
PC2=3.
PC3=0.
        PC4=15.E-9
PC5=370.E-9
        PC6=15.E-9
PC7=900.E-9
PC8=100.
PK1=0.
PK2=3.
        PK3=0.
PK4=15.E-9
PK5=700.E-9
PK6=15.E-9
PK7=1500.E-9
PK8=100.
PJ1=0.
PJ2=3.
PJ3=1500.E-9
PJ4=15.E-9
PJ5=1700.E-9
PJ6=15.E-9
PJ7=3900.E-9
PJ8=100.
        FUNCTIONS
TI=-100.E-9,0.,0.,0.,0.,2.4
        OUTPUTS
EC,EJ,EK,PLOT
        RUN CONTROLS
START TIME = -100.E-9
MAXIMUM PRINT POINTS = 200
COMPUTER TIME LIMIT = 5.5
STOP TIME = 3200.E-9
END

SYSTEM NOW ENTERING SIMULATION
```

Figure V-23. Test Circuit Description for J-K Inputs

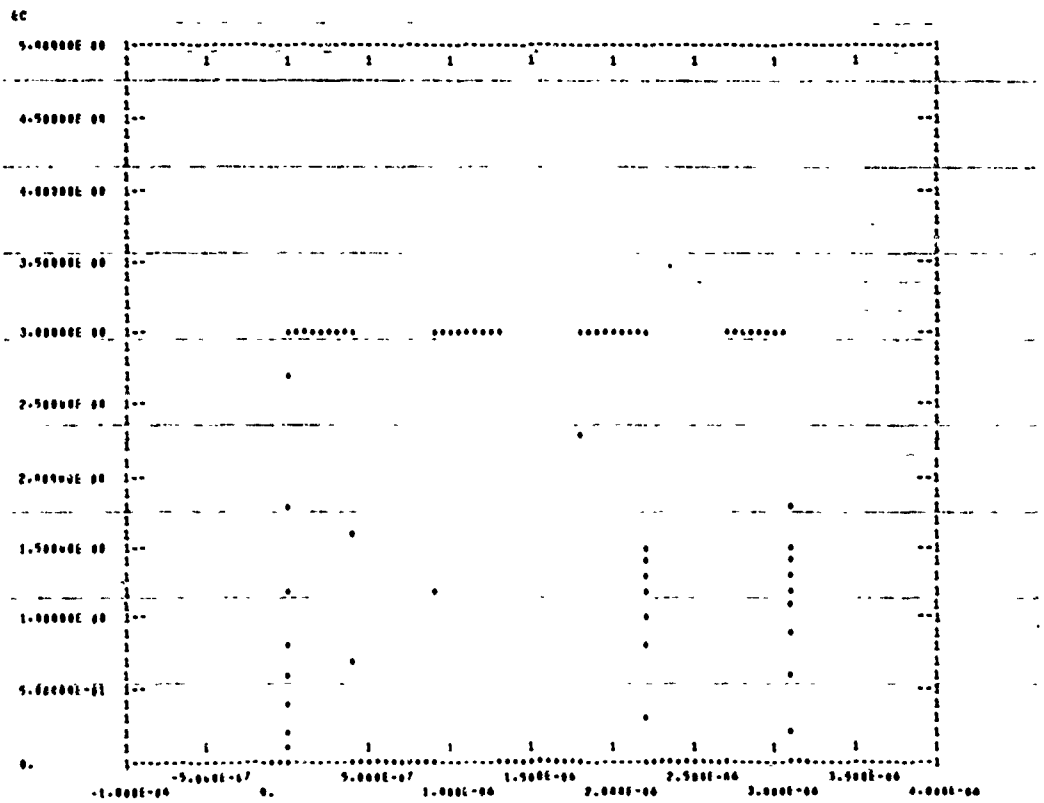


Figure V-24 CLOCK Input Signal

```
        RSN54L72 SWITCHING TIME TEST
        SAVED UNDER FILE NAMEJ1 9-21-71
        ELEMENTS
F1,S-RS-C-J-J-J-K-K-K-Q-QB-Q=MODEL RSN54L72
ES,8-S=2.4
ERS,8-RS=T1
EC,8-C=FGEN(PC1,PC2,PC3,PC4,PC5,PC6,PC7,PC8,TIME)
EK,8-K=FGEN(PK1,PK2,PK3,PK4,PK5,PK6,PK7,PK8,TIME)
EJ,6-J=FGEN(PJ1,PJ2,PJ3,PJ4,PJ5,PJ6,PJ7,PJ8,TIME)
R1,Q-Q1=4300.
C1,Q-Q1=2.E-12
R2,Q1-8=750.
C2,Q1-8=11.5E-12
D1,Q-5=MODEL 1N3685 (PERM)
R5,5-7=800.
EL,8-7=2.4
R3,QB-Q2=4300.
C3,QB-Q2=2.E-12
R4,Q2-8=750.
C4,Q2-8=11.5E-12
D2,QB-6=MODEL 1N3685 (PERM)
R6,6-7=900.
        DEFINED PARAMETERS
PC1=8.
PC2=3.
PC3=8.
        PC4=15.E-9
PC5=370.E-9
        PC6=15.E-9
PC7=900.E-9
PC8=100.
PK1=8.
PK2=3.
        PK3=8.
PK4=15.E-9
PK5=700.E-9
PK6=15.E-9
PK7=1500.E-9
PK8=100.
PJ1=8.
PJ2=3.
PJ3=1500.E-9
PJ4=15.E-9
PJ5=1700.E-9
PJ6=15.E-9
PJ7=3900.E-9
PJ8=100.
        FUNCTIONS
TI=-100.E-9,8.,8.,8.,2.4
        OUTPUTS
EC,FJ,FK,PLOT
        RUN CONTROLS
START TIME = -100.E-9
MAXIMUM PRINT POINTS = 200
COMPUTER TIME LIMIT = 5.5
STOP TIME = 3200.E-9
END

SYSTEM NOW ENTERING SIMULATION
```

Figure V-23. Test Circuit Description for J-K Inputs

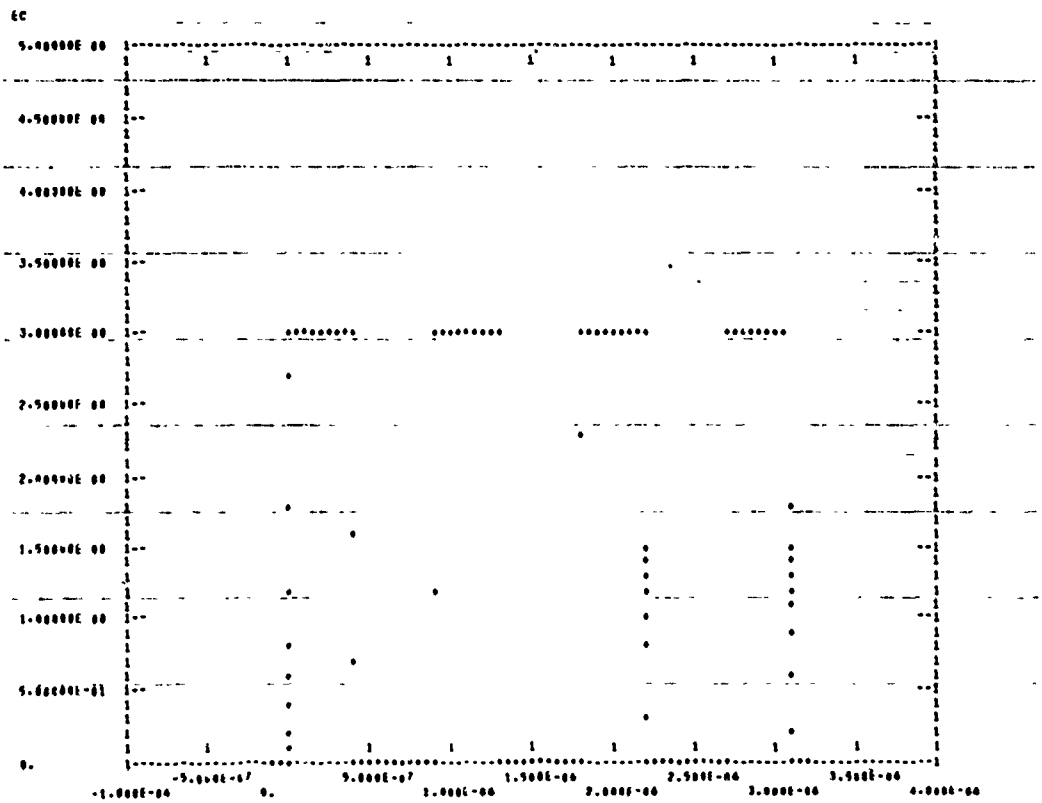


Figure V-24 CLOCK Input Signal

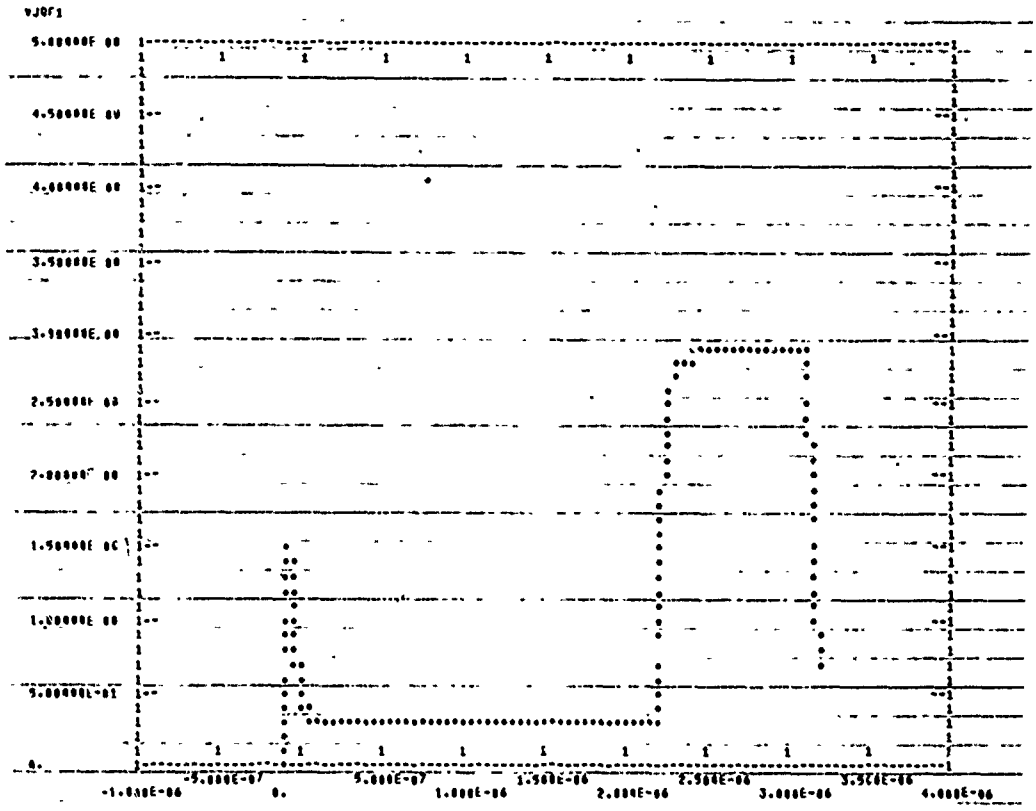


Figure V-27. Q-Response

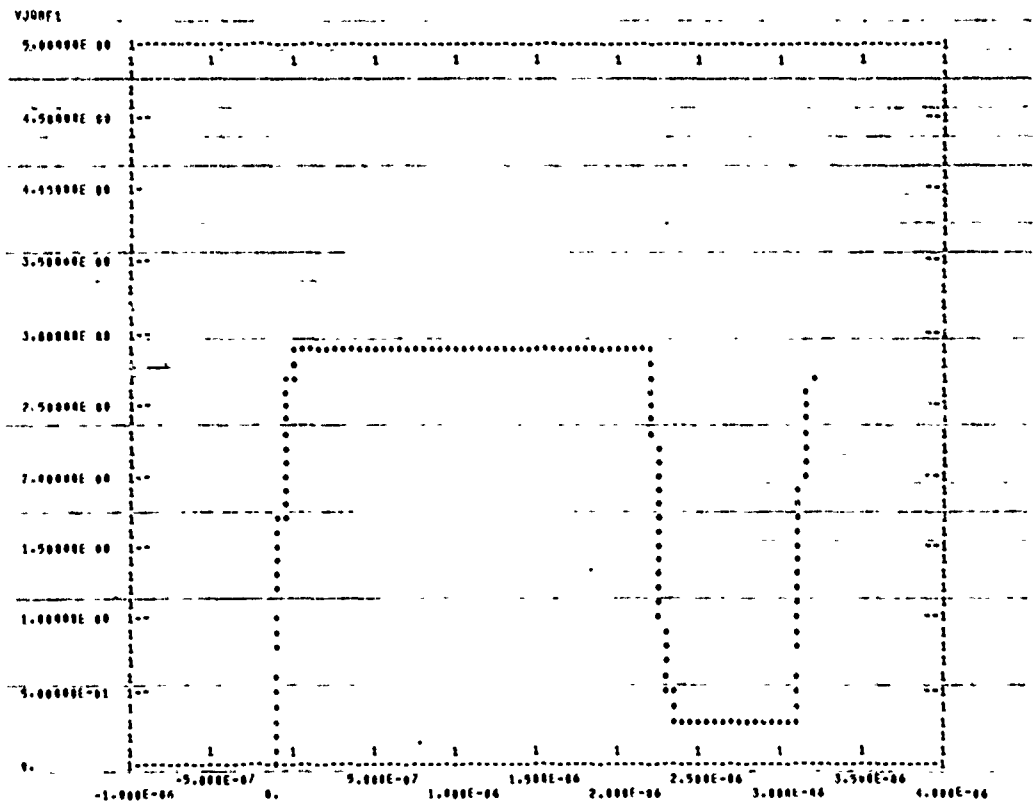


Figure V-28. $\overline{Q}$-Response

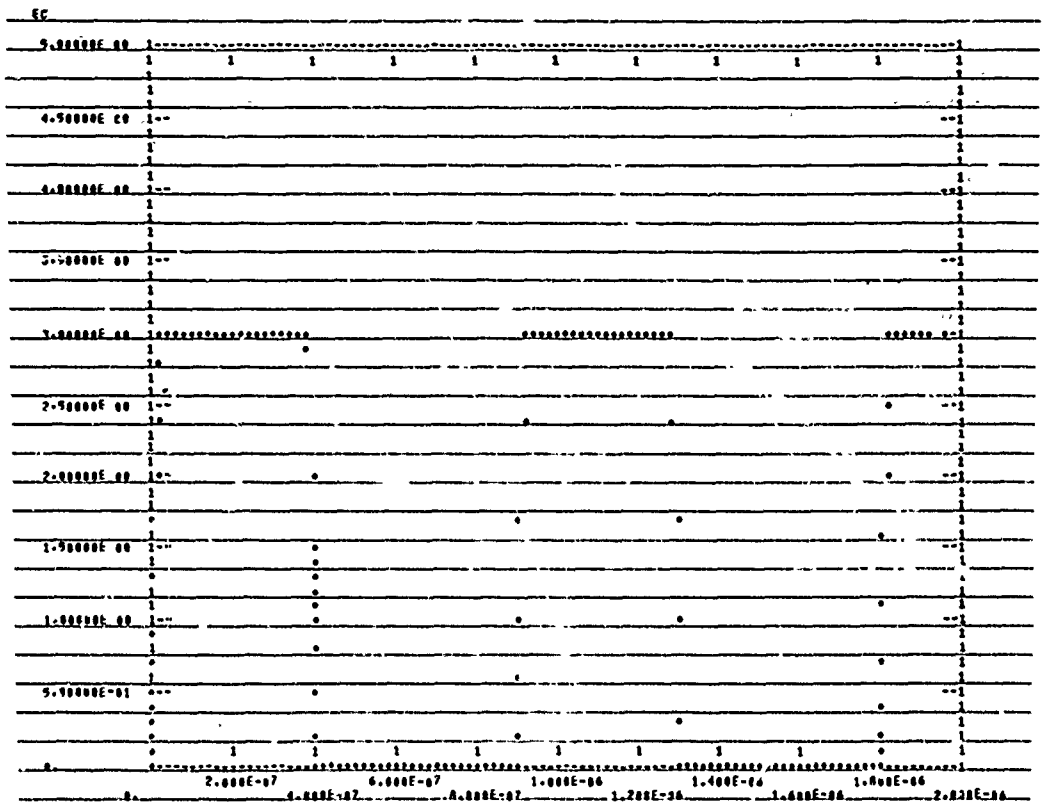


Figure V-29. CLOCK Signal

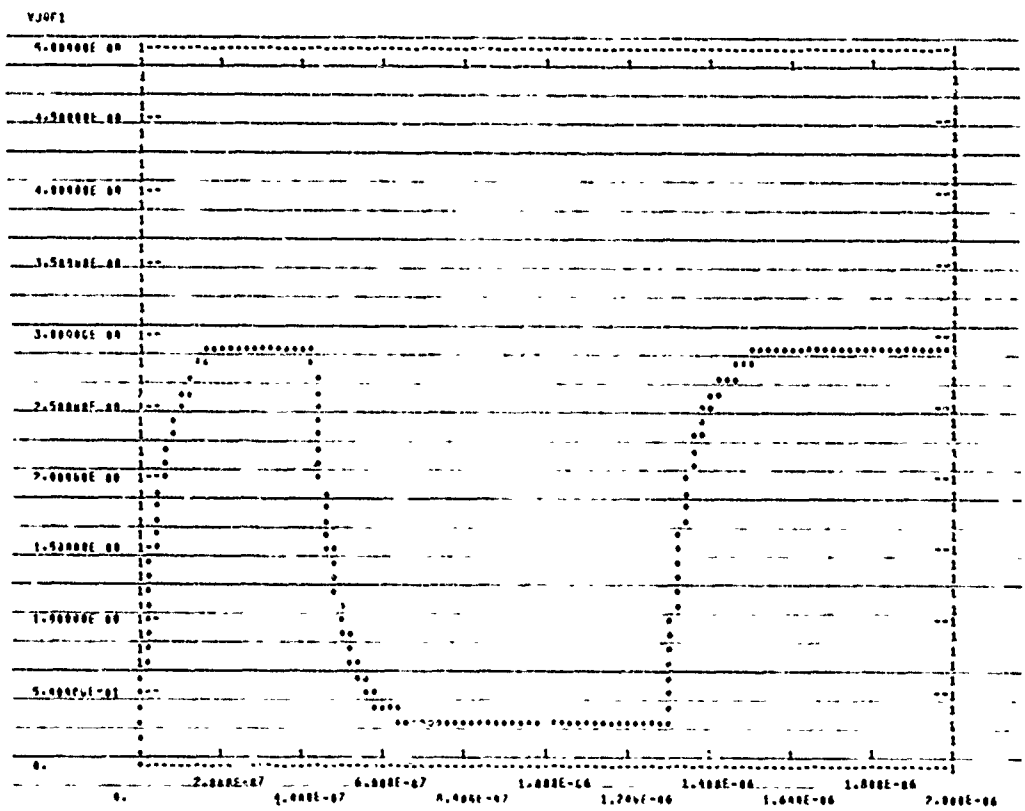


Figure V-30. Q-Response

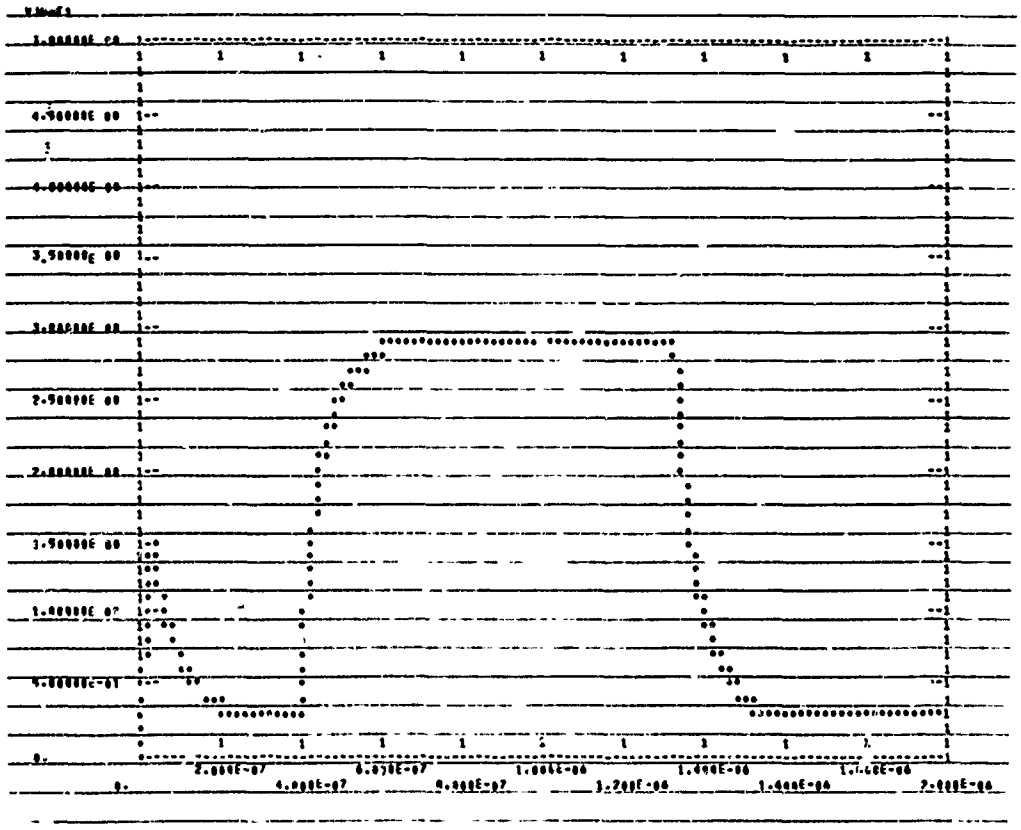


Figure V-31. $\overline{Q}$-Response

TABLE V-3.

DELAY TIMES

OUTPUT	DELAY TIME	
	t_{pd0}	t_{pd1}
Q	76 sec	21 sec
$\overline{Q}$	76 sec	31 sec

The method for simulating the pulsed ionizing gamma radiation induced transient effects is to change the value of P1 in Figure V-14. As shown on Figure V-32, P1 is redefined as a signal that is time dependent and represented by Table 2 of this figure. By changing the time entries in Table 2, the radiation simulation is caused to occur whenever desired. In this figure, the transient gamma pulse is caused to occur at 620 nanoseconds which simulates radiation test condition 5, in Appendix V-B.

As seen on Figure V-33, a positive excursion of the Q output is observed to occur at the desired time. For test condition 5, this output is in a 0 state, since both the J and K signals are in a high or 1 condition, and the clock in a 0 state. The second positive excursion of the Q signal, which occurs at 1125 nanoseconds, demonstrates that the model response is the same when the clock is in a 1 state, while the other signals remain constant. This result would normally be expected. Figure V-34 indicates the $\overline{Q}$ output signal behavior for the same conditions. Superimposed on the computer results of both figures are the observed laboratory test results.

For test condition No. 2 (i.e., J in the low state, K in the high state, and the clock in either state), the computer results are shown in Figures V-35 and V-36, for the Q and $\overline{Q}$ output signals respectively. Observed laboratory test results are superimposed on these figures. As was the case in Figures V-33 and V-34, both the low and high state of the clock signal conditions are presented.

Test condition No. 1 computer analysis results are shown in Figures V-37 and V-38. For this test both J and K signals are in the 0 state and therefore the Q is at the 1 level. Again radiation is simulated at times when the clock is in both the low and high states. Figure V-37 shows the Q output and Figure V-38 the $\overline{Q}$ output, for the same condition. Again observed laboratory results are superimposed upon the computer output. Figure V-39 shows the circuit description used by the computer to obtain the above results.

Test condition No. 3 (J signal in the high state, the K signal in the low state, and the clock in both states), produces results that are the same as for test condition No. 1. The results are shown in Figures V-40 and V-41.

These figures demonstrate excellent agreement between the computed results and the laboratory observations.

2. NEUTRON RADIATION

When the device is exposed to neutron radiation conditions, its performance may be degraded either temporarily or permanently. The degree of the degradation as well as the device recovery time, for those conditions which permit recovery, depends upon the exposure level.

Exposure of test circuits of fluence levels of 1.2×10^{14} results in an output level reduction of approximately 0.4 volt, when the signal is at a 1 level. When the output signal is at a 0 level, the voltage is increased by about 0.2 volt. The results were observed by the Air Force Weapons Laboratory when they tested these devices and are reported in Reference 1.* Figure V-42 presents the circuit transfer function

*Ibid. page 16

```
        RSN54L72 SWITCHING TIME TEST
        SAVED UNDER RSN54L72  9-21-71
1PPTEST CONDITION NO.5
        ELEMENTS
F1,S-RS-C-J-J-J-K-K-K-Q-QB-B=MODEL RSN54L72(CHANGE P1=TABLE2)
ES,0-S=2.4
ERS,A-RS=T1
EC,0-C=FOLN(PC1,PC2,PC3,PC4,PC5,PC6,PC7,PC8,TIME)
EK,0-K=2.4
EJ,0-J=2.4
R1,0-01=4300.
C1,0-01=2.E-12
R2,01-A=750.
C2,01-B=11.5E-12
D1,0-5=MODEL 1N3685 (PERM)
R5,5-7=800.
EL,0-7=2.4
R3,QB-02=4300.
C3,QB-02=2.E-12
R4,02-B=750.
C4,02-B=11.5E-12
D2,QB-6=MODEL 1N3685 (PERM)
R6,6-7=900.
        DEFINED PARAMETERS
PC1=0.
PC2=3.
PC3=0.
        PC4=15.E-9
PC5=370.E-9
        PC6=15.E-9
PC7=900.E-9
PC8=100.
PK1=0.
PK2=3.
PK3=0.
PK4=15.E-9
PK5=700.E-9
PK6=15.E-9
PK7=1500.E-9
PK8=100.
PJ1=0.
PJ2=3.
PJ3=1500.E-9
PJ4=15.E-9
PJ5=1700.E-9
PJ6=15.E-9
PJ7=3000.E-9
PJ8=100.
        FUNCTIONS
T1=-100.E-9,0.,0.,0.,0.,2.4
TABLE 2 = 0.,0.
600.E-9,0.
615.E-9,1.
620.E-9,1.5
625.E-9,1.
640.E-9,0.
1115.E-9,0.
1115.E-9,.5
1125.E-9,1.
1135.E-9,.5
```

Figure V-32. Model Description With Gamma Effects

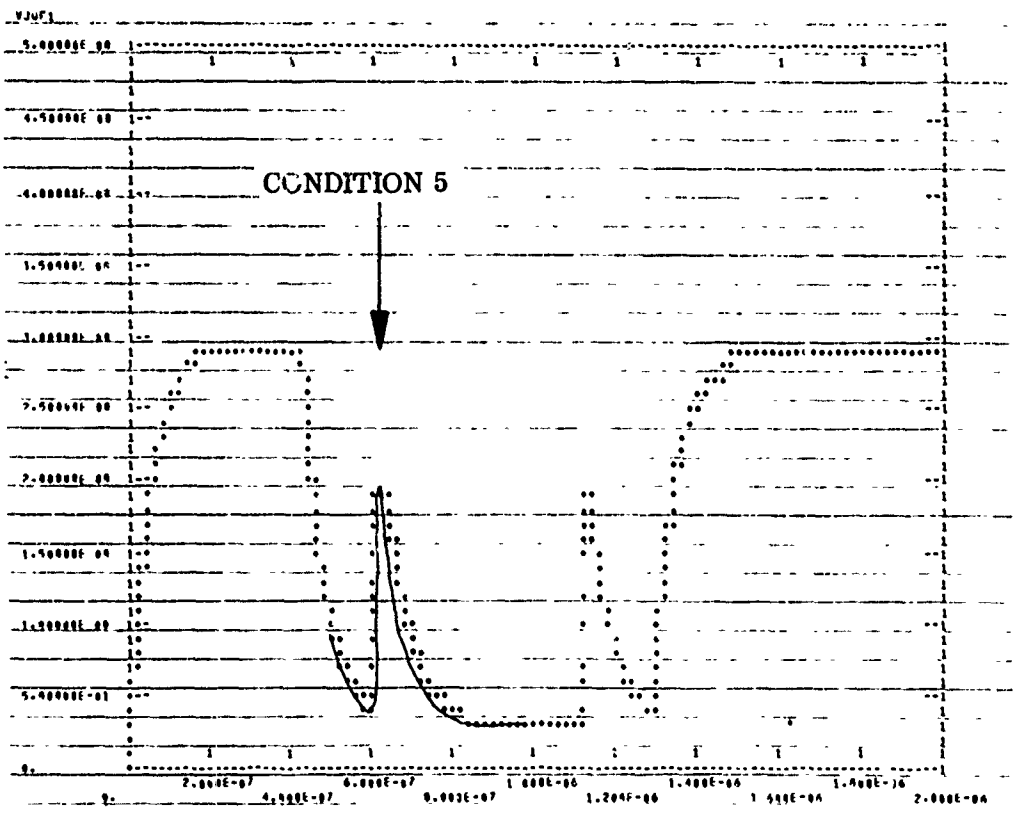


Figure V-33. Q-Response for Condition 5

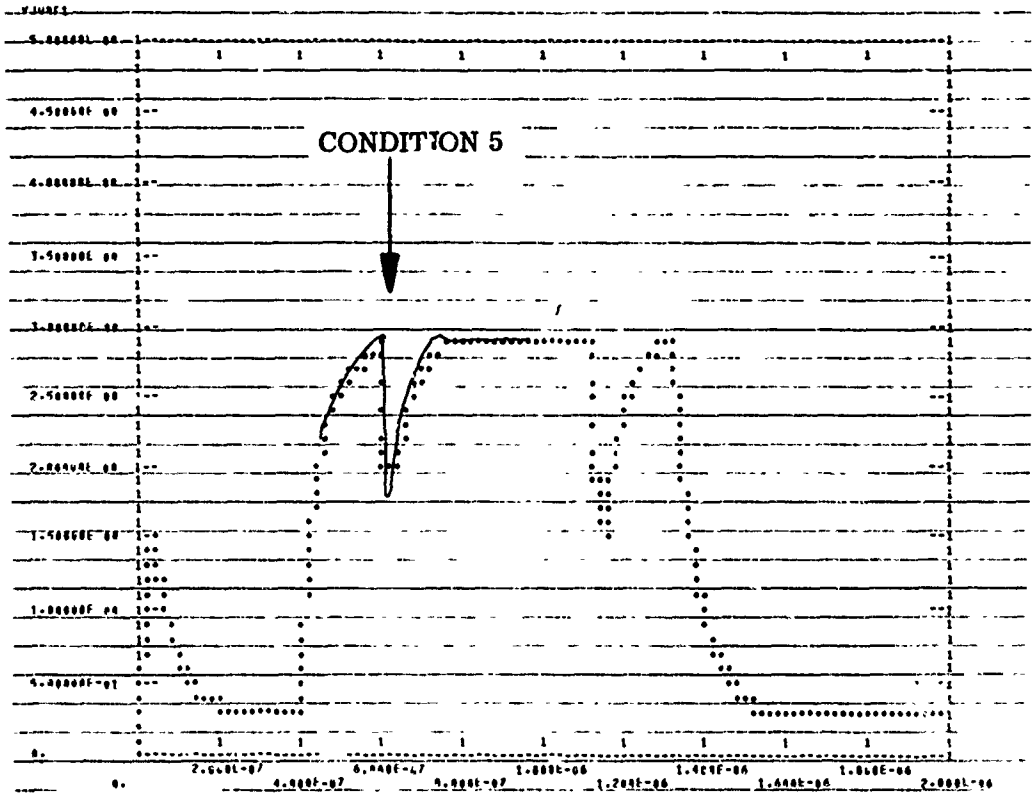


Figure V-34. $\overline{Q}$-Response for Condition 5

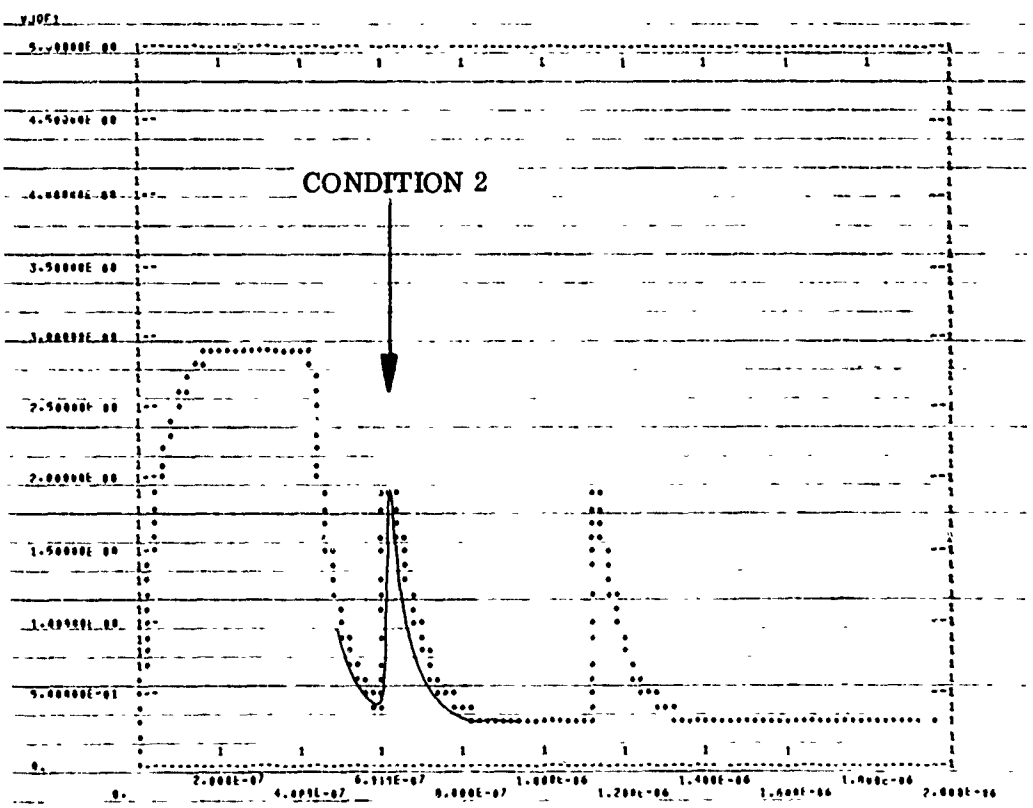


Figure V-35. Q-Response for Condition 2

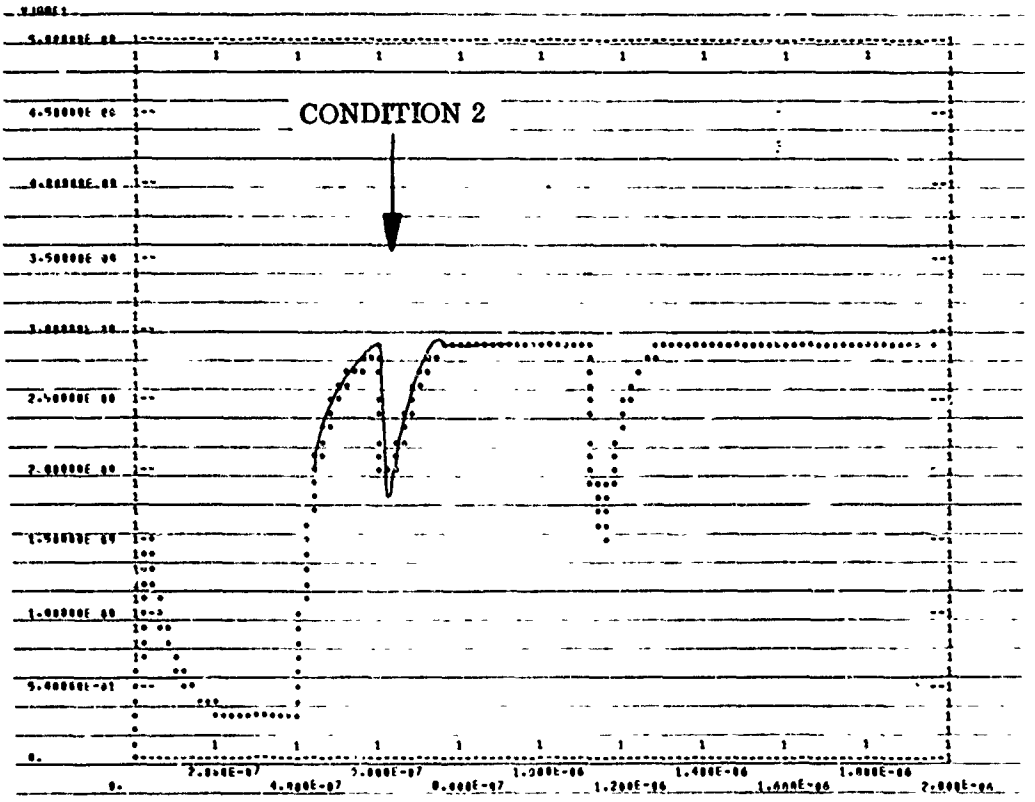


Figure V-36. $\overline{Q}$-Response for Condition 2

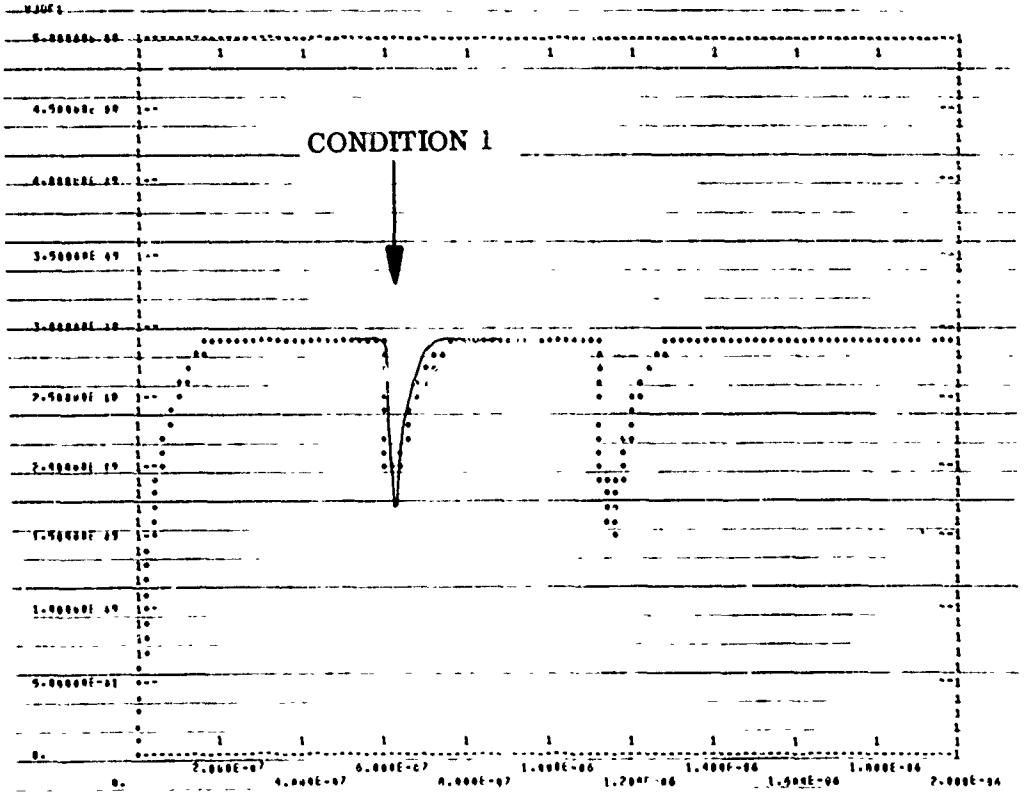


Figure V-37. Q-Response for Condition 1

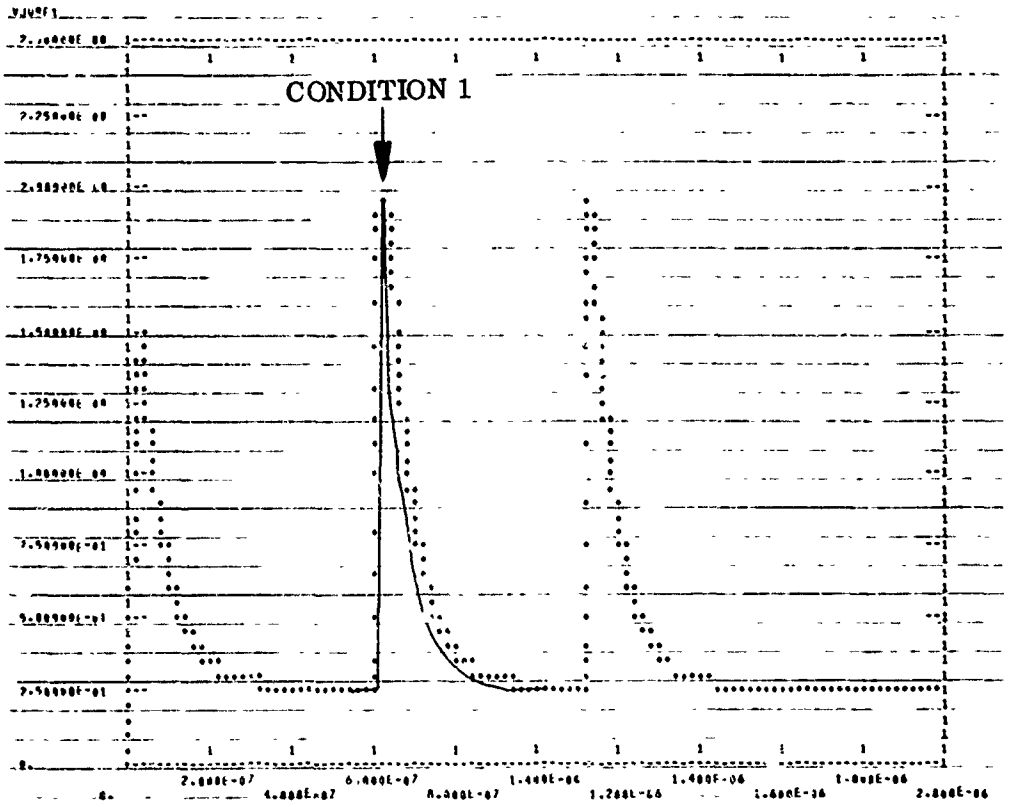


Figure V-38. $\overline{Q}$-Response for Condition 1

```
        RSN54L72 SWITCHING TIME TEST
        SAVED UNDER RSN54L72 9-21-71
 IPP TEST CONDITION NO.1
        ELEMENTS
F1.S-RS-C-J-J-J-K-K-K-O-OB-O=MODEL RSN54L72(CHANGE P1=TABLE2)
FS.0-S=2.4
ERS.0-RS=T1
EC.0-C=FOEN(PC1,PC2,PC3,PC4,PC5,PC6,PC7,PC8,TIME)
EK.0-K=0.
EJ.0-J=0.
R1.0-01=0300.
C1.0-01=2.E-12
R2.01-0=750.
C2.01-0=11.5E-12
D1.0-5=MODEL 1N3605 (PERM)
R5.5-7=800.
EL.0-7=2.4
R3.08-02=4300.
C3.08-02=2.E-12
R4.02-0=750.
C4.02-0=11.5E-12
D2.08-6=MODEL 1N3605 (PERM)
R6.6-7=900.
        DEFINED PARAMETERS
PC1=0.
PC2=3.
PC3=0.
        PC4=15.E-9
PC5=1700.E-9
        PC6=15.E-9
PC7=900.E-9
PC8=100.
PK1=0.
PK2=3.
PK3=0.
PK4=15.E-9
PK5=700.E-9
PK6=15.E-9
PK7=1500.E-9
PK8=100.
PJ1=0.
PJ2=3.
PJ3=1500.E-9
PJ4=15.E-9
PJ5=1700.E-9
PJ6=15.E-9
PJ7=3000.E-9
PJ8=100.
        FUNCTIONS
T1=-100.E-9,0.,0.,0.,0.,2.4
TABLE 2 = 0.,0.
600.E-9,0.
615.E-9,1.
620.E-9,1.5
625.E-9,1.
640.E-9,0.
1115.E-9,0.
1115.E-9,.5
1125.E-9,1.
1135.E-9,.5
```

Figure V-39. Gamma - Test Circuit Description

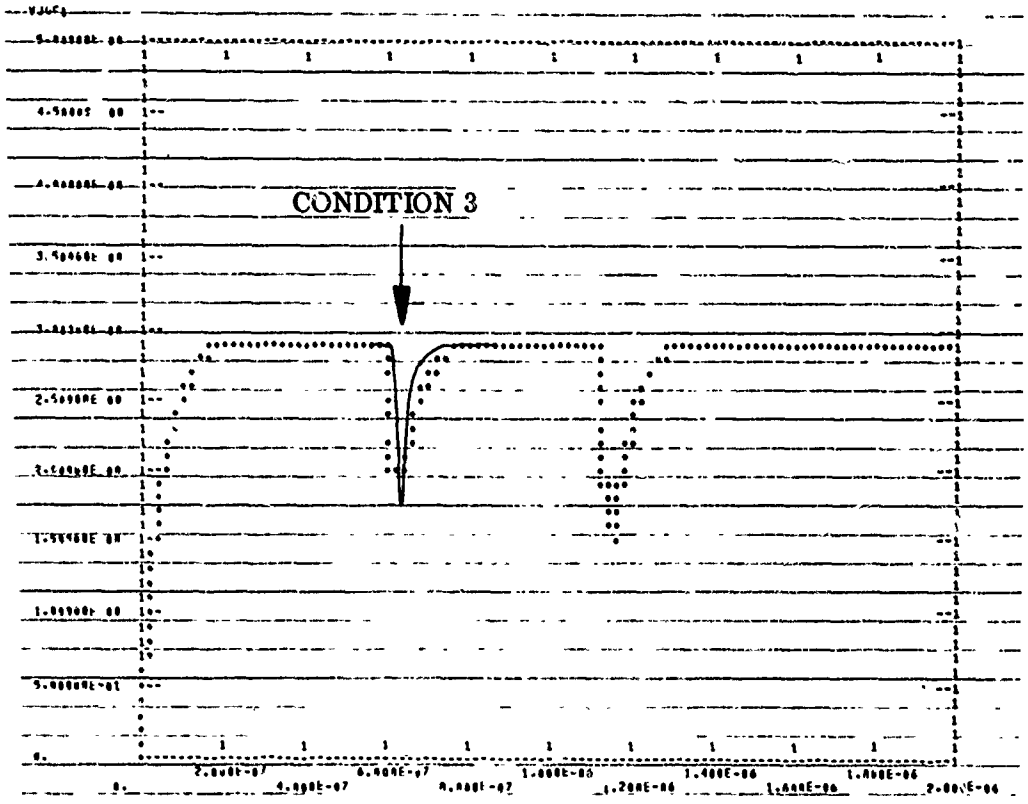


Figure V-40. Q-Response for Condition 3

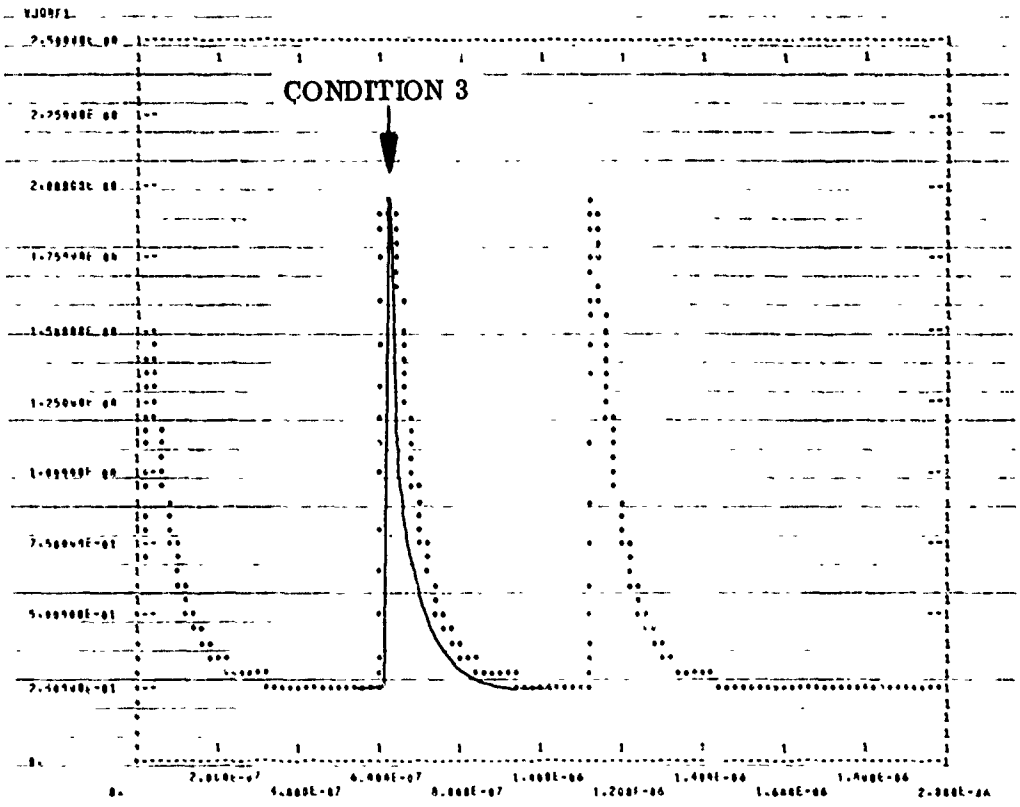


Figure V-41. $\overline{Q}$-Response for Condition 3

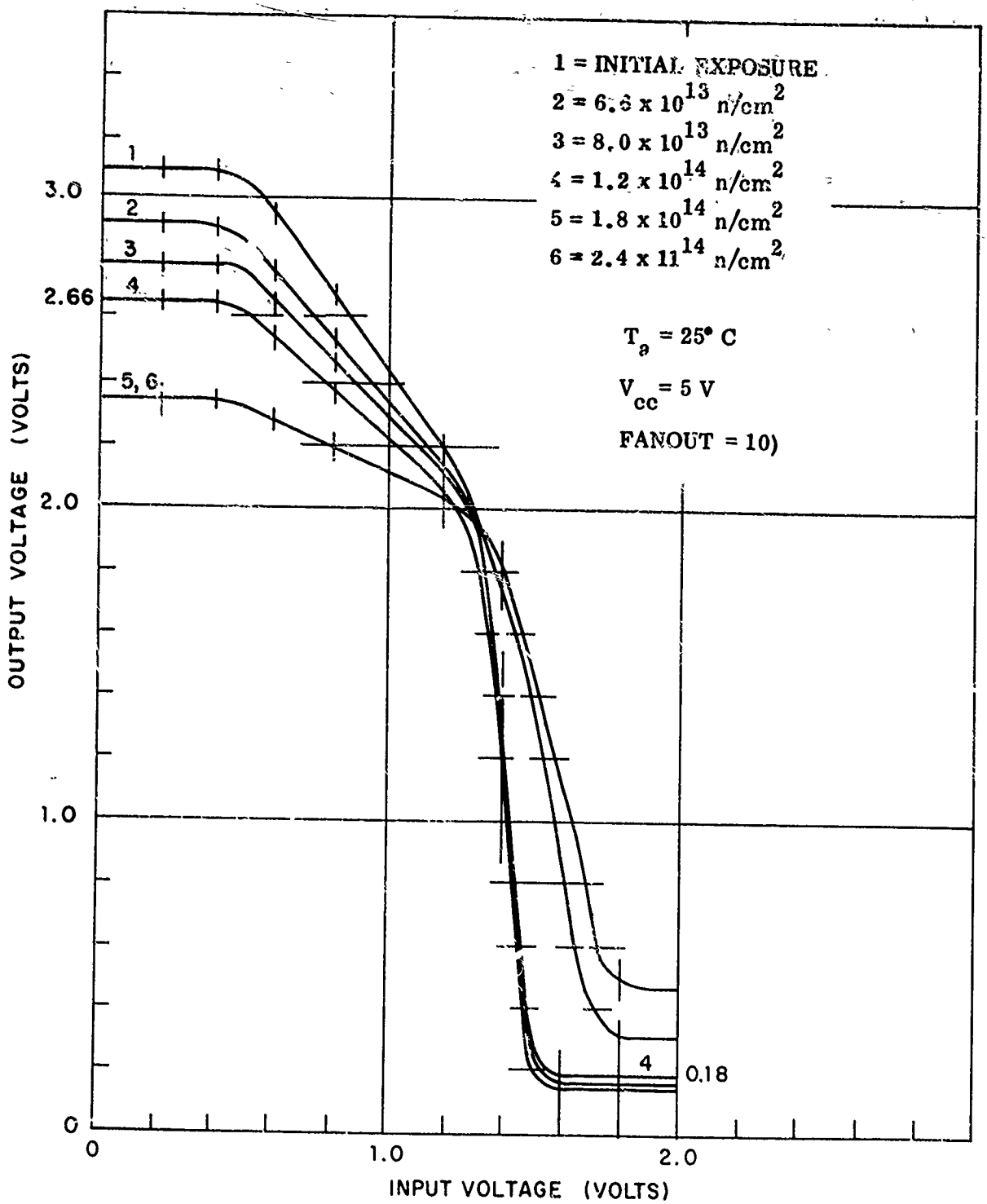


Figure V-42. Neutron Radiation - Circuit Transfer Function

degradation observed during these tests, for various fluence levels. For curve 4, which represents test condition 4, the output signal level drops from about 3.1 volts to approximately 2.7 volts and rises from about 0.16 volt to approximately 0.18 volt.

The method for incorporating this response change into the model is shown in Figure V-43. The value of the output voltages EQ and EQB are changed from a simple dependency on the voltage across sources JR1 and JR2 respectively, to a dependency upon both the voltage across the source and the fluence level. To permit both the increase and decrease to be effective, a subroutine, FNVT, was incorporated into the model description as P4.

The subroutine FNVT is shown in Figure V-44; the circuit computer description to produce the analysis in Figure V-45. The results of the effects subroutine FNVT, identified as P4F1, are shown in Figure V-46. The circuit analysis results for Q and $\overline{Q}$ are shown in Figures V-47 and V-48, respectively.

An examination of these last three figures results in two major conclusions:

1) When the time relationship between the values assumed by P4F1 and the 1 and 0 levels of the Q output are compared, it is seen that P4 equals +0.2 volt when the Q signal is in its low state, and -0.4 volt when the Q signal is in the high state.

2) When Figures V-47 and V-48 are compared with Figures V-30 and V-31 respectively, it is seen that the 1 level voltage has been reduced from 2.9 volts to 2.5 volts and that the 0 level voltage has been increased from 0.4 volt to 0.6 volt. This is the expected response to neutron environment exposure.

```
MODEL NSK54L72 (S-RS-CK-J1-J2-J3-K1-K2-K3-Q-QB-GND)
ELEMENTS
JS,S-GND=0.
JRS,RS-GND=0.
JCK,CK-GND=0.
J1,J1-GND=0.
J2,J2-GND=0.
J3,J3-GND=0.
JK1,K1-GND=0.
JK2,K2-GND=0.
JK3,K3-GND=0.
E1,GND-A=P02
R1,A-B=100.
C1,B-GND=FCAP(E1,VC1)
JR1,B-GND=Q1(TABLE 1(VC1),P1)
EQ,GND-C=X1(VJR1+P4)
RQ,C-Q=100.
JQ,Q-GND=0.
E2,GND-D=P04
R2,D-E=100.
C2,E-GND=FCAP(E2,VC2)
JR2,E-GND = Q1(TABLE 1(VC2),P1)
EQB,GND-F=X2(VJR2-P4)
RQB,F-QB=100.
JQB,QB-GND=0.
DEFINED PARAMETERS
P4=FNVT(VC1,3.4,0.2)
P1=0.
P01=FO1(P03,VJRS,VJ1,VJ2,VJ3,VJQB,VJRS,VJCK)
P02=FO2(VJQB,P01,VJS,VJQB,VJS,VJCK)
P03=FO1(P02,VJS,VJK1,VJK2,VJK3,VJQ,VJS,VJCK)
P04=FO2(VJQ,P03,VJRS,VJQ,VJRS,VJCK)
FUNCTIONS
Q1(A,B) = (A*B)
TABLE 1 = 0.,-2.,  1.,-1.,  2.,0.,  3.,2.
OUTPUTS
E1,E2,VJQ,VJQB,PLOT
P4,PLOT
```

Figure V-43. Computer Model Description With Neutron Effects

```
0057T 02  11-30-71   12.205

      *FO1
            FUNCTION FO1(A,B,C,D,E,F,G,H)
      *     SUBPROGRAM FOR JK FLIP FLOP
      *     WAM 9-21-71
      ***********************************************************
            X=1.5
            NPART1=1
            IF(A.GE.X.AND.B.GE.X) NPART1=2
            NPART2=1
            IF(C.GE.X.AND.D.GE.X.AND.E.GE.X) NPART2=2
            NPART3=1
            IF(F.GE.X.AND.G.GE.X.AND.H.GE.X) NPART3=2
            NPART4=1
            IF(NPART2.EQ.2.AND.NPART3.EQ.2) NPART4=2
            FO1=0.1
            IF(NPART1.EQ.1.AND.NPART4.EQ.1) FO1=3.0
            RETURN
            ENTRY FO2(A,B,C,D,E,F)
            X=1.5
            FO1=0.1
            NPART1=1
            IF(A.GE.X.AND.B.GE.X.AND.C.GE.X) NPART1=2
            NPART2=1
            IF(D.GE.X.AND.E.GE.X.AND.F.GE.X) NPART2=2
            IF(NPART1.EQ.1.AND.NPART2.EQ.1) FO1=3.0
            RETURN
            ENTRY FCAP(A,B)
            FO1 = 600.E-12
            IF(A .GE. B) FO1 = 475.E-12
            RETURN
            ENTRY FNVT(A,B,C)
      C      SUBPROGRAM FOR NEUTRON BEHAVIOR
             IF(A.LE.2.) GO TO 10
             X=B
            FO1=X
             GO TO 100
      10    Y=C
            FO1=Y
      100   RETURN
            END

      23545 WORDS OF MEMORY USED BY THIS COMPILATION
```

Figure V-44. Model Subprogram With Neutron Effects

```
        RSN54L72 SWITCHING TIME TEST
        SAVED UNDER RSN54L72  9-21-71
        ELEMENTS
F1,S-RS-C-J-J-J-K-K-Q-QR-B=MODEL RSN54L72
FS,A-S=2.4
FRS,A-RS=11
EC,0-C=FGEN(PC1,PC2,PC3,PC4,PC5,PC6,PC7,PC8,TIME)
EK,0-K=FGEN(PK1,PK2,PK3,PK4,PK5,PK6,PK7,PK8,TIME)
EJ,0-J=FGEN(PJ1,PJ2,PJ3,PJ4,PJ5,PJ6,PJ7,PJ8,TIME)
R1,0-Q1=4300.
C1,0-Q1=2.E-12
R2,Q1-A=750.
C2,Q1-A=11.5E-12
D1,0-5=MODEL 1N3600 (PERM)
R5,5-7=800.
FL,0-7=2.4
R3,QR-Q2=4300.
C3,QR-Q2=2.E-12
R4,Q2-A=750.
C4,Q2-A=11.5E-12
D2,QR-6=MODEL 1N3685 (PERM)
R6,6-7=900.
        DEFINED PARAMETERS
PC1=0.
PC2=3.
PC3=0.
        PC4=15.E-9
PC5=370.E-9
        PC6=15.E-9
PC7=900.E-9
PC8=100.
PK1=0.
PK2=3.
PK3=0.
PK4=15.E-9
PK5=700.E-9
PK6=15.E-9
PK7=1500.E-9
PK8=100.
PJ1=0.
PJ2=3.
PJ3=1500.E-9
PJ4=15.E-9
PJ5=1700.E-9
PJ6=15.E-9
PJ7=3600.E-9
PJ8=100.
        FUNCTIONS
T1=-100.E-9,0.,0.,0.,0.,2.4
        OUTPUTS
EC,EJ,FK,PLOT
        RUN CONTROLS
MAXIMUM PRINT POINTS = 200
COMPUTER TIME LIMIT = 5.5
STOP TIME=3999.E-9
END

SYSTEM NOW ENTERING SIMULATION
```

Figure V-45. Neutron Radiation - Test Circuit Description

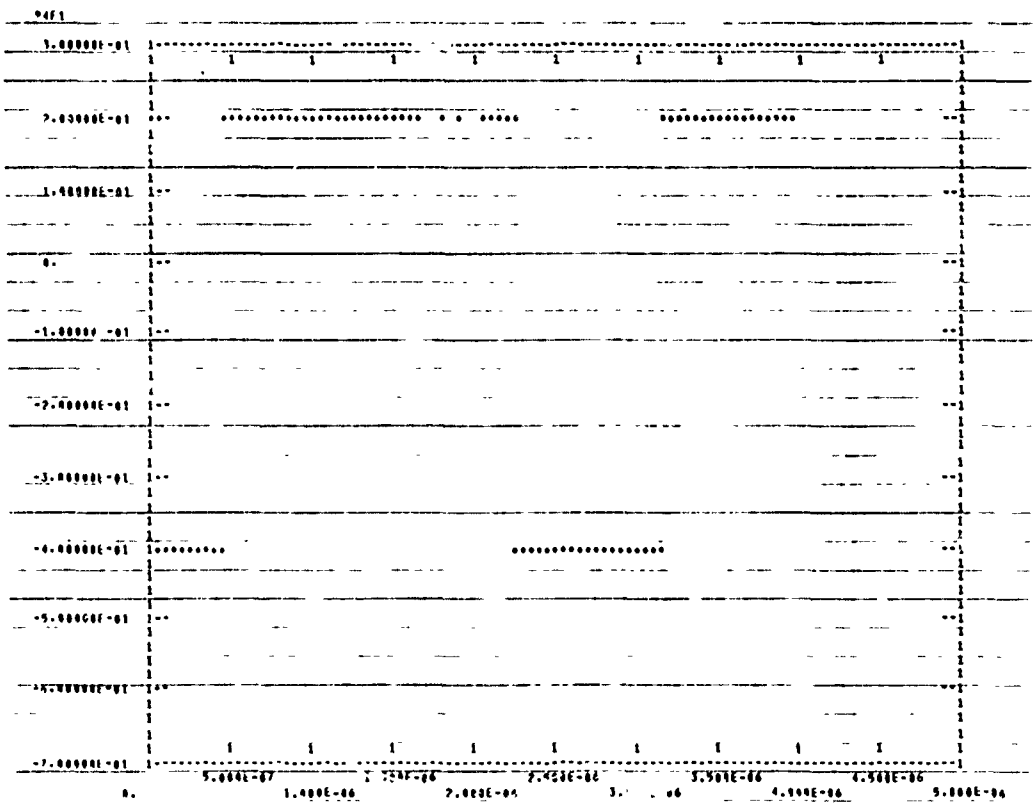


Figure V-46. Output FNVT - Neutron Effects Subroutine

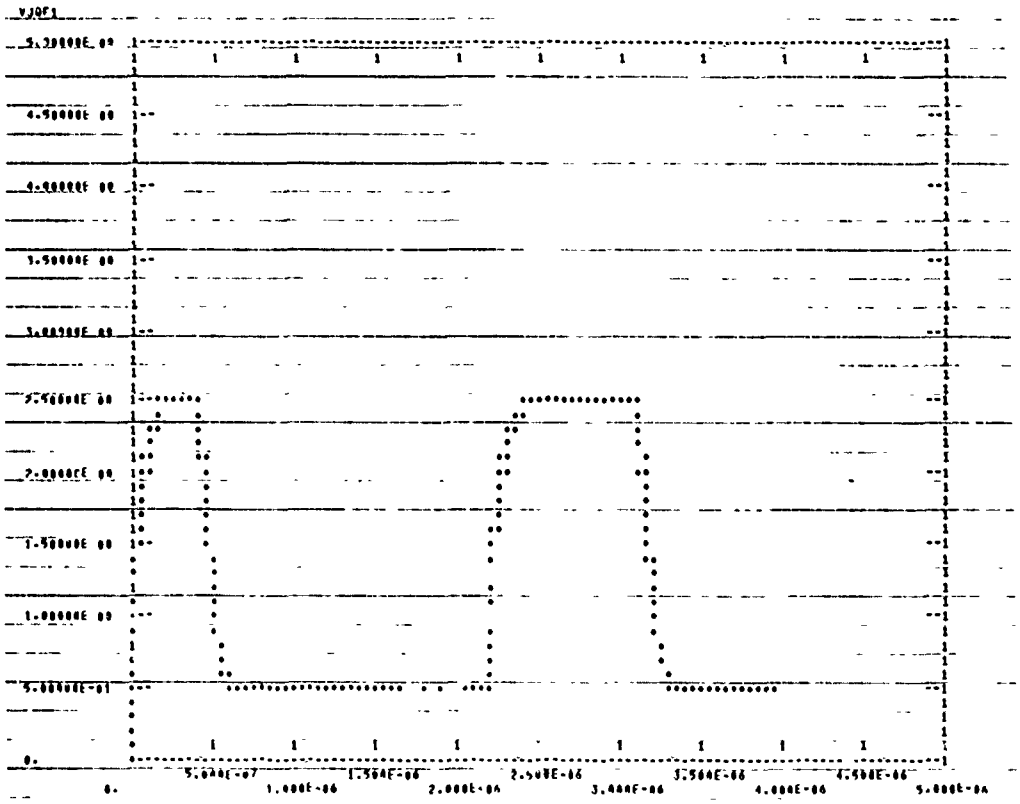


Figure V-47. Q-Response to Neutron Radiation

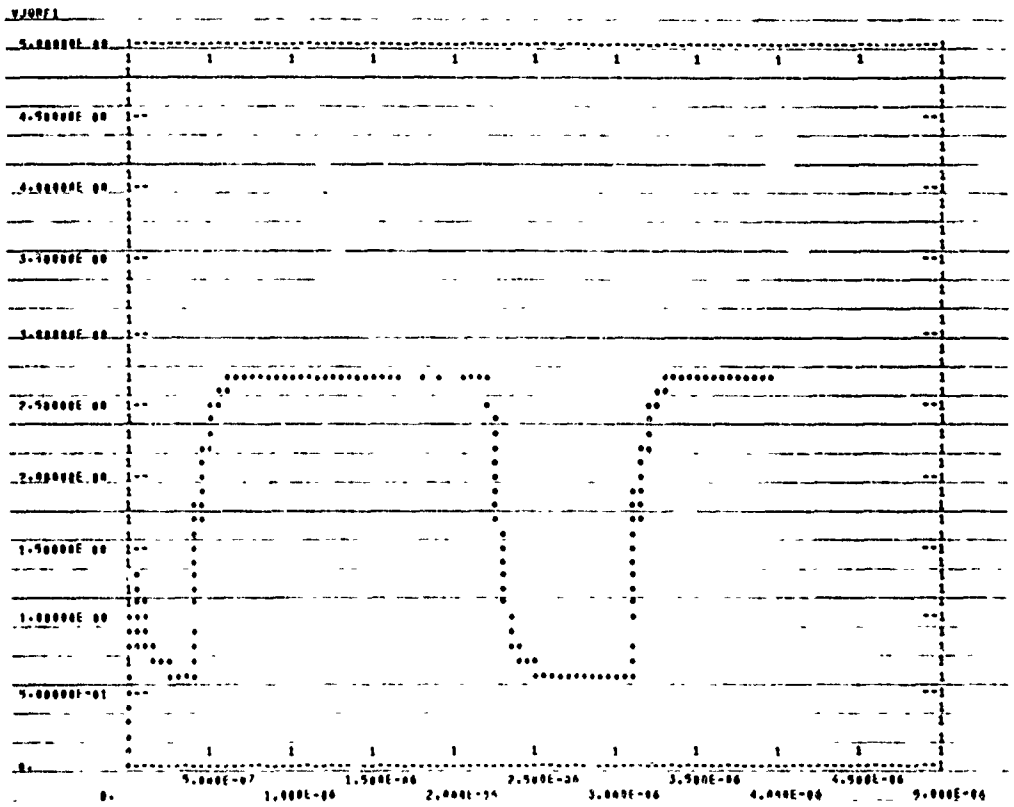


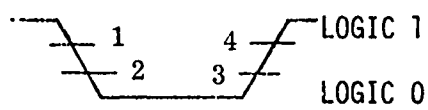
Figure V-48. $\overline{Q}$-Response to Neutron Radiation

SECTION VI

FAIRCHILD 9780 SHIFT REGISTER

The 9780 is a serial-in, parallel-out, synchronous 4 bit shift register. It provides an output (Q_0, Q_1, Q_2 and Q_3) for each of the four stages plus a $\overline{Q}_3$ output at the last stage, an overriding asynchronous master reset, and J-K input configuration. Data entry is synchronous with an input change of state after each low to high transition of the clock. The asynchronous master reset, when activated, overrides all other input conditions and clears the register.

Each stage of the shift register is a J-K, master-slave, flip-flop. Logic information present on the J and K inputs, plus information fed back from the Q and $\overline{Q}$ outputs, sets the master section.



The sequence of operation for the flip-flop is as follows:*

1) With the clock input at a logic 1 level, the master section is isolated from the slave section by transfer gates.

2) As soon as the clock pulse falls to the threshold level, approximately 0.8 volt, logic information present on the J and K inputs is entered into the master section.

3) With the clock at a logic 0 level, the master section is again isolated from the slave. When the clock pulse begins to rise, the input gates to the master section become disabled.

4) As soon as the clock pulse reaches the threshold level, the transfer gates are turned on and the logic information present at the output of the master section is transferred to the slave which controls the output.

*Numbers refer to corresponding numbers on the clock waveform sketch above.

As long as the logic information on the J and K inputs remain stable while the clock is at a logic 0 level, the output will correspond to the truth table when the clock makes a 0 to 1 transition.

The truth table for a stage of the device, as described by the manufacturer, is shown in Table VI-1 (for the condition when the reset signal is at a logic 0 level).

TABLE VI-1.

TRUTH TABLE

t_n		t_{n+1}	
INPUT		OUTPUT	
J	K	Q_0	$\bar{Q}_0$
L	L	Q_{0th}	$\bar{Q}_{0th}$
L	H	L	H
H	L	H	L
H	H	$\bar{Q}_{0th}$	Q_{0th}

t_n = bit time before clock pulse

t_{n+1} = bit time after clock pulse

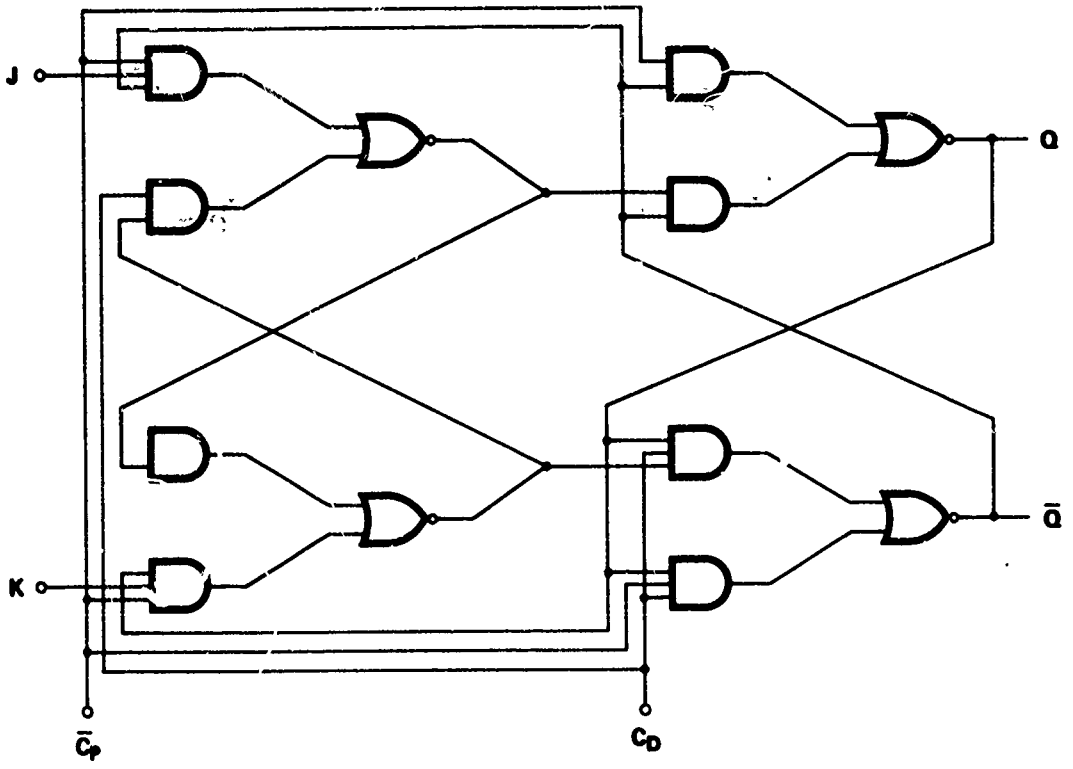
The functional logic representation is shown in Figure VI-1(A) and is represented by eight AND gates and four NOR gates. The schematic diagram of each of the integrated AND and NOR gates is shown in Figure VI-2.

The electrical characteristics of the device as provided by the manufacturer are shown in Table VI-2.

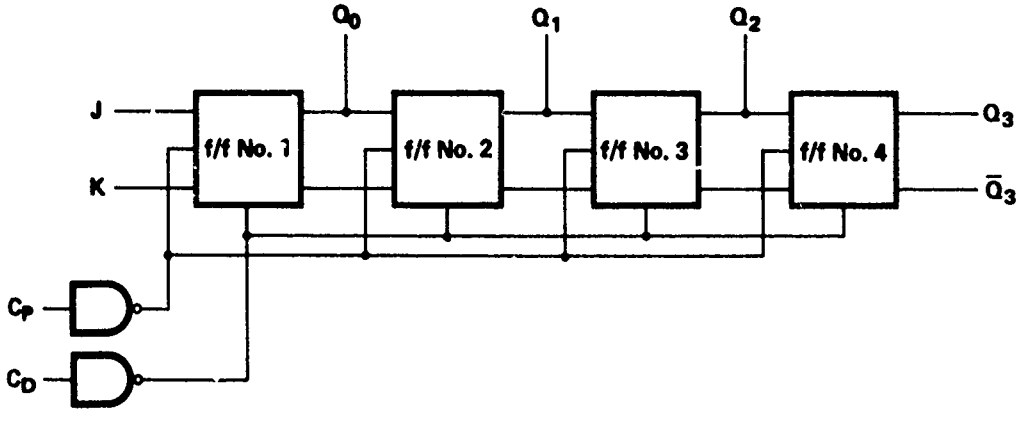
A. MODEL DEVELOPMENT

The computer model that has been developed to duplicate observed performance is shown in Figure VI-3. The computer model description is shown in Figure VI-4 and the subprogram which establishes the logic output signal levels, delay characteristics and radiation response behavior, in Figure VI-5.

The signal input impedances, J, JK, JRS and JCK, are represented as zero current sources. In SCEPTRE, this implies that the input signal terminals have infinite impedance (although the gates have measurable and varying impedance values which depend upon the applied signal level). This, as a first order approximation, will provide reasonably accurate results. For greater accuracy, the current sources should be modeled as "tabled" functions of current versus applied voltage in SCEPTRE. This method will provide a realistic device input impedance representation.

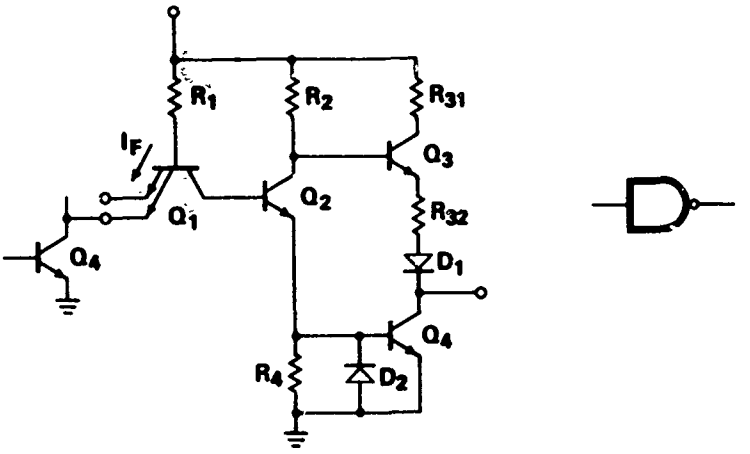


(A) A-O-1 Master-Slave Flip-Flop

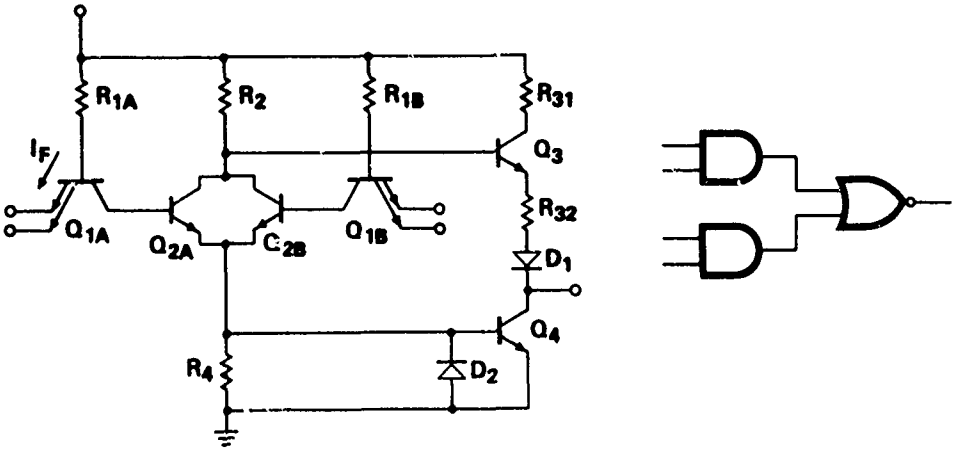


(B) Four Bit Shift Register

Figure VI-1. Logic Diagram



(A) NAND Gate



(B) A-O-1 Gate

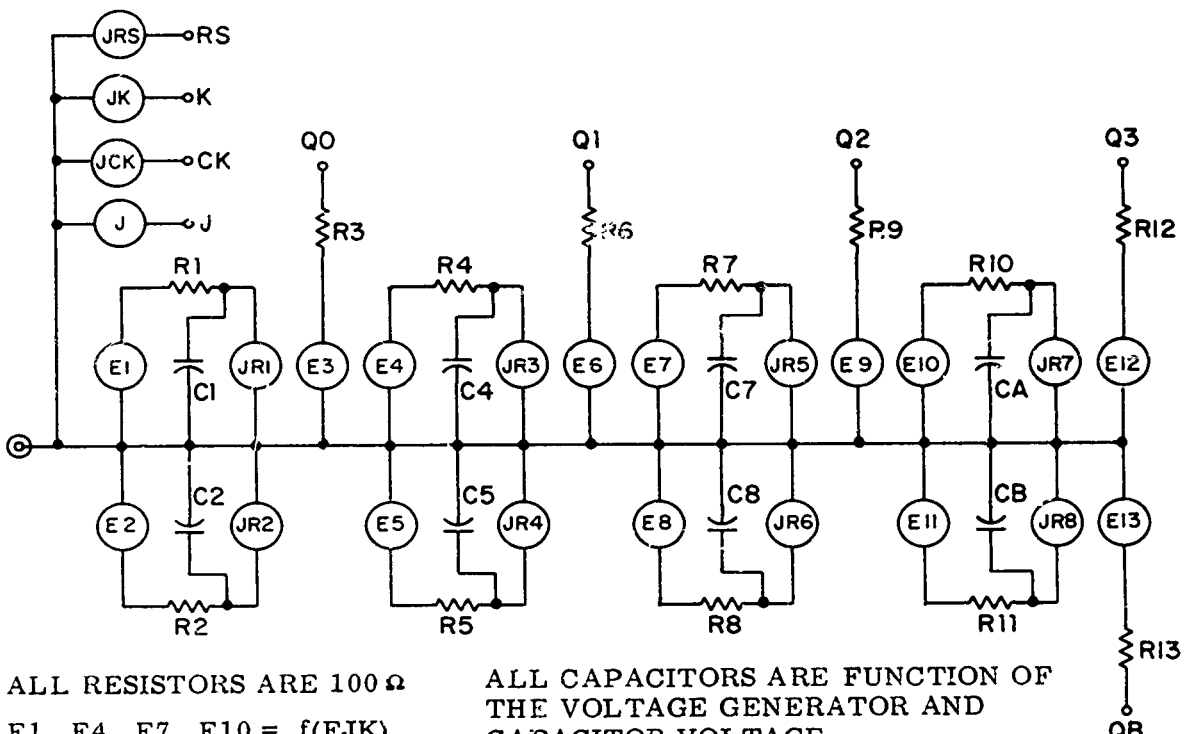
Figure VI-2. Schematic Diagram of Integrated AND and NOR Gates

TABLE VI-2.

ELECTRICAL CHARACTERISTICS FOR 9780 DEVICE

SYMBOL	CHARACTERISTICS	25°C LIMITS MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.40	3.0	----	Volts	Vcc = 4.5v, I_{OH} = -1.2 mA
V_{OL}	Output Low Voltage	----	0.25	0.40	Volts	Vcc = 5.5v, I_{OL} = 16 mA
V_{IH}	Input High Voltage	1.70	----	----	Volts	
V_{IL}	Input Low Voltage	----	----	0.90	Volts	
I_F	Input Load Current	----	-1.1	-1.6	mA	Vcc = 5.5v, V_F = 0.4v
I_R	Input Leakage Current	----	20	60	μA	Vcc = 5.5v, V_R = 4.5v
I_{PD}	Power Supply Current	----	55	80	mA	Vcc = 5.0v

SCEPTRE MODEL OF 9780 DEVICE



ALL RESISTORS ARE 100 Ω

E1, E4, E7, E10 = f(FJK)
E2, E5, E8, E11 = f(FJK1)

ALL CAPACITORS ARE FUNCTION OF THE VOLTAGE GENERATOR AND CAPACITOR VOLTAGE.

Figure VI-3. SCEPTRE Model of 9780 Device

```
MODEL 9/80 (RS-CK-J-K-Q0-Q1-Q2-Q3-Q3B-0)
              4-BIT SHIFT REGISTER
                   ELEMENTS
JRS,RS-0=0.
JCK,CK-0=0.
J,J-0=0.
JK,K-0=0.
F1,0-1=FJK(VJR2,P11,VJCK)
R1,1-2=100.
C1,2-0=FCAP(F1,VC1)
JR1,2-0=0.
F2,0-4=FJK1(VJR1,VJRS,P12,VJCK)
R2,4-5=100.
C2,5-0=FCAP(E2,VC2)
JR2,5-0=0.
F3,0-3=X1(VJR1)
R3,3-Q0=100.
F4,0-6=FJK(VJR4,P21,VJCK)
R4,6-7=100.
C4,7-0=FCAP(E4,VC4)
JR3,7-0=0.
F5,0-9=FJK1(VJR3,VJRS,P22,VJCK)
R5,9-10=100.
C5,10-0=FCAP(E5,VC5)
JR4,10-0=0.
F6,0-8=X2(VJR3)
R6,8-Q1=100.
F7,0-11=FJK(VJR6,P31,VJCK)
R7,11-12=100.
C7,12-0=FCAP(E7,VC7)
JR5,12-0=0.
C8,0-14=FJK1(VJR5,VJRS,P32,VJCK)
R8,14-15=100.
C8,15-0=FCAP(E8,VC8)
JR6,15-0=0.
F9,0-13=X3(VJR5)
R9,13-Q2=100.
F10,0-16=FJK(VJR8,P41,VJCK)
R10,16-17=100.
C10,17-0=FCAP(E10,VC10)
JR7,17-0=0.
F11,0-19=FJK1(VJR7,VJRS,P42,VJCK)
R11,19-20=100.
C11,20-0=FCAP(E11,VC11)
JR8,20-0=0.
F12,0-18=X4(VJR7)
R12,18-Q3=100.
F13,0-21=X5(VJR8)
R13,21-Q3B=100.
                   DEFINED PARAMETERS
P11=FJK2(P12,VJRS,VJ,VJR2,VJCK)
P12=FJK3(P11,VJK,VJR1,VJCK)
P21=FJK2(P22,VJRS,F3,VJR4,VJCK)
P22=FJK3(P21,VJR2,VJR3,VJCK)
P31=FJK2(P32,VJRS,F6,VJR6,VJCK)
P32=FJK3(P31,VJR4,VJR5,VJCK)
P41=FJK2(P42,VJRS,E9,E13,VJCK)
P42=FJK3(P41,VJR6,F12,VJCK)
                   OUTPUTS
VJR1,VJR2,PLOT
```

Figure VI-4. Computer Model Description

```
      FUNCTION FJK(A,B,C)
C
C     SR TO TRIG ON POS. SLOPE OF CLOCK 10-8-71 WAM
C     SR TO RESET FOR HIGH AT RS INPUT 10-8-71 WAM
      N1=1
      IF(A.GE.1.5.AND.B.GE.1.5) N1=2
      N2=1
      IF(A.GE.1.5.AND.C.LE.2.0) N2=2
      GO TO 1
C
      ENTRY FJK1(A,B,C,D)
C
      N1=1
      IF(A.GE.1.5.AND.B.LE.1.5.AND.C.GE.1.5) N1=2
      N2=1
      IF(A.GE.1.5.AND.D.LE.2.0.AND.B.LE.1.5) N2=2
      GO TO 1
C
      ENTRY FJK2(A,B,C,D,E)
C
      N1=1
      IF(C.GE.1.5.AND.D.GE.1.5 AND.E.LE.0.8) N1=2
      N2=1
      IF(A.GE.1.5.AND.B.LE.1.5) N2=2
      GO TO 1
C
      ENTRY FJK3(A,B,C,D)
C
      N1=1
      IF(A.GE.1.5) N1=2
      N2=1
      IF(B.GE.1.5.AND.C.GE.1.5.AND.D.LE.0.3) N2=2
C
    1 FJK=0.1
      IF(N1.EQ.1.AND.N2.EQ.1) FJK=3.0
      RETURN
C
      ENTRY FCAP(A,B)
C
      FJK=300.E-12
      IF(A.LT.B) FJK=75.E-12
      RETURN
      ENTRY FNVT(A,B,C)
C     NEUTRON BEHAVIOR OF CIRCUIT
      IF(A .LE. 2.)GO TO 100
      X=-B
      FJK=X
      GO TO 1000
  100 Y=C
      FJK=Y
 1000 RETURN
```

Figure VI-5. Model Subprogram

As indicated on Figure VI-1(B), each section of the shift register is considered an independent master-slave J-K flip-flop, as shown in Figure VI-1(A). The inputs to the first stage are the signals on the J, K, C_P, and C_D terminals (Figure VI-1). The input to subsequent stages are the same C_P and C_D signals. However, the J and K signals are the Q and $\overline{Q}$ outputs from the preceding stage. Since each stage uses the same functions to generate the output signals, only one will be discussed.

The voltage associated with dependent sources E1 and E2 (Figure VI-3) are determined by the functions FJK, FJK1, FJK2 and FJK3. The functions are an implementation of the logic in Figure VI-6. The functions are connected to form the master and slave gates as shown in Figure VI-1(A). These complex relationships are entered into the model descriptions as functions, thereby allowing the use of the relatively simple model shown in Figure VI-3. This figure schematically presents how the functions are included in the model, while Figure VI-4 indicates the method for inclusion in a SCEPTRE listing.

Defined parameters P11 and P12, in the computer model description, are the output signals for the master gates determined by FJK2 and FJK3, respectively. The slave gate outputs are E1 and E2, determined by FJK and FJK1, respectively. The output signals from the master gates are saved as defined parameters to avoid confusion with use of multiple J-K flip-flops. The logic levels are 1 for signals greater than or equal to 1.5 volts, and 0 for signals less than 1.5 volts.

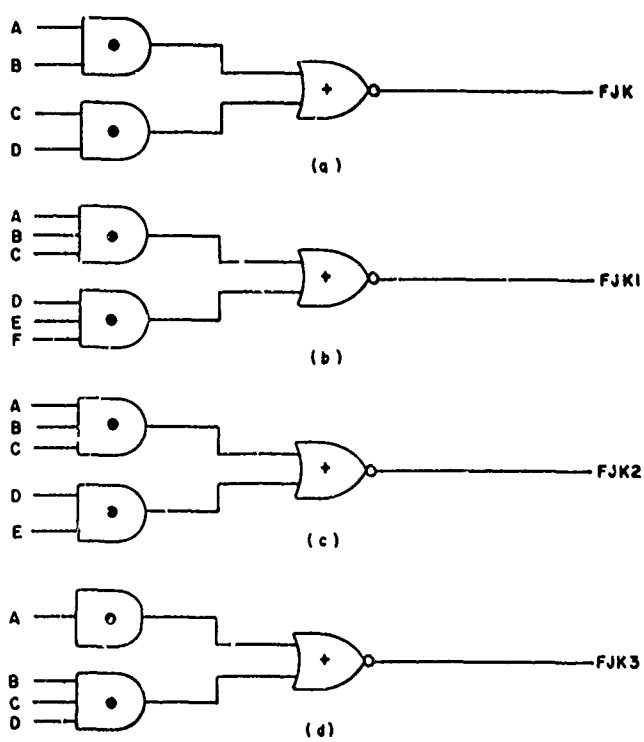


Figure VI-6. Subfunction Logic Diagram

Although the device manufacturer indicates (Table VI-3) that the switching delay times for either positive or negative going output signals will be approximately 20 nanoseconds, laboratory test measurements on many units indicate not only that both delays are shorter than this worst case value, but that they are different from each other. Therefore, the delay times t_{pd1} and t_{pd0} are established in the model by the time constants R1 - C1 and R2 - C2. Each time constant is changed by varying the value of C1 or C2, depending upon whether a logic 1 or 0 is required as an output signal.

The value of C1 and C2 is determined by means of subprogram FCAP. Thus, C1 is set to 75 picofarads unless E1 is greater than, or equal to, VC1 (voltage across C1). When this latter condition occurs, C1 assumes the value of 300 picofarads. In a similar manner C2 is determined. The output voltage E3 is equal to the voltage across the capacitor C1 (JR1 is a zero valued current source, required by SCEPTRE for dc circuit evaluation conditions and is in parallel with C1); therefore, a relationship between the input signal levels and output voltages is readily established. JR1 is also used as a source of gamma radiation injection in the model, when required. The FORTRAN flow charts associated with these functions are shown in Appendix VI-A.

The output impedance of the bit (Q_0) is fixed at 100 ohms. Although this value is not an accurate impedance representation for all voltage and load conditions, it provides first order accuracy of output signal level. To duplicate actual impedance variations, the value of resistor R3 would be made variable and a function of the load voltage and currents.

The $\overline{Q}$ for each stage is modeled to provide the necessary feedback for the latching of the master gates as shown in Figure VI-1. Since the 9780 device provides a $\overline{Q}$ output only for the last bit (Q3), the model includes an output buffer stage only for the last bit.

B. MODEL VERIFICATION

To demonstrate the validity of the model, the circuit shown in Figure VI-7 was described to the computer.

The topological description for SCEPTRE of the 9780 connected in a test circuit configuration is shown in Figure VI-8. The circuit is used to demonstrate that the reset is independent of the clock and also that the first stage of the shift register toggles between a high and low level with each clock pulse. The J and K inputs are maintained at a high level during these tests.

The results of the computer analysis are shown in Figures VI-9 through VI-14. The reset signal plotted in Figure VI-9, is active for the first 100 nanoseconds to initialize all of the shift register Q outputs to a low level. Both the J and K inputs are maintained at a high level so that the output at Q_0 will toggle between a high and low level on the leading edge of each clock pulse shown in Figure VI-10. The Q_1 and succeeding stages will then see either a high or low level at the J-K input and behave in accordance with the truth table. Therefore, one clock pulse delay should occur between the time when the Q_0 signal is high and when the Q_1 signal goes high. Thus,

TABLE VI-3.

SWITCHING CHARACTERISTICS FOR 9780

SYMBOL	CHARACTERISTIC	25°C LIMIT			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
t_{pd+}	Turn-off delay	----	18	----	ns	Vcc = 5v, C_L = 15pf
t_{pd-}	Turn-on delay	----	22	----	ns	Vcc = 5v, C_L = 15pf

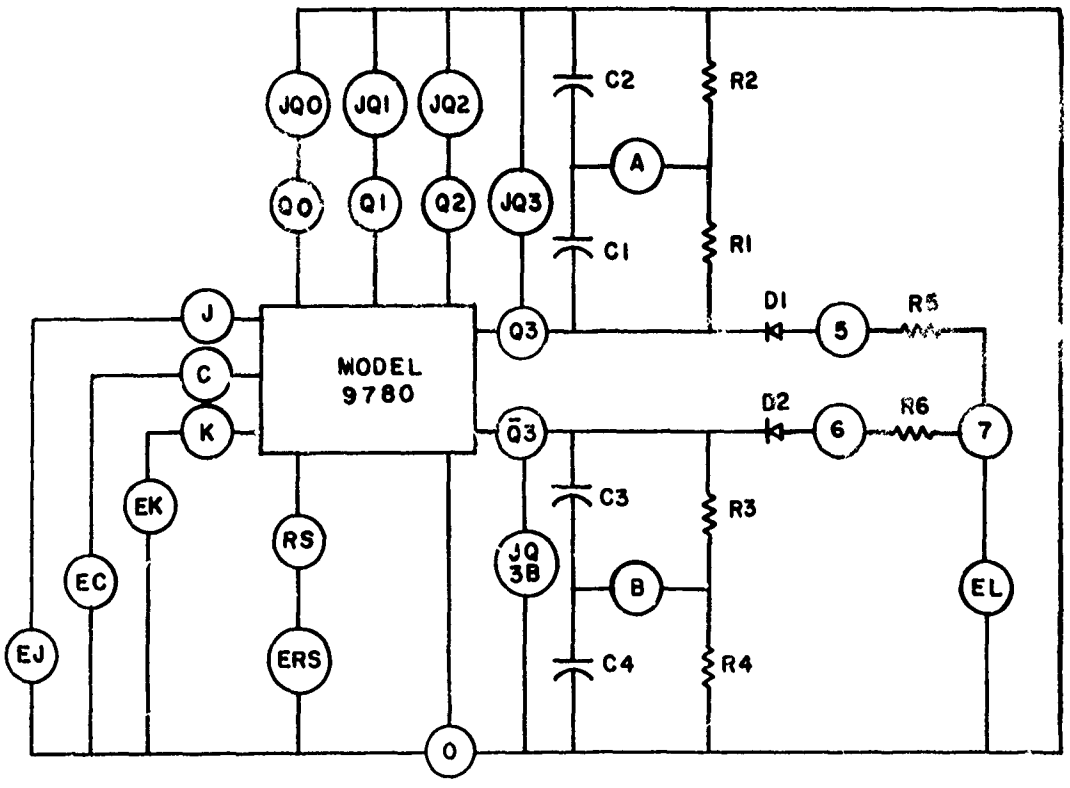


Figure VI-7. Shift Register Test Circuit

```
F1,RS-C-J-K-Q)-Q1-Q2-Q3-QW3-B=MODEL 9700
ERS,B-RS=T1
EC,B-C=FCOW(0.,3.,1.E-7,1.5E-8,2.E-7,1.5E-8,4.E-7,100.,TIME)
EJ,B-J=T2
EK,B-K=T3
R1,Q3-A=4300.
C1,Q3-A=2.E-12
R2,A-B=750.
C2,A-B=11.5E-12
D1,Q3-5=MODEL 1N3685 (PERM)
R5,5-7=900.
F1,4-7=2.4
R3,QW3-B=4300.
C3,QB3-B=2.E-12
R4,B-8=750.
C4,B-8=11.5E-12
D2,QB3-6=MODEL 1N3685 (PERM)
R6,6-7=900.
IQ0,Q0-0=0.
IQ1,Q1-0=0.
IQ2,Q2-0=0.
IQ3,Q3-0=0.
IQB3,QB3-0=0.
        FUNCTIONS
T1=0.,3.,1.E-7,3.,1.15E-7,1.4.E-6,1.4.015E-6,3.
T2=0.,3.,5.E-6,3.
T3=0.,3.,5.E-6,3.
        OUTPUTS
EC,EJ,EK,ERS,PLOT
VJQ0,VJQ1,VJQ2,VJQ3,VJQB3,PLOT
        RUN CONTROLS
START TIME = 0.
MAXIMUM PRINT POINTS = 200
COMPUTER TIME LIMIT = 5.5
STOP TIME = 5000.E-9
END
```

Figure VI-8. Test Circuit Description - CLOCK Trigger

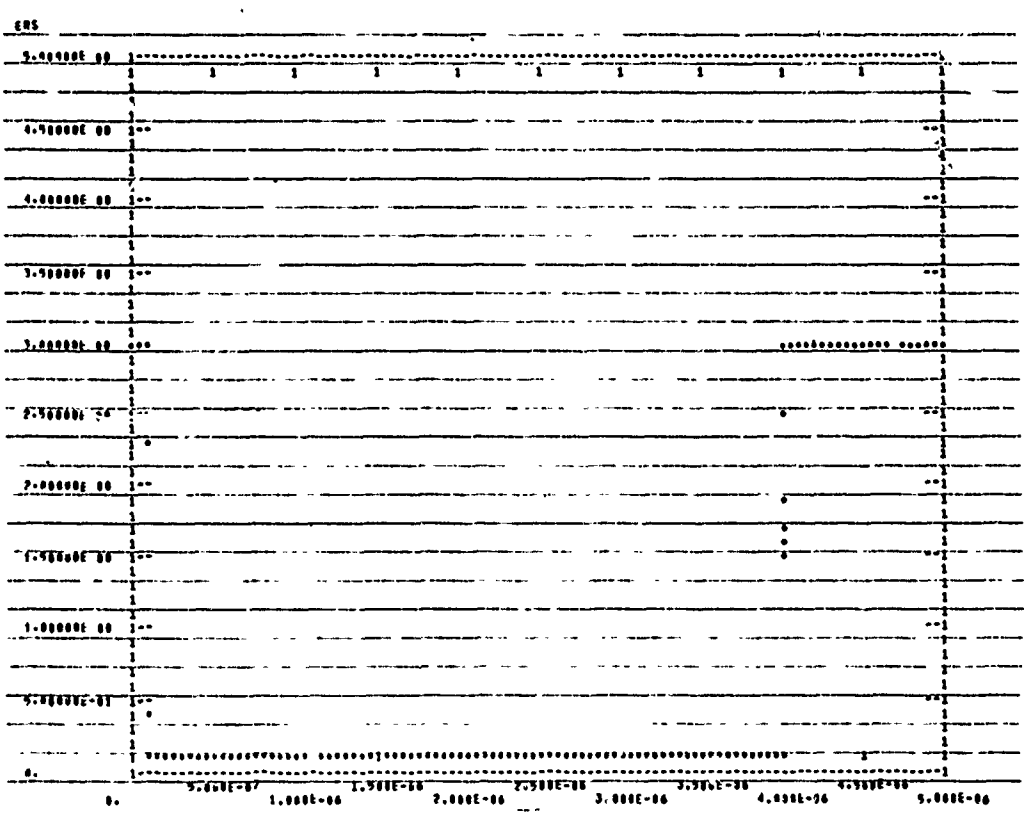


Figure VI-9. RESET Input Signal

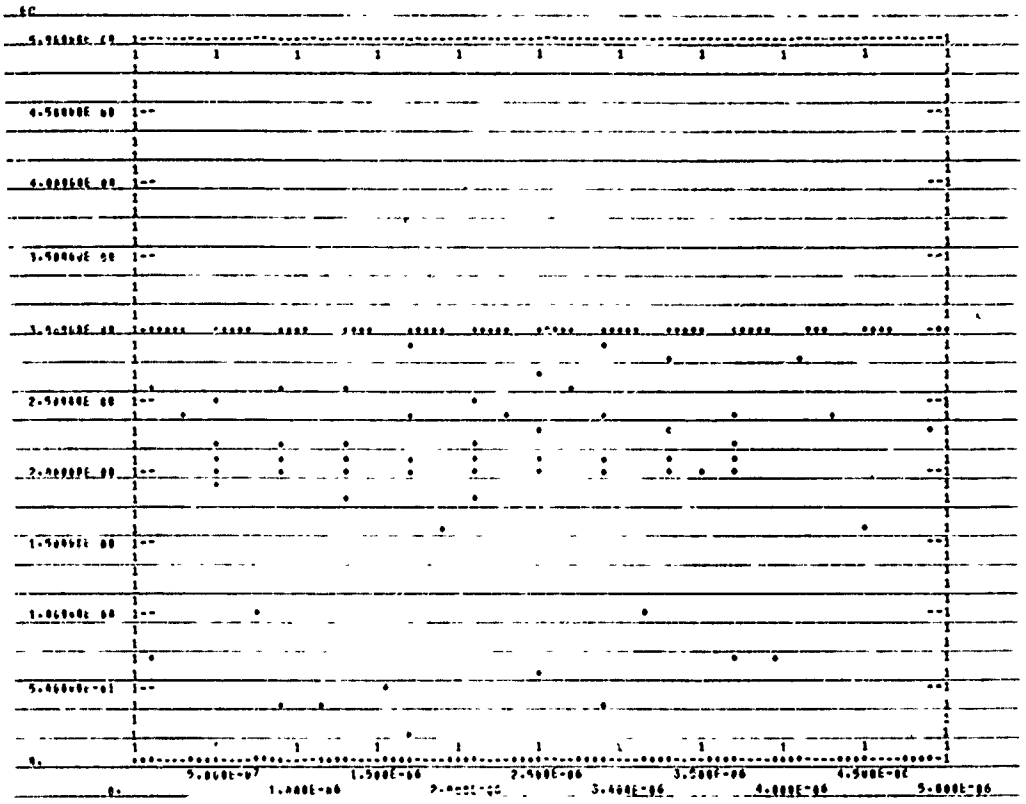


Figure VI-10. CLOCK Input Signal

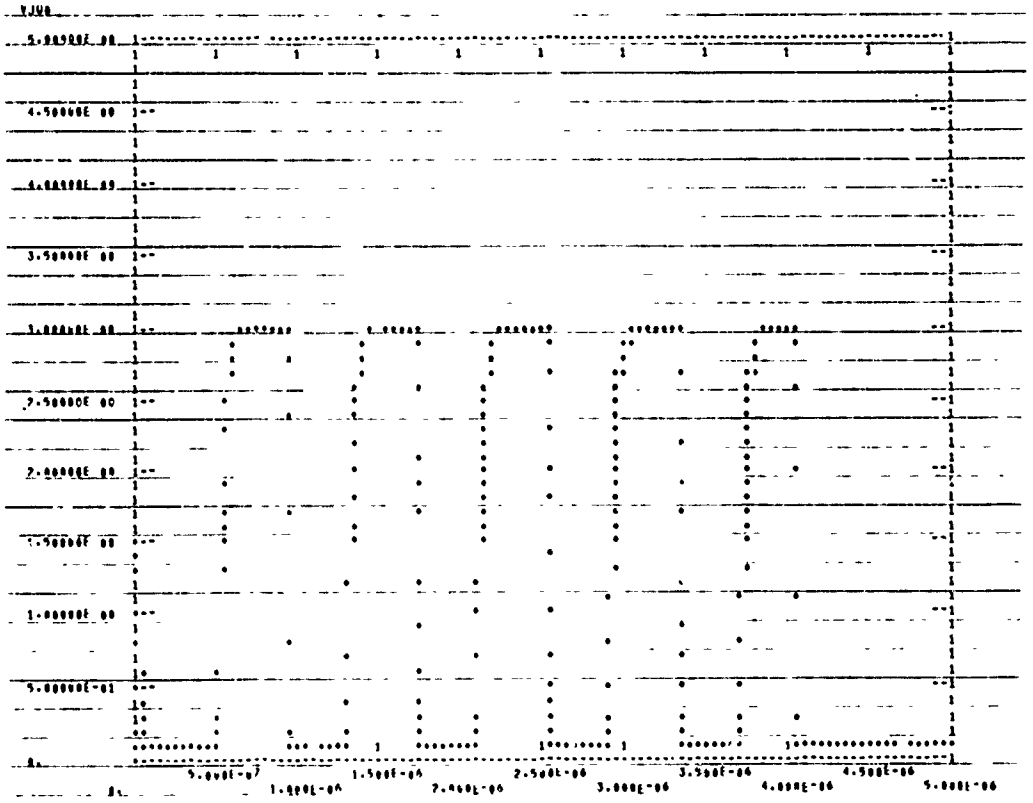


Figure VI-11. Q_0 - Output

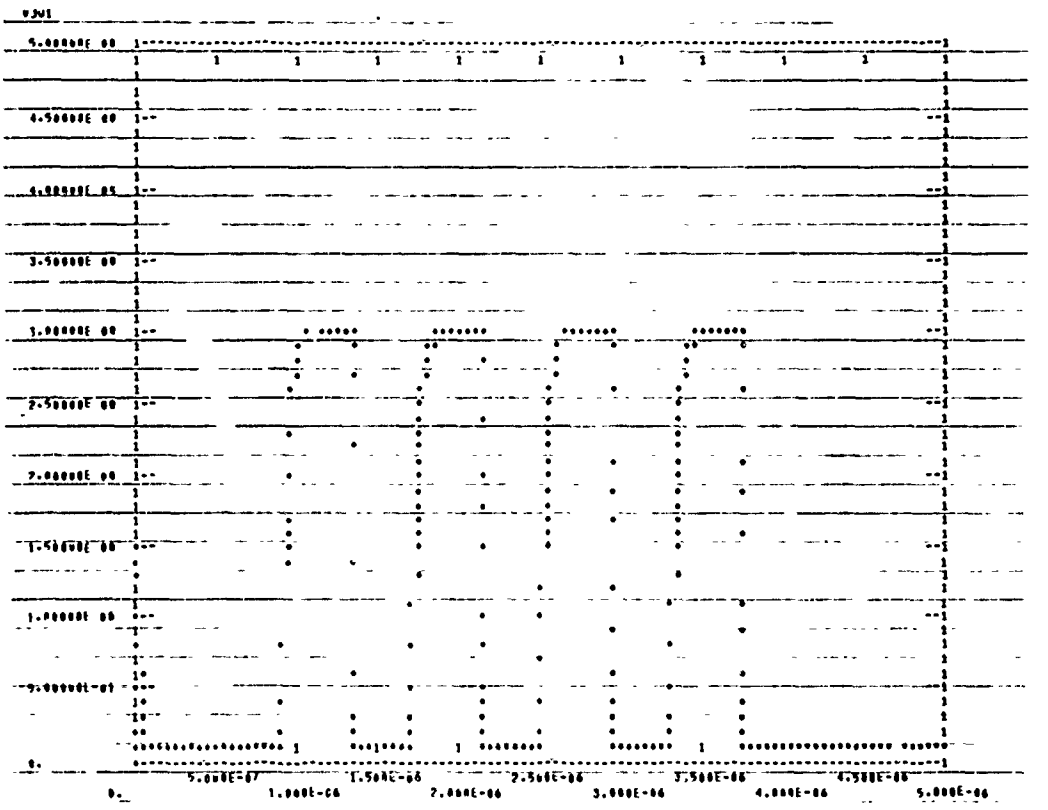


Figure VI-12. Q_1 - Output

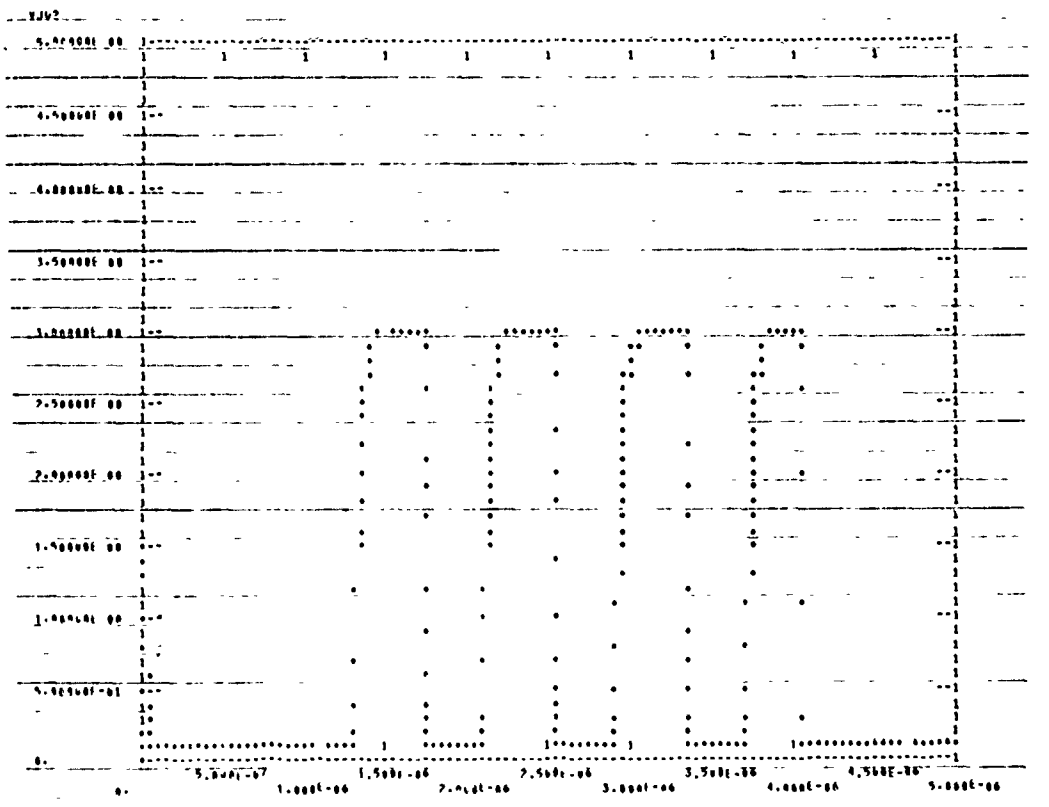


Figure VI-13. Q_2 - Output

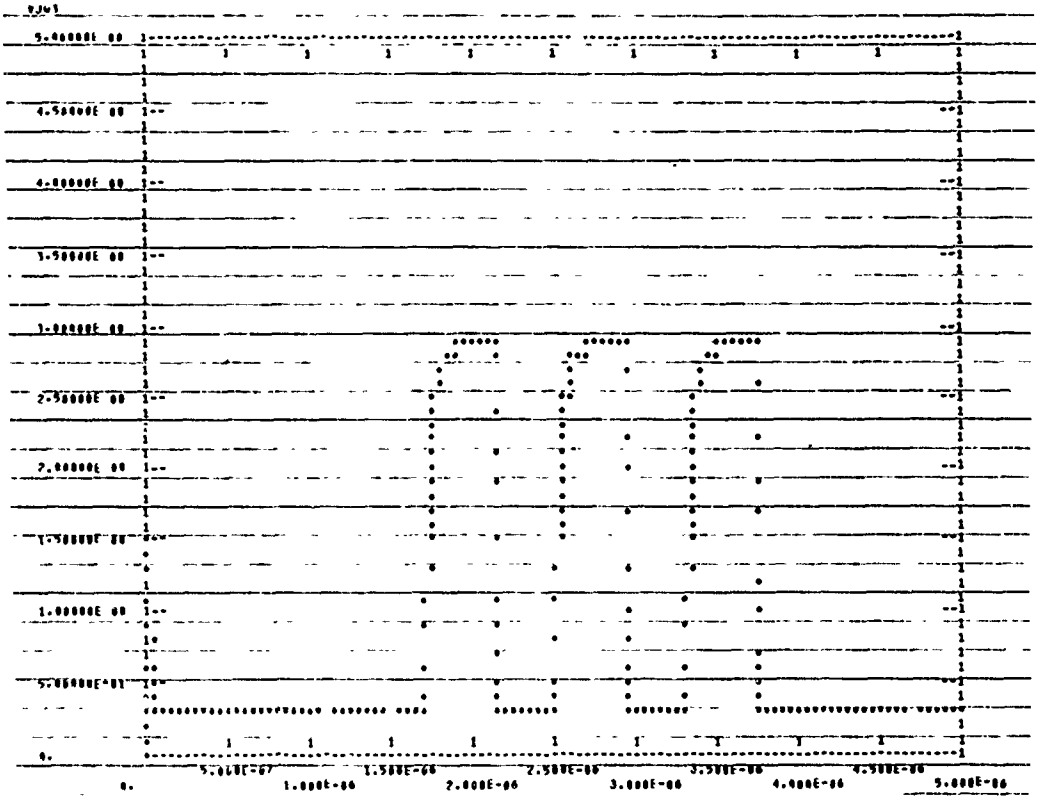


Figure VI-14. Q_3 - Output

each Q output should be a square wave signal delayed by N clock pulses (where N = the number of stages from the input stage). Proper delay operation is shown in Figures VI-11 through VI-14 since the signal remains low until the proper number of clock counts occur. The output $\overline{Q3}$ is the complement of Q3. The waveforms shown in Figures VI-14 and VI-15 demonstrate these expected relationships.

The reset in Figure VI-9 is activated again where time = 4000 nanoseconds. This forces the Q output state of each flip-flop stage to a 0 level and the $\overline{Q}$ output to a 1 level. The waveforms shown in Figures VI-11 through VI-15 indicate that desired result.

To verify that the input stage of the 9780 model and succeeding stages respond to the remainder of the truth table combinations, where either J or K is in a high state (but not both at the same time), the inputs to the circuit are changed per the listings in Figure VI-16.

The reset signal, Figure VI-17, is active for the first 100 nanoseconds to initialize all of the Q outputs in the low (0 state). The clock pulse timing is as in Figure VI-10. The J input, shown in Figure VI-18, is high for one clock pulse; the K input, shown in Figure VI-19, is high during the following clock pulse. This combination of signals should be a pulse to flow through the shift register, delayed by one clock pulse at each output. Figures VI-20 through VI-24 demonstrate proper model performance.

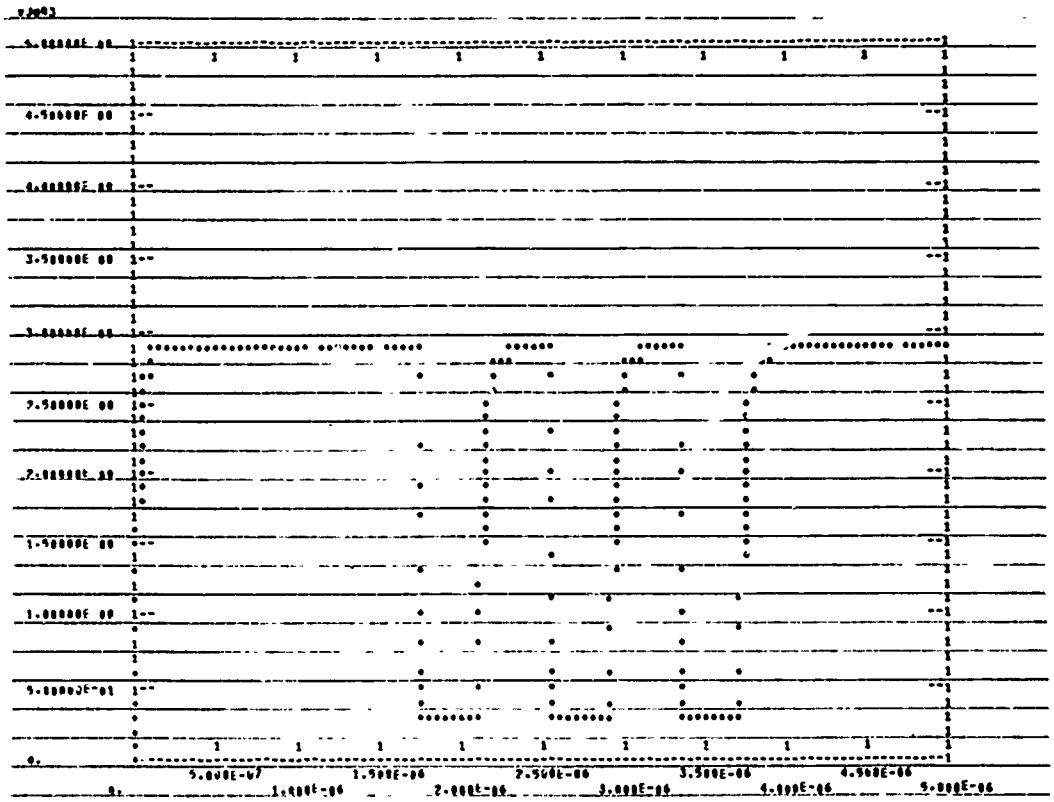


Figure VI-15. $\overline{Q}_3$ - Output

```
EJ,RS-C-J-K-Q0-Q1-Q2-Q3-QB3-0=MODEL 9780
EKS,0-RS=T1
EC,0-C=FOGEN(0.,3.,1.E-7,1.5E-8,2.E-7,1.5E-8,4.E-7,100.,TIME)
EJ,0-J=T2
EK,0-K=T3
R1,Q3-A=4300.
C1,Q3-A=2.E-12
R2,A-0=750.
C2,A-0=11.5E-12
D1,Q3-5=MODEL 1N3605 (PERM)
R5,5-7=800.
EL,0-7=2.4
R3,QB3-8=4300.
C3,QB3-0=2.E-12
R4,0-0=750.
C4,0-0=11.5E-12
D2,QB3-6=MODEL 1N3605 (PERM)
R6,6-7=900.
JQ0,Q0-0=0.
JQ1,Q1-0=0.
JQ2,Q2-0=0.
JQ3,Q3-0=0.
JQB3,QB3-0=0.
        FUNCTIONS
T1=0.,3.,1.E-7,3.,1.15E-7,.1
T2=0.,.1,1.5E-8,3.,4.E-7,3.,4.15E-7,.1
T3=0.,.1,8.5E-7,.1,8.65E-7,3.,1.265E-6,3.,1.28E-6,.1
        OUTPUTS
EC,EJ,EK,EKS,PLOT
VJQ0,VJQ1,VJQ2,VJQ3,VJQB3,PLOT
        RUN CONTROLS
START TIME = 0.
MAXIMUM PRINT POINTS = 200
COMPUTER TIME LIMIT = 5.5
STOP TIME = 5000.E-9
END
```

Figure VI-16. Test Circuit Description - Input Trigger

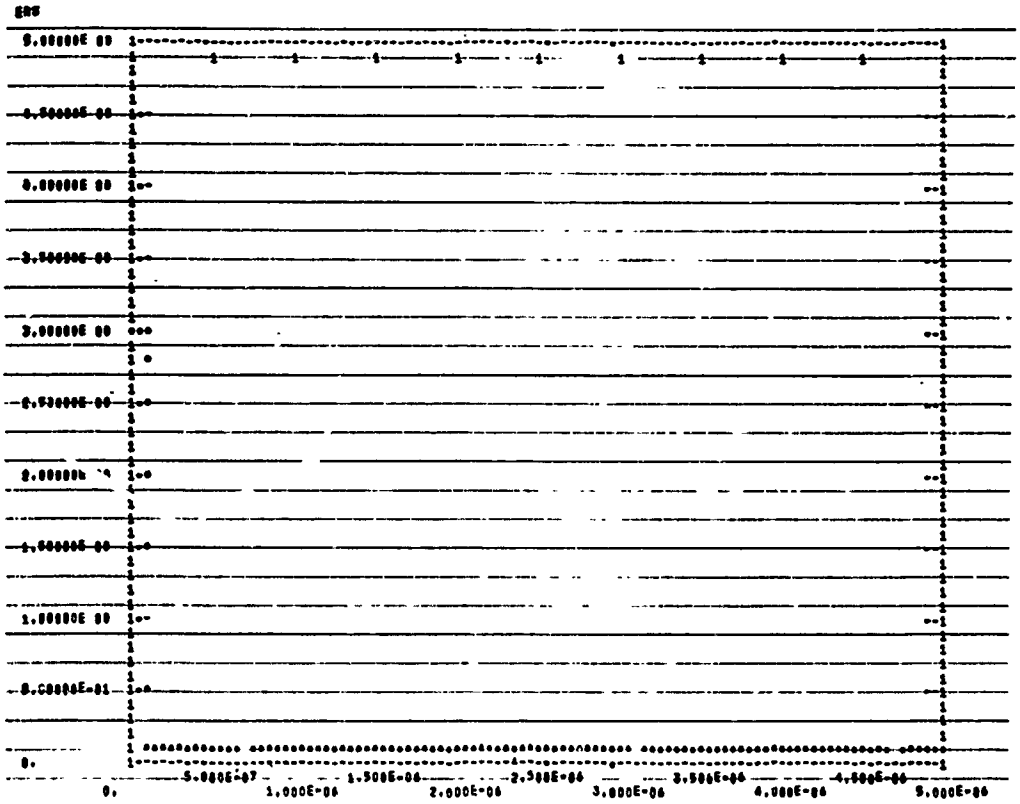


Figure VI-17. RESET Input Signal

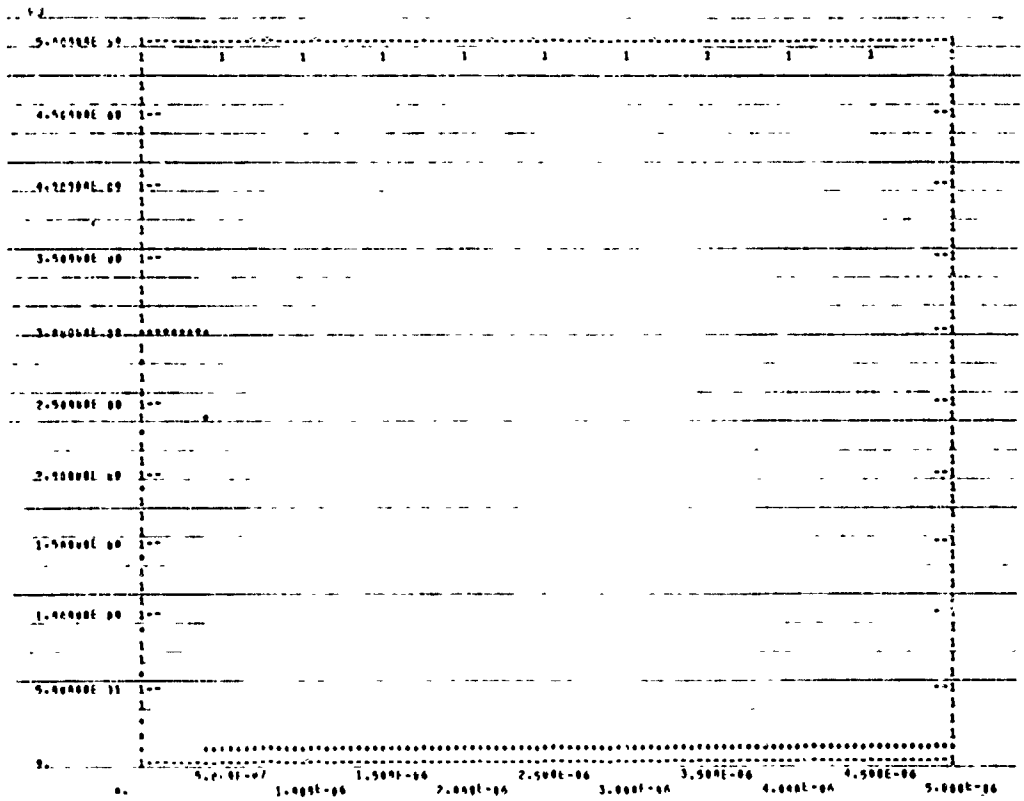


Figure VI-18. J - Input Signal

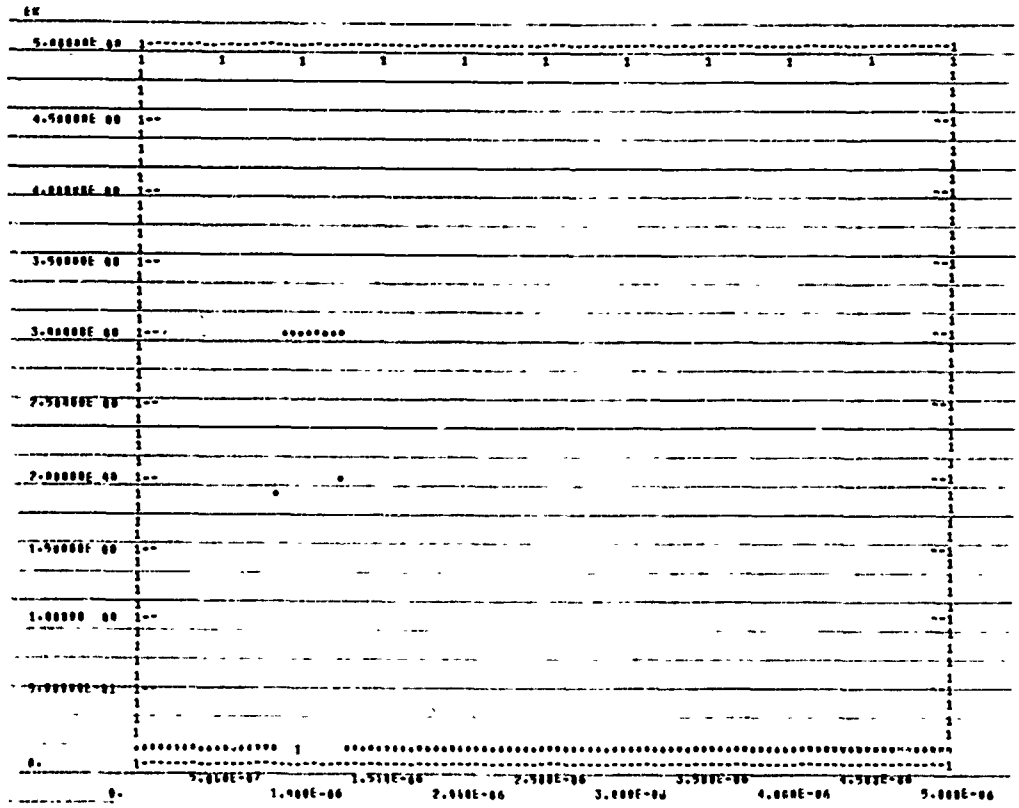


Figure VI-19. K - Input Signal

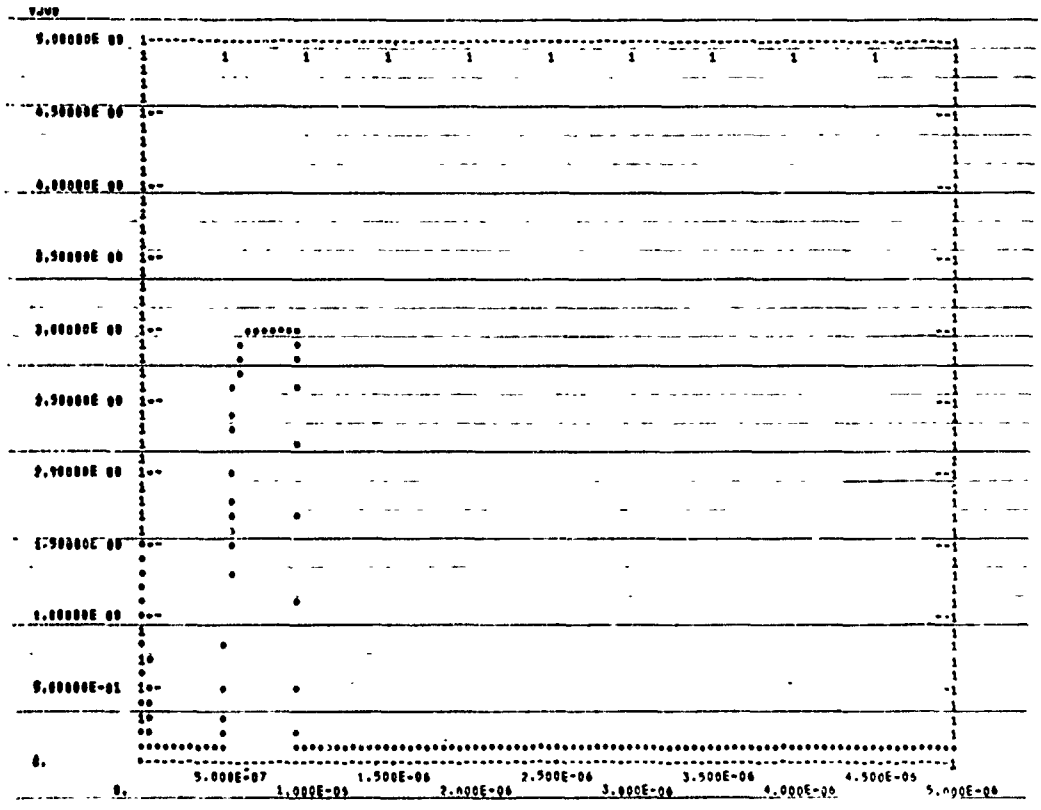


Figure VI-20. Q_0 - Output

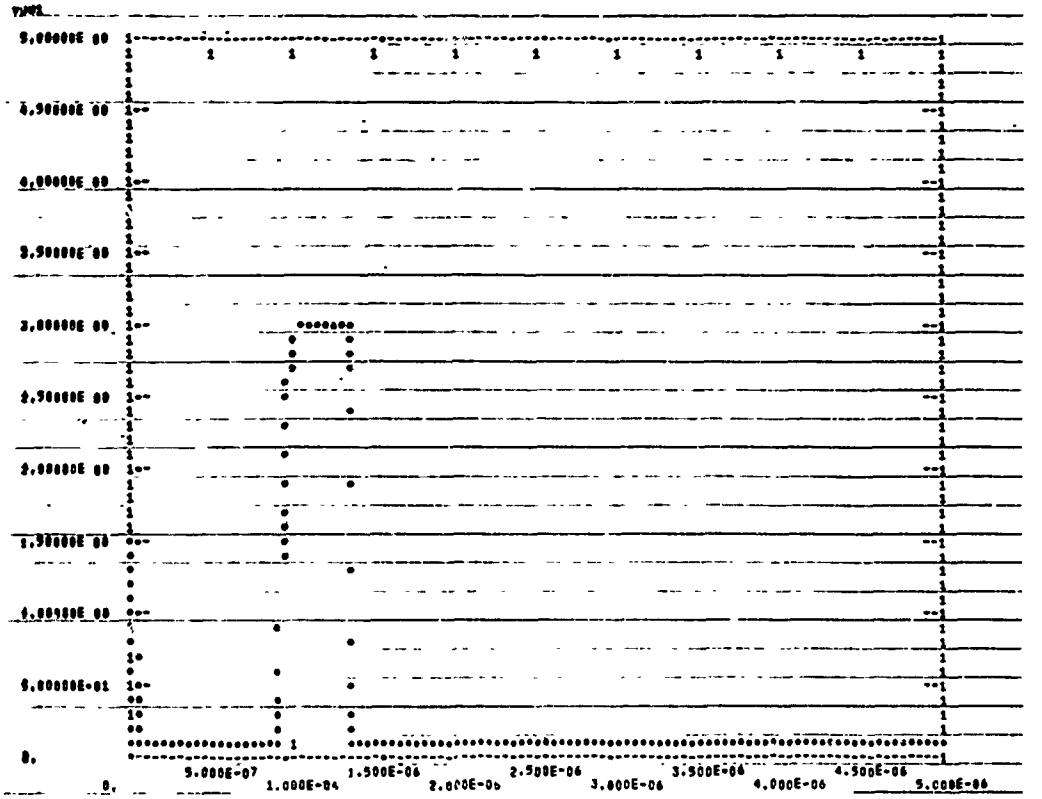


Figure VI-21. Q_1 - Output

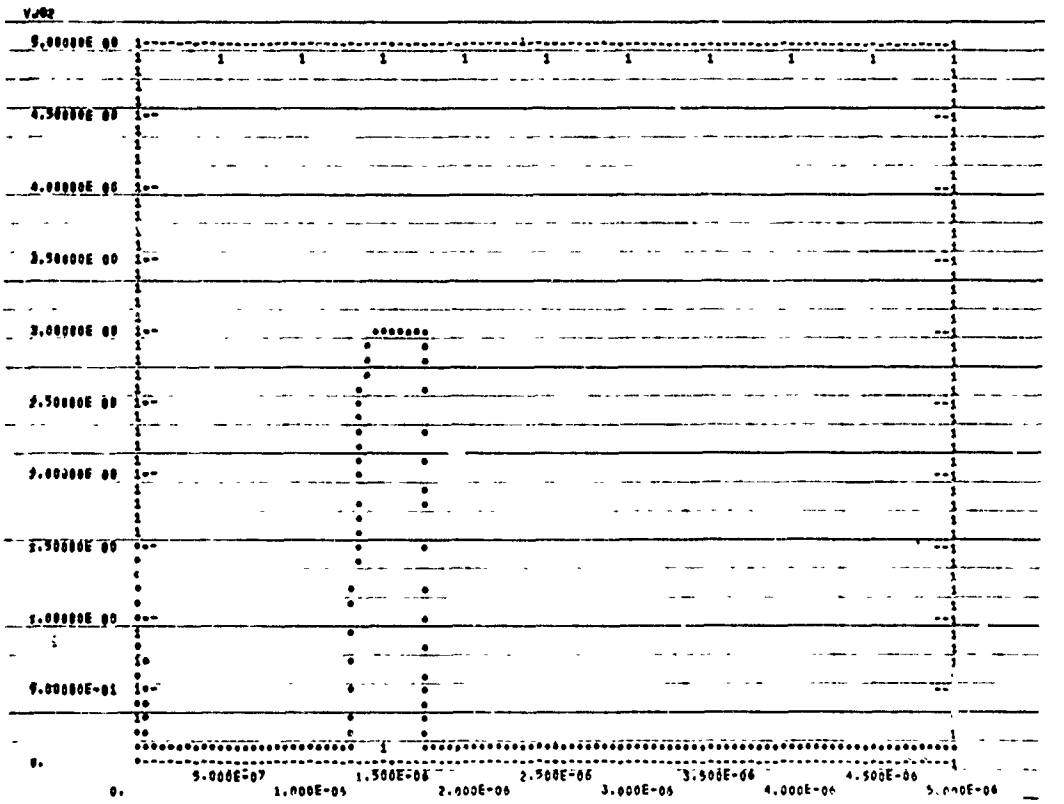


Figure VI-22. Q_2 - Output

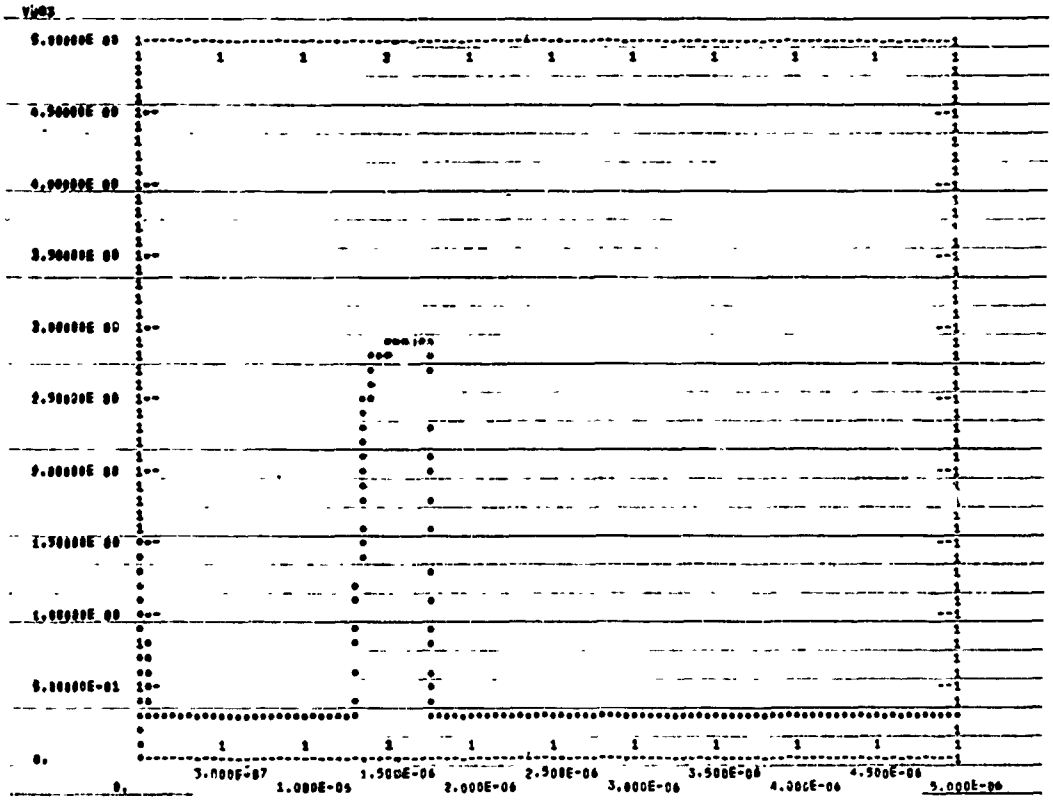


Figure VI-23. Q_3 - Output

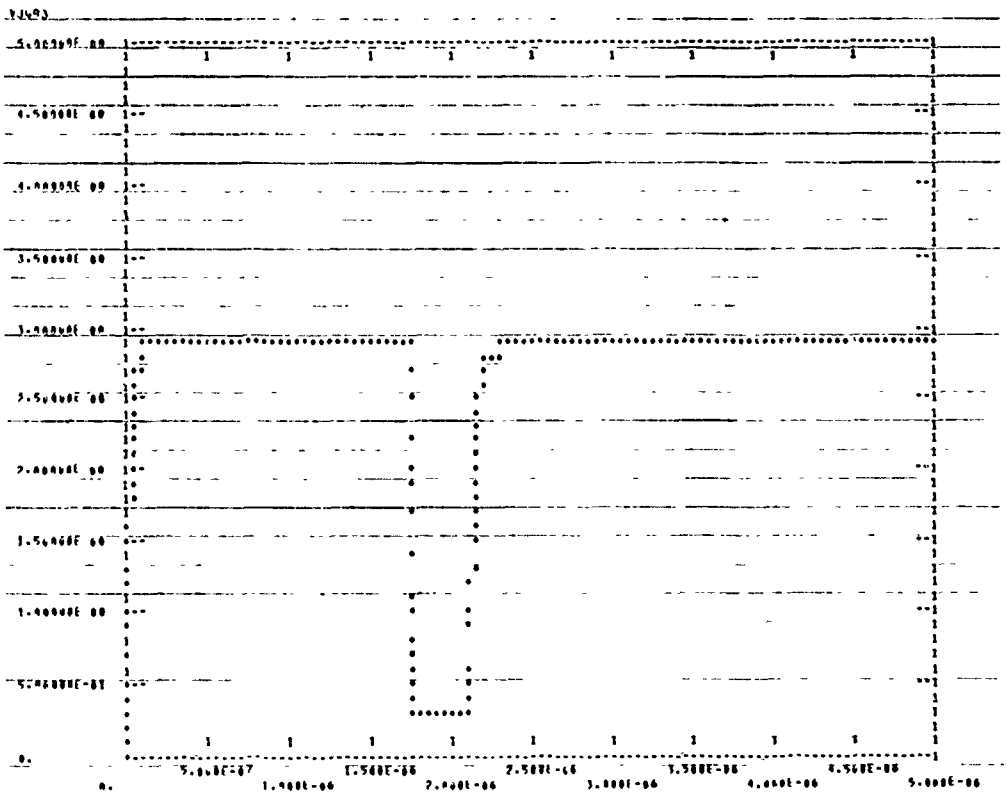


Figure VI-24. $\overline{Q}_3$ - Output

The delay time between the clock pulse rising to 1.5 volt and the output rising to 1.5 volts is the turn-on time, t_{pd+}. The delay time between the clock rising to 1.5 volts and the output falling to 1.5 volts is the turn-off time, t_{pd-}. The manufacturer's prescribed switching times are shown in Table VI-3. The computer time delays, shown in Table VI-4, correspond favorably with the manufacturer's typical values.

C. RADIATION EFFECTS

1. GAMMA RADIATION

Exposing the device to a nuclear radiation environment may affect normal performance by causing the output signal level to vary. When exposed to pulsed ionizing rays (gamma radiation) at dose rate levels of approximately $3 \times 10^{+10}$ rad (Si)/second, the performance is only momentarily affected. Extensive testing was done by the General Electric Company on many of these devices. The test report with photographic recording of the results is included in Appendix VI-B.

When a gamma radiation pulse simulation is caused to occur at about 2.75 micoseconds, the output response of the device is momentarily changed. The method for including this effect into the model is shown in Figure VI-25. Table 4 of this figure simulates the gamma pulse. Figures VI-26 through VI-30 show the computer response to the radiation pulse. The circuit performance conditions are the same as those shown in Figure VI-8, with the exception that several of the current sources in the device model description are changed from a zero value (Figure VI-5) to a dependency on the voltage across the parallel capacitor and the gamma pulse (Figure VI-31). The current sources that are involved are JR1, JR3, JR5, JR7 and JR8, which affect the outputs Q_0, Q_1, Q_2, Q_3 and QB_3, respectively.

TABLE VI-4

COMPUTER TIME DELAYS

OUTPUT	TIME DELAY	
	Turn-On	Turn-Off
Q	22 sec	27 sec
$\overline{Q}$	23 sec	28 sec

```
                    TIMING DELAY TEST
                    SAVED UNDER FILE 9780
                    ELEMENTS
E1.RS=C-J-K-00-01-02-03-0B3-B=MODEL 9780(CHANGE P6=T4)
FRS,0-RS=11
FC,0-C=LGEN(0.,3.,1.E-7,1.5E-6,2.E-7,1.5E-8,4.E-7,100.,TIME)
EJ,0-J=12
FK,0-K=13
R1,03-A=4300.
C1,03-A=2.E-12
R2,A-0=750.
C2,A-0=11.5E-12
D1,03-5=MODEL 1N3605 (PERM)
R5,5-7=800.
EL,0-7=2.4
R3,0B3-B=4300.
C3,0B3-B=2.E-12
R4,B-0=750.
C4,B-0=11.5E-12
D2,0B3-6=MODEL 1N3605 (PERM)
R6,6-7=900.
100,00-0=0.
101,01-0=0.
102,02-0=0.
103,03-0=0.
10B3,0B3-0=0.
DEFINED PARAMETERS
P11=ENVT(VC1F1,0.4,0.06)
P12=ENVT(VC4F1,0.4,0.06)
P13=ENVT(VC7F1,0.4,0.06)
P14=ENVT(VCAF1,0.4,0.06)
P15=ENVT(VCEF1,0.4,0.06)
        FUNCTIONS
T1=0.,3.,1.E-7,3.,1.15E-7,.1,3.4E-6,.1,3.415E-6,3.
T2=0.,3.,10.E-6,3.
T3=0.,3.,10.E-6,3.
T4=0.,0.
2.7E-6,0.
2.7E-6,0.03
2.8E-6,0.03
2.8E-6,0.
10.E-6,0.
        OUTPUTS
EC,F1,EN,FRS,PLOT
VJ00,VJ01,VJ02,VJ03,VJ0B3,PLOT
        RUN CONTROLS
MAXIMUM PRINT POINTS = 200
COMPUTER TIME LIMIT = 5.5
STOP TIME = 5000.E-9
END
```

Figure VI-25. Gamma Radiation Test Circuit Description

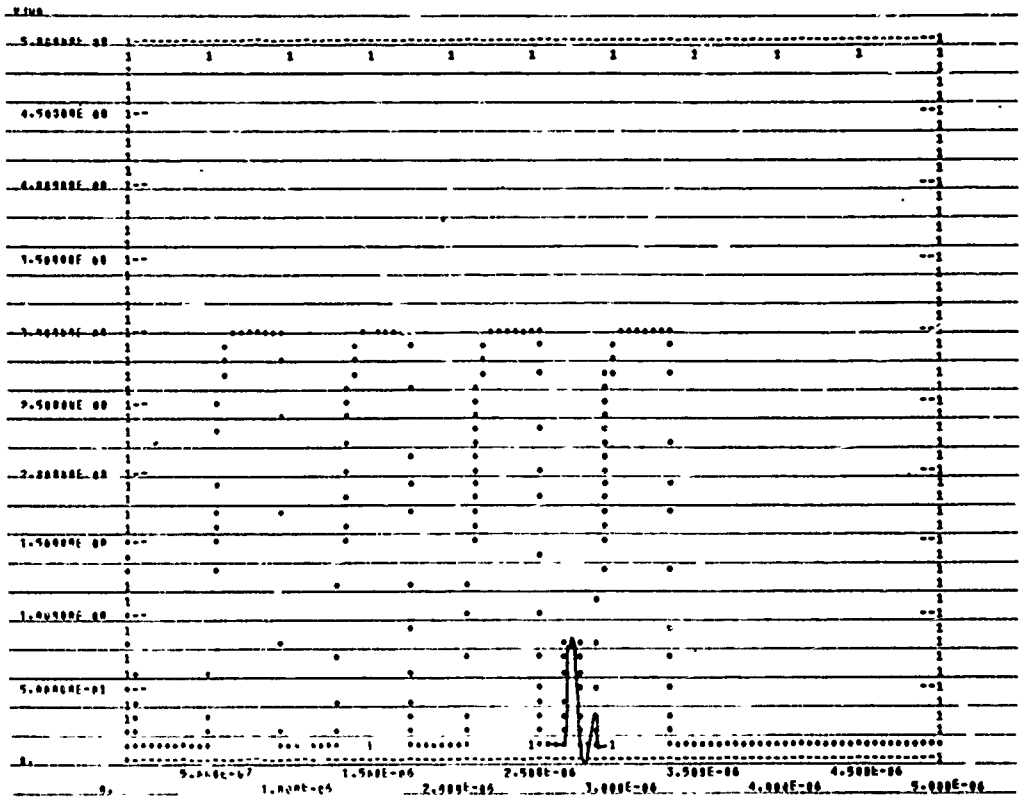


Figure VI-26. Q_0 - Response to Gamma Radiation

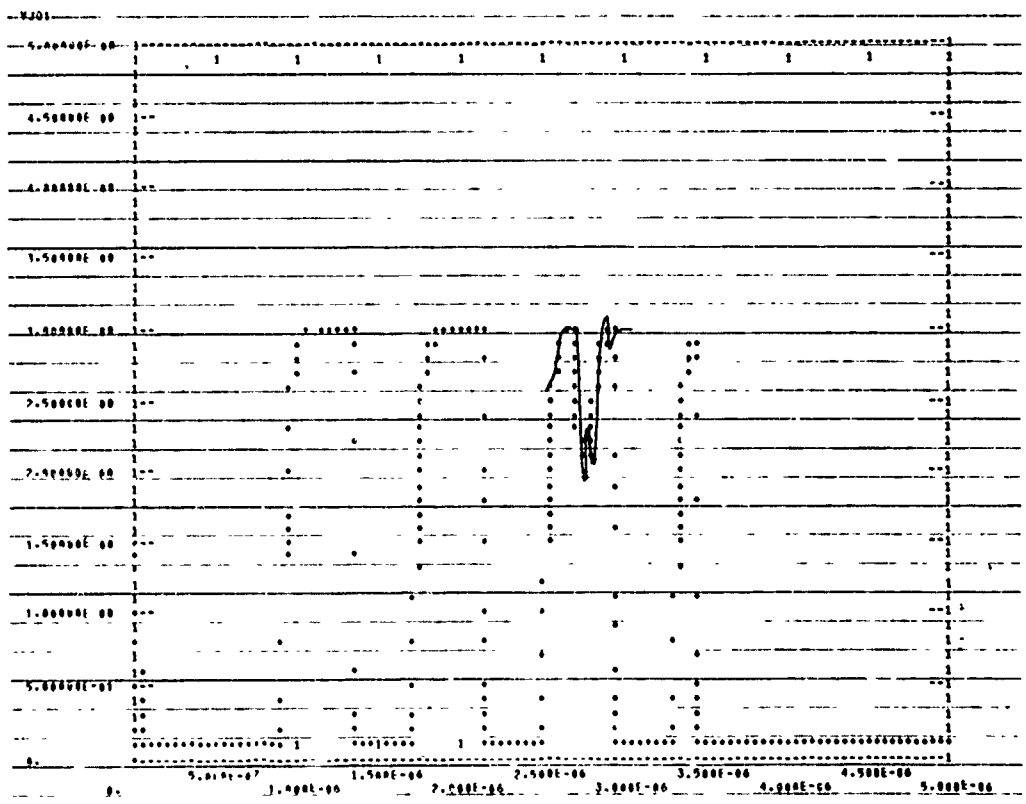


Figure VI-27. Q_1 - Response to Gamma Radiation

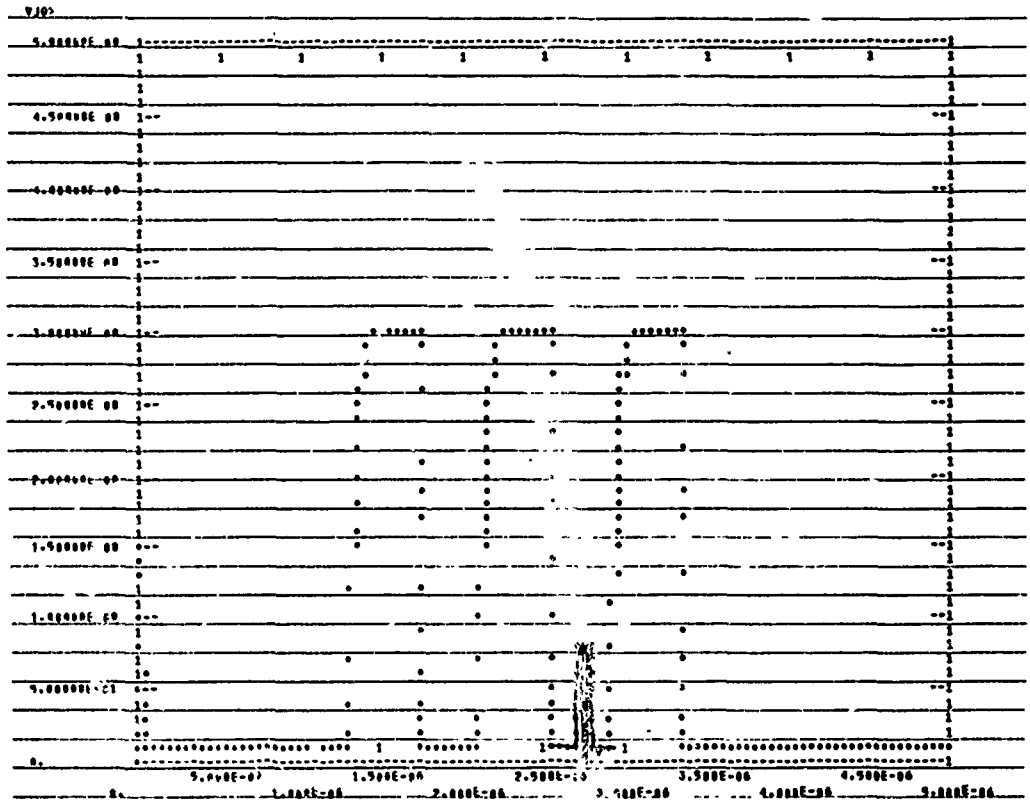


Figure VI-28. Q_2 - Response to Gamma Radiation

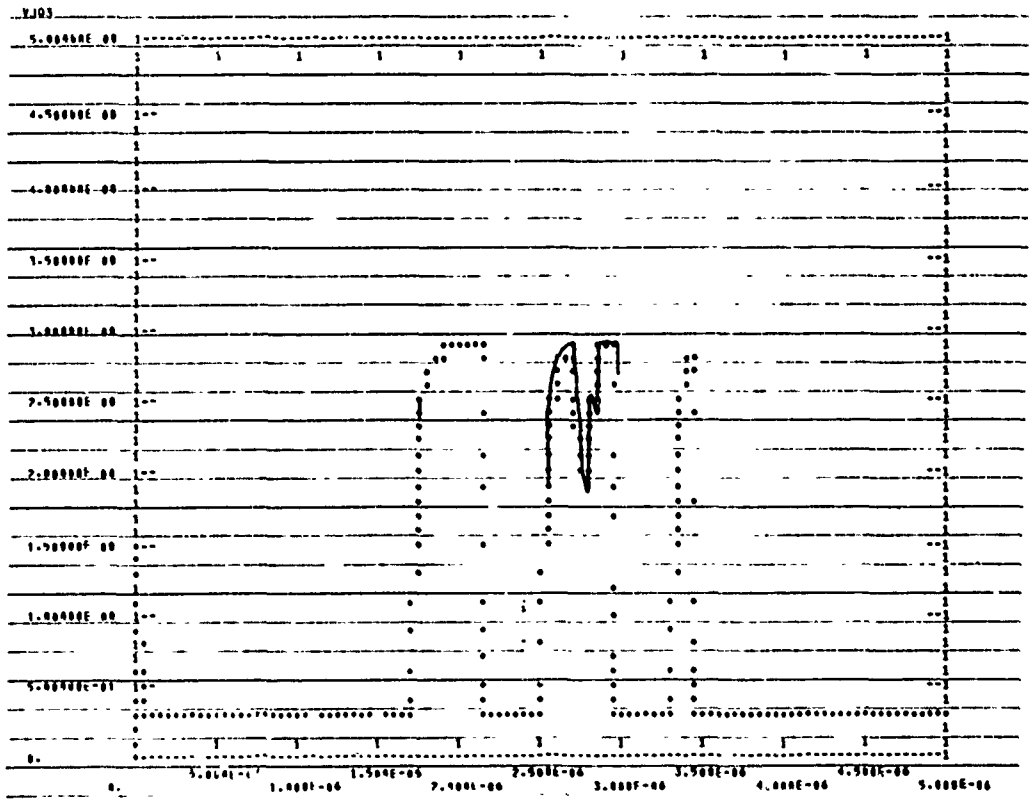


Figure VI-29. Q_3 - Response to Gamma Radiation

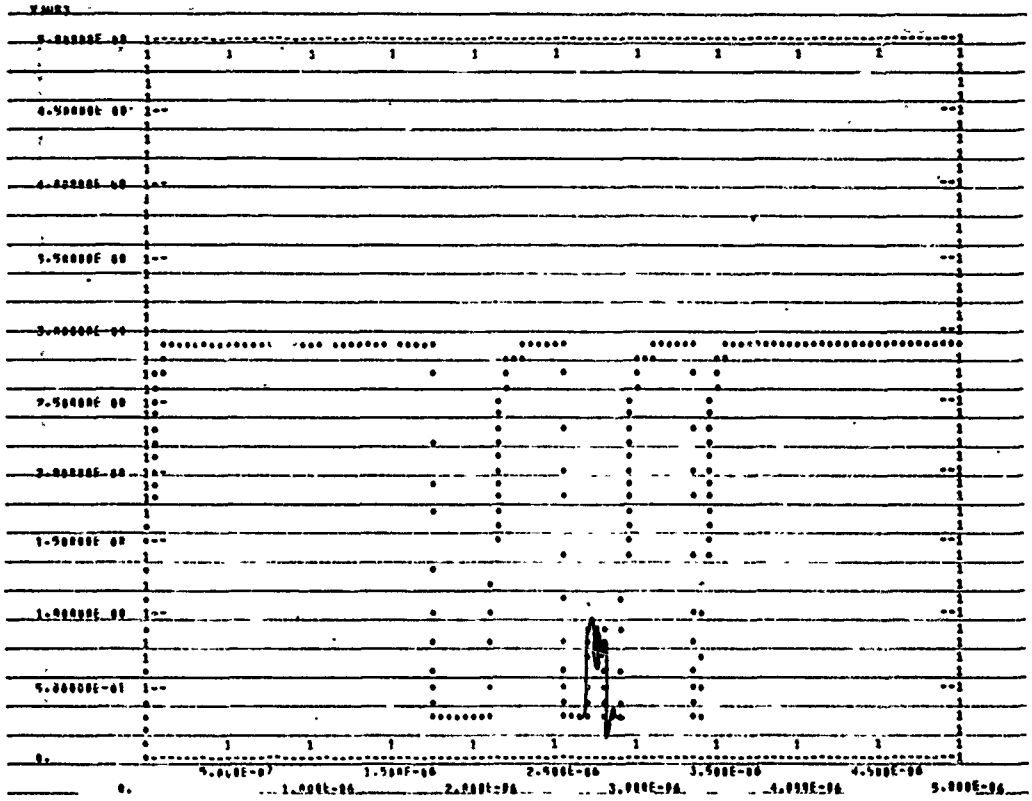


Figure VI-30. $\bar{Q}_3$ - Response to Gamma Radiation

```
MODEL 9/80 (RS-CK-J-K-Q0-Q1-Q2-Q3-QJR-0)
                4-BIT SHIFT REGISTER
                ELEMENTS
JRS,RS-0=0.
JCK,CK-0=0.
J,J-0=0.
JK,K-0=0.
E1,0-1=FJK(VJR2,P11,VJCK)
R1,1-2=100.
C1,2-0=FCAP(E1,VC1)
JR1,2-0=Q1(TABLE1(VC1),P6)
E2,0-4=FJK1(VJR1,VJRS,P12,VJCK)
R2,4-5=100.
C2,5-0=FCAP(E2,VC2)
JR2,5-0=0.
E3,0-3=X1(VJR1+P1)
R3,3-Q0=100.
E4,0-6=FJK(VJR4,P21,VJCK)
R4,6-7=100.
C4,7-0=FCAP(E4,VC4)
JR3,7-0=Q1(TABLE1(VC4),P6)
E5,0-9=FJK1(VJR3,VJRS,P22,VJCK)
R5,9-10=100.
C5,10-0=FCAP(E5,VC5)
JR4,10-0=0.
E6,0-8=X2(VJR3+P2)
R6,8-Q1=100.
E7,0-11=FJK(VJR6,P31,VJCK)
R7,11-12=100.
C7,12-0=FCAP(E7,VC7)
JR5,12-0=Q1(TABLE1(VC7),P6)
E8,0-14=FJK1(VJR5,VJRS,P32,VJCK)
R8,14-15=100.
C8,15-0=FCAP(E8,VC8)
JR6,15-0=0.
E9,0-13=X3(VJR5+P3)
R9,13-Q2=100.
E10,0-16=FJK(VJR8,P41,VJCK)
R10,16-17=100.
CA,17-0=FCAP(E10,VCA)
JR7,17-0=Q1(TABLE 1(VCA),P6)
E11,0-19=FJK1(VJR7,VJRS,P42,VJCK)
R11,19-20=100.
CB,20-0=FCAP(E11,VCB)
JR8,20-0=Q1(TABLE1(VCB),P6)
E12,0-18=X4(VJR7+P4)
R12,18-Q3=100.
E13,0-21=X5(VJR8+P5)
R13,21-QJR=100.
FUNCTIONS
Q1(A,B)=(A+B)
TABLE 1=0.,-.5,.3,-.8,1.,0.,2./.,5,3.,.8
                DEFINED PARAMETERS
P6=0.
P11=FJK2(P12,VJRS,VJ,VJR2,VJCK)
P12=FJK3(P11,VJK,VJR),VJCK)
P21=FJK2(P22,VJRS,F3,VJR4,VJCK)
P22=FJK3(P21,VJR2,VJR3,VJCK)
P31=FJK2(P32,VJRS,F6,VJR6,VJCK)
P32=FJK3(P31,VJR4,VJR5,VJCK)
P41=FJK2(P42,VJRS,F9,E13,VJCK)
P42=FJK3(P41,VJR6,E12,VJCK)
P1=0.,P2=0.,P3=0.,P4=0.,P5=0.
                OUTPUTS
VJR1,VJR2,PLOT
```

Figure VI-31. Computer Model Description With Both Gamma and Neutron Effects

As indicated in Figures VI-26 through VI-30. when the output signal is at a 0 level, the normal reaction is for the output to increase; for the condition when the output signal is at a 1 level, the output decreases.

Drawn on the figures are the observed laboratory results.

2. NEUTRON RADIATION

When the device is exposed to neutron radiation conditions, the performance may be degraded either temporarily or permanently. The degree of the degradation as well as the device recovery time, for those conditions which permit recovery, depends upon the exposure level.

The method for incorporating this effect into the model is also shown in Figure VI-31. The value of the input voltages, E3, E6, E9, E12 and E13, are changed from a simple dependency on the voltage across current sources to a dependency upon both the source voltage and the fluence level; the levels are identified as P1 through P5. In this instance, the radiation effects reduce the value of the voltage across the current sources by 0.4 volt when the output signal is at a 1 level and increase the voltage by 0.06 volt (Reference 2)* when the output is at a 0 level. The method for including these changes in signal level is shown on Figure VI-5 as function FNVT.

The computer description to produce an analysis of the device in the test circuit configuration is shown in Figure VI-32. To cause the neutron effects to be included in the analysis, model-defined parameters P1 through P5, which were originally set equal to zero, are made dependent upon the function FNVT. This is accomplished by changing the parameters P1 through P5 to be equal to P11 through P15 respectively. These latter parameters are seen to be dependent upon the radiation function.

The computer results of the analyses are shown in Figures VI-33 through VI-37. In each output it can be seen that the 1 signal level is reduced from that observed in Figures VI-20 through VI-24, and the 0 signal level is increased.

---

*Clemens, D. R., et al, Advanced Hardening Techniques for Complex Integrated Circuitry, AFAL-TR-71-139, Fairchild Camera and Instrument Co., August 1971

```
                    TIMING DELAY TEST
                    SAVED UNDER FILE 9780
                    ELEMENTS
F1,RS-C-J-K-Q0-Q1-Q2-Q3-QB3-0=MODEL 9780(CHANGEP1=P11,
 P2=P12,P3=P13,P4=P14,P5=P15)
FRS,0-RS=T1
  EC,0-C=FGEN(0.,3.,1.E-7,1.5E-8,2.E-7,1.5E-8,4.E-7,100.,TIME)
  EJ,0-J=T2
  EK,0-K=T3
  R1,03-A=4300.
  C1,03-A=2.E-12
  R2,A-0=750.
  C2,A-0=11.5E-12
  D1,03-5=MODEL 1N3605 (PERM)
  R5,5-7=600.
  EL,0-7=2.4
  R3,QB3-6=4300.
  C3,QB3-6=2.E-12
  R4,6-0=750.
  C4,6-0=11.5E-12
  D2,QB3-6=MODEL 1N3605 (PERM)
  R6,6-7=900.
  JQ0,Q0-0=0.
  JQ1,Q1-0=0.
  JQ2,Q2-0=0.
  JQ3,Q3-0=0.
  JQB3,QB3-0=0.
  DEFINED PARAMETERS
  P11=FNVI(VC1F1,0.4,0.06)
  P12=FNVI(VC4F1,0.4,0.06)
  P13=FNVI(VC7F1,0.4,0.06)
  P14=FNVI(VCAF1,0.4,0.06)
  P15=FNVI(VCBF1,0.4,0.06)
        FUNCTIONS
  T1=0.,3.,1.E-7,3.,1.15E-7,.1
  T2=0.,.1,1.5E-8,3.,4.E-7,3.,4.15E-7,.1
  T3=0.,.1,8.5E-7,.1,8.65E-7,3.,1.265E-6,3.,1.28E-6,.1
        OUTPUTS
  EC,EJ,EK,ERS,PLOT
  VJQ0,VJQ1,VJQ2,VJQ3,VJQB3,PLOT
        RUN CONTROLS
  MAXIMUM PRINT POINTS = 200
  COMPUTER TIME LIMIT = 5.5
  STOP TIME = 5000.E-9
  END
```

Figure VI-32. Neutron Radiation Test Circuit Description

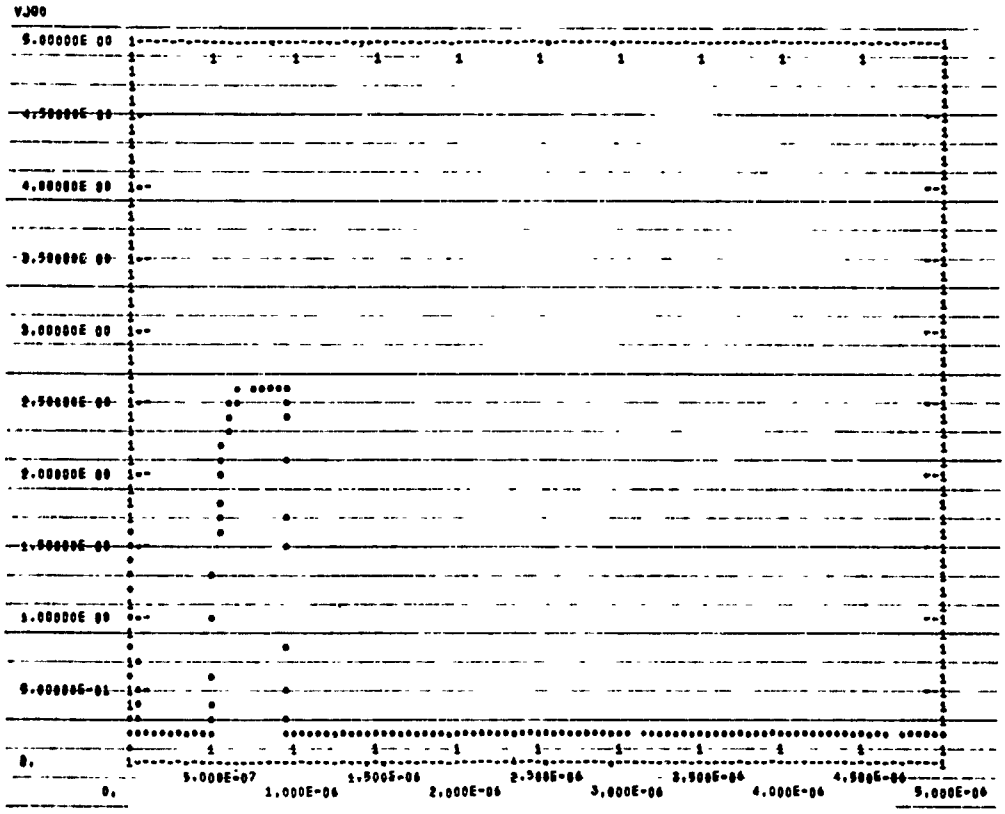


Figure VI-33. Q_0 - Response to Neutron Radiation

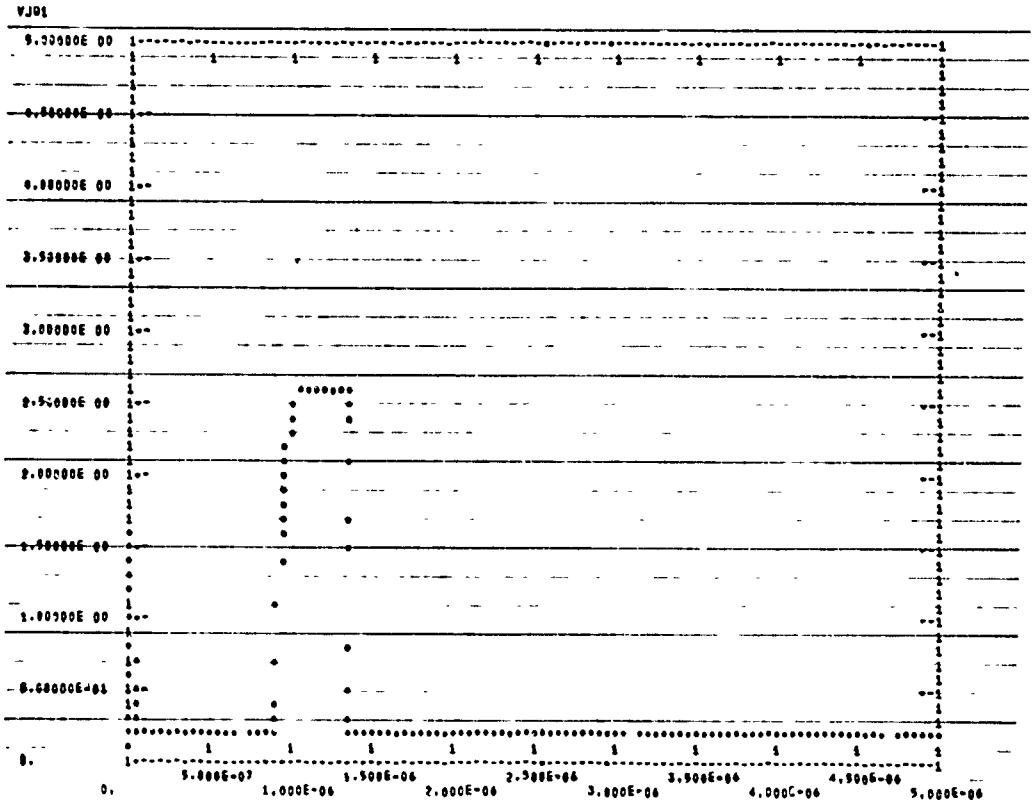


Figure VI-34. Q_1 - Response to Neutron Radiation

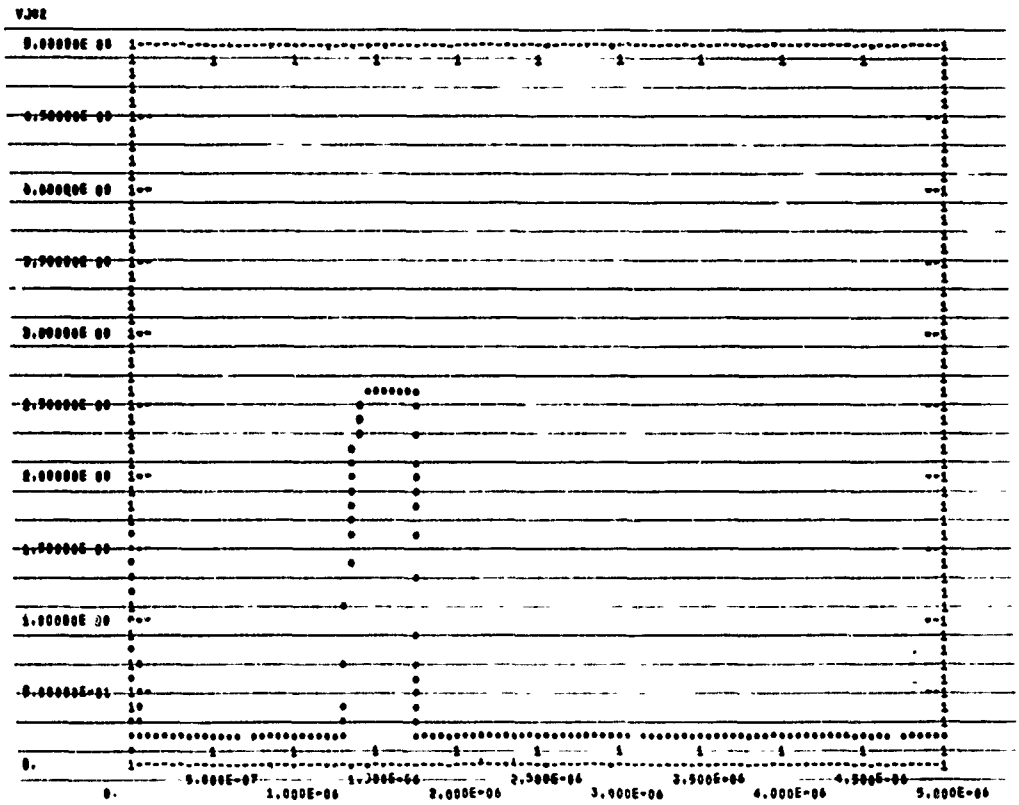


Figure VI-35. Q_2 - Response to Neutron Radiation

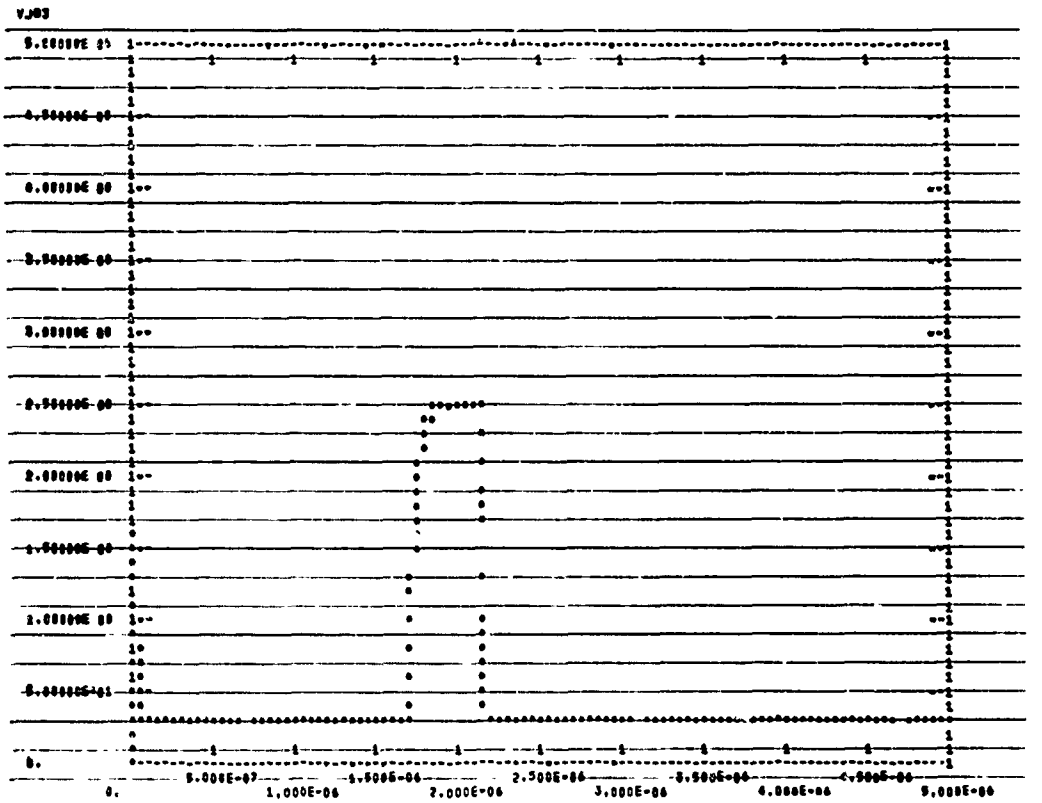


Figure VI-36. Q_3 - Response to Neutron Radiation

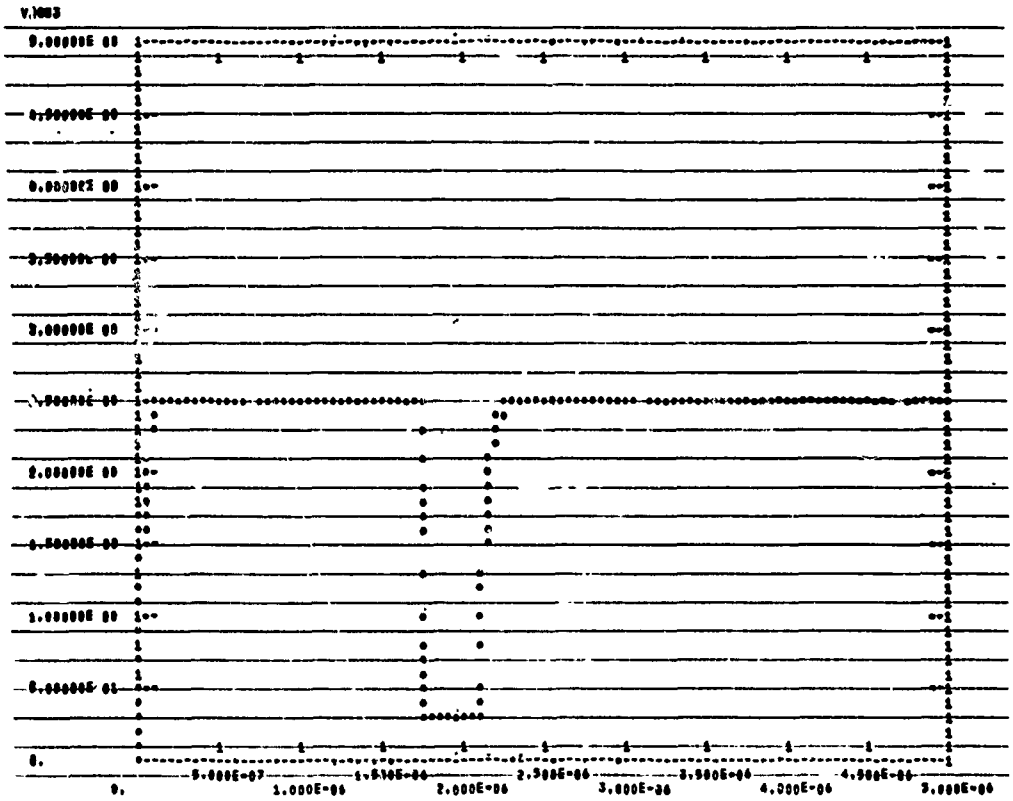


Figure VI-37. $\overline{Q}_3$ - Response to Neutron Radiation

SECTION VII

TEXAS INSTRUMENTS RSN54L122 MONOSTABLE MULTIVIBRATOR

The RSN54L122 monostable multivibrator features d-c triggering from positive or gated, negative-going inputs, with inhibit facility and an overriding reset. Both positive and negative-going output pulses are provided.

Pulse triggering occurs at a particular voltage level and therefore is not directly related to the transition time of the input pulse. Once fired, the outputs are independent of further signal transitions on the input terminals (function of the circuit timing components). With no external time controlling components (i.e., pin 9 connected to pin 14, pins 11, 13 open), a nominal output pulse of 800 nanoseconds duration is achieved which is independent of input pulse length.

The schematic diagram of the integrated circuit is shown in Figure VII-1 and the functional representation in Figure VII-2. The A1 and A2 terminals are negative-edge-triggered logic inputs, and will trigger the one shot when either or both go to logic 0, with B1 and B2 maintained at logic 1 levels. The B1 and B2 inputs are positive Schmitt-trigger inputs for slow rise time signals or level detection, and will trigger the one shot when either of the B signals goes to a logic 1, while the other B is at a logic 1 and either A1 or A2 at logic 0.

The truth table for the device as described by the manufacturer is shown in Table VII-1 for the condition when the reset signal levels are high (at level 1). The electrical characteristics for the device as defined by the manufacturer, are shown in Table VII-2.

A. MODEL DEVELOPMENT

The computer model that has been developed to duplicate observed (and/or manufacturer-published) performance is shown in Figure VII-3. The A inputs (A1, A2)*, B inputs (B1, B2)*, and reset (RS)* are defined as the input signals. The output signals are defined as Q (Q)* and $\overline{Q}$ (QB)*. The one shot pulse width is controlled by internal capacitor CF and resistors RF1 and RF2 when no external timing components are used (a short circuit connection is required between terminal VCC and TP1 Timing Pin #9). For variable pulse widths, an external resistor is connected between terminal VCC and TP2 (Timing Pin #11) and an external capacitor is connected between terminal TP2 and TP3 (Timing Pin #13).

Triggering of the one shot is performed by dependent voltage source EF. The state of EF is either "ON" or "OFF" depending on the function FSS which tests the inputs, A1, A2, B1 and B2, to establish compliance with the truth table. When a valid set of input signals is present, EF is set to 3.0 volts. This level charges the timing capacitor through the resistor, RFF, which behaves like a diode, having a value of 1 ohm when EF equal 3 volts and an 1×10^{20} ohms impedance when EF equals 0 volt.

*As described to the computer.

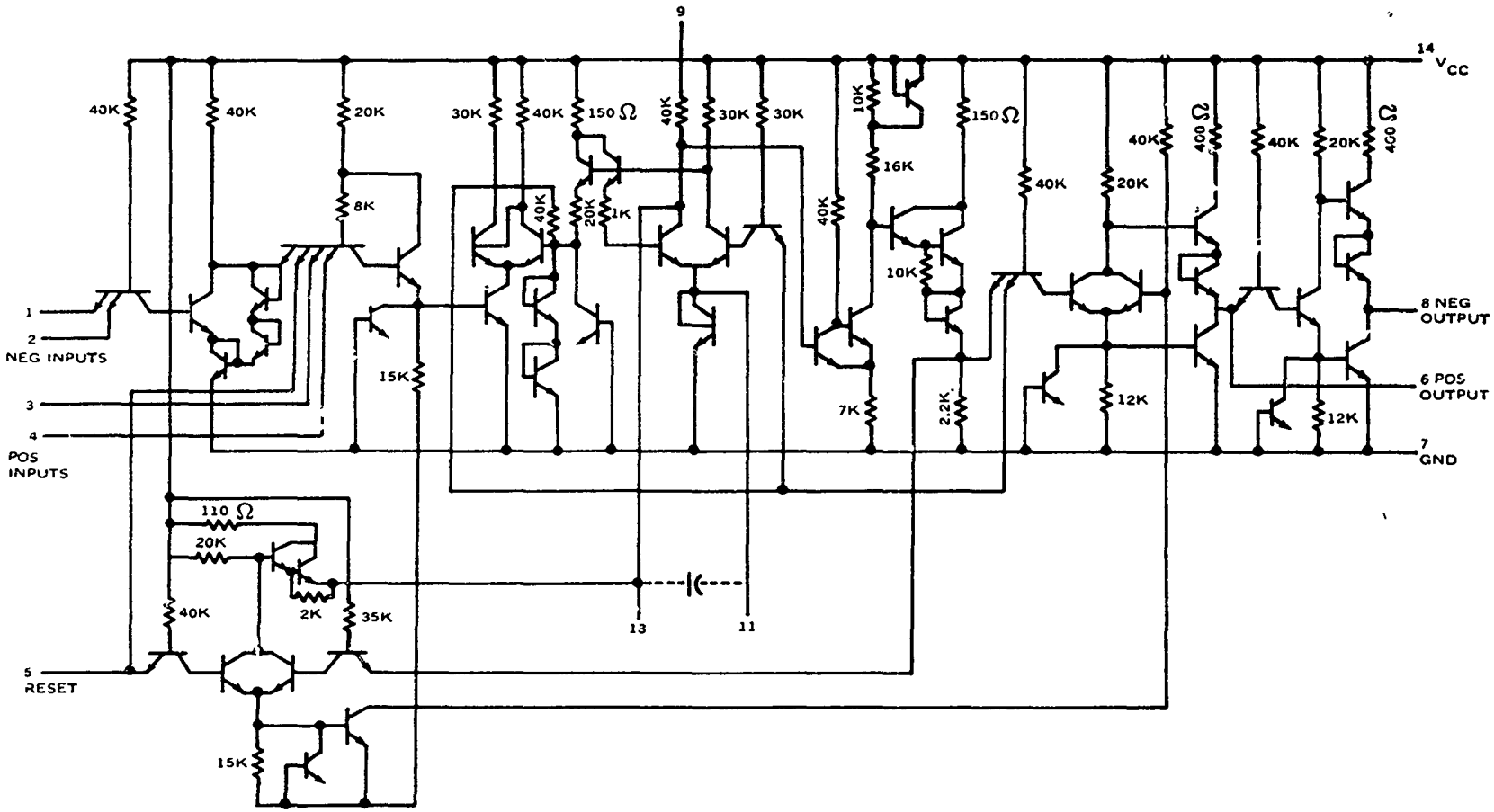


Figure VII-1. Schematic RSN54L122 One-Shot

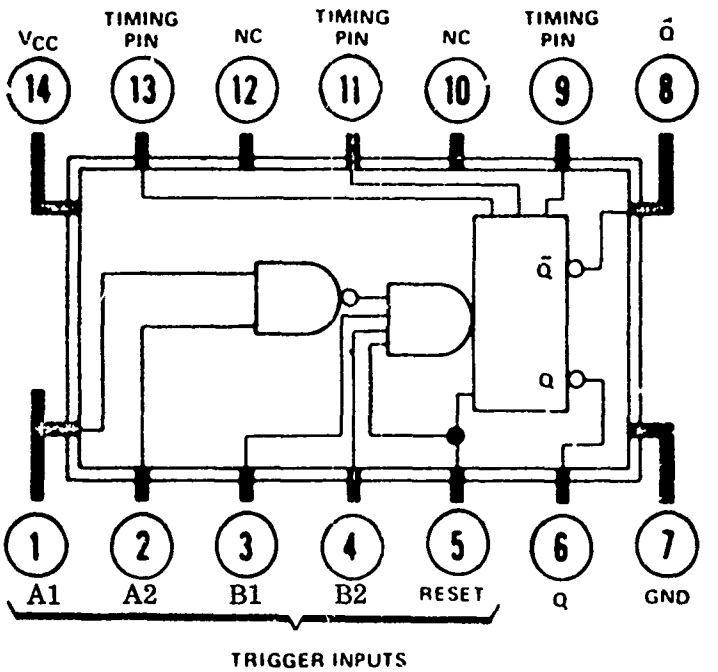


Figure VII-2. Logic Diagram

TABLE VII-1.

TRUTH TABLE

INPUT				OUTPUT	
A1	A2	B1	B2	Q	$\bar{Q}$
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⎍	⎎
L	X	H	↑	⎍	⎎
X	L	H	H	L	H
X	L	↑	H	⎍	⎎
X	L	H	↑	⎍	⎎
H	↓	H	H	⎍	⎎
↓	↓	H	H	⎍	⎎
↓	H	H	H	⎍	⎎

H = high level
L = low level
↑ = transition from low to high level
↓ = transition from high to low level
⎍ = one high level pulse
⎎ = one low level pulse
X = any input including transition

TABLE VII-2.

ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range, unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at any input terminal	$V_{CC} = 4.5V$	1.9			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal	$V_{CC} = 4.5V$			0.8	V
$V_{out(1)}$	Logical 1 output voltage at positive or negative output with logical 1 level at positive or negative input terminal respectively.	$V_{CC} = 4.5V$ $V_{in} = 1.9V$ $I_{load} = -100\ \mu A$, N = 0	2.4			V
$V_{out(0)}$	Logical 0 output voltage at positive or negative output with logical 0 at positive or negative input respectively.	$V_{CC} = 4.5V$ $V_{in} = 0.8V$ $I_{sink} = 2$ mA			0.3	V
$I_{in(0)}$	Logical 0 level input current	$V_{CC} = 5.5V$ $V_{in} = 0.3V$			-0.18	mA
$I_{in(0)}$	Logical 0 level reset current	$V_{CC} = 5.5V$ $V_{in} = 0.3V$			-0.38	mA
$I_{in(1)}$	Logical 1 level input current	$V_{CC} = 5.5V$ $V_{in} = 2.4V$ $V_{CC} = 5.5V$ $V_{in} = 5.5V$			10 0.10	μA mA
$I_{in(1)}$	Logical 1 level reset current	$V_{CC} = 5.5V$ $V_{in} = 2.4V$ $V_{CC} = 5.5V$ $V_{in} = 5.5V$			20	μA
I_{OS}	Short-circuit output current	$V_{CC} = 5.5V$	1		-15	mA
I_{CC}	Quiescent power supply drain	$V_{CC} = 5.5V$		3.5		mA
t_{pd}	Negative trigger input to negative output	$V_{CC} = 5.0V$ Connect Load = 15 pF, V_{CC} to $R_{in_t} = 40\ k\Omega$ Pin 9			300	ns
$t_{pw\ (min)}$	Minimum true output pulse width	$V_{CC} = 5.0V$, V_{CC} Load = 15 pF, to Pin 9 $R_{in_t} = 40\ k\Omega$		800		ns

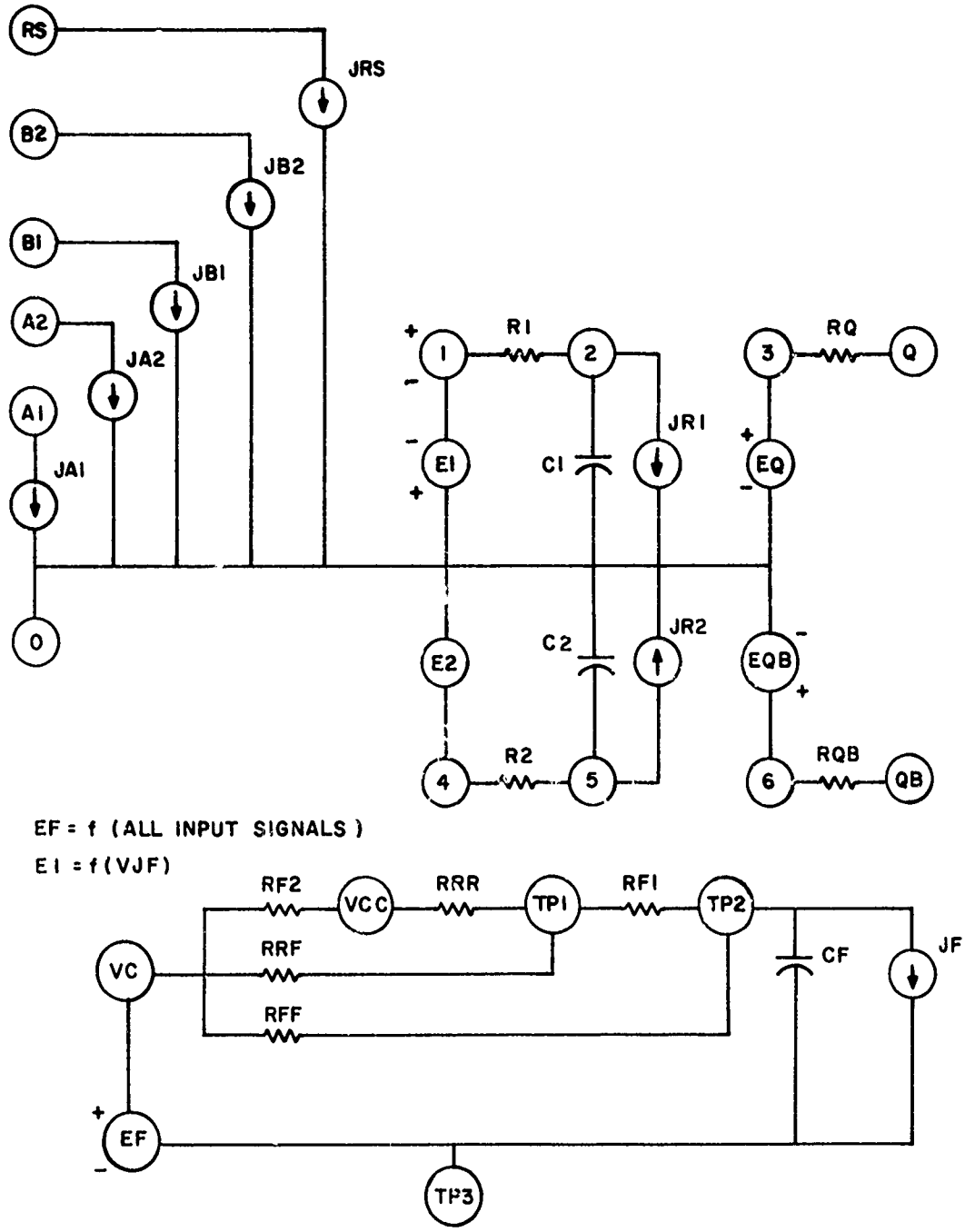


Figure VII-3. Model RSN54L122

When this latter condition exists, the timing capacitor discharges through the timing resistors RF1 and RF2. The internal resistance circuit is in two parts; one part (RF1) is always in series with CF, while the other part (RF2) is used only when terminal VCC is shorted to terminal TP1. The two are necessary to provide agreement between computer and lab results for both internal and external timing configurations. The resistors RRR and RRF were added to overcome SCEPTRE program problems for those situations where EF is dependent upon itself.

The dependent voltage source E1 is high (3 volts) when the voltage across CF is greater than 1.5 volts; E2 is always the complement of E1. The Q and $\overline{Q}$ delays computed in function FCAP are controlled by time constants R1 - C1 and R2 - C2 for Q and $\overline{Q}$ respectively. The function tests for a rising or falling voltage across C1 or C2 and selects the appropriate linear capacitor equation which is dependent upon the voltage across the capacitor. The dependent current sources, JR1 and JR2, allow the program to produce normal electrical performance analyses under d-c conditions and also act as sources of radiation signal injection when required. The dependent voltage sources, EQ and EQB, isolate the frequency sensitive RC circuits from the effects of external circuit loading. RQ and RQB represent the output impedance of the device.

The RSN54L122 model listing, as described to the computer, is shown in Figure VII-4. The subprogram to establish the trigger EF, the E1 signal levels, the capacitance for the delay characteristics, and the neutron radiation response is shown in Figure VII-5. The FORTRAN flow charts associated with these functions are shown in Appendix VII-A.

```
MODEL RSN54L122 (A1-A2-B1-B2-RS-VCC-TP1-TP2-TP3-Q-QB-0)
      MONOSTABLE MULTIVIBRATOR
      ELEMENTS
JA1,A1-0=0.
JA2,A2-0=0.
JB1,B1-0=0.
JB2,B2-0=0.
JRS,RS-0=0.
EF,TP3-VC=FIN(VJA1,VJA2,VJB1,VJB2,TIME,EF,VJRS)
RRF,VC-TP1=1.E20
RF1,TP1-TP2=33.E3
RF2,VC-VCC=7.E3
RRR,VCC-TP1=1.E20
RFF,VC-TP2=11(EF)
CF,TP2-TP3=25.E-12
JF,TP2-TP3=0.
E1,0-1=FSS(VJF,VJRS)
R1,1-2=1000.
C1,2-0=FCAP(E1,VC1)
JR1,2-0=0.
EQ,0-3=X1(VJR1)
RQ,3-Q=100.
E2,0-4=X2(3.1-E1)
R2,4-5=1000.
C2,5-0=FCAP(E2,VC2)
JR2,5-0=0.
EQB,0-6=X3(VJR2)
RQB,6-QB=100.
      FUNCTIONS
T1=0.,1.E20,.8,1.E20,2.,10.,3.,10.
      OUTPUTS
VJF,PLOT
```

Figure VII-4. Computer Model Description

```
      C     MODEL RSN54L122 MONOSTABLE MULTIVIBRATOR SUBPROGRAM
      C
            FUNCTION FSS(VF,RS)
      C
            FSS=0.1
            IF(VF.GT.1.5) FSS=3.0
            IF(RS.LT.1.5) FSS=0.1
            RETURN
      C
            ENTRY FIN(A1,A2,B1,B2,TIME,XFIN,RS)
      C
            IF(TIME.LE.0..OR.RS.LE.1.5) GO TO 40
            IF(TIME.LE.XTIME) GO TO 60
            DA1=A1-XA1
            DA2=A2-XA2
            DB1=B1-XB1
            DB2=B2-XB2
            IF((A1.LE.1.5.AND.ABS(DA1).LE.0.1).OR.(A2.LE.1.5.AND.
           *ABS(DA2).LE.0.1)) GO TO 20
            GO TO 25
       20   IF((DB1.GT.0..AND.B1.GT.1.3.AND.B1.LT.1.7.AND.B2.GT.1.5).OR.
           *(B1.GE.1.5.AND.DB2.GT.0..AND.B2.GT.1.3.AND.B2.LT.1.7)) GO TO 35
       25   IF((B1.GE.1.5.AND.ABS(DB1).LE.0.1).AND.(B2.GE.1.5.
           *AND.ABS(DB2).LE.0.1)) GO TO 30
            GO TO 40
       30   IF((A1.GE.1.5.AND.ABS(DA1).LE.0.1).AND.(DA2.LT.0..AND.A2.GT.
           *1.3.AND.A2.LT.1.7)) GO TO 35
            IF((DA1.LT.0..AND.A1.GT.1.3.AND.A1.LT.1.7).AND.(A2.GE.1.5
           *.AND.ABS(DA2).LE.0.1)) GO TO 35
            IF(DA1.LT.0..AND.A1.GT.1.3.AND.A1.LT.1.7.AND.DA2.LT.0..AND.
           *A2.GT.1.3.AND.A2.LT.1.7) GO TO 35
            GO TO 40
       35   FSS=3.0
            GO TO 50
       40   FSS=0.1
       50   XTIME=TIME
            XA1=A1
            XA2=A2
            XB1=B1
            XB2=B2
            RETURN
       60   FSS=XFIN
            RETURN
      C
            ENTRY FCAP(VGEN,VCAP)
      C
            IF(VGEN-VCAP) 100,110,110
      110   FSS=-100.E-12*VCAP/3.+130.E-12
            RETURN
      100   FSS=35.E-12*VCAP/3.+5.E-12
            RETURN
            ENTRY FNVT(A,B,C)
      C     SUBPROGRAM FOR NEUTRON BEHAVIOR
            IF(A-1.5)140,150,160
      140   Y=C
            GO TO 1500
      150   Y=.1
            GO TO 1500
      700   Y=0.05
            GO TO 1500
      160   IF(A.LE.2.)GO TO 700
            IF(A.LT.2.3)GO TO 800
            IF(A.LT.2.5)GO TO 1000
            IF(A.LT.2.7)GO TO 900
            IF(A.LT.2.8)GO TO 1100
            Y=-B
            GO TO 1500
      800   Y=-0.05
            GO TO 1500
      900   Y=-0.15
            GO TO 1500
     1000   Y=-0.1
            GO TO 1500
     1100   Y=-0.25
     1500   FSS=Y
            RETURN
            END

  23621 WORDS OF MEMORY USED BY THIS COMPILATION
```

Figure VII-5. Model Subprogram

B. MODEL VERIFICATION

The circuit shown in Figure VII-6 was described to the computer to demonstrate the performance of the single shot with no external timing components.

The topological description for the SCEPTRE circuit analysis program to test for the condition of triggering on a rising input signal, is shown in Figure VII-7. The A1 and A2 inputs are held at 0.1 volt, the B2 input at 3.1 volts, and the RS and B1 inputs are shown in Figures VII-8 and VII-9, respectively. Figure VII-10 (the Q output) and Figure VII-11 (the $\overline{Q}$ output) show the circuit response to these input signals. The results verify the model capability of being triggered by a rising input signal and immunity to retriggering by the falling edge of the pulse. The computer model pulse width between the 1.5 volt levels shown in Figure VII-10 is approximately 700 nanoseconds. The manufacturer's data sheet (Table VII-2) shows a typical pulse width of 800 nanoseconds.

The same circuit as shown in Figure VII-6 was described to the computer to demonstrate that the model, with no external timing components, would trigger on the falling edge of an input pulse at Terminal A1. The topological description for the SCEPTRE circuit analysis program is shown in Figure VII-12. For this condition the input signals A2, B1 and B2 are held at 3.1 volts while the pulse EA1, shown in Figure VII-13, is applied to the A1 input. The resulting outputs, Q and $\overline{Q}$, are shown in Figures VII-14 and VII-15 respectively, and verify the inhibit function for the leading edge of EA1 and the triggering action on the falling edge of the pulse. The pulse width is seen to be approximately 700 nanoseconds.

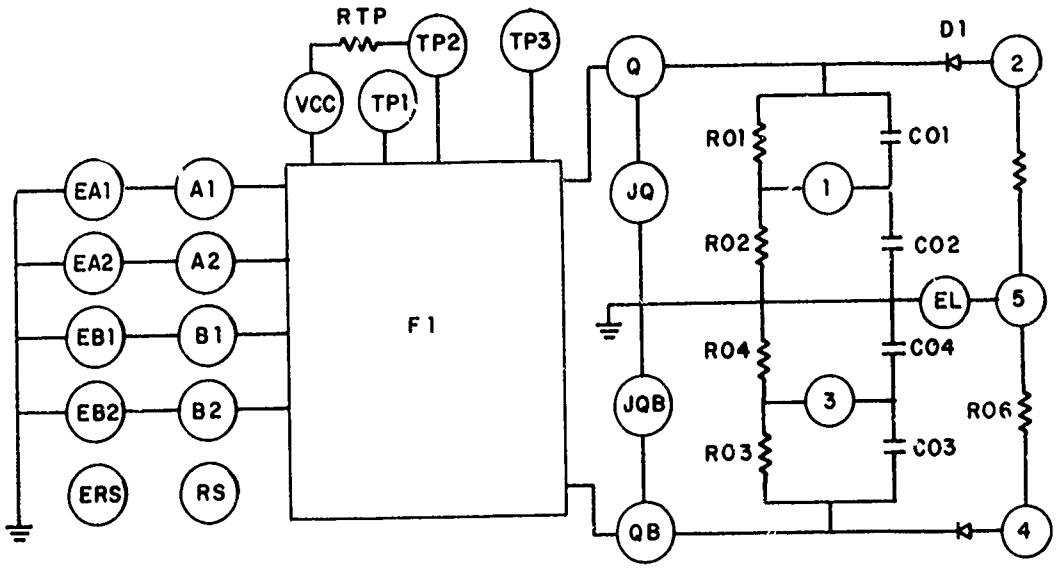


Figure VII-6. Test Circuit

```
                    SAVED UNDER FILE RSNL122
                    TEST CONDITION 6
                    PULSE WIDTH TEST - NO EXTERNAL TIMING COMPONENTS
                    TRIG ON LEADING EDGE OF INPUT PULSE
        ELEMENTS
F1,A1-A2-B1-B2-RS-VCC-TP1-TP2-TP3-Q-QB-0=MODEL RSN54L122
ERS,0-RS=T1
EA1,0-A1=0.1
EA2,0-A2=0.1
EB1,0-B1=PIN
EB2,0-B2=3.1
RIP,VCC-TP1=1.
JQ,Q-0=0.
JQB,QB-0=0.
R01,Q-1=4300
C01,Q-1=2.E-12
R02,1-0=750.
C02,1-0=11.5E-12
R03,QB-3=4300.
C03,QB-3=2.E-12
R04,3-0=750.
C04,3-0=11.5E-12
D1,0-2=MODEL 1N3605 (PERM)
R05,2-5=800.
D2,QB-4=MODEL 1N3605 (PERM)
R06,4-5=800.
EL,0-5=2.4
        DEFINED PARAMETERS
PIN=FGEN(0.,3.,1.E-7,15.E-9,1.6E-7,15.E-9,9.E-7,10.,TIME)
        FUNCTIONS
T1=0.,.1,50.E-9,.1,65.E-9,3.,5.E-7,3.
        OUTPUTS
EA1,EA2,EB1,EB2,ERS,VJQ,VJQB,PLOT
XSTPSZ,PLOT
        RUN CONTROLS
START TIME = 0.
STOP TIME = 1.E-6
MINIMUM STEP SIZE = 1.E-18
MAXIMUM STEP SIZE=5.E-9
MAXIMUM PRINT POINTS = 100
COMPUTER TIME LIMIT = 5.5
END
```

Figure VII-7. Test Circuit Description - Leading Edge Trigger

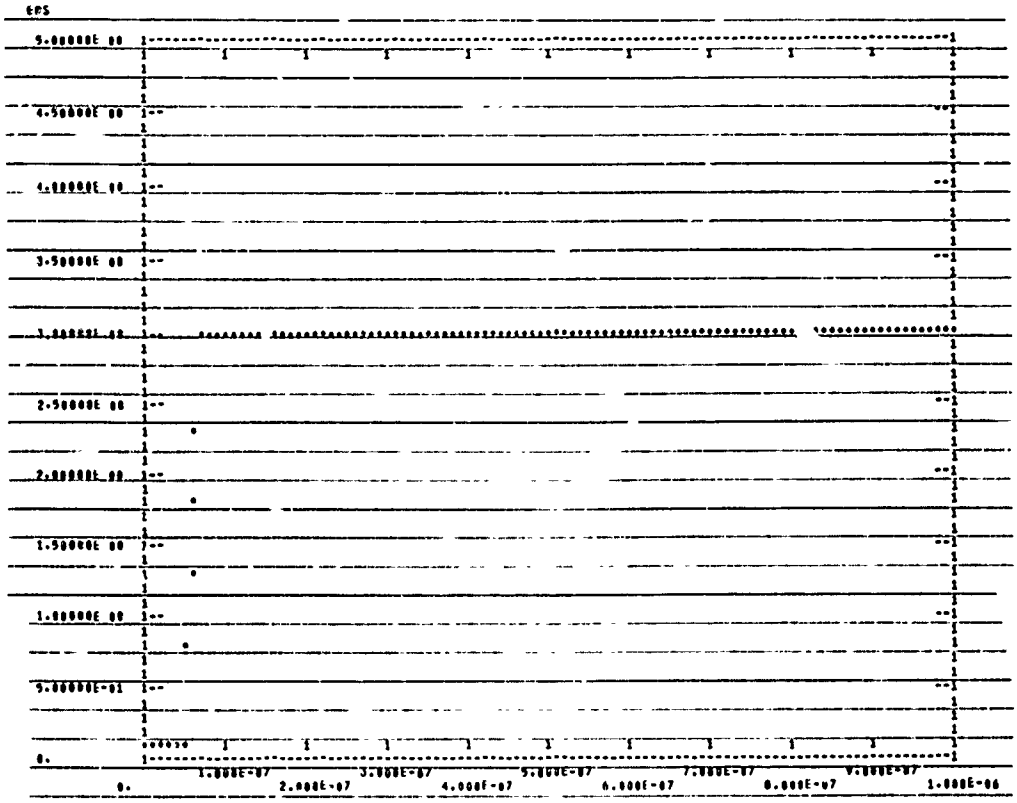


Figure VII-8. RESET Input Signal

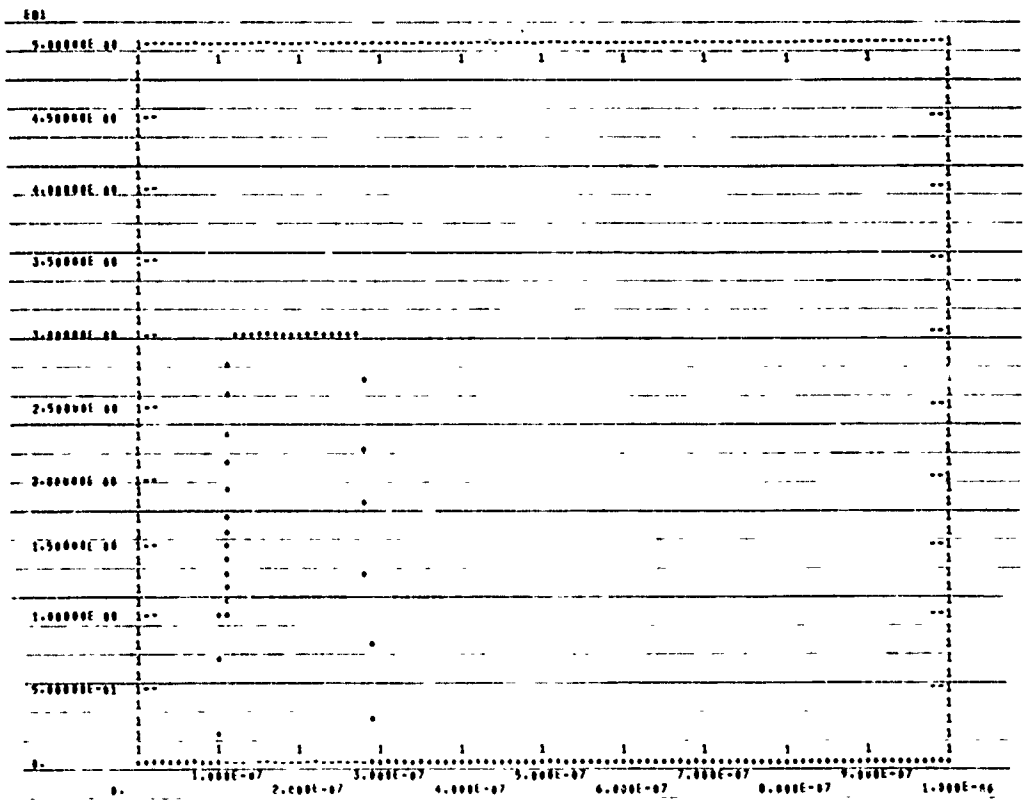


Figure VII-9. B1 Input Signal

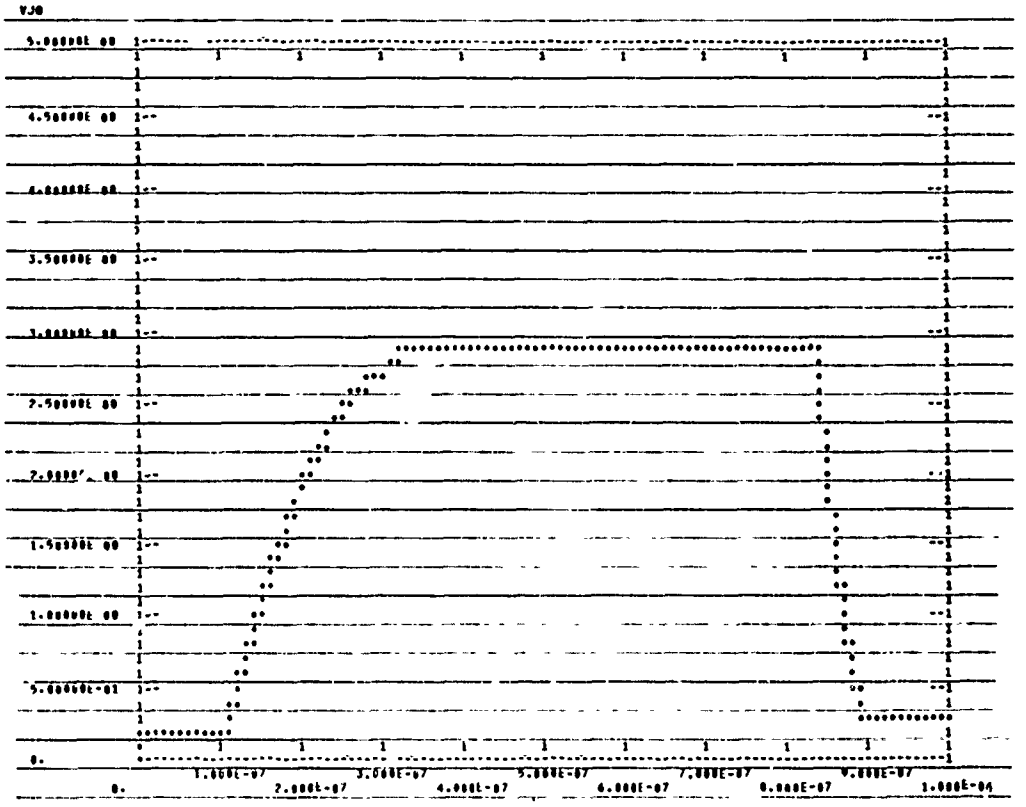


Figure VII-10. Q - Output

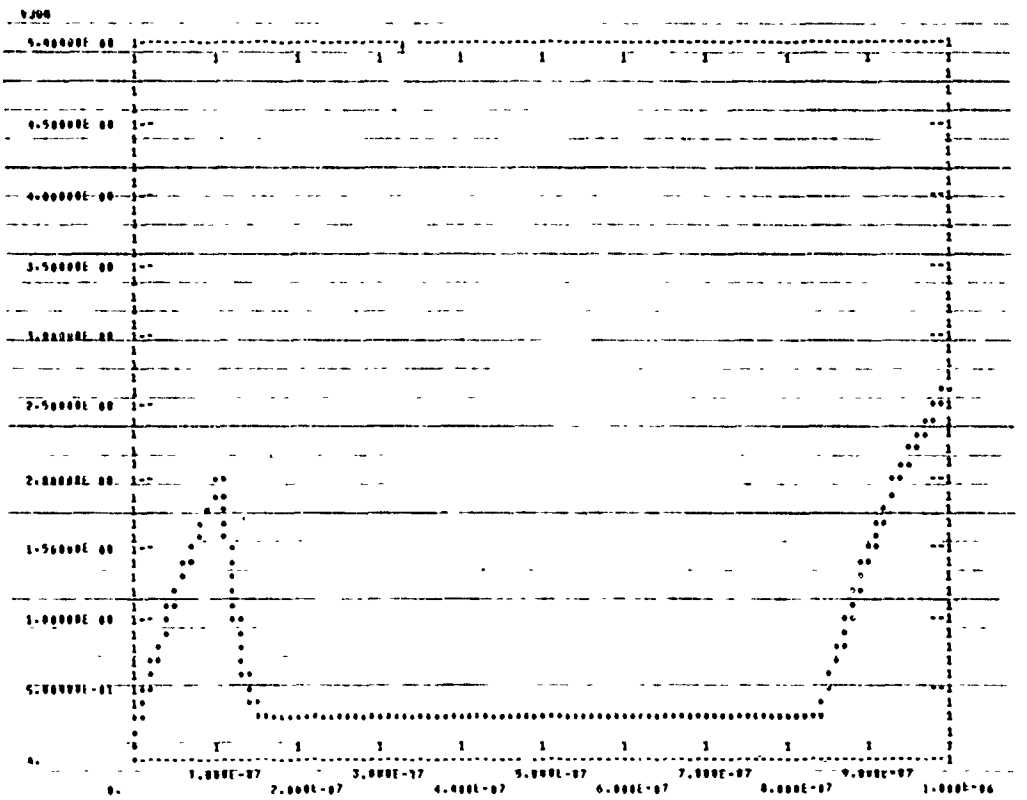


Figure VII-11. $\overline{Q}$ - Output

```
                    SAVED UNDER FILE RSNL122
                    TEST CONDITION 5
                    NO EXTERNAL TIMING COMPONENTS
        ELEMENTS
F1,A1-A2-B1-B2-RS-VCC-TP1-TP2-TP3-Q-QB-0=MODEL RSN54L122
ERS,0-RS=T1
EA1,0-A1=PIN
EA2,0-A2=3.1
EB1,0-B1=3.1
EB2,0-B2=3.1
RTP,VCC-TP1=1.
JQ,Q-0=0.
JQB,QB-0=0.
R01,Q-1=4300
C01,Q-1=2.E-12
R02,1-0=750.
C02,1-0=11.5E-12
R03,QB-3=4300.
C03,QB-3=2.E-12
R04,3-0=750.
C04,3-0=11.5E-12
D1,Q-2=MODEL 1N3605 (PERM)
R05,2-5=800.
D2,QB-4=MODEL 1N3605 (PERM)
R06,4-5=800.
EL,0-5=2.4
        DEFINED PARAMETERS
PIN=FGEN(0.,3.,1.E-7,15.E-9,1.6E-7,15.E-9,2.E-6,5.,TIME)
PNVT1=FNVT(VC1F1,0.4,0.2)
PNVT2=FNVT(VC2F1,0.4,0.2)
        FUNCTIONS
T1=0.,.1,50.E-9,.1,65.E-9.3.,5.E-7,3.
        OUTPUTS
EA1,EA2,EB1,EB2,ERS,VJQ,VJQB,PLOT
XSTPSZ,PLOT
        RUN CONTROLS
START TIME = 0.
STOP TIME =2.E-6
MINIMUM STEP SIZE = 1.E-18
MAXIMUM STEP SIZE=5.E-9
MAXIMUM PRINT POINTS = 100
COMPUTER TIME LIMIT = 5.5
END
```

Figure VII-12. Test Circuit Description - Falling Edge Trigger

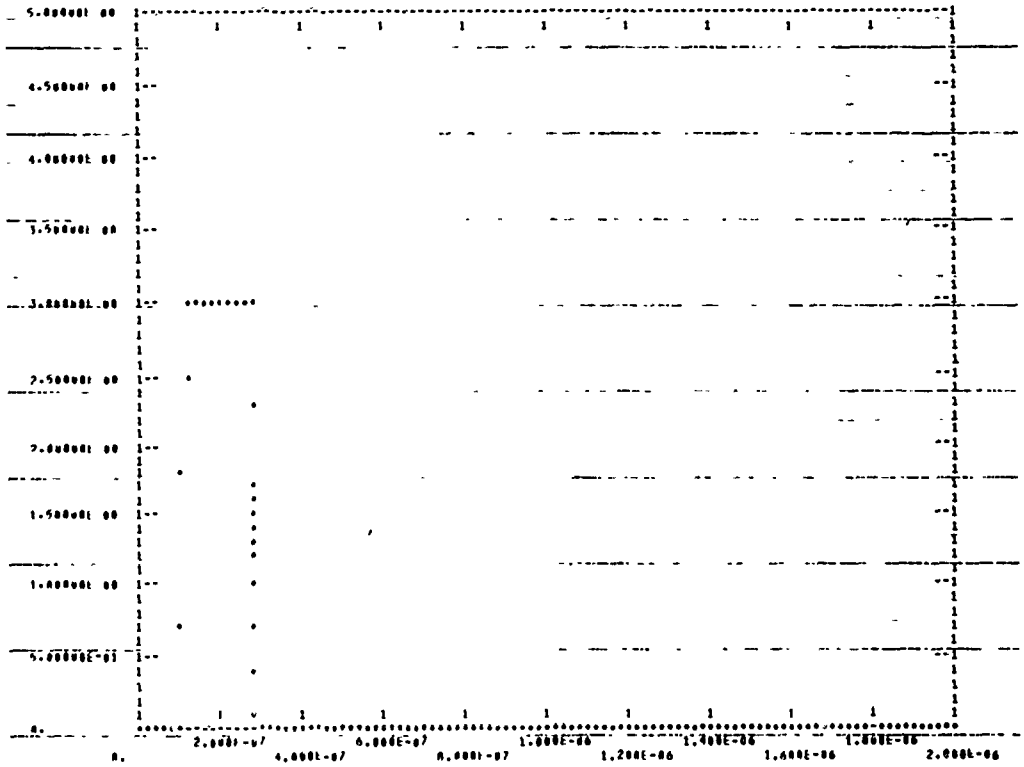


Figure VII-13. A1 Input Signal

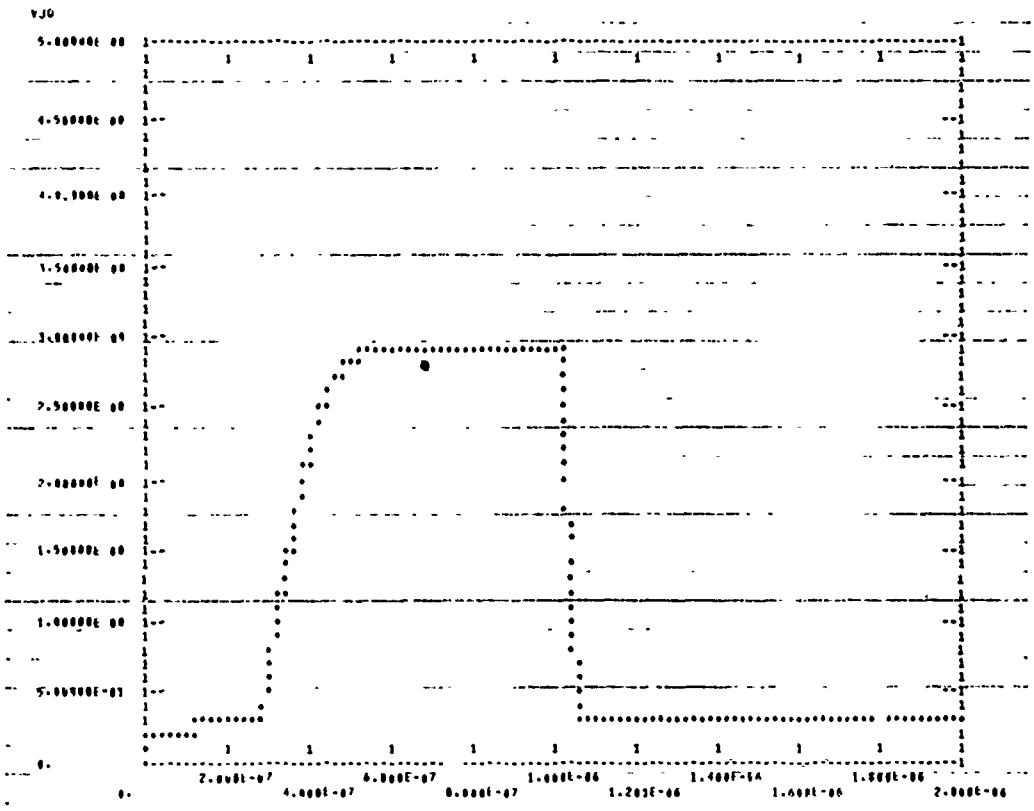


Figure VII-14. Q - Output

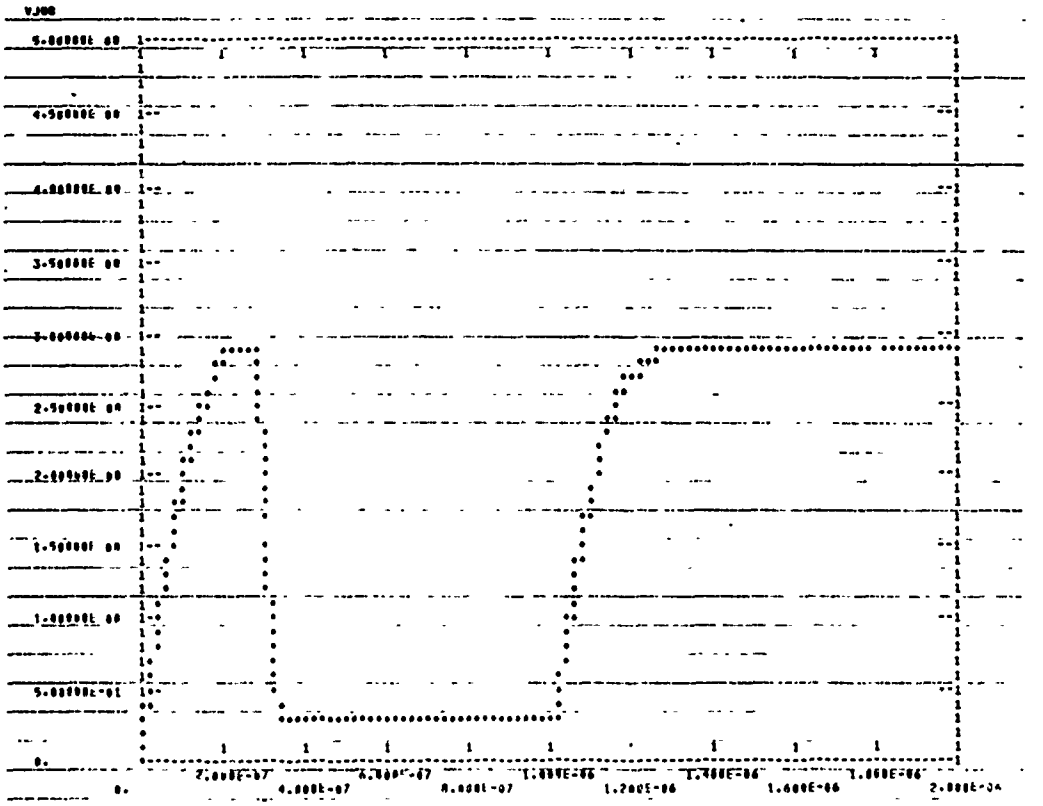


Figure VII-15. $\overline{Q}$ - Output

The circuit shown in Figure VII-16 was described to the computer to demonstrate the performance of the single shot to trigger on the falling edge of a pulse when the device is used with external timing components. The timing components were chosen to decrease the pulse width to assure agreement with laboratory results.

The topological description for the SCEPTRE circuit analysis program is shown in Figure VII-17. The A2, B1 and B2 inputs are held at 3.1 volts and the RS and A1 inputs are as shown in Figures VII-8 and VII-18, respectively.

Figures VII-19 and VII-20 show the circuit response to these input signals; Figure VII-19 shows the Q output, and Figure VII-20 the $\overline{Q}$ output. The results verify the capability of the model to be triggered by a falling edge input signal at the A1 input and inhibited from being retriggered prematurely by the rising edge of the A1 pulse. The computer model pulse width between 1.5 volt levels shown in Figure VII-15 is approximately 250 nanoseconds. Laboratory measurements with RTP = 2K Ω and CTP = 20 pf provided pulse widths of 280 nanoseconds.

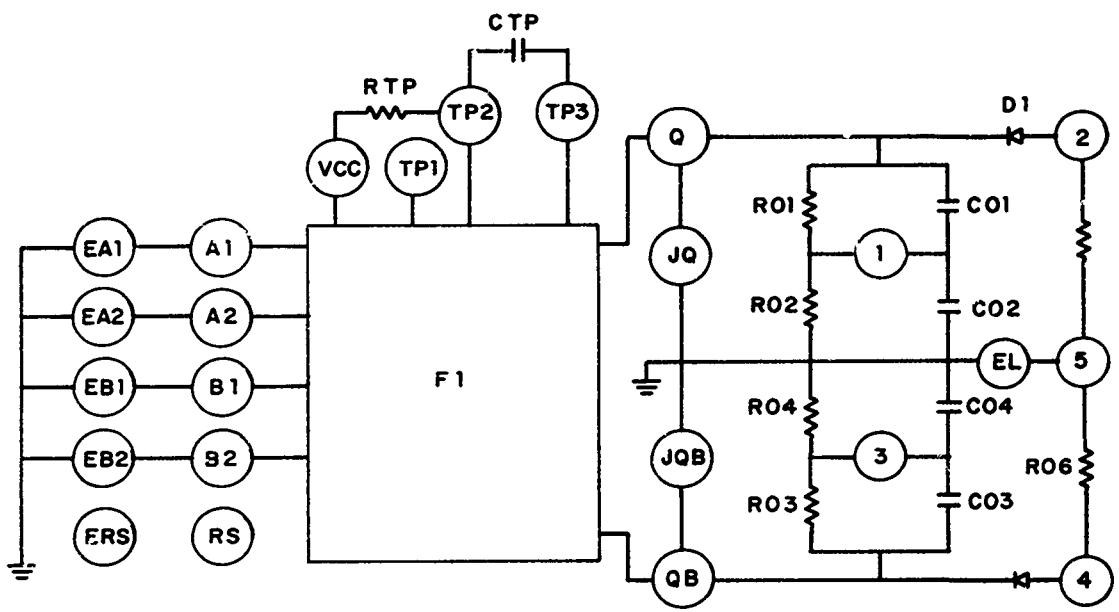


Figure VII-16. Test Circuit - With External Timing Components

```
                SAVED UNDER FILE RSNL122
                TEST CONDITION-6
                PULSE WIDTH TEST - EXTERNAL RC TIMING COMPONENTS
                TRIG ON FALLING EDGE OF INPUT PULSE
        ELEMENTS
F1,A1-A2-B1-B2-RS-VCC-TP1-TP2-TP3-Q-QB-0,MODEL RSN54L122
ERS,0-RS=T1
EA1,0-A1=PIN
EA2,0-A2=3,1
EB1,0-B1=3,1
EB2,0-B2=3,1
RTP,VCC-TP2=2,E3
CTP,TP2-TP3=20,E-12
JQ,Q-0=0,
JQB,QB-0=0,
RO1,Q-1=4300
CO1,Q-1=2,E-12
RO2,1-0=750,
CO2,1-0=11,5E-12
RO3,QB-3=4300,
CO3,QB-3=2,E-12
RO4,3-0=750,
CO4,3-0=11,5E-12
D1,Q-2=MODEL 1N3605 (PERM)
RO5,2-5=800,
D2,QB-4=MODEL 1N3605 (PERM)
RO6,4-5=800,
EL,0-5=2,4
        DEFINED PARAMETERS
PIN=FGEN(0.,3.,1,E-7,15,E-9,1,6E-7,15,E-9,9,E-7,10.,TIME)
        FUNCTIONS
T1=0.,.1,50,E-9,.1,65,E-9,3.,5,E-7,3.
        OUTPUTS
EA1,EA2,EB1,EB2,ERS,VJQ,VJQB,PLOT
XSTPSZ,PLOT
        RUN CONTROLS
START TIME = 0,
STOP TIME = 1,E-6
MINIMUM STEP SIZE = 1,E-18
MAXIMUM STEP SIZE=5,E-9
MAXIMUM PRINT POINTS = 100
COMPUTER TIME LIMIT = 5,5
END
```

Figure VII-17. Test Circuit Description

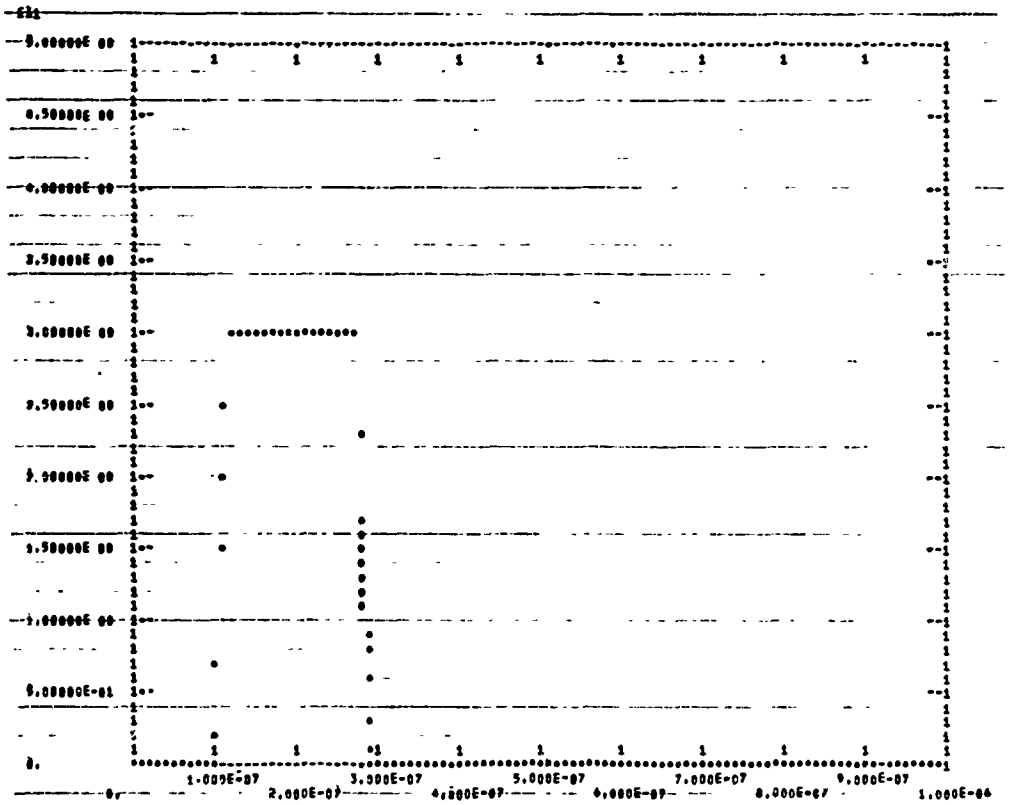


Figure VII-18. A1 Input Signal

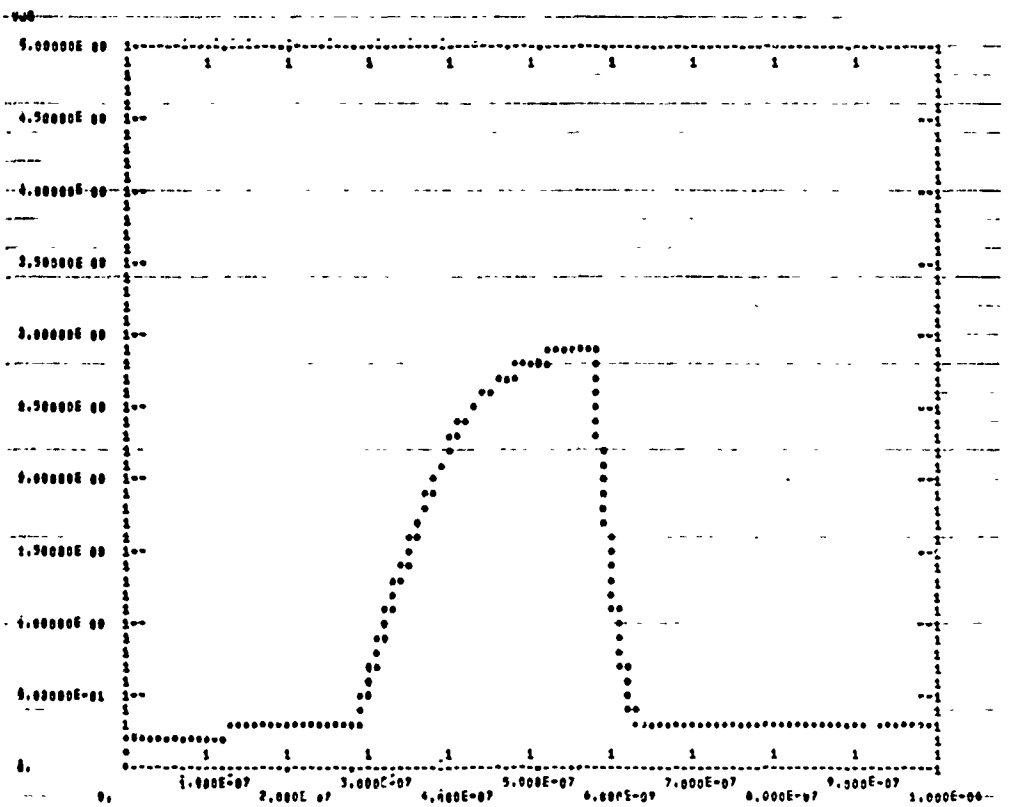


Figure VII-19. Q - Output

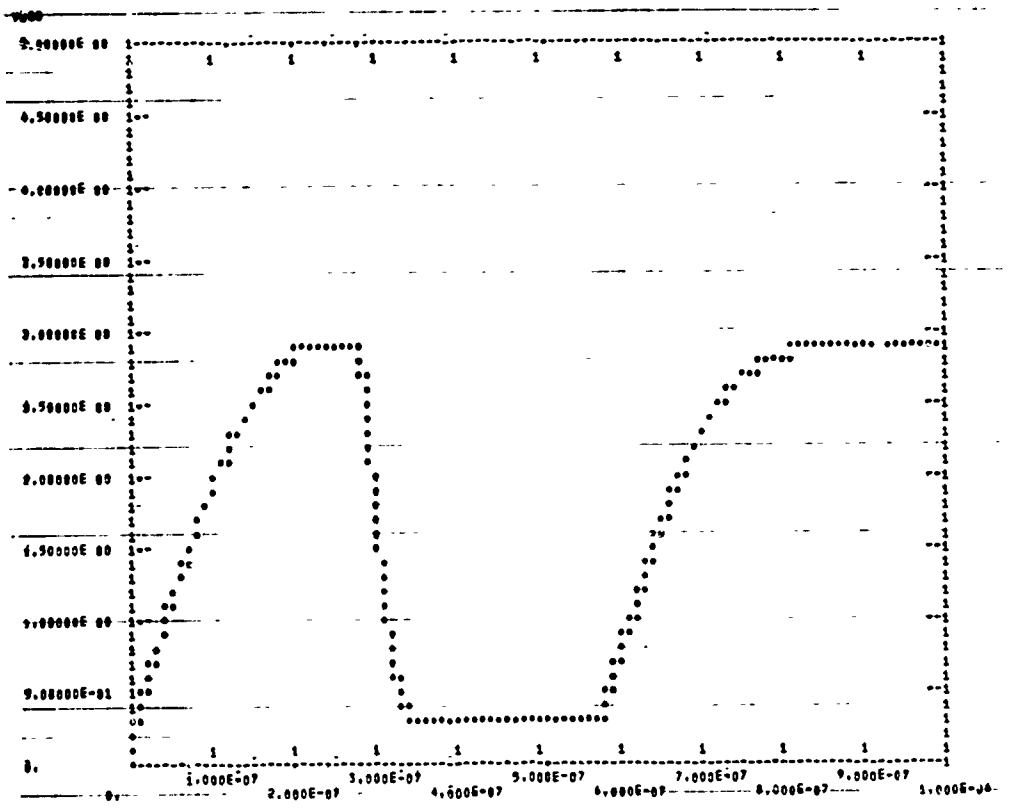


Figure VII-20. $\overline{Q}$ - Output

The circuit shown in Figure VII-16 was described to the computer to demonstrate that the pulse width could be increased using external timing components. The topological description of the SCEPTRE circuit analysis program is shown in Figure VII-21. The input signals EA1 and EA2 are held at 0.1 volt, EB2 is held at 3.1 volts, and EB1 is a pulse as shown in Figure VII-22. The external timing components are a 20-kilohm resistor and a 40-pf capacitor. The manufacturer's preliminary information is inadequate to determine the validity of the resulting output pulse width of 1.2 μsec as shown in Figures VII-23 and VII-24. However, this is reasonable, since the external resistance is half the internal resistance while the total capacitance is tripled. Therefore one would expect the time to be approximately 1100 nanoseconds.

C. RADIATION EFFECTS

1. GAMMA RADIATION

Exposing the device to a nuclear radiation environment may affect normal performance by causing the Q and $\overline{Q}$ signal levels to vary. When exposed to pulsed gamma radiation at dose rate levels of approximately $3 \times 10^{+10}$ rads (Si)/second, the performance is only temporarily affected. Extensive testing was done by the General Electric Company. The test report with photographic recording of the results is included in Appendix VII-B.

```
                SAVED UNDER FILE RSNL122
                TEST CONDITION 6
                EXTERNAL TIMING COMPONENTS 40PF  20K
        ELEMENTS
 F1,A1-A2-B1-B2-RS-VCC-TP1-TP2-TP3-Q-QB-0=MODEL RSN54L122
 ERS,0-RS=T1
 EA1,0-A1=0.1
 EA2,0-A2=0.1
 EB1,0-B1=PIN
 EB2,0-B2=3.1
 RIP,VCC-TP2=20.E3
 CIP,TP2-TP3=40.E-12
 JQ,Q-0=0.
 JQB,QB-0=0.
 RU1,Q-1=4300
 CU1,Q-1=2.E-12
 RU2,1-0=750.
 CU2,1-0=11.5E-12
 RU3,QB-3=4300.
 CU3,QB-3=2.E-12
 RU4,3-0=750.
 CU4,3-0=11.5E-12
 D1,Q-2=MODEL 1N3605 (PERM)
 RU5,2-5=800.
 D2,QB-4=MODEL 1N3605 (PERM)
 RU6,4-5=800.
 EL,0-5=2.4
        DEFINED PARAMETERS
 PIN=FGEN(0.,3.,1.E-7,15.E-9,1.6E-7,15.E-9,2.E-6,5.,TIME)
 PNVT1=FNVT(VC1F1,0.4,0.2)
 PNVT2=FNVT(VC2F1,0.4,0.2)
        FUNCTIONS
 T1=0.,.1,50.E-9,.1,65.E-9,3.,5.E-7,3.
        OUTPUTS
 EA1,EA2,EB1,EB2,ERS,VJQ,VJQB,PLOT
 XSTPSZ,PLOT
        RUN CONTROLS
 START TIME = 0.
 STOP TIME =2.E-6
 MINIMUM STEP SIZE = 1.E-18
 MAXIMUM STEP SIZE=5.E-9
 MAXIMUM PRINT POINTS = 100
 COMPUTER TIME LIMIT = 5.5
 END
```

Figure VII-21. Test Circuit Description

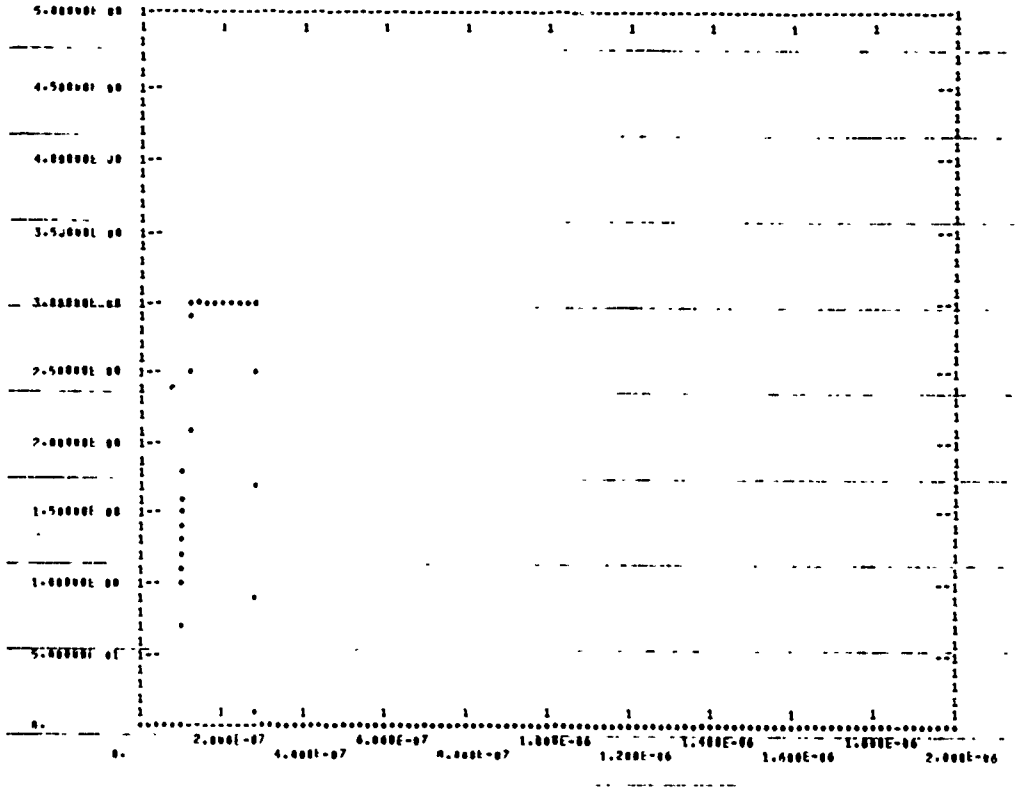


Figure VII-22. B1 Input Signal

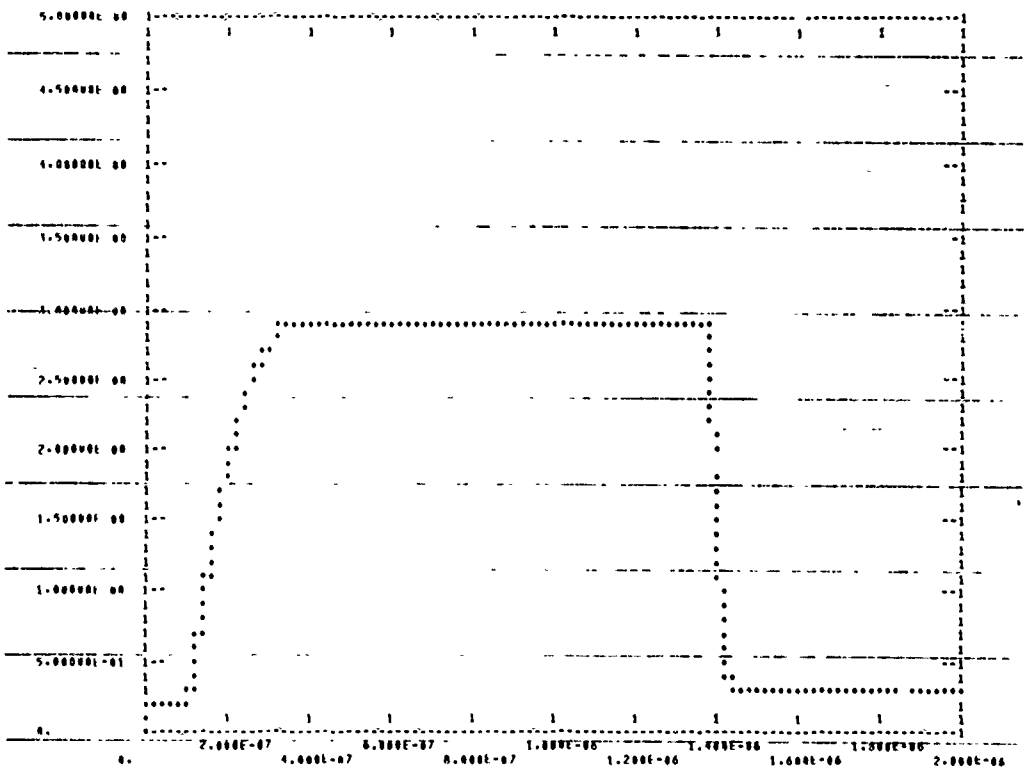


Figure VII-23. Q - Output

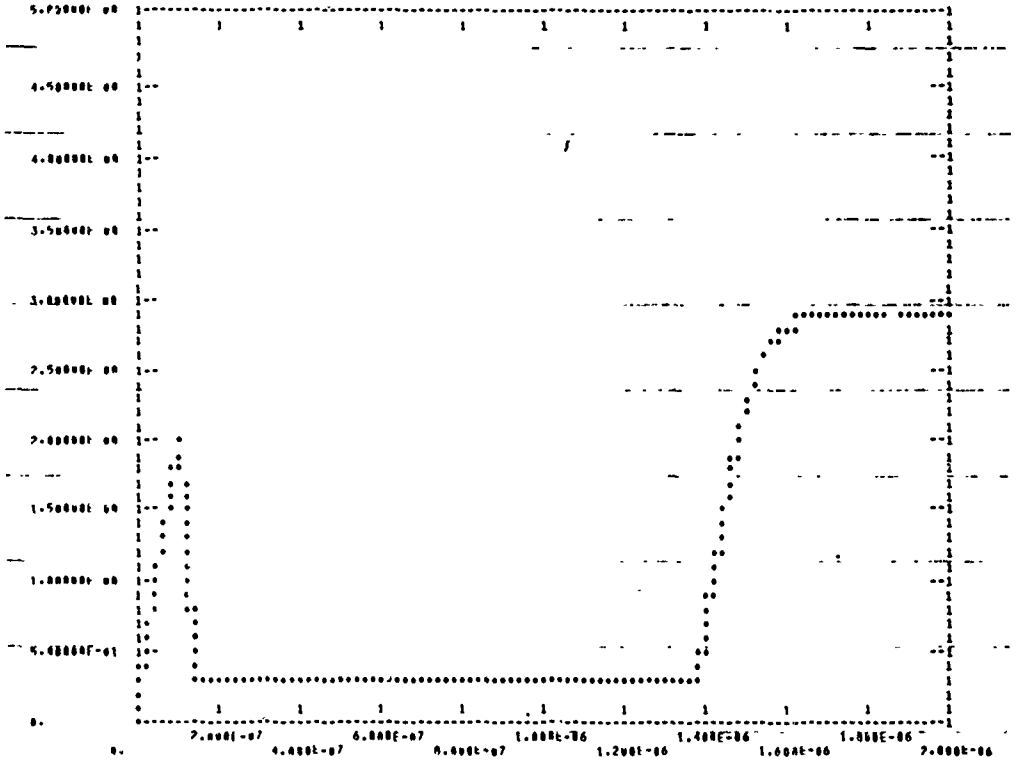


Figure VII-24. $\overline{Q}$ - Output

To appropriately include the radiation effects, it was necessary to modify the device model. This was accomplished by adding Table 2 to the model description (Figure VII-4), to reflect the response of the circuit to the radiation in such a manner as to agree with the observed results. Thus the response is indicated to have a value of -2 when the voltage across JR1 and/or JR2 is 0 volts, a value of -1.0 when the voltage is 1 volt, a value of +0 when the voltage is 2 volts, and a value of 2.0 when the voltage is 3 volts. Figure VII-25 shows the manner in which this was accomplished.

To simulate test condition 6, the radiation effect in the computer is caused to occur when time equals 3.51 μseconds. The gamma ray pulse is 20 nanoseconds wide and is described in Table 3 on Figure VII-26, which also describes the test circuit conditions. Condition 6 requires that the preset be set "high", which results in the Q being low and $\overline{Q}$ high. These conditions exist at 3.51 μseconds, at which time the radiation effects are simulated. Figure VII-27 indicates the relative change

```
MODEL RSN54L122 (A1-A2-B1-B2-RS-VCC-TP1-TP2-TP3-0-QB-0)
      MONOSTABLE MULTIVIBRATOR
      ELEMENTS
JA1,A1-0=0.
JA2,A2-0=0.
JB1,B1-0=0.
JB2,B2-0=0.
JRS,RS-0=0.
EE,TP3-VC=FIN(VJA1,VJA2,VJB1,VJB2,TIME,EE,VJRS)
RRF,VC-TP1=1.E20
RF1,TP1-TP2=33.E3
RF2,VC-VCC=7.E3
RRR,VCC-TP1=1.E20
RFF,VC-TP2=T1(EE)
CF,TP2-TP3=25.E-12
JF,TP2-TP3=0.
E1,0-1=FSS(VJF,VJRS)
R1,1-2=1000.
C1,2-0=FCAP(E1,VC1)
JR1,2-0=Q1(TABLE 2(VC1),P1)
EQ,0-3=X1(VJR1+P2)
RQ,3-0=100.
E2,0-4=X2(3.1-E1)
R2,4-5=1000.
C2,5-0=FCAP(E2,VC2)
JR2,5-0=Q1(TABLE 2(VC2),P1)
RQB,6-QB=100.
EQB,0-6=X3(VJR2+P3)
DEFINED PARAMETERS
P1=0.
P2=0.
P3=0.
      FUNCTIONS
Q1(A,B)=(A*B)
T1=0.,1.E20,.6,1.E20,2.,10.,3.,10.
TABLE 2=0.,-2.,1.,-1.,2.,0.,3.,2.
      OUTPUTS
VJF,PLOT
```

Figure VII-25. Computer Model Description With Gamma Effects

```
SAVED UNDER FILE RSNL122
TEST CONDITION 6
      ELEMENTS
F1,A1-A2-B1-B2-RS-VCC-TP1-TP2-TP3-0-QB-0=MODEL RSN54L122(CHANGE
P1=T3)
ERS,0-RS=11
EA1,0-A1=0.1
EA2,0-A2=0.1
EB1,0-B1=PIN
EB2,0-B2=3.1
RTP,VCC-TP2=2.E3
CTP,TP2-TP3=20.E-12
J0,0-0=0.
JQB,QB-0=0.
RQ1,0-1=4300
CQ1,0-1=2.E-12
RQ2,1-0=750.
CQ2,1-0=11.5E-12
RQ3,QB-3=4300.
CQ3,QB-3=2.E-12
RQ4,3-0=750.
CQ4,3-0=11.5E-12
D1,0-2=MODEL 1N3605 (PERM)
RQ5,2-5=800.
D2,QB-4=MODEL 1N3605 (PERM)
RQ6,4-5=800.
EL,0-5=2.4
      DEFINED PARAMETERS
PIN=FGEN(0.,3.,1.E-7,15.E-9,1.6E-7,15.E-9,9.E-7,10.,TIME)
PNVT1=FNVT(VC1F1,0.4,0.2)
PNVT2=FNVT(VC2F1,0.4,0.2)
      FUNCTIONS
T1=0.,.1,50.E-9,.1,65.E-9,3.,5.E-7,3.
T3=0.,0.,3.5E-7,0.,3.5E-7,.5,3.51E-7,1.,3.52E-7,.5,3.52E-7,
0.,2.E-6,0.
      OUTPUTS
EA1,EA2,EB1,EB2,ERS,VJQ,VJQB,PLOT
XSTPSZ,PLOT
      RUN CONTROLS
START TIME = 0.
STOP TIME = 1.E-6
MINIMUM STEP SIZE = 1.E-18
MAXIMUM STEP SIZE=5.E-9
MAXIMUM PRINT POINTS = 100
COMPUTER TIME LIMIT = 5.5
END
```

Figure VII-26. Gamma Test Circuit Description

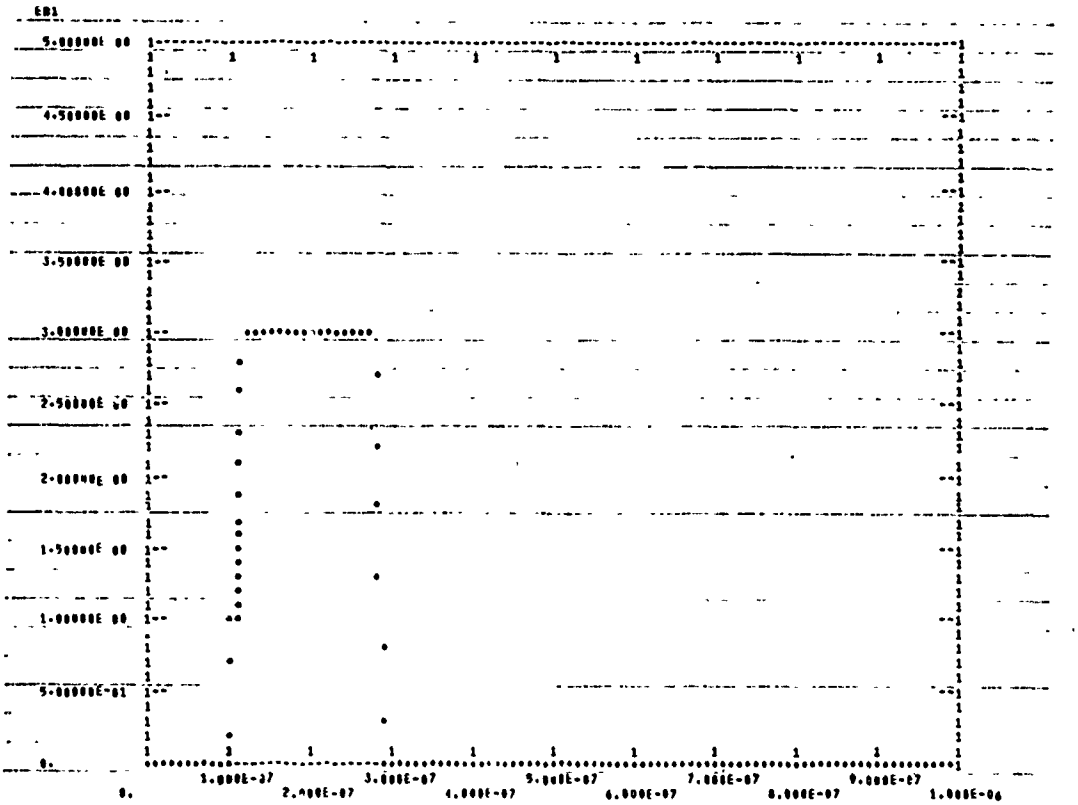


Figure VII-27. B1 Input Signal

condition (i.e., EB varying from a 0 level to a 1 level and then returning) which initiates a change in the output state since all other signal levels are kept constant. The result of this application of simulated radiation is shown in Figures VII-28 and VII-29 for Q and $\overline{Q}$ respectively. Drawn on the computer printouts are the results observed during the actual tests.

The figures indicate excellent agreement between the computed results and the laboratory test observations.

2. NEUTRON RADIATION

When the device is exposed to neutron radiation conditions, its performance may be degraded either temporarily or permanently. The degree of the degradation, as well as the device recovery time for those conditions which permit recovery, depends upon the exposure level.

Exposure of test circuits to fluence levels of 1.2×10^{14} results in an output level reduction of approximately 0.4 volt, when the output signal is at a 1 level. When the output signal is at a 0 level, the voltage is increased by about 0.2 volt. These results were observed by the Air Force Weapons Laboratory when they exposed these devices and are reported in Reference 1.*

Figure VII-30 presents the circuit transfer degradation observed during these tests, for various fluence levels. For curve 4, which represents the contract test condition, the output signal level drops from about 3.1 volts to approximately 2.7 volts and rises from about 0.4 volt to approximately 0.6 volt.

*Olson, R. J., op. cit. page 16

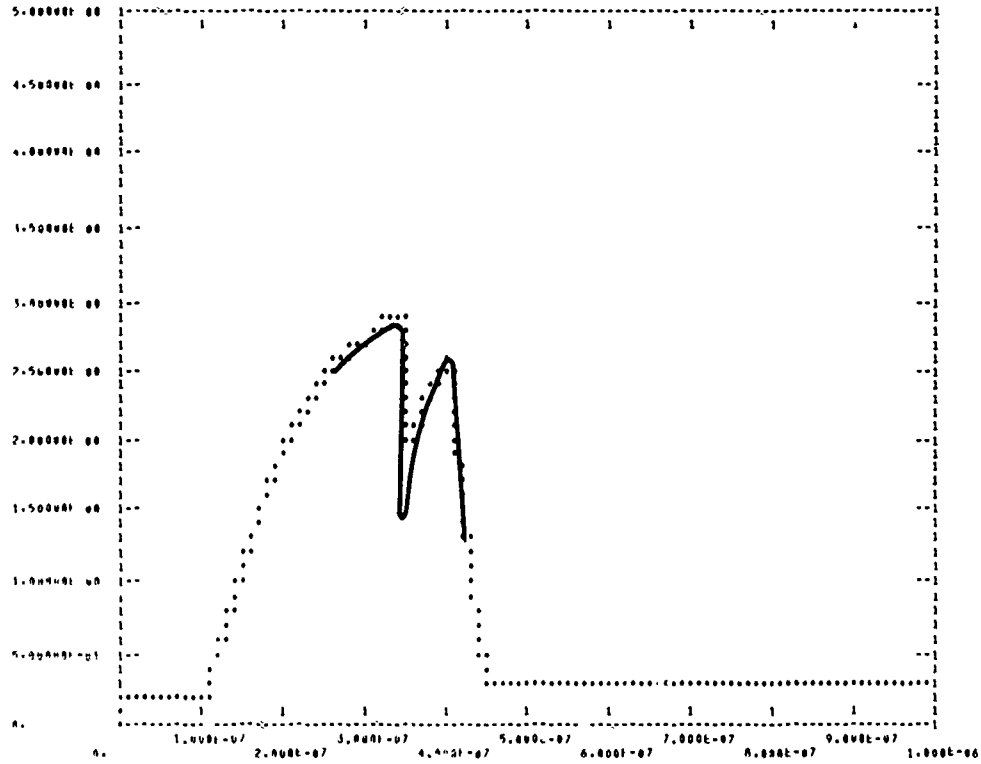


Figure VII-28. Q - Response to Gamma Radiation

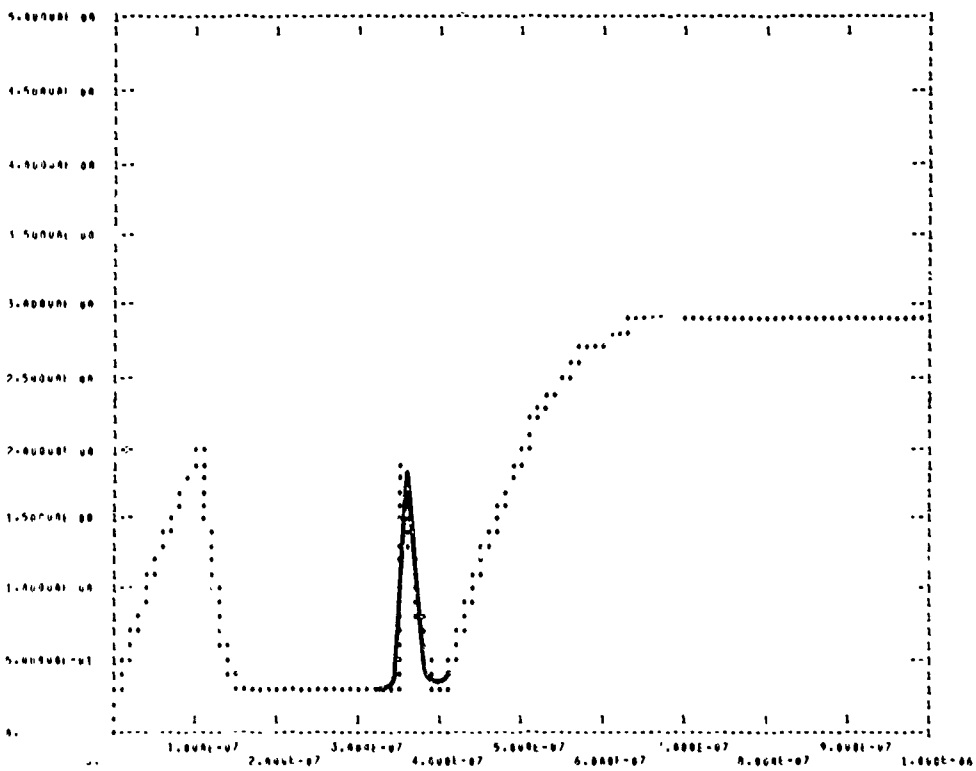


Figure VII-29. $\overline{Q}$ - Response to Gamma Radiation

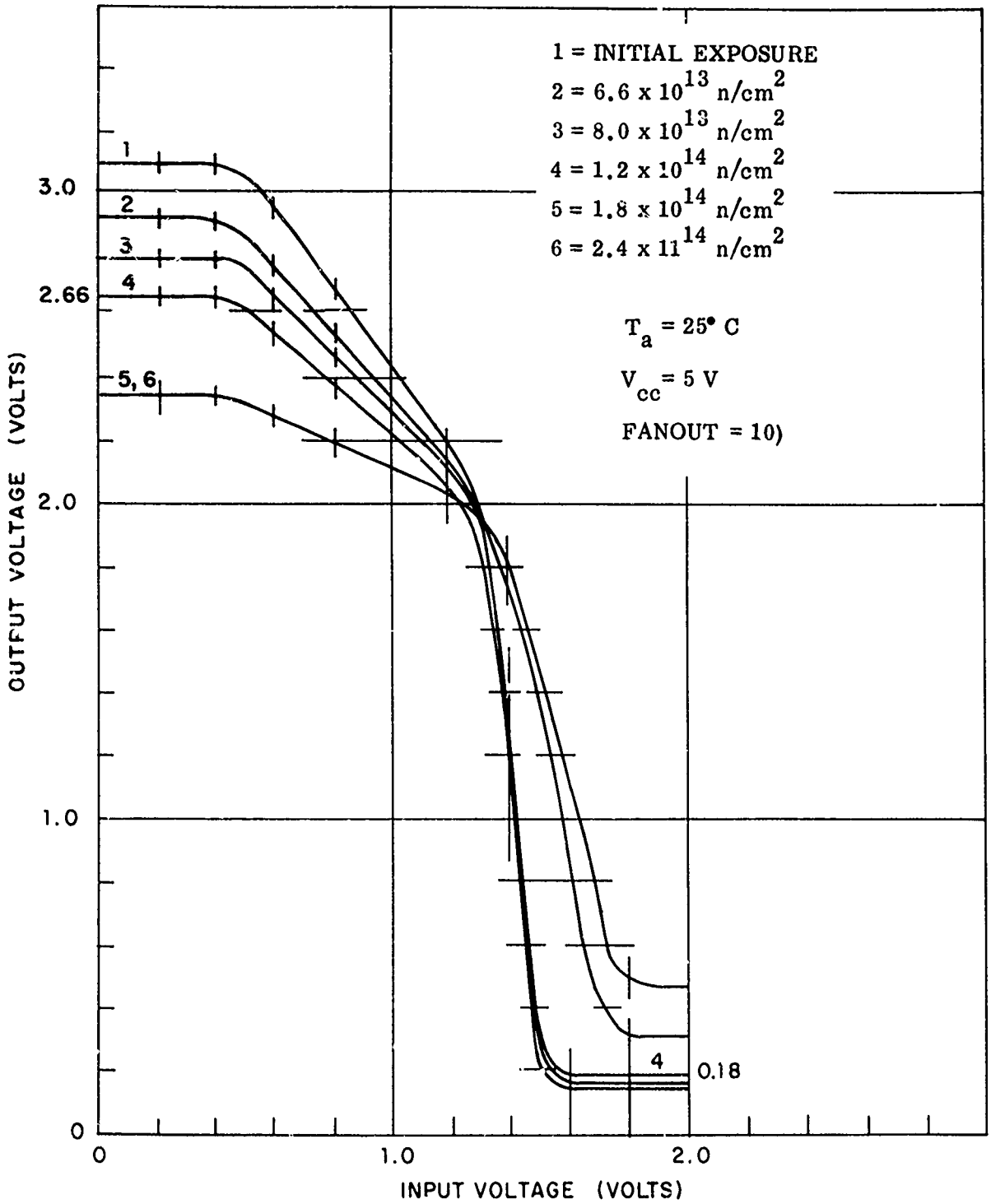


Figure VII-30. Neutron Radiation - Circuit Transfer Function

The method for incorporating this response change into the model is shown in Figure VII-31. The values of voltage sources EQ and EQB, and thus the output voltage EQ and EQB, are changed from a simple dependency on the voltage across the sources JR1 and JR2, respectively, to a dependency upon both the voltage across the source and the fluence level. The fluence is identified as P2 for EQ and P3 for EQB. This change in dependency is accomplished by use of an additional subroutine, FNVT, which is incorporated into the model description.

The subroutine FNVT is shown in Figure VII-5; the computer circuit description to produce the analysis in Figure VII-32. The inclusion of the neutron exposure effects is accomplished by redefining P1 and P2, in the model callout, to be PNVT1 and PNVT2 respectively. PNVT1 and PNVT2 establish a value for the function FNVT, and thus modify the values of EQ and EQB in the device model.

The effect of the subroutine FNVT is seen in Figures VII-33 and VII-34, for Q and $\overline{Q}$ respectively. Figure VII-33 shows that the 1 level voltage is reduced from about 2.9 volts (Figure VII-10) to approximately 2.5 volts, and the 0 signal increased from about 0.2 volt to 0.4 volt. The same change is observed when Figure VII-34 is compared with Figure VII-11. These results agree with the observed laboratory data.

```
MODEL RSN54L122 (A1-A2-B1-B2-RS-VCC-TP1-TP2-TP3-Q-QB-0)
      MONOSTABLE MULTIVIBRATOR
      ELEMENTS
JA1,A1-0=0.
JA2,A2-0=0.
JB1,B1-0=0.
JB2,B2-0=0.
JRS,RS-0=0.
EF,TP3-VC=FIN(VJA1,VJA2,VJB1,VJB2,TIME,EF,VJRS)
RRF,VC-TP1=1.E20
RF1,TP1-TP2=33.E3
RF2,VC-VCC=7.E3
RRR,VCC-TP1=1.E20
RFF,VC-TP2=T1(EF)
CF,TP2-TP3=25.E-12
JF,TP2-TP3=0.
E1,0-1=FSS(VJF,VJRS)
R1,1-2=1000.
C1,2-0=FCAP(E1,VC1)
JR1,2-0=Q1(TABLE 2(VC1),P1)
EQ,0-3=X1(VJR1+P2)
RQ,3-0=100.
E2,0-4=X2(3.1-E1)
R2,4-5=1000.
C2,5-0=FCAP(E2,VC2)
JR2,5-0=Q1(TABLE 2(VC2),P1)
RQB,6-QB=100.
EQB,0-6=X3(VJR2+P3)
DEFINED PARAMETERS
P1=0.
P2=0.
P3=0.
      FUNCTIONS
Q1(A,B)=(A*B)
T1=0.,1.E20,.8,1.E20,2.,10.,3.,10.
TABLE 2=0.,-2,,1.,-1.,2.,0.,3.,2.
      OUTPUTS
VJF,PLOT
```

Figure VII-31. Computer Model Description With Neutron Effects

```
                    SAVED UNDER FILE RSNL122
                    TEST CONDITION 6
          ELEMENTS
 F1,A1-A2-B1-B2-RS-VCC-TP1-TP2-TP3-Q-QB-0=MODEL RSN54L122(CHANGE
 P2=PNVT1,P3=PNVT2)
 FRS,0-RS=T1
 EA1,0-A1=0.1
 EA2,0-A2=0.1
 EB1,0-B1=PIN
 EB2,0-B2=3.1
 RTP,VCC-TP2=2.E3
 CTP,TP2-TP3=20.E-12
 JQ,Q-0=0.
 JQB,QB-0=0.
 R01,Q-1=4300
 C01,Q-1=2.E-12
 R02,1-0=750.
 C02,1-0=11.5E-12
 R03,QB-3=4300.
 C03,QB-3=2.E-12
 R04,3-0=750.
 C04,3-0=11.5E-12
 D1,Q-2=MODEL 1N3605 (PERM)
 R05,2-5=800.
 D2,QB-4=MODEL 1N3605 (PERM)
 R06,4-5=800.
 EL,0-5=2.4
        DEFINED PARAMETERS
 PIN=FGEN(0.,3.,1.E-7,15.E-9,1.6E-7,15.E-9,9.E-7,10.,TIME)
 PNVT1=FNVT(VC1F1,0.4,0.2)
 PNVT2=FNVT(VC2F1,0.4,0.2)
        FUNCTIONS
 T1=0.,.1,50.E-9,.1,65.E-9,3.,5.E-7,3.
        OUTPUTS
 EA1,EA2,EB1,EB2,ERS,VJQ,VJQB,PLOT
 XSTPSZ,PLOT
        RUN CONTROLS
 START TIME = 0.
 STOP TIME = 1.E-6
 MINIMUM STEP SIZE = 1.E-18
 MAXIMUM STEP SIZE=5.E-9
 MAXIMUM PRINT POINTS = 100
 COMPUTER TIME LIMIT = 5.5
 END
```

Figure VII-32. Neutron Test Circuit Description

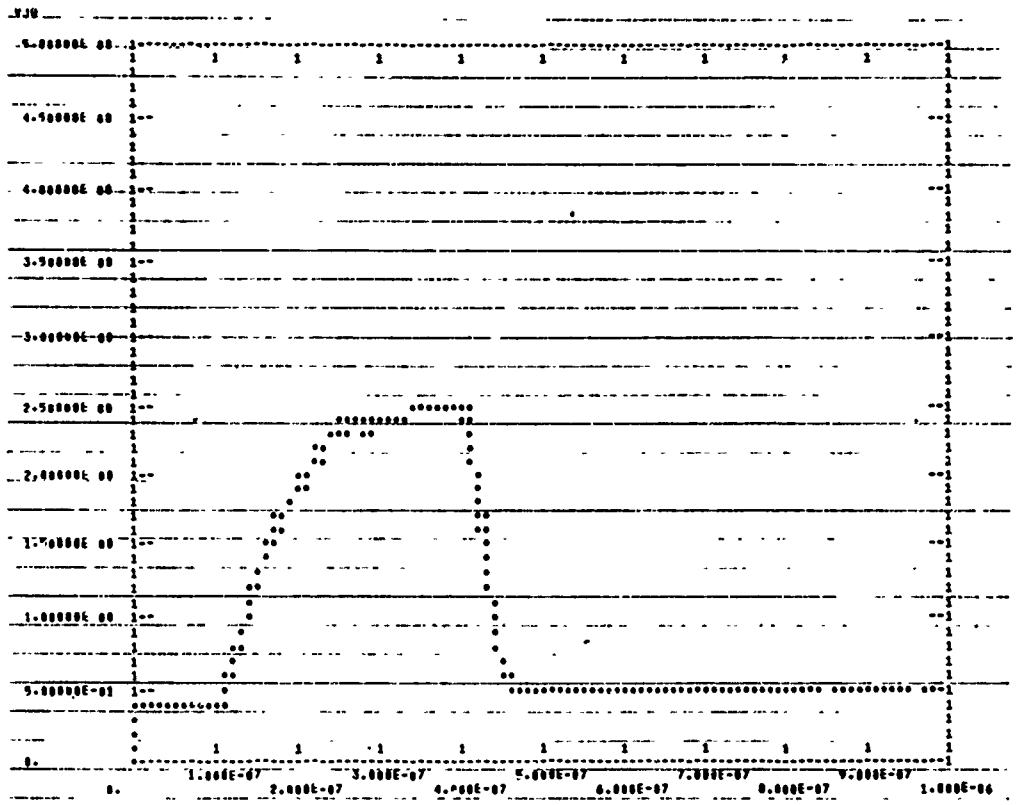


Figure VII-33. Q - Response to Neutron Radiation

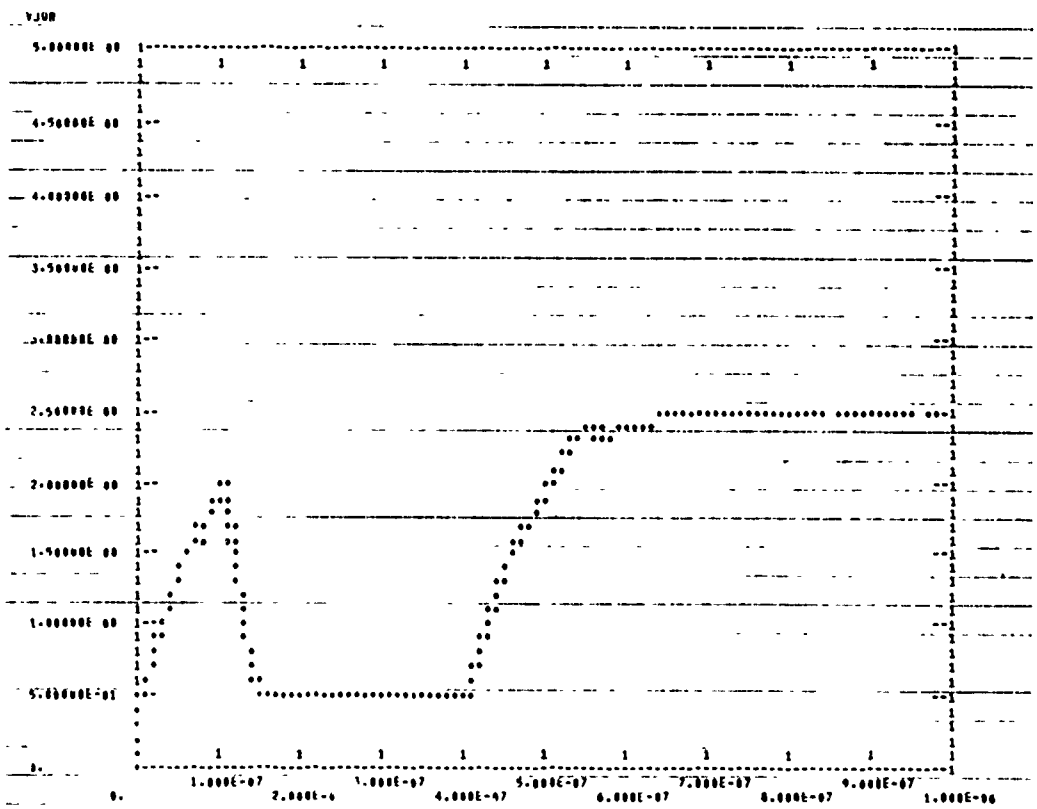


Figure VII-34. $\bar{Q}$ - Response to Neutron Radiation

SECTION VIII

TEXAS INSTRUMENTS RSN54L57 AND-OR INVERT GATE

The integrated circuit is a 4-wide 3-3-2-3 AND-OR INVERT gate. The circuit behaves in such a manner that if no AND gate is true, the circuit output is a logic 1; if any one of the four AND gates is true, the circuit output is a logic 0.

The logic representation for the circuit is shown in Figure VIII-1; the schematic representation in Figure VIII-2. The device electrical specifications as published by the manufacturer are shown in Table VIII-1.

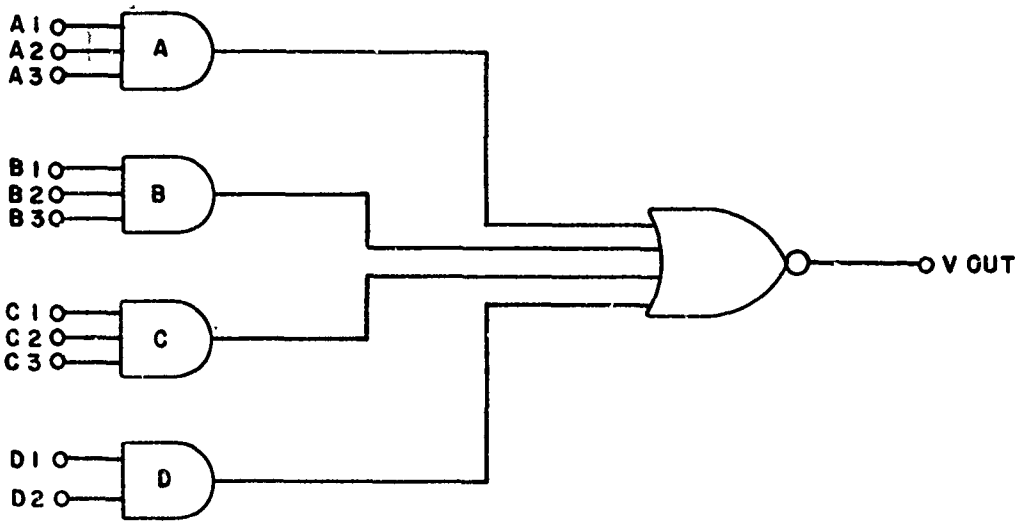


Figure VIII-1. Logic Diagram

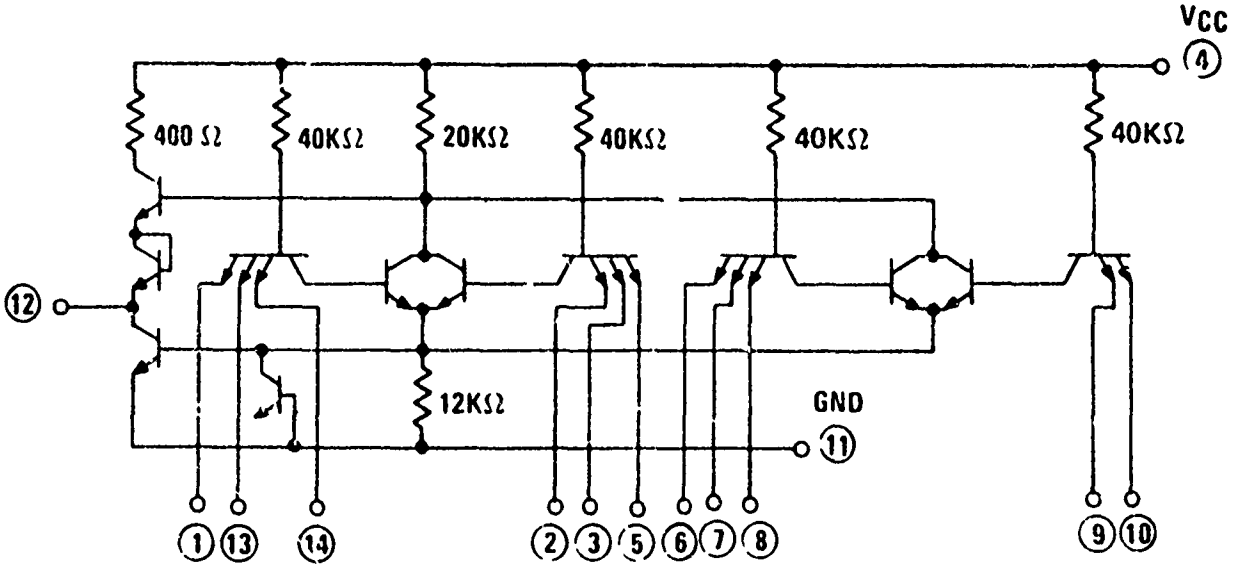


Figure VIII-2. Schematic RSN54L57

TABLE VIII-1.
ELECTRICAL CHARACTERISTICS
(Over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*	MIN	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of either AND section to ensure logical 0 at output	V_{CC} = Min.	1.9		V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	V_{CC} = Min.		0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = Min. V_{in} = 0.8V I_{load} = -100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = Min. V_{in} = 1.9V I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = Max. V_{in} = 0.3V		-0.18	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = Max. V_{in} = 2.4V V_{CC} = Max. V_{in} = 5.5V		10 100	μA μA
I_{OS}	Short-circuit output current	V_{CC} = Max. V_{in} = 0 V_{out} = 0	-1	-15	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = Max. V_{in} = 5V		0.99	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = Max V_{in} = 0		0.8	mA

Switching Characteristics V_{CC} = 5V, T_A = 25°C, N = 10

tpd0	Propagation delay time to logical 0 level	C_L = 50 pF R_L = 4 kΩ		60	ns
tpd1	Propagation delay time to logical 1 level	C_L = 50 pF R_L = 4 kΩ		90	ns

*For conditions shown as Min. or Max. use the appropriate value specified under recommended operating conditions for the applicable circuit type.

A. MODEL DEVELOPMENT

The computer model that has been developed to duplicate observed performance is shown in Figure VIII-3; the computer model description in Figure VIII-4. It will be noted that, as a result of earlier experience in developing models for other device types, provisions for both gamma and neutron behavior have been included in the initial model description; P1 for gamma and P4 for neutron effects.

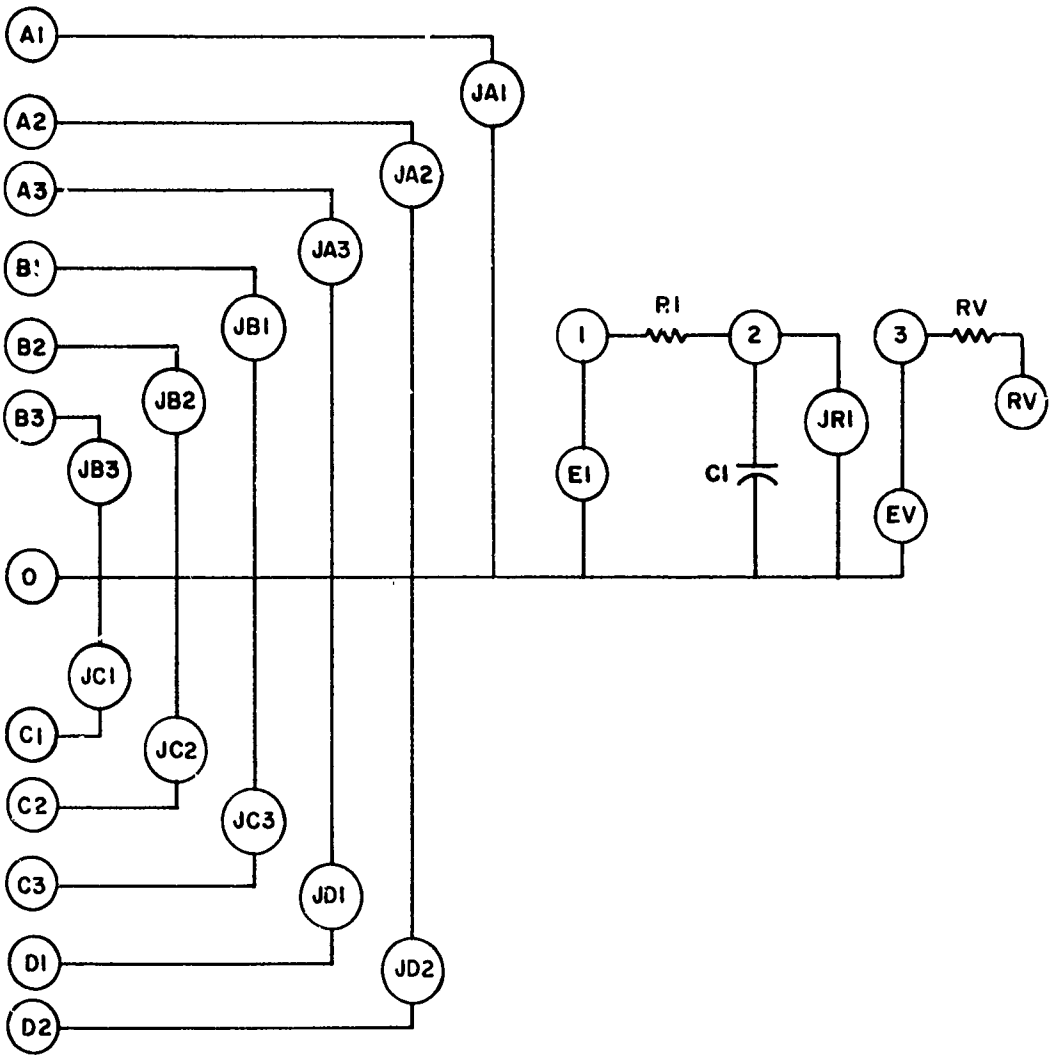


Figure VIII-3. Computer Model

```
MODEL RSN54L57 (A1-A2-A3-B1-B2-B3-C1-C2-C3-D1-D2-V-0)
                    ELEMENTS
JA1,A1-0=0.
JA2,A2-0=0.
JA3,A3-0=0.
JB1,B1-0=0.
JB2,B2-0=0.
JB3,B3-0=0.
JC1,C1-0=0.
JC2,C2-0=0.
JC3,C3-0=0.
JD1,D1-0=0.
JD2,D2-0=0.
E1,0-1=F57(VJA1,VJA2,VJA3,VJB1,VJB2,VJB3,VJC1,VJC2,VJC3,VJD1,VJD2)
R1,1-2=100.
C1,2-0=FCAP(E1,VC1)
JR1,2-0=O1(TABLE2(VC1),P1)
EV,0-3=X1(VJR1+P4)
RV,3-V=100.
JV,V-0=0.
DEFINED PARAMETERS
P1=0.
P4=0.
                    FUNCTIONS
T1=0.,300.E-12,3.,100.E-12
TABLE2=0.,-2.,1.,-1.,2.,0.,3.,2.
O1(A,B)=(A*B)
OUTPUTS
VJV,C1,PLOT
```

Figure VIII-4. Computer Model Description

The subprogram that establishes the logic output signal level, the delay characteristics and the neutron radiation behavior is shown in Figure VIII-5.

If any of the input signals to any of the four NAND gates is less than, or equal to, 0.8 volt, an intermediate value of 1 is established as the output of the gate. Each of the intermediate values is established in this manner and then all are tested to determine their value. If all have been set to 1, then the function F57 is set equal to 3.0 volts; this represents a logic 1 for E1. If all values are not a 1, then the function is set to 0.3 volt, which represents a logic 0. Thus the signal voltage associated with E1 of Figure VIII-3, and therefore the device model output, is determined by this subprogram which also simulates the exclusive OR function of Figure VIII-1.

The time delays associated with the controlling signals, as defined by the manufacturer, are given in Table VIII-1. To obtain delays, the time constant R1 - C1 is used. Since the time delay, t_{pd1}, associated with an increase in the value of the output signal, is different from that associated with a decrease in the signal level, t_{pd0}, the value C1 is changed. This is accomplished by means of the function subprogram, FCAP. This subprogram sets the value of C1 equal to 300 picofarads plus a small variable that is dependent upon the voltage across C1, when the value of the voltage across C1 is less than the output signal level. If the value of the voltage E1 is equal to, or greater than, the output signal level, C1 is set to 450 picofarads, plus a small variable which is again dependent upon the actual voltage across C1. The reason for including this variable in the function is to provide better duplication of measured results; the normal R-C time constant curve deviates too much from observed waveshapes after 3τ is reached. The FORTRAN flow charts associated with these functions as well as the radiation response are shown in Appendix VIII-A.

```
1998T 02  01_25_72   12.762

      FUNCTION F57(A1,A2,A3,B1,B2,B3,C1,C2,C3,D1,D2)
      NA=2
      NB=2
      NC=2
      ND=2
      X=0.8
      IF(A1.LE.X.OR.A2.LE.X.OR.A3.LE.X) NA=1
      IF(B1.LE.X.OR.B2.LE.X.OR.B3.LE.X) NB=1
      IF(C1.LE.X.OR.C2.LE.X.OR.C3.LE.X) NC=1
      IF(D1.LE.X.OR.D2.LE.X) ND=1
      F57=0.3
      IF(NA.EQ.1.AND.NB.EQ.1.AND.NC.EQ.1.AND.ND.EQ.1) F57=3.0
      RETURN
      ENTRY FCAP(A,B)
      IF(A-B)10,20,20
   10 F57=300.E-12*B/3.+300.E-12
      RETURN
   20 F57=300.E-12*B/3.+450.E-12
      RETURN
      ENTRY FNVT(A,B,C)
C     SUBPROGRAM FOR NEUTRON BEHAVIOR
      IF(A-1.5) 40,50,60
   40 Y=C
      GO TO 150
   50 Y=.1
      GO TO 150
   70 Y=0.05
      GO TO 150
   60 IF(A.LE.2.)GO TO 70
      IF(A.LT.2.3)GO TO 80
      IF(A.LT.2.5)GO TO 100
      IF(A.LT.2.7)GO TO 90
      IF(A.LT.2.8)GO TO 110
      Y=-8
      GO TO 150
   80 Y=-0.05
      GO TO 150
   90 Y=-0.15
      GO TO 150
  100 Y=-0.1
      GO TO 150
  110 Y=-0.25
  150 F57=Y
      RETURN
      END

  23672 WORDS OF MEMORY USED BY THIS COMPILATION
```

Figure VIII-5. Model Subprogram

The output impedance associated with the circuit is fixed at 100 ohms. Although this is not an accurate impedance representation for all voltage and load conditions, it provides first order accuracy of output signal level. To duplicate actual impedance variations, the value of resistor RV would be made variable and a function of the load voltage and currents.

B. MODEL VERIFICATION

To demonstrate the validity of the model, the circuit shown in Figure VIII-6 was described to the computer. The topological description for the SCEPTRE circuit analysis program is shown in Figure VIII-7. The relative timing of the forcing functions EA and ED, which cause the output to change from the 0 state to the 1 state, is shown in Figures VIII-8 and VIII-9 respectively. The circuit response to these signals is shown in Figure VIII-10.

The response time of the model (i.e., the delay from the time when the forcing signal reaches 1.5 volts until the output signal rises, or falls, to 1.5 volts) is 48 nanoseconds in the positive going direction (t_{pd1}) and 32 nanoseconds in the negative going direction (t_{pd0}). These times compare with the manufacturer's published data of t_{pd1} = 90 nanoseconds maximum and t_{pd0} = 60 nanoseconds maximum.

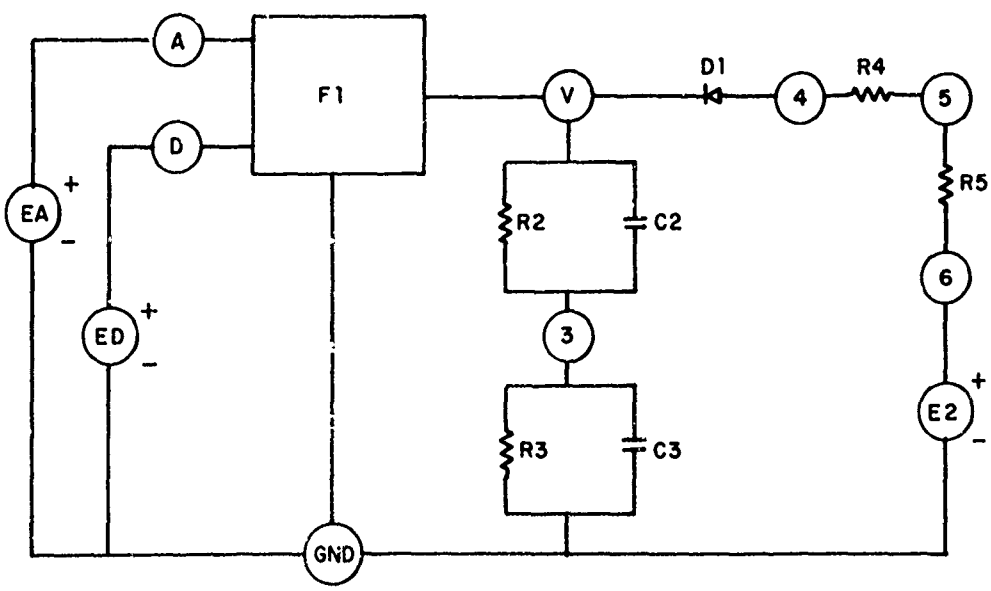


Figure VIII-6. Test Circuit

```
                    ELEMENTS
F1,A-A-A-A-A-A-D-D-D-D-D-V-0=MODEL RSN54L57
EA,0-A=FGEN(0.,3.,0.,PR,165.E-9,PF,500.E-9,100,TIME)
EU,0-D=FGEN(0.,3.,0.,PR,500.E-9,PF,1000.E-9,100,TIME)
R2,V-3=4300
C2,V-3=2.6E-12
R3,3-0=750
C3,3-0=15.E-12
D1,V-4=MODEL1N3605(PERM)
R4,4-5=880
R5,6-5=1.
C2,6-6=2.4
                    DEFINED PARAMETERS
PR=15.E-9
PF=15.E-9
PNVT=FNVT(VCIF1,0.4,0.2)
                    OUTPUTS
EA,EO,PLOT
                    RUN CONTROLS
START TIME = 0.
MAXIMUM PRINT POINTS = 200
COMPUTER TIME LIMIT = 5.5
STOP TIME=1999.E-9
END

SYSTEM NOW ENTERING SIMULATION
```

Figure VIII-7. Test Circuit Description

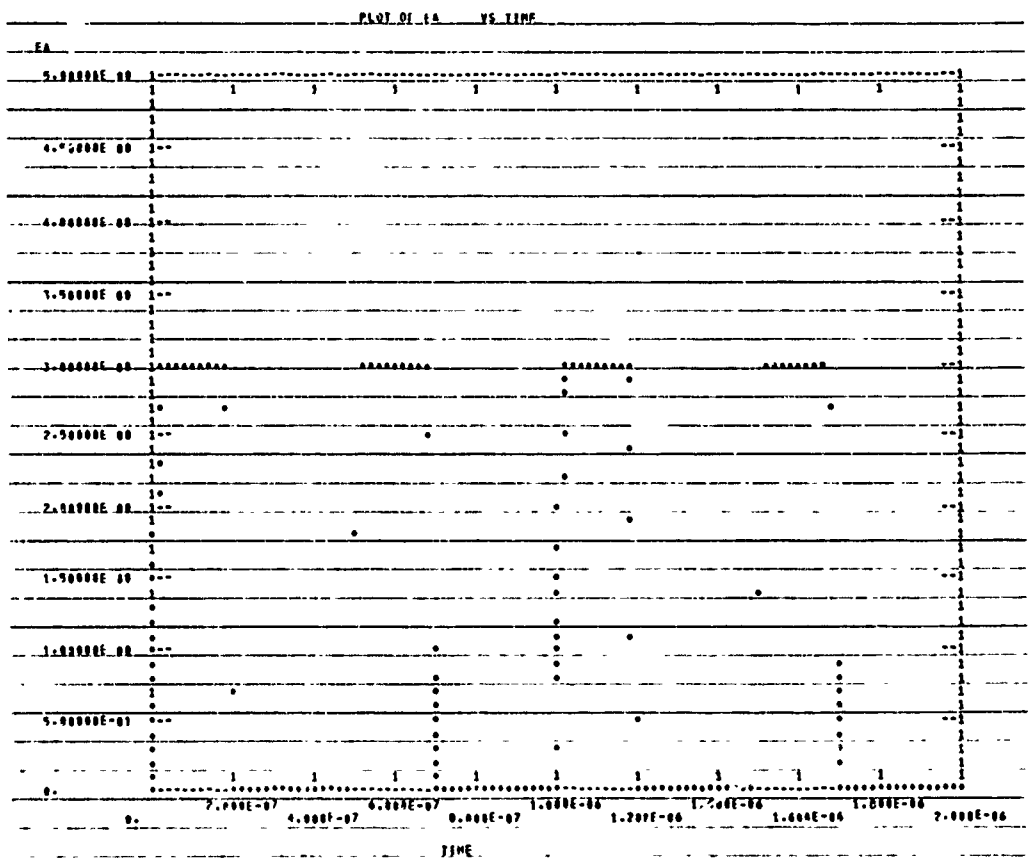


Figure VIII-8. A Input Signal

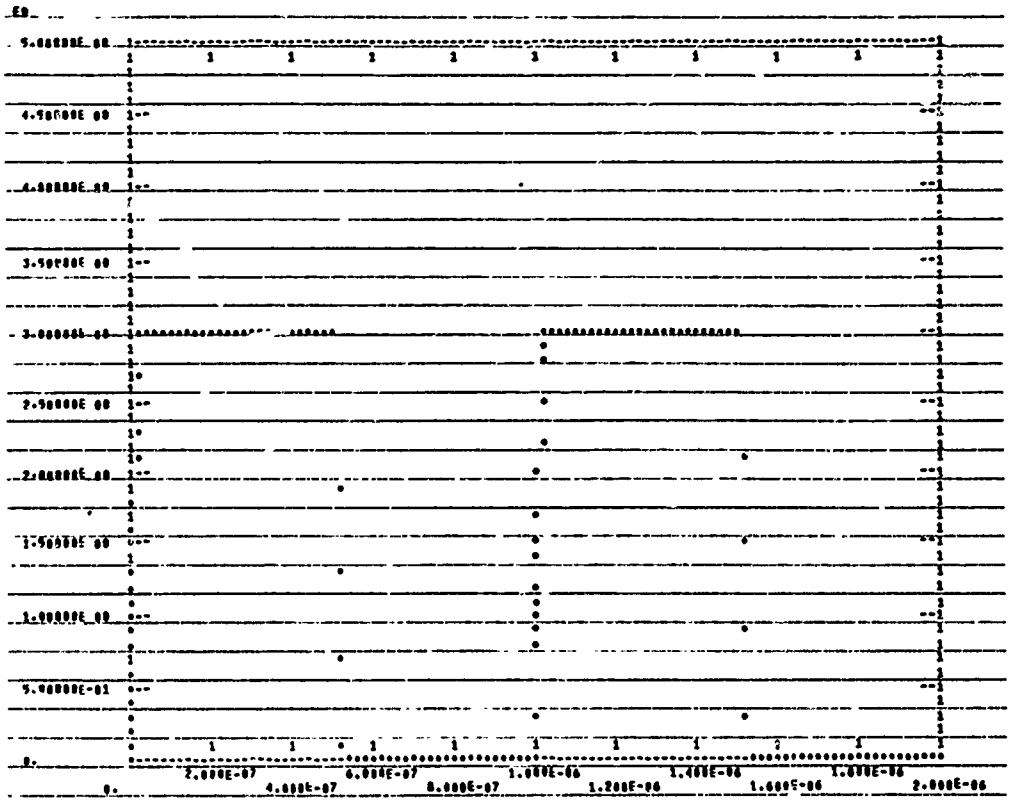


Figure VIII-9. D Input Signal

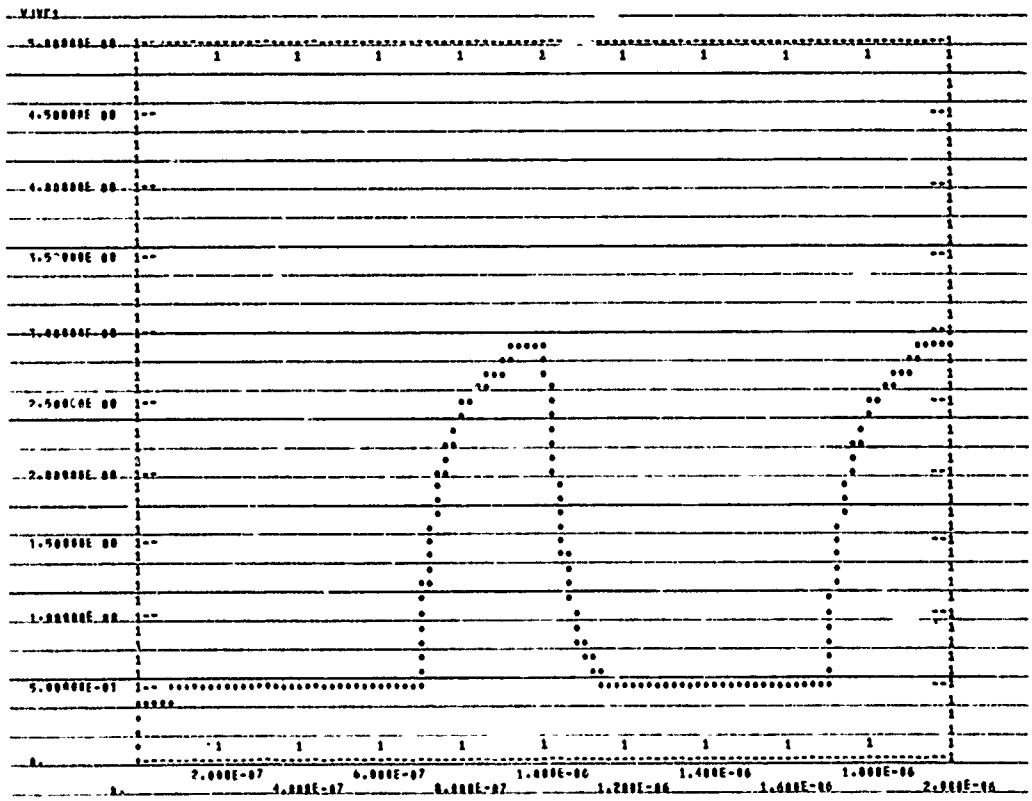


Figure VIII-10. Device Response

C. RADIATION EFFECTS

1. GAMMA RADIATION

Exposing the device to a nuclear radiation environment may affect normal performance by causing the output signal level to vary. When exposed to pulsed ionizing rays (gamma radiation) at dose rate levels of approximately $3 \times 10^{+10}$ rads (Si)/second, the performance is only momentarily affected. Extensive testing was done by the General Electric Company. The test report with photographic recording of the results is included as Appendix VIII-B.

When a gamma radiation pulse simulation is caused to occur while the output is at a 1 level, the response of the device is momentarily reduced. Figure VIII-11 shows both the observed and computer response to the radiation pulse.

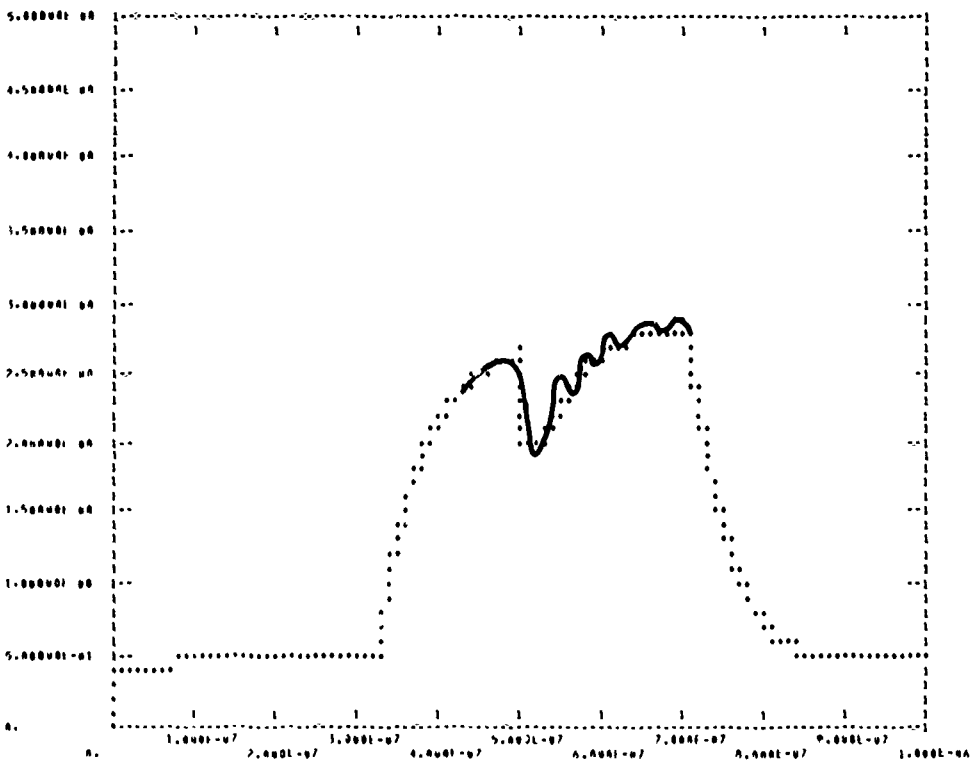


Figure VIII-11. 1 Response to Gamma Radiation

When the radiation is caused to occur when the gate output is at a 0 level, the normal reaction for the output level is to increase slightly. Figure VIII-12 shows both the observed and computer results.

The method for simulating the pulsed ionizing gamma radiation induced transient effects is to establish values for P1 of Figure VIII-4. As shown on Figure VIII-13, P1 is defined by Table 4; this change is identified as P1 = T4. By changing the time-related entries in Table 4, the radiation simulation is caused to occur whenever desired. For the results shown on Figure VIII-11, the gamma pulse is caused to occur at 0.51 μseconds.

Figures VIII-11 and VIII-12 demonstrate the agreement between the computed results and the laboratory observations.

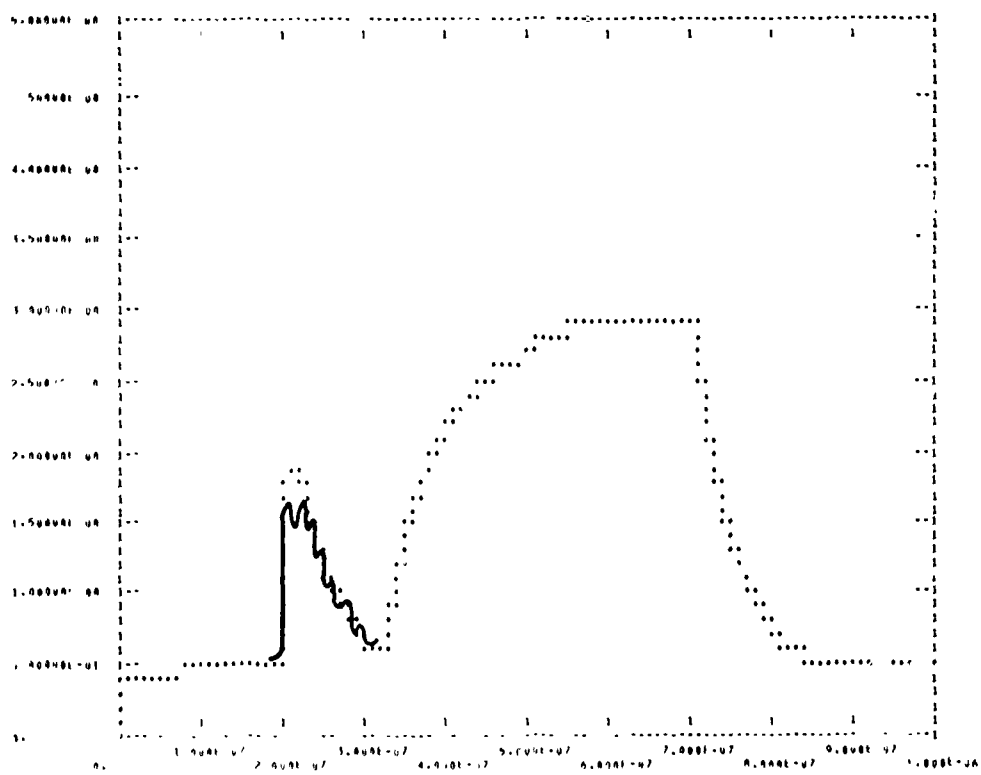


Figure VIII-12. 0 Response to Gamma Radiation

```
                    ELEMENTS
F1,A-A-A-A-A-A-D-D-D-D-D-V-0=MODEL RSN54L57(CHANGE P1=T4)
EA,0-A=FGEN(0.,3.,0.,PR,2.E-7,PF,7.E-7,5.,TIME)
ED,0-D=FGEN(0.,3.,1.E-7,PR,2.E-7,PF,7.E-7,5.,TIME)
R2,V-3=4300
C2,V-3=2.6E-12
R3,3-0=750
C3,3-0=15.E-12
D1,V-4=MODEL1N3605(PERM)
R4,4-5=800
R5,6-5=1.
E2,0-6=2.4
                    DEFINED PARAMETERS
PR=15.E-9
PF=15.E-9
PNVT=FNVT(VG1F1,0.4,0.2)
                    FUNCTIONS
T4=0.,0.,5.E-7,0.,5.E-7,.5,5.1E-7,1.,5.2E-7,.5,5.2E-7,0.,1.E-6,0.
                    OUTPUTS
EA,ED,PLOT
                    RUN CONTROLS
START TIME = 0.
MAXIMUM PRINT POINTS = 200
COMPUTER TIME LIMIT = 5.5
STOP TIME = 999.9E-9
                    RERUN DESCRIPTION
       FUNCTIONS
T4=0.,0.,5.E-7,0.,5.E-7,.05,5.1E-7,.1,5.2E-7,.05,5.2E-7,0.,1.E-6,0.
END

SYSTEM NOW ENTERING SIMULATION
```

Figure VIII-13. Gamma Radiation Test Circuit Description

2. NEUTRON RADIATION

When the device is exposed to neutron radiation conditions, its performance may be degraded either temporarily or permanently. The degree of the degradation as well as the device recovery time, for those conditions which permit recovery, depends upon the exposure level.

Exposure of test circuits of fluence levels of 1.2×10^{14} results in an output level reduction of approximately 0.4 volt, when the signal is at a 1 level. When the output signal is at a 0 level, the voltage is increased by about 0.2 volt. The results were observed by the Air Force Weapons Laboratory when they tested these devices and are reported in Reference 1.* Figure VIII-14 presents the circuit transfer function degradation observed during these tests, for various fluence levels. For curve 4, which represents test condition 4, the output signal level drops from about 3.1 volts to approximately 2.7 volts and rises from about 0.16 volt to approximately 0.36 volt.

*Olson, R. J., op. cit. page 16

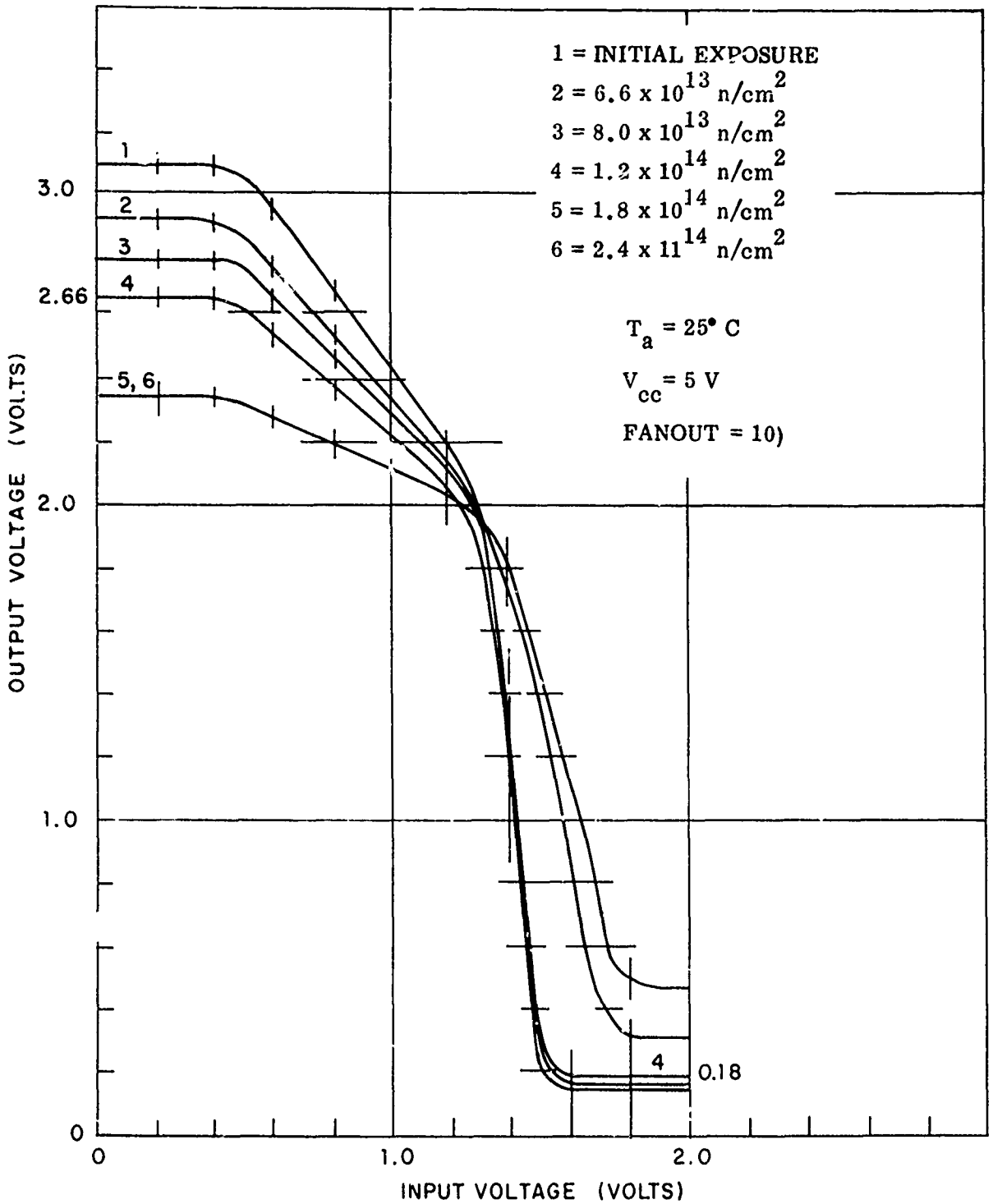


Figure VIII-14. Neutron Radiation - Circuit Transfer Function

The method for incorporating this response change into the model is shown on Figure VIII-15. Since P4 was originally set equal to zero, the value of the output voltage, EV, is changed from a simple dependency on the voltage across current source, JR1, to a dependency upon both the capacitor voltage and the fluence level. This is done by setting P4 equal to the function FNVT.

The computer description to produce an analysis of the device in the test circuit configuration is shown in Figure VIII-15 and is accomplished by changing the value of P4 to be equal to PNVT, which is defined as dependent upon the function FNVT. The results of the analysis are shown in Figure VIII-16. It can be seen that the 1 signal level is reduced from that observed in Figure VIII-10 (from 2.9 volts to 2.5 volts) and the 0 signal level is increased from 0.5 volt to 0.7 volt. These results would be those expected from a radiation exposure of the device to the specified fluence level.

```
                    ELEMENTS
F1.A-A-A-A-A-A-D-D-D-D-D-V-0=MODEL RSN54L57 (CHANGE P4=PNVT)
EA.0-A=FGEN(0.,3.,0.,PR,165.E-9,PF,500.E-9,100,TIME)
ED.0-D=FGEN(0.,3.,0.,PR,500.E-9,PF,1000.E-9,100,TIME)
R2.V-3=4300
C2.V-3=2.6E-12
R3.3-0=750
C3.3-0=15.E-12
D1.V-4=MODEL1N3605(PERM)
R4.4-5=800
R5.6-5=1.
E2.0-6=2.4
                    DEFINED PARAMETERS
PR=15.E-9
PF=15.E-9
PNVT=FNVT(VC1F1,0.4,0.2)
                    OUTPUTS
EA.ED.PLOT
                    RUN CONTROLS
START TIME = 0.
MAXIMUM PRINT POINTS = 201
COMPUTER TIME LIMIT = 5.5
STOP TIME=1999.E-9
END

SYSTEM NOW ENTERING SIMULATION
```

Figure VIII-15. Neutron Radiation Test Circuit Description

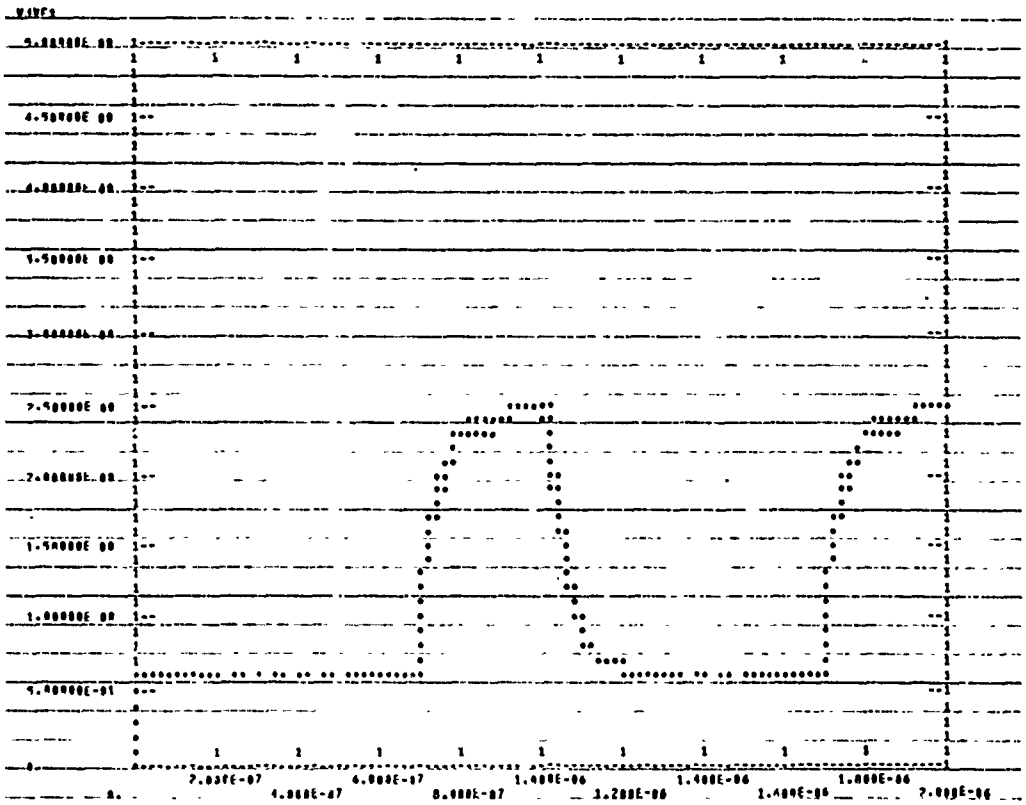


Figure VIII-16. Device Response to Neutron Radiation

SECTION IX

HARRIS HA2700 OPERATIONAL AMPLIFIER

The Harris Semiconductor HA2700 Operational Amplifier is a radiation-resistant integrated circuit. No schematic representation or frequency response data for the device is available from the manufacturer. However, the published electrical characteristics are shown in Figure IX-1.

ABSOLUTE MAXIMUM RATINGS

Maximum ratings are limiting values above which permanent damage may occur.

Voltage Between V^+ and V^- Terminals . . . . . +44.0 Volts
Differential Input Voltage . . . . . ±18.0 Volts
Internal Power Dissipation 300mW
Storage Temperature Range . . . . . $-65^oC \leq TA \leq +150^oC$

ELECTRICAL CHARACTERISTICS

$V^+ = +15.0$ V.D.C. $V^- = -15.0$ V.D.C.

PARAMETER	TEMP	HA 2700 -55° to +125°C			HA 2704 -25°C to +85°C			HA 2705 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		0.5	3.0		0.5	0		1.0	5.0	mV
(Note 1)	Full		1.0			1.0			2.0		mV
Bias Current	+25°C		5.0	[illegible]		5.0	200		5.0	400	nA
	Full		100			100			100		nA
Offset Current	+25°C		2.5			2.5			2.5		nA
	Full		5.0			5.0			5.0		nA
Common Mode Range	Full		±11			±11			±11		V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Notes 2 & 3)	+25°C		2M			2M			2M		V/V
Common Mode Rejection Ratio (Note 4)	Full		106			106			106		dB
Gain Bandwidth Product (Note 2)	+25°C		1.0			1.0			1.0		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 2)	Full		±13			±13			±13		V
Output Current (Note 3)	+25°C		20			20			20		mA
TRANSIENT RESPONSE											
Slew Rate (Note 2)	+25°C		20			20			20		V/μs
Settling Time (0.1%) (Notes 2 & 6)	+25°C		10			10			10		μs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		7.5	15.0		7.5	15.0		7.5	15.0	μA
Power Supply Rejection Ratio (Note 5)	Full		100			100			100		dB

NOTES:

(1) Can be adjusted to zero with 1 megohm pot between Pins 1 and 8, tap to 7. CAUTION Device may be destroyed by shorting Pins 1 or 8 to any other pin or voltage while power is applied.

(2) $R_L = 2K$, $C_L = 100pF$

(3) $V_O = \pm 10.0$ Volts

(4) $V_{CM} = \pm 5$ Volts

(5) $V_{SUP} = \pm 10.0$ Volts to ± 20.0 Volts

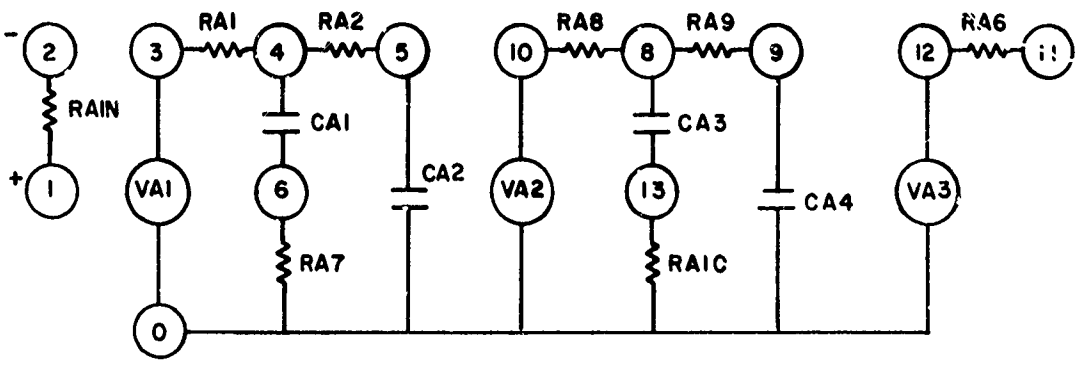
(6) Noninverting, unity gain, output voltage swing is 10.0 Volts

Figure IX-1. Published Electrical Characteristics

A. MODEL DEVELOPMENT

1. LINEAR MODEL

Two different models have been developed for this device. The first, for use with linear programs is shown in Figure IX-2. Figure IX-3 shows the open loop gain measured in the laboratory for the device and the computer analysis results for the model using the CORNAP circuit analysis program. The circuit was also analyzed in the unity gain configuration; the computer circuit description for the analysis is shown in Figure IX-4 and the analysis results in Figure IX-5.



RA1 - CA1 - RA7	POLE @ 0.7 Hz
RA2 - CA2	POLE @ 35 kHz
RA8 - CA3 - RA10	POLE @ 5 kHz
RA9 - CA4	POLE @ 400 kHz
RA7 - CA1	ZERO @ 2.5 kHz
RA10 - CA3	ZERO @ 50 kHz

Figure IX-2. HA 2700 Model - Linear Model

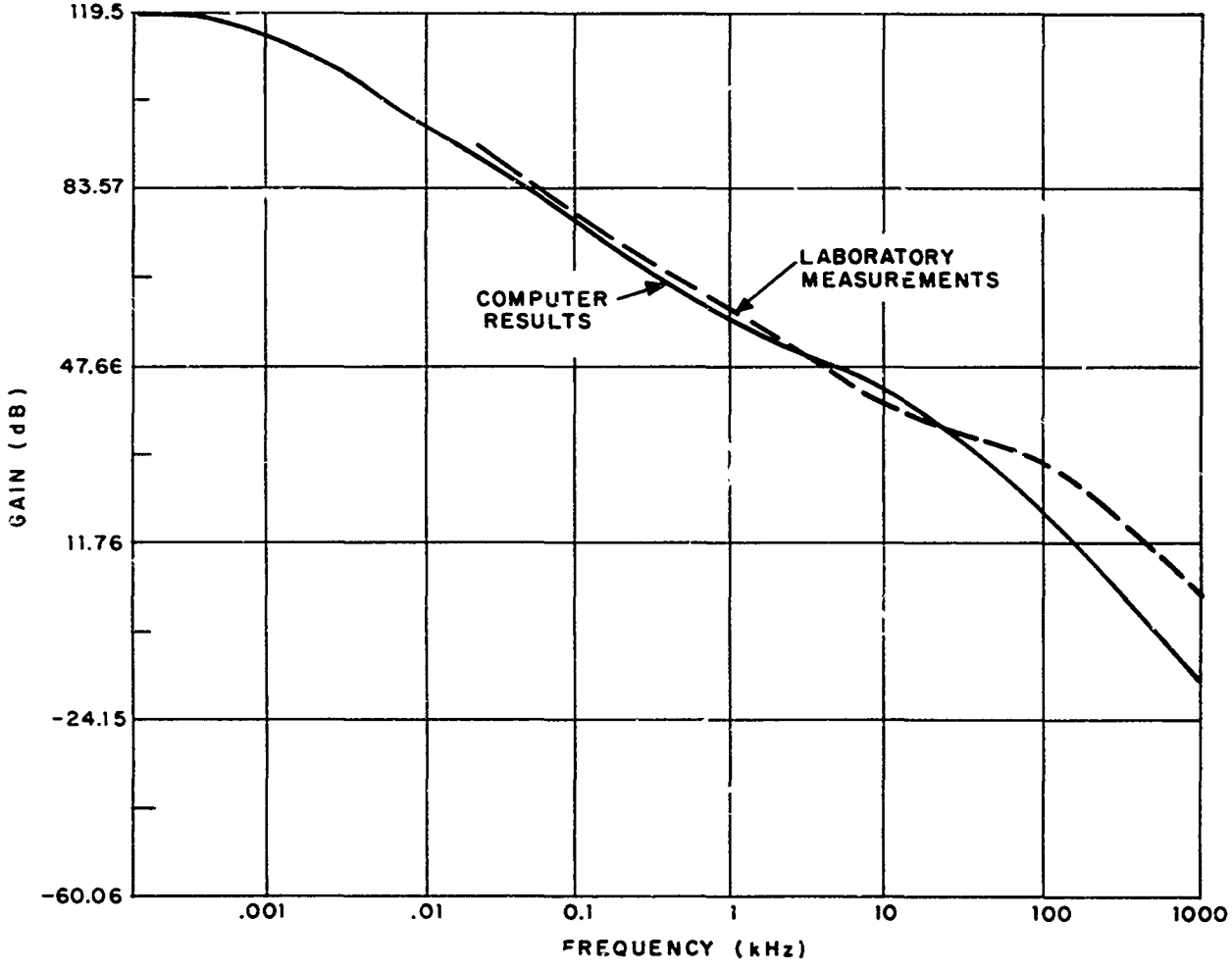


Figure IX-3. Open Loop Gain - Bode Plot

```
12:43     02087 2          ELAPSED TIME =          0  SECONDS

'HA2700 OP AMP  0133T VERSION MODIFIED'
V1,7,0
R4,7,1,50.
R2,11,2,10.E3
C1,11,0,100.E-12,+V
R3,11,0,2000.
RAIN,1,2,1.E6
VA1,3,0,1.,V,RAIN
RA1,3,4,100.
CA1,4,6,2280.E-6
RA7,6,0,.028
RA2,4,5,100.E3
CA2,5,0,45.E-12
VA2,10,0,1.,V,CA2
RA8,10,8,900.
CA3,8,13,32.E-9
RA10,13,0,50.
RA9,8,9,100.E3
L1,9,14=2.E-6
CA4,14,0=4.E-12
VA3,12,0,1.E6,V,CA4
RA6,12,11=100.
FSCALE=1.E7
RSCALE = 1.E6
LOGEREQ=10,.1,1.E7
TIME RESPONSE,LAPLACE,10.,1.E-6,.01E-6
EXECUTE

THIS NETWORK HAS BEEN SCALED FOR COMPUTATION BY THE FOLLOWING FACTORS

 FREQUENCY 1.0000000E 07 RADIANS/SEC.     IMPEDANCE 1.0000000E 06 OHMS
     EXP UNDERFLO  AT LOCATION      064651
```

Figure IX-4. Computer Description - Linear Model

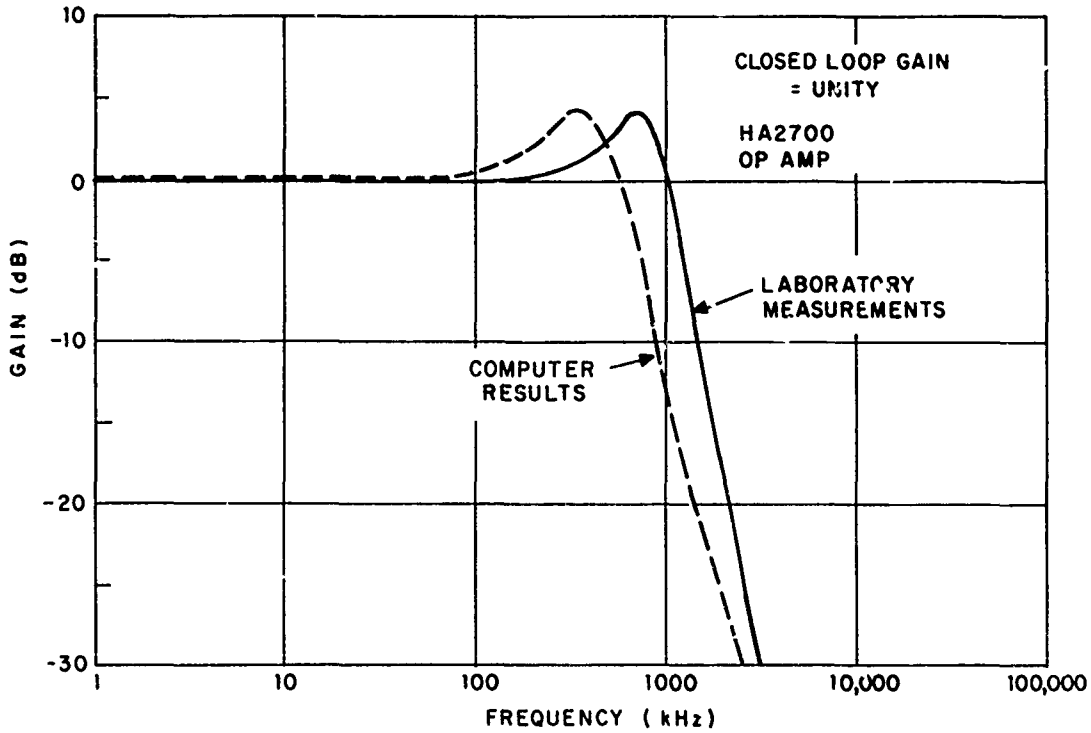
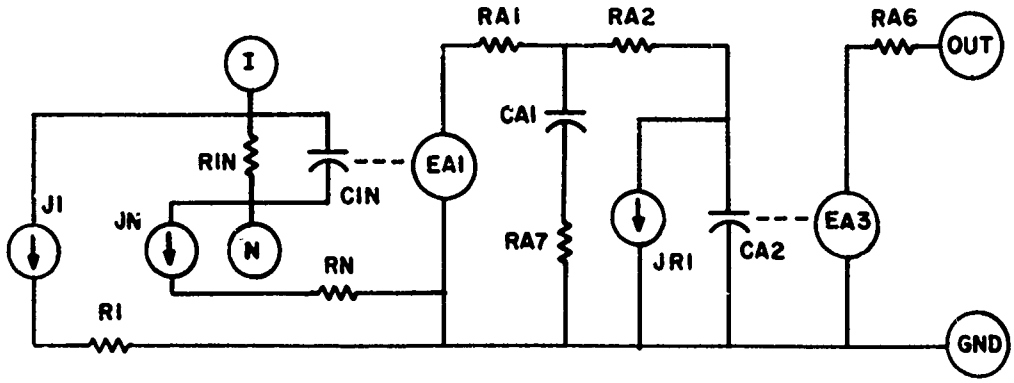


Figure IX-5. Close Loop Gain - 0 dB - Bode Plot

2. NONLINEAR MODEL

The model that has been developed for use with the SCEPTRE circuit analysis program is shown in Figure IX-6. It will be noted that this model is simpler than that used for the linear programs. The reduction in the quantity of elements needed results primarily from a desire to improve computer analysis time when an iterative analysis procedure is used. Experience has established that only the low frequency poles and zeros are required for this type of nonlinear model. Therefore the entire high frequency network has been eliminated from the model. Also, since the time response of the device is dependent upon the input impedance, capacitor C_{IN} is included in the model to duplicate observed conditions. The current sources JI and JN and their associated resistors RI and RN, are incorporated in the model to accommodate the limitations of SCEPTRE as well as in anticipation of including offset current conditions in future work. The computer model description is shown in Figure IX-7.



EA1 = f (GAIN, VCIN)
EA3 = f (VCA2, FOSC)
FOSC = f (INPUT SIGNAL)

Figure IX-6. HA 2700 Model - Non-Linear Model

```
MODEL HA2700(N-I-OUT-GND)
ELEMENTS
J1,I-II=0.
R1,II-GND=1.E-3
JN,N-NN=0.
RN,NN-GND=1.E-3
RIN,N-I=1.E6
CIN,N-I=1.E-12
EA1,GND-3=X1((2.E6-P4)*VCIN)
RA1,3-4=100.
CA1,4-6=2280.E-6
RA7,6-GND=.025
RA2,4-5=100.E3
CA2,5-GND=45.E-12
EA3,GND-12=Q1(VCA2,P1,P3)
RA6,12-OUT=100.
JO,OUT-GND=0.
FUNCTIONS
Q1(A,B,C)=(A+B*C)
DEFINED PARAMETERS
P1=4.
P2=10.
P3=FOSC(VJN,TIME)
P4=0.
OUTPUTS
VJN,PLOT
P3,PLOT
P1,VCIN,VCA2,EA3,VJO,PLOT
```

Figure IX-7. Computer Description - Non-Linear Model

Both published data and laboratory measurements indicate the presence of high frequency oscillations which occur during a change in signal level when the device is connected in a unity gain configuration. Measurements indicate that the frequency of the oscillations is between 8 and 12 megahertz. For the sake of visual clarity, the frequency used in the model is set at approximately 5 megahertz. The presence of the oscillatory signal is established by the subprogram FOSC shown in Figure IX-8.

The oscillation generator, FOSC, produces a constant amplitude sine wave (fixed frequency = 4.78 MHz) when the slope of the input signal at the non-inverting input terminal exceeds a threshold level of 1×10^6 volts/sec. A time function is included in the generator to establish an arbitrary time that is equivalent to time-equal-to-zero conditions, when the threshold of any signal exceeds the defined slope. The slope of the input (DVDT) is determined by comparing the incremental change in voltage, at the input terminal, to the integration step size time change. As long as the absolute value of DVDT is less than the threshold, the oscillator output is zero and the time delay, TØ, is reset to the present time. When the absolute value of DVDT exceeds the threshold, the oscillator output is a constant amplitude sine wave delayed by TØ. The function generator output is established only for inputs to the non-inverting terminal of the op amp, but can be extended, in similar fashion, to the inverting input. The FORTRAN flow charts associated with these functions as well as the radiation response are shown in Appendix IX-A.

```
1948T 02   02-07-72    12.395        OSCILLATION GENERATOR

  1        CI OSC            OSCILLATION GENERATOR
  2                  FUNCTION FOSC(VJN,TIME)
  3                  IF(TIME-0.) 1,1.2
  4          1       OSC=0.
  5                  T0=0.
  6                  XVJN=VJN
  7                  XTIME=TIME
  8          2       IF(TIME-XTIME) 20,20,10
  9         10       DVDT=ABS((VJN-XVJN)/(TIME-XTIME))
 10                  IF(DVDT-1.E6) 12,12,11
 11         11       OSC=SIN(30.E6*(TIME-T0))
 12                  GO TO 20
 13         12       OSC=0.
 14                  T0=TIME
 15         20       FOSC=OSC
 16                  XVJN=VJN
 17                  XTIME=TIME
 18         25       RETURN
 19                  END

     23585 WORDS OF MEMORY USED BY THIS COMPILATION
```

Figure IX-8. Model Subprogram

B. MODEL VERIFICATION

To duplicate the observed performance of the amplifier when it is connected in a unity gain configuration, the circuit was described to the computer as shown in Figure IX-9. Applied to the circuit was an input signal (Figure IX-10) that rises from 0 volts to 5 volts in 0.5 microsecond, and returns at the same rate. The response of the device is shown in Figure IX-11. The photographically recorded laboratory signal which this output is intended to duplicate is shown in Figure IX-12. It can be seen that the computer response closely simulates the observed performance.

```
TIMING TEST CIRCUIT HA2700
SAVED AS HA2700A
ELEMENTS
A1,3-2-6-GND=MODEL HA2700
E1,GND-3=FGEN(0.,5.,0...5E-6,1.E-6,.5E-6,5.E-6,5.,TIME)
R2,6-2=1.
RL,6-GND=2.E3
RUN CONTROLS
STOP TIME = 2.E-6
COMPUTER TIME LIMIT = 9.
MAXIMUM PRINT POINTS = 100.
MAXIMUM INTEGRATION PASSES = 75000
MINIMUM STEP SIZE = 1.E-15
OUTPUTS
E1,PLOT
XSTPSZ,PLOT
END
```

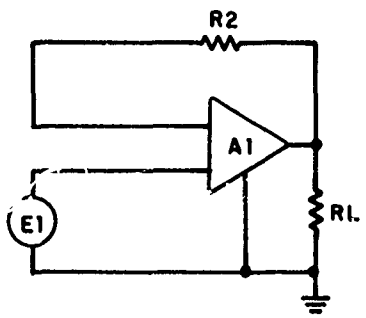


Figure IX-9. Test Circuit and Computer Description

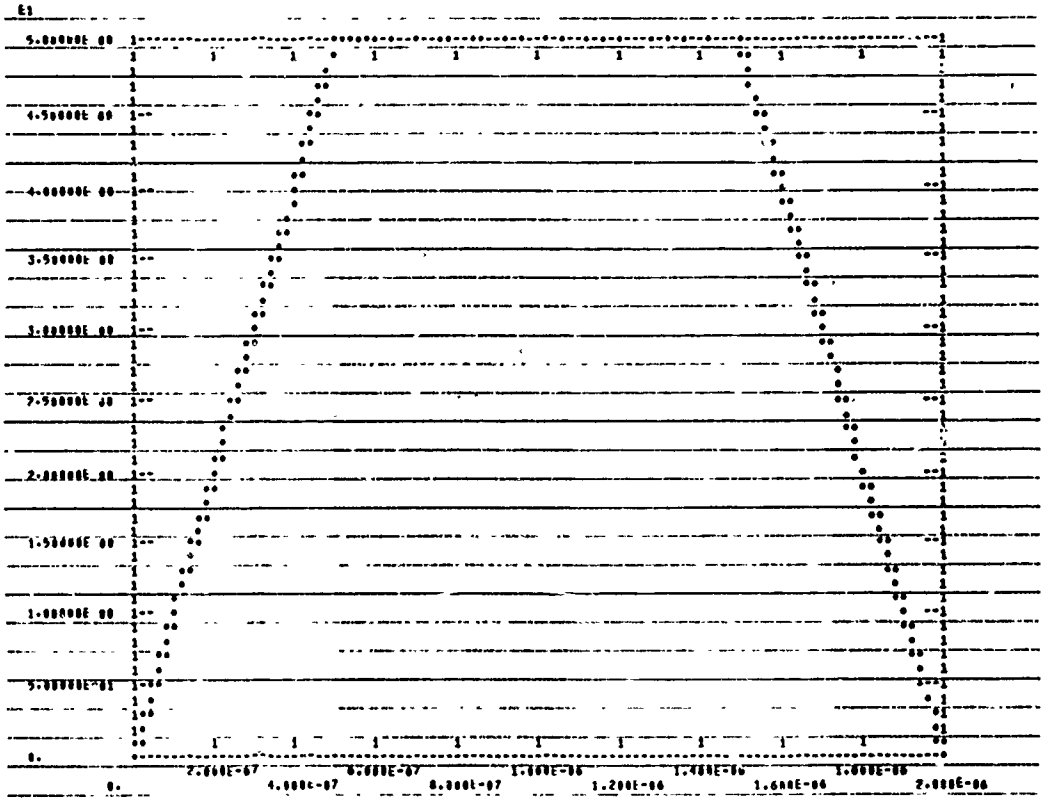


Figure IX-10. Input Signal

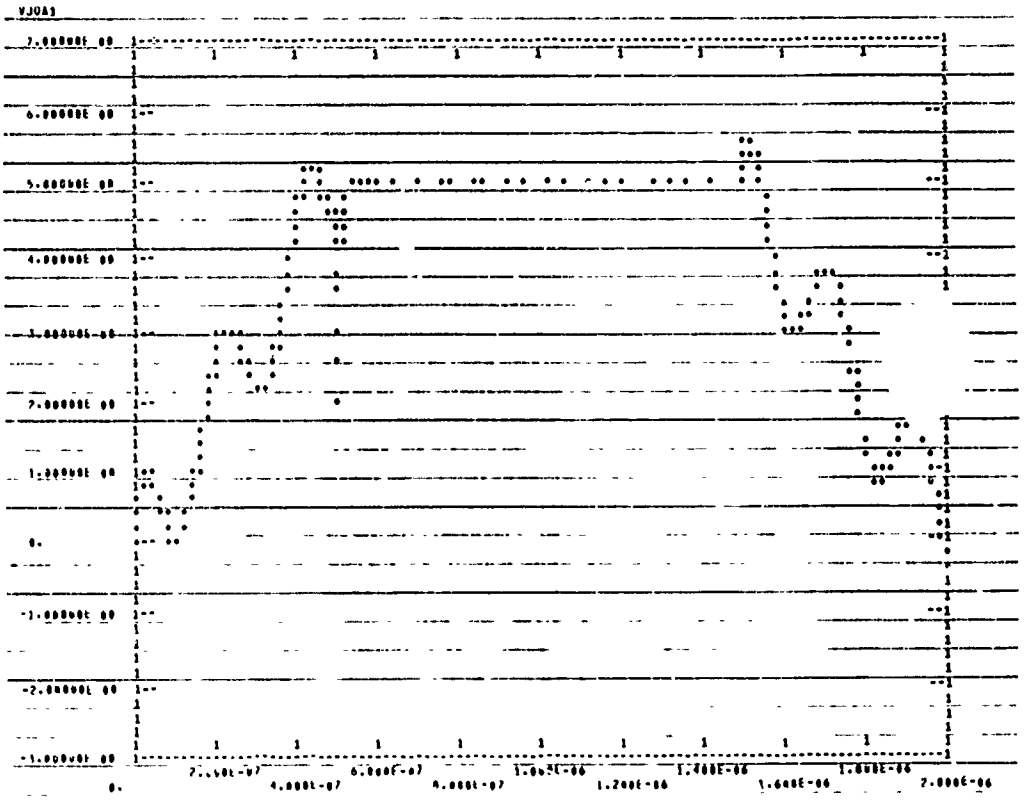
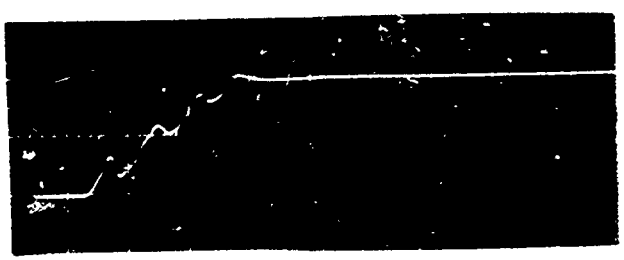


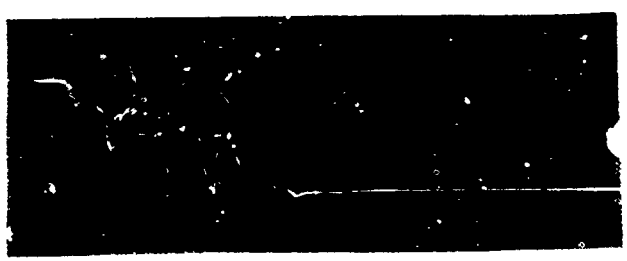
Figure IX-11. Output Response

Input Signal Leading Edge

Input Signal Trailing Edge



Output Signal Leading Edge



Output Signal Trailing Edge

Figure IX-12. Observed Device Response

C. RADIATION EFFECTS

1. GAMMA RADIATION

Exposing the device to a nuclear radiation environment may affect normal performance by causing the output signal level to vary. When exposed to pulsed ionizing rays (gamma radiation) at dose rate levels of approximately $3 \times 10^{+10}$ rads (Si)/second, the performance is only momentarily affected. Extensive testing was done by the General Electric Company. The test report, with photographic recording of the results, is included in Appendix IX-B.

When the amplifier is connected in the same voltage follower configuration as described earlier, but with a constant voltage applied to the non-inverting input terminal, the output remains constant. If the voltage is established at 5 volts and the device exposed to a gamma transient, the output is perturbed.

When this condition is simulated in the computer, the output change is as shown in Figure IX-13. This response is intended to be a copy of Shot 5410 in Appendix IX-B. The computer output is obtained by means of subprogram FGAM, which is shown in Figure IX-14.

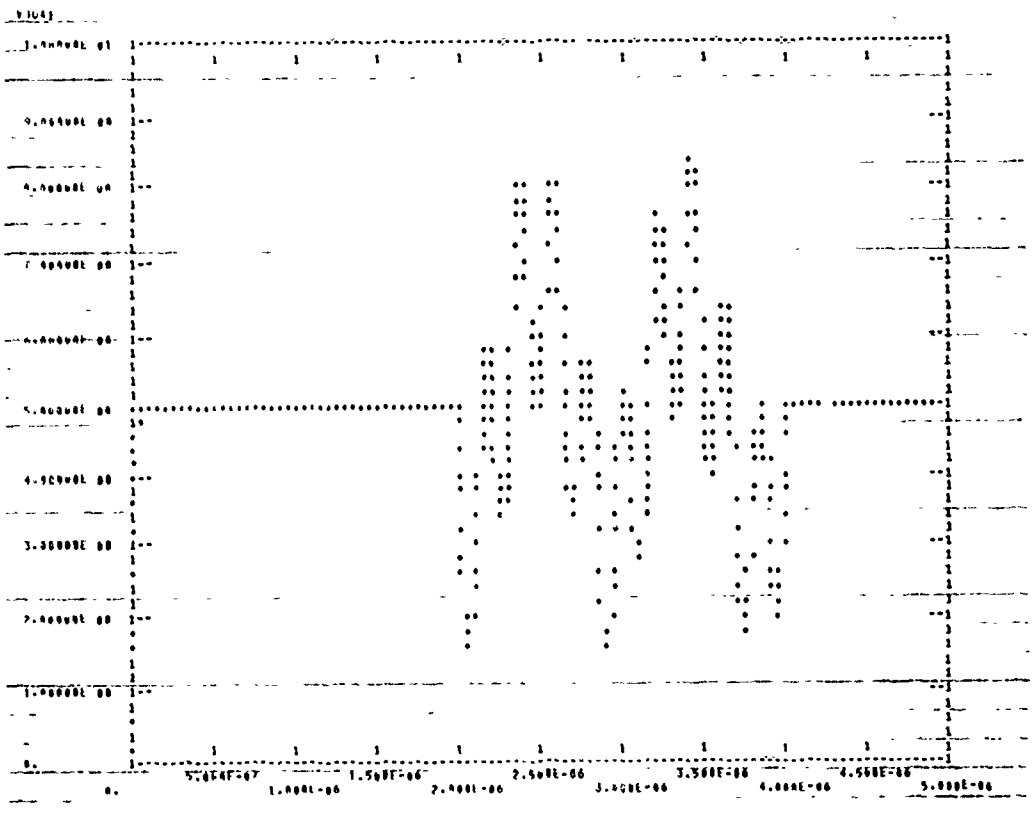


Figure IX-13. Output Response to Gamma Radiation

```
1246T 05  02-11-72   14.706        GAMMA FUNCTION SIMULATOR

      1        CGAM              GAMMA FUNCTION SIMULATOR
      2                  FUNCTION FGAM(GAM,TIME,XMULT)
      3                  IF(TIME-0.) 1,1,2
      4            1     T0=TIME
      5                  NBURST=0
      6                  XGAM=GAM
      7                  XTIME=TIME
      8                  GAMMA=0.
      9            2     IF(TIME-XTIME) 20,20,10
     10           10     DGAMDT=(GAM-XGAM)/(TIME-XTIME)
     11                  IF(DGAMDT.GT.0..AND.GAM.GT.0.2) NBURST=1
     12                  IF(1-NBURST) 11,12,11
     13           11     GAMMA=0.
     14                  T0=TIME
     15                  GO TO 20
     16           12     IF(TIME-(T0+2.E-6)) 15,15,16
     17           15     GAMMA=XMULT*(SIN(30.E6*(TIME-T0))+SIN(7.E6*TIME))
     18                  GO TO 20
     19           16     GAMMA=0.
     20                  NBURST=0
     21           20     FGAM=GAMMA
     22                  XGAM=GAM
     23                  XTIME=TIME
     24                  RETURN
     25                  END
```

Figure IX-14. Gamma Function Subprogram

The gamma simulator, FGAM, produces an oscillatory burst when a gamma pulse is simulated in the computer circuit description. A function is included in the generator to establish an arbitrary time that is equivalent to time-equal-to-zero-conditions, when the leading edge of a gamma pulse exceeds a threshold level of 0.2 volt. When the slope of the gamma pulse (DGAMDT) is positive and the level of the gamma signal exceeds the threshold level, the burst generator flag (NBURST) is set to a 1.

The integration time immediately prior to NBURST changing to a 1 is saved as TØ is summed with a laboratory observed burst width to determine the TIME when the burst generator is to be turned off (NBURST = 0). The interval of time during which NBURST is equal to 1, FGAM, is a "beat" signal which is the sum of two periodic sine waves (1.11 MHz and 4.9 MHz) and for all other TIME is zero.

To incorporate this effect into the model, JR1 is changed from a zero valued current source to a dependency upon FGAM, as shown in Figure IX-15. The means of causing the circuit to respond to a gamma pulse is shown in Figure IX-16, which is the computer circuit description. In the amplifier callout, PGAM, one of the arguments in FGAM, is changed to be equal to TGAM which represents the presence of a 20 nanosecond gamma transient at 6.010 microseconds.

The computer results shown in Figure IX-13 indicates reasonable agreement with observed responses of this type of device.

```
MODEL HA2700(N-I-OUT-GND)
ELEMENTS
JI,I-II=0.
RI,II-GND=1.E-3
JN,N-NN=0.
RN,NN-GND=1.E-3
RIN,N-I=1.E6
CIN,N-I=1.E-12
EA1,GND-3=X1((2.E6-P1)*VCIN)
RA1,3-4=100.
CA1,4-6=2280.E-6
RA2,6-GND=.028
RA2,4-5=100.E3
CA2,5-GND=45.E-12
JR1,5-GND=FGAM(PGAM,TIME,.01)
EA3,GND-12=Q1(VCA2,P1,P3)
RA6,12-OUT=100.
JO,OUT-GND=0.
FUNCTIONS
Q1(A,B,C)=(A*B*C)
DEFINED PARAMETERS
P1=4.
PGAM=0.
P3=FOSC(VJN,TIME)
P4=0.
OUTPUTS
VJN,PLOT
P3,PLOT
P1,VCIN,VCA2,EA3,VJO,PLOT
JR1,PLOT
```

Figure IX-15. Model Description With Gamma Effects

```
GAMMA TEST
SAVED AS HA2700A
ELEMENTS
A1,3-2-6-GND=MODEL HA2700 (CHANGE PGAM=TGAM)
E1,GND-3=5.
R2,6-2=1.
RL,6-GND=2.E3
FUNCTIONS
TGAM=0.,0., 2.E-6,0., 2.E-6,.5, 2.01E-6,1., 2.02E-6,.5,2.02E-6,0.
RUN CONTROLS
STOP TIME = 5.E-6
COMPUTER TIME LIMIT = 9.
MAXIMUM PRINT POINTS = 100
MAXIMUM INTEGRATION PASSES = 75000
MINIMUM STEP SIZE = 1.E-15
OUTPUTS
E1,PLOT
XSTPSZ,PLOT
END
```

Figure IX-16. Gamma Radiation - Test Circuit Description

2. NEUTRON RADIATION

When a device is exposed to neutron radiation conditions, its performance may be degraded either temporarily or permanently. The degree of degradation as well as the device recovery time, for those conditions which permits recovery, depends upon the exposure level.

Exposure of circuits to a fluence level of 1.2×10^{14} results in a reduction of the device gain. Although no precise data is available at this time, it is estimated that exposure of the amplifier to the referenced fluence level will result in a gain reduction of about 10; i.e., the gain will be reduced from 2 million to 200,000. This latter value was used in the model to demonstrate that the method of reflecting device behavior to neutron radiation atmospheres is correct, even if the numerical results prove to be slightly in error.

The method for incorporating this capability into the model is shown in Figure IX-17. The value of the voltage EA1 is changed from a dependency upon the device gain and the voltage across the capacitor, CIN, to a dependency that also includes the fluence level. The fluence level is defined in the model as P4, which under normal conditions is set equal to zero. When radiation exposure performance is desired, P4 is redefined to have a value of 1.8×10^{6}, as indicated under "rerun description" on Figure IX-18.

Since the gain of the device is still high (200,000), the output signal would still be expected to closely resemble that obtained under non-radiation conditions. Figure IX-19 indicates that this does occur. However, a comparison between this figure and Figure IX-11 shows the effects of the reduced gain condition. It is seen that the phase of the oscillations present on the rising and falling edges of the output signal are different; the time required for the signal to stabilize at 5 volts is about 0.8 microseconds, compared to less than 0.6 microseconds for normal operation; and the return to a zero signal level is progressing at a much slower rate. Thus, the expected results of reduced performance capability are demonstrated by the model.

```
MODEL HA2700(N-I-OUT-GND)
ELEMENTS
JI,I-II=0.
RI,II-GND=1.E-3
JN,N-NN=0.
RN,NN-GND=1.E-3
RIN,N-I=1.E6
CIN,N-I=1.E-12
EA1,GND-3=XI((2.E6-P4)*VCIN)
RA1,3-4=100.
CA1,4-6=2280.E-6
RA7,6-GND=.028
RA2,4-5=100.E3
CA2,5-GND=45.E-12
EA3,GND-12=Q1(VCA2,P1,P3)
R36,12-OUT=100.
JO,OUT-GND=0.
FUNCTIONS
Q1(A,B,C)=(A+B*C)
DEFINED PARAMETERS
P1=4.
P2=10.
P3=FOSC(VJN,TIME)
P4=0.
OUTPUTS
VJN,PLOT
P3,PLOT
P1,VCIN,VCA2,EA3,VJO,PLOT
```

Figure IX-17. Model Description With Neutron Effects

```
TIMING TEST CIRCUIT HA2700
SAVED AS HA2700A
ELEMENTS
A1,3-2-6-GND=MODEL HA2700
E1,GND-3=FGEN(0.,5.,0.,.5E-6,1.E-6,.5E-6,5.E-6,5.,TIME)
R2,6-2=1.
RL,6-GND=2.E3
RUN CONTROLS
STOP TIME = 2.E-6
COMPUTER TIME LIMIT = 9.
MAXIMUM PRINT POINTS = 100.
MAXIMUM INTEGRATION PASSES = 75000
MINIMUM STEP SIZE = 1.E-15
OUTPUTS
E1,PLOT
XSTPS7,PLOT
RERUN DESCRIPTION


DEFINED PARAMETERS
P4A1=1.0E6
END
```

Figure IX-18. Neutron Radiation - Test Circuit Description

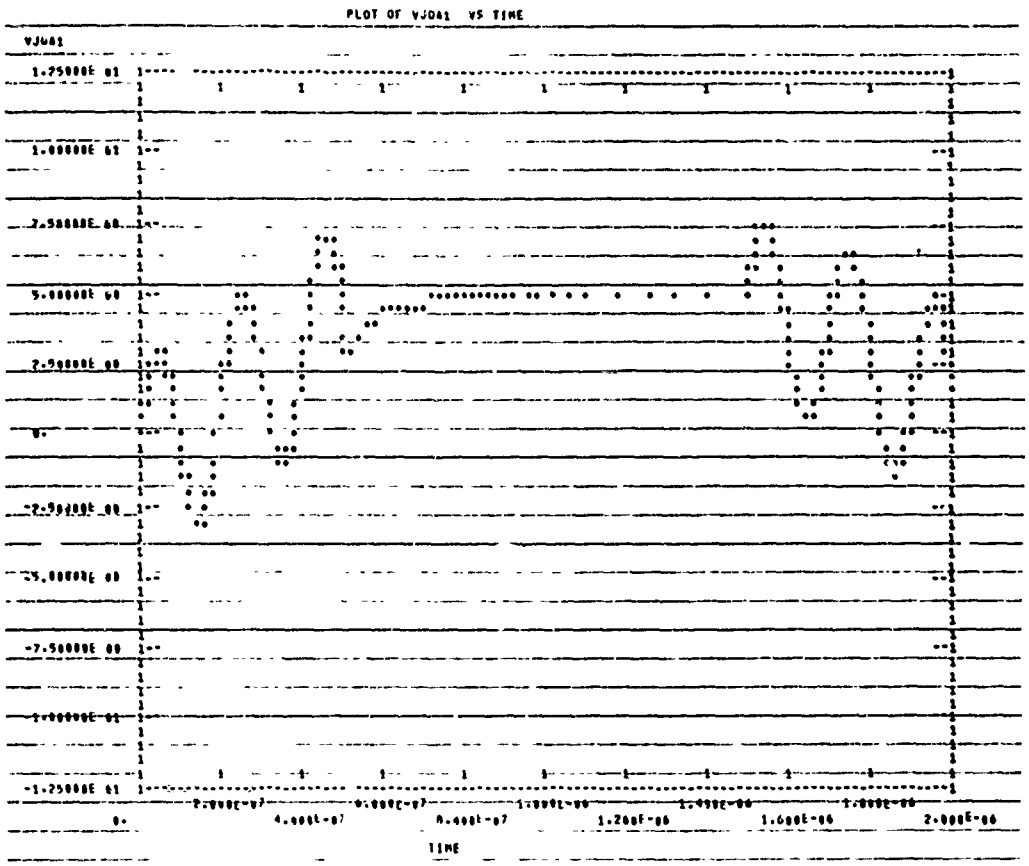


Figure IX-19. Response to Neutron Radiation

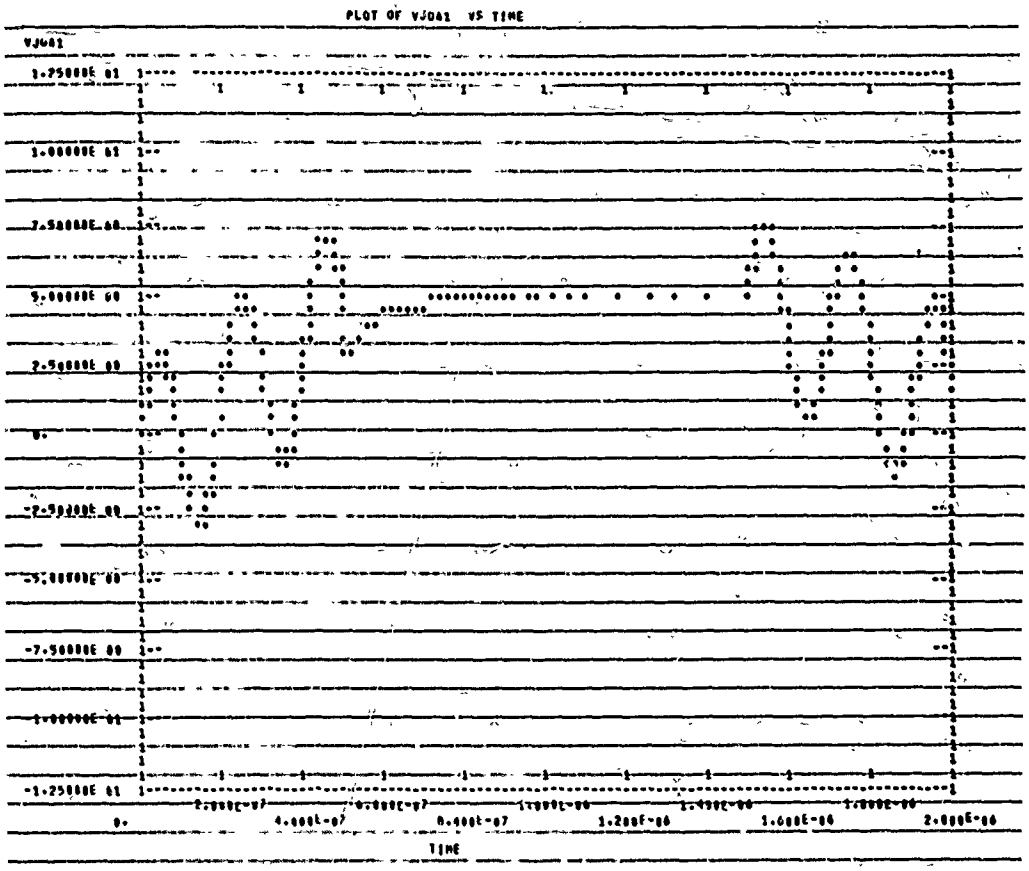


Figure IX-19. Response to Neutron Radiation

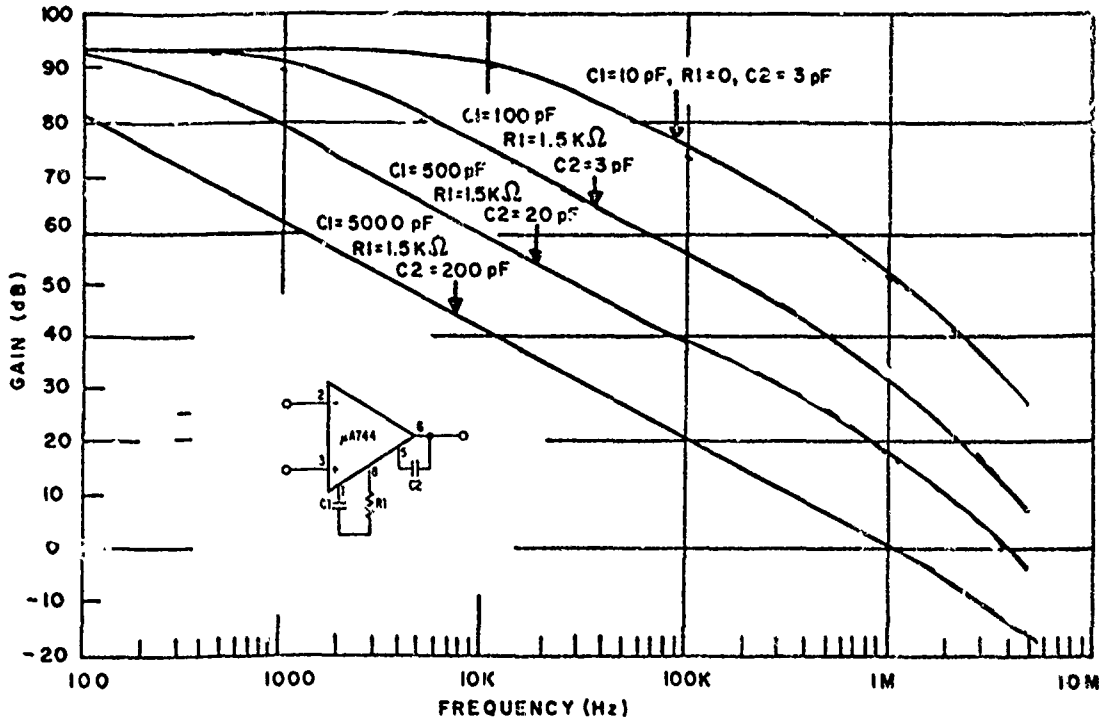


Figure X-2. Op-Amp Frequency Response

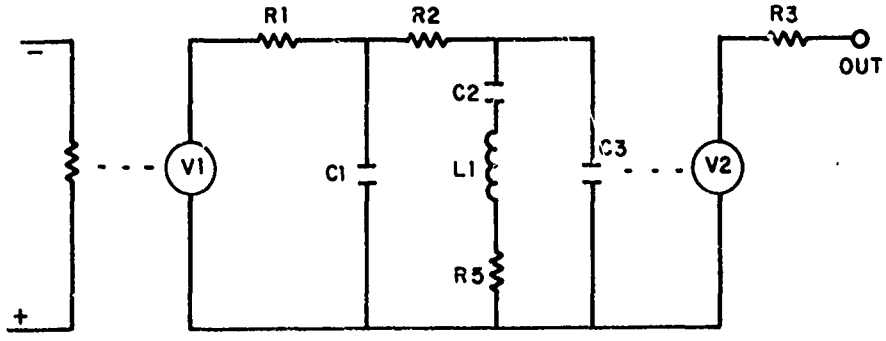


Figure X-3. μA744 Linear Model

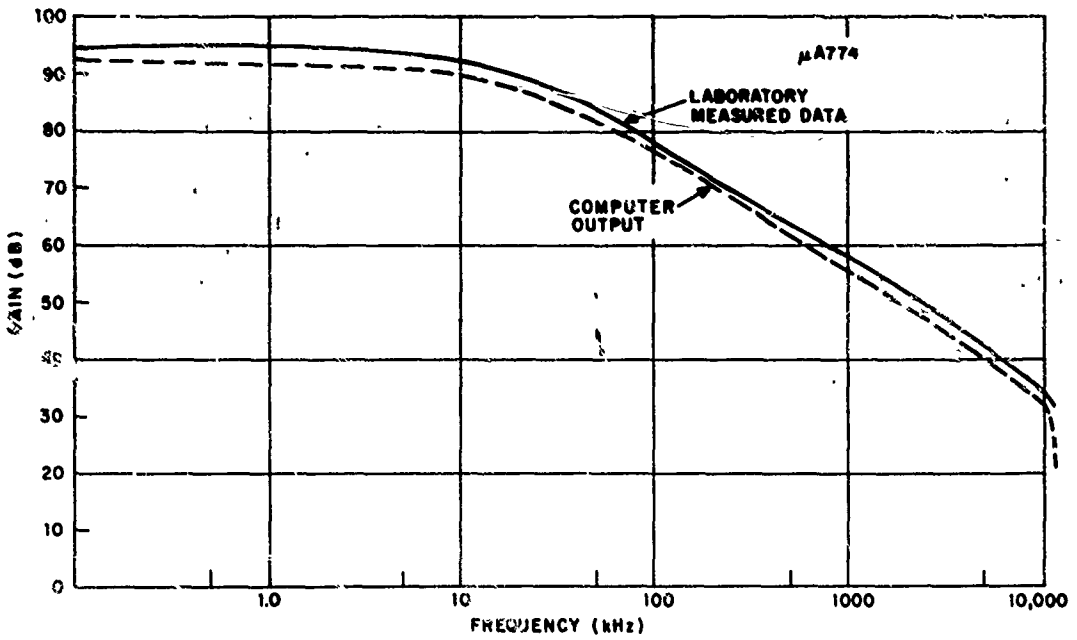


Figure X-4. Open Loop Gain - Bode Plot

```
 10.39    0208/2          ELAPSED TIME =          0  SECONDS

'UA744 OP AMP MODEL AND TEST CIRCUIT'
V1,3,0=1.,V,RA
V2,6,0=5.6E4,V,C5
V,1,0
C1,4,0=1.6E-8
C2,5,8=1.6E-14
RF,2,2=1.E8
R1,2,0=1.E3
RL,2,0=10.E3,+V
RA,1,2=750.E3
R1,3,4=1.E3
R2,4,5=1.E6
R3,14,7=150.
R5,9,0=5.E3
L1,8,9=.1E-3
C3,5,0=0.
R6,6,12=1500.
C5,12,13=1.6E-5
R7,13,0=500.
V3,14,0=1.,V,C4
C4,12,0=0.
LOGFREQ=10,100,1.E6
PRINT DATA
TELETYPE
EXECUTE
```

Figure X-5. Computer Description - Linear Model

2. NONLINEAR MODEL

The model that has been developed for use with the SCEPTRE circuit analysis program is shown in Figure X-6. It will be noted that this model is simpler than that used for the linear programs. The reduction in the number of elements needed for a satisfactory model results primarily from a desire to improve computer analysis time when an iterative analysis procedure is used. The computer model description for the SCEPTRE analysis program is shown in Figure X-7. The input signal characteristic is shown in Figure X-8, and the device response signal in Figure X-9. It is seen that the slew rate limitation of the device causes a delay before the output signal reaches the input signal level, as well as a delay in returning to the zero input signal level, when the device is connected in a gain-of-10 voltage amplifier circuit. The test circuit schematic and computer description are shown on Figure X-10.

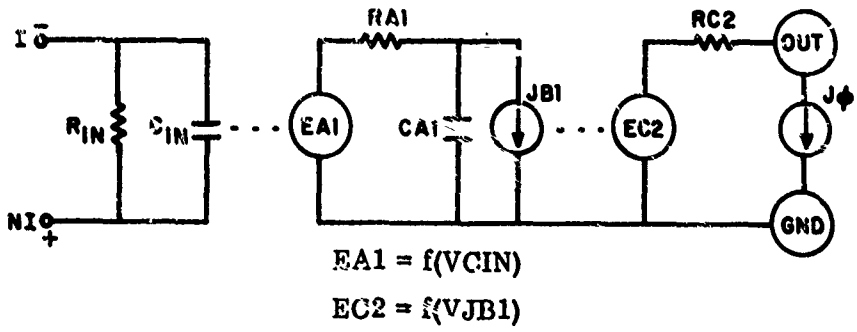


Figure X-6. μA744 Non-Linear Model

```
MODEL UA744(NI-1=OUT-GND)
OPERATIONAL AMPLIFIER
ELEMENTS
RIN,NI-1=750.E3
CIN,NI-1=1.E-12
EA1,GND-3=X1(45000.*VCIN)
RA1,3-4=1.5E3
CA1,4-GND=Q1(VCA1)
JB1,4-GND=0.
EC1,GND-12=X3(VJB1)
RC1,12-OUT=150.
J0,OUT-GND=0.
OUTPUTS
VCIN,CA1,VJB1,VJ0,PLOT
CA1,PLOT
FUNCTIONS
Q1(A)=(32.E-6-30.E-6*ABS(A)/15.)
```

Figure X-7. Computer Description - Non-Linear Model

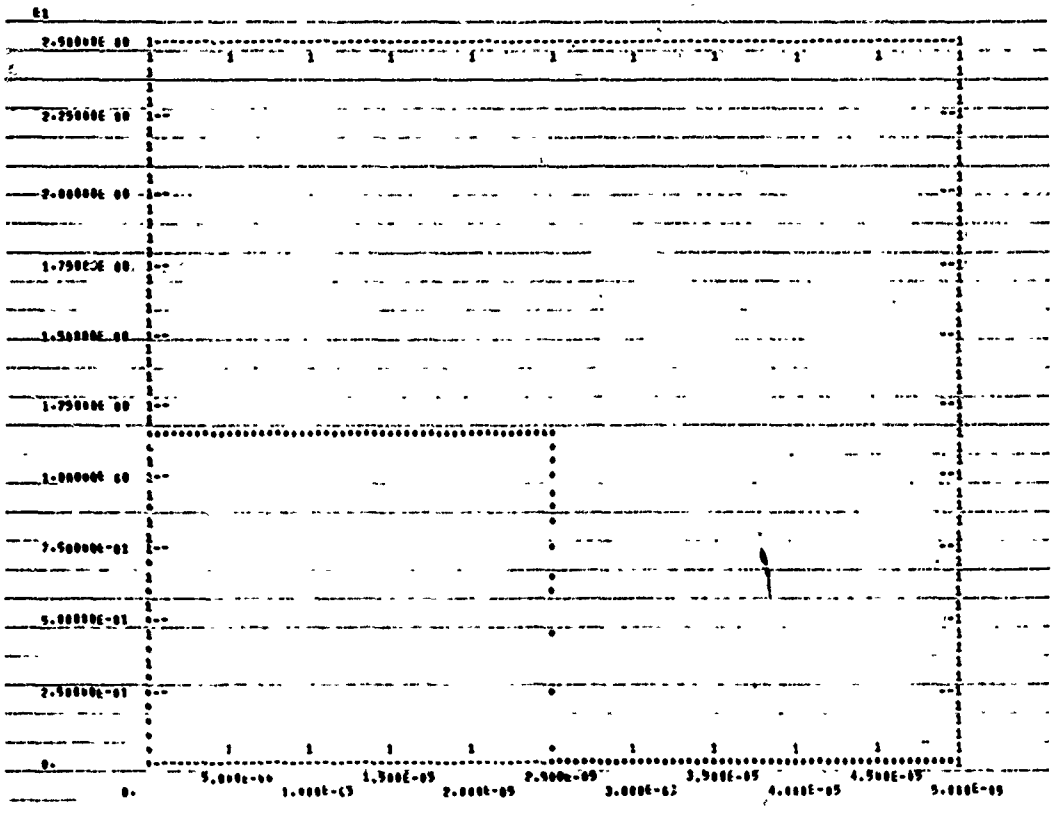


Figure X-8. Input Signal

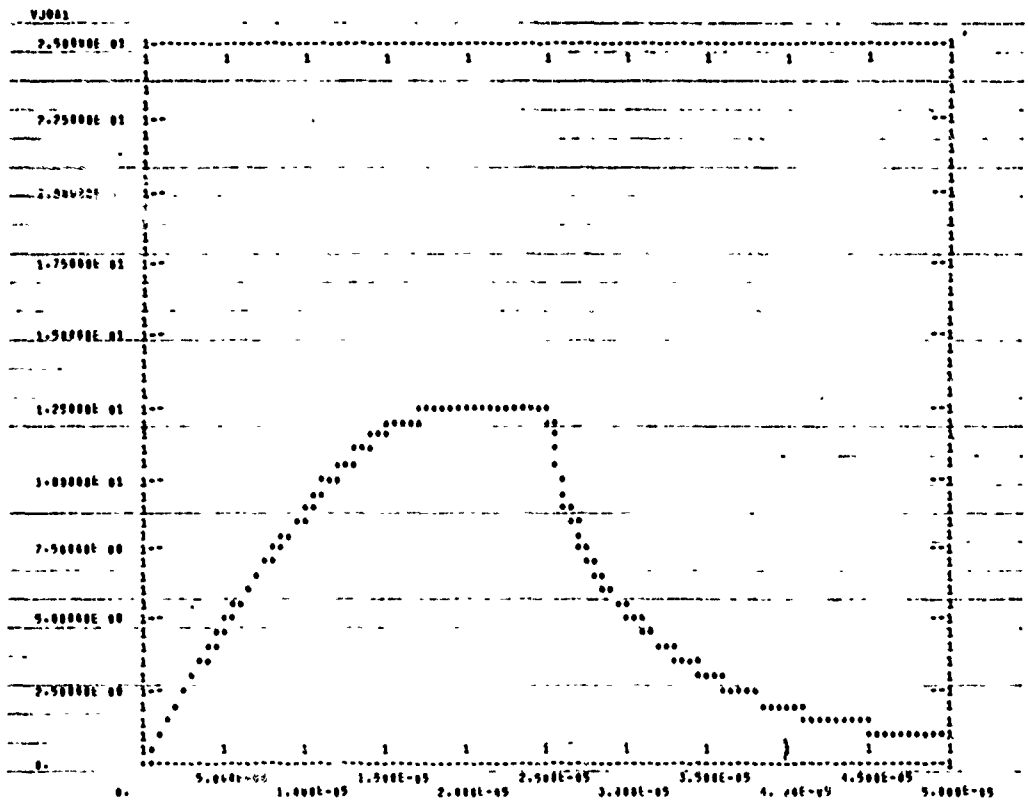


Figure X-9. Output Response

```
                TIMING TEST UA/44
                SAVED UNDER FILE UA/44
                CLOSED LOOP GAIN 20 DB
ELEMENTS
E1,GND-1=PGEN(0.,1.15.0.,5.E-8,25.E-6,5.E-8,50.E-6,5.,TIME)
A1,3-2-4-GND=MODEL UA/44
R1, 1-3=50.
RF,4-2=100.E3
RI,2-GND=10.E3
RL,4-GND=2.E3
CL,4-GND=100.E-12
OUTPUTS
E1,PLOT
RUN CONTROLS
MAXIMUM PRINT POINTS = 100
COMPUTER TIME LIMIT=5.
STOP TIME = 49.99E-6
END

SYSTEM NOW ENTERING SIMULATION
```

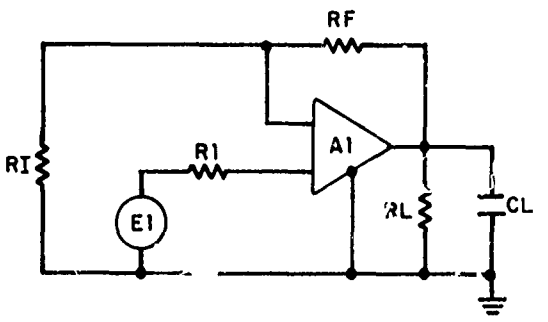


Figure X-10. Test Circuit and Computer Description

B. RADIATION EFFECTS

1. GAMMA RADIATION

Exposing the device to a nuclear radiation environment may affect normal performance by causing the output signal level to vary. When exposed to pulsed ionizing rays (gamma radiation) at dose rate levels of approximately 3×10^{10} rads (Si)/second, the performance is only momentarily affected. Extensive testing was done by the General Electric Company. The test report, with photographic recording of the results, is included as Appendix X-B.

The tests were conducted with a fixed dc input signal on the non-inverting terminal. The circuit was then exposed to a gamma pulse and the results photographically recorded. For radiation test condition #7 (i.e., a gain-of-10 circuit configuration with a 1.15 volt input signal), it is seen that the device goes into negative saturation. For the many devices tested, delays between a minimum of 5 microseconds to a maximum of 30 microseconds were observed, before the device started out of saturation.

The computer description for including this radiation effect into the model is shown in Figure X-11. The independent current source, JB1, is changed from a zero value to a dependency upon the device response to gamma exposure (Table 1 of Figure X-11), and the time of occurrence of the transient (Table 2). This change is defined as P1 in the computer description.

For the computer analysis, the radiation transient is simulated to occur at 19 microseconds. The input signal, E1, is set to 1.15 volts to simulate the laboratory test conditions. The computer analysis of this circuit is shown in Figure X-12. Considerable variation was observed in the response of devices subjected to these tests. The results showed some devices recovered with almost no delay, at approximately the same rate as shown on Figure X-12, while others had recovery times less than that drawn on the figure. The observed results for the maximum delay device are drawn on this figure. The small, transient recovery pulse drawn on the figure was not present in all devices tested but appears to be partially correlatable with increased delay to recovery.

```
MODEL UA744(NI-I-OUT-GND)
OPERATIONAL AMPLIFIER
ELEMENTS
RIN,NI-I=750.E3
CIN,NI-I=1.E-12
RA1,GND-3=X1((45000.-P2)*VCIN)
RA1,3-4=1.5E3
CA1,4-GND=Q2(VCA1)
JB1,4-GND=P1
RC1,GND-12=Q1(VJB1,T3(VJB1))
RC1,12-OUT=150.
J0,OUT-GND=0.
FUNCTIONS
Q1(A,B) = (A*B)
Q2(A)=(32.E-6-30.E-6*ABS(A)/15.)
T1=0.,160., 1.,800., 2.,1600., 3.,3200.
T2=0.,0., 18.E-6,0., 18.E-6,.5, 19.E-6,1., 20.E-6,.5, 20.E-6,0.
T3=-15.,0., 0.,0., .1,1., 15.,1.
DEFINED PARAMETERS
P1=Q1(T1(VCA1),T2)
P2=0.
OUTPUTS
VCIN,EA1,VJB1,VJ0,PLOT
P1(GAMMA),PLOT
```

Figure X-11. Model Description With Gamma Effects

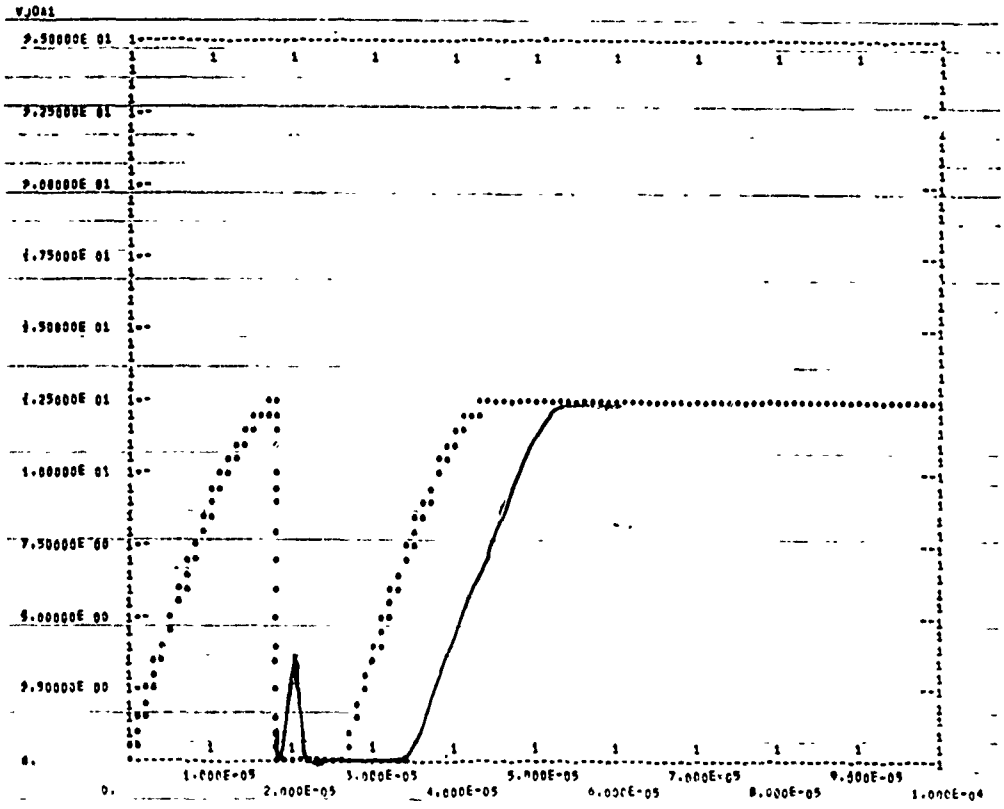


Figure X-12. Output Response to Gamma Radiation

It should be noted that the model description as it exists is limited to providing proper gamma radiation response for either a positive input signal on the non-inverting terminal or a negative input signal on the inverting terminal. Further effort will be required to accommodate all input signal/gamma transient combinations. However, the method for incorporating the proper device response has been developed in the existing model.

2. NEUTRON RADIATION

When a device is exposed to neutron radiation conditions, its performance may be degraded either temporarily or permanently. The degree of degradation as well as the device recovery time, for those conditions which permit recovery, depends upon the exposure level.

Exposure of circuits of fluence levels of 1.2×10^4 results in an output level reduction. Data obtained from manufacturer published data and a Fairchild Semiconductor in-house memorandum indicates that a gain reduction, as a result of exposure to a fluence level of 10^{14}, is such as to reduce the gain of the amplifier immediately after exposure to 18000. Figure X-13 shows the published data.

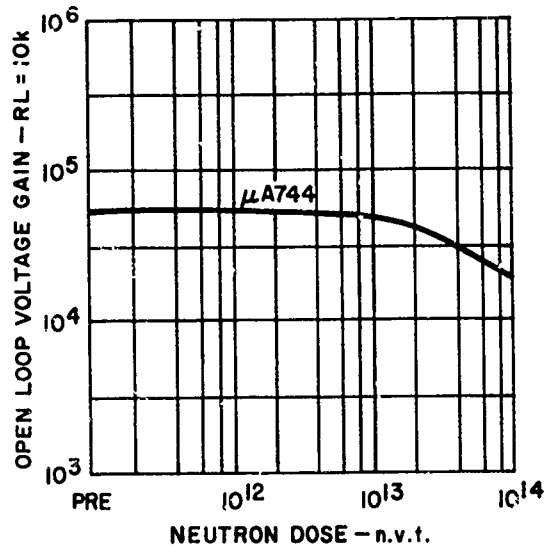


Figure X-13. Effect of Neutron Irradiation on Open-Loop Voltage Gain

The method for incorporating this capability into the model is shown in Figure X-14. The value of the voltage EA1 is changed from a dependency upon the device gain and the voltage across the capacitor, CIN, to a dependency that also includes the fluence level. In this case the gain is reduced to a level of 18000 by changing the expression X1 to include the factor P2. Under no radiation conditions, P2 is set equal to zero; after exposure, it is set equal to 27000. The method to accomplish this is shown in Figure X-15. Under "rerun" conditions, P2 in Figure X-14 is changed from zero to 27000.

Since the level of the output signal for the overall test circuit is controlled by the relationship of resistors RI and RF, it would be expected that the 12.5 signal level observed in Figure X-9 would be unchanged.

Figure X-16 shows the effects of the analysis under the neutron radiation exposure; i.e., reduced gain conditions. It is seen that the time required for the output signal to reach the level of the input signal has been increased to such an extent that it never reaches the 12.5 volt level, when the circuit is subjected to the same condition that resulted in the performance shown in Figure X-9. It is seen that increased time is also required for the device to return to the zero signal level. Thus, the expected result of reduced performance capability is demonstrated by the model.

```
MODEL UA744(NI-I-OUT-GND)
OPERATIONAL AMPLIFIER
ELEMENTS
RIN,NI-I=750.E3
CIN,NI-I=1.E-12
EA1,GND-3=X1((45000.-P2)*VCIN)
RA1,3-4=1.5E3
CA1,4-GND=16.E-6
JB1,4-GND=P1
EC1,GND-12=X3(VJB1)
RC1,12-OUT=150.
JO,OUT-GND=0.
FUNCTIONS
Q1(A,B) = (A*B)
Q2(A)=(32.E-6-30.E-6*ABS(A)/15.)
TABLE 1 = 0.,-1., 1.,-.5, 2.,1., 3.,2.
T2=0.,0., 18.E-6,0., 18.E-6,.5, 19.E-6,1., 20.E-6,.5, 20.E-6,0.
DEFINED PARAMETERS
P1=0.
P2=0.
OUTPUTS
VCIN,EA1,VJB1,VJO,PLOT
P1(GAMMA),PLOT
```

Figure X-14. Model Description With Neutron Effects

```
                    TIMING TEST UA744
                    SAVED UNDER FILE UA744
                    CLOSED LOOP GAIN 20 DB
 ELEMENTS
 E1.GND-1=FGEN(0.,1.15,0.,5.E-8,25.E-6,5.E-8,50.E-6,5.,TIME)
 A1,3-2-4-GND=MODEL UA744
 R1, 1-3=50.
 RF.4-2=100.E3
 RI.2-GND=10.E3
 RL.4-GND=2.E3
 CL.4-GND=100.E-12
 OUTPUTS
 E1.PLOT
 RUN CONTROLS
 MAXIMUM PRINT POINTS = 100
 COMPUTER TIME LIMIT=5.
 STOP TIME = 50.E-6
 RERUN DESCRIPTION
 DEFINED PARAMETERS
 P2A1=27000.
 END

SYSTEM NOW ENTERING SIMULATION
```

Figure X-15. Neutron Radiation - Test Circuit Description

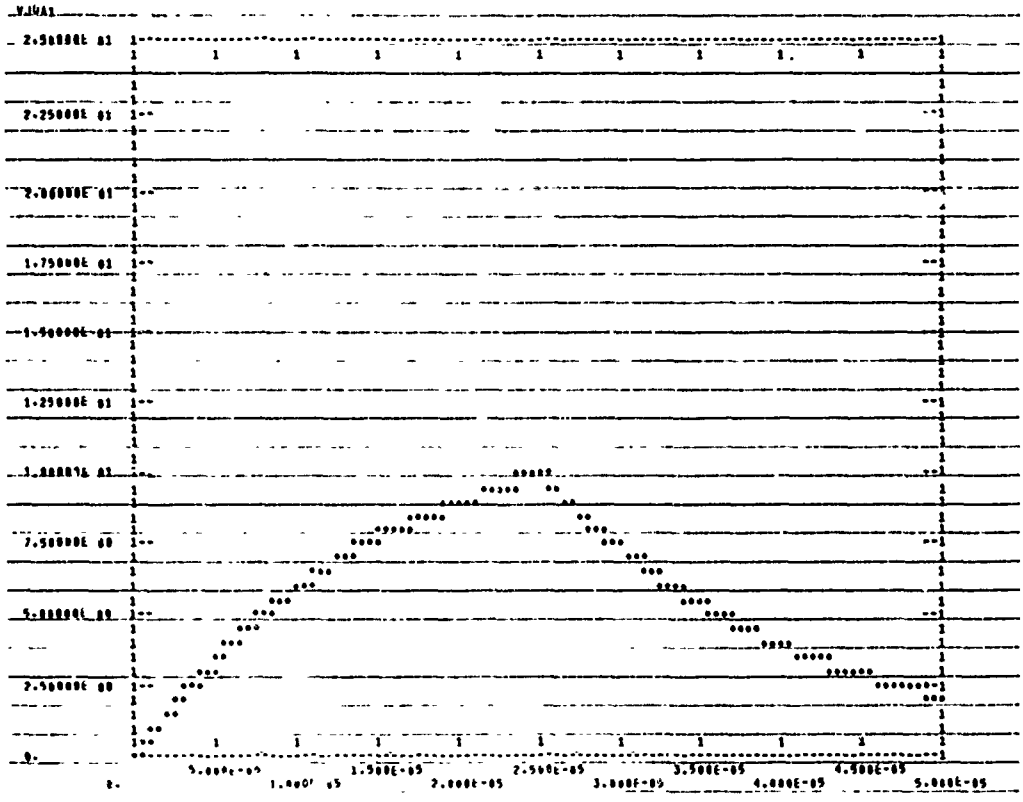


Figure X-16. Response to Neutron Radiation

APPENDIX I

INTRODUCTION TO INDIVIDUAL DEVICE TESTS

This appendix describes the data base for FXR and NVT responses for the ten different devices selected for modeling. The FXR responses were obtained by test at the Radiation Effects Laboratory of the Space Division, General Electric Company, with one exception. The one exception is the FSC 9704; data on this device has been generated earlier and was supplied through the courtesy of Capt. D. Alexander of the AFWL. The FXR responses are for dose rates of the order of 1 to 3×10^{10} rads (Si)/second. Photographs of the physical conditions under which the tests were conducted are shown in Figures A-1 through A-4. Figure A-5 represents a summation of tests conducted.

The neutron degradation data was primarily collected from prior reports; these reports were obtained from AFWL, SAMSO, REIC, Fairchild and others. The exception is the HA-2700-2; data for this device was obtained by irradiations at the Aberdeen (Army) Pulsed Base Reactor. The neutron degradation data is generally for 10^{14} ns/cm^2 (1 Mev silicon damaged equivalent), and the data follows the FXR data in each section of this appendix.

Typical eletrical test circuits are shown in Figures A-6 and A-7. Figure A-6 indicates the manner of connecting a digital device into the radiation test installation; Figure A-7, an analog device. The gain data for the emitter follower circuit that was used to couple the circuit response to the oscilloscope are shown in Table 1-1.

A single, representative, sample for each device type is included in the appendices. All information is not included in this report.

Table 1-2 indicates the number of integration steps required to evaluate device performance under varying conditions. This information permits some evaluation of the device models and the effects of including radiation performance characteristics in the descriptions.

TABLE 1-1

V_{in} (DC)	V_{out} (DC)
0 Volts	0 Volts
1	0.01
2	0.06
3	0.1
4	0.15
5	0.2
6	0.28

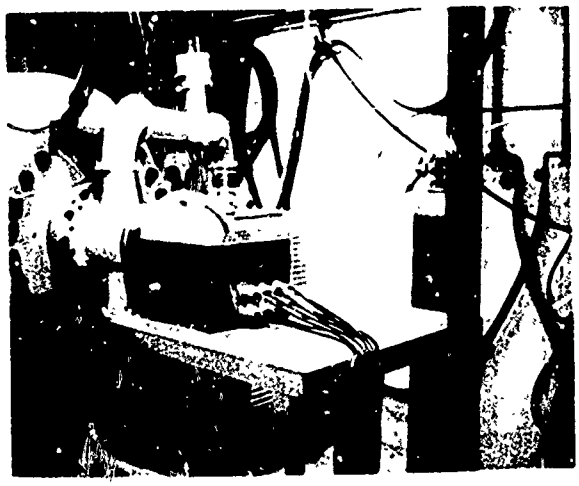


Figure A-1. Test Setup at Face of Flash X-Ray Machine

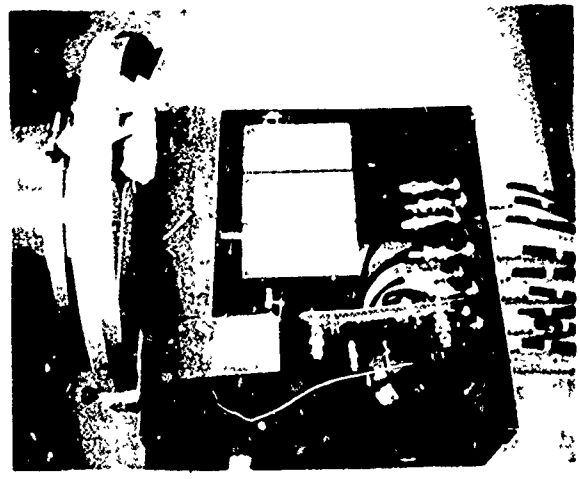


Figure A-2. Interior View of Test Box Showing Lead Shielding and Electronics

Figure A-3. Side View Showing Addition of Lead Aperture Brick

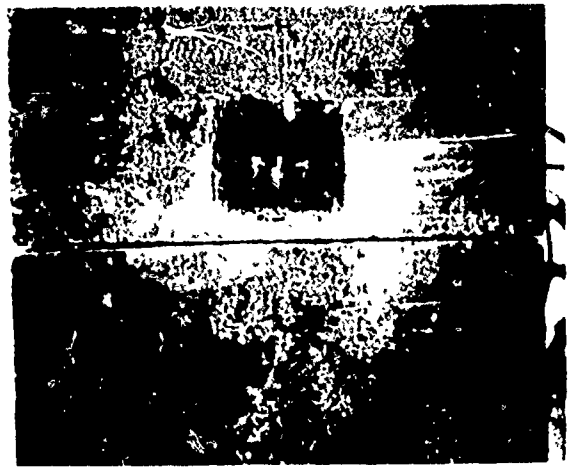


Figure A-4. Detail View Through Aperture

Device	Circuits Per Device	FXR Circuits Tested	FXR Test Conditions	FXR Outputs Monitored Per Circuit	NVT Tested
FSC 9704 Dual 4 Input Nand Gate	2	3 (Ref 3)	6	1	(Ref 2)
FSC 9774 Dual D Flip-Flop	2	8	12	2	(Ref 2)
FSC 9780 4 Bit Shift Register	1	4	5	4	12 (Ref 2)
FSC μA744 Operational Amplifier	1	5	8	1	24 (Ref 4)
HA 2700 Operational Amplifier	1	8	8	1	(TBD) 12
TI RSN54L00 Quad 2-Input Nand Gate	4	8	5	1	≥6 (Ref 2, 5)
TI RSN54L57 AND-OR-Invert Gate	1	5	5	1	≥1 (Ref 2, 5)
TI RSN54L72 J-K Master Slave Flip-Flop	1	4	10	2	6 (Ref 2, 5)
TI RSN54L74 Dual D Flip-Flop	2	4	12	2	5 (Ref 2, 5)
TI RSN54L122 Monostable Multivibrator	1	7	5	2	5 (Ref 2, 5)

Figure A-5. Radiation Response Summary

[2] Clemens, D. P., op. cit. page 121

[3] Alexander, D. R., "Report on the 9704 NAND Gate", Air Force Weapons Laboratory, 15 August 1969

[4] MacDougall, J., "Tests Performed on the μA744 and Other Products Using Neutron Radiation", Private Communication

[5] Orndorff, R. M., et al, "Radiation Testing of Hardened Electronic Components", SAMSO-TR-71-301, December 1971

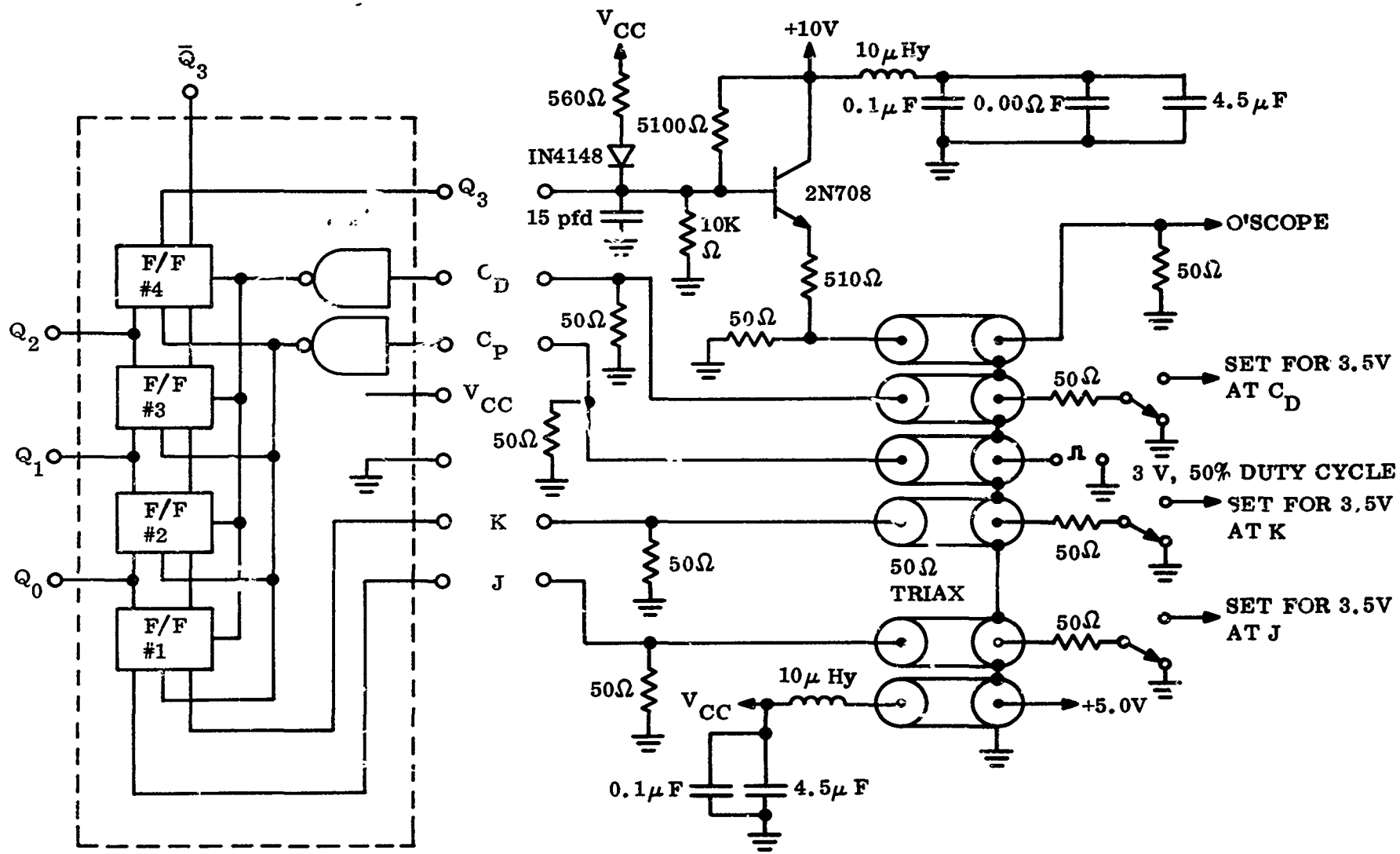
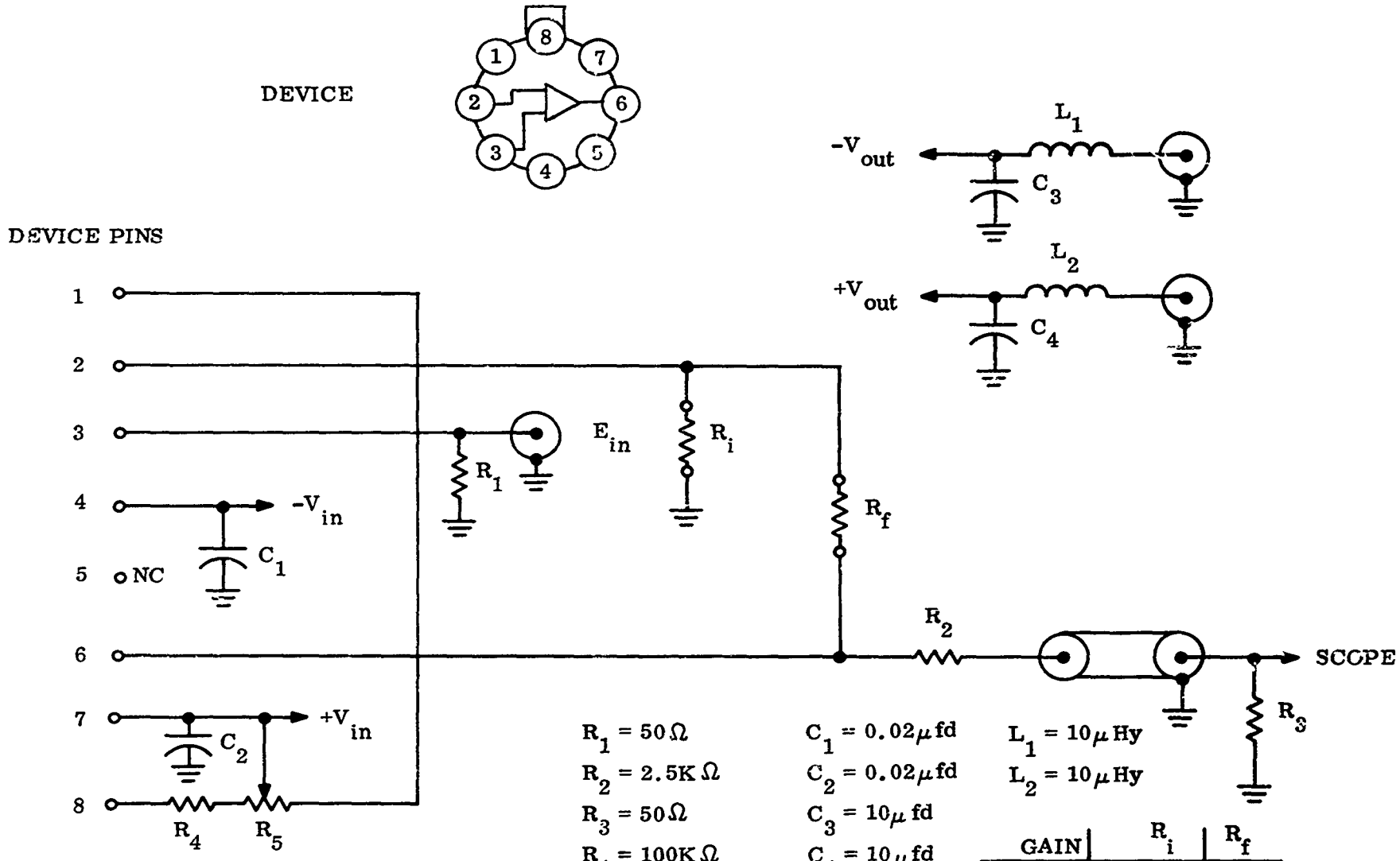


Figure A-6. 9780 Test Schematic



GAIN	R_i	R_f
10	$10K\Omega$	$100K\Omega$
1	∞	0

Figure A-7. HA-2700 Test Schematic

TABLE 1-2.

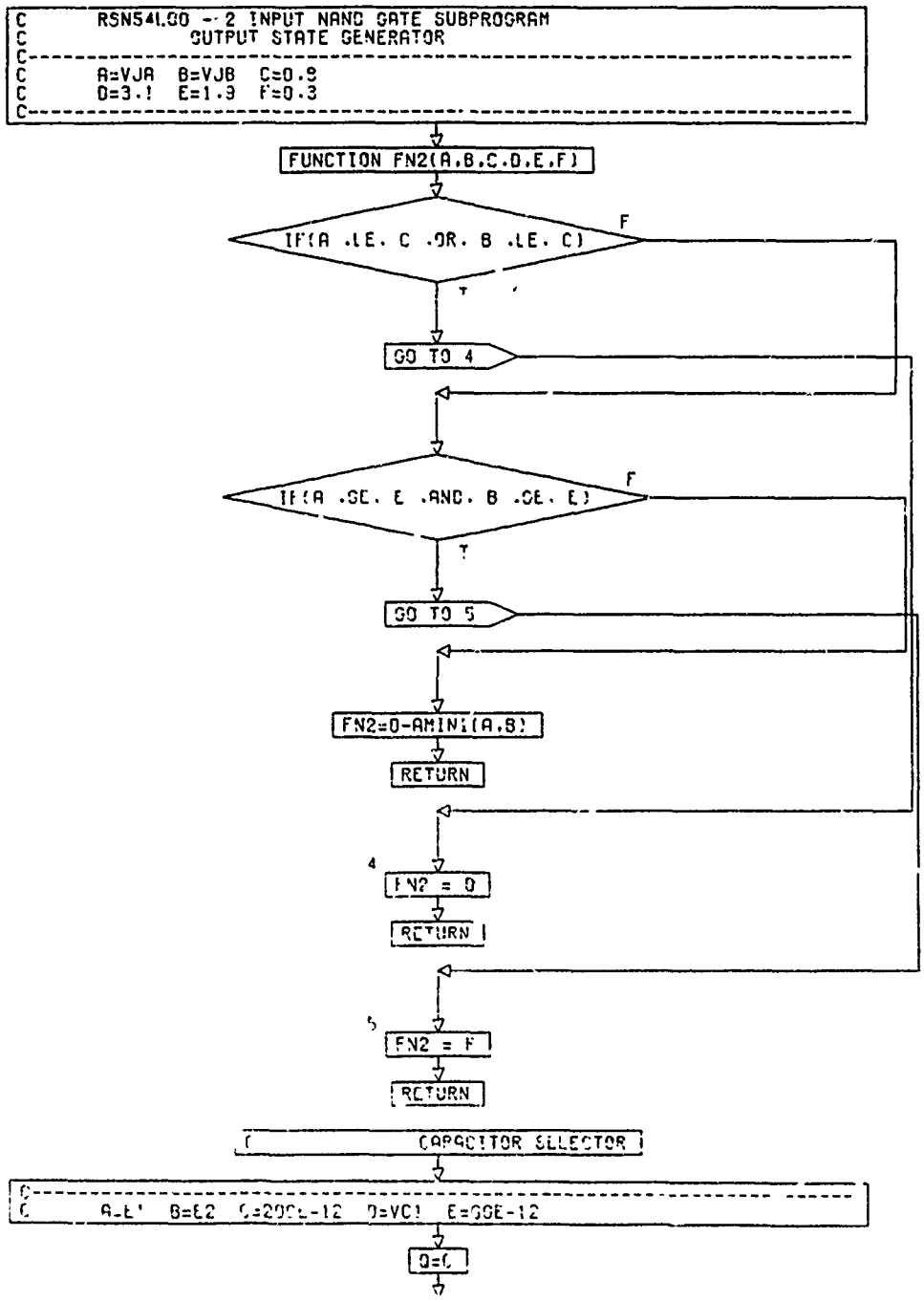
INTEGRATION STEPS REQUIRED

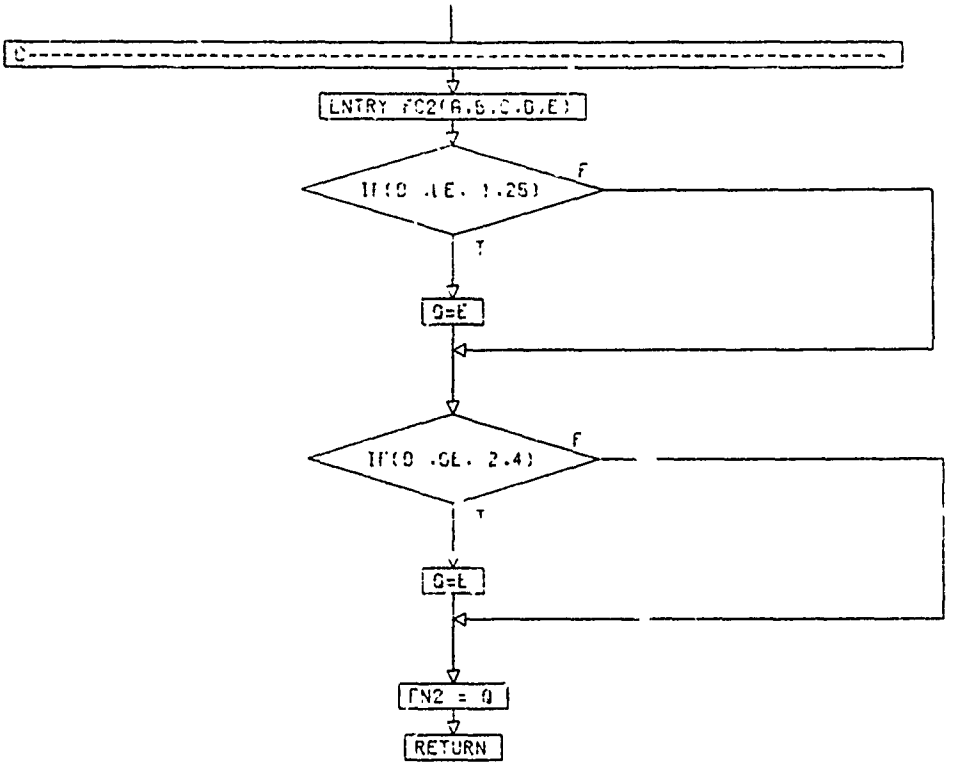
DEVICE	ANALYSIS TIME (MICROSECONDS)	NO RADIATION	WITH GAMMA	WITH NEUTRON
RSN54L00	1	1100	1170	1070
9704	1	9200	10,900	8860
9774	1	970	1400	1600
RSN54L72	2	1500	1600	1400
9780	5	3480	4800	3570
RSN54L122	1	1060	1280	1920
RSN54L57	2	1060	1650	1710
HA 2700	2	8930	3100	8930
μA744	50	1190	1400	765

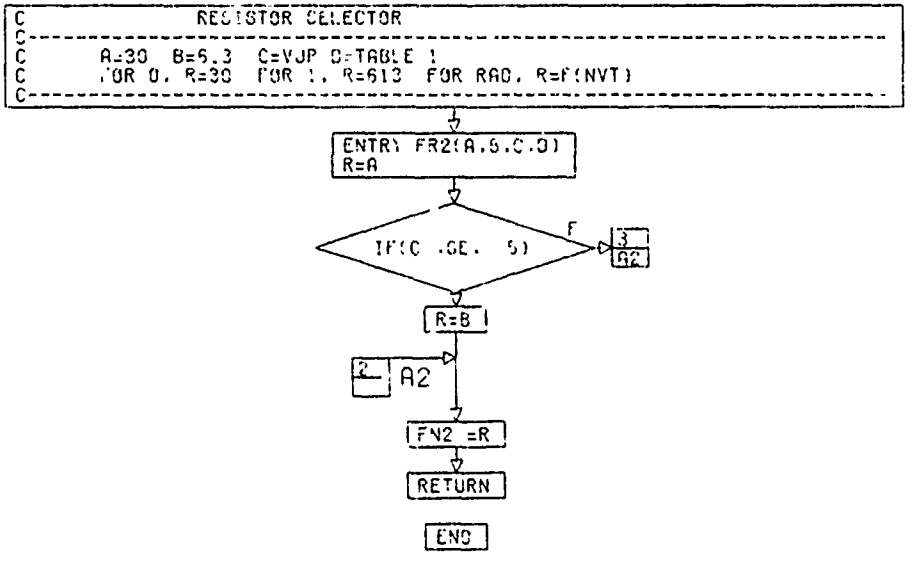
APPENDIX II

RSN54L00 NAND GATE

A. FLOW CHARTS




C
ENTRY FC2(A,B,C,D,E)
IF(D .LE. 1.25)
F
T
D=E
IF(D .GE. 2.4)
F
T
D=E
FN2 = D
RETURN


C RESISTOR SELECTOR
C
C A=30 B=6.3 C=VUP D=TABLE 1
C FOR 0, R=30 FOR 1, R=613 FOR RAD, R=F(NVT)
C
ENTRY FR2(A,B,C,D)
R=A
IF(C .GE. 5)
F
3
A2
R=B
2
A2
FN2 =R
RETURN
END

B. TEST CONDITIONS AND RESULTS

1. GAMMA RADIATION

Two of these devices were tested on the flash X-ray under several circuit performance conditions. A cross-reference between the circuit conditions and the photographed test results is shown in Table 2-1. The irradiations, at 20 nanoseconds pulse width, were at 3.1×10^{10} rads (Si)/second. The response photographs presented are for device #1.

All test conditions show substantial transient response due to radiation when the results are compared with the pretest performance as seen in the first photograph.

2. NEUTRON RADIATION

All neutron radiation behavior data was obtained from Reference 1. *

TABLE 2-1.

TEST CONDITIONS

SHOT # (Device 1)	COND. #	INPUTS A	INPUTS B	NORMAL OUTPUT Y
5333	1	H	H	L
5318	2	L	H	H
5319	3	L	L	H
5320	4	H	L	H
5330	5	H..L..H	H	L..H..L
5331	6	L..H..L	H	H..L..H

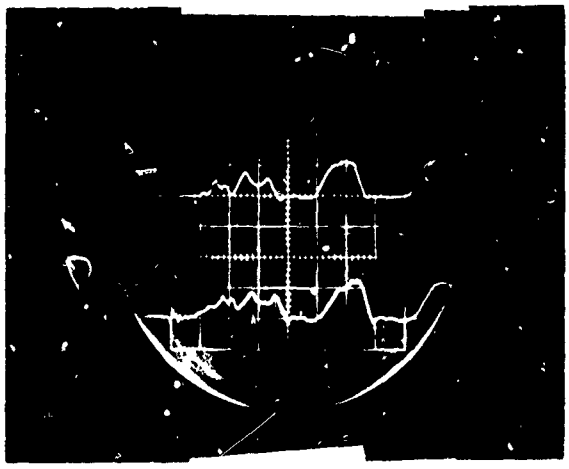
*Olson, R. J., op. cit. page 16

Pretest - Device #1

A. 1Y
0.1 V Div
0.1 μsec Div

B. 2Y
0.1 V Div
0.1 μsec Div

Condition 1 - Device #1 - Shot #5315



A. 1Y
0.1 V/Div
0.1 μsec/Div

B. 2Y
0.1 V/Div
0.1 μsec/Div

Condition 2 - Device #1 - Shot #5318

A. 1Y
0.1 V Div
0.1 μsec Div

B. 2Y
0.1 V Div
0.1 μsec Div

Condition 3 - Device #1 - Short #5319

A. 1Y
0.1 V Div
0.1 μsec Div

B. 2Y
0.1 V Div
0.1 μsec Div

*A Upper Trace; B Lower Trace.

Condition 4 - Device #1 - Shot #5320

A. 1Y
0.1 V/Div
0.1 μsec/Div

B. 2Y
0.1 V/Div
0.1 μsec/Div

Condition 5 - Device #1 - Shot #5322

A. 1Y
0.1 V/Div
0.1 μsec/Div

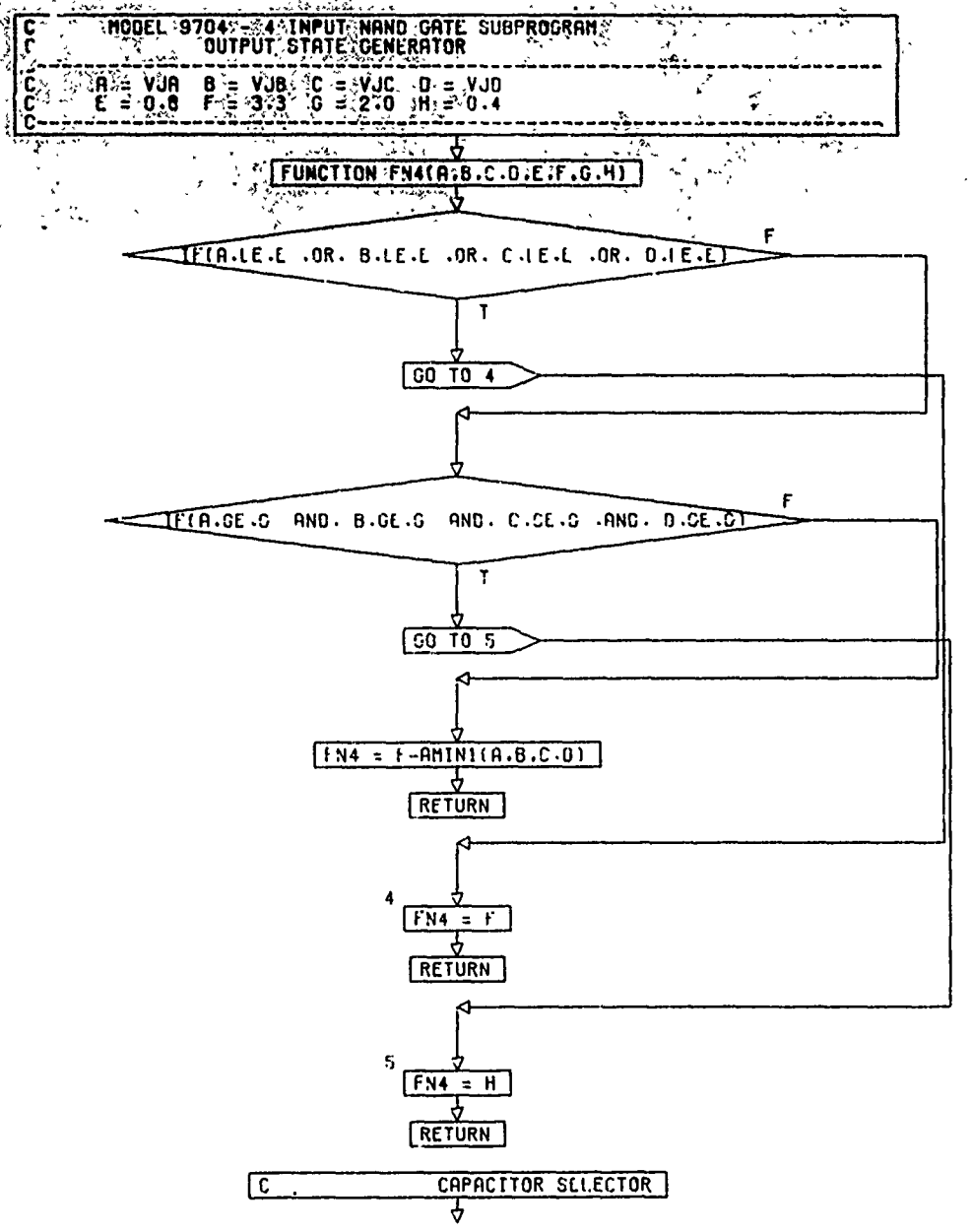
B. 2Y
0.1 V/Div
0.1 μsec/Div

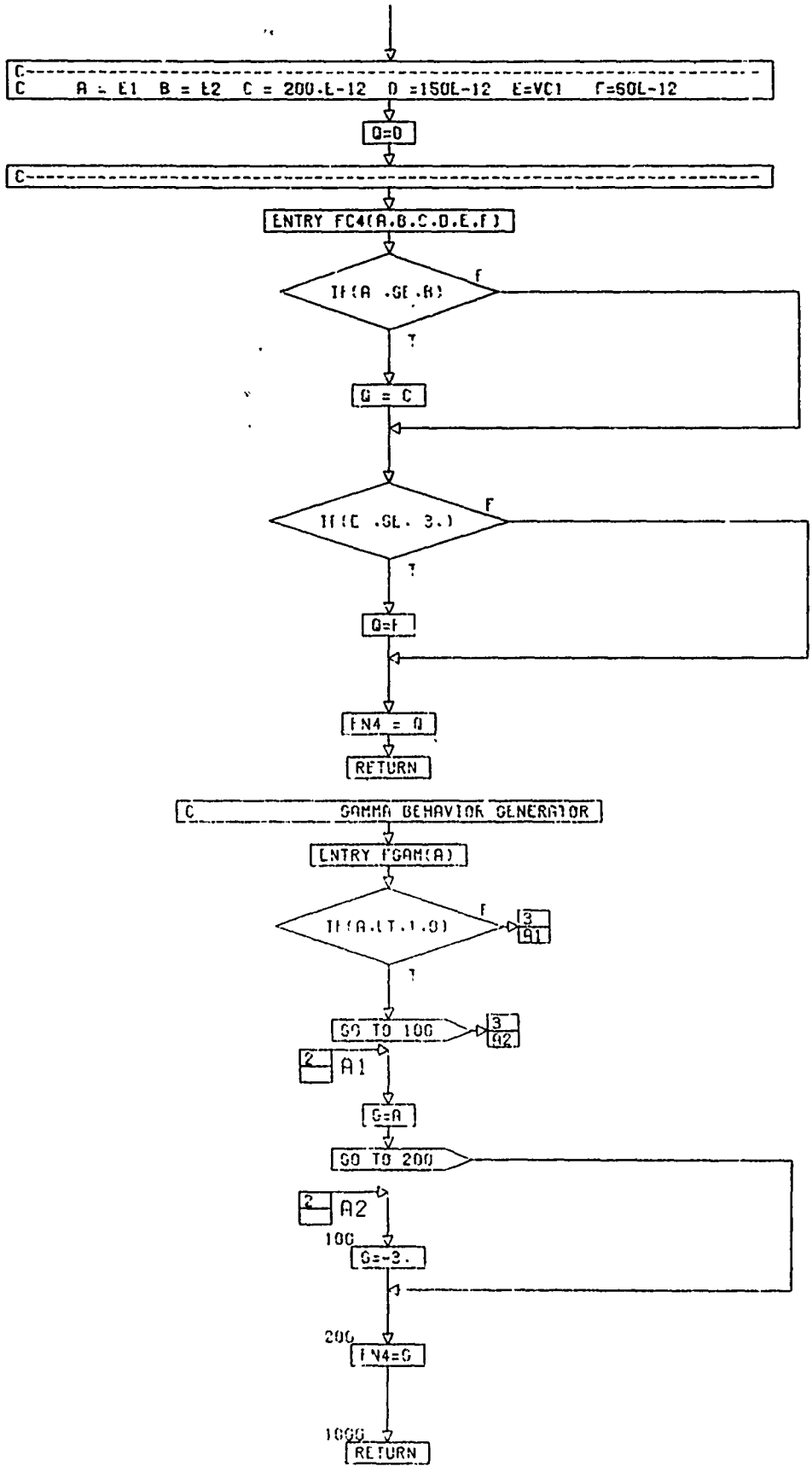
Note: A = Upper Trace; B = Lower Trace.

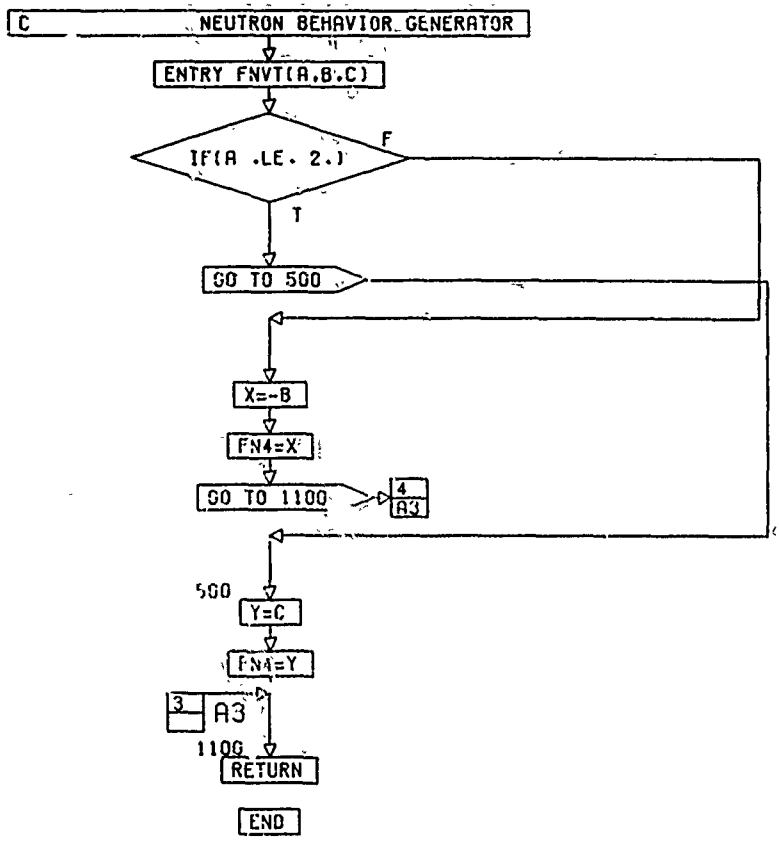
APPENDIX III

FAIRCHILD 9704 FOUR-INPUT NAND GATES

A. FLOW CHARTS




C
C A = E1 B = E2 C = 200.E-12 D =150E-12 E=VC1 F=60E-12
Q=0
C
ENTRY FC4(A,B,C,D,E,F)
IF(A .GE.B)
F
T
Q = C
IF(C .GE. 3.)
F
T
Q=F
FN4 = Q
RETURN
C GAMMA BEHAVIOR GENERATOR
ENTRY FGAM(A)
IF(A.LT.1.0)
F
3
A1
T
GO TO 100
3
A2
2
A1
G=A
GO TO 200
2
A2
100
G=-3.
200
FN4=G
1000
RETURN



B. TEST CONDITIONS AND RESULTS

1. GAMMA RADIATION

Test conditions and results are based on Air Force Weapons Laboratory data and are not included in this appendix.

2. NEUTRON RADIATION

The performance characteristics of these devices should change with neutron exposure in a manner quantitatively similar to that of the 9780 device, as described in Reference 2*, per the advice of D. Myers of Fairchild Semiconductor.

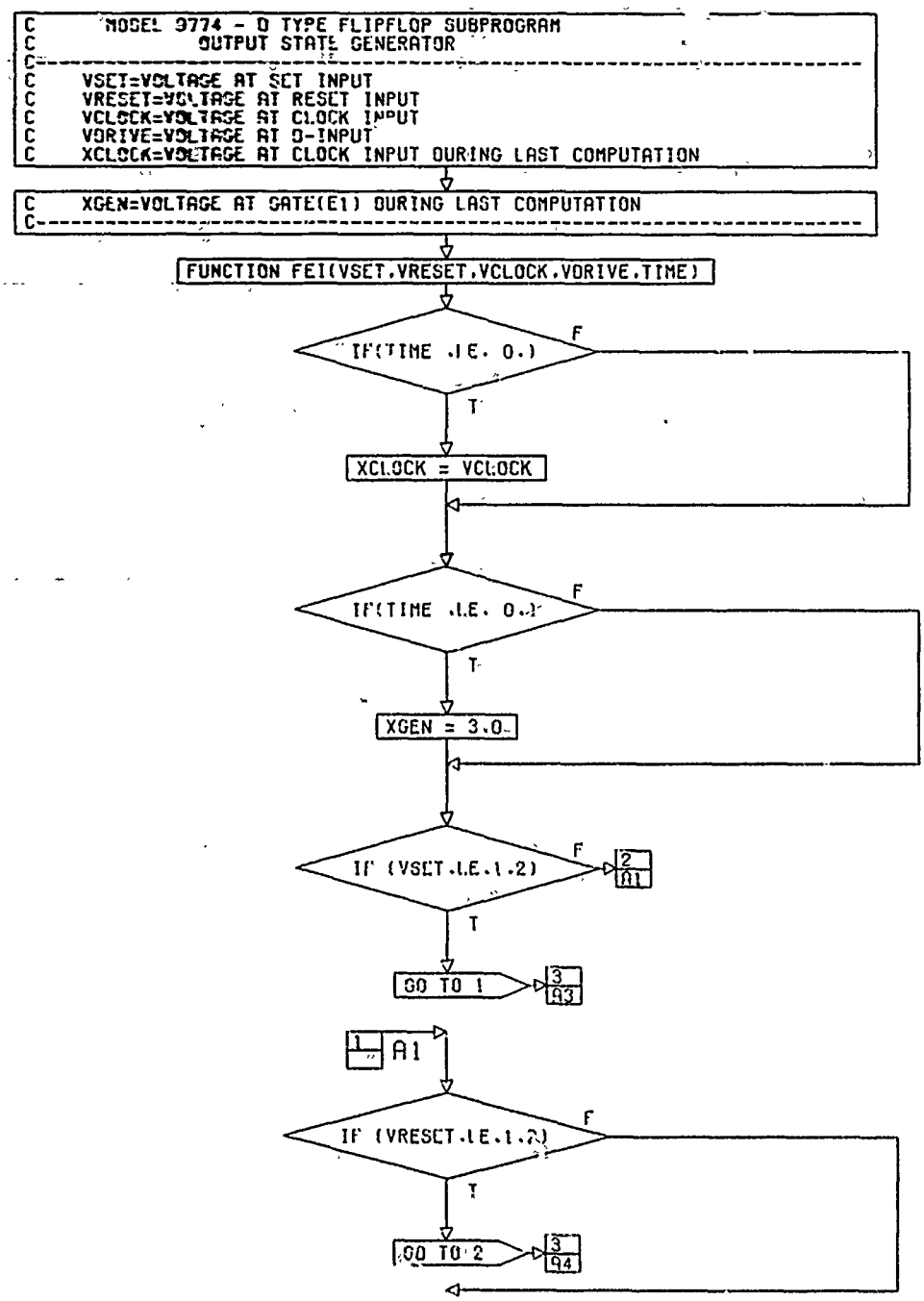
---

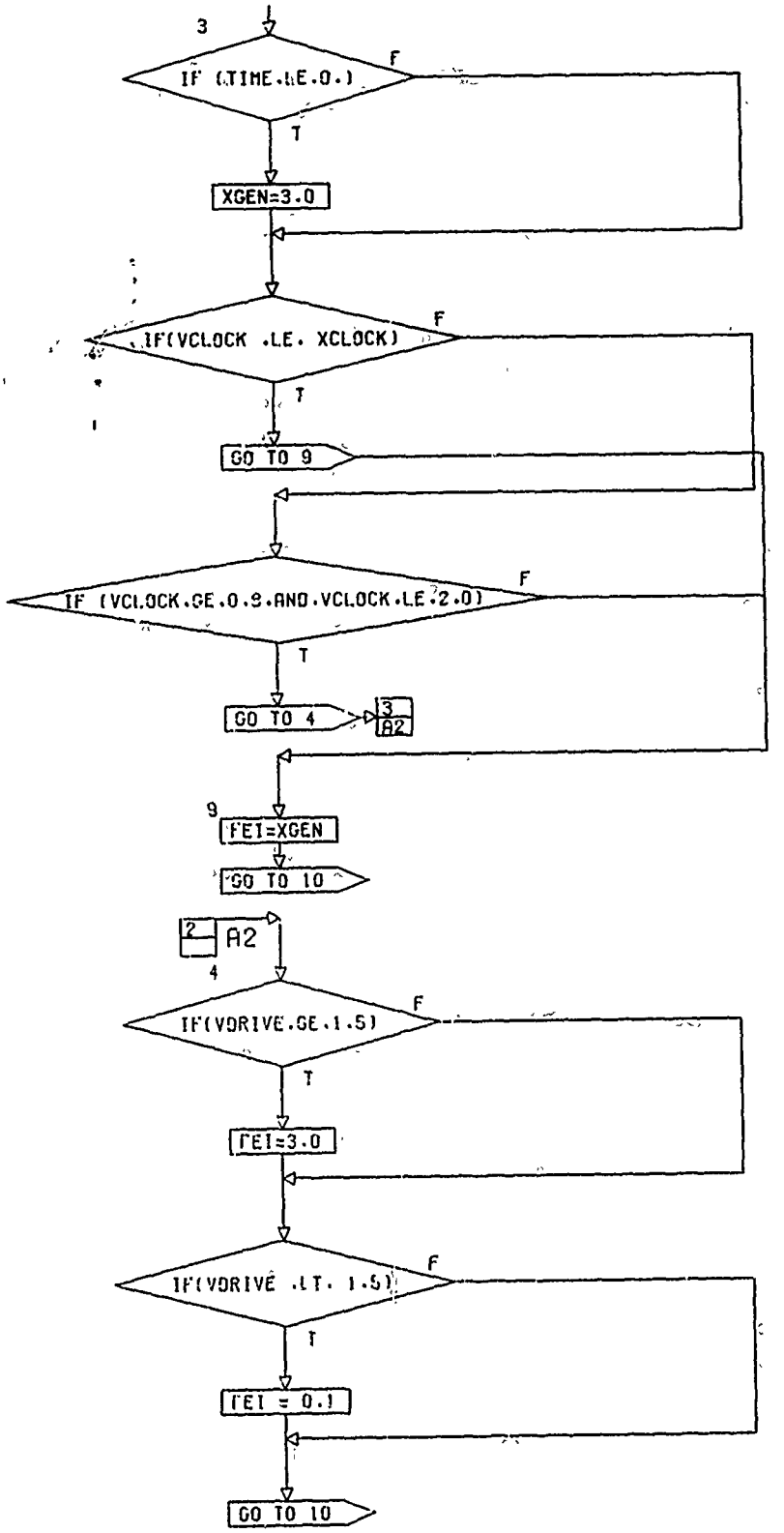
*Clemens, D. P., op. cit. page 121

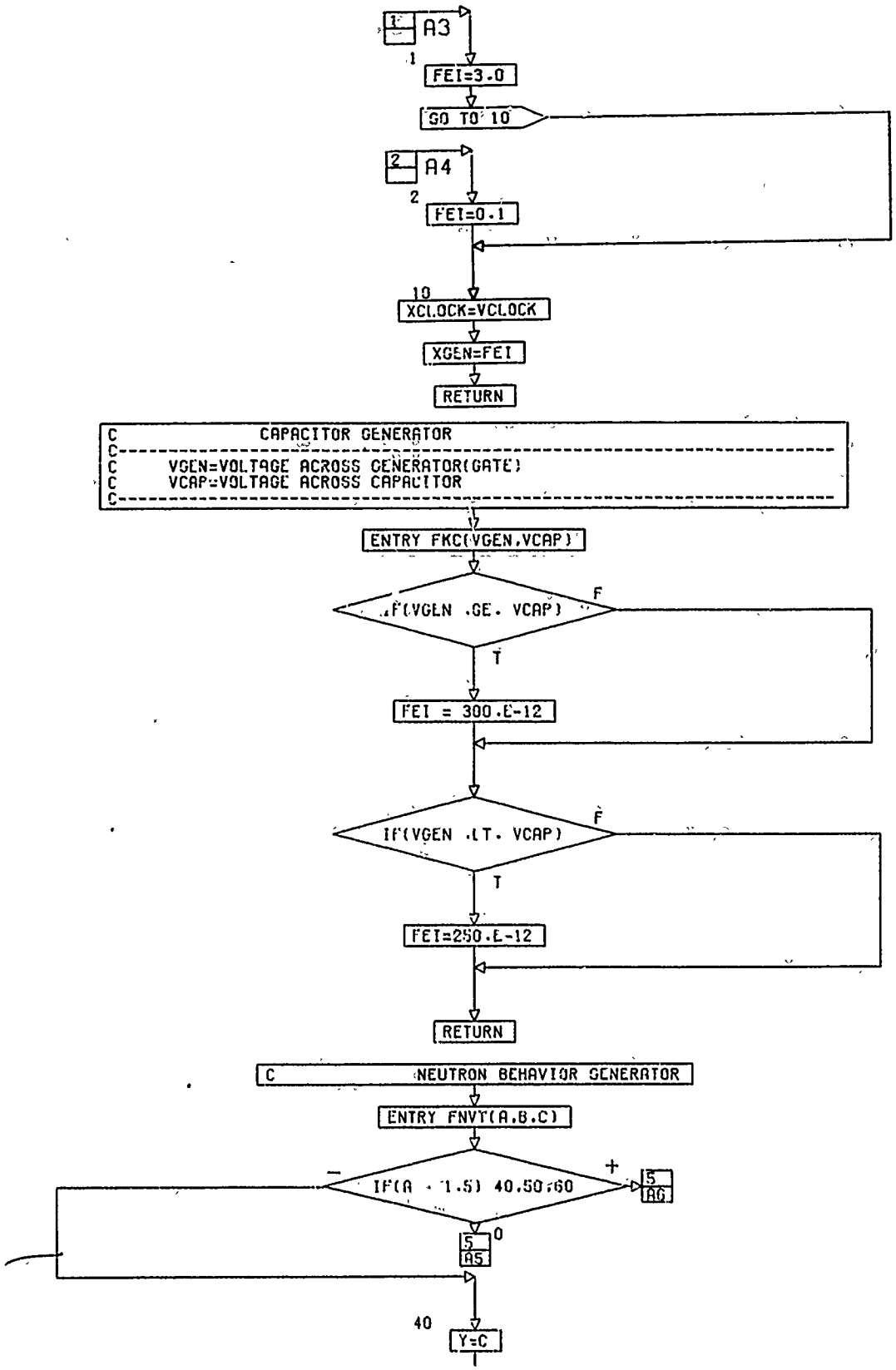
APPENDIX IV

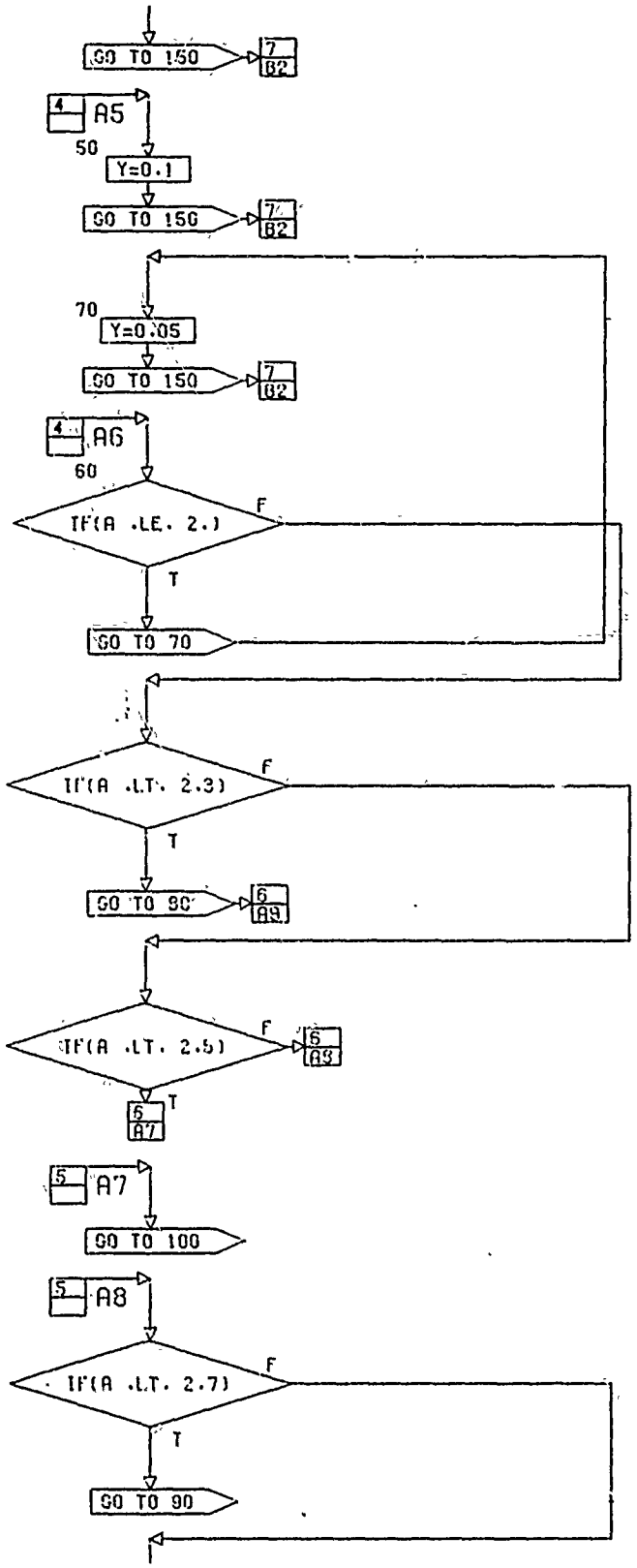
FAIRCHILD 9774-D FLIP-FLOP

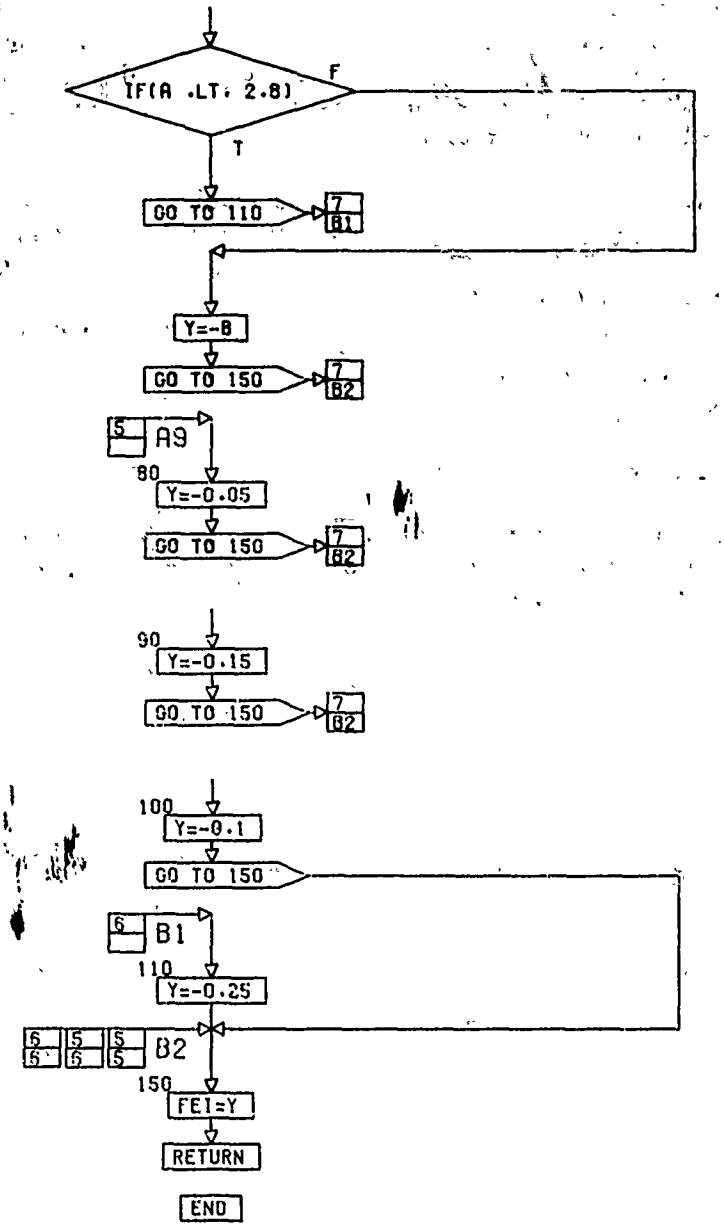
A. FLOW CHARTS




3
IF (TIME.LE.0.)
F
T
XGEN=3.0
IF(VCLOCK .LE. XCLOCK)
F
T
GO TO 9
IF (VCLOCK.GE.0.9.AND.VCLOCK.LE.2.0)
F
T
GO TO 4
3
A2
9
FEI=XGEN
GO TO 10
2
A2
4
IF(VDRIVE.GE.1.5)
F
T
FEI=3.0
IF(VDRIVE .LT. 1.5)
F
T
FEI = 0.1
GO TO 10


1
A3
1
FEI=3.0
GO TO 10
2
A4
2
FEI=0.1
10
XCLOCK=VCLOCK
XGEN=FEI
RETURN
C CAPACITOR GENERATOR
C
C VGEN=VOLTAGE ACROSS GENERATOR(GATE)
C VCAP=VOLTAGE ACROSS CAPACITOR
C
ENTRY FKC(VGEN,VCAP)
IF(VGEN .GE. VCAP)
F
T
FEI = 300.E-12
IF(VGEN .LT. VCAP)
F
T
FEI=250.E-12
RETURN
C NEUTRON BEHAVIOR GENERATOR
ENTRY FNVT(A,B,C)
IF(A - 1.5) 40,50,60
−
+
5
AG
0
5
A5
40
Y=C


GO TO 150
7
B2
4
A5
50
Y=0.1
GO TO 150
7
B2
70
Y=0.05
GO TO 150
7
B2
4
A6
60
IF(A .LE. 2.)
F
T
GO TO 70
IF(A .LT. 2.3)
F
T
GO TO 80
6
A9
IF(A .LT. 2.5)
F
6
A9
T
6
A7
5
A7
GO TO 100
5
A8
IF(A .LT. 2.7)
F
T
GO TO 90


IF(A .LT. 2.8)
F
T
GO TO 110
7
B1
Y=-8
GO TO 150
7
B2
5
A9
80
Y=-0.05
GO TO 150
7
B2
90
Y=-0.15
GO TO 150
7
B2
100
Y=-0.1
GO TO 150
6
B1
110
Y=-0.25
6
5
5
B2
150
FE1=Y
RETURN
END

B. TEST CONDITIONS AND RESULTS

1. GAMMA RADIATION

Four of these devices were tested singly on the flash X-ray, in active circuits at dose rates of about 3×10^{10} rads (Si)/second. Each device has two identical circuits and inputs were set up simultaneously, parallel. The devices were tested in 11 different conditions, as detailed on Table 4-1. Data is presented for device #123. The pretest and No. 1 conditions involved switching the data input at 50 percent of the clock rep rate; hence the output clocked also. Input conditions 2 and 3 involved clocking with other inputs fixed.

All other conditions involved d-c input levels. The pretest shot shows the precise clock pulse shape; but does not show the a-c data input signal as it was on the pretest and condition 1 shots. The radiation pulse time relationship to the clock pulse is shown on all the condition 1-3 shots as a superposition (-) on the clock pulse. The radiation pulse effect on the Q and $\overline{Q}$ output traces is quite obvious as to time and effect. The dose rate as measured ahead of the sample was 3.2×10^{10} rads (Si)/second.

2. NEUTRON RADIATION

The performance characteristics of these devices should change with neutron exposure in a manner quantitatively similar to that of the 9780 device, as described in Reference 2*, per the advice of D. Myers of Fairchild Semiconductor.

TABLE 4-1.

TEST CONDITIONS

SHOT#	COND. #	PRESET (Normally High)	CLEAR (Normally High)	CLOCK (Switching except as noted)	DATA (Switching except as noted)	Q
Pretest	1					L
5262	1					L
5261	2				H	H
5260	3				L	L
5265	4		L	H	H	L
5266	5		L	L	H	L
5267	6	L		H	L	H
5268	7	L		L	L	H
5269	8	H		H	H	H
5270	9	H		H	H	L
5271	10	H		L	H	L
5272	11			L	L	H

*Clemens, D. P., op. cit. page 121

Pretest

A. 1Q
0.1 V/Div
50 nsec/Div

B. 50 nsec/Div
2V - 50 nsec

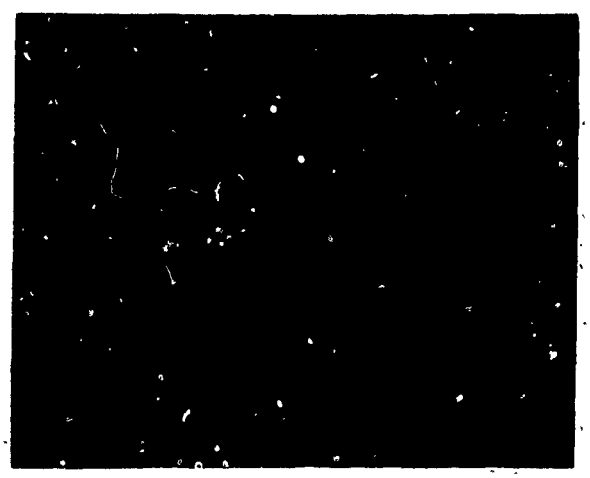
C. Data
2V - 50 nsec

Condition 1 - Shot #5262

A. 1Q
0.1 V/Div
0.1 μsec/Div

B. $1\overline{Q}$
0.1 V/Div
0.1 μsec/Div

Condition 2 - Shot #5261



A. 1Q
0.1 V/Div
0.1 μsec/Div

B. $1\overline{Q}$
0.1 V/Div
0.1 μsec/Div

Condition 3 - Shot #5260

A. 1Q
0.1 V/Div
0.1 μsec/Div

B. $1\overline{Q}$
0.1 V/Div
0.1 μsec/Div

*A = Upper Trace; B = Lower Trace.

Condition 4 - Shot #5265

A. 1Q
0.1 V/Div
0.1 μsec/Div

B. $1\bar{Q}$
0.1 V/Div
0.1 μsec/Div

Condition 5 - Shot #5266

A. 1Q
0.1 V/Div
0.1 μsec/Div

B. $1\bar{Q}$
0.1 V/Div
0.1 μsec/Div

Condition 6 - Shot #5267

A. 1Q
0.1 V/Div
0.1 μsec/Div

B. $1\bar{Q}$
0.1 V/Div
0.1 μsec/Div

Condition 7 - Shot #5268

A. 1Q
0.1 V/Div
0.1 μsec/Div

B. $1\bar{Q}$
0.1 V/Div
0.1 μsec/Div

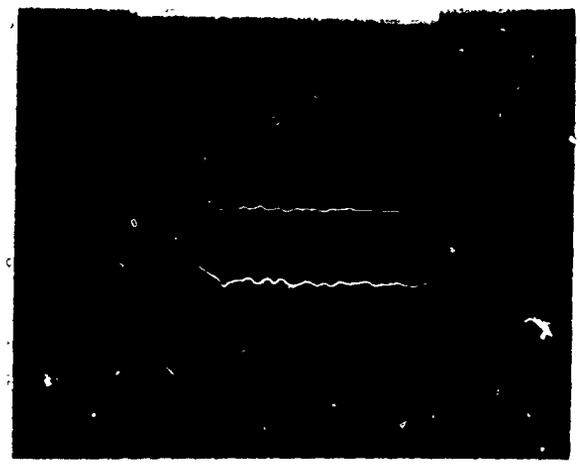
Note: A = Upper Trace; B = Lower Trace.

Condition 8 - Shot #5269

A. 1Q
0.1 V/Div
0.1 μsec/Div

B. $1\overline{Q}$
0.1 V/Div
0.1 μsec/Div

Condition 9 - Shot #5270



A. 1Q
0.1 V/Div
0.1 μsec/Div

B. $1\overline{Q}$
0.1 V/Div
0.1 μsec/Div

Condition 10 - Shot #5271

A. 1Q
0.1 V/Div
0.1 μsec/Div

B. $1\overline{Q}$
0.1 V/Div
0.1 μsec/Div

Condition 11 - Shot #5272

A. 1Q
0.1 V/Div
0.1 μsec/Div

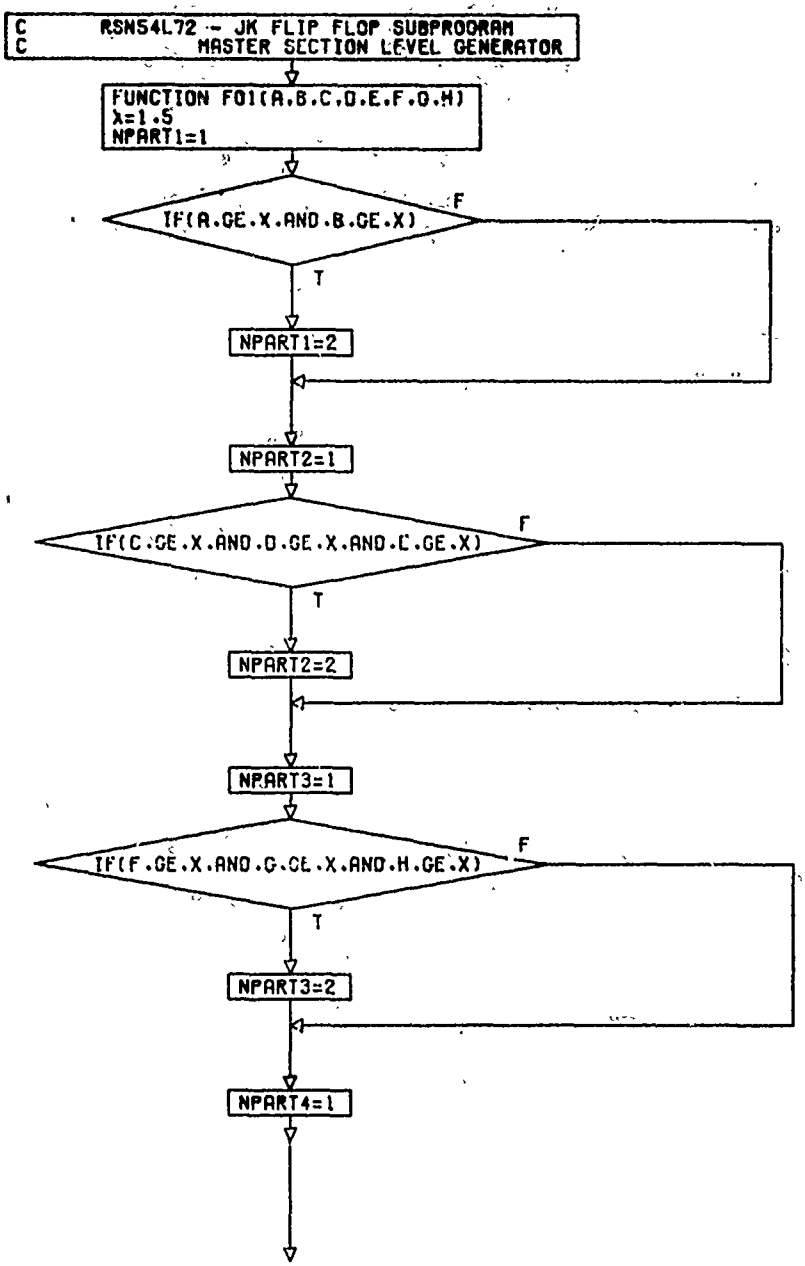
B. $1\overline{Q}$
0.1 V/Div
0.1 μsec/Div

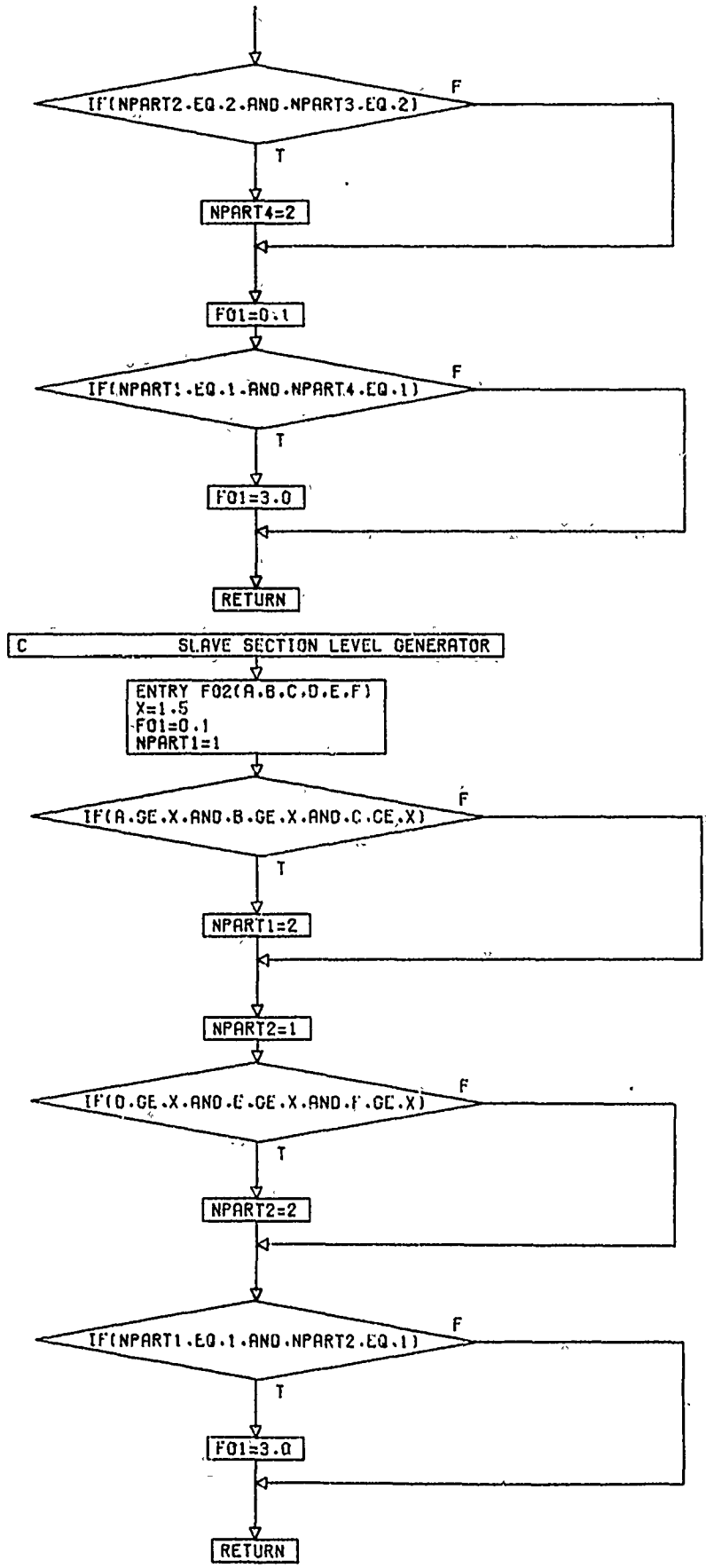
Note: A Upper Trace; B Lower Trace.

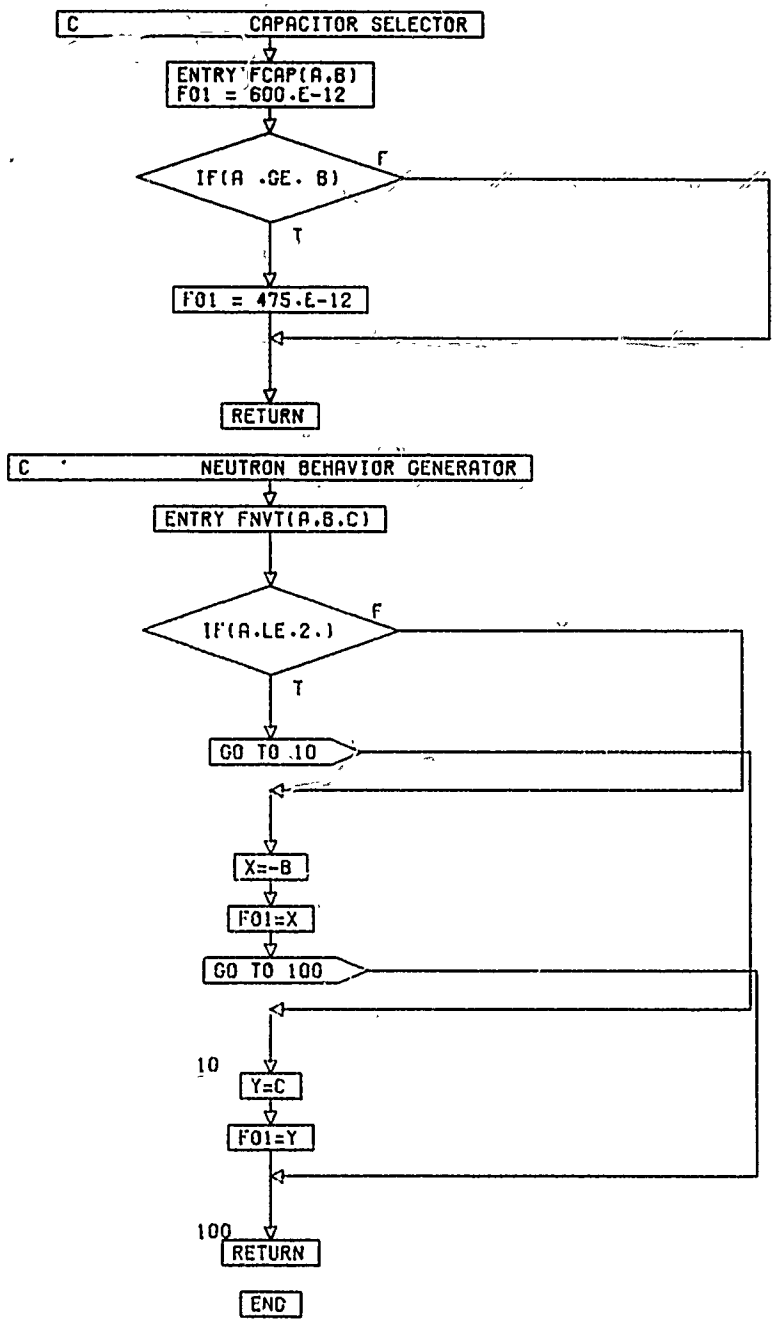
APPENDIX V

RSN54L72 FLIP-FLOP

A. FLOW CHARTS




IF(NPART2.EQ.2.AND.NPART3.EQ.2)
F
T
NPART4=2
F01=0.1
IF(NPART1.EQ.1.AND.NPART4.EQ.1)
F
T
F01=3.0
RETURN
C SLAVE SECTION LEVEL GENERATOR
ENTRY F02(A,B,C,D,E,F)
X=1.5
F01=0.1
NPART1=1
IF(A.GE.X.AND.B.GE.X.AND.C.GE.X)
F
T
NPART1=2
NPART2=1
IF(D.GE.X.AND.E.GE.X.AND.F.GE.X)
F
T
NPART2=2
IF(NPART1.EQ.1.AND.NPART2.EQ.1)
F
T
F01=3.0
RETURN


C CAPACITOR SELECTOR
ENTRY FCAP(A,B)
F01 = 600.E-12
IF(A .GE. B)
F
T
F01 = 475.E-12
RETURN
C NEUTRON BEHAVIOR GENERATOR
ENTRY FNVT(A,B,C)
IF(A.LE.2.)
F
T
GO TO 10
X=-B
F01=X
GO TO 100
10
Y=C
F01=Y
100
RETURN
END

B. TEST CONDITIONS AND RESULTS

1. GAMMA RADIATION

These tests were conducted with RSN54L71 flat packs with external connections to cause it to perform as an RSN54L72-JK flip-flop. A total of four samples were tested.

The general philosophy for establishing device test conditions was to try all input combinations, including clocked inputs, check for override action (clean, etc.) maximize the clock rate and utilize heavy low state loading. For clocked states, generally a series of shots was used to see if the response was dependent on the radiation-clock time relationship.

The flash X-ray dose rates were 1.3×10^{10} rads (Si)/second over a 20 nanosecond radiation pulse. The tests were conducted per 10 different conditions as detailed in Table 5-1. Data is presented for device no. 153.

2. NEUTRON RADIATION

All neutron radiation behavior data was obtained from Reference 1.*

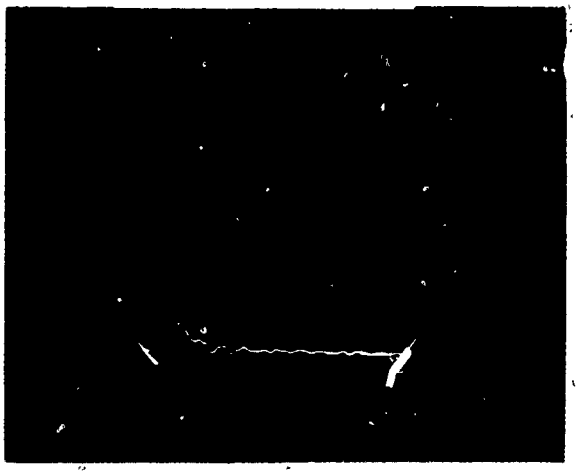
TABLE 5-1.

TEST CONDITIONS

SHOT#	COND. #	J	K	Q_N	CLOCK (Norm. Low)	PRE (Norm. High)	CLEAR
4925	1	L	L	H			
4926	2	L	H	L/H			
4927	3	H	L	L/H			
4928	4	H	H	H			
4929	5	H	H	L			
4930	6	L	L	L			
4924	9A	H	H	H	H		
4923	9B	H	H	L	H		
4931	10	H	H	H		L	
4932	11	H	H	L			L

*Olson, R. J., op. cit. page 16

Condition 1 - Shot #4925



A. Q
0.1 μsec/Div

B. $\overline{Q}$
0.1 μsec/Div

Condition 2 - Shot #4926

A. Q
0.1 μsec/Div

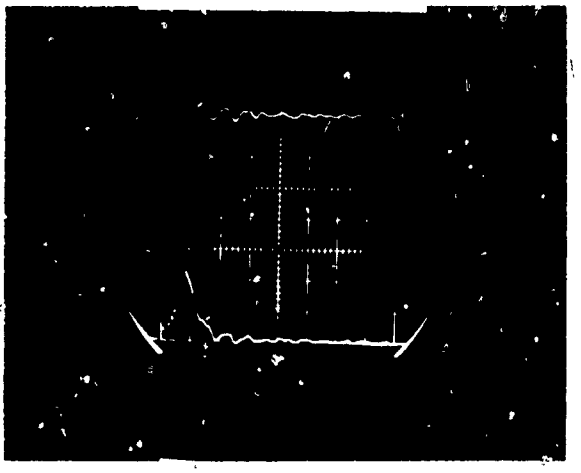
B. $\overline{Q}$
0.1 μsec/Div

Condition 3 - Shot #4927

A. Q
0.1 μsec/Div

B. $\overline{Q}$
0.1 μsec/Div

Condition 4 - Shot #4928



A. Q
0.1 μsec/Div

B. Q
0.1 μsec/Div

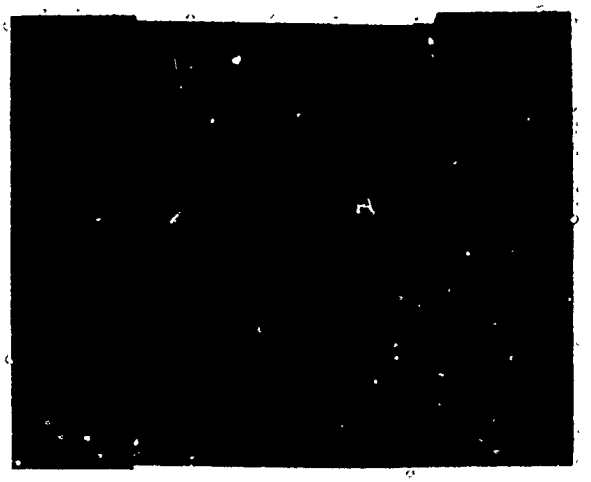
*A = Upper Trace; B = Lower Trace.

Condition 5 - Shot #4929

A. Q
0.1 μsec/Div

B. $\overline{Q}$
0.1 μsec/Div

Condition 6 - Shot #4930



A. Q
0.1 μsec/Div

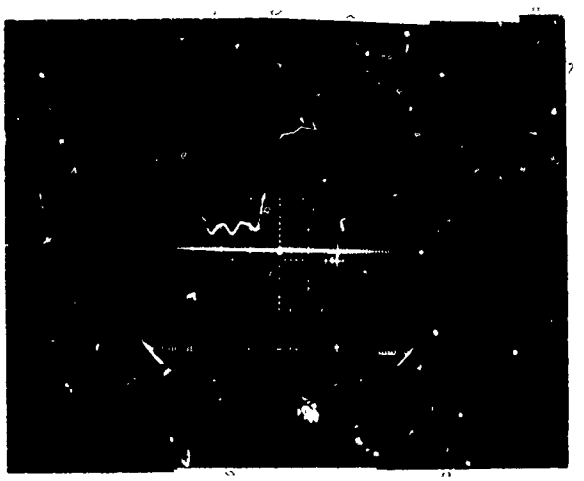
B. $\overline{Q}$
0.1 μsec/Div

Condition 9A - Shot #4924

A. Q
0.1 μsec/Div

B. $\overline{Q}$
10 μsec/Div

Condition 9B - Shot #4923



A. Q
0.1 μsec/Div

B. $\overline{Q}$
10 μsec/Div

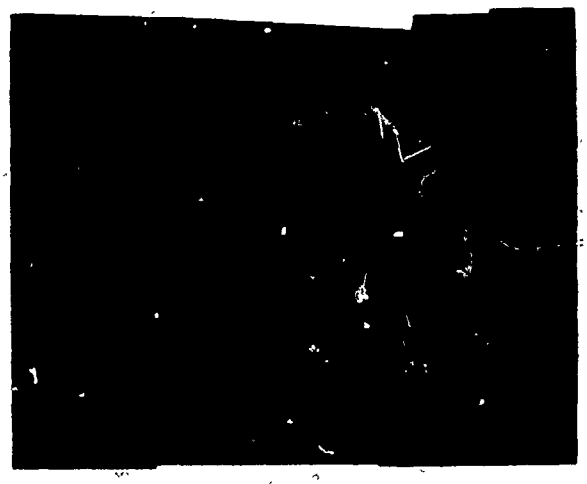
Note: A = Upper Trace; B - Lower Trace.

Condition 10 - Shot #4931

A. Q
0.1 μsec/Div

B. $\overline{Q}$
0.1 μsec/Div

Condition 11 - Shot #4932



A. Q
0.1 μsec/Div

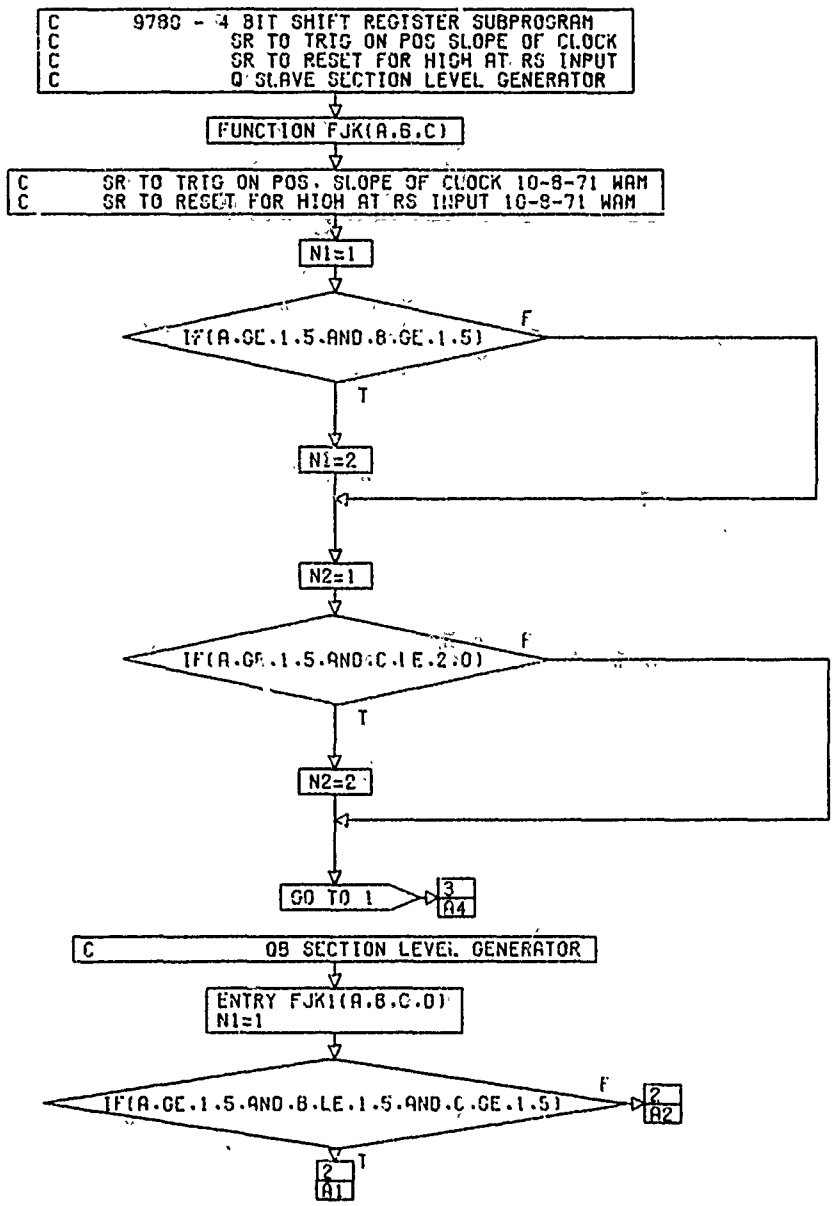
B. $\overline{Q}$
0.1 μsec/Div

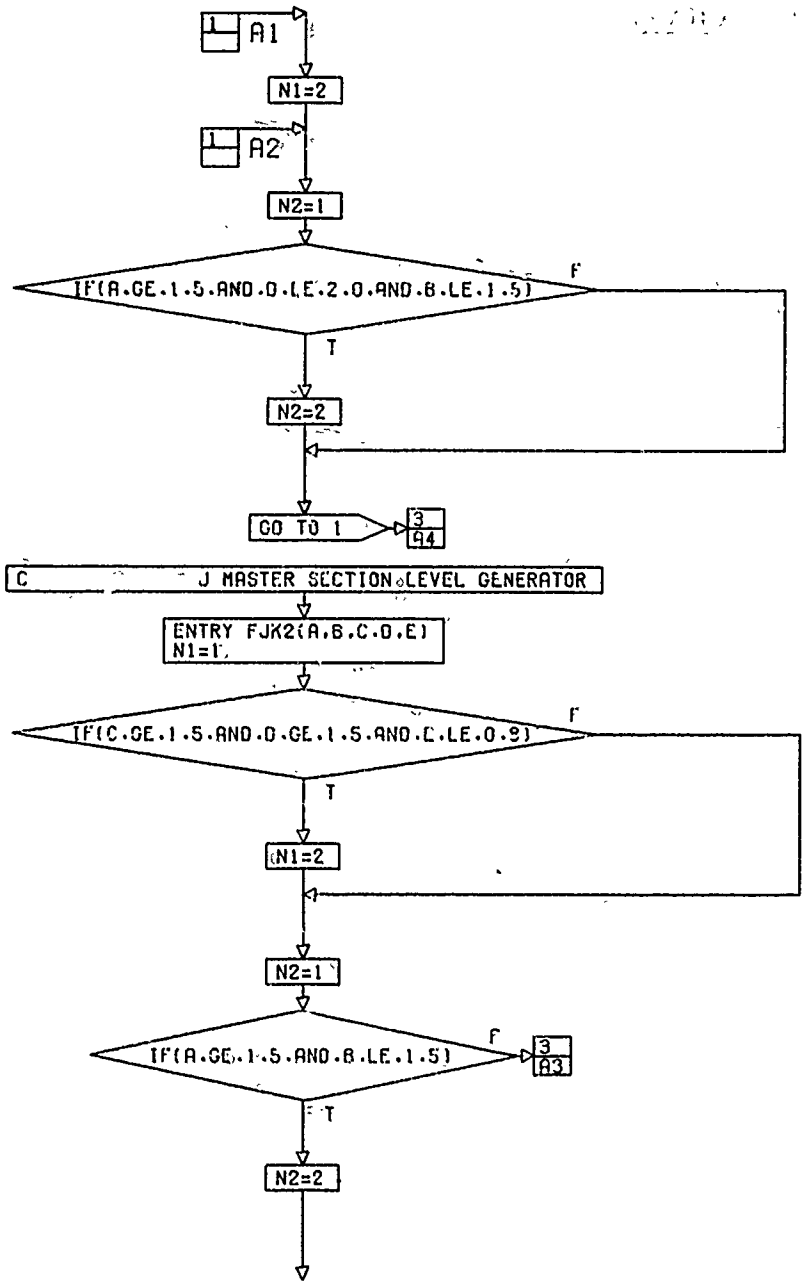
Note: A = Upper Trace; B = Lower Trace.

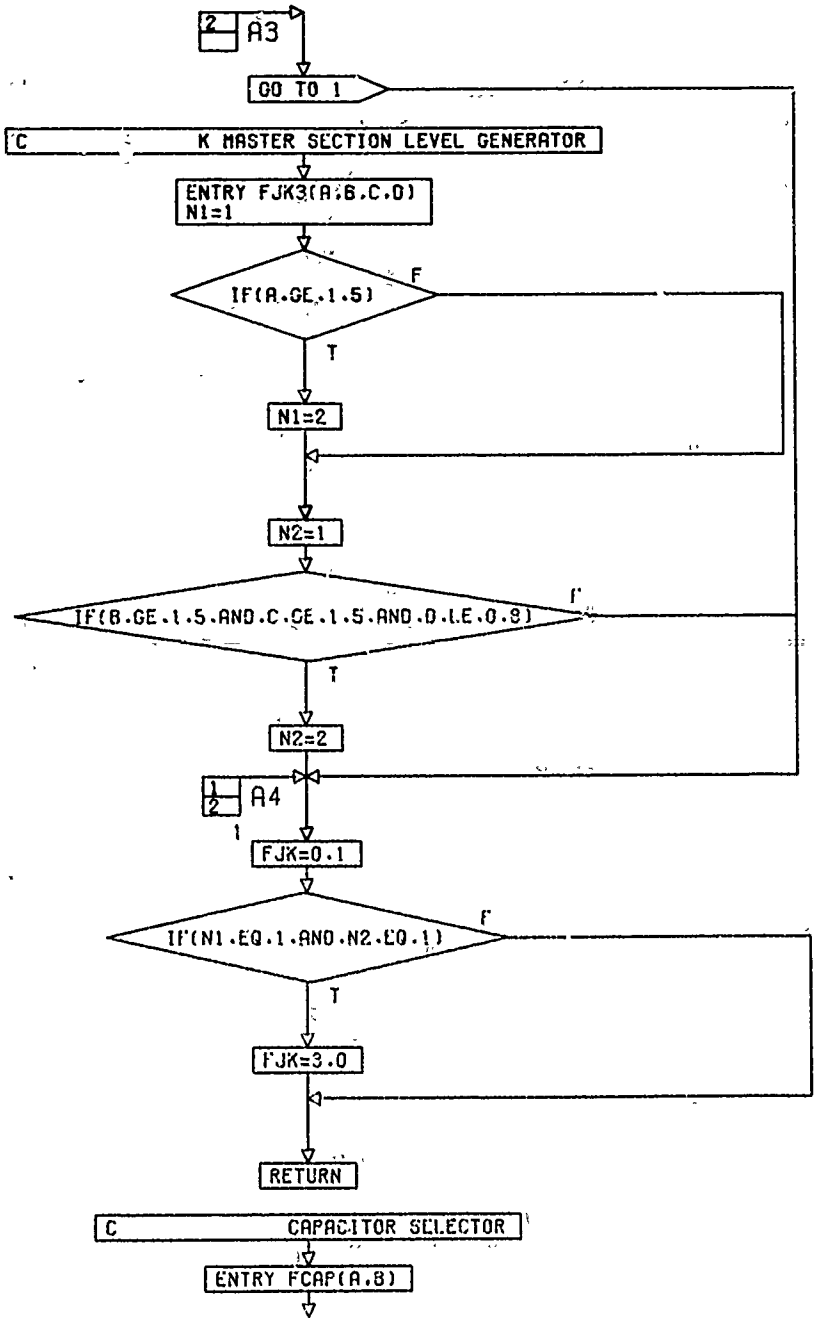
APPENDIX VI

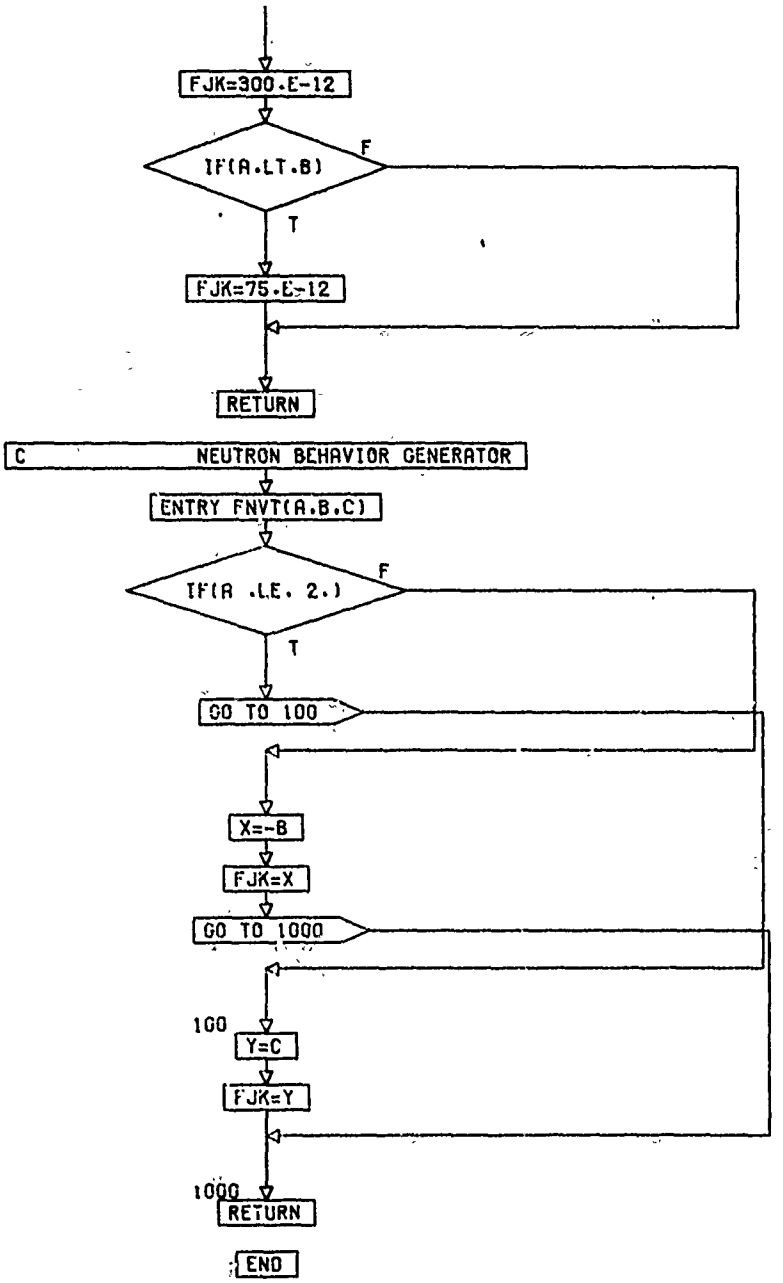
FAIRCHILD 9780 SHIFT REGISTER

A. FLOW CHARTS




1
A1
N1=2
1
A2
N2=1
IF(A.GE.1.5.AND.D.LE.2.0.AND.B.LE.1.5)
F
T
N2=2
GO TO 1
3
A4
C J MASTER SECTION LEVEL GENERATOR
ENTRY FJK2(A,B,C,D,E)
N1=1
IF(C.GE.1.5.AND.D.GE.1.5.AND.C.LE.0.9)
F
T
N1=2
N2=1
IF(A.GE.1.5.AND.B.LE.1.5)
F
3
A3
T
N2=2


2
A3
GO TO 1
C K MASTER SECTION LEVEL GENERATOR
ENTRY FJK3(A,B,C,D)
N1=1
IF(A.GE.1.5)
F
T
N1=2
N2=1
IF(B.GE.1.5.AND.C.GE.1.5.AND.D.LE.0.8)
F
T
N2=2
1
2
A4
1
FJK=0.1
IF(N1.EQ.1.AND.N2.EQ.1)
F
T
FJK=3.0
RETURN
C CAPACITOR SELECTOR
ENTRY FCAP(A,B)


FJK=300.E-12
IF(A.LT.B)
F
T
FJK=75.E-12
RETURN
C NEUTRON BEHAVIOR GENERATOR
ENTRY FNVT(A,B,C)
IF(A .LE. 2.)
F
T
GO TO 100
X=-B
FJK=X
GO TO 1000
100
Y=C
FJK=Y
1000
RETURN
END

B. TEST CONDITIONS AND RESULTS

1. GAMMA RADIATION

Four (4) of these radiation hardened devices were tested on the flash X-ray machine at dose rates of about 1.9×10^{10} rads (Si)/second in an active high fanout circuit. Transient responses were recorded (from every Q_i output) for various conditions.

Each device was exposed to at least 8 shots covering five test conditions. Data for sample #2 are reported here, with test conditions shown in Table 6-1.

All test conditions show transient response due to radiation compared with pretest performance, as seen in the first photograph.

2. NEUTRON RADIATION

All neutron radiation behavior was obtained from Reference #2.*

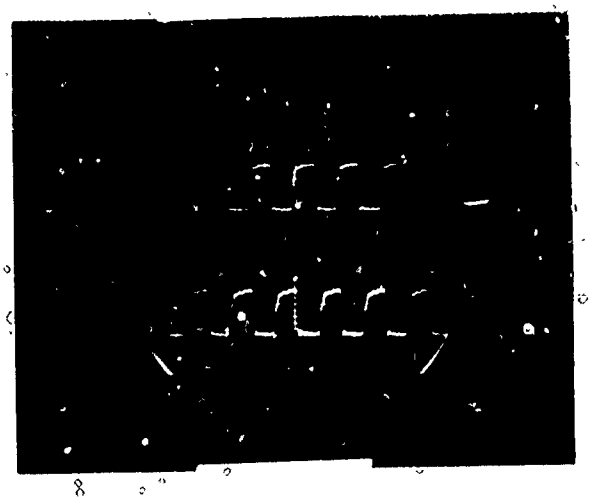
TABLE 6-1.

TEST CONDITIONS

SHOT#	COND. #	J	K	C_D	C_P
Pretest	1	H	H	L	Clocking
5591	1	H	H	L	Clocking
5595	2	L	L	L	Clocking
5596	3	H	H	H	Clocking
5597	4	L	H	L	Clocking
5599	5	H	L	L	Clocking

*Clemens, D. P., op. cit. page 121

Pretest - Condition 1



A. Q_0
0.1 V/Div
0.2 μsec/Div

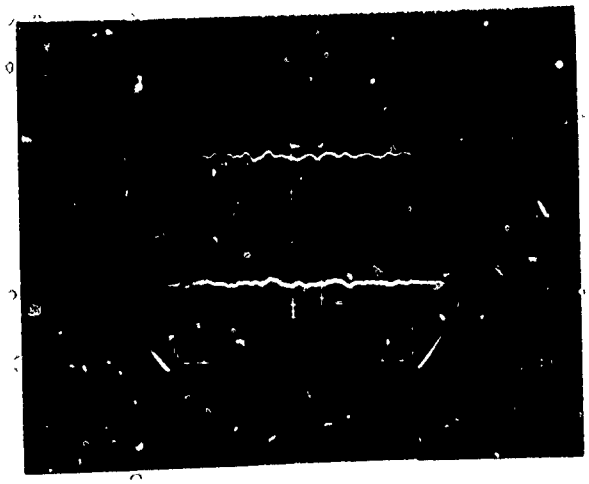
B. Q_1
0.1 V/Div
0.2 μsec/Div

Condition 1 - Dose 432r-Shot #5591

A. Q_0
0.1 V/Div
0.2 μsec/Div

B. Q_1
0.1 V/Div
0.2 μsec/Div

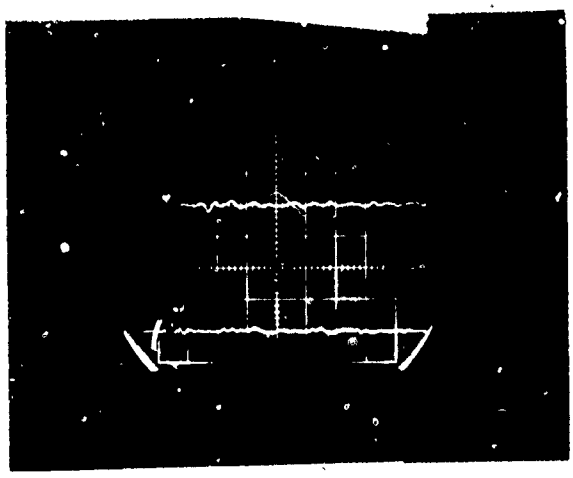
Condition 2 - Dose 432r-Shot #5595



A. Q_0
0.1 V/Div
0.1 μsec/Div

B. Q_1
0.1 V/Div
0.1 μsec/Div

Condition 3 - Dose 432r-Shot #5596



A. Q_0
0.1 V/Div
0.1 μsec/Div

B. Q_1
0.1 V/Div
0.1 μsec/Div

*A = Upper Trace; B = Lower Trace.

Condition 4 - Dose 432r-Shot #5597

A. Q_0
0.1 V/Div
0.1 μsec/Div

B. Q_1
0.1 V/Div
0.1 μsec/Div

Condition 5 - Dose 432r-Shot #5599

A. Q_0
0.1 V/Div
0.1 μsec/Div

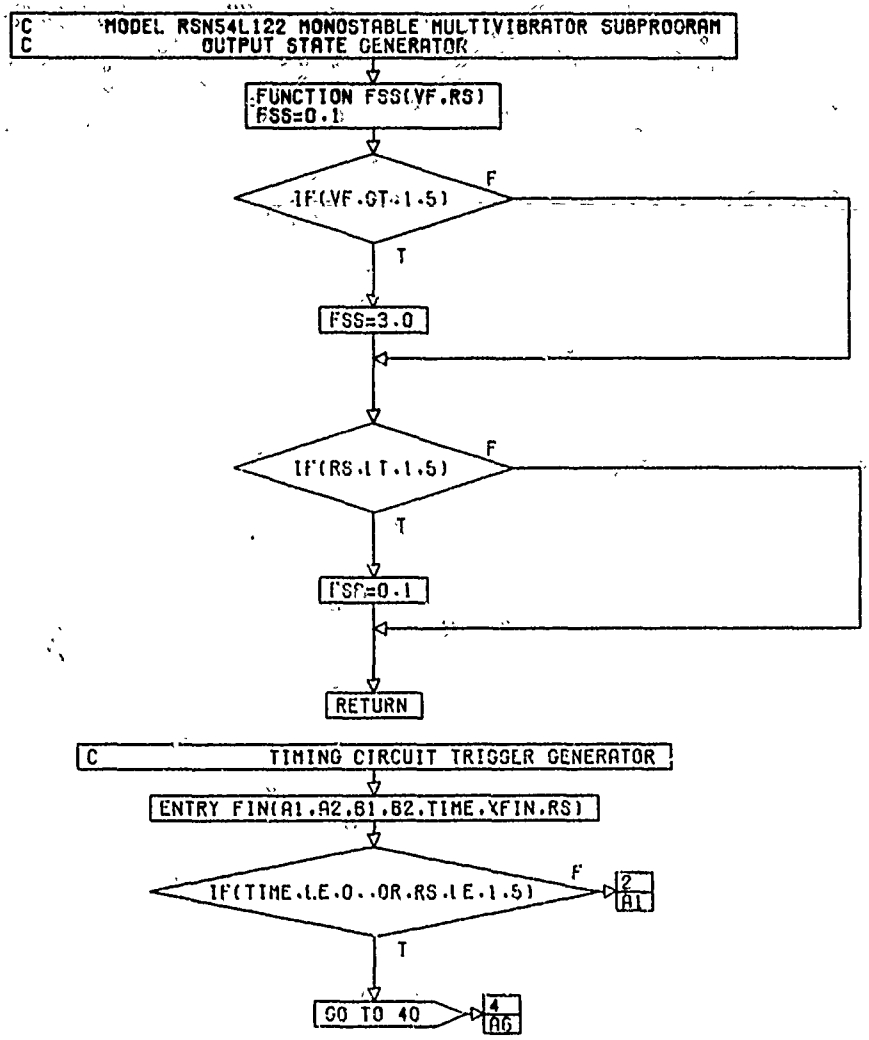
B. Q_1
0.1 V/Div
0.1 μsec/Div

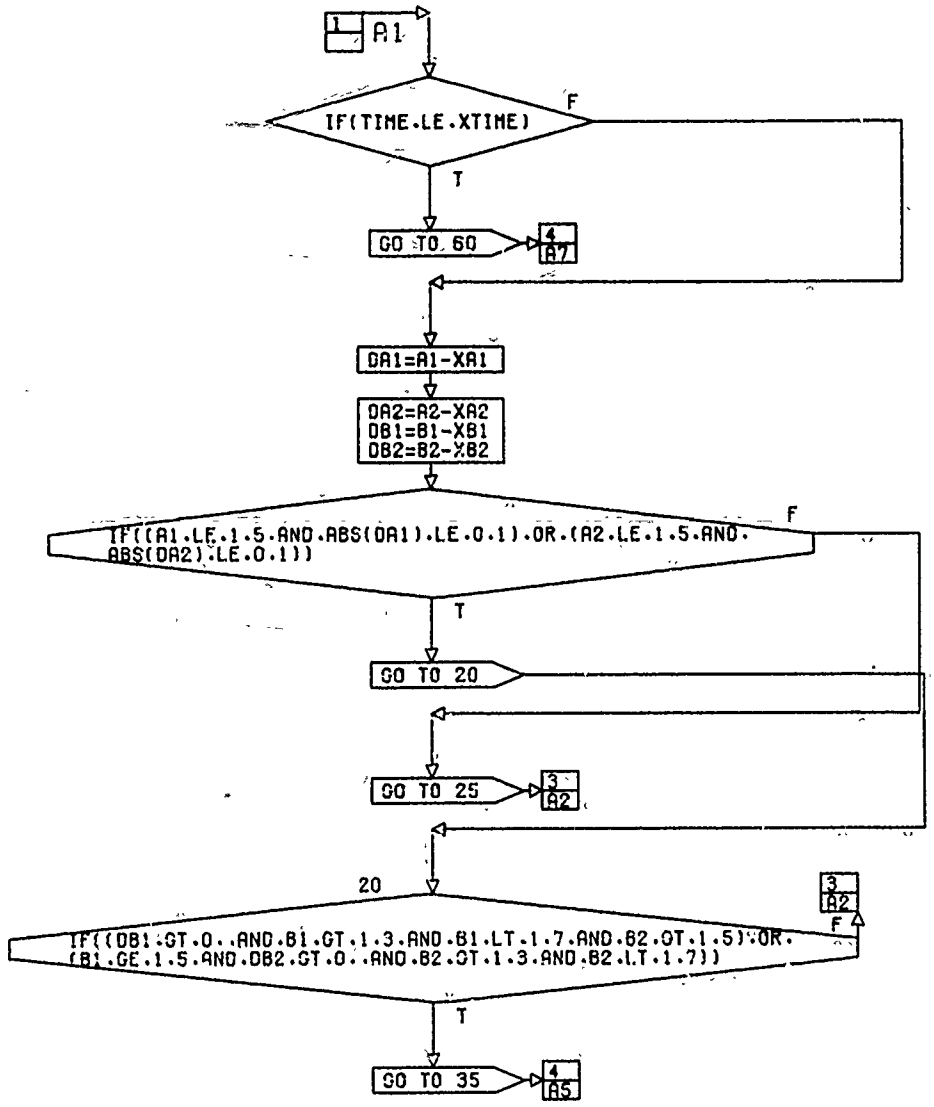
Note: A = Upper Trace; B = Lower Trace.

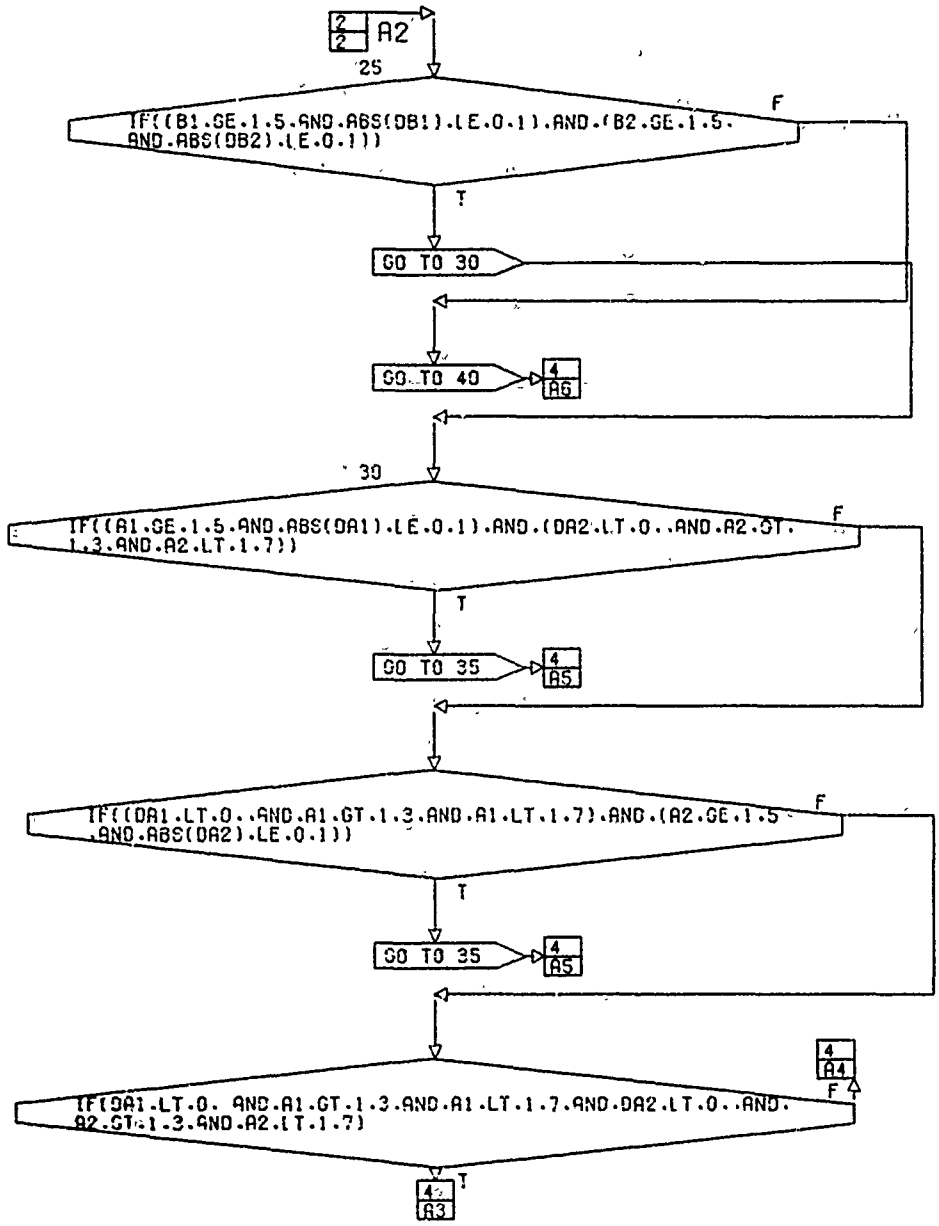
APPENDIX VII

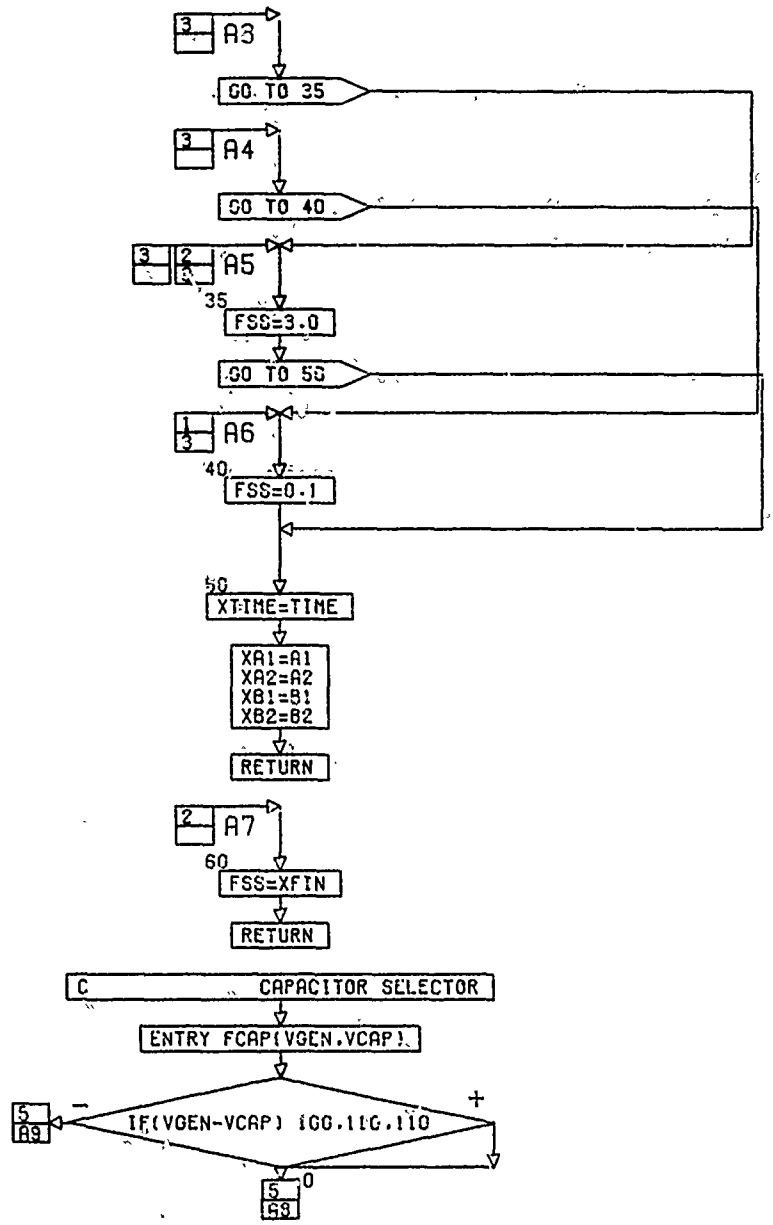
RSN54L122

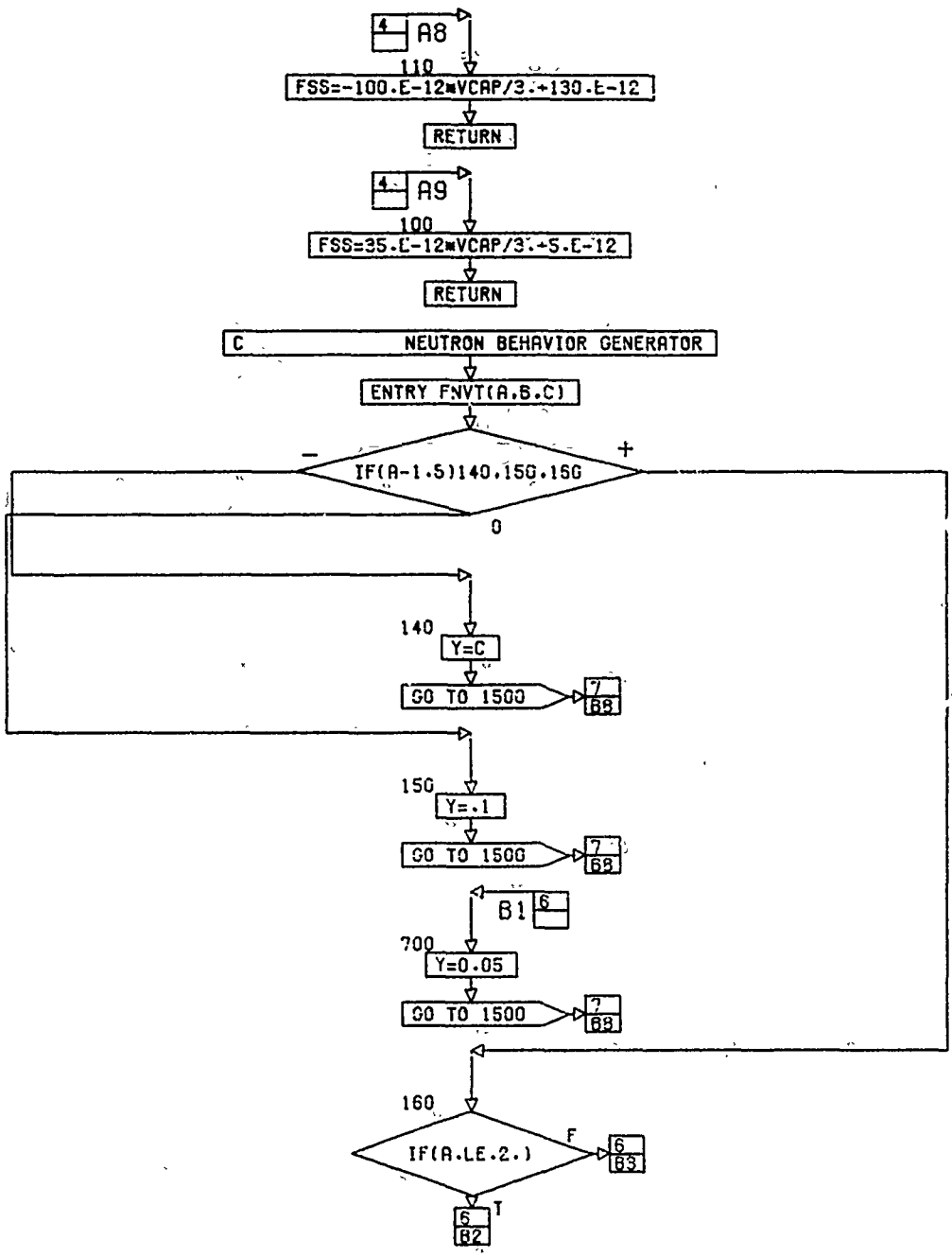
A. FLOW CHARTS

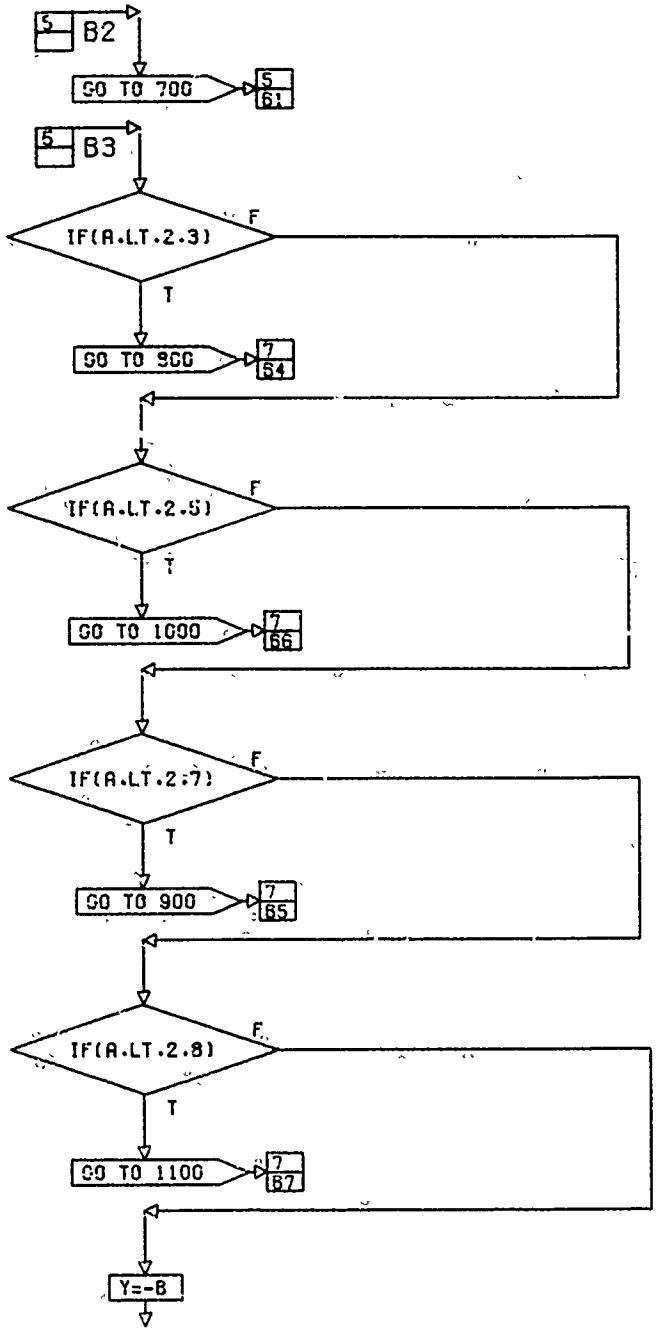


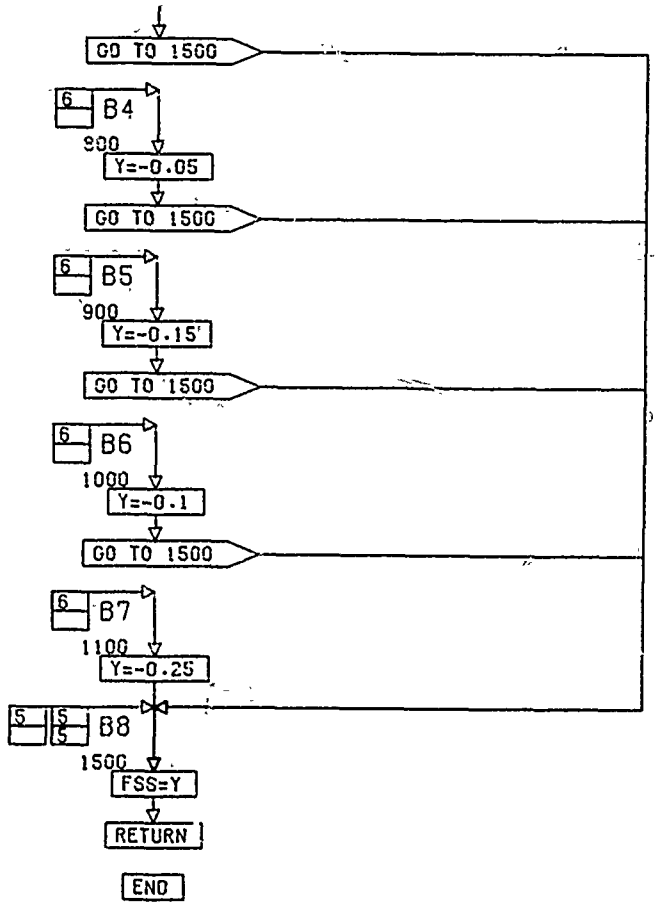

1
A1
IF(TIME.LE.XTIME)
F
T
GO TO 60
4
A7
DA1=A1-XA1
DA2=A2-XA2
DB1=B1-XB1
DB2=B2-XB2
IF((A1.LE.1.5.AND.ABS(DA1).LE.0.1).OR.(A2.LE.1.5.AND.
ABS(DA2).LE.0.1))
F
T
GO TO 20
GO TO 25
3
A2
20
3
A2
IF((DB1.GT.0..AND.B1.GT.1.3.AND.B1.LT.1.7.AND.B2.GT.1.5).OR.
(B1.GE.1.5.AND.DB2.GT.0..AND.B2.GT.1.3.AND.B2.LT.1.7))
F
T
GO TO 35
4
A5


2
2
A2
25
IF((B1.GE.1.5.AND.ABS(DB1).LE.0.1).AND.(B2.GE.1.5.
AND.ABS(DB2).LE.0.1))
F
T
GO TO 30
GO TO 40
4
A6
30
IF((A1.GE.1.5.AND.ABS(DA1).LE.0.1).AND.(DA2.LT.0..AND.A2.GT.
1.3.AND.A2.LT.1.7))
F
T
GO TO 35
4
A5
IF((DA1.LT.0..AND.A1.GT.1.3.AND.A1.LT.1.7).AND.(A2.GE.1.5
.AND.ABS(DA2).LE.0.1))
F
T
GO TO 35
4
A5
4
A4
IF(DA1.LT.0. AND.A1.GT.1.3.AND.A1.LT.1.7.AND.DA2.LT.0..AND.
A2.GT.1.3.AND.A2.LT.1.7)
F
T
4
A3


A3
GO TO 35
A4
GO TO 40
A5
35
FSS=3.0
GO TO 50
A6
40
FSS=0.1
50
XTIME=TIME
XA1=A1
XA2=A2
XB1=B1
XB2=B2
RETURN
A7
60
FSS=XFIN
RETURN
C CAPACITOR SELECTOR
ENTRY FCAP(VGEN,VCAP)
IF(VGEN-VCAP) 100,110,110
A9
A8
0


4 A8
110
FSS=-100.E-12*VCAP/3.+130.E-12
RETURN
4 A9
100
FSS=35.E-12*VCAP/3.+5.E-12
RETURN
C NEUTRON BEHAVIOR GENERATOR
ENTRY FNVT(A,B,C)
IF(A-1.5)140,150,160
-
+
0
140
Y=C
GO TO 1500
7 B8
150
Y=.1
GO TO 1500
7 B8
B1 6
700
Y=0.05
GO TO 1500
7 B8
160
IF(A.LE.2.)
F
6 B3
T
6 B2


5
B2
GO TO 700
5
B1
5
B3
IF(A.LT.2.3)
F
T
GO TO 900
7
B4
IF(A.LT.2.5)
F
T
GO TO 1000
7
B6
IF(A.LT.2.7)
F
T
GO TO 900
7
B5
IF(A.LT.2.8)
F
T
GO TO 1100
7
B7
Y=-B


GO TO 1500
6
B4
900
Y=-0.05
GO TO 1500
6
B5
900
Y=-0.15
GO TO 1500
6
B6
1000
Y=-0.1
GO TO 1500
6
B7
1100
Y=-0.25
5
5
5
B8
1500
FSS=Y
RETURN
END

B. TEST CONDITIONS AND RESULTS

1. GAMMA RADIATION

Seven (7) of the RSN54L122 monostable multi-vibrators were tested at dose rates of about 2.2×10^{10} rads (Si)/second in an active high fanout circuit. Transient output responses (Q, $\overline{Q}$) were recorded for various conditions; the responses were quite similar for each condition among the devices tested. The data presented here is for sample #36 for the test conditions shown on Table 7-1.

Typically, the output was a single pulse for test conditions 1, 2, and 3. On test conditions 4 and 5, the recovery was in the low microsecond range and device output was subnormal for a few microseconds (5-20 "Clock Pulses"). The time to recovery is shown, but generally for $\overline{Q}$, not Q.

NOTE: The RSN device has an 800 ns pulse width (min) compared to that of the SN device of 90 ns; in these tests the 800 ns was reduced by using a 2KΩ resistor in the timing circuit, rather than the worst case value of 5KΩ; this wiring change turns 2 diodes on without hurting the circuit (radiation would also turn them on). The 2KΩ was used to obtain a higher repetition rate and also to determine the clocked recovery time more accurately.

2. NEUTRON RADIATION

All neutron radiation behavior data was obtained from Reference #1*.

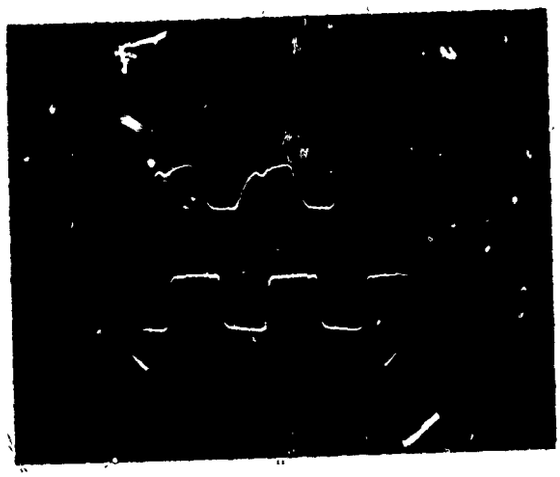
TABLE 7-1.

TEST CONDITIONS

SHOT#	COND. #	A_1	$B_1 - A_2$	B_2
Pretest	5			
5506	1	H	H	H
5507	2	H	H	L
5508	3	L	H	H
5505	4	L	H	Clocking
5502	5	Clocking	H	H

*Olson, R. J., op. cit. page 16

Pretest – Condition 5



A. Q
0.1 V/Div
0.1 μsec/Div

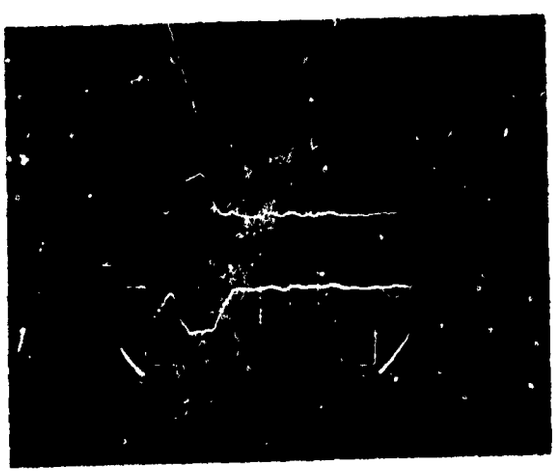
B. A1
2.0 V/Div
0.1 μsec/Div

Condition 1 – Dose 504r-Shot#5506

A. Q
0.1 V/Div
0.1 μsec/Div

B. $\overline{Q}$
0.1 V/Div
0.1 μsec/Div

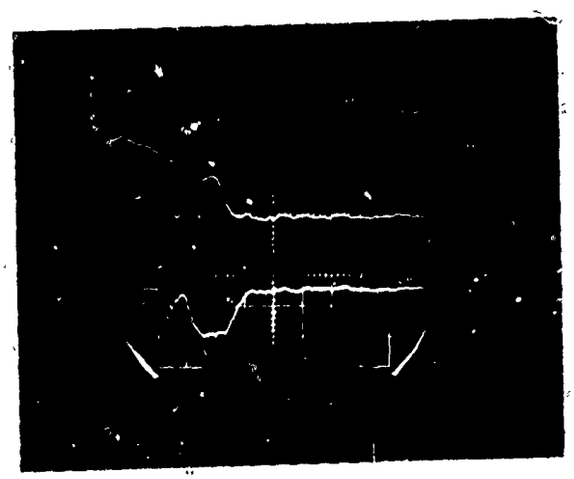
Condition 2 – Dose 504r-Shot#5507



A. Q
0.1 V/Div
0.1 μsec/Div

B. $\overline{Q}$
0.1 V/Div
0.1 μsec/Div

Condition 8 – Dose 504r-Shot#5508



A. Q
0.1 V/Div
0.1 μsec/Div

B. $\overline{Q}$
0.1 V/Div
0.1 μsec/Div

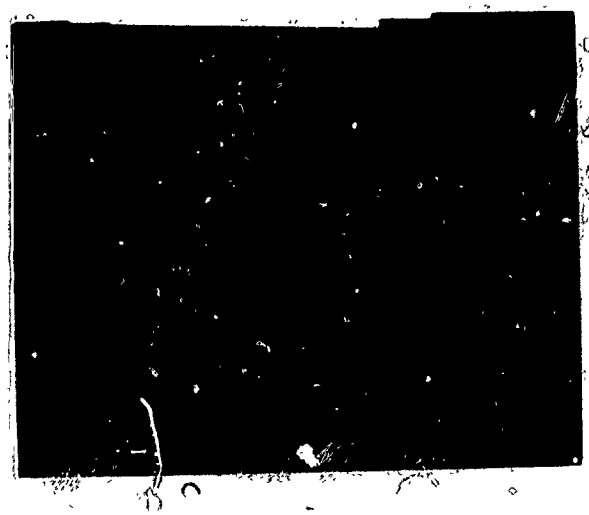
*A = Upper Trace; B = Lower Trace.

Condition 4 - Dose 504r-Shot#5505

A. $\bar{Q}$
0.1 V/Div
0.1 μsec/Div

B. $\bar{Q}$
0.1 V/Div
0.1 μsec/Div

Condition 5 - Dose 504r-Shot#5502



A. Q
0.1 V/Div
0.1 μsec/Div

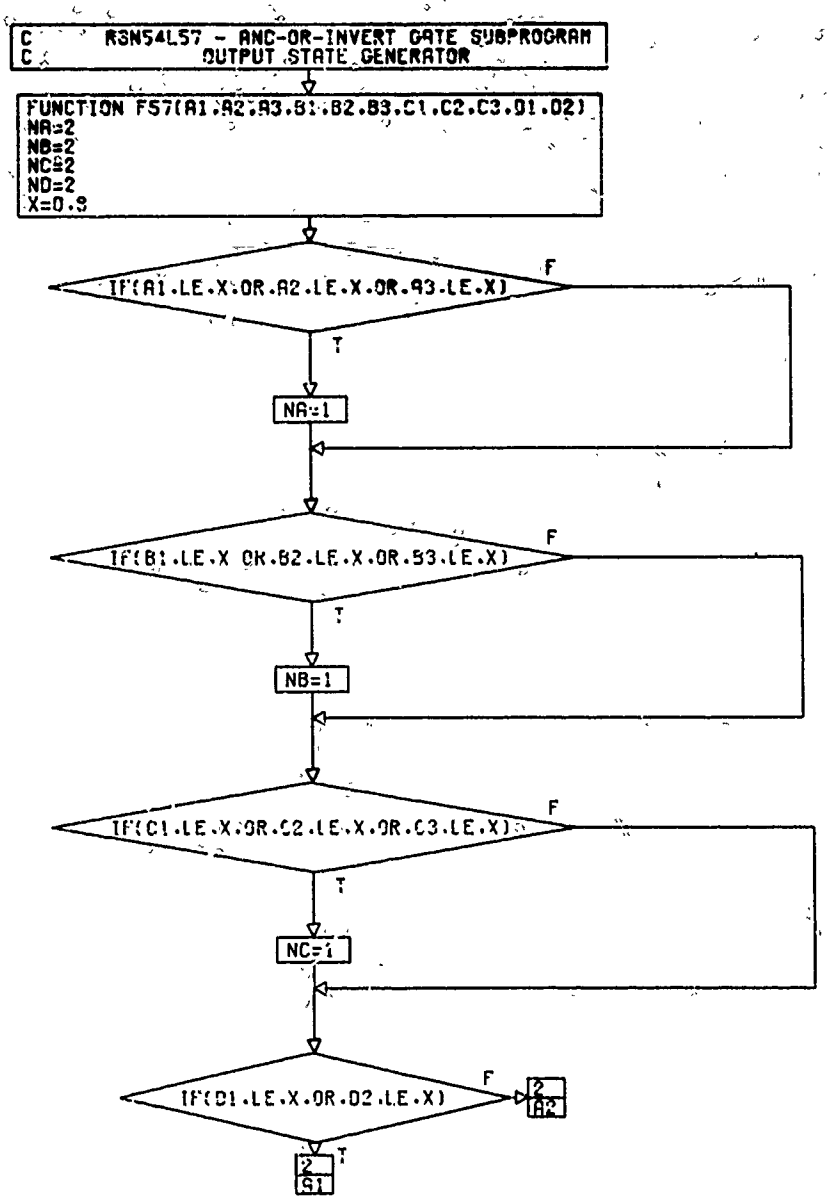
B. $\bar{Q}$
0.1 V/Div
0.1 μsec/Div

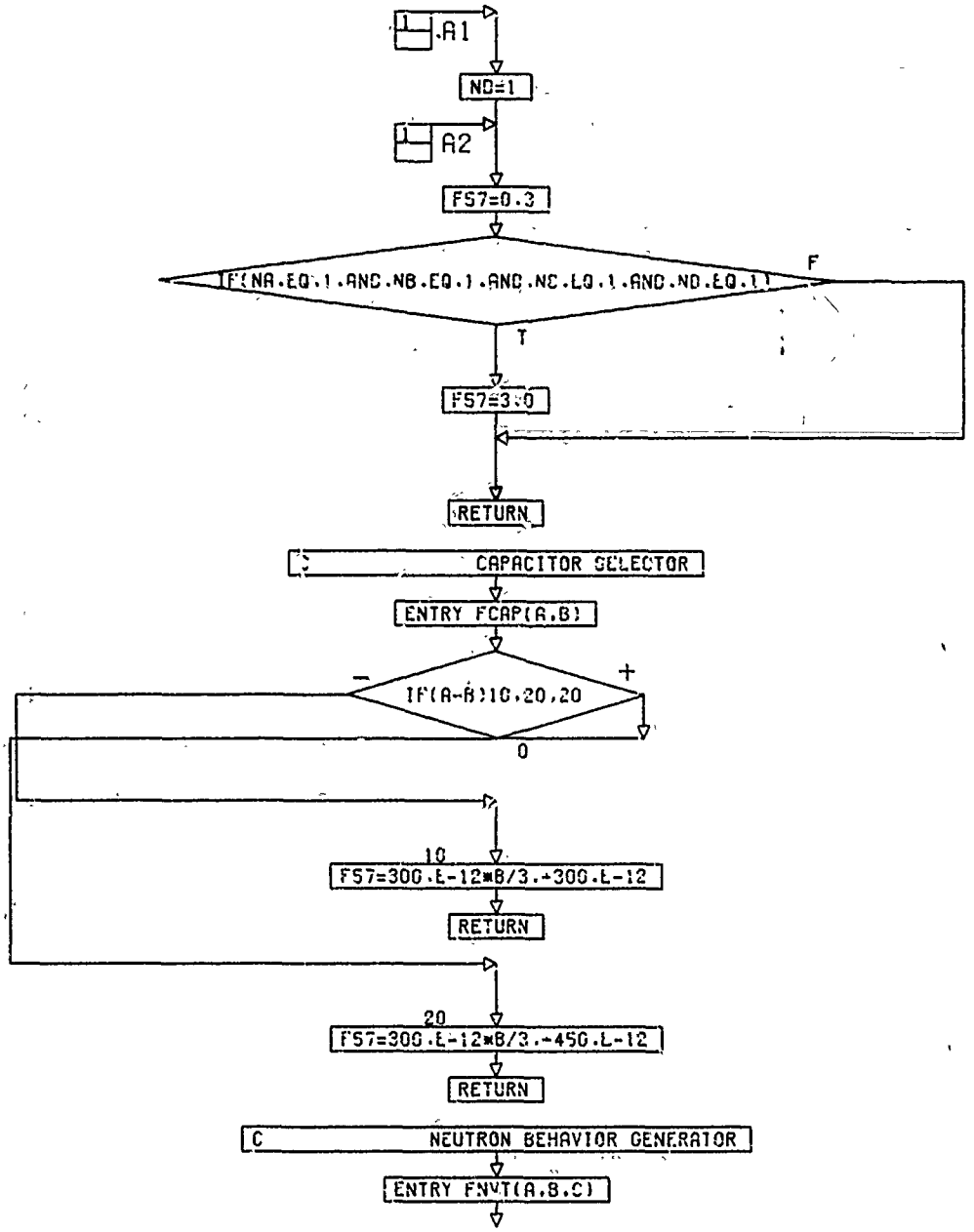
Note: A = Upper Trace; B = Lower Trace.

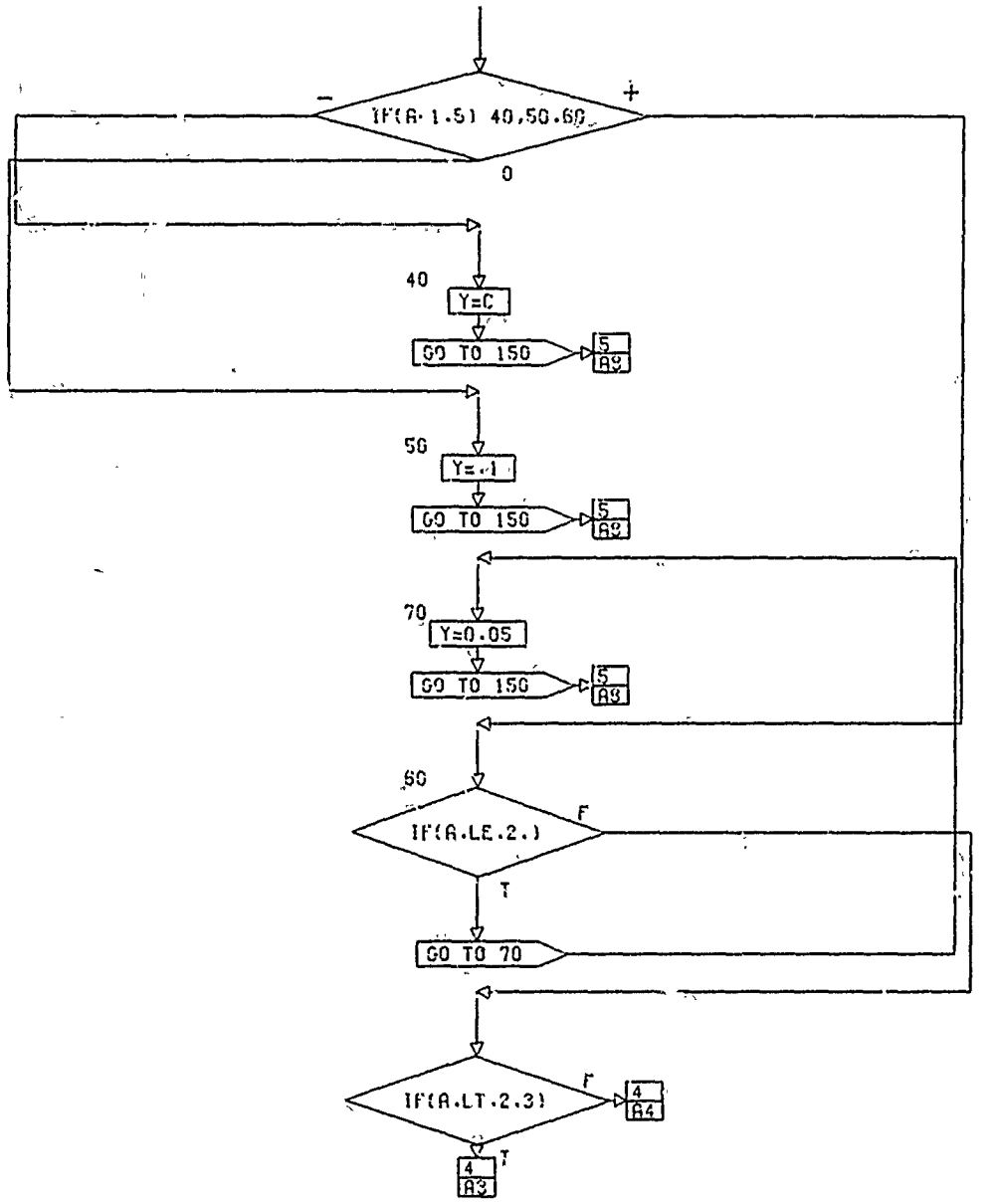
APPENDIX VIII

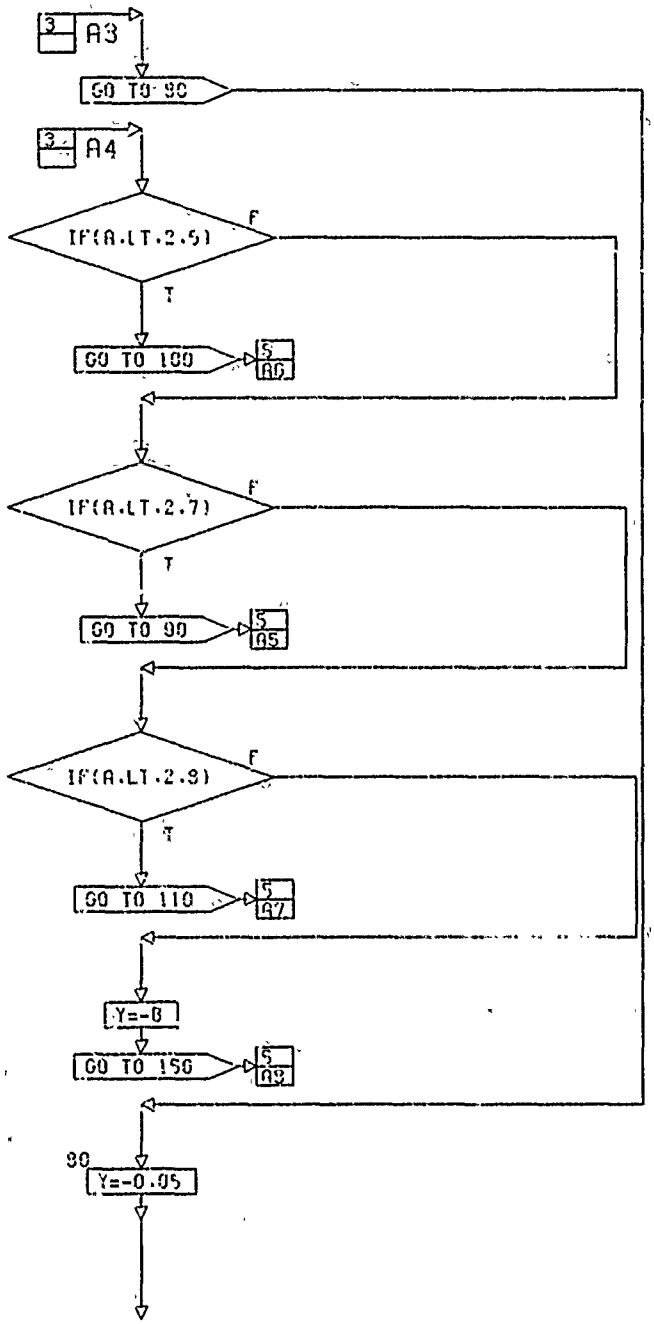
RSN54L57

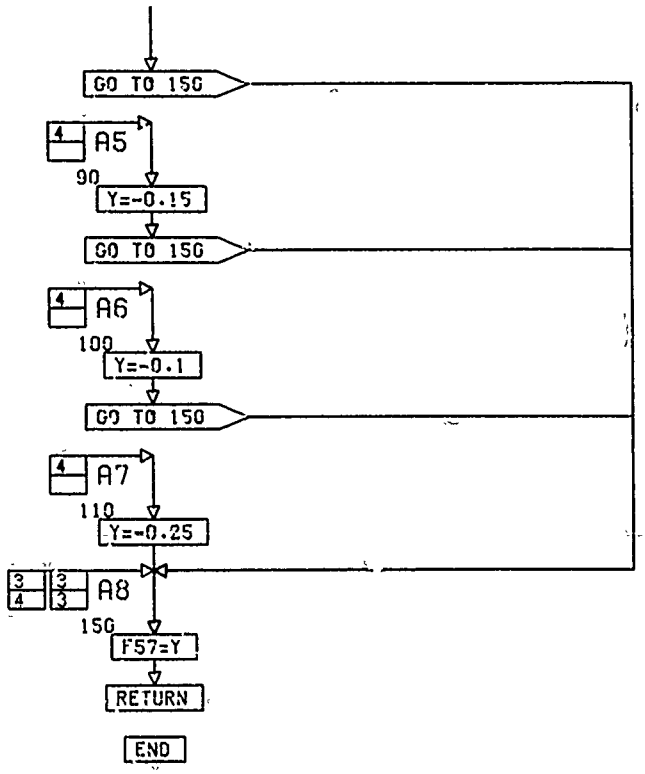
A. FLOW CHARTS




1 A1
ND=1
1 A2
FS7=0.3
IF(NA.EQ.1.AND.NB.EQ.1.AND.NC.EQ.1.AND.ND.EQ.1)
F
T
FS7=3.0
RETURN
C CAPACITOR SELECTOR
ENTRY FCAP(A,B)
IF(A-B)10,20,20
−
+
0
10
FS7=300.E-12*B/3.-300.E-12
RETURN
20
FS7=300.E-12*B/3.-450.E-12
RETURN
C NEUTRON BEHAVIOR GENERATOR
ENTRY FNVT(A,B,C)


IF(A-1.5) 40,50,60
-
+
0
40
Y=C
GO TO 150
5
A9
50
Y=-1
GO TO 150
5
A9
70
Y=0.05
GO TO 150
5
A3
60
IF(A.LE.2.)
F
T
GO TO 70
IF(A.LT.2.3)
F
4
A4
T
4
A3


3
A3
GO TO 90
3
A4
IF(A.LT.2.5)
F
T
GO TO 100
5
A6
IF(A.LT.2.7)
F
T
GO TO 90
5
A5
IF(A.LT.2.9)
F
T
GO TO 110
5
A7
Y=-8
GO TO 150
5
A9
90
Y=-0.05



B. TEST CONDITIONS AND RESULTS

1. GAMMA RADIATION

Five (5) of the RSN54L57 And-Or-Invert gate devices were tested in an active circuit at an average dose rate of 1.45×10^{10} rads (Si)/second over a 20 nanosecond pulse. Transient output responses were recorded for various conditions; responses were quite similar and recovery was rapid. The results for Sample 89 are presented here.

The clocked input frequency was maintained at 1 MHz; identified as A1 on the pretest shot. Exposures were made for 5 different test conditions, as noted on the Table 8-1.

2. NEUTRON RADIATION

All neutron radiation behavior data was obtained from Reference 1. *

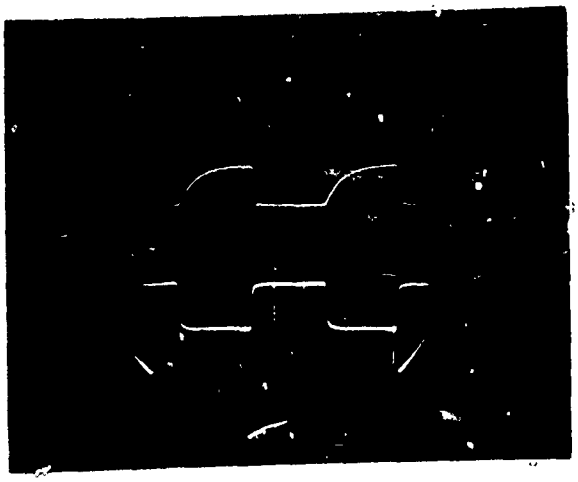
*Olson, R. J., op. cit. page 16

TABLE 8-1.

TEST CONDITIONS

SHOT#	COND. #	1 1A	2,3,5 2	6,7,8 3	9,10 4	13,14 1B
Pretest	3					
5575	1	H	H	H	H	H
5576	2	L	L	L	L	L
5572	3	Clock	L	L	L	H
5574	4	Clock	H	H	H	H
5577	5	H	L	L	L	H

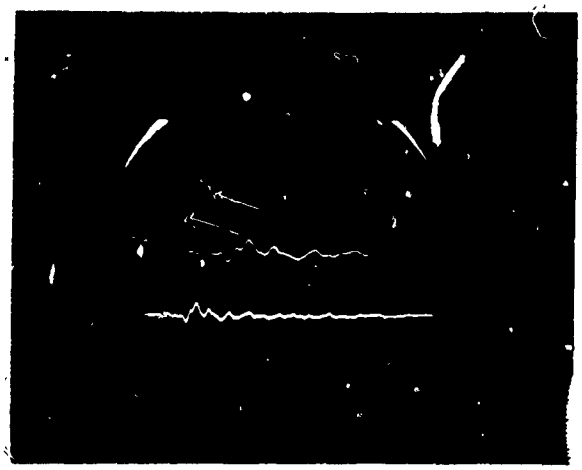
Pretest - Condition 3



A. Out
0.1 V/Div
0.2 μsec/Div

B. A1
2.0 V/Div
0.2 μsec/Div

Condition 1 - Dose 339r-Shot#5575

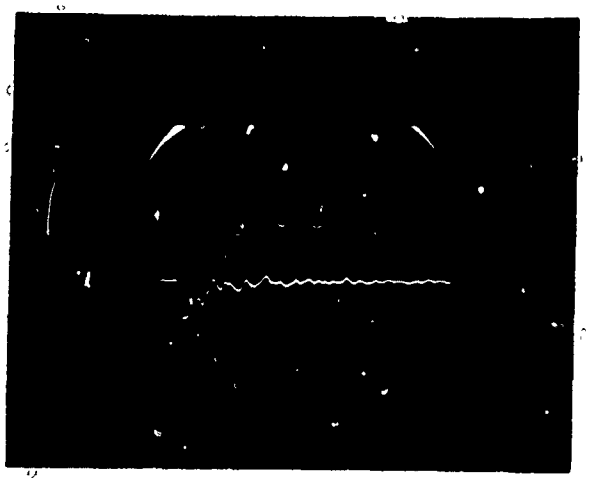


A. Out
0.1 V/Div
0.1 μsec/Div

B. Out
0.1 V/Div
0.1 μsec/Div

*A - Upper Trace; B - Lower Trace.

Condition 2 - Dose 339r-Shot#5576



A. Out
0.1 V/Div
0.1 μsec/Div

B. Out
0.1 V/Div
0.2 μsec/Div

Condition 3 - Dose 339r-Shot#5572

A. Out
0.1 V/Div
0.2 μsec/Div

B. A1
2.0 V/Div
0.2 μsec/Div

Condition 4 - Dose 339r-Shot#5574

A. Out
0.1 V/Div
0.2 μsec/Div

B. A1
2.0 V/Div
0.2 μsec/Div

Condition 5 - Dose 339r-Shot#5577

A. Out
0.1 V/Div
0.1 μsec/Div

B. Out
0.1 V/Div
0.2 μsec/Div

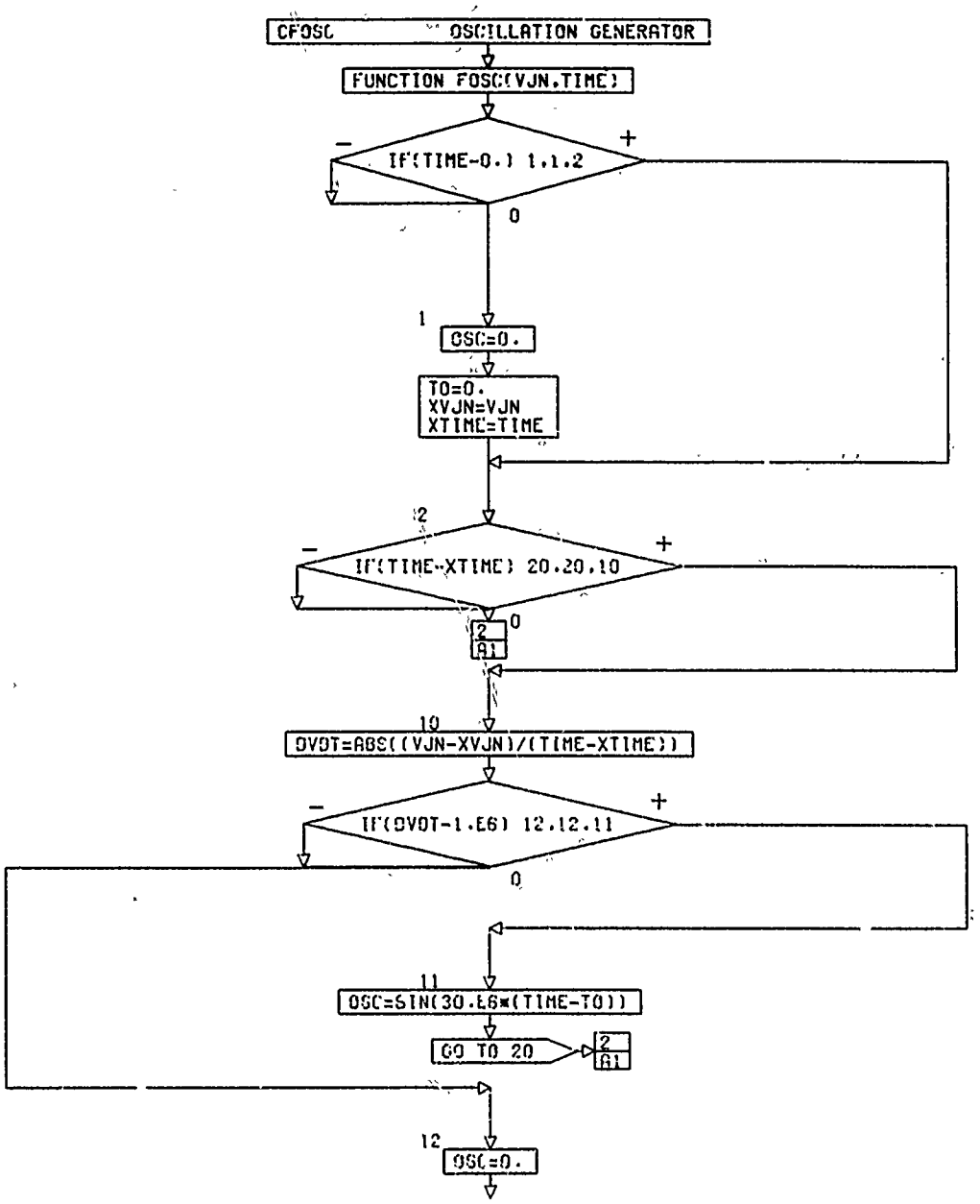
Note: A = Upper Trace; B = Lower Trace.

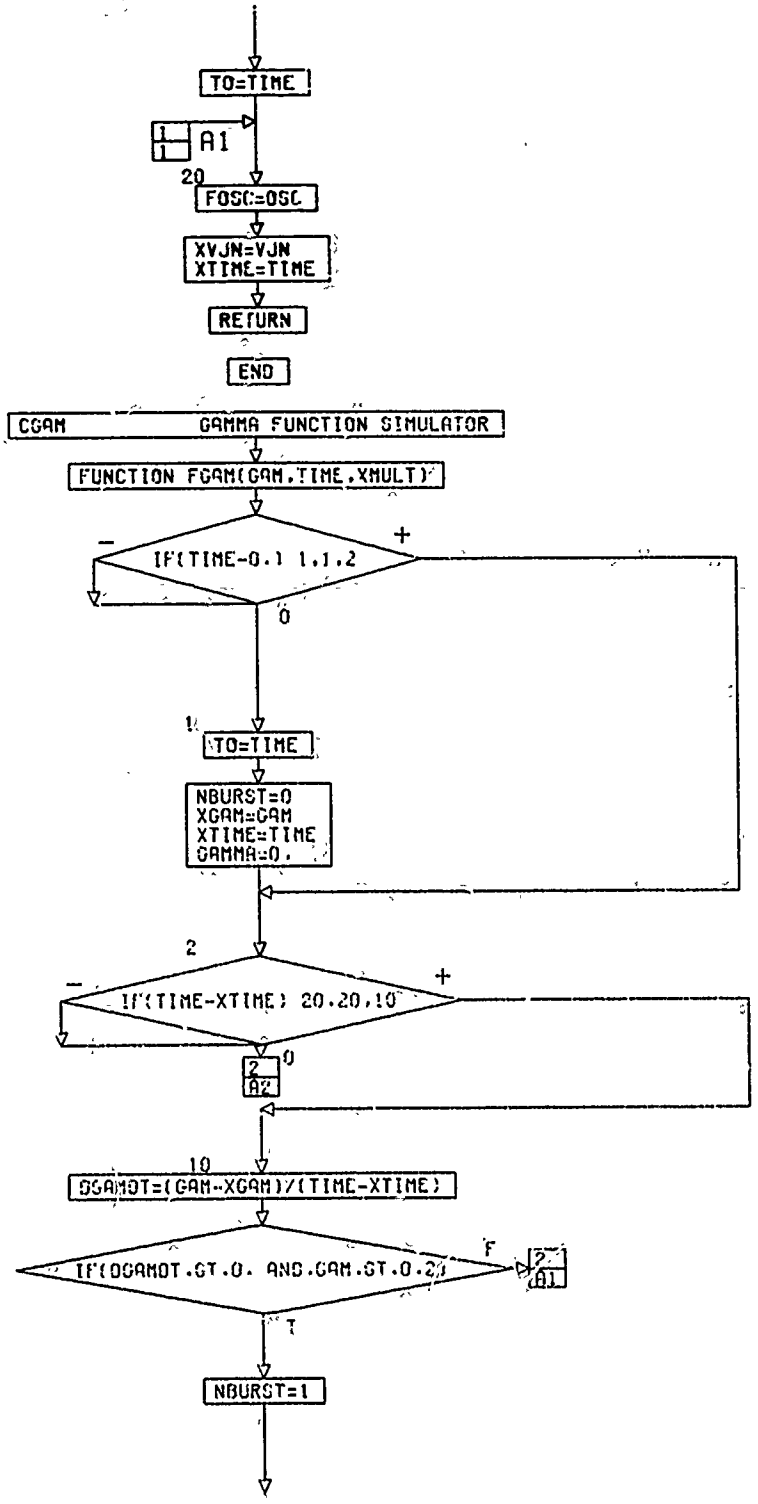
APPENDIX IX

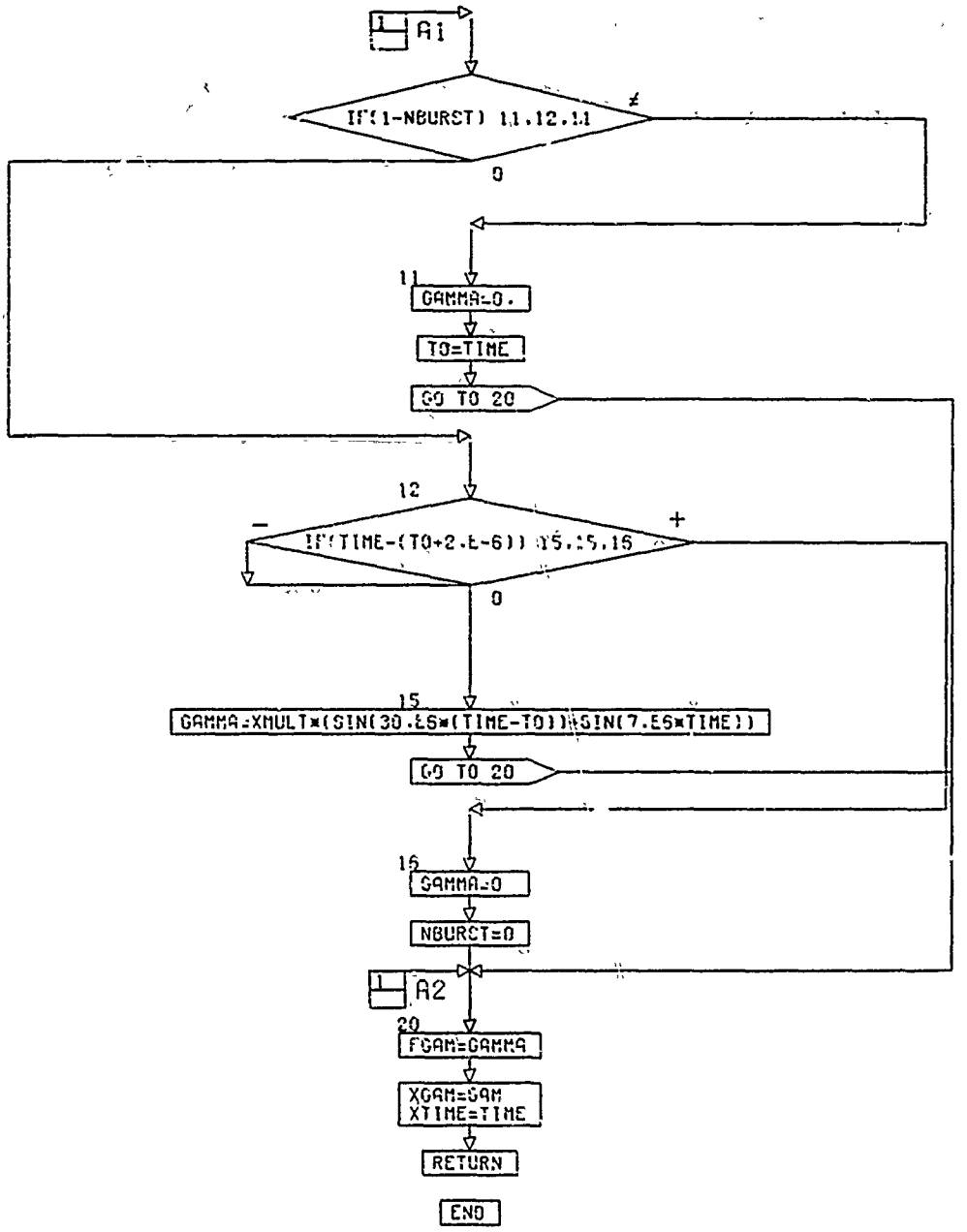
HA-2700

A. FLOW CHARTS

(TO BE SUPPLIED)




TO=TIME
A1
20
FOSC=OSC
XVJN=VJN
XTIME=TIME
RETURN
END
CGAM GAMMA FUNCTION SIMULATOR
FUNCTION FGAM(GAM,TIME,XMULT)
IF(TIME-0.) 1,1,2
1
TO=TIME
NBURST=0
XGAM=GAM
XTIME=TIME
GAMMA=0.
2
IF(TIME-XTIME) 20,20,10
A2
10
DGAMDT=(GAM-XGAM)/(TIME-XTIME)
IF(DGAMDT.GT.0. AND.GAM.GT.0.2)
A1
NBURST=1


A1
IF(1-NBURST) 11,12,11
≠
0
11
GAMMA=0.
T0=TIME
GO TO 20
12
IF(TIME-(T0+2.E-6)) 15,15,15
−
+
0
15
GAMMA=XMULT*(SIN(30.E6*(TIME-T0))*SIN(7.E6*TIME))
GO TO 20
16
GAMMA=0
NBURST=0
A2
20
FGAM=GAMMA
XGAM=GAM
XTIME=TIME
RETURN
END

B. TEST CONDITIONS AND RESULTS

1. GAMMA RADIATION

Flash X-ray response data has been obtained for the irradiation of 8 samples of the HA2700-2 general operational amplifier in active circuits. Both gain of 1 and gain of 10 circuits were exposed at 1.2 (±0.1) x 10^{10} rads (Si)/second to a pulse of 20 nanoseconds duration. The time to complete recovery ranged from 5-14 μsec for a gain of 1, and up to 2 μsec for a gain of 10 under the DC input conditions studied. During the time of dynamic effect, the responses exhibited widely varying oscillations to both positive and negative saturation.

A series of photographs, which follow, show the test results. The test conditions are identified in Table 9-1.

TABLE 9-1.

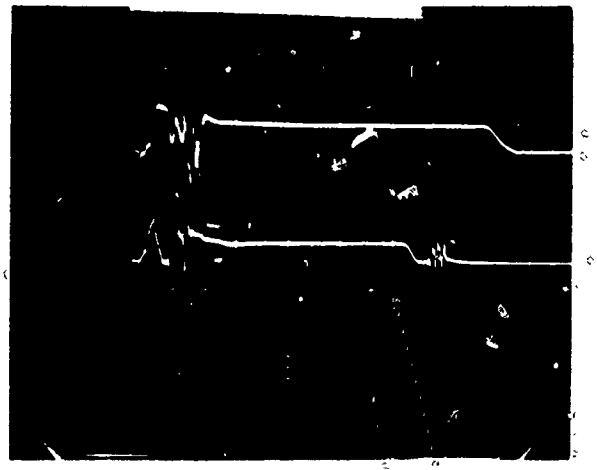
TEST CONDITIONS

SHOT#	CONDITION#	EIN (v)	GAIN	EOUT (v)
5410	1	5.4	1	5.0
5408	2	0	1	0
5411	3	-4.8	1	-5.0
5406	4	.495	10	5.0
5407	5	0	10	0
5405	6	-.495	10	-5.0
5403	7	1.32	10	13.0
5404	8	-1.28	10	-13.0

2. NEUTRON RADIATION

Since no neutron test results were available at the time the computer model was evaluated, the results obtained for the μA744 were assumed for this device. The results of the computer analyses for the assumed neutron fluence levels are shown in Section IX.

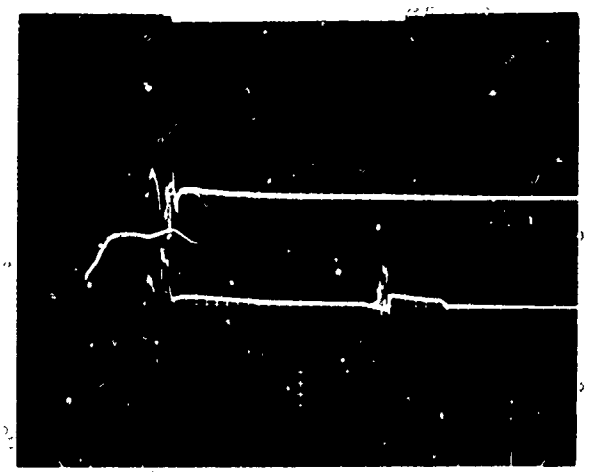
Condition 1 - Shot #5410



A. E_o#F-14
0.2 V/Div
1 μsec/Div

B. E_o#F-13
0.2 V/Div
1 μsec/Div

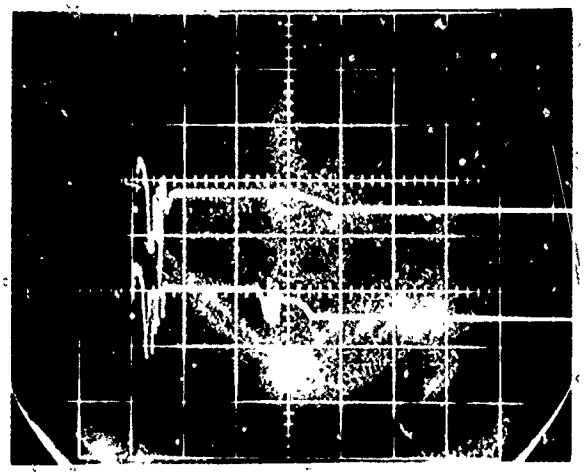
Condition 2 - Shot #5408



A. E_o#F-14
0.2 V/Div
2 μsec/Div

B. E_o#F-13
0.2 V/Div
2 μsec/Div

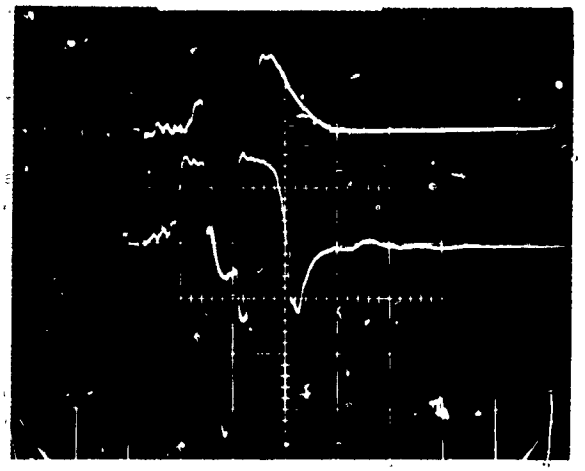
Condition 3 - Shot #5411



A. E_o#F-14
0.2 V/Div
2 μsec/Div

B. E_o#F-13
0.2 V/Div
2 μsec/Div

Condition 4 - Shot #5406

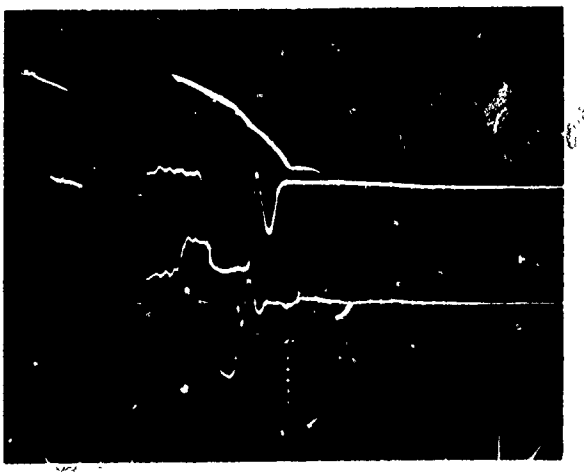


A. E_o#F-14
0.1 V/Div
0.5 μsec/Div

B. E_o#F-13
0.1 V/Div
0.5 μsec/Div

*A = Upper Trace; B = Lower Trace.

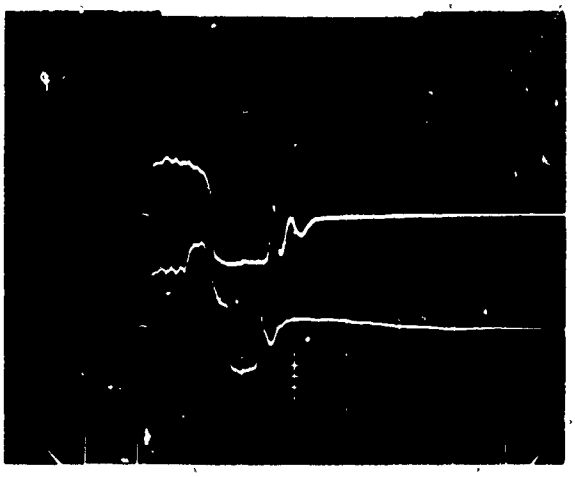
Condition 5 - Shot #5407



A. E_o#F-14
0.2 V/Div
0.5 μsec/Div

B. E_o#F-13
0.2 V/Div
0.5 μsec/Div

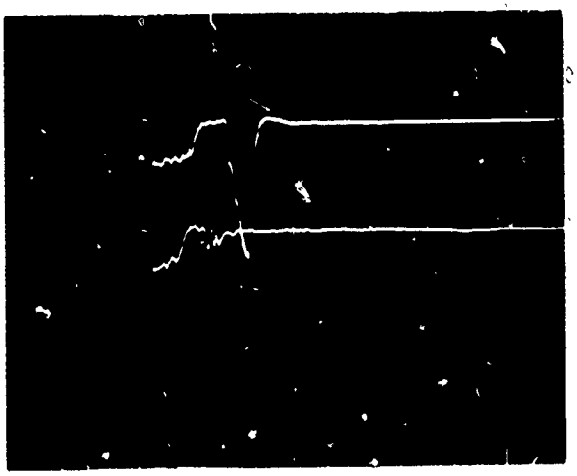
Condition 6 - Shot #5405



A. E_o#F-14
0.2 V/Div
0.5 μsec/Div

B. E_o#F-13
0.2 V/Div
0.5 μsec/Div

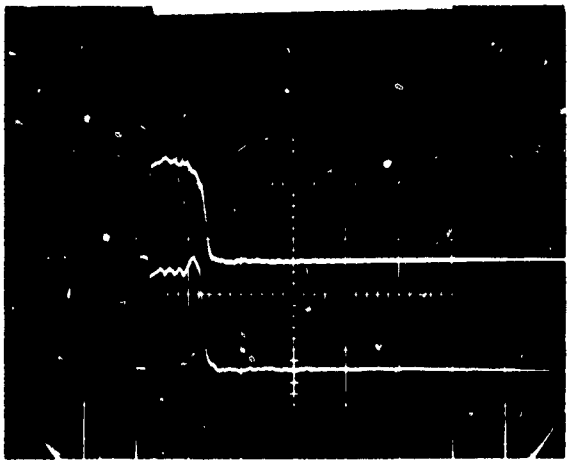
Condition 7 - Shot #5403



A. E_o#F-14
0.2 V/Div
0.5 μsec/Div

B. E_o#F-13
0.2 V/Div
0.5 μsec/Div

Condition 8 - Shot #5404



A. E_o#F-14
0.2 V/Div
0.5 μsec/Div

B. E_o#F-13
0.2 V/Div
0.5 μsec/Div

Note: A = Upper Trace; B = Lower Trace.

APPENDIX X

FAIRCHILD μAMP A744

A. FLOW CHARTS

(Not applicable)

B. TEST CONDITIONS AND RESULTS

1. GAMMA RADIATION

Flash X-ray response data has been obtained with five samples of the Fairchild μA744 Operational Amplifier. Variation in recovery times for the devices was very substantial, ranging from 20 to 110 μseconds in the gain-of-10 configuration. Generally, the response was negative saturation followed by a standard slew rate recovery. The responses presented here are for sample #1.

The average dose rate over a 20 ns radiation pulse was measured at 1.9×10^{10} rads (Si)/second for the tests. The test conditions for which exposures were made are shown on Table 10-1.

TABLE 10-1.

TEST CONDITIONS

SHOT#	COND. #	E_{in} (V)	VOLTAGE GAIN (V)	E_{out} (V)
5460	1	+4.8	1	+5.0
5454	2	0*	1	0
5453	3	-4.8	1	-5.0
5440	4	+0.46	10	+5.0
5437	5	0*	10	0
5439	6	-0.46	10	-5.0
5432	7	+1.2	10	+12.8
5434	8	-1.1	10	-12.8

-V = -15V

+V = +15V

*Leads shorted at power supply.

2. NEUTRON RADIATION

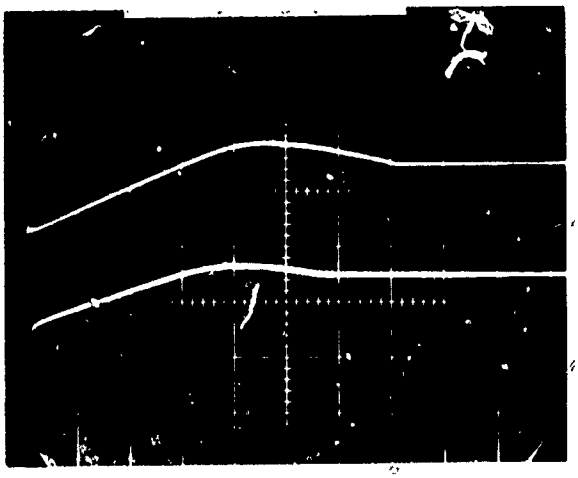
Samples from three runs of the μA744 were submitted to Northrup for reactor irradiation at four levels between 2×10^{12} and 10^{14} nvt, using 2 samples per run per level. Pre and post test measurements were made on 9 parameters. The only parameters showing significant variations with radiation were the open loop voltage gain and the input bias current; these effects are shown in Table 10-2.

TABLE 10-2.

NEUTRON FLUENCE DEGRADATION OF GAIN AND INPUT BIAS CURRENT

FLUENCE (nvt)	GAIN	INPUT BIAS CURRENT
0	50K	90 na
2×10^{12}	50K	120 na
1×10^{13}	45K	200 na
3×10^{13}	33K	300 na
1×10^{14}	18K	700 na

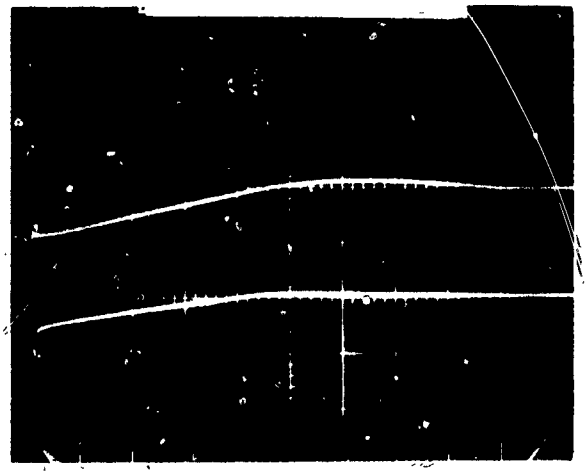
Condition 1 - Shot #5460



A. E_o#1
0.2 V/Div
10 μsec/Div

B. E_o#2
0.2 V/Div
10 μsec/Div

Condition 2 - Shot #5454



A. E_o#1
0.2 V/Div
5 μsec/Div

B. E_o#2
0.2 V/Div
5 μsec/Div

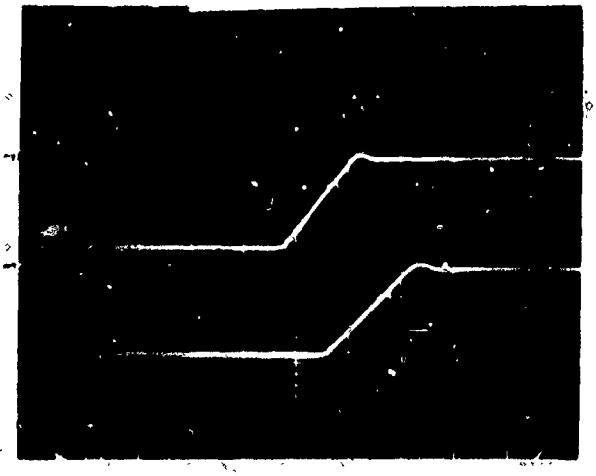
*A = Upper Trace; B = Lower Trace.

Condition 3 - Shot #5453

A. E_o#1
0.2 V/Div
5 μsec/Div

B. E_o#2
0.2 V/Div
5 μsec/Div

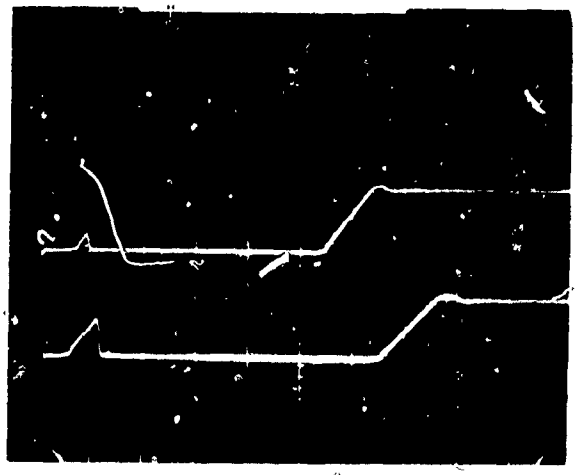
Condition 4 - Shot #5440



A. E_o#1
0.2 V/Div
5 μsec/Div

B. E_o#2
0.2 V/Div
5 μsec/Div

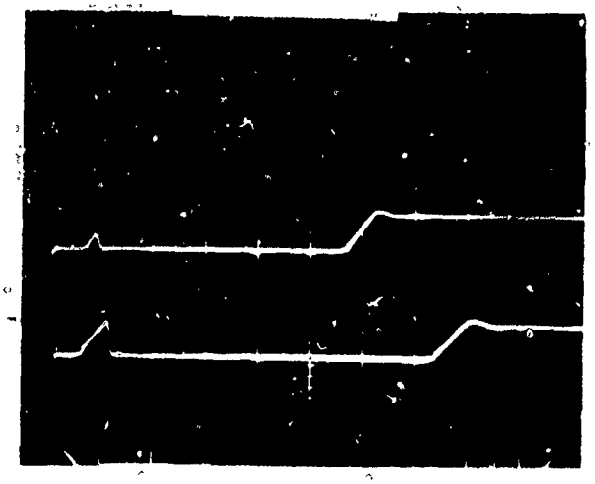
Condition 5 - Shot #5437



A. E_o#1
0.2 V/Div
5 μsec/Div

B. E_o#2
0.2 V/Div
5 μsec/Div

Condition 6 - Shot #5439



A. E_o#1
0.2 V/Div
5 μsec/Div

B. E_o#2
0.2 V/Div
5 μsec/Div

Note: A = Upper Trace; B = Lower Trace.

Condition 7 - Shot #5432

A. E_o#1
0.2 V/Div
10 μsec/Div

B. E_o#2
0.2 V/Div
10 μsec/Div

Condition 8 - Shot #5434

A. E_o#1
0.2 V/Div
1 μsec/Div

B. E_o#2
0.2 V/Div
1 μsec/Div

Note A = Upper Trace; B = Lower Trace.