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SPUTTERED THIN FILM RESEARCH

Alexander J. Shuskus, et al

United Aircraft Research Laboratories

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SPUTTERED THIN FILM RESEARCH

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The deposition of aluminum nitride was studied by comparing results obtained by reactive rf sputtering in nitrogen and ammonia ambients. Physical and optical properties of the films were measured.

Charge storage characteristics of MIS capacitors employing a composite insulator structure of $SrTiO_3$-SiO_2 were studied. The strontium titanate was deposited by rf sputtering. Field effect transistors using $SrTiO_3$-SiO_2 gate insulation were fabricated and evaluated.

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SPUTTERED THIN FILM RESEARCH

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SPUTTERED THIN FILM RESEARCH

SUMMARY

The United Aircraft Research Laboratories under ONR Contract N00014-72-C-0415, is conducting a research program to establish the feasibility of reactive rf sputtering as a viable technology for the synthesis and deposition of (1) high quality single crystalline thin films of selected III-V compound semiconductors suitable for integrated optics, and microwave devices and of (2) high quality, high dielectric constant thin films for microelectronics, microwave and integrated optics applications. The secondary objective of the proposed research program is to perform the necessary integrated optics, microwave, and microelectronic device design, fabrication and evaluation to ascertain the device potential of the films produced.

The effort under this contact during the first six month reporting period is summarized below.

Reactive sputtering of aluminum nitride films initiated the III-V semiconductor work. This material was chosen for its high acoustic velocity and excellent piezoelectric properties which make it extremely attractive for fabrication of acousto-optic modulators and acoustooptic filters for integrated optics applications. The relative merits of ammonia and nitrogen as the reactive gas were compared. It was determined that ammonia produced films of superior quality. Even at deposition temperatures as low as 50°C the ammonia sputtered films were optically clear and exhibited an absorption edge near 5.9 eV, similar to that reported for bulk single crystals of aluminum nitride. Sputtering in nitrogen at substrate temperatures as high as 700°C resulted in amber to brown colored films which indicates an off stoichiometric composition attributed to a nitrogen deficiency. To date epitaxy has not been achieved at substrate temperatures up to 700°C but highly oriented films with $(11\bar{2}0)$ planes parallel to the film surfaces have been prepared. A pronounced difference in ordering is found between films sputtered in ammonia and nitrogen. Nitrogen sputtered films tend to orient with $(00.\ell)$ and $(h0.\ell)$ planes parallel to the film surface. At a deposition temperature of 700°C the films reactively sputtered in ammonia show the highest degree of ordering with predominantly $(11\bar{2}0)$ planes parallel to the film surface. The results obtained to date indicate that substrate temperatures in excess of 700°C are required to achieve epitaxy and the substrate heater assembly is being modified to achieve temperatures up to 1200°C.

The system designed for reactive sputtering of gallium arsenide in an arsenic ambient has been completed and runs will commence in the next quarter. These efforts

if successful could lead to a technique for the fabrication of thin uniform epitaxial layers of gallium arsenide which are required for the fabrication of microwave field effect transistors.

High dielectric constant thin film work started with the sputtering of strontium titanate. This work was primarily centered on films deposited on silicon. This combination is particularly interesting for the fabrication of high transconductance, small geometry, low threshold voltage field effect transistors and nonvolatile semiconductor memory elements with low voltage switching of memory states.

MIS (Metal-Insulator-Semiconductor) capacitors with a composite dual insulator consisting of 1000Å $SrTiO_3$-20Å SiO_2 were fabricated on 10 Ω-cm n-type silicon. The charge storage characteristics of this structure were determined as a function of bias voltage applied across the capacitor. The high dielectric constant strontium titanate (K=80) films in combination with the thin silicon dioxide (K=3.9) films permit high fields to be developed across the SiO_2 layer at relatively low applied voltages. For this structure, at threshold, 6V was found sufficient to tunnel charge across the silicon dioxide into traps at the SiO_2-$SrTiO_3$ interface. Capacitance-voltage measurements showed that a total flat-band shift of 10V could be obtained for a slowly varying bias ranging between ± 18V.

For 200 nsec, 15V pulses, a flat-band voltage shift of 1.5V was achieved and a 20V 1 μsec pulse produced a 4V shift. Switching characteristics for positive and negative pulses of short duration were asymmetric in voltage and time. Useful charge retention times of the order of a day were observed. With further development, these devices have potential for application as a nonvolatile semiconductor memory element with much lower voltage requirements for switching memory states than current state of the art MNOS (Metal-Silicon Nitride-Oxide Semiconductor) transistors.

High transconductance, low threshold voltage transistors were fabricated with the above gate structure. The threshold voltage was -1.1V and the transconductance was thirteen times greater than for a silicon dioxide gate transistor with the same device geometry and operating voltages.

1.0 INTRODUCTION

Numerous applications exist for semiconductors and dielectrics in thin film form which essentially exhibit the same electrical and optical properties as they do in bulk single crystal form. In many cases these applications require the fabrication of structures which not only combine materials having appreciable differences in thermal coefficients of expansion, but also incompatible high temperature properties. In order to overcome these problems, a low temperature deposition process is mandatory. This in itself will not prove to be adequate unless the process will yield films with good structure. In fact, many applications require use of single crystal films. The objective of this program is to establish the feasibility of reactive rf sputtering for synthesis and deposition of selected high quality semiconductor and high permittivity insulating films suitable for many optical and electronic applications. The secondary objective of the program is to fabricate devices to assess the potential of the grown material in selected device applications.

Rf reactive sputtering was chosen as the mode of deposition for several reasons. Rf discharges can be maintained at much lower pressure than a DC plasma, therefore, the high energy of the sputtered species will not be degraded by multiple collisions as would be the case for the high pressure ambient in a DC system. This particularly important since there is evidence that the high energy of the arriving sputtered atoms can be accommodated by the substrate surface (Ref. 1), and this will facilitate the growth of epitaxialy films at low temperature. It also has been suggested that the high energy of sputtered atoms plays a significant role in the lowering of the epitaxial temperature through enhanced substrate cleaning (Ref. 2). Although low pressure DC discharges may be supported thermionically by hot filaments, the life of the filaments will be severely impaired by the presence of the reactive gas, and the filament would be a source for system contamination. The combination of rf sputtering with ultrahigh vacuum techniques yields a system suitable for the preparation of high purity films.

The semiconductor materials work will concentrate on the epitaxial deposition of AlN, GaN, AlAs and GaAs. Preparation of the nitrides will compare the relative merits of nitrogen and ammonia as the reactive ambient. The relative merits of arsenic and arsine will be studied in preparation of the arsenides. Deposition of high dielectric constant materials, such as strontium titanate, lead titanate, and rutile will be considered in insulating film portion of the program.

The progress made during the course of the first six months of the program is presented below. Data on structure and properties of aluminum nitride films reactively sputtered in nitrogen and ammonia is reported. The status of a system constructed for the reactive sputtering of the arsenides is presented. Charge storage characteristics of MIS capacitors with composite $SrTiO_3$-SiO_2 insulators were studied. High transconductance field effect transistors employing a strontium titanate gate were fabricated and tested.

2.0 SPUTTERING TECHNIQUES AND EQUIPMENT

2.1 Introduction

Sputtering is the technique of bombardment of a solid or liquid target with positive ions of sufficient energy to cause emission of atomic or molecular species from the target surface. Ion beams and glow discharges at pressures from 100 millitorr down to a fraction of a millitorr are common sources of bombarding species. As a technologically useful tool, the ion beam sputtering rate is far too low and poses some experimental difficulties in collection of uniform layers on the substrate. The glow discharge in argon is the most common tool for sputtering.

A metal electrode negative with respect to ground will develop a sheath in a glow discharge. The most distinctive features observed are the dark space at the cathode and a glow region extending from the edge of the dark space to the anode if the latter is spaced some 2 to 5 centimeters away from the cathode, as is commonly the case. Most of the applied cathode voltage is dropped across the dark space. Such an arrangement of cathode and anode will lead to a self-sustaining glow discharge in the 100 millitorr range or less because of the emission of secondary electrons from the cathode surface. These secondary electrons acquire enough energy from the field across the dark space to ionize gaseous species with which they collide, yielding generally a univalent positive ion and an electron.

The sputtering mechanism is generally accepted as a process of momentum transfer from the bombarding ion to atomic or molecular species in the target. Higher mass ions have been found to be much more efficient for sputtering. Many are not readily available at reasonable cost. Hence, argon is the best compromise choice.

Rf sputtering is a technique using high-frequency alternating voltages applied to the target electrode of an otherwise conventional sputtering system. The glow discharge initiated in the sputtering chamber constitutes the load of a radio-frequency generator capable of supplying a few hundred to a few thousand watts output power. The generator and the load must be matched for optimum performance of the generator. A simple L-network containing inductance and capacitance is generally adequate. The rf power may be supplied at frequencies from about 100 kilohertz up to about 100 megahertz. Good sputtering rates are obtained at 13.56 MHz.

Insulators, metals, and semiconductors may be rf sputtered in contrast to the metals and semiconductors only for dc sputtering. In the dc case, the metal or semiconductor permits continued charge flow through the electrical path-electrons flowing through the metal or semiconductor target to neutralize the impinging positive ions. Obviously, no charge crosses the insulator so that only a brief ion bombardment of the surface can occur before charge flow ceases.

When a radio-frequency voltage is applied across the insulator, charge and discharge occur with the frequency of the applied voltage and positive ion bombardment occurs during alternate half cycles. A net negative dc bias is observed on the insulator because electrons in the glow discharge are many times more mobile than positive ions and tend to build up a negative potential so that no net current flows to the insulator surface.

Rf discharges are sustained at lower pressures than dc discharges. The secondary electrons emitted from insulators during rf sputtering tend to have longer range than for the higher pressure dc case. These longer range electrons have acquired the average dc-bias voltage and bombard the substrate, heating it oftentimes to much higher temperatures than are desired unless heat sinking is properly used or electron deflection schemes applied.

Reactive sputtering is the name given to the process when the sputtering ambient has an added constituent reactive toward the target species. The reactive species will be raised to an excited state in the glow discharge and will combine with atoms of the target material to form a compound in thin film form on the substrate. Three mechanisms may be postulated for this process: (1) The reaction between excited species and target atom takes place on the target surface and is sputtered by subsequent ion bombardment; (2) the reaction is caused by a collision between the emitted target species and some form of the reactant species in the gas phase; or (3) the excited reactant species is adsorbed on the substrate surface and combines with the arriving target species to form a compound. The first and third mechanisms seem most likely but rarely occur singly. Indeed, mechanism (1) often is a complicating factor in attempts to dc sputter metals such as aluminum in an oxygen contaminated ambient. The reaction at the target forms aluminum oxide faster than it can be removed by sputtering and the process eventually stops because of the insulating character of the aluminum oxide layer on the target.

Reactive sputtering has two main advantages. Refractory compounds may be synthesized in thin film form at relatively low substrate temperatures compared to chemical vapor deposition. Because of the difficulty in purification of highly refractory materials, reactive sputtering often leads to drastic reductions in impurity concentrations since many elements can be much more readily purified. The low temperature synthesis minimizes stress resulting from depositing films on substrates having a thermal coefficient of expansion different from the film material. This particular feature of reactive sputtering permits consideration of a wider range of single crystal substrate materials for epitaxial growth.

A noncondensable gas such as nitrogen or oxygen may be the reagent in a reactive sputtering process. No special precautions are required beyond those normally practiced in conventional sputtering. High purity gases and elevated temperature baking of the sputtering chamber are required. Construction materials for the chambers are chosen for ease of cleaning and for good out-gassing characteristics.

If one desires to reactively sputter a material such as gallium arsenide both constituents of which have very low vapor pressure at room temperature, one means for introducing one of the constituents is as a chemically combined volatile gas. Arsine (AsH_3) might be considered as a possible form for introducing arsenic into the system. Arsenic vapor may also be introduced simply by heating solid arsenic in the chamber to raise its vapor pressure to the necessary level--from 1 to 100 mtorr. The latter approach was adopted for this program.

Section 2.2 describes the equipment for both types of reactant gases used in the reactive sputtering portions of this program.

2.2 Sputtering Chamber Design

Two sputtering systems are being used in this program. Both chambers were designed for reactive sputtering. In the first chamber sputtering is performed with materials which are in the gaseous state at room temperature. This first chamber is referred to as the reactive sputtering (RS) system. In the second system, the materials used to sputter must be at an elevated temperature to maintain a high enough pressure to maintain a glow discharge. This second system is for deposition of the arsenide films and is referred to as the high temperature reactive sputtering (HTRS) system. Basic design considerations are the same in both systems.

Both film adhesion and epitaxial growth are profoundly affected by contaminants adsorbed or chemically bound to the surface of the substrate. The most likley adsorbed contaminants for the usual sputtering process are water vapor, oxygen and hydrocarbons. All are present in the air to which substrates are exposed during preparation and the last adsorbed layers must be removed in the sputtering chamber by high temperature bakeout or by sputter cleaning. The sputtering chamber itself must be designed to minimize or eliminate admission of these contaminants just prior to or during the sputtering process.

Conventional oil diffusion pumped systems suffer from the continual admission of hydrocarbons from the diffusion pump, exquisitely designed as the baffle between chamber and diffusion pump may be. Once it is pumped to the desired pressure a chamber may be sealed and a closed process used for sputtering. This has the disadvantage of permitting contaminants desorbed from the chamber walls by the glow discharge to have ample time for diffusion to the substrate. A continuously pumped sputtering chamber is, thus, desirable. The chambers are therefore evacuated by a Welsh 3103 turbomolecular pump which is capable of a pumping speed of 250 L/sec in the millitorr range. Thus "backstreaming" hydrocarbons are completely eliminated and a high rate flushing action can be maintained. Chambers are constructed of stainless steel and all feedthroughs are sealed with crushed copper gaskets so that the systems are bakeable to 300°C without degradation of seals or contamination by them. Sputtering pressure is measured by Varian Millitorr ion gauges. Substrate temperature is controlled by heaters which are welded into stainless steel mounting blocks (Figs. 3 and 4).

2.2.1 Reactive Sputtering System

This system incorporates several features not incoprorated in the HTRS chamber. The substrate mounting block is isolated from ground to permit both bias sputtering of the substrate and sputter cleaning of the substrate. Two electromagnets are welded into stainless steel cases. These magnets enhance as well as confine the plasma between the target and substrate. Adjustment of the field strength and direction alters the substrate heating and the uniformity of the deposition. A shutter can be rotated between the target and the substrate allowing sputter cleaning of the target prior to deposition on the substrate. While these features are helpful and sometimes necessary, they have not been included in the HTRS system until the practicality of the basic concept has been assessed.

2.2.2 High Temperature Reactive Sputtering System

To maintain a constant arsenic pressure, a controller was designed which has an output proportional to the difference between the ion gauge voltage and a preset voltage. This output regulates an S.C.R. circuit which supplies current to a pair of crucibles in the chamber. Aluminum oxide coated tungsten wire crucibles are used to prevent the arsenic from reacting with the hot wire (Fig. 7). If the chamber walls were at room temperature, the arsenic would condense. The system, therefore, is heated and surrounded by an insulating shroud. Since arsenic condensation would take place in the turbine pump, a liquid nitrogen trap is placed between the chamber and the pump. It is this baffle which actually pumps the arsenic. A flap type valve is located inside the heated shroud just before the baffle to provide control of the arsenic consumption. The gallium target is liquid at the 250°C to 300°C chamber temperature and must be held in a saucer shaped electrode (Fig. 3). Because of its low reactivity with gallium, molybdenum was chosen as the material from which the electrode was fabricated. A grounded ring was placed over the electrode edge to shield it from sputtering. Only the gallium is then permitted to be exposed to the plasma. The copper gaskets react with the arsenic at 250°C so they are nickel plated.

2.2.3 HTRS System Evaluation

The system has been assembled and has undergone tests to determine if it will function as desired.

The temperature of the various parts of the chamber were measured to determine if any "cold" parts existed. Several flanges were found below 250°C so one of these flanges were used as the new control point. The amount of insulation was increased on the inner shroud and reduced the temperature variation to 50°C, when the system is cycling about its set point.

Arsenic was placed in the crucibles and the control circuit was able to maintain the arsenic pressure to within 2% of the desired value between one and ten millitorr. The arsenic was found to diffuse through the nickel plate on the copper seals

and corrode them. Another material will have to be found to protect these gaskets; platinum would seem a likely candidate. The ion gauge grids were also corroding due to the high temperature and proximity of the filament. An attempt to lengthen the life of these grids by operating at a reduced emission current is being made. The thoria coated filament does not seem to be affected by the arsenic. More testing of the ion gauge in an arsenic ambient will be required before it is determined whether they are practical for this application.

3.0 REACTIVELY SPUTTERED ALUMINUM NITRIDE

Aluminum nitride is one of the more refractory materials of the III-V semi conductor group. It has a decomposition temperature in excess of 2400°C. The band gap of AlN is 5.9 eV (Ref. 3) and it crystallizes in the hexagonal wurtzite structure (Ref. 4) with unit cell dimensions of a_o = 3.111Å and c_o = 4.980Å. In addition to its insulating properties it holds considerable interest because of its excellent piezoelectric properties. It has the highest known acoustic velocity of 10.4×10^5 cm/sec (Ref. 5). This makes feasible, using conventional photolithographic techniques, the fabrication of surface acoustic wave devices operating at microwave frequencies. It is a particularly interesting material for integrated optics applications. Devices such as acoustooptic modulators and acoustooptic filters can be fabricated. For these applications single crystal films are required if scattering losses are to be kept to a minimum.

The objective of this study is to explore the feasibility of reactive rf sputtering for the preparation of epitaxial films of aluminum nitride on various single crystal substrates suitable for integrated optics applications. The initial efforts of this program are described below. Structural, optical, and electrical data are presented for films prepared using nitrogen and ammonia as the reactive gas ambient.

3.1 Experimental Procedures

3.1.1 Film Deposition

Films of aluminum nitride were synthesized by reactive rf sputtering in either nitrogen or ammonia ambients. The sputtering system, described in detail in the preceding section is capable of an ultimate background pressure of 1×10^{-8} torr. All necessary precautions were taken to insure the deposition of high purity films. The reactive gases had an assayed purity of 99.999% or better. The target was 99.999% pure aluminum. Films were deposited on single crystal substrates of (0001) ZnO, (0001) Al_2O_3, $(10\bar{1}2)$ Al_2O_3, (0001) SiC and (100) silicon. Fused silica and 7059 Corning glass substrates were also used. The preparation of the substrates is described in Appendix I. Sputtering pressure ranged from 5×10^{-3} torr to 10^{-2} torr for films prepared with nitrogen gas and the ammonia pressures studied covered the range from 5×10^{-3} torr to 7×10^{-2} torr. Substrate temperatures were varied between 50°C and 700°C. A typical sputtering run was as follows:

(1) The sputtering system was evacuated to 10^{-6} torr or less. Substrates were heated to 700°C during evacuation and then cooled to the deposition temperature required.

(2) The reactive gas was introduced to the desired pressure and the rf discharge started while the substrates were protected with a shutter during sputter

cleaning of the target. The target was sputter cleaned at a power density of 4.4 watts/cm^2 for one-half hour. This removes approximately 0.5μ of material from the target before film deposition is started.

(3) With the shutter removed the sputtering of the films was started. Rf power density was varied between 0.16 watts to 4.4 watts/cm^2. This corresponded to a range of AlN deposition rates between 1-60 Å/min. Films deposited ranged between 1000Å and 18μ in thickness.

3.1.2 Film Thickness

Film thickness in excess of one micrometer was measured with the Taylor-Hobson Talysurf profilometer. Film thickness less than a micron was determined by means of a Gaertner ellipsometer on samples grown on silicon substrates.

3.1.3 Optical Measurements

Optical transmission measurements were made at room temperature using a Carey Dual-Beam Spectrophotometer covering wavelengths 0.2 to 2.5μ. Infrared reflectance spectra covering wavelengths of 2.5μ to 50μ was obtained using a Perkin Elmer Model 621 Dual Beam Spectrophotometer. Index of refraction data at 5461Å was obtained on thin films with the Gaertner ellipsometer. Refractive index data at other wavelengths was obtained from the wavelength position of the constructive and destructive interference peaks occurring in the transmission and reflectance curves and the thickness which had been determined by Talysurf measurement.

3.1.4 Electrical Evaluation

The dielectric constant and the resistivity were determined for films deposited on silicon. Aluminum or gold dots, 250μ in diamter, were evaporated over the dielectric through a mask. Ohmic contact was made to the back side of the silicon wafer. Capacitance measurements were made at 1 MHz using a Boonton 71A capacitance meter. A Keithly 602 electrometer was used to measure currents through the aluminum nitride films. All measurements were made at room temperature.

3.1.5 Structure Determination

On removal from the vacuum system the structure of the films was first examined using a Phillips X-ray diffractometer. Subsequent measurements were made in a Read Thin Film camera using Cu-Kα radiation. This camera is a Debeye Scherrer type. A fixed beam-to-film plane angle of 29.5° was used in analyzing the films. Variations in orientation and texturing in polycrystalline samples are readily detected by this technique.

3.2 Experimental Results and Discussion

3.2.1 Film Structure

The crystal structures observed for aluminum nitride films reactively sputtered in nitrogen or ammonia over a range of substrate temperatures of 200°-700°C are shown in Figs. 9-13. All films possessed the hexagonal wurtzite structure of bulk aluminum nitride. A marked difference in structure occurs between films sputtered in nitrogen and ammonia. Nitrogen deposited films tend to grow with the c axis normal to the plane of the film whereas films grown in ammonia tend to grow with the c axis in the plane of the film. The degree of ordering increases with substrate temperature. To our knowledge this is the first ordering effect observed due to reactant gas. Foster (Ref. 6) has observed that hydrocarbon contamination can affect the orientation of sputtered ZnO films. Sputtered films of ZnO normally grow with the c axis perpendicular to the film plane while on hydrocarbon contaminated substrates the films tend to grow the the c axis in the film plane.

Noreika (Ref. 7) deposited AlN films by dc reactive sputtering in nitrogen at a substrate temperature of 900°C and failed to achieve epitaxy but obtained films with a highly preferred fiber texture with (0001) planes parallel to the substrate surface. The maximum temperature of our nitrogen gas runs was 700°C and the degree of ordering achieved was not as great but tends to agree with Noreika's results. At 700°C the degree of ordering achieved in the ammonia runs was high with $(11\bar{2}0)$ planes parallel to the substrate surface. The ordering was found to be most pronounced with $(10\bar{1}2)$ Al_2O_3 substrates sputtered at 700°C in a 7×10^{-2} torr ammonia ambient (see Figs. 12 and 13d).

The orientation dependence on the reaction with the gas in which the AlN films are sputtered may be related to the relative reactivities on NH_3 and N_2. A far greater percentage of reactive N^{+++} ions will be formed in the NH_3 discharge than in N_2. This raises the possibility of reaction at the target where the resulting sputtered species is in the form of AlN. Further work remains to be done on achieving a better understanding of films sputtered in an ammonia ambient.

The film deposition rates, a function of power level and pressure, generally ranged between 30-60 Å/min. Several runs were made to determine if deposition rates had a marked influence on nucleation and, hence, epitaxy. In these instances film deposition was initiated at a rate of 1 Å/min for the first 150Å of the deposit and then raised to the higher rate for the remainder of the run. No apparent influence on film orientation nor degree of ordering could be determined with the lower deposition rates.

Higher substrate temperatures will be required for epitaxy. The present substrate heater is being redesigned to reach the higher temperatures required.

3.2.2 Optical Characteristics

Films sputtered in nitrogen were amber to brown in color and showed an absorption edge shifted to lower frequencies. Similar results were reported by Noreika (Ref. 7) for films sputtered at 900°C in an argon-nitrogen mixture (85×10^{-3} torr Ar, N_2 partial pressure 5×10^{-3} torr). The band edge shift was attributed to a probable nitrogen deficiency and a built in surplus of argon due to the relatively high-pressure argon ambient. An anneal of these films in N_2 at 900°C for 2 hours produced a band edge shift to values reported for bulk single crystals (5.9 eV). Our samples sputtered at 1×10^{-2} torr N_2 and a substrate temperature of 700°C and annealed for a comparable period did not yield as dramatic a shift of the band edge to shorter wavelengths. This is probably indicative of the reduced reactivity of the nitrogen at the lower substrate temperature. Films sputtered in ammonia even at a substrate temperature as low as 50°C were colorless and exhibited the band edge absorption of stoichiometric materials. This clearly points up the superiority of ammonia for the synthesis of stoichiometric AlN films.

The index of refraction of the films were found to vary from 2.1 at 3000Å to 1.91 at 5461Å. Good agreement was found between index values determined ellipsometrically for thin samples and those determined using a Talysurf measurement and interference peak positions for thick samples.

Infrared reflectance of the AlN films exhibited the reststrahlen band similar to bulk single crystals (Ref. 8). The AlN reststrahlen peak falls between 10.5 and 15μ. Little difference was observed in the shape of the reststrahlen band for samples deposited at 200°C or 700°C but samples sputtered in ammonia peaked more sharply at 15μ than those sputtered in nitrogen. This is illustrated in Fig. 14. It is not clear whether this may be associated with the difference in stoichiometry of N_2 and NH_3 deposited films or if it might be due to size or shape effects of the polycrystalline samples. Pasternak and Hejda (Ref. 9) have shown the influence of surface modes on the shape of the absorption (reflectance) spectrum in the long wavelength region. One other possibility exists and this is associated with the orientation of the crystallites. As the angle between the propagation vector and and the c axis of a uniaxial crystal is decreased from 90°, the width of the reststrahlen band is known to decrease markedly for the extraordinary ray, the long wavelength side of the band moving to shorter wavelengths (Ref. 8). Since the c axis tends to be aligned perpendicular to the plane of the films sputtered in nitrogen and parallel to the film plane in films sputtered in NH_3 this may account for difference in shape of the reststrahlen band.

3.2.3 Electrical Evaluation

Resistivity measurements were made on AlN films deposited on Si. Attempts to measure the current levels in these highly resistive films proved difficult. The resistivity was estimated to be greater than 10^{12} Ω-cm. The dielectric constant at room temperature and 1 MHz was determined to be 8.7.

3.3 Conclusions

(1) Aluminum nitride films reactively sputtered in ammonia result in the deposition of clear stoichiometric films with optical and physical properties of bulk single crystal AlN, whereas, films sputtered in nitrogen under similar conditions result in an amber colored nitrogen deficient film. This absorption tail in the visible makes the nitrogen deposited films less attractive for optical waveguide applications.

(2) Aluminum nitride films deposited by reactive sputtering in ammonia tend to grow with $(11\bar{2}0)$ and $(10\bar{1}0)$ planes parallel to the films surface whereas films reactively sputtered in nitrogen tend to grow with (0001), $(10\bar{1}1)$, $(10\bar{1}2)$ and $(10\bar{1}3)$ parallel to the film surface. At a substrate temperature of 700°C the degree of ordering of ammonia films is very high with primarily $(11\bar{2}0)$ planes parallel to the film surface.

(3) Substrate temperatures in excess of 700°C are required if epitaxy of AlN films is to be achieved.

4.0 HIGH DIELECTRIC CONSTANT FILMS

4.1 Introduction

The initial phase of this portion of the program focused primarily on the deposition of strontium titanate films. At room temperature $SrTiO_3$ crystallizes in the simple cubic perovskite structure and exhibits a dielectric constant of about 300 (Ref. 10). Pennebaker has reported on the properties of sputtered $SrTiO_3$ films on metal substrates (Ref. 11). A particularly interesting combination for study is $SrTiO_3$ deposited on silicon. This configuration holds potential for the fabrication of high transconductance insulated gate field effect transistors and charge storage memory transistors.

The charge storage memory is a variable threshold field effect transistor with the gate insulator consisting of a dual dielectric layer. When a bias of sufficient magnitude is applied across the dual insulator structure to cause charge transport, charges are trapped at sites in the vicinity of the interface of the two insulators. The presence or absence of charge at these traps close to the surface of the semiconductor has a direct influence on the surface potential of the semiconductor, and hence the threshold voltage of the transistor. The relative thickness of the two insulators determines to a large extent the mechanisms for current transport, and the write and erase speed of the device. Strontium titanate in combination with SiO_2 will permit high fields to be developed across the SiO_2 layer at a considerably lower voltage than for comparable layer structures employing Si_3N_4-SiO_2 or Al_2O_3-SiO_2 and hence lead to considerably lower threshold voltages for switching memory states. The charge storage memory is treated in more detail in Appendix II. MIS (Metal-Insulator-Semiconductor) capacitors with dual insulator gate structures comprised of 1000Å $SrTiO_3$-20Å SiO_2 were fabricated and studied with regard to charge storage characteristics. Insulated gate field effect transistors with the above gate structure were fabricated and evaluated.

4.2 Preparation of MIS Capacitors and Transistors

MIS capacitors were fabricated on 7-10 ohm-cm (100) n-type silicon wafers. The silicon substrates were degreased, stripped of oxide, rinsed in deionized water and spun dry. They were then placed in the vacuum chamber which was evacuated and baked out. The system was then allowed to cool to room temperature and an equilibrium pressure in the low 10^{-8} to 10^{-9} torr was reached.

Substrate temperature was then raised to 600°C and 10 microns of ultrapure argon is introduced into the system. The silicon wafers were then sputter cleaned to remove any contamination which may have occurred during the baking of the chamber or which may have been left as residue from the cleaning process. This high temperature sputter cleaning does not degrade the silicon surface as was believed by many

workers in the field. MIS transistors made by this technique have high transconductance which would not be the case if the surface mobility had been appreciably degraded by the process. The use of high temperatures during sputter cleaning tends to anneal out damage caused by ion bombardment.

One atmosphere of ultrapure oxygen was then bled into the vacuum chamber and the substrate was maintained at 600°C for one hour. This method reproducibly yields a 19 to 20Å tunnel barrier. Many samples were oxidized in this manner and measured with an ellipsometer. These measurements verified the high degree of reproducibility possible with this technique.

MIS capacitors fabricated with $SrTiO_3$ deposited directly onto the thermal oxide layer generally show only a small degree of charge trapping and the following step was introduced to enhance the flat band voltage shift due to trapping.

A small sputtering target was placed above the wafer which is held at 300°C and 120×10^{-3} torr was bled into the system after the atmosphere has been removed. A target of Ni was used to sputter 50 to 100Å of nitride to obtain a suitable trapping layer between the tunnel barrier and the high dielectric constant gate insulator. The small target was then moved out of the way and 1000Å of strontium titanate was deposited over the trapping layer. The process parameters for the strontium titanate were optimized with respect to overall device characteristics. For example, higher values of dielectric constant could be achieved with higher temperature, post deposition heat treatment. This procedure, however, caused the tunnel barrier to react with the strontium titanate thus degrading the memory effect. The parameters were varied to maximize resistivity and dielectric constant of the gate insulator within the constraints of overall device operation. The best process parameters for the strontium titanate found are the following: 20 millitorr of pure oxygen, substrate temperature of 400°C, a deposition rate of 35 Å/min, and a post deposition heat treatment of 15 min in pure O_2 at 750°C. The post deposition heat treatment eliminates trapping due to surface states. Gold is alloyed into the back of the wafer to provide an ohmic contanct. Fifteen mil gold or aluminum dots are evaporated through a mask onto the high dielectric constant layer to complete the MIS capacitor.

The transistors were fabricated in the following manner. Boron was diffused into the wafer to form the source and drain of the transistors. Contact holes were opened up, platinum deposited and alloyed to form the ohmic contacts to the source and drain diffusions. This material will not oxidize, melt, or diffuse during the subsequent high temperature processing. Platinum silicide contacts are used because conventional alloying of aluminum at the end of fabrication, in a vacuum or inert gas can reduce the strontium titanate. Following the formation of the platinum silicide contacts, the gate region was opened and the wafer was placed in the sputtering chamber. The same deposition procedure was followed as with the MIS capacitor with one exception, the trapping layer was omitted. Aluminum was deposited and the gate electrode and contact pads were delineated.

4.3 Results and Discussion

4.3.1 Charge Storage Characteristics of $SrTiO_3$ MIS Capacitors

The deposition parameters for the strontium titanate were dictated by considerations in an attempt to optimize charge retention, switching speed and total flat-band voltage shift and reproducibility of the dielectric constant. Devices fabricated with a dielectric constant of 80 generally gave the best results. The breakdown voltage of the films was > 2 x 10^6 V/cm. Figure 15 shows the current field characteristics of a $SrTiO_3$.

As mentioned earlier, structures fabricated with $SrTiO_3$ deposited directly on SiO_2 did not show an appreciable shift in flat-band voltage (~ 2V). The switching and memory retention of a charge storage device depends on the nature of the trapping sites in the vicinity of the insulator-silicon dioxide interface. Considerations, such as trap density, the spatial distribution of traps, and their distribution in energy affect device characteristics and are intimately related to the material combined with the silicon dioxide tunnel barrier. This is exemplified by the widely different switching characteristics of memory states exhibited by charge storage devices fabricated from silicon nitride-silicon dioxide (MNOS) (Ref. 12) and aluminum oxide-silicon dioxide (MAOS) (Ref. 13). In the aforementioned devices, device characteristics were optimized by variations in the deposition conditions of the insulating film.

A novel approach to the introduction of trapping centers was undertaken during the course of this study. It involved the sputtering of 50-100Å of a third material at the insulator-SiO_2 interface. The motivation to this approach was that the advantages of the high dielectric constant of $SrTiO_3$ could be retained in combination with the trapping characteristics of the material introduced. Experiments were performed where the interface layers of selected transition metal nitrides, carbides and sulfides were introduced by reactive sputtering. The choice of these materials was based primarily on the availability of pure metal targets and the ease of obtaining pure gases which allows synthesis of the compounds by reactive sputtering. A wide range of trapping characteristics were observed and results obtained indicate that sputtering of "interface states" is a viable approach to the problem.

The best results overall were obtained with 50Å of nickel nitride sputtered at the interface of 20Å SiO_2-1000Å $SrTiO_3$. The threshold for charge transfer was determined to be 6V in close agreement with the predicted value for a tunneling of charge through a 20Å SiO_2 barrier in combination with a 1000Å film with a dielectric constant of 80 (see Table I Appendix II). The hysteresis in the capacitance-voltage characteristics (Fig. 14) show the shift in flat-band voltage for a dc bias ranging between +15 and -15V. The overall flat-band voltage shift is 11V. Charge transfer characteristics are asymmetric under pulse bias. The flat-band voltage is shifted more readily by positive pulses applied to the gate. A flat band voltage shit of 1V could

be obtained for +15V, 200 nsec pulses but a 20 μsec, -20V pulse is required to restore it to its initial state. The shift in flat band voltage to more positive values for positive pulses applied to the gate electrode is indicative that charge transfer is by tunneling of electrons from the n-type silicon into the traps at the interface. Flat-band voltage shifts as a function of pulse duration and amplitude for positive pulses is illustrated in Figs. 16 and 17. The asymmetry in switching characteristics for positive and negative pulses is probably indicative of the asymmetric disposition of the trap levels with respect to the condution and valence bands of the silicon. The longer pulse duration required to clear the electrons from the traps is probably due to redistribution of charge away from the interface, which would require a longer time to clear the charge. The charge storage duration was less than a day. Devices charged to a flat band voltage of +5V decayed to near zero in about 24 hours. It is certain that device performance could be improved with regard to charge retention and switching characteristics. It must be emphasized that the results presented are based upon a limited investigation of sputtered interface states and that additional work is required to arrive at a better understanding of interface trap control.

4.3.2 Strontium Titanate Field-Effect Transistor

Insulated gate field effect transistors were fabricated using sputtered strontium titanate for the gate dielectric. The gate was a dual insulator structure comprised of 20Å of thermally grown silicon dioxide overlaid with a 1000Å of sputtered strontium titanate. To our knowledge the devices fabricated in this manner may have the highest transconductance for an insulated gate field effect transistor of equivalent geometry and operating voltage. The transistors were p-channel devices fabricated on 10 Ω-cm n-type, (100) silicon. The channel length was 6 microns and the channel width was 30 microns. A transconductance of of approximately 300 μmhos was obtained at a gate voltage of -2.0V and drain voltage of -1.5V. The effective dielectric constant of the composite gate insulator was 52, approximately 13 times greater than that of silicon dioxide. The transconductance is directly proportional to the dielectric constant. Turn on voltage for the transistors was -1.1V. Stability of the transistors under bias and temperature stress was good provided the bias voltage was kept below five volts. Gate voltages in excess of five volts resulted in some charge transfer and trapping at the SiO_2-$SrTiO_3$ interface. A shift in device threshold therefore resulted. The transfer characteristics are shown by Fig. 18. Figure 19 depicts the $SrTiO_3$ IGFET. The low voltage restriction on gate voltage may pose a problem for practical applications. Threshold voltage shifts of close to two volts may occur if the 5V bias level is exceeded.

4.4 Conclusions

(1) A dual insulator structure of 1000Å $SrTiO_3$-20Å SiO_2 has a low threshold voltage (~ 5V) for transfer of charge to traps at the $SrTiO_3$-SiO_2 interface. Charge storage of current devices are too short to be practical.

(2) The sputtering of a third material at the $SrTiO_3$-SiO_2 interface has been proven to be a practical means of affecting charge trapping of these devices. Further work is required for device optimization.

(3) High transconductance, low threshold voltage, small geometry $SrTiO_3$ can be fabricated by rf sputtering. Gate voltages must be restricted to values less than five volts to prevent threshold voltage shift due to charge trapping.

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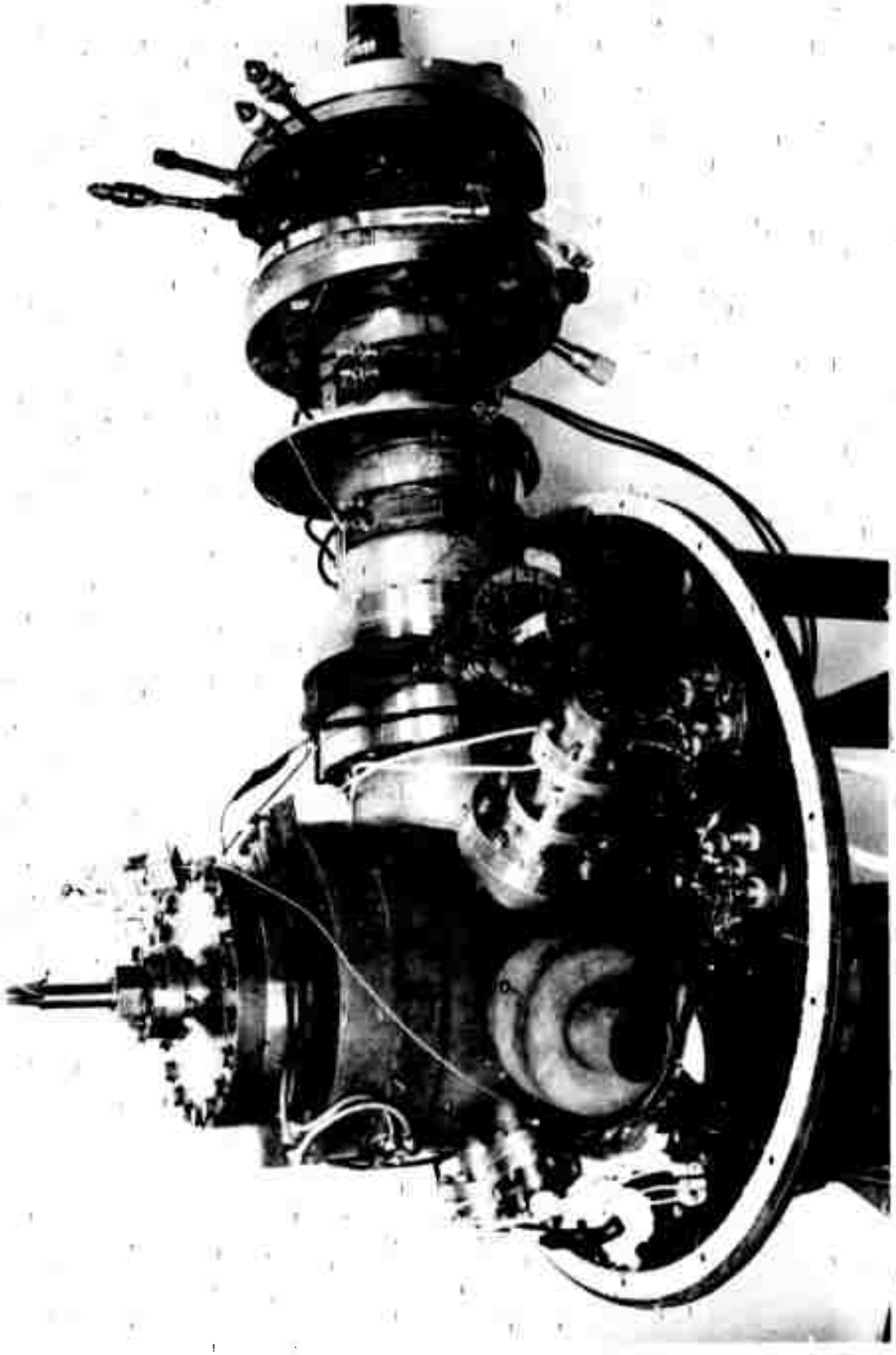
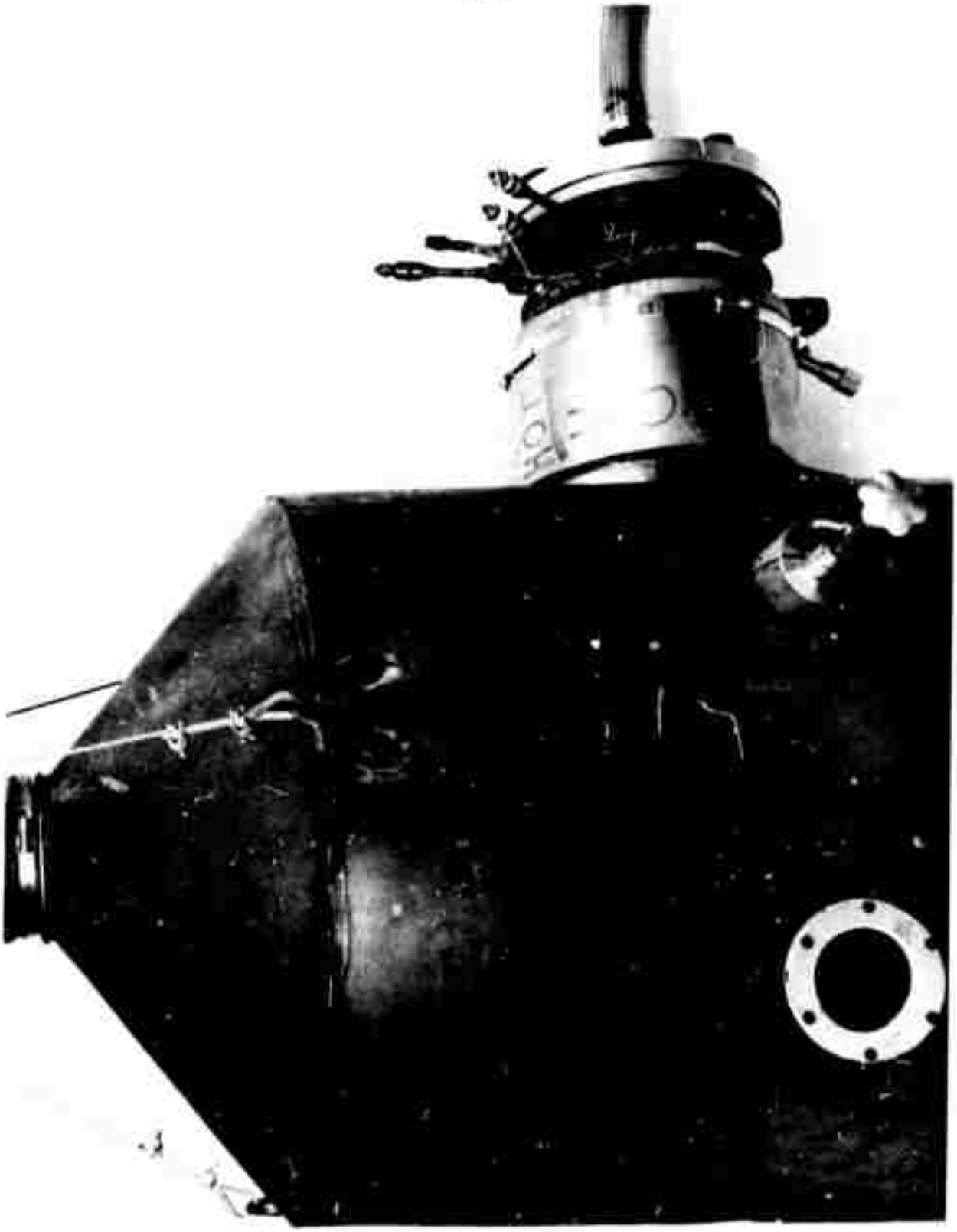
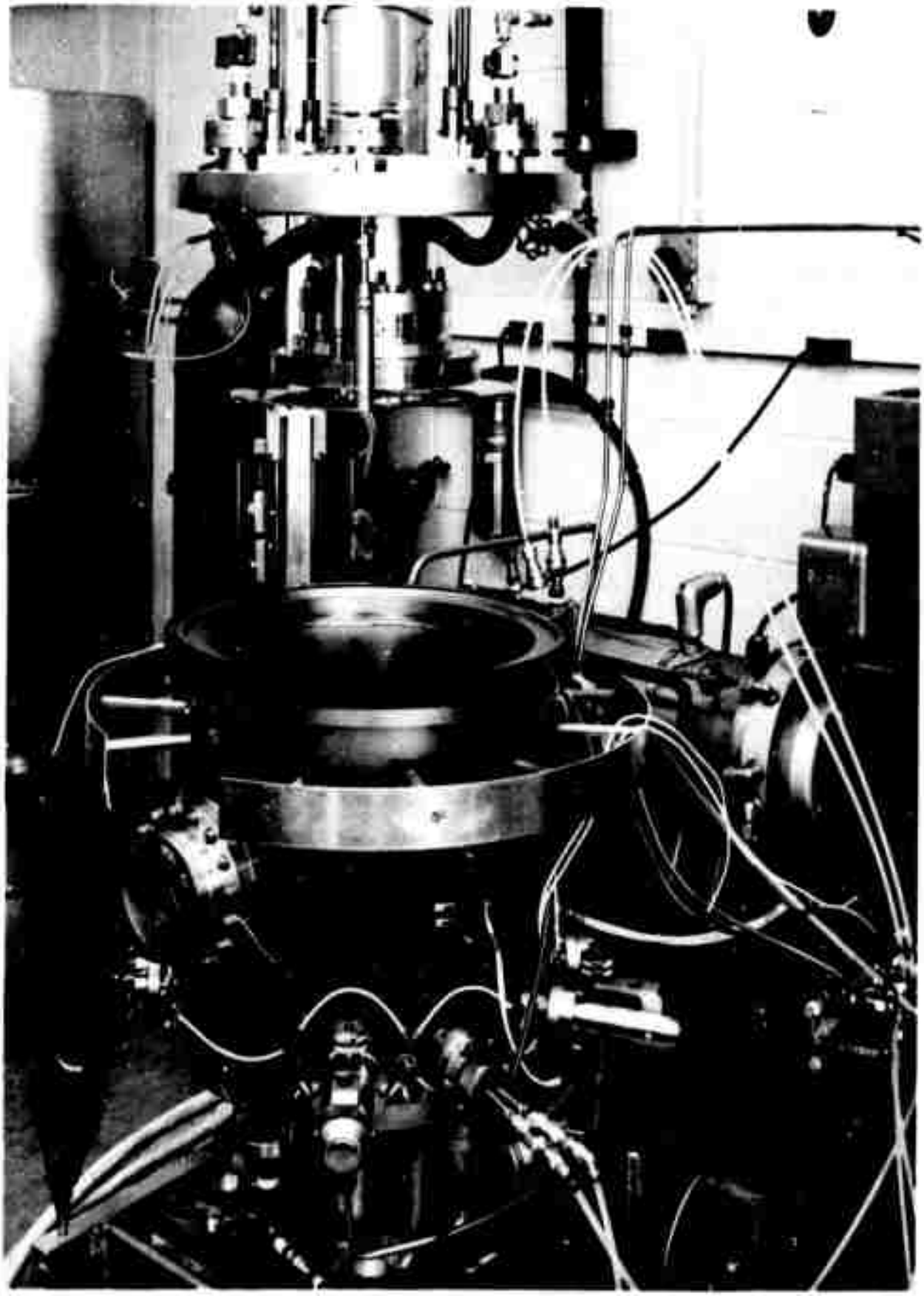


HIGH TEMPERATURE REACTIVE SPUTTERING CHAMBER (HTRS)

HTRS CHAMBER WITH HEAT SHROUD

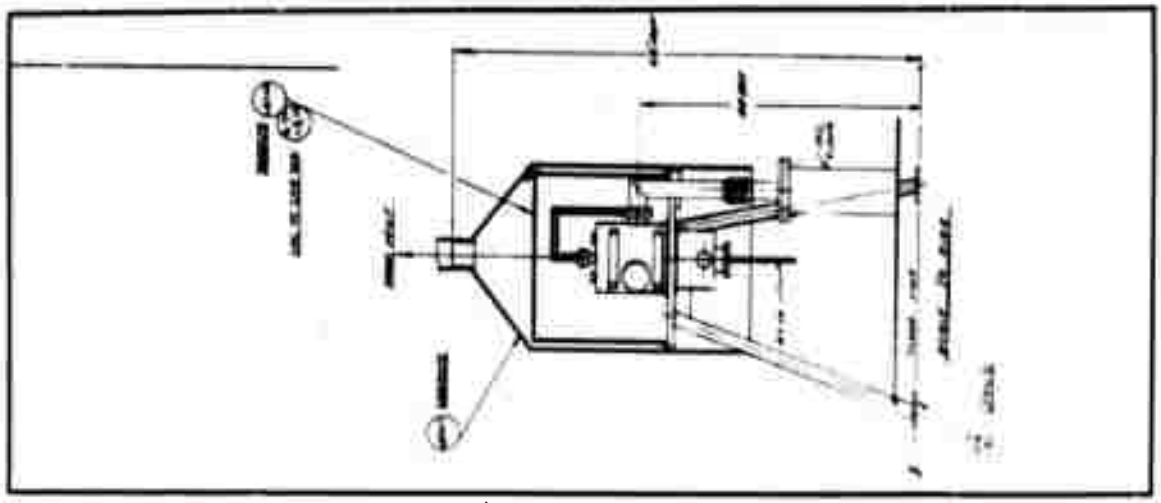


HTRS CHAMBER WITH EPITAXIAL SAFETY SHROUD

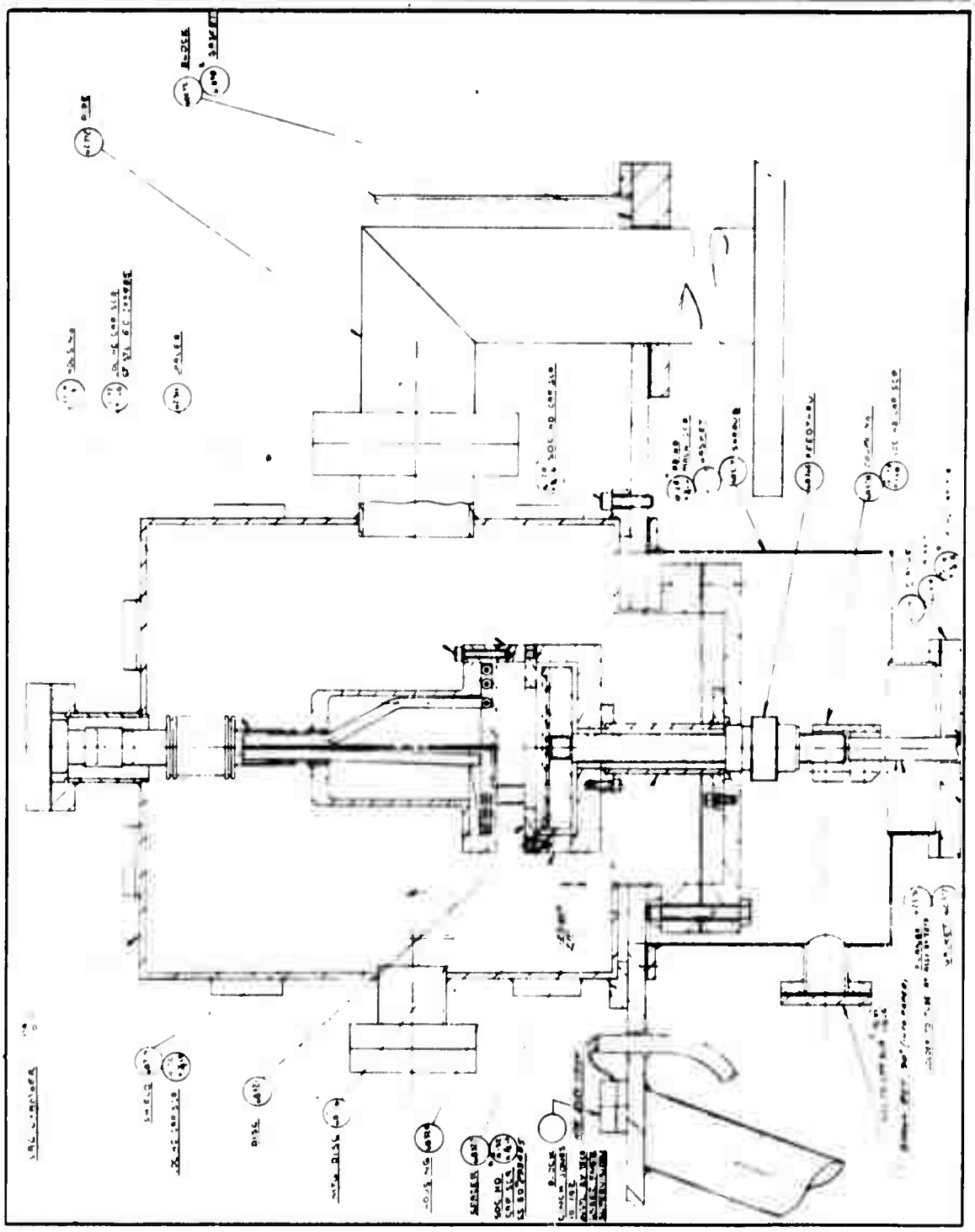


A HIGH PURITY, TURBOMOLECULAR PUMPED RF SPUTTERING SYSTEM

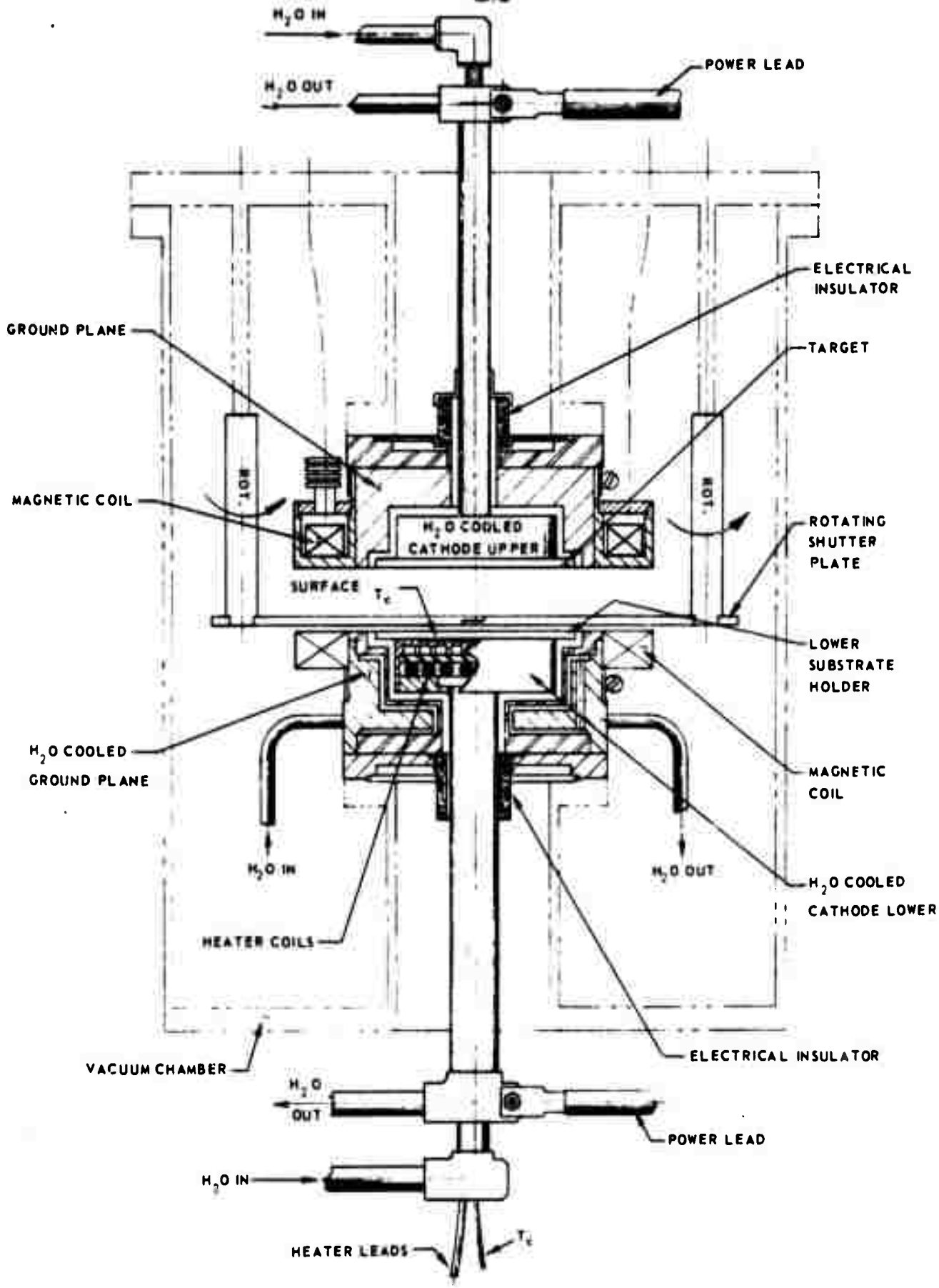
SCHEMATIC OF GaAs SPUTTERING SYSTEM

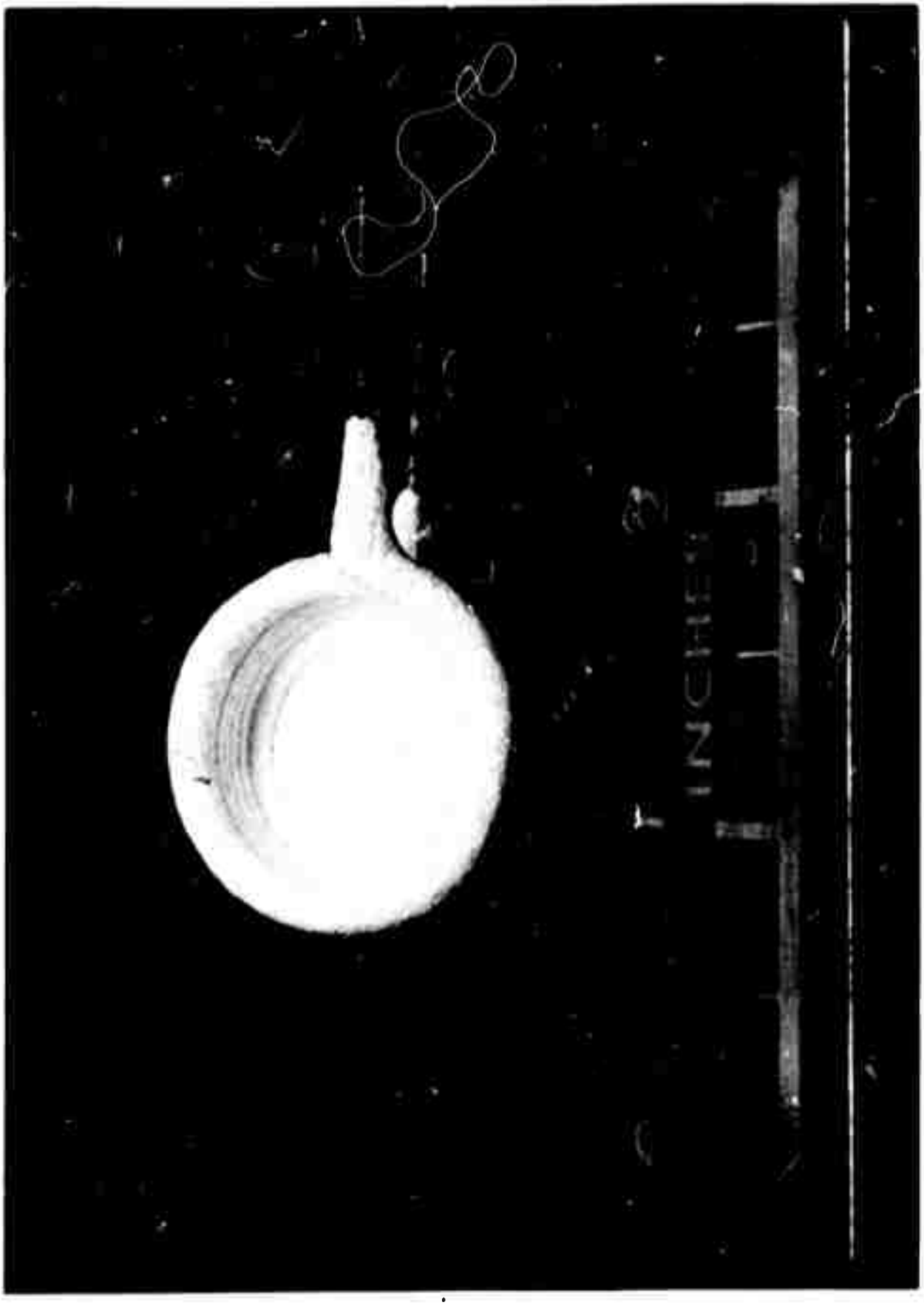


b)



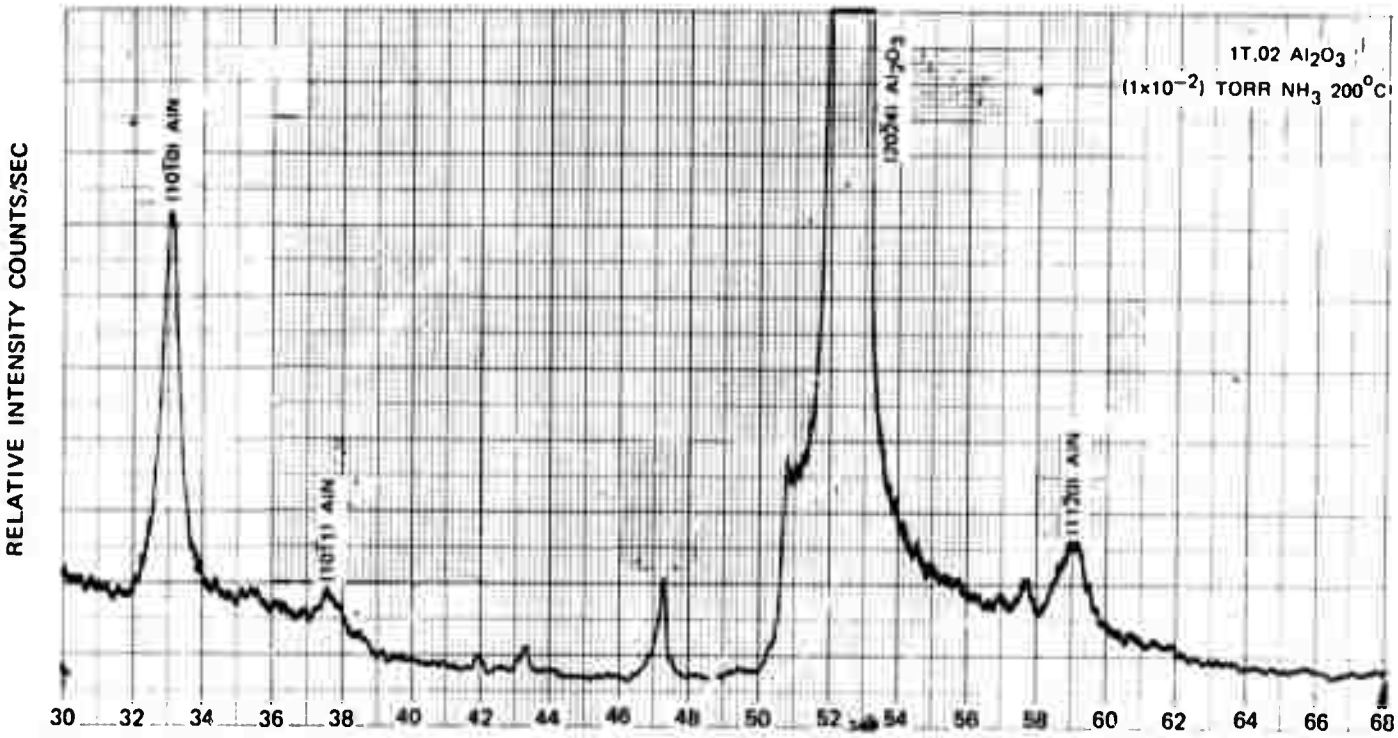
a)

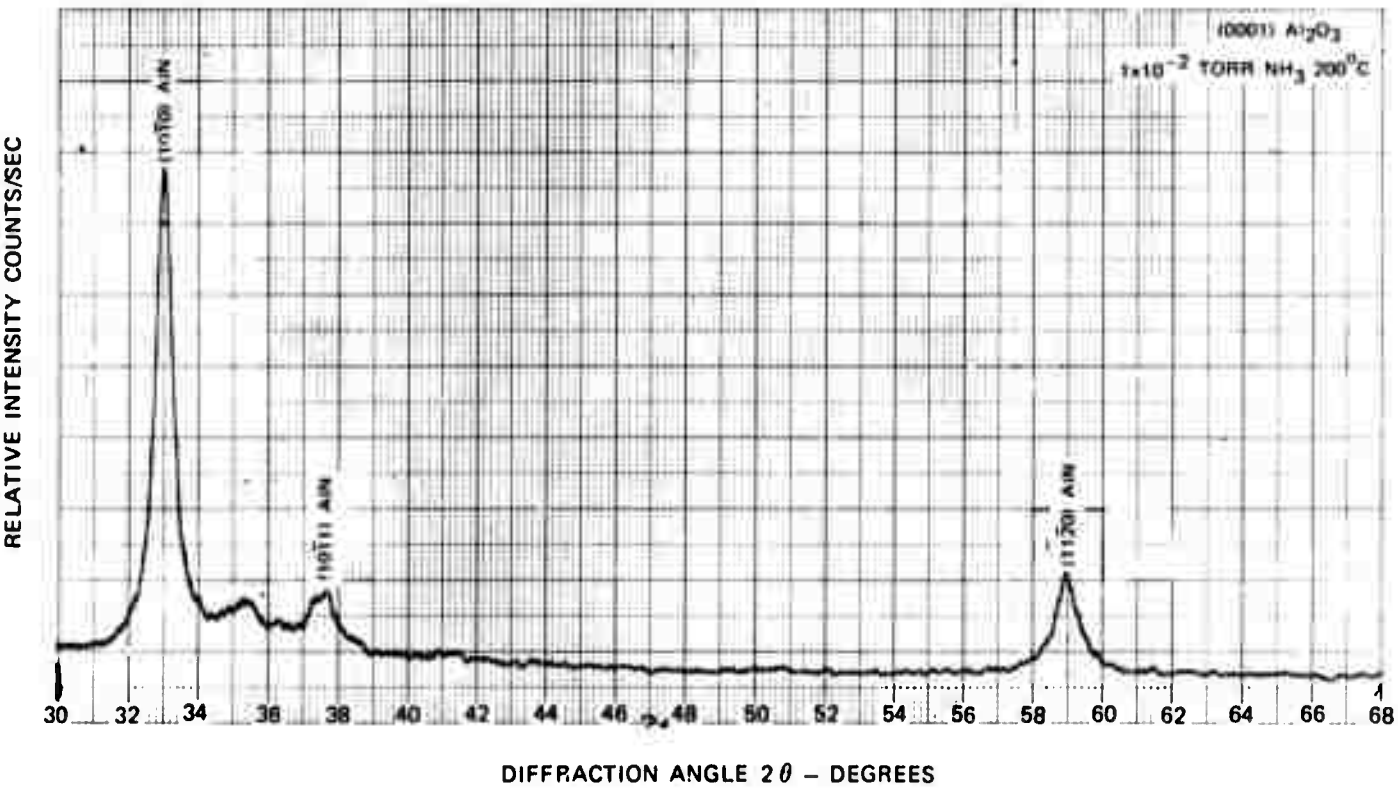

H_2O IN
H_2O OUT
POWER LEAD
ELECTRICAL INSULATOR
GROUND PLANE
TARGET
MAGNETIC COIL
HOT
HOT
H_2O COOLED CATHODE UPPER
ROTATING SHUTTER PLATE
SURFACE
T_c
LOWER SUBSTRATE HOLDER
H_2O COOLED GROUND PLANE
MAGNETIC COIL
H_2O IN
H_2O OUT
H_2O COOLED CATHODE LOWER
HEATER COILS
ELECTRICAL INSULATOR
VACUUM CHAMBER
H_2O OUT
POWER LEAD
H_2O IN
HEATER LEADS
T_c



ALUMINUM OXIDE COATED TUNGSTEN WIRE CRUCIBLE

DIFFRACTOMETER TRACES OF AlN FILMS REACTIVELY SPUTTERED IN NH_3 AT 200° C ON $(00\bar{0}1)$ AND $(10\bar{1}2)$ Al_2O_3 SUBSTRATES.

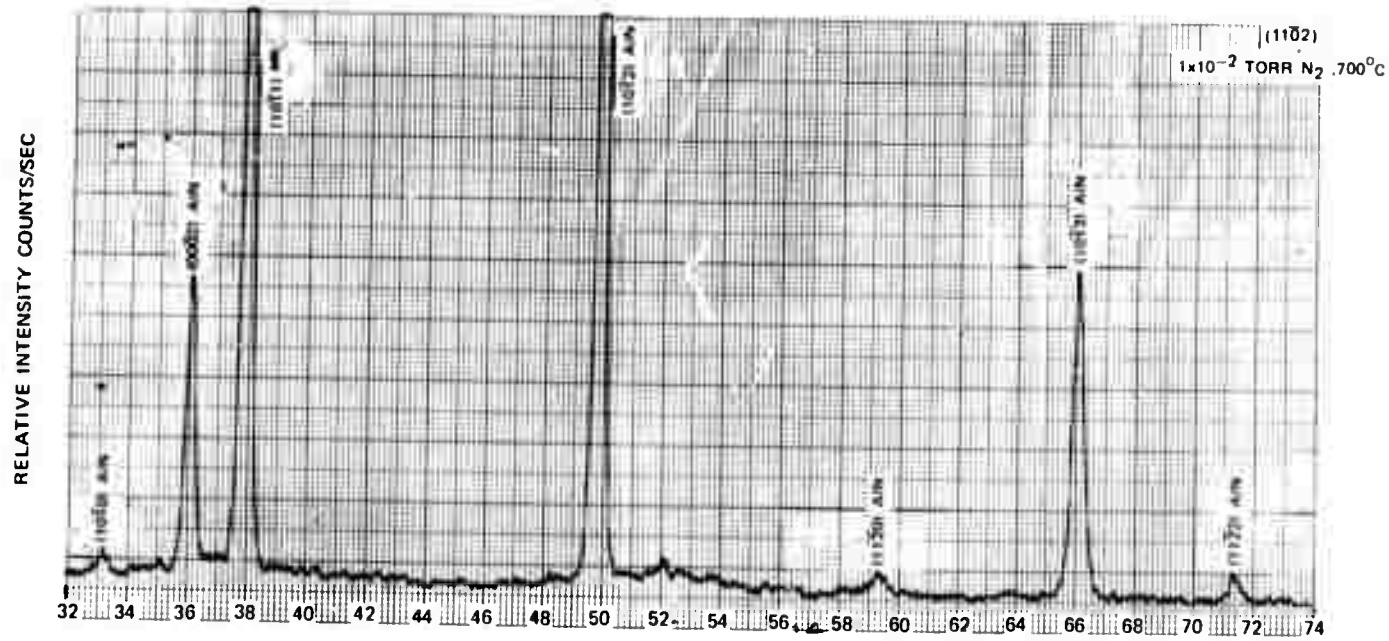


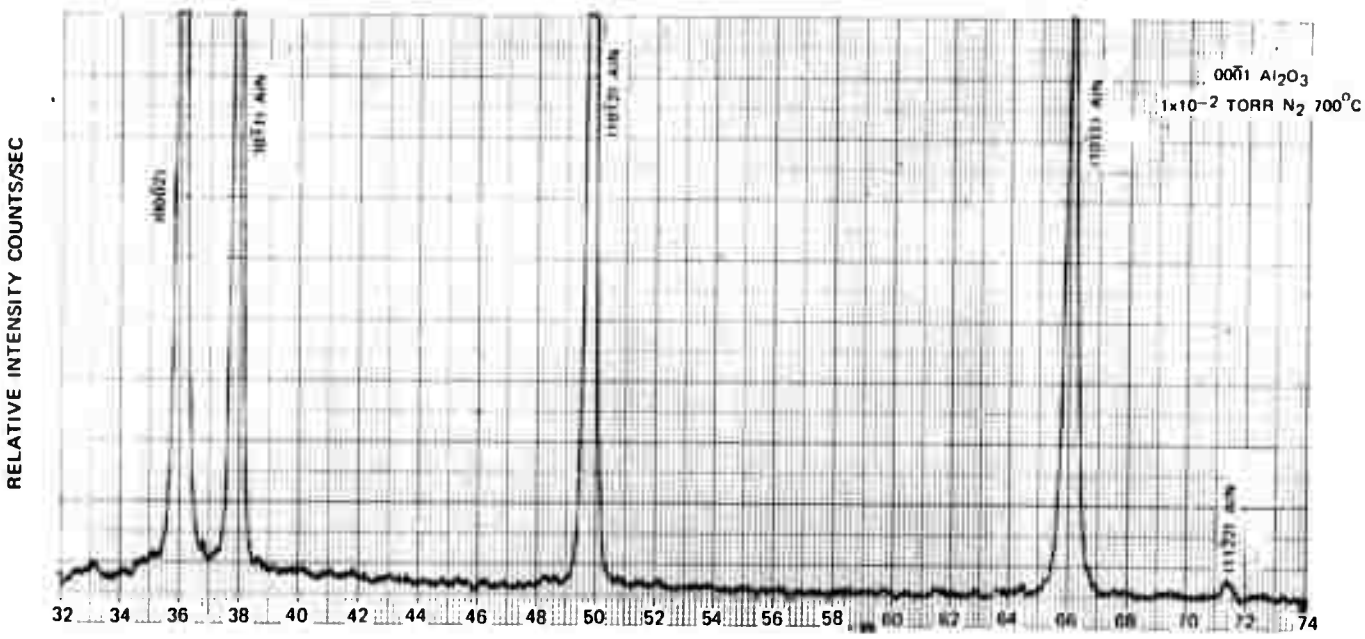


L951337-3

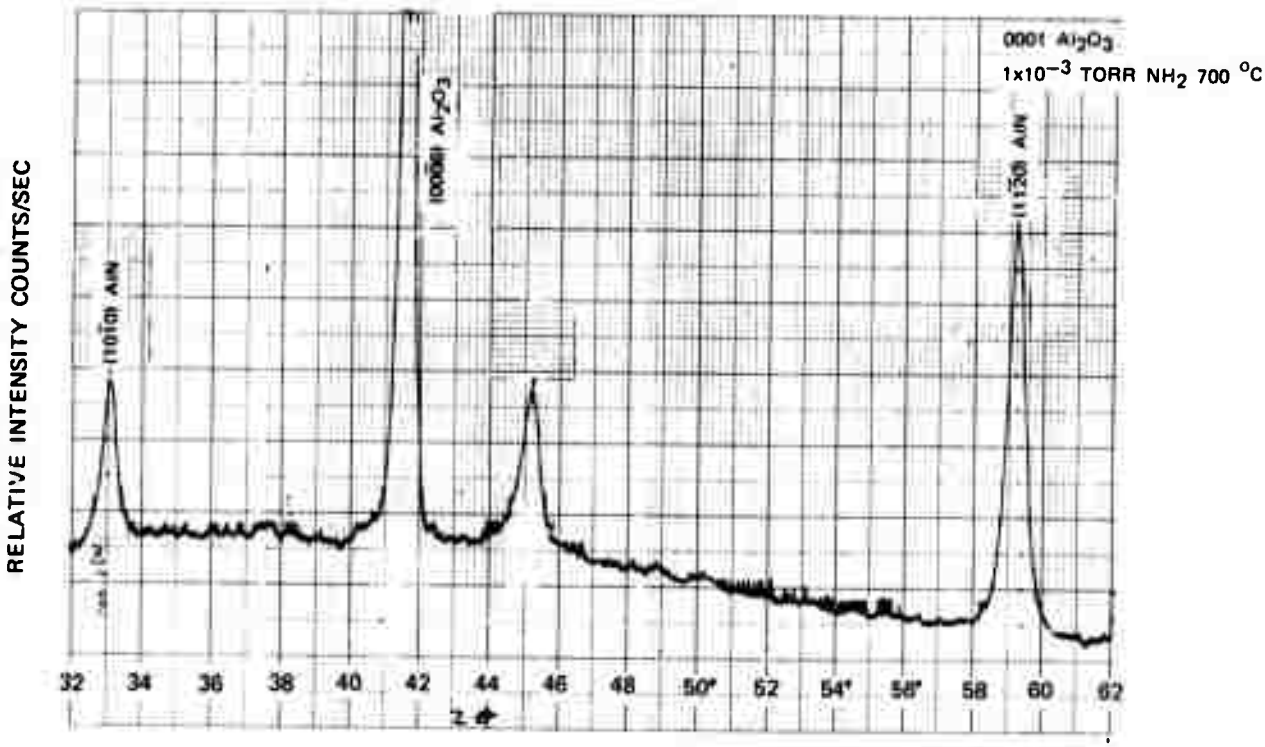
FIG. 9

DIFFRACTOMETER TRACES OF AlN FILMS REACTIVELY SPUTTERED IN N_2 AT 700°C ON $(00\bar{0}1)$ AND $(10\bar{1}2)$ Al_2O_3 SUBSTRATES

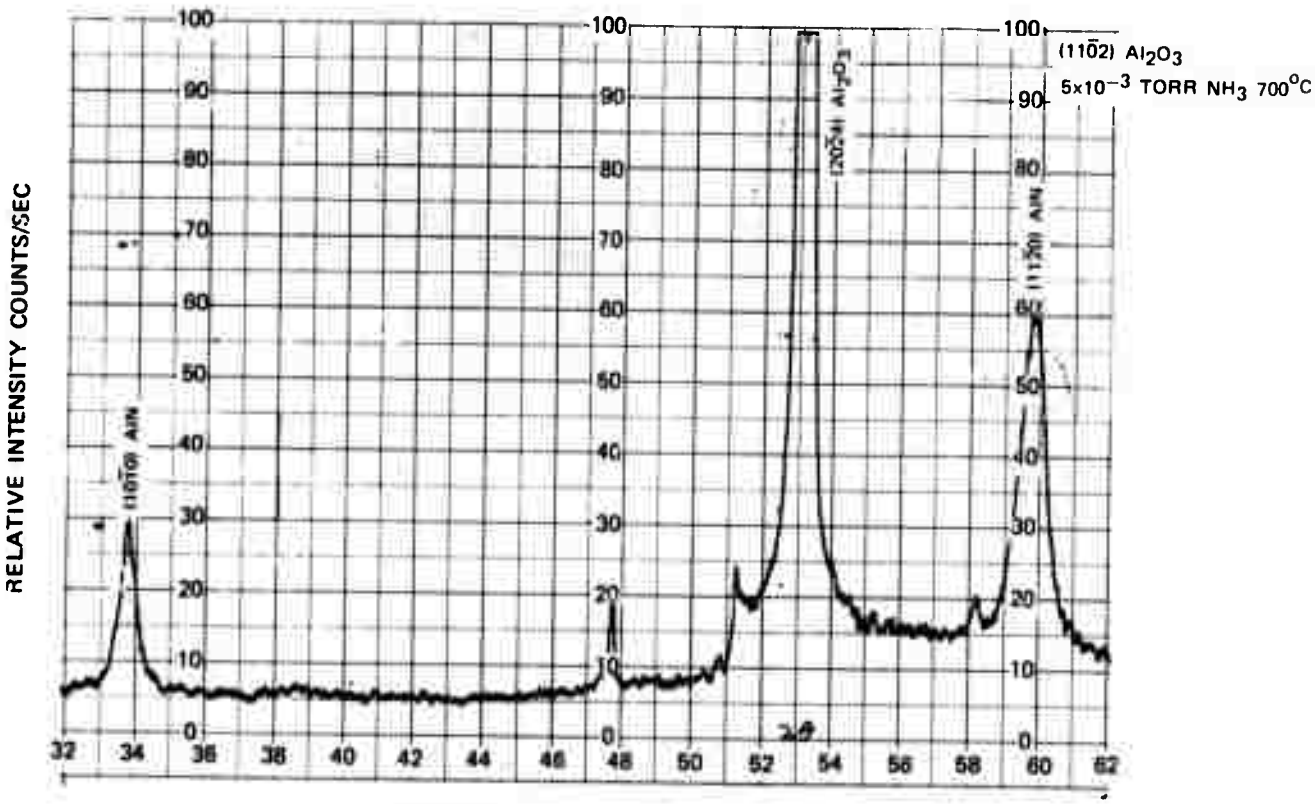




DIFFRACTOMETER TRACES OF AlN FILMS REACTIVELY SPUTTERED IN 5 X 10^{-3} TORR NH_3 AT 700 °C ON (00$\bar{1}$1) AND (10$\bar{1}$2) Al_2O_3 SUBSTRATES.

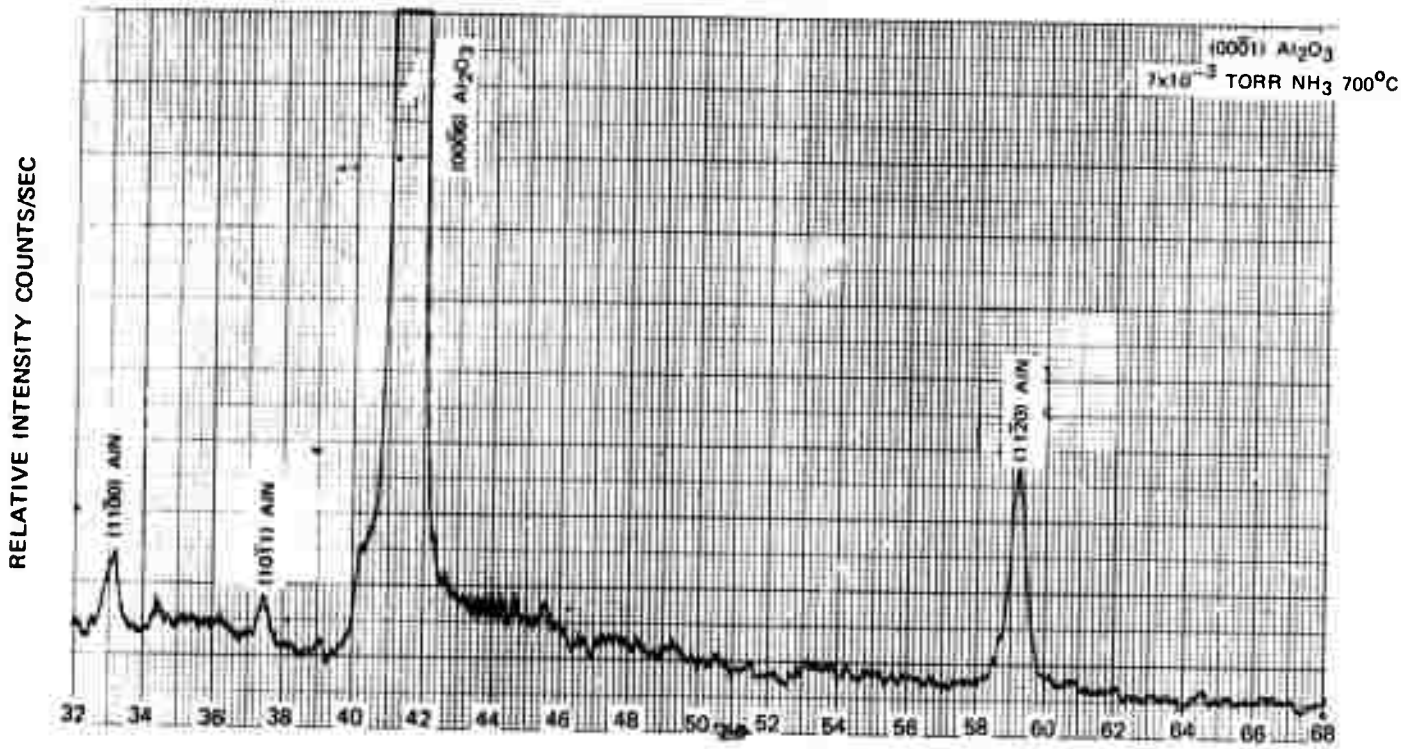


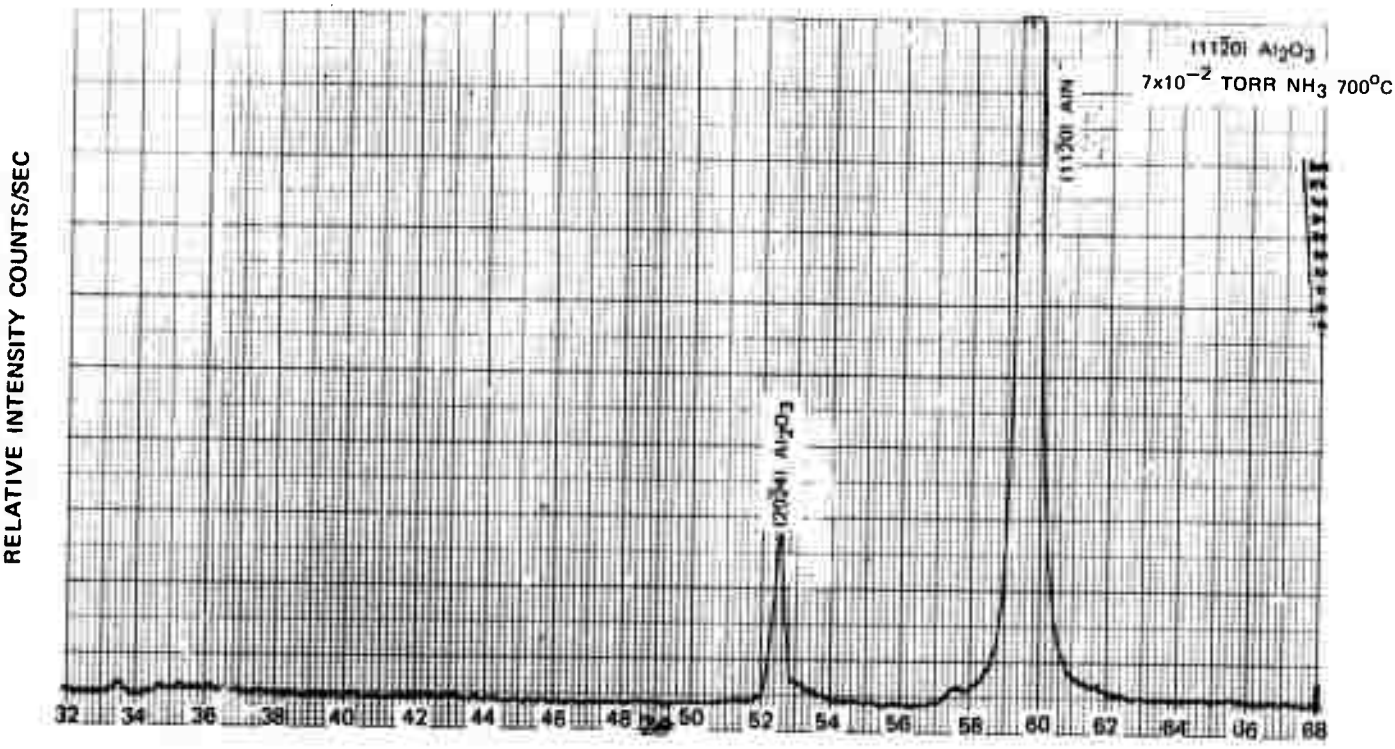
DIFFRACTION ANGLE 2θ – DEGREES



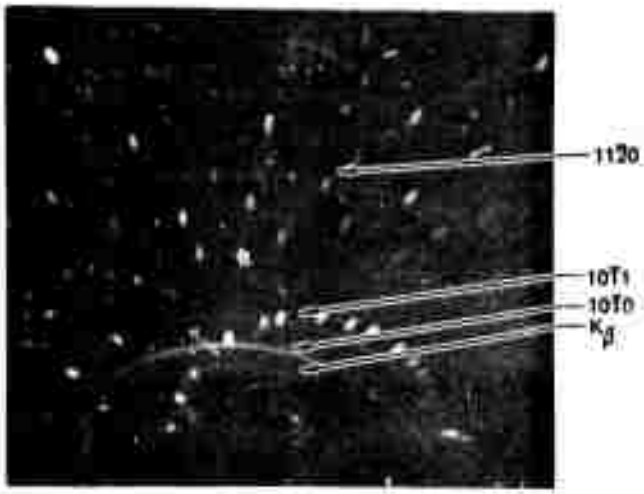
DIFFRACTION ANGLE 2θ – DECREES

DIFFRACTOMETER TRACES OF AlN FILMS REACTIVELY SPUTTERED IN 7 X 10^{-2} TORR NH_3 AT 700 °C ON (00$\bar{0}$1) AND (10$\bar{1}$2) Al_2O_3 SUBSTRATES.



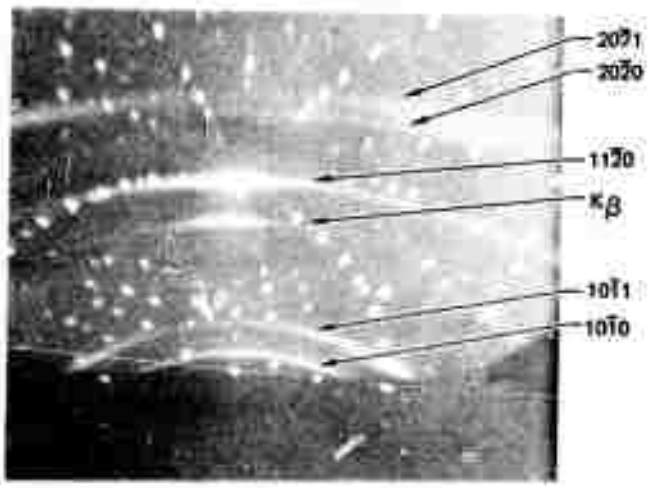


X–RAY DIFFRACTION DATA FOR REACTIVELY SPUTTERED ALUMINUM NITRIDE

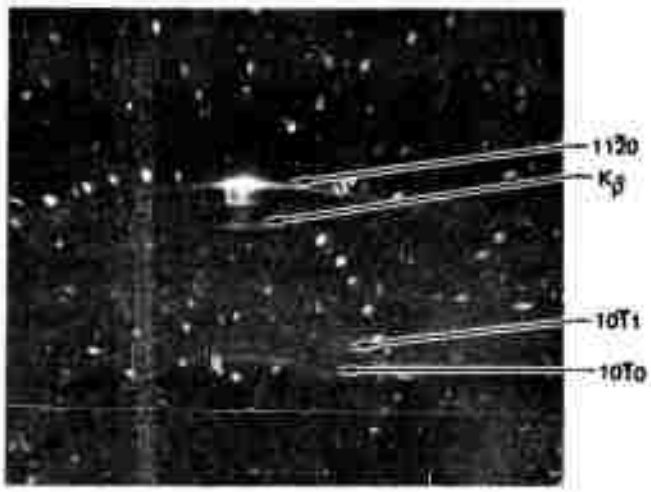


(a) 1 X 10^{-2} TORR NH_3 (0001) Al_2O_3 SUBSTRATE 200°C DEPOSITION TEMP.

(b) 1X10^{-2} TORR (1$\bar{1}$02) Al_2O_3 SUBSTRATE 700°C DEPOSITION TEMP.

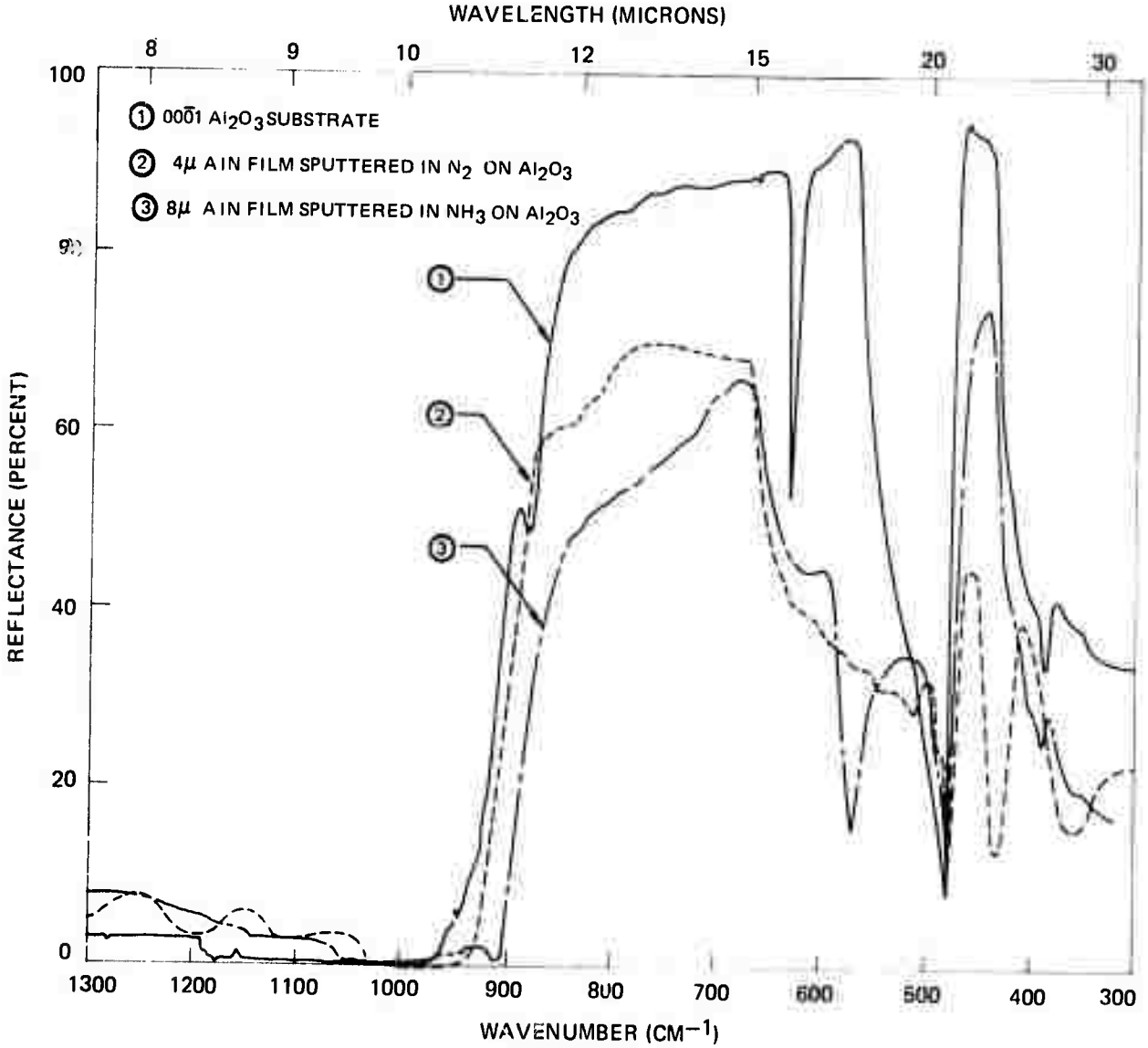


(c) 5 X 10^{-3} TORR (1$\bar{1}$02) Al_2O_3 SUBSTRATE 700°C DEPOSITION TEMP.



(d) 7 X 10^{-2} TORR NH_3 (1$\bar{1}$02) Al_2O_3 SUBSTRATE 700° DEPOSITION TEMP.

FAR INFRARED REFLECTANCE SPECTRUM OF AlN



C–V CHARACTERISTICS OF 1000Å $SrTiO_3$ – 20 Å SiO_2 ON 10 Ω – CM n–TYPE SILICON

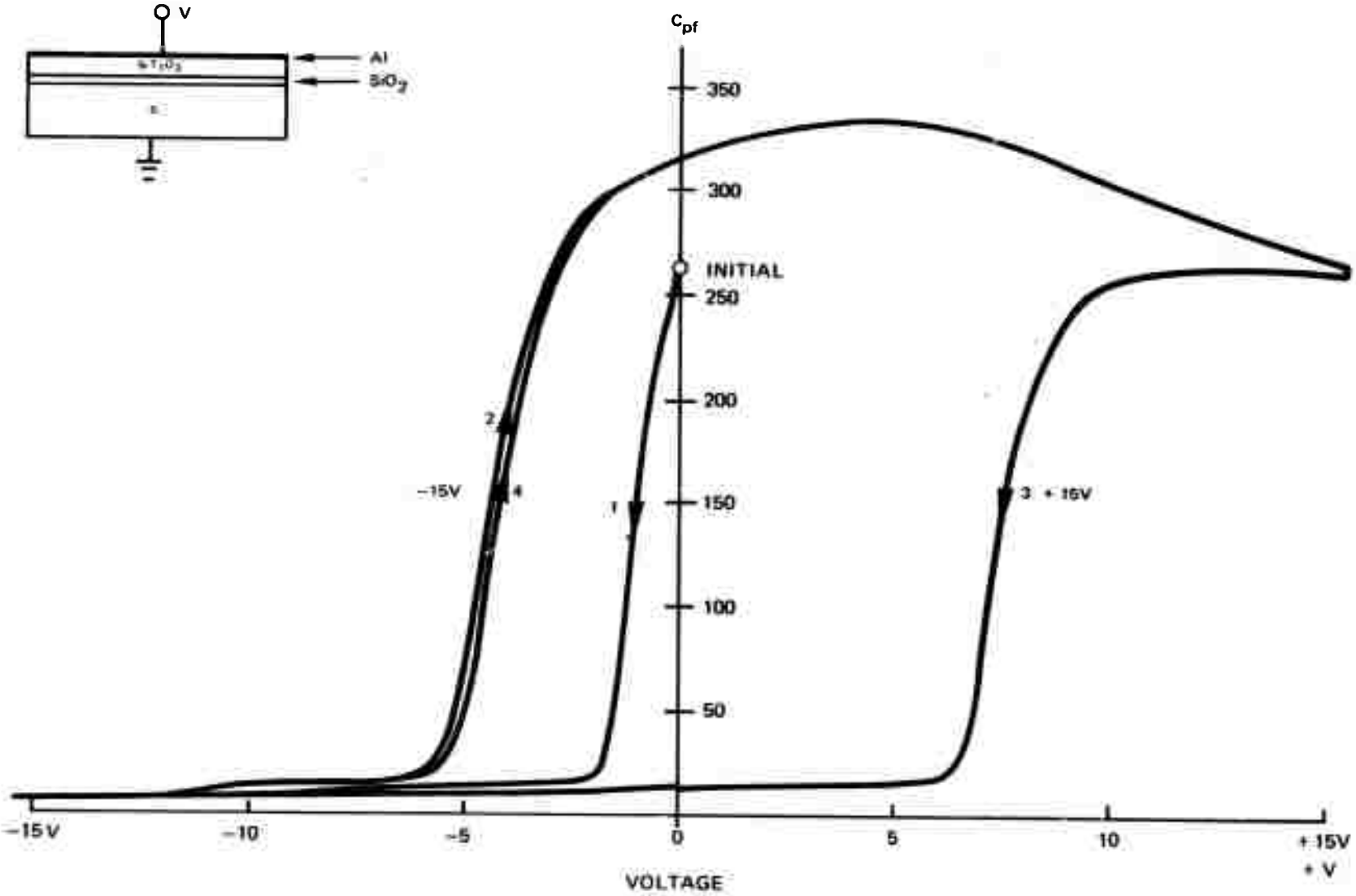


FIG. 14

FIG. 15

CURRENT–FIELD CHARACTERISTICS OF $SrTiO_3$

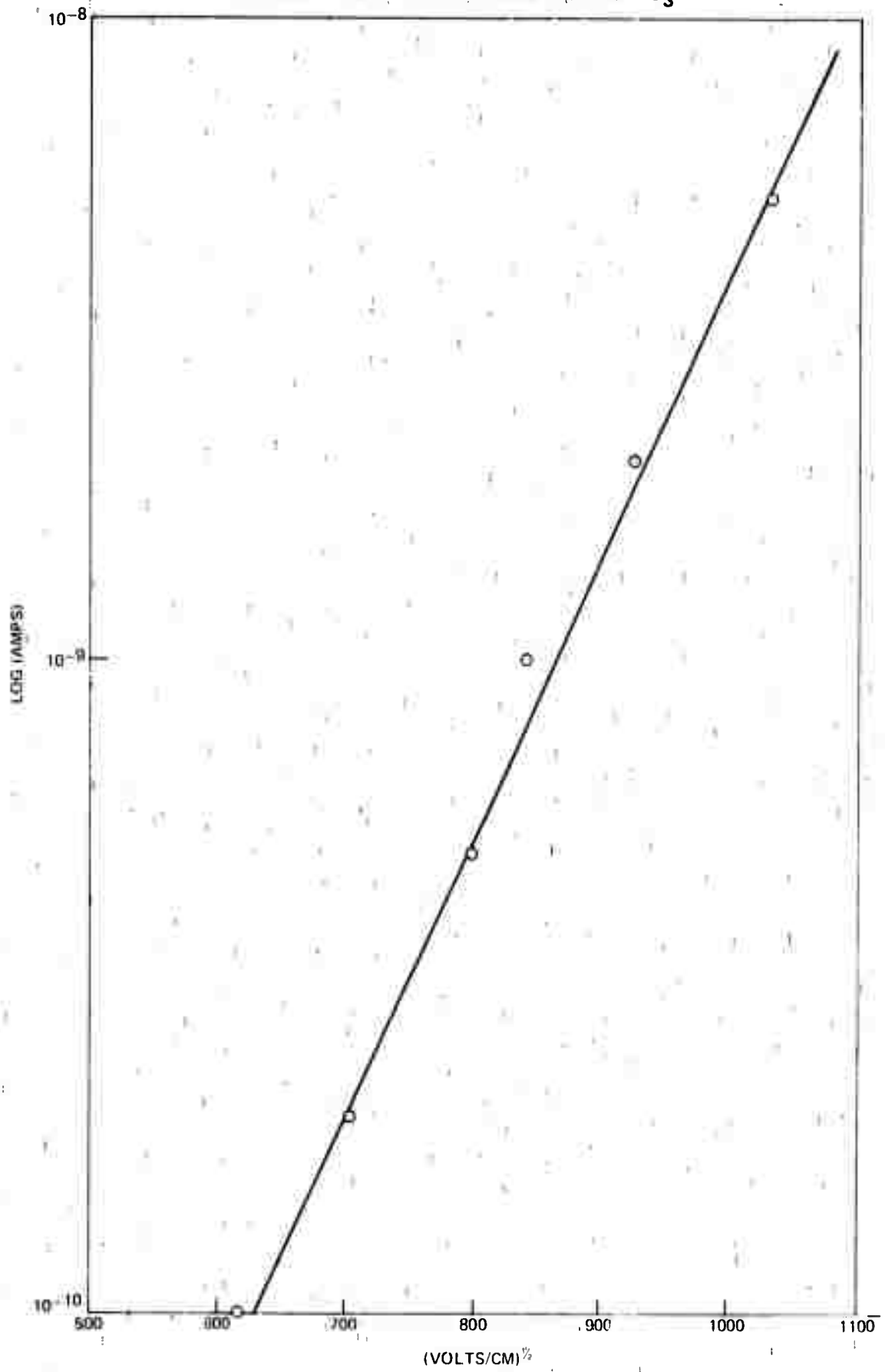
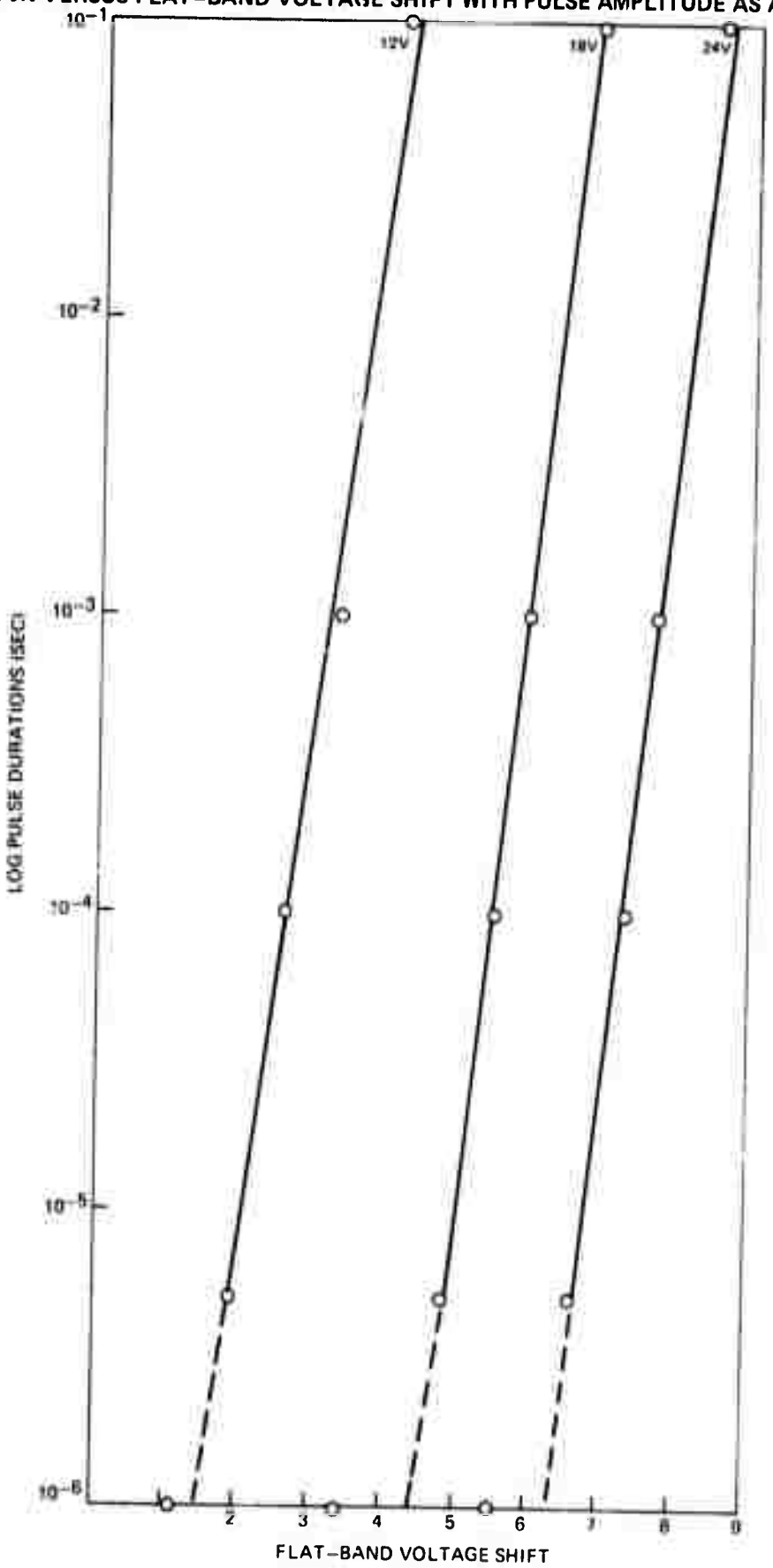
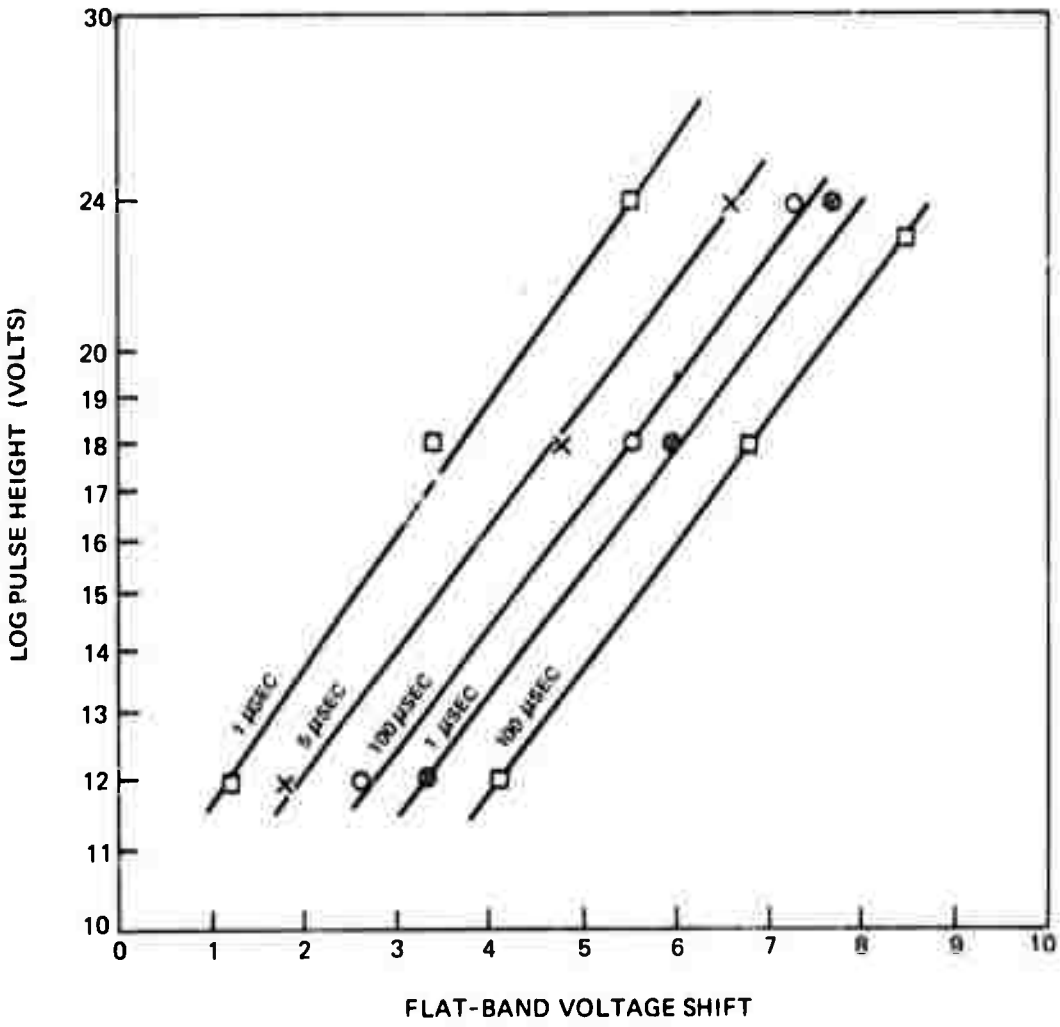


FIG. 16

PULSE DURATION VERSUS FLAT-BAND VOLTAGE SHIFT WITH PULSE AMPLITUDE AS A PARAMETER



FLAT-BAND VOLTAGE SHIFT VERSUS PULSE VOLTAGE WITH PULSE LENGTH AS A PARAMETER



TRANSFER CHARACTERISTICS OF $SrTiO_3$ - IGFET

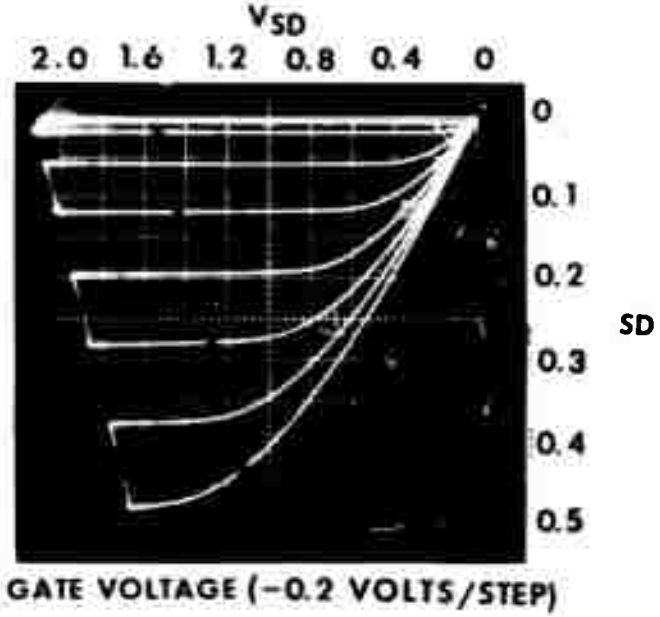
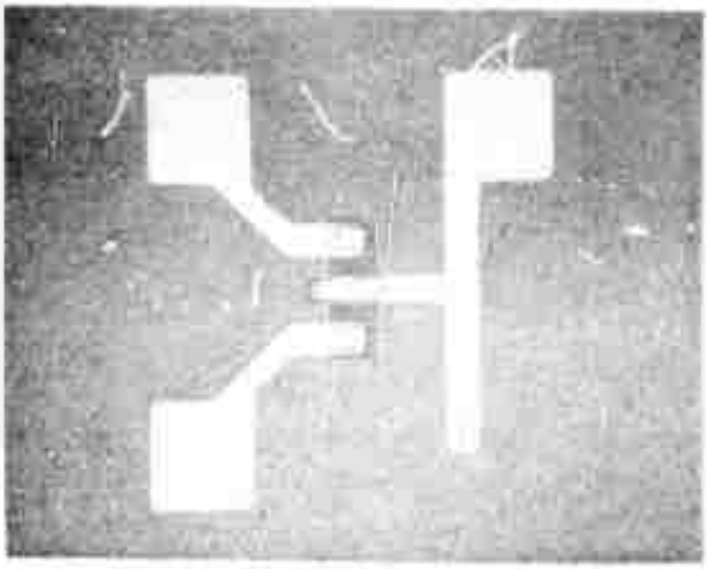


FIG. 18

STRONTIUM TITANATE –IGFET



APPENDIX I-SUBSTRATE PREPARATION

Among the many requirements necessary to initiate epitaxial growth, the substrate lattice parameters, symmetry and its surface preparation are important factors. Accordingly, a variety of substrate materials and substrate lattice orientations were used in this part of the program. Furthermore, some substrates of a particular material and lattice orientation were prepared differently to determine that effect on film growth. The types of substrate materials chosen and the surface prepararation given them are summarized in Table AI. The normal sequence of preparation was that implied by reading the table from left to right.

The mechanical preparation consisted in polishing the substrates smooth. The final step in the polishing utilized a water slurry of 0.3 μ alumina grit in a Buehler Metallurigical Vibromet Polisher. Standard cleaning of all substrates consisted of; (1) boiling in trichloroethylene, (2) rinsing in acetone, (3) rinsing in methanol, (4) thorough flushing with deionized water,and finally (5) spinning dry in a centrifuge. All solvents used were MOS grade.

Heat treatment was intended to anneal and eliminate the damage produced by the mechanical polishing and leave the surface of the substrate as a well ordered crystal. For this stage of preparation, the substrates were placed in an alumina boat and annealed at 1200°C in air for 2 hours.

Chemical etching of the substrate varied depending on substrate material. As with the annealing, this step of the preparation was intended primarily to remove the damaged layer and expose a crystal face for film growth. In some cases, however, chemical etching served only to remove amorphous surface oxides. Chemical etching of the Al_2O_3 consisted of a 6 minute dip in 320°C to 350°C phosphoric acid. As noted in the table, some Al_2O_3 substrates were annealed before chemical etching. MgO and ZnO were both chemically etched in a 20 percent solution of nitric acid for 1.5 minutes. Silicon was dipped in concentrated hydrofloric acid to remove any surface oxide while SiO_2 was dipped in hydrofloric acid for 3 minutes for a surface etch. SiC was first dipped into hydrofloric acid to remove surface SiO_2. The crystals were next etched in 400°C potassium hydroxide for 15 minutes. This was followed by a second 1 minute dip in hydrofloric acid. After the final acid etch, all substrates were rinsed in boiling deionized water followed by a thorough flush in cold deionized water then spun dry.

TABLE AI–1

CRYSTAL CONSTANTS Å

SUBSTRATE	CRYSTAL TYPE	a	c	ORIENTATION	AS RECEIVED	MECHANICAL	THERMAL	CHEMICAL
Al_2O_3	HEXAGONAL	4.76	12.99	0001	POLISHED	–	1200°C	–
Al_2O_3				1012	POLISHED	–	1200°C	–
Al_2O_3				0001	POLISHED	–	1200°C	YES
Al_2O_3				1012	POLISHED	–	1200°C	YES
SiC	WURTZITE	3.08	5.05	0001	PLATELETS	–	–	YES
ZnO	WURTZITE	3.24	5.18	0001	CUT	YES	–	YES
MgO	CUBIC	4.21	–	100	CLEAVED	–	–	–
MgO	CUBIC	4.21	–	100	CLEAVED	YES	–	YES
SiO_2	AMORPHOUS				POLISHED	–	–	YES
Si	CUBIC	5.43	–	100	POLISHED	–	–	YES

APPENDIX II-VARIABLE THRESHOLD FIELD EFFECT MEMORY TRANSISTOR

A.II-1 Principles of Operation

Controlled charge storage in the gate dielectric of an insulated gate field effect transistor can be utilized as a nonvolatile, electrically alterable store for digital data (Refs. 1 and 2). The form of the memory element is a modified MOS (Metal-Oxide-Semiconductor) transistor in which the silicon dioxide gate insulator is replaced by a double insulator. This is illustrated in Fig. AII-1. Typically a layer of SiO_2 10-100Å thick is nearest the silicon substrate and a second insulator 300-1000Å thick is deposited over the SiO_2. The second insulator, in structures reported to date, has been either silicon nitride (Refs. 3 and 4) or aluminum oxide (Ref. 6). Trapping sites exist at the dual dielectric interface and can be charged and discharged by applying a voltage of sufficient magnitude and suitable polarity to the gate electrode. The silicon surface potential is influenced by the charge states of the traps, thereby, affecting the threshold voltage of the dual dielectric MIS (Metal-Insulator-Semiconductor) transistor. The degree of threshold shift is dependent on pulse amplitude and duration. Information is stored by setting the threshold to a predetermined high (-8 volts) and low (-2 volts) values which correspond to a digital zero or one state. An interrogation voltage intermediate (-5 volts) to the two possible threshold voltage extremes applied to the gate electrode of the transistor will turn on only the device preset to a low threshold. Current will be drawn only by memory transistors in the low state and only during the interrogation cycle. Writing is generally done at much higher levels (20-50 volts) and therefore the interrogation voltages will have a negligible effect on the preset threshold. Characteristics of a typical memory element is illustrated in Fig. AII-2.

The mechanisms responsible for charging and discharging the gate insulator are reasonably well understood. There are a number of possible modes of operation by which the trap can be charged and discharged. These include direct tunneling between the traps and the silicon (Ref. 8); Fowler-Nordheim tunneling into the conduction band of the silicon dioxide (Ref. 5), Poole-Frankel bulk conduction through the insulator (Ref. 7). Which of the above conduction mechanisms predominates in a given structure is determined by the thickness of the silicon dioxide layer, the insulator layer thickness and its stoichiometry. The most interesting structure occurs when direct tunneling is the principal mode of charge transfer to the interface traps. This condition is met for SiO_2 film thickness under 20Å and will result in devices with the fastest switching times. Ross and Wallmark (Ref. 8) were the first to present a theory explaining the switching behavior on thin oxide MNOS memory transistors in which direct tunneling from the silicon into the interface states located at the interface between the two insulators is the principal mechanism for charge transfer. The theory predicts that charge transfer in such a device is logarithmically dependent on the gate pulse duration and exponentially dependent on the amplitude of the applied gate pulse. The theory was shown to be in good agreement with experimental results. More recently, Svensson and Lundstrom (Ref. 13) showed that the properties of the thin oxide device

could also be explained by a modified Fowler-Nordheim current. They point out that direct tunneling to mid-gap states in the Si_3N_4 would take place at lower fields and that, at higher fields, charge from the silicon will be injected directly into the conduction band of the Si_3N_4 and subsequently trapped. Again, theory and experiment was shown to be in good agreement. Although the charge transfer mechanisms in MNOS are apparently well understood and device performance predictable, little if anything at all is understood about the nature of the trapping sites for charge. Based only on first principles, the theory is not adequate to predict characteristic switching behavior of new dual insulator combinations. Every new insulator system must be studied experimentally. Only after the current-voltage characteristics are determined can device performance be modeled. The nature of the interface traps, their energy, and spatial distribution can influence the operation of a memory device and they are process dependent variables.

A.II-2 Current State of the Art

To date, only two insulator systems have received much attention in the quest for fabricating a nonvolatile semiconductor memory. They have been the SiO_2 - Si_3N_4 and SiO_2 - Al_2O_3 systems. The results obtained to date on the two systems indicate that charge retention periods in excess of several years are feasible (Refs. 9 and 10). In most cases, long-term data retention is obtained with long write and clear times as a penalty (Ref. 10). Devices fabricated to have short write and clear times generally have a short term charge storage capability. In all cases high clear and write voltages (25-50 volts) are required and it is this requirement which imposes severe restrictions on the organization of the memory (Ref. 11) and introduces fabrication problems when the address-decode networks are to be integrated onto same chip with the memory transistor matrix. Transistors initially fabricated utilizing SiO_2 - Al_2O_3 for the gate dielectric were not truly electrically alterable and required a pulse of ionizing radiation during the clear cycle (Ref. 6). More recently an electrically alterable version was reported but the write-erase cycle was very slow and required voltages in excess of 60V (Ref. 14).

In an attempt to lower the required switching voltages of MNOS devices it has been reported (Ref. 9) that attempts are being made to fabricate devices with a silicon nitride layer thickness of 300Å. The feasibility of maintaining process control to produce continuous layers with uniform thickness on this scale and achieve reasonable yields seems highly questionable. Even if this goal is to be realized, switching voltages in the vicinity of 25 volts or more will still be required to achieve reasonable device performance. In other words, one is left with similar problems and the only gain is a small improvement in switching speed. Device yield remains a questionable matter. To date, the best result reported for a Si_3N_4 - SiO_2 device which exhibits long term charge storage is a switching speed of 10 μsec, with a 30V pulse for an insulator structure composed of a 20Å SiO_2 film and a 433Å silicon nitride film (Ref. 9). Clearly, staying with the conventional MNOS (Metal-Nitride-Oxide-

Semiconductor) structure leaves little hope for a dramatic improvement in device performance. A possible way out of this dilemma may be through the utilization of high dielectric constant insulators such as rutile, rare earth oxides or ternaries such as $SiTiO_3$, etc., in place of silicon nitride. High dielectric constant materials lower the required operating voltages sufficiently such that compatibility with low threshold MOS and T^2L circuits would be no problem.

A.II-3 High Dielectric Constant Gate Insulator

To date, efforts expended on the MNOS structure have resulted in a succession of marginal improvements in device performance. New insulator systems utilizing high dielectric constant materials should be investigated. RF sputtering is the technology which offers a wide degree of flexibility for the deposition and synthesis (reactive sputtering) of a wide variety of materials. The relatively low deposition temperatures possible by this technique eliminates high temperature processing which could result in adverse reactions of the deposited film with the thin silicon dioxide layer required in memory structures.

In the previous section it was stated that direct tunneling through a silicon dioxide layer of approximately 20Å into traps at the dual dielectric interface would yield devices with the fastest switching times. Tunneling will occur in this silicon dioxide films at an electric field intensity of approximately 7×10^6 V/cm (Ref. 12). Table I lists the dielectric constants for some of the materials discussed and the corresponding switching voltages and insulator fields generated in the SiO_2 - insulator structures for the case when tunnel currents will flow through the SiO_2 film. The figures in the table clearly illustrate the fact that the switching voltage required for a device fabricated with a high dielectric constant film such as $SrTiO_3$ is considerable less than that required for Si_3N_4 or Al_2O_3. The smaller electric fields in the high dielectric constant film should reduce charge leakage and, hence, improve charge retention. The lower switching voltage will eliminate all the associated address decode and clear-write network problems encountered with devices using the silicon nitride and aluminum oxide systems and also eliminate the need for extra power supplies. A device fabricated along these lines could serve as a random access memory with a nonvolatile store. Switching times of one microsecond or less seem feasible. The switching time for a device with a tunnelable SiO_2 film varies exponentially with pulse amplitude. Hence, doubling of the switching voltage from 5V to 10V should produce a substantial increase in device speed with no penalty in the form of added complications to the control circuitry. A final advantage to be gained through the utilization of high dielectric constant films lies in the fact that the relatively "thick" insulator film in the dual dielectric composite should result in higher device yields. The preparation of continuous and uniform films of 1000Å or more in thickness over large areas appears to be a far more tractable problem than deposition of 300Å thick films.

A.II-4 References

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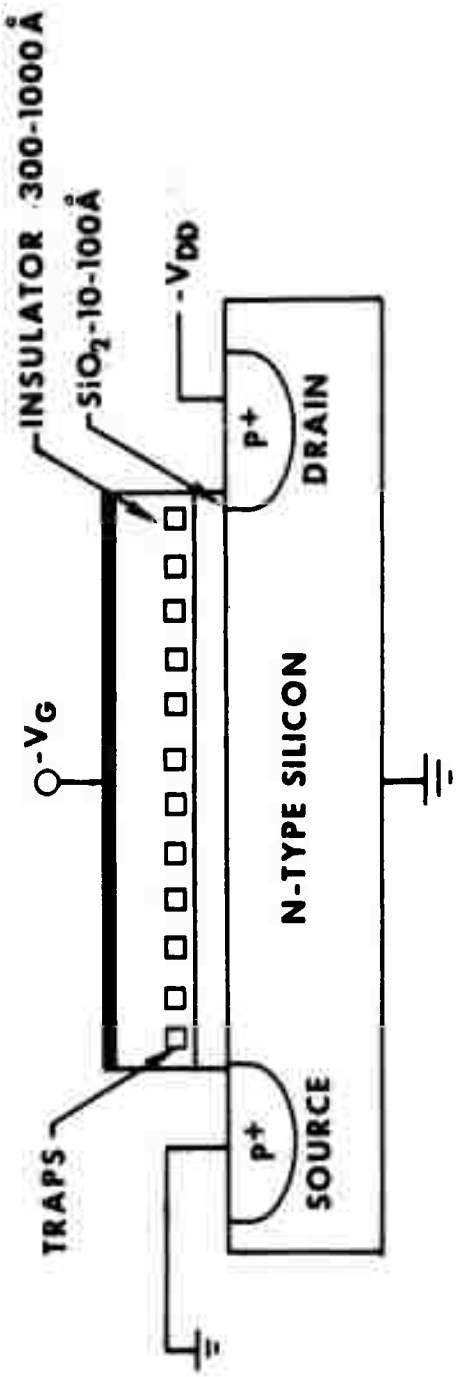
VARIABLE THRESHOLD MIS TRANSISTOR



TYPICAL TRANSFER CHARACTERISTICS FOR
A VARIABLE THRESHOLD FIELD EFFECT MEMORY TRANSISTOR

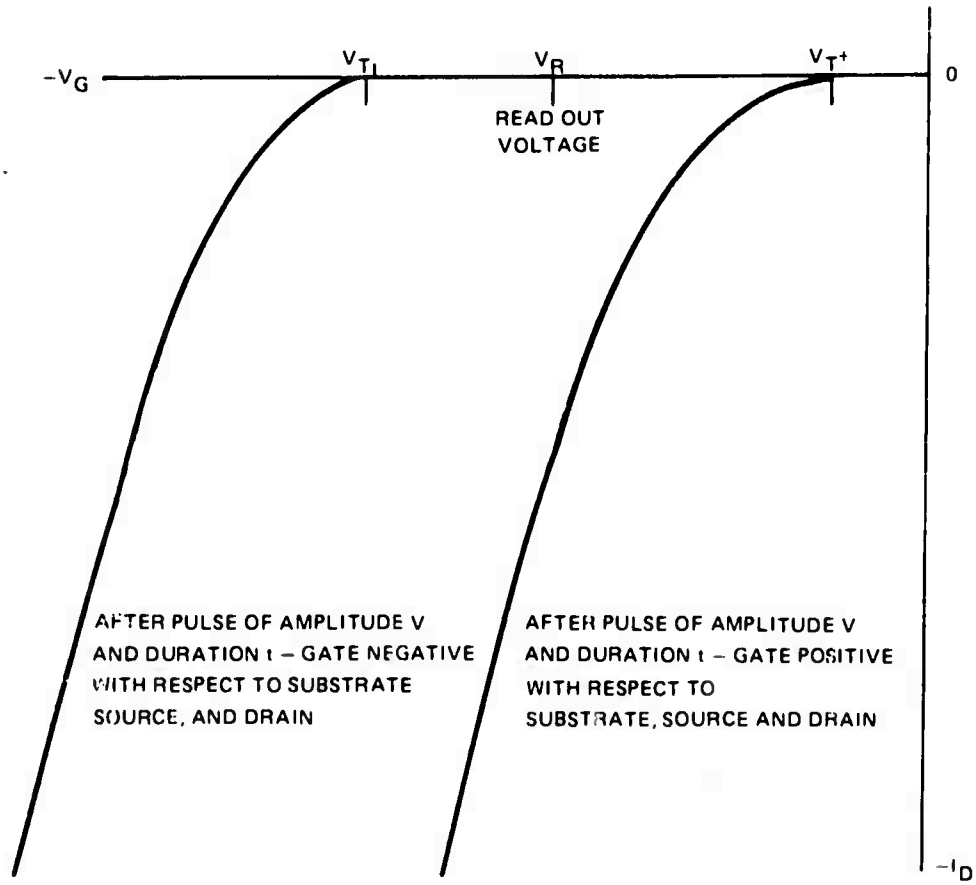
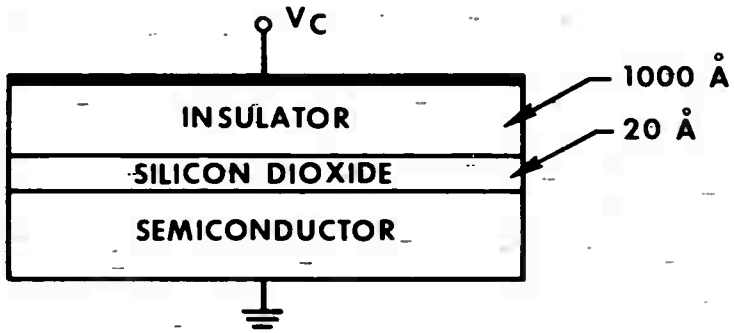


TABLE AII-1



$$E_I = \frac{K_o}{K_I} E_o$$

$$V_C = E_o \left(X_o + \frac{K_o}{K_I} \times X_I\right)$$

INSULATOR	DIELECTRIC CONSTANT	INSULATOR FIELD WHEN SiO_2 FIELD $E_o \sim 7 \times 10^6$ V/CM	V_C-CHARGING VOLTAGE REQUIRED TO PRODUCE $E \sim 7 \times 10^6$ V/CM IN SiO_2	FILM THICKNESS
SiO_2	3.9	7×10^6 V/CM	——	20 Å
Si_3N_4	6.5	4.2×10^6 V/CM	43 V	1000 Å
Al_2O_3	9.5	3×10^6 V/CM	31 V	1000 Å
HfO_2	14	2×10^6 V/CM	21 V	1000 Å
$SrTiO_3$	80	3.5×10^5 V/CM	4.9 V	1000 Å