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SHORT PULSE EFFECTS IN SEMICONDUCTOR DIODES

Derek J. Fitzgerald, et al

IKOR Incorporated
Burlington, Massachusetts

August 1972

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SHORT PULSE EFFECTS IN SEMICONDUCTOR DIODES

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Derek J. Fitzgerald
James J. Stekert

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13 ABSTRACT

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FOREWORD

This Final Report, "Short Pulse Effects in Semiconductor Diodes," covering the period 13 September 1971 to 13 May 1972, was prepared by IKOR Incorporated, N.W. Industrial Park, Burlington, Massachusetts, under contract F30602-72-C-0046, Job Order Number 45060251.

This program was administered by Rome Air Development Center, Griffiss Air Force Base, New York. Mr. Leon L. Stevens (OCTE) was the Project Engineer for the Center.

This report has been reviewed by the Information Office (OI) and is releasable to the National Technical Information Service (NTIS).

This technical report has been reviewed and is approved.

Leon L. Stevens

Approved: LEON L. STEVENS
Project Engineer
Electron Devices Section

Alfred J. Parker

Approved: JAMES L. RYNNING
Colonel, USAF
Chief, Surveillance and
Control Division

FOR THE COMMANDER: Fred I. Diamond

FRED I. DIAMOND
Acting Chief, Plans Office

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An investigation has been made to determine the feasibility of using PIN diodes as switching elements to control 150 ps, 8 MW impulse signals. Single diodes in shunt and in series with a 50 ohm stripline were studied, as were series stacks of up to 8 diodes. It is found in the series configurations that good signal fidelity obtains in forward bias at all signal voltages, with insertion loss being a function of I region thickness. Reverse bias isolation also is a function of I region thickness. At higher signal voltages it is an even stronger function of the signal, since diode conductance significantly increases with internal voltage stress. A new reverse bias equivalent circuit for high voltage transient signals is shown. Forward to reverse bias stack switching occurs in less than 500 ns with parallel bias address. No irreversible signal or switching effects are observed within the signal limits. Some irreversible increase in reverse bias current is noted. A non-optimized SPDT switch was constructed and studied. Results show definite feasibility for a high voltage, short pulse PIN diode duplexer.

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LIST OF NOTATION

A	=	Antenna terminal, a constant (See Figure 13)
C_J	=	Junction Capacitance
C_P	=	Package Capacitance
C_T	=	$C_P + C_J$
d	=	Diode stack spacing
E	=	Electric field intensity
G	=	Conductance
ISOL	=	Isolation (ratio of forward bias to reverse bias transmission)
L	=	Inductance
L_1	=	Internal Inductance
L_2	=	External Inductance
L_T	=	$L_1 + L_2$
n	=	An exponent (See Figure 13)
N	=	Number of Diodes
P	=	Parallel (See Figure 23)
R	=	Receiver terminal
R_F	=	Forward bias resistance
R_R	=	Reverse bias resistance
S	=	Series (See Figure 23)
t_{fr}	=	Forward to reverse bias switching time
V	=	Voltage
V_{ji}	=	Voltage across diode in stack
V_{ST}	=	Voltage input to stack
W	=	I region thickness
X	=	Transmitter terminal
Z_o	=	Characteristic impedance
ω	=	Angular frequency

SECTION I

INTRODUCTION

1. BACKGROUND

The existence of high peak power, short pulse sources has created a control problem. It is desirable to be able to switch such sources in and out of microwave networks in times which would make feasible such applications as Radar duplexing.

Since free space electromagnetic propagation is roughly one foot per nanosecond, devices with switching times on the order of 250 ns or less are desirable. Also, since sources with sub-nanosecond peak powers on the order of 10 MW are available, it is desirable for switch circuitry to be able to cope with the full output at useful repetition rates. Not only must the circuit elements pass such pulses with electromagnetic integrity, but they must be able to provide sufficient throughput along desired paths while providing sufficient isolation to others. Should it be desired to duplex a transmitter and receiver to a single antenna, a sensitive receiver must not see peak power levels of more than several watts during transmit, yet be available for reception within 250 ns. Meanwhile, the quality of the transmitted and received signal should not be significantly degraded. Given pulse widths on the order of 100 ps, this means instantaneous bandwidths of amplitude and phase fidelity on the order of 5 GHz, and a type of non-dispersive circuitry uncommon to less transient signals.

Conventionally, high power duplexers utilize gas discharge tubes or ferrites to achieve the rf switching action. Such devices have been built with extremely high power handling capabilities. However, the gas clean-up and the associated long recovery time of the TR tubes is not attractive for the short pulse application. Although ferrite circulators and limiters possess many of the desired characteristics, inherent limitations in time response exist which reduce the protection afforded the receiver against main bang, the effects of high antenna mismatch and the return from large nearby targets. When a high power microwave pulse of sufficient amplitude to exceed a threshold value is applied to the ferrite, a uniform precession will build up

in the time order of 10^{-8}s. Consequently, a leading edge spike problem is associated with these devices which make them relatively unattractive for sub-nanosecond short pulse application.

Semiconductor diodes have been used as microwave control elements for several years now. Characteristically, they have fast response, relatively low driving power, the ability to eliminate spike leakage, and the potential for long life. However, little or no information exists on the suitability of these elements for sub-nanosecond applications. Thus, it is apparent that investigation and characterization of the properties of semiconductor devices when subjected to short pulses is required.

2. PURPOSE OF PROGRAM

The object of this program is to develop PIN diode techniques which individually or in multiple can be used to switch 100 ps 20,000 V pulses in a 50 ohm non-dispersive transmission line. The diode switching time from non-conducting to conducting should be less than 250 ns. The turn-off time should be less than 500 ns.

3. WORK PERFORMED

During this program both theoretical and experimental investigations of the short pulse effects on semiconductor diodes were conducted.

In Section II, various types of individual PIN diodes mounted in both series and parallel configurations are characterized. Details of the test fixtures and the experimental procedures are discussed, and the findings are presented. The relative merits of different types of diodes are compared, and a new diode equivalent circuit for short pulse operation emerges.

In Section III, the diodes are combined into series mounted stacks and the theoretical and experimental properties of such stacks are described. Appropriate design criteria for diode stacking under short pulse conditions are developed.

As a final evaluation, Section IV considers the embodiment of diode stacks into SPDT switch configurations for short pulse duplexing applications. Experimental results with a breadboard SPDT diode switch are shown and discussed.

The results of the program are summarized and conclusions made in Section V, while recommendations for future study and development are presented in Section VI.

SECTION II

DIODE CHARACTERIZATION

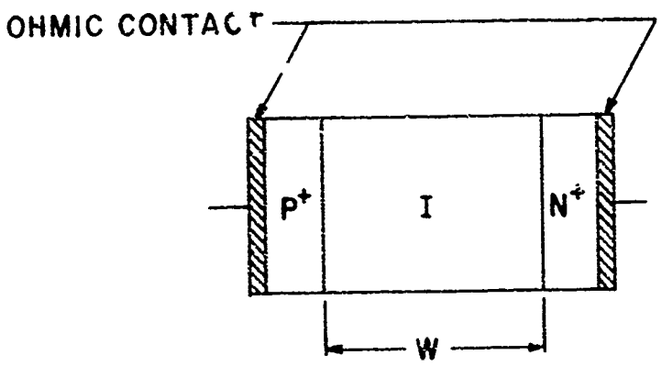
In this section, the concept of switching with individual diode elements is reviewed and the problems specifically associated with short pulse applications are discussed. Experimental results are presented showing the characteristics of various types of individual PIN diodes when subjected to short pulse stresses in series and in shunt. The relationship between the diode conductance and the impressed short pulse electric field then is developed. From this, a new equivalent circuit model of a reverse biased diode is established.

1. PIN DIODE PROPERTIES[1]

PIN type semiconductor diodes have been used for many years as microwave switching elements. The rf impedance of the diode may be switched from a usually small value in the forward biased, conducting state to another usually larger impedance in the non-conducting, reverse biased state. In an rf switching network, the diodes are incorporated into a transmission system in such a manner that a change in diode impedance results in a desired change in the rf signal transmission. The diode impedance is controlled via a dc bias circuit which must then be isolated from the signal circuit, usually by means of chokes and bypass capacitors.

The ideal PIN diode structure is shown in Figure 1. The silicon diode usually consists of an intrinsic or very lightly doped I-region, with abrupt junctions to heavily doped P^+ and N^+ regions. Metalization layers and electrical contact are made to the highly doped diffused faces.

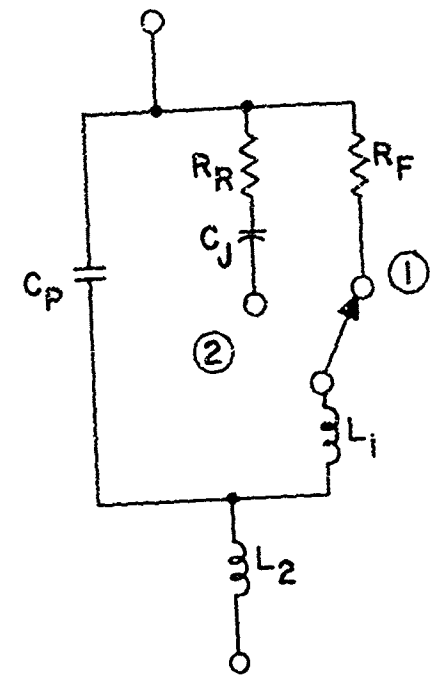
The commonly used equivalent circuit of the forward and reverse biased diode is presented in Figure 2. When the diode is forward biased, holes and electrons are injected into the I-layer from the P^+ and N^+ regions respectively. If the carrier lifetimes are relatively long, the I-region becomes flooded with carriers giving rise to the low resistance and inductive reactance of the forward biased diode. Under forward bias a carrier moves primarily by diffusion. Given a short pulse signal the transit



PIN DIODE STRUCTURE

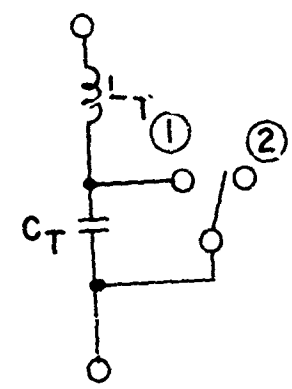
FIGURE I

R_F = FWD. BIAS RESISTANCE
R_R = REV. BIAS RESISTANCE
C_P = PACKAGE CAPACITY
C_J = JUNCTION CAPACITY
L_1 = INTERNAL INDUCTANCE
L_2 = EXTERNAL INDUCTANCE



(A) DETAIL EQUIVALENT CIRCUIT

$L_T = L_1 + L_2$
$C_T = C_P + C_J$



1 FORWARD BIAS
2 REVERSE BIAS

(B) SIMPLIFIED LOSSLESS EQUIVALENT CIRCUIT

DIODE EQUIVALENT CIRCUITS
FIGURE 2

time of carriers in the I-region then can be much longer than the duration of the applied signal. Under such conditions, no rectification occurs for either positive or negative signal polarity. Such is the case for the 100 to 200 ps impulses used in this program.

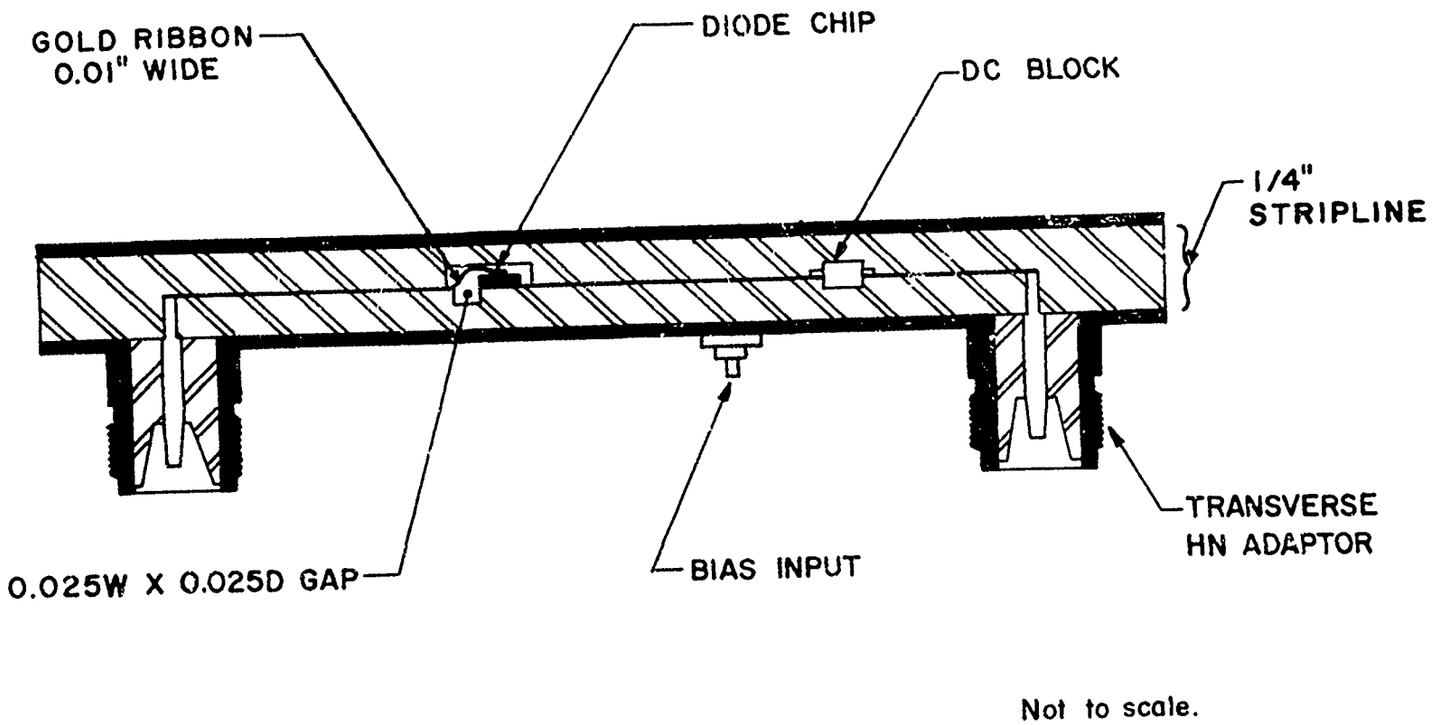
When a diode is switched from the forward to reverse bias state by application of a reverse voltage, the current does not decay immediately because the excess carriers within the diode have a finite lifetime and the external circuit cannot remove them instantaneously. Transient currents are generated which decay as the space charge regions developing at the I-junction become progressively wider and the residual charge is swept out. The diode impedance then rapidly increases as the voltage across the diode increases to a steady-state reverse-bias value. At this point the diode impedance looks essentially capacitive as shown in Figure 2A. It often is more convenient for many circuit design applications to use the simplified equivalent circuit model of the diode shown in Figure 2B.

Under conditions of high voltage short pulse excitation it is found that reverse bias conductivity as well as the capacitive character of the I-region must be taken into account. It is shown below that such conductivity is an increasing function of the electric field intensity in the bulk of the device. This necessitates a modification of the reverse bias equivalent circuit for the diode.

2. TEST FIXTURES

Two types of test fixtures were developed for mounting diodes in a 50 ohm transmission line structure. One accommodates diode mounting in series with the transmission line, while the other provides shunt mounting of the diode. The purpose of the test fixture is to allow investigation of the properties of the various types of PIN diodes under high power, short pulse stresses.

An assembly detail of the series mounting test fixture is shown in Figure 3. It is seen that the fixture is a stripline structure, with transverse HN adaptors for coupling the high voltage pulse signals into and out of the structure. The diode bias circuit is built into the fixture. A 200 nh coil connects the bias input to a point in the transmission line between the diode



DIODE TEST FIXTURE

FIGURE 3

and the dc block. A similar coil provides a dc return path to ground on the other side of the diode. A 20 pF chip by-pass capacitor is used at the bias input. The purpose of the gap or transverse slot cut through the dielectric in the vicinity of the gold ribbon is not only to provide a mounting point for the series diode, but also to inhibit voltage tracking across the teflon-fibre-glass dielectric surface. A single gap without a diode can withstand a 150 ps pulse with an amplitude of approximately 13 kV before breaking down. The breakdown voltage can be increased to greater than 20 kV by air pressurization to 50 p.s.i.

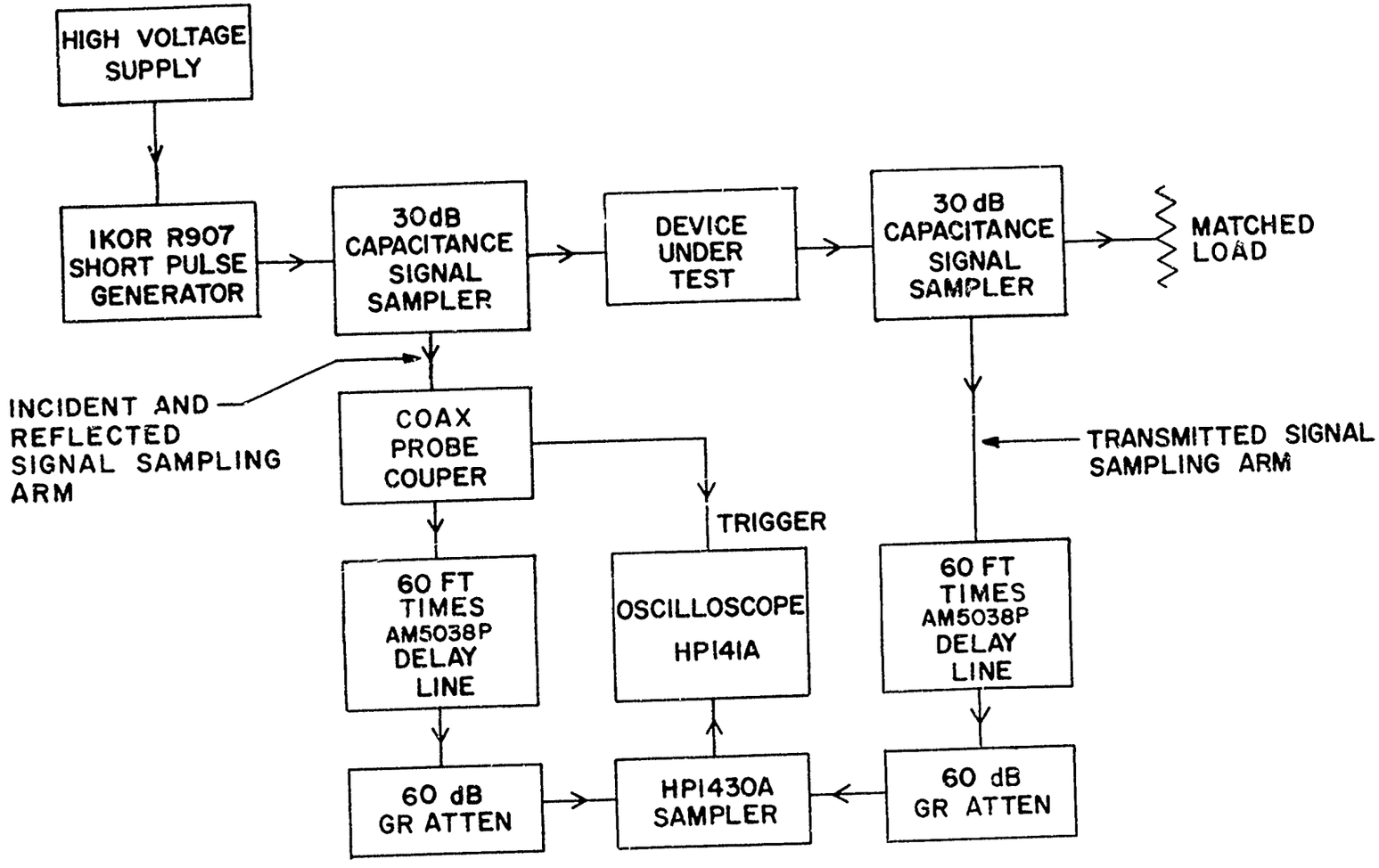
The transverse HN to stripline adaptors can transmit a 20 kV, 150 ps pulse with good fidelity. The VSWR of two adaptors joined by a length of 50 ohm stripline is 1.2:1. Similar adaptor results have been obtained using both 0.250" and 0.125" stripline ground plane spacing (GPS).

The voltage stress on a reverse biased, series mounted diode is twice that of a shunt mounted diode in the same impedance transmission line.[2] Further, it will be shown in Section IV that series mounting is fundamental to realizing a short pulse SPDT switch function. Thus, most emphasis has been placed on characterizing series diodes. However, for comparison purposes and completeness, some shunt mounted diodes were tested.

The shunt mounted diode test fixture consists of a length of GR 874 type coaxial transmission line. An Erie feed thru capacitor screwed into the outer coaxial conductor provides the mounting and bias contact for the diode under test. The diode-to-inner-conductor contact is insured by having a gold plated phosphor bronze fuzz button between these parts. All shunt-mounted diodes tested were sealed in glass or metal-ceramic packages, which have inherently more inductance than the non-packaged chips used in the series mounted tests.

3. EXPERIMENTAL APPARATUS

The experimental apparatus used to test the diodes is illustrated schematically in Figure 4. Shown are two capacitive signal samplers, one on either side of the device under test. One sampler is used to monitor the input and reflected signals from the device, while the other monitors the



EXPERIMENTAL TEST FACILITY

FIGURE 4

transmitted signals. The amplitude of the incident voltage is controlled by adjustment of the short pulse generator. Determination of the absolute value of the signals is made by careful calibration of the attenuation from the signal sampler to the input of the HP 1430A sampler.

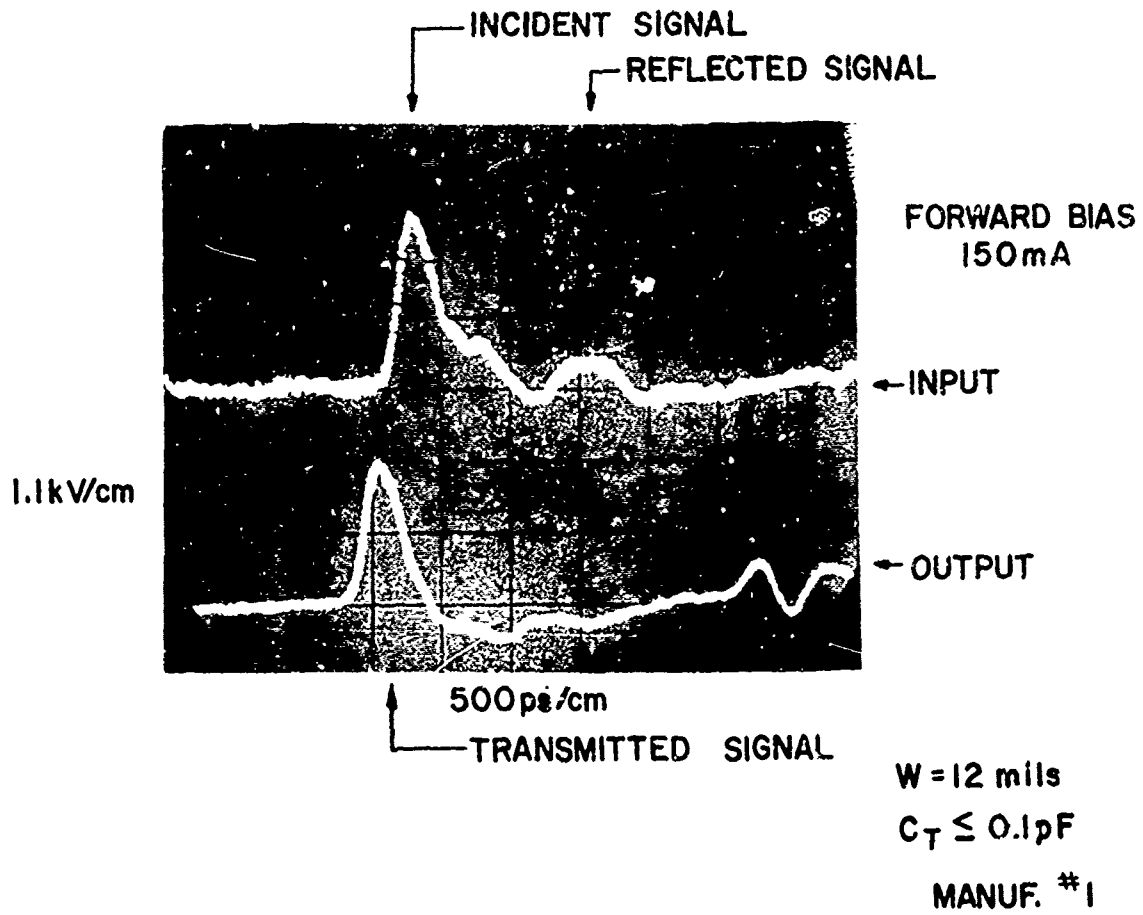
The procedure for measuring the transmission and reflection coefficients is quite straightforward with this set up. The device first is removed from the circuit and a short length of transmission line is substituted. An adjustment of the gain of either of the two oscilloscope channel amplifiers is used to provide equal signal levels from the two samplers. The diode device then is substituted back into the circuit, and direct comparison can be made on the oscilloscope of the incident voltage, the reflected voltage and the transmitted voltage.

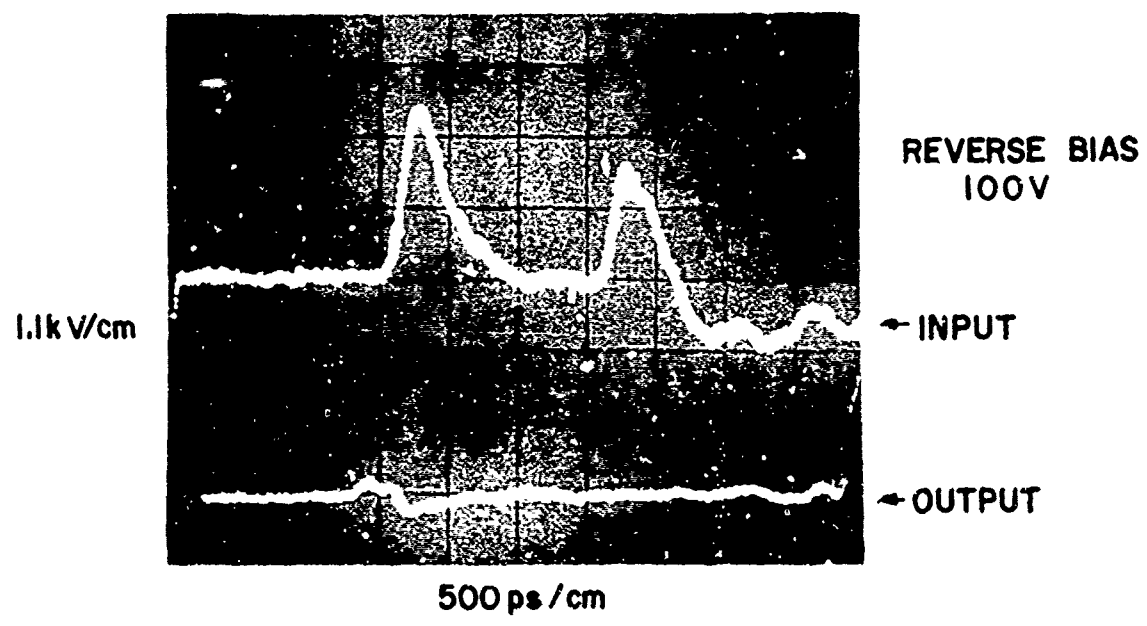
4. SERIES DIODE MEASUREMENTS

Using the measurement procedure described above, the transmission and reflection properties of various diodes were obtained.

Photographs showing the typical reflection and transmission properties of a series mounted diode are presented in Figure 5. All scales are linear. The upper and lower photographs correspond to the forward bias and the reverse bias characteristics respectively. Comparing the two traces in the upper photograph we see that the forward bias insertion loss is 2.0 dB. The slight displacemer of the peak amplitudes between the traces is attributed to a small difference in delay within the measuring system. The small bump in the upper trace 1.5 ns after the incident voltage is due to reflections from the diode. The magnitude of the reflection shown is attributed mostly to the length of gold ribbon which joins the upper contact of the diode to the transmission line. The small peaks in the tail of the output response result from load reflections.

The lower photograph indicates a signal isolation of greater than 22 dB when the diode is switched to 100 V reverse bias. The signal transmitted in the isolation state loses fidelity because of the frequency dependent nature of the diode capacitive reactance. Further, as shown, most of the energy is reflected.





SERIES MOUNTED DIODE TRANSMISSION AND REFLECTION
FIGURE 5

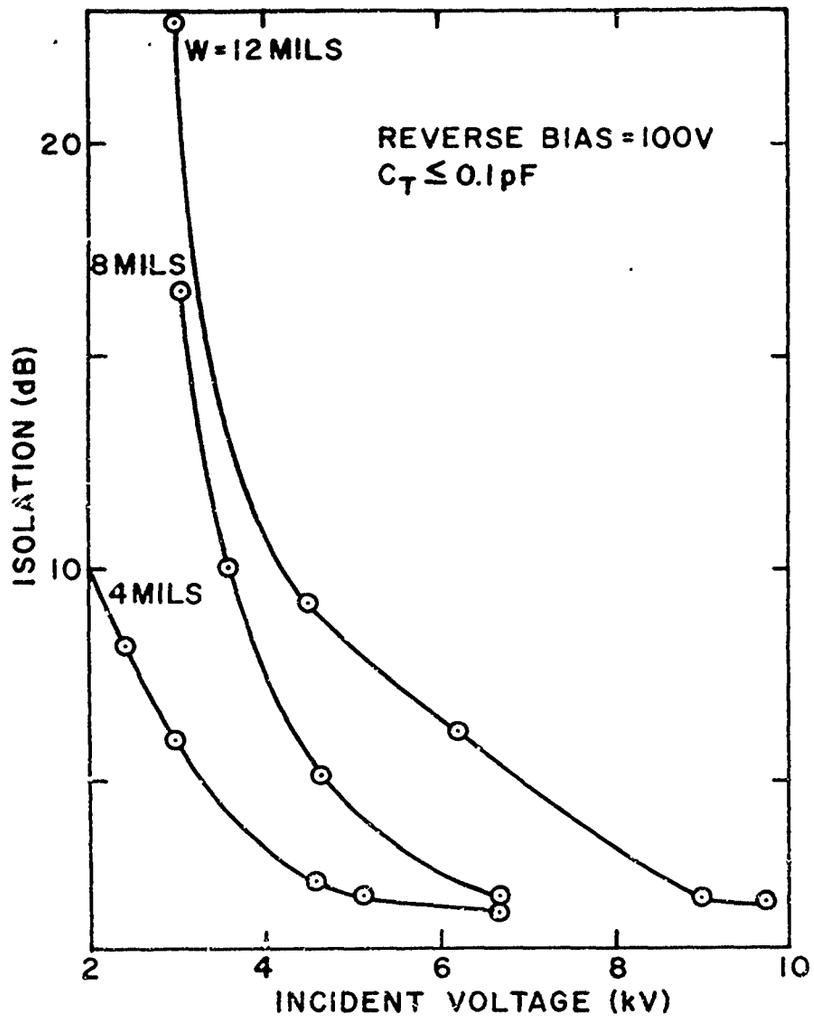
In general, the forward bias characteristics of the diode are found to remain the same for all incident voltage stresses up to 20 kV, the maximum voltage applied. Pulse fidelity is retained and no adverse effects are noted in the transmission properties. However, as the incident voltage is increased, the isolation in the reverse bias state decreases. The point at which this occurs has been found to depend on the I-region thickness of the diode. This is shown in Figure 6 where the reverse bias isolation versus incident voltage is plotted for diodes with different I-region thickness. Generally, the greater the I-region thickness the greater the isolation. However, as indicated from the table of forward bias insertion loss in Figure 6, the series resistance of the diode also increases with I-region thickness. Further, it is found that varying the bias voltage from 0 to 250 V has negligible effects on the diode isolation characteristics. Thus, the reduction in isolation does not appear to be nearly as critically dependent on the width of the depletion region as on the overall I-region thickness.

An effort was made to determine if the observed decrease in isolation was due to surface or bulk resistivity changes. Various diode encapsulants such as Dow Corning 646 were applied to the diodes. Also, the air surrounding the diode was pressurized to 100 p.s.i. None of these experiments appeared to change the isolation characteristics. It therefore seems likely that the mechanism is internal to the diode and not a surface effect.

5. SHUNT DIODE MEASUREMENTS

Experimental measurements were made on various packaged diodes mounted in shunt. Typical transmission characteristics of a shunt mounted diode are shown in Figure 7 for both the forward and reverse bias states. The reverse bias state corresponds to the low loss transmitting mode, which progressivly becomes more lossy as the incident voltage increases. In the shunt configuration, a large change in diode conductance is required before any applicable non-linear effects are observed in the transmission characteristics.

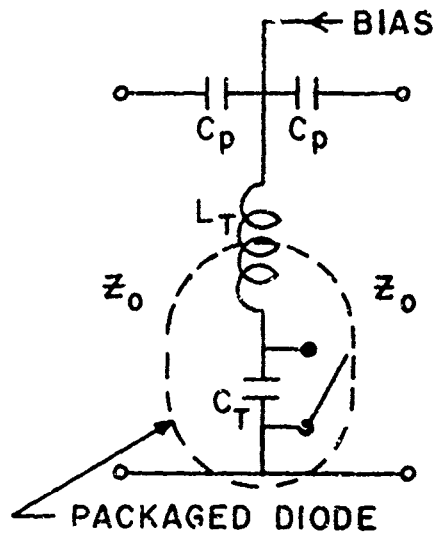
In the forward bias state the isolation is the order of 10 dB. This low value is attributed to the inductance, L_T, which primarily results from the

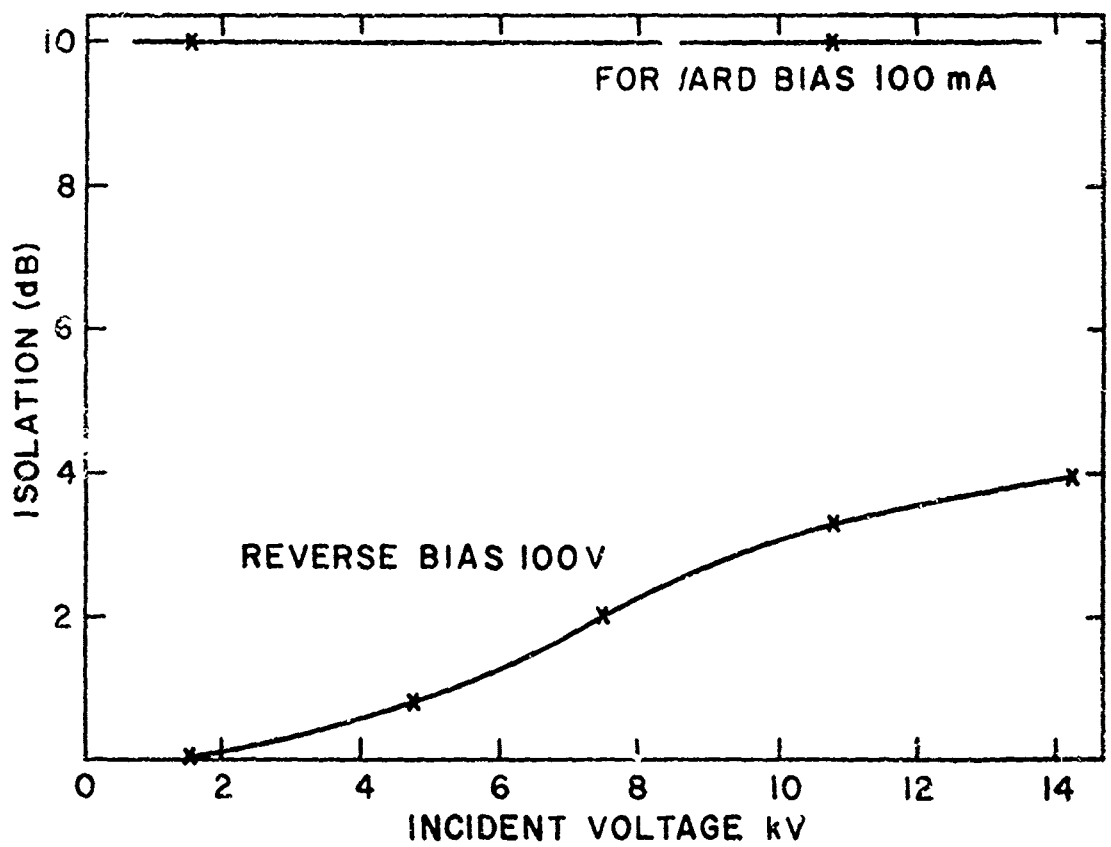


W	FORWARD BIAS INSERTION LOSS
4	0.5 dB @ 100 mA
8	0.55 dB @ 100 mA
12	2.4 dB @ 100 mA
12	2.0 dB @ 150 mA

EXPERIMENTAL SERIES DIODE TRANSMISSION
FIGURE 6

W = 8 MILS
C_T = 0.2 pF
C_p = 5 pF





TYPICAL EXPERIMENTAL CHARACTERISTICS OF A SHUNT PIN DIODE

FIGURE 7

diode package. The isolation could be increased by resonating the parasitic elements. However, this clearly indicates why a packaged diode configuration is unsuitable as a switch function over the multi-octave bands required for short pulse operation.

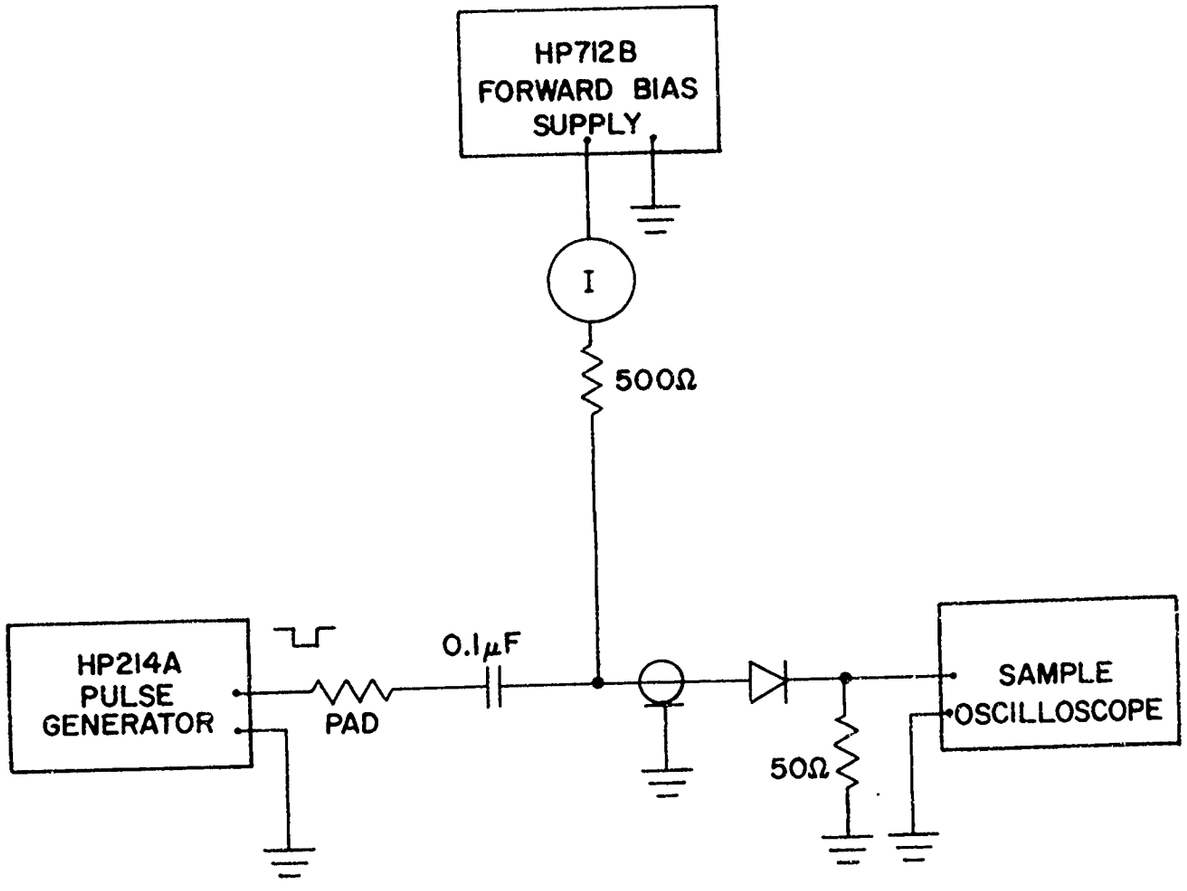
In addition to monitoring the shunt diode transmission characteristics, an effort was made to observe the diode pulse current. This was done by placing a current meter or a current probe in the bias lead. The attempt was not completely successful, since part of the diode current always passed through the by-pass capacitors, C_p. However, by monitoring the portion of the diode current passing through the bias lead, changes in the diode leakage current could be observed as the short pulse voltage stresses were increased. Generally changes in the leakage current could be observed before any noticeable changes in the transmission characteristics occurred. Quite often application of the input signal resulted in permanent deterioration of the reverse voltage leakage current. However, permanent deterioration in the transmission characteristics was not observed. Detailed characterizations of the diode I-V curve, before and after the application of the short pulse stress, were not made.

6. DIODE SWITCHING TIME

The circuit employed for measuring the switching time characteristics of the diodes is shown in Figure 8. The switching time may be defined as the time taken for the diode current to decay from 90% to 10% of the initial current. This is an extremely conservative estimate of the switching time since the rf impedance of the diode changes substantially only near the beginning of the current decay. A summary of the typical switching times of the diodes tested is shown in Figure 9.

7. DIODE CONDUCTANCE

A plot of conductance, G, versus electric field intensity, E, is given in Figure 10 for various PIN diode structures. These curves are derived from the data presented previously in Figure 6 using the assumption of a uniform, ideal parallel plate capacitor field. Below 100 kV/cm the



DIODE SWITCHING TIME MEASUREMENT CIRCUIT

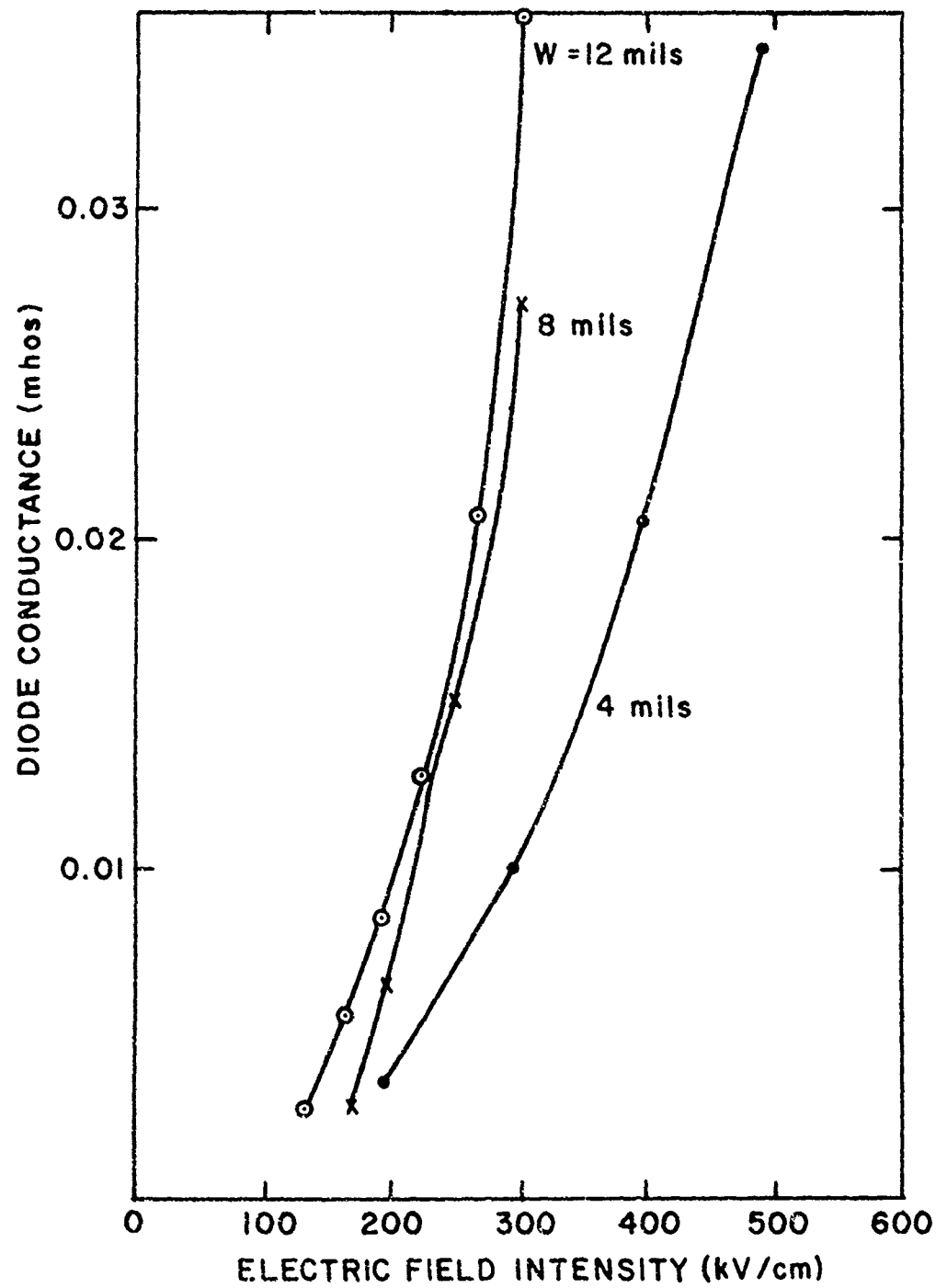
FIGURE 8

MANUFACTURER	C_T (pF)	R_S (Ω) @100mA	W (mils)	t_{fr}* (ns)
1	0.1	12.0	12	230
1	0.1	2.0	8	150
1	0.55	.5	4	50
2	0.65	.5	4	250
3	2.0	1.0	–	1000

*t_{fr} = TIME REQUIRED TO SWITCH FROM A FORWARD BIAS CURRENT OF 100mA TO A STEADY REVERSE VOLTAGE OF 100V. MEASURED FROM THE 10% AND 90% POINTS OF THE TRANSIENT CURRENT WAVEFORM.

TYPICAL DIODE CHARACTERISTICS

FIGURE 9



DIODE CONDUCTANCE VS ELECTRIC FIELD

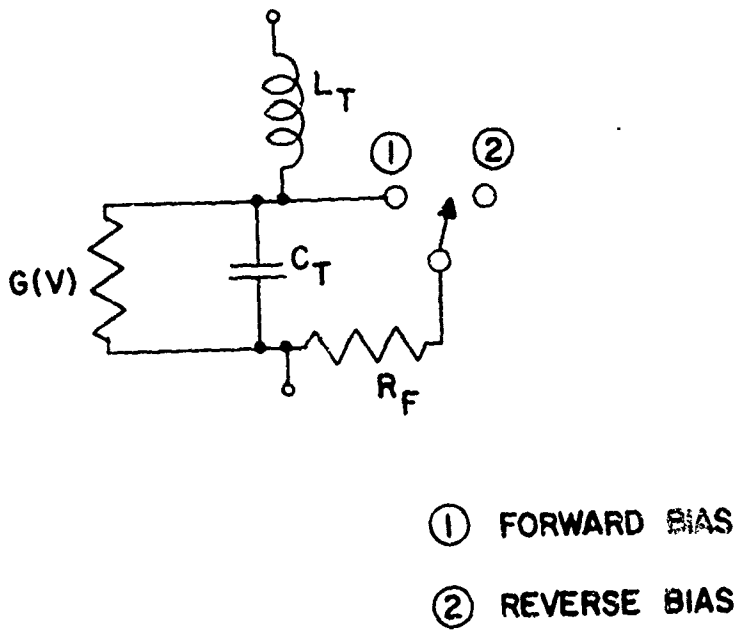
FIGURE 10

conductance falls to the point where the diode capacitive reactance becomes the major impedance to transmission. In the range 100 to 250 kV/cm, the conductance increases rapidly with field and asymptotes to a linear behavior observed in the 250 to 500 kV/cm range. It should be noted that the above behavior is very similar to that observed by J. N. Park, et al.[3] in near-intrinsic silicon using voltage pulses of 20 μs duration. However, the field intensity under short pulse excitation is approximately a factor of 10 greater for the same effects. It appears that under such intense field conditions, electrons and holes that are present in equilibrium in the I-region are accelerated and create additional hole-electron pairs by bulk ionization of the lattice structure. The electron-hole pairs then accelerate and generate further pairs resulting in avalanche multiplication.

8. NEW DIODE EQUIVALENT CIRCUIT

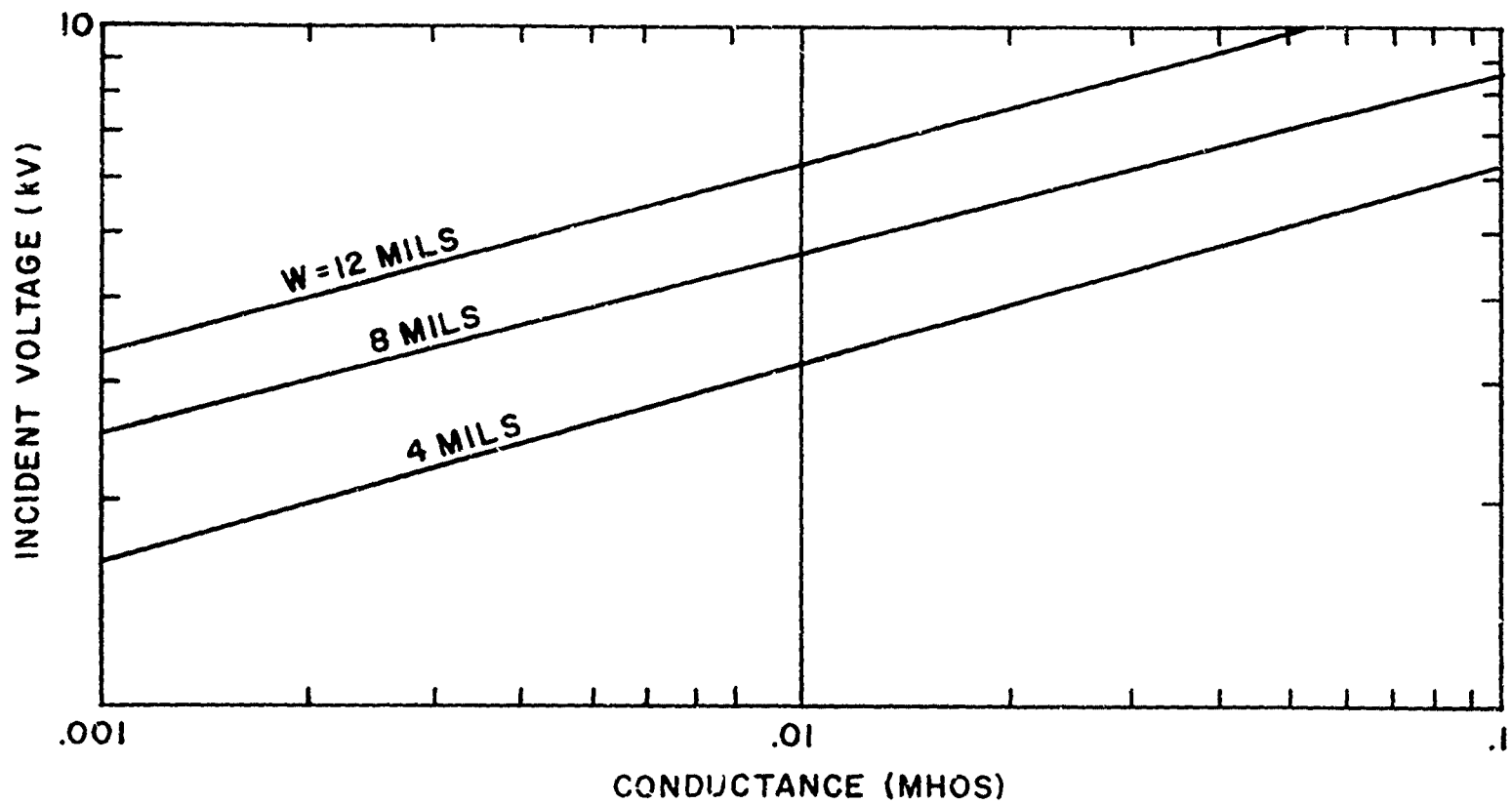
It has been shown that the conductivity of the I-region is highly dependent on the electric field intensity. Thus the reverse bias equivalent circuit of a PIN diode previously presented is inadequate to describe the behavior of the diode under high level short pulse excitation. An alternate simplified equivalent circuit of a reverse biased PIN under short pulse conditions is shown in Figure 11. The capacitive reactance of the diode is shunted by a conductance, G(V), which is a function of the applied voltage.

Since the inductance, L_T, is small for an unpackaged diode, one may neglect L_T and directly relate the conductance to the applied voltage. A summary of the relationship between diode conductance and applied voltage for the various diodes tested is presented in Figures 12 and 13. Note that the data appears to be well defined by the relationship $G = AV^n$.



SHORT PULSE SIMPLIFIED EQUIVALENT CIRCUIT

FIGURE II



INCIDENT VOLTAGE VS. DIODE CONDUCTANCE

FIGURE 12

$G = AV^n$

MANUFACTURER	W (MILS)	n	A (mhos/kvolt)
1	4	3.01	2×10^{-4}
1	8	2.86	3×10^{-5}
1	12	3.04	1.5×10^{-5}
2	8	2.0	1.6×10^{-3}

REVERSE BIAS = 100V
DIODE CAPACITANCE ≤ 0.1 pF

SUMMARY INCIDENT VOLTAGE VS. CONDUCTANCE

FIGURE 13

SECTION III

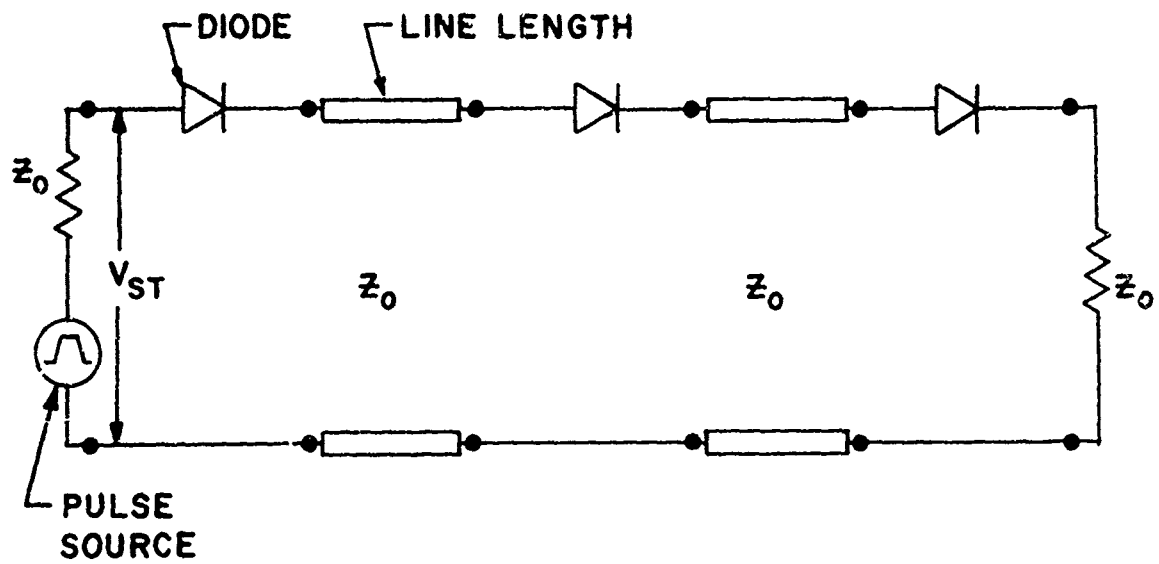
DIODE STACKS

We now turn to a discussion of the theoretical and experimental properties of a stack of closely mounted series diodes in a transmission line.

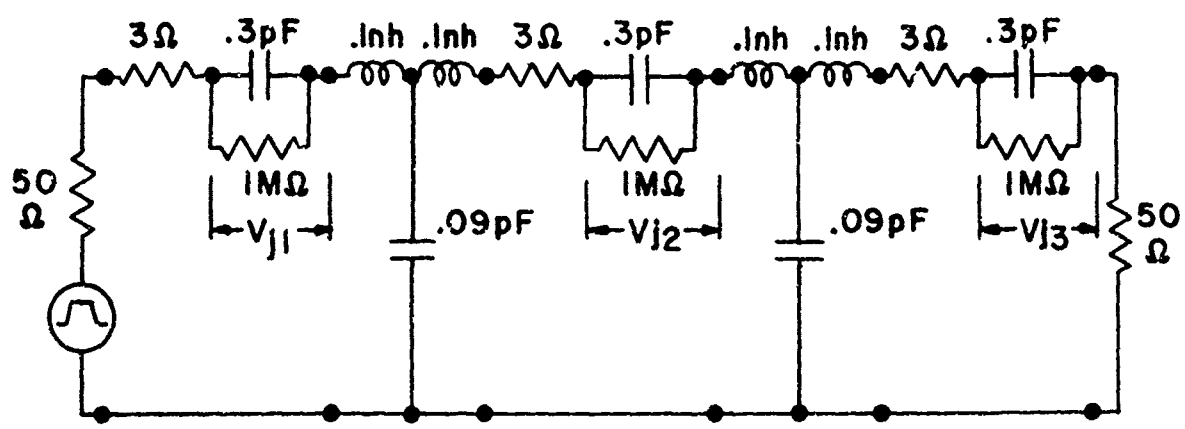
1. ANALYTIC RESULTS

The short time domain signals being considered here present several problems not usually encountered in microwave design. Since the signals being used have transients of well under 100 ps duration, the propagation sequence through a diode stack becomes important. If the diode stacking is to be most effective in reverse bias, it is desirable for the signal voltage to be evenly distributed across all the diodes. With a short risetime on the leading edge of the signal, it is possible that the voltage stress on the first diodes may build to inordinate levels before the voltage wave can propagate across the following diodes in the stack. As shown in Section II, this would significantly increase the conductance of each diode in turn to a higher level than would a more evenly distributed voltage, thereby significantly decreasing the overall isolation capabilities of the stack. To check the possible occurrence of such a "domino" reaction, and to determine the effect of the reverse biased stack on pulse integrity, a time domain transient analysis was carried out.

A computer circuit analysis program was utilized to examine stack properties. The program performs a linear transient pulse response analysis on a simulated diode stack. The three diode series arrangement chosen for analysis is represented by the circuit shown in Figure 14. The source pulse is represented by 50 ps linear rise and fall times separated by a 150 ps constant amplitude, for a total duration of 250 ps. The three reverse biased diodes are each represented by a 0.3 pF capacitor with a 1 Mohm resistor in shunt and a 3 ohm resistor in series. The diodes are separated by 0.050" lengths of 50 ohm air line which are simulated by low pass LC filter structures. It should be noted that the program is not capable of performing the non-linear transient analysis required if the 1 Mohm shunt resistor were to be a function of the input voltage, V_{st}.



(A) THREE DIODE STACK



(B) LUMPED EQUIVALENT CIRCUIT (DIODES REVERSED BIASED)

STACK EQUIVALENT CIRCUIT

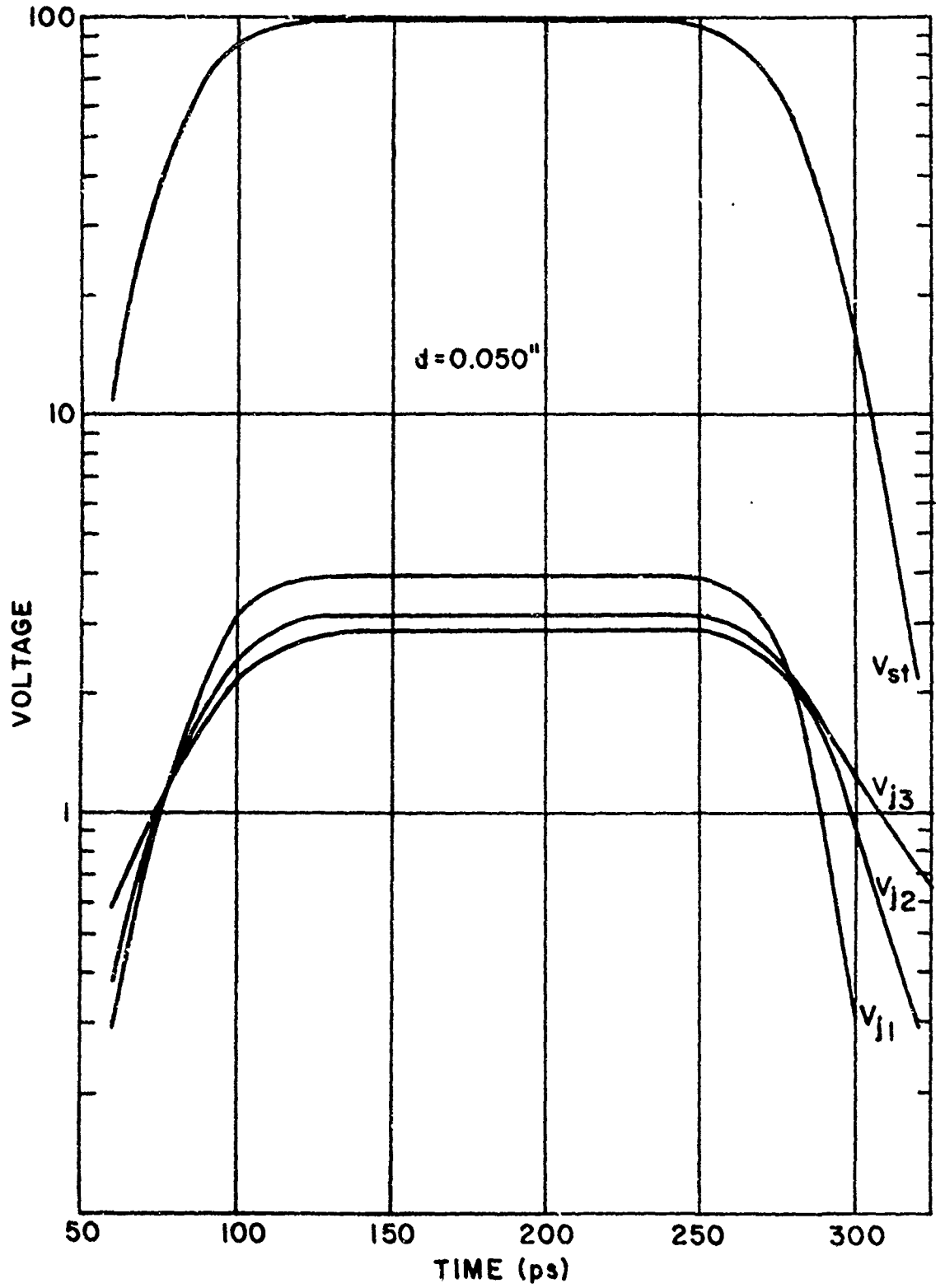
A typical result of the analysis using 20 harmonics of the pulse source, is shown in Figure 15. The voltages, V_{j1}, V_{j2}, V_{j3}, across each diode junction are compared with the incident stack voltage, V_{st}. As expected the greatest voltage stress occurs on the first diode in the stack. In this case 40% of V_{st} develops across the first diode junction. The risetime of the pulse is limited by the time constant of the source. In general, as the distance between the diodes is decreased, the difference in the junction voltages tends to zero. With no spacing between the diodes the stack voltage is equally distributed between the diodes. Clearly, in practice the diodes should be spaced as close together as is practical. The small spacing at which appreciably uneven distribution of voltage occurs further suggests the advantages of utilizing unpackaged diode chips.

2. EXPERIMENTAL RESULTS

During the development of the series diode stacks, units were built containing from two to eight diodes. The configurations were simple extensions of the stripline fixture used to test single series diodes, with the addition of sufficient 0.025" wide transverse slots across which to mount the additional diodes.

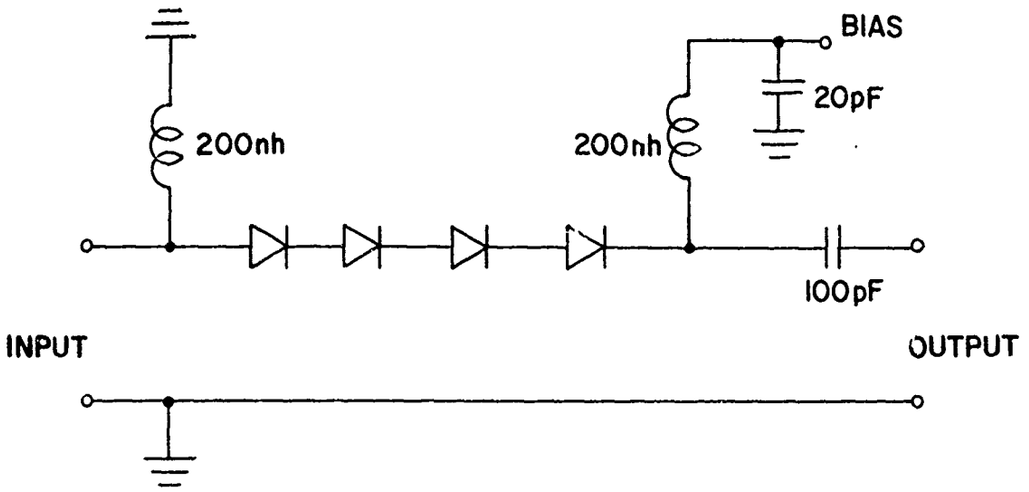
The two circuits used to bias diodes in the stack are illustrated in Figure 16. The single feed bias structure is identical to that used in the single diode series test fixture. Being relatively simple to construct, this structure was used for most of the diode stack characterization. However, biasing the diodes in series significantly increases the switching time. To achieve fast switching,especially from forward bias to reverse bias, the multi-feed parallel bias structure illustrated in Figure 16B is necessary.

Some typical incident and reflected signals from a series stack of four, 8 mil I-region diodes are shown in the photographs of Figure 17. The incident voltage is 9.7 kV. When the diodes are forward biased at 100 mA, a small reflected signal is just visible 3.2 ns after the incident signal. On the other hand, most of the signal is reflected by the diodes when they are reverse biased, as illustrated in the lower photograph. The total reverse bias voltage across the four diodes is 100 V. The signal occurring

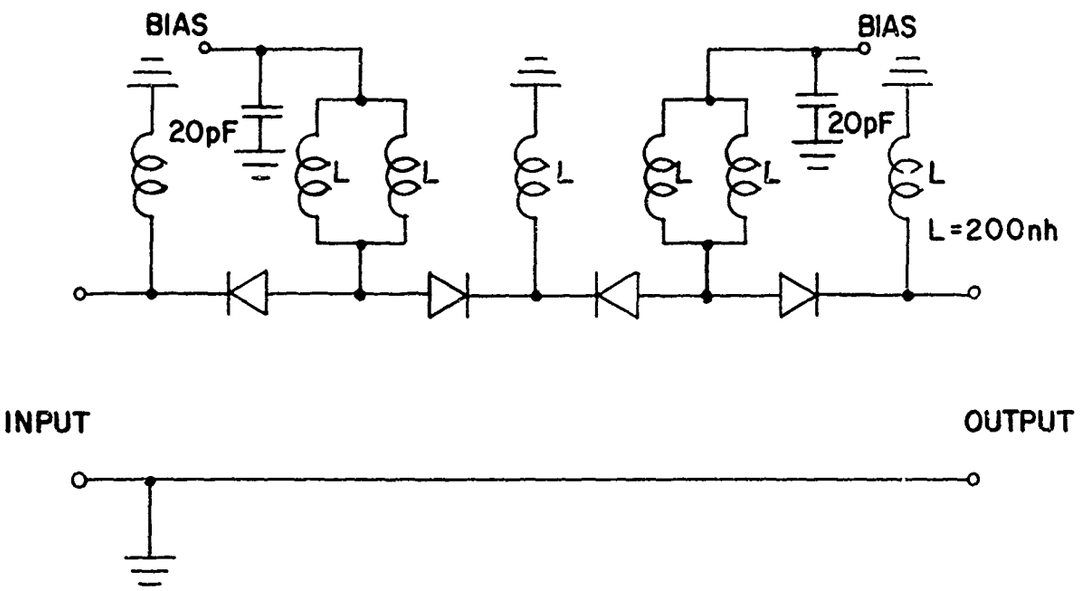


THEORETICAL STACK VOLTAGE STRESS

FIGURE 15



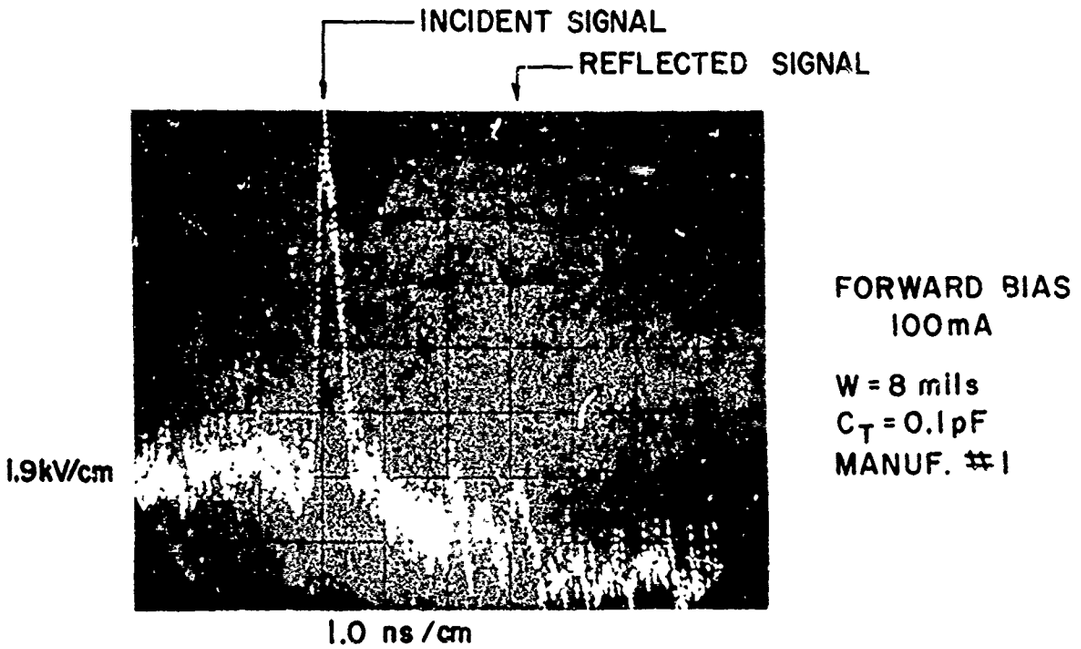
(A) SINGLE FEED BIAS STUCTURE.

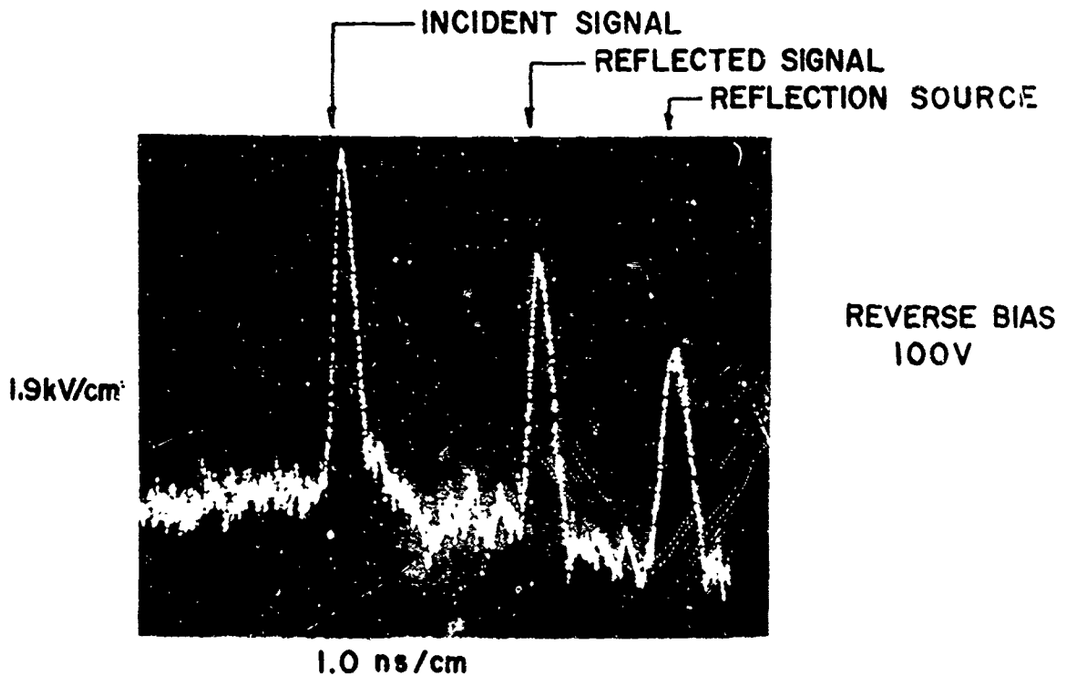


(B) MULTI-FEED BIAS STRUCTURE.

DIODE STACK CIRCUIT DIAGRAM

FIGURE 16





FOUR DIODE STACK INCIDENT AND REFLECTED SIGNALS

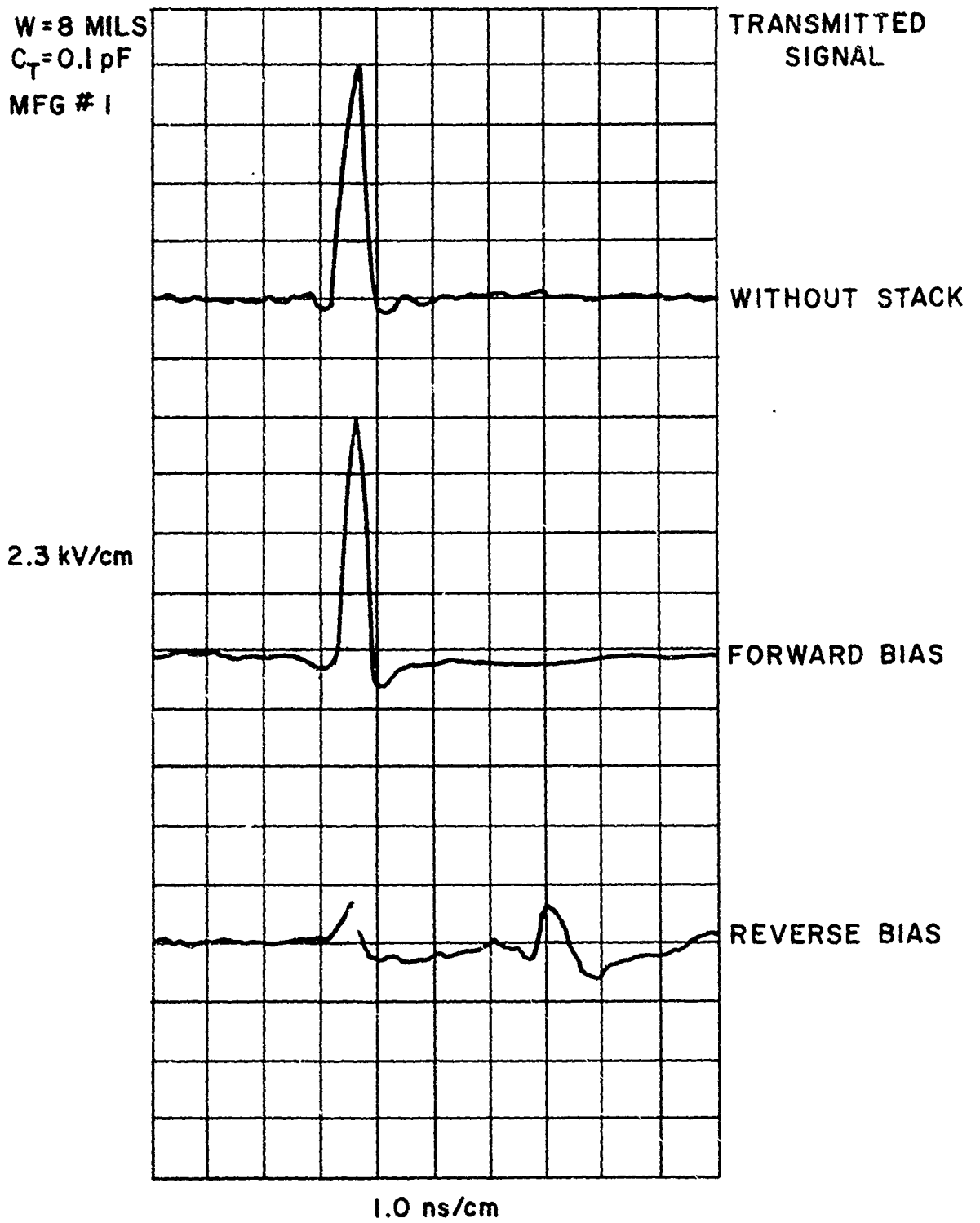
FIGURE 17

a short time after the first reflected signal is due to a second reflection, this time from the source generator. The corresponding transmitted signals through the four diode stack are presented in the reconstructions of Figure 18. There is good pulse fidelity through the forward biased diodes, as illustrated by a direct comparison of the transmitted signal with and without the diodes in the circuit. The forward bias insertion loss can be seen to be 2.4 dB, while the difference between the forward and reverse bias transmission is approximately 10.0 dB.

The 100 V reverse bias to 100 mA forward bias switching speed of the four diode stack using the single feed bias structure is approximately 400 ns. Longer switching times (15 μs) result in switching from forward bias to reverse bias. This occurs because in a series stack, the first diode to switch presents a high impedance path which slows removal of the stored charge from the other diodes. It has been found that using the parallel feed bias structure results in the switching times being less than 500 ns in switching from either bias state.

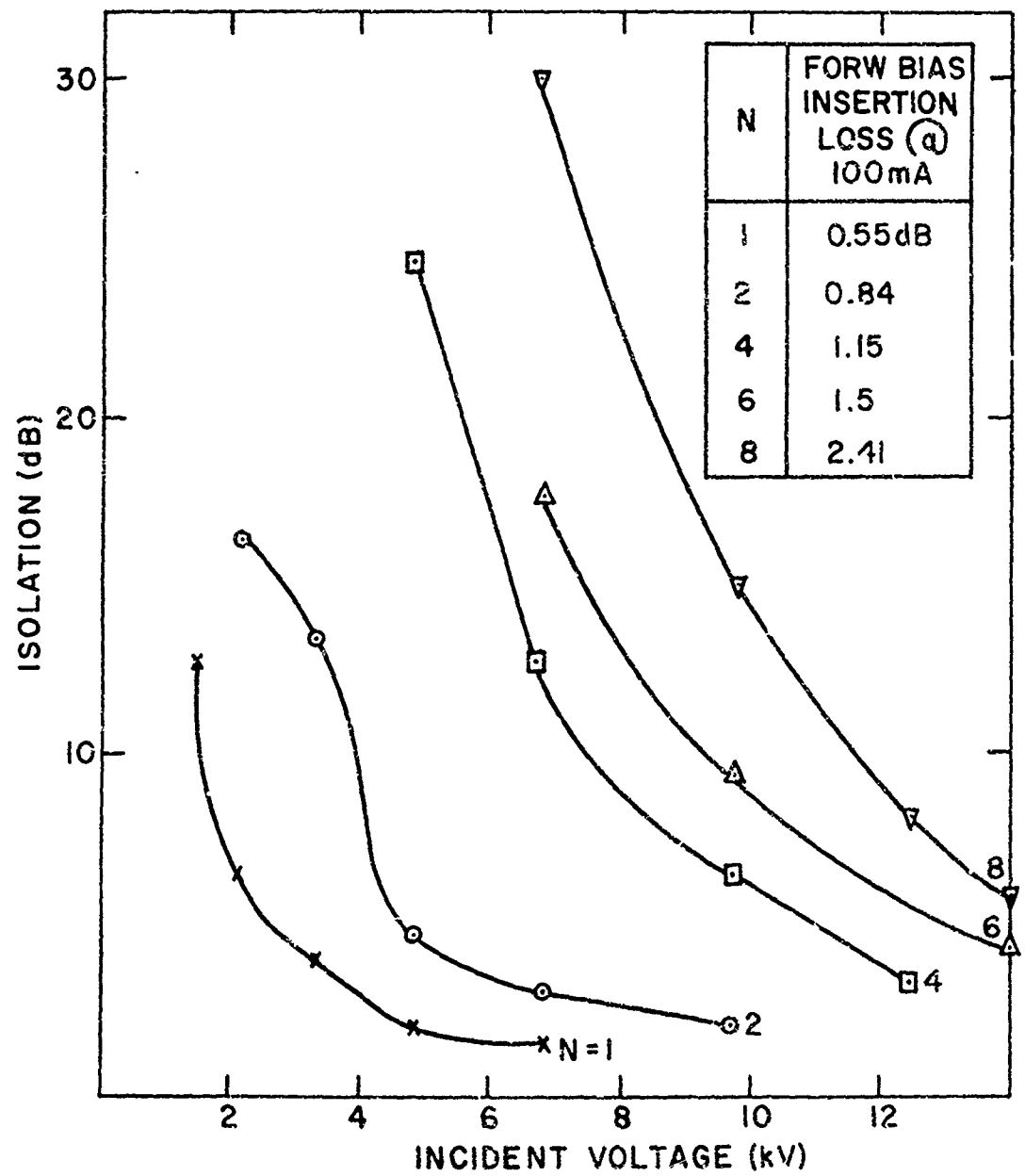
The transmission characteristics of various stacks containing up to eight diodes are presented in Figures 19A and 19B. All the data presented are for nominally 8 mil thick I-region diodes. However, differences in I-region thickness appear to exist between various manufacturers. This is evidenced by comparing the isolation and the forward bias insertion loss in the two figures. The isolation as plotted is simply the difference in insertion loss between the forward biased and reverse biased stack. In general the greater the number of diodes in the stack, the greater the isolation when the diodes are reverse biased. However, as expected, more diodes result in greater insertion loss when the diodes are forward biased.

The isolation obtained from a multiple diode stack is less than that predicted from data obtained from a single series diode characteristic. The calculated theoretical isolation versus incident voltage for various size diode stacks is shown in Figure 20. Note that although the theoretical curves have the same characteristic shape as the experimental data, the isolation does not decrease as rapidly with increasing incident voltage. This discrepancy is probably due to the inadequacy of the theoretical



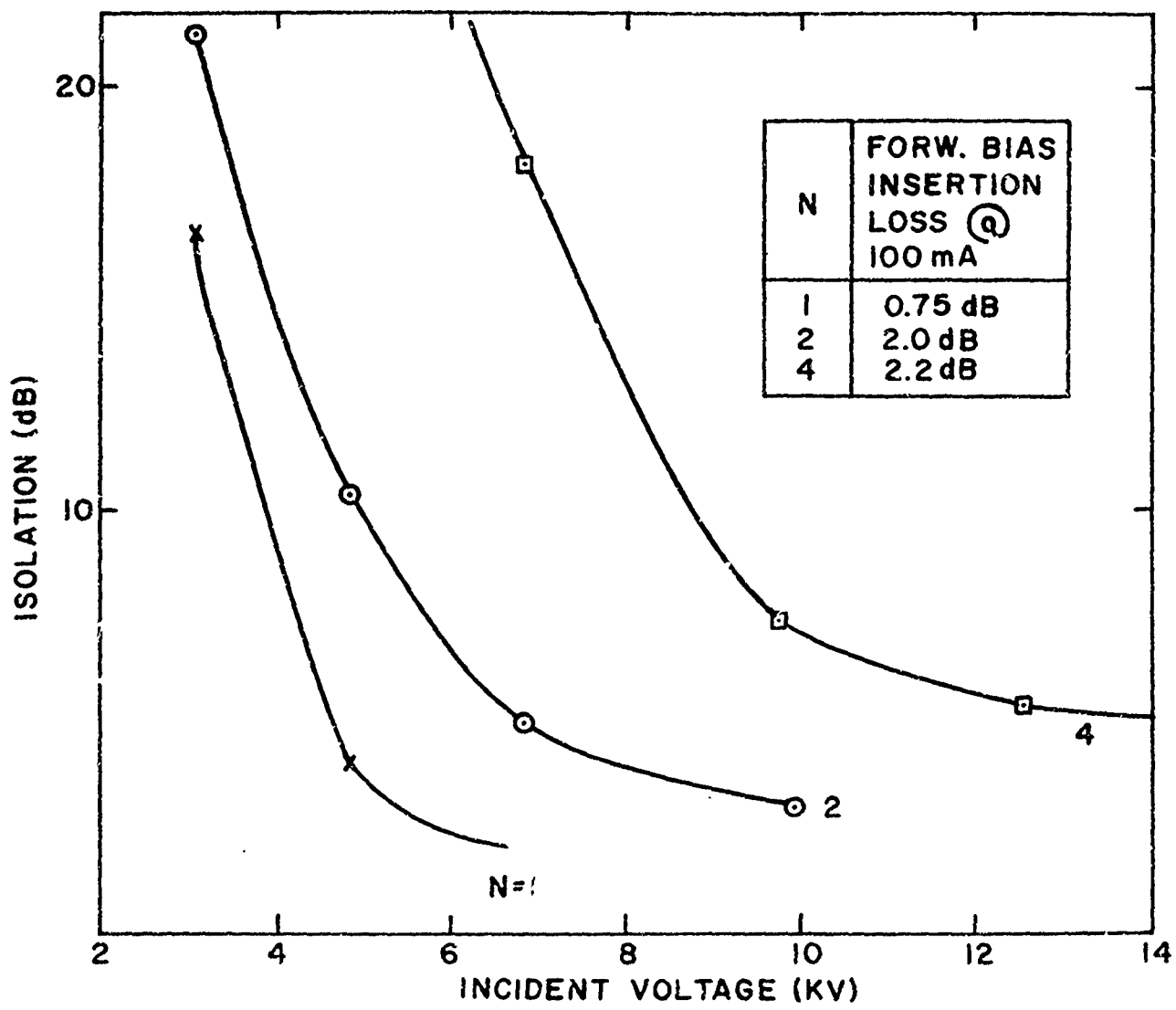
FOUR DIODE STACK TRANSMISSION

FIGURE 18



EXPERIMENTAL STACK ISOLATION VS INCIDENT VOLTAGE—MANUFACTURER # 2

FIGURE 19A



EXPERIMENTAL STACK ISOLATION VS. INCIDENT VOLTAGE-MANUFACTURER #1
FIGURE 19B

$$\text{ISOL.} = 10 \text{ LOG.} \left\{ \frac{(2Z_0G+N)^2 + (2Z_0\omega C)^2}{(2Z_0G)^2 + (2Z_0\omega C)^2} \right\}$$

$G = 1.6 \times 10^{-3} \left(\frac{V}{N}\right)^2$ (mhos)

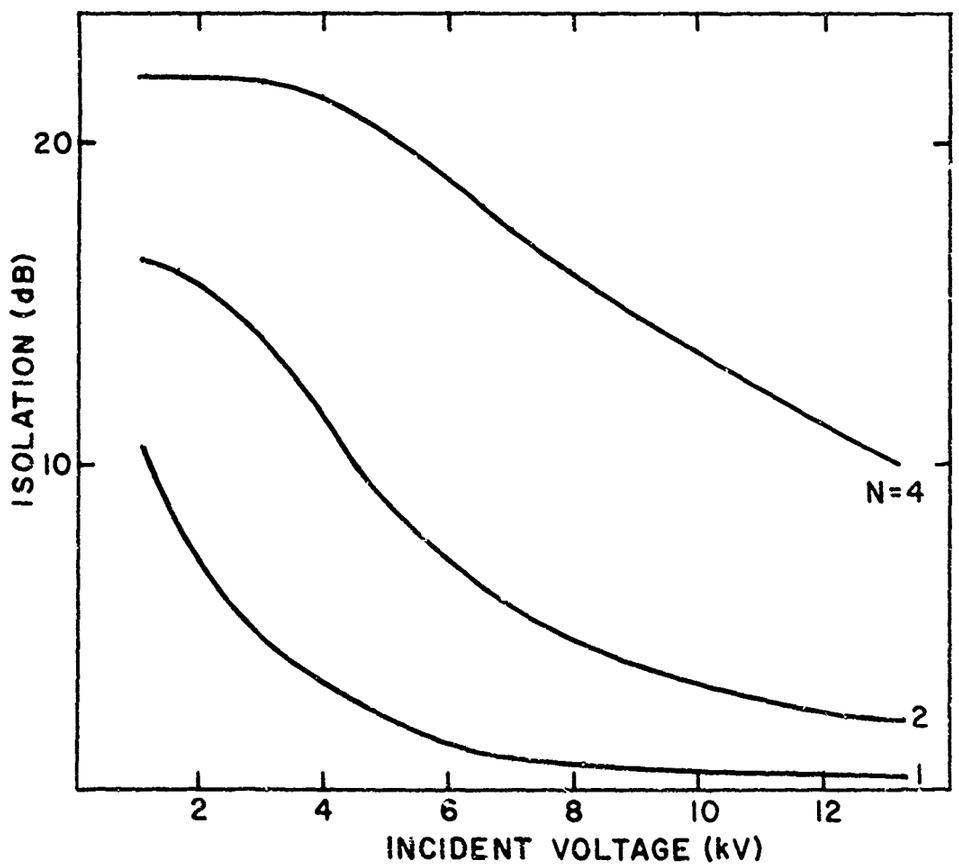
N = NUMBER OF DIODES

V = INCIDENT VOLTAGE (kV)

C = 0.1 pF

$Z_0 = 50\,\Omega$

$f = \frac{\omega}{2\pi} = 5\text{GHz}$

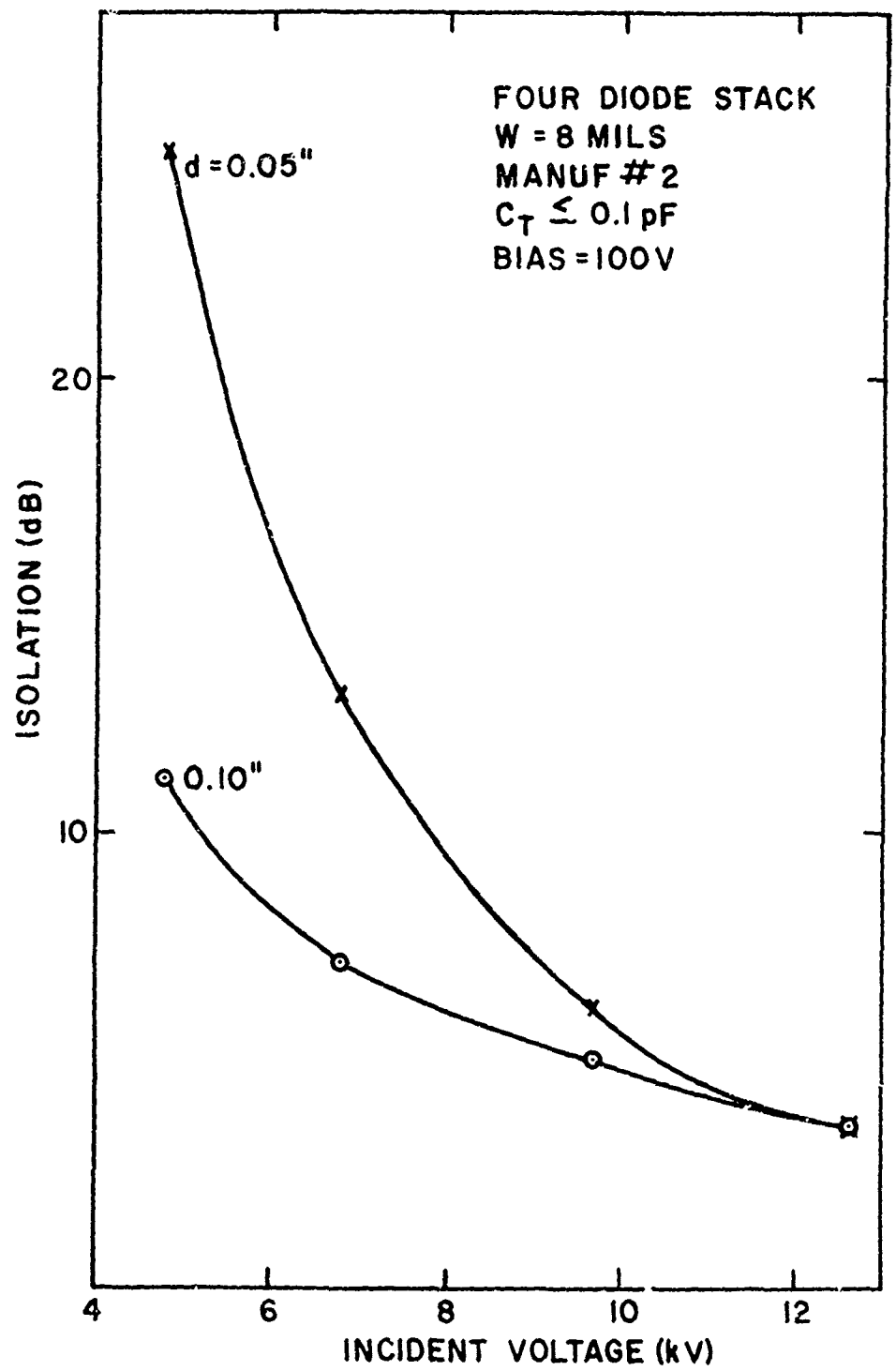


THEORETICAL STACK ISOLATION VS INCIDENT VOLTAGE

FIGURE 20

model which does not account for the varying voltage stress between the individual diodes in the stack.

Considerable experimental effort has been expended in investigating the diminished isolation characteristics of diode stacks as the incident voltage is increased. It is found that the spacing between the diodes in the stack must be made as small as possible. This is illustrated in Figure 21 where the isolation versus incident voltage of a four diode stack is compared for various diode spacing. In addition a circular ground shield (0.120" dia) was placed around the diodes to inhibit any spurious moding which may occur. Since no appreciable change was noted, it is concluded that moding is not the cause of the observed diminished isolation.



ISOLATION VS. INCIDENT VOLTAGE FOR VARIOUS DIODE SPACING

FIGURE 21

SECTION IV

THE SPDT SWITCH

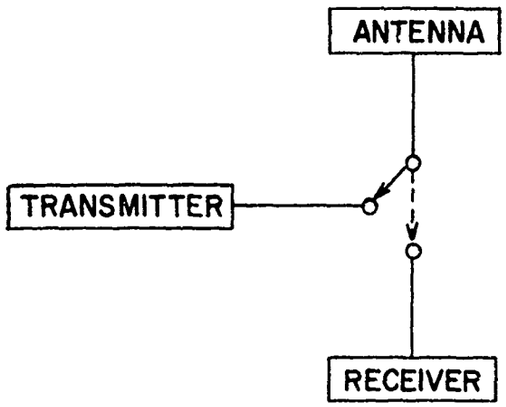
Investigation to this point has given insight into the short pulse switching characteristics of individual PIN diodes and diode stacks. It now is of interest to briefly investigate the performance of such diodes within a single-pole-double-throw (SPDT) switch.

1. SWITCHING CONFIGURATIONS

One of the more important uses of an SPDT switch is as the basis for a short pulse duplexer, the block diagram for which is indicated in Figure 22. Toward this end, there are several possible series and parallel diode configurations which can be considered. Figure 23 shows five of them, with X, R and A denoting transmitter, receiver and antenna terminals respectively. Of the five, the configurations shown in Figure 23 b and c are inappropriate to short pulse signals because of the particular use of shunt elements. With a steady state signal, such elements can be positioned to turn the closed line section into a quarter wave shorted stub in parallel with the open section of the line. However, the short pulse signals considered here are highly transient. Hence, the presence of a shorted stub would cause distortion of the input pulse in the form of echos. Moving the diode closer to the junction to reduce the echos would effectively short out the line.

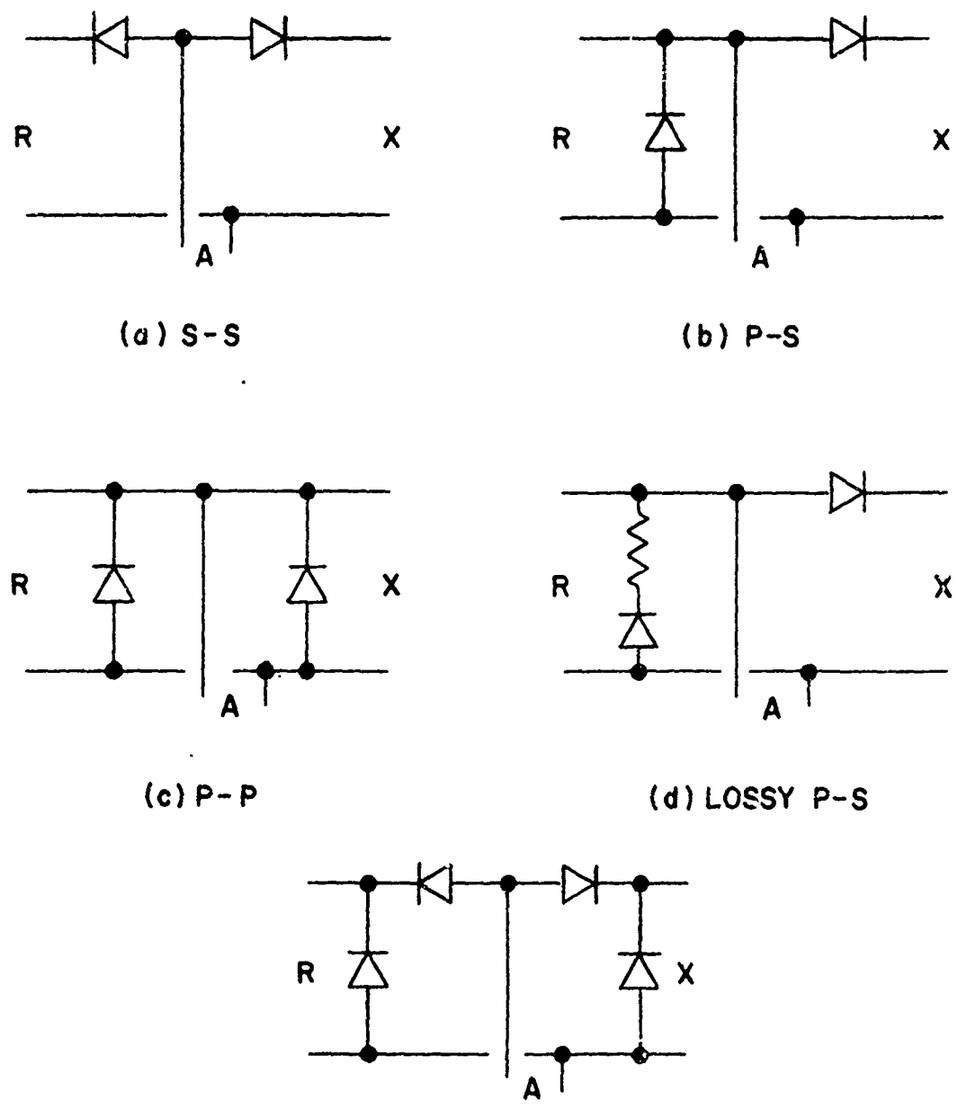
The configuration of Figure 23d is intended to isolate R by presenting a matched resistive termination when the shunt diodes are in forward bias. In reverse bias, the shunt diode capacitance must be low so as to minimize dispersion or insertion loss to R. However, the sacrifice of half power during transmit as well as the loss and dispersion during receive, make this approach undesirable.

The most promising configurations are those in Figures 22 a and e. Key to both, are the series diodes which function to isolate the closed line from the open line without causing transient signal distortion. Nevertheless, the data of Section III shows that for acceptable forward bias insertion loss,



BASIC DUPLEXER FUNCTION

FIGURE 22



SPDT SWITCH CONFIGURATIONS

FIGURE 23

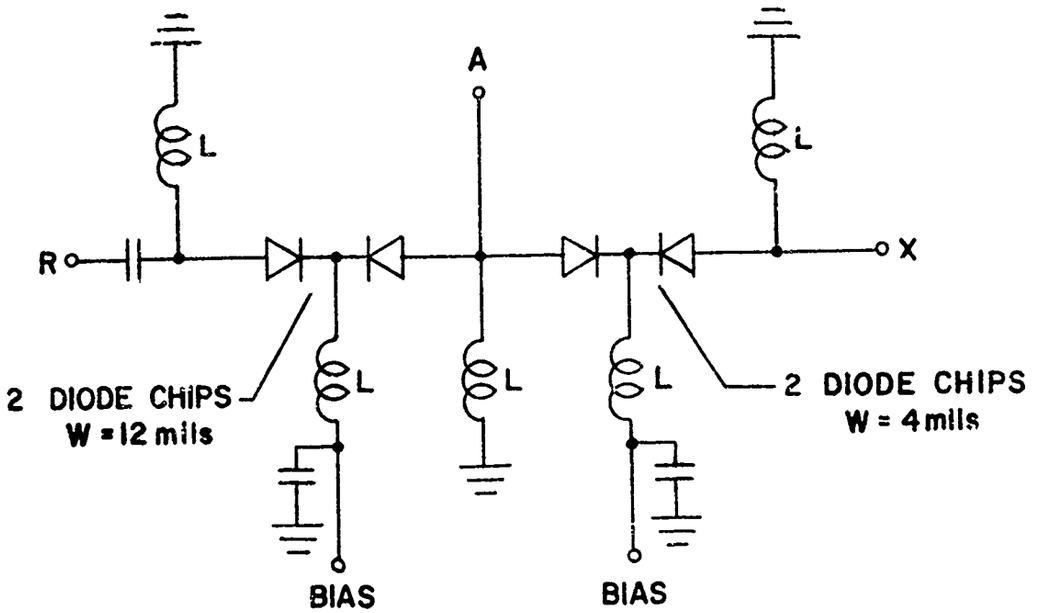
the reverse bias isolation of a series stack may not be sufficient for some requirements e.g., 60 dB for 10 kV input. In such a case, isolation can be brought to an acceptable level by following the series stack with one or more forward biased shunt diodes. In this case, the disruptive effects of signal echoes are minimized by the isolation resulting from two signal passes across the reverse biased series stack, and the superior isolation properties of shunt diodes can appropriately be used.

Two characteristics of a duplexer are to be considered when choosing an SPDT configuration. The first is that the power involved in the receive mode is much less than that in transmit. Thus the series diodes in the X branch, which are in forward bias during transmit, need not be as voltage resistant at the ones in the R branch. Also, the isolation requirements for the X branch during receive need only be enough to insure signal integrity into the R branch. Thus shunt diodes in the X branch may not be necessary.

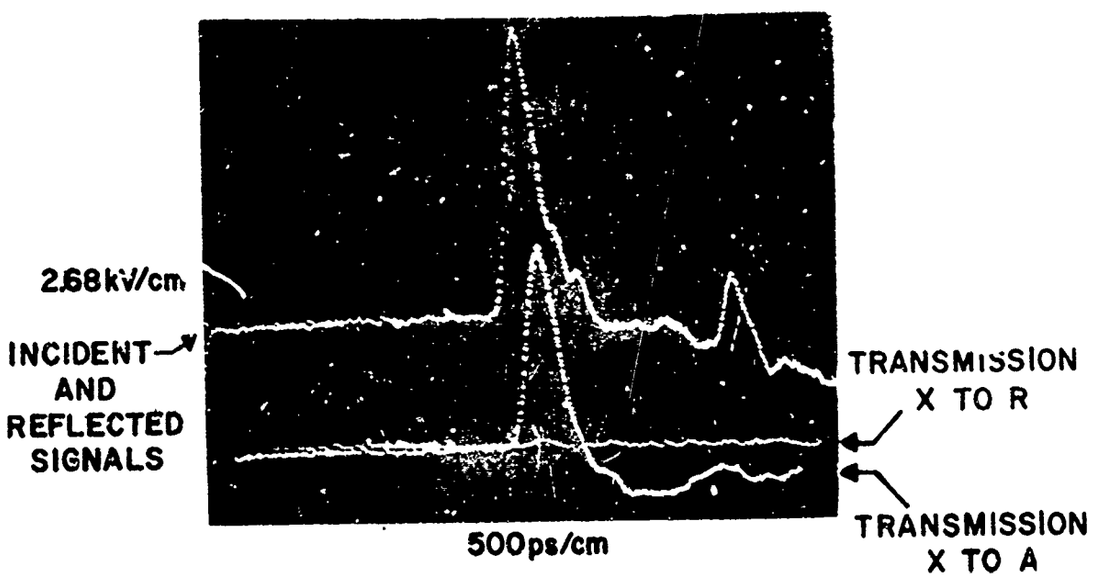
2. SPDT MEASUREMENTS

The SPDT configuration chosen for fabrication and measurement is one containing only the key series elements, corresponding to Figure 23a. A circuit diagram of the actual arrangement is shown in Figure 24a. In accordance with the above discussion, the two diodes in the R branch have 12 mil I-regions, while those in the X branch have 4 mil I-regions. As with the diode stacks discussed in Section III, they are mounted back-to-back in pairs within a 50 ohm stripline. There is a separate bias input for each pair. No attempt was made to tune or optimize the circuits. The diodes used were chosen for availability rather than design preference (8 mil I-region).

Figure 24b shows some of the performance characteristics of the SPDT switch. During the measurements the X to A channel was open. Thus the R branch diodes are in reverse bias (100 V) while the X branch diodes are forward biased (150 ma). The incident signal peaks at 12 kV. The signal appearing at the antenna terminal is a good replica of the input, but is down by some 3 dB. 0.4 dB of this is accounted for by the reflected signal appearing 1.7 ns after the incident signal. The other 2.6 dB is most likely lost in transit through the two X branch diodes, since a negligible signal



(A) CIRCUIT DIAGRAM



(B) SPDT SWITCH CHARACTERISTICS

A BREADBOARD SPDT SWITCH

FIGURE 24

appears at the receiving terminal. The R branch is isolated by better than 25 dB, which is much greater for an equivalent input than that observed in the simple series stack as presented in Figures 19A and B. This results from the reduced voltage stress on the reverse biased diodes in the SPDT switch configuration. It should be mentioned that the relatively high forward bias insertion loss, which also appears in the opposite polarity across the R branch diodes, results from temporary unavailability during the experiment of the better performing diodes described in Section III. Switching speeds for both states are less than 400 ns.

The response of the switch is considered quite promising. With a better choice of available diodes and after some optimization work on the circuit, it is felt that appropriate R branch isolation can be maintained with much less insertion loss and better transmission characteristics. Switching times also can be improved. Thus the realization of a PIN diode short pulse duplexer appears to be well within the range of accomplishment.

SECTION V

SUMMARY AND CONCLUSIONS

1. DIODE CHARACTERIZATION

Experimental results have been obtained showing the characteristics of various types of PIN diodes when subjected to short pulse high voltage stresses including switching in both shunt and series configurations. Single diode elements have been subjected to voltage stress levels of greater than 10 kV without failure. In general, it is found that series diodes transmit a faithful replica of the incident signal in the forward bias state, while in reverse bias, the diodes tend to isolate the incident signal from the output terminals. However, high incident fields tend to increase the conductance through the diode. The conductance has proved to be a function of diode geometry, in particular the thickness of the intrinsic region. The relationship between conductance and the impressed short pulse electric field is established. In the range 100 to 250 kV/cm the conductance increases rapidly with electric field and asymptotes to a linear behavior in the 250 to 500 kV/cm range. It is noted that this behavior is very similar to bulk ionization effects observed in near intrinsic silicon, however the short pulse electric field needed for similar effects is approximately a factor of 10 greater. Based on the results, a new equivalent circuit model of the reverse biased diode with voltage variable conductance is found to be necessary for short pulse design applications.

The investigation also identified coax-to-stripline adaptors (1.2 VSWR) and bias coupling structures which are suitable for use with 20 kV, 150 ps pulse signals.

2. DIODE STACKS

Both the theoretical and the experimental properties of a stack of diodes, series mounted relatively close together in a transmission line, were investigated. The theoretical and experimental results indicate the necessity for close diode-to-diode spacing to minimize the applied signal voltage stresses on the diodes. Experimental results from stacks containing from

two to eight diodes were obtained. Good transmission fidelity is demonstrated, and it is found that stacking enhances the isolation. For example, a four diode series stack using nominal 8 mil I-region thicknesses, with diode capacitances of 0.1 pF and diode spacing of 0.050" when subjected to a 10 kV input is found to have an insertion loss of 2.4 dB and an isolation of 10 dB. Other units with the same nominal I-region thickness are found to have less isolation but lower insertion loss. These variations can probably be attributed to non-uniformity of I-region thickness measuring techniques.

3. SPDT SWITCH

Various SPDT switch structures have been examined and it is concluded that the series stacking configuration is necessary for good short pulse operation. Therefore, an SPDT switch using series diode stacks was designed and a breadboard model fabricated. The initial test results are quite promising indicating maximum insertion loss of 3 dB and minimum isolation of more than 25 dB at 10 kV input signal. The switching speeds of the diodes are less than 400 ns. These preliminary results were obtained without any adjustments being made to the device. Based on the diode characterization study it is predicted that a much lower insertion loss device can be obtained using available diodes with thinner I-regions than the 12 mils used.

SECTION VI
RECOMMENDATIONS

During the program, individual PIN diodes were investigated as control elements for high peak power, sub-nanosecond duration, impulse type signals. Series stacks of diodes were also investigated for the same purpose as were SPDT switch configurations of such stacks. The results show that PIN diodes will not only survive the signals, but individually and in stacks they make appropriate design elements for signal control. A new equivalent circuit representation is defined and a functional and optimum set of specifications has been identified for such purposes from among available production diodes. Experiments with a non-optimum breadboard SPDT switch, show that applications are not only feasible, but are well within range of successful implementation. Thus it is recommended that work on implementation and improvement continue toward a useable capability. Several areas of logical follow-on are suggested.

A. Duplexer

With the experience gained through the present program, SPDT switch performance can be improved and optimized for short pulse applications. It therefore is recommended that further switch development be pursued with emphasis on meeting necessary performance specifications and on realizing a complete, working PIN diode short pulse duplexer. Work also should be done to develop a switch driver to control the duplexer/transmitter sub-system.

B. Semiconductor Switch Structure

Theoretical and experimental work should be performed to better characterize the behavior and mechanisms of diode stacks. To broaden capabilities for controlling high peak power, short pulse signals, semiconductor devices in addition to PIN's should be investigated as switching elements appropriate to various configurations.

C. Diode Long Term Effects

No irreversible changes occur in the switching or transmission properties of PIN diodes with application of high voltage short pulse signals. However, irreversible changes are observed in the diode reverse leakage current. This suggests that some emphasis be placed on determining the long term effects on semiconductor elements subjected to short pulse voltage stresses. Both operational mechanisms and failure modes should be identified as functions of element design. Failure rates should be established.

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