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INVESTIGATION OF SILICON CARBIDE (SiC) GUN-ELECTRON-INDUCED-SEMICONDUCTOR-HYBRID-AMPLIFIER (GEISHA) DIODE FEASIBILITY AND FABRICATION

by

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1. INTRODUCTION

The device potential of silicon carbide (SiC) Gun-Electron-Induced-Semiconductor-Hybrid-Amplifier (GEISHA) diode targets is very favorable relative to silicon. The Johnson figure of merit (power-frequency-impedance product) for SiC was estimated to exceed Si by more than a factor of 50. Additionally, SiC has a threefold higher thermal conductivity than Si and could be operated to 500°C. The purpose of this initial study was to evaluate the feasibility and fabrication of a SiC GEISHA diode. As will be evidenced in the report, values for carrier velocity and critical field largely confirm theoretical prediction and the practical feasibility of Schottky barrier diodes of SiC substrates has been demonstrated. A background review of GEISHA operation and material parameters of interest is included in Section 2 and Appendix A, for readers unfamiliar with the device.

2. TECHNICAL BACKGROUND

2.1 GEISHA OPERATION

In the simplest form, the hybrid amplifier (GEISHA) consists of an electron beam source (together with accelerating potential), a beam modulator (intensity or deflection), and a reverse-biased semiconductor target. An effective current gain is obtained when a modulated beam of electrons, which has been accelerated to a potential of 10 to 25 kV, is directed at the target, normally at the semiconductor junction face. If the metal contact is sufficiently thin so as to be transparent to the electron beam, the semiconductor is bombarded with high energy electrons. Part of this beam energy may be dissipated in the process of electron-hole pair creation by exciting valence band electrons into the conduction band. The penetration depth of electrons is dependent on the density of the material and the initial electron energy.

Furthermore, if the carriers are created in a region of high electric field, they separate rapidly before recombination can take place. For an n-type depletion region, electrons will be swept across this region at hot carrier velocities, forming the carrier current. Therefore, under the condition of zero trapping, one electronic charge is collected in the load circuit for each electron-hole pair created and the current gain of the device is the electron beam induced current (EBIC) gain of the material. For silicon, this can be quite significant; 2,000 or more for an electron beam energy of 10 keV.

Obviously, a material with a narrow bandgap is desirable from a current gain point of view, although in most materials this inevitably leads to low avalanche ionization energy and hence low breakdown voltage. The effective voltage output is consequently limited, since the field in the drift region begins to collapse as the output voltage approaches the bias voltage.

A similar collapse, leading to current saturation, also arises from space charge effects which tend to lower the field at the injecting plane of the drift region. This effect can be minimized by higher carrier drift velocity. In almost all solids, the hot carrier velocity does not increase indefinitely with electric field, but saturates at a threshold field, E_s, due to scattering. This scattering-limited velocity, V_{SAT}, is necessary for linear operation since carrier transport is now relatively insensitive to minor field fluctuation. In addition, the intrinsic rise time of the device is inversely proportional to V_{SAT}. Thus, from trapping, space-charge, rise time, and bandwidth considerations, a high carrier drift velocity which saturates at a low electric field is necessary for high power operation.

In practice, additional material constraints are imposed by fabrication methods and material growth techniques. The electric field of a reverse-biased p^+-n diode is maximum at the junction plane, and falls off rapidly in the highly doped p^+ region. For such a junction, therefore, the width of the p^+ region should be a small fraction of the electron penetration depth for optimum gain. On the other hand, the p^+ conductivity must be sufficiently high for a good lateral ohmic contact.

This requirement of high p^+ doping concentration (> 10^{19} atoms/cm^3) over a narrow width (< 1 micron) presents some problem in fabrication. Alternatively, the junction may be of the Schottky-barrier type to avoid the ohmic contact problem. In this case, a large barrier height is desired to reduce the reverse leakage current.

Another area of concern in GEISHA application, especially under cw and high-duty-cycle pulse conditions, is the extraction of heat from the device. Since thermal impedance is inversely proportional to the thermal conductivity, σ_T, of the material, a high σ_T is necessary for this application.

2.2 GEISHA PERFORMANCE LIMITATIONS

2.2.1 Johnson Figure of Merit

An abbreviated form of the Johnson[1] relation for the ultimate performance of the semiconductor device, is derived in Appendix A. It is shown that the Johnson figure of merit (PF^2Z) can be related to two material constants (F_c and V_{SAT}).

$$P_m F_m^2 Z_m = \frac{E_c^2 V_{SAT}^2}{4\pi} \qquad (1)$$

where P_m = maximum power output

F_m = maximum operation frequency

Z_m = maximum load impedance

V_{SAT} = the high field saturation velocity of carriers

E_c = the maximum or critical field which can be applied to a material before avalanche

Thus, it is seen from Equation 1 that the critical field (E_c) and the saturated drift velocity (V_{SAT}) have a profound influence on the ultimate power-frequency limit of the device. Higher E_c means higher ac voltage swing at the same depletion width (same approximate transit time). E_c imposes an additional constraint on the depletion width, since in practice it is desirable to tailor a punch-through condition just prior to breakdown for minimum parasitic resistance. A large V_{SAT} is preferred, since the optimum operating frequency ($f_m = V_{SAT}/2W$; where W = depletion width) determines the optimum depletion width, W, at any frequency.

2.2.2 Thermal Limitation

The thermal impedance (Z_T) of any device is a measure of its ability to carry away heat generated from loss mechanisms within the device. Since a significant fraction (~25 to 50%) of the dc energy expended in a GEISHA target is converted to heat, the thermal impedance constitutes a major problem. Values of dissipative heat fluxes approaching 10^5 watts/cm^2 have been achieved in silicon IMPATT diodes.[2]

Assuming ideal conditions where the heat removal is only limited by the length of semiconductor material in the depletion region, one can show that:

$$Z_T = W/2\sigma_T A \qquad (2)$$

where Z_T = thermal impedance

W = depletion width

σ_T = thermal conductivity of semiconductor

A = area of the semiconductor

The minimum temperature rise at maximum power can then be shown to be directly proportional to the Johnson figure of merit and inversely related to thermal conductivity, where:

$$\Delta T(°C) \Big|_{P_{max}} = \frac{\pi^2 \varepsilon}{\sigma_T} \cdot \frac{(PF^2Z)}{F} \qquad (3)$$

where (PF^2Z) = Johnson figure of merit

ε = dielectric constant

F = desired maximum frequency

Thus, a high figure of merit means a larger temperature rise since the device can be run to higher power levels. However, this is offset by high thermal conductivity and increased frequency of operation.

Table 2.1 presents the best available data and estimates of the three material parameters affecting GEISHA performance for SiC. The values for silicon are included for comparison.

TABLE 2.1 -- Comparison of Important GEISHA Diode Material Parameters

Material	Critical Field (volts/cm)	Saturation Velocity (cm/sec)	Thermal Conductivity (watt/cm°C)	$E_c^2 V_{SAT}^2$ (volts^2/sec^2)
Silicon	3×10^5	10^7	0.8 at 300°C	9×10^{24}
Silicon Carbide	$2\text{-}4 \times 10^6$	*$1.3 - 2 \times 10^7$	1.5 at 500°C	*$0.7\text{-}6 \times 10^{27}$

*Extrapolated from work performed in this report.

2.2.3 Keyes Figures of Merit

Recognizing that thermal considerations, as well as electronic, set the real limit on high speed semiconductors, Keyes[3] recently derived a new figure of merit. The Keyes figures of merit takes into account the minimum switching time consistent with the RC time constant, power to be dissipated, maximum temperature rise, and the thermal impedance. The expression derived is:

$$\text{Keyes Figure of Merit} = \sigma_t (cV_{SAT}/4\pi\varepsilon)^{1/2} \text{ [watts/degree-sec]}$$

where c = velocity of light

σ_t = thermal conductivity

ε = dielectric constant

Table 2.2, as compiled by Keyes, compares the various semiconductor materials. Keyes assumed a V_{SAT} for SiC equal to that of Si and did not assume a higher operating temperature for SiC.

Table 2.2 -- Keyes Figure of Merit for Several Semiconductors

Material	Dielectric Constant	Conductivity (watts/cm°C)	Saturation Velocity (cm/sec)	Figure of Merit $\sigma_t(cV_{SAT}/4\pi\varepsilon)^{1/2}$ (watts/deg-sec)
Si	12	1.5	1.0×10^7	6.7×10^7
Ge	16	0.5	0.6×10^7	1.5×10^7
GaAs	12	0.5	1.5×10^7	2.7×10^7
SiC	7	5.0	1.0×10^7*	29.0×10^7

*Estimated by Keyes.

2.3 SILICON CARBIDE FOR GEISHA APPLICATIONS

In summary, the requirements of a high power GEISHA semiconductor target are:

- High breakdown voltage, v_b, or critical field, E_c
- High saturation velocity, V_{SAT}
- Low threshold field for velocity saturation, E_s
- Minimal carrier trapping in the depletion region
- High thermal conductivity, σ_T

Silicon carbide has a great potential for meeting all these requirements, since work in this study has shown that E_c, V_{SAT}, and thermal conductivity for SiC are higher than are those of the most common semiconductor materials. Additionally, the practical feasibility of producing GEISHA device structures, using Schottky barrier formation techniques, has been demonstrated.

3. TECHNICAL APPROACH

3.1 FUNDAMENTAL PARAMETERS

The thermal conductivity (σ_T) and critical field (E_c) are reasonably well established in the literature.[4,5] However, the carrier saturation velocity (V_{SAT}) for SiC had not been previously determined. Therefore, as a first priority, specimens of known carrier concentration and mobility were fabricated into appropriate sample configurations for measurement of V_{SAT}. Corelative determinations of E_c can be made from $1/c^2$ vs V and avalanche measurements on suitable abrupt junctions as produced for GEISHA evaluation.

3.2 SiC SCHOTTKY BARRIER FORMATION

The major effort was aimed at the formation and characterization of Schottky barriers on various SiC substrates. A reliable, low reverse leakage Schottky barrier diode is virtually ideal for fabrication of a GEISHA device since the Schottky barrier gives good ohmic contact, transparency to electrons and ease of device processing.

3.3 SiC SINGLE CRYSTAL SUBSTRATES

Single crystals of α-SiC (hexagonal) are prepared by the sublimation growth technique. Dopants can be serially added to the growth chamber to produce n-type and p-type layers in the crystal, and relatively pure (10^{17}) crystals can be readily grown in an undoped environment.

Schottky barrier substrates (pure n-type, n^+n and p^+p) and grown p-n junctions were produced for the program using this technique.

3.4 OHMIC CONTACTS

Evaluation of the ohmicity of direct tungsten-SiC bonds were made for the bottom contact to the GEISHA device. Thin tungsten (CVD or sputter deposited) top contacts were evaluated for possible use as ohmic contact to grown junction devices where the top junction is less than three microns thick.

4. RESULTS

4.1 CARRIER SATURATION VELOCITY

The carrier saturation velocity (V_{SAT}) for SiC has not been previously determined. The results of the Johnson figure of merit (Section 2.2) point out the need for knowing this quantity for evaluation of the true device potential. Assuming the same scattering mechanism as we find in silicon where the hot electrons are relaxed by optical phonons we have the relationship[6]:

$$V_{SAT} \approx [8E_{Lo}/3M_o]^{1/2} \quad \text{(cm/sec)} \tag{4}$$

where: E_{Lo} = longitudinal optical phonon energy

M_o = free electron mass

The longitudinal optical phonon energy in SiC has been found[7] to be about 0.107 eV which gives a predicted value of about 1.3×10^7 cm/sec for V_{SAT}. There is uncertainty in this prediction in that the bulk mobility for electrons in SiC tends to be lower than that for Si. Lower bulk mobility (which is determined by impurity scattering and acoustic phonon scattering) might lead to a lower V_{SAT} if the high field relaxation mechanism is not optical phonon dominated. Thus, it was necessary to measure the carrier velocity as a function of electric field to determine if the V_{SAT} of SiC was lower or higher than that of silicon.

4.1.1 Measurement Technique

Of the various techniques available for generating carrier velocity (V) versus electric field strength (E) curves, the most applicable is a Ryder[8] type conductivity measurement since our relatively high doping levels do not experimentally lend themselves to time-of-flight measurements. However, samples of 10^{15} cm^{-3} p-type SiC were sent to Stanford University for time-of-flight evaluation with a sophisticated technique they have developed.

Using the Ryder technique, if one has a material of known carrier concentration (N_o) and known dimensions, then a simple sample current (I) versus applied voltage (V) plot can be manipulated to give current density (J), electric field (E), drift field mobility (μ) and carrier velocity (V).

We have:

$$E = V/\text{length (volts/cm)} \tag{5}$$

$$J = I/\text{Area (amperes/cm}^2) \tag{6}$$

$$J = N_o e\mu E = N_o eV \tag{7}$$

Thus $$V = J/N_o e \text{ (cm/sec)} \tag{8}$$

and $$\mu = dV/dE \text{ (cm}^2\text{/volt-sec)} \tag{9}$$

The power densities involved in such a measurement are quite high, and to avoid heating effects, a pulsed arrangement is necessary.

The block diagram of Fig. 1 shows the experimental arrangement. Typically, the pulse width was near 0.2 microseconds with a 200 Hz repetition rate.

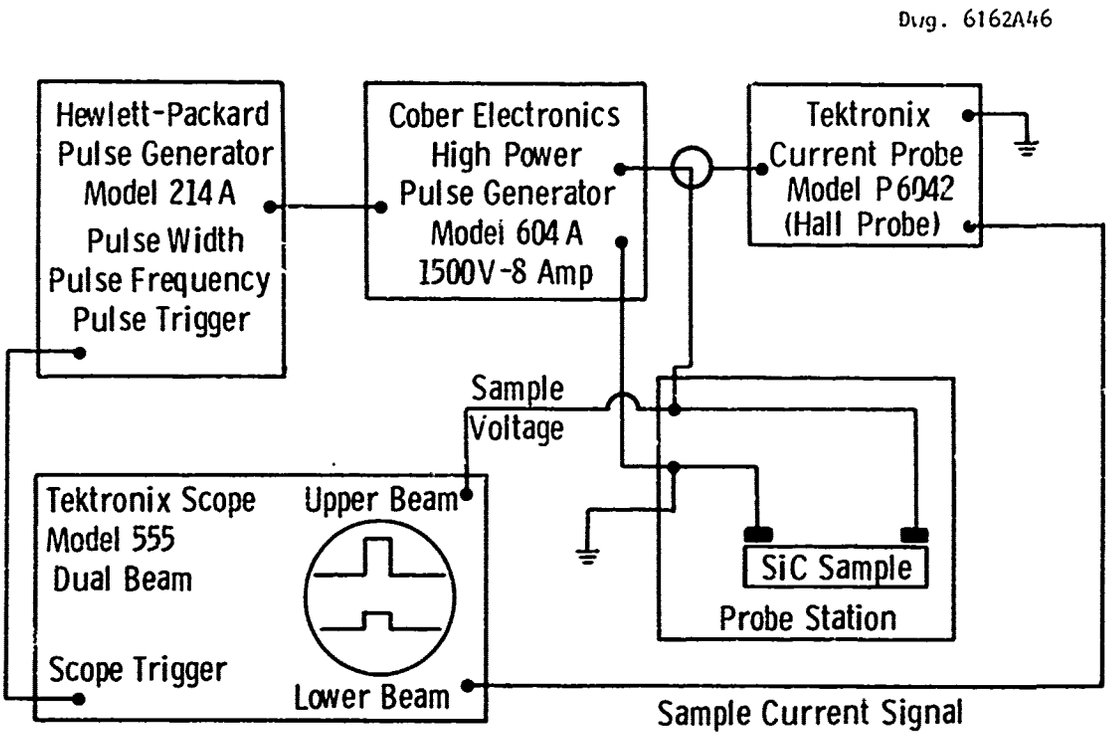

Fig. 1 Experimental Arrangement for Obtaining Pulsed I-V Data

A 50 ohm impedance matching termination and a dropping resistor were also required in the experimental arrangement. This is shown schematically in Fig. 2 where we have:

I = measured current

V_o = voltage measured at oscilloscope

V_s = voltage across SiC sample

I_s = current through the sample

R_s = sample resistance.

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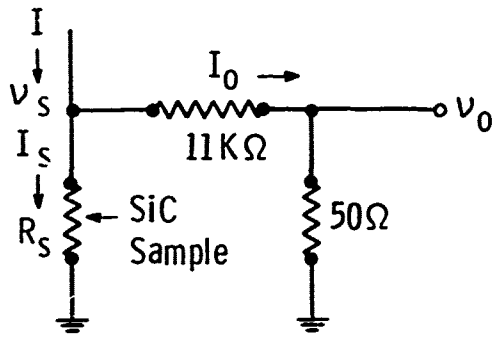

Fig. 2 Schematic of Current-Voltage Sampling Circuit

Thus, measuring I and V_o we can calculate I_s and V_s (the quantities of interest) where:

$$I_s = I - (V_o/50) \tag{10}$$

$$V_s = 221\ V_o \tag{11}$$

and

$$R_s = V_s/I_s \tag{12}$$

4.1.2 Sample Preparation

Conductivity samples were made from SiC crystals which had been characterized with Hall measurements in previous work. The n-type samples were typical SiC material with carrier concentrations near 10^{17} and Hall mobilities near 250 (cm^2/volt-sec). The p-type samples were more of a problem since the p-type crystals were the result of "pure" n-type growth runs which happened to be compensated p-type. Thus there are few characterized p-type crystals and these tend to be highly compensated and of low mobility. Additionally, ohmic contacts to these highly compensated p-type crystals has so far proved impossible to

fabricate, as will be shown in the results. Ohmic contact to the n-type samples was made by heating them in contact with tungsten discs up to 1900°C.

Originally, the V_{SAT} samples were in the form of thin rectangular bars made by lapping and diamond cutting before contacting. However, since the power supply was rated at 1500 volts and 8 amperes (with overruns to 2000 volts and 16 amperes by "ringing" the line) and field strengths in the range of 10^5 volts/cm were needed at current densities of the order of 1.8×10^5 amps/cm^2, it soon became obvious that thermal and power supply limitations required samples of very small length and cross sectional area. The only convenient method of producing such a sample is an oxidation-photoresist-chlorination technique as shown in Fig. 3. Final trimming of the channel width was accomplished with an abrasive technique.

This procedure is very difficult since one has to mechanically handle an unsupported crystal with a channel of about 50 micron thickness. Since the tungsten contacts are attacked by the oxidation and chlorination procedures, they must be the last step. As a result, yield of samples is very low and limited by the number of characterized crystals available.

Nevertheless, a range of suitable samples were prepared and measured. The photographs of Fig. 4 show a typical specimen where the channel width has been reduced with a boron carbide sandblast.

4.1.3 V_{SAT} Results

The data generated from these V_{SAT} measurements are shown in the curves of Fig. 5. Figure 5 graphically summarizes progress to date.

As can be seen, both GaAs and Si samples were also measured as an experimental check. Good agreement with published data is demonstrated. Additionally, the slope of the SiC V-E curves (plotted on linear paper) gave excellent agreement with previously obtained Hall mobility ($\mu_{Hall} \cong \mu_{drift} = dV/dE$).

The n-type samples have been measured up to a velocity of 8.2×10^6 cm/sec. The curve is still unsaturated (Ohm's Law region) up to this high value. Some hint of the beginning of saturation is seen in the highest value, but nothing definite can be said without additional measurements. Si, by comparison, starts to show saturation at about 4×10^6 cm/sec. Thus it is presumed that the V_{SAT} for SiC will be at least as high as that of Si and will in fact probably reach between 1.3 to 2×10^7 cm/sec.

Contact problems (carrier injection) with available p-type material (sample D-49-4 shown on Fig. 5) frustrated attempts to obtain hole data.

Attempts were made to cool some of the specimens to liquid nitrogen temperature. This would somewhat decrease the carrier concentration and increase mobility, thus enabling us to take the samples to higher V and E regions. However, all specimens fractured due to differential thermal expansion problems.

At this point, further V_{SAT} measurements were de-emphasized due to time limitations and the difficulty of obtaining higher current densities and electric field strengths.

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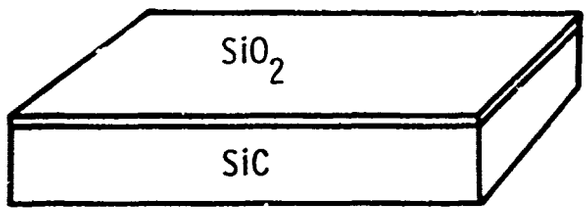
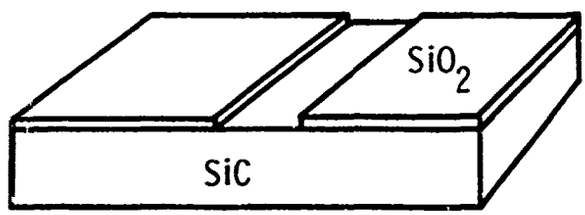
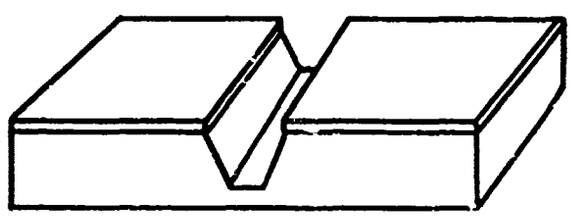


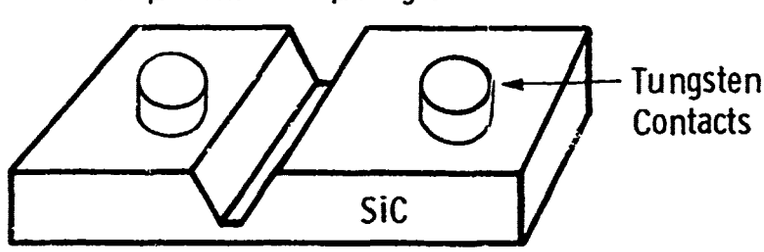
(1) Oxidize Crystal Bar (on carbon side) at 1200°C.



(2) Open Line in Oxide with Photoresist



(3) Chlorine Etch at 940°C to Produce Channel
(≈ 50μ thick × 100 μ long).



(4) Remove Oxide and Attach Tungsten Contacts at 1900°C.

Fig. 3—Technique for producing V_{sat} samples from SiC crystals

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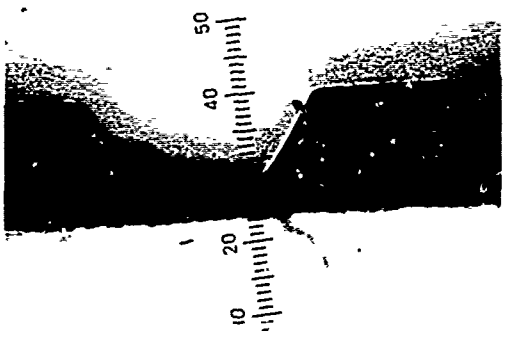
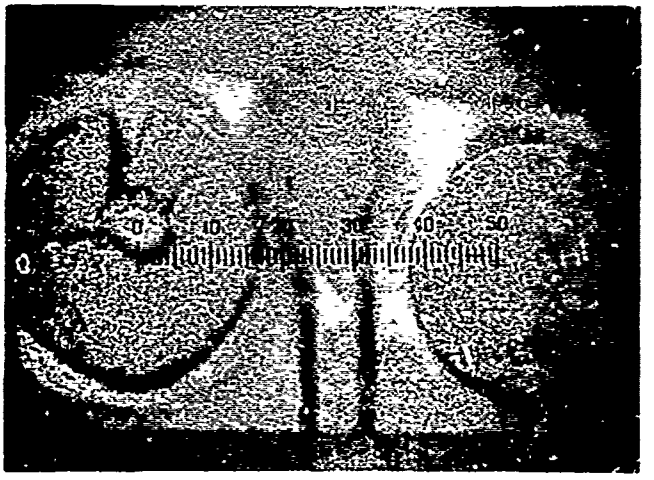


(a) Cross-section shadowgraph of SiC Sample D-102-3. 100X magnification



(b) Top view of SiC sample D-102-3. Showing Tungsten Contacts and Channel. Magnification is 30X

Figure 4 — Side and top view of typical SiC V_{SAT} sample.

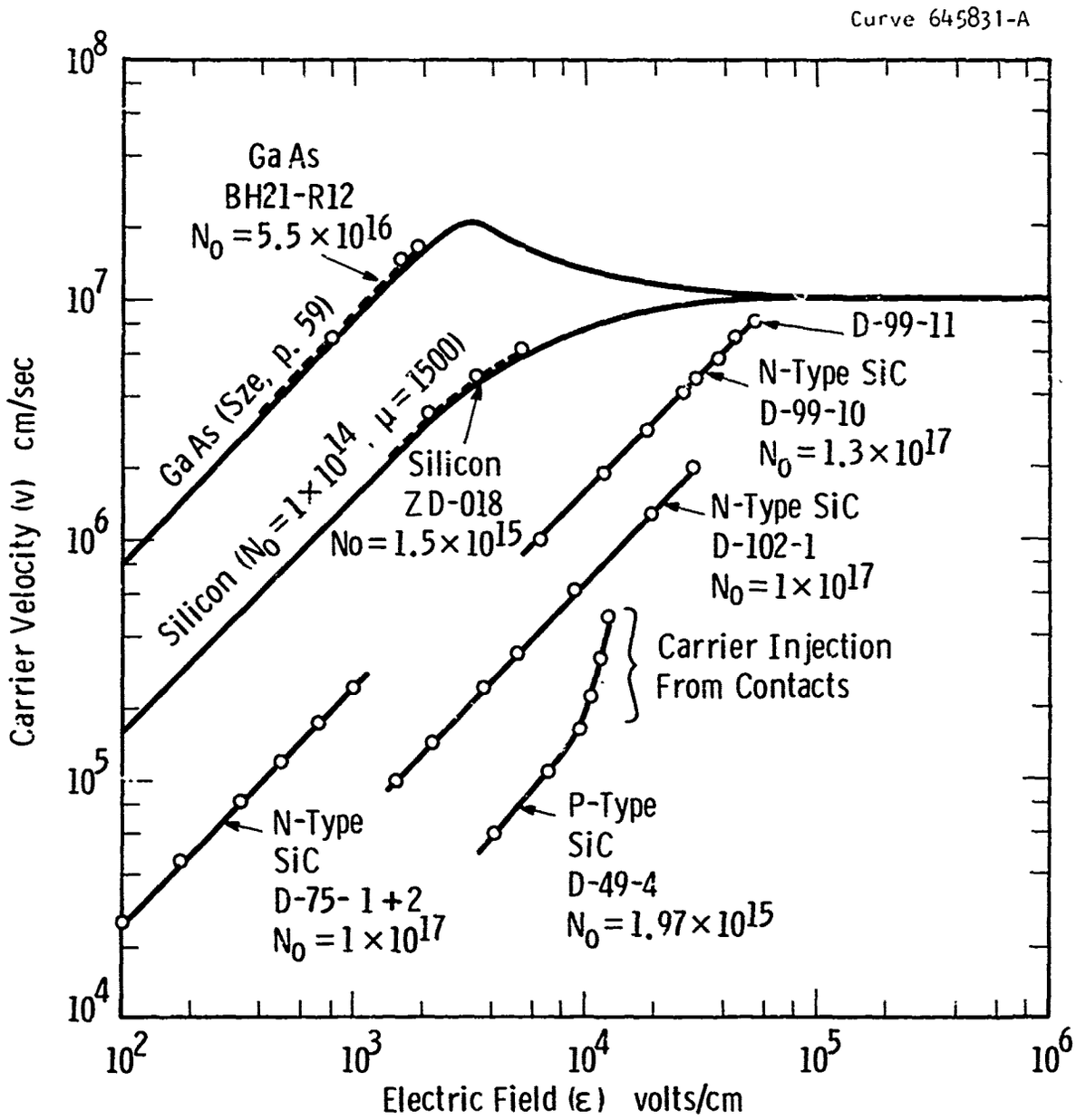


Fig. 5--Summary of carrier saturation velocity measurements on SiC

4.2 SCHOTTKY BARRIER DIODE STUDY

4.2.1 SiC Substrates

A variety of SiC substrates was prepared for the Schottky barrier evaluation. The initial samples were made from the same crystal batches used for the V_{SAT} measurements. These n-type ($\approx 1 \times 10^{17}$ cm^{-3}) SiC discs were directly bonded to tungsten electrodes at 1900°C to form ohmic bottom contacts. These samples were used to survey the various metallizations. Additionally, several samples of the above variety were used for surface preparation studies which included molten salt etching and chlorine gas etching.

SiC Schottky barrier samples were also made on 10^{16} uncompensated n-type crystals and on $\approx 10^{15}$ compensated n-type material. Etched (Cl_2) grown junctions were used as n^+n and p^+p substrates, in order to approximate a true GEISHA structure. Contacts to the n^+ and p^+ faces were made with a AuTa braze alloy (1150°C). No pure p-type crystal substrates were made due to the difficulty of making ohmic contact; as discussed under the V_{SAT} measurements. Techniques for directly growing n^+n and p^+p substrates were developed at the end of the program.

4.2.2 Surface Preparation

Four types of surface preparations were employed during the course of this study; these are schematically illustrated in Fig. 6. Initially, as-grown surfaces were employed since they are reasonably smooth and processing (bottom contact and metallization) can be done without a determination of the carbon or silicon face. Oxidation and chlorine etch techniques require this determination since these processes

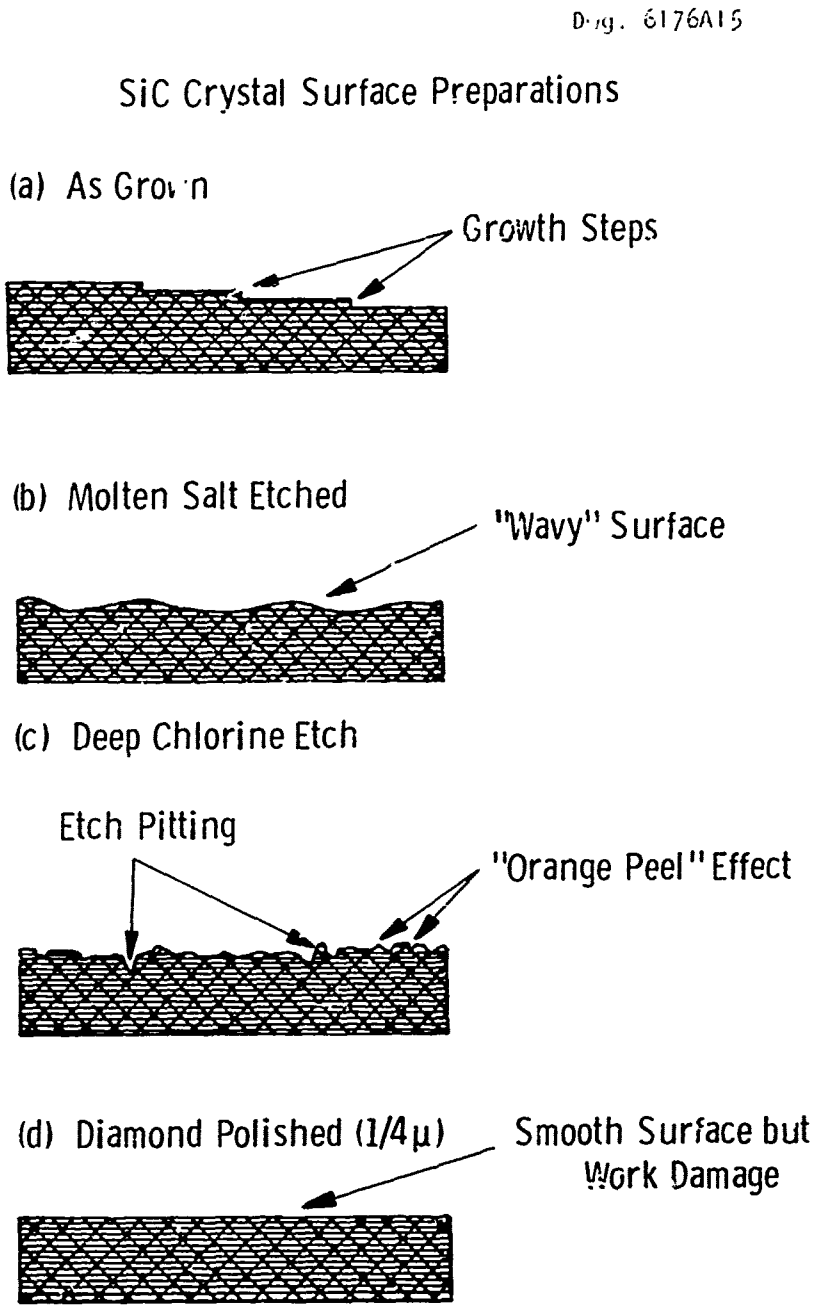


Fig. 6 — Various SiC surface preparations.

only work on the carbon face. The disadvantages of the as-grown surfaces as shown in Fig. 6(a) are the presence of some growth steps and residual surface damage. This surface stress is present since the temperature is dropping in the sublimation growth furnace at the end of the run.

Molten sodium hydroxide (at about 700°C) can be used to etch SiC. This etch does not differentiate between the silicon or carbon face, and is slow to attack the tungsten contact. Thus, it can be utilized on an already formed SiC-tungsten substrate. The disadvantages of this technique as shown in Fig. 6(b) are that the amount of material removed is relatively large ($\sim$ 100 microns in 10 seconds) and difficult to control; sample edges are rounded off and the surface is left with a wavy texture.

Chlorine etching by contrast is a very controllable technique, and in conjunction with a thermally grown oxide, can utilize photoresist techniques. The etching takes place in a chlorine-oxygen-argon mixture at about 950°C, and only affects the carbon face of the SiC crystal (etch rates are typically 30-40 microns/hour). Since this process rapidly attacks the tungsten contacts, it can only be used on SiC crystals before they are bonded to the tungsten. The disadvantage of chlorine etching is that on etches of more than 30 microns, the surface takes on an "orange peel" texture and dislocation etch pits will appear, as illustrated in Fig. 6(c).

Diamond polishing down to 1/4 micron grit size leaves a very smooth flat surface as shown in Fig. 6(d). However, there is still residual work damage from the polishing.

Chemical cleaning in concentrated HF followed by glow discharge cleaning in the vacuum evaporator prior to the Schottky barrier metallization was used for all the SiC samples.

4.2.3 Schottky Barrier Formation

Initially, various metal films were evaporated onto the as-grown, pure SiC substrates. The metals tested were Au, Al, Ti, Pt and W (sputtered). Chemical cleaning techniques (solvent cleaning with conc. HF soak prior to deposition) and in situ cleaning by back sputtering were used to try to obtain a clean crystal surface. Schottky barrier regions were delineated by wax masking and chemical etching in the case of Au, Al and Ti. The Pt and W metallizations were obtained by a metal mask and air abrasive technique.

The results showed that regardless of SiC substrate or metal used (Au, Al, Ti, Pt, W) the resulting Schottky barrier diodes were virtually indistinguishable as to I-V characteristics and barrier height.

Capacitive voltage plots were made and $1/C^2$ vs. V curves were produced. Values of barrier height near 2.6 volts were obtained. Figure 7 is a $1/C^2$-V plot for a typical sample. As an independent check, this sample (which had a 200 to 400 Å gold layer) was placed in a visible-UV spectrophotometer. The photoresponse (photocurrent) was measured as a function of wavelength, normalized for equal photon flux at each wavelength. The plot of the square root of the response versus photon energy extrapolates to 2.4 to 2.6 eV barrier height. Figure 8 shows this $R^{1/2}$ vs. eV graph.

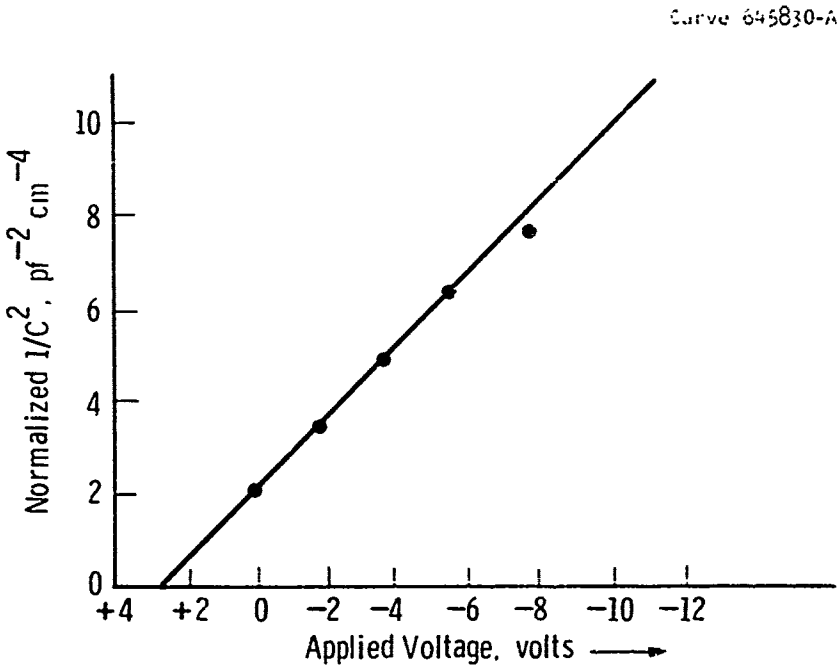


Fig. 7 — $1/C^2$-V plot for sample D-99-2 (n-type SiC) with a gold Schottky barrier.

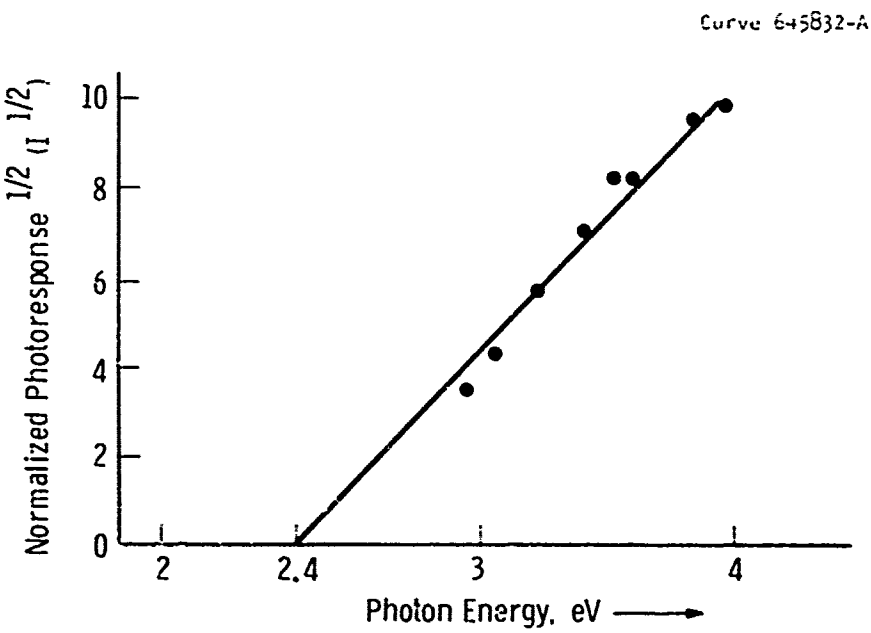


Fig. 8 — Square root of photoresponse versus photon energy for sample D-99-2 (n-type SiC).

These Schottky barrier diodes achieved about 50% of their maximum expected reverse voltage, but were characterized by "soft" reverse characteristics. A typical current-voltage characteristic of these as-grown surfaces is shown in Fig. 9.

Diamond polishing (down to 1/4 micron grit size) of the crystal surface gave essentially the same results on the 10^{17} cm^{-3} material. However, dramatic improvements resulted when the samples were etched in molten sodium hydroxide ($\sim$ 700°C) prior to metallization.

A number of these salt etched samples had a "hard" reverse characteristic (low leakage) and would go out to a true avalanche breakdown. The I-V characteristics of such a sample are shown in Fig. 10. Unfortunately, these samples initially had a storage instability and would degrade over a period of a few hours. This instability was found to be caused by residual salt contamination. Improved cleaning techniques seem to have eliminated the instability on the samples tested to date, and no change in I-V characteristics have been noted over a 4 week period.

The avalanche samples did enable us to calculate E_c and a value near 3×10^6 volts/cm was obtained. Computer calculations were run from Schottky barrier theory to generate curves for depletion layer width and breakdown voltage versus doping level. These are shown in Figs. 11 and 12, with silicon shown for comparison.

As can be seen, the SiC is capable of supporting much larger breakdown voltages than were comparable silicon samples and with greater depletion layer width at breakdown. Also shown on these figures is the

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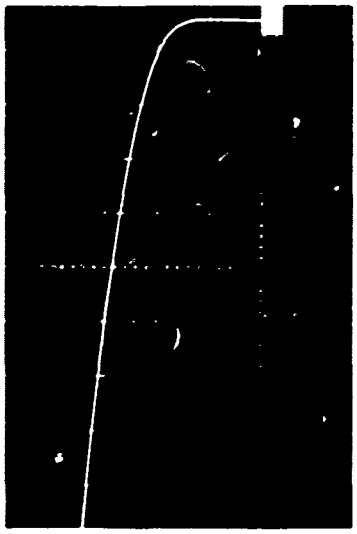
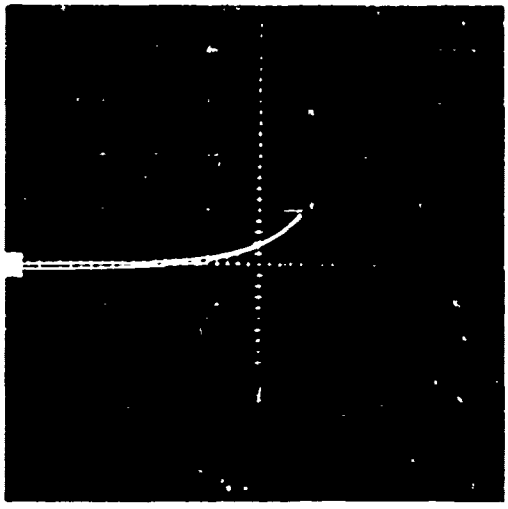


Forward I-V

0.05 mA/div. vertical
1.0 V/div. horizontal
(□ is origin)



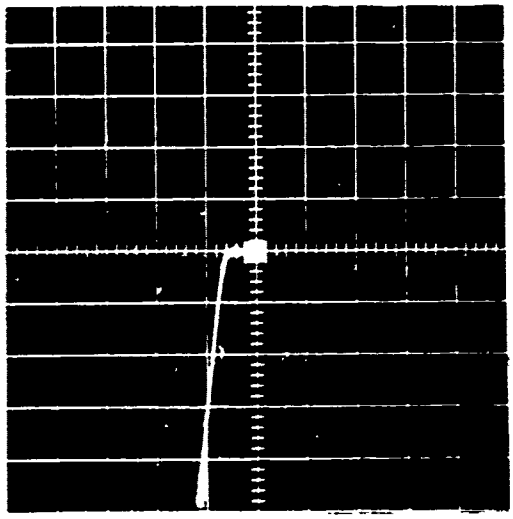
Reverse I-V

0.05 mA/div. vertical
5.0 V/div. horizontal
(□ is origin)

Note: 5 μA leakage at 20 V_r for a 4000 Å depletion width.

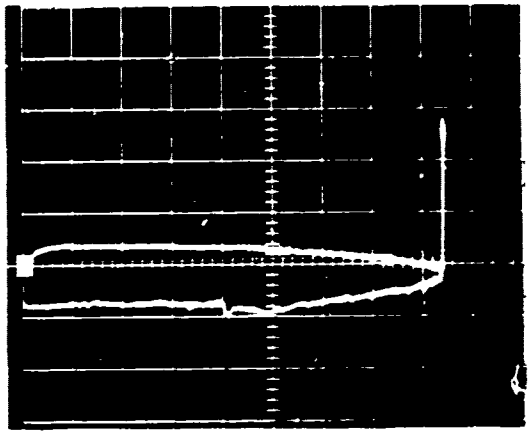
Figure 9 — Current voltage characteristics for Au on n-type SiC (D-99, 1.3×10^{17} cm^{-3}) with no surface treatment.

RM-5



Forward I-V

0.2 mA/div. vertical
1.0 V/div. horizontal
(□ is origin)



Reverse I-V

0.01 mA/div. vertical
10.0 V/div. horizontal
(□ is origin)

(Note avalanche at 84 V_R)

Figure 10 — Electrical characteristic of molten salt etched SiC (n-type, 1.6×10^{17} cm^{-3}) with a gold Schottky barrier.

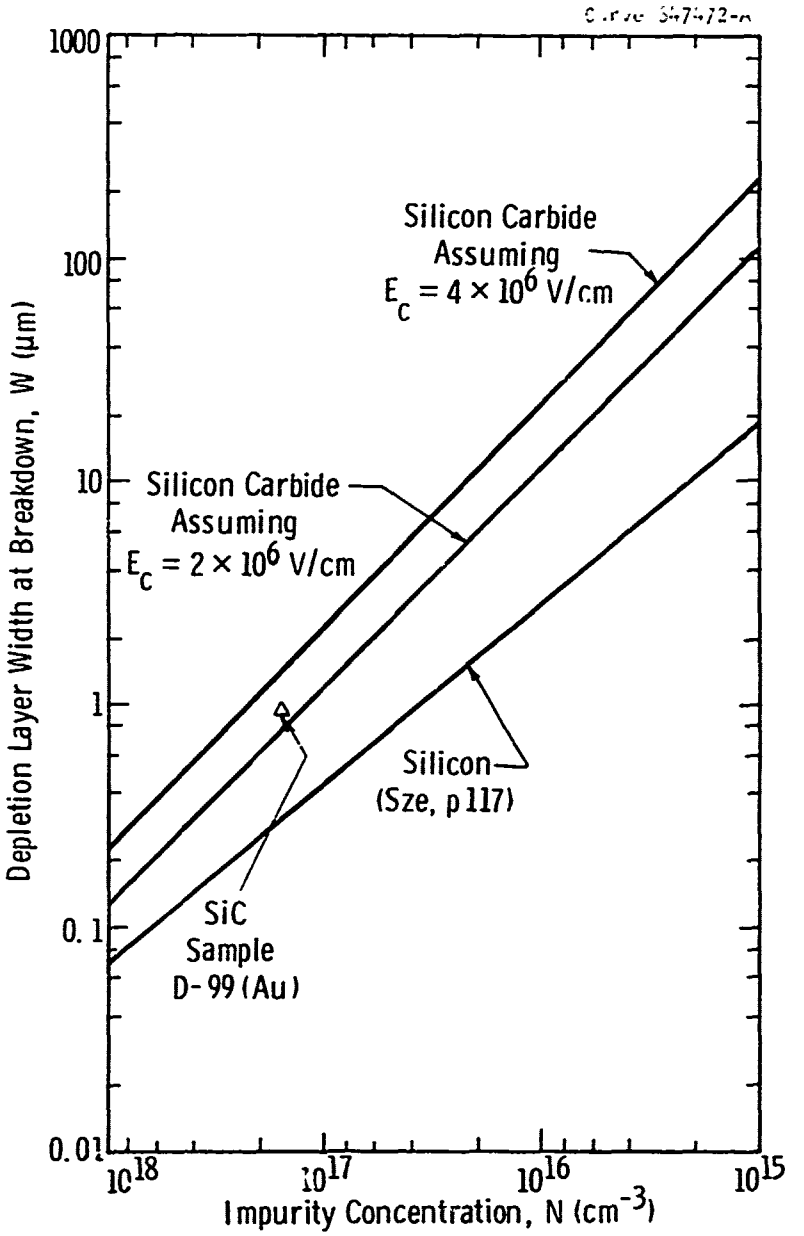


Fig. 11 — Calculated depletion width at breakdown versus impurity concentration for silicon carbide Schottky barrier diodes (Si curve for comparison).

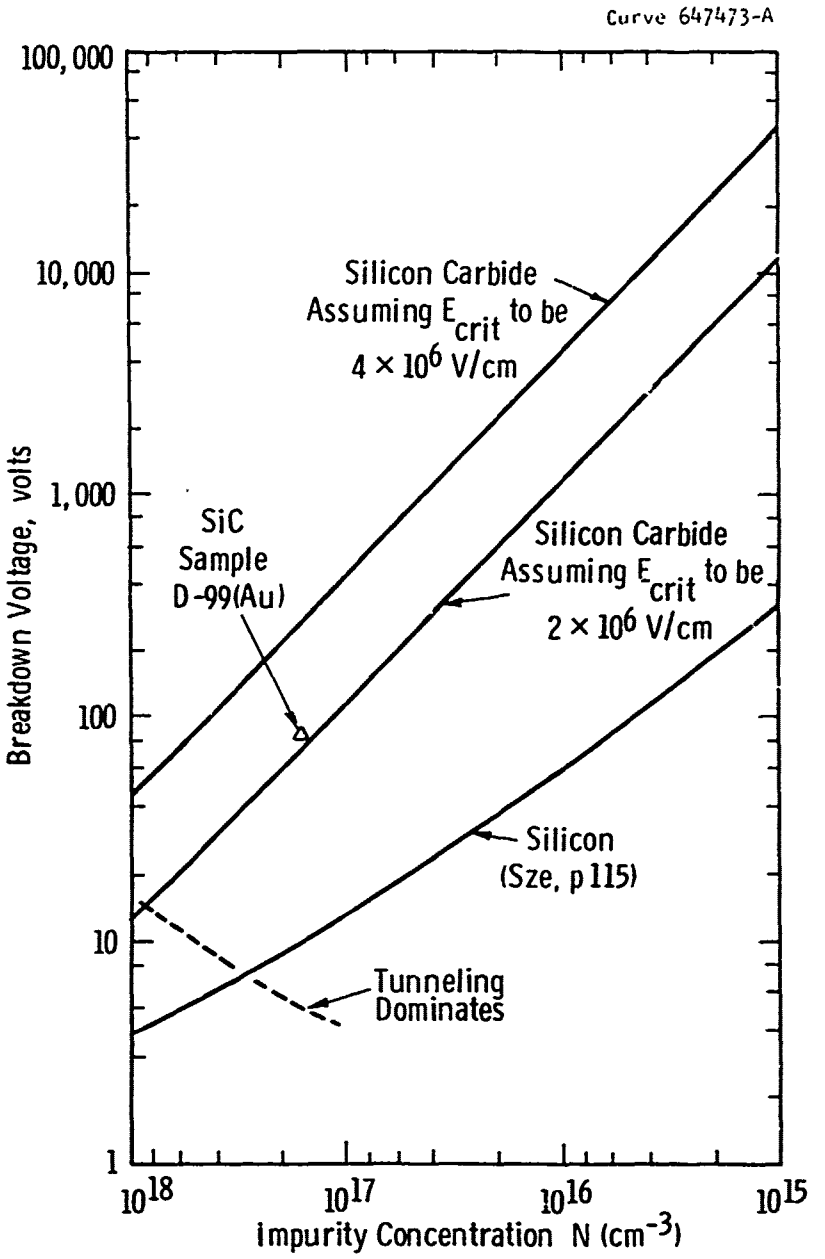
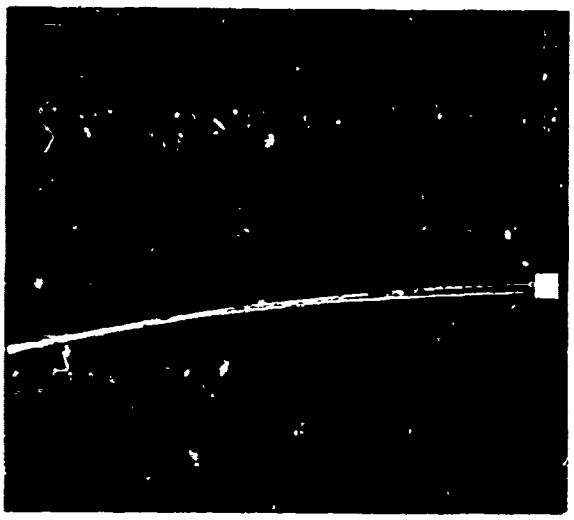


Fig. 12 — Calculated breakdown voltage versus impurity concentration for Schottky barriers on SiC (Si curve shown for comparison).

experimental point derived from the "hard" Schottky barrier diodes. The fit with the theoretical curves is very good and implies that the calculated characteristics are achievable. Figure 12 also indicates that lower doping should support enormous voltages (viz., over 500 volts reverse for 1×10^{16} cm^{-3} material). Diamond polished samples (work damaged, without etching of any kind) were made from $\sim 2 \times 10^{16}$ uncompensated n-type SiC and approximately 5×10^{15} compensated material. These were metallized and gave the expected high reverse voltages. Figures 13 and 14 show the characteristics obtained. The 5×10^{15} material supported over 700 volts without breakdown (of course the forward drop is extremely high due to the non-ohmic nature of the bottom contact to 10^{15} material). Figure 15 is a photograph of the 2×10^{16} sample which supported over 200 volts reverse.

4.2.4 GEISHA Structure

All the previous Schottky barrier samples enabled us to study the Schottky barrier formation, but are not usable as GEISHA devices. Since these samples are made from pure crystal runs, they have a high series resistance due to the 10 mils or so of undepleted, low doped crystal below the depletion region. The RC time constant of such a device would be extremely large compared with transit time across the depletion zone. An ideal SiC GEISHA structure would have about 10 to 20 microns of relatively undoped material ($\sim 10^{15}$ cm^{-3}) below the Schottky barrier, followed by a heavily doped (10^{18}-10^{19} cm^{-3}) layer and then the bottom contact.



Reverse

0.1 mA/div. vertical
20.0 V/div. horizontal
(□ is origin)

Figure 13 — Reverse I-V characteristic of Al on SiC sample D-69-4 (n-type 2×10^{16} cm^{-3}) diamond polished surface.

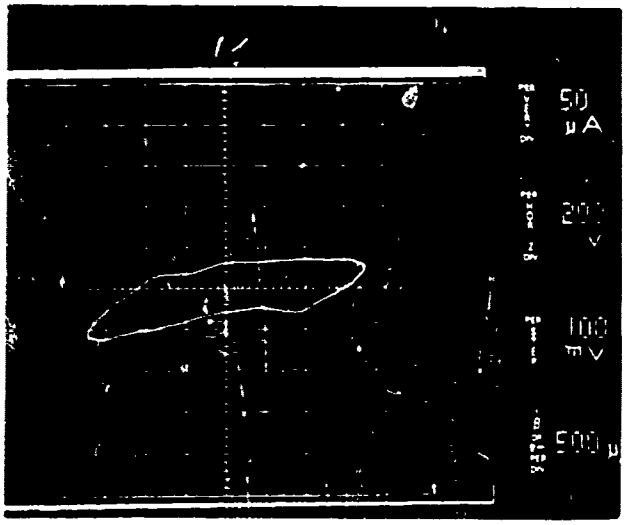


Figure 14 -- Electrical characteristic of Al on SiC sample C-327 (n-type, $\approx 5 \times 10^{15}$ cm^{-3}) diamond polished surface.

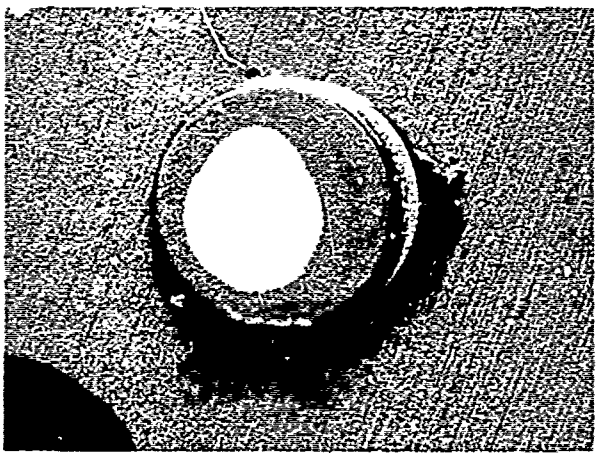


Figure 15 — Schottky barrier specimen D-69-4 (n-type 2×10^{16} cm^{-3}). Diamond polished and metallized with 2000 Å of aluminum (10×).

Since epitaxial growth of SiC is presently unavailable, it was felt that such an n^+n structure might be obtained by chlorine etching of available grown p-n junction SiC crystals as outlined in Fig. 16. However, the deep chlorine etching produced a rough and uneven surface ("orange peel" and etch pit texture), which was unsuitable for metallization. Thus another effort was made to produce p^+p substrates from these grown junction crystals. The chlorine etch plus lapping method for p^+p, is shown in Fig. 17, and involves much shorter etching times. This method was much more acceptable, although not optimal, and several samples were made in this way. The forward and reverse electrical characteristics are shown in Fig. 18. The forward drop is quite small and the junction was "hard" out to 48 volts (beyond this point it became unstable).

A design curve has been generated from Figs. 11 and 12 which includes breakdown voltage, depletion width and doping level; this is shown in Fig. 19. The curve of Fig. 19 is useful for determining GEISHA parameter design. As an example, to obtain a 10 micron depleted layer, we need approximately 1×10^{16} cm^{-3} doping and this layer would support about 1000 volts. Thus a SiC GEISHA structure with 10 to 20 microns of 10^{15} cm^{-3} material on a base of 10^{18} to 10^{19} cm^{-3} could be easily depleted to punch through.

The Schottky barrier results, surface etching studies and GEISHA design curve indicated that direct sublimation growth of an n^+n (or p^+p) would be desirable. The method of directly growing an n^+n (or p^+p) SiC substrate is illustrated in Fig. 20. Oxidation or

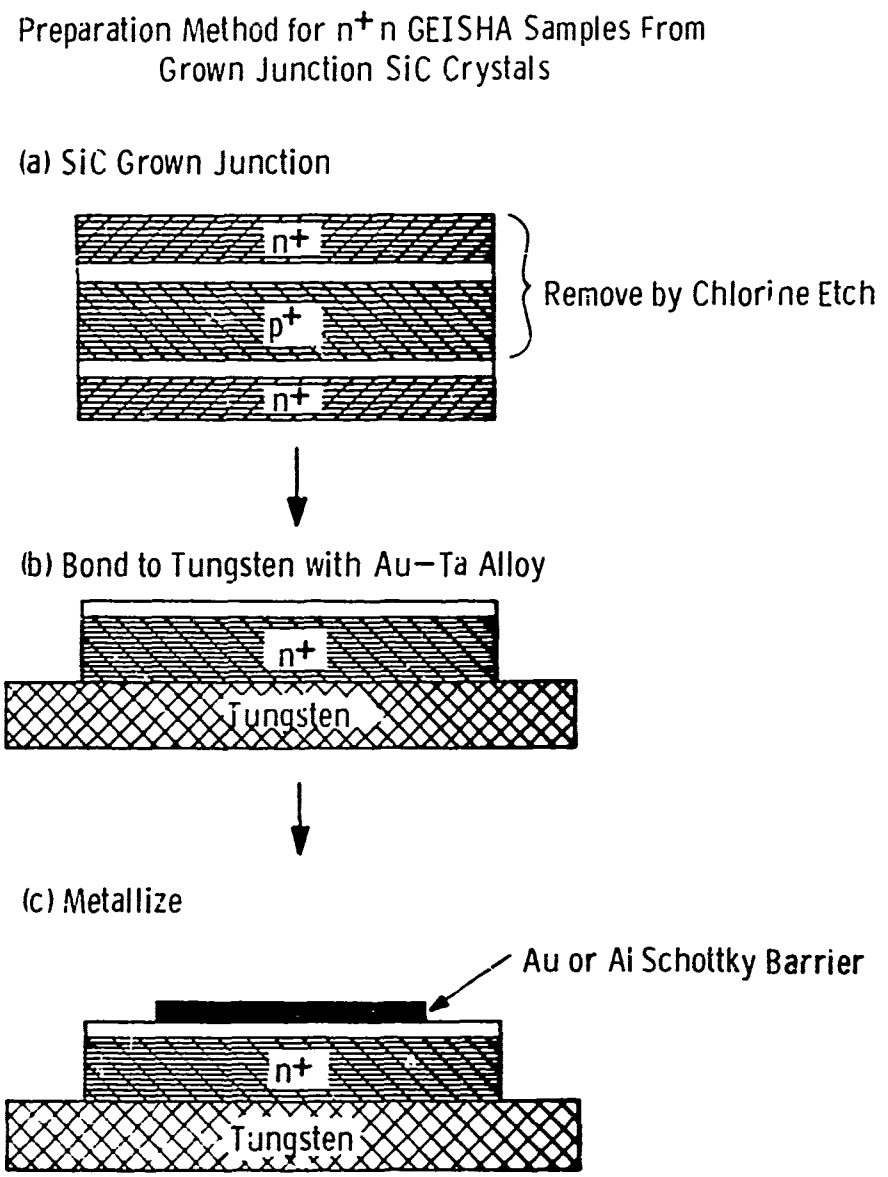


Fig. 16 — Processing steps to obtain n^+n SiC substrates from grown junction crystals.

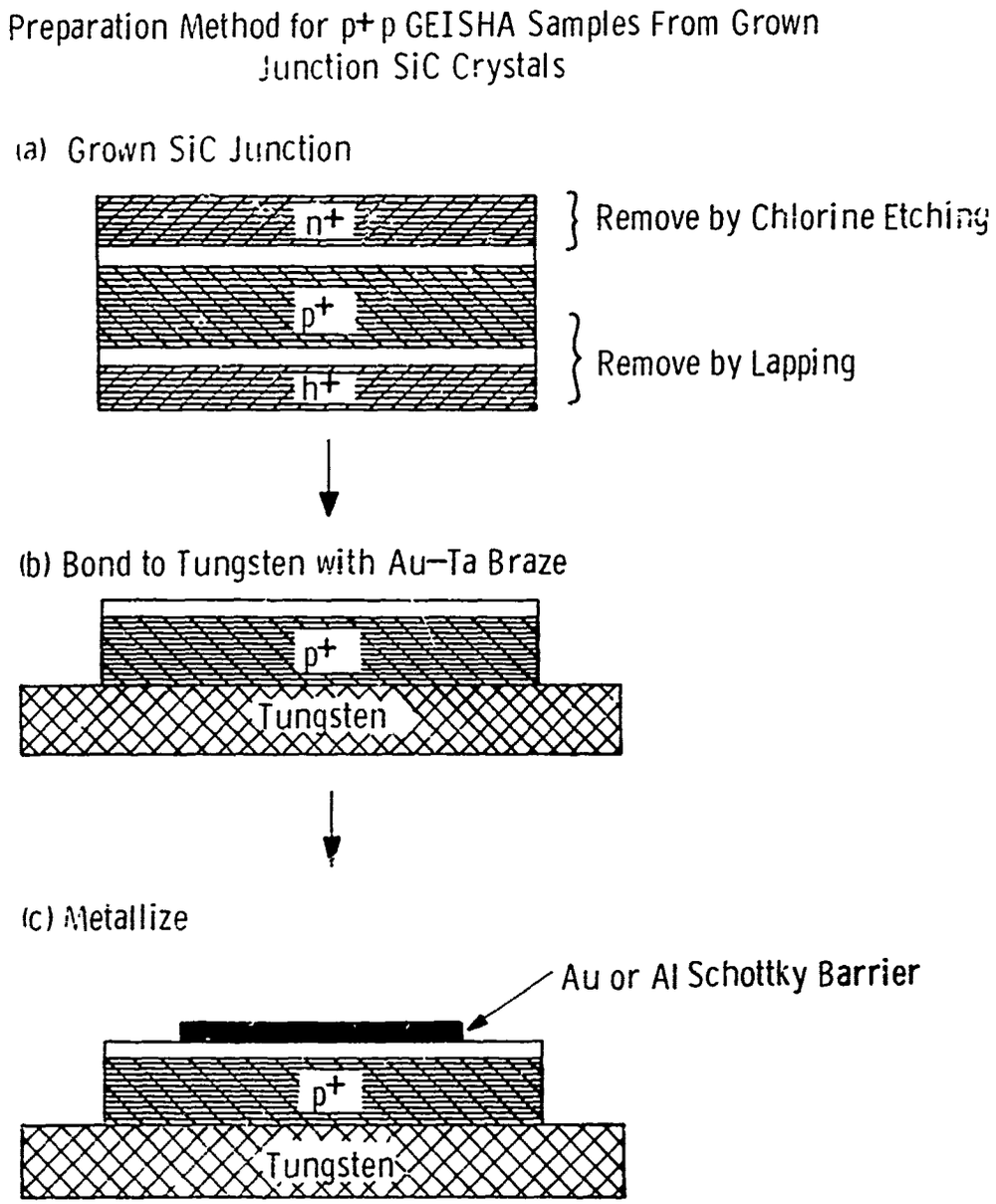
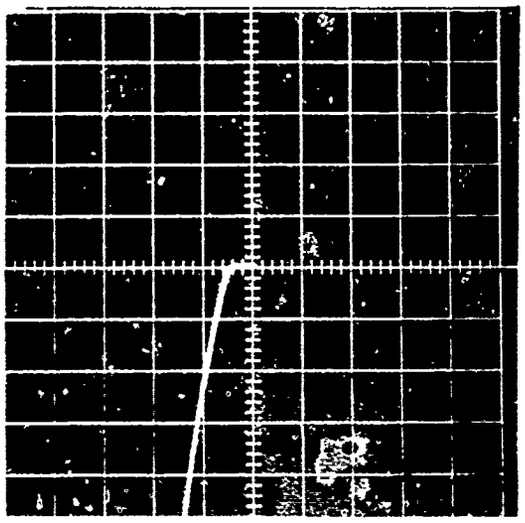
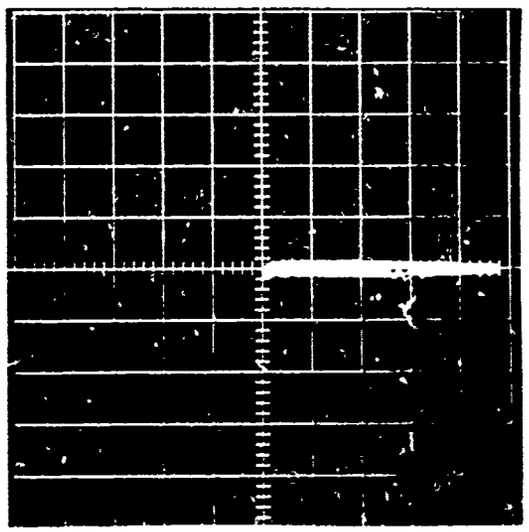


Fig. 17 — Processing steps to obtain p^+p SiC substrates from grown junction crystals.



Forward

0.5 mA/div. vertical
1.0 V/div. horizontal



Reverse

0.01 mA/div. vertical
10.0 V/div. horizontal

Figure 18 — Electrical characteristics of a chlorine etched p⁺p SiC (XRF-200) substrate with a gold Schottky barrier (1000 Å).

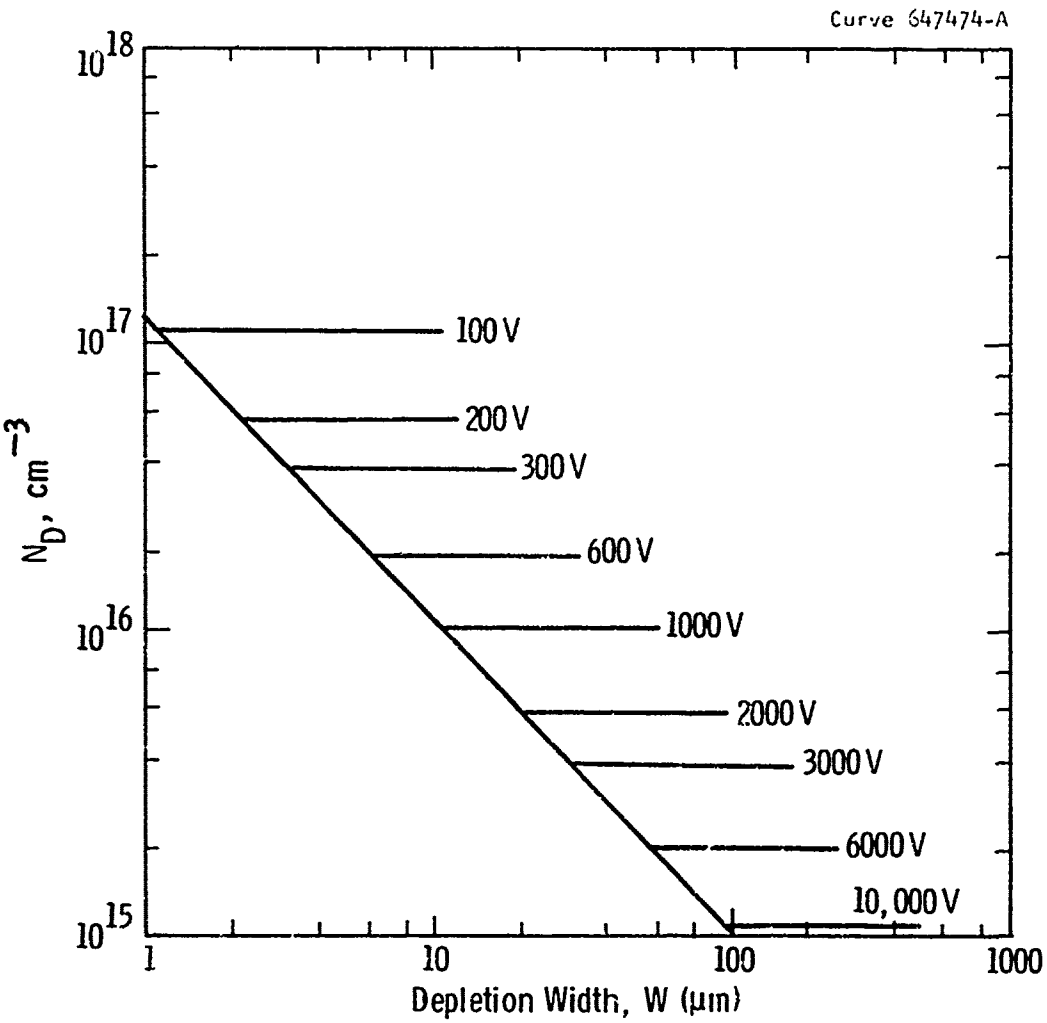


Fig. 19 — Depletion width versus doping level and breakdown voltage for silicon carbide (assuming $E_c = 2 \times 10^6$ V/cm).

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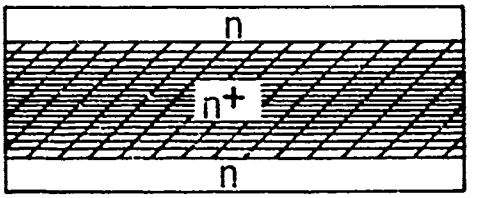
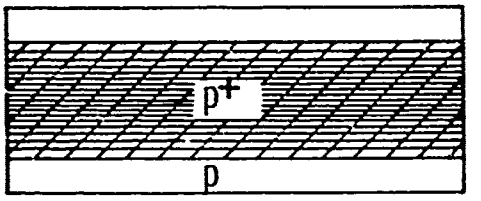
Direct Sublimation Growth of SiC GEISHA Crystal Substrates

(a) n^+ n Crystal



Initial Growth in N_2 to Give n^+ Core. Remove N_2 to get n–Type Skin

(b) p^+ p Crystal



Initial Growth with Al in Argon Ambient to Give p^+ Core. Add Dilute N_2 to Get P–Type

Fig. 20 — Method for directly growing n^+n and p^+p SiC GEISHA substrates.

polishing and oxidation after growth, would provide a smooth damage free layer for the metallization, without the disadvantages of the chlorine or molten salt etching.

Both the n^+n and p^+p growth techniques were tried experimentally at the end of the program. No unforeseen problems were evident, and the technique looks quite workable, giving the structures shown in Fig. 20. However, the doping levels and layer thicknesses must be optimized for the GEISHA applications.

5. SUMMARY

The work performed under this feasibility study has established that the interest in SiC GEISHA devices based on practical and theoretical speculations is well founded. Measurements of the critical field and electron carrier velocity indeed show the enormous potential of SiC relative to Si for high frequency, high power devices as limited by the Johnson figure of merit. Device fabrication using Schottky barrier techniques has been shown to be feasible and practical. Schottky barriers on SiC have been taken to avalanche and barriers on low doped material are capable of sustaining very high reverse voltages. Additionally, the technology for producing appropriate SiC substrates of reasonable size and quantity is reasonably well developed.

6. RECOMMENDATIONS FOR FUTURE WORK

Further work on SiC GEISHA should include sublimation growth of suitable n^+n substrates. Additionally, a guard ring configuration should be employed, using thermally grown SiO_2 on SiC to approach bulk breakdown values on relatively large area GEISHA devices. These substrates should be grown as large as practical (probably a square geometry of about 3 mm per side) for prototype configurations.

Some effort should be spent in further investigation of other Schottky barrier formation techniques and processing. Effects and characteristics of heat treatment (annealing), sputtered layers, ion implanted metal layers as Schottky barriers, are some of the possibilities to be evaluated. Finally, several state-of-the-art SiC GEISHA diode prototypes should be fabricated, which would be suitable for measurements of electron beam gain, rise time, thermal conductivity and electron beam irradiation.

This program of further study should include:

1. Sublimation growth and fabrication of n^+n SiC GEISHA substrates (approaching 3 mm on a side).

2. Fabrication and characterization of Schottky barriers on SiC with a guard ring configuration.

3. Continued evaluation of Schottky barrier formation techniques and processing.

4. Fabrication of SiC GEISHA prototypes suitable for EBIC gain, rise time, and electron beam irradiation measurements.

Such a program would answer the remaining questions as to the practicability of a SiC GEISHA and provide the technology for production of operational units.

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APPENDIX A

POWER-FREQUENCY^2 IMPEDANCE LIMITATIONS ON GENERALIZED TRANSIT-TIME LIMITED POWER SEMICONDUCTOR DEVICES

In 1965, Johnson[1] derived a limiting relation for the ultimate performance of any semiconductor device. We will rederive this relationship in shortened form because it is relevant in comparing the potential of SiC GEISHA targets to state-of-the-art silicon GEISHA targets.

First, we will derive an expression for ultimate power of a semiconductor device, the ultimate power P being the instantaneous product of maximum peak ac voltage swing and maximum peak ac conduction current, here assumed in phase with the voltage maximum under ideal circuit conditions.

The maximum or critical field E_c (volts/cm) which can be applied to a semiconductor junction is a useful concept inasmuch as the value of E_c varies only slowly with different profiles and doping in junctions useful for microwave amplification. This value is approximately a constant of the material selected, and for silicon, $E_c \approx 3 \times 10^5$ volts/cm.

The maximum voltage (V_m) which can be applied across a semiconductor junction of depleted width W (cm) is then

$$V_m = \eta E_c W \text{ volts} \qquad (1)$$

where $1/2 < \eta < 1$ for most junctions of interest. In particular, for the case where a $p^+ i n^+$ diode is used, $V_m \approx E_c W$. This relationship is used since it represents a practical approximate upper limit on V_m for a diode design.

The maximum current I_m (amps) that a junction is capable of handling is related to space-charge effects in the junction depletion region. The current flowing in a reverse-biased junction is given by $I = qV_{SAT}nA$, where n (no./cm^3) is the density of carriers in transit, V_{SAT} is the high field saturation velocity of carriers (cm/sec), and A is the junction area.

Since these carriers are not compensated, they form a space charge of width W and density qn (coulombs/cm^3) in the space charge region. The voltage drop across this uncompensated space charge is obtained from Poisson's equation by integrating qn/ϵ_{SiC} twice over W, resulting in a voltage drop equal to

$$\frac{IW^2}{2\epsilon_{SiC}V_{SAT}A} \quad \text{volts}$$

The maximum current in a semiconductor junction is thus that current which will result in a voltage drop across the depletion region which is on the order V_m, the maximum possible blocking voltage of the diode. Under these conditions, the field must approach zero somewhere in the depletion region and maximum saturation velocity cannot be maintained, an important constraint for GEISHA operation. Thus the maximum possible current is given by:

$$I_m = \frac{V_m}{2\,\dfrac{W^2}{\varepsilon_{SiC} V_{SAT} A}} \equiv \frac{V_m}{R_{SC}} \qquad (2)$$

the term $R_{SC} = W^2/2\varepsilon_{SiC}V_{SAT}A$ is defined as the junction space charge resistance (ohms). The peak power is then $V_m Im/4$ for an idealized ac signal.

The next step is to derive an expression for the maximum frequency f_m (sec^{-1}) and maximum impedance for the GEISHA device.

In the GEISHA, the load impedance Z_{load} is chosen such that the output time constant $Z_{load}\ C_{out}$ is equal to the transit time across the GEISHA depletion region (W/V_{SAT}) sec.* Under these optimum conditions, the maximum operation frequency is related to the inverse rise time by:

$$f_m \approx \frac{V_{SAT}}{2W}\ (sec)^{-1} \qquad (3)$$

Finally, because of this necessity of matching the output time constant to the transit time, the maximum load impedance of the device is essentially bounded by the capacitance impedance $1/\omega C$ associated with the junction depletion region width W and the frequency f_m:

$$Z_m = \frac{1}{2\pi f_m C} = \frac{W}{2\pi f_m \varepsilon_{SiC} A}\ \text{ohms} \qquad (4)$$

where ε_{SiC} is the dielectric constant of the semiconductor (farads/cm).

*Here we assume a lumped output impedance. Travelling wave structures relax the impedance matching of C_{out} and Z_L somewhat although the conclusions relative to the importance of E_c and V_{SAT} are unaffected for ultimate performance.

Combining Equations 1 through 4 into the Johnson PF^2Z figure of merit, it is found:

$$P_m f_m^2 Z_m = \frac{V_m^2}{4R_{SC}} \cdot \frac{V_{SAT}^2}{4W^2} \cdot \frac{2W^2}{2\pi V_{SAT}\varepsilon A} \tag{5}$$

and recalling that

$$V_m = E_c W$$

$$R_{SC} = W^2/2\varepsilon_{SiC}V_{SAT}A,$$

then

$$P_m f_m^2 Z_m = \frac{E_c^2 V_{SAT}^2}{4\pi} \tag{6}$$

The significance of Equation 6 is that the product of the three most important quantities of interest in microwave GEISHA devices is a constant of the material $E_c^2 V_{SAT}^2/4\pi$. The higher this constant for a given material, the greater the potential for this material for high frequency generation.