Report No.
TOR-469(5540-10)-1

STATE OF THE ART OF INTEGRATED CIRCUITS

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Contract No. AF 04(695)-469

10 September 1964

Prepared for

COMMANDER SPACE SYSTEMS DIVISION
AIR FORCE SYSTEMS COMMAND
LOS ANGELES AIR FORCE STATION
Los Angeles, California

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ABSTRACT

Integrated circuits are distinguished from thin-film and hybrid circuits. Current and probable future failure rates, performance, and physical characteristics are described. Yield and its relation to cost are discussed, as are other manufacturing and application considerations. High reliability, smaller size, and the ultimate low cost of high volume production are expected. Because of these factors the use of integrated circuits rather than thin-film circuits is predicted for all cases except the few for which they inherently lack the necessary performance.

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I. INTRODUCTION

Remarkable progress has been made in integrated circuit technology in the first six years of its existence. This circuit technique has come to be accepted as the dominant one of the future. For this reason, increasing numbers of companies refer to their circuits as integrated when, in reality, they are either types of thin-film or hybrid circuits. Some manufacturers who make true, integrated circuits have had to resort to calling them "monolithic" integrated circuits; it is these circuits that the author classifies as integrated circuits. A more proper name for the three techniques, classed as a group, is microcircuitry.

To avoid misunderstanding, in this report the following definitions apply: the term, integrated circuit, when used without the modifying words, hybrid or thin film, refers to the technique whereby the entire circuit is formed from a single-crystal chip of semiconductor material; the chip, itself, contains the various active and passive circuit elements. Thin-film refers to a circuit comprised of discrete elements that are deposited in layers and that have a common, passive substrate. The designation, hybrid, means a circuit that is formed by the combination of an integrated circuit with one or more discrete devices.

II. FAILURE RATE AS A FUNCTION OF TIME

A. DETERMINING A FAILURE-RATE MODEL

For many years reliability engineers have utilized a constant failure-rate (exponential distribution) model to describe the behavior of most electronic components. There are two primary reasons for this:

a. Tests established that within the useful life of equipment using these components, failures appear to be random.

b. From a statistical and testing viewpoint, the constant failure-rate model is the simplest to use.

Many engineers now doubt the validity of the first reason. Some recent tests have shown that transistors, capacitors, and other components have a decreasing failure rate, and that their behavior is best represented by the Weibull distribution,

$$F(t) = 1 - \exp\left[\frac{-(t-\gamma)^{\beta}}{a}\right]$$

where, for our purposes, γ, the location parameter, is zero; and β, the shape parameter, is less than one. If β were one, the Weibull distribution would simplify to the exponential distribution.

The Weibull distribution has two disadvantages. First, it has very limited flexibility, because failure rates are a function of time, and, second, there are diminishing returns on obtaining failures as test time is increased. The advantages of the Weibull model are the reduction in life test unit hours required to demonstrate reliability goals and the applicability of burn-in to improve reliability.

The primary problem in determining the most realistic failure-rate model is to accumulate enough test hours and failures under controlled conditions to discriminate statistically between different models. This is especially true of integrated circuits where tens of millions of test hours must be accumulated just to estimate the failure rate.

At present, the hypothesis that integrated circuits have a decreasing failure rate is based more on the nature of the technology than on test results. Many manufacturers believe that the nature of integrated circuit construction precludes any "wearout" during reasonable lifetimes, and that failures are traceable to weaknesses that existed in the circuit structure and should have been detected in most cases at final inspection.

The question of constant vs decreasing failure-rate models for integrated circuits will probably not be settled for several years, if ever. As failure rates are decreased to below 10^{-8} per hour, such questions will become more academic than important except, perhaps, to determine the advisability of integrated circuit burn-in.

B. ESTIMATED CURRENT AND FUTURE FAILURE RATES

Current standard integrated circuit failure rates appear to be between 1×10^{-8} and 5×10^{-8} per hour under laboratory conditions at 25°C. This estimate is for devices that have passed rigid environmental tests and optical and electrical inspection. Carefully designed custom circuits that are produced in volume should also approach this failure rate. The failure rate appears to be independent of circuit size and complexity.

Prediction of future failure rates is difficult because of the significance of the human factor in the manufacture of such high-reliability devices. Currently, many failures can be attributed to human error. This is especially true in such operations as optical inspection, handling, testing, and application. For these reasons, it is not expected that the failure rate will drop very much below 10^{-8} per hour, since the human factor will eventually become the primary source of failures. Automation is expected to improve the situation somewhat in the areas of device processing, but improper handling and application are expected to be continuing causes of failure.

III. FAILURE RATE AS A FUNCTION OF TEMPERATURE

All failures of integrated circuits or other semiconductor devices can be considered to manifest themselves as parameter degradations. Indeed, even catastrophic failures, such as open bonds, often forecast their imminent failure through parametric fluctuations.

A. MATHEMATICAL MODEL

The mathematical model that has been proposed to express parameter degradation, hence, failure rate as a function of temperature, is derived from the Arrhenius Equation, which is used by chemists to describe chemical reaction rates as a function of temperature. The usual form of the equation is $k = k_o \exp(-\epsilon/RT)$, where k is the reaction rate, ϵ is the activation energy, R is the universal gas constant, and T is absolute temperature.

Chemists have found that k_o is a constant for those reactions that proceed by a single mechanism. For bimolecular reactions, k_o must be taken as proportional to $\sqrt{T}$, while for more complex reactions, k_o must be proportional to T. However, in most cases, this linear or square-root dependence upon the temperature is usually negligible compared with the exponential factor.

If the Arrhenius Equation is modified for our use, we can combine ϵ and R into one constant, b, and consider k as the failure rate rather than a chemical reaction rate. This gives us the failure rate, $k = k_o \exp(-b/T)$. From the common log of both sides, we have

$$\log k = \log k_o - \frac{b}{2.3T}$$

This function will plot as a straight line with slope $-b/2.3$ on log-inverse paper if k_o is indeed independent of T, i.e., if the failure proceeds by a single mechanism. Empirical tests on integrated circuits have established that for a wide range of temperature ($25 \leq C \leq 300$), this is the case.

Furthermore, the value of b appears to be a constant ($b \cong 3358$) for most circuits tested; i.e., temperature accelerates the failure rate of all integrated circuits to the same extent. The value of k_o varies with the manufacturer, date of manufacture, and type of circuit. Test results from 1963 have placed the value of k_o between $10^{-1.5}$ and 10^{-3}. The value may be even smaller than 10^{-3} for circuits currently being manufactured.

Incorporation of these constants into the equation and expression as an exponential gives the failure rate per hour as $k = 10^{-[(1460/T)+a]}$, where $k_o = 10^{-a}$.

B. TEST RESULTS

In Fig. 1 are shown the results of two tests that were conducted to determine failure rate as a function of temperature (the solid lines representing Signetics data from October 1962 to February 1964 and TI data from 1962). Two other recent single-temperature test results have also been plotted. (Since no failures occurred in the MIT test of Fairchild circuits, the observed point actually represents the 50 percent confidence-level point.) A dashed line has been drawn through one of these – the Fairchild '61 - '64 datum point – with the same slope as the solid lines. This line probably represents the best failure rate that can be expected at any given temperature for integrated circuits being produced today. The curves should not be interpreted as reflecting relative differences between these manufacturers' abilities to produce reliable circuits. Instead, these variations are due primarily to differences in manufacturing dates and other tests the circuits are subjected to before being placed on life test.

In Fig. 2 is illustrated even more clearly the effect of temperature on the failure rate. With the adoption of 25°C as a norm, the curve shows the failure acceleration factor as a function of temperature. While some manufacturers specify the use of their circuits at temperatures as high as 125°C, data in Fig. 2 show that the expected failure rate at this temperature is 17 times the rate for 25°C. Thus, operating at low temperatures is as important a reliability consideration as derating is for conventional discrete devices.

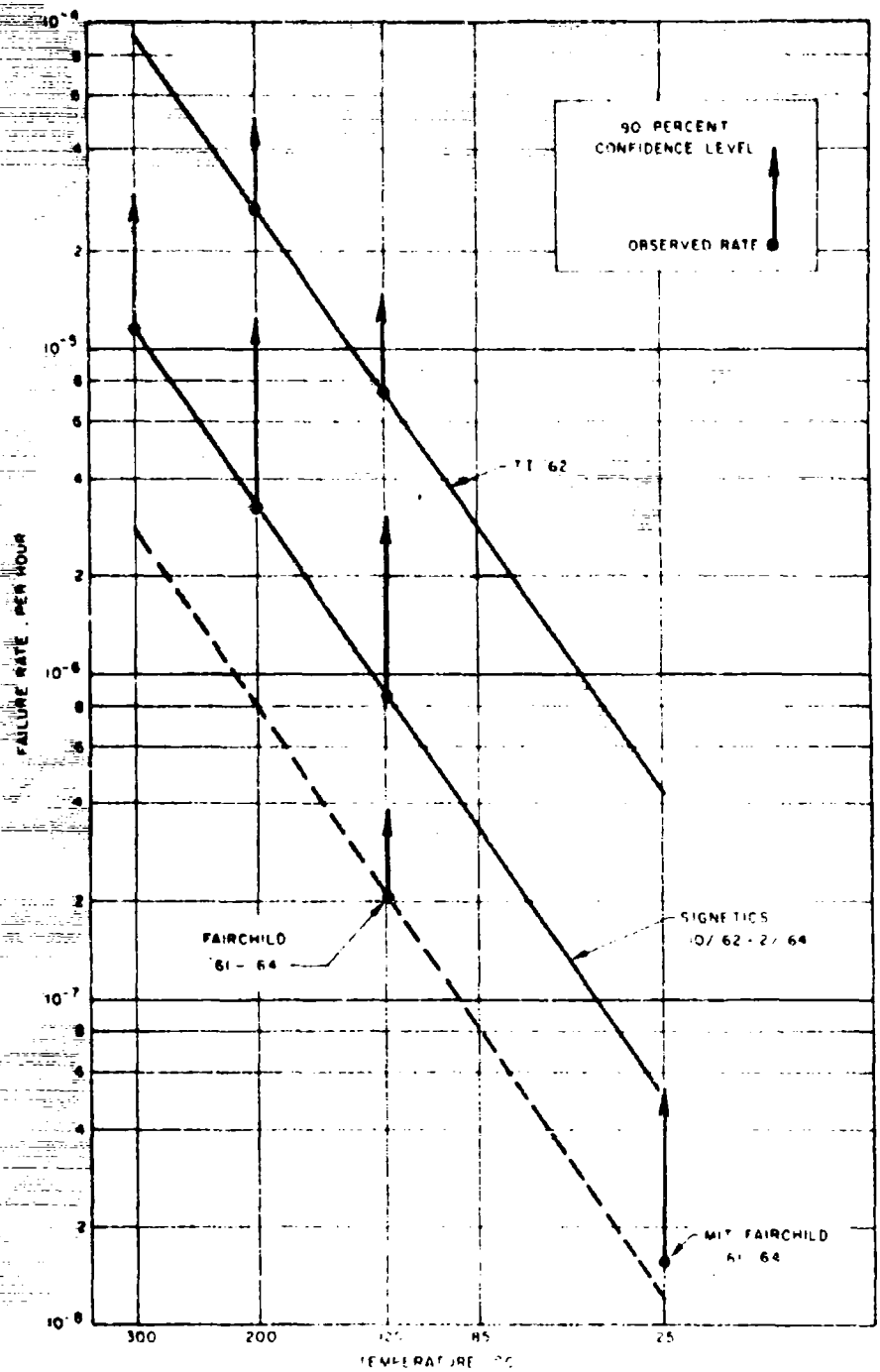

Fig. 1. Failure Rate as a Function of Temperature

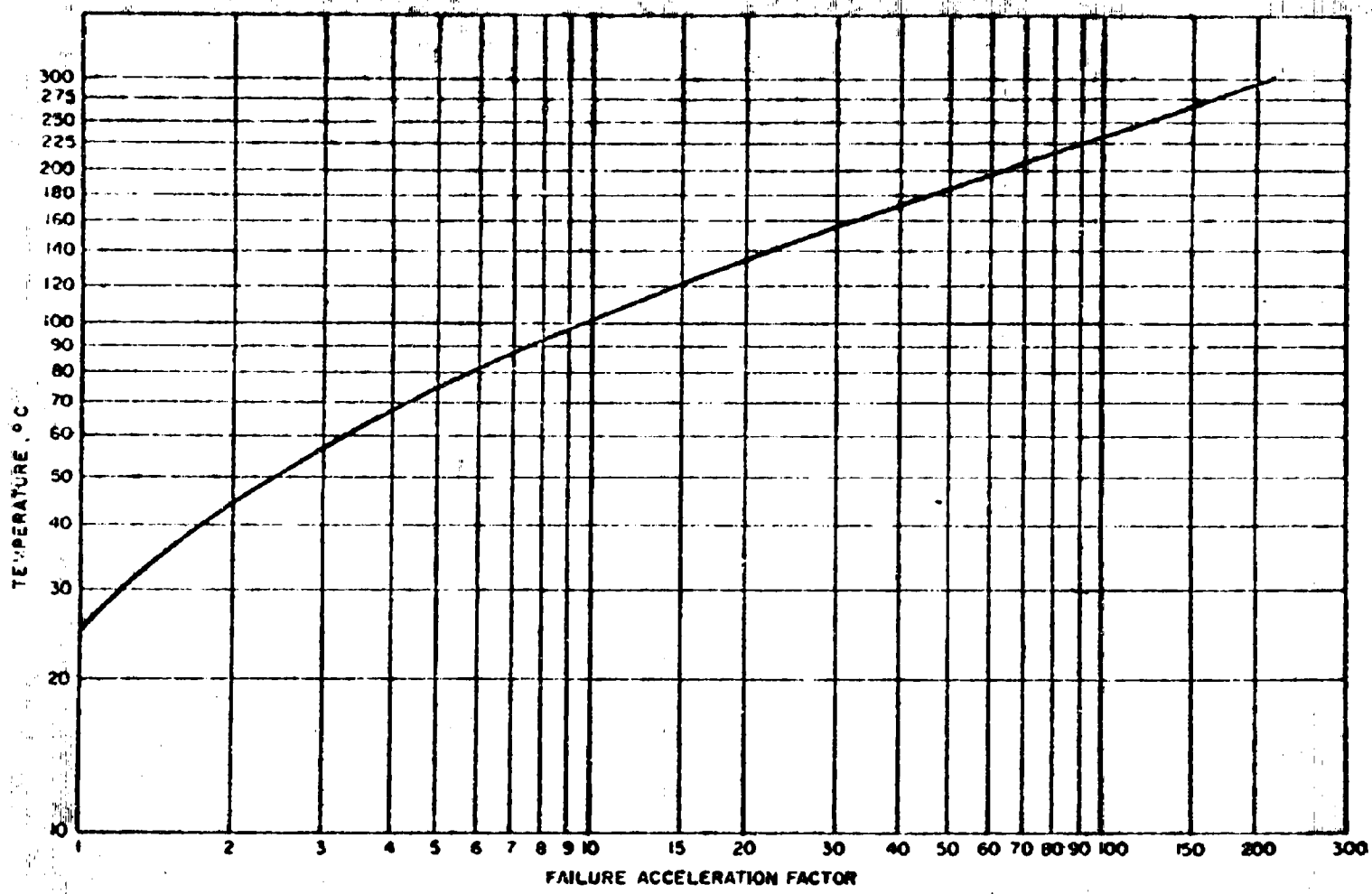

Fig. 2. Failure Acceleration Factor as a Function of Temperature

IV. PERFORMANCE AND CHARACTERISTICS

In the use of integrated circuits a considerable number of performance compromises must be made. Fortunately, most of them are not critical for digital computer circuitry.

A. VAILABLE ELEMENTS

Although a great deal of effort is being made, integrated circuit inductors are not expected to be developed within the foreseeable future. It appears that thin-film coils will have to be used in applications requiring inductance.

The values and tolerances of available resistors are somewhat limited in integrated circuits. A tolerance of 20 percent is nominal for integrated circuit resistors, primarily because of width variations resulting from chemical undercutting effects during processing. A 10-percent tolerance can be obtained by making the resistors twice as wide, but this requires four times the surface area for the same resistance and also increases parasitic capacitance. While absolute resistance tolerance is poor, this problem can often be circumvented by designing around resistance ratios where tolerances of 4 percent are easily maintained.

The total amount of useful resistance on an integrated circuit chip of nominal size is from 75,000 to 100,000 ohms at the 20-percent tolerance level. Needs in excess of this are most economically obtained via thin-film resistors. While improvements are being made to increase the resistance of integrated circuits, it does not appear that an increase by much more than a factor of two or three can be economically achieved in the future, unless there is a major breakthrough in the technology or a thin-film technique is used.

Most integrated circuit capacitors use thermally grown silicon dioxide as a dielectric to avoid the lower Q, voltage sensitivity, and low-breakdown voltage of diffused junction capacitors. Silicon dioxide capacitors have a breakdown voltage of about 50 volts and a value of approximately 0.3 pf/square mil. The total value of useful capacitance available on a typical integrated

circuit chip is from about 150 to 200 pf. For capacitance much greater than this, some type of thin-film technique should be considered.

B. SPEED

The speed of operation of integrated circuits has been increasing rapidly. In the past few years, the rate has doubled every year. Currently available logic stages operate in the 15-nsec propagation delay time range; integrated circuit speed is being limited by the parasitic capacitance between the junction-isolated portions of the circuit and the substrate.

A buried-layer process, in which an extra n+ layer is diffused between the p-type substrate and the n-type collector, has reduced the propagation delay time for diode-transistor logic (DTL) to a range of from 10 to 15 nsec. This technique shunts the high-resistance collector sheet to the substrate and allows a reduction in the epitaxial layer thickness; results are a 50-percent reduction in parasitic capacitance and the higher speed.

Later this year, a new technique will reach the production lines whereby a thin isolating barrier of silicon dioxide will be used between the substrate and transistor to essentially eliminate the parasitic capacitance. This development will enable integrated circuits to break the 10-nsec propagation delay time barrier for DTL logic, which places them in the same class as hybrid and discrete circuits. This isolating barrier will also allow integrated circuits to have radiation-resistant characteristics equivalent to those of thin-film circuits. At present, integrated circuits are somewhat more sensitive to radiation than thin films, due to the breakdown under radiation of the back-biased diodes now used in junction isolation.

C. VOLTAGE AND POWER LIMITATIONS

Usually, the voltage limitations of integrated circuits are not a problem for digital circuits, except perhaps at interfaces with other types of circuits. Power is currently in the 3- to 5-milliwatt range for digital gates and is generally traded off somewhat for increased speed. Maximum power dissipation for integrated circuits is a few-hundred milliwatts and special consideration must be given to applications requiring more than this.

V. PHYSICAL ASPECTS

A. SIZE AND COMPLEXITY

Today, most standard-line integrated circuit chips measure from 35 to 70 mils on a side. Since they are processed from a 1-inch-diameter wafer, there are approximately 150 to 600 circuits per wafer. When special circuits are considered, the number per wafer varies from less than 50 to about 1000. While circuit chips can be made almost any size, experience has shown that yield is exponentially related to chip area and that chip sizes less than a 20-mil square are too difficult to handle and process.

As the technology improves and process tolerances are reduced, the yield-size relationship will encourage chip size reductions toward the 20-mil square lower limit. In from three to four years, circuit functions are expected to occupy only between 10 and 20 percent as much chip surface as they do today. This reduction will take two forms. First, the highly complex circuits now being placed on larger chips will gradually decrease in size as the resolution with which circuits are built is improved. This will result not only in smaller chips--but also in the surface efficiency (the amount of silicon chip utilized) being increased.

The second reduction will come from more complex circuits being placed on a single chip. Interconnections between the chips currently cause size, weight, and reliability problems. Reduction of the number of chips in a subsystem by placing more circuit functions on a single chip drastically reduces the number of interconnections required. Logic gates, flip-flops, and adders are now being placed on a single chip. Within a year, shift registers and decade counters will be produced in quantity. Within about three years, combinations of these circuits will be built on the same chip.

Since integrated circuit economy depends upon a large volume of like circuits, complexity is not expected to go much beyond the point of placing two different types of circuits on the same chip. More complex circuits would be too specialized for them to be used in quantity.

B. WEIGHT

Typically, the use of integrated circuits has reduced the weight of subsystems by a factor of from 5 to 10. Some of this reduction was achieved because integrated circuits are lighter than the discrete components they replace. Most of the reduction in weight is due to the fact that the subsystem has fewer circuit boards, plugs, interconnections, and a smaller case.

In the future, the weight is expected to be saved almost entirely from reduced packaging weight. Reduction in the size of integrated circuits will not contribute significantly to this saving, but the incorporation of several circuit functions on a single chip will. In a few years, when more complex circuits are integrated on a single chip, weight reduction by a factor of about 2 can be expected for integrated subsystems.

C. PACKAGING

Integrated circuits are packaged in one of two ways: a modified metal transistor header or a flat pack.

1. THE TRANSISTOR HEADER

This type of package, similar to a TO-5 can, is typically 3/8 inch in diameter, about 1/4-inch high, and has 8 to 12 pins. There is usually some variation in height, depending on the type of circuit. Another header used is 1/4 inch in diameter, 0.075-inch high, and similar to the TO-47 can.

The transistor header package was introduced first. It has the advantages of a long history in the transistor field, high yield, relatively low cost, and can be easily sealed.

2. THE FLAT PACK

The flat pack is typically 1/4 by 1/4 or 3/8 by 1/8 inch with a thickness of from 0.04 to 0.06 inch and has 8 to 14 leads. It is usually constructed of glass or similar material and has a higher breakage and seal failure rate because of this. However, the flat pack is smaller, lends itself more easily to the use of a larger number of leads, and is easier to arrange in the

subsystem package. High customer demand and success in reducing the breakage and seal problem are expected to result in a marked volume advantage for them by the end of the year. Considerable effort is being made to make them less fragile and more easily processed.

VI. YIELD

Currently, the factor of yield has the greatest influence on the economics of integrated circuits. There is considerable controversy and mystery concerning yield, partly due to its many definitions. The general definition of yield is the ratio of potential circuits that can be successfully processed through a series of manufacturing steps to the total number of potential circuits that can begin the process.

A. TYPES OF YIELD

The problem of yield arises because of the different points that are chosen for the beginning and end of the process cycle. Some consider the freshly cut wafer as the starting point, others the first diffusion. Among the various end points selected are: immediately before scribing, prior to packaging, after final inspection. In a certain sense, it may seem that over-all yield is the most important one. However, the later a failure occurs in the processing cycle, the more expensive it is, since all the previous processing has been fruitless. This is especially true in such final steps as scribing, packaging, and final testing. Thus, the determination and control of the yield are necessary all along the line for process improvement.

B. FACTORS AFFECTING YIELD

Yield has been lower for integrated circuits than for other semiconductor products. A year ago, most manufacturers of integrated circuits were operating at well under 1-percent over-all yield. Yield is not only an unknown complex function of all the processing parameters, but in general depends on the abilities and conscientiousness of the semiskilled labor operating the process facilities.

Such occurrences as a slight variation in oven temperature or careless procedures in a clean room can easily ruin thousands of dollars of partially processed circuits. Each oven has its individual characteristics and a switch in operators can cause a yield drop for several batches until the new operator

obtains a feel for the oven. Often a company will use a set of pilot ovens to determine the feasibility of a new custom circuit. When all modifications have been made and a prototype has been produced, the production run will be made in a new set of ovens by different operators. Yield problems are especially critical at times like these and often account for the increased price and longer delays in obtaining custom circuits.

In a sense, yield is more important for integrated circuits than for other types of semiconductor devices because for most semiconductor devices, poor yield usually results in a product which, although it does not meet desired specifications, can normally be marketed as a lower grade at a lower price. In the case of integrated circuits, poor yield usually results in a device with little or no market value.

C. CURRENT STATUS

Today, due to technological improvements, integrated circuit yield is comparable with that of the most critical discrete transistors. It is sufficient to enable most companies to make a profit and to supply the needs of industry. The exact figures are not released, however, primarily because they would disclose a company's competitive position, i.e., how much they can reduce prices and still make a profit.

It is not the industry's goal to perfect its processes so as to obtain 100 percent yield. Certain techniques are available for increasing yield, which are not cost effective. Integrated circuits are produced in such large quantities that maximum economy is achieved when a reasonable yield is obtained at moderate process cost.

VII. COST

A. CURRENT PRICES

The retail cost of integrated circuits has been dropping rapidly. Price depends primarily on circuit complexity, order size, and on whether the circuit is one of a standard line or requires a custom design. For quantities in the 200 range, prices vary from $ 7 to $17 for diode arrays up to $75 for one-shot multivibrators in standard line TO-5 configurations. Other indicative prices for computer circuits are: single gates, $12 to $17; line drivers, $21 to $50; registers, $29 to $55.

These circuits meet military specifications (-55° to 125°C). Circuits for commercial or industrial applications (15° to 55°C) typically sell for from one-third to one-fifth the cost indicated above.

B. EFFECTS OF ORDER SIZE AND PACKAGE TYPE

Cost varies considerably with the size of the order. When masking and other fixed costs can be spread over thousands of circuits, the per-unit cost drops sharply. For orders in the range of 100,000, the cost is likely to be less than half that of small orders. Most manufacturers do not list prices for quantities greater than several hundred. For larger orders, they prefer direct negotiation between the factory and customer.

Standard prices usually refer to the TO-5 package. Flat packs cost up to about 20 percent more. They are inherently less expensive to manufacture, but yield has been low resulting in higher price. Most customers prefer the flat pack configuration. Improvements in the technology (especially in lead strength and better sealing), along with the greater demand, are expected to result in a flat-pack transistor-header price cross-over by the end of 1964.

C. FACTORS THAT WILL REDUCE COST

The largest factors in cost are yield and packaging. The cost today of processing in quantity a moderately complex circuit up to the point of packaging is less than three cents, assuming 100 percent yield. While major

circuit function cost reductions in the future will come from increased yield and improve packaging, another factor which will significantly reduce integrated circuit costs is improved circuit resolution. Packaging cost is fairly independent of circuit complexity, and yield is influenced mostly by circuit size, not complexity. Thus, better circuit resolution will eventually allow more complex circuits and multiple function circuits to be placed on a chip no larger than that currently used, with little effect on device price. Hence, the price per circuit function will drop appreciably. There will also be moderate reduction in price due both to increased production as more systems are integrated, and increased competition as the integrated circuit supply exceeds industry's demands.

By the end of this decade, the above factors will cause the price of integrated circuits of the complexity used today to be reduced by another order of magnitude. Thus, in many cases, prices of less than a dollar a circuit function will be achieved. However, for many applications, price reduction per circuit function will not be reflected in price reductions per device due to the tendency to make more complex circuits and multiple circuits on a single chip as the technology develops.

VIII. THIN-FILM TECHNIQUES VS INTEGRATED CIRCUITS

As pointed out in previous sections, there are performance levels beyond which integrated circuits are not capable of operating at this time. In addition, there are certain situations in which it is not economical to use integrated circuits. Often, in each of these cases, the solution is either to utilize some type of thin-film technique, or a combination of thin-film and integrated circuits.

A. RELIABILITY

The principal advantage of integrated circuits over all other techniques, including thin film, is improved reliability. This is obtained chiefly through the elimination of interconnections and a reduction in the number of individual elements required. In general, any type of thin-film technique requires more interconnections and interfaces than do integrated circuits.

B. FLEXIBILITY AND CAPABILITY

Thin-film techniques gain most of their current advantage from increased flexibility and capability. High isolation between elements is more easily achieved, and closer tolerances can be obtained for resistors (1 to 5 percent) and capacitors (5 to 10 percent). Passive elements with low temperature coefficients and semiconductors with closely controlled parameters can be produced. Thin-film techniques allow add-ons and circuit modifications to be incorporated with little tooling change or time delay. Their power dissipation capability is usually several times better than that for integrated circuits.

C. COST

The economic tradeoff between thin-film circuits and integrated circuits is complex. If the circuit must be custom designed, thin films are generally less expensive for quantities up to 1000 or so. For larger quantities, the integrated circuit masking costs (about $5000) and other fixed costs are spread out over enough circuits for the per-unit cost to be lower than for thin-film.

However, when the circumstances are such that standard integrated circuits can be used, the price advantage is usually with integrated circuits, even for relatively small quantities. As the integrated circuit product lines expand and prices drop, it is expected that thin-film circuits will be used only in cases where integrated circuits lack the necessary performance.

IX. SUMMARY

A FAILURE RATE

Standard integrated circuits produced today have a failure rate approaching 10^{-8} per hour under benign conditions. Sufficient data is not available to determine whether this failure rate is constant or is decreasing with time. The failure rate increases logarithmically with the inverse of absolute temperature. At normal operating temperatures, this relationship can be approximated by doubling the failure rate for each 20°C temperature rise.

B. VALUES AND TOLERANCES

The values and tolerances of integrated circuit resistors and capacitors are somewhat limited, but this is usually not a problem for digital circuitry. Integrated circuit logic speed is currently approaching the 10 nanosecond propagation delay point. Further improvements will result from new manufacturing processes now being introduced. Power dissipation and voltage limitations are not serious problems for digital applications, but they can be troublesome in analog circuits.

C. INTEGRATED CIRCUIT CHIPS

Integrated circuit chips are usually square and vary from 20 to 80 mils on a side. Improved processing resolution is expected to result in some reduction in chip size and the inclusion of several circuit functions in a single chip. Integrated subsystems are typically only 10 to 20 percent as heavy as their discrete circuit counterparts. Much of this improvement is due to the reduction in the number of circuit boards, interconnections, and the use of a smaller case.

D. TRANSISTOR HEADERS VS FLAT PACKS

Currently, integrated circuits are being supplied in transistor headers and flat packs. Although they are currently more expensive because of their lower yield and higher breakage rate, eventually, the flat packs are expected

NOT REPRODUCIBLE

to dominate the market due to their smaller size, increased flexibility, and ultimate lower manufacturing cost.

E. YIELD

Yield is the governing economic variable in the integrated circuit manufacturing process. Due to the newness of this complex technology and its reliance on semiskilled labor during several critical process steps, yield has been lower for integrated circuits than for other semiconductor products. However, within the last year, technological improvements and manufacturing experience have advanced the state-of-the-art sufficiently to enable most companies to meet demand and make a profit.

F. PRICE

The price of integrated circuits depends primarily on circuit complexity, order size, and whether the circuit is in a standard line or a custom design. Before the end of this decade it is expected that improved packaging, increased yield, and better circuit resolution will drop the price of integrated circuits by an order of magnitude. In many cases, prices of one dollar per circuit function will be realized.

G. ADVANTAGES OF INTEGRATED CIRCUITS

The primary advantages of integrated circuits over thin-film techniques are higher reliability, smaller size, and a lower high-volume cost. The use of thin-film techniques provides more flexibility or capability in the areas of circuit design and modification, element tolerance, and power dissipation. Thin films will ultimately be used only in cases where integrated circuits lack the necessary performance.

APPENDIX A

INTEGRATED CIRCUIT CONSTRUCTION

There are several different series of techniques used in integrated circuit construction, especially in regard to the types of diffusions used. The Fairchild planar epitaxial is typical of the construction being used in production runs by most manufacturers. Planar denotes that all junctions of the circuit are terminated on one plane, i.e., on one side of the substrate. Epitaxial refers to a single crystal layer of doped silicon grown upon a silicon substrate in an oven, usually by the hydrogen reduction of silicon tetrachloride. Following are the steps used in this construction.

1. WAFER PREPARATION

This process is begun by cutting 0.01-inch slices of p-type doped silicon from a 1-inch-diameter crystal cylinder. The wafers are then lapped, polished, and chemically etched until they are smooth and have a thickness of about 5 mils. Next, the wafers are placed in a high-temperature furnace having an oxidizing atmosphere. The oxygen combines with the surface silicon to form an encapsulating and passivating layer of silicon dioxide.

2. MASKING PRODUCTION

For each diffusion and deposition process, a high resolution mask has been made. This is achieved by first drawing the desired pattern to a scale many times actual size. The drawing is then photographically reduced and duplicated repeatedly until the final mask for the particular process has hundreds of identical tiny patterns that correspond to the circuits to be made from a single wafer.

3. INITIAL DIFFUSION

The wafers are coated with a photosensitive material in the absence of light and then exposed through the high resolution collector cut-out mask.

The portions not exposed (due to the opaque pattern on the mask) are soluble and removed by a special rinse. The exposed portions are not removed by the rinse and resist the etch, which is used to remove the protecting silicon dioxide layer from the unexposed portions of the wafer.

Next these wafers are placed in a high-temperature furnace that contains an n-type dopant. This impurity diffuses into the surface of the wafers where the silicon dioxide has been removed. These highly doped n+ diffusion areas are the transistor collector portions of the circuit.

4. EPITAXIAL GROWTH

Next, an epitaxial layer is grown over the entire wafer surface, by first removing the passivating silicon dioxide layer with an acidic etch. The wafers are returned to a furnace where, through chemical reactions to volatile gases, n-doped silicon is grown on the wafer surface. This layer assumes the same crystal orientation as the p-type wafer substrate, and it actually becomes an extension of this material. The thickness and resistivity of this layer are chosen to meet the needs of the particular circuit being formed. Following this growth, a new passivating layer of silicon dioxide is grown in preparation for the next diffusion.

5. ISOLATION DIFFUSION

The next step is the isolation diffusion. In this process, bands are etched through the silicon dioxide surface in such a manner as to separate the different portions of the circuit from one another. The wafers are then placed in a furnace containing a p-type dopant that diffuses through the exposed epitaxial n-type region and extends through to the substrate. This diffusion isolates several pockets of n-type material from each other in each circuit, which become transistor or resistor regions as the circuit is formed. During this diffusion, a new protective layer of silicon dioxide is formed over the wafer.

6. BASE, RESISTOR, AND EMITTER DIFFUSIONS

Following this diffusion step the wafer is etched for simultaneous base and resistor diffusion. A p-type impurity is diffused into the epitaxial layer to form the base collector diode in the transistor regions, as well as all of the resistors in the resistor regions. The oxygen atmosphere of the furnace re-oxidizes the exposed portions of the surface, preparing the wafer for the next step.

The next, and last, diffusion step is for the emitter. After etching, an n-type impurity is introduced into the furnace to form the emitter regions and the topside collector contacts. As before, a new layer of silicon dioxide forms to seal the surface. Now, all of the regions have been formed. The next step is to intraconnect them to form the desired circuit.

7. INTERCONNECTIONS

The first step in forming the intraconnections is that of photoengraving holes over the appropriate regions of the device in order to make contact with the different portions of the circuit. Then the wafers are placed in a high-vacuum oven containing a metal evaporator. Aluminum is boiled from a hot filament and forms a thin coat over the entire wafer surface. After removal from the oven, the wafer is selectively etched to leave a pattern of intra-connections between the various circuit elements. The wafers are placed in an alloying oven to assure good electrical contact with the circuit elements. This completes the deposition and diffusion processes.

8. FINAL PROCESSING

A diamond scribe is used to cut the wafers into individual circuits. The dice are cleaned and inspected individually for defects, and then soldered to the center of the header using a high temperature alloy. Fine gold wires are thermal-compression bonded to the contact regions of the dice and then spot-welded to a header post. Final optical inspection and capping the header are the last steps before the circuits undergo electrical and environmental tests.

APPENDIX B

THIN-FILM CONSTRUCTION

Thin films are deposited in a variety of ways. Five currently popular methods are: vapor plating, vacuum deposition, cathode sputtering, electrochemical techniques, and silk screening. Brief descriptions of these techniques follow.

1. VAPOR PLATING

Vapor plating is used primarily for semiconductors, oxides, and refractories. The material to be deposited must be easily vaporized. The vapor is mixed with other gases and passed over the surface to be plated. The target surface is heated to a temperature high enough to cause a chemical reaction. The principal advantages of this technique are that oxides can be deposited at relatively low temperatures and compound semiconductors can be epitaxially grown. In addition, vapor plating results in more stable, and less porous, depositions for many materials than do other plating techniques.

2. VACUUM DEPOSITION

Vacuum deposition requires a heating source such as an electron gun or resistance heater in a high vacuum. The heating source evaporates the material, which rises through a template to be deposited in the designed pattern on the substrate above. The substrate may be active or passive. Vacuum deposition is a convenient method of evaporating a wide range of metals, cermets, and dielectrics.

3. CATHODE SPUTTERING

Cathode sputtering is used to deposit refractory metals at room temperature in spite of their characteristically low vapor pressures and high melting points. In general, sputtering is slower than other deposition techniques, but its advantage lies in the capability of depositing metals of superior stability,

which cannot be practically accomplished with other techniques. The material is deposited in the following manner: A chamber is filled with inert gas at a low vacuum. The material to be deposited serves as a cathode at several thousand volts below the substrate material, which is the anode. This causes ionized gas molecules to bombard the cathode and dislodge its atoms, depositing them through a mask onto the substrate. This process is used for the formation of resistors and capacitors.

4. ELECTROCHEMICAL TECHNIQUES

Electrochemical techniques (electroplating) are used to deposite metals for resistors, electrodes of capacitors, and conducting strips. Photoresist techniques are normally used to obtain the desired pattern on the substrate. The advantages of these techniques are very high accuracy, both in width and thickness of deposition, and the simplicity of the conventional electroplating equipment used.

5. SILK-SCREENING

Silk-screening, the direct application of circuit materials on a substrate through a mask, is used for the deposition of high-resistivity, high-stability compounds at temperatures in the range of from 600 to 800°C. Tolerances of 5 percent after deposition are further refined by abrasive tailoring. Capacitors having thick dielectrics and low capacitance per unit area are also deposited in this manner. The technique is usually confined to the production of passive networks.