

**RESEARCH AND DEVELOPMENT**

**OF**

**HIGH SPEED PROCESSOR ARRAYS**

Prepared by  
Philco-Ford Corporation  
Microelectronics Division  
Blue Bell, Pennsylvania 19422

For  
Massachusetts Institute of Technology  
Lincoln Laboratory

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FIFTH INTERIM REPORT  
August 1970

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OF  
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For  
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## ABSTRACT

This report describes program progress during the eight-month extension period of a research and development program directed toward the development of high performance, digital, MSI-LSI microcircuits and their application in feasibility studies of high speed data processing systems.

The tasks of this report period included the fabrication of a high speed 80-gate array with three levels of metallization and the performance evaluation of a high speed ( $<1.0$  nsec), low power ( $<15$  mW), ECL gate design, for various on-chip gate loading conditions. Both tasks were completed.

Also required was the fabrication and delivery of three different, custom, ECL Two-Bit Fast Carry Gated Adder microcircuits (two levels of metallization) for application in a high speed  $17 \times 17$  Array Multiplier. A total of 136 adders are required for the multiplier. The required number of adders were delivered and the multiplier which was assembled using those adders functioned properly. The time required for the multiplier to perform its function was measured to be 40 nsec, a 10-nsec improvement over the expected time.

Accepted for the Air Force  
Joseph R. Waterman, Lt. Col., USAF  
Chief, Lincoln Laboratory Project Office

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## I - INTRODUCTION

### 1.1 SCOPE OF REPORT

This report describes the work performed by Philco-Ford during the eight-month extension to a program entitled "Research and Development of High Speed Processor Arrays." This program was conducted under subcontract with MIT Lincoln Laboratory. (The prime contract, sponsored by the U. S. Air Force, is No. AF19(628)-5167.) A summary report covering the first twelve months of the program was published in December 1969.

### 1.2 PROGRAM GOALS

The goals of the eight-month extension to the program were:

1. Evaluate the performance of an optimized high speed, low power ECL gate (which was designed during the previous program period) under various intrachip loading conditions. This task was to be accomplished through fabrication and proper interconnection of the 80-gate Processor Master Array which was also designed during the previous program, incorporating the optimized gate. The resultant chip was called the Processor Loading Test Chip.
2. Fabricate and evaluate a 4-bit Adder Chip. The Adder Chip was also designed to be formed through

custom interconnection of the 80-gate Processor Master Array.

3. Fabricate and deliver three versions of a custom designed, high speed 2-bit Fast Carry Gated Adder Chip. A total of 136 packaged adders were to be delivered.

The Processor Loading Test Chip and 4-bit Adder have three levels of metallization, while the 2-bit Adders have two levels of metallization. All the chips have 0.1-mil geometries and shallow diffusions ( $\sim 0.6$ -micron base depth) in order to obtain high speed performance.

The layout designs for all of the complex chips in this program resulted from a cooperative effort between MIT Lincoln Laboratory and Philco-Ford, with final mask layout being done by MIT Lincoln Laboratory. Layout designs for the two 80-gate chip designs were generated using computer aid.<sup>1</sup> Photomasks were produced using commercial equipment for pattern generating and photorepeating. Artwork for the custom 2-bit Adders was generated at 1000X using a taping technique. Photomasks were generated by conventional optical reduction and photorepeating techniques.

## II - PROGRAM DEVELOPMENTS

### 2.1 PROCESSOR LOADING TEST CHIP

#### 2.1.1 Evaluation of Processor Basic Gate for Various Intra-Array Loading Conditions

During the initial twelve-month period of the program "Research and Development of High Speed Processor Arrays," several ECL gate designs were evaluated for speed-power properties in order to obtain an optimum gate for use in microcircuit arrays in high speed computer circuits. This evaluation was made for on-chip fanin and fanout of one, using a test chip<sup>2</sup> referred to as the SMX14. A gate design which performed with a propagation delay,  $\tau_{pd}$ , of 0.6 to 0.8 nsec at 12 to 15 mW (complementary outputs) dissipation was selected and used to design an 80-gate multipurpose array called the Processor Master Array (SMX17). The Processor Master Array is simply a matrix of optimized gates and reference bias circuits which can be interconnected to form any of a number of complex functions. Figure 1 is a schematic diagram of the Processor basic gate. Figure 2 is a photomicrograph of the basic gate. Figure 3 is a photomicrograph of a Processor Master Array to which a first-level metal interconnect pattern has been applied.

The first task of the eight-month extension to the program was to evaluate the speed performance of the Processor basic gate

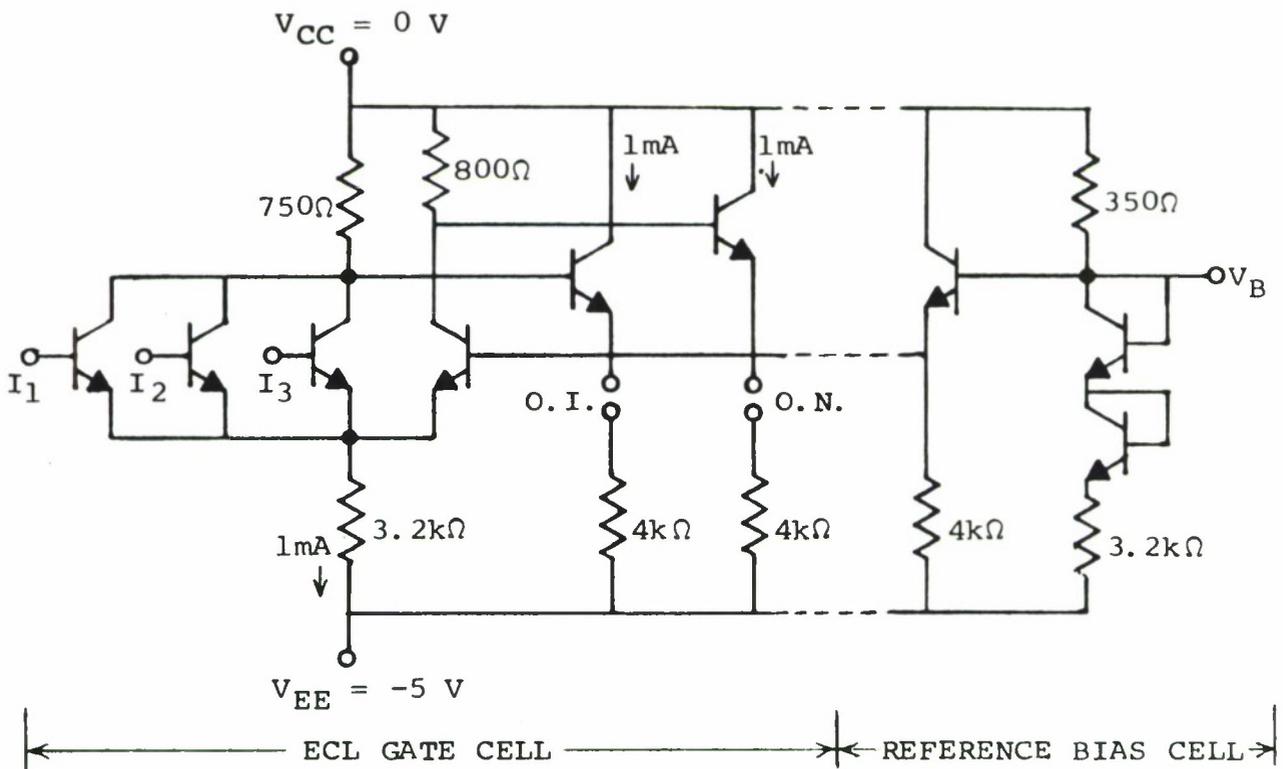


Figure 1. Schematic diagram of the Processor basic gate and reference bias circuits.

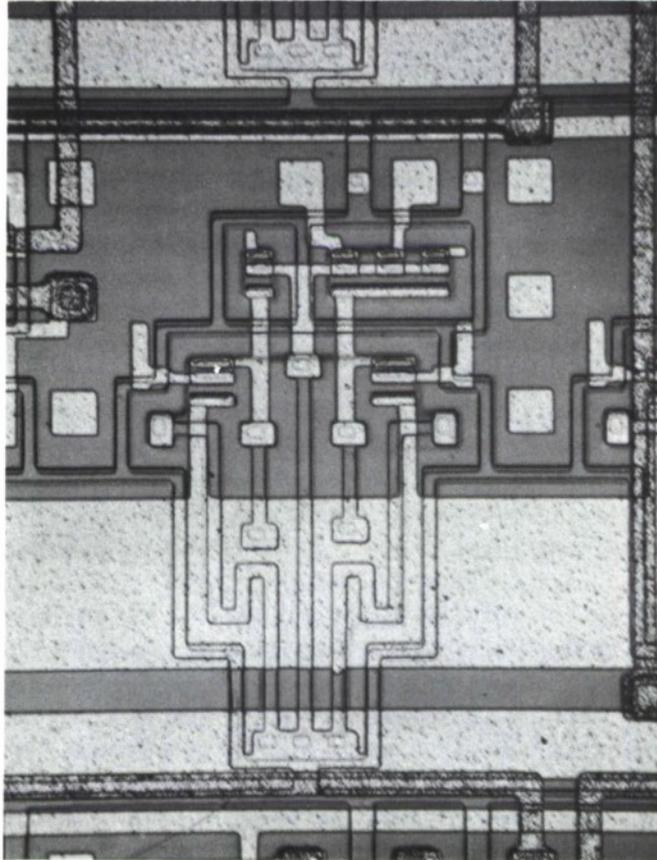


Figure 2. Photomicrograph of the Processor basic gate.

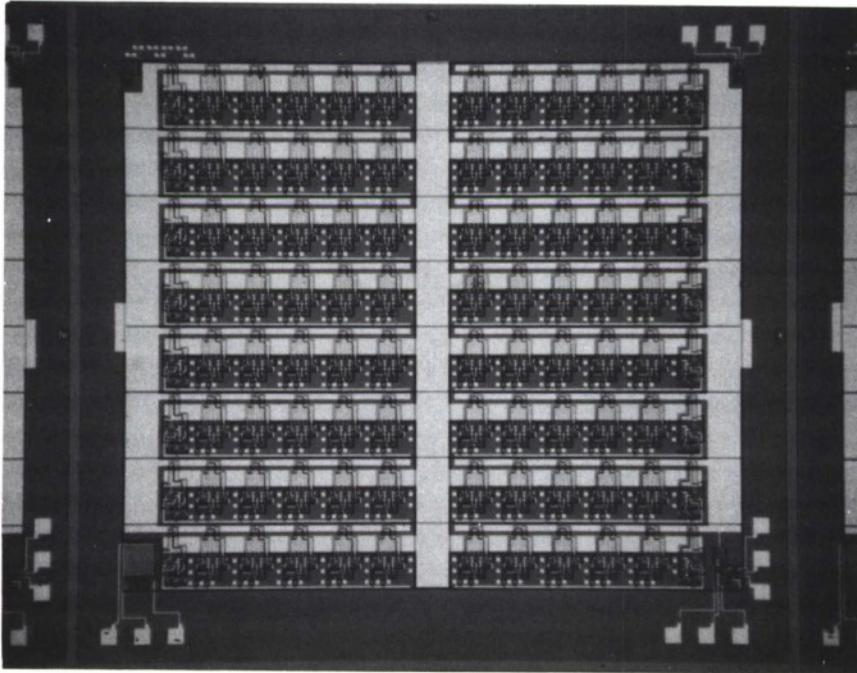


Figure 3. Photomicrograph of the Processor Master Array Chip.

under various representative intrachip loading conditions which the gate would typically experience in anticipated functional applications. To accomplish this, an appropriate multilevel (3 levels) interconnection structure was designed for the 80-gate Processor Master Array. The resultant chip is referred to as the Loading Test Chip. The Loading Test Chip essentially consists of four test configurations referred to as "gate test chains;" these gate test chains are listed in Table I along with the output which is tested and the loading conditions of the test.

TABLE I

TEST CONFIGURATIONS CONTAINED ON THE LOADING TEST CHIP

Gate Test Chain	Output Tested	Loading Conditions	
		Fanin	Fanout
D	Inverted ( $O_I$ )	1	1
C	Noninverted ( $O_N$ )	1	1
B	Noninverted ( $O_N$ )	1	7
A	Noninverted ( $O_N$ )	7	1

Figure 4 is a functional representation of the gate test chains. The gate test chain technique for measuring gate

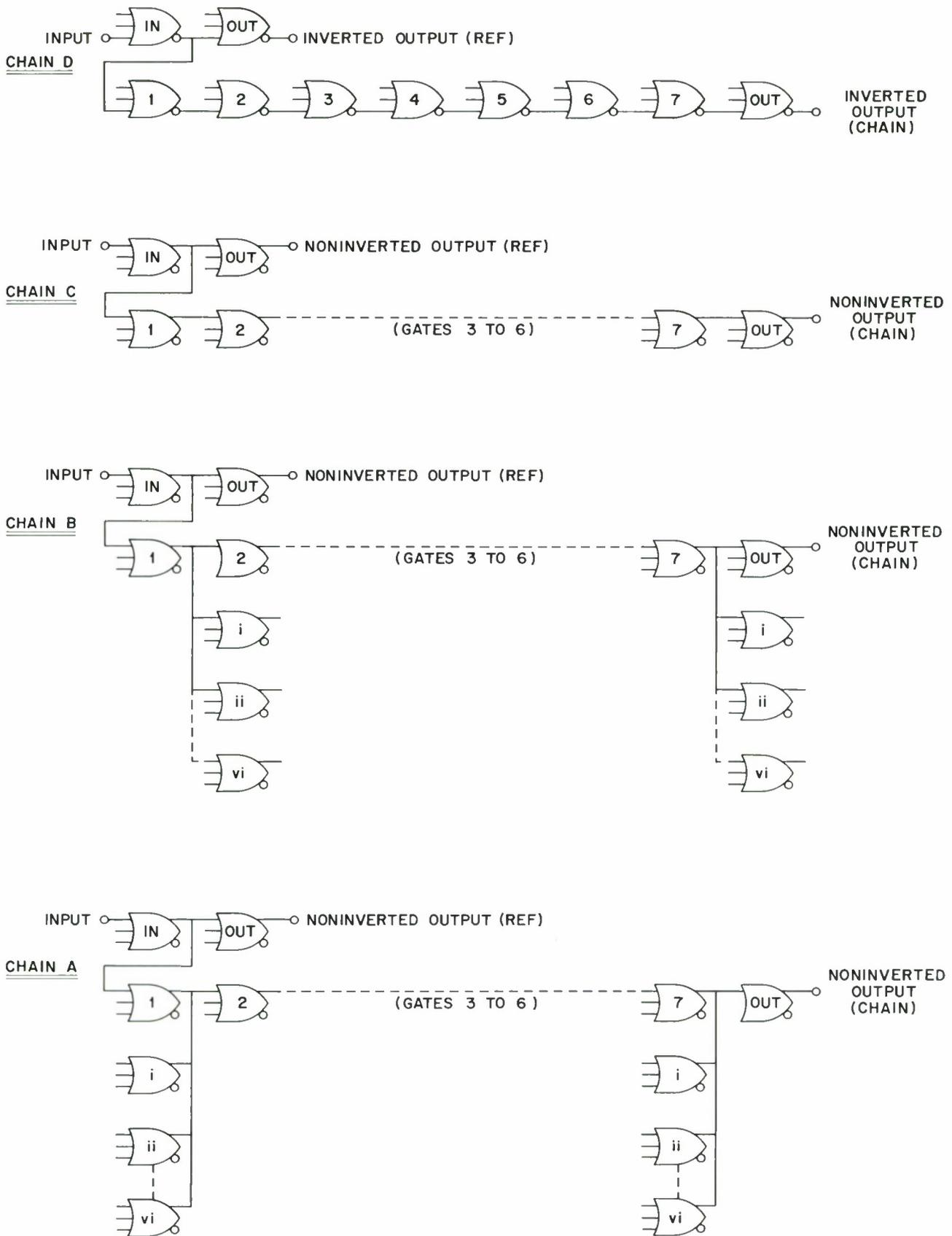


Figure 4. Functional representation of the 4-gate test chains contained on the Loading Test Chip.

propagation delay had been developed during the initial twelve-month period of the program and discussed in the Fourth Interim Summary Report.<sup>2</sup> The technique is significant because it measures gate propagation delay independent of the loading effects of the test equipment; therefore the technique gives the true on-chip gate propagation delay. Referring to Figure 4,  $\tau_{pd}$  per gate for each loading configuration is obtained by the equation

$$\tau_{pd} = \frac{\tau_{pd}(\text{Chain}) - \tau_{pd}(\text{Ref})}{7}$$

One lot of Loading Test Chip wafers was fabricated and evaluated. Resistor values and operating currents were within 4% of the design values shown in Figure 1. A group of eight packaged Loading Test Chips from this lot was delivered to Lincoln Laboratory for final evaluation. The results of propagation delay measurements made on these devices are given in Table II. The  $\tau_{pd}$  data represent an average of the values obtained on the eight chips evaluated. From Table II, it is seen that the gate delay for fanin and fanout of 1, for both gate outputs, lies well within the design goal of <0.8 nsec. Furthermore, the data indicate that with a fanin of 7 or a fanout of 7 (the maximum fanin or fanout conditions anticipated to be

necessary in high speed Processor Chips), the gate delay is less than 1.3 nsec in the slowest transient condition.

TABLE II

PROPAGATION DELAY DATA FOR THE PROCESSOR BASIC GATE  
OBTAINED FROM THE SMX176 LOADING TEST CHIP

Gate Chain	Wired Fanin	Fanout	Avg $t_{pd}^+$ per stage (nsec)	Avg $t_{pd}^-$ per stage (nsec)
D. Noninverting Chain	1	1	0.72	0.66
C. Inverting Chain	1	1	0.71	0.68
B. Fanout Chain Noninverting	1	7	1.02	1.26
A. Wired Fanin Chain Noninverting	7	1	0.96	1.16

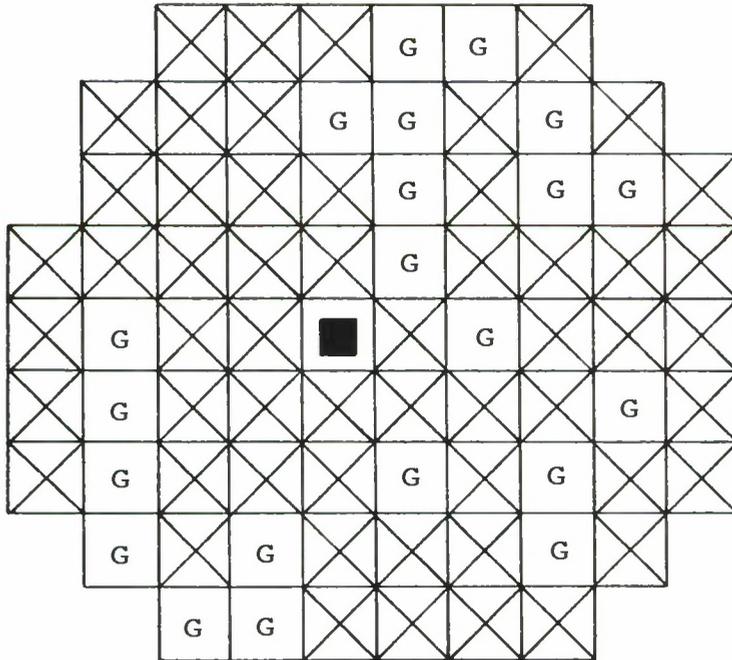
2.1.2 Fabrication Process and Yield Evaluations

The Loading Test Chip was the most complex chip which we have attempted to fabricate; it contains about 500 transistors and 425 resistors which are interconnected by three levels of metallization. This chip therefore served as a useful vehicle for evaluating our high performance microcircuit technology and our three-level metallization technology in terms of effectiveness and yield.

Employing a functional test in which 75 of the gates on the chip are exercised at least once (every gate is not exhaustively tested), it was found that 2/3 of the wafers in the lot had good chips and that die sort yields per wafer varied from 6% to 27%. Figure 5 is a yield map of the highest yield wafer in the lot. Analyses indicated that the major remaining cause of yield loss was transistor emitter-to-collector shorts. This determination was made through evaluation of a special test transistor included on each chip. The emitter of the test transistor has a large area and periphery (45% of the total emitter area and periphery in the 80-gate array) and thereby serves as a sensitive monitor of transistor failure modes such as emitter-to-collector and emitter-to-base shorts.

With regard to the multilevel interconnect structure, we determined that the design rules which were employed in designing the interconnect layout were satisfactory with one possible exception. Discontinuities occurred occasionally in a specific second-level metal stripe where it crossed over underlying worst-case topography. The worst-case topography existed whenever a first-level metal stripe had an edge coincident with the edge of an adjacent resistor region. The resistor region is recessed about 4500 Å relative to the microcircuit field region, creating a total topography step of about 10,000 Å, as illustrated in Figure 6.

WAFER FLAT



YIELD OF FUNCTIONAL CHIPS (G) = 27.6%

Figure 5. Functional die sort map for Loading Chip Wafer 1A.

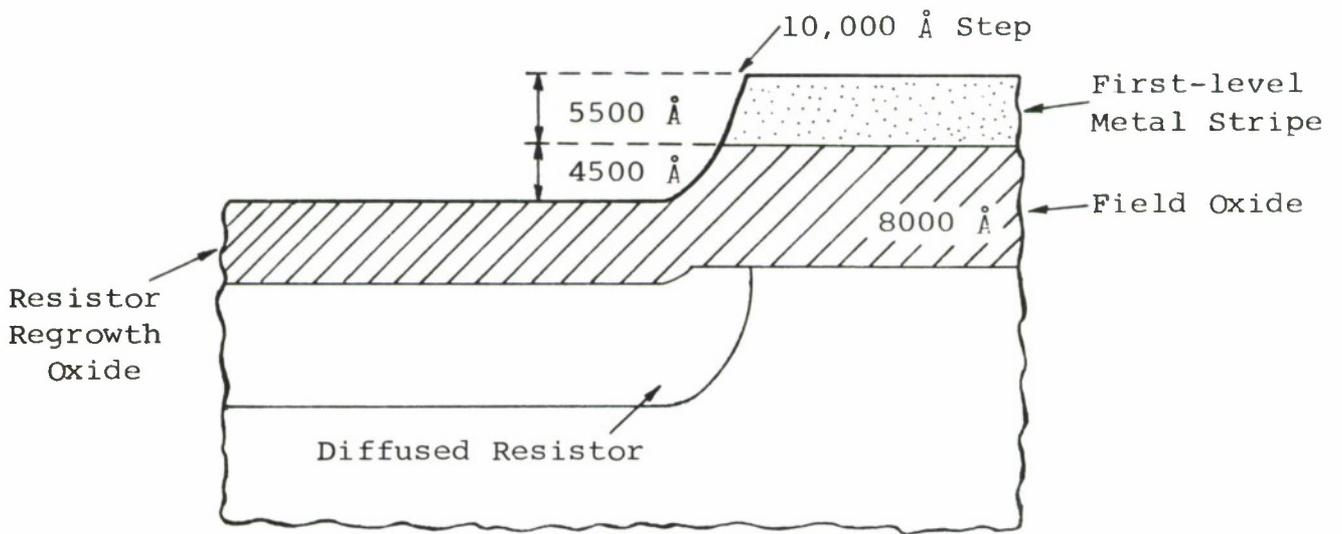


Figure 6. Cross section of worst-case topographical step created by resistor region and first-level metal.

The steepness of these steps is increased somewhat during the deposition of the first-level insulating layer (deposition process: chemical vapor plating) due to the growth mechanism of the insulating films. Consequently, these steps are believed to then cause discontinuities (microcracks) to form in the overlying second-level film, during deposition, due to complex shadowing effects caused by the sharp steps. This effect can be eliminated on future designs of complex arrays simply by changing the design rules to avoid positioning the first-level metal stripes where compound steps would be created. Alternatively, the effect could be minimized by substantially decreasing the edge angles of first-level metal stripes.

During the first twelve-month part of this program, studies were conducted toward optimizing a three-level metallization process for high speed LSI chips. Aluminum and phos-vapox (phosphorus-doped  $\text{SiO}_2$  deposited by chemical vapor plating) were selected as the conductor and insulator films. It was found during this study that a multilevel structure consisting of the film thicknesses given in Table III has excellent system properties except that discontinuities often occurred in third-level metal stripes where they crossed second-level metal steps. The problem was found to be caused by microcracks in third-level metal

TABLE III

FILM THICKNESSES FOR THE MULTILEVEL STRUCTURES WHICH EXPERIENCED  
MICROCRACK OPENS IN THIRD-LEVEL METALLIZATION STRIPES

Film	Thickness, Å
First-Level Metal	5,500
First-Level Insulator	7,500
Second-Level Metal	9,000
Second-Level Insulator	11,000
Third-Level Metal	18,000

similar to those discussed in the preceding paragraph; it was determined that the microcrack problem:

1. was essentially caused by the steep edges of second-level metal stripes,
2. was worse for thicker layers of second-level metal,
3. was worse for thicker layers of second-level insulator because the chemically vapor-plated  $\text{SiO}_2$  grows in such a manner as to increase the step angle of the underlying aluminum. The angle increases as the vapox thickness increases, and ultimately the step profile becomes re-entrant.

The following changes were made in the metal and insulator thickness specifications of the three-level metal system used on the Processor Loading Test Chip:

1. second-level metal was specified to be no thicker than 9,000 Å,
2. second-level insulator was reduced to a thickness of 6,000 Å.

These changes improved the multilevel interconnection structure, and chip yields up to 27.6% were obtained. We believe, however, that an even more effective and reliable multilevel interconnection system could be fabricated by reducing the angle of the edge profile of first- and second-level metal stripes. Efforts are being directed toward this end.

### 2.1.3 Thermal Analysis of Packaged Loading Test Chips

When dealing with complex chips, an important system consideration is the dissipation of heat from the packaged chips. This is especially important in small geometry, high speed LSI arrays because the high component density is accompanied by high power density.

The thermal properties of packaged Processor Loading Test Chips were characterized using infrared scanning techniques. The chips, which measure 120 mils x 130 mils,<sup>2</sup> were packaged in Philco-Ford 40-lead FP2011 circular metal-bottom flat packages

having a body diameter of 0.50 inches. Figure 7 shows a packaged chip. Chip surface temperatures were recorded as the chip was powered to 770 mW. Measurements were taken with the package not heat sunk and with the package heat sunk to a copper slug with dimensions of 1.0" x 0.5" x 0.1".

The maximum chip temperatures that were measured and the resultant calculated thermal resistance to noncirculated room air (27°C) are listed in Table IV.

TABLE IV

COMPARATIVE THERMAL DATA FOR A PACKAGED LOADING CHIP  
OPERATING WITH AND WITHOUT HEAT SINKING

Test Mode	Maximum Chip Temperature	Thermal Resistance to Air (27°C)
Package Not Heat Sunk	81.0°C	70°C/watt
Package Bottom Heat Sunk	57.5°C	40°C/watt

This data predicts that when the 80-gate array is interconnected so as to dissipate its maximum designed power of 1.3 watts, chip temperature would rise to 118°C. Clearly, this device will require heat sinking and possibly even cooling. From the data above it can also be seen that even relatively crude heat sinking, alone, would drop chip temperature about 39°C. Thus it is

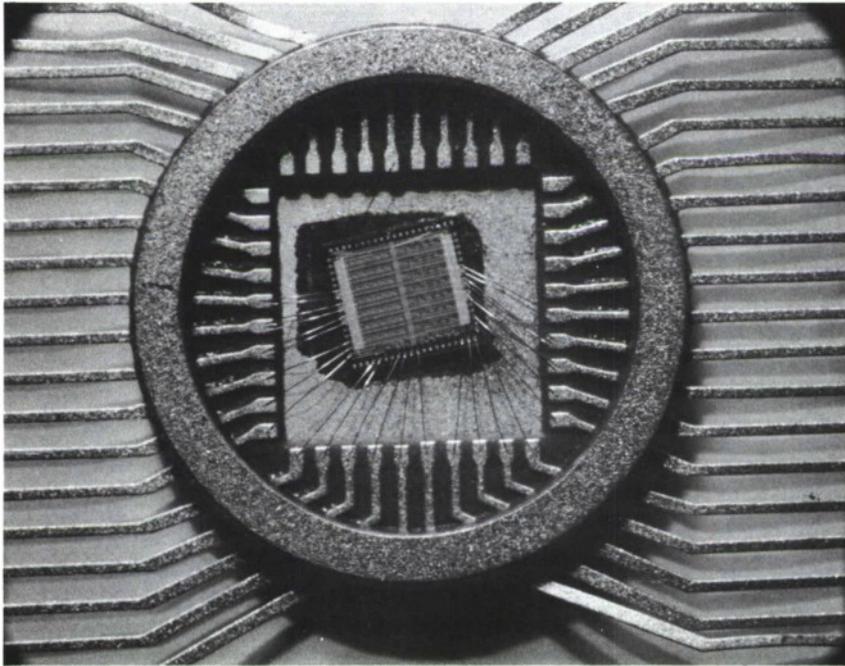


Figure 7. Photomicrograph of a packaged Loading Test Chip.

reasonable to expect that more efficient heat sinking and possibly forced air cooling would be sufficient to maintain acceptable chip operating temperatures in a system.

## 2.2 FOUR-BIT ADDER CHIP - SMX17A

A second task of the extension program was to fabricate a 4-bit Adder Chip by custom interconnecting the 80-Gate Processor Master Array. To obtain the 4-bit Adder function with differential inputs, 76 of the 80-gate cells of the array are utilized as inverters, AND gates and OR gates. To complete the required custom interconnections, three levels of metallization are required. A schematic diagram of the 4-bit Adder Chip is given in Figure 8. A photomicrograph of the completed adder is shown in Figure 9.

Two lots of 4-bit Adder Chips were fabricated. The insulating multilevel layers used in these Adder Chips was r-f sputtered  $\text{SiO}_2$ . R-F sputtered  $\text{SiO}_2$  was used in an attempt to minimize the microcrack problem in third-level metallization stripes, described in paragraph 2.1.2. The choice of r-f sputtered  $\text{SiO}_2$  as an alternative to thin vapox for minimizing microcracks in third-level metal was made as a result of experiments which compared equivalent layers of r-f sputtered  $\text{SiO}_2$  and phos-vapox layers for their effect on the microcrack problem.

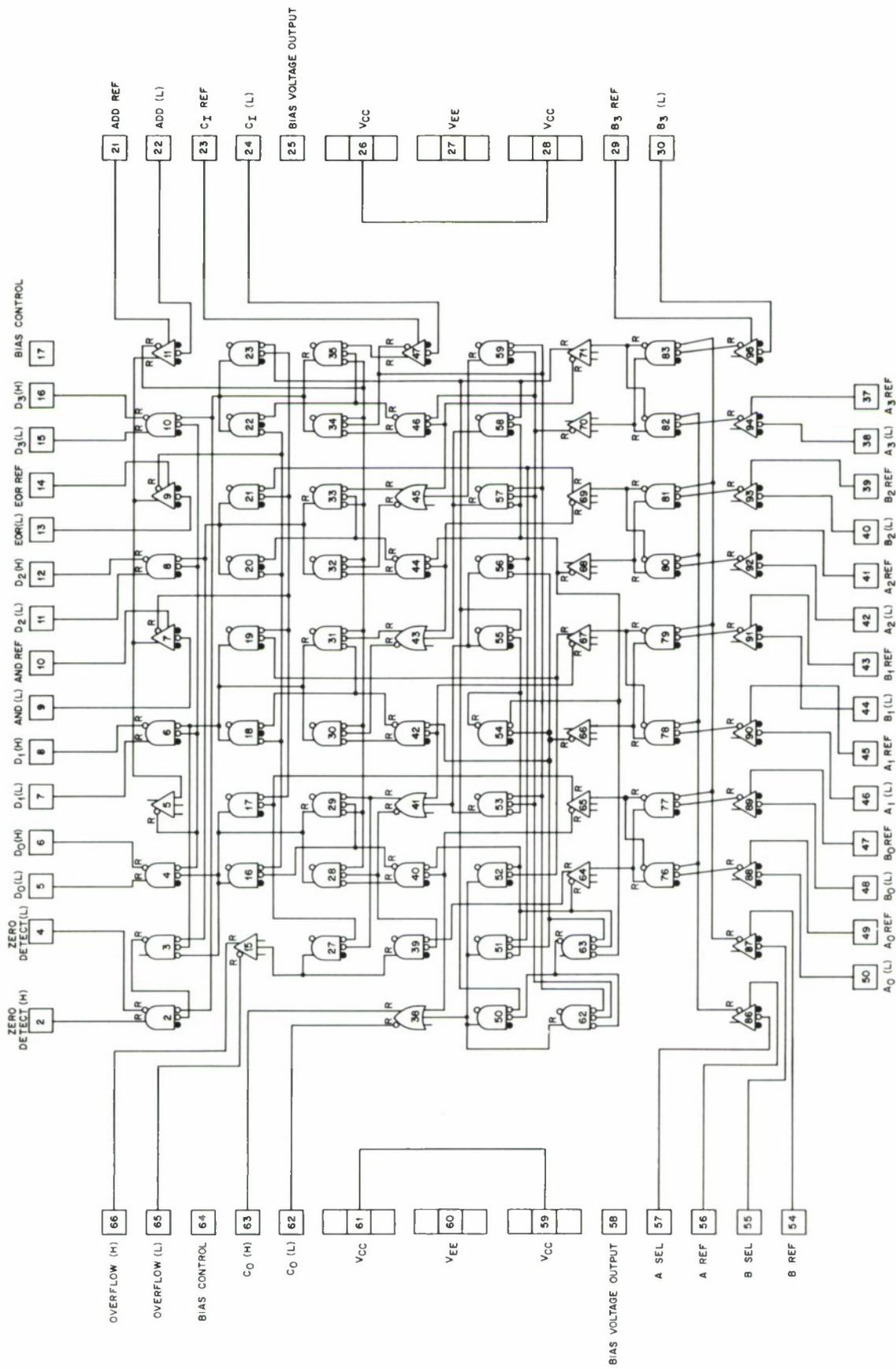


Figure 8. Schematic diagram for the 4-bit Adder Chip.

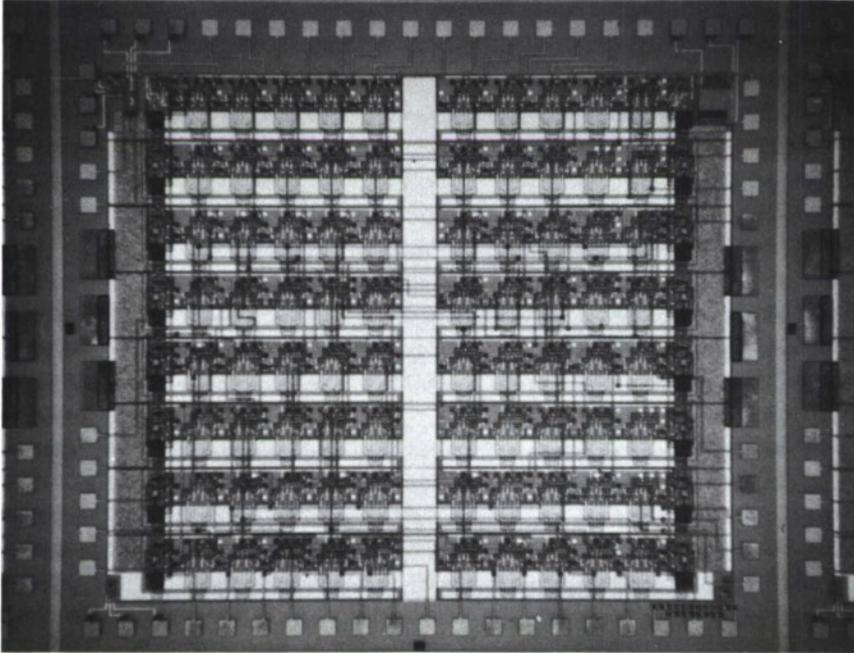


Figure 9. Photomicrograph of 4-bit Adder Chip.

From these experiments, it was found that thick layers of r-f sputtered SiO<sub>2</sub> do not increase the steepness of underlying metal steps as do thick layers of phos-vapox and consequently result in improved continuity in overlying third-level metal conductor stripes.

Electrical evaluations of the two lots of Adder wafers indicated that the yield of functional adders was zero. The major failure mode was determined to be pinholes in the r-f sputtered insulators caused during via etching. The cause of the problem was ultimately shown to be insufficient control of substrate temperature during r-f sputtering. Nonuniform substrate temperatures led to nonuniform etching properties in the sputtered layers. This, in turn, led to gross overetching of some parts of wafers with consequent creation of pinholes. This problem can be resolved by improved substrate temperature control during r-f sputtering. However, due to increased emphasis on the third task of this program, discussed in the next section, sufficient time was not available to complete additional 4-bit Adder wafers.

## 2.3 TWO-BIT FAST CARRY GATED ADDER - SMX19

### 2.3.1 General Discussion

The third task of this program was to fabricate and deliver to MIT Lincoln Laboratory, custom high speed MSI microcircuits

for a high speed multiplier subsystem. The subsystem, a 17 x 17 Array Multiplier was to be assembled by Lincoln Laboratory to demonstrate a significant new concept for increasing speeds of arithmetic multipliers. The required MSI microcircuits consisted of 2-bit Fast Carry Gated Adders, referred to as SMX19, of three different types. The Type I Adder performs the conventional add logic function. The Type III and Type IV Adder perform logic functions which are slightly different from the conventional adder. A total of 136 2-bit Adders are used in the Array Multiplier.

### 2.3.2 Circuit and Logic Design

Circuit design of the Adder was performed by MIT Lincoln Laboratory using negative ECL logic. A schematic diagram of the Type I Adder, for example, is shown in Figure 10. The logic performed by the Type I Adder is given in Figure 11, wherein  $A_0 = a_0 \cdot a_0'$ ,  $A_1 = a_1 \cdot a_1'$ ,  $B_0 = b_0 \cdot b_0'$  and  $B_1 = b_1 \cdot b_1'$ . Note that the "exclusive or" functions (designated by +) are generated very conveniently in this circuit design with two-level series gates. The dashed lines from points L, M, N, P, Q and R in Figure 10 indicate the correct optional interconnections for the Type I Adder. The proper connections for the Type III and Type IV Adder are shown in Figure 12.  $V_{EE}$  supply voltage is -5.2 V and "1" and "0" levels are -1.6 and -0.80 V, respectively.

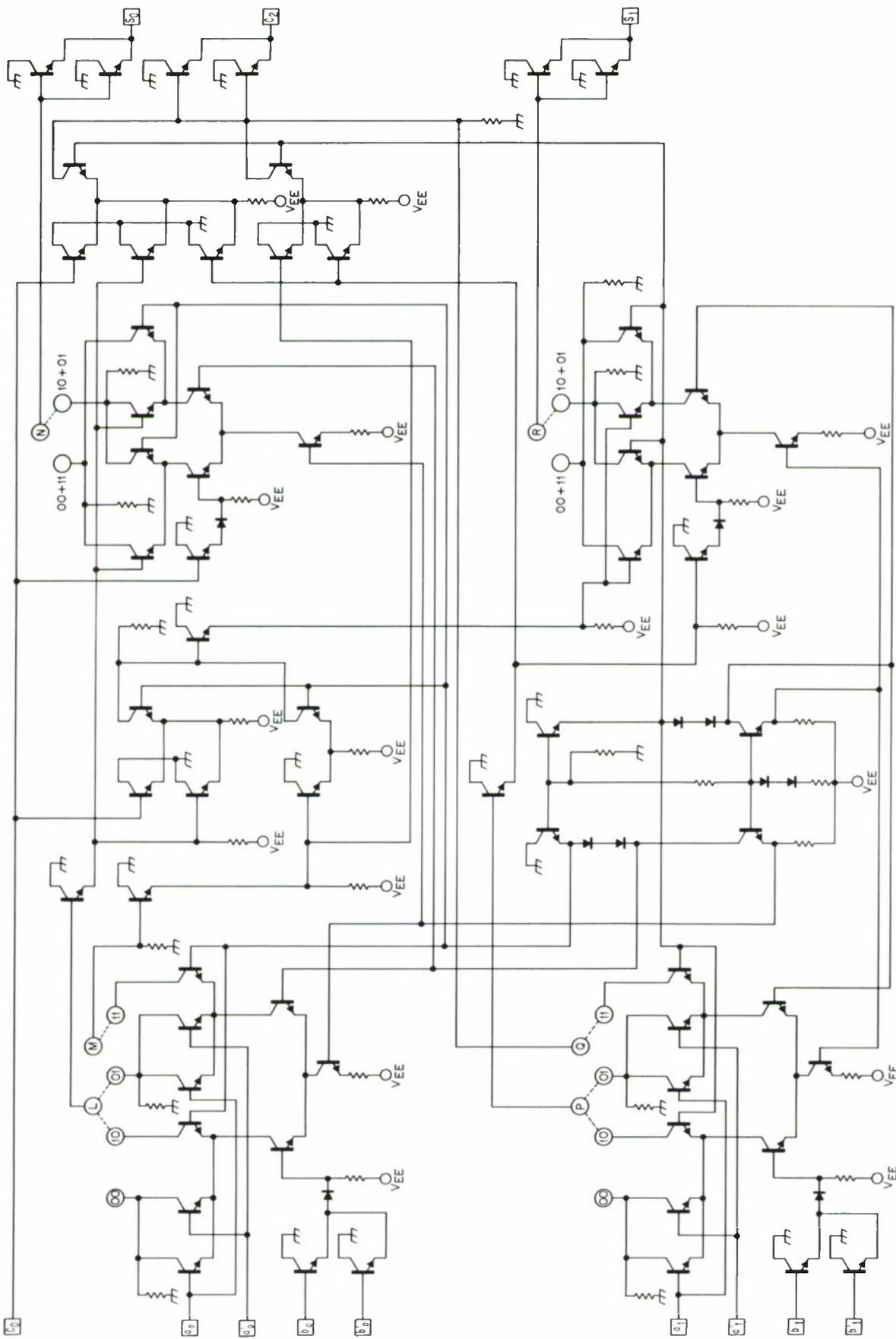


Figure 10. Schematic diagram for the Type I 2-bit Fast Carry Gated Adder Chip (SMX19-I).

$$S_0 = (A_0 \oplus B_0) \oplus C_0$$

$$S_1 = (A_1 \oplus B_1) \oplus [C_0(A_0 \oplus B_0) + (A_0B_0)]$$

$$C_2 = C_0(A_0 \oplus B_0)(A_1 \oplus B_1) + (A_0B_0)(A_1 \oplus B_1) + A_1B_1$$

Figure 11. Definitions of the logic performed by the Type I Adder Chip.

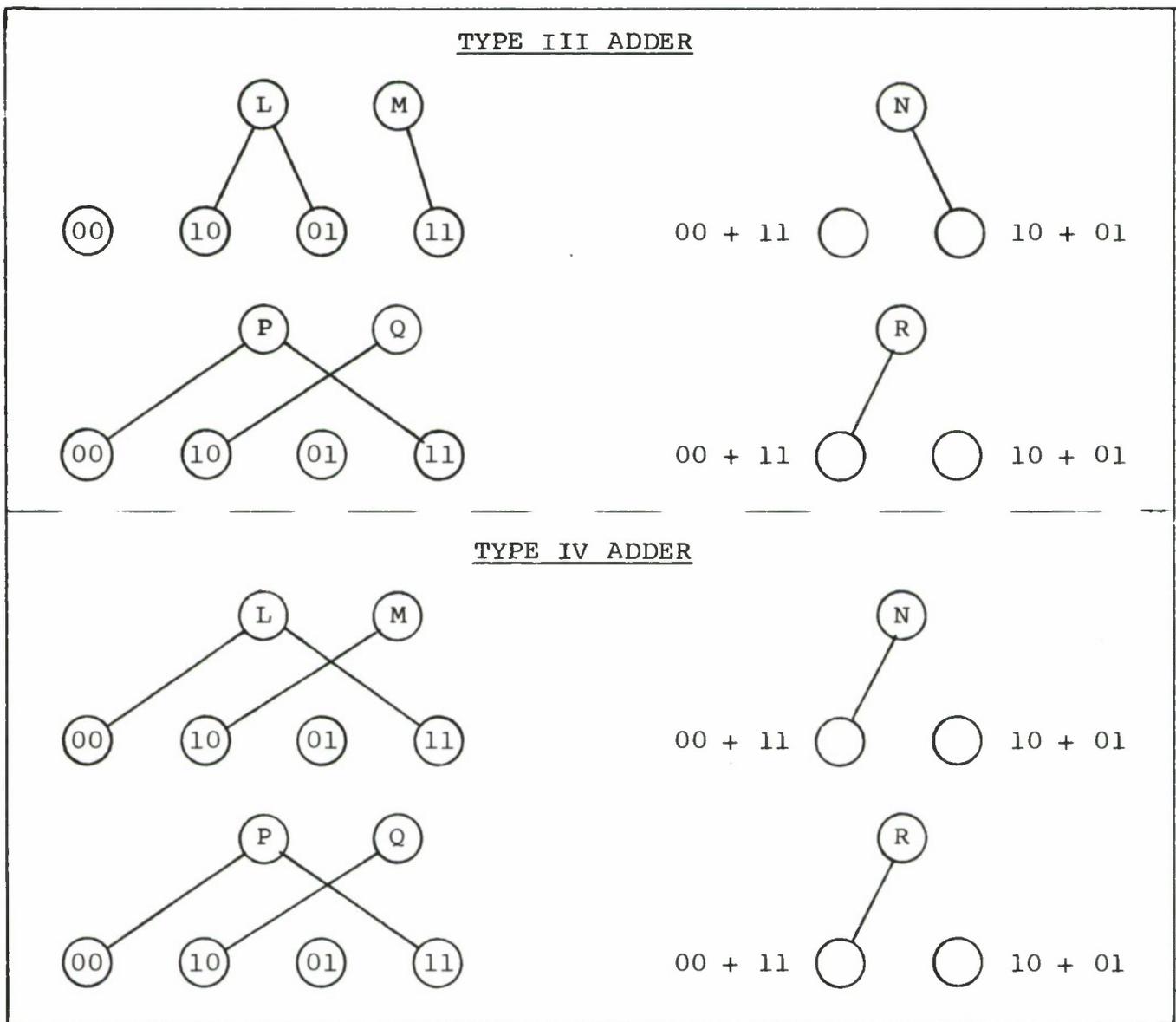


Figure 12. Correct interconnections for Type III and Type IV Adders (refer to Figure 10).

### 2.3.3 Microcircuit Design

The layout design for the SMX19 Adders was carried out using design rules and process specifications similar to those employed in designing the high speed 80-gate arrays of subsections 2.1 and 2.2. For example, resistor sheet resistance was specified to be  $100 \Omega/\square$ , base diffusion depth was specified at  $0.6 \mu$  and transistor emitter widths and base contact cut widths were specified to be 0.1 mil. Several deviations from previous rules concerning spacings were made; the deviations include:

1. The spacing between emitters and base contacts on all transistors except the input transistors was increased to 0.15 (from 0.1 mil) in order to permit improved contacting of emitter regions by circuit metallization (emitter metal stripes were 0.2 mil wide, overlapping the emitter by 0.05 mils on each side).
2. On input devices, emitter to base contact spacing was increased to 0.25 mils in order to increase transistor base resistance and thereby preclude oscillation effects.

All three types of SMX19 Adder chips have 73 transistors, 32 resistors, and two levels of metallization. Photomask designs for all three Adder types were identical except for the

second-level interconnect mask. The second-level metal pattern determines the type of Adder. The SMX19 chip contains a substantial test pattern area in addition to the Adder circuit; its size is 58 x 60 mils.<sup>2</sup>

#### 2.3.4 Fabrication and Yield

Two lots of Adder wafers (5 wafers per lot) were completed. The total number of adders required for delivery were obtained from these lots. The required delivery consisted of 107 Type I Adders, 24 Type III Adders and 5 Type IV Adders. Functional die sort yields ranged from 13.6% to 44.5% on wafers which passed wafer test. A photomicrograph of a fabricated 2-bit Adder Chip is shown in Figure 13.

The multilevel-metallization structure in this chip consists of:

First-level metal - 5,500 Å

First-level insulator - 7,000 Å

Second-level metal - 13,000 Å

The second-level metal was deposited under heated substrate conditions. The metallization discontinuity problem discussed in subsections 2.1 and 2.2 is eliminated in chips interconnected with two levels of metallization by this combination of process and structure.

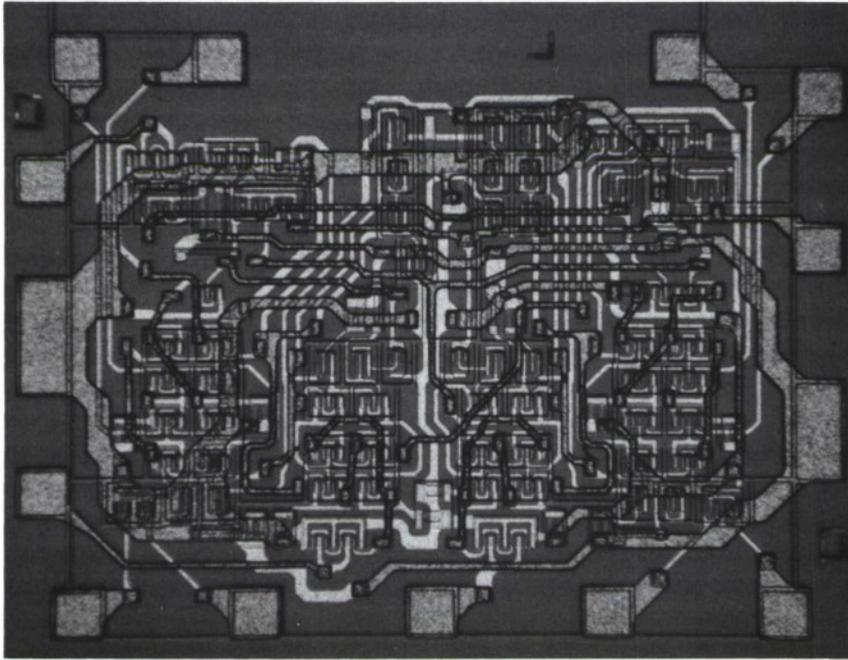


Figure 13. Photomicrograph of 2-bit Adder Chip -- Type I.

The SMX19 Adders were assembled on 14-lead ceramic dual in-line packages. Chips were bonded in the packages using eutectic die bonding. The chip-to-package connections were made with 1.0-mil diameter, ultrasonically-bonded aluminum wires.

#### 2.3.5 Performance, Evaluation and Conclusions

The 17 x 17 Array Multiplier which was constructed at MIT Lincoln Laboratory with the SMX19 Adders is reported to have performed well. Delay time through the multiplier was measured as 40 nsec, an improvement of 10 nsec over the predicted value of 50 nsec, and a much more substantial improvement (about 50 nsec) over what might be expected when using standard multiplier techniques.

The performance of the individual SMX19 Adders was also generally quite satisfactory, an encouraging result considering it was the first implementation of these particular 2-bit Fast Carry Adder circuit and microcircuit designs. The majority of the delivered devices (those from Wafer Lot 1) were characterized by a carry delay of about 1.8 nsec, and a sum delay of approximately 3.0 nsec. From this data the estimated equivalent gate delay is about 1.0 nsec. On these same devices, "1", "0" and threshold voltage levels were very close to the design values of -1.6 V and -0.8 V, respectively. Some of the Adders (from Lot 5) had somewhat higher delays, namely a carry delay of approximately 2.5 nsec and a sum delay of 4 to 6 nsec.

Analyses of the causes of the variations in propagation delay on SMX19 Adders led us to conclude that the intrinsic transistor delay which was to be negligible was not so in any of the Adders. The peak  $f_T$  of the gating transistors under worst-case bias of  $V_{CB} = 0$ , was only 1.6 to 1.9 GHz instead of the design value of  $\geq 2.5$  GHz. More importantly, the gating transistors tended to be partially saturated at their "full on" operating collector currents of 4.4 to 4.8 mA at the collector-emitter voltage of 0.8 V. (This effect was reflected in a sharp drop-off in transistor  $f_T$  and transistor d-c  $\beta$  at collector currents in the range of 3 to 4.5 mA.)

Based upon the above information and on process information concerning the SMX19 Wafer Lots 1 and 5, we believe that reduced delays could be obtained from the present SMX19 layout design by reducing intrinsic transistor delay by:

1. Using a more optimum profile for the base diffusion.

The base diffusion process can be reprogrammed to increase  $f_T$  at all currents with basewidths equivalent to those which have been used.

2. Reducing the epitaxial layer thickness. This change would decrease transistor  $R_{SAT}$ , reduce the tendency to saturate, and reduce  $f_T$  drop-off.

3. Increasing circuit resistor values. This change would limit transistor  $I_C$  in the gate "full on" condition.

Alternatively the circuit layout could be redesigned to allow the transistors a higher current handling capability. Process and design changes 1 and 2 above would still be necessary. It is expected that the proposed improvements in Adder delays would result in Multiplier delays of 30 nsec or less.

### III - DELIVERIES

During this program period, the following items were delivered to MIT Lincoln Laboratory:

1. Eight SMX17L Loading Chips, wired to permit gate chain evaluations. These SMX17L Loading Chips were packaged in 40-lead flat packages.
2. Five SMX17L Loading Chips, wired to permit evaluation of test structures other than the gate chains. These SMX17L Loading Chips were also packaged in 40-lead flat packages.
3. Two hundred nineteen SMX19, 2-bit Fast Carry Adder microcircuits of which:

144 were Type I  
19 were Type III  
56 were Type IV

The SMX19 Adders were packaged in 14-lead ceramic dual in-line packages.

#### IV - REFERENCES

1. "R&D of the Technologies Required to Design and Fabricate Ultrahigh-Speed Computer Systems," Final Report, Contract No. AF19(628)-5167, January 1969, p. 82.
2. "Research and Development of High Speed Processor Arrays," Fourth Interim Summary Report, Contract AF19(628)-5167, December 1969, pp. 3-15.

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13. ABSTRACT This report describes program progress during the eight-month extension period of a research and development program directed toward the development of high performance, digital, MSI-LSI microcircuits and their application in feasibility studies of high speed data processing systems. The tasks of this report period included the fabrication of a high speed 80-gate array with three levels of metallization and the performance evaluation of a high speed (<1.0 nsec), low power (<15 mW), ECL gate design, for various on-chip gate loading conditions. Both tasks were completed. Also required was the fabrication and delivery of three different, custom, ECL Two-Bit Fast Carry Gated Adder microcircuits (two levels of metallization) for application in a high speed 17 x 17 Array Multiplier. A total of 136 adders are required for the multiplier. The required number of adders were delivered, and the multiplier which was assembled using those adders functioned properly. The time required for the multiplier to perform its function was measured to be 40 nsec, a 10-nsec improvement over the expected time.			
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