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THE UNIVERSITY OF MICHIGAN

COLLEGE OF ENGINEERING
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Radiation Laboratory
Ann Arbor, Michigan 48108

Circuit Realization of Impedance Loading for Cross Section Reduction

By
E. LAWRENCE McMAHON

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Scientific Report No. 8
Contract No. F19628-68-C-0071
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Work Unit No. 56350201

Contract Monitor: JOHN K. SCHINDLER
MICROWAVE PHYSICS LABORATORY

Prepared for:

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ABSTRACT

Techniques for realizing a reactance which is a decreasing function of frequency are discussed. A Negative Impedance Converter (NIC) circuit is analyzed and techniques given for compensating for imperfections and frequency dependence. An RC realization of the desired impedance is given, and it is demonstrated that this realization can be modified to compensate for phase shift in the NIC. An analytical and numerical analysis of a NIC based on amplifiers with 50 Ω input and output impedances is presented.

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I

INTRODUCTION

The reduction of the radar cross section of conducting bodies by impedance loading has been studied for a number of geometries. The frequency range for which this technique is particularly attractive is that for which the dimensions of the conducting body are comparable to a wavelength. In this range, the load required generally has a real part whose frequency dependence is not easily characterized, but which is generally small compared to the imaginary part. In the particular case which has been the object of investigation under this contract — that of a sphere loaded by a slot in the plane of incidence — the real part is essentially zero over the frequency range of interest, while the imaginary part is quite well approximated by the negative of a series LC reactance. Such a reactance, which decreases as the frequency increases, will be referred to hereafter as a negative reactance; there should be no occasion for confusion between this term and the negative, but increasing with frequency, reactance of a capacitor.

Since it is well known that the reactance at any lossless, passive network is an increasing function of frequency, the negative reactance required for loading obviously cannot be realized by a passive network. Of the active elements available for synthesis the most obvious choice is the Negative Impedance Converter, or NIC; the properties and some realizations of the NIC are discussed in the following.

II

THE NEGATIVE IMPEDANCE CONVERTER

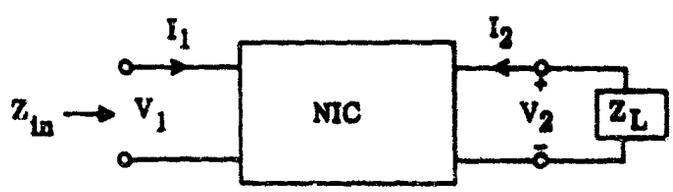


FIG. 1: NIC with load.

Figure 1 shows the referencing conventions used throughout this report. The NIC is characterized by the relation $Z_{in} = -Z_L$. In order to determine how the NIC must behave in order to satisfy this relation, it is convenient to use the h-parameters. These parameters have the general form

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix} \quad . \tag{1}$$

The addition of the load impedance, Z_L, imposes the additional constraint

$$V_2 = -I_2 Z_L \tag{2}$$

where the minus sign is a consequence of the reference direction chosen for I_2. Combining (1) and (2), and solving for Z_{in}, we obtain

$$Z_{in} = h_{11} - \frac{h_{12}h_{21}}{h_{22} + Y_L} \quad . \tag{3}$$

The requirement that $Z_{in} = -Z_L$ then imposes the conditions

$$h_{11} = h_{22} = 0 \ , \tag{4a}$$

$$h_{12}h_{21} = \pm 1 \ . \tag{4b}$$

Although (4b) can be satisfied in an infinite number of ways, only two cases are encountered in practice. The first is the current inversion NIC, or INIC, where

$$h_{12} = h_{21} = 1 \tag{5}$$

and the other is the voltage inversion NIC, or VNIC, where

$$h_{12} = h_{21} = -1 \ . \tag{6}$$

The INIC has the property that

$$V_1 = V_2 , \tag{7a}$$

$$I_1 = I_2 ; \tag{7b}$$

the voltages are thus the same as they would be with the NIC replaced by a direct connection, while I_2 is equal and opposite to the value it would have in a direct connection. For a VNIC,

$$V_1 = -V_2 , \tag{8a}$$

$$I_1 = -I_2 ; \tag{8b}$$

here the voltages are reversed and the currents have the values normal in a direct connection.

Of the numerous circuit realizations of the NIC available in the literature, one originally given by Yanagisawa (1957) was chosen for investigation. A simplified diagram of the circuit, with bias circuitry omitted, is shown in Fig. 2a. Figure 2b shows a model of the circuit suitable for first-order analysis; the

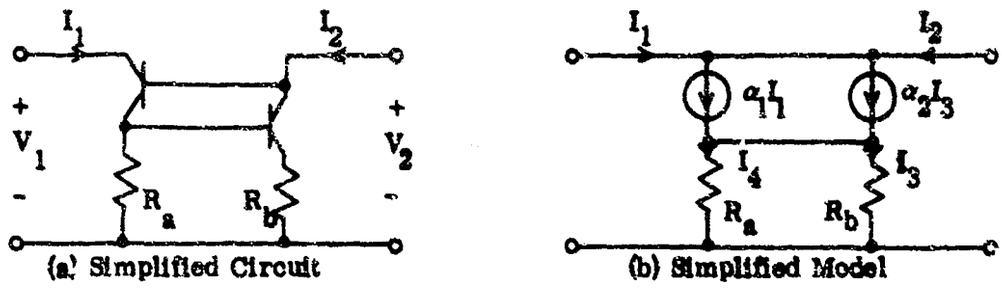


FIG. 2: Yanagisawa NIC.

transistors have been replaced by simple, controlled current-source models, with base resistance and base-emitter drop neglected. Assuming further that $\alpha = 1$ for both transistors, Kirchhoff's Current Law gives

$$I_3 = I_2 \tag{9}$$

and

$$I_4 = I_1 \ . \tag{10}$$

We also have the constraint

$$I_4 R_a = I_3 R_b \ . \tag{11}$$

Combining these three relations, we have

$$I_2 = \frac{R_a}{R_b} I_1 \ . \tag{12}$$

Since V_1 and V_2 are obviously equal, the circuit function as an INIC; the conversion factor is unity when $R_a = R_b$.

A more accurate analysis takes into account the collector capacitances of the two transistors, which can be expected to be significant in the frequency range of interest. Since the two collector-base junctions are in parallel, the circuit model is that of Fig. 3, where $C = 2\ C_b$, the sum of the two collector-base capacitances.

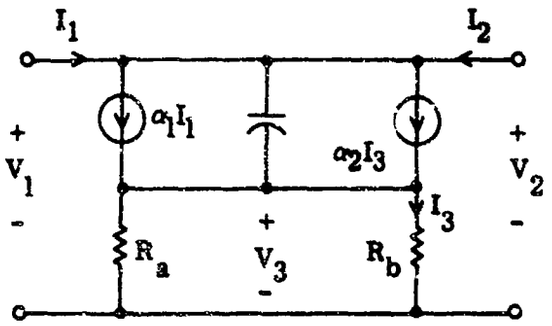


FIG. 3: High-frequency model of NIC.

Again assuming that $\alpha_1 = \alpha_2 = 1$, we may write

$$V_1 = V_2 \tag{13}$$

as before; from Kirchhoff's Current Law at the upper node we have

$$I_1 + I_3 - \alpha_1 I_1 - \alpha_2 I_3 = I_2 - I_3 = sC(V_2 - V_3) , \tag{14}$$

and summing currents at the lower node gives

$$I_1 + I_2 = V_3(G_a + G_b) . \tag{15}$$

Combining these equations with the relationship

$$I_3 = V_3 G_b \tag{16}$$

and eliminating I_3 and V_3 in Eqs. (14) - (16), we obtain

$$I_2 = \frac{G_b - sC}{G_a + sC} I_1 + sC \frac{G_a + G_b}{G_a + sC} V_2 . \tag{17}$$

When C = 0, this equation reduces to Eq. (12), as expected. With $C \neq 0$, there are two departures from ideal behavior: the frequency dependence of h_{21} and the non-zero h_{22}. The first of these effects can be eliminated by adding a capacitance 2C in parallel with G_b; mathematically, this is equivalent to replacing G_b in (17) by $G_b + 2C$. Making this substitution, and letting $G_a = G_b$, we obtain

$$I_2 = I_1 + 2sCV_2 . \tag{18}$$

There remains the non-zero h_{22} term, which is equivalent to a capacitance 2C across the output terminals of the circuit. Since the NIC is otherwise ideal, this appears as a negative capacitance, -2C, across the input terminals and can be cancelled by an equal positive capacitance. In practice, this was found unnecessary, the capacitance added by the input circuitry being sufficient for compensation.

The complete NIC circuit is illustrated in Fig. 4. The functions of R_1, R_2 and C_2 have already been explained. R_3 and R_4 are biasing resistors; since for signals they are across the input and output, respectively, they cancel one another by NIC action. The remaining resistors , with their associated bypass capacitors, are needed to maintain the transistors in their active regions. If they were omitted, the circuit would have a stable state in which both transistors were cut off, with zero base-emitter voltages. If either transistor were to turn on even momentarily when power is first applied both transistors would be forced into the active region. It was found, however, that this mechanism could not be depended upon, necessitating the additional bias circuitry.

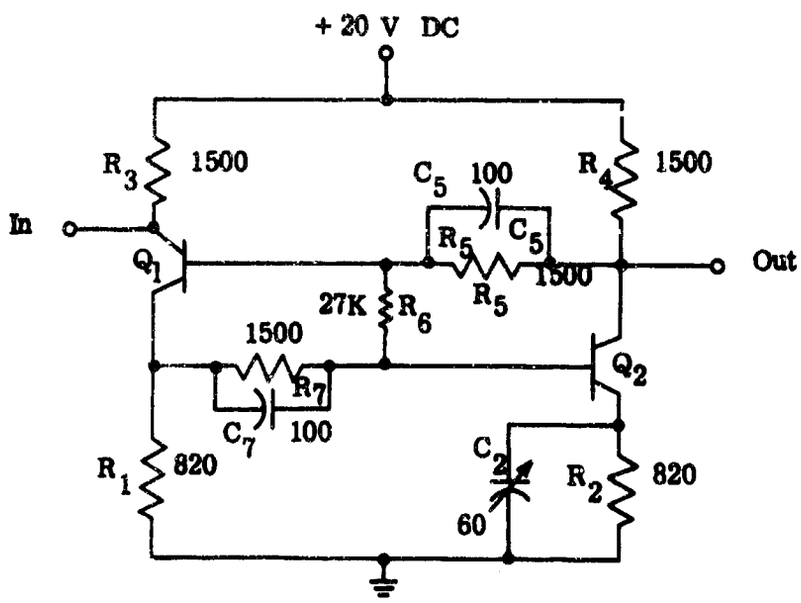


FIG. 4: Complete NIC circuit. Values in ohms pF; Q_1=2N711B, Q_2= MPS 6521 .

In the analysis above, both base resistance and the frequency dependence of α have been neglected for the sake of simplicity. Inclusion of the base resistance complicates the analysis to the point where algebraic analysis is no longer fruitful. Computer analysis, using the CIRAN circuit analysis program available of the University of Michigan IBM 360 system, was therefore initiated. These studies led to the conclusion that non-zero base resistance does not seriously degrade the performance of the circuit as long as it is small compared to the external resistances; experimental results have borne out this conclusion.

The frequency dependence of transistor α is a much more serious problem, and proved to be a serious obstacle in the early stages of this investigation. Making the usual first-order assumption that α is given by

$$\alpha = \frac{1}{1+s/\omega_o} \tag{19}$$

where s is the complex frequency variable and ω_o is the alpha-cutoff frequency, leads, after considerable algebraic manipulation, to an approximate h-parameter description of the NIC having the form

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ \dfrac{1-3s/\omega_o}{1+3s/\omega_o} & 2sC\,\dfrac{1+s/\omega_o}{1+3s/\omega_o} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix} \tag{20}$$

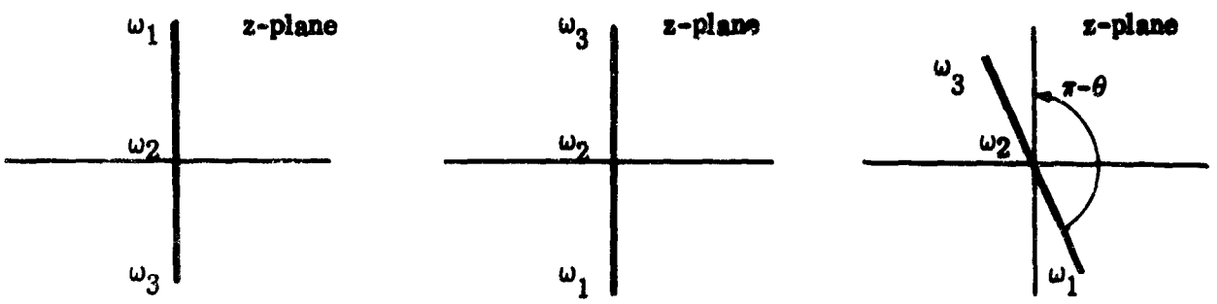
as compared with the ideal (to which Eq. (20) reduces for s = 0) of the form

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix} . \tag{21}$$

The non-zero h_{22} in Eq. (20) represents a parasitic RC admittance across the output terminals of the NIC . This is not a serious problem in an otherwise ideal device, since a parasitic admittance across one part of the NIC can be cancelled out by an equal admittance across the other port.

The forward current gain, h_{21}, in (20) has the form of an all-pass phase shift function, with a phase angle which departs significantly from 0° at frequencies as low as $\omega_0/30$, which is in or below the frequency range of interest.

After extensive analysis, it was concluded that this phase shift could not be compensated for by modification of the NIC itself. This immediately led to the further conclusion that the desired input impedance could not be realized (in the frequency range of interest) by means of an NIC and an LC load. This is illustrated in Fig. 5, where for clarity, it has been assumed that the NIC exhibits a constant phase shift, θ; that is $Z_{in}=Z_L\,\epsilon^{j(\pi-\theta)}$.



a) Desired input impedance. b) Load impedance required w/o phase shift. c) Load impedance required w/phase shift.

FIG. 5: Effect of phase shift in NIC.

The desired input impedance shown in Fig. 5a, is a pure reactance decreasing as frequency increases. Without phase shift, that is, with a conversion factor $\epsilon^{j\pi}=-1$, the required load impedance is a pure reactance increasing as frequency increases, as shown in Fig. 5b. As is well known, such a reactance is easily realized with passive elements. The situation resulting when the conversion factor is $\epsilon^{j(\pi-\theta)}$ is

shown in Fig. 5c; here, in order to obtain the desired input impedance, the load impedance must be shifted by an angle θ from the ideal load impedance. Since this impedance has a negative real part for $\omega_2 < \omega < \omega_3$, it obviously cannot be realized with passive elements. Fortunately, this difficulty can be circumvented, at the cost of a few extra passive elements, by means of an RC realization (Kinariwala, 1959).

The desired input impedance, frequency and magnitude-normalized, is given by

$$Z(s) = -\frac{s^2+1}{s} \quad . \tag{22}$$

If a positive constant of appropriate value is subtracted from Z(s), we obtain

$$Z_1(s)=Z(s)-(a+\frac{1}{a}) = -\frac{s^2+(s+\frac{1}{a})\,s+1}{s} = -\frac{(s+a)(s+\frac{1}{a})}{s} \tag{23}$$

where it is assumed, without loss of generality, that $a < 1$. Now $Y_1(s)$, the reciprocal of $Z_1(s)$, has all its poles on the negative-real axis of the s-plane. $Y_1(s)$ can therefore be expanded in the same manner as an RC admittance, although it is not actually an RC admittance, since its poles and zeros do not alternate on the negative-real axis. The result of this expansion is

$$Y_1(s) = \frac{\frac{a}{1-a^2}s}{s+\frac{1}{a}} - \frac{\frac{a}{1-a^2}s}{s+a} \tag{24}$$

which is the difference of two RC admittances. $Y_1(s)$ can therefore be realized with two passive RC networks and a single NIC. The realization of Z(s) is then achieved by the trivial operation of adding in series the constant originally subtracted in (23). The final realization is shown in Fig. 6. Subject to the constraint that it be less than unity, the parameter a is 'free', and its value may be chosen to attain objectives such as convenient element size or reduced sensitivity.

The effect of phase shift in the NIC is shown in Fig. 7, which should be compared with Fig. 5. As before, the NIC is assumed to exhibit a constant phase

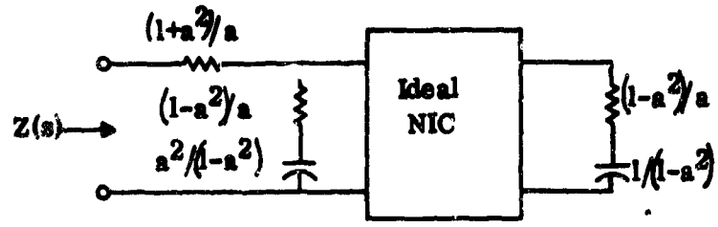
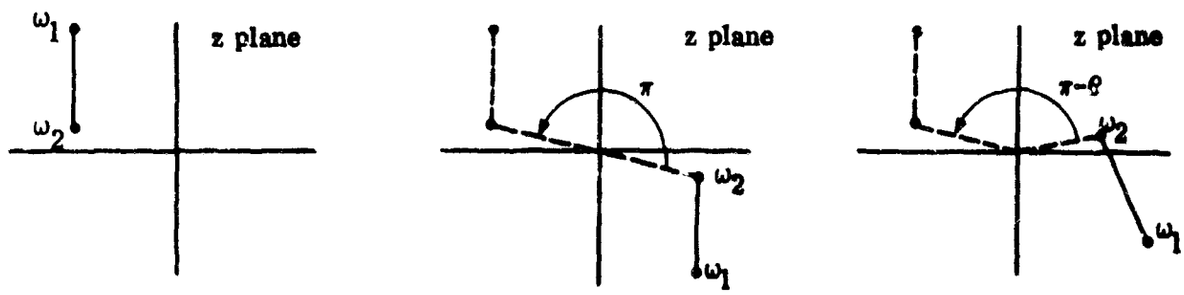


FIG. 6: RC realization of desired load.



a) Impedance desired at NIC input.

b) Load impedance required w/o phase shift.

c) Load impedance required w/phase shift.

FIG. 7: Effect of NIC phase shift on RC realization.

shift, θ, giving a conversion factor $\epsilon^{j(\pi-\theta)}$. In order to obtain the desired impedance at the NIC input in the presence of phase shift, the load impedance must be rotated in the z-plane through an angle θ, as before, The crucial difference between the RC realization and the LC realization is that in the RC case, the rotated load impedance remains in the right half of the z plane and is therefore at least potentially realizable.

This realizability was checked by attempting to match the load impedance required, using measured values of the NIC conversion factor, Z_{in}/Z_L . The form of the modified load impedance is shown in Fig. 8. The element values were chosen

a) Load impedance w/o phase shift. b) Load impedance w/phase shift.

FIG. 8: Load compensation for NIC phase shift.

for an exact match at ka = 0.7 and 1.2. C_1 and R were chosen to match the real part of these two points, and C_2 and L were then chosen to give the correct imaginary part; the procedure thus required simultaneous solution of two pairs of nonlinear equations. The two values of ka used for matching points were picked by trial and error; obviously, bandwidth can be traded for better accuracy by choosing frequencies closer together, and vice versa.

The calculated results are given in Table I. As might be expected, since the desired load impedance is a well-behaved function of normalized frequency, an excellent, broadband match was obtained at the load. Some deterioriation is observed when this load is transferred to the NIC input. Although this is almost entirely due to numerical error (the calculations were carried out on a desk calculator, not a digital computer), it is felt that the values obtained are reasonable. An actual circuit could not be expected to operate in as smooth and consistent a manner as a smoothed set of measurements. There would thus be a similar deterioration in practice, although arising from a different mechanism.

The correspondence between the impedance desired and that actually achieved is markedly poorer at the circuit input. This is due to the fact that operation of the

TABLE I

ka	Z_l Load Impedance Desired	Z_l Load Impedance Obtained	Z_{in} Impedance at NIC Input Desired	Z_{in} Impedance at NIC Input Obtained	Z Impedance at Circuit Input Desired	Z Impedance at Circuit Input Obtained
.5	10.17 - j11.37	10.45 - j10.70	-2.35 + j3.18	-2.44 + j3.01	0 + j5.80	0.65 + j4.14
.6	10.13 -j8.84	10.25 - j8.55	-2.35 + j2.65	-2.38 + j2.58	0 + j3.71	0.36 + j3.02
.7	10.02 - j6.91	10.02 - j6.92	-2.35 + j2.27	-2.35 + j2.27	0 + j2.03	-0.02 + j2.03
.8	9.83 - j5.44	9.76 - j5.61	-2.35 + j1.99	-2.32 + j2.04	0 + j0.62	-0.54 + j1.15
.9	9.58 - j4.22	9.49 - j4.50	-2.35 + j1.77	-2.31 + j1.84	0 + j0.64	-0.92 + j0.14
1.0	9.2[illegible] - j3.21	9.21 - j3.52	-2.35 + j1.59	-2.31 + j1.67	0 - j1.78	-1.28 - j0.87
1.1	8.95 - j2.44	8.91 - j2.63	-2.35 + j1.45	-2.33 + j1.50	0 - j2.84	-1.05 + j2.61
1.2	8.61 - j1.79	8.61 - j1.79	-2.35 + j1.33	-2.35 + j1.33	0 - j3.86	-0.13 - j3.83
1.3	8.25 - j1.23	8.30 - j1.00	-2.35 + j1.22	-2.39 + j1.15	0 - j4.84	1.46 - j4.96
1.4	7.88 - j0.85	7.99 - j0.22	-2.35 + j1.14	-2.45 + j0.97	0 - j5.81	3.11 - j6.01
1.5	7.51 - j0.53	7.69 + j0.53	-2.35 +j1.06	-2.41 + j0.74	0 - j6.79	4.79 - j5.29

circuit depends on the subtraction of two impedances of the same order of magnitude; this is an error-magnifying process in both numerical calculation and physical operation. The RC combination connected across the NIC input combines in parallel with the negative RC impedance seen across the input terminals of the NIC to yield

$$Y = \frac{sC_1}{1+sC_1R_1} - \frac{sC_2}{1+sC_2R_2} = \frac{s(C_1-C_2)+s^2C_1C_2(R_2-R_1)}{)1+sC_1R_1)(1+sC_2R_2)} . \tag{25}$$

The correct operation of the circuit depends on the exact equality of R_1 and R_2 and the resultant cancellation of the second term in the numerator of (25). In practice, this condition cannot be achieved exactly; as will be seen from Table I, the input impedance of the NIC has a real part which varies about ± 5 percent around its mean value and thus cannot be exactly cancelled by the constant R_1. However, by careful adjustment, it should be possible to move the spurious pole introduced by incomplete cancellation far enough from the origin that its effect will be negligible.

The impedances given in the last column of Table I were checked by a computer program which calculates the change in cross section produced by a given load. For purposes of comparison, the input impedance of the idealized circuit, with no phase shift, was also calculated by the same numerical procedure and the corresponding cross section reduction calculated. The two circuits are shown in Fig. 9, and the calculated changes in cross section are given in Table II.

The calculations discussed above were carried out primarily to check the feasibility of adjusting the load to compensate for phase shift, and no attempt at optimization was made. The results given in Table II should therefore not be viewed as the best attainable. In practice, it should be possible to approach fairly closely the cross section reductions obtained using the idealized circuit.

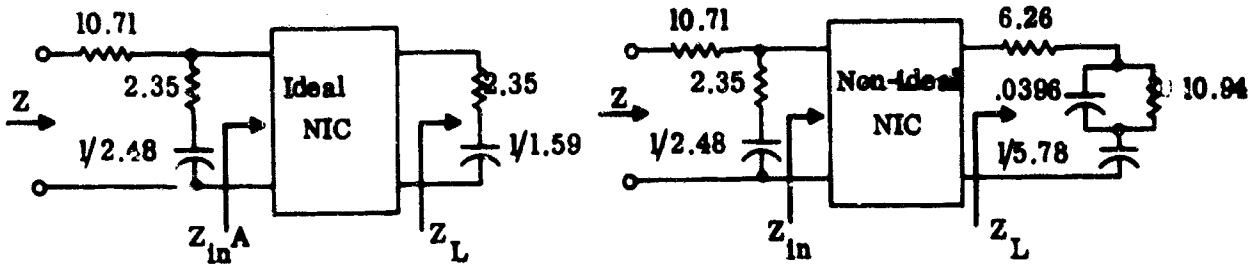


FIG. 9: Load realization with ideal and non-ideal NIC's.

TABLE II

ka	Change in Cross Section (dB) Idealized Circuit	Change in Cross Section (dB) Actual Circuit
.5	-11.01	2.30
.6	-12.83	3.39
.7	-28.43	-27.66
.8	-22.35	- 3.45
.9	-19.16	- 1.58
1.0	-12.56	- 0.57
1.1	- 4.43	1.27
1.2	- 5.51	- 5.48
1.3	- 7.18	- 2.07
1.4	+ 2.24	- 1.02
1.5	- 6.36	-

Experimental results obtained in the 1 - 10 MHz band have substantiated the calculations quite well. Figure 10 shows the measured input impedance of the NIC with a series RC load; the measured reactance has been multiplied by frequency for convenience in presenting the data. Since the nominal values of real part and imaginary part times frequency are respectively -120 Ω and + 160 Ω for perfect operation, it can be seen that the data of Fig. 10 represents nearly ideal behavior.

Figure 11 shows the measured input impedance of the "idealized" circuit shown; a number of points merit comment. First, since no load compensation was used, the results shown represent that which is relatively easy to achieve; variation of the load should produce further improvement. The short lengths of coaxial cable shown in the diagram were for the attachment of monitoring equipment which was not being used when these measurements were made; it is probable that they contributed to capacitive compensation at the input, as discussed above. It should be noted that the real part of the measured impedance is not zero but rather is equal to the 100 Ω contributed by the resistance in series with the input. Since the RC realization theoretically requires a series resistance to achieve a purely reactive input impedance, this result is somewhat surprising. It is felt that resistances unaccounted for in the original analysis (particularly base resistances) are producing this result. In any case, removal of the 100 Ω resistor (or replacing it by a much smaller resistor) would obviously yield the desired, purely reactive, input impedance.

The operation of this circuit in the 1 - 10 MHz band, and the degree of success achieved without using the more elaborate load-compensation techniques discussed above, warrant some optimism for achievement of the desired input impedance at higher frequencies.

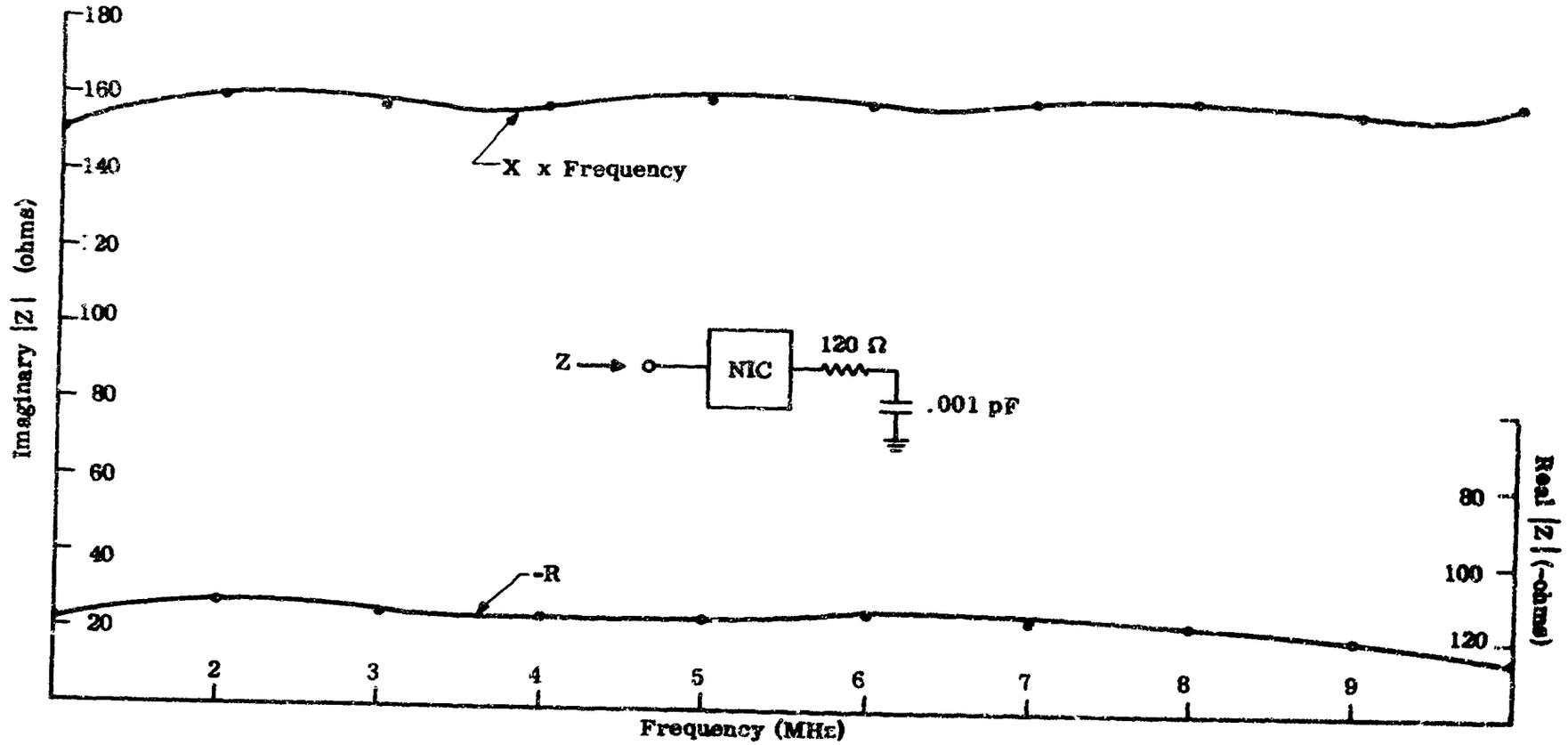


FIG. 10: Measured input impedance of NIC.

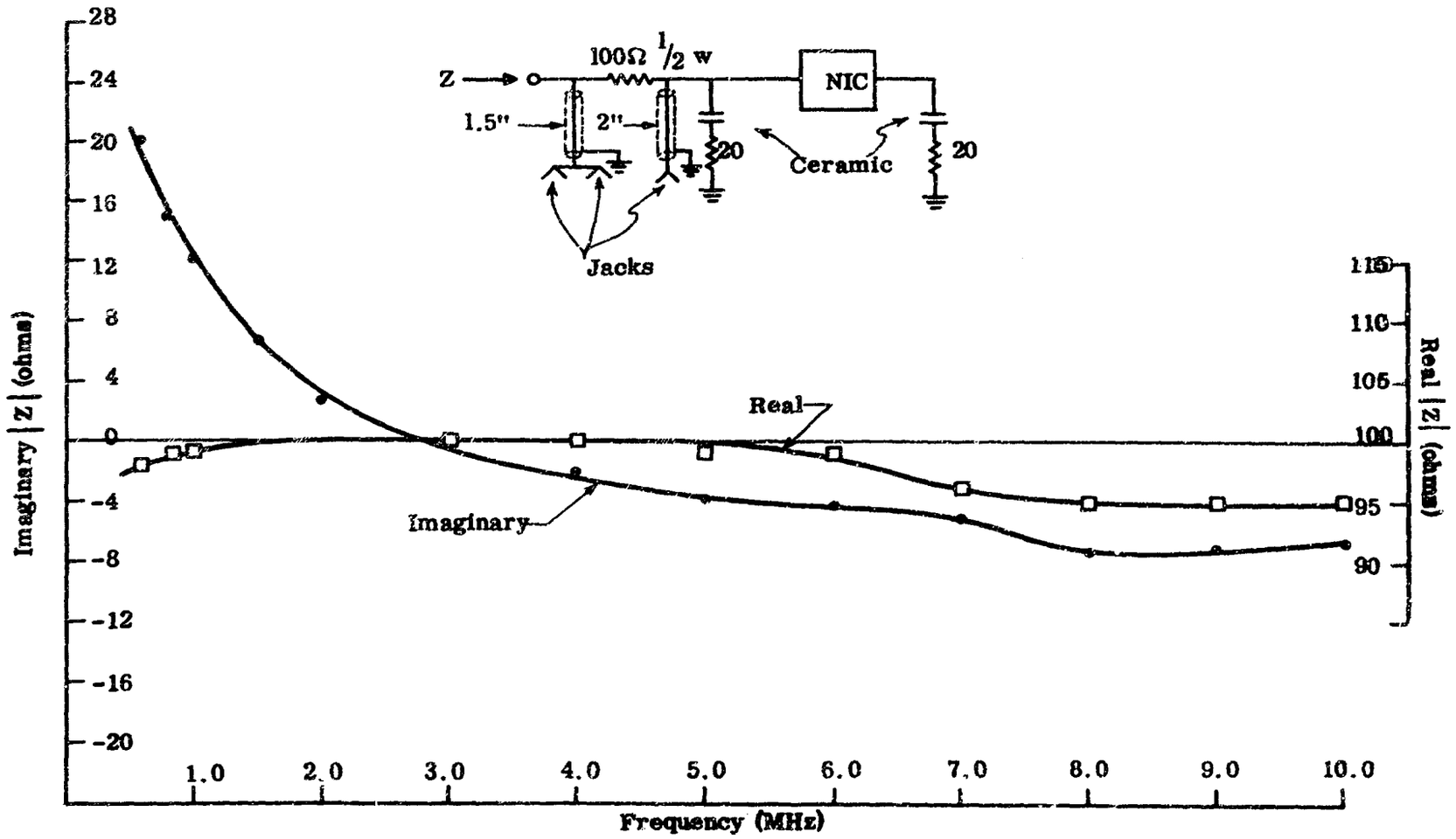


FIG. 11: **Measured impedance of RC realization.**

A variation on this circuit, carrying out the same realization in a different manner, has also proved successful. Referring back to Eq. (24), the admittance is expanded in the form

$$Y_1(s) = \frac{\frac{a}{1-a^2}s}{s+\frac{1}{a}} - \frac{\frac{a}{1-a^2}s}{s+a} .$$

In the circuit discussed above, this was realized by a series RC network in parallel with a negative, series RC network consisting of a NIC loaded by a series RC combination. An alternative realization is obtained by expanding the second term on the right side in partial fractions, yielding

$$-\frac{\frac{a}{1-a^2}s}{s+a} = -\frac{a}{1-a^2} + \frac{\frac{a^2}{1-a^2}}{s+a} \tag{26}$$

which is a negative resistance in parallel with a postive, series RL combination. This leads to the realization of Z(s) shown in Fig. 12. The complete circuit is shown in Fig. 13, and measured results are displayed in Fig. 14. Although the frequency

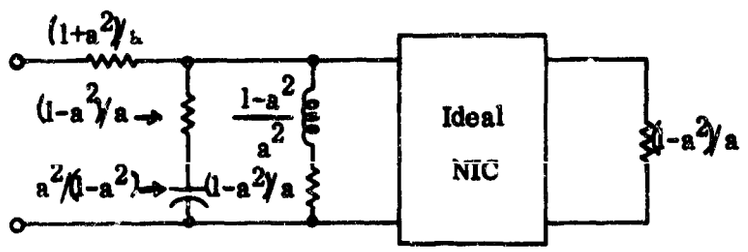


FIG. 12: Alternate realization of Z(s) .

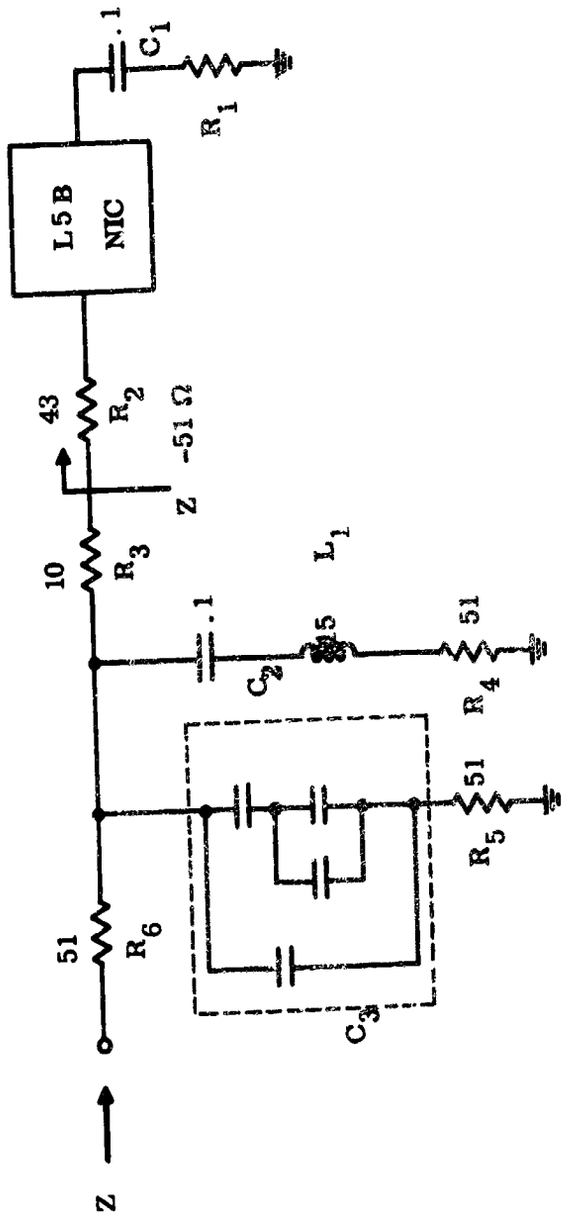


FIG. 13: RL realiza. on.

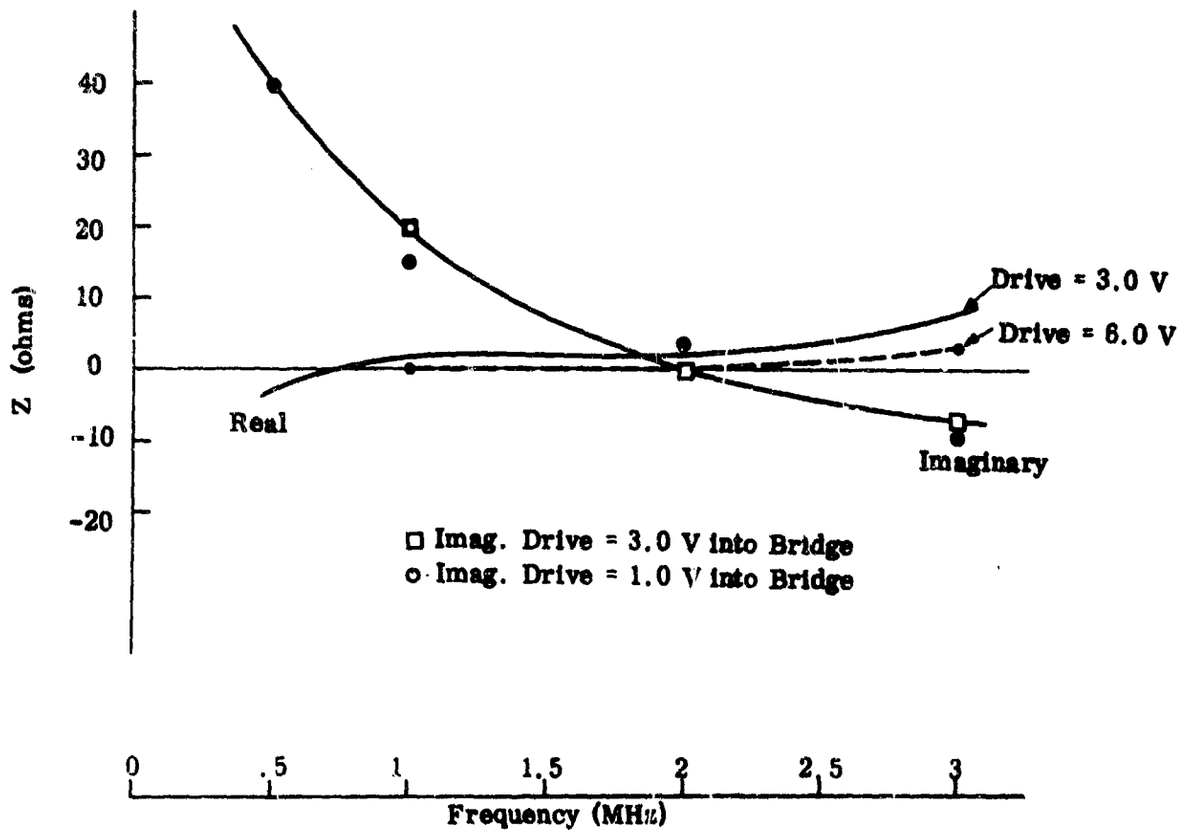


FIG. 14: Measured impedance of RL realization.

range is somewhat lower, the results are as good or better than those from the previous realization, and the circuit appears somewhat more stable. The principal limitation at this point seems to be the passive components rather than the NIC; the stray capacitance of the resistances is particularly troublesome. Ways of alleviating these difficulties are being studied, and development of the circuit is being actively pursued.

III
OTHER REALIZATIONS

Although the Yanagisawa NIC has been investigated to the greatest extent, others have been considered to some degree. One circuit which was briefly considered was given by Larky (1957); it is shown in Fig. 15. The operation of

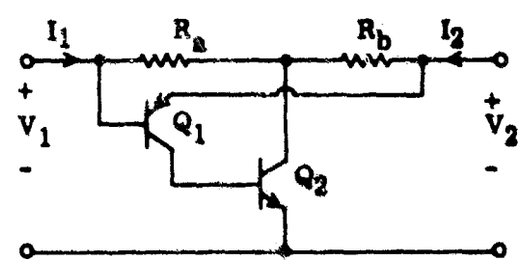


FIG. 15: Larky NIC circuit.

this circuit is in many respects quite similar to that of the Yanagisawa circuit. Since V_1 and V_2 differ only by the base-emitter drop of Q_1, they are essentially equal. Neglecting base current, all of I_1 flows through R_a; since the equality of

V_1 and V_2 produces equal voltages across R_a and R_b, we have $I_1R_a = I_2R_b$, thus achieving NIC action.

This circuit was investigated in the hope that it might have some theoretical advantage over the Yanagisawa circuit in terms of phase shift, stability, etc. No such advantage was in fact found, and since biasing of this circuit is more difficult, the investigation was carried no further.

Since there is a strong tendency among designers of active networks toward the adoption of the differential-input operational amplifier as a "universal" active element, a NIC realization using such an amplifier received considerable attention. The fact that development of this circuit is not being actively pursued at the present time is the result of limited manpower rather than unsatisfactory results.

The diagram of this circuit is given in Fig. 16. Although based on completely

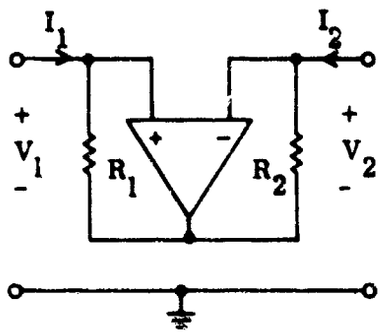


FIG. 16: Operational amplifier NIC.

different physical mechanisms, the operation of the circuit is very similar to that of the Larky circuit. The virtual short at the amplifier input forces the approximate equality of V_1 and V_2, and thus of the voltages across R_1 and R_2. Since the amplifier draws no input current, I_1 and I_2 flow in R_1 and R_2, respectively. It therefore follows that $I_1R_1 = I_2R_2$. More exact analysis yields essentially the same result provided $r_o \ll R_1, R_2 \ll r_i$ and $\mu \gg 1$, where

r_i and r_o are respectively, the input and output impedances of the amplifier, and μ is the open circuit voltage gain.

A conventional differential amplifier was constructed using 2N 4959 transistors. A number of feedback compensation schemes were tried before settling on a series RL feedback element. Reasonably flat gain to 100 MHz was thereby achieved; this was accompanied, however, by phase shift of almost 30° at 100 MHz. The gain was also disappointing low, on the order of 5 - 10 dB in all cases giving otherwise reasonable results.

Despite these difficulties, the circuit of Fig. 16 operated successfully as a NIC, although the conversion factor was frequency dependent both in magnitude and phase. It is felt that the real usefulness of this approach is dependent on the development of an integrated or hybrid, high-frequency differential amplifier. With the rapid advances being made in the solid state and integrated-circuit areas of technology, the development of the necessary amplifier should not lie too far in the future.

VHF amplifiers which are commercially available at the present time most commonly have 50 Ω input and output impedances and linear phase shift in the gain characteristic. An investigation into the usability of such amplifiers as the active element in a NIC has been undertaken. The investigation was aimed at obtaining a practical realization of the ideal NIC illustrated in Fig. 17, in which

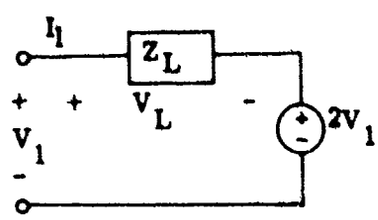
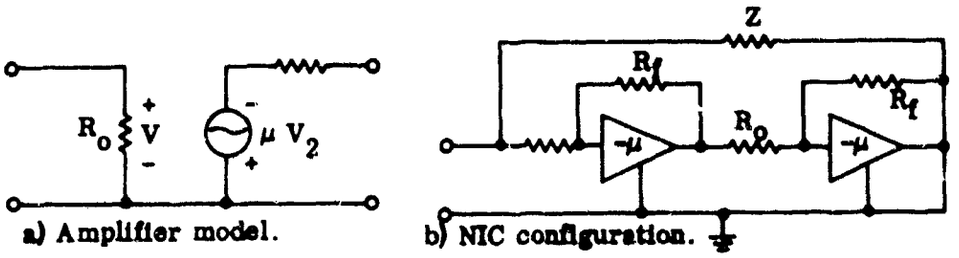


FIG. 17: Amplifier NIC .

an ideal, voltage-controlled voltage source is used to make $V_L = -V_1$, thus giving $I_1 = -V_1/Z_L$ and $Z_{in} = -Z_L$. An extremely straightforward approach to this realization uses two stages, each consisting of an inverting amplifier with large negative feedback. Each stage is assumed to have input and output impedance R_o; the model assumed for the amplifier and the diagram of the NIC circuit are shown in Fig. 18. This circuit, as expected, does not behave as an ideal NIC due to the non-zero input admittance and output impedance of the amplifier stages.



a) Amplifier model. b) NIC configuration.

FIG. 18: Realization of NIC with amplifiers ($R_f = \sqrt{2}\ R_o$).

Analysis has shown that the input admittance of the circuit of Fig. 18 b is given by

$$Y_{in} = \frac{a-bY}{c+dY}, \tag{27}$$

where a, b, c and d are appropriately dimensioned constants. Letting $Y = \frac{a}{b} + Y_L$, which is equivalent physically to connecting a resistance $R_p = b/a$ in parallel with the desired load, gives

$$Z_{in} = \frac{c + \frac{ad}{b} + d\,Y_L}{-b\,Y_L} = -\frac{d}{b} - \frac{ad+bc}{b^2}\,Z_L. \tag{28}$$

Then adding a resistance $R_s = d/b$ in series at the input gives

$$Z_{in} = -\frac{ad+bc}{b^2}\,Z_L = -K\,Z_L \tag{29}$$

The final form of the circuit is shown in Fig. 19. The compensating resistances

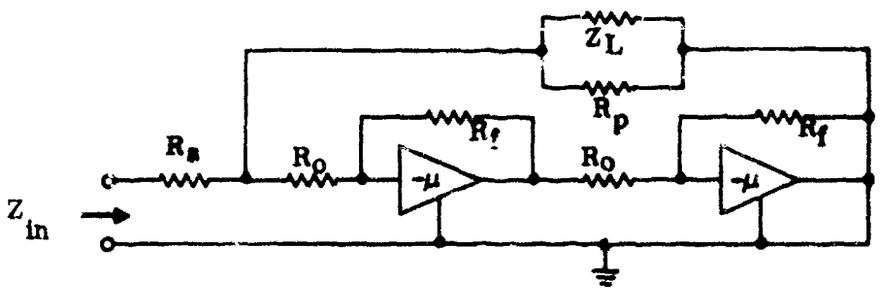


FIG. 19: Feedback amplifier NIC with compensation.

have values $R_p = 0.65\ R_o$ and $R_s = 0.04\ R_o$. Computer analysis of this circuit, with phase shift in the amplifiers neglected, showed essentially ideal NIC operation. Phase shift was then introduced by replacing the amplifier model of Fig. 18a with the model shown in Fig. 20, with R and C chosen to give 45° phase shift (and 3 dB gain reduction) at the highest frequency investigated.

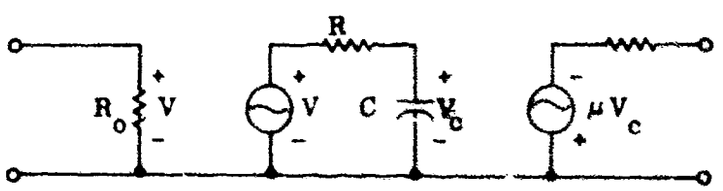


FIG. 20: Amplifier model with phase shift.

Because of the large negative feedback in the overall circuit, this large open-loop phase shift had a surprisingly small effect. Calculated results for a series RC load, both with and without phase shift, are shown in Fig. 21. The figure also shows the load impedance required to compensate for phase shift and produce the correct input impedance. Since this is a smooth curve in the Z-plane, it should be possible to match it quite closely with a fairly simple

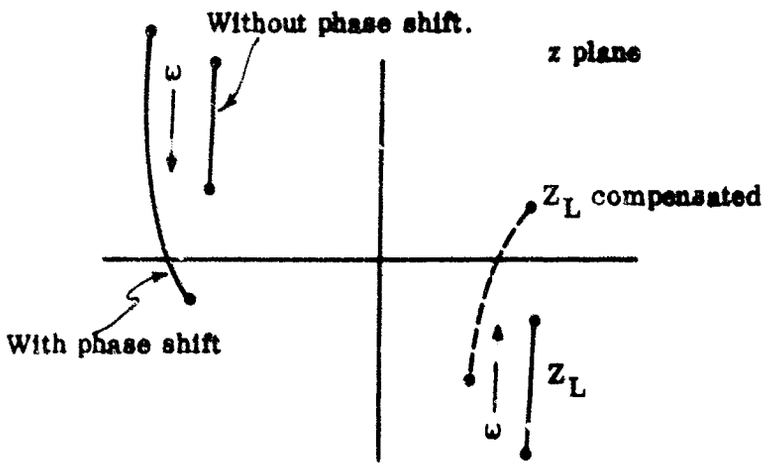
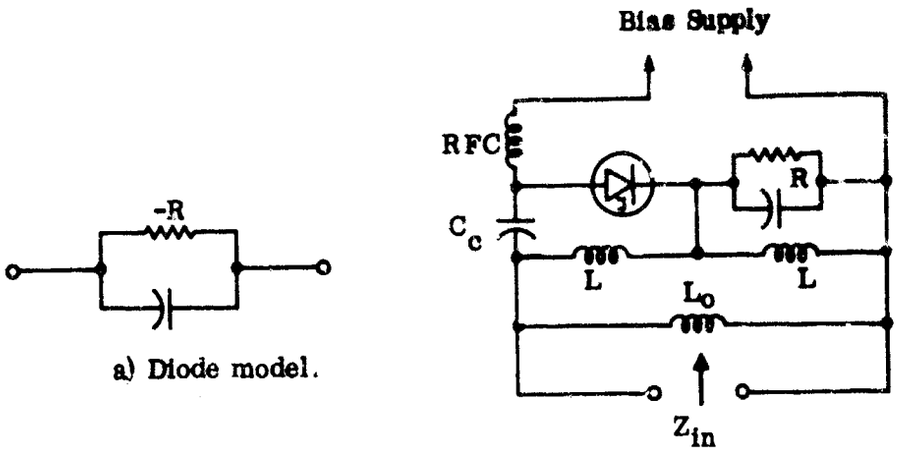


FIG. 21: Effect of phase shift on NIC performance.

network similar to that shown in Fig. 8b . Due to the tediousness of the calculations, the load parameters were not determined but the process is relative straightforward.

The NIC is not the only active device which could be used to realize the desired impedance, although many of the other possibilities (operational amplifiers, controlled sources, etc.) actually reduce to variations of the NIC. One approach which does not fall into this category is a realization using the negative-resistance characteristic of a tunnel diode. Although unsuccessful, this realization is presented for the sake of completeness. The tunnel diode may be modelled to the first order, by a negative resistance in parallel with a capacitance, as shown in Fig. 22a. After examining various configurations incorporating the model, the circuit of Fig. 22b was arrived at. Straightforward analysis indicates that Z_{in} of this circuit should exhibit a negative resistive characteristic in a band around the resonant frequency of the LC combination. In practice, difficulties with biasing and stability proved insurmountable, and the investigation was not pursued further.



a) Diode model.

b) Complete circuit.

FIG. 22: Tunnel-diode negative-reactance circuit.

IV

CONCLUSIONS

To date, this investigation has produced one circuit (the Yanagisawa NIC) which operates satisfactorily in the 1 - 10 MHz range without load compensation, and which shows promise for operation at substantially higher frequencies. Another circuit, the operational amplifier NIC, has been shown to be feasible, although limited by the present state of the art. A very promising configuration using single-ended amplifiers with 50 Ω input and output impedances has been investigated analytically and numerically, with excellent results. An RC realization of the desired impedance has been developed, and the technique of modifying this realization to compensate for phase shift and other imperfections in the NIC has been shown to be feasible.

REFERENCES

Kinariwala, B.K. (1959), "Synthesis of Active RC Networks," Bell System Technical Journal, 38, pp.1269-1316.

Larky, A.I. (1957), "Negative Impedance Convergers," IRE Trans., CT-4, 124-131.

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13. ABSTRACT

Techniques for realizing a reactance which is a decreasing function of frequency are discussed. A Negative Impedance Converter (NIC) circuit is analyzed and techniques given for compensating for imperfections and frequency dependence. An RC realization of the desired impedance is given, and it is demonstrated that this realization can be modified to compensate for phase shift in the NIC. An analytical and numerical analysis of a NIC based on amplifiers with 50 ohm input and output impedances is presented.

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