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# RESEARCH AND DEVELOPMENT OF HIGH SPEED PROCESSOR ARRAYS

Prepared by
Philco-Ford Corporation
Microelectronics Division
Blue Bell, Pennsylvania 19422

For
Massachusetts Institute of Technology
Lincoln Laboratory

AD0694554

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SECOND INTERIM REPORT
March 1969

# RESEARCH AND DEVELOPMENT

# OF

# HIGH SPEED PROCESSOR ARRAYS

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Under
Purchase Order BB-398
Prime Contract No. AF 19(628)-5167

Period Covered:
22 October 1968 to 21 January 1969

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## ABSTRACT

The reported work was performed during the second interim (quarterly) period of a research and development program directed toward the development of high density, high performance, complex digital arrays and their application in high speed system feasibility studies.

During this interim, high speed ECL microcircuit cells of several designs were fabricated and characterized. Specific gate and reference bias circuits were selected for use in the Processor Arrays.

Development continued on high yield microcircuit and multilevel interconnection techniques. Preliminary design of a multilevel process evaluation chip was completed.

Thermal studies of discretely packaged high power (1 watt) LSI chips were made using a thermal test chip as a vehicle.

Final design of a 256-Bit Read-Only Memory Array was completed.

The photomasks were all generated using computer aid.



Accepted for the Air Force
Franklin C. Hudson
Chief, Lincoln Laboratory Office

CONTENTS


| | Page |
|---|---|
| I - INTRODUCTION | 1 |
| 1.1 Program Objective | 1 |
| 1.2 Areas of Investigation | 1 |
| II - PROGRAM DEVELOPMENTS | 3 |
| 2.1 Introduction | 3 |
| 2.2 Selection of Basic Gate and Reference Bias Circuits For Processor Arrays | 4 |
| 2.3 Read-Only Memory | 10 |
| 2.4 High Yield Microcircuit Array Fabrication Technology | 13 |
| 2.5 Thermal Studies | 15 |
| 2.6 Multichip Assembly Techniques | 17 |
| III - FUTURE PLANS | 19 |
| IV - DELIVERIES | 20 |

## ILLUSTRATIONS


| | | Page |
|---|---|---|
| Figure 1. | Schematic diagrams of high-speed ECL gate cells and reference bias cells. ---------- | 5 |
| Figure 2. | Photomicrograph of SMX14 Microcircuit Test Chip. -- | 6 |
| Figure 3. | Schematic diagram illustrating the technique employed to measure propagation delay time on SMX14 ECL gates. ---------- | 7 |
| Figure 4. | Diagram of small geometry, high speed transistors employed in SMX14 gate cells. ---------- | 9 |
| Figure 5. | $f_T$ versus $I_E$ for transistors of gate design #1. --- | 11 |
| Figure 6. | $f_T$ versus $I_E$ for transistors of gate design #2. --- | 11 |
| Figure 7. | Schematic diagram of Read-Only Memory Array. ------ | 12 |

## TABLES


| | | Page |
|---|---|---|
| Table I | - Propagation Delay and Power Dissipation Data for Gate Designs #1 and #2 ---------- | 8 |
| Table II | - Thermal Characteristics of Thermal Chip Uniformly Powered to Level of 1 Watt ---------- | 16 |
| Table III | - Thermal Characteristics of Thermal Chip - One Quadrant Powered to 400 mW ---------- | 16 |

# I - INTRODUCTION

## 1.1 PROGRAM OBJECTIVE

The objective of this program is the continued development of high density, high performance, complex digital arrays and their application in high speed system feasibility studies.

## 1.2 AREAS OF INVESTIGATION

During the past few years, Philco-Ford has directed research and development efforts toward the establishment of device, microcircuit, and large-scale array technologies which can be applied in high speed complex data processing systems. This has been accomplished in part on previous programs subcontracted to Philco-Ford by MIT Lincoln Laboratory, under the primary sponsorship of the United States Air Force. During the present program, development of these technologies is continuing. In addition, specific two- and three-level arrays are being designed and fabricated for application in feasibility studies of a high speed Central Processor. Program efforts will also include the continued investigation of multichip assembly techniques which are compatible with high speed systems.

The principal responsibility of Philco-Ford is the fabrication and preliminary testing of the designed devices, microcircuits and

arrays. In addition, Philco-Ford is serving as technology consultants by specifying component, microcircuit and array design rules.

# II - PROGRAM DEVELOPMENTS

## 2.1 INTRODUCTION

During this interim, we continued efforts toward selecting the basic ECL gate and reference circuit layout designs for use in high speed Processor Arrays. These efforts culminated in the selection of basic gate and reference circuit layouts. In addition, the preliminary and final designs for a 256-Bit Read-Only Memory array, having 256 transistors, was completed.

The development of high yield microcircuit and multilevel interconnection techniques was continued. Preliminary design of a "Multilevel Process Test Chip," to be used for process evaluation studies and for process control, was completed. Also, techniques were investigated for simplifying microcircuit fabrication for purposes of decreasing process defects and increasing yield.

Investigations were begun into the thermal aspects of packaging microcircuit and microcircuit array chips which dissipate on the order of 1 watt, the level of dissipation anticipated for typical processor array chips. In conjunction with this effort, initial designs for face-down bonded and beam lead versions of the Thermal Chip test vehicle were completed.

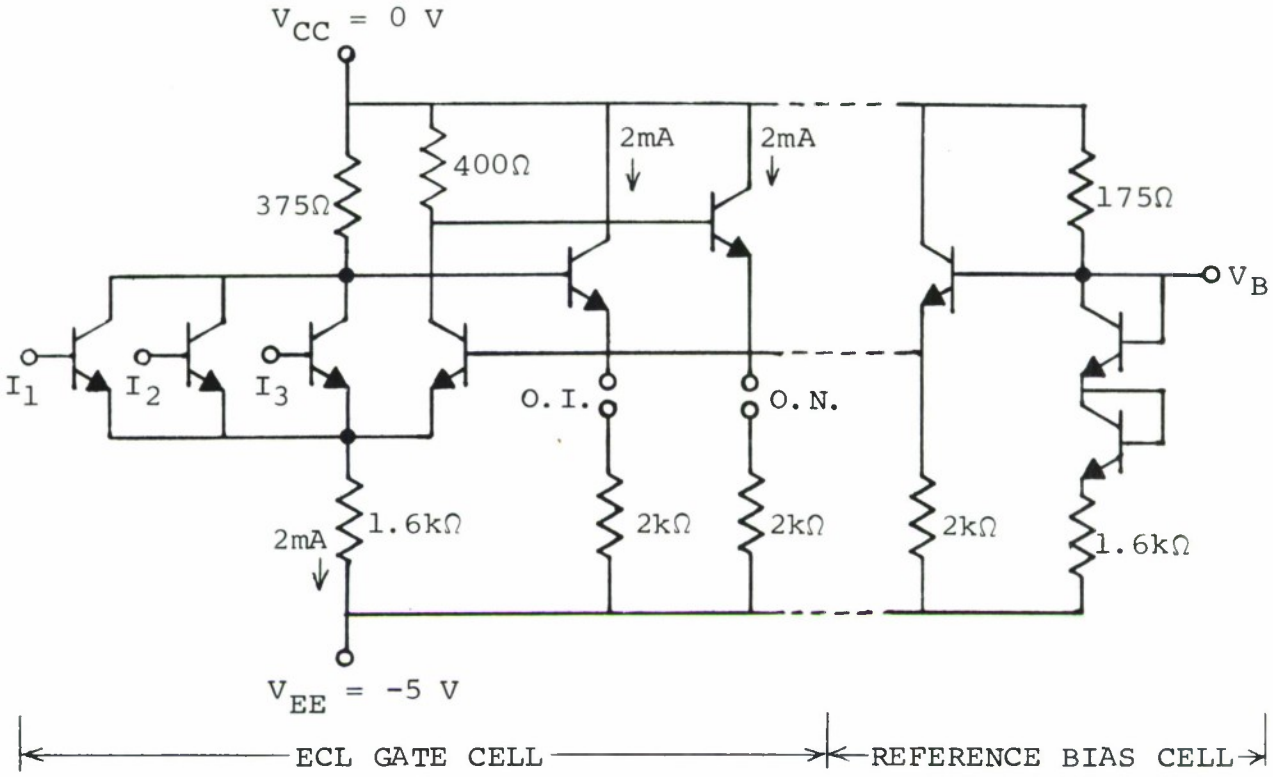
## 2.2 SELECTION OF BASIC GATE AND REFERENCE BIAS CIRCUITS FOR PROCESSOR ARRAYS

The selection of the basic gate and reference bias circuit layouts to be used on complex Processor Array chips (as indicated in the First Interim Report) was to have been based on evaluations of microcircuit versions of the two circuit designs shown in Figure 1. During this interim, a microcircuit test chip (referred to as SMX14) containing these two circuit designs was designed. Samples were fabricated, packaged and delivered to MIT Lincoln Laboratory for evaluation. Figure 2 illustrates the SMX14, a 100 x 100 $mils^2$ chip which contains, in addition to the complete microcircuits, a variety of test transistors and resistors, sheet resistance test patterns, and a via test vehicle having ten series-connected vias.

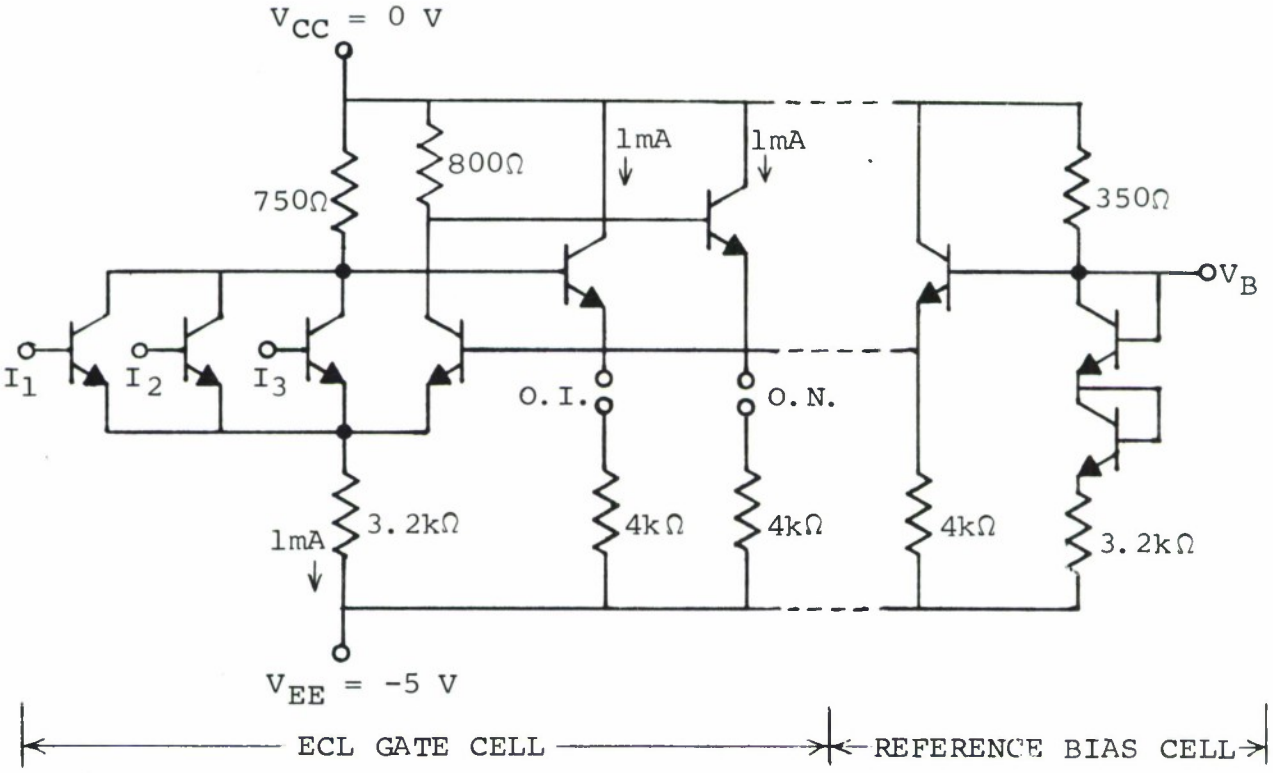
The SMX14 test chip actually contains groups of each of the gate types, interconnected through two levels of metal in a manner that allows measurement of the basic gate speed in an array environment. Figure 3 is a schematic diagram of the interconnection scheme. After measuring $\tau_{pd(chain)}$ and $\tau_{pd(ref)}$, the average propagation delay time, $\tau_{pd}$, of a single gate, unaffected by the test apparatus, is obtained using the expression

$$\tau_{pd} = \frac{\tau_{pd(chain)} - \tau_{pd(ref)}}{4}$$

where $\tau_{pd(chain)}$ is the propagation delay through the chain of




a. Design #1.




b. Design #2.

Figure 1. Schematic diagrams of high-speed ECL gate cells and reference bias cells.

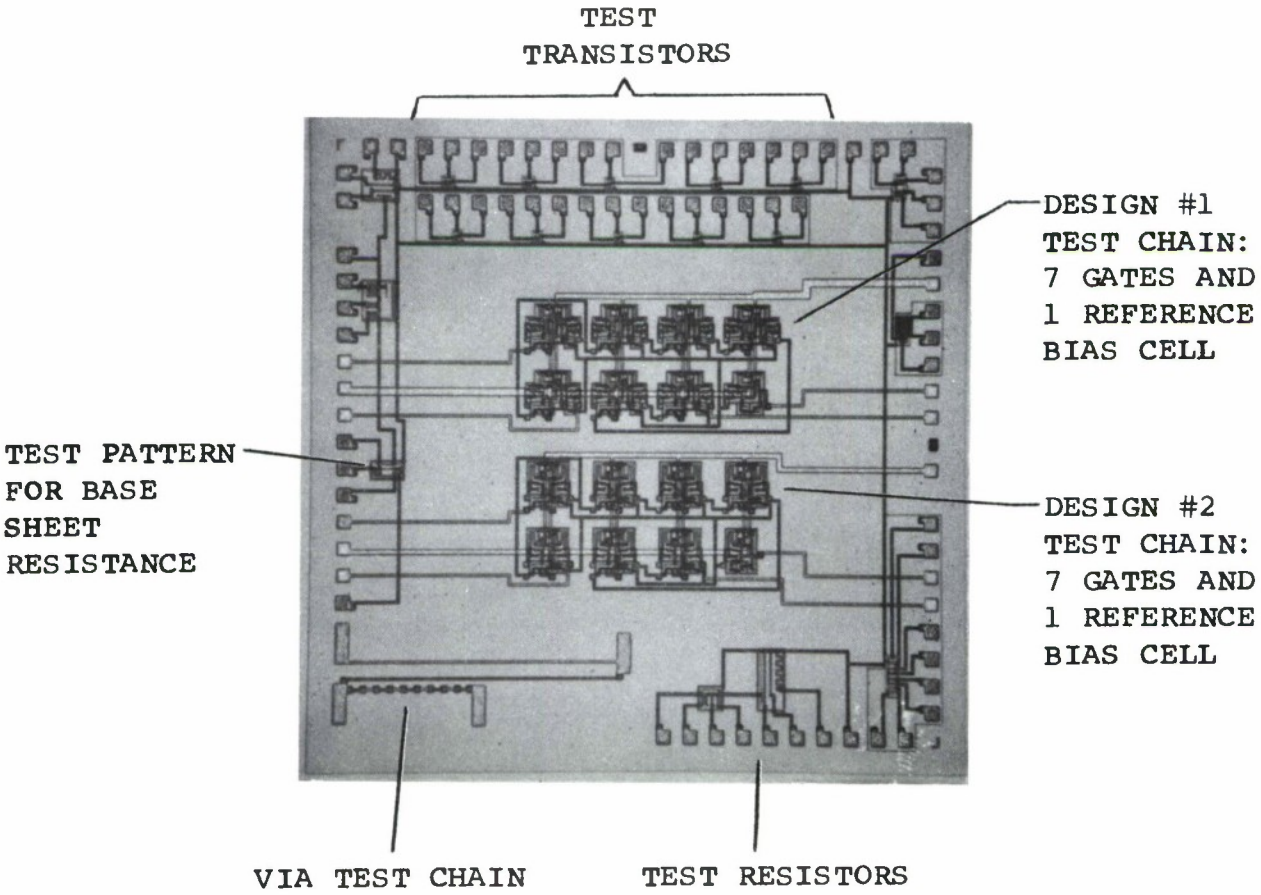
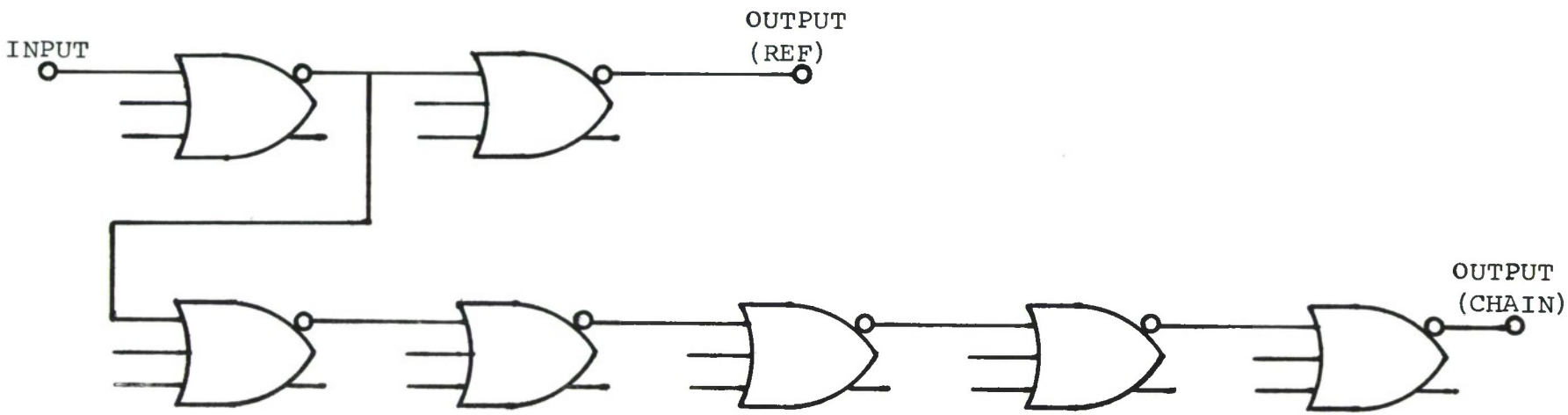



Figure 2. Photomicrograph of SMX14 Microcircuit Test Chip.




NOTE: ALL UNUSED INPUTS ARE BIASED "OFF".

Figure 3. Schematic diagram illustrating the technique employed to measure propagation delay time on SMX14 ECL gates.

six gates and $\tau_{pd(ref)}$ is the propagation delay through the input and output stages only.

In evaluation tests, both versions of the ECL gate operated at subnanosecond speeds, confirming their design predictions. Table I lists the propagation delay-power dissipation data for both gate designs. Each of the emitter followers in the gates (under low fan-out conditions) was designed to dissipate the same power as the current switch; consequently, the designed total power dissipation for Design No. 1 was 30 mW, and for Design No. 2, was 15 mW. Inasmuch as the resistors of the first samples were fabricated 20% above design value, the power dissipations listed in Table I are approximately 20% lower than design center values.

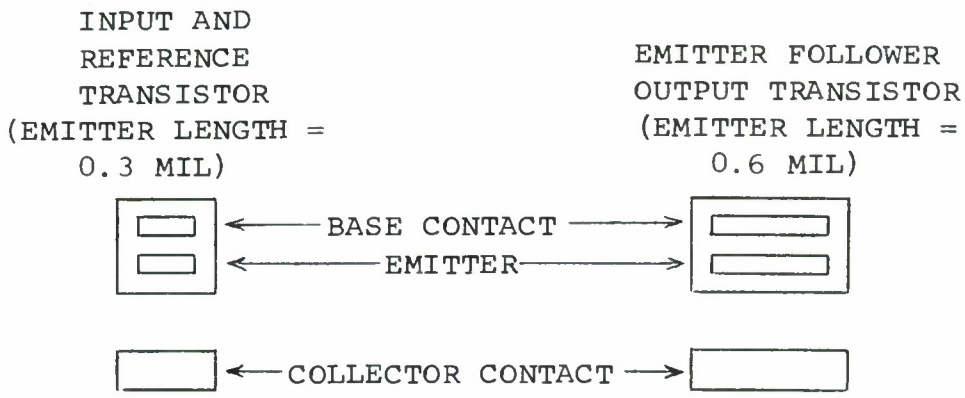
TABLE I

Propagation Delay and Power Dissipation Data for Gate Designs #1 and #2

| Gate Design | Total Gate Power* | $\bar{\tau}_{pd}$** |
|---|---|---|
| #1 | 24 mW | .52 n sec. |
| #2 | 12 mW | .60 n sec. |

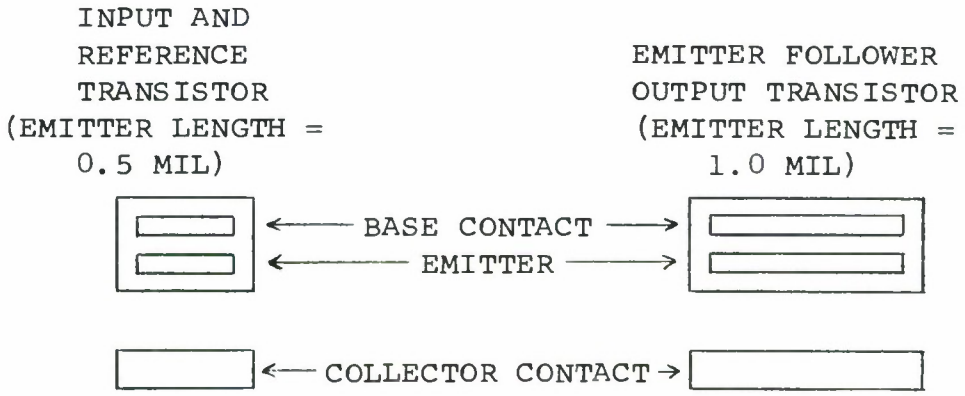
* - Including Complementary Outputs
** - Fan-out = Fan-in = 1

The transistors used in Gate Designs No. 1 and No. 2 are shown in Figures 4a and 4b, respectively. Typical $f_T$ versus $I_E$ curves




a. Transistors employed in gate design #1.

SCALE: ⇥|⇤ = 0.1 MIL




b. Transistors employed in gate design #2.

Figure 4. Diagram of small geometry, high speed transistors employed in SMX14 gate cells.

for these devices are shown in Figures 5 and 6. The emitter-follower transistors are designed to conduct 4 mA and 2 mA (Designs No. 1 and No. 2, respectively) under maximum fan-out conditions.

Based on the data obtained for Gate Designs No. 1 and No. 2, Design No. 2 was selected for tentative use in the Processor Arrays. Meanwhile, additional propagation delay-power dissipation data will be accumulated using the SMX14 chip by varying the values of resistor sheet resistance. Of particular interest is the propagation delay at lower levels of power dissipation -- levels down to 5.0 mW/gate.

## 2.3 READ-ONLY MEMORY

Preliminary and final layout designs for a 256-Bit Read-Only Memory (ROM) Array have been completed during this period. Shown schematically in Figure 7, the ROM will consist of an array of 256 high speed transistors interconnected through two levels of metal to form a programmable matrix of 16 words, with 16 bits per word. This ROM chip, designated the SMX15, is a refined version of the ROM developed during the previous program.* Among the refinements are the following:

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* "R&D of the Technologies Required to Design and Fabricate Ultra-high-Speed Computer Systems," Final Report dated January 1969 covering the period July 1, 1967 to June 30, 1968, prepared by Philco-Ford Corporation, Microelectronics Division for MIT Lincoln Laboratory under Purchase Order No. BB-114, Prime Contract No. AF19(628)-5167.

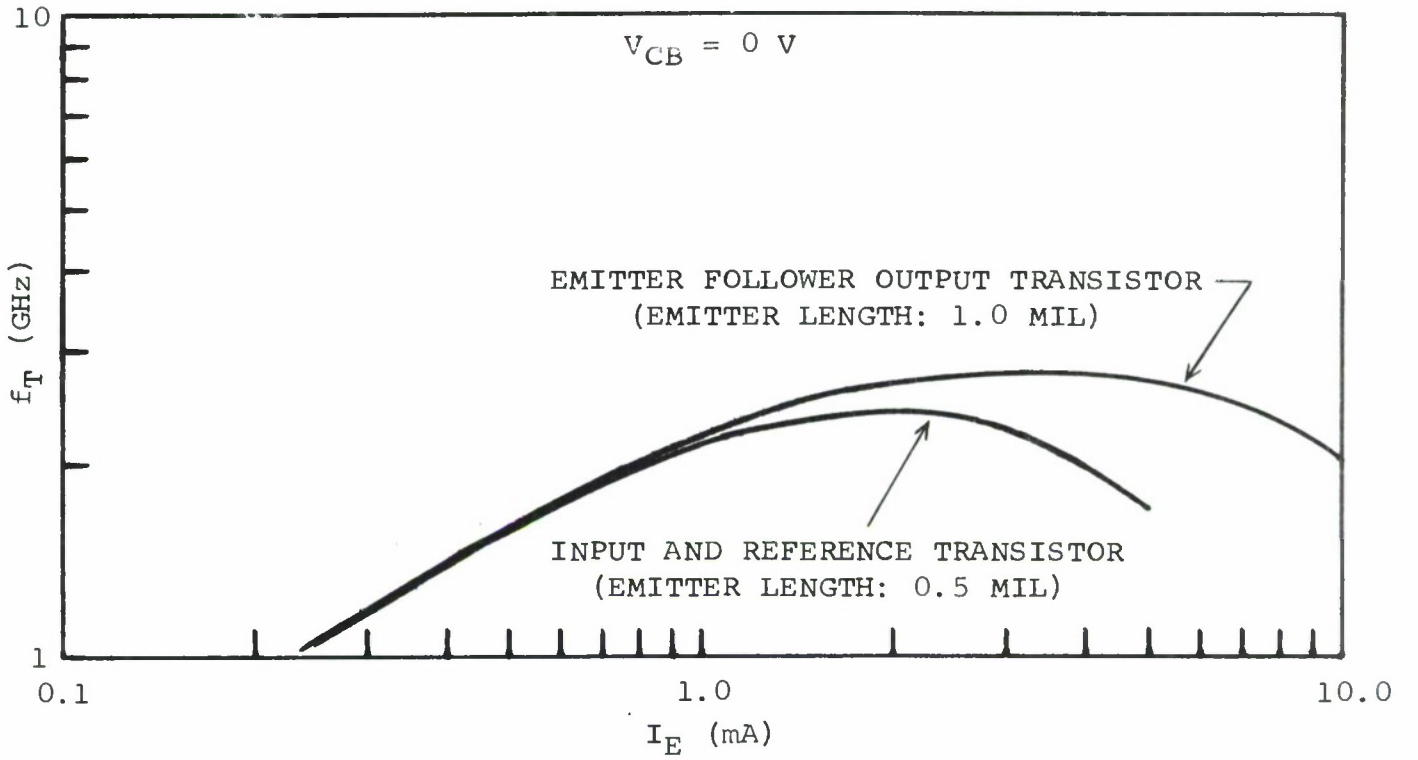


Figure 5. $f_T$ versus $I_E$ for transistors of gate design #1.

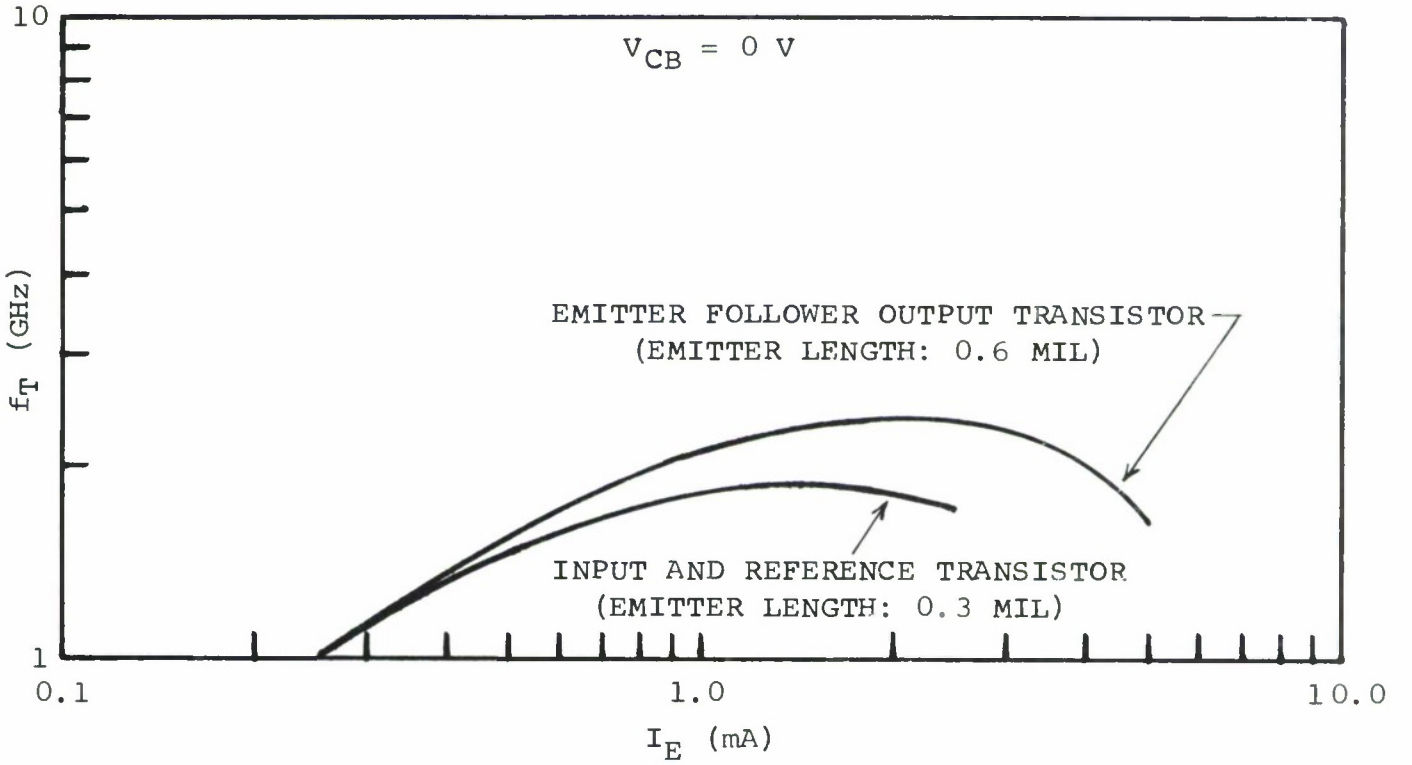


Figure 6. $f_T$ versus $I_E$ for transistors of gate design #2.

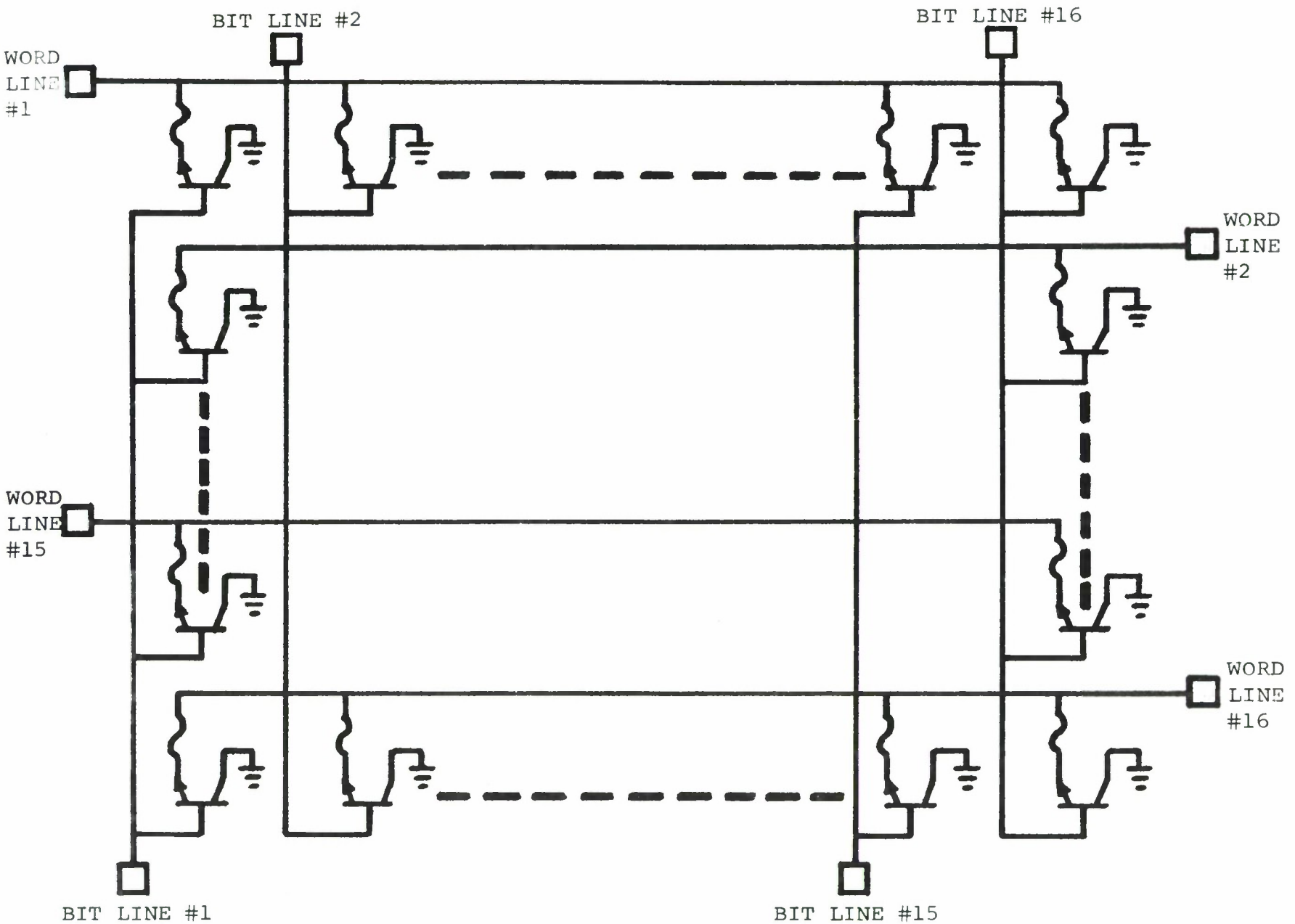


Figure 7. Schematic diagram of Read-Only Memory Array.

1. Transistors have a larger drive capability.
2. Programming options are provided in the emitter-conductor lines rather than in the base-conductor lines.
3. Fine-line fuse links are provided in the second level of metal so that programming of the ROM can be attempted at the chip level. The ROM can, of course, be programmed at the wafer level by customizing either the "via" mask or the mask for the top level of metal.

Fabrication of the ROM will begin early in the next interim. Initial samples of the ROM are expected before the end of the next interim.

## 2.4 HIGH YIELD MICROCIRCUIT ARRAY FABRICATION TECHNOLOGY

Die sort data obtained on the first SMX14 wafer indicated a 29% yield of chips containing, effectively, 16 functional gates. Calculations indicate transistor yield to be about 98%. While this yield is encouraging, considering that it was obtained on the first wafer of this particular microcircuit design, higher yields are required to insure that functional arrays of the anticipated complexity of the Processor Arrays (60 to 80 gates) can be laboratory fabricated at practical yields. Additional SMX14 wafers are nearly completed. These will be carefully analyzed in an effort to

determine how yields can be further improved. A number of technology refinements related to photoengraving, epitaxial layer growth, and wafer processing will be evaluated.

Microcircuit yield is an inverse function of microcircuit area and of the complexity of the microcircuit fabrication process. Consequently, methods for increasing component densities and simplifying the required microcircuit processing are being investigated in an effort to improve the yield. One particular process similar to the Collector Diffused Isolation (CDI) Process introduced by B. Murphy* is being examined for use with high speed ECL. This process has two less photoengraving steps than the conventional process and can lead to a factor of two or more increase in component density. A tentative design for a single ECL gate was completed, and preliminary experiments with shallow (1.0 to 1.5 μ) p-type epitaxial layers were concluded. Final design and the start of fabrication of the CDI-ECL gate structure are planned for the next interim.

As indicated in subsection 2.2, the SMX14 test chips contain via test patterns. Evaluations of the first lot of SMX14 chips confirmed that our present two-level design rules and two-level interconnection process result in reproducible, low resistance

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* Murphy, B. T., Neville, S. M., and Pederson, R. A., "New, Simplified, Bipolar Technology and Its Application to Systems," ISSCC Digest of Technical Papers, pp. 150-153; February 1969.

interconnects between levels. Interlevel resistance for a via with a 0.12 $mil^2$ cross section is about 67 mΩ.

Future evaluations of our multilevel process and refinements in the process will use a "Multilevel Process Chip" (MLPC). The preliminary design of the MLPC has been completed. The MLPC will simulate small-geometry microcircuit-level topographies, and will contain a number of test patterns designed for monitoring the quality of the insulating layers and the effectiveness of various geometries of vias and conductors in multilevel structures. The MLPC will be used as a study vehicle and as a process monitor.

## 2.5 THERMAL STUDIES

During the preceding interim, a microcircuit test chip referred to as the Thermal Chip was designed and fabricated for studying thermal properties of large microcircuit chips which dissipate substantial power (about one watt). During this interim, preliminary experiments were performed using the Thermal Chip.

The Thermal Chip is a 100 x 100 $mil^2$ chip consisting of a matrix of heating resistors and an array of sensing resistors dispersed throughout the chip. All four quadrants of the chip have design symmetry and can be powered independently. In one experiment, the entire chip was powered to the 1 watt level and the temperature of the chip surface was sampled in various places. The package was not heat sunk. This experiment was repeated with

the package heat sunk to a copper block measuring approximately 1.0" x 0.5" x 0.1". In another experiment, one quadrant of the chip was powered to the 400 mW level. Again junction temperatures were measured with and without heat sinking the package. Table II and III give results of these experiments. In all experiments, temperature was determined using infrared scanning techniques. The Thermal Chips were mounted in 40-lead metal-bottom flat packs having a 0.5" body diameter.

TABLE II

Thermal Characteristics of Thermal Chip
Uniformly Powered to Level of 1 Watt

| | Junction Temperature Range on Chip | Thermal Resistance*- Junction to 27°C Free Air |
|---|---|---|
| Package Not Heat Sunk | 93.5 - 99.3°C | 72.3° C/Watt |
| Package Heat Sunk to Cu Plate | 67.3 - 72.0°C | 45.0° C/Watt |

* Calculated using the maximum temperature on the chip.

TABLE III

Thermal Characteristics of Thermal Chip -
One Quadrant Powered to 400 mW

| | Junction Temperature Range in Powered Quadrant | Junction Temperature Range in Unpowered Quadrants | Thermal Resistance* - Junction to 27°C Free Air |
|---|---|---|---|
| Package Not Heat Sunk | 53.7 - 54.5°C | 50.7 - 53.5°C | 69°C/Watt |
| Package Heat Sunk to Cu Plate | 42.3 - 43.4°C | 40.7 - 43.4°C | 41.2°C/Watt |

* Calculated using the maximum temperature on the chip.

These experiments showed that junction temperatures on an LSI chip which dissipates 1 watt and is packaged in a 40-lead, metal-bottom flat pack can be expected to be about 100°C. They further show that simple heat sinking is effective in reducing this temperature. It should be noted that the thermal resistance, junction to air, of the packaged device was similar for the two different power configurations but consistently lower for the case of a single powered quadrant. This is because the factor of increase of the effective thermal resistance through the silicon is less than the factor of decrease in total power when comparing the single-quadrant to the full-chip power configurations. Viewed another way, one can see that thermal interactions between the quadrants (treating each as an integral power source) cause the thermal resistance of the system to be higher when all four quadrants are powered.

Thermal studies similar to these will be conducted on beam lead and face-down bonded versions of the Thermal Chip to compare thermal properties of these structures with those of a discretely packaged chip. In addition, the experiments herein described will be repeated so that junction temperatures can be read using the sense resistors located on the Thermal Chip.

## 2.6 MULTICHIP ASSEMBLY TECHNIQUES

In addition to packaging LSI chips individually there is the alternate approach of mounting and interconnecting two or more

to form a multichip assembly. Two popular techniques for multichip assembly are:

(1) the face-down bonding of active chips onto an interconnection substrate through use of interconnect pedestals, and

(2) the face-up or face-down bonding of beam lead chips onto interconnected substrates.

Both of these techniques will be investigated. Photomasks are being designed which will permit the Thermal Chip to be used for this study. The photomasks will be completed during the nest interim.

## III - FUTURE PLANS

Future work on this program will include:

1. Continued development of high-yield fabrication technologies for high speed arrays. This includes the final design and generation of photomasks for the Multilevel Process Chip.
2. Continued speed-power evaluations (particularly at lower power levels) using the SMX14 test chip as a vehicle.
3. Continued yield improvement experiments using the SMX14 test array as a vehicle.
4. Fabrication and evaluation of Read-Only Memory Arrays.
5. Evaluation of the applicability of the CDI process to high speed ECL.
6. Design and fabrication of Processor Arrays using the basic gate and reference bias cells selected during this period.
7. Continued investigation of multichip assembly techniques.
8. Continued thermal studies of high power LSI chips.

## IV - DELIVERIES

The following were delivered to MIT Lincoln Laboratory:

1. Nineteen packaged SMX14 gate test chips,
2. Nineteen packaged test transistors from SMX14 gate test chips.

## DOCUMENT CONTROL DATA - R&D

*(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)*

| | |
|---|---|
| 1. ORIGINATING ACTIVITY *(Corporate author)*<br>Philco-Ford Corporation, Microelectronics Division under Purchase Order No. BB-398 to M.I.T. Lincoln Laboratory | 2a. REPORT SECURITY CLASSIFICATION<br>Unclassified<br>2b. GROUP<br>None |

3. REPORT TITLE

Research and Development of High Speed Processor Arrays

4. DESCRIPTIVE NOTES *(Type of report and inclusive dates)*

Second Interim Report (22 October 1968 to 21 January 1969)

5. AUTHOR(S) *(Last name, first name, initial)*

None given

| | | |
|---|---|---|
| 6. REPORT DATE<br>March 1969 | 7a. TOTAL NO. OF PAGES<br>26 | 7b. NO. OF REFS<br>2 |
| 8a. CONTRACT OR GRANT NO. AF 19(628)-5167<br>b. PROJECT NO. 649L<br>c. Purchase Order No. BB-398<br>d. | 9a. ORIGINATOR'S REPORT NUMBER(S)<br>X-528<br>9b. OTHER REPORT NO(S) *(Any other numbers that may be assigned this report)*<br>ESD-TR-69-246 | |

10. AVAILABILITY/LIMITATION NOTICES

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|---|---|
| 11. SUPPLEMENTARY NOTES<br>None | 12. SPONSORING MILITARY ACTIVITY<br>Air Force Systems Command, USAF |

13. ABSTRACT

The reported work was performed during the second interim (quarterly) period of a research and development program directed toward the development of high density, high performance, complex digital arrays and their application in high speed system feasibility studies. During this interim, high speed ECL microcircuit cells of several designs were fabricated and characterized. Specific gate and reference bias circuits were selected for use in the Processor Arrays. Development continued on high yield microcircuit and multilevel interconnection techniques. Preliminary design of a multilevel process evaluation chip was completed. Thermal studies of discretely packaged high power (1 watt) LSI chips were made using a thermal test chip as a vehicle. Final design of a 256-Bit Read-Only Memory Array was completed. The photomasks were all generated using computer aid.

14. KEY WORDS

| | |
|---|---|
| high speed ECL microcircuit cells | Processor Arrays |
| Read-Only Memory | high-yield array fabrication |
| multilevel process evaluation chip | thermal studies of high power LSI chips |