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(FINAL REPORT)

A FREQUENCY-DIFFERENTIAL PHASE-SHIFT KEYED DIGITAL DATA MODEM FOR OPERATION AT 4800, 2400, 1200, AND 600 BITS PER SECOND OVER LONG-RANGE HF PATHS

G. C. PORTER, M.B. GRAY, and C. E. PERKETT

October 1966

DIRECTOR OF AEROSPACE INSTRUMENTATION
ELECTRONIC SYSTEMS DIVISION
AIR FORCE SYSTEMS COMMAND
UNITED STATES AIR FORCE
L. G. Hanscom Field, Bedford, Massachusetts

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(Prepared under Contract No. AF 19(628)-5536, by General Dynamics, Electronics Division, Rochester, New York.)

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FOREWORD

This final technical report summarizes activity on the study, analysis, development and test of the ANDEFT/SC 320 prototype ultra high speed digital data modem which was fabricated under Contract No. AF 19(628)-5536 and its subsequent modification No. 1. As required by the contract, this report presents the prototype model technique, engineering studies, and laboratory evaluation as its principal contents. It also contains brief sections which discuss growth potential and recommendations for field tests.

Material for the three principal sections was taken from the handbook[1], engineering and tradeoff studies[2], and the test plan and procedures[3] which was used as a guide in the final acceptance tests.

REVIEW AND APPROVAL

This technical report has been reviewed and is approved.

OTIS R. HILL, Colonel, USAF
Director of Aerospace Instrumentation
Program Office

ABSTRACT

The ANDEFT/SC-320 is a variable rate (4800, 2400, 1200, or 600 bits per second) digital data modem prototype specifically designed for reliable communication over long-range high-frequency radio circuits. This modem employs such advanced and proven techniques as frequency-differential phase-shift keying, correlation detection, extended symbol length, guard time, segmented AGC, and dual-mode precision synchronization to combat HF anomalies such as multipath delay spread, frequency selective fading, high intensity atmospheric noise and man-made interference. The modem has provision for dual signal source diversity operation to capitalize on available space, frequency, or polarization diversity facilities, and in addition, can be operated with in-band frequency diversity. The prototype is built in two separate cabinets(modulator and demodulator) to enable field testing and to allow for easy expansion to an ultimate data capacity of 9600 bits per second. This report presents the principles of operation of the modem and the results of tests to determine the back-to-back performance in additive white Gaussian noise.

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SECTION I

INTRODUCTION

In September 1965, the Electronics Division of General Dynamics undertook studies and analyses as a part of Electronics Systems Division Contract AF 19(628)-5536 to apply the design requirements of the correlation detection and crosstalk compensation portions of a proposed ultra high speed digital data modem for HF communication to the construction of a feasibility model for test and evaluation in the laboratory. This model was to include one 600 bit per second (bps) signal detection group to be operated at a keying rate of 37.5 Hz and a baud length of 26.6 milliseconds using four-phase modulation (one bit per orthogonal trigonometric function). However, early in the program the contract was modified and expanded to include the fabrication of a complete variable rate (4800/2400/1200/600 bps) frequency-differential phase-shift keyed digital data modem prototype with the same signalling parameters capable of operating in a nominal 3 kHz channel. Also, the prototype modem was to be designed and fabricated to allow for easy expansion to 7200 and 9600 bps operation without major mechanical or electrical redesign.

The prototype data modem has been completed according to the work statement of the contract. It has been evaluated in the laboratory at General Dynamics in the presence of A. F. technical representatives of the MITRE Corporation at which time back-to-back tests with white noise were performed. This technical report summarizes many technical facts and data which are pertinent to the design, fabrication, operation, and evaluation of the prototype modem.

SECTION II

PRINCIPLES OF OPERATION

Introduction

The ANDEFT/SC-320 ultra high speed digital data modem is specifically designed for high capacity and reliable digital communication over long-range high-frequency radio circuits with an ultimate data capacity of 4800-9600 bps in a standard 300-3000 Hz voice frequency band. This modem employs such advanced and proven techniques as frequency-differential phase-shift keying, correlation detection, extended symbol length, guard time, segmented AGC, and dual-mode precision synchronization to combat HF anomalies such as multipath delay spreads, frequency selective fading, high-intensity atmospheric noise and man-made interference.

The frequency-differential PSK signalling technique (FDPSK) evolved at General Dynamics from studies of techniques which could be optimized in terms of the measured statistical parameters of the HF medium. The DEFT/SC-302 feasibility model (a predecessor of the present equipment), constructed and field tested under Electronics Systems Division Contract No. AF 19 (628)-3268, employed one implementation of the technique. Further Company-sponsored development effort [4, 5, 6] determined that improved bandwidth efficiency could be obtained with the ANDEFT modulating and detecting method and the implementation of this technique would result in an even closer approximation to ideal frequency-differential PSK.

This study revealed that the ANDEFT modulation technique for transmission of digital data would permit a bandwidth efficiency of better than 1.8 bits per cycle of bandwidth which would enable a data capacity of 4800 bps in a standard voice frequency band if quadriphase modulation were employed. Although implementation of this or any technique over long-range ionospheric paths necessitates compromises which reduce transmission efficiency, the FDPSK technique minimizes this reduction as it is capable of closely approaching the theoretical data capacity.

The performance of phase-shift keyed data transmission systems over HF radio circuits is dependent upon the ability to establish an accurate phase-coherent reference at the receiver. The ANDEFT frequency differential technique derives the phase reference required by coherent signalling by transmitting the PSK modulation as a difference in phase between two tones closely spaced in frequency. During the detection process, one of these tones supplies a real time phase reference for the other. The frequency-differential PSK demodulator is relatively unaffected by the time-varying absolute phase-shifts induced by the ionosphere because such absolute phase perturbations are highly correlated for closely-spaced frequencies.

The presence of multipath delay spreads ranging to several milliseconds produces intertone and intersymbol crosstalk in a multiple-tone modem which may result in errors during the recovery of the binary data. The ANDEFT/SC-320 modem employs an extended-length detection interval of 25 milliseconds to create a tolerance to large multipath delay spreads. An additional 1-2/3 millisecond guard time between successive symbols is used to achieve an immunity to small delay spreads and band-limiting effects.

The ANDEFT/SC-320 modem employs a segmented AGC system in which the 64 parallel orthogonal data channels in the voiceband are separated into eight independent groups of channels. In this way, deep frequency-selective fades accompanying normal multipath transmission conditions can be more favorably compensated to maintain the desired average signal level.

The ANDEFT/SC-320 employs a highly accurate synchronization system capable of determining the correct symbol framing initially and tracking subsequent multipath-induced symbol framing shifts in the presence of considerable noise and man-made interference (QRM). The coarse synchronization is accomplished by an electronically-separate coarse sync receiver which evaluates the baseband signal, continuously monitors the framing of the two transmitted reference tones, and provides a correctly framed time base for comparison with the main receiver time base. To achieve the precise symbol framing necessary when employing high-order phase modulation, the ANDEFT/SC-320 employs a novel phase-error analyzer and fine sync circuit which measures the perturbations of the received data to derive fast, accurate compensations and corrections.

The ANDEFT/SC-320 system has provision for dual signal source (reception) diversity operation to capitalize on available space, frequency, or polarization diversity facilities. In addition, the modem can be operated with dual (2400 and 1200 bps) or quadruple (600 bps) in-band frequency diversity to provide additional immunity to high-intensity natural and man-made interference.

Recent field tests indicated that propagation disturbances in general are not always the main factors ultimately limiting the equipment performance. Instead, QRM (co-channel interference) and high intensity noise disturbances (atmospherics) tend to introduce periods of relatively poor performance and thus substantially raise the average error rate for a given circuit. Due to the particular character of these types of interference, digital error correction coding appears to be the most promising method of combating these effects. Error correction coding, however, means that the transmitted bit rate is considerably higher than the original data rate and thus emphasizes the data capacity ability of the ANDEFT/SC-320 modulation-demodulation system.

Frequency-differential signalling is eminently suited to this application. As a result of its inherent multipath-protection features, the application of higher level phase modulation (such as eight-phase modulation) in combination with an appropriate time and frequency spread bit commutation scheme, will result in a performance level

under multipath conditions which is still considerably better than that presently experienced under interference conditions. The increase in data capacity so obtained may then be used for digital error-correction coding, resulting in significantly higher throughput data rates at acceptable error rate levels. Furthermore, such a system lends itself particularly well to a communications system designed to adapt the data rate to prevailing transmission conditions.

Signal Modulation

The function of the ANDEFT/SC-320 modulator (see block diagram, Figure 1) is to convert a serial binary data input into a frequency-differentially encoded multitone baseband signal which can be used directly by a conventional HF voice transmitter. The modulator consists of a differential-encoding circuit processing the binary input data, a bank of registers which receive and hold the encoded binary data for the duration of each 26-2/3 millisecond interval, a bank of 64 character selector gates which select the appropriate digitized sinusoidal tones in accordance with the stored encoded data, a set of eight band-limiting multiplier circuits each translating groups of eight tones to their correct frequency positions in the baseband spectrum, and a group adder combining the eight group outputs into one baseband signal to be fed to the transmitter. In addition, the modulator includes a timing and function generator to produce the necessary timing pulses and digital tones, two modulated reference tones, and a 600 bps converter.

The ANDEFT/SC-320 modem achieves true frequency-differential PSK signalling by employing progressive block coding and character selection. With this technique, each differentially-encoded two-bit block of binary data serves as the starting point or reference for encoding the succeeding two bits of input data. The differential encoding, performed in accordance with the truth table of Figure 2, renders the binary data into a form which may be utilized directly by the character selection circuits. The character selector gates permit one and only one of four digital tones present at the input to pass. The selection is controlled by the encoded data contained in the storage register in accordance with the associated transmitted phases and functions listed in Figure 3.

Signal Detection

ANDEFT Demodulator

The voice frequency input spectrum to the demodulator (see block diagram, Figure 4) is applied to a bank of group demultiplexers, one for each group. The output of each group demultiplexer, now at a common processing frequency, is filtered and applied to an AGC amplifier. The AGC amplifier output is applied to nine pairs of correlator inputs.

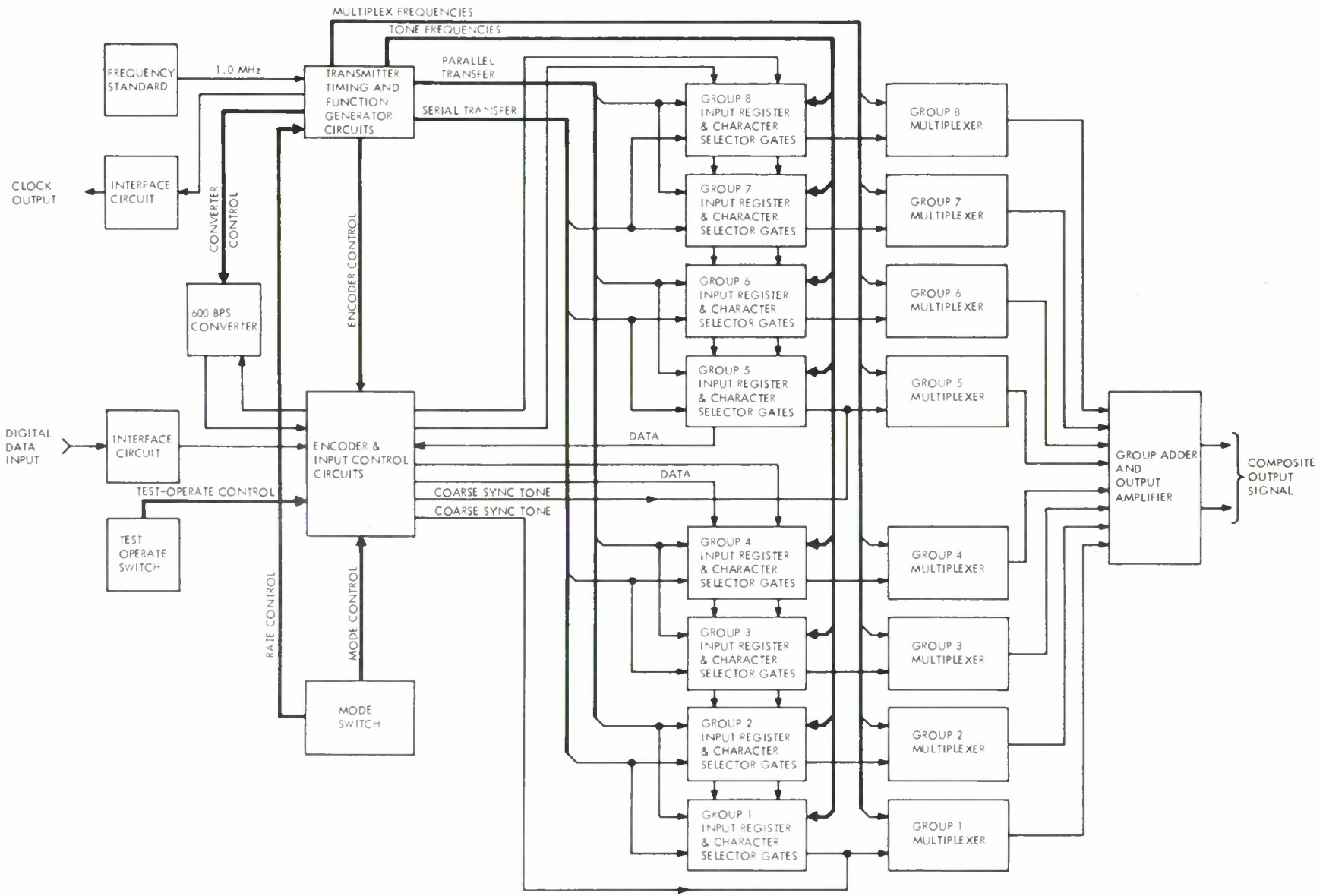

Figure 1. ANDEFT/SC-320 Modulator, Block Diagram

Four-Phase Operation		Previous ANDEFT Encoder Output			
		00	01	11	10
Present Data Input	00	00	01	11	10
	01	01	11	10	00
	11	11	10	00	01
	10	10	00	01	11

Two-Phase Operation		Previous ANDEFT Encoder Output	
		00	11
Present Data Input	00	00	11
	11	11	00

Figure 2. ANDEFT Differential Encoding Truth Tables

Four Phase Operation		
Differentially Encoded Data	Absolute Transmitted Phase	Transmitted Function
00	0°	+ Sine
01	$+ 90^{o}$	+ Cosine
11	$+180^{o}$	- Sine
10	$+270^{o}$	- Cosine

Two Phase Operation		
Differentially Encoded Data	Absolute Transmitted Phase	Transmitted Function
00	0°	+ Sine
11	$+180^{o}$	- Sine

Figure 3. ANDEFT Character Selection

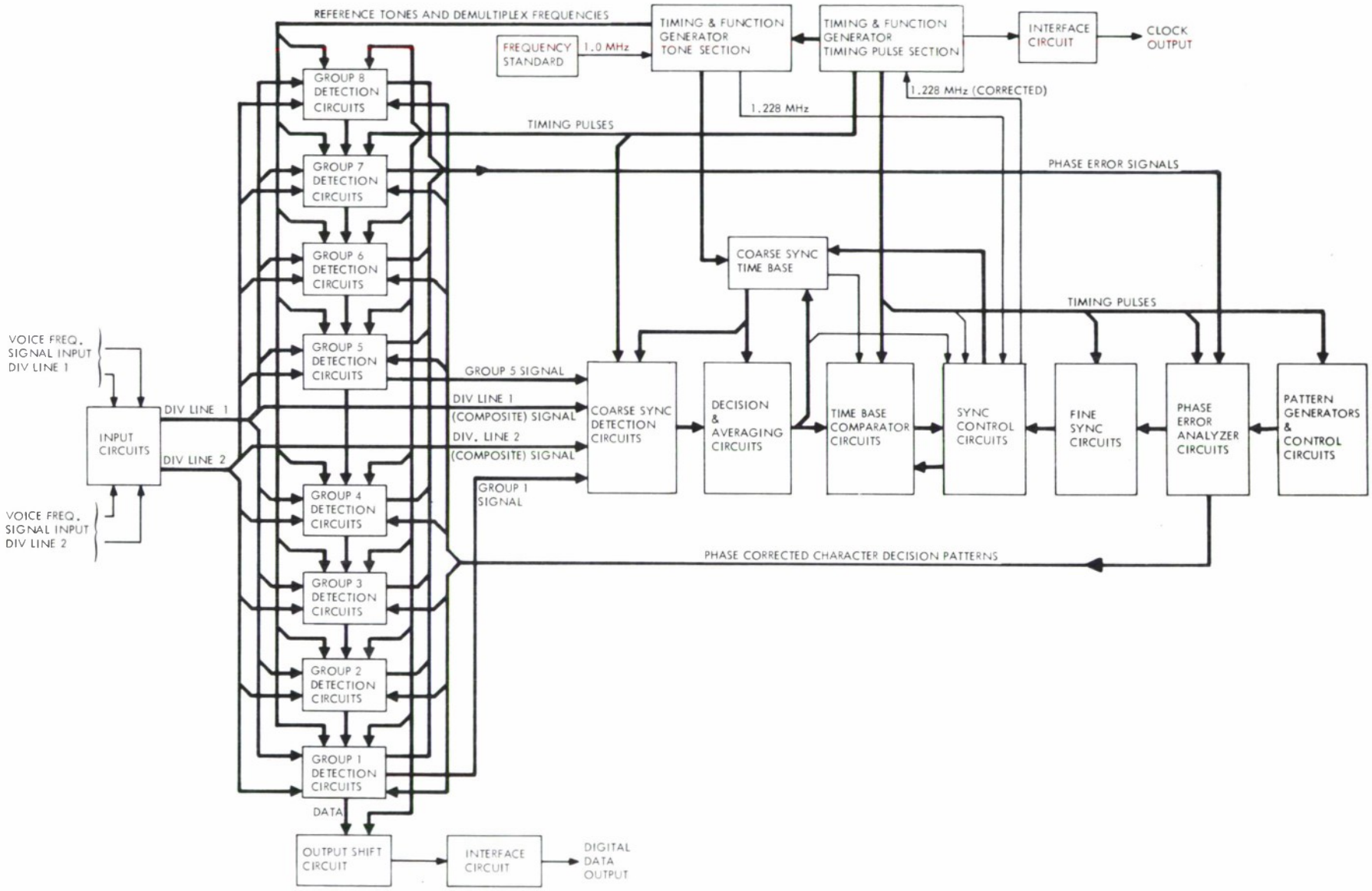

Figure 4. ANDEFT/SC-320 Demodulator Block Diagram

The key area in the demodulator is the frequency-differential phase demodulation technique. In brief, each signal tone is correlated with a corresponding (in frequency) locally-generated reference tone. The outputs of a pair of correlators (sine and cosine) completely define the phase of the signal tone with respect to the receiver time base. The frequency-differential phase angle between two signal tones may be determined by use of the standard trigonometric equalities.

$$\sin(\phi_1 - \phi_2) = \sin\phi_1 \cos\phi_2 - \cos\phi_1 \sin\phi_2, \text{ and} \tag{1}$$

$$\cos(\phi_1 - \phi_2) = \sin\phi_1 \sin\phi_2 + \cos\phi_1 \cos\phi_2. \tag{2}$$

A block diagram of the ANDEFT demodulation technique starting with the correlator inputs is shown in Figure 5. To implement this demodulation technique, the correlators are commutated at a standard processing frequency which combines the functions of DC to AC conversion and multiplexing in one step. The phase comparison and character decision is made after completion of the correlation detection interval.

Signal Detection Circuits

The composite group signal is applied in parallel to a bank of correlators. Three pairs corresponding to the $(n - 1)^{th}$, n^{th}, and $(n + 1)^{th}$ signal tones are shown in the block diagram of Figure 5. For this discussion only, the correlators for the nth and $(n + 1)^{th}$ tones will be considered.

Reference inputs to the correlators are derived from the local clock, and the reference frequencies correspond to the signal input frequencies, but their phase, of course, is not locked in any way to the received signal phase. At the end of the integration period, the outputs of the pair of correlators (1) and (2) in Figure 5 are

$$A_n \cos\phi_n \text{ and } A_n \sin\phi_n, \tag{3}$$

where A_n represents the relative amplitude of the nth signal tone, and ϕ_n represents the difference angle between the average phase of the nth signal tone and the phase of the local reference signal.

Similarly, the outputs of the correlator pair (3) and (4) are

$$A_{n+1} \cos\phi_{n+1} \text{ and } A_{n+1} \sin\phi_{n+1}. \tag{4}$$

These outputs are applied to four modulators (5), (6), (7), and (8), respectively. Modulators (5) and (6) are driven by signals $\sin\omega_p t$ and $\cos\omega_p t$ where ω_p is the processing frequency (9.6 kHz) which is derived from the local clock. The outputs of modulators (5) and (6) are summed in linear adder (9), and the output is

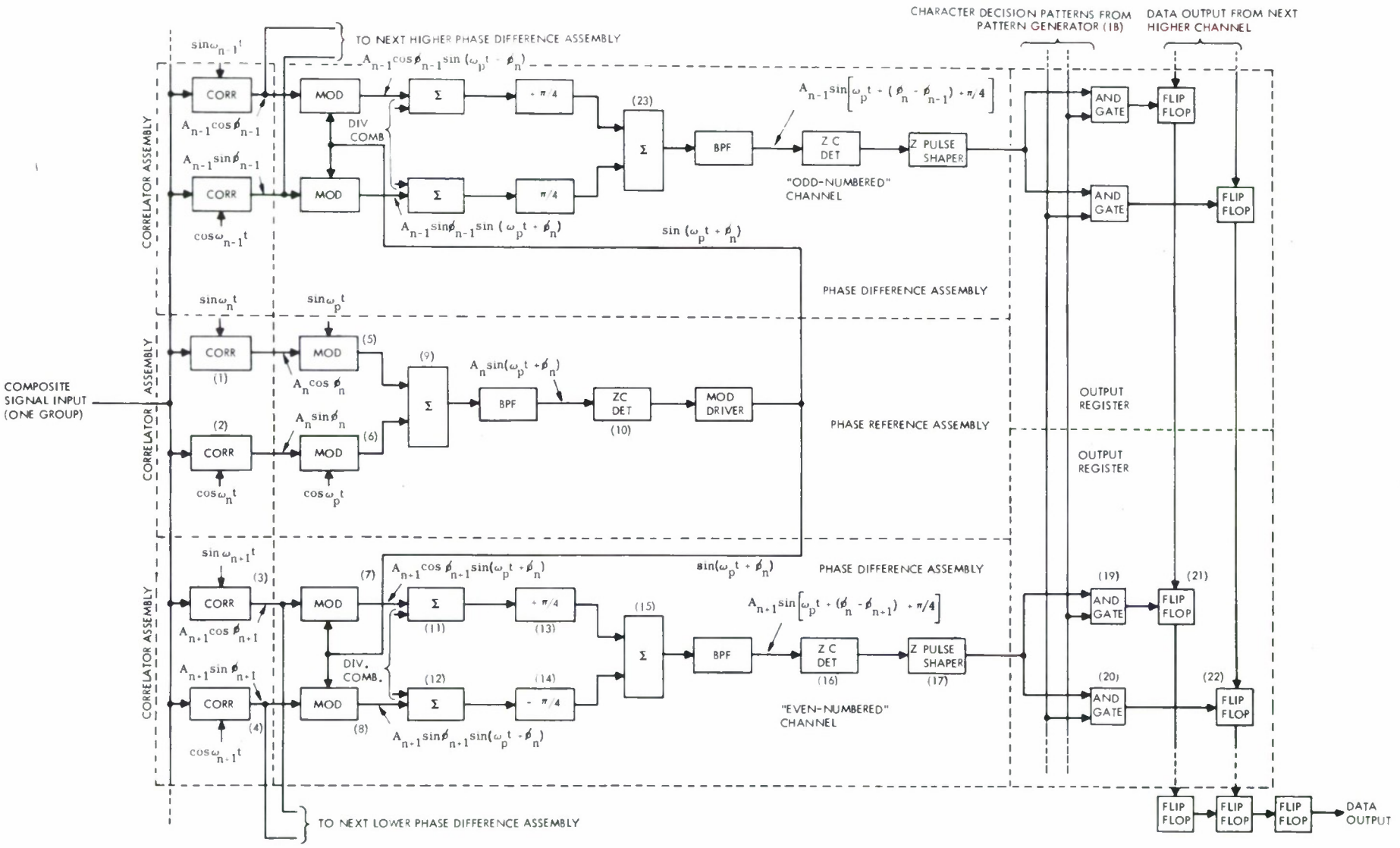

Figure 5. Correlation Detection and Decision Circuits

$$A_n \cos \phi_n \sin \omega_p t + A_n \sin \phi_n \cos \omega_p t = A_n \sin (\omega_p t + \phi_n). \qquad (5)$$

In effect, the amplitude and phase (relative to the receiver clock) of the nth signal tone has been transferred to the locally generated processing frequency f_p.

The output of adder (9) is processed by a zero crossing detector which removes the amplitude component A_n, but retains the phase information ϕ_n. This signal is used to drive modulators (7) and (8). These outputs are

$$A_{n+1} \cos \phi_{n+1} \sin (\omega_p t + \phi_n) \text{ and,} \qquad (6)$$

$$A_{n+1} \sin \phi_{n+1} \sin (\omega_p t + \phi_n), \text{ respectively.} \qquad (7)$$

The signal is combined with the corresponding channel of the other diversity in adders (11) and (12). A positive phase shift of $\pi/4$ is applied to the output of (11), and a negative phase shift of $\pi/4$ is applied to the output of (12). The outputs of the phase shifting networks (13) and (14) are then summed in linear adder (15). The output of this adder is

$$A_{n+1} \cos \phi_{n+1} \sin (\omega_p t + \phi_n + \pi/4) + A_{n+1} \sin \phi_{n+1} \sin (\omega_p t + \phi_n - \pi/4 =$$

$$A_{n+1} \sin \left[\omega_p t + (\phi_n - \phi_{n+1}) + \pi/4 \right] \qquad (8)$$

The phase of the signal at this point is, therefore, independent of the absolute phases of the received signal tones, and it represents only the differential phase modulation of the nth and $(n + 1)^{th}$ tone pair. This channel configuration is denoted an "even-numbered" channel.

In the same manner, the differential phase information between the nth and $(n - 1)^{th}$ tone pair is derived (see Figure 5). This channel configuration is denoted an "odd-numbered" channel.

The output of adder (23) is

$$A_{n-1} \sin \left[\omega_p t + (\phi_n - \phi_{n-1}) + \pi/4 \right] \qquad (9)$$

A block diagram of a complete group is shown in Figure 6 where the reference designations A, B, C, and D corresponding to the correlator, phase reference, phase difference, and output register "assemblies" of Figure 5 have been shown. It will be noted that the first and last tones of the group are used only once in the detection process. This method makes each group in the demodulator completely self-sufficient

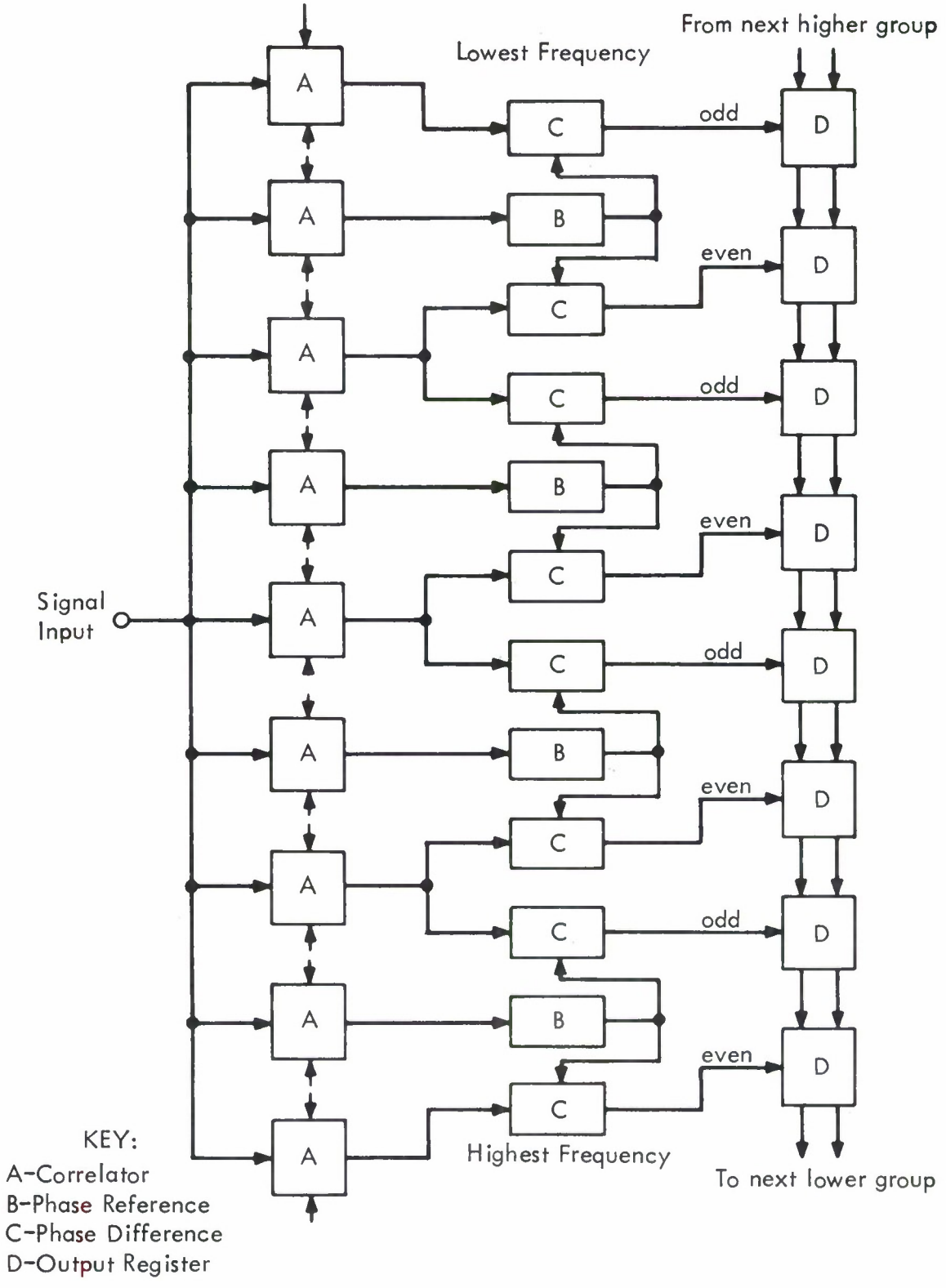

Figure 6. Group Demodulator

and eliminates the need for phase alignment or control in the group demultiplexing process. In addition, it reduces the number of circuits required in the demodulator without impairing technical performance.

Character Decision Process

The output of adder (15) of Figure 5 is processed by a zero crossing detector (16) and pulse shaper (17) so that the output of the pulse shaper is a train of narrow pulses with repetition frequency f_p, and the time-position of these pulses is determined by the positive going zero crossing of the adder output signal. Thus, for a $\Delta\phi = (\phi_n - \phi_{n+1}) = 0$, the "Z" pulses will occur in a relative time position corresponding to the $\pi/4$ point of the local reference frequency f_p. The "Z" pulses serve to momentarily connect a pattern generator (18), which is common for the entire demodulator, to the appropriate stages of the output data register (21) and (22) by means of "and" gates (19) and (20). The use of "and" gates has the effect that only the "ones" which are present in the parallel output of the pattern generator when the "Z" pulse occurs are transferred to the output register.

The decision process is accomplished as follows. At the end of the receiver integration period, all the data from the previous character have been shifted out of the output register so that this register now contains all "zeros". A very short time after the completion of the integration period, a gating pulse from the receiver timing generator causes the pattern generator to cycle through one (and only one) complete sequence in synchronism with the local reference frequency f_p. As the duration of this cycle is equal to the period of the pulse train from pulse generator (17), one of "Z" pulses will occur within this cycle, and the pattern corresponding to the relative position of the "Z" pulse with respect to f_p will be transferred to the output data register. The timing diagram shown in Figure 7 depicts the pattern generator cycle and the relative position of the "Z" pulse for the case of four-phase modulation. From the diagram it can be seen that this method automatically provides a maximum likelihood decision, as any position of the "Z" pulse between successive dotted lines will be registered as the pattern corresponding to the center of the interval.

Phase Error Correction

The block diagram shown in Figure 8 shows the method for obtaining phase-error correction information. Z_1 through Z_8 are the eight "Z" pulses whose time position with respect to the local reference frequency correspond to the detected differential phase angles of the eight channels in a signal group. In order to reduce the probability of time coincidence, the eight "Z" pulses are split in two groups and combined on two lines by means of "or" gates. One line carries the odd, and the other line carries the even numbered "Z" pulses. The two sets of "Z" pulses are compared with the appropriate phase reference pattern. This is accomplished by two "and" gates which have their outputs connected to count-up and count-down inputs of a reversible counter.

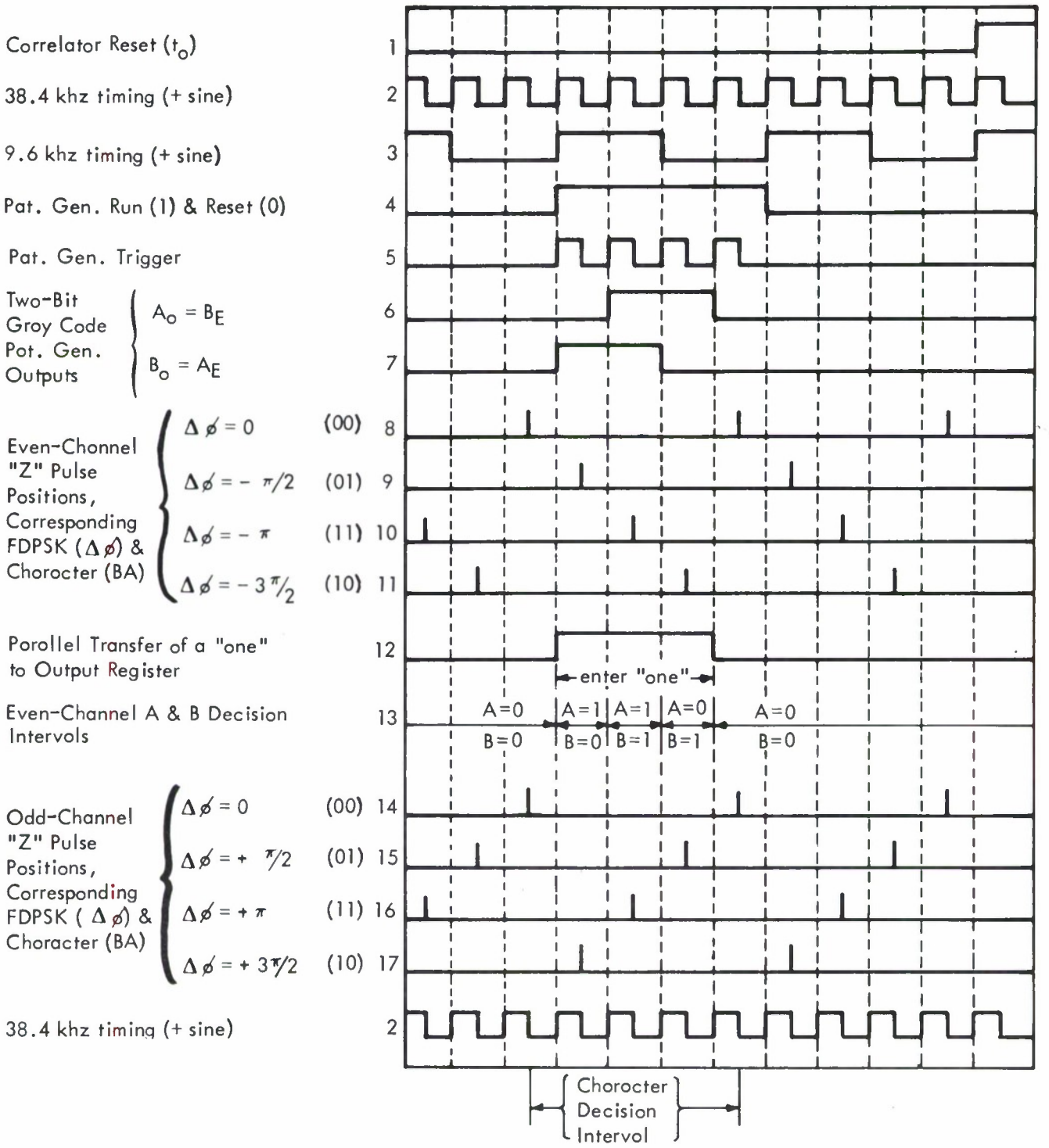

Figure 7. Four-Phase Decision Process

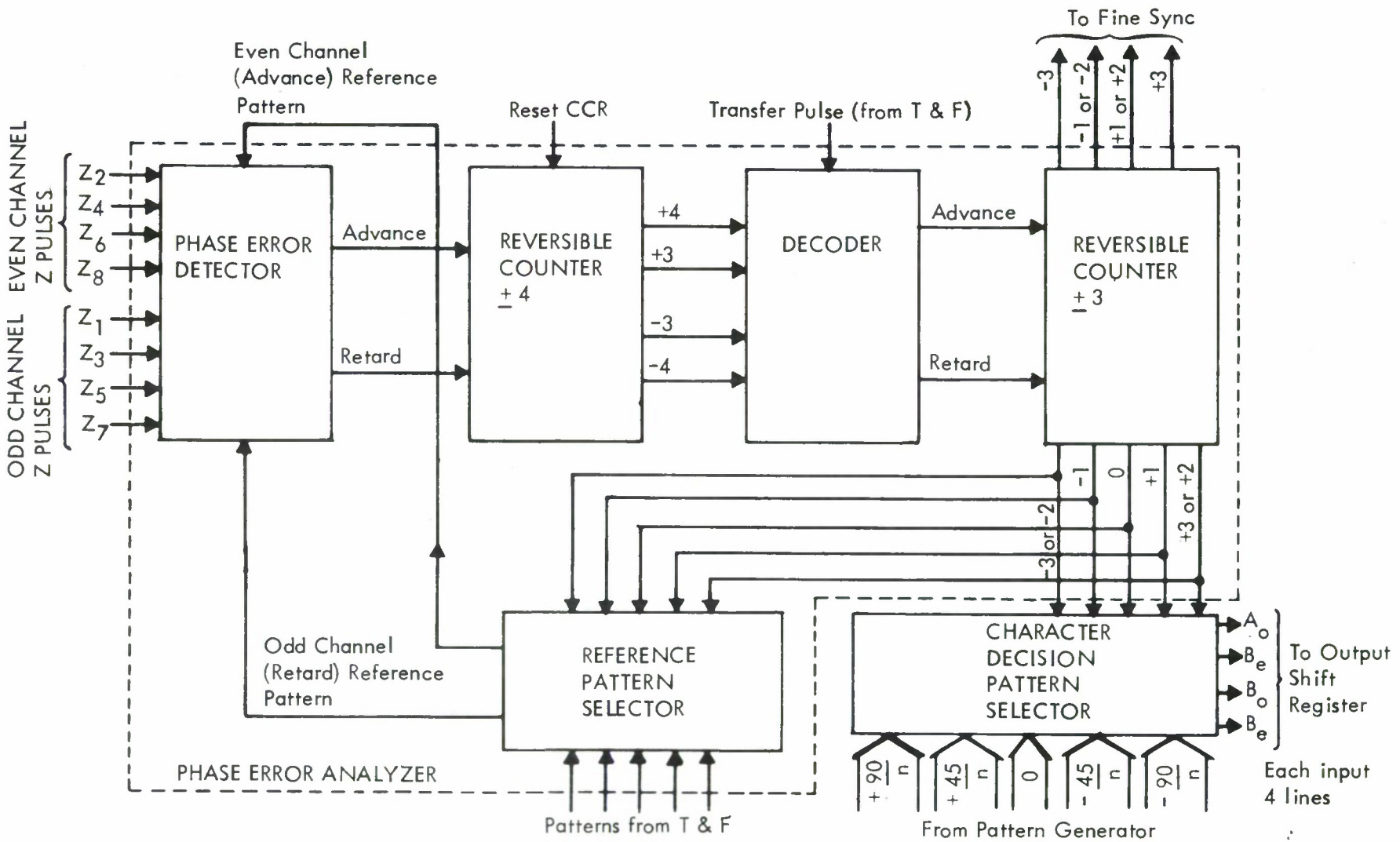

Figure 8. Phase Error Analyzer and Character Decision Pattern Selector

The phase reference patterns consist of a sequence of (either two or four) pulses (for two or four-phase modulation, respectively), locked to the main receiver time base, so positioned that they are coincident with "advanced" even channel "Z" pulses and with "retarded" odd channel "Z" pulses. (The theoretical positions of the "Z" pulses for a perfect unperturbed channel is depicted in Figure 7.)

A time-lag in the occurrence of any of the "odd-channel" "Z" pulses will result in a "count-down" input to the reversible counter, while a lag in the occurrence of any of the "even-channel" "Z" pulses will result in a "count-up" input to this counter. Thus, phase advance information is obtained from even-channel and retard information from odd-channel pulses. This simple scheme avoids duplication of circuitry, i.e., advance and retard information from both even and odd channels is not necessary.

At the end of each phase-error detection period, the state of the reversible counter indicates how many more actual "Z" pulses were counted as being shifted in one direction from the theoretical position as compared to the other direction, and thus indicates the direction in which the receiver time base should be corrected in order to provide a balance. This counter serves as a temporary storage that is reset at the end of each symbol interval. Whenever the absolute count of this counter exceeds two at the end of a phase-error detection period, a "count-up" (for a count > 2) or "count-down" (for a count < -2) input is given to a second reversible counter which acts as a storage device. This digital integration prevents phase decisions being made on single phase errors in a group. The storage reversible counter provides outputs to the fine synchronizing circuit, the reference pattern selector circuits, and the character decision pattern selector circuits.

Phase error correction will compensate for any systematic phase errors in a group. Instead of generating one pair of advance-retard reference patterns and one pair of character-decision patterns, five of each type of pattern are generated in the timing and function generator. One of each type is centered, two are leading (with respect to the reference frequency) by amounts of τ and 2τ, and two are lagging by the same amount, respectively.

The output of the storage reversible counter of the phase-error analyzer circuit is applied to the phase reference pattern selector. When the storage register output is zero, the normal patterns are selected by these matrices and fed to the appropriate inputs. However, when a systematic phase error exists in a group, the storage register will first be stepped to the +1 or -1 position (depending on the sign of the phase error) which in turn will cause the reference pattern selector to select the $+\tau$ (or $-\tau$) pattern. If this shift is sufficient to correct for the original phase error, then the storage counter will remain in the +1 (or -1) position, as the probability of the first reversible counter reaching a count > 2 will now be very small. If the phase error is substantially greater, the storage counter will be stepped to the ± 2 (or ± 3) position and the gating matrices in the pattern selector will then select the $+2\tau$ (or -2τ) patterns.

Note that, regardless of which of the reference (and corresponding inverted reference patterns) are used, the storage counter output will always indicate the desired direction of phase error correction for the particular group it represents. Any change of sufficient magnitude in the systematic phase error (such as may occur when a sync correction is made) will result in a change in the storage counter output and thus ensure selection of the corresponding new patterns.

Phase error compensation during the character decision interval is achieved by selecting the appropriately advanced, normal, or retarded character decision patterns based on the results of the immediately preceding phase-error detection interval. Hence, a measurement of any phase-error present is made and a compensating character decision pattern is selected for each symbol interval prior to the actual recovery of the binary data from the "Z" pulse positions.

Figure 9 shows the way in which logical decisions are made for advance or retard phase steps depending on the count stored. The circuit is arranged to make only one step at a time; this allows the circuit to provide a degree of "smoothing" to impulse distortion, i.e., if the phase information from the phase error detector indicates that the reference pattern from the selector should change from fully retarded to fully advanced, this would be accomplished by stepping through the three intervening patterns sequentially, providing phase information continued to indicate a change to fully advanced. The character decision pattern selector circuit operates in exactly the same manner as the reference pattern selector.

Phase error compensation is obtained when the appropriately advanced or retarded character decision pattern is selected to achieve the best group average position with respect to the "Z" pulses. The procedure fulfills the requirements of a decision directed measurement scheme.

Frequency and Time Assignments

The ANDEFT/SC-320 modem employs 64 intelligence tones plus two reference tones to form 64 channels each carrying up to 75 bps with quadriphase PSK, an orthogonal symbol length of 25 milliseconds, and a tone separation of 40 Hz. The baseband frequencies of the 64 intelligence tones (tone number 1 through 8 for each of 8 groups) and the two reference tones (tones numbered zero in groups 1 and 5) are listed in Figure 10 as they appear at the output of the modulator. The nomenclature used to identify each of the 66 transmitted tones and the intelligence channels is presented in this figure.

The ANDEFT signal spectrum is divided into groups to enable the use of segmented AGC in the demodulator, to limit the dynamic range requirements of the correlators, and to facilitate signal coding and decoding operations. However, each tone is modulated with phase information relative to the phase of the preceding adjacent tone. In the modulator, the adjacent groups are phase aligned in order to prevent a discontinuity between the last tone of one group and the first

Total Count	Decision	Increment
+3, +2	Medium Step Advanee	$+90^{o}/n$
+1	Small Step Advance	$+45^{o}/n$
0	Normal	0
-1	Small Step Retard	$-45^{o}/n$
-3, -2	Medium Step Retard	$-90^{o}/n$

n = number of phases in modulation

Figure 9. Phase Error Compensation

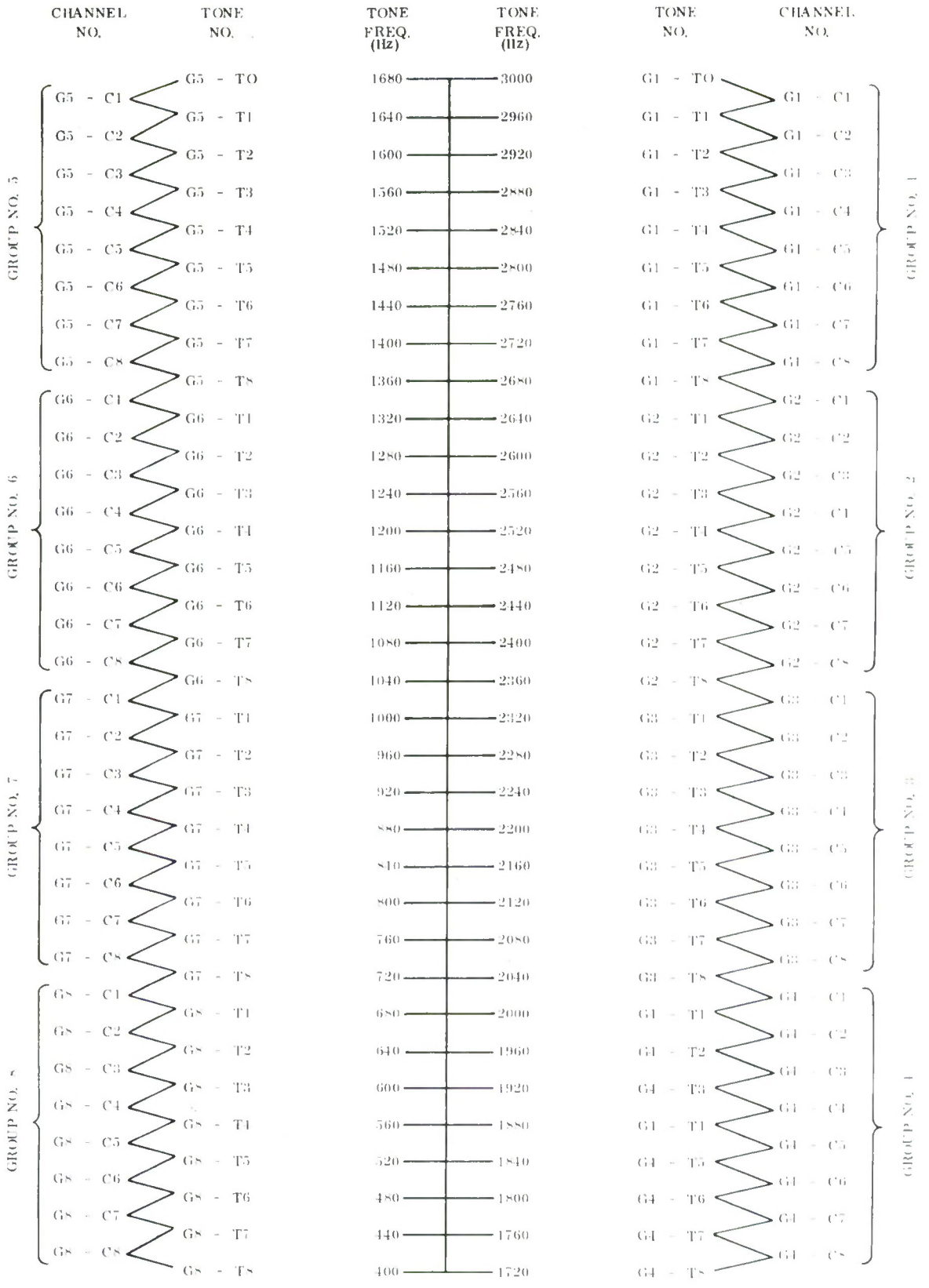

Figure 10. Tone and Channel Designations

tone of the next group. This makes each group in the demodulator completely self-sufficient and eliminates the need for phase alignment or control in the group demultiplexing process.

The ANDEFT baseband spectrum including significant sidebands ranges from 362.5 to 3018.75 Hz. The baseband spectrum displaying the group structure and reference tones is shown in Figure 11. The frequencies at which each of the 8 groups of tones is modulated (the character selections made) and detected (the correlator reference frequencies) are listed in Figure 12 with their respective tone number 1 through 8. Tone number zero is the reference tone to be added to groups 1 and 5. The phase difference, phase reference, odd channel, and even channel designations refer to the implementation of the demodulator detection circuitry. The multiplex/demultiplex frequencies used to translate each of the eight tone groups from their common modulation/detection frequency band to/from their baseband locations are listed in Figure 13.

The basic symbol interval of the modem is divided as shown in Figure 14. The interval is 26-2/3 milliseconds long with guard times of 5/6 milliseconds at the front and rear. The intervening 25 milliseconds, known as the detection interval, is used by the integrator in the correlation detection process. During the rear guard time, phase error detection, character decision, and fine synchronization decision are made.

The rear guard time has five main sub-periods, labeled (1) to (5), the first of these being 403* microseconds long (1), followed by three periods of 104* microseconds during (2, 3, and 4), and a final period of 117* microseconds (5). Period (1) is provided to allow the filters shown in Figure 5 to reach a steady state. Period (2) is the phase error decision period, during which "Z" pulses from the zero-crossing detector are presented to the phase-error detector, Figure 8. Period (4) of the rear guard time is used by the character decision circuit to decode the "Z" pulses. The decoded pulses are stored in a register and then converted into a serial output data stream as shown in Figure 5. The final period (5) is of 117* microseconds duration, made up of a basic 104* microsecond period plus an additional 13 microseconds. This extra 13* microseconds represents a $\pi/4$ phase delay in the preceding circuitry (shown in Figure 5) at a processing tone frequency, 9.6 kHz. The strobing of the eight group phase analyzers occurs during the front guard period.

Fine Sync

The function of the fine sync circuits is to determine desirable highly-precise corrections to the receiver main time base once the proper approximate framing with respect to the incoming signal has been achieved via the coarse sync circuits. The fine sync circuit utilizes the medium and small advance-retard indications from each of the eight group phase-error analyzers to determine the best all-group average correction of the receiver main time base.

*Fractional values omitted here. See Figure 14.

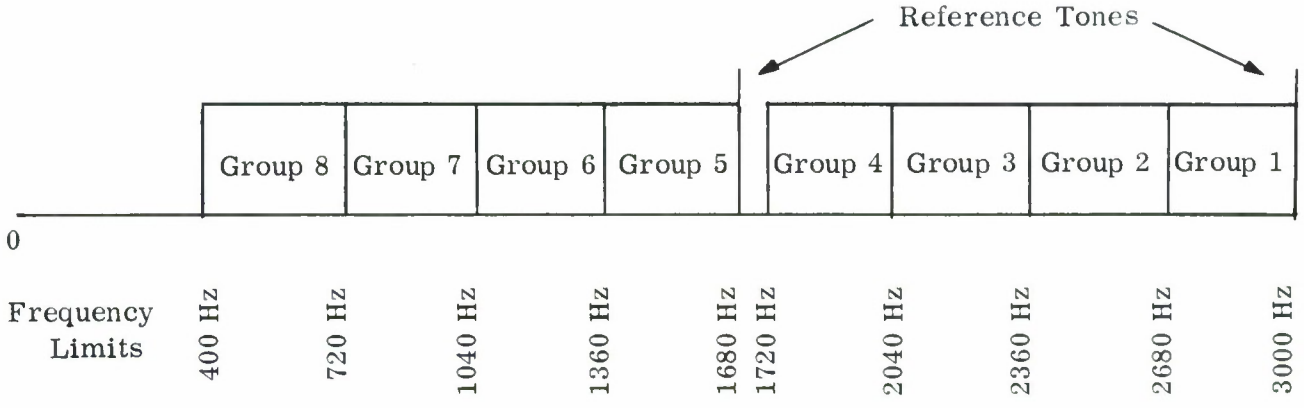

Figure 11. Baseband Spectrum

Tone Number	Signal Processing Circuit Type	Modulation-Detection Frequency (Hz)	Channel Designation for Group X	Channel and Z Pulse Type
0	Phase Difference	3640	GX-C1	Odd
1	Phase Reference	3680	GX-C2	Even
2	Phase Difference	3720	GX-C3	Odd
3	Phase Reference	3760	GX-C4	Even
4	Phase Difference	3800	GX-C5	Odd
5	Phase Reference	3840	GX-C6	Even
6	Phase Difference	3880	GX-C7	Odd
7	Phase Reference	3920	GX-C8	Even
8	Phase Difference	3960		

Figure 12. Group Channel and Tone Designations

Group Number	Multiplex-Demultiplex Injection Frequencies (Hz)
1	6640
2	6320
3	6000
4	5680
5	5320
6	5000
7	4680
8	4360

Figure 13. Multiplex-Demultiplex Frequencies

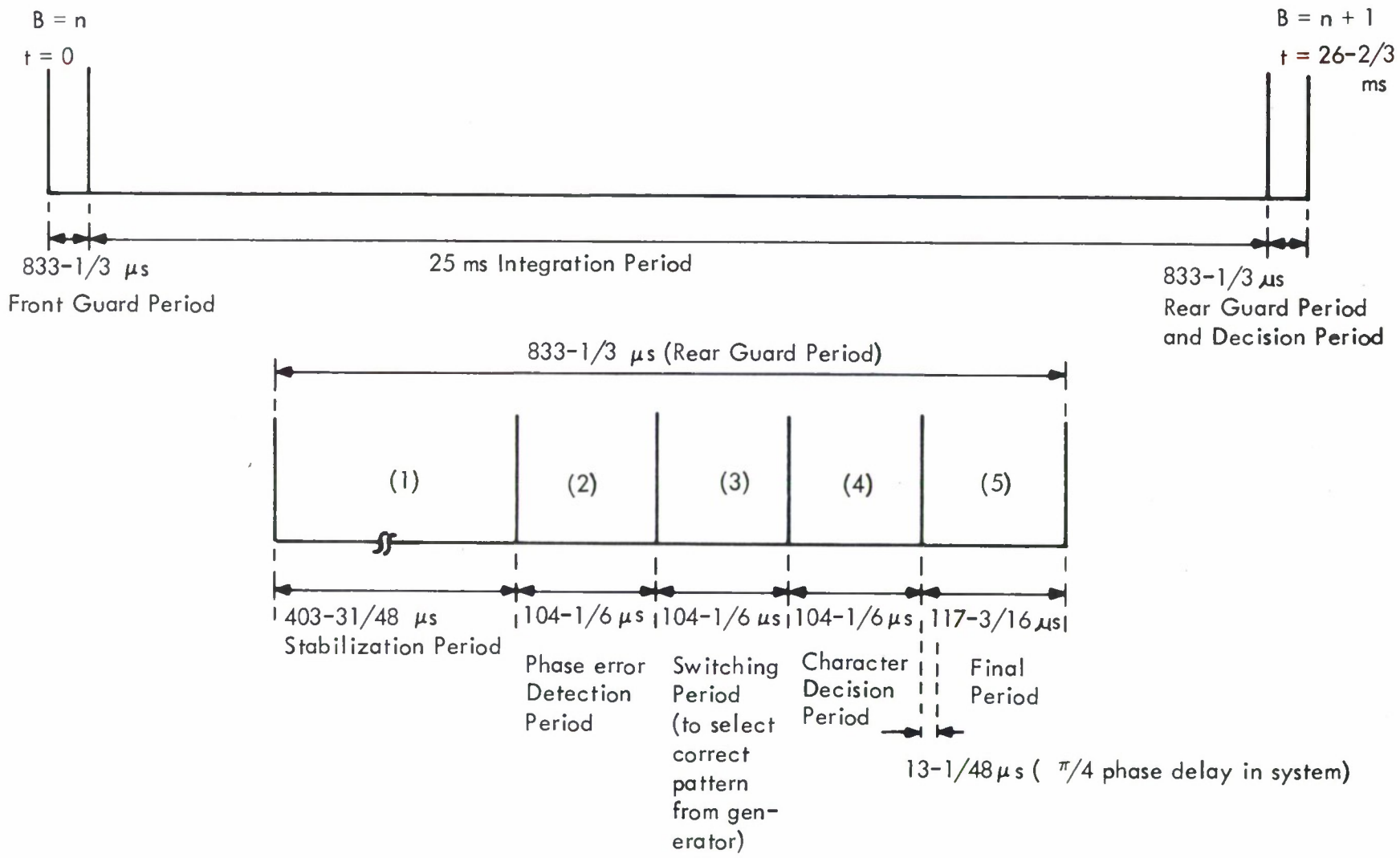

Figure 14. Symbol Period Time Allocation

The fine sync sequentially strobes the eight phase error analyzers obtaining one medium or small advance or retard indication from each. The first three small correction indications in both directions are neglected. Any additional small corrections and all medium corrections are counted to arrive at the desirable time base correction. As shown in Figure 15, the slow correction rate is 0.975 milliseconds/second while the medium rate is 1.96 milliseconds/second. If a faster correction rate is required, the fine sync will slip out of its ±3 1/8 millisecond quadriphase misframing correction range and will be overridden by the coarse synchronization circuits.

Operation of the fine sync is inhibited whenever one or more of the following conditions exist:

1. Low signal level or low signal-to-noise ratio on both diversity lines.

2. Sync mode selector switch is set to inhibit the fine sync.

3. Coarse sync correction enabled indicating that the fine sync is probably out of operating range.

Coarse Sync

As indicated in the preceding section, the ANDEFT/SC-320 fine sync system is designed for fast, accurate correction of the relatively small framing errors encountered under normal operating conditions. The fine sync system is, however, incapable of correcting large framing errors between the main receiver time base and the received signal. (Abnormally high error rates will occur if large framing errors are not corrected.) The ANDEFT/SC-320 coarse sync system is a slower acting, less accurate system designed specifically for correction of large framing errors. Although these errors most often appear prior to the initial alignment of the main receiver time base, large framing errors will occasionally occur after sync acquisition as a result of abrupt changes in ionospheric radio propagation contions or as a result of a complete loss of signal for a long period of time.

Synchronizing tones are transmitted in groups 1 and 5 at a power level 6 db above that of the intelligence tones. Both sync tones are phase reversal modulated at a 9.375 Hz rate. The received signal from both diversity lines is fed to the coarse sync detection circuits from the group 1 and 5 correlator drive amplifiers. A functional block diagram of the coarse sync system and associated circuits is shown in Figure 16. Correlator reference tones used in the detection process are synthesized in the tone section of the receiver timing and function generator (main

*Fractional values omitted here. See Figure 14.

Fine Sync Counter State	Decision	Correction Rate
+ 3	Medium Advance	+1.96 ms/second (1 part in 2^9)
+ 2, 1	Slow Advance	+0.975 ms/second (1 part in 2^{10})
0	Stationary	zero
- 2, 1	Slow Retard	-0.975 ms/second (1 part in 2^{10})
- 3	Medium Retard	-1.96 ms/second (1 part in 2^9)

Figure 15. Fine Sync Correction Rates

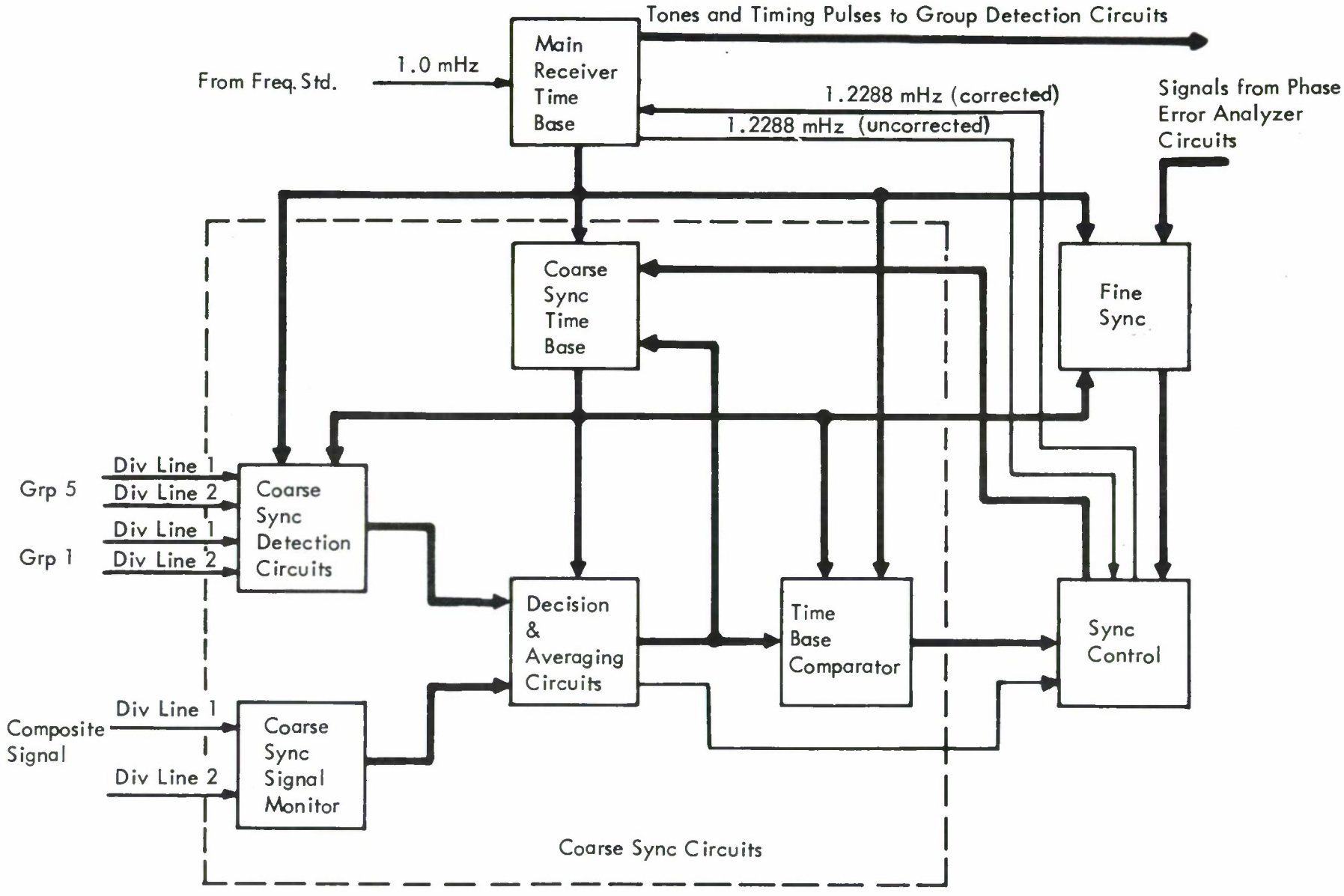

Figure 16. Coarse Sync System

receiver time base). The "00" and "01" correlator reference patterns shown in Figure 17 are generated by gating the reference tones with timing patterns ("B" and "C" in Figure 17) derived from the coarse sync time base.

When the coarse sync time base is correctly aligned with the received signal, the "01" correlator reference pattern is highly correlated with the coarse sync input signal (see Figure 17) and the "00" pattern is orthogonal with the input signal. Misaligning the coarse sync time base decreases the correlation between the "01" pattern and the input signal while increasing the correlation between the "00" pattern and the input signal. The ratio of the "01" to "00" cross correlation coefficients is, therefore, useful in identifying a correctly framed ANDEFT sync tone. An unacceptable ratio between the cross correlation coefficients indicates either an incorrectly framed sync tone or an unusable signal, e.g., noise, QRM, etc.

Because the absolute phase of the sync tone is unknown, it is necessary to cross correlate the input signal with both sine and cosine reference patterns. In the absence of extraneous signals, the magnitude of the vector sum of the sine and cosine correlator outputs is then proportional to the desired cross correlation coefficient and is independent of the absolute phase of the sync tone.

The angle of the "01" vector represents the phase difference between the received sync tone and the local reference. When the time base of the received signal is lagging the coarse sync time base, the "00" vector has the same angle as the "01" vector. However, when the received signal leads the coarse sync time base, the "00" vector is 180 degrees out of phase with the "01" vector. The phase relationship between the two vectors is, therefore, useful in determining whether advance or retard corrections are required to improve the alignment of the coarse sync time base.

The magnitude and angle of the vector ratio are quantitized and processed digitally by the coarse sync decision and averaging circuits. If it is determined that the correlation coefficient ratio is unacceptable (based on the magnitude of the vector ratio), the coarse sync system searches for an acceptable condition by advancing or retarding (based on the angle of the vector ratio) the coarse sync time base. This takes place without altering the alignment of the main receiver time base. Coarse sync time base corrections are normally made in increments of ± 5/6 milliseconds. However, when it is apparent that a gross framing error exists, a one step retard correction of 13-1/3 milliseconds is applied. This allows the coarse sync time base to move rapidly out of a region in which more precise time base adjustments are unnecessary.

When an acceptable correlation coefficient ratio is achieved (for both sync tones), the distribution of coarse sync advance and retard corrections is examined to determine whether or not the coarse sync time base has been aligned within the resolution of the system. Once the framing of the coarse sync time base has been validated (or on command from the manual "frame" switch) the main receiver time base is aligned with the coarse sync time base. Corrections are made to the main time base by the sync control circuit at a rate of 1 part in 2^7. The corrections continue until the time

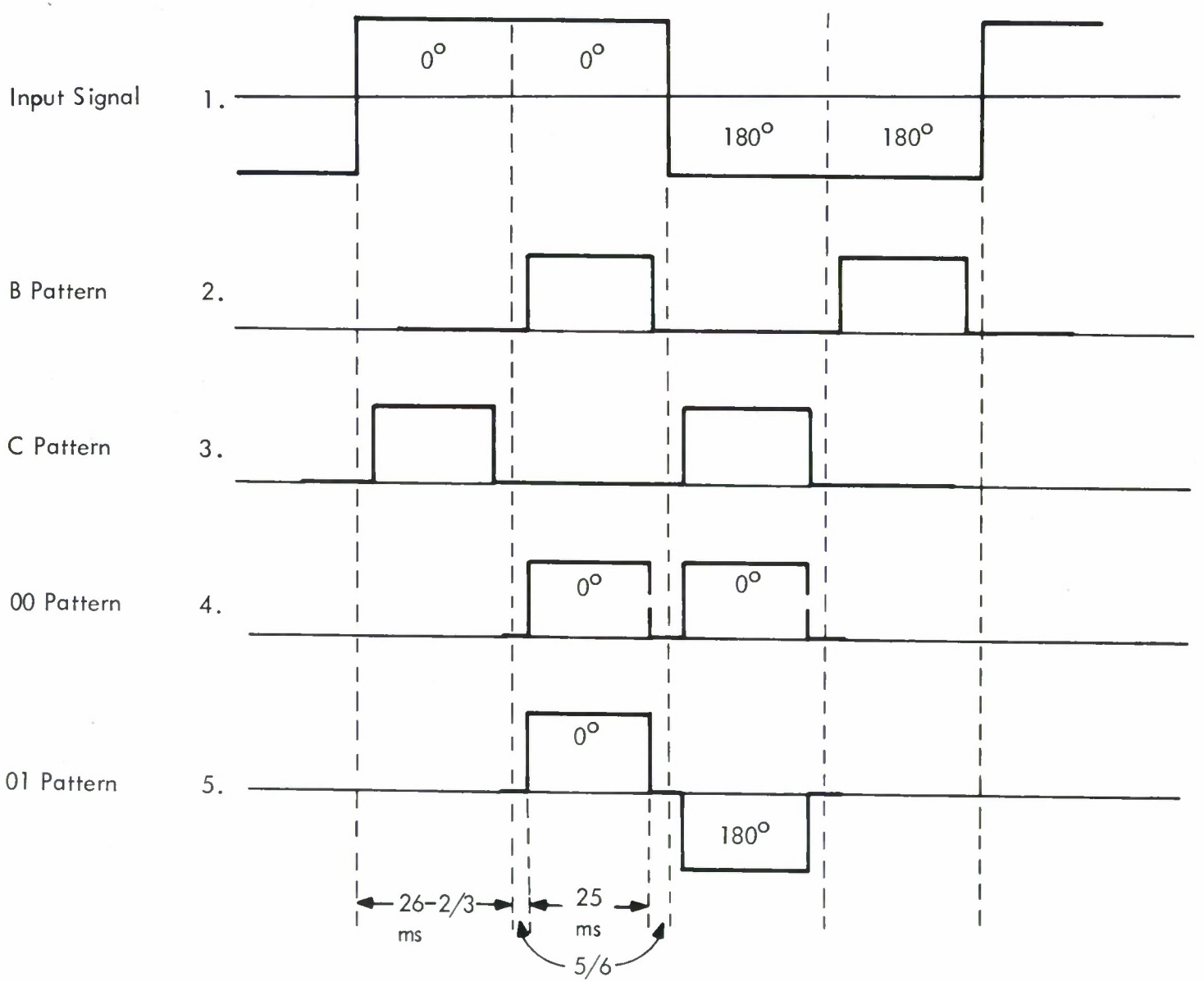

Figure 17. Coarse Sync Correlation Patterns

base comparator indicates the two time bases are aligned. This is done by comparing timing patterns from the coarse sync time base and main receiver time base. Subsequent corrections to the main receiver time base are initiated only if the difference between the two time bases exceeds a predetermined threshold (this threshold is selected by the sync range switch on the basis of channel conditions and operating mode). This facility prevents the coarse sync from realigning the main time base unless the alignment error is large enough to indicate that the main receiver time base is outside the normal operating range of the fine sync system.

The coarse sync signal level monitor compares the level of the composite signal on each diversity line with a fixed reference level. If the signal level should fall below this threshold on either diversity line, the coarse sync information from that line is discarded. If the signal level on both diversity lines is consistently below the threshold, all main receiver time base corrections (from both coarse and fine sync systems) are inhibited. This prevents the modem from driving itself out of sync in periods during which signal has been lost.

Rate Changing

The ANDEFT/SC-320 has five operating modes and four data rates shown in Figure 18. The 4800 bps rate, mode E in Figure 18,employs four-phase modulation without in-band frequency diversity. The 2400 bps rate is available in either of two modes,C or D. Mode C uses four-phase modulation and dual in-band frequency diversity in which groups separated by half the voice band are paralleled. Mode D uses two-phase modulation (phase reversal) without in-band frequency diversity. Mode B corresponds to the 1200 bps rate and is achieved with phase reversal modulation and dual in-band frequency diversity. The 600 bps rate, mode A, uses phase reversal modulation and quadruple in-band frequency diversity in which groups 1, 3, 5, and 7 are paralleled (odd numbered groups) and groups 2, 4, 6, and 8 are paralleled (even numbered groups). The modes are designated 600/2Ø, 1200/2Ø, 2400/4Ø, 2400/2Ø and 4800/4Ø for A, B, C, D, and E in Figure 18.

Modulator

The modulator employs a single multi-pole five-position switch to effect mode changes. The basic function of this switch is shown in Figure 19, a basic diagram of the modulator input circuits.

In modes B, C, D, and E the incoming data is fed directly to the encoder for processing. In modes D and E the data from the encoder is shifted into the input registers of group 8 through group 1, sequentially. In modes B and C the data from the encoder is shifted into the input registers of group 8 through group 5 and group 4 through group 1, simultaneously. The latter two modes enable dual in-band frequency diversity operation.

Mode Designation	A	B	C	D	E	
Throughput Rate	600	1200	2400	2400	4800	
Phase Modulation	2	2	4	2	4	
Frequency Diversity	4	2	2	1	1	
Reception Diversity	2	2	2	2	2	
Serial Shift (SST1)*	600	-	-	-	-	Modulator
Serial Shift (SST2)*	1200	-	-	-	-	
Serial Shift (SST3)*	2400	2400	2400	4800	4800	
Parallel Transfer (PTT1)*	37 1/2	37 1/2	37 1/2	37 1/2	37 1/2	
Parallel Transfer (PTT2)*	1200	1200	1200	2400	2400	
Serial Shift	600	1200	1200	2400	2400	Demodulator
Parallel Transfer	600	1200	1200	2400	2400	
Output Shift	1200	2400	2400	4800	4800	
Character Decision Patterns	2 phase	2 phase	4 phase	2 phase	4 phase	
Phase Reference Pattern	2 phase	2 phase	4 phase	2 phase	4 phase	
Register Input Inhibited	Groups 2,4,6,8	Groups 4, 8	Groups 4, 8	Group 8	Group 8	
Frequency Diversity Jumpers	Groups 1-3-5-7 2-4-6-8	Groups 1-5,3-7 2-6, 4-8	Groups 1-5,3-7 2-6,4-8	None	None	

Note: All rates are bits per second; Shift and transfer pulses given in pulses per second.

* See Figure 19.

Figure 18. Operating Modes and Timing

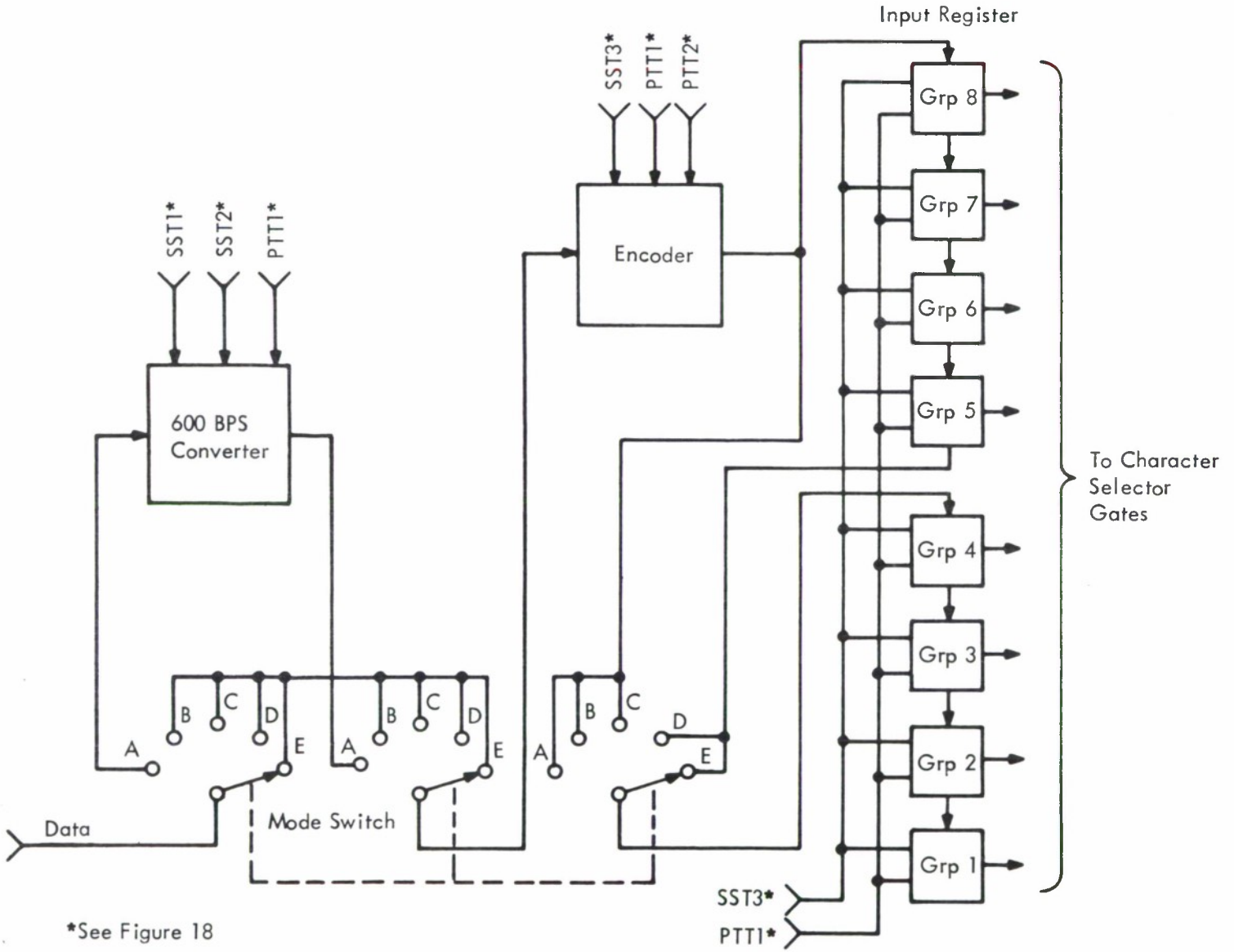

Figure 19. Modulator Mode Switching

In mode A, the 600 bps converter processes the incoming data. The data is shifted into the converter at a 600 bps rate; the data is recycled in the converter and shifted out at a 1200 bps rate to the encoder. This operation enables the quadruple in-band frequency diversity mode for the 600 bps rate.

Demodulator

The demodulator employs a single multi-pole five-position switch to effect mode changes. In addition to selecting the proper shift pulse rates for each mode, the switch inhibits the output register as shown in the table of Figure 18 and the block diagram of Figure 20.

In order to effect dual and quadruple in-band frequency diversity operation at the demodulator, the appropriate tones are combined at the input of the bandpass filter of each phase difference assembly. Shorting plugs and jumper cables are then used to effect the in-band frequency diversity modes A, B, and C. Mechanical pairing of the groups as shown in Figure 20 simplifies the interconnection. In the dual in-band frequency diversity mode (B and C) the groups are combined as follows: 8 and 4, 6 and 2, 7 and 3, 5 and 1. In the quadruple in-band frequency diversity mode A all even-numbered groups are combined, and all odd-numbered groups are combined.

Failure to connect these cables will not cause a gross modem malfunction in any of the operating modes where they are specified. However, loss of in-band frequency diversity benefits will be experienced.* For this reason, an in-band frequency diversity fault indicator is provided on the front panel to warn the operator that an improper in-band frequency diversity patch has been made.

Expansion to 9600 Bps

The ANDEFT/SC-320 has been designed for ready expansion to data rates of 7200 and 9600 bps in a standard 3 kHz hf voice band. Operation at 7200 bps may be attained with eight-phase coding while operation at 9600 bps may be achieved by employing both eight-phase coding and frequency-differential level modulation (FDLM).

Conversion to 9600 bps will require replacement of the present modulator input register and character selector gates with a new design capable of storing four bits of encoded data and making character decisions by selecting one combination of eight input phases and two levels. Expansion of the demodulator will necessitate the addition of FDLM detection and eight phase pattern generation circuitry and doubling the storage capacity of the output register. Both the

*Failure to disconnect these cables when operating in modes for which they are not specified will cause an intolerably high error rate. This condition also produces a diversity fault indication.

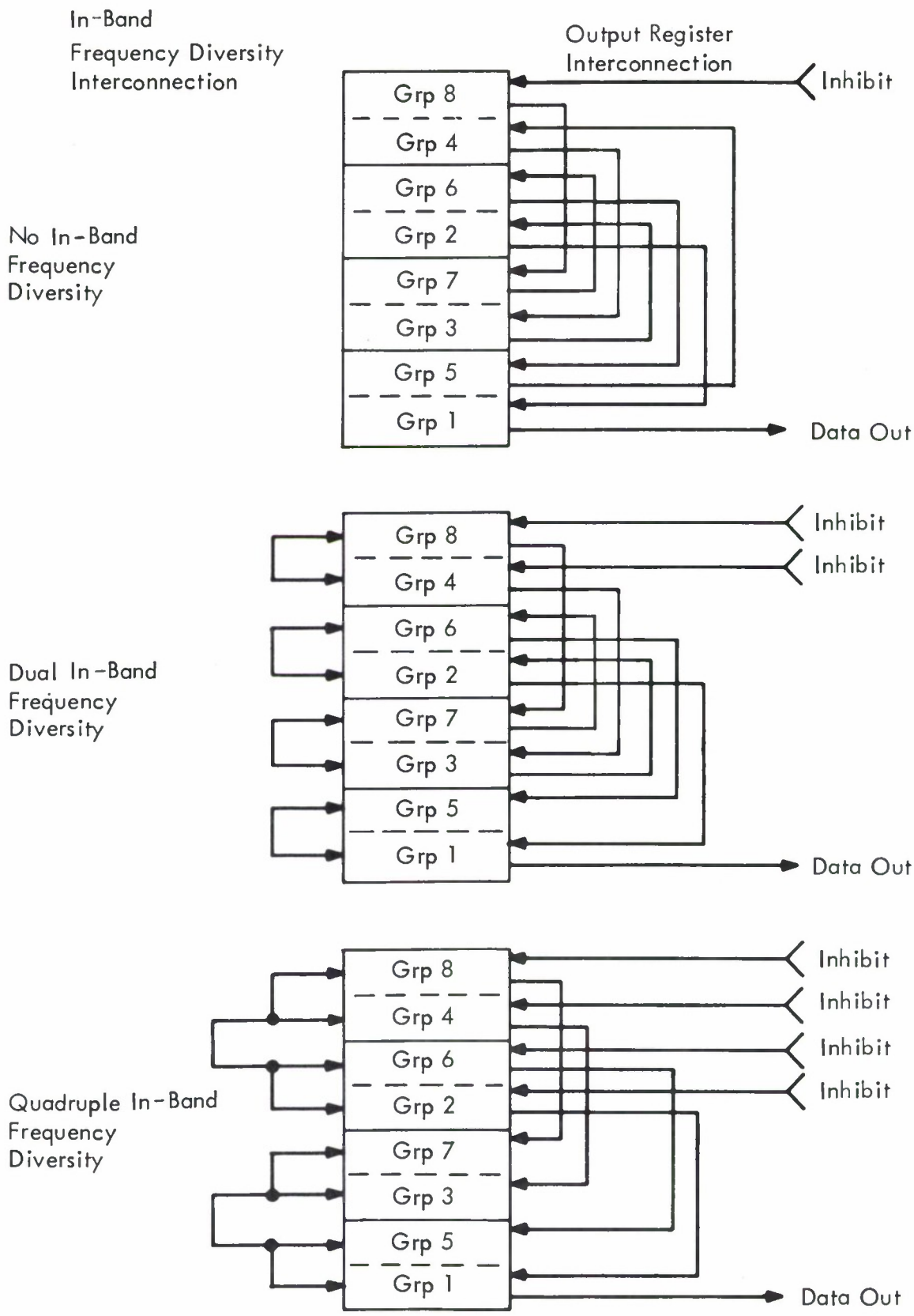

Figure 20. Demodulator Group Interconnection for Frequency Diversity

modulator and demodulator cabinets have sufficient unused space to accommodate the additonal PC boards required to implement the required functions.

Although an increase in the raw data error rates must be anticipated when operating at 7200 or 9600 bps, the increased data rates can be utilized to reduce significantly, the 4800bps system throughput error rate via the application of appropriate error control techniques.

SECTION III

ENGINEERING STUDIES

Introduction

A report entitled "Detailed Engineering Analysis, Tradeoff Studies, and Technical Solutions of the Design Requirements for the Correlation Detection and Crosstalk Compensation Portions of a 4800 BPS Frequency-Differential Phase-Shift Keyed Digital Data Modem" (2) was prepared to fulfill the requirements of Contract No. AF 19(628)-5536 Mod. 1, and was submitted on 1 December 1965 with the third monthly milestone report. The study included an analysis of the design requirements for correlation detection and crosstalk compensation of the proposed modem and an evaluation of possible technical solutions.

The basic problems which had to be solved to implement the ANDEFT technique were:

1. To select a technique for the coherent detection of a frequency-differential phase-shifted modulated signal which does not contain multiple unmodulated reference tones.

2. To investigate the effects of crosstalk caused by multipath propagation and methods to reduce these effects.

3. To consider the implementation of a decision directed measurement scheme.

The following sections discuss the techniques considered, the reasons which led to the selection of a particular technique, and the actual method of implementation.

Correlation Detection

Several solutions to the problem of selecting a demodulation technique were investigated and are described below, together with some comments on their practicality.

1. Low level balanced diode multipliers which make use of the square law behavior of semi-conductor diodes at low current levels were investigated. In order to obtain the dynamic range required, it is necessary to operate the circuits to very low levels. Noise problems appear at low levels and this is

a major deterrent to this approach. In addition, tracking, especially with varying temperature, between pairs of multipliers, presents a serious problem.

2. High level balanced networks which provide the desired square law characteristic through multiple diode-resistor networks were investigated. The difficulty encountered with this approach was that it was necessary to work with levels higher than convenient in order to obtain an adequate range of operation. Furthermore, the number of diodes and resistors was too large for an application requiring a large number of circuits.

3. Hall-effect multipliers were considered, but were ruled out for this program because of their high cost.

4. AC integrate and dump techniques using either LC filters or commutated RC digital filters were investigated. The extremely high Q's required with this technique makes the use of LC filters less desirable from a component and stability point of view. In the RC digital filter, the composite input signal is commutated (sampled) at a rate of n x f_d times per second, where f_d corresponds to the frequency of the desired signal tone. Each of the n commutator positions connects to an RC integration network, and the output of the n integrators are reassembled by means of a second commutator running in synchronism with the input commutator. The bandwidth of such a "filter" can be made arbitrarily small by increasing the time constants of the n integrators, and the circuit has the valuable property that the center frequency accuracy is determined solely by the stability of the commutating frequency. Use of this technique in its basic form in the ANDEFT demodulator was found to be somewhat impractical for two reasons:

   a. The bandwidth requirements necessitate the use of time constants which are inconvenient to realize with simple RC networks using reasonable component values. Furthermore, the use of such long time constants results in a very low level of the output signal.

   b. The use of this scheme would still necessitate the use of individual multiplexers before or after the commutation in order to make the differential phase comparison.

The technique finally developed for use in the ANDEFT demodulator has all the advantages of the RC digital filters without incurring the above mentioned penalties. Section II presents a detailed description of the technique. In this scheme, a pair (sine and cosine) of correlators are provided for each signal tone and reference frequencies are derived from the local clock. This, to some extent, corresponds to the input commutation and integration of the digital filter with n = 2. The output of the pair of correlators is now, however, commutated at a standard processing frequency which thus combines the functions of DC to AC conversion and multiplexing in one step, which is made possible because of the fact that the phase

comparison and character decision is only made after completion of the correlation interval.

Crosstalk Compensation

A computer study was conducted to determine the amount of interchannel and adjacent symbol crosstalk caused by the effects of limited bandwidth, multipath delay spread, and misframing, and to evaluate methods for reducing the effects of these phenomena. The computer program was devised to calculate the amplitudes of the outputs of both a sine and a cosine correlator for a given tone position with a four-pole Butterworth filter (of the same characteristics as the receiver group filters) in the transmission path under the following conditions:

1. Receiver time base misframing of 0 to 2.5 milliseconds corresponding to multipath spread of 0 to 5 milliseconds.

2. Input signal corresponding to correlator reference frequency, i.e., an input tone which produces desired output.

3. Input signal differing from correlator reference frequency by n x Δf, i.e., interchannel crosstalk.

4. Input signal consisting of adjacent symbol transmission only, for all tone positions, i.e., intersymbol crosstalk.

The program was run for all the foregoing cases with:

a. Signal tone in the center of the group filter passband.

b. Signal tone near the edge of the group filter passband.

Also, each of the foregoing cases was run with:

a. No guard time — The receiver integration period is equal to the transmitted symbol length; both are the reciprocal of the tone spacing.

b. Shortened detection time - The receiver integration period is six percent or 1-2/3 milliseconds less than the transmitted symbol length and interchannel compensation is applied within the group; the transmitted symbol length is the reciprocal of the tone spacing.

c. Guard time — The receiver integration period is six percent or 1-2/3 milliseconds less than the transmitted symbol length; the receiver integration period is the reciprocal of the tone spacing.

The computer program was checked out by comparing the results with values obtained by manual computation for several selected cases and by running the program under the condition of no filter in the transmission path for which case the expected results are easily calculated. The sketches in Figure 21 show the resultant crosstalk (both interchannel and adjacent symbol) as a function of the input signal tone position for a misframing δ of the receiver time base of 0, 0.83, and 2.5 milliseconds, respectively. Figures 21a and 21b present the case where no special measures to combat crosstalk effects are employed. Figure 21a depicts the desired signal tone position centrally located with respect to the signal group, and Figure 21b depicts the desired signal tone at the edge of the group.

Figures 21a and 21b show that the effect of the presence of the filter in the transmission path is twofold:

1. Crosstalk contributions from tones outside the passband decrease rapidly.

2. Crosstalk for perfect framing does not reduce to zero, i.e., some residual crosstalk remains due to the "smearing" effect of the filter.

Figures 21c and 21d correspond to Figures 21a and 21b. However, the receiver integration period has been shortened by 1-2/3 milliseconds and a crosstalk compensation matrix has been applied to the outputs of the correlators corresponding to all tones within the signal group. The following conclusions are drawn from these results:

1. For misframing up to the edge of the guard interval, i.e., $\delta \lesssim 0.83$ milliseconds, the crosstalk results from tones within the group is substantially reduced.

2. For misframing greatly exceeding this value, the advantage gained with respect to crosstalk resulting from tones within the group is much smaller.

3. An increase is noted in crosstalk from tones just outside the group limits for very small values of δ. Further analysis shows this to be caused by the fact that the compensation matrix actually acts to increase the amount of crosstalk from tones whose correlator outputs are not used in the compensation scheme, i.e., tones outside the signal group. Unfortunately, this effect exceeds the benefits derived from the reduction of crosstalk resulting from tones within the group and effectively rules out the use of this method of crosstalk compensation for a system where it is impractical to incorporate all signal tones in the compensation process.

Figures 21e and 21f show the results for the case where guard time is used, i.e., transmitted symbol length is greater than the reciprocal of the tone spacing. As expected, the reduction in crosstalk for this case is uniform and does not exhibit any of the above effects.

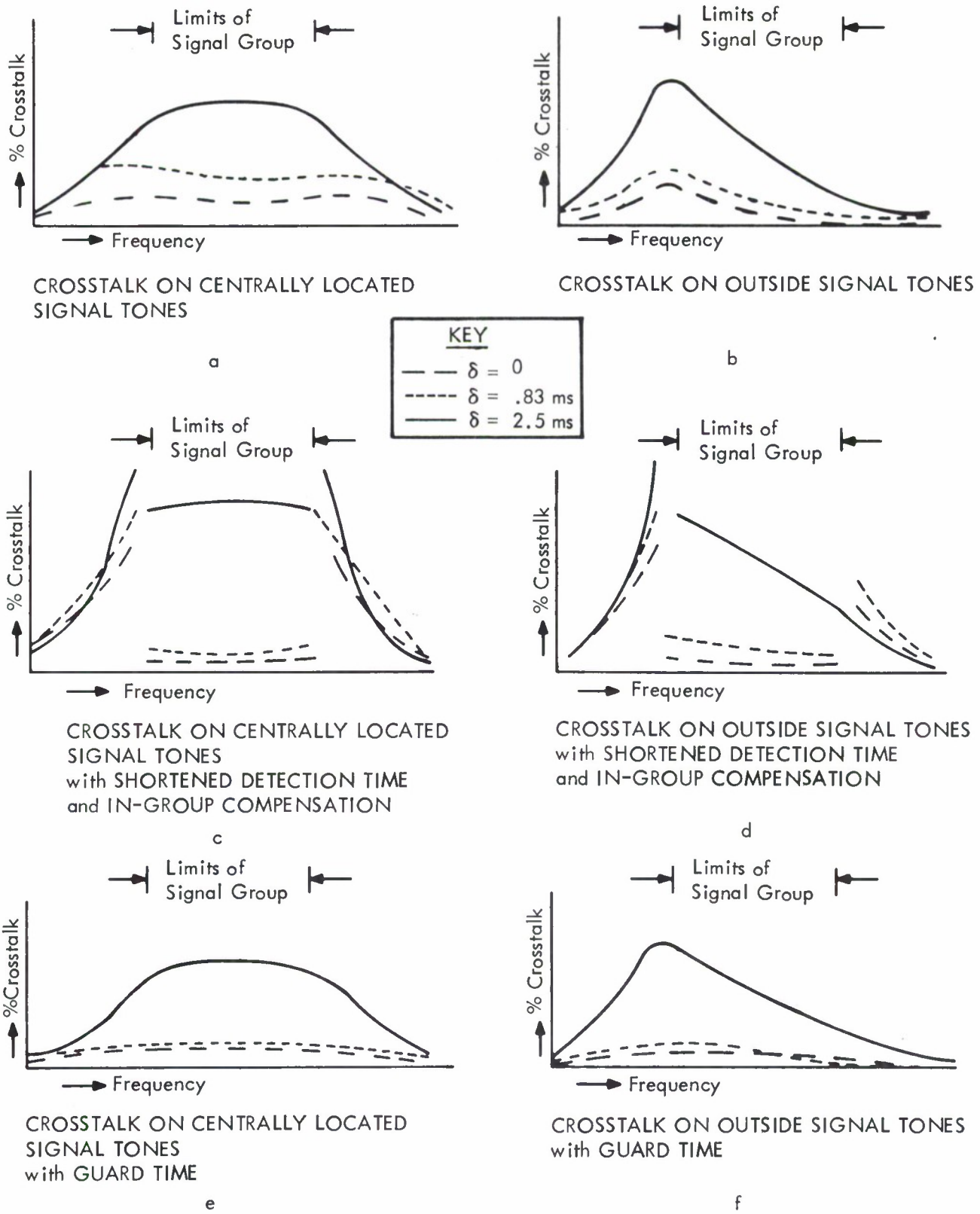

Figure 21. Crosstalk Test Results

Figures 22 and 23 show the resultant signal-to-(rms) crosstalk ratio for each of the preceding cases plotted against multipath spread, assuming two paths of equal amplitude. For comparative purposes, an additional run of the computer program was made using constants corresponding to the SC-302 DEFT modem. The results are also shown in Figures 22 and 23. The "flatness" of this curve labeled "SC-302" compared to the other curves is due to the fact that the SC-302 precorrelation filters have only half the bandwidth and the symbol length is 50 percent greater than the ANDEFT signalling parameters.

The results plotted in Figures 21a, 21b, 21e, and 21f point out an important fact, namely, that the signal-to-crosstalk ratio remains relatively constant under fading conditions due to the fact that most of the crosstalk energy is contributed by tones not more than approximately 150 Hz away. Because of this, a first order evaluation of the signal-to-crosstalk ratios in terms of self-error rate is justified. Consequently, a line representing a self-error rate of 1×10^{-6} is shown in Figures 22 and 23. The position of this line was derived from the test data from the SC-302 modem. As the two equal-path multipath condition assumed in Figures 22 and 23 is actually a worst-case condition (which for multipath spreads exceeding 1-1/2 to 2 milliseconds will never be encountered in practice), the self-error rate of the ANDEFT modem using 1-2/3 milliseconds guard time can be safely neglected.

Decision Directed Measurement Scheme

A complete discussion of the character decision process is presented in Section II of this report. Phase error compensation is obtained in the equipment by selecting the appropriately advanced or retarded character decision pattern to achieve the best group average position with respect to the "Z" pulses. The procedure described fulfills the requirements of a decision directed measurement scheme.

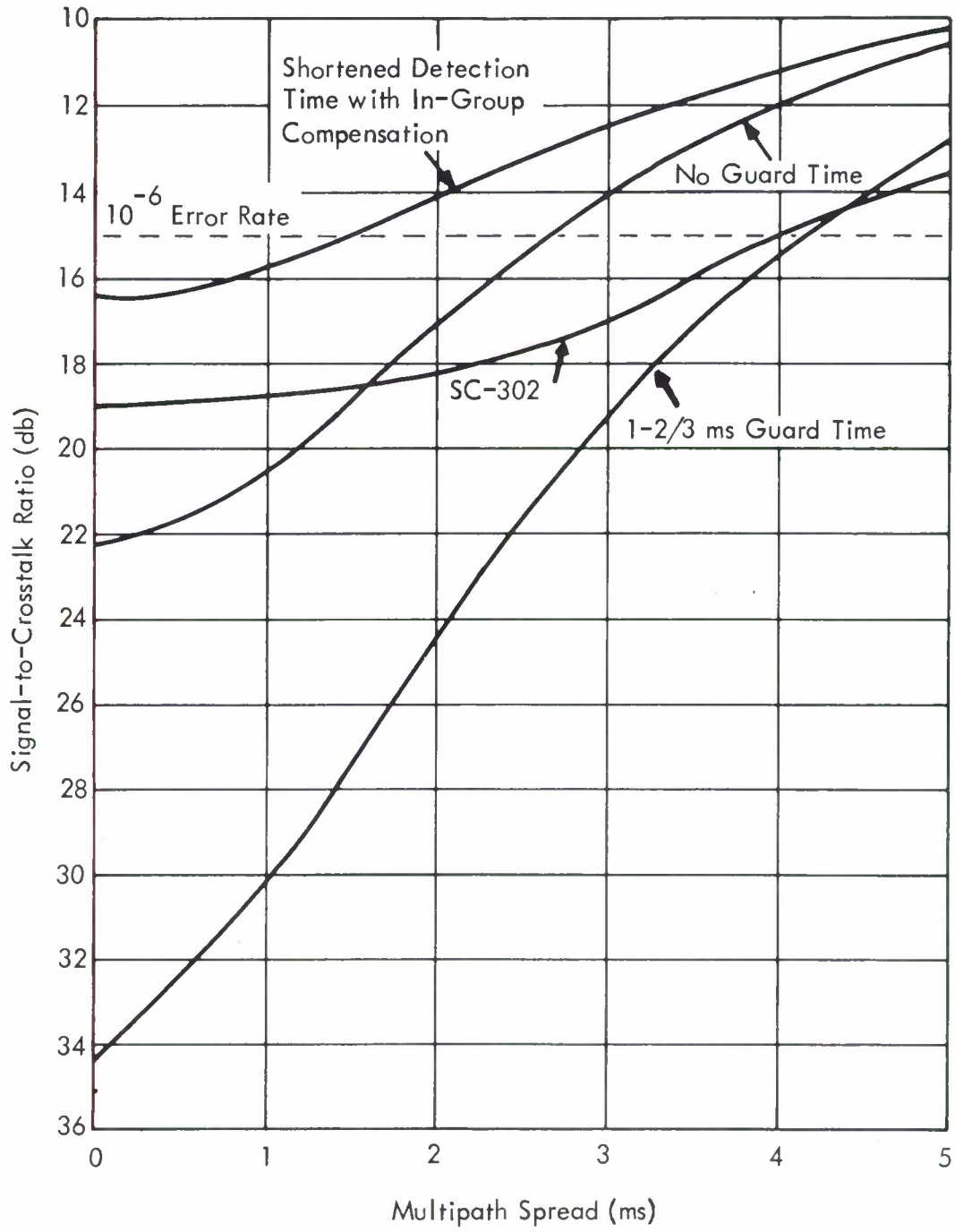

Figure 22. Signal-to-Crosstalk Ratio for Centrally Located Signal Tones

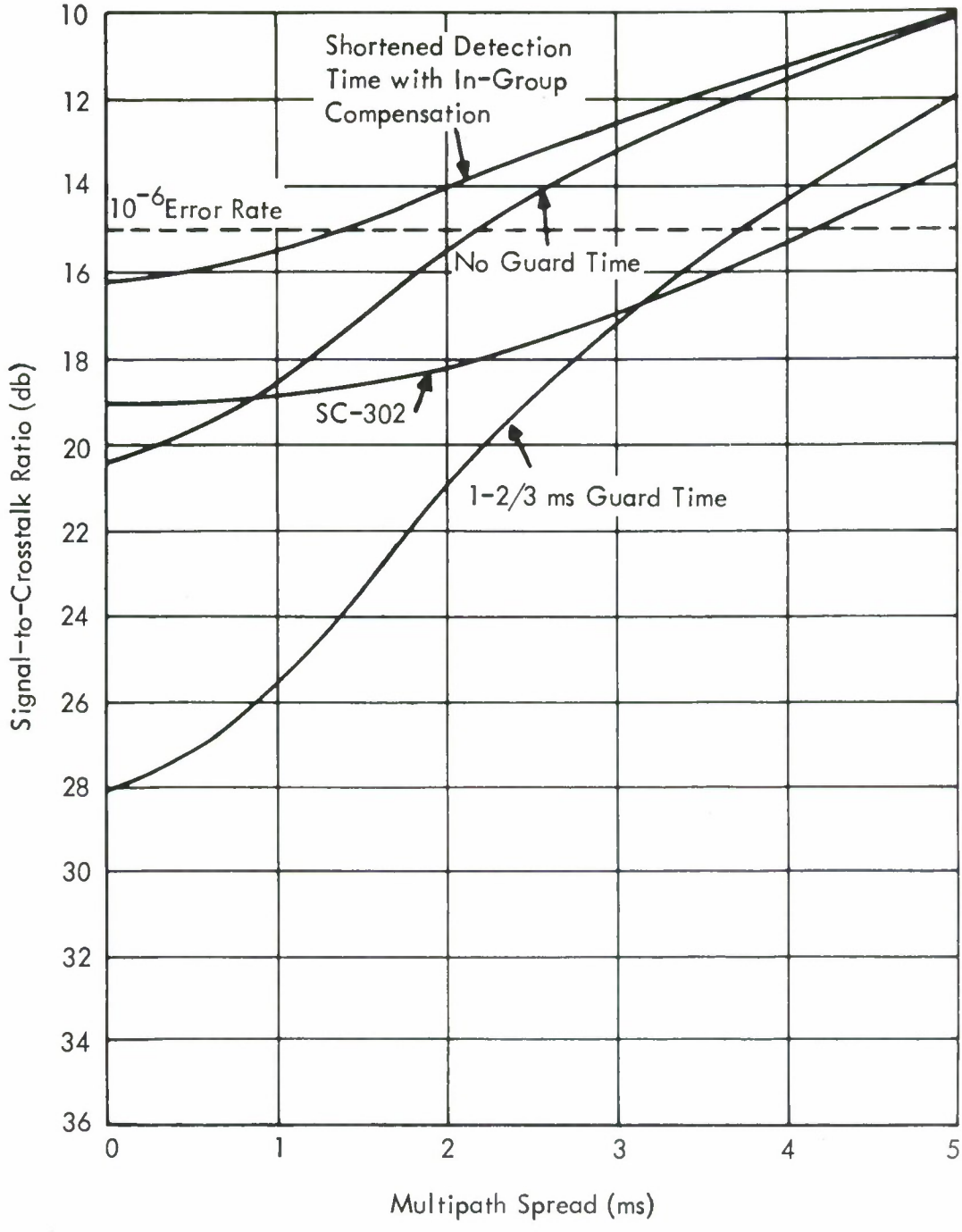

Figure 23. Signal-to-Crosstalk Ratio for Outside Signal Tones

SECTION IV

LABORATORY EVALUATION AND TEST

The primary objective of the test program was to demonstrate the feasibility and performance, when subject to additive Gaussian noise, of the "true" frequency-differential phase-shift keyed modulation technique as implemented in the ANDEFT/SC-320, a full-scale prototype ultra high speed digital data modem. The test program was conducted by the Advanced Development Department of the Electronics Division of General Dynamics of Rochester, New York on 20, 21, and 22 September 1966.

A block diagram of the test set-up is shown in Figure 24. The noise bandwidth for the tests is defined by the receiver input circuit frequency response which has an equivalent rectangular noise bandwidth of 4250 Hz. The tests were performed according to the procedures detailed in the Final Test Plan.[3]

Two series of tests were performed. The first of these measured the error rate performance of the prototype modem when subject to additive Gaussian noise at the 4800, 2400, and 1200 bps rates. The equipment was operated back-to-back with no reception (signal source) diversity. Tests were conducted to determine the measured bit error rate to at least 10^{-6}.

The second series of tests were performed to demonstrate the ability of the prototype modem to establish and maintain synchronization when subject to additive Gaussian noise. The equipment was operated back-to-back at 4800 bps with no reception diversity. The tests were conducted to a measured bit error rate of 10^{-2}. After the receiver was synchronized at a noise level corresponding to this error rate, misframing was accomplished by momentarily turning off the receiver power. The time required to re-establish synchronization after power was returned was measured. This test was repeated four times and the results are reported in Section V.

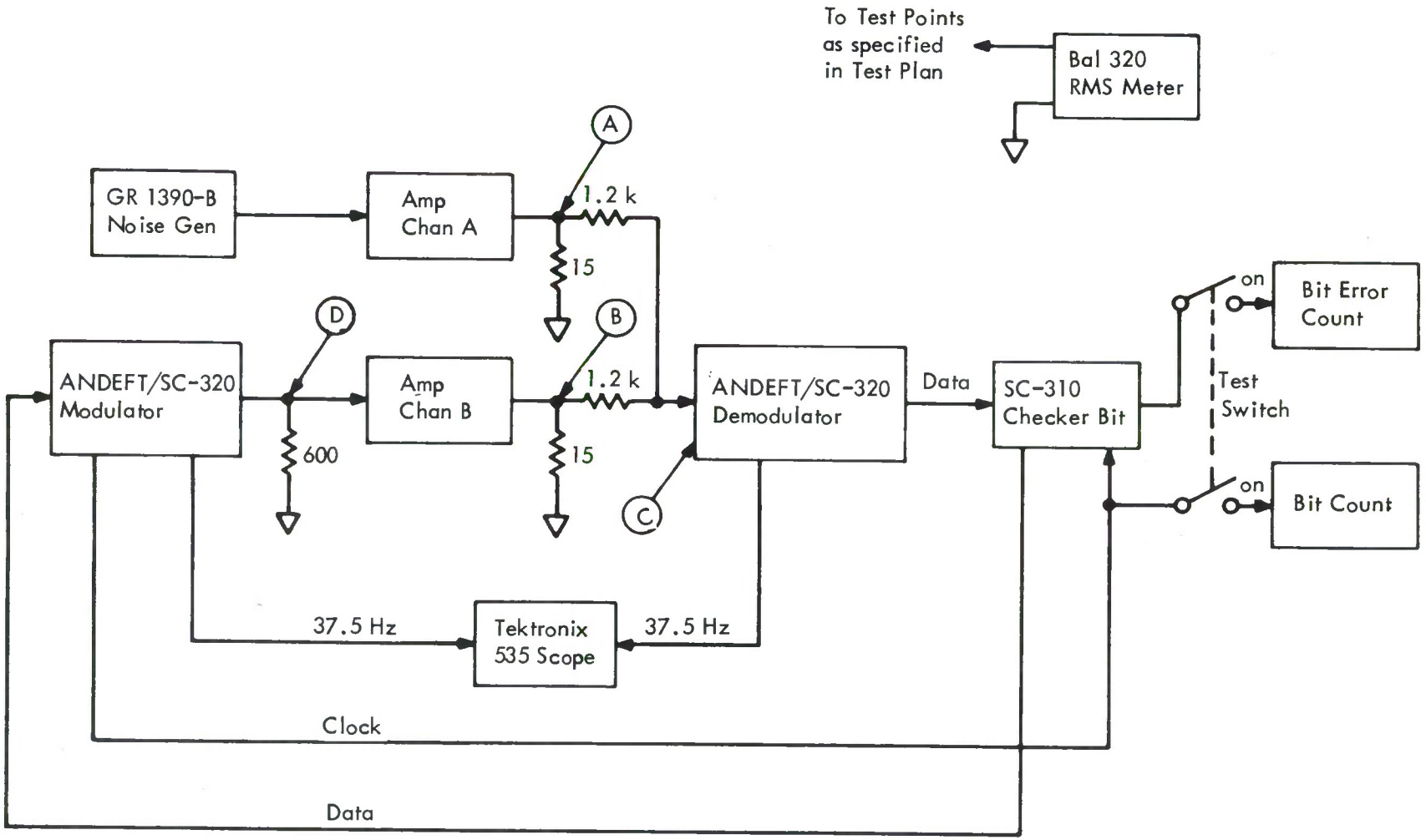

Figure 24. Acceptance Test Block Diagram

SECTION V

TEST RESULTS AND ANALYSES

Four tests were performed to measure the performance of the ANDEFT/SC-320 when subject to additive Gaussian noise on a back-to-back basis with no reception (signal source) diversity. Test times and procedures were established by the Final Test Plan. The performance data is plotted in Figure 25 for each of the four modes of operation tested. The raw data is compiled in Figure 31 of the APPENDIX.

The data was evaluated by comparing the actual experimental performance to the theoretical performance prediction for an ideal differentially-coherent phase-shift keyed system as derived by Bussgang and Leiter.[7] For this purpose the data was replotted in Figures 26, 27, and 28, where the abscissa is the ratio of the energy per binary digit (E_0) in joules (including energy in the reference/sync tones) to the noise power density (N_0) in watts per hertz. These normalized presentations permit a direct comparison with the theoretical predictions of the performance of the prototype modem at different data rates for two and four-phase operation.

A comparison of the experimental performance of the ANDEFT/SC-320 operating at 4800 bps using four-phase modulation and no diversity to the predicted theoretical performance of an ideal differentially-coherent, phase-shift keyed system with no diversity in additive Gaussian noise is shown in Figure 26. At high bit error rates, between 10^{-2} and 10^{-3}, the experimental performance is within a few tenths of a db of the theoretical curve. At low bit error rates in the order of 10^{-5}, the experimental performance is within about 1.0 db of the theoretical prediction.

A comparison of the experimental performance of the ANDEFT/SC-320 operating at 2400 bps using four-phase modulation and dual in-band frequency diversity to the predicted theoretical performance of an ideal differentially-coherent, phase-shift keyed system with no diversity in additive Gaussian noise is shown in Figure 27. At high bit error rates, in the order of 10^{-2} to 10^{-3}, the experimental curve is within about 0.5 db of the theoretical curve. At low bit error rates, that is, between 10^{-5} and 10^{-6}, the experimental curve is within about 1.0 db of the theoretical curve.

A comparison of the experimental performance of the ANDEFT/SC-320 operating at 2400 bps using two-phase modulation and no diversity to the predicted theoretical performance of an ideal differentially-coherent, phase-shift keyed system with no diversity in additive Gaussian noise is shown in Figure 28. At high bit error rates the experimental curve is within about 0.5 db of the theoretical curve. At low bit error rates the experimental curve is within about 1.0 db of the theoretical curve.

A comparison of the experimental performance of the ANDEFT/SC-320 operating at 1200 bps using two-phase modulation and dual in-band frequency diversity to the

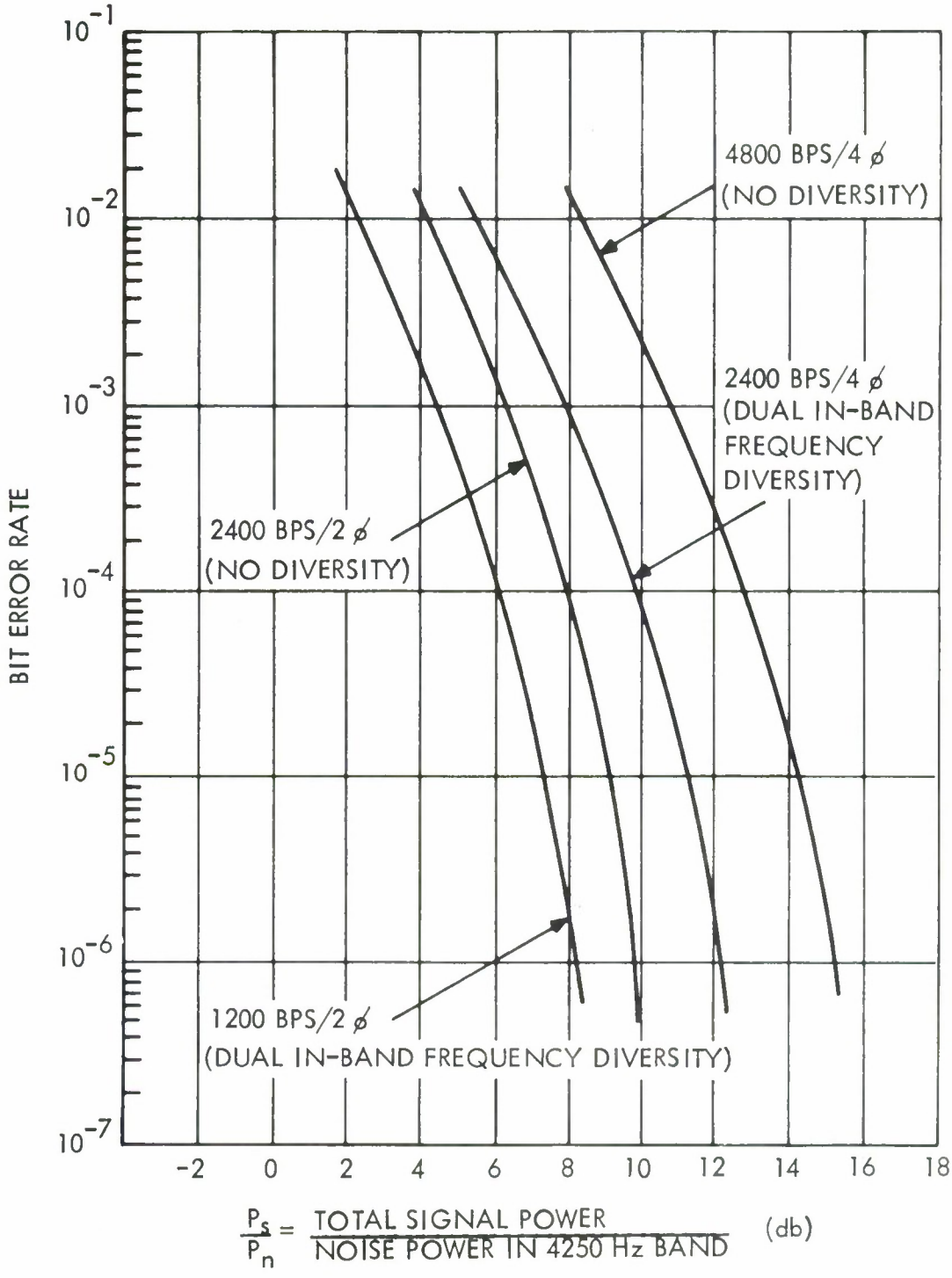

Figure 25. Acceptance Test Data of the ANDEFT/SC-320

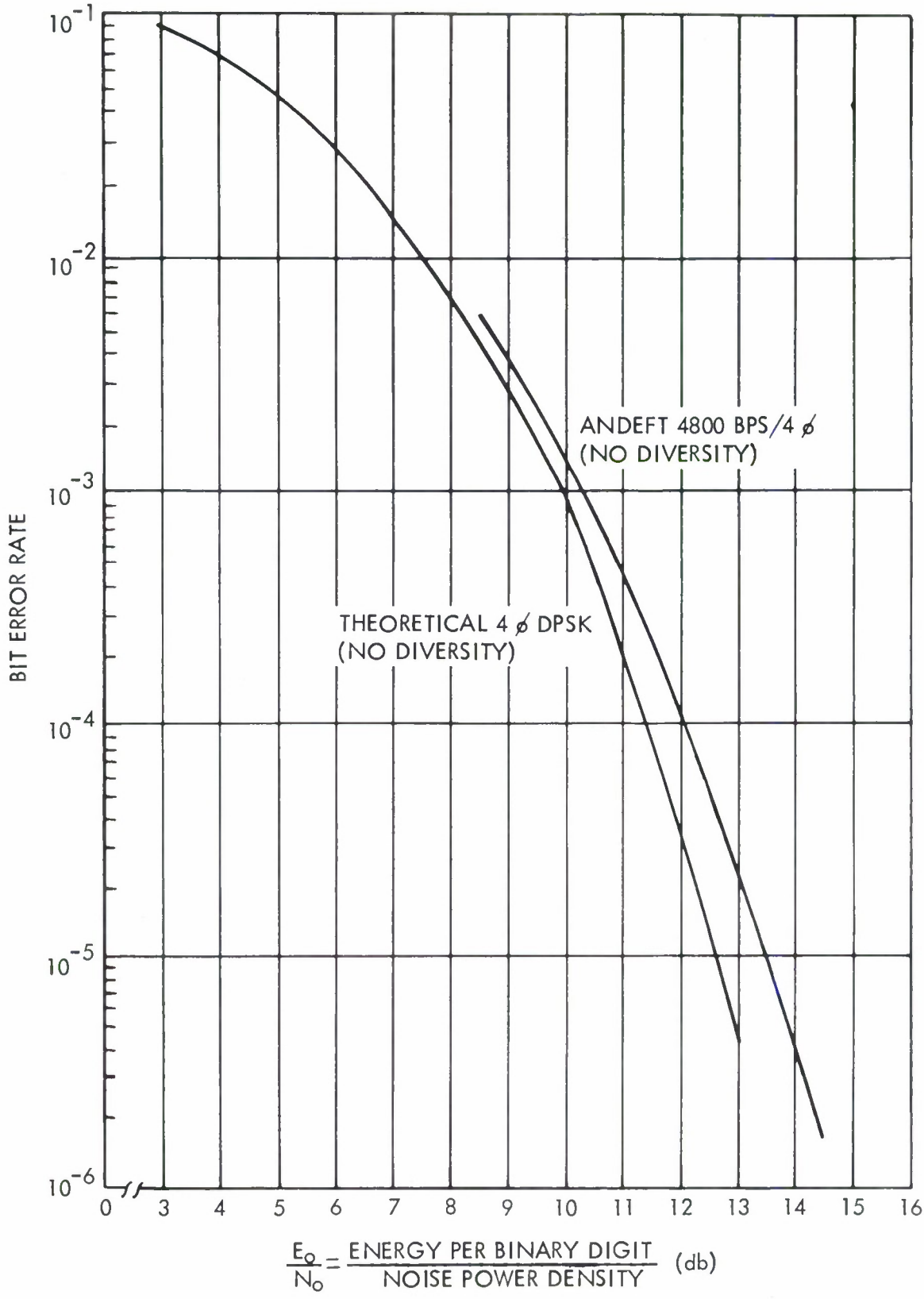

Figure 26. Performance of the ANDEFT/SC-320 in the 4800 BPS, Four-phase Mode

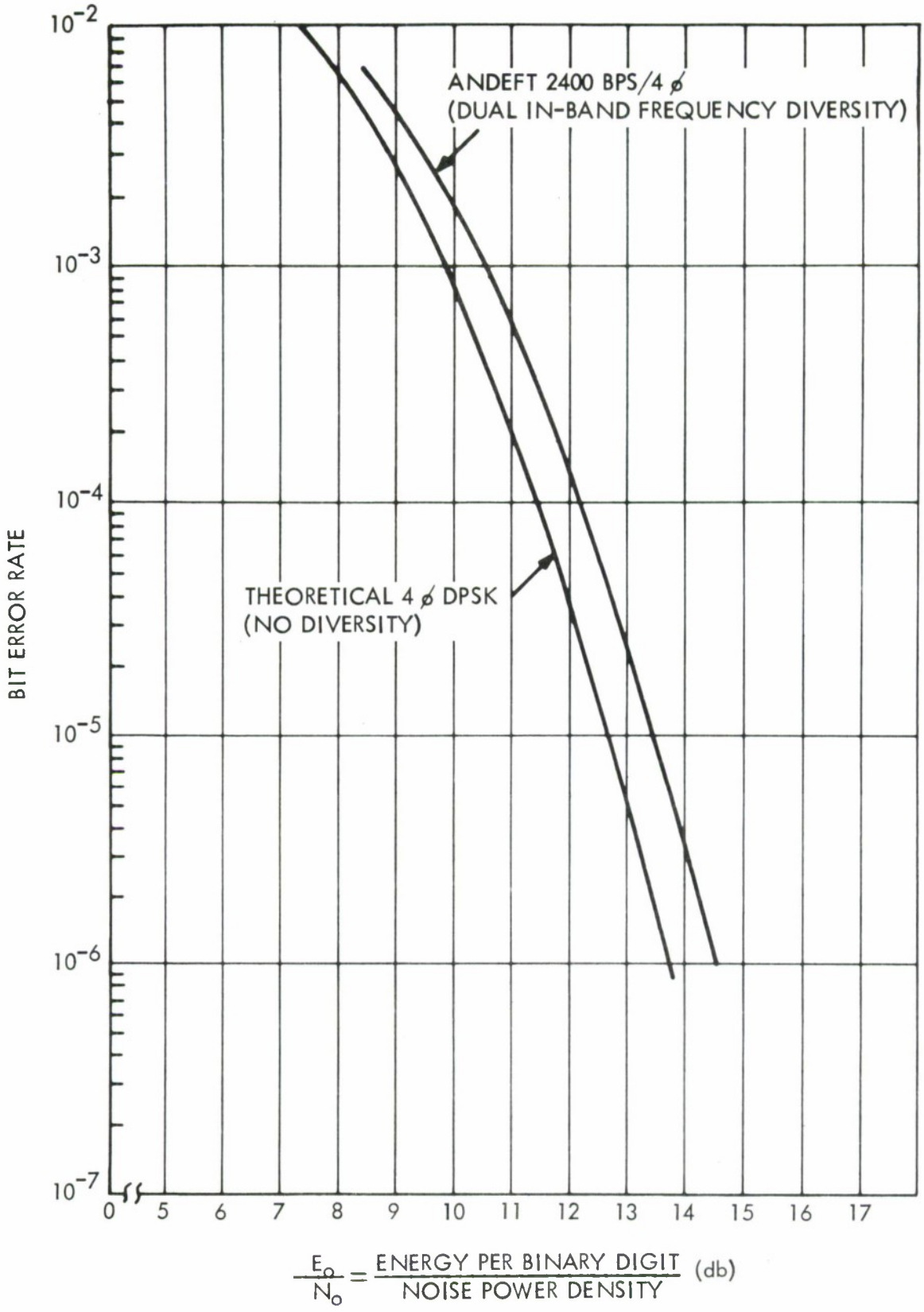

Figure 27. Performance of the ANDEFT/SC-320 in the 2400 BPS, Four-phase Mode

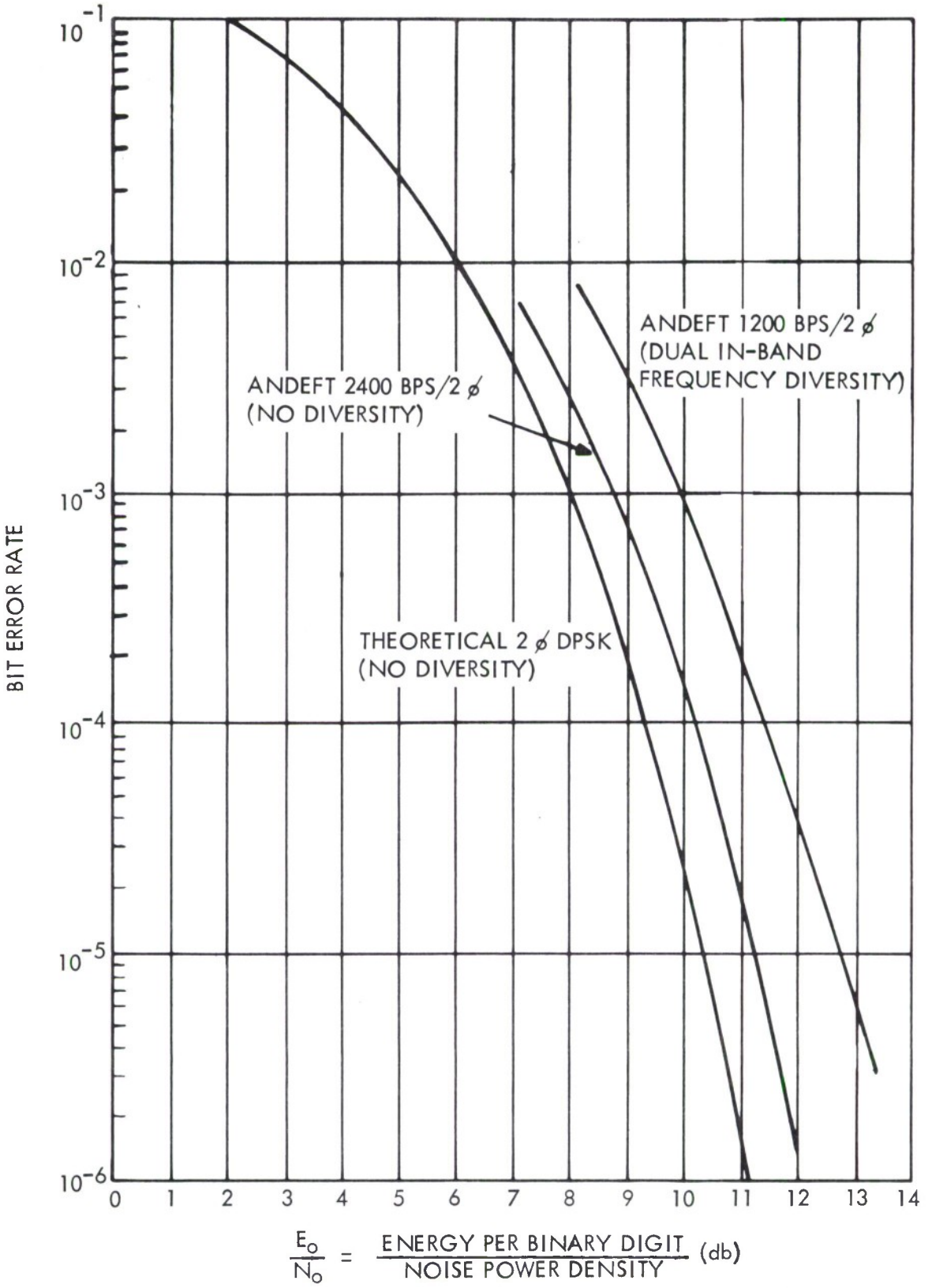

Figure 28. Performance of the ANDEFT/SC-320 in the 2400 BPS, and 1200 BPS, Two-phase Modes

predicted theoretical performance of an ideal differentially-coherent phase-shift keyed system with no diversity in additive Gaussian noise is also shown in Figure 28. This experimental curve is within about 2.0 db of the theoretical curve at high bit error rates, and at low bit error rates it is within about 2.5 db of the theoretical curve.

It should be recognized that the theoretical in-band diversity and non-diversity error rate vs. bit-energy-to-noise-density ratio curves are not necessarily identical for any differentially coherent demodulator employing equal-gain (or maximal-ratio) post detection diversity combining. The reason for this is that the differential phase errors from individual detectors are bounded (at $\pm 180^{o}$) and the phase error distributions are therefore not Gaussian. The non-Gaussian nature of the phase error distribution is most pronounced when the coding angle is large and when the waveform-energy-to-noise-density ratio is low. Both of these facts tend to magnify the effect of the non-Gaussian distribution when dual in-band frequency diversity is used with two-phase modulation. Although theoretical error rate curves have not been derived for the operating modes employing in-band diversity, it is not surprising that the difference between diversity and non-diversity error rates is small for the four-phase mode and somewhat larger for the two-phase mode.

A test was also performed to demonstrate the ability of the ANDEFT/SC-320 to establish and maintain synchronization when subject to additive Gaussian noise when operated back-to-back at 4800 bps with no reception (signal source) diversity. The table of data below shows the results of the four test trials required by the Final Test Plan.

Test No.	Approximate BER	P_s/P_n*	Time to Synchronize
1	1.27×10^{-2}	8.0 db	20 seconds
2	1.27×10^{-2}	8.0 db	27.5 seconds
3	1.27×10^{-2}	8.0 db	22.5 seconds
4	1.27×10^{-2}	8.0 db	21.5 seconds

* See Figure 25

The average time to acquire synchronization for the four tests is 22.875 seconds.

SECTION VI

CONCLUSIONS

The conclusions set forth below are based on the back-to-back tests with additive Gaussian noise described in Sections IV and V of this report. The equipment was operated at the 4800 and 2400 bps rates with four-phase modulation and at the 2400 and 1200 bps rates with two-phase modulation for the bit error rate performance evaluation with no reception (signal source) diversity although dual in-band frequency diversity was employed at the 2400 bps, four-phase, and 1200 bps, two-phase rates. The synchronizing tests were performed only at the 4800 bps rate. The following conclusions are drawn from the data:

1. The bit error rate of the ANDEFT/SC-320 at 4800 bps with four-phase modulation and 2400 bps with two-phase modulation (modes which do not use dual in-band frequency diversity) is within 1.0 db of the theoretical performance prediction for an ideal differentially-coherent, phase-shift keyed system at all measured signal-to-noise ratios.

2. The performance at the 2400 bps, four-phase, rate which uses dual in-band frequency diversity is nearly equal to the 4800 bps, four-phase, mode on a normalized energy-per-bit-to-noise density ratio basis.

3. The performance at the 1200 bps, two-phase, rate which also uses dual in-band frequency diversity is degraded approximately 1.0 db over the 2400 bps two-phase mode.

4. Since the nature of the synchronizing test data is statistical, it is felt that the four sample values taken in the acceptance test described herein, are insufficient to draw any precise conclusions. It was noted, however, that the average coarse sync acquisition time observed in these four trials (22.875 seconds) is nearly identical to the average time observed for this signal-to-noise ratio in previous laboratory tests at the time of system checkout. All sync acquisition times measured are within the design goal of 30 seconds.

5. Conclusively, it has been demonstrated that modem performance on a back-to-back basis with additive Gaussian noise and no reception (signal source) diversity closely approaches the predicted performance of an ideal differentially-coherent phase-shift keyed system.

SECTION VII

GROWTH POTENTIAL

The ANDEFT/SC-320 prototype modem was designed and fabricated to allow for easy expansion to 7200 and 9600 bps operation without major mechanical or electrical redesign. Also, according to the statement of work, the modem was fabricated in two separate independent sections (modulator and demodulator) to allow for testing over an HF link. Finally, cabinet volume was made sufficient to house a complete 9600 bps system, and plug-in positions for additional printed circuit boards within existing assemblies have been provided.

The requirements given in the statement of work determined the "shape" of the prototype equipment. The modulator and demodulator are pictured in Figures 29 and 30, respectively. The modulator has been housed in a separate rack that closely duplicates either of the two receiver racks, yet, for the 4800 bps version, contains just under 75 printed circuit boards. The receiver, on the other hand, is contained in two racks with a total board count of somewhat less than 500. As a prototype, experimental model, with expansion capability, power supplies and cooling blowers have been conservatively rated. No attempt has been made to "package" circuits in restricted space or to miniaturize. The objectives have been to meet the requirements of the work statement without sacrificing feasibility requirements for size, especially before the technique and circuits have proven themselves.

SECTION VIII

RECOMMENDATIONS FOR FIELD TESTS

Because existing laboratory test facilities often fail to adequately simulate many of the conditions which occur on actual HF radio links, a field test program is almost always necessary to conclusively demonstrate the performance characteristics of an HF data modem. It is therefore anticipated that the ANDEFT/SC-320 modem will be field tested over one or more long-haul HF links. A complete evaluation of the equipment would require that the modem be operated under a wide range of ionospheric propagation conditions using both two and four-phase modulation with all available combinations of in-band and reception diversity. The primary objective of the field test program would be the collection of error rate and error distribution data with collateral data on the characteristics of the propagation medium. The field test program also provides an excellent opportunity for performing the following experiments which may be of considerable value in determining the growth potential of the ANDEFT modem.

Frequency-Differential Phase Error Measurement

Expansion of the ANDEFT/SC-320 modem for 9600 bps operation requires the use of frequency-differential eight-phase modulation. The feasibility of using eight-phase modulation can be determined on the basis of phase error statistics which can easily be obtained from the field test program. The frequency-differential phase information for each channel can be derived from signals available at the appropriate test points in the modem.

Frequency-Differential Level Error Measurements

Also required for expansion of the ANDEFT/SC-320 modem for 9600 bps operation is the use of frequency-differential binary level modulation. Frequency-differential level error statistics obtained from the field test program would be a valuable aid in determining the feasibility of utilizing frequency-differential level modulation. The required level information can be derived from signals available at the appropriate test points in the modem.

Phase Error Correction Effectiveness Measurements

There is little doubt that the automatic phase error correction system will reduce the deleterious effects of the phase errors which it is designed to correct. Whether or not the on-the-air performance of the modem is sufficiently improved to justify the cost of the phase error correction system is another question. The effectiveness of the phase error correction system could be easily evaluated by comparing error rates when the modem is operated with and without phase error correction. The number of uncontrolled variables in this experiment could be minimized by using one recorded signal sample (rather than two different live signal samples) for the two test runs.

Comparison of Reception Diversity Combining Techniques

Post-detection equal-gain combining is presently being used in the ANDEFT/SC-320 modem for reception diversity operation. A significant reduction in the size and cost of the modem could be achieved by using predetection selection of group signals rather than post-detection equal-gain combining. The extent to which the modem performance would be altered by such a modification depends on the fading bandwidth, multipath delay spread, and a number of other factors. If the selection combining circuits were available for at least two groups in the ANDEFT/SC-320 modem, a comparison of the two reception diversity combining techniques could be made using magnetic recordings of the received signal.

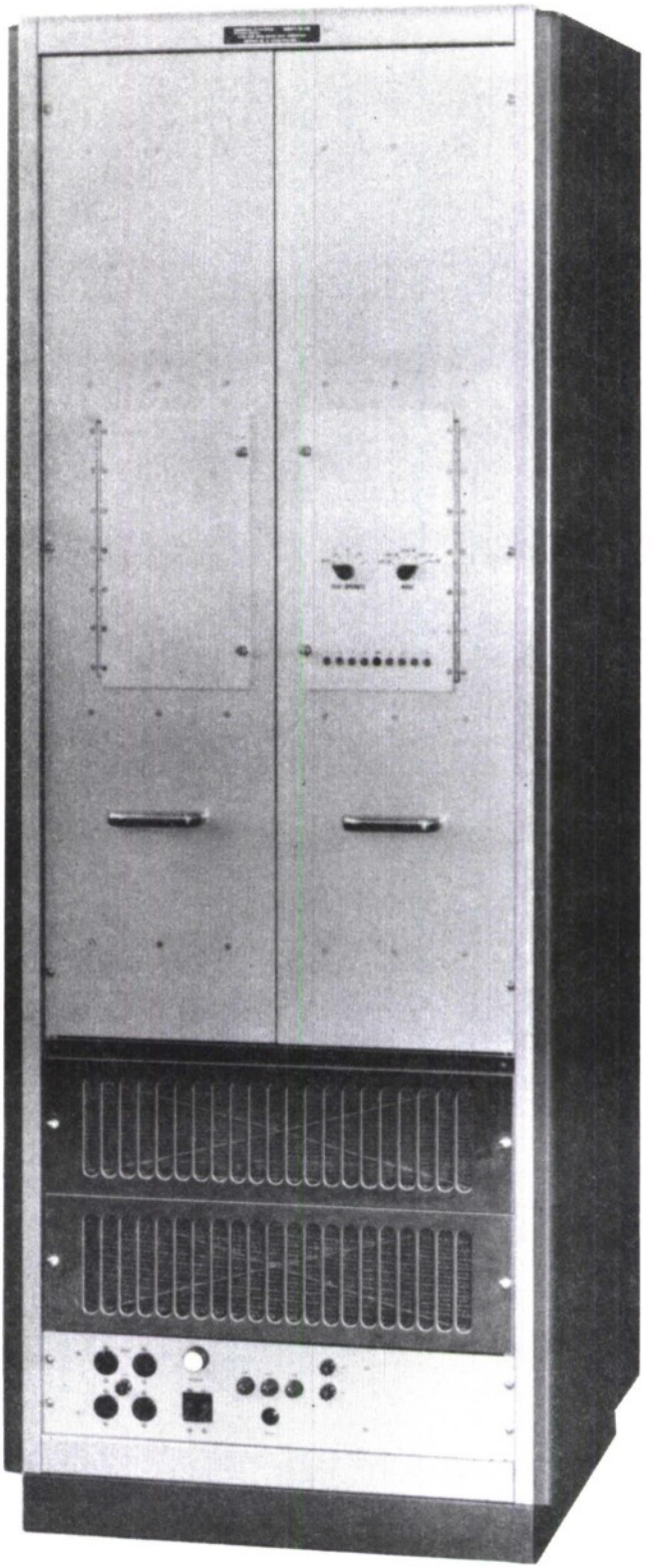

Figure 29. ANDEFT/SC-320 Data Modem Prototype Modulator

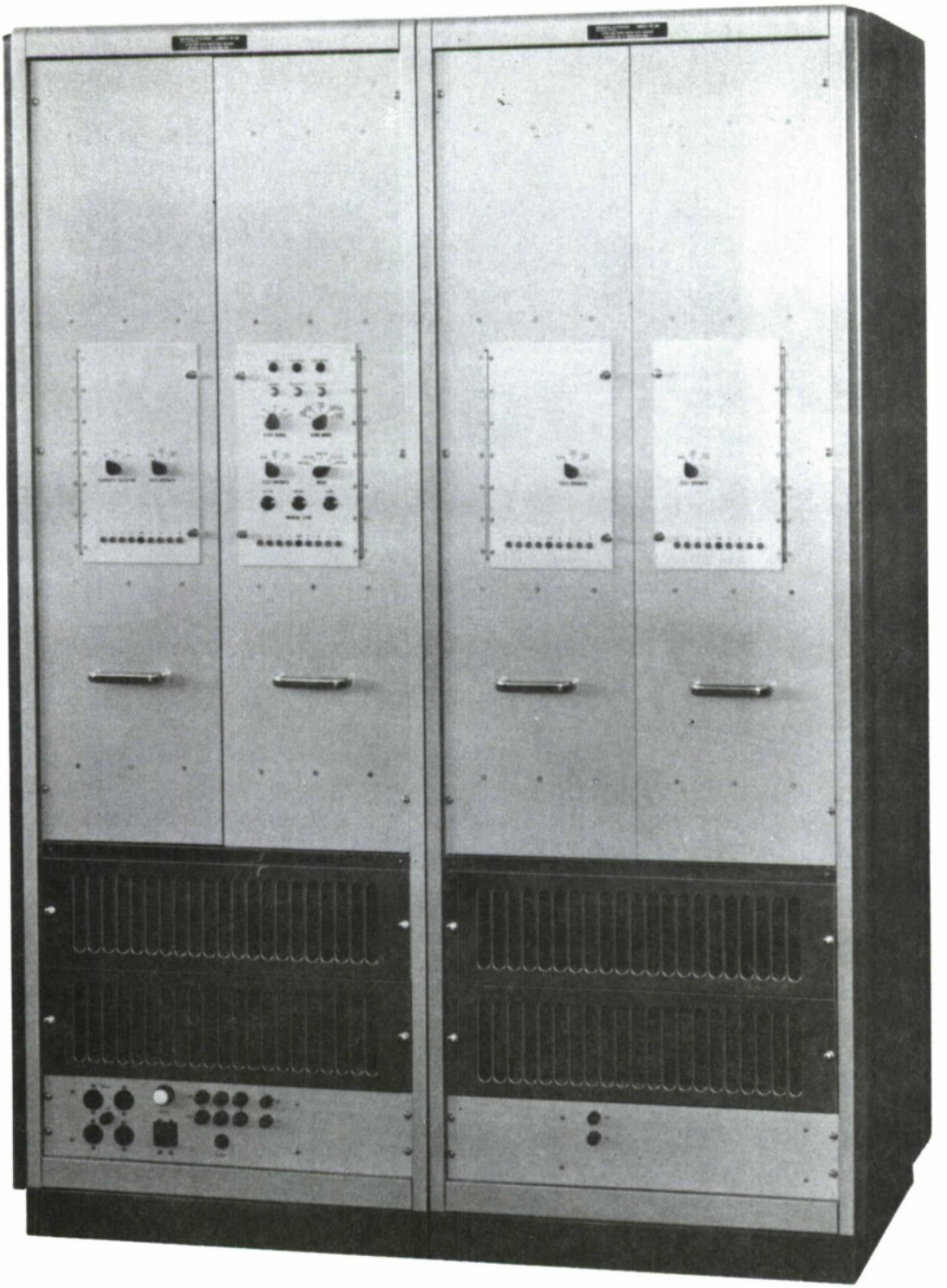

Figure 30. ANDEFT/SC-320 Data Modem Prototype Demodulator

APPENDIX

21 & 22 September 1966

ANDEFT/SC-320 ACCEPTANCE TEST RAW DATA

Test Series No. 1 4800/4-phase No Diversity

Pt. No.	P_s/P_n *	Total Bits	Total Errors	BER
1	9.0	1,501,170	8372	$.558 \times 10^{-2}$
2	11.0	1,500,831	1119	$.745 \times 10^{-3}$
3	12.5	1,500,500	145	$.965 \times 10^{-4}$
4	13.5	10,001,030	250	2.5×10^{-5}
5	15.0	10,001,144	15	1.5×10^{-6}

Test Series No. 2 2400/2-phase No Diversity

Pt. No.	P_s/P_n *	Total Bits	Total Errors	BER
1	4.5	750,371	5519	$.736 \times 10^{-2}$
2	6.0	750,497	942	1.25×10^{-3}
3	7.5	1,500,432	171	1.14×10^{-4}
4	8.5	10,000,497	221	2.21×10^{-5}
5	9.5	10,000,461	13	1.30×10^{-6}

Test Series No. 3 2400/4-phase Dual In-band Frequency Diversity

Pt. No.	P_s/P_n *	Total Bits	Total Errors	BER
1	6.0	750,520	4855	$.648 \times 10^{-2}$
2	8.0	751,111	667	$.889 \times 10^{-3}$
3	10.0	1,500,332	95	$.633 \times 10^{-4}$
4	12.0	10,000,576	9	0.9×10^{-6}
5	-	-	-	-

* See Figure 25.

Figure 31. ANDEFT/SC-320 Acceptance Test Raw Data (Sheet 1 of 2)

APPENDIX

ANDEFT/SC-320 ACCEPTANCE TEST RAW DATA (Cont.)

Test Series 4 1200/2-phase Dual In-band Frequency Diversity

Pt. No.	P_s/P_n *	Total Bits	Total Errors	BER
1	2.5	400,126	3474	$.868 \times 10^{-2}$
2	4.5	400,017	325	$.813 \times 10^{-3}$
3	6.0	1,500,136	123	$.820 \times 10^{-4}$
4	7.0	10,000,125	101	1.01×10^{-5}
5	8.0	10,000,155	27	2.70×10^{-6}

* See Figure 25.

Figure 31. ANDEFT/SC-320 Acceptance Test Raw Data (Sheet 2 of 2)

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13. ABSTRACT

The ANDEFT/SC-320 is a variable rate (4800, 2400, 1200, or 600 bits/second) digital data modem prototype specifically designed for reliable communication over long-range high-frequency radio circuits. This modem employs such advanced and proven techniques as frequency-differential phase-shift keying, correlation detection, extended symbol length, guard time, segmented AGC, and dual-mode precision synchronization to combat HF anomalies such as multipath delay spread, frequency selective fading, high intensity atmospheric noise and man-made interference. The modem has provision for dual signal source diversity operation to capitalize on available space, frequency, or polarization diversity facilities, and in addition, can be operated with in-band frequency diversity. The prototype is built in two separate cabinets (modulator and demodulator) to enable field testing and to allow for easy expansion to an ultimate data capacity of 9600 bits/second. This report presents the principles of operation of the modem and the results of tests to determine the back-to-back performance in additive white Gaussian noise.

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