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High Speed Tunnel Diode Transistor Micrologic Circuits

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MASSACHUSETTS INSTITUTE OF TECHNOLOGY

LINCOLN LABORATORY

HIGH SPEED TUNNEL DIODE TRANSISTOR MICROLOGIC CIRCUITS

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Group 62

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LEXINGTON MASSACHUSETTS

ABSTRACT

A set of logically flexible digital building blocks capable of implementing various logic functions with delays of less than one nanosecond has been developed and fabricated in microcircuit form.

The set consists of two basic types of circuit modules; with these, all conceivable digital system logic functions can be implemented. Tunnel junction diodes and silicon transistors provide gating functions, and a universal amplifier circuit module reshapes signal waveforms, restores amplitudes, and stores signals (flip-flop operations).

Subnanosecond switching time is achieved by the effective utilization of a tunnel diode transistor circuit and hybrid integration techniques for microcircuit fabrication. The circuit provides the following characteristics: (1) low power delay time product (efficient switching); (2) effective noise immunity; (3) well-defined temperature invariant transfer characteristics; (4) relaxed component tolerances as compared to other tunnel diode logic circuits; (5) high fan-in and fan-out ratios; and (6) capability of performing all logical functions with two basic circuit configurations.

The circuits were developed primarily for a high-speed digital system operated at a 100- to 200-Mcps clock rate with a low impedance transmission line signal distribution scheme.

Analysis of the circuit, optimization of the circuit characteristics, fabrication techniques of the circuit modules, and experimental results in a high-speed digital system are discussed.

Accepted for the Air Force
Franklin C. Hudson
Chief, Lincoln Laboratory Office

1.0 INTRODUCTION

Recent advances in integrated circuit technology have reduced the switching times of digital circuits in microcircuit forms to the nanosecond speed range. This advance has made a great impact on digital system technology, not only on digital-computer design, but also on information processing by digital means.

Signal processing by digital circuits is attracting more attention in various data processing fields. To process high-frequency signal waveforms by digital circuits in real time, extremely high switching speeds are required for a basic logic element. For this requirement, a set of logic modules that is capable of implementing various logic functions with less than a 1-nanosecond stage delay have been developed.

Design considerations for a logic circuit for an extremely high-speed digital system are discussed in the early sections of this paper. A detailed design and practical applications of the proposed circuits in a high-speed digital system are presented in the latter sections.

2.0 FUNDAMENTAL DESIGN CONSIDERATIONS FOR A HIGH-SPEED LOGIC CIRCUIT

In general, the term "very high speed" used in connection with a digital system is assumed to refer to a clock rate higher than 50 Mcps. Therefore, unless the signal transmission paths are short, the signal distribution system must be based on microwave transmission techniques.

Two basic distribution methods can be conceived. In one, a high impedance output stage drives the line, placing the termination at the line input. In the second, a low impedance output stage drives the line, placing the termination at the far end of the line. Each method has its merits, but the second can drive more than one line and, hence, provides higher fan-out capability. Consequently, the second method was adopted.

Transmission line distribution methods impose the following special considerations on the design of logic circuits: First, the circuit must be able to drive low impedance lines. Second, since the load is low impedance, the signal amplitude should be selected on the basis of the current level and the high-frequency gain characteristics of the active output device. Third, the output stage drives a fixed

number of lines, i.e., a nearly constant load; thus, the fan-out is determined mainly by the permissible number of circuits that can be attached at the termination point.

These three considerations led to the following ground rules: (a) 75-ohm strip lines are adopted for the basic signal distribution media; (b) the output stage of the logic circuit should be capable of driving at least two 75-ohm lines; (c) the input impedance of the circuit at the far end of the transmission line must be high enough relative to the line impedance to make the effective termination for the line nearly constant, or within specified limits; and (d) the signal amplitude should be lower than 1 volt to restrict the current drain from the output stage to 30 ma or less.

Of several semiconductor switching elements available that are capable of switching in the nanosecond range, the transistor is the most flexible, albeit the slowest. One advantage to using transistors in a logic circuit is that they assure isolation between input and output, thus simplifying the clocking system. However, as a high-speed waveshaping element, the transistor is least suitable, because of the inherent excessive base storage effect. If transistors are not operated into saturation, the propagation delay through the device is not objectionable. The tunnel diode is suitable for waveshaping purposes because it has the least storage effect, and serves as a fast switching bi-stable clamp yielding a signal amplitude suitable for the requirements of low impedance signal distribution lines. From this point of view, the resulting tunnel diode transistor circuit in the proper circuit topology is both fast and flexible.

Based on these considerations (signal distribution methods and the device characteristics), the following basic logic circuit scheme is established. At the input, a high input impedance transistor amplifier is adopted to allow three similar circuits to load a 75-ohm distribution line. This stage provides gain, isolation, and logic functions. At the output, an emitter-follower is used to drive at least two 75-ohm lines. This stage serves as an impedance transformer without affecting the signal amplitude. Tunnel diodes are chosen for waveshaping, and are placed between the input and output transistor stages. They not only provide waveshaping, but also level and amplitude restoration, and storage as required.

Although the advantages of microcircuit packaging in ultra high-speed digital circuits are well established, the following points should be considered for economical and efficient fabrication of microcircuit modules:

(a) Circuit configurations should be simple to lay out and require as few components as possible.

(b) All components should be compatible with thin-film or monolithic fabrication techniques, and passive energy storing components should be avoided.

(c) A single circuit format should be considered for a multi-purpose module.

3.0 BASIC LOGIC CIRCUIT CONFIGURATION

The emitter-follower is a useful circuit configuration for impedance matching with low impedance transmission lines. However, in high-speed digital circuits, the emitter-follower configuration is usually avoided because of its instability.

Since the characteristics of the emitter-follower are discussed elsewhere[1, 2, 3], only a brief survey is given here.

For a simple circuit model of an emitter-follower (Fig. 1), the output voltage V_o is given by the following equation[3]:

$$V_o(S) = V_g(S) \cdot \frac{S + \omega_o}{R_1 C_o \left[S^2 + S(\omega_o' + \frac{1}{RC_o}) + \frac{\omega_o}{C_o R_1} \right]} , \qquad (1)$$

where

V_g = voltage source

ω_o = α cut-off frequency of the transistor

ω_o' = $\omega_o(1 - \alpha_o)$, α_o = dc (common base) gain

R_1 = base resistance plus source resistance $r_g + r_b'$

R = $1/\left(\frac{1}{R_1} + \frac{1}{R_e}\right)$

R_e = emitter load resistance

C_o = stray output capacitance .

The output voltage is accompanied by oscillatory ringing if

$$\frac{4\omega_o}{R_1 C_o} > \left(\omega_o' + \frac{1}{RC_o}\right)^2 \quad . \tag{2}$$

Equations (1) and (2) show that the instability of an emitter-follower is governed by (a) transistor parameters, (b) driving source impedance, and (c) output loading condition. E. Tammaru's[3] comprehensive report graphically illustrates that the emitter-follower's instability characteristics are governed by five parameters: (a) gain-bandwidth product of the transistor, (b) load resistance, (c) stray output capacity, (d) stray input (base) inductance, and (e) source impedance of the generator plus the base resistance of the transistor. From these parameters, the following conclusion may be drawn: For a given transistor, the instability of an emitter-follower can be reduced by increasing the source impedance and reducing the resistive load impedance. Accordingly, if an emitter-follower is driven by a current source and is loaded by a low impedance transmission line, the instability of the circuit is effectively eliminated.

To have firm logic levels, a tunnel diode is placed between the input current source and the emitter-follower output stage, and the two voltage levels are clamped by the tunnel diode bi-stable regions without saturating or cutting off the input current amplifier stage. During the switching transition, however, the emitter-follower is effectively driven by the high impedance current source. This arrangement, when used in conjunction with a low impedance transmission line, greatly improves the stability of the emitter-follower, even when an extremely high-frequency transistor is employed.

In a practical circuit, a nonsaturated transistor amplifier may be used as the input current source (transistors with high collector impedance are desirable for this purpose). Either the common base or common emitter configuration can be utilized as an input stage; however, only the common emitter configuration is a suitable input stage if more than one fan-out is desired from a single distribution line. In any event, the combination of tunnel diode coupled emitter-follower driven by a nonsaturated current mode amplifier (Fig. 2) is the basic logic circuit configuration adopted. Design analyses of this configuration are given in Section 5.

By using an emitter-follower configuration at the output stage, the outputs of two or more circuits can be connected to implement the OR logic function (with a positive-going logic pulse) with negligible additional delay or signal attenuation (Fig. 2). This wired OR logic was adopted throughout the system.

4.0 UNIVER AND ASSOCIATED LOGIC-GATE CIRCUITS

A multi-logic amplifier circuit based on the tunnel diode coupled emitter-follower configuration was developed and named UNIVER -- universal inverter and register (flip-flop). The basic circuit properties of the UNIVER (Fig. 3) circuit were reported previously[4] and its basic function is that of a set-reset flip-flop which provides complementary outputs. By dividing the basic UNIVER into two identical circuits and modifying the emitter connection of the input stage Fig. 3(b), two independent inverters are obtained. Since this modification is simple, the actual UNIVER circuit module provides additional components for a dual inverter operation. Various applications of a UNIVER circuit module are shown in Fig. 4.

Although the UNIVER configuration was originally developed for a multi-purpose logic amplifier, it can be also adapted to a logic gate circuit. A transistor gate in two configurations (Fig. 5) may be added to the basic UNIVER circuit. In addition to the gating function, the circuit can be used instead of the UNIVER. As a result, the circuits shown in Fig. 5 may be regarded as forming an ideal universal logic set.

Unfortunately, compared to the npn type, the pnp silicon transistor of today is far inferior in very high-speed applications. The circuit shown in Fig. 5(b), therefore, may not be realistic in the desired speed range. For this reason, an alternate approach was taken to replace the pnp type transistor-gated UNIVER (TG UNIVER) for the logic implementation of the AND function. This approach involves a simple backward-diode gate attached to the basic UNIVER inputs (Fig. 6). The signal propagation delay through a high quality backward diode, is less than 0.5 nanosecond. The overall speed of the circuit arrangement (Fig. 6) is comparable to that of the npn type TG UNIVER. A backward diode with low junction capacity and high conductance is necessary for this purpose. Because of the large physical size of the currently available germanium tunnel junction devices, a separate package is required to accommodate the backward diode gate.

Three circuits -- UNIVER, TG UNIVER (with npn transistors), and backward diode gate (BDG) -- are the proposed high-speed logic set that can implement all conceivable logic functions. If "negation" logic is adopted in a system, only one circuit module (TG UNIVER) is required. On the other hand, if negation logic is not employed, two modules, UNIVER and BDG, are satisfactory for a system logic design.

Since the TG UNIVER can be used in the same modes of operation as the UNIVER, the separate module may not be necessary. However, it is economical at present to have the separate UNIVER modules made as both types of modules are being fabricated by a hybrid integration technique. Packaging and system applications of these modules are discussed in Section 6.

5.0 DESIGN ANALYSIS

UNIVER is a current mode switching circuit. Although the circuit configuration is very similar to that of the emitter coupled logic (ECL) or the current mode logic (CML) circuits, the operational characteristic of UNIVER has a definite distinction from them. The most distinctive characteristic of the UNIVER circuit is that the reshaped output signal is completely decoupled from the input signal. Accordingly, ECL circuit analysis[5,6] cannot be applied directly to the UNIVER circuit.

The design analysis is presented in two subsections: DC Analysis (5.1) and High-Frequency Analysis (5.2). The circuit stability against component and parameter variations is considered in the first part, whereas the switching or transient characteristics are determined in the latter part. The major portion of the design analysis deals with the basic UNIVER circuit because the operation of this circuit is fundamental to all other modes of operation.

5.1 DC Analysis

A. Quiescent Point Stability

Since the basic UNIVER is a bi-stable circuit, the establishment of steady operating points must be based on the tunnel diode dc characteristics. Thus, allowable component and power supply tolerances can be determined by dc analysis.

The bias condition of the tunnel diode is shown in Fig. 7. Thus, two tunnel diodes, located at the collectors of the input stage, are normally biased at one of the bi-stable regions. This indicates that before switching, the collectors of the input stage drive a low load (approximately $10 \sim 15$ ohms), or essentially a short circuited load. Since the stage will never be saturated with the normal input voltage swings, the simplified dc equivalent circuit of the UNIVER circuit (Fig. 8) can be used. The use of a silicon transistor in the emitter coupled configuration at a low-power level makes it possible to ignore leakage or drift current components in the equivalent circuit at room temperature operation.

The collector current of the input stage I_{C1} is

$$
\begin{aligned}
I_{C1} &= \alpha_F \cdot I_{E1} \\
&= \alpha_F \cdot I'_{E0}\left(e^{\frac{q}{KT}\phi_{e1}} - 1\right) \\
&= \alpha_F \cdot I'_{E0}\left[e^{\frac{q}{KT}V_{b1} - V_o} - 1\right] \quad , \qquad (3)
\end{aligned}
$$

where α_F is the common base forward current gain; I'_{E0}, saturation current (constant); ϕ_{e1}, the base-emitter junction potential; and V_{b1} and V_o are node voltages at the points shown in Fig. 8.

The voltage at the common emitter junction V_o can be found from the following nonlinear relations:

$$
\begin{aligned}
\frac{V_o + E_1}{R_1} &= I_{E1} + I_{E2} \\
&= I_{E01}\left[e^{\frac{q}{KT}(V_{b1} - V_o)} - 1\right] \\
&\quad + I'_{E02}\left[e^{\frac{q}{KT}(V_{b2} - V_o)} - 1\right] \quad , \qquad (4)
\end{aligned}
$$

since
$$\left.\begin{aligned} V_{b1} &= e_1 - I_{B1}\, r'_{b1} \\ V_{b2} &= e_2 - I_{B2}\, r'_{b2} \end{aligned}\right\} , \tag{5}$$

$$I_{B1,2} = (1 - \alpha_F)\, I_{E1,2} \quad . \tag{6}$$

The relationship between I_{C1} vs e_1, e_2 can be determined by substituting Eqs. (3) and (5) in Eq. (4). The nonlinear relationships in the above equations are due to the nonlinear characteristic of the base emitter-junction current and voltage for large signals. When the base-emitter characteristic is approximated by the following relationship:

$$\begin{aligned} \phi_e &= \frac{KT}{q} \ln\left(\frac{I_E}{I'_{E0}} + 1\right) \\ &\cong V'_{BE} + r_e\, I_E \quad ; \end{aligned} \tag{7}$$

where V'_{BE} is a constant voltage, the base-emitter voltage V_{BE} is then approximated by

$$\begin{aligned} V_{BE} &= V'_{BE} + r_e\, I_E + r_b\, I_B \\ &= V'_{BE} + [r_e + r_b(1 - \alpha_F)] I_E \\ &= V'_{BE} + h_{IB}\, I_E \quad , \end{aligned} \tag{8}$$

and
$$h_{IB} = r_e + r_b(1 - \alpha_F) \quad .$$

From the above relationships, solving for I_{E1} in terms of input voltages e_1 and e_2, and by substituting in Eq. (3),

$$
\begin{aligned}
I_{C1} &= \alpha_F I_{E1} \\
&= \alpha_F \left\{ \frac{E_1 + e_1 - V'_{BE1}}{h_{IB1} + \left(1 + \frac{h_{IB1}}{h_{IB2}}\right) R_1} + \frac{(e_1 - V'_{BE1}) - (e_2 - V'_{BE1})}{h_{IB1} + h_{IB2} + \frac{h_{IB1} h_{IB2}}{R_1}} \right\} \\
&\cong \alpha_F \left\{ \frac{E_1 + e_1 - V'_{BE1}}{h_{IB1} + 2R_1} + \frac{(e_1 - V'_{BE1}) - (e_2 - V'_{BE2})}{h_{IB1} + h_{IB2}} \right\} \quad . \qquad (9)
\end{aligned}
$$

In the bi-stable region, the tunnel diode dc bias current I_d is determined by

$$
I_d = \frac{E_2 - (V_d + E_3)}{R_2} - I_{B3} - I_{C1} \quad , \qquad (10)
$$

where

V_d = tunnel diode dc terminal voltage, and is a function of I_d

E_2, E_3 = power supply voltages

R_2 = bias resistance

I_{C1} = collector current of the input stage

I_{B3} = base current of the output stage.

By substituting the worst case conditions [Eqs. (9) and (10)], the allowable component and supply voltage tolerances can be determined within the given range of the dc tunnel diode bias current I_d.

In the numerical dc analysis of the UNIVER circuit shown in Appendix II, the following steps were taken: First, using Eq. (9) and by substituting worst case conditions, the range of standby dc collector-current I_{C1} variation is determined. This variation of I_{C1} should not offset the dc tunnel diode bias current at either the high or low state. Thus, at high state, the lowest allowable bias current $I_{d1\,min}$, may be set to $1.5\, I_{Vmax}$ (I_V is the valley current of the tunnel diode); then, from Eq. (10) (see Fig. 7),

$$1.5\, I_{Vmax} \le I_{d1\,min} = \frac{E_{2\,min} - (V_{d1\,max} + E_{3\,min})}{R_{2\,max}} - I_{B3\,max} - I_{C1\,max}\,. \quad (11)$$

Second, in the low state, the highest allowable bias current $I_{do\,max}$ may be set to $0.9\, I_{p\,min}$ (I_p is the peak current); then, from Eq. (10) (see Fig. 7),

$$0.9\, I_{p\,min} \ge I_{do\,max} = \frac{E_{2\,max} - (V_{d1\,min} + E_{3\,max})}{R_{2\,min}} - I_{B3\,min} - I_{C1\,min}. \quad (12)$$

If the variation of I_{C1}, which is determined by Eq. (10) at worst case conditions, satisfies Eqs. (11) and (12), then the tunnel diode is biased in a theoretically stable region. As shown in Appendix II, the UNIVER circuit design was based on a most-critical component, and power supply tolerance of ± 5 percent, and a matched input transistor pair. This is a wide permissible tolerance range compared with previously published tunnel diode logic circuitry in this speed range.

The foregoing results were based on the piece-wise linear model of the base-emitter junction. More accurate results may be obtained by machine calculations that use the nonlinear model expressed by Eqs. (3), (4), and (5).

B. DC Transfer Characteristic

The output emitter follower stages of the UNIVER circuit serve as isolation amplifiers so that the tunnel diode bias condition will be affected by a factor of I/h_{FE} times the actual external load variations. The output amplitude, on the other hand, is solely determined by the tunnel diode switching amplitude and there is no direct relationship between input and output signals. Typical dc transfer characteristics of the UNIVER circuit are shown in Fig. 9. As seen, the transition is extremely sharp (typically less than 1 mv) and invariant with temperature variations.

The turn-on transition has an ideal thresholding characteristic as compared with that at the turn-off transition. The broad valley region, characteristic of the tunnel diode is responsible for the gradual fall characteristic during the initial portion of the turn-off transition. In the range of 0 to 100°C, the peak and valley characteristics of a tunnel diode are fairly stable with temperature variation[7] and, accordingly,

the transition characteristic of the UNIVER circuit is negligibly influenced by the ambient temperature change in the same range. The amplitude of the transition is determined by the forward diode characteristic of the tunnel diode and susceptible to the same temperature variations as the regular junction diode. The exceptionally stable reference level seen in Fig. 9 results from the thermal compensation employed in the circuit and as discussed in Section 5.1(C).

The dc trigger level of the UNIVER circuit is typically $40 \sim 60$ mv (Fig. 9). Relatively high dc gain (transconductance, approximately 35×10^{-3} mho typical) is the main contributor to this low trigger level. Although no apparent difficulties were introduced in the system application with this low dc threshold level, it can be improved substantially by using a coupling resistor at the common emitter junction. An example of this improvement is shown in Fig. 10. By using a 100-ohm resistor for the emitter coupling, the dc threshold level is improved from 50 to 200 mv. To keep high-frequency gain characteristics, a bypass capacitor ($10 \sim 20$ pf) is needed, if the required coupling resistor is higher than 75 ohms.

This resistor coupling is not generally needed, but it could improve, not only the dc threshold characteristic, but also the circuit performance in the case of mismatched input transistors. Accordingly, a provision is made in the module for external attachment of the resistor coupling when desired. The transfer characteristics of a UNIVER module with three different coupling resistor values are shown in Fig. 10. A circuit module with a slightly mismatched input transistor pair was selected to demonstrate the improvement offered by increasing the value of the emitter coupling resistor.

The threshold characteristic for an input pulse signal is quite different than that at dc. This characteristic is discussed further in Section 5.2(C).

C. Thermal Compensation

The output dc level of a UNIVER circuit (Fig. 12) can be expressed as

$$E_{o1} = E_3 + V_{d1} - V_{BE3}$$

$$= E_3 + V_{d1}(I_{d1}) - \left[\frac{KT}{q} \ln\left(\frac{I_{E3}}{I_{E0}} + 1\right) + r_{e3}(T)\, I_{E3} + r'_{b3}(T)\, I_{B3}\right]$$

$$= E_3 + V_{d1}(I_{d1}) - [V_{BE3}(T_o) + \theta_T \Delta T] \quad , \tag{13}$$

where $r(T)$ indicates a function of temperature, and θ_T is the temperature coefficient of the base-emitter junction potential.

Thus, the output voltage level is temperature dependent, and the main variation is contributed by the base-emitter junction potential of the output transistor. The typical temperature coefficient (θ_T) of the base-emitter junction voltage of a diffused silicon transistor in the medium current range is approximately -2 mv/^{o}C. If the thermal resistance of output transistor junction to the alumina substrate is taken as 0.25^{o}C/in.^{2}/w, and the transistor chip size as 30-mil square, then, for a continuous 100-mw dissipation, the output stage raises the junction temperature 30°C from the initial value and causes the output voltage level to increase approximately 60 mv. Since the nominal signal amplitude is 0.5 volt, the above level shift is not a desirable one.

When assuming a positive going pulse logic, a small amount of level shift up at the high logic level is not as important as at the reference ground level. This implies that thermal compensation for the long term time-average temperature variation of the package is sufficient for the purpose. From this consideration, a simple but unique temperature compensation scheme was incorporated in the circuit. Thus, the tunnel diode fixed return voltage supply E_3 (Fig. 8), is replaced by a junction diode whose thermal characteristic is similar to that of the base-emitter junction of the output transistor (Fig. 11). The output voltage level can now be rewritten as

$$
\begin{aligned}
E_{o1} &= V_s + V_{d1} - V_{BE3} \\
&= \left[\frac{KT}{q} \ln\left(\frac{I_{d1} + I_{d2}}{I_{so}} + 1\right) + (I_{d1} + I_{d2})\, r_s(T)\right] \\
&= V_{d1}(I_{d1}) - [V_{BE3}(T_o) + \theta_r \cdot \Delta T] \\
&= [V_s(T_o) + \theta_s\, \Delta T'] + V_{d1}(I_{d1}) - [V_{BE3}(T_o) + \theta_T\, \Delta T] \\
&= V_s(T_o) + V_{d1}(I_{d1}) - V_{BE3}(T_o) + \theta_s\, \Delta T' - \theta_T\, \Delta T \quad , \qquad (14)
\end{aligned}
$$

where θ_s is the temperature coefficient of the diode, while $\Delta T'$ is the junction temperature increment at the diode junction.

It is evident that complete thermal compensation may be obtained if thermal junction characteristics and junction temperature variations of the output transistor and that of the diode are equal at a given instant. Although this complete compensation may not be achieved in the practical case, highly effective results were obtained by carefully selecting chip locations, and pad sizes, and specifying the compensation diode junction as the same type as the output transistor base-emitter junction. Some of the experimental oven test results are shown in Fig. 11(b).

As shown in Fig. 11(b), without the compensation diode (with fixed E_3), the low level output voltage is shifting up approximately $1.3 \sim 1.6$ mv/^{o}C, which is close to the thermal coefficient of the base-emitter junction of a silicon transistor. In this condition and at the high level, the shifting rate is much less, approximately 0.6 mv/^{o}C. In this case, the thermal variation of the base-emitter junction of the output transistor is being compensated for by the forward diode characteristic of the tunnel diode. When a compensation diode, which is the base-emitter junction of the same type transistor chip with collector and base connected together is used instead of E_3, the low level is effectively compensated so that only a 5-mv shift is observed for ambient temperature variation of 0 to 80°C (less than 0.06 mv/^{o}C). UNIVER modules with 2N918 and 2N2784 chips were tested and approximately the same results were obtained. At the high level, however, the output voltage level is over-compensated for by the diode so that the level shifts down with increased ambient temperature at a rate of approximately 1 mv/^{o}C. The cause of the over compensation at the high level is the result of the sum of the effect of the compensation

diode plus the forward diode characteristic of the tunnel diode. In practical use, tunnel diodes are mounted well away from the heat source (output transistors) and, therefore, the expected over compensation is much less than that in the oven test.

5.2 High-Frequency Analysis

When all transistors in the UNIVER circuit are operating in a "quasi-linear" amplification mode, the high-frequency analysis can be based on the linear transistor high-frequency model. In the high-frequency equivalent circuit of the basic UNIVER (Fig. 12), the T-equivalent transistor model is chosen for the input stage, and a simplified H model is presented for the emitter-follower output stage. The exact solution for this equivalent circuit is quite involved and, therefore, an extensive analog computer simulation, based on the high-frequency model (Fig. 12), was conducted to supplement circuit analysis. The brief analysis given here, based on the simplified equivalent circuit model, serves for studying the fundamental relationship between the circuit performance and the component parameters.

A. Switching Time Analysis

The major purpose of the high-frequency analysis is to determine the switching characteristics of the circuit with given input conditions and circuit component parameters. Numerical analysis of the switching performance discussed in this report is based on a charge-control analysis. The characteristics of tunnel diode and nonsaturated transistor stages fit into the analysis. For convenience, the analysis is given by dividing the basic UNIVER circuit into two sections: the tunnel diode coupled emitter-follower output stage and the differential-amplifier input stage.

When an input signal voltage is applied to the circuit, the input stage will transfer this signal into an amplified signal current and cause a change in the tunnel-diode bias point from one state to the other. The delay time -- from the moment the input signal is applied to the tunnel diode until switching occurs -- is determined by the high-frequency gain characteristic of the input stage and the required current swing for tunnel diode switching. The rise and fall times of the shaped signal are determined by the tunnel diode characteristic and the loading condition at the node

of the tunnel diode. The shaped signal is then delivered to the load (transmission lines) through the wide-band impedance transformer, the emitter-follower.

(1) High-Frequency Characteristic of the Input Stage

The simplified equivalent circuit of the input stage is shown in Fig. 13. All stray inductive components are omitted; the base-to-emitter diodes are replaced by fixed small signal equivalent components; and the output stages (tunnel diode coupled emitter-followers) are lumped into Z_{K1} and Z_{K2}, which are equivalent loads to the input stage.

When solving for the loop currents in the equivalent circuit as shown in Fig. 13, the tunnel diode driving current or the collector output current of the input stage i_{c1} can be determined in terms of input voltages and transistor parameters.

Since every Z and α is a complex number, the exact solution of the simplified equivalent circuit is quite involved. However, the model may be further simplified to determine the time delay corresponding to the collector current change from the initial bias point [I_o in Fig. 18(b)] to the peak point [I_p in Fig. 18(b)]. During this process, the load on the input stage (Z_K) is fairly low and essentially resistive (approximately $10 \sim 15$ ohms). Accordingly, the capacitive component at this node is negligible. In addition, the input transistors are in matched pairs for dc parameters, and assumed to be matched within a narrow range for high-frequency parameters. Because of the low impedance load, the circuit has a relatively low voltage gain and, therefore, the voltage feedback from the collector to the base is negligible.

From the above considerations, the collector current can be expressed in terms of input voltages as

$$i_{c1} = \frac{e_1\Delta_1 - e_2\Delta_2}{\Delta} \frac{\alpha_1}{1-\alpha_1} , \tag{15}$$

where

$$
\left.
\begin{aligned}
\Delta &= \begin{vmatrix} r_1 + (Z_{e1} + R_1)\dfrac{1}{1-\alpha_1} & \dfrac{R_1}{1-\alpha_2} \\[2ex] \dfrac{R_1}{1-\alpha_1} & r_2 + (Z_{e2} + R_1)\dfrac{1}{1-\alpha_2} \end{vmatrix} \\[2ex]
\Delta_1 &= r_2 + (Z_{e2} + R_1)\frac{1}{1-\alpha_2} \\[2ex]
\Delta_2 &= \frac{R_1}{1-\alpha_2}
\end{aligned}
\right\} \quad , \quad (16)
$$

and the above parameters are defined as

$$
\alpha = \frac{\alpha_o \, e^{-\frac{ms}{\omega_\alpha}}}{1 + \frac{s}{\omega_\alpha}} \cong \frac{\alpha_o}{1 + \frac{s(1+m)}{\omega_\alpha}} = \frac{\alpha_o}{1 + \frac{s}{\omega_t}}
$$

$$
Z_e = \frac{K_T}{qI_e} \, \frac{1 - \frac{ms}{\omega_\alpha}}{1 + \frac{s}{\omega_\alpha}} \cong r_e \, \frac{1}{1 + \frac{s}{\omega_t}}
$$

$$
r = r_b' + r_{ext.} \quad .
$$

If $e_1 \neq 0$ and $e_2 \equiv 0$, then,

$$
i_{c1} = \frac{\alpha_1 e_1}{r_1(1-\alpha_1) + Z_{e1} + Z_2} \quad , \qquad (17)
$$

where

$$
Z_2 = \frac{R_1[r_2(1-\alpha_2) + Z_{e2}]}{r_2(1-\alpha_2) + Z_{e2} + R_1} \quad .
$$

For large R_1, and assuming a matched input pair, Z_2 can be approximated as

$$Z_2 \cong r_2(1-\alpha_2) + Z_{e2} \cong r_1(1-\alpha_1) + Z_{e1} \quad .$$

By substituting this approximation in Eq. (17),

$$i_{c1}(s) = e_1(s) \frac{\alpha_1}{2[r_1(1-\alpha_1) + Z_{e1}]}$$

$$= e_1(s) \frac{\alpha_o \dfrac{\omega_\alpha}{1+\alpha_o m}}{2r_1\left[s + \dfrac{\omega_\alpha}{1+\alpha_o m}\left(\dfrac{r_e}{r_1} + 1 - \alpha_o\right)\right]}$$

$$= e_1(s) \frac{\alpha_o \omega_t}{2r_1\left[s + \omega_t\left(\dfrac{r_e}{r_1} + 1 - \alpha_o\right)\right]}$$

$$= e_1(s) \frac{\alpha_o \omega_t}{2r_1[s + \omega_1]} \quad , \tag{18}$$

where ω_1 is defined as $\omega_t\left(\dfrac{r_e}{r_1} + 1 - \alpha_o\right)$.

From Eq. (18), the time function of i_{c1} can be determined in terms of input voltage e_1. Since the circuit will be driven by the output voltage of the previous stage, it can be expressed as

$$e_1(s) = \frac{E_1 \omega_s}{s(s+\omega_s)} \quad .$$

Thus, it has a finite slope determined by the time constant $1/\omega_s$. By substituting $e_1(s)$ as defined in Eq. (18) and by taking the inverse transform, the time function of $i_{c1}(t)$ can be written as

$$i_{c1}(t) = L^{-1}\left\{\frac{E_1\,\omega_s}{s(s+\omega_s)} \cdot \frac{\alpha_o\,\omega_t}{2_{r1}(s+\omega_1)}\right\}$$

$$= g_m\,E_1\left[1 + \frac{\omega_1}{\omega_s-\omega_1}\,e^{-\omega_s t} - \frac{\omega_s}{\omega_s-\omega_1}\,e^{-\omega_1 t}\right] , \qquad (18a)$$

where $g_m = \dfrac{\alpha_o}{2[r_1(1-\alpha_o)+r_e]}$, the transconductance of the input stage. From Eq. (18a), the stage delay can be determined (time required to trigger tunnel diode) as

$$t_d = \tau_1 \ln \frac{1}{1-\dfrac{\Delta I_{C1}}{g_m\,E_1}} \quad (\text{for } \omega_s >> \omega_1) \qquad (19a)$$

$$\cong \tau_1 \ln \frac{1}{1-\sqrt{\dfrac{\Delta I_{C1}}{g_m\,E_1}}} \quad (\text{for } \omega_s = 2\omega_1) , \qquad (19b)$$

where $\tau_1 = \dfrac{1}{\omega_1}$, $\Delta I_{C1} = I_p - I_o$ or $I_1 - I_V$, the required current swing to trigger the tunnel diode from the steady state bias point.

Eq. (19a) is applicable for a step voltage input. Eq. (19b) is, however, the typical representation of the actual case. Some numerical calculations are shown in Appendix II-B.

(2) Tunnel Diode and Emitter-Follower Switching Characteristics

Since the output impedance of the input stage is relatively high, the switching characteristic of the output stage may be analyzed on the basis of the current driven condition shown in Fig. 14.

The equivalent model of a tunnel diode may be shown as a parallel RC network that neglects the effect of lead inductance in the frequency range of circuit operation. The resistive component of the equivalent model is a variable and is determined by the characteristic curve of the tunnel diode. The node capacitance is also terminal voltage dependent, but can be regarded as a constant for the typical voltage swing here.

Although the emitter-follower is operating in the linear amplification mode and acting as an isolator between the output load and the switching element, the switching performance of the tunnel diode is deteriorated by the output loading because of the limited gain bandwidth of the emitter-follower stage. The actual loading of the tunnel diode can be determined by charge control analysis, and the deterioration of the tunnel diode switching may be interpreted by the charge concept as an additional charge clean-up time for this extra loading.

In a switching circuit, the sum of the charge supplied to a load by the circuit and the charge loss in the circuit at any given period of time is equal to the charge supplied to the circuit by the input driving source during the same period. This relationship can be stated as

$$\int_o^{t_1} i_{in}(t) \cdot dt = Q_L + Q_X$$

$$= \int_{I_{L1}}^{I_{L2}} T_o \cdot dI_L(t) + \int_o^{t_1} i_{CK}(t) \cdot dt \quad . \tag{20}$$

Here Q_L is the charge supplied to the load, and it can be shown that the charge is equal to the product of the load current swing and the effective time constance (or the reciprocal of the gain-bandwidth product) of the circuit. Q_X is the charge loss during the period and is equal to the time integral of the drain or leakage current through the passive components. The relationship shown in Eq. (20) is true regardless of the number of cascade stages involved inside the circuit.

Accordingly, the amount of charge supplied to the emitter-follower (Q_{ef}) during the switching transient can be stated as

$$Q_{ef} = \int_{I_{e1}}^{I_{e2}} T_e \cdot di_{ef} + \int_o^t \frac{q_b}{\tau_e} \cdot dt + \int_{V_2}^{V_1} C_X \cdot dV \quad , \tag{21}$$

where τ_e = minority carrier lifetime in the base and $T_e = \frac{\tau_e}{h_{FE}+1} = \frac{1}{\omega_t}$.

The first term in the right-hand side of Eq. (21) is the base charge required and corresponds to the emitter current increment from the standby current I_{e1} to the full load current I_{e2}. The second term is the recombination charge loss that occurs during the transition, and the third term is the charge loss due to junction capacity and stray capacitances. This Q_{ef} must then be supplied by the input stage to get the desired output current of I_{e2} at the end of the transition. Thus, including Q_{ef} at the tunnel diode node, the switching performance under the output load can be determined.

The charge equivalent circuit of the output circuit of UNIVER is shown in Fig. 14(a). The current source i_{c1} represents the input stage. The tunnel diode is replaced with a parallel RC network, as discussed previously. The capacity C_t represents the sum of the junction capacitance of the tunnel diode and the output capacitance of the input stage; r_d, the tunnel diode internal resistance determined by the characteristic curve; and R_b, the bias resistances R_2 or R_3 (shown in Fig. 12), plus the output resistance of the input stage. The charge load of the emitter-follower circuit is shown by Q_{ef}. Accordingly, the total capacitive load at the tunnel diode node is the sum of C_t plus the equivalent capacity of Q_{ef} at a given voltage swing.

The tunnel diode bias condition is shown in Fig. 14(b). Initially, it is assumed that the tunnel diode is biased at the lower state I_o; and, when a current step is applied by i_s, the bias point A is lifted to $i_s + I_o$, and is forced to transit to the new intersection at point C. During this transition, the charge current i_g is available as indicated in Fig. 14(b). The time required to switch from V_o to V_f is

$$t_r = \int_{V_o}^{V_f} \frac{C_t(V)}{i_g(V)} \cdot dV + \int_o^{Q_{ef}} \frac{dq}{i_g(V)} \quad . \tag{22}$$

Since i_g is a function of the terminal voltage, the exact solution is not simple. A few simplified mathematical models were proposed in the past[8,9]. In a practical

case (for hand calculation), however, the "piece-wise linear approximation"[10] may suffice for the purpose. C_t and Q_{ef}, on the other hand, may be taken as constant values in the range of the tunnel diode switching voltage.

By using the piece-wise linear approximation in conjunction with constant C_t and Q_{ef}, Eq. (22) may be rewritten as

$$t_r = \sum^{n} \left[\frac{(V_{n+1} - V_n)\, C_t + \Delta\, Q_{ef}}{I_g(V_n)} \right] \quad . \tag{23}$$

Now I_g becomes a linear function of voltage at each voltage segment between V_n and V_{n+1}. To obtain a satisfactory result, a typical tunnel diode characteristic may be approximated with 4 to 6 linear segments. An example that uses a 5-segment approximation is shown in Appendix II (Fig. 15), and further simplification may be made because of the slow rising input current source signal due to the limited bandwidth of the input stage. Thus, the time constant of the input stage is much larger than the time constant of the tunnel diode at the segment $A - B$ (Fig. 15), so the time delay from initial voltage V_o to the peak voltage V_P is essentially the propagation delay through input stage t_d. By the same token, the overdrive current Δi (Fig. 15) is time dependent, and is relatively small at the beginning of the tunnel diode switching. Further modification, therefore, is required to simulate the actual case. From results given in Appendix II-B, the total transition time (time required for the output current to reach the desired full load current I_{e2} from the moment that the input voltage step is applied) is

$$\begin{aligned} t_{sr} &= t_{dr} + t_r \\ &= \tau_1 \ln \frac{1}{1 - \dfrac{I_P - I_o}{g_m E_1}} + \sum^{n} \left[\frac{(V_{n+1} - V_n)\, C_t + \Delta\, Q_{ef}}{I_g(V_n)} \right] \\ &\cong \tau_1 \ln \frac{1}{1 - \dfrac{I_P - I_o}{g_m E_1}} + C_t \left[\frac{2(V_K - V_P)}{I_P - I_V} + \frac{V_F - V_K}{I_F - I_V} \right] + \frac{Q_{ef}}{I_F - I_V} \quad . \end{aligned} \tag{24}$$

Similar analysis can be applied to the turn-off period, so that it can be written as (Appendix II)

$$t_{sf} = t_{df} + t_f$$

$$\cong \tau_1 \ln \frac{1}{1 - \frac{I_1 - I_V}{g_m E_1}} + \left(C_t + \frac{Q'_{ef}}{V_1 - V_o}\right)\left[\frac{V_V - V_K}{I_V + I_R} + \frac{V_K - V_P}{I_P - I_V}\right] \quad . \quad (25)$$

The first term of Eq. (24) or (25) is the trigger delay due to the input stage propagation time, the second term is the charge clean-up time at the tunnel diode node, and the third term corresponds to the charge clean-up time for the emitter-follower under loading. Accordingly, t_{dr} and t_{df} represent the initial stage delay for the turn-on and the turn-off period respectively, while t_r and t_f are the corresponding rise and fall times. The average propagation delay measured from the midpoint of the input signal amplitude to the midpoint of the corresponding output edge can be defined as

$$\overline{t_{md}} = \frac{1}{2}\left[t_{dr} + \frac{1}{2} t_r + t_{df} + \frac{1}{2} t_f\right] \quad . \quad (26)$$

In the foregoing discussion, the input signal is assumed to be an ideal voltage step. If it has a finite slope, the initial trigger-delay time will deteriorate, and is expressed as shown in Eq. (19b). The finite slope has no effect on the rise time transition since the tunnel diode generates an approximately fixed amount of charging current after it has been triggered.

Note also that the circuit can be switched from one state to the other with a short duration input pulse. For instance, during the turn-on period, if the collector swing of the input stage is high and long enough for the tunnel diode bias voltage to be moved over to point V_N from initial bias point V_o (Fig. 15), the tunnel diode then switches to the new stable point D, even after removal of the input current. The charge requirement for the guaranteed turn-on switching of the circuit may be stated as

$$Q_{B1m} = \int_{I_o}^{I_P} T_{C1} \cdot di_{c1} + \int_o^{t_d} \frac{dq_{B1}}{\tau_{B1}} + \int_{V_o}^{V_N} C_t \cdot dV + \int_o^{t_d} dQ_{ef}$$

$$\simeq [I_P - I_o](T_{C1} + \delta) + C_t[V_N - V_o] + Q_{ef} \frac{V_N - V_o}{V_F - V_o} \quad . \tag{27}$$

The first term of the right-hand side of Eq. (27) is the required base-charge increment of the input stage transistor corresponding to the collector current swing from I_o to I_P; and T_{C1} is the collector time constant of the input transistor. The second term represents the charge loss in the input transistor during the process and is typically a fraction of the total base-charge stored. The third and fourth terms correspond to the charge required to move the tunnel diode node voltage from V_o to V_N with the load of C_t, node-stray capacitance, and Q_{ef}, the emitter-follower charge load. The charge Q_{B1m} must be supplied by the input stage to switch the tunnel diode. The required duration of the input pulse can be found from

$$\int_o^t i_{B1}(t) \cdot dt = Q_{B1m} \quad ,$$

where i_{B1} is the input base current of the input stage. Thus, Q_{B1m} determines the threshold level of the circuit [Section 5.2(C)].

To summarize: The circuit propagation time is determined by three components: the input stage delay, tunnel diode characteristics (including stray capacities), and the limited bandwidth of the output stage emitter-follower. It is apparent that the fast switching characteristic obtained from UNIVER circuit is due to the extra charging current i_g available from the tunnel diode during the transition. Accordingly, a higher peak current, I_p, and peak-to-valley ratio, I_p/I_V, will implement the faster switching for a given load and stray capacities. On the other hand, the higher the peak current, the higher the input current swing required to trigger the tunnel diode. Consequently, more input stage delay will result. C_t, the stray capacitance at the tunnel diode node, is another key parameter for the switching characteristic. As in the circuit schematic, it is not only contributed by the tunnel

diode junction capacity, but also by the output capacity of the input stage and the input capacity of the emitter-follower stage.

The circuit propagation time of the UNIVER can be optimized by using Eqs. (24), (25), and (27), and the following assumptions are made: (a) circuit is driven by a constant current step, I_{B1}; (b) tunnel diode load line is essentially a constant current load (very high R_2 or R_3) so that $I_o = I_1$; (c) steady state bias point I_o or I_1 is located at the midpoint of the peak-to-valley points $I_1 = I_o = 1/2(I_P - I_V)$; (d) peak-to-valley current ratio I_P/I_V of the tunnel diode is very high; and (e) overdrive current is relatively small, so that $I_F \cong I_P$, or $I_R \cong I_V$.

From Eqs. (21), (24), and (27),

$$t_d \sim \frac{(I_P - I_o)}{I_{B1}} T_{C1} \sim \frac{1}{2} \frac{(I_P - I_V)}{I_{B1}} T_{C1} \sim \frac{1}{2} \frac{I_P}{I_{B1}} T_{C1}$$

$$t_r = C_t \left[2 \frac{V_K - V_P}{I_P - I_V} + \frac{V_F - V_K}{I_F - I_V} \right] + \frac{Q_{ef}}{I_F - I_V}$$

$$\sim C_t \frac{V_S}{I_P - I_V} + \frac{(I_{e2} - I_{e1}) T_{e3}}{I_P - I_V}$$

$$\sim C_t \frac{V_S}{I_P} + \frac{I_L T_{e3}}{I_P} \quad ,$$

where $V_S = V_F - V_o \cong$ the signal amplitude, and $I_L = I_{e2} - I_{e1}$ the output load current.

Then, the total transition time, Eq. (24), can be rewritten as

$$t_s = t_d + t_r$$

$$\sim \frac{1}{2} \frac{I_P}{I_{B1}} T_{C1} + \frac{C_t V_S}{I_P} + \frac{I_L T_{e3}}{I_P} \quad . \tag{28}$$

Taking the derivative of t_s with respect to I_P and setting it equal to zero, the condition for the minimum circuit propagation time can be determined as a function of the tunnel diode peak current I_P. Thus, t_s is minimum when

$$I_P = \sqrt{2 \frac{C_t V_S + I_L T_{e3}}{T_{C1}} I_{B1}} \quad . \tag{29}$$

A similar result may be obtained by substituting the above approximations in Eq. (25). Equation (28) is a very useful expression from which the design optimization can be carried out. Thus, for given input/output transistors, input driving current and output load, the tunnel diode that gives the optimum circuit switching characteristic can be determined. Since the product of the steady state bias current level I_o or I_1 and the switching voltage swing V_S determines the power dissipation of UNIVER during the transition period, and the required bias current level is directly proportional to the peak current of the tunnel diode, the optimized peak current for the minimum stage delay results in the minimum power-delay-time product for the circuit.

Some numerical examples of switching times are shown in Appendix II. As previously mentioned, to study the exact switching behavior of a UNIVER circuit, an extensive analog computer simulation was conducted. The simulations were based on the equivalent circuit shown in Fig. 12, and the results were very accurate. It is planned that complete results of the analog simulation will be published in a separate report, but an example of the typical waveforms obtained from the analog simulation is shown in Fig. 16.

B. Input Impedance and Line Termination

As discussed in Section 1, each circuit input is driven by a terminated transmission line and, normally, more than one input is attached to a line. To avoid signal waveform distortion, it is desirable to have constant effective termination during the transient. Unfortunately, the circuit input impedance is frequency-dependent and, therefore, constant effective termination cannot be maintained in the practical case. If line impedance is very low compared with the circuit impedance at high frequencies, the mismatching problem is minor. On the other hand, the lower the line impedance, the heavier the circuit load is (each output drives at least two

lines to have reasonable fan-outs). With present high-speed transistors (silicon chips), the optimum collector current range lies between 2 to 30 ma (for the maximum gain-bandwidth product). This limits the total load to 17 ohms for a 0.5-volt signal level and is included as signal distribution line loads as well as current sink loads for diode gates. From these considerations, the preferred line impedance level is in the 50- to 100-ohm range. In this case, a 75-ohm line impedance was chosen.

Input impedance of a UNIVER circuit Z_i can be determined from Eqs. (15), (16), and (17) as

$$Z_i = r_1 + Z_{e1} \frac{1}{1-\alpha} + Z_2$$

$$\cong 2r_1 + 2\frac{r_e}{1-\alpha_o} \frac{1}{1 + \frac{s(1+\alpha_o m)}{\omega_\alpha(1-\alpha_o)}} \quad . \tag{30}$$

The equivalent input circuit may be seen in Figs. 12 and 13. Due to the diffusion capacity $C_d = 1/\omega_t(1-\alpha_o) \cdot r_e$, the input impedance could be as low as $2r_1$ at very high frequencies. At steady state, however, the input impedance will be $2r_1 + 2r_e/(1-\alpha_o)$. The finite slope of the input pulse will generally restrict the impedance variation to $2r_e/1-\alpha_o$ or less. The base current response to an input voltage step with a finite rise time can be found from Eq. (30) as

$$i_{B1}(t) = L^{-1}\left[\frac{e_1(s)}{Z_i(s)}\right] = E_1\, h(t)$$

where

$$h(t) = \frac{1}{2r_1}\left[\frac{r_1}{r_1 + \frac{r_e}{1-\alpha_o}} - \frac{\omega_s - \omega_\beta}{\omega_s - \omega_1} e^{-\omega_s t} + \frac{\omega_s}{\omega_s - \omega_1}\frac{\omega_1 - \omega_\beta}{\omega_1} e^{-\omega_1 t}\right] , \tag{31}$$

$$e_1(s) = \frac{E_1}{s(1+\frac{s}{\omega_s}} \quad \text{(input voltage step)}$$

$$\omega_\beta = (1-\alpha_o)\,\omega_t$$

$$\omega_1 = \omega_\beta\left[1+\frac{r_e}{r_1(1-\alpha_o)}\right] = \frac{1}{\tau_1}\ [\text{of Eq. (19)}] \quad .$$

Theoretical base currents with several values of ω_s are plotted in Fig. 17(a). Time of peak response T_P may be found from Eq. (31) as

$$T_P = \frac{1}{\omega_s-\omega_1}\ln\frac{\omega_s-\omega_\beta}{\omega_1-\omega_\beta} \quad . \tag{32}$$

At $t = T_P$, the base current [Eq. (31)] can be found as

$$i_{B1}(t = T_P) = \frac{E_1}{2\left(r_1+\frac{r_e}{1-\alpha_o}\right)}\left[1+\frac{r_e}{r_1(1-\alpha_o)}\,e^{-\omega_1 T_P}\right]$$

$$\cong \frac{E_1}{2r_1}\left[1-\frac{r_e}{r_1}\,\omega_t\,T_P\right] \quad (\text{for } \omega_1 T_P \ll 1) \quad . \tag{33}$$

Since the initial transient duration is $2T_P$, as seen in Fig. 17(a), the effective input impedance during transient may be approximated by taking the time-average value of the input base current during this period so that

$$\overline{Z_1} \cong 4\,r_1\left[1+\frac{r_e}{r_1}\,\omega_t\,T_P\right] \quad . \tag{34}$$

The magnitude of $\overline{Z_1}$ for typical transistor parameter values is approximately 300 ohms, while the steady state input impedance is approximately 1000 ohms. For three input loads (1000/3 ohms steady state), the required external resistor for a 75-ohm termination is 100 ohms. During the transient, the effective termination

may drop to approximately 50 ohms and, accordingly, the line mismatch could be $\Gamma_R = 0.2$; or approximately 20 percent of the signal amplitude may be lost during the initial period of $2T_P (\cong 2\text{nsec})$. As discussed in Section 5.2C, the typical trigger level of a UNIVER circuit for a pulse input is approximately 0.15 volt, or 30 percent of signal amplitude; 20 percent loss of peak signal amplitude has virtually no ill effect on the circuit response. At the same time, a reflected pulse, with an amplitude of $0.2 \times$ signal amplitude and pulse width of $2T_P$, is far under the circuit threshold level. The above analysis implies that a signal distribution scheme using a 75-ohm transmission line with three fan-outs is adequate with the UNIVER type of logic circuit. Use of a 50-ohm line will allow a fan-out of four. A load of two 50-ohm lines, however, should be considered the upper limit of the circuit driving capability. Typical base currents with two different sets of input transistors are shown in Fig. 21(b).

C. Noise Immunity and High-Frequency Transfer Characteristics

The reliable logic decision of a digital circuit requires good noise immunity characteristics. It is a relatively severe requirement in a high-speed digital system where logic circuit sensitivity is rather high, and noise generation sources are abundant. Generally, the wider the circuit bandwidth, the more susceptible it is to noise. Accordingly, the threshold level of a high-speed circuit is normally a compromise between the circuit-switching response and the desired noise immunity.

The noise immunity characteristic of a logic circuit is normally determined by the threshold level of the circuit transfer characteristic. The typical dc transfer characteristic of the UNIVER circuit is shown in Fig. 9. As shown there, the threshold level is determined by the input stage gain and the required collector current swing to trigger the tunnel diode. As seen in Eq. (18), the gain of the input stage is frequency dependent and, therefore, the threshold level is a function of the input signal frequency component. In Fig. 18, typical high-frequency transfer characteristics of the UNIVER circuit are shown along with the dc transfer characteristic. As shown, the threshold level for a pulse input is higher and the slope of the transfer characteristic is more gradual than that at dc. The lower gain of the input stage at high frequencies and the requirement of an extra current to change

the shunt capacitance at the tunnel diode are major reasons. At dc or with a low-frequency input signal (< 50 Mcps), the threshold level of the UNIVER circuit can be determined as follows:

$$E_{1s} = \Delta I_{C1}/g_m$$

$$= \frac{2\left[r_1(1-\alpha_o) + r_e\right]\Delta I_{C1}}{\alpha_o} \quad , \tag{35}$$

where E_{1s} is the threshold input voltage amplitude.

With a narrow input pulse, the threshold level can be found from either Eq. (18) or the condition expressed by Eq. (27). The minimum required charge for switching (Q_{B1m}) must be supplied by the input voltage source, so that

$$Q_{B1m} = \int_o^t i_{B1}(t)\, dt$$

$$= \int_o^t E_{1s} \cdot h(t) \cdot dt \quad , \tag{36}$$

where h(t) is a time function expressed in Eq. (31). It is evident from Eq. (36) that the threshold level is determined not only by the input voltage amplitude, but also by the period of input voltage applied (or input pulse width) and the slope of the input voltage step. Experimental threshold levels of the UNIVER circuit with a narrow input voltage pulse are plotted in Fig. 18(b). As shown, the typical threshold level for a pulse input 3 nanoseconds wide and approximately 0.7 nanosecond rise and fall times (typical clock signal) is approximately 0.15 volt or 30 percent of the nominal signal amplitude of 0.5 volt. For the narrower input pulse, the threshold level is much higher. This implies high noise immunity for spike-like noise, which is the most likely noise form in a high-speed system.

The foregoing analysis and experimental results indicate that the UNIVER circuit with direct emitter coupling at the input stage has sufficiently high noise immunity for a typical high-speed digital system application. However, the noise immunity or threshold level may be raised simply by inserting an external series coupling resistor in the common emitter junction, as discussed in Section 5.1, DC

Analysis. With a given transistor pair, the value of this coupling resistor determines the input stage gain. Consequently, the switching response is also affected. With the use of the coupling resistor, the high-frequency characteristic of the input stage can be varied by a shunt capacitor across the resistor. The threshold characteristics with various combinations of the coupling resistor and capacitor are shown in Fig. 22(b). There, the input pulse width was varied with constant rise and fall slope (approximately 0.7 nanosecond). To have the optimum high-frequency compensation, the time constant of a RC-coupling network must be chosen as equal or slightly larger than that of the input transistor emitter time constant. As previously mentioned, this arrangement also improves the circuit performance in the case of a mismatched front pair.

6.0 CIRCUIT MODULES AND CHARACTERISTICS

6.1 Circuit Module Packaging

More than 150 modules of the UNIVER circuit were made with conventionally packaged components on 0.6-inch square printed circuit cards. As circuit configurations of the modules were confirmed in a high-speed digital system (100 Mcps clock rate)[11], the circuits were made in integrated form.

Monolithic integration was considered unsatisfactory at present because of the circuit's extremely high-speed requirements. Instead, the modules were made in microcircuit form by the hybrid technique (chips on passive substrate). One of the commercially fabricated circuit modules was a 10-lead-TO-5 can package, containing the totally integrated basic UNIVER circuit including tunnel diodes, and the other was a 14-lead, 0.26 x 0.36-in. flat package with or without tunnel diodes (Fig. 19). Screen printing or thin-film vacuum deposition techniques were used to fabricate the passive substrates, and transistors were selected 2N918 or 2N2784 chips.

In addition, two packaging methods were developed for modules in flat packages: one has a completely integrated circuit in a single flat package; and the second, dual flat packages with the transistor and resistor in separate packages

(Fig. 20). Thus, A package contains only transistor chips, while P package accommodates the resistor network. The pin assignments for these two packages are assigned so that when two packages are stacked together and the leads joined, they form the desired circuit configurations. Dual packaging has these advantages: (a) product yield is substantially improved; (b) repairability (transistor or resistor package can be replaced); (c) transistor package can be used for other circuit configurations; and (d) available pins increased.

Modules fabricated by single packaging techniques are convenient to handle, but dual packaging techniques are more economical at present.

6.2 Circuit Module Characteristics and System Logic Implementations

Typical operational characteristics of the three circuit modules -- UNIVER, TG UNIVER, and BD Gate -- are summarized in Table 1. Total stage delay was measured from the midpoint of the input signal amplitude to the midpoint of the output signal amplitude at the corresponding edge. The results are average values based on the results of tests on approximately 150 modules. Component specifications are listed in Appendix I. Typical gain-bandwidth product f_T of the individual transistor chip is in the range of $900 \sim 1300$ Mcps at $V_{CE} = 2v$ and $I_C = 10$ ma, and tunnel diodes are the typical GE TD252A or TD253B (only in some of the TG UNIVER). A special circuit module tester was employed for testing and generating the test signals, and a sampling scope was used to observe the waveforms. Normally, the flip-flop operation of UNIVER or TG UNIVER modules is tested at the set-reset rate of 200 Mcps under a terminated 50-ohm line load (permissible fan-out is 4 with this condition), and the gating function of TG UNIVER modules is tested with a 100-Mcps clock signal at one of the four inputs with a terminated 50-ohm line load. Typical waveforms observed with the test jig are shown in Fig. 21.

Since the BD Gate has no provisions for amplitude restoration nor line drive capability, it must be used with or directly followed by either UNIVER or TG UNIVER. A wide range of logic can be implemented with these combinations. Logic applications shown in Table 2 are a few examples and are by no means exhaustive of the possibilities. As an example, four levels of logic, AND-OR-STORE (FF)-OR, may be obtained by a combination of a BD Gate and a UNIVER with total delay of less

TABLE 1

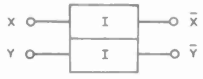
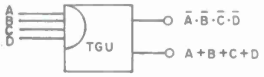
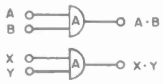
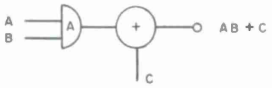
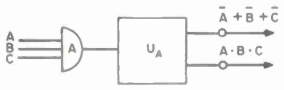
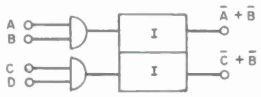
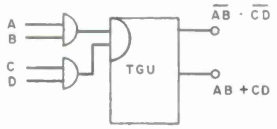
Typical Circuit Module Characteristics

	UNIVER	TG UNIVER	BD Gate
Transition Time[1]			
Rise Time	0.6-0.9 nanosecond	0.8-1.0 nanosecond	
Fall Time	0.8-1.0 nanosecond	0.9-1.1 nanosecond	
Total Stage Delay[1,2]	0.7-1.0 nanosecond	0.9-1.2 nanosecond	0.3[4)]-0.6[5)] nanosecond
Output Amplitude[1]	0.45-0.55 v	0.45-0.55 v	
Noise Threshold[1,3]	0.18-0.22 v	0.2-0.25 v	0.05 v
Fan-in		4	4
Max Load	25 Ω	25 Ω	UNIVER or TG UNIVER input
Fan-out[6]	8 max/output	8 max/output	
Power Supply Regulation	± 5%	± 5%	

1. All tests with a terminated 50-Ω line load at each output.
2. Time measured from the midpoint of input pulse to the midpoint of the corresponding output edge.
3. An input pulse of approximately 2-nanoseconds width.
4. AND function only.
5. AND followed by OR function.
6. Number of permissible inputs to be attached at the termination points when the output circuit is driving two 50-ohm lines.

TABLE 2

TYPICAL LOGIC IMPLEMENTATIONS BY UNIVER, TG UNIVER, AND BD GATE MODULES

Circuit Module Type	Typical Logic Applications	Symbols	Note
UNIVER	Set-Reset Flip-Flop		1. Output may be wired in to the other module output to perform additional OR function (up to 4 outputs). 2. With the amplifier mode, a delay feedback path must be provided from F output to R input.
	Amplifier with Complementary Outputs		
	Dual Inverters		
TG UNIVER	Can be used as a UNIVER		
	NOR/OR Gate		
BD Gate	Dual 2-input AND Gate		To be used by attaching the output to an unterminated UNIVER or TG UNIVER input.
	4-input AND Gate		
	AND – OR Gate		
BD Gate plus UNIVER	AND/NAND Gate		
	Dual NAND Gate		
BD Gate plus TG UNIVER	AND – NOR/OR Gate		

than 1.6 nanoseconds. This example shows that a shift register with provisions for parallel word-to-serial word conversion can be shifted reliably up to a 250-Mcps clock rate (Fig. 22). Another example is shown in Fig. 22(c) where the Exclusive OR function is obtained by a combination of a BD Gate and a TG UNIVER. The typical delay for this function is approximately 1.8 nanoseconds, so that full binary addition can be obtained under 4 nanoseconds with provisions for complementary outputs for both "full-sum" and "carry" outputs. A total addition time of a 64-bit parallel adder with full anticipated carry (three levels) configuration may be expected within 15 nanoseconds for the above combination.

A prime objective in developing this logic set was to provide a basic building block in a high-speed special arithmetic unit. The first experimental test assembly (built with hybrid integrated circuit modules) is a 10-bit serial-parallel multiplier capable of executing 10-bit multiplication within 200 nanoseconds at a 100-Mcps clock rate. The assembly includes most classes of logic functions that might be encountered in a full scale general purpose arithmetic unit. Some experimental results of the sublogic sections of the assembly are shown in Fig. 22.

7.0 CONCLUSION

A universal inverter and register (UNIVER), (fast logic circuit to be used with low impedance transmission signal distribution lines) was analyzed, and the basic circuit behavior was characterized so that the circuit module could be fabricated in microcircuit forms by commercial manufacturers. The analysis showed that by using a tunnel diode in the bi-stable mode of operation in conjunction with nonsaturated current mode transistor operation, the following characteristics could be provided: (a) allowable component tolerance is relaxed; (b) transfer characteristic is sharp and invariant to the temperature change; (c) effective immunity is obtained; (d) most efficient switching is achieved; and (e) multiple logic functions can be performed. Optimization of the circuit characteristic was shown to be dependent

on the choice of the proper tunnel diode for given transistors and load. From the transition time analysis, the condition for the minimum total circuit-delay was derived and, from this result, the design optimization was carried out. Transition time of the UNIVER circuit is limited only by the forward gain-bandwidth product of the active devices and, therefore, the switching characteristic can be determined relatively simply and rather precisely for given active device parameters. Consequently, the transition time of the UNIVER circuit will be improved as higher speed active components become available in the future.

The extremely fast switching capability of the UNIVER circuit is due to regeneration of the charging current from the tunnel diode during the switching process. Since power dissipation in the tunnel diode is negligibly small, the addition of a tunnel diode improves the power-delay-time product of the nonsaturated transistor-switching circuit substantially. Thus, while the UNIVER configuration was developed primarily for a high-speed medium power application, it is also suitable for micro-power applications. For instance, by using 2N3493 transistors and 1N4090 tunnel diodes (I_p = 160 μa) in the UNIVER configuration, a flip-flop operation, with a 10-nanosecond propagation delay at 300-μw total power dissipation, was obtained. The lower power operation is feasible, but limited by the unavailability of a lower peak current tunnel diode with a good peak-to-valley ratio.

The UNIVER circuit (except for its tunnel diodes) can be fabricated by a monolithic integration technique. Because of the isolation problem in the silicon dioxide layer, the speed of the circuit module fabricated by present monolithin integration methods cannot reach the speed obtained by circuits made by hybrid integration techniques. A substantial improvement in switching speed of a monolithic circuit can be gained by altering it to a UNIVER configuration. For example, by adding tunnel diodes externally to commercially available ECL modules (monolithic integrated) to form a UNIVER circuit, the switching time can be speeded up by a factor of two or three so that the expected switching time is within 2 to 4 nanoseconds.

By using the UNIVER circuit module in an experimental high-speed arithmetic unit, it has been shown that a flexible, reliable, and versatile sub-nanosecond universal logic circuit can now be made by commercial manufacturers.

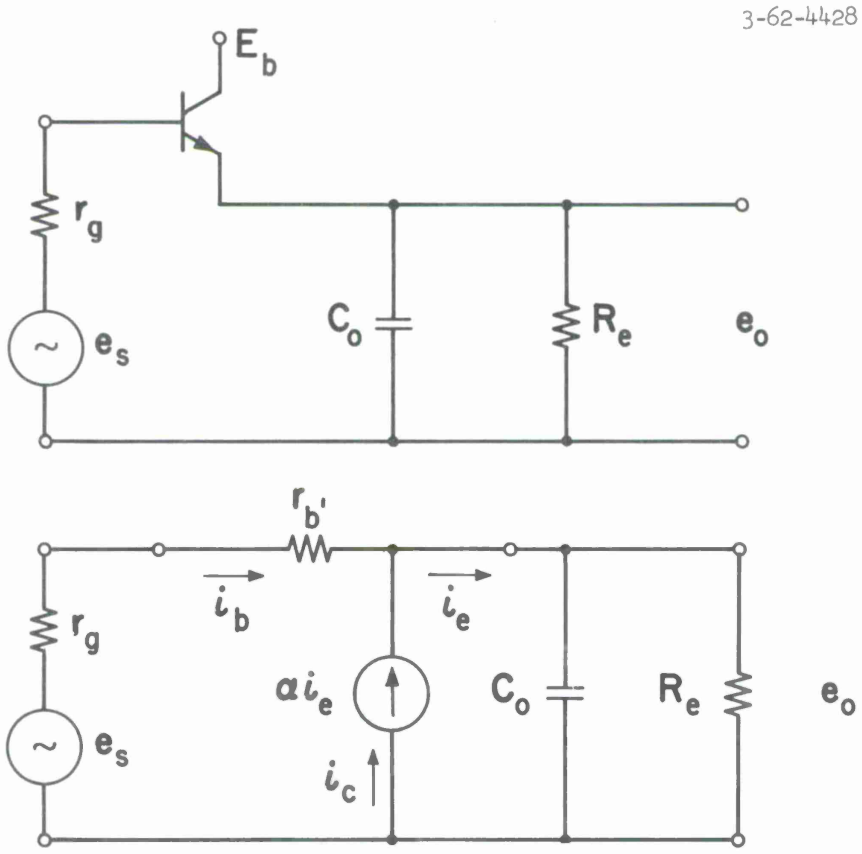


Fig. 1. Emitter-follower circuit and ac equivalent model.

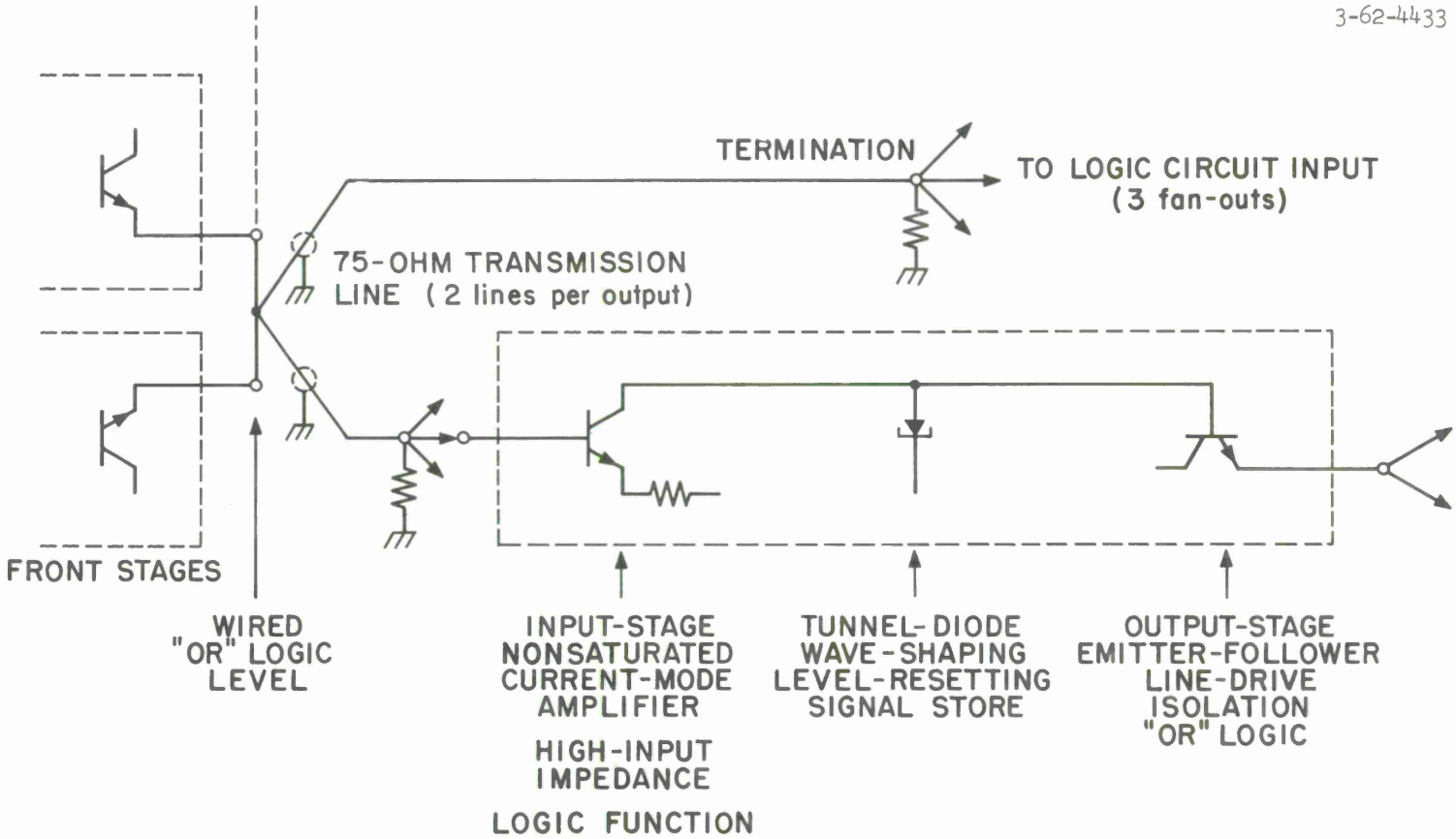
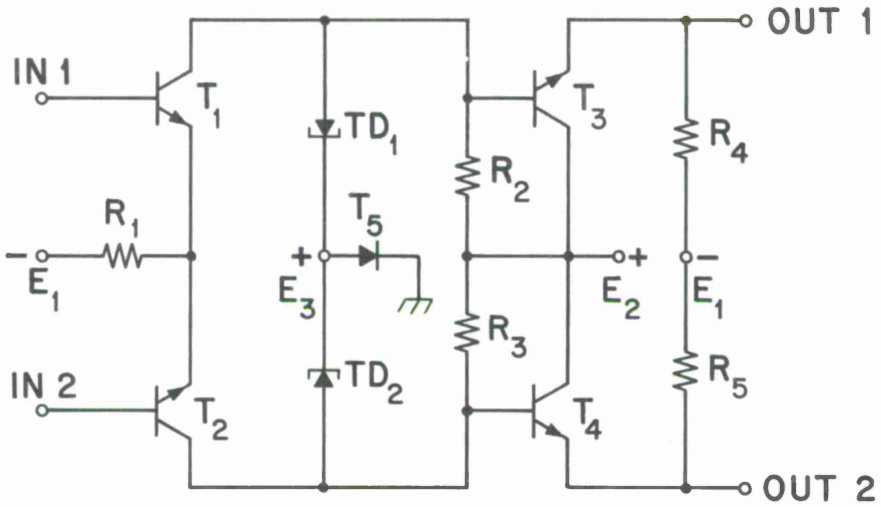


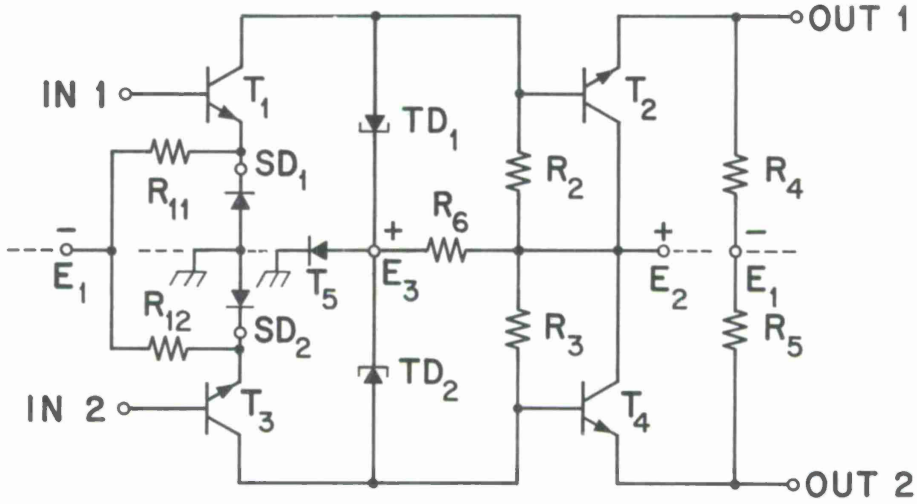
Fig. 2. Basic logic circuit configuration associated with transmission line signal distribution system.

3-62-4431



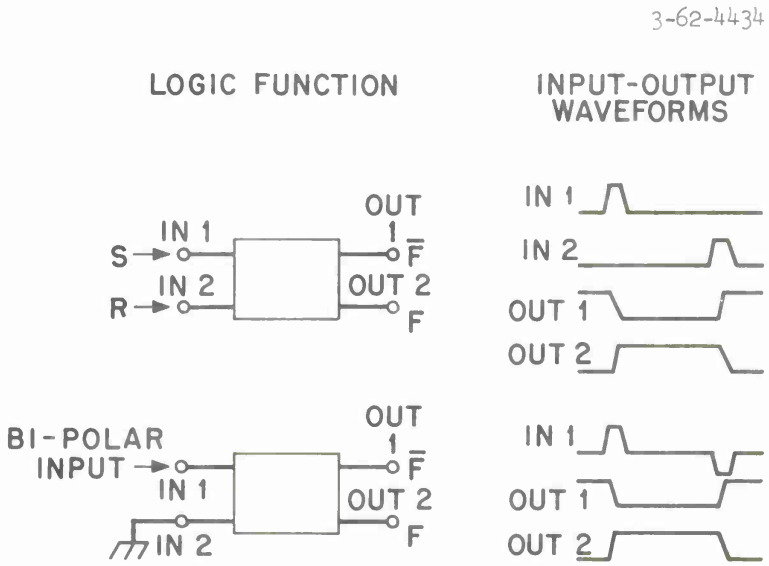
(a) UNIVER as a set-reset flip-flop or complementary output amplifier.

3-62-4432

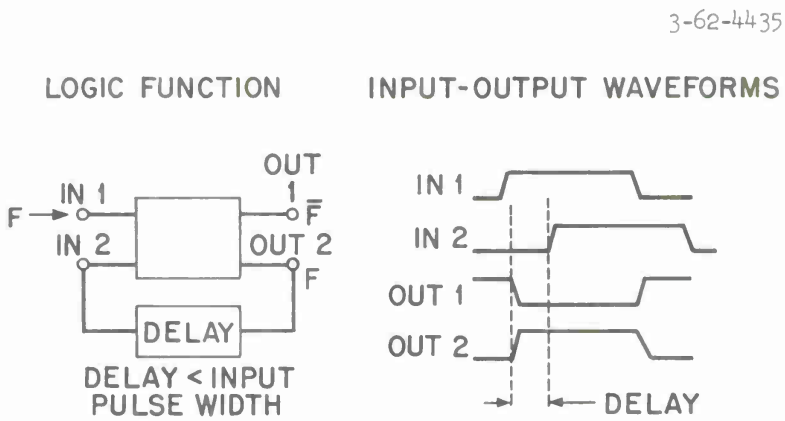


(b) UNIVER as dual inverters.

Fig. 3. Basic UNIVER circuit configuration.



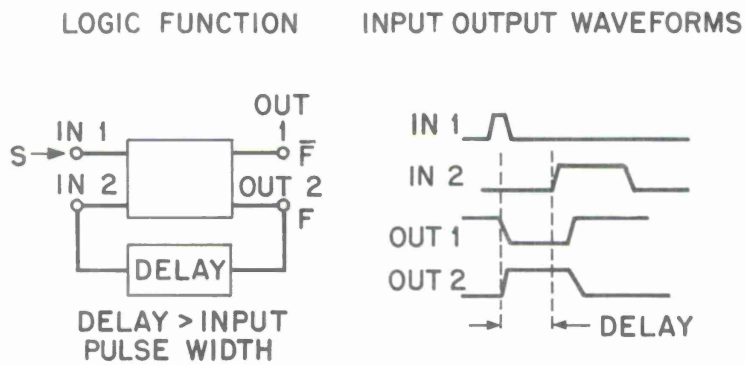
(a) Set-reset flip-flop (basic operation).



(b) Complementary output amplifier.

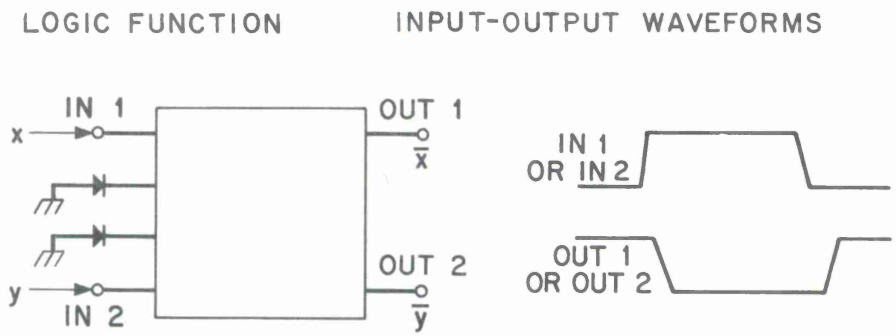
Fig. 4. Various logic functions implemented by the basic UNIVER circuit.

3-62-4435(b)



(c) Monostable or pulse width stretcher.

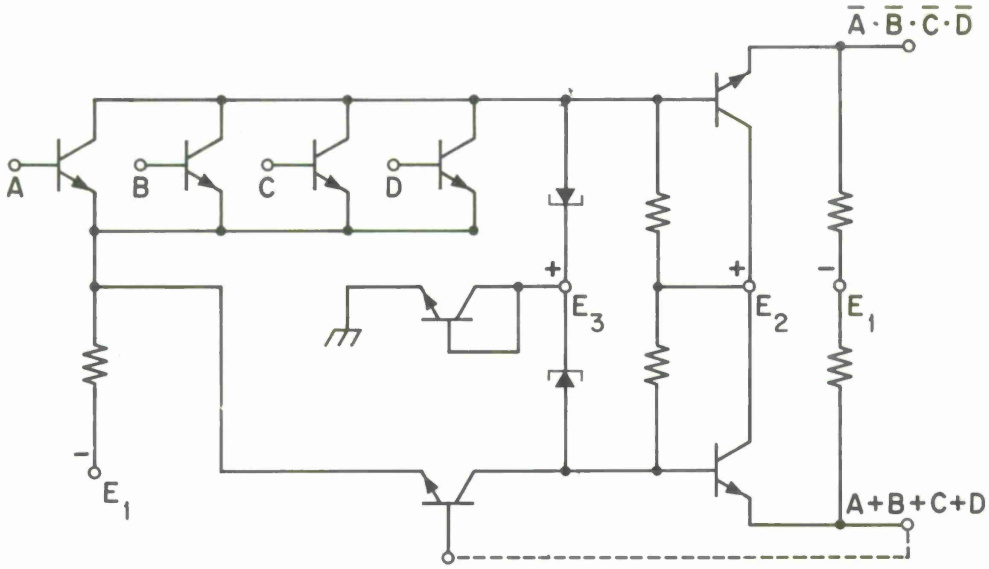
3-62-4436



(d) Dual inverters.

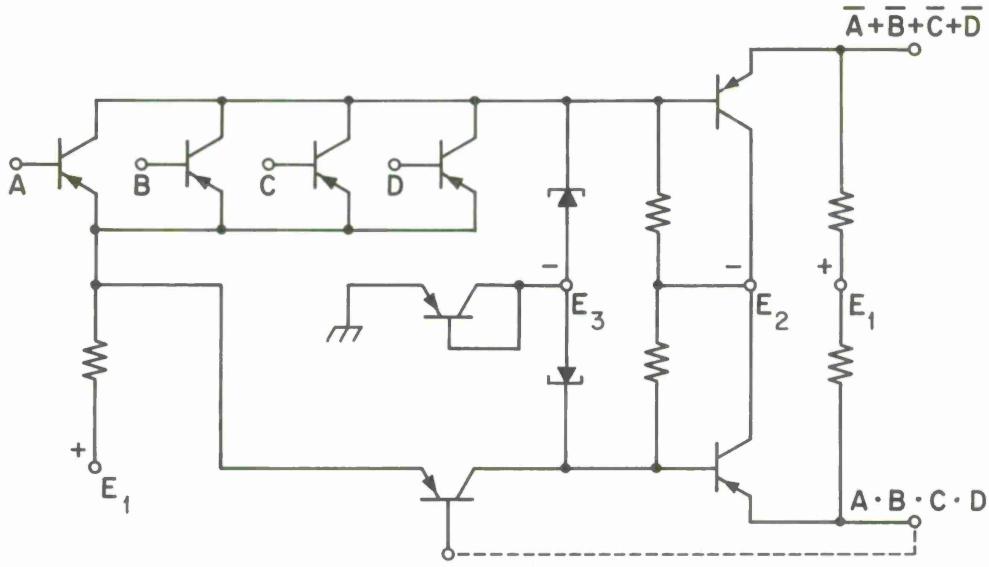
Fig. 4 Cont.

3-62-4429



(a) NPN transistor TG UNIVER.

3-62-4430



(b) PNP transistor TG UNIVER.

Fig. 5. Transistor-gated UNIVER circuit.

3-62-4427

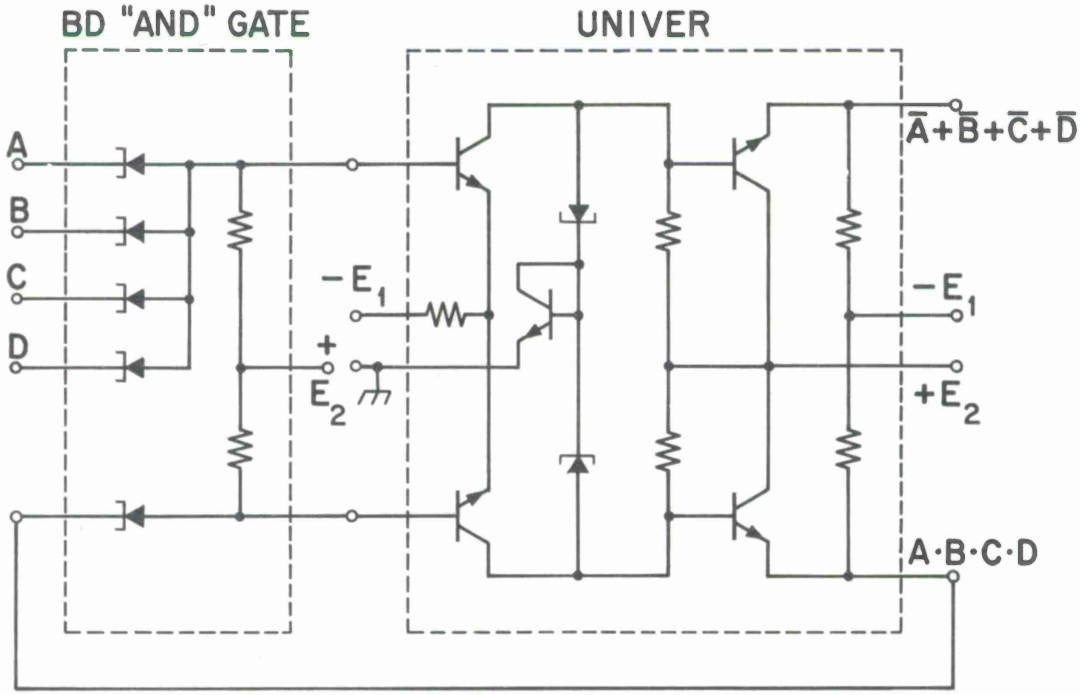


Fig. 6. "AND" logic function implemented by backward diode gate and UNIVER modules.

3-62-4417

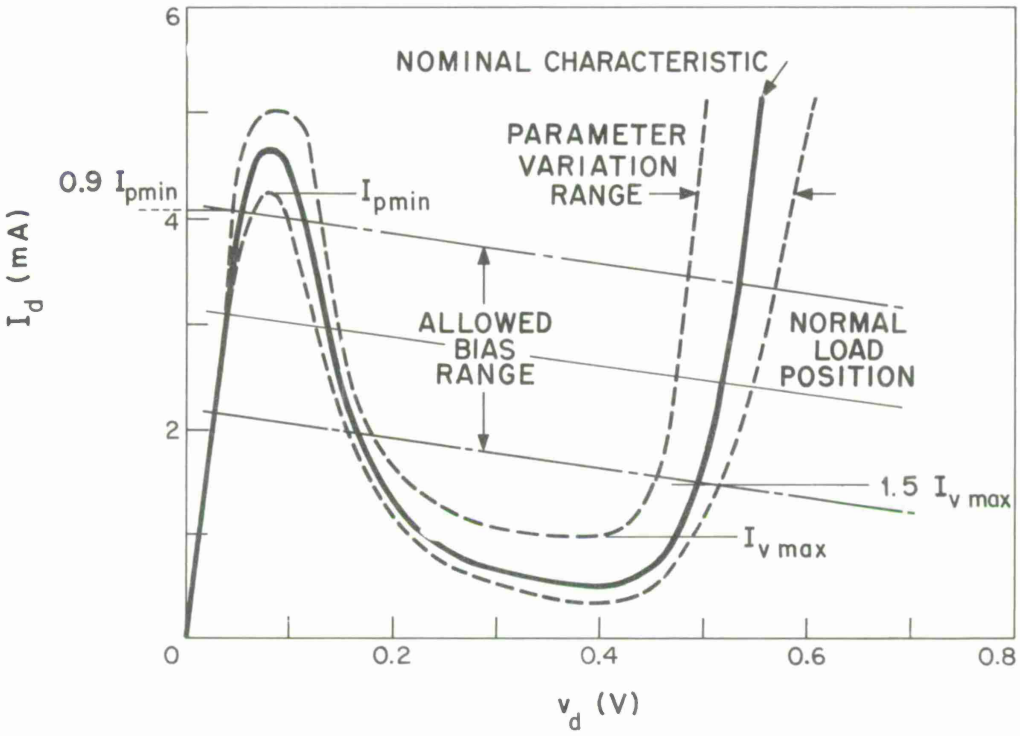


Fig. 7. Typical 4.7-ma peak current tunnel diode dc characteristic and allowed bias conditions in the UNIVER circuit.

3-62-4415

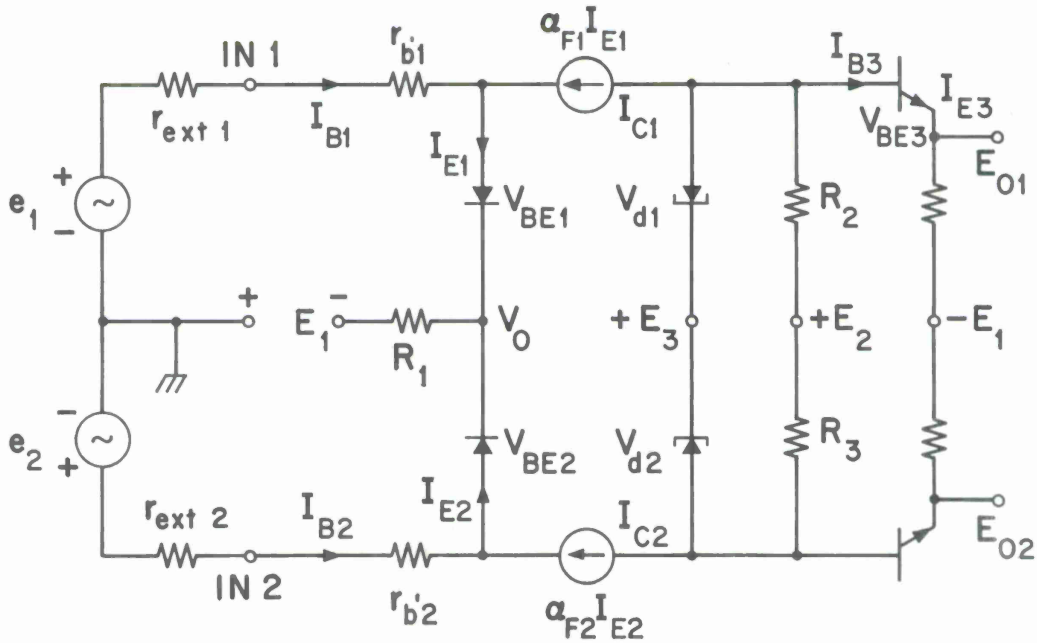


Fig. 8. Simplified dc equivalent model of UNIVER input stage.

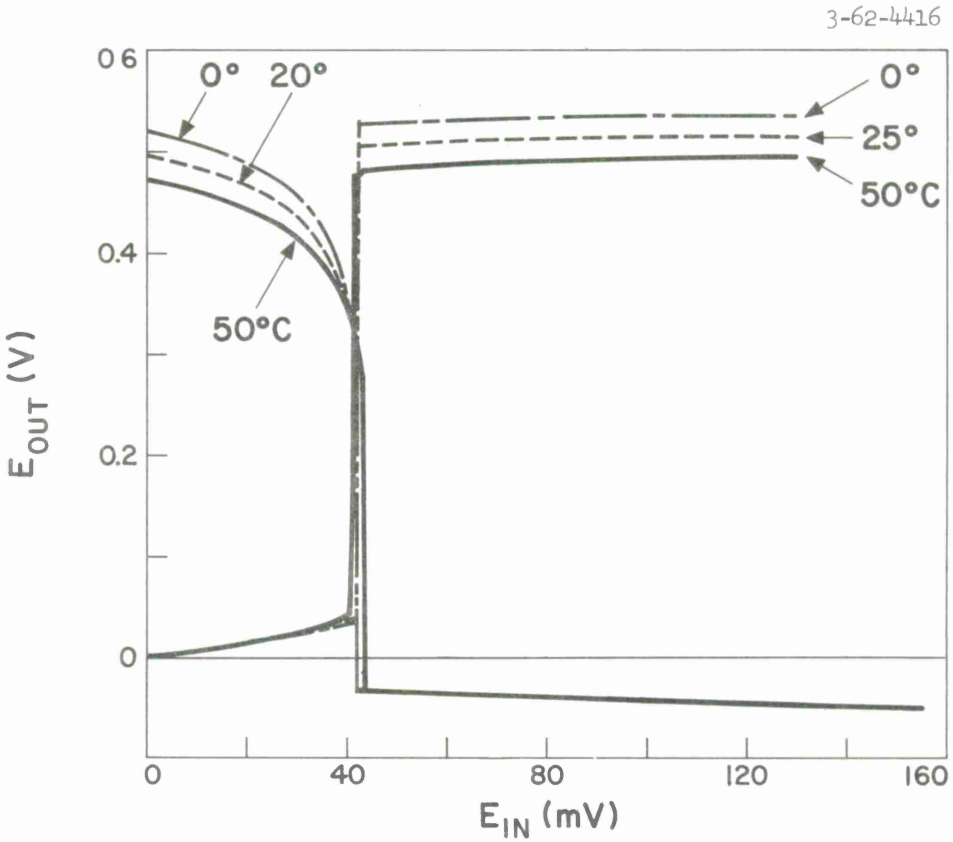
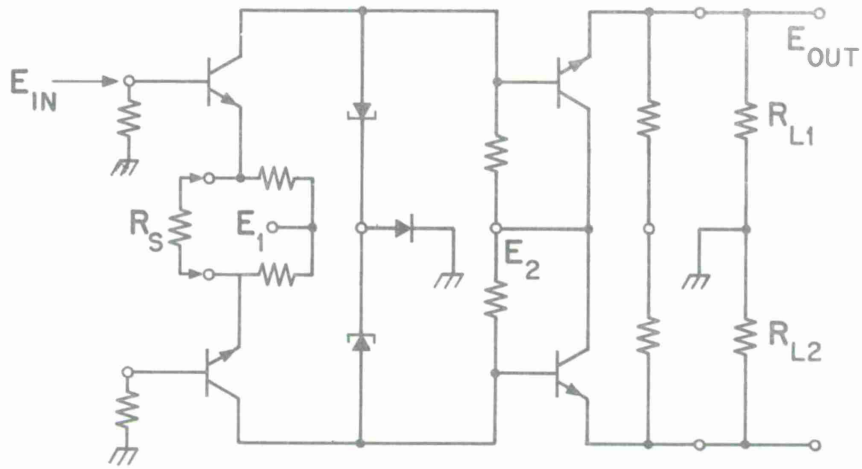


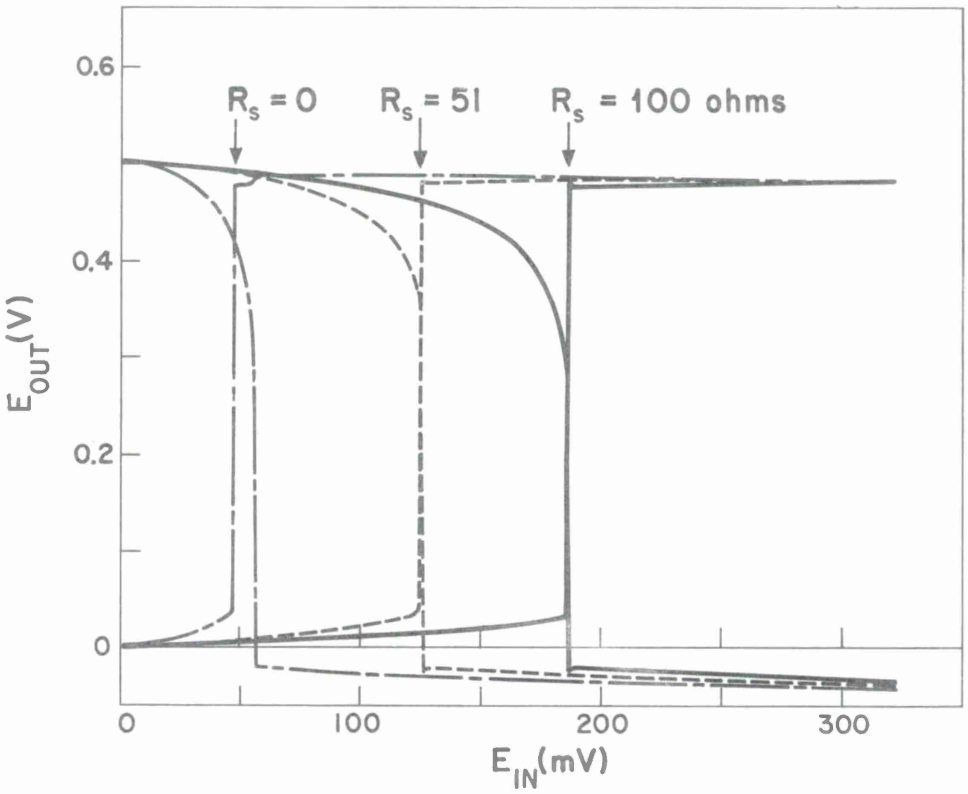
Fig. 9. Typical dc transfer characteristic of UNIVER circuit.

3-62-4413



(a) Circuit schematic with series emitter coupling resistor.

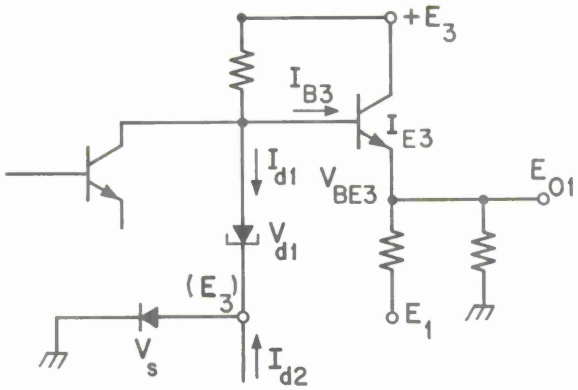
3-62-4414



(b) Transfer characteristics at room temperature.

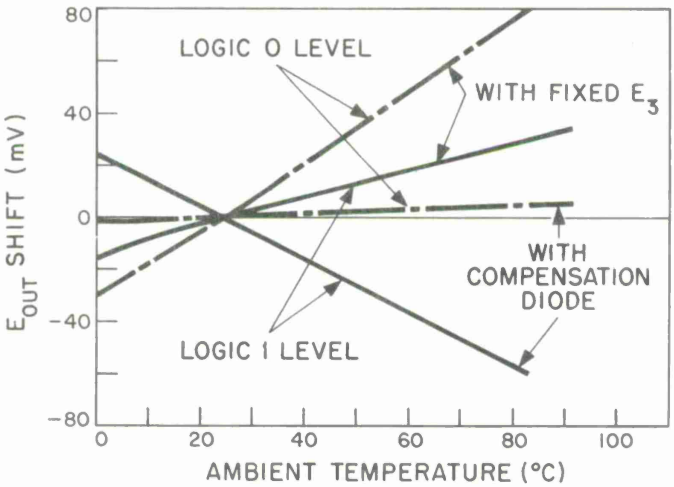
Fig. 10. DC transfer characteristics of UNIVER circuit with series emitter coupling resistors.

3-62-4410



(a) Circuit schematic with thermal compensation diode (V_s).

3-62-4412



(b) Variations of output voltage level against ambient temperature change. Normalized at 25°C.

Fig. 11. Thermal characteristic of output voltage levels in UNIVER circuit.

3-62-4437

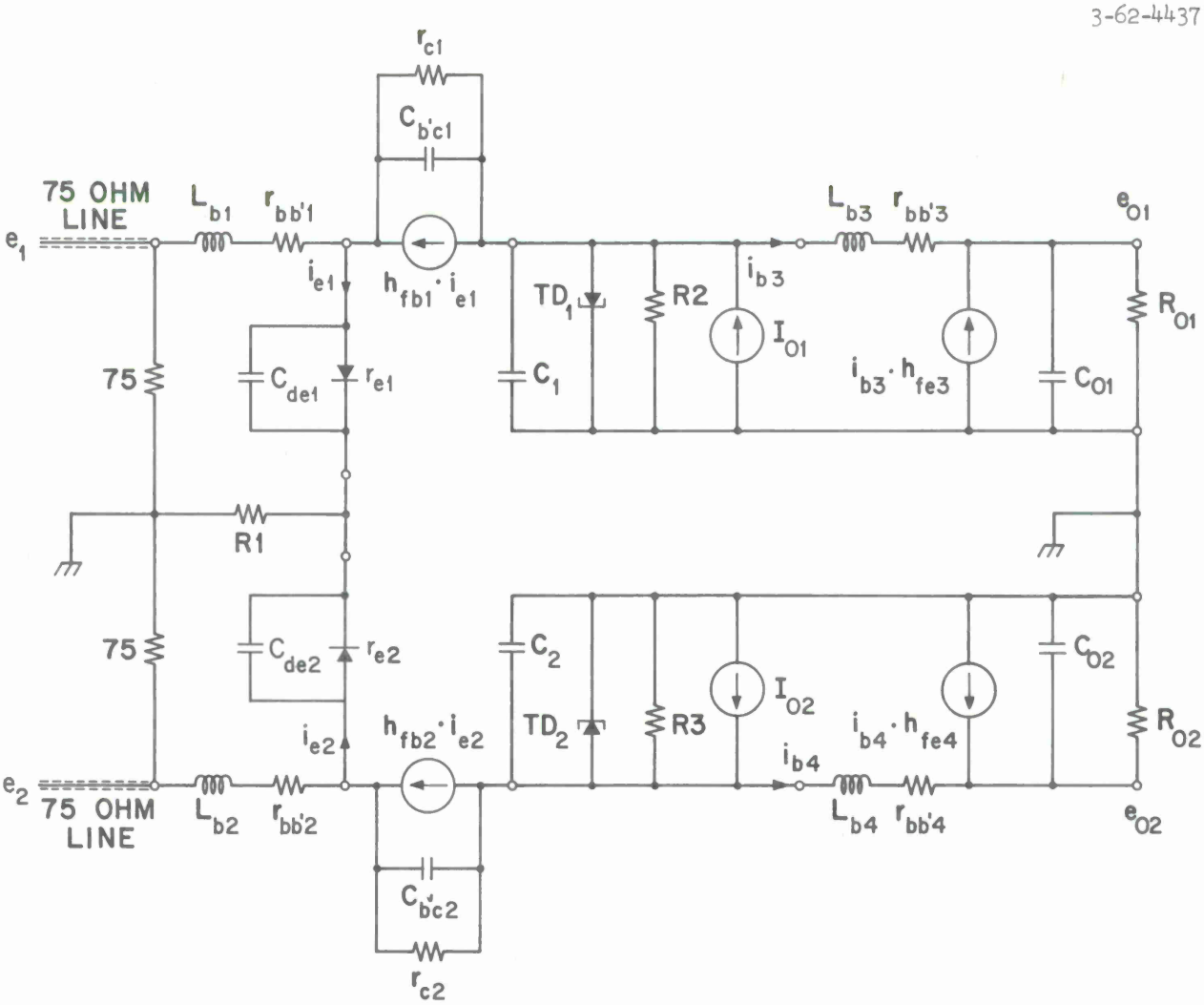


Fig. 12. High-frequency model of UNIVER circuit.

3-62-4409

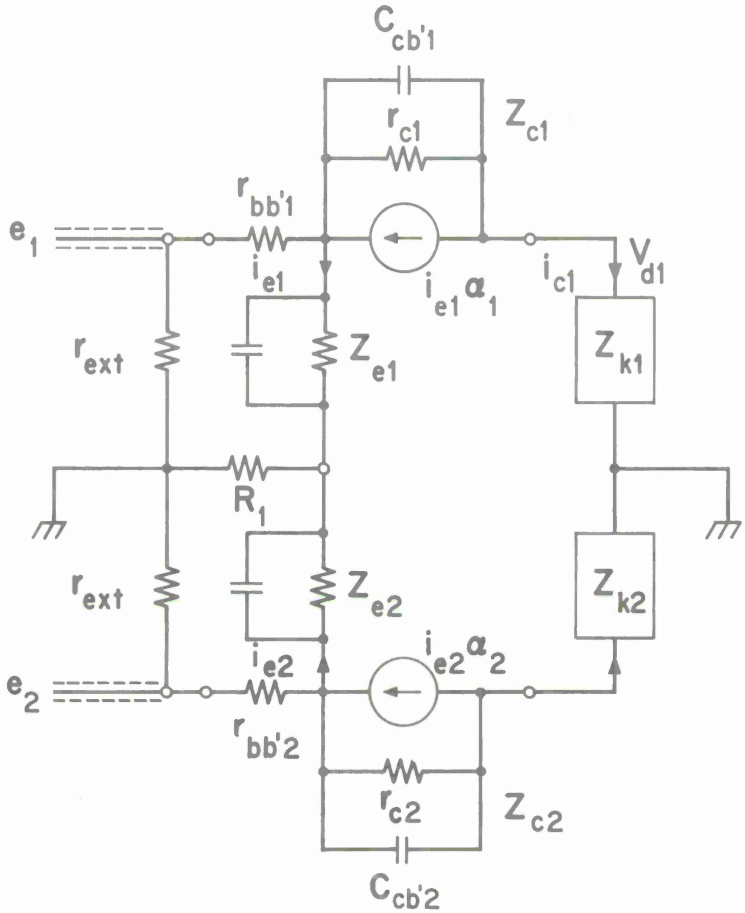
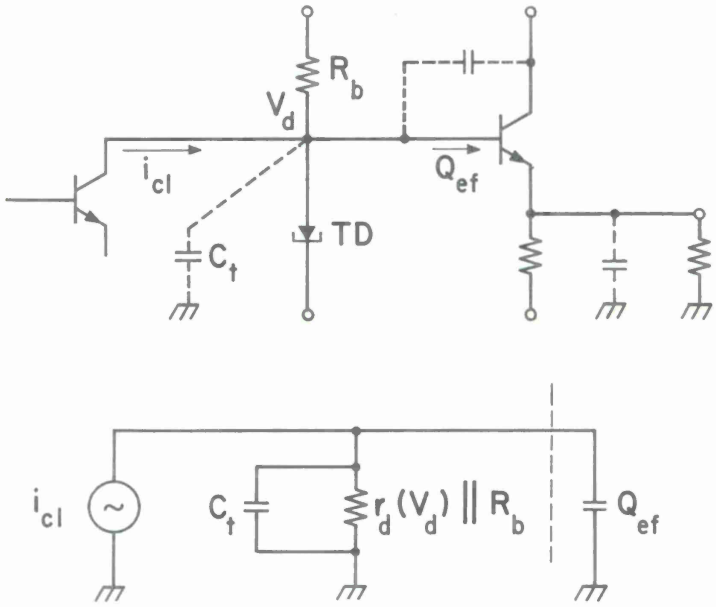


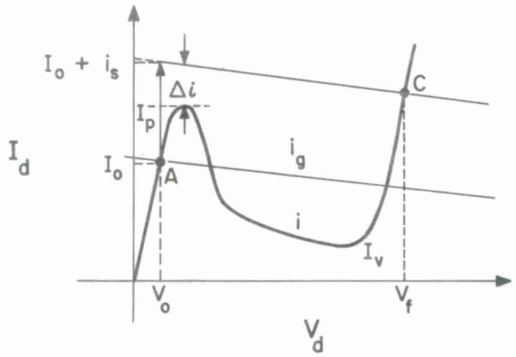
Fig. 13. Simplified high-frequency equivalent model of UNIVER input stage.

3-62-4407



(a) Charge-control model applied to the output stage of UNIVER circuit.

3-62-4408



(b) Charging current available from current steered tunnel-diode switch.

Fig. 14. Charge-control model of UNIVER output stage and charging current generated by tunnel diode during switching process.

3-62-4406

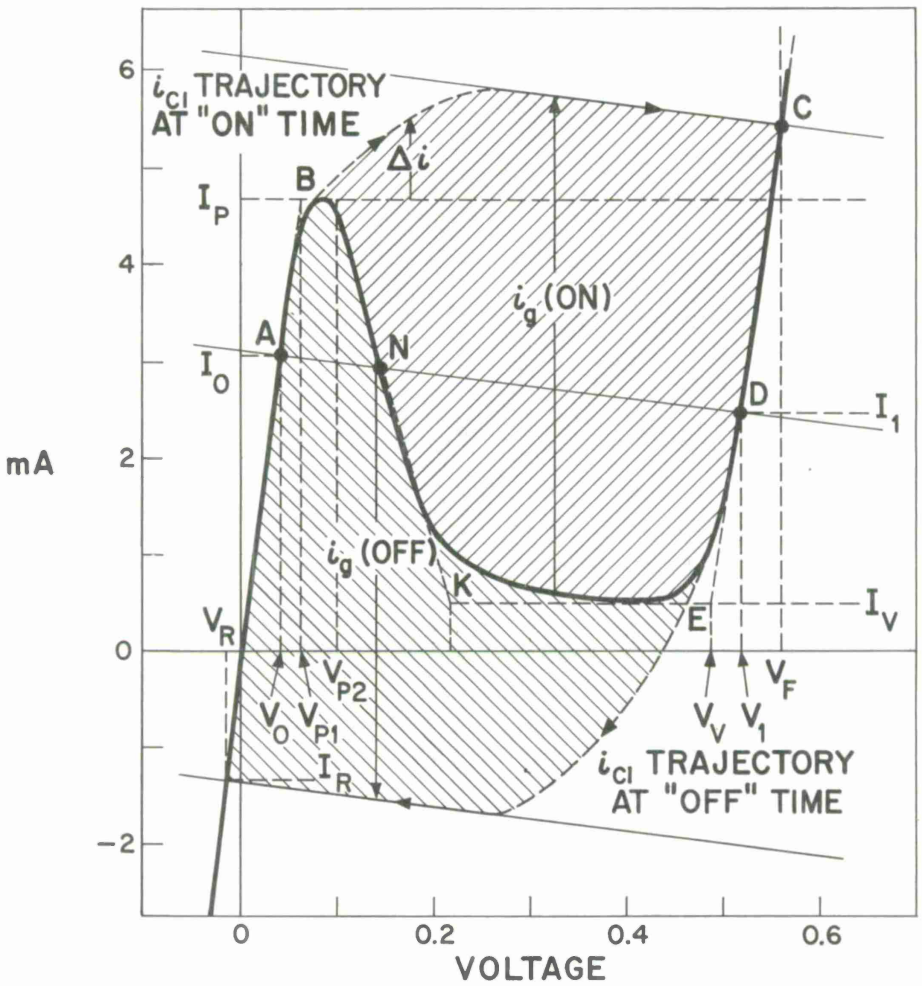


Fig. 15. Locus of tunnel diode switching process in UNIVER circuit.

3-62-4405

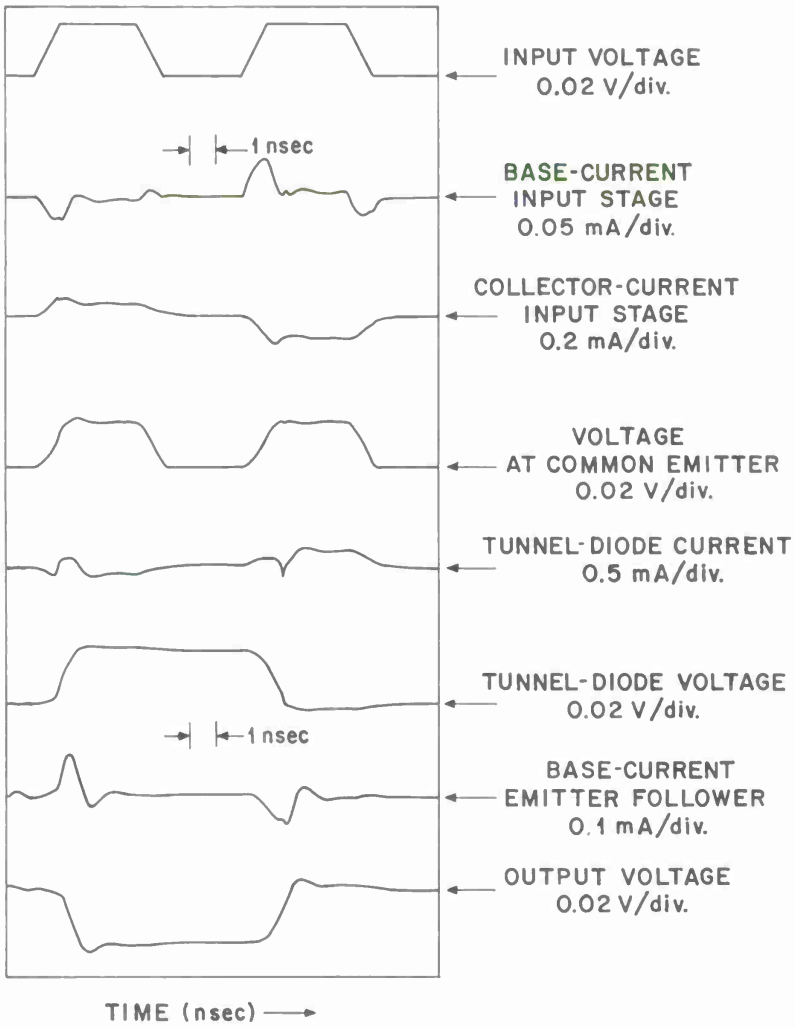
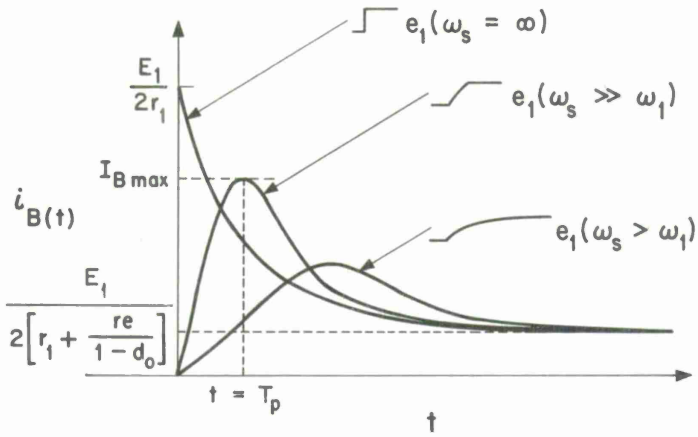


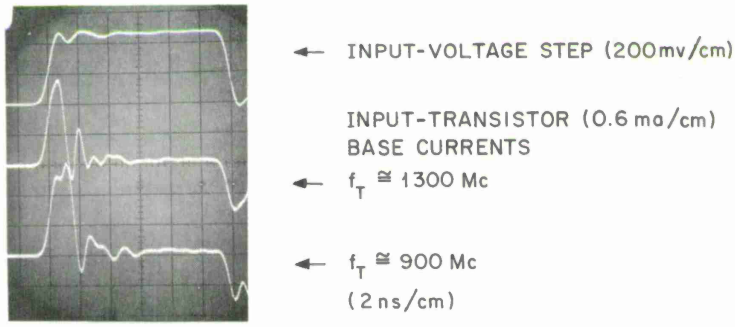
Fig. 16. Waveforms obtained by analog computer simulation.

3-62-4404



(a) Input base current as a time function of input-voltage step rise time.

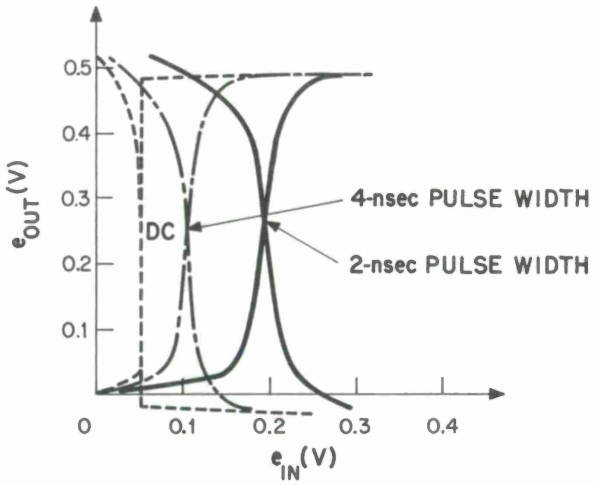
3-62-4401



(b) Experimental base currents with different cutoff frequencies of input transistor pairs.

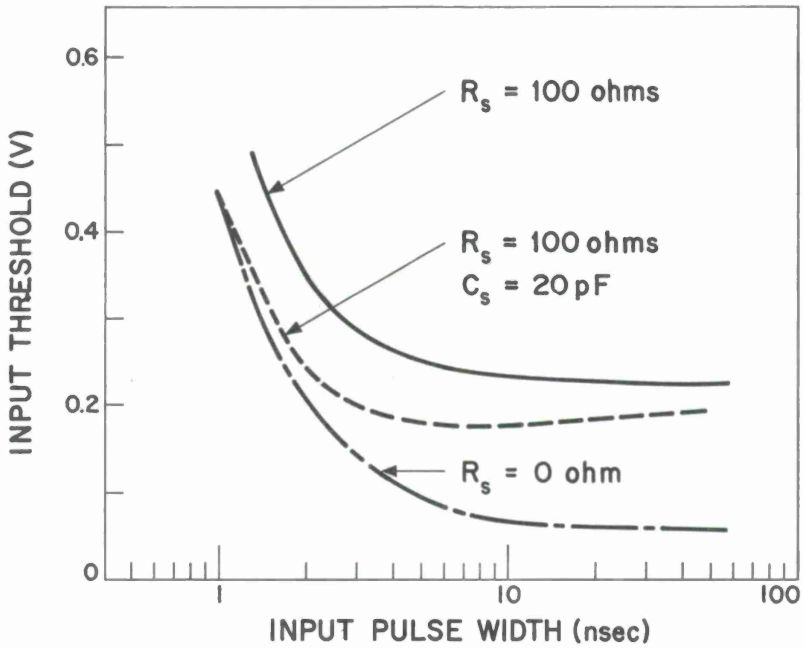
Fig. 17. Input base current transient.

3-62-4400



(a) Typical transfer characteristics with pulse inputs.

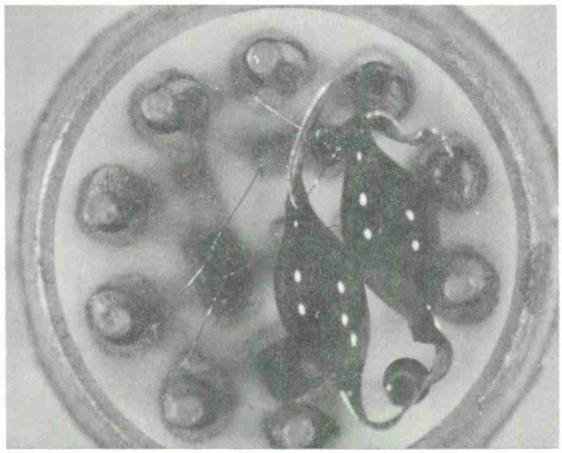
3-62-4402



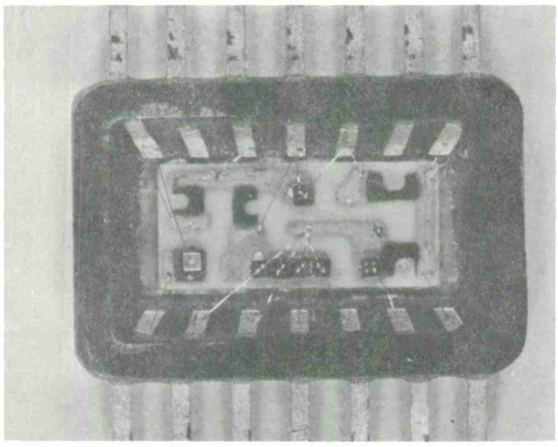
(b) Threshold voltage vs input-pulse width.

Fig. 18. High-frequency threshold characteristics of UNIVER circuit.

3-62-4062



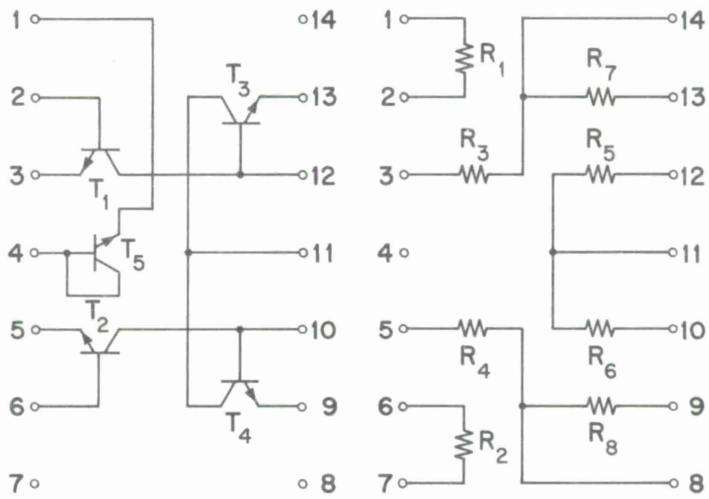
(a) UNIVER in TO-5 package including tunnel diode pair.



(b) TG UNIVER in 14-lead flat package excluding tunnel-diode pair.

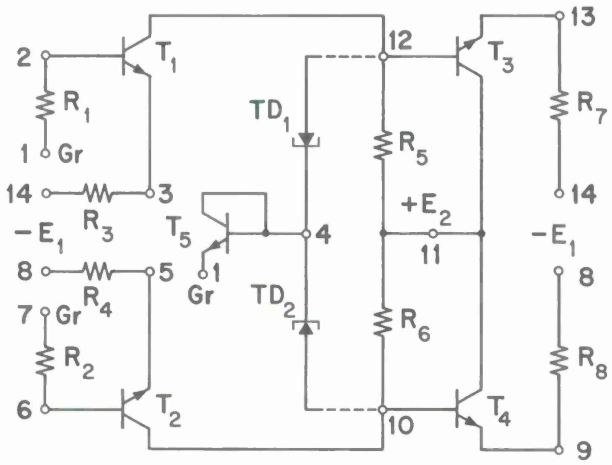
Fig. 19. Internal views of UNIVER circuit modules fabricated by hybrid integration technique.

3-62-4425



(a) Internal circuit layout of A-pack transistor package and P-pack resistor package.

3-62-4426

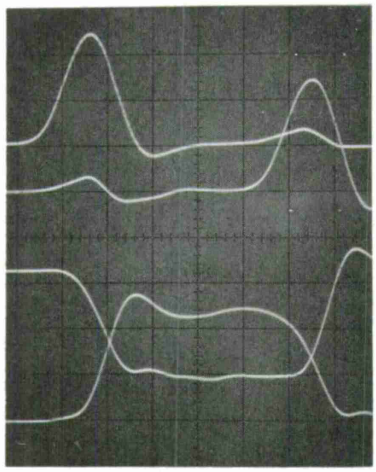


(TD1 and TD2 attached externally)

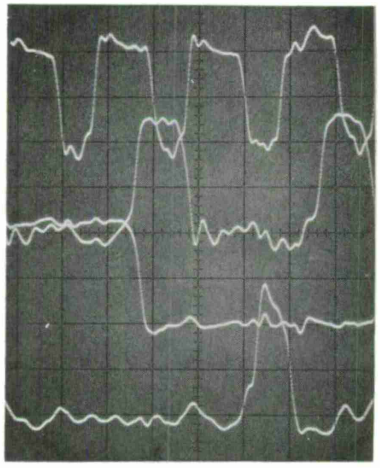
(b) Stacking A and P packages together completes desired UNIVER circuit configuration. TD_1 and TD_2 are attached externally.

Fig. 20. UNIVER module made by dual 14-lead flat package.

-62-4061



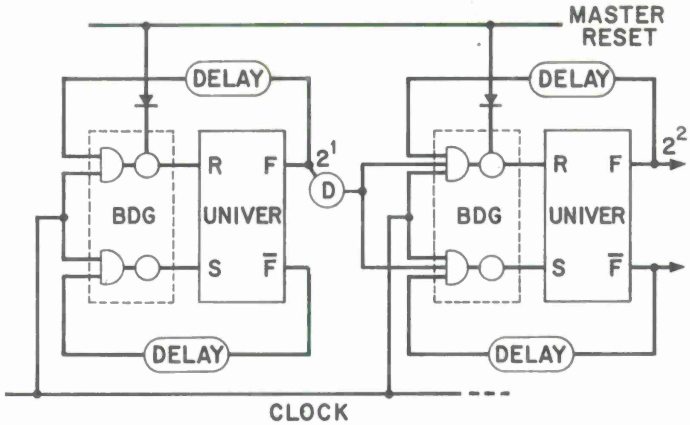
(a) Time response of flip-flop operation of typical UNIVER module. Modules are tested with 200 Mcps set-reset rate.



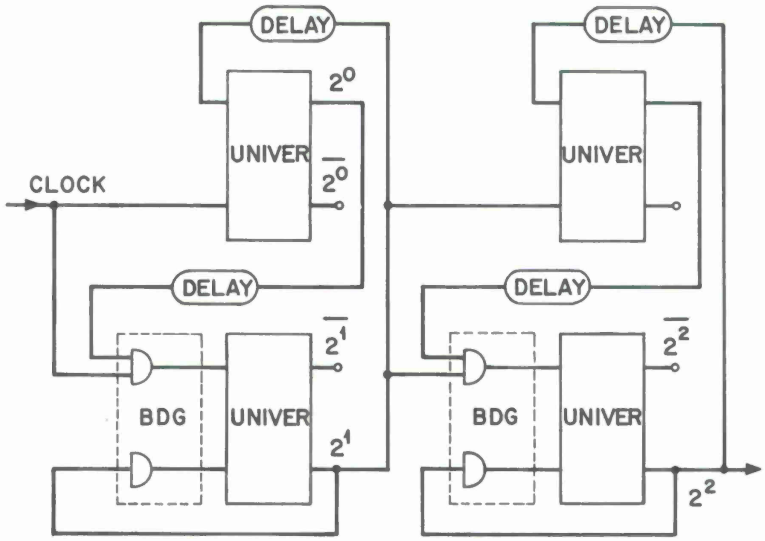
(b) Time response of 3-input NOR gate operation of typical TG UNIVER module. Modules are tested with 100-Mcps clock rate.

Fig. 21. Typical waveforms observed on a sampling-scope at UNIVER and TG UNIVER module tester.

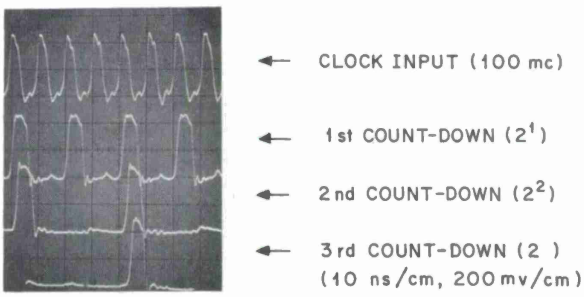
3-62-4418



3-62-4419



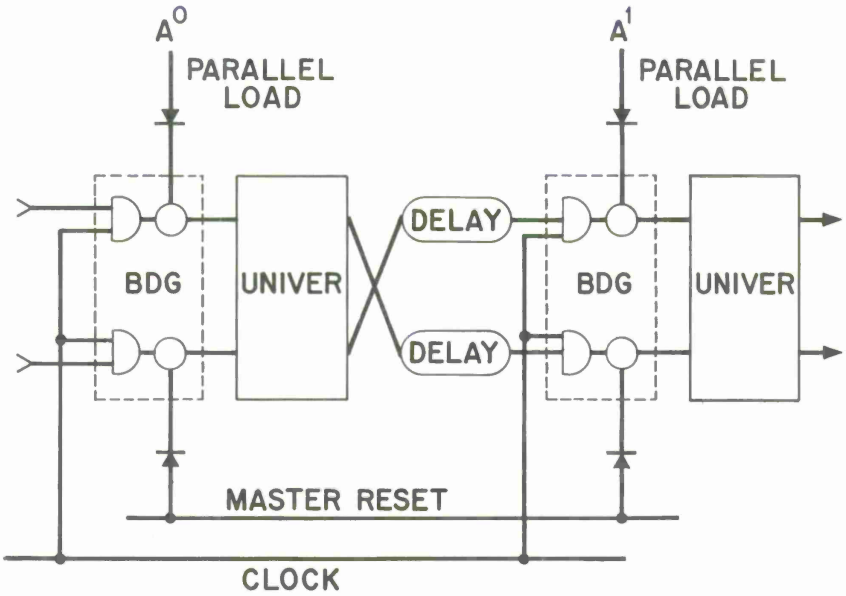
3-62-4420



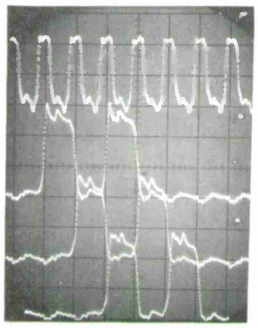
(a) Binary counting circuits.

Fig. 22. Typical system logic implementations by using various combinations of BDG, UNIVER, and TG UNIVER modules. All waveform photos were taken at the logic boards used in the experimental 10-bit multiplier operated under 100-Mcps clock rate.

3-62-4421



3-62-4422



← CLOCK INPUT (100 Mc)

← 1st STAGE SHIFT

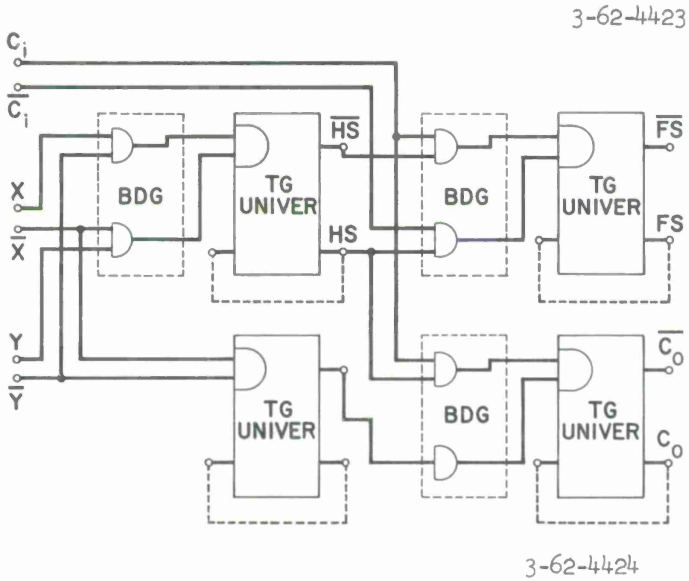
← 2nd STAGE SHIFT

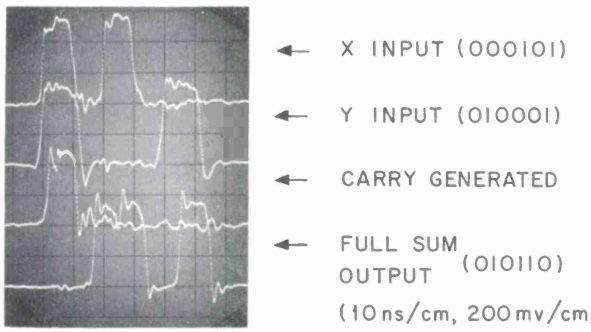
← 3rd STAGE SHIFT

(200 mv/cm, 10 ns/cm)

(b) Shift register with parallel-to-serial conversion.

Fig. 22. Cont.





(c) Binary full adder.

Fig. 22. Cont.

APPENDIX I

Circuit Module Layouts and Component Specification

In Figs. I-1 through I-7, the layouts of the three circuit modules, UNIVER, transistor gated UNIVER, and backward diode-AND-gate, are shown. All components are mounted in a 1/4 x 3/8-inch flat package. The specifications of each component are as follows:

A. Active Package Components

Typical package size: 0.25 x 0.375 x 0.1 in. flat package with 14 leads (gold-plated Kovar flat ribbon).

1. Transistor Chips

Physical Size: approximately 30 x 30 mil

Type: 2N918, 2N2784, or equivalent

Electrical Characteristics:

H_{FE} = 50 min @ V_{CE} = 2 v I_C = 10 ma

f_T = 900 Mcps min @ V_{CE} = 2 v I_C = 10 ma

C_{ob} = 1.2 pf max @ V_{CE} = 2 v

C_{ie} = 1.5 pf max @ V_{BE} = 0.5 v

BV_{CEO} = 8 v min @ I_C = 10 μA

BV_{BEO} = 4 v min @ I_E = 10 μA

V_{BE} match within 10 mv spread @ I_E = 5 ma.

2. Tunnel Diode

Physical Size: 60-mil dia. x 100-mil long epoxy packaged with flat ribbon leads.

Type: GE TD 252A (I_P = 4.7 ma) } or equivalent
GE TD 253B (I_P = 10 ma) }

Electrical Characteristics:

I_P = 4.7 ma $\pm$ 5% or 10 ma $\pm$ 5%

I_P/I_V = 6 min, 8 typical

V_P = 80 mv $\pm$ 30%

V_F = 550-mv min, 700-mv max @ I_P+

C_V = 1.0-pf max (I_P = 4.7 ma), 2.0-pf max (I_P = 10 ma).

3. Backward Diode

Physical Size: 60-mil dia. x 100-mil long, epoxy packaged with flat ribbon leads.

Type: GE 1N4090 or equivalent

Electrical Characteristics:

V_R = 80-mv min, 100-mv max @ I_R = 2 ma

V_F = 500-mv min, @ I_F = 1 ma

I_P = 180-μa max

C_V = 1.5-pf max.

4. Voltage Reference Diode

For the voltage reference diode, the same type transistor chip is used as a diode (base-emitter junction; collector is connected to the base). Only V_{BE} specification is applied, as in the transistor specification.

B. Resistor Package

Physical Size: 0.25 x 0.375 x 0.1-in. flat pack with 14 leads (gold-plated, Kovar flat ribbon).

Resistor Material: Vacuum deposited thin-film Nichrome or thick-film Cermet.

Temperature Coefficient: less than 100-ppm/^{o}C.

Resistor Value and Tolerance:

UNIVER

R_1, R_2, 100 Ω ± 10%

R_3, R_4, 470 Ω ± 2%

R_5, R_6, 750 Ω ± 2%

R_8, R_9, 1000 Ω ± 10%

TG UNIVER

R_1, R_2, R_3, R_4, R_5, 100 Ω ± 10%

R_6, R_7, 470 Ω ± 2% (4.7-ma TD)
220 Ω ± 2% (10-ma TD)

R_8, R_9, 750 Ω ± 2% (4.7-ma TD)
380 Ω ± 2% (10-ma TD)

R_{10}, R_{11}, 1000 Ω ± 10%

R_{12}, 50 Ω ± 10% (4.7-ma TD)
20 Ω ± 10% (10-ma TD)

BD GATE

R_1, R_2, 3000 Ω ± 5%

R_3, R_4, 5600 Ω ± 5%

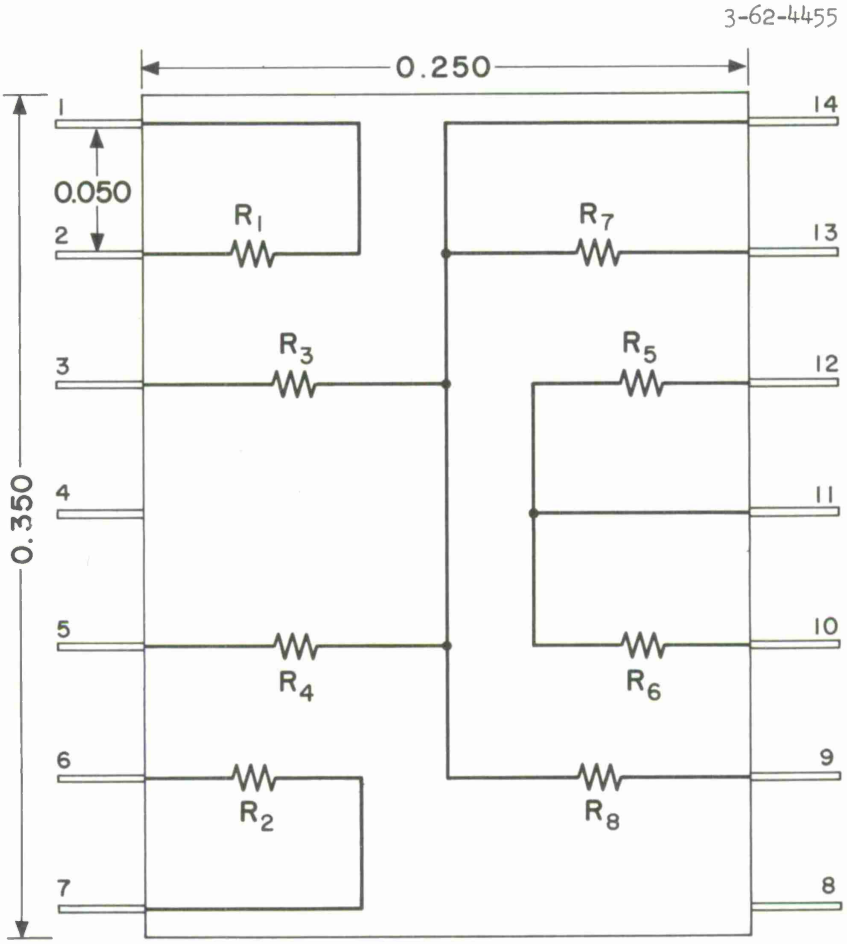


Fig. I-1. UNIVER resistor package.

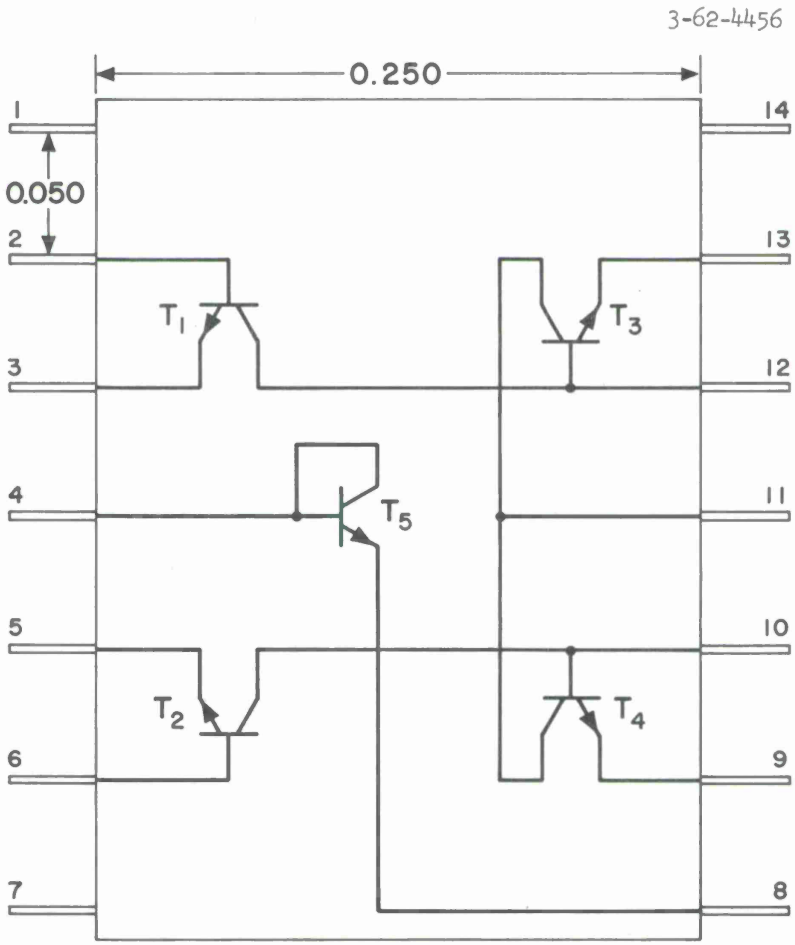


Fig. I-2. UNIVER transistor package.

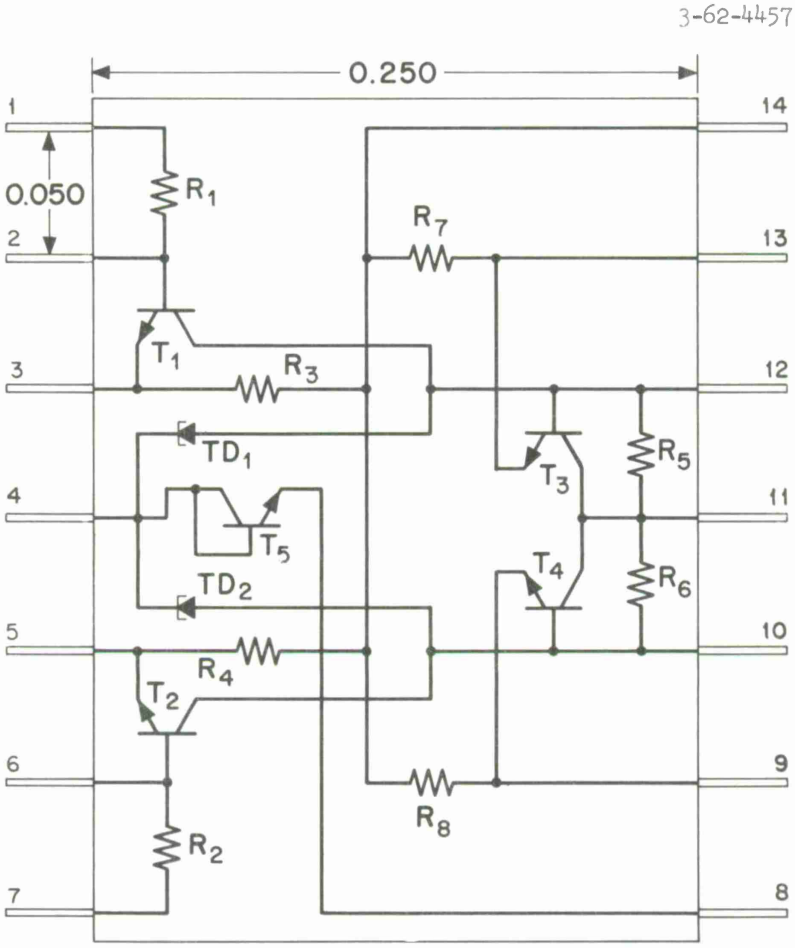


Fig. I-3. UNIVER in single package.

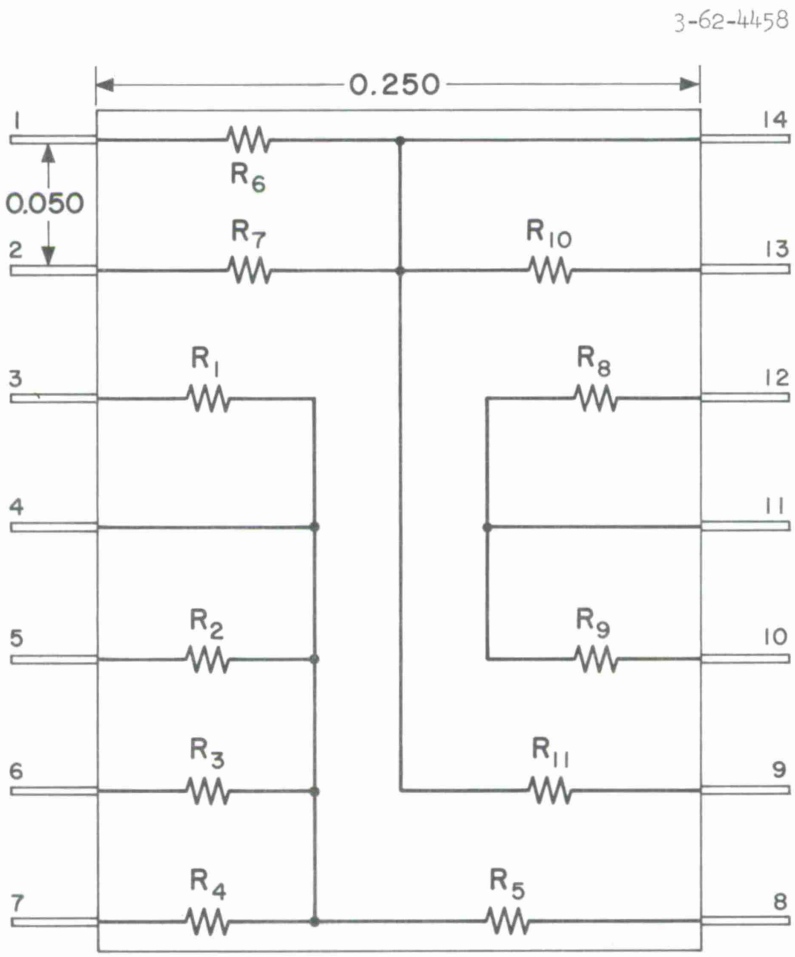


Fig. I-4. Transistor-gated UNIVER resistor package.

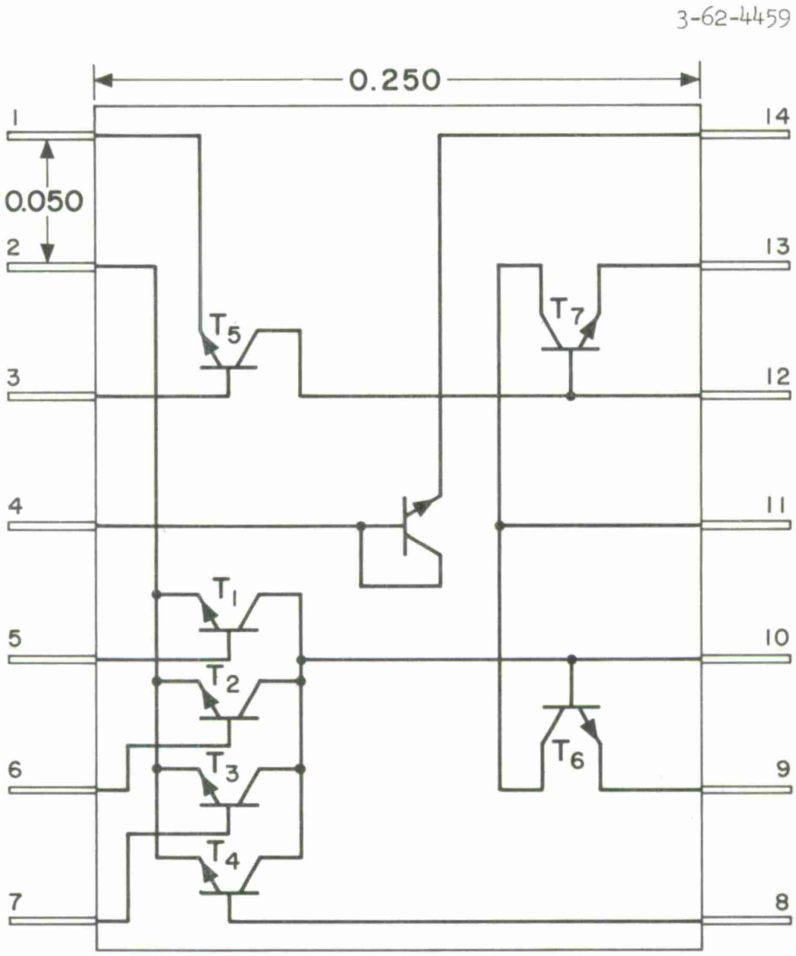


Fig. I-5. Transistor-gated UNIVER transistor package.

3-62-4460

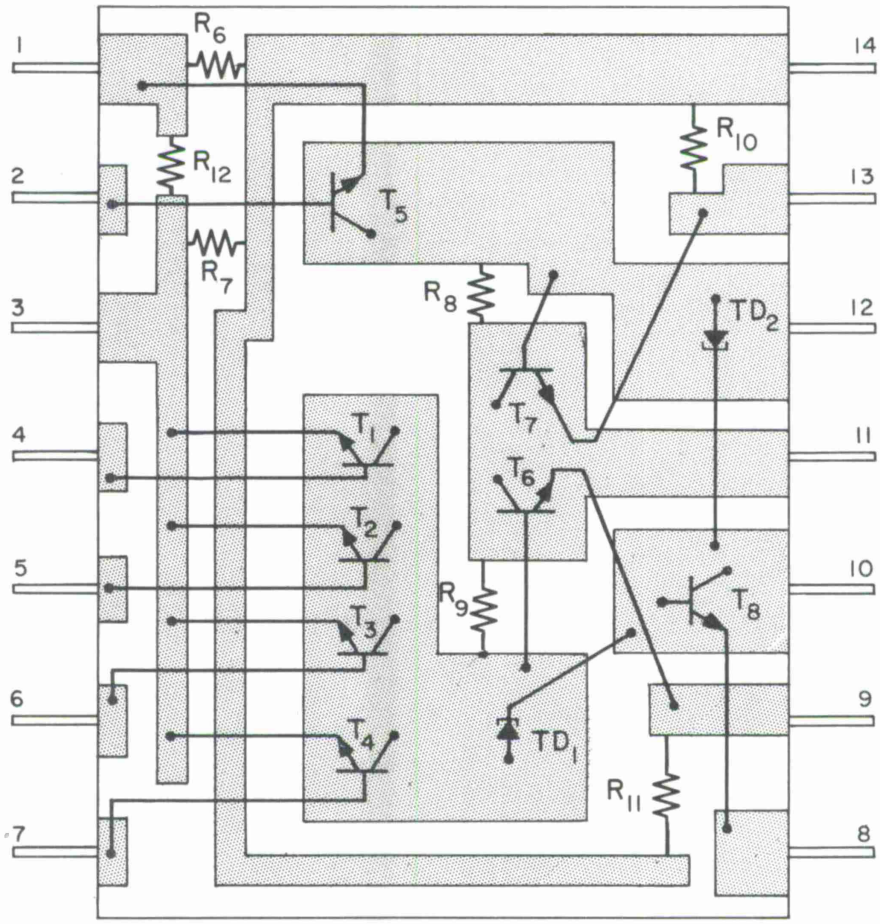


Fig. I-6. Transistor-gated UNIVER in single package.

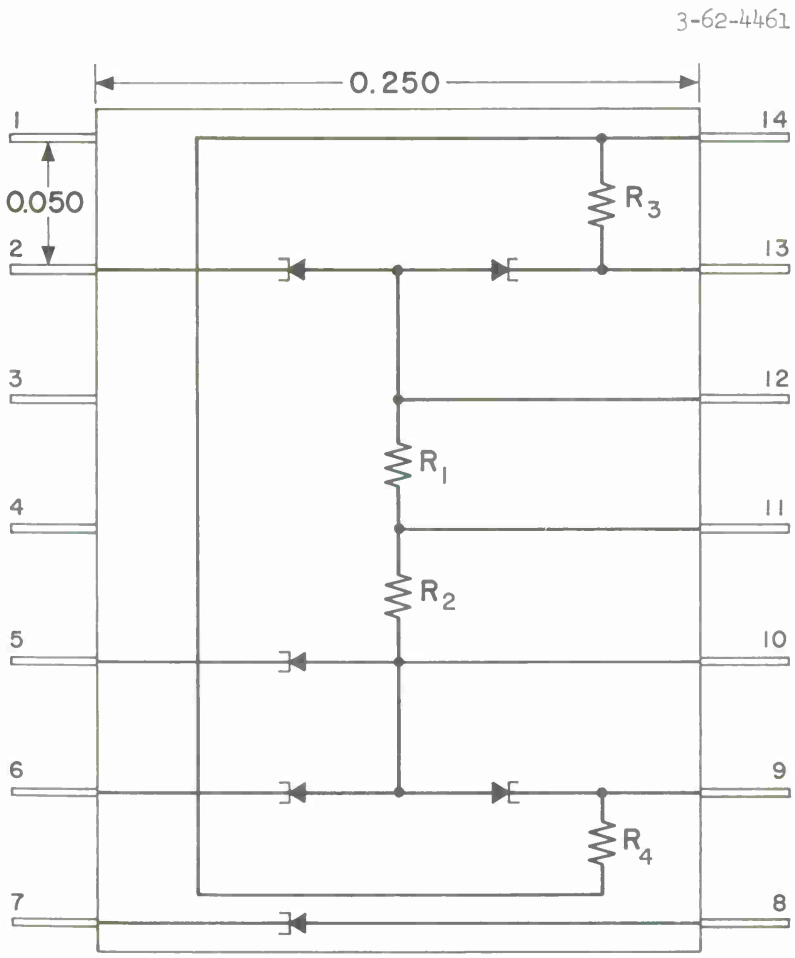


Fig. I-7. Backward diode gate module.

APPENDIX II

Numerical Calculations

A. DC Analysis

The steady state stability of the circuit operation can be determined by substituting the worst case component values in Eqs. (9), (11), and (12). In the numerical dc analysis of steady state stability, the evaluation of allowable passive component tolerances and power supply regulations are of primary interest.

From Eq. (9), the variation of I_{C1} with various component values and input reference levels can be determined. At the worst case, if this variation does not alter the tunnel diode bias state, it can be regarded as a stable circuit.

From Eqs. (11) and (12) and by replacing E_3 with V_S, the allowable worst case I_{C1} variation can be found. For instance, by taking a 5-percent variation of E_2 and R_3 and the active component variations, as shown in the table of Appendix I,

$$\text{allowable } I_{C1\,max} = \frac{E_{2min} - (V_{d1\,max} + V_{s\,min})}{R_{3\,max}} - I_{B3\,max} - 1.5\, I_{V\,max}$$

$$= 2.90 \text{ ma} \quad ,$$

and

$$\text{allowable } I_{C1\,min} = \frac{E_{2\,max} - (V_{d1\,min} + V_{s\,max})}{R_{3\,min}} - I_{B3\,min} - 0.9\, I_P$$

$$= 2.025 \text{ ma} \quad .$$

From Eq. (9), if the difference input $|e_1 - e_2|$ is zero and the base-emitter junction potential of the input transistor pair are perfectly matched,

$$I_{C1} = \alpha_F \frac{E_1 + e_1 - V'_{BE}}{2R_1 + h_{IB1}} \tag{IIa-1}$$

and $= 2.495$ ma ,

with typical component values: $\alpha_F = 0.99$; $E_1 = 2$v; $e_1 = 0$; $V'_{BE} = 0.78$v; $R_1 = 235\Omega$; and $h_{IB1} = 13\Omega$. By taking a 5-percent variation on E_1 and R_1; a $\pm$ 5-mv variation on V'_{BE}; a α_F min of 0.98 ($h_{FE} = 50$); and from Eq. (IIa-1),

$$I_{C1\,max} = 2.874 \text{ ma}$$

$$I_{C1\,min} = 2.153 \text{ ma} \quad ,$$

which is within the requirement of I_{C1} variation that will not alter the tunnel diode steady state bias condition. Thus, the circuit is shown to be stable against resistor and power supply variations within ± 5 percent of the specified center value. The above result is based on the assumption that there is a perfectly matched condition at the input; and by substituting the above result in Eq. (9), the allowable input offset voltage (input differential plus mismatch V_{BE} voltage) is found to be under $\pm$ 5 mv for the worst case. This tight requirement can be relaxed by (1) specifying tighter resistor tolerances and power supply regulation, or (2) inserting a series resistor between the common emitter junction of the input stage. In the actual fabrication of the UNIVER, the critical resistors have a specified tolerance of ± 2 percent, as seen in Appendix I. By using an integrated passive substrate in the circuit, an additional benefit is that the ratio of two resistor values that can easily be kept within a 1-percent variation. The deviation of R_1 and R_2 or R_3 in the same direction improves the worst case input offset voltage allowance substantially. The offset voltage is found by substituting Eq. (9) in Eq. (10) and solving for $(e_1 - V'_{BE2})$, thus,

$$\text{the offset voltage} = |e_1 - e_2| + |V'_{BE2} - V'_{BE1}|$$

$$= \left| \frac{E_1 - (V_1 + V_s)}{R_2} - I_{B3} - I_d - \alpha_F \frac{E_1 + e_1 - V'_{BE1}}{2R_1 + h_{IB1}} \right| (h_{IB1} + h_{IB2} + R_s) \quad , \qquad \text{(IIa-2)}$$

where R_s is the series emitter resistor. Taking the same worst case condition as before, except for R_1 and R_2, whose variations are now assumed to be $\pm$ 2 percent, the allowable input offset voltage for the worst case becomes approximately 14 mv (without the series emitter resistor). This gives enough margin for a system design in the most practical cases. With a series emitter resistor, the condition improves proportionally so that with a 50-ohm resistor, approximately 40-mv offset voltage is allowed for the same worst case. Accordingly, if one requires greater margins for a system design, the latter method is suggested. To maintain fast switching characteristics, a bypass capacitor may be necessary if the required series emitter resistor is greater than 75 ohms.

B. Switching-Time Calculations

1. Input-Stage Delay t_{dr}, t_{df}

Input-stage delay t_d is defined as the time required to trigger the tunnel diode from the moment of input-signal voltage is applied. It can be determined from Eq. (18).

If the input voltage is not an ideal step, the delay time is affected by the rise time of the input signal. By assuming an exponential rise of input waveform and that its time constant of the input waveform is approximately one half the time constant of the input stage, a simple relationship [Eq. (19b)] can be derived. The following numerical example and experimental results indicate that the above assumption closely represents the actual case.

From Eq. (19b), the input-stage delay t_d is found to be as

$$t_d \cong \tau_1 \ln \frac{1}{1 - \sqrt{\frac{\Delta I_{C1}}{g_m E_1}}} \quad (\text{with } \omega_1 \cong \frac{1}{2}\omega_s) \quad . \qquad \text{(IIb-1)}$$

By substituting the following typical parameters in the above equation,

$$\tau_1 = \frac{1}{\omega_1} = \frac{1}{\left(1 - \alpha_o + \frac{r_e}{r_1}\right)\omega_t} = \frac{1}{1.23 \times 10^9} = 0.81 \times 10^{-9} \text{ sec}$$

$$\omega_t = 2\pi f_t = 7.55 \times 10^9 \text{ r/s} \quad , \quad f_t = 1200 \times 10^6 \text{ c/s}$$

$$\alpha_o = 0.98$$

$$[r_1(1 - \alpha_o) + r_e] \cong 13 \text{ ohms} \quad , \quad r_1 \cong 80 \text{ ohms } (r_b' + r_{ext})$$

$$g_m = \frac{\alpha_o}{2[r_1(1 - \alpha_o) + r_e]} = 37.6 \times 10^{-3} \text{ mhos}$$

ΔI_{C1} = $I_p - I_o$ = 1.6 ma for the rise-time period

= $I_1 - I_V$ = 2.1 ma for the fall-time period (See Fig. 15 or Fig. II-2)

E_1 = 0.45-volt typical input signal amplitude, the nominal output voltage of the UNIVER circuit with 35-ohm load;

the input-stage delay for the rise time period is

$$t_{dr} = 0.296 \times 10^{-9} \text{ sec} \quad ,$$

and the input-stage delay for the fall-time period is

$$t_{df} = 0.35 \times 10^{-9} \text{ sec} \quad .$$

2. Rise Time t_r

To evaluate the charging current $i_g(V)$, the piece-wise linear approximation technique may be used. An example is shown in Fig. II-2, where the $V - I$ characteristic curve of the tunnel diode (4.7 ma peak current; type GE 252A) used in the UNIVER circuit is approximated by five segments in the range of interest. With this approximation, the charging current $i_g(V)$ becomes a linear function of the voltage within a segment. By substituting these relations in Eq. (23), the switching time of a tunnel diode can be calculated manually with reasonable accuracy.

In referring to Fig. II-1, it can be assumed first that the tunnel diode is initially loaded with constant current I_o, which is being applied by current step i_s. Then, the initial bias point A is lifted up and shifted toward the new intersection point C. During this process, the following charging currents are available at each segment and, on the basis of them, the following transition times are determined (the node capacitance is assumed to be the constant value C_n).

In the first segment $(V_o \rightarrow V_{P1})$,

$$\begin{aligned} i_{g1}(\text{the charging current}) &= I_F - i_r \\ &= I_F - \frac{V}{r_o} \end{aligned}$$

$$r_o = \frac{V_{P1} - V_o}{I_P - I_o} \quad .$$

From Eq. (22),

$$t_{r1} = \int_{V_o}^{V_{P1}} \frac{C_n \cdot dV}{i_{g1}(V)} = \int_{V_o}^{V_{P1}} \frac{C_n}{I_F - \frac{V}{r_o}} \cdot dV$$

$$= C_n r_o \ln \frac{I_F - I_o}{I_F - I_P} \quad . \tag{IIb-2}$$

In the second segment $(V_{P1} \rightarrow V_{P2})$,

$$i_{g2} = I_F - I_P \quad \text{(constant)}$$

$$t_{r2} = \int_{V_{P1}}^{V_{P2}} \frac{C_n}{i_{g2}} dV = \frac{C_n(V_{P2} - V_{P1})}{I_F - I_P} \quad . \tag{IIb-3}$$

In the third segment $(V_{P2} \rightarrow V_K)$,

$$i_{g3} = (I_F - I_P) + i_n = (I_F - I_P) + \frac{V}{r_n} \quad . \qquad r_n = \frac{V_K - V_{P2}}{I_P - I_V}$$

$$t_{r3} = \int_{V_{P2}}^{V_K} \frac{C_n}{i_{g3}} dV = C_n \, r_n \, \ln \frac{I_F - I_V}{I_F - I_P} \quad . \tag{IIb-4}$$

In the fourth segment $(V_K \rightarrow V_V)$,

$$i_{g4} = I_F - I_V \quad \text{(constant)}$$

$$t_{r4} = \int_{V_K}^{V_V} \frac{C_n \cdot dV}{i_{g4}} = \frac{C_n[V_V - V_K]}{I_F - I_V} \quad . \tag{IIb-5}$$

In the fifth segment $(V_V \rightarrow V_F)$,

$$i_{g5} = I_F - i_r = I_F - \frac{V}{r_f} r_f = \frac{V_F - V_V}{I_F - I_V}$$

$$t_{r5} = \int_{V_V}^{V_1} \frac{C_n \, dV}{i_{g5}} = C_n \, r_f \ln \frac{I_F - I_V}{I_F - I_I} \quad . \qquad \text{(IIb-6)}$$

Here, point V_1, I_1 is the desired final amplitude point (for instance, 90 percent of V_F).

Accordingly, the total switching time t_r, is

$$t_r = \sum_{n=1}^{5} t_{rn}$$

A qualitative rise time characteristic is shown in Fig. II-1.

In the actual UNIVER circuit, the tunnel diode is not driven by a current step, but by a slow rising current ramp [Eq. (18a)]. Therefore, the delay times corresponding to the first and second segments are essentially dictated by the input-stage delay. Similarly, the overdrive current, which is the applied current over the peak current, is time dependent and, therefore, relatively small at the initial phase of the second-to-third segment switching process. A qualitative picture is shown in Fig. 15, which represents the above situation. To simulate the actual switching process, further approximations are taken for the numerical calculations of each segment.

One of the key parameters in the following calculations is total node capacitance C_n. It is the sum of C_t and the effective capacitive load of the emitter-follower. The node capacitance C_t includes the input stage output capacity, mainly C_{ob}, and the junction capacitance of tunnel diode C_V. The effective capacitive load of the emitter-follower is contributed by the required base charge store for the corresponding output load current increment and the stray capacity, mainly C_{ie} plus C_{ob} of the output transistor. Though all the above mentioned capacities are voltage dependent, they are treated as fixed values in the following discussion for analytical simplicity. Since the voltage swing is relatively small, no significant error will be involved for the above assumption.

Typically,

$$C_t = 2.5 \times 10^{-12} \text{ farad}$$

$$Q_{ef} = I_L T_{e3} + Q_{loss} + C_X V_S$$

$$I_L = \text{load current swing } 15 \text{ ma for } 35\text{-ohm load}$$

$$T_{e3} \cong \frac{1}{\omega_T} = 0.13 \times 10^{-12} \text{ for } f_T = 1200 \text{ mc}$$

$$Q_{loss} \cong 0.1\, I_L T_{e3} \text{ typical}$$

$$C_X = 2_{pf} \text{ typical} \quad , \quad V_S = V_F - V_O \cong 0.55 \text{ volt;}$$

accordingly,

$$C_n = C_t + \frac{Q_{ef}}{V_F - V_O}$$

$$= 8.4 \times 10^{-12} \text{ farad typical} \quad .$$

In the first and second segments and as shown in the previous calculation, input stage delay time t_{dr} is defined as the time required to reach the peak point I_P from the initial bias point I_o by the input stage collector current swing. Accordingly, the input stage delay time covers these two segments and no significant delay is contributed by the rest of the circuit.

In the third segment, involvement of the negative conductance at this segment means the charging current is starting to increase, while the input current (the input stage collector current) is also increasing [Eq. (18a)]. To simplify the problem, it can be assumed that the input driving current is a constant ramp during the switching process in this segment. Slope of the input current can be found from Eq. (18a) to determine the slope at $t = t_{dr}$, or at the peak current point, so that

$$i_{c1}(t = t_{dr}) = \frac{g_m E_1}{\tau_1} \eta_1 t \quad ,$$

where

$$\eta_1 = 2\left[e^{-\omega_1 t_{dr}} - e^{-2\omega_1 t_{dr}}\right] \quad .$$

By applying this current ramp to the parallel RC circuit, where R is r_n, the effective negative resistance, and

$$r_n = \frac{V_K - V_P}{I_P - I_V} \quad .$$

In solving for the charging current (which flows through the capactive component),

$$i_{g3} = \frac{g_m E_1}{\tau_1} \eta_1 C_n r_n\left[e^{\frac{t}{r_n C_n}} - 1\right] \quad . \qquad \text{(IIb-7)}$$

The charge supplied by i_{g3} must be equal to the charge stored in C_n during the given interval, therefore,

$$\int_o^{t_{r3}} i_{g3} \cdot dt = \int_{V_P}^{V_K} C_n \cdot d_V \quad , \qquad \text{(IIb-8)}$$

or

$$\left(e^{\frac{t_{r3}}{r_n C_n}} - 1\right) - \frac{t_{r3}}{r_n C_n} = \frac{(V_K - V_P)\,\tau_1}{\eta_1 g_m E_1 r_n^2 C_n} \quad . \qquad \text{(IIb-8a)}$$

If only the first and second-order terms of the exponential expansion are taken, then,

$$t_{r3} = \sqrt{\frac{2(V_K - V_P)\, C_n \tau_1}{\eta_1 g_m E_1}} \quad . \qquad \text{(IIb-9)}$$

By substituting the following numerical values,

$$C_n = 8.4 \times 10^{-12} \text{ farad}$$

$$\tau_1 = 0.81 \times 10^{-9} \text{ sec}$$

$$g_m = 37.6 \times 10^{-3} \text{ mho}$$

$$E_1 = 0.45 \text{ volt}$$

$$\eta_1 = 0.43(t_{dr} = 0.3 \times 10^{-12} \quad , \quad \omega_1 = \frac{1}{\tau_1}$$

$$V_K - V_P = 0.14 \text{ volt}$$

and, then, $$t_{r3} = 0.495 \times 10^{-9} \text{ sec} \quad .$$

In the fourth segment, Eq. (IIb-5) is valid, assuming the input current i_{c1} has been reached at the beginning of this segment, so that

$$t_{r4} = C_n \frac{V_V - V_K}{I_F - I_V} = 0.481 \times 10^{-9} \text{ sec} \quad .$$

By substituting,

$$V_V - V_K = 0.275 \text{ volt}$$

$$I_F - I_V = 4.8 \times 10^{-3} \text{ amp}$$

$$C_n = 8.4 \times 10^{-12} \text{ farad} \quad .$$

In the fifth segment, Eq. (IIb-6) is valid as

$$t_{r5} = C_n \frac{V_F - V_V}{I_F - I_V} \ln \frac{I_F - I_V}{I_F - I_1} = 0.065 \times 10^{-9} \text{ sec} \quad .$$

If the following values are substituted,

$$V_F - V_V = 0.07 \text{ volt}$$

$$I_F - I_V = 4.8 \times 10^{-3} \text{ amp}$$

$$I_F - I_1 = 2.8 \times 10^{-3} \text{ amp}$$

$$C_n = 8.4 \times 10^{-2} \text{ farad} \quad .$$

Accordingly, the total rise time contributed by the tunnel diode switching is

$$t_r = t_{r3} + t_{r4} + t_{r5} = 1.068 \times 10^{-9} \text{ sec.}$$

3. Fall Time t_f

A similar method (as discussed in the rise time calculation) can be adopted for the numerical calculation of the fall time process.

By referring to Fig. (II-1), the tunnel diode switches from the initial bias point $D(I_1)$ to point $F(I_R)$ by applying an input current step i_R. Since the same piece-wise linear approximation may be used, the equation derived previously is applicable with minor modifications.

In the first segment $(V_1 \rightarrow V_V)$ and from Eq. (IIb-5),

$$t_{f1} = C_n r_f \ln \frac{I_R + I_o}{I_R + I_V} \quad . \tag{IIb-10}$$

In the second segment $(V_V \rightarrow V_K)$ and from Eq. (IIb-5),

$$t_{f2} = C_n \frac{|V_V - V_K|}{|I_R + I_V|} \quad . \tag{IIb-11}$$

In the third segment $(V_K \rightarrow V_{P2})$ and from Eq. (IIb-4),

$$t_{f3} = C_n r_n \ln \frac{|I_R + I_P|}{|I_R + I_V|} \quad . \tag{IIb-12}$$

In the fourth segment $(V_{P2} \rightarrow V_{P1})$ and from Eq. (IIb-3) ,

$$t_{f4} = C_n \frac{|V_{P2} - V_{P1}|}{|I_R + I_P|} \quad . \tag{IIb-13}$$

In the fifth segment $(V_{P1} \rightarrow V_R)$ and from Eq. (IIb-2),

$$t_{f5} = C_n r_o \ln \frac{|I_R + I_P|}{|I_R + I_2|} \quad . \tag{IIb-14}$$

Here point V_2, I_2 is the desired final amplitude point (for instance, 90 percent of of V_R).

Accordingly, the total switching time t_f is

$$t_f = \sum_{n=1}^{5} t_{fn} \quad .$$

As discussed in the turn-on period analysis in Appendix II B2, the input driving signal is not an ideal current step, but a slow rising current ramp due to the limited bandwidth of the input stage. Accordingly, the initial portion of the fall time process is affected by the input stage delay. The switching analysis at this portion is complicated by the fact that the input stage collector current will reach the final clamp current I_R while the tunnel diode node voltage is at the mid-portion of the swing in the broad valley region. By referring to Fig. II-2, it can be assumed that the input-stage delay t_{df} (the delay from I_1 to I_V) is covered by the voltage swing from V_1 to V_{V1}. Thereafter, the current swing supplied by the input stage will be used effectively to charge up the node capacitance due to the relatively high equivalent resistance in the second segment. If it is assumed that the input stage is a current source so that Eq. (18a) is still valid in this segment; then, the time delay to swing from the initial current I_1 to the final clamp current I_R is found from Eq. (18a) as

$$t_{dV1} = \tau \ln \frac{1}{1 - \sqrt{\frac{\Delta I_{C1}}{g_m E_1}}} = 0.49 \times 10^{-9} \quad \text{sec} \quad ,$$

where

$$\Delta I_{C1} = |I_R + I_1| \cong 2.5 \times 10^{-3} \text{ amp} .$$

During the period of $t_{df} - t_{dV1}$, the input current charges the node capacitance C_n and the corresponding voltage swing is found from Eq. (18a)

$$\int_{t_{df}}^{t_{dV1}} i_{c1} \cdot dt = C_n \cdot \Delta v$$

and, accordingly,

$$\Delta v = \frac{g_m E_1}{C_n} \left[t - \frac{\tau_1}{2} e^{-\frac{2t}{\tau_1}} + 2\tau_1 e^{-\frac{t}{\tau_1}} \right]_{t_{df}}^{t_{dV1}}$$

$$= 32 \times 10^{-3} \text{ volt} .$$

In the rest of segment II, $V_{V1} + \Delta v \rightarrow V_K$, the node capacitance is charged by $|I_R - I_V|$ and, therefore, the corresponding switching time is

$$t'_{f2} = C_n \frac{V_K - V_{V1} + \Delta v}{I_R + I_V} = 0.63 \times 10^{-9} \text{ sec} ,$$

where

$C_n = 8.4 \times 10^{-12}$ farad (it is assumed that the effective node capacitance is equal to that of the turn-on process. Actually, Q_{ef} is slightly less in the fall-time process.)

$$V_K - V_{V1} + \Delta v = 0.18 \text{ volt}$$

$$I_R - I_V = 2.4 \times 10^{-3} \text{ amp} .$$

Accordingly, the total switching time in this segment is

$$t_{f2} = t'_{f2} + (t_{dV1} - t_{df}) = 0.77 \times 10^{-9} \text{ sec} .$$

In the third segment, Eq. (IIb-12) is valid as

$$t_{f3} = C_n r_{n1} \ln \left| \frac{I_R + I_P}{I_R + I_V} \right| = 0.252 \times 10^{-9} \quad \text{sec} \quad ,$$

where

$$C_n = 8.4 \times 10^{-12} \quad \text{farad}$$

$$r_{n1} = \frac{V_K - V_{P2}}{I_P - I_V} = 28.6 \quad \text{ohm}$$

$$I_R + I_P = 6.3 \times 10^{-3} \quad \text{amp}$$

$$I_R + I_V = 2.2 \times 10^{-3} \quad \text{amp} \quad .$$

In the fourth segment, Eq. (IIb-13) is valid as

$$t_{f4} = C_n \frac{V_{P2} - V_{P1}}{I_R + I_P} = 0.053 \times 10^{-9} \quad \text{sec} \quad ,$$

where

$$C_n = 8.4 \times 10^{-12} \quad \text{farad}$$

$$V_{P2} - V_{P1} = 0.04 \quad \text{volt}$$

$$I_R + I_P = 6.3 \times 10^{-3} \quad \text{amp} \quad .$$

In the fifth segment, Eq. (IIb-14) is valid. Point A (I_o, V_o) is taken as the desired final amplitude, or

$$t_{f5} = C_n r_o \cdot \ln \frac{I_R + I_P}{I_R + I_o} = 0.038 \times 10^{-9} \quad \text{sec} \quad ,$$

where

$$C_n = 8.4 \times 10^{-12} \text{ farad}$$

$$r_o = 17 = \left(\frac{V_{P1}}{I_P}\right) \text{ ohm}$$

$$I_R + I_P = 6.3 \times 10^{-3} \text{ amp}$$

$$I_R + I_o = 4.8 \times 10^{-3} \text{ amp} \quad .$$

Accordingly, the total fall time is

$$t_f = t_{f2} + t_{f3} + t_{f4} + t_{f5} = 1.113 \times 10^{-9} \text{ sec} \quad .$$

4. Characterization of Rise and Fall Times and Switching-Time Optimization

From the foregoing results, it can be seen that 90 percent of the transit time corresponds to the voltage swing between the peak point V_P and the knee point of the forward diode characteristic V_V, or vice versa. Thus, the characteristics of the negative conductance and the valley regions of a tunnel diode have the dominant effect upon the switching time. From this point of view, the switching time equation may be written as follows (during the turn-on):

$$t_r = t_{r3} + t_{r4} + t_{r5}$$

$$\cong C_t\left[2r_n + \frac{V_1 - V_K}{I_F - I_V}\right] + \frac{Q_{ef}}{I_F - I_V} \quad , \qquad \text{(IIb-15)}$$

where the following approximations were assumed:

$$t_{r3} \cong C_n \frac{V_K - V_P}{I_P - I_V} \ln \frac{I_F - I_V}{I_F - I_P}$$

$$\cong 2\, C_n \frac{V_K - V_P}{I_P - I_V} = 2\, C_n r_n$$

$$t_{r4} + t_{r5} \cong C_n \frac{V_1 - V_K}{I_F - I_V} \quad ,$$

and C_n is defined as

$$C_n = C_t + \frac{Q_{ef}}{V_1 - V_o} \quad .$$

Similarly, for the turn-off period,

$$t_f = t_{f2} + t_{f3} + t_{f4} \tag{IIb-16}$$

$$\cong C_n \left(\frac{V_V - V_K}{I_R + I_V} + \frac{V_K - V_P}{I_P - I_V} \right)$$

$$= \left(C_t + \frac{Q'_{ef}}{V_1 - V_o} \right) \left(\frac{V_V - V_K}{I_R + I_V} + r_n \right) \quad .$$

These two equations give a fairly good estimate of the rise and fall times of the UNIVER circuit within the limited range of the overdrive currents.

By using a tunnel diode as in the UNIVER circuit and, thus, operating in the bi-stable mode with biasing midway between the peak-to-valley point and triggered by an approximately equal current swing, the available charging current is generally greater at the turn-on process from the low state (before the peak) to the high state (the forward diode characteristic) and, accordingly, the rise time is slightly faster than the fall time. In the actual UNIVER circuit, however, because the input signal is fed to the tunnel diode through the more favorable path at the turn-off process, the actual overall transition times at the rise and fall times are closely matched.

The simplified transition time equation, Eq. (IIb-15) or Eq. (IIb-16), may be used as the general guide for the optimization of the switching characteristic of the UNIVER circuit. Since the turn-on switching process of the tunnel diode may be regarded as a favorable switching mode operation, Eq. (IIb-15) is suitable for this purpose. By using Eqs. (18a) and (IIb-15) for the expression of the total transition time, and taking a constant input drive along with proper approximations, the condition for the minimum circuit delay time is given by Eq. (29)

$$I_P = \sqrt{2 \frac{C_t V_S + I_L T_{e3}}{T_{C1}} I_{B1}} \quad .$$

By substituting the following numerical values,

$$C_t = 2.5 \times 10^{-12} \text{ farad}$$

$$V_S = 0.5 \text{ volt}$$

$$I_L = 15 \times 10^{-3} \text{ amp (with a 35-ohm load)}$$

$$T_{C1} \cong \frac{1}{\omega_{t1}} = 0.13 \times 10^{-9} \text{ sec}$$

$$T_{e3} \cong \frac{\alpha_o}{\omega_{t1}} \cong 0.13 \times 10^{-9} \text{ sec}$$

$$I_{B1} = 1 \times 10^{-3} \text{ amp (at the threshold voltage), and}$$

then,

$$I_P = 7 \times 10^{-3} \text{ amp (with a 35-ohm load)}$$

$$= 5.7 \times 10^{-3} \text{ amp (with a 75-ohm load)} \quad .$$

This result indicates that the UNIVER circuit with tunnel diodes whose peak current of $5 \sim 8$ ma is properly optimized for the minimum-circuit delay. Since standard tunnel diodes are not available in this range, tunnel diodes with I_P of 4.7-ma and 10-ma are employed. The former type is used in the basic UNIVER circuit module, while the latter type is used in the transistor-gated UNIVER where the expected node capacitance is slightly higher.

3-62-4398

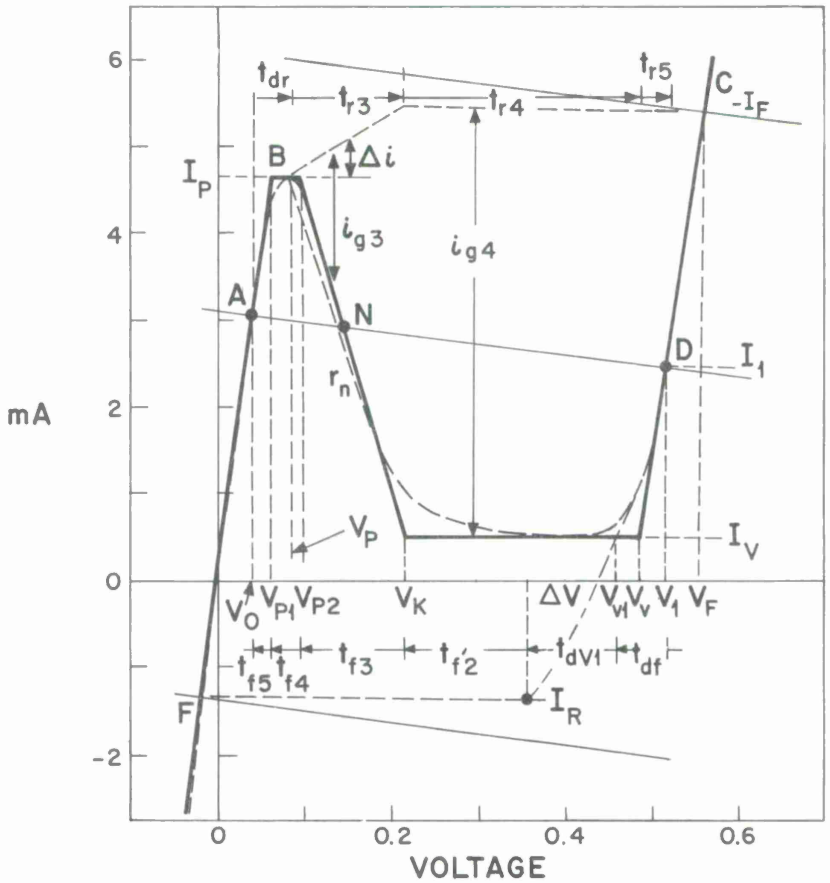


Fig. II-1. Rise- and fall-time analysis of a constant current loaded tunnel diode switch using piece-wise linear approximations.

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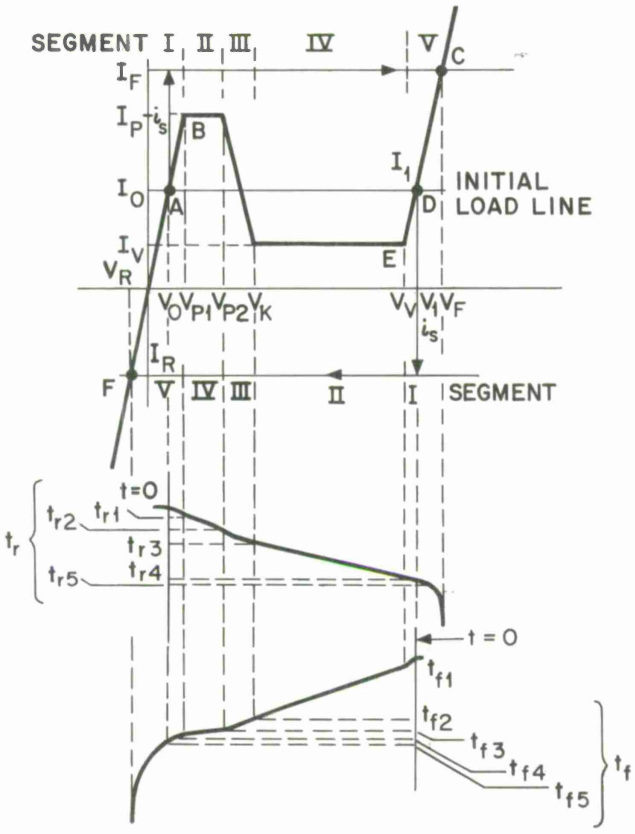

Fig. II-2. Piece-wise linear approximations on a TD-252A tunnel diode characteristic curve.

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13. ABSTRACT

A set of logically flexible digital building blocks capable of implementing various logic functions with delays of less than one-nanosecond has been developed and fabricated in microcircuit form.

The set consists of two basic types of circuit modules; with these, all conceivable digital system logic functions can be implemented. Tunnel junction diodes and silicon transistors provide gating functions, and a universal amplifier circuit module reshapes signal waveforms, restores amplitudes, and stores signals (flip-flop operations).

Subnanosecond switching time is achieved by the effective utilization of a tunnel diode transistor circuit and hybrid integration techniques for microcircuit fabrication. The circuit provides the following characteristics: (1) low power delay time product (efficient switching); (2) effective noise immunity; (3) well-defined temperature invariant transfer characteristics; (4) relaxed component tolerances as compared to other tunnel diode logic circuits; (5) high fan-in and fan-out ratios; and (6) capability of performing all logical functions with two basic circuit configurations.

The circuits were developed primarily for a high-speed digital system operated at a 100- to 200-Mcps clock rate with a low impedance transmission line signal distribution scheme.

Analysis of the circuit, optimization of the circuit characteristics, the fabrication techniques of the circuit modules, and experimental results in a high-speed digital system are discussed.

14. KEY WORDS

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