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Progress Report for  
Sixth Quarterly Period

R & D PROGRAM TO DESIGN AND FABRICATE  
DIGITAL MONOLITHIC MICROCIRCUITS HAVING  
AVERAGE PROPAGATION DELAY TIME OF 1 NS.

MIT, Lincoln Laboratory  
Extension of Subcontract No. 295  
Prime Contract No. AF 19(625)-500

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## SECTION 1 - INTRODUCTION

### 1.1 Program Objective

This research and development program, which is an extension of M.I.T. Lincoln Laboratory Subcontract No. 295 (Prime Contract No. AF 19(625)-500), has as its primary objective the fabrication of silicon monolithic microcircuits with average propagation delay times in the subnanosecond region. The high speed performance of such microcircuits can be most effectively utilized in an environment which has a minimal slowing effect on the speed of the microcircuit.

In computer systems which can involve large numbers of similar microcircuit configurations, interstage delays play a large role in addition to stage delays in limiting the system speed. Therefore, a secondary objective of this program is a preliminary investigation of the speed improvements obtainable by fabricating and interconnecting arrays of high performance microcircuits within a single silicon chip, thereby minimizing the interstage signal delays (due to signal path and parasitic elements) associated with conventional microcircuit interstage wiring. Successful application of these arrays will depend upon prudent solution of power dissipation-speed problems which naturally arise from the increased component densities inherent in monolithic microcircuits.

## 1.2 Areas of Investigation

Present transistor fabrication capabilities are useful in construction of high speed monolithic microcircuit gates. Their utility is being enhanced by refinements in transistor design and fabrication techniques that permit more precise prediction and thus further optimization of specific transistor properties such as  $f_T$ ,  $r_b'$ ,  $\tau_s$ , and  $V_{PT}$ . In addition, work is continuing on the ultrasmall-geometry (0.05-mil patterns and 0.05-mil spacings) SX4 transistor to determine performance improvements obtainable from reducing transistor geometries below 0.1 mil. Small geometry, shallow diffusion techniques have also been used in an effort to obtain high performance pnp transistor structures.

Development of microcircuits centered about the high performance transistor has been aimed at two specific areas:

1. High-speed gates,
2. High-speed, high-density microcircuit arrays.

Simple 3-input TTL and ECL microcircuit gates are being fabricated to determine the extent of the improvements in speed, in both saturated and non-saturated microcircuits, made possible by the use of high performance transistor structures and, equally important, to determine which factors limit further improvement. Thus far, "first design" TTL and ECL (SMX1 and SMX2) have been successfully fabricated, tested, and analyzed to show speed properties an order

of magnitude higher ( $\tau_{pd} = 1.3$  ns for TTL gate;  $\tau_{pd} < 0.6$  ns for ECL gate) than obtainable in commercially available microcircuits. A second design of the ECL (SMX4) microcircuit expected to result in additional speed improvement has been completed and will be constructed shortly. A second design of the TTL microcircuit is being delayed, pending further investigations of the first design.

Finally, preliminary investigation was performed on the various factors relating to the fabrication of high-speed monolithic microcircuit arrays. This effort is aimed at determining the speed improvements that are possible in repetitive microcircuit systems as a result of fabricating and interconnecting arrays of high-speed microcircuit stages in monolithic form rather than conventionally interconnecting individual high-speed microcircuits to perform the same array function.

## SECTION 2 - FACTUAL DATA

### 2.1 Transistor Design Improvements

Principal effort in this area was directed at improving the design capability of the electrical properties of high-speed transistors such as described in Section 1. Data has been accumulated on the various small-area transistor structures studied to date (i.e., the SX3, with four 0.1- x 1.0-mil emitters, the SMX1T, with two 0.1- x 1.5-mil emitters, the SMX2T, with one 0.1- x 0.8-mil emitter, and the AMX1, with one 0.1- x 0.5-mil emitter). This data has yielded significant quantitative information on the basic relationships between transistor geometry and structure and transistor performance. Present efforts, aimed at refining in-process control of the transistor impurity distribution will result in more precise design control. This capability is particularly important to fabricating high performance microcircuits and is essential to fabricating high performance microcircuit arrays. In a typical experiment, transistor parameter uniformity was improved by increasing the impurity concentration of the transistor base region. Table 1 shows typical parameter values on transistors from two wafers which had been diffused to yield higher base concentrations. (Transistors in wafer 229A

TABLE 1

Typical Parameter Values of Transistors  
Made from Two Different Diffused Wafers

<u>PARAMETER</u>	<u>CONDITIONS</u>	<u>WAFER NO.</u> <u>229A</u>	<u>WAFER NO.</u> <u>229B</u>
$f_{Tmax}$	$V_{CB} = 3 \text{ V}$	3.0 - 3.2 GHz	3.5 - 4.3 GHz
$I_{pk}$		7 - 8 mA	8 - 10 mA
$r'_b$	$I_B = 3 \text{ mA}$	15 - 17 ohms	15 - 17 ohms
$\tau_s$	$I_{B1} = I_{B2}$ $= I_C = 8 \text{ mA}$	5.3 ns	5.3 ns
$\beta$	$V_C = 3 \text{ V}$ $I_C = 1 \text{ mA}$	60 - 90	100 - 180
Typical $V_{PT}$	0.001 mA	12 V	5 V
$V_{SAT}$	$I_B = 1 \text{ mA}$ $I_C = 10 \text{ mA}$	0.14 - 0.18 V	0.13 - 0.18 V

were designed to obtain  $f_T$  of 3 GHz, and those in wafer 229B were designed to obtain  $f_T$  of 4 GHz.) This experiment revealed that although increasing the base concentration improved the device parameter uniformity and control, it resulted in an increase (2:1) in storage time,  $\tau_s$ , and a decrease in the current,  $I_{pk}$ , at which  $f_T$  reached its maximum value. Both of these effects are suspected to be due to modifications in the structure of the base-collector junction which results from the increased base doping.

In an effort to determine the transistor performance improvements that can result from these geometries below 0.1-mil, experimental work on the SX4 transistor (0.05-mil geometry) has continued. The potential performance of this device can be vital to future very-high-density, very-low-power microcircuit systems. Photomask problems have hampered the fabrication of this device to date. However, recent improvements in our photomask production process are expected to be used in fabricating devices during the next period.

PNP transistor structures, with the same geometry as the SX3, high performance npn device have been successfully fabricated. Transistor  $f_T$  values were typically 1200-1400 MHz.

## 2.2 Microcircuit Performance Improvements

Investigative development has been continued on the SMX1 (TTL) and SMX2 (ECL), 3-input gate microcircuits. During this period, efforts were concentrated on optimizing the speed of these circuits, while simultaneously observing the resultant speed-power relationships.

### 2.2.1 TTL Microcircuits

TTL (SMX1) microcircuits, fabricated with 2.5 GHz transistors, were shown to have propagation delay times as low as 1.3 ns. These represent the highest speed saturated switching microcircuits known. Recent analyses indicate that the speed of this microcircuit design may be improved further by optimizing the microcircuit transistor  $f_T$  and storage time properties. Microcircuits which are currently in process are designed to have higher  $f_T$ 's. Moreover, techniques for further reducing storage time are being evaluated. One method which was tried without success on the SMX1 involves back biasing the isolation channel to reduce storage time originating in the transistor collector. It became evident that successfully applying this technique to the SMX1 would require removing the n+ buried layer from the collector regions. Although there are microcircuits in process which will

embody the proper structure, it is expected that the increased  $V_{SAT}$  resulting from removing the  $n+$  regions will preclude use of the method.

Speed-power properties of a number of SMX1 devices were examined to determine the relative utility of the basic TTL switching circuit in high-speed multicomponent microcircuit arrays. Data taken on single SMX1 microcircuits and on a 5-stage SMX1 ring oscillator indicated that, based on present SMX1 performance levels, monolithic microcircuit arrays can be made which would function at average propagation delay times of 1 to 2 ns/stage at power levels of 8 to 12 mW/stage. Circuit redesign could be expected to improve this speed-power relationship.

### 2.2.2 ECL Microcircuits

During this quarterly period, the basic speed and power properties of the unsaturated SMX2 microcircuits were evaluated. It was found on recent circuits that the SMX2 microcircuit design is capable of operation at propagation delay times of 0.65 ns or less (when fan-in and fan-out are 1) at power levels of approximately 35 mW/stage\*. (Earlier circuits had calculated delays of

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\* The average power dissipation is estimated with only one emitter follower output to make comparisons with the TTL circuit more realistic.

0.8 ns.) These values were obtained by correcting single micro-circuit measurements for the delay times introduced by the driving pulse, and by direct measurements made on a 5-stage SMX2 ring oscillator.

Detailed evaluation and analysis of four lots of SMX3 micro-circuits fabricated to date suggested that the speed-power performance of this microcircuit can be further improved if the following changes are made in the SMX2 microcircuit design:

1. Redesign Microcircuit Transistors to Optimize Transistor  $f_T$  Response -- The SMX2 transistor may be redesigned to optimize the device  $f_T$  at circuit operating currents, and thereby improve microcircuit speed.
2. Reduce Parasitic Resistor in the  $V_{CC}$  Conduction Path -- By making appropriate changes in the micro-circuit structure, detrimental parasitic resistances can be eliminated from the  $V_{CC}$  conductor path. In the SMX2 design, 40 to 60 ohms parasitic resistance is unavoidably added to the load resistors ( $R_{C1}$  and  $R_{C2}$ ) of the gate and reference transistors. In addition, about 30 ohms is interposed between  $V_{CC}$  and the collector of the emitter follower. These parasitics,

shown schematically in Figure 1, affect both the speed and power dissipation of the circuit. The increase in effective  $R_{C1}$  and  $R_{C2}$  results in a non-symmetrical output voltage. To restore symmetry,  $V_{CC}$  and  $V_{EE}$  must be adjusted in directions which result in an increase in the circuit's total power dissipation. The 30 ohms between  $V_{CC}$  and the collectors of the emitter followers result in an additional circuit delay because of the added RC delay at this node.

3. Optimize Emitter Follower Resistors to Improve Circuit Speed and Power -- Transient analysis shows that the speed of the SMX2 microcircuit could be improved by raising  $R_{E2}$  (to make this emitter node appear as a constant current source) and by lowering  $R_{E1}$  (to reduce the RC time constant at these nodes). D-C considerations, however, require that these changes be accompanied by the addition of another  $V_{EE}$  supply, and appropriate changes in  $R_{C1}$  and  $R_{C2}$ . Figure 2 is a schematic of the improved ECL design.

The microcircuit layout design for the improved version of the SMX2, to be designated SMX4, has been completed. It is expected that the first finished SMX4 microcircuits will be evaluated during the next period.

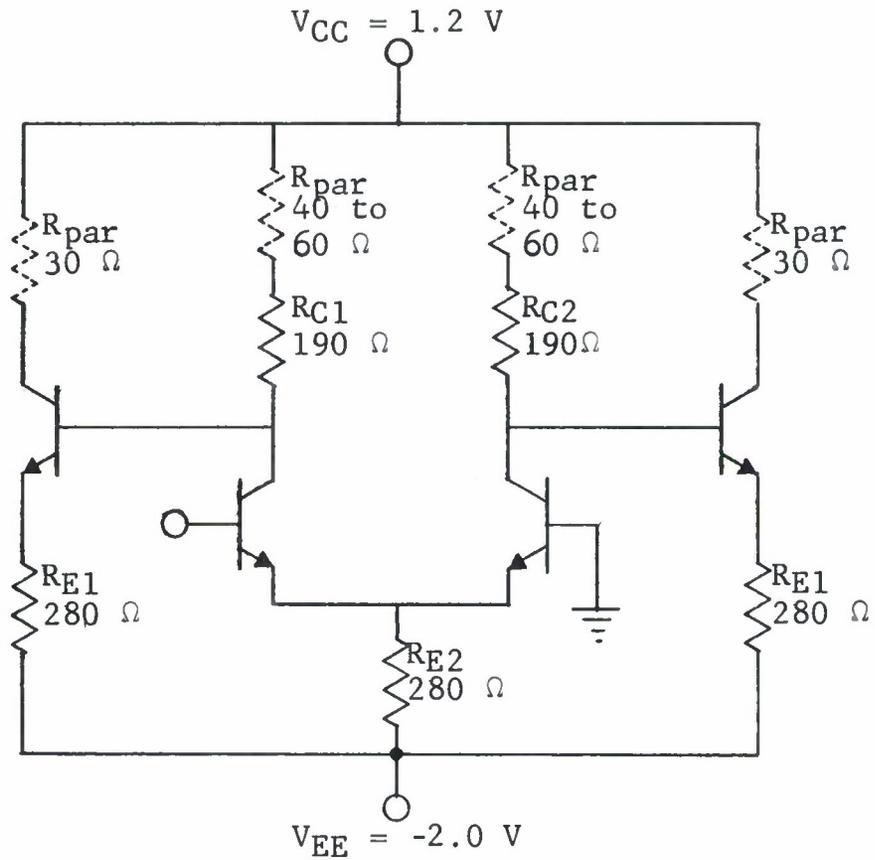


Figure 1. SMX2 design showing parasitic resistances.

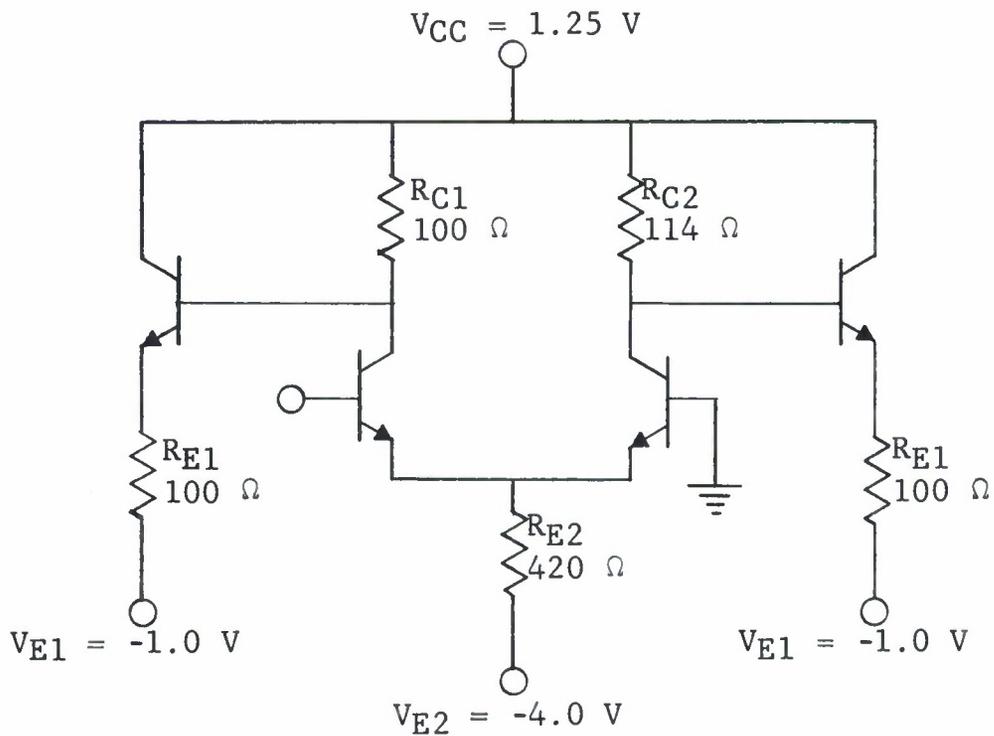


Figure 2. Improved ECL design (SMX4).

### 2.2.3 Fabrication of Microcircuits for Computer Circuit Evaluation

SMX3 microcircuits have been fabricated and are being evaluated. To more efficiently test this circuit, equipment has been assembled for functionally testing the SMX3 at the die sort operation. Preliminary testing indicates that functionally adequate circuits are being obtained.

### 2.2.4 High Density - Small Geometry Microcircuit Arrays

As a result of a number of discussions between Lincoln Laboratory and Philco personnel, a vehicle has been selected for investigating the problems associated with producing and testing high density, small geometry microcircuit arrays. This vehicle, a computer circuit termed, "Parity Check Circuit", was selected because it will introduce the problems associated with:

1. Fabricating and interconnecting,
2. Testing high performance complex monolithic circuit arrays.

The decision as to what form of logic to use to implement the Parity Circuit will be made shortly. Tentative TTL and ECL designs indicate that a basic microcircuit array chip (25 to 35 mil chip) will contain approximately 40 high performance transistors, a factor of 5 to 10 times the number that exist on the basic SMX1 and SMX2 microcircuits.

SECTION 3 - DELIVERY OF SAMPLE DEVICES

During the period covered by this report, the following devices were delivered to Lincoln Laboratory for evaluation:

<u>UNIT</u>	<u>TYPE</u>	<u>QUANTITY</u>
Transistors	SX3	10
Microcircuits	SMX1	10
	SMX2	5
Ring Oscillator	SMX2 (5-stage)	1

## SECTION 4 - WORK FOR THE NEXT PERIOD

The following is an outline of the work planned for the next quarterly period of the program.

### 1. Transistor Development

- a. Fabricate improved npn silicon transistors.
- b. Fabricate high performance SX4 transistor geometry.
- c. Continue investigation of low power operation of high performance npn silicon transistors.

### 2. Microcircuit Development

- a. Fabricate and evaluate improved final design version of SMX1 and SMX2 microcircuits.
- b. Fabricate and evaluate very-high-speed SMX4 microcircuit.
- c. Select circuit form for the Parity Check Circuit. Fabricate preliminary samples after mask design and preparation.

### 3. Microcircuits for Computer Evaluation

- a. Fabricate improved versions of SMX3.

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