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Transistorized Digital Clock with Serial Binary-Coded Readout

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Space Surveillance Branch
Applications Research Division

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ABSTRACT

A transistorized digital clock and coder unit has been developed which is being used as part of the time standard equipment at the U.S. Naval Space Surveillance Stations in Hawkinsville, Georgia, Red River, Arkansas, and Raymondville, Texas, which were instrumented in 1965. This unit is powered by a 24-v battery supply and is capable of 24 hours of emergency service in case of commercial power failure. Decimal digits are read out in binary format at a rate of one decimal digit per second. Each group of pulses comprising a decimal digit is clearly separated from the next pulse group. Once the code is learned, it is much easier to recognize than the one formerly used in the Space Surveillance system.

The transistorized circuitry used in this unit has resulted in a considerable reduction in size and power input (12 w) as compared with the vacuum tube unit which has been used for a similar purpose in other Space Surveillance stations. Also, the error in coding due to aging of components has been eliminated since only two levels must be distinguished in the binary logic as compared with the ten voltage levels of the decimal logic in the earlier equipment. The new unit employs two cascaded gates, one switching at 0.1-sec intervals and the other at 1.0-sec intervals.

PROBLEM STATUS

This is an interim report on one phase of the problem; work on the problem continues.

AUTHORIZATION

NRL Problem R02-35
BuWeps Project RT-8801-001/6521/S434-00-01

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TRANSISTORIZED DIGITAL CLOCK WITH SERIAL BINARY-CODED READOUT

BACKGROUND

In space surveillance work using continuously running multichannel recorders, the practice has been to record the time with a single marker pen along one margin of the recording. The digital clock and time coding equipment adopted by the U.S. Naval Space Surveillance System was designed originally for the Project Vanguard Minitrack System.* It employed vacuum-tube circuitry and, consequently, required a relatively large amount of rack space and power. A serial coded readout at 10-sec intervals gave Universal Time in five decimal digits. The digits were spaced 1 sec apart, with each digit coded in from one to ten deflections occurring at the rate of ten deflections per second. Reading of this code was difficult, however, on recordings made at rates of 5 mm/sec or less.

The need to reduce each space requirement, to reduce heat generation, and to increase reliability has lead to the development of a transistorized digital clock and coder. The inherent characteristics of transistor circuitry provide the desired high reliability, small size, and low power consumption.

Experience over several years has shown the desirability of several features not included in the original digital clock and associated coding equipment. These desirable features have been incorporated in the new transistorized clock. The reduction in size has made it possible to replace the digital clock chassis and the time comparison chassis* by a single chassis with a total power consumption of approximately 12 w. Among other circuit changes, decimal logic has been replaced by binary logic to eliminate the critical resistance values in the time coding circuitry. The new unit employs two cascaded gates, one switching at 0.1-sec intervals and the other at 1.0-sec intervals.

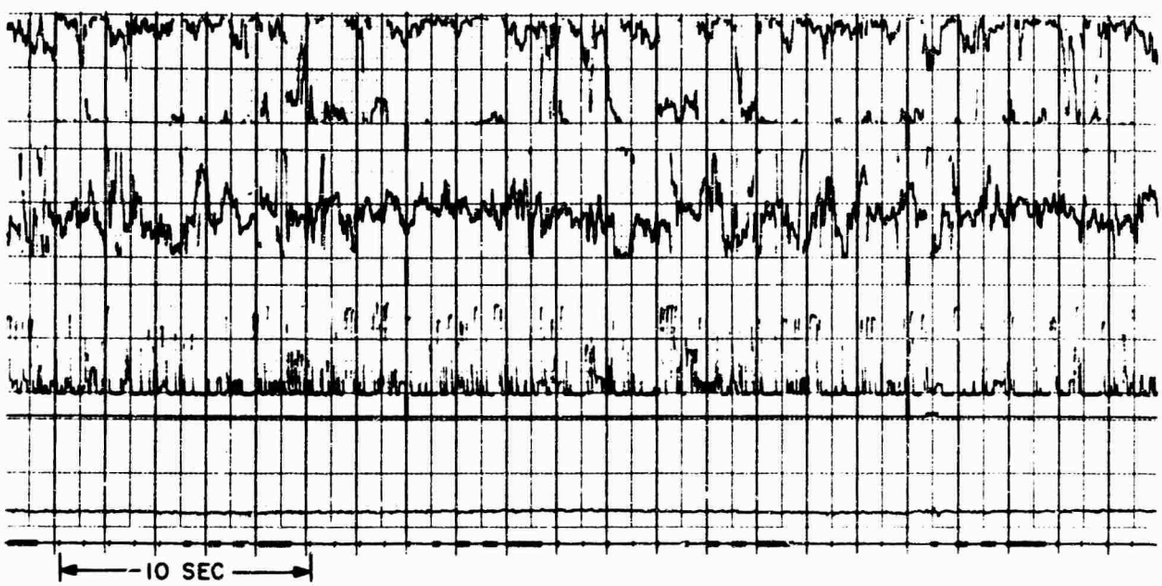
TIME CODE

The station clock, in addition to keeping correct time, must generate a time code suitable to record the time on a slow-moving (5 mm/sec) paper tape with a marker pen. A sample of the code used in the earlier clock is shown at the bottom of Fig. 1(a). Five decimal digits are read out at a rate of one digit per second every 10 sec. The decimal digit is one less than the number of deflections, except that the tens-of-hours digit is two les than the number of digits. A nine in the hours or minutes position completely fills the available space, eliminating separation between the nine and the next digit.

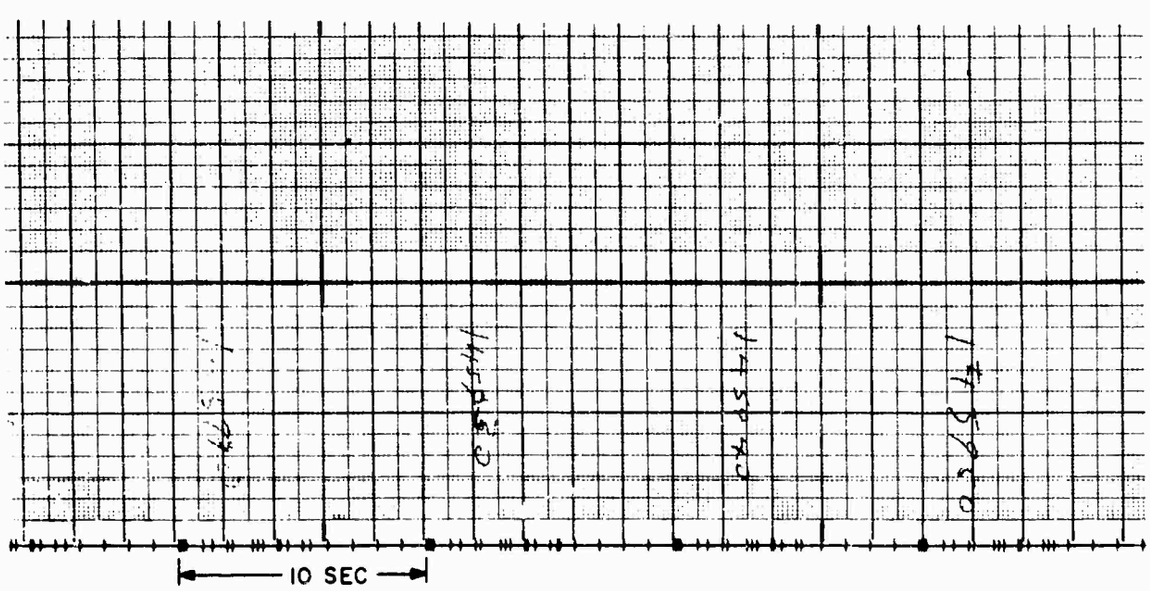
The revised code is illustrated at the bottom of Fig. 1(b). Special coding of the first digit is avoided by the insertion of a four-pip marker which starts at the beginning of the 10-sec interval. The digits are read out in the same order as before, but each is delayed by 1 sec when compared to the older code. The first pip associated with each decimal digit is the 1-sec marker and is a reference identifying the position of any other pulses. The other pulses, if they occur, follow at 0.1, 0.2, 0.3, and 0.4 sec after the marker and have values of 8, 4, 2, and 1, in that order, the sum being equal to the decimal digit which they represent. Lack of a pulse in any of the four positions indicates the binary value of

*C.A. Schroeder, E.J. Habib, and W.R. Silvester, NRL Report 5227 [Project Vanguard Report 36 (Minitrack Report 8)], "Time Standard," Oct. 1958.

zero. Memorizing the binary number system (although this is no special difficulty) is not necessary. A reader may simply memorize the form of the ten possible symbols which may appear for decimal numbers 0 to 9. The numbers 1 through 9 are illustrated in Fig. 2. A card similar to Fig. 2 may be trimmed from the top to the row of pips and placed directly under the readout by an inexperienced reader to make a quick determination of a digit. In this code, a digit requires a maximum of 0.4 sec out of a 1-sec interval, and the running together of 10-sec intervals is completely eliminated.

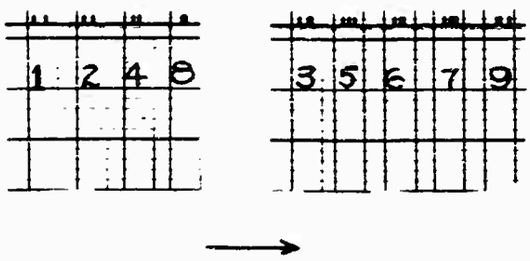


(a)



(b)

Fig. 1 - Samples of (a) previously-used digital method and (b) presently-used binary method of time code generation at the U.S. Naval Space Surveillance Stations



READ IN DIRECTION OF ARROW

(CHART RATE: 5mm/SEC)

Fig. 2 - Illustration of binary-coded digits from 1 to 9

Figure 3(a) shows the front panel of the new digital clock and coder. The "stop" button at the lower right is used to interrupt the 100-pps output of the first decimal divider. When any of the "reset" buttons is depressed, the count registered on the decimal indicator directly above is reduced to zero. Each "advance" button increases the associated indicator by one count each time the button is depressed. Figure 3(b) shows the layout of printed circuit boards. At the right-hand end of the front row is a rheostat control knob which is used to adjust current consumption for maximum economy. The overall system is shown in Fig. 4, and circuit details are given in additional drawings which will be discussed later.

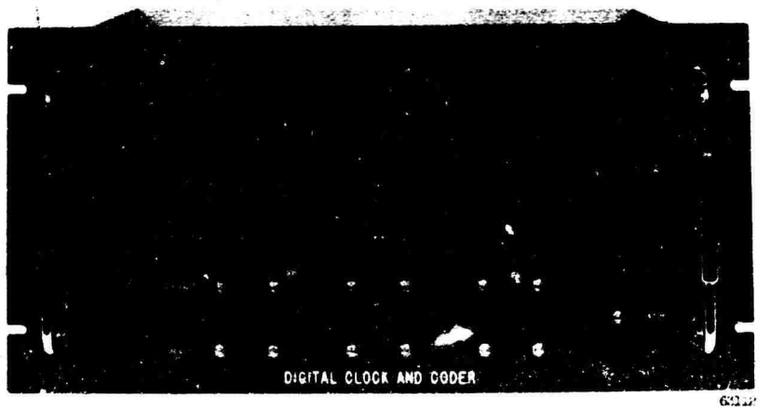
GENERAL DESCRIPTION OF CIRCUITRY

Referring to Fig. 4, a 1000-pps signal is introduced to pin 13 of the reset-pulser-marker card HA-2 (see Fig. 5). The reset-pulser-marker provides triggering pulses which drive decade counter CO-9. The counter CO-9 drives CO-8, and so on to the last counter CO-1. All of these counters are decade dividers,* except CO-3 and CO-5 which divide by six. Together they maintain a count of input pulses in terms of hours, minutes, seconds, and decimal fractions of a second in binary format. Decimal indicators DI-1 to DI-6 † are coupled to the corresponding decade counters CO-1 to CO-6 to give visual reading of time in decimal digits.

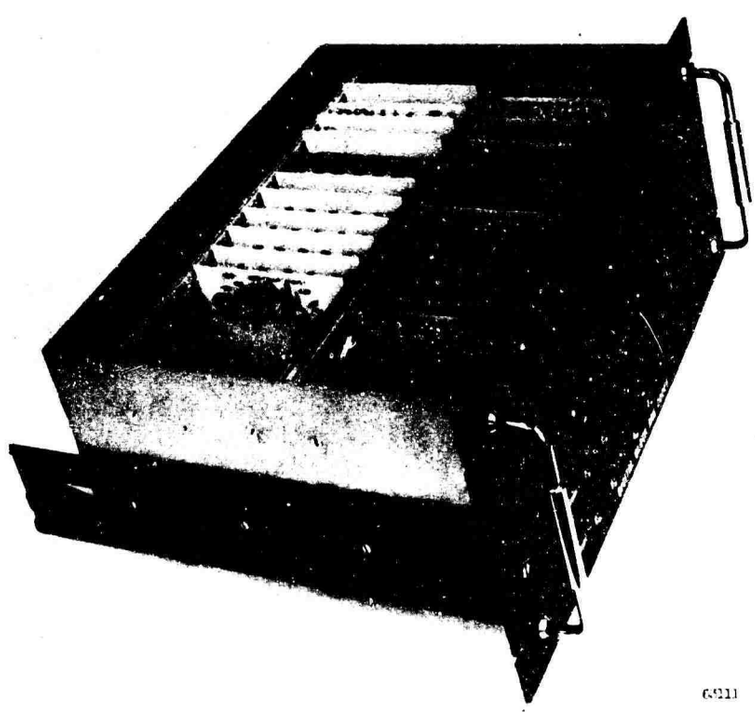
The count stored in counters CO-1 to CO-5, inclusive, are gated through the fast gates HA-3A to E (see Fig. 6) which are controlled by the count on CO-7 through emitter-follower card HA-5B. Gate control connections to the five fast gates are in parallel. Consequently, each gate passes the signals from one of its input lines 10, 8, 3, or 2 to the output lines 15 simultaneously with all the other fast gates. The fast-gate cards are wired to gate the input according to the following schedule:

Time Interval (Fraction of Sec)	Gated Input Signal Connections (CO's to HA-3's)	Value
0.0-0.1	None (-12 volt, connected to internal source)	None (Marker)
0.1-0.2	14 to 2	2^3
0.2-0.3	12 to 3	2^2
0.3-0.4	7 to 8	2^1
0.4-0.5	5 to 10	2^0
0.5-0.0	None (gate closed for last 0.5 sec of interval)	-

*The decimal counting units are Beckman/Berkely, Model 750. The divide-by-six counters are modified units of the same type.
†The decimal indicators are Beckman/Berkeley, Model 751.



(a)



(b)

Fig. 3 - (a) View of front panel and (b) view showing printed circuit boards of the new digital clock and coder unit

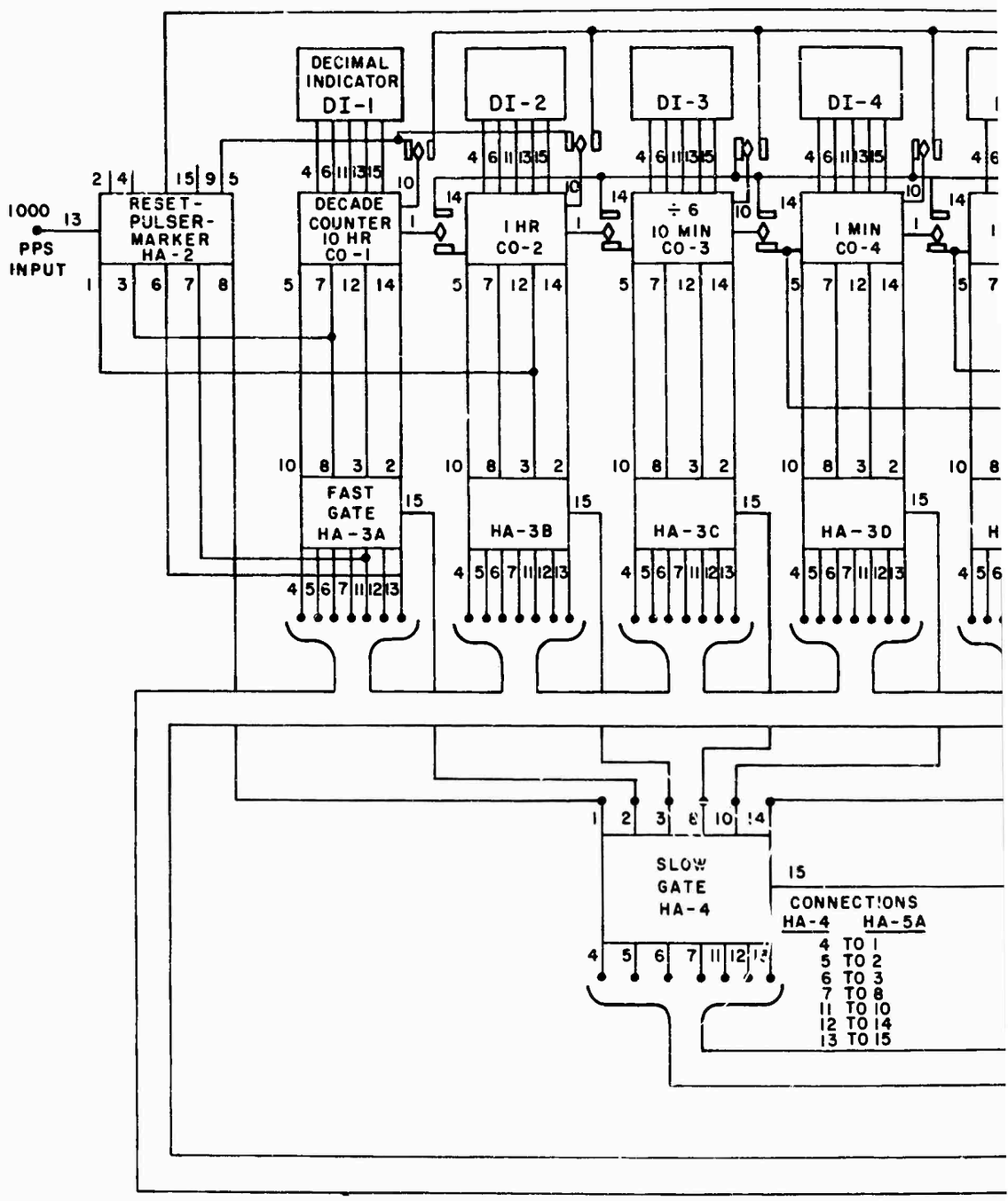
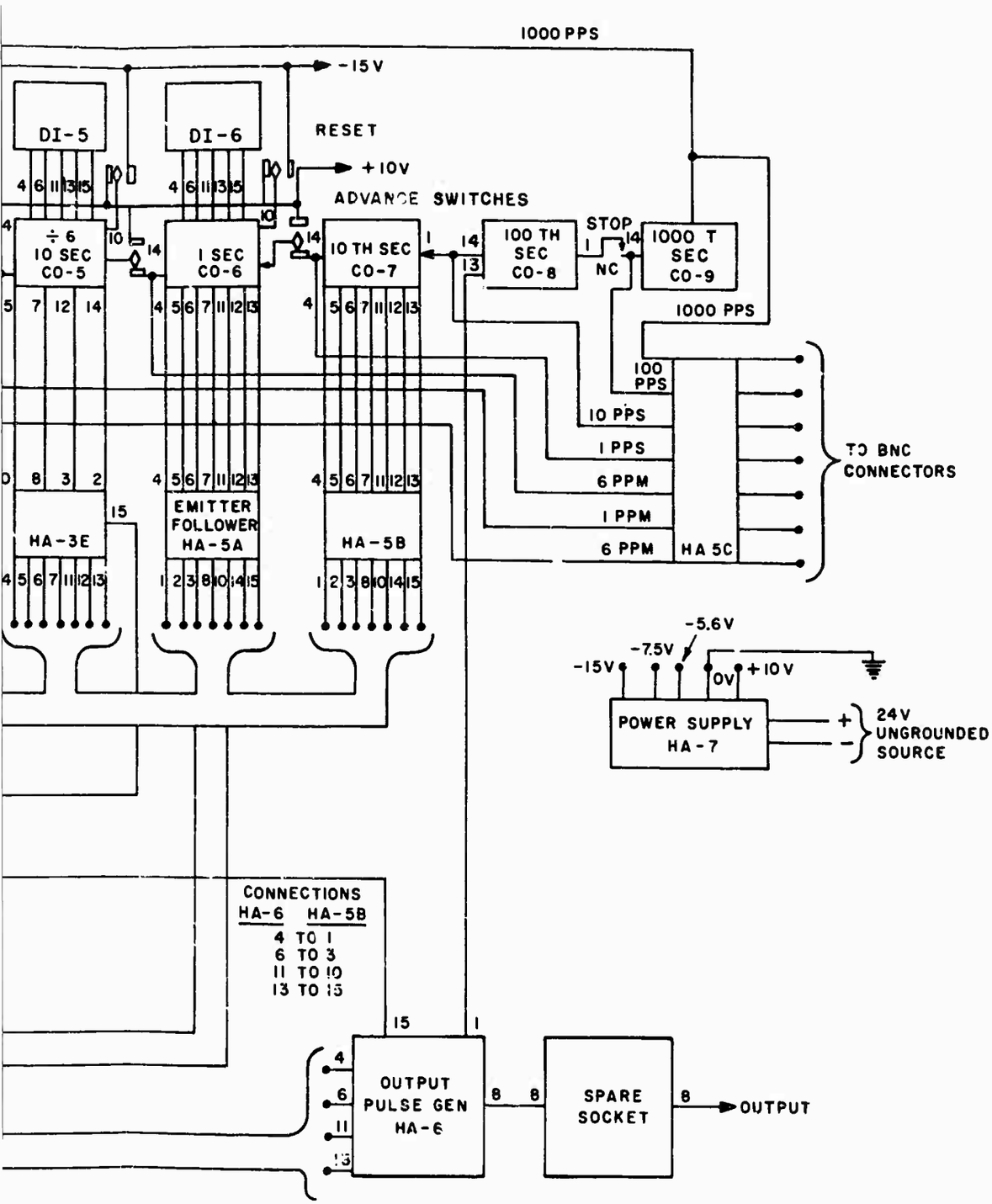
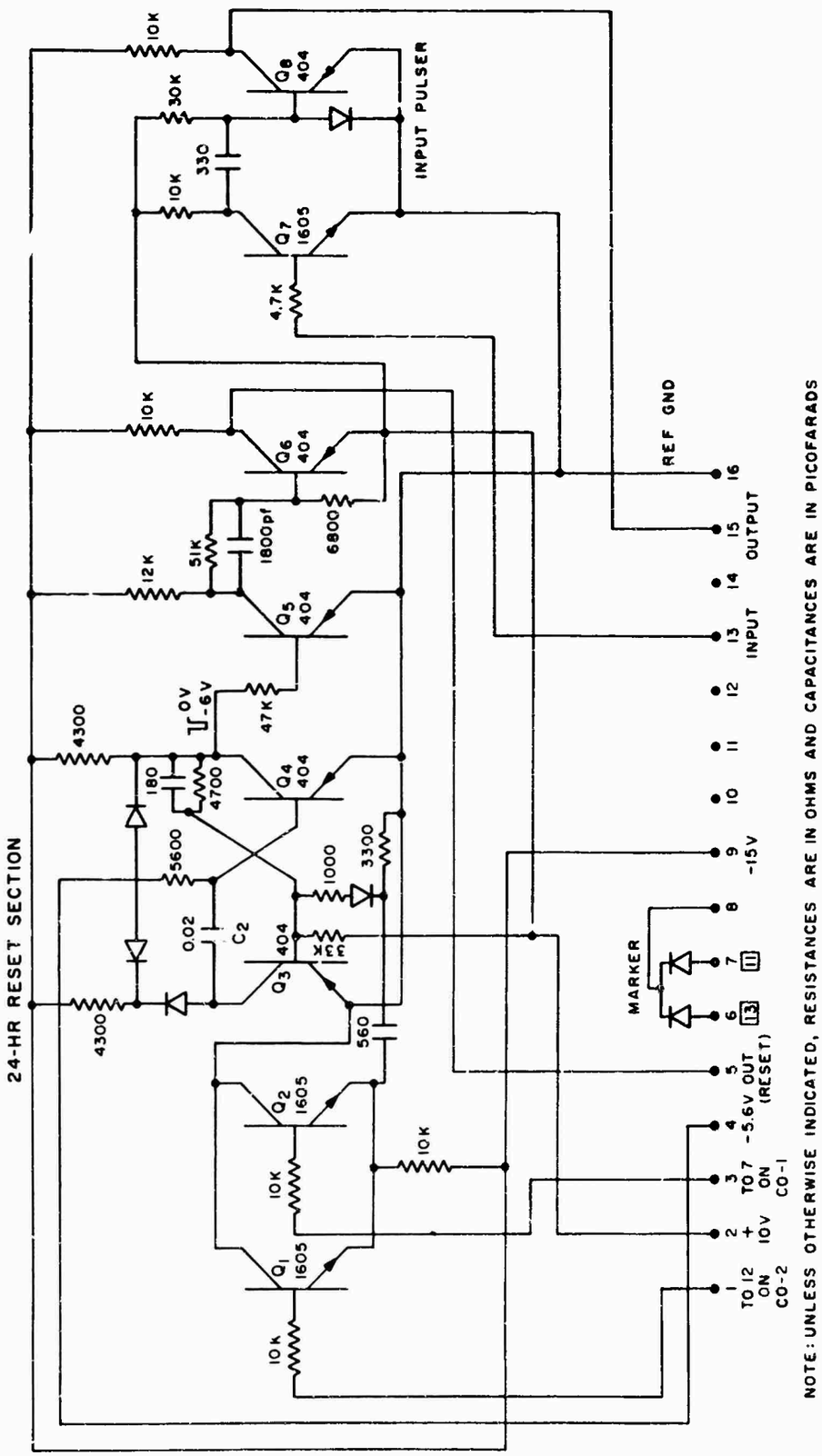


Fig. 4 - Diagram of digital clo



l clock and coder interconnections



NOTE: UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS AND CAPACITANCES ARE IN PICOFARADS

Fig. 5 - Diagram of reset-pulser-marker (HA-2, Fig. 4)

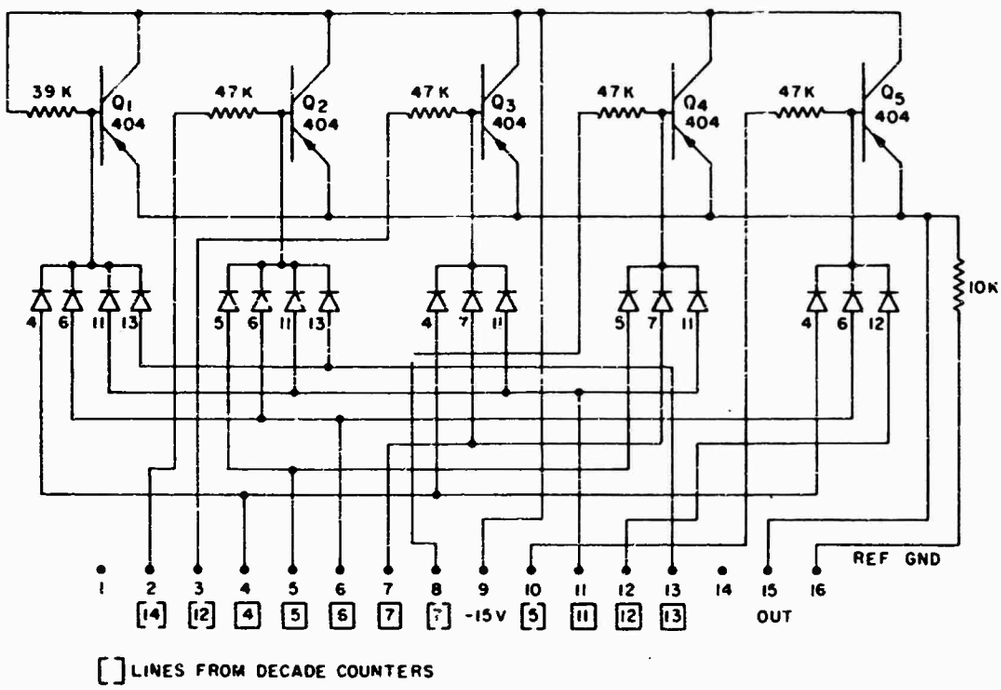


Fig. 6 - Diagram of fast gate (HA-3, Fig. 4)

The five simultaneous outputs of the fast gates are coupled to the slow gate HA-4 (Fig. 7) on input lines 2, 3, 8, 10, and 14. (Line 1 is used for the four-pip marker.) The slow gate is switched by the voltages derived from CO-6 through emitter-follower card HA-5A (Fig. 8) and consequently switches only one tenth as fast as the fast gate. The slow-gate card is wired to gate its inputs according to the following schedule:

Time Interval (sec)	Gated Input Signal Connections (CO's to HA-4)
0-1	None (-12 volt, four-pip marker)
1-2	10's of hours (line 2)
2-3	Hours (line 3)
3-4	10's of minutes (line 8)
4-5	Minutes (line 10)
5-6	10's of seconds (line 14)
6-10	None

Complete time information is contained in the output of line 15 of the slow gate in the form shown in Fig. 9(a). Each negative pulse has a 0.1-sec duration so that pulses in adjacent positions join together. Further, no pulses appear between 6 to 9 sec in each 10-sec interval. It is desirable to have pips to indicate the beginning of each second and to have gaps between them of approximately the same width as the pips. The output pulse generator HA-6 (Fig. 10) inserts the desired pulses during the first 10th second of

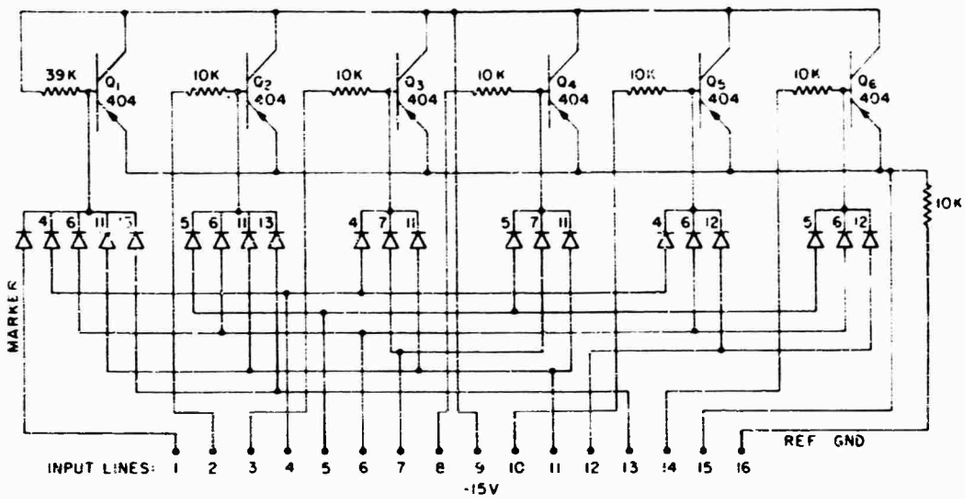


Fig. 7 - Diagram of slow gate (HA-4, Fig. 4)

the 6th through 9th seconds. It also shortens the 0.1-sec pulses to 40 msec so that adjacent pulses are separated by 60 msec. The output after processing in card HA-6 is shown in Fig. 9(b).

Since some recorders are designed for dc input and others for ac input, converting the negative time code pulses to the necessary form is done in a separate circuit external to the digital clock and coder. A spare socket has been reserved for possible inclusion of such circuitry in the chassis if it proves advantageous in the future.

The power supply circuit HA-7 (Fig. 11) supplies the correct operation voltages when powered by an ungrounded source of approximately 24 volt dc. CAUTION: Never use a grounded power supply as this would bypass certain parts of the internal circuitry and may cause damage.

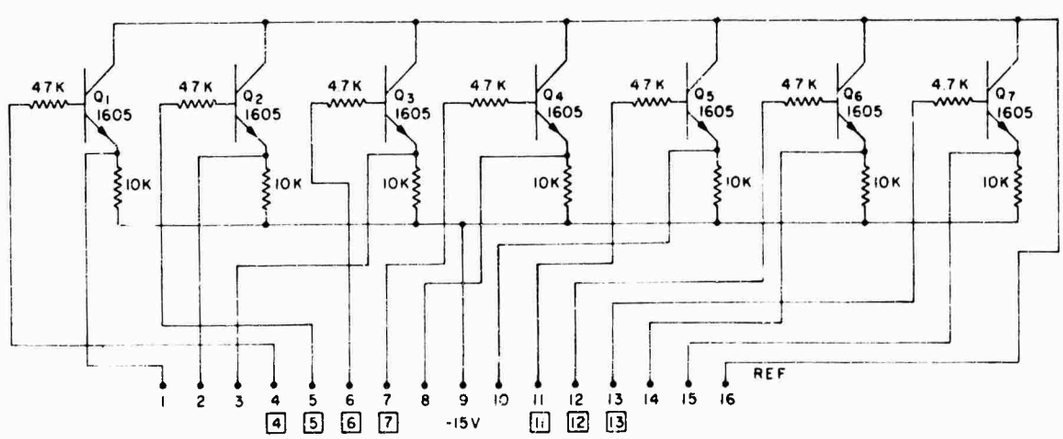


Fig. 8 - Diagram of emitter followers (HA-5, Fig. 4)

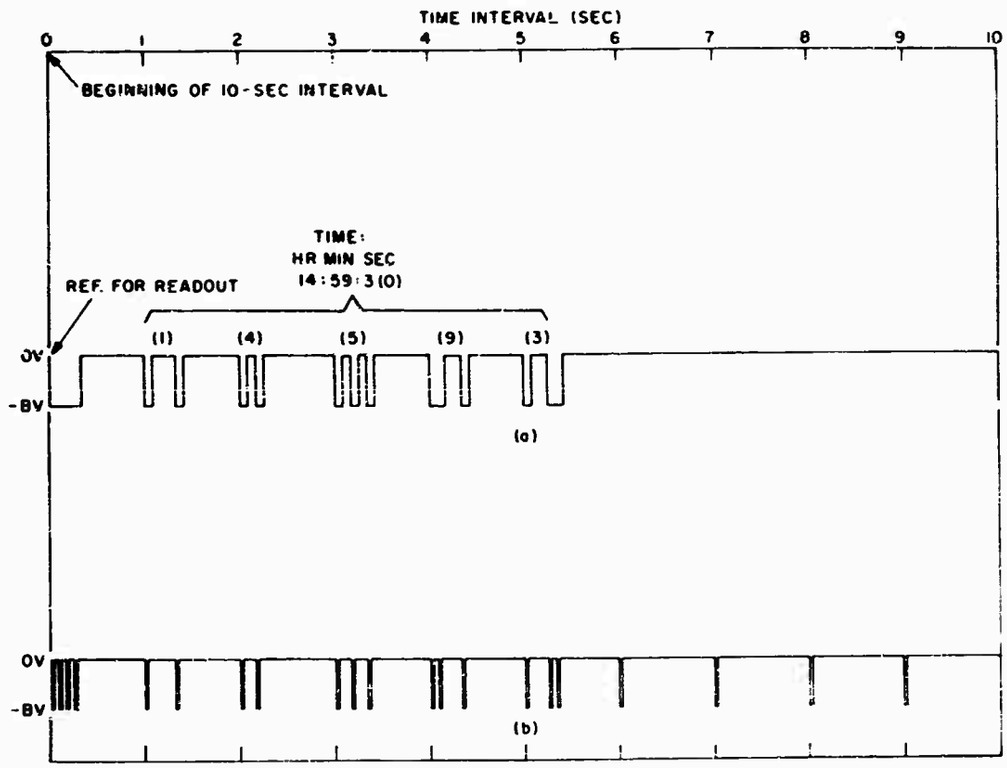


Fig. 9 - (a) Time information output from line 15 of slow gate HA-4 (Fig. 7); (b) output on line 8 of output pulse generator showing insertion of 1-sec pips between 6 and 9 sec and pulse-width compression

DETAILED DESCRIPTION OF CIRCUITRY

Decade Counters

The decade counters CO-1, 2, 4, 6, 7, 8, and 9 (Beckman/Berkely Counting Unit, Model 750-A) are commercially available as plug-in cards. Power requirements are +10 and -15 v. Driving requirements are voltage pulses of +10 to +25 v, 1 μsec minimum duration, and 0.5 μsec rise time. Details of circuit functioning are given in the manufacturer's manual for this unit. Voltage levels on both sides of each binary pair of transistors are brought out to the terminal strip. Lines to the collectors of the eight transistors are numbered as follows:

Transistor No.	Line No.	Transistor No.	Line No.
Q_1	4	Q_2	5
Q_3	6	Q_4	7
Q_5	11	Q_6	12
Q_7	13	Q_8	14

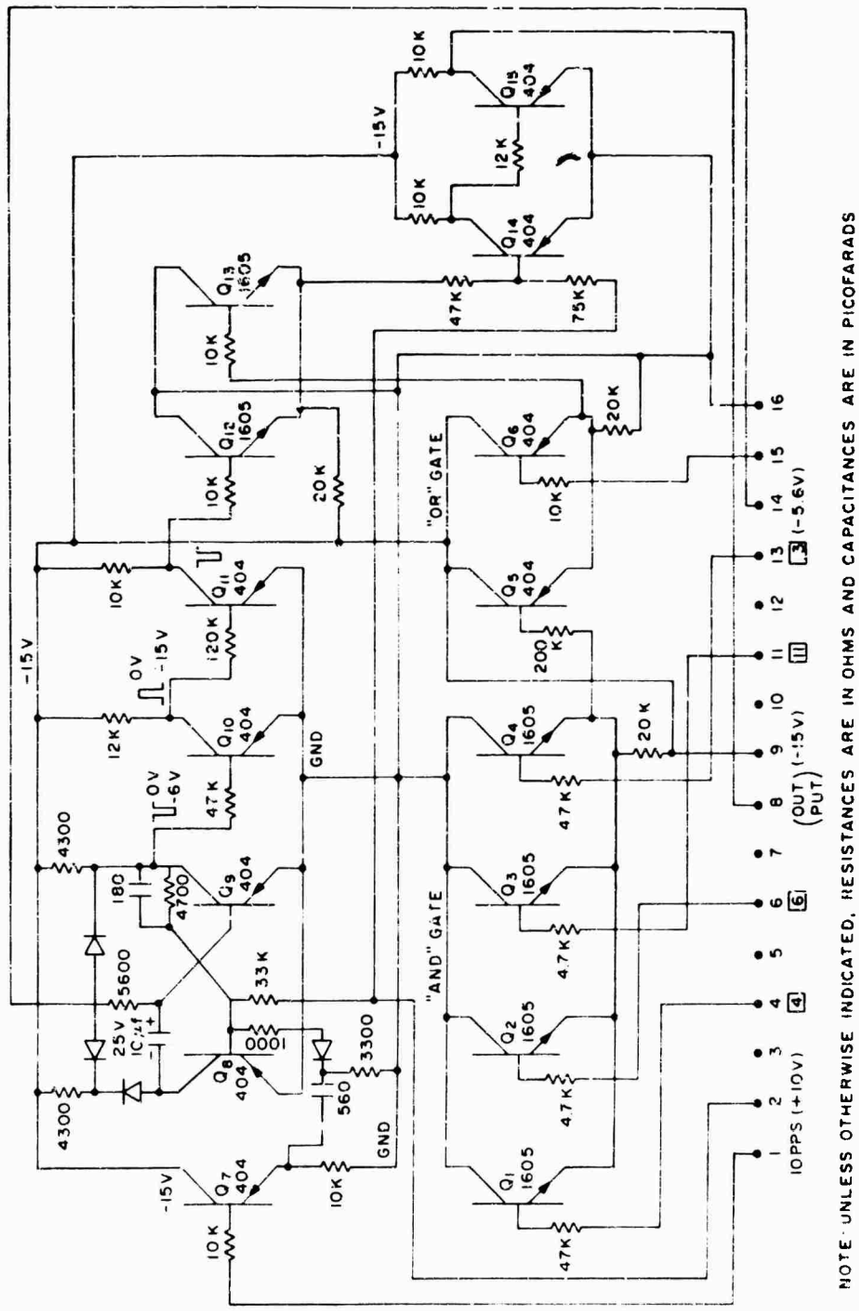


Fig. 10 - Diagram of output pulse generator (HA-6, Fig. 4)

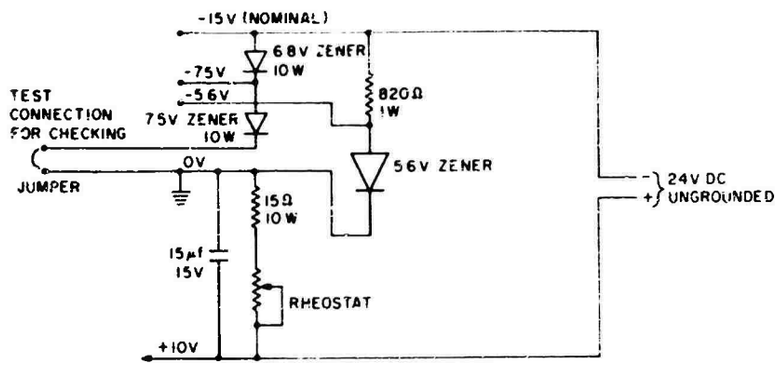


Fig. 11 - Diagram of power supply circuit (HA-7, Fig. 4)

A count of zero corresponds to zero voltage and a count of one corresponds to -13 v on the even-numbered transistors (Q_2, Q_4, Q_6, and Q_8); the reverse is true on the odd-numbered set. The even-numbered set was selected as the source of the count for the coding circuitry.

In the modified counting units CO-3 and CO-5, Model 750-A, division by six is obtained by modification of the decade divider, Type 750-A, in such a way as to preserve the correct binary count on its output lines. The fourth binary is not required for division by six and has been removed. Instructions for the modification are as follows:

1. Remove lines from 13 to collector of Q_7. Remove line from 14 to collector of Q_8.
2. Connect 39-kohm resistor from line 9 (-15 v) to pin 13.
3. Connect pin 14 to pin 15.
4. Remove CR_5.
5. Disconnect CR7 from base of Q_7 and connect to base of Q_5.
6. Increase C_7 to 220 $\mu\mu$f. Remove CR_6. Connect C_7 to base of Q_6.
7. Remove C_{10}.
8. Disconnect line from R_{13} to collector of Q_8 and reconnect to collector of Q_6.
9. Remove R_{26}, R_{29}, Q_7, and Q_8.

Decimal Count Indicators DI-1 to 6 (Beckman/Berkely, Model 751-A)

This unit is coupled to the binary levels on the decimal counters, as indicated on Fig. 4, and gives a visual reading in decimal digits of the binary count contained in the CO counter series. Circuit details are given in the manufacturer's instruction manual for this unit. Power requirements are 40 ma at -7.5 v.

Reset-Pulser-Marker (HA-2)

The reset-pulser-marker card performs three distinct functions: (a) it generates suitably shaped pulses to drive CO-9, (b) it resets CO-1 and CO-2 to 00 when they reach 24, and (c) it assembles the pulse for the four-pip marker of the slow gate HA-4.

Pulser– A 1000-pps input signal arrives at pin 13 (HA-2) and is fed to Q_7 which passes, as a square wave, the positive part of the input waveform and rejects the negative phase. The pulse appears inverted on the collector of Q_7. This is differentiated and applied to the base of Q_8, which is normally cut off. The negative spike, which is coincident with the leading edge of the driving pulse, causes Q_8 to conduct momentarily, generating a positive pulse sufficient to drive CO-9. The positive spike, which is coincident with the trailing edge of the driving pulse, does not pass through Q_8.

24-Hour Reset– Line 7 from CO-1 and line 12 from CO-2 are connected to the bases of Q_2 and Q_1, respectively, which forms an "and" circuit. These lines become negative when the hours count reaches 24. The negative pulse generated on the emitters of Q_1 and Q_2 at that moment is coupled through a capacitor to the monostable multivibrator Q_3 and Q_4.* A negative pulse of about 6 v is generated on the collector of Q_4 for a period determined by the value of C_2. This produces a rise in the collector voltage of Q_5. The base voltage of Q_6 is adjusted slightly negative with respect to the emitter by means of a voltage divider between +10 and -15 v so that the collector voltage is about +9.5 v. When a positive-going pulse is applied to its base, Q_6 is cutoff. This causes the collector voltage to fall by about 20 v, which is sufficient for resetting CO-1 and CO-2. The output pulse of Q_6 is connected from line 5 of HA-2 to line 10 of the Model 750 counters CO-1 and CO-2 through the reset switches shown on Fig. 4.

Marker– This is part of the circuit for generating the four-pip marker for the slow gate. If either line 11 or 13 is in the zero state, line 8 will be held at ground potential. During the first 0.4 sec of each second (Fig. 9), the lines 11 and 13 are negative. This allows a 0.4-sec negative output from the marker portion of the slow gate, which will be discussed later. (The marker is located on the pulser-reset-marker card because of a lack of the required number of terminals on the slow-gate card.)

Emitter Followers (HA-5)

Direct coupling of the multiple loads of the gating cards to the decade dividers would cause faulty functioning of the flip-flop circuits. To avoid this, each of the control circuits from CO-6 and CO-7 are coupled through an emitter follower for isolation. A similar card (HA-5C) is used for connecting oscilloscopes, etc. for test purposes. Figure 12 shows the voltage states on the output lines from the decade dividers. This diagram is useful for checking out circuit functioning. Each emitter-follower card has seven independent circuits. When the transistor is cut off (negative voltage on the base), very little power is called for. When the base is reduced to zero voltage by the input signal, the transistors are conducting and can deliver the relatively large amount of power to the gates to clamp the bases of the transistors in those circuits to the zero level.

Fast Gates (HA-3)

The fast gates are controlled by the voltage levels derived from CO-7. Gating of input voltages to the bases of Q_1 to Q_5 is obtained by clamping the bases to zero, except for the tenth of a second that the input is to be gated. It is clear from reference to Fig. 12 that this requirement will be met by the following combinations of inputs from CO-7.

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*The monostable multivibrator is Preferred Circuit No. PSC 10, "Handbook of Preferred Circuits for Navy Aeronautical and Electronic Equipment, Vol. II," NAVWEPS 16-1-519-2, Bureau of Naval Weapons, Washington, D.C.

Gated Interval (sec)	CO-7 Lines	Fast-Gate Transistor	Circuit to be Gated
0.0 - 0.1	4, 6, 11, 13	Q_1	marker
0.1 - 0.2	5, 6, 11, 13	Q_2	"8"
0.2 - 0.3	4, 7, 11	Q_3	"4"
0.3 - 0.4	5, 7, 11	Q_4	"2"
0.4 - 0.5	4, 6, 12	Q_5	"1"

The lines from the counters CO-1 to CO-5 to the bases of transistors Q_2 to Q_5 of each of the fast-gate cards is coupled through a 47-kohm resistor. This value is large enough to prevent reactions on the counters without resorting to emitter followers for isolation. The gated output of the transistors appears on line 15, whence it is fed to an appropriated line on the slow gate. After 0.5 sec this line remains at the zer level until the beginning of the next 1-sec interval.

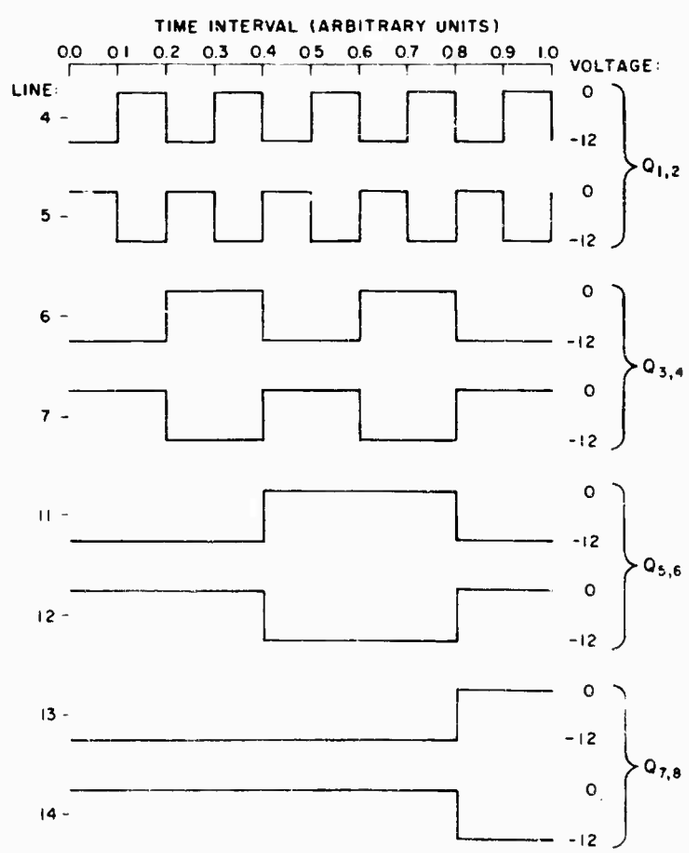

Fig. 12 - Voltage states of decade divider output lines for counts from 0 through 9 for an arbitrary time interval.

Slow Gate (HA-4)

The behavior of the slow gate resembles that of the fast gate, but the switching rate is only once per second. It has an additional transistor Q_6 which is gated from 5 to 6 sec of each 10-sec interval by the control voltage derived from lines 5, 6, and 12 on CO-6. With the diodes coupled to lines 4, 6, 11, and 13, only Q_1 would be gated for an entire second, which is not desired. To prevent this, an additional diode connected to the marker circuit of HA-2 clamps the base of Q_1 to zero voltage from 0.4 to 1.0 sec to provide the proper interval for the four-pip marker in the final code. The combined output of all the transistors is fed out on line 15 to the output pulse generator HA-6.

Output Pulse Generator (HA-6)

The output pulses from the slow gate contain the complete time code information in the form shown in Fig. 9(a). It is desired to have markers appear each second and to break up the long pulses into two or more short pulses as shown in Fig. 9(b). To do this, transistors Q_1, Q_2, Q_3, and Q_4 form an "and" gate with inputs derived from lines 4, 6, 11, and 13 of CO-7. The only time that these lines are simultaneously negative is over the interval from 0.0 to 0.1 sec. This series of negative pulses is fed to Q_5 of an "or" gate. The code from the slow gate (HA-4) is fed to Q_6 of the same "or" gate. The output of this gate is equivalent to the code in Fig. 9(a), with 0.1-sec pulses added during the seconds which previously lacked them. The combined signal is fed to the base of Q_{13}.

A 10-pps pulse from pin 13 of CO-8 is introduced on pin 1 and fed to Q_7. This pulse goes negative, coincident with the beginning of each 0.1-sec interval. The negative-going pulse drives the monostable multivibrator Q_8, Q_9, producing a negative-going pulse on the collector of Q_9 of about 6 v with a duration of 40 msec. This pulse is converted to a positive-going pulse on the collector of Q_{10} and a negative pulse with respect to ground on Q_{11}. The 10-pps negative pulses are applied to Q_{12}. The output of the "and" gate Q_{12}, Q_{13} is the type desired for the final output (Fig. 9(b)). During the processing the pulses have become somewhat irregular in amplitude and fall short of the zero voltage line in the "no-signal" condition. These pulses are fed to the base of Q_{14} through a 47-kohm resistor. Transistor Q_{14} is biased above ground by a 75-kohm resistor connected to +10 v so that Q_{14} is cut off; its collector runs near -15 v. When a negative pulse from Q_{13}, Q_{12} arrives, the base voltage is shifted in the negative direction, allowing Q_{14} to conduct and raise the collector voltage to zero. Transistor Q_{15} inverts the pulses received from Q_{14} to pulses which go negative with respect to ground, as shown in Fig. 9(b). The output from Q_{15} is delivered via pin 8 to a BNC terminal connector for any further processing to suit the type of load circuit which will be driven by the pulses.

Power Supply (HA-7)

A 24-v, 600-ma power supply is required to provide dc power for the digital clock and coder. This power supply must be ungrounded, and hence cannot be used in combination with other units which would place a ground on it. The zener diodes provide regulated -14.3, -7.5, and -5.6 v. The +10-v supply is not regulated. By eliminating external grounds, both positive and negative voltages are obtained without resorting to expensive (and electromagnetically noisy) dc-dc convertors. The largest load current is drawn through the -7.5 v zener diode. Jumpered contacts are provided between this zener and ground so that a milliammeter may be inserted to measure the current. The current fluctuates with time as the various counters are switched. By adjusting this current to a value near zero for periods of minimum zener current, minimum power consumption will be obtained without adversely affecting the regulating properties of the power supply.

ACKNOWLEDGMENTS

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5. AUTHOR(S) *(Last name, first name, initial)*

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13. ABSTRACT

A transistorized digital clock and coder unit has been developed which is being used as part of the time standard equipment at the U.S. Naval Space Surveillance Stations in Hawkinsville, Georgia, Red River, Arkansas, and Raymondville, Texas, which were instrumented in 1965. This unit is powered by a 24-v battery supply and is capable of 24 hours of emergency service in case of commercial power failure. Decimal digits are read out in binary format at a rate of one decimal digit per second. Each group of pulses comprising a decimal digit is clearly separated from the next pulse group. Once the code is learned, it is much easier to recognize than the one formerly used in the Space Surveillance system. The transistorized circuitry used in this unit has resulted in a considerable reduction in size and power input (12 w) as compared with the vacuum tube unit which has been used for a similar purpose in other Space Surveillance stations. Also, the error in coding due to aging of components has been eliminated since only two levels must be distinguished in the binary logic as compared with the ten voltage levels of the decimal logic in the earlier equipment. The new unit employs two cascaded gates, one switching at 0.1-sec intervals and the other at 1.0-sec intervals.

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Security Classification

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