ESD TDR 65-167
ESTI FILE COPY

R-65-167

ESD RECORD COPY
RETURN TO
SCIENTIFIC & TECHNICAL INFORMATION DIVISION
(ESTI), BUILDING 1211

COPY NR._____ OF_____ COPIES

(FINAL REPORT)

# PROGRAMMING AND OPERATING FOR HIGH DENSITY DRUM SYSTEM

TECHNICAL DOCUMENTARY REPORT NO. ESD-TDR-65-167

JANUARY 1965

ESTI PROCESSED

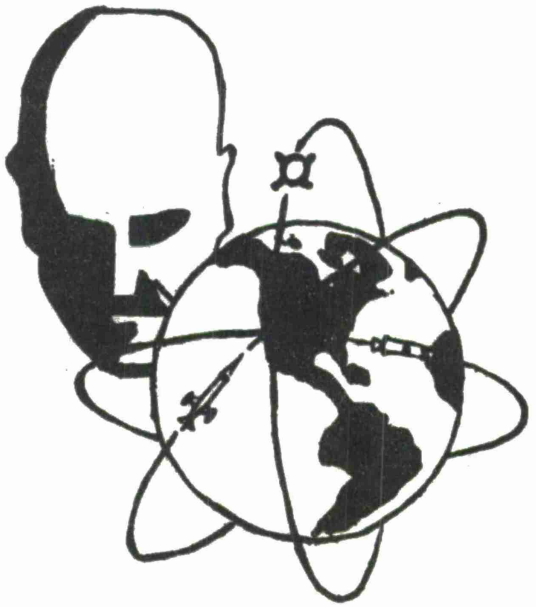
☐ DDC TAB ☐ PROJ OFFICER
☐ ACCESSION MASTER FILE
☐ _____

DATE_____

ESTI CONTROL NR AL 45180

CY NR 1 OF 1 CYS

496L/474L SYSTEM PROGRAM OFFICE
ELECTRONIC SYSTEMS DIVISION
AIR FORCE SYSTEMS COMMAND
UNITED STATES AIR FORCE
L. G. Hanscom Field, Bedford, Massachusetts



AD0612801

(Prepared under Contract No. AF 19 (628)-3395 by the Philco Corporation, A Subsidiary of Ford Motor Company, Communications and Electronics Division, Willow Grove, Pa.)

## DDC AVAILABILITY NOTICE

Qualified requesters may obtain copies from Defense Documentation Center (DDC). Orders will be expedited if placed through the librarian or other person designated to request documents from DDC.

## DISSEMINATION NOTICE

Copies available at Office of Technical Services, Department of Commerce.

## LEGAL NOTICE

When US Government drawings, specifications or other data are used for any purpose other than a definitely related government procurement operation, the government thereby incurs no responsibility nor any obligation whatsoever; and the fact that the government may have formulated, furnished, or in any way supplied the said drawings, specifications, or other data is not to be regarded by implication or otherwise as in any manner licensing the holder or any other person or conveying any rights or permission to manufacture, use, or sell any patented invention that may in any way be related thereto.

## OTHER NOTICES

Do not return this copy. Retain or destroy.

ESD-TDR-65-167

# PROGRAMMING AND OPERATING FOR HIGH DENSITY DRUM SYSTEM

TECHNICAL DOCUMENTARY REPORT NO. ESD-TDR-65-167

JANUARY 1965

496L/474/ SYSTEMS PROGRAM OFFICE
ELECTRONIC SYSTEMS DIVISION
AIR FORCE SYSTEMS COMMAND
UNITED STATES AIR FORCE
L. G. Hanscom Field, Bedford, Mass.

(Prepared under Contract No. AF 19(628)-3395
by the Philco Corporation, a Subsidiary of the
Ford Motor Company, Communications and
Electronics Division, Willow Grove, Pa.)

# PROGRAMMING AND OPERATING FOR HIGH DENSITY DRUM SYSTEM

## ABSTRACT

This report gives a programming description of the High Density Drum System. The purpose of this report is to ensure effective implementation of the High Density Drum System in the development of computer programs and to ensure efficient operation of the High Density Drum with the Philco 2000 Model 212 Computer. Included in this report is a description of operating controls and operating instructions.

## REVIEW AND APPROVAL

This technical documentary report has been reviewed and is approved.

Thomas O. Wear

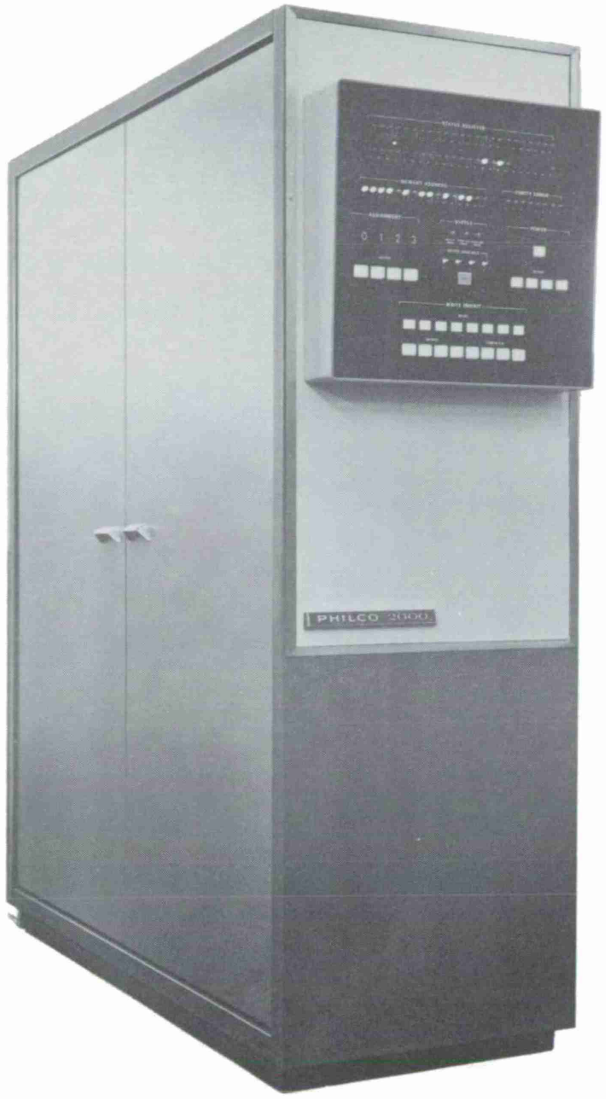
THOMAS O. WEAR
Colonel, USAF
System Program Director
496L/474L System Program Office
Deputy for Surveillance
and Control Systems

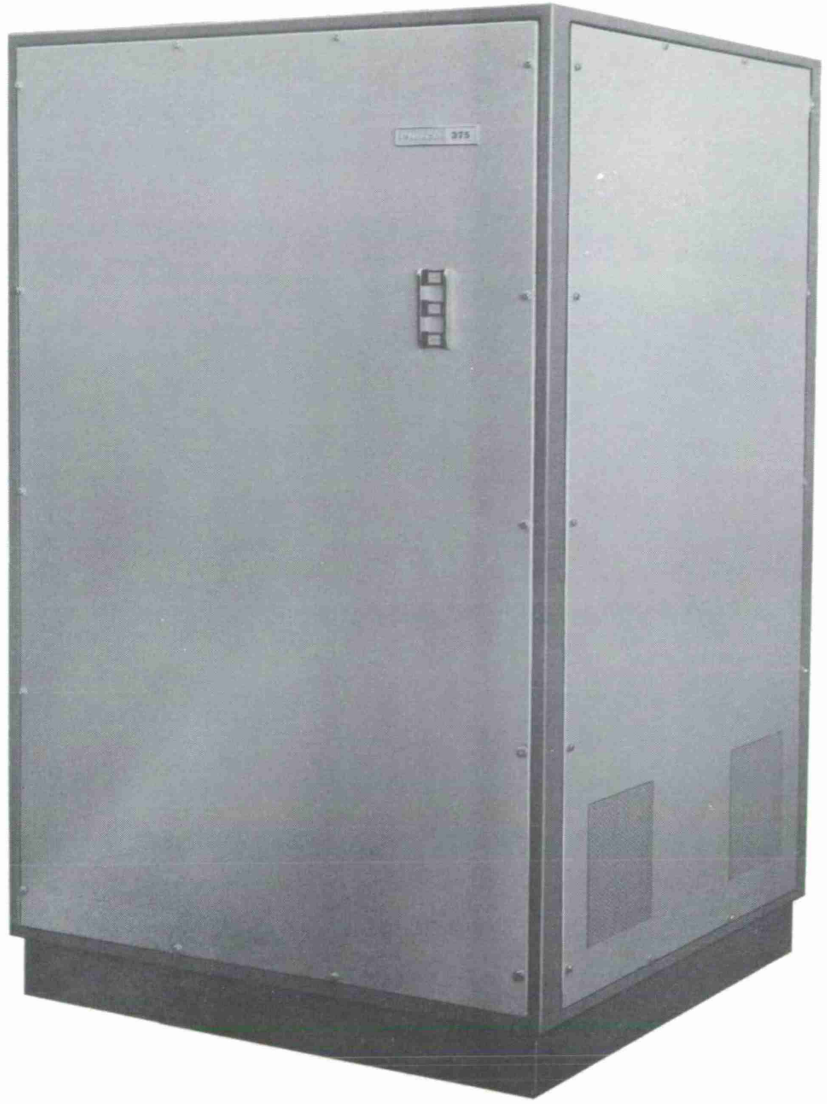
CONTENTS


| Section | | Page |
|---|---|---|
| 1. | INTRODUCTION | 1 |
| 2. | SYSTEM DESCRIPTION | 2 |
| 3. | DATA RATES | 3 |
| 4. | COMMANDS | 4 |
| 5. | COMMAND STRUCTURE | 5 |
| 6. | STATUS REGISTER FORMAT OR "Q" REGISTER FORMAT | 7 |
| 7. | ACCEPTANCE/REJECTION OF COMMANDS | 10 |
| 8. | RESUME MODE | 11 |
| 9. | RELATIVE ADDRESS MODE (ZERO LATENCY) | 13 |
| 10. | DATA OVERFLOW | 14 |
| 11. | WRITE INHIBIT AREAS | 15 |
| 12. | INTERRUPTS | 17 |
| | 12.1 End Interrupt | 17 |
| | 12.2 Fault Interrupt | 17 |
| 13. | FAULTS | 18 |
| 14. | OPERATING CONTROLS | 20 |
| 15. | POWER TURN-ON PROCEDURE | 24 |
| 16. | POWER FAILURE PROCEDURE | 25 |
| 17. | POWER TURN-OFF PROCEDURE | 26 |
| 18. | DEVICE ASSIGNMENT | 27 |

# ILLUSTRATIONS


| Figure | | Page |
|---|---|---|
| Frontispiece | Philco Model 2371 Expandable Drum System | vi |
| 1. | Format of Computer "D" Register | 5 |
| 2. | Status Register and "Q" Register Format | 9 |
| 3. | Control Panel Layout | 21 |
| 4. | Drum Motor Control Panel | 23 |



Philco Model 2371 Expandable Drum System

# SECTION 1

# INTRODUCTION

This report gives a programming description of the High Density Drum System. The purpose of this report is to ensure effective implementation of the High Density Drum System in the development of computer programs and to ensure efficient operation of the High Density Drum with the Philco 2000 Model 212 Computer. Included in this report is a description of operating controls and operating instructions.

## SECTION 2

## SYSTEM DESCRIPTION

The High Density Drum System is a medium capacity, random access data storage facility specifically intended for use with the Philco Model 212 Central Processor. The drum system time shares the 1.5 microsecond core storage with the computer and all other input/output devices. The system is designed to allow access to any individual word, or multiple of words up to a maximum of 8,192 words per instruction.

The High Density Drum System consists of a drum controller and one to four drums. The system capabilities are:

| | |
|---|---|
| One (1) Drum | 2,097,152 seven (7) bit characters;<br>262,144 fifty-six (56) bit words. |
| Two (2) Drums | 4,194,304 seven (7) bit characters;<br>524,288 fifty-six (56) bit words. |
| Three (3) Drums | 6,291,456 seven (7) bit characters;<br>786,432 fifty-six (56) bit words. |
| Four (4) Drums | 8,388,608 seven (7) bit characters;<br>1,048,576 fifty-six (56) bit words. |

# SECTION 3

# DATA RATES

The average or effective data rates are affected by:

a. Frequency of drum commands.

b. Number of words transferred on a given command.

c. The location of the addressed heads with respect to the word addressed in the drum command. Assuming the addressed word has just passed the head, 35 milliseconds would be required to place the addressed word under the head.

d. Use of relative addressing.

The maximum (or instantaneous) data rate of the drum system is 240 Kc (word rate) between the High Density Drum Controller and core memory.

# SECTION 4

# COMMANDS

The drum system recognizes two commands: the READ Command, which specifies that information transfer is to be from the drum system to core memory, and the Write Command, which specifies that information transfer is to be from the core memory to the drum system. Only one command may be stored in the drum controller at any one given time because once a command has been accepted by the drum controller, no further instructions will be accepted until the system returns to a non-busy status.

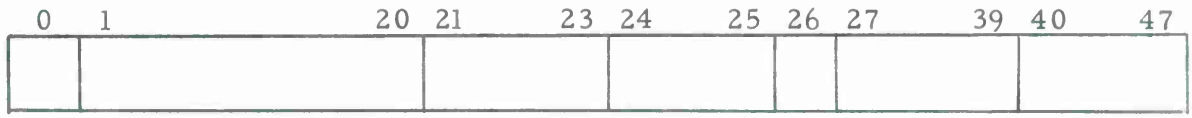
The Interrogate Command is not recognized as a drum system command since it requires no action by the Drum System. The Interrogate Command transfers the Drum System Status Register to the "Q" Register in the 212 Central Processor. For the remainder of this report the Interrogate Command will be treated as a drum system command.

## SECTION 5

## COMMAND STRUCTURE

The Drum System Commands are issued by placing the Drum Command (Read, Write, Interrogate) in the "D" Register of the 212 Central Processor, and issuing a TIO Instruction. The TIO instruction contains the Core Memory Starting Address in the PR (V) field.

The format of the "D" register is shown in Figure 1.




| | |
|---|---|
| Bit 0 | Resume |
| Bits 1 through 20 | Word starting address bits 1 and 2 specify the drum number (D0 - D3).<br><br>Bits 3 through 7 specify the band number (Band 0 - Band 31).<br><br>Bits 8 through 20 specify the discrete word starting address (word 0 - 8, 191). |
| Bits 21 - 23 | Specify the controller number (Controller 0 - 7). |
| Bits 24 and 25 | Specify the computer number (Computer 0 - 3). |
| Bit 26 | Not used. |
| Bits 27 - 39 | Specify the number of words to be processed (1 - 8, 192). |
| Bits 40 - 47 | Specify the command: core to drum $(0102)_4$, drum to core $(0201)_4$, status to "Q" $(0200)_4$. |

Figure 1. Format of Computer "D" Register

The functions of the various bits in the "D" register are outlined as follows:

a. The Resume Bit (Bit 0 of the "D" register) signifies that the drum is to resume reading or writing at the Core Memory Starting Address specified by the CMA register of the drum controller. When the Resume bit is not set, the core memory starting address is supplied by the memory address field PR (V) of the TIO instruction.

b. The Word Starting Address for the drum is given by bits 1 through 20.

1. Bits 1 and 2 specify the drum address (Drum 0 - Drum 3).

2. Bits 3 through 7 specify the band address (Band 0 - Band 31).

3. Bits 8 through 20 specify the discrete word starting address (Word 0 - Word 8, 191).

c. The controller number is specified by bits 21 through 23. These bits decode controller 0 - controller 7.

d. The computer number is specified by bits 24 and 25. These bits decode as Computer 0 - Computer 3.

e. Bit 26 of the "D" register is not used or decoded.

f. The number of words to be processed is specified by bits 27 through 39. These bits are decoded as 1-8, 192. All zeros are decoded as 8, 192 words to be processed.

g. The drum command (Core to Drum or Drum to Core) is specified by bits 40 through 47. The core to drum command (WRITE) is $(0102)_4$. The drum to core command (READ) is $(0201)_4$.

The Interrogate Command (Status to "Q") is $(0200)_4$. To issue an Interrogate Command it is only necessary to load the "D" register with the command and controller number (Bits 21 through 23) and issue a TIO in PR. If only one controller is in the system, it is not necessary to load the controller number in "D".

## SECTION 6

## STATUS REGISTER FORMAT OR "Q" REGISTER FORMAT

The format of the Status Register is shown in Figure 2.

The functions of the various bits in the Status Register are outlined as follows;

a. The Resume Bit (Bit 0) when set to a one signifies that the last order was not a Relative Address Command or that a timing error did not occur on the last order. This signifies that the Core Address stored in the Drum Controller can safely be used to retry commands that have been terminated or that the programmer can use a Resume to continue sequentially loading/unloading Core Memory from/to the Drum System.

b. The updated Word Starting Address or the Drum System is given by bits 1 through 20.

   1. Bits 1 and 2 specify the Drum Address (Drum 0-Drum 3).

   2. Bits 3 through 7 specify the Band Address (Band 0-Band 31).

   3. Bits 8 through 20 specify the discrete Word Starting Address (Word 0 - Word 8191).

c. Bits 21 through 23 specify the controller number (controller 0-controller 7). The controller number is meaningless in a single controller system.

d. Bits 24 and 25 specify the computer number to which the Drum System was last assigned. These bits are decoded as Computer 0 - Computer 3. The computer number is meaningless for a single computer system.

e. Bit 26 of the Status Register is meaningless.

f. Bits 27 through 39 specify the number of words remaining to be processed. These bits are decoded as 0 - 8191 words to be processed. For a Relative Address Command rejected due to the Drum Write Inhibit or unavailable decode of 0 means 8192 words remaining to be processed.

g. Bits 40 through 47 give Drum System Status. For a detailed discussion refer to Section 13 (Faults).

1. Bit 40 - Channel Busy. Channel Busy is meaningless for a single controller system.

2. Bit 41 - Controller Busy. Controller Busy specifies that the controller is processing a Read/Write Command.

3. Bit 42 - Mechanical Fault.

4. Bit 43 - Write Inhibit.

5. Bit 44 - Timing Error.

6. Bit 45 - Memory Cycle Error.

7. Bit 46 - Parity Error.

8. Bit 47 - Last Command or Command being processed is a Write Command.

| | |
|---|---|
| Bit 0 | Resume (1) |
| Bits 1 through 20 | Updated word starting address<br><br>Bits 1 and 2 - Drum Number<br>Bits 3 through 7 - Band Number Updated<br>Bits 8 through 20 - Word Address Updated |
| Bits 21 through 23 | Controller Number |
| Bits 24 and 25 | Computer Number |
| Bit 26 | Not Used |
| Bits 27 through 39 | Specify the number of words remaining to be processed. |
| Bit 40 | Channel Busy |
| Bit 41 | Controller Busy |
| Bit 42 | Mechanical Fault |
| Bit 43 | Write Inhibit |
| Bit 44 | Timing Error |
| Bit 45 | Memory Cycle Error |
| Bit 46 | Parity Error |
| Bit 47 | Read (0) Write (1) |

Figure 2. Status Register and "Q" Register Format

## SECTION 7

## ACCEPTANCE/REJECTION OF COMMANDS

The Drum command (READ/WRITE) will be accepted only if the following conditions exist:

a. The controller is not busy.

b. The controller has no timing errors on the previously selected drum and no timing errors on the drum to be selected by this command.

c. The selected device is available.

d. The command is not a Write command with a Drum Starting Address which lies within a Write Inhibited Area.

A Read/Write Command is always either accepted or rejected but not both. When a Read/Write Command is accepted, the instruction following the TIO is skipped. When a Read/Write Command is rejected, the Status Register is automatically loaded to the "Q" register and the instruction following the TIO is executed.

An Interrogate Command is neither accepted nor rejected. The action of the Interrogate Command is to transfer the contents of the Drum Controller Status Register to the "Q" Register of the 212 Central Processor. The instruction following an Interrogate TIO is always executed.

## SECTION 8

## RESUME MODE

When a Read/Write Command is issued to the Drum System with Bit 0 of the "D" Register set to one the command is defined as a Resume Order. A Resume Command discards the PR(V) field of the TIO and uses the Core Memory Address which is stored in the Drum Core Memory Address (CMA) Register.

The resume bit (bit "0" of the status register) will be set to one by the drum controller at the completion or termination of drum instructions (both read and write) other than those making use of the relative addressing feature, except for the case in which a timing error has been detected.

Two methods for using the Resume feature are as follows:

a. When a drum read/write order has been successfully completed, the Drum Status Register contains the complete word starting address of the next higher word (on the drum) and the Core Memory Address (CMA) contains the core memory starting address of the next higher word which would be transferred from/to the drum. Thus, when an order has been completed, the drum system can be interrogated, the "Q" register shifted to the "D" Register, the command portion of the read/write instruction loaded in the "D" Register (bit 40-47), the words to be processed loaded in the "D" Register (bits 27-39), and the next drum TIO instruction can be issued. The PR(V) field of the TIO is not used. The above sequence can be used to read/write successive words from/to the drum and to/from the magnetic core memory.

b. When a drum read/write order has been terminated (not successfully completed) as a result of any error other than a timing error, the drum Status Register contains both the complete word starting address of the word in which the error occurred and the number of words left to be processed; and, CMA* contains the core memory address of the word in error. Thus, when an order has been terminated because of an error, the drum system can be interrogated, the "Q" Register shifted to the "D" Register, and the command portion of the read/write instruction loaded in the "D" Register (bits 40-47). By issuing a TIO instruction, the remaining portion of the previous drum order can be retried.

The Resume feature should not be used following a drum read/write instruction which made use of the Relative Addressing feature; thus, under no condition should it be necessary for the program to set bit "1" of the "D" Register format to the one state when issuing drum read/write orders.

## SECTION 9

## RELATIVE ADDRESS MODE (ZERO LATENCY)

A relative address command is a Read/Write Command which specifies 8,192 words to be processed ("D" Bits 27 through 39 are zero) and the Word Starting Address is zero ("D" Bits 8 through 20 are zero). When a Relative Address Command is used, the average latency time of 17.5 milliseconds to find the starting address is eliminated by processing an entire band in one revolution of the drum.

The latency time is eliminated by determining the present address at which heads are located. This address is added to the Core Starting Address to determine the Core Address for the word address which is approaching the drum heads. When this drum address starts to pass under the drum heads, processing of data is started. Data is processed until the no-data gap is reached, then the remainder of data is processed by resetting the Core Address to the original Core Starting Address, and processing data until the word counter is zero.

NOTE

Do not attempt to use a Resume order following a Relative Address Command since Core Starting Address will not reflect a predictable address.

When using Relative Address Mode the programmer must keep track of the band being processed and Core Memory Starting Address of the command. When a Relative Address Command is terminated due to an error, retry must be made by reissuing the complete order.

## SECTION 10

## DATA OVERFLOW

When a command causes an overflow of data on a given band the remainder of the data is processed on the next higher band. If the command causes overflow of the last band (Band 31) the remainder of the data is processed on Band 0 of the same drum.

Drum addressing is cyclic within each drum connected in the system

For a Write Command which causes overflow to a Write Inhibited Band, the Write Inhibit Fault in Status (Bit 43) is set and the order is terminated, generating a Fault Interrupt.

## SECTION 11

## WRITE INHIBIT AREAS

There are eight write inhibit areas on the drum. These areas represent a total of 65,536 words which may be write inhibited, in increments of 8,192 words per write inhibit area, starting with the last 8,192 words on the drum. The write inhibit switches must be activated from right to left. This ensures that, if a given group of 8,192 words is inhibited, then all words from that group up to and including the last word on the drum (word 262,143) are inhibited.

The Write Inhibit Switches are labeled with the word number of the first word which is write inhibited.

| | |
|---|---|
| Switch 253,952 | Write Inhibits Band 31 or Words 253,952 through Word 262,143. |
| Switch 245,760 | In conjunction with the above switch Write Inhibits Bands 30 and 31 or Words 245,260 through Word 262,132. |
| Switch 237,568 | In conjunction with the above switches Write Inhibits Bands 29-31 or Words 237,568 - 262,143. |
| Switch 229,376 | In conjunction with the above switches Write Inhibits Bands 28-31 or Words 229,376- 262,143. |
| Switch 221,184 | In conjunction with the above switches Write Inhibits Bands 27-31 or Words 221, 184 - 262,143. |
| Switch 212,992 | In conjunction with the above switches Write Inhibits Bands 26-31 or Words 212, 992 - 262,143. |
| Switch 204,800 | In conjunction with the above switches Write Inhibits Bands 25-31 or Words 204,800 - 262,143. |
| Switch 196,608 | In conjunction with the above switches Write Inhibits Band 24-31 or Words 196,608 - 262,143. |

The Device Write Inhibits Switches relate the above switches to a particular device.

EXAMPLE

If device 0 and device 1 are Write Inhibited and device 2 and 3 are not, and Write Inhibit Switches 253, 952 and 245, 760 are on; Words 245, 760 - 262, 143 are Write Inhibited on drums 0 and 1, there would be no areas Write Inhibited for drums 2 and 3.

The computer switches cause the controller to be Write Inhibited for the specified computer in a multicomputer system.

When the Drum Word Starting Address lies within a Write Inhibited area, the Write Inhibit bit of Status (Bit 43) is set and the command is rejected. If an order overflows to Write Inhibit, Status bit 43 is set and a Fault Interrupt is generated.

NOTE

Fault Interrupts are not generated for rejected commands.

# SECTION 12

# INTERRUPTS

There are two interrupts in the Drum System; for every Read/Write Command that is accepted a Fault or End Interrupt will be generated.

## 12.1 END INTERRUPT

The End Interrupt is a signal generated by the drum controller to tell the computer system (Auto Control Unit) that a Read or Write Command has been completed without error. The drum system gives an end interrupt only after the drum system accepts a command and that command is successfully completed.

## 12.2 FAULT INTERRUPT

The Fault Interrupt is a signal generated by the drum controller which tells the computer system (Auto Control Unit) that a Read or Write Command (which has been accepted by the drum system) has been aborted due to any of the following reasons:

a. Parity Error

b. Overflow to Write Inhibit - A Fault Interrupt is not generated when a Write Command is rejected due to Write Inhibit.

c. Memory Cycle Error

d. Timing Error - A Fault Interrupt is not generated when a Timing Error occurs and a drum command is not being performed. A Fault Interrupt is not generated when a TIO is rejected due to a Timing Error.

## SECTION 13

## FAULTS

The following are recognizable errors of the drum system along with the action taken by the drum system when the errors occur.

a. Parity Error - The High Density Drum Controller checks for odd parity during a Read or Write Instruction. When a parity error is detected, the drum order is terminated (not completed), the word in error is transmitted to the magnetic core memory in the case of a read instruction or to the drum in the case of a write instruction, and a Fault Interrupt is generated.

b. Write Inhibit - When a Write Instruction specifies a word address which is located in a Write Inhibited portion of a drum, the drum system issued a TIO reject. If after a write instruction has been accepted the drum word address overlaps into a Write Inhibited portion of the drum, then the order is terminated and a Fault Interrupt is generated.

c. Timing Error - There are two timing errors in the drum controller: one is a function of the block address counters associated with the selected drum. During the time the TIO is being processed, it is possible for a timing error to occur but not be detected until after the end interrupt has been generated. For this reason, the following action occurs when a TIO is received by the drum controller.

1. A check is made to determine if a word address counter error or a block address counter error has occurred since the last TIO as a function of the previously selected drum. If an error has not been detected, drum selection for the new TIO is performed. If a timing error is detected on the previously selected drum, the status register is not updated, and contains the logical number of the drum in error.

2. After the drum selection has been performed, a block address counter for the new drum is checked to determine if an error has occurred since the last TIO had accessed this drum. If a timing error is detected on the newly selected drum the status register will contain the logical number of the newly selected drum.

3. If a counter error is detected during the time a TIO is being processed, a fault interrupt will be generated. If a timing error is detected under conditions "1" or "2", a TIO reject is generated. Under the conditions of "1", "2", or "3", the timing error bit in the Status Register will be set to one and can only be cleared with a manual reset at the drum controller.

d. Mechanical Fault - A Mechanical Fault occurs as a result of an instruction specifying an unavailable device. A device appears unavailable when it is physically absent or when it is in the off (power not applied) state. When an instruction specifies a drum which is unavailable, the drum system issues a TIO reject.

e. Memory Cycle Error - A Memory Cycle Error occurs when the drum controller fails to obtain a memory access in the allotted period of time. Upon detecting a Memory Cycle Error, the High Density Drum Controller terminates the TIO order and generates a Fault Interrupt.

f. Channel Busy - In a multi-computer/multi-drum controller system, Channel Busy indicates that a computer which is busy processing data has attempted to access the controller in which channel busy status return was activated. An active channel busy status return indicates that the processor which received the return cannot be assigned to any drum system until the order which is processing data has been completed. Channel busy is meaningless in a single processor system.

g. Controller Busy - Controller Busy specifies that the controller is processing a Read/Write Command.

## SECTION 14

## OPERATING CONTROLS

The Operating Controls and Indicators for the Drum System are located on the end of the Drum Controller (refer to Figure 3). The control panel contains the following:

a. Status Register Display - The 48-bit register is displayed on the control panel. Refer to Section 6 for the bit assignment.

b. Memory Address Display - At the completion of a read/write TIO, the memory address of the next higher word is displayed if bit 0 of the Status Register is in the "1" state.

At the termination of a read/write TIO, the memory address for the word where the error occurred is displayed if bit 0 of the Status Register is in the "1" state.

> NOTE
>
> The resume bit (bit "0" of the status register) will be set to one by the drum controller at the completion or termination of drum instructions (both read and write) other than those making use of the relative addressing feature, except for the case in which a timing error has been detected. When the resume bit is zero (0), the Memory Address Display indicates the Memory Address which is one higher than the last word actually processed without error. It is not a useable address for resuming the order which made the error.

c. Parity Error Display - Parity error for each character of the word is displayed.

d. Device Assignment - The lighted pushbutton corresponding to the physical device places the device in the system when active. The plugs allow logical assignment of the device. (Example - If plugs number one (1) and zero (0) are interchanged, then physical device zero (0) will be logical device one (1) and physical device one (1) will be logical device zero (0).

e. Status - A timing error is defined as either a word address error or a block address error, or both. If either (or both) of these indicators is active, bit 44 of the Status Register will be active. If the memory cycle error indicator is active, bit 45 of the Status will be active.

f. Device Available - Each of these indicators will become active provided the following conditions are met for their respective device:

1. The drum has reached running speed.
2. The drum power supplies are on.

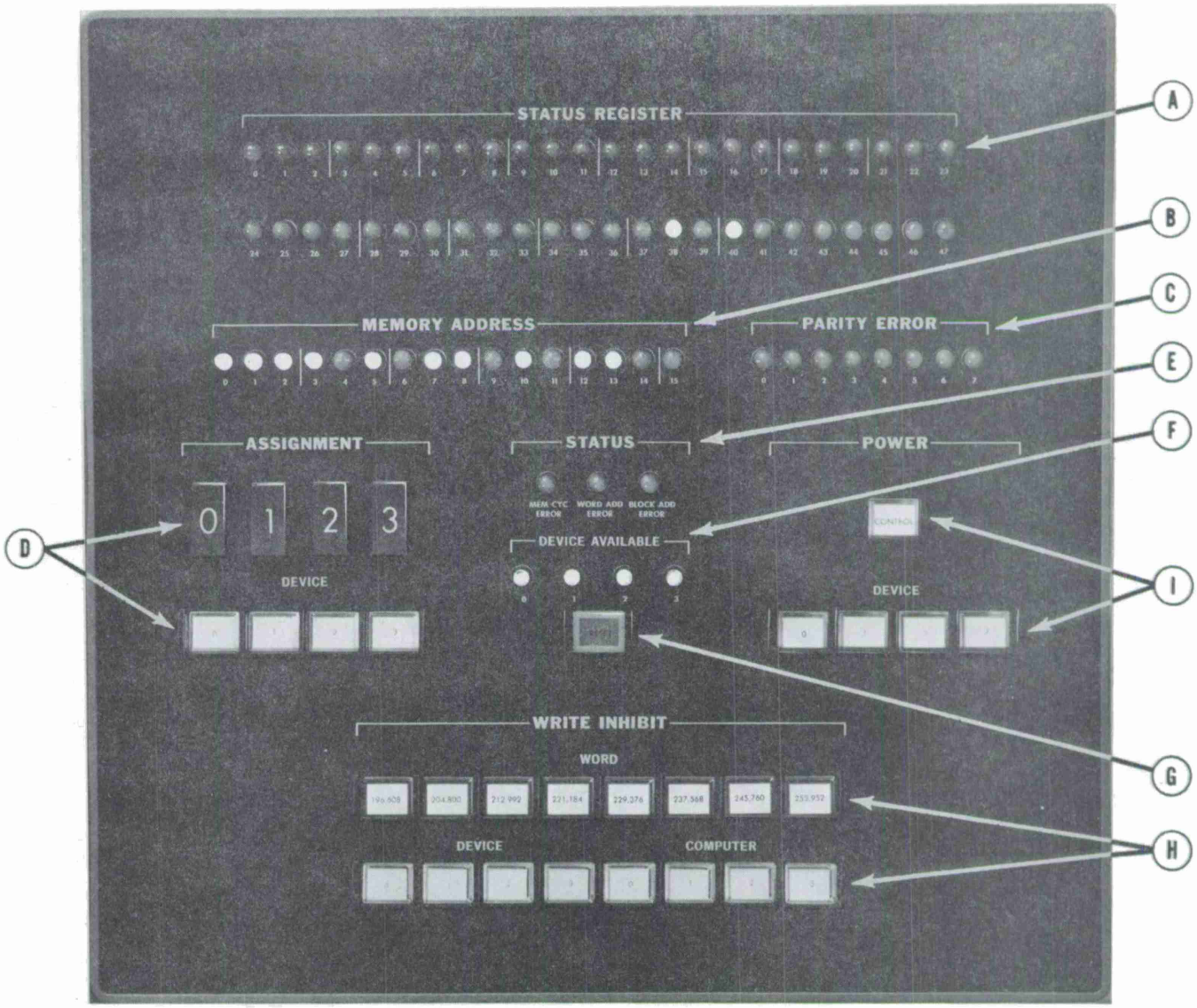



Figure 3. Control Panel Layout

g. Reset - The reset switch clears the control logic.

h. Write Inhibit - The device switches in this section select the device or devices to which the eight Write Inhibit Switches apply. The computer switches cause the controller to be Write-Inhibited for the specified computer (the computer switches are used only in a multiprocessor system).

A total of 65, 536 words per drum may be Write-Inhibited, in increments of 8, 192 words per Write-Inhibit Switch, starting with the last 8, 192 words on the drum. The Write-Inhibit switches must be activated from right to left. This ensures that, if a given group of 8, 192 words is inhibited, than all words from that group, up to and including the last word on the drum (word 262, 143) are inhibited. (See Figure 3.)

i. Power Section - Input AC for the drum power supplies and drum controller power supplies is applied through relays which are controlled by the five switches in the power section. These switches may be operated in any sequence.

j. Drum Motor Controls - Pressing the Start Switch turns drum motor power on and lights the Start indicator. When the drum has reached running speed, the Ready Indicator is lighted. Pressing the Stop Switch turns the drum motor power off and lights the Stop Indicator. (Refer to Figure 4 for layout of drum motor power controls.)

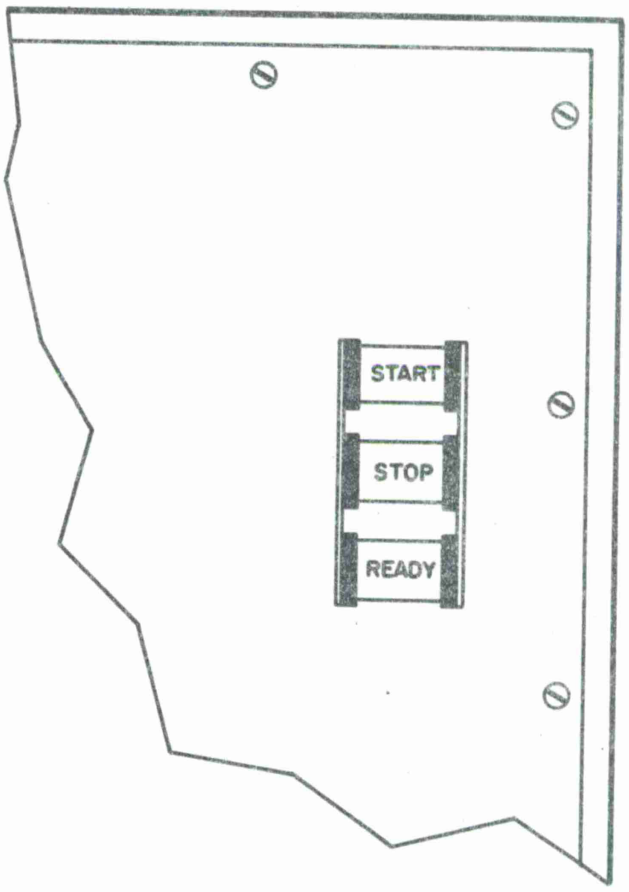



Figure 4. Drum Motor Control Panel

## SECTION 15

## POWER TURN-ON PROCEDURE

Instructions for turning on power to the High Density Drum System are as follows:

a. To turn on the Drum Motor, press the Start switch located on the Drum Control Panel. Refer to Figure 4. Pressing the Start Switch lights the Start indicator and applies power to the drum motor. When the drum has reached operating speed, the Ready Indicator is lighted. (A timer set for 12.5 minutes prevents the drum from being used until it reaches operating speed.)

b. To turn on the Drum Electronics, press the Device Power Switch located in the Power Section of the Drum Controller Control Panel. Refer to Figure 3. The Device Power Indicator will be lighted and the Drum Electronics will be sequenced on.

c. To turn on the Drum Controller, press the Control Switch located in the Power Section of the Drum Controller Control Panel. Refer to Figure 3. Pressing the Control Switch lights the Control Indicator and sequences the Drum Controller Power on.

## SECTION 16

## POWER FAILURE PROCEDURE

In case of power failure, a holding relay prevents power from being re-applied to the Drum Electronics. To sequence the power back on, first press the Device Power Switch to sequence power off; wait at least 30 seconds (allowing the sequence to cycle off), and then press the Device Power Switch again to sequence power back on.

If the Drum Motor Power fails, it will be necessary to restart the Drum Motor by pressing the Start Switch on the Drum Control Panel. It will then be necessary to wait for 12.5 minutes before the drum motor timer (see Section 15) will allow the Drum Ready Signal to activate.

## SECTION 17

## POWER TURN-OFF PROCEDURE

Instructions for turning power off the High Density Drum System are as follows:

a. To turn off the Drum Motor, press the Stop Switch located on the Drum Control Panel. Refer to Figure 4. Pressing the Stop Switch removes power from the Drum Motor, lights the Stop Indicator, and turns the Start and Ready Indicators off.

b. To turn off the Drum Electronics, press the Device Power Switch located in the Power Section of the Drum Controller Control Panel. Refer to Figure 3. Pressing the Device Power Switch turns the Device Power Indicator off and sequences the Drum Electronics off.

c. To turn off the Drum Controller, press the Control Switch located in the Power Section of the Drum Controller Control Panel. Refer to Figure 3. Pressing the Control Switch turns off the Control Indicator and sequences the Drum Controller Power off.

## SECTION 18

## DEVICE ASSIGNMENT

The switches in the Device Assignment Section of the Control Panel correspond to the physical devices. Pressing the Device Assignment Switch lights the Device Assignment Indicator and places the device into the system. Turning the Device Assignment Switch off removes the device from the system.

The device assignment plugs allow logical assignment of the device. Example - If plugs number one and zero are interchanged, then physical device zero will be logical device one and physical device one will be logical device zero.

Security Classification

**DOCUMENT CONTROL DATA - R&D**

*(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)*

| | |
|---|---|
| 1. ORIGINATING ACTIVITY *(Corporate author)*<br>Philco Corporation, A Subsidiary of Ford Motor Company<br>Communications and Electronics Division, Willow Grove, Pa. | 2a. REPORT SECURITY CLASSIFICATION<br>Unclassified<br>2b. GROUP<br>n/a |

3. REPORT TITLE

Programming and Operating for High Density Drum System

4. DESCRIPTIVE NOTES *(Type of report and inclusive dates)*

TDR

5. AUTHOR(S) *(Last name, first name, initial)*

Littrell, James H.

| 6. REPORT DATE | 7a. TOTAL NO. OF PAGES | 7b. NO. OF REFS |
|---|---|---|
| January 1965 | 27 | 0 |

| | |
|---|---|
| 8a. CONTRACT OR GRANT NO.<br>AF 19 (628)-3395<br>b. PROJECT NO.<br>c.<br>d. | 9a. ORIGINATOR'S REPORT NUMBER(S)<br>ESD-TDR-65-167<br>9b. OTHER REPORT NO(S) *(Any other numbers that may be assigned this report)*<br>None |

10. AVAILABILITY/LIMITATION NOTICES

Qualified requesters may obtain copies from DDC.
Copies available from OTS.

| 11. SUPPLEMENTARY NOTES | 12. SPONSORING MILITARY ACTIVITY |
|---|---|
| | 496L/474L System Program Office, Electronic Systems Division, Air Force Systems Command, USAF, L. G. Hanscom Field, Bedford, Mass., 01731 |

13. ABSTRACT

This report gives a programming description of the High Density Drum System. The purpose of this report is to ensure effective implementation of the High Density Drum System in the development of computer programs and to ensure efficient operation of the High Density Drum with the Philco 2000 Model 212 Computer. Included in this report is a description of operating controls and operating instructions.

DD FORM 1 JAN.64 1473

Security Classification

| 14. KEY WORDS | LINK A | | LINK B | | LINK C | |
|---|---|---|---|---|---|---|
| | ROLE | WT | ROLE | WT | ROLE | WT |
| Computers<br>Data Processing System<br>Data Storage System<br>Information Retrieval<br>Programming (Computers)<br>Handbook<br>Documentation<br>Instruction Manual | | | | | | |

## INSTRUCTIONS

1. ORIGINATING ACTIVITY: Enter the name and address of the contractor, subcontractor, grantee, Department of Defense activity or other organization *(corporate author)* issuing the report.

2*a*. REPORT SECURITY CLASSIFICATION: Enter the overall security classification of the report. Indicate whether "Restricted Data" is included. Marking is to be in accordance with appropriate security regulations.

2*b*. GROUP: Automatic downgrading is specified in DoD Directive 5200.10 and Armed Forces Industrial Manual. Enter the group number. Also, when applicable, show that optional markings have been used for Group 3 and Group 4 as authorized.

3. REPORT TITLE: Enter the complete report title in all capital letters. Titles in all cases should be unclassified. If a meaningful title cannot be selected without classification, show title classification in all capitals in parenthesis immediately following the title.

4. DESCRIPTIVE NOTES: If appropriate, enter the type of report, e.g., interim, progress, summary, annual, or final. Give the inclusive dates when a specific reporting period is covered.

5. AUTHOR(S): Enter the name(s) of author(s) as shown on or in the report. Enter last name, first name, middle initial. If military, show rank and branch of service. The name of the principal author is an absolute minimum requirement.

6. REPORT DATE: Enter the date of the report as day, month, year; or month, year. If more than one date appears on the report, use date of publication.

7*a*. TOTAL NUMBER OF PAGES: The total page count should follow normal pagination procedures, i.e., enter the number of pages containing information.

7*b*. NUMBER OF REFERENCES: Enter the total number of references cited in the report.

8*a*. CONTRACT OR GRANT NUMBER: If appropriate, enter the applicable number of the contract or grant under which the report was written.

8*b*, 8*c*, & 8*d*. PROJECT NUMBER: Enter the appropriate military department identification, such as project number, subproject number, system numbers, task number, etc.

9*a*. ORIGINATOR'S REPORT NUMBER(S): Enter the official report number by which the document will be identified and controlled by the originating activity. This number must be unique to this report.

9*b*. OTHER REPORT NUMBER(S): If the report has been assigned any other report numbers *(either by the originator or by the sponsor)*, also enter this number(s).

10. AVAILABILITY/LIMITATION NOTICES: Enter any limitations on further dissemination of the report, other than those imposed by security classification, using standard statements such as:

(1) "Qualified requesters may obtain copies of this report from DDC."

(2) "Foreign announcement and dissemination of this report by DDC is not authorized."

(3) "U. S. Government agencies may obtain copies of this report directly from DDC. Other qualified DDC users shall request through _____."

(4) "U. S. military agencies may obtain copies of this report directly from DDC. Other qualified users shall request through _____."

(5) "All distribution of this report is controlled. Qualified DDC users shall request through _____."

If the report has been furnished to the Office of Technical Services, Department of Commerce, for sale to the public, indicate this fact and enter the price, if known.

11. SUPPLEMENTARY NOTES: Use for additional explanatory notes.

12. SPONSORING MILITARY ACTIVITY: Enter the name of the departmental project office or laboratory sponsoring *(paying for)* the research and development. Include address.

13. ABSTRACT: Enter an abstract giving a brief and factual summary of the document indicative of the report, even though it may also appear elsewhere in the body of the technical report. If additional space is required, a continuation sheet shall be attached.

It is highly desirable that the abstract of classified reports be unclassified. Each paragraph of the abstract shall end with an indication of the military security classification of the information in the paragraph, represented as *(TS)*, *(S)*, *(C)*, or *(U)*.

There is no limitation on the length of the abstract. However, the suggested length is from 150 to 225 words.

14. KEY WORDS: Key words are technically meaningful terms or short phrases that characterize a report and may be used as index entries for cataloging the report. Key words must be selected so that no security classification is required. Identifiers, such as equipment model designation, trade name, military project code name, geographic location, may be used as key words but will be followed by an indication of technical context. The assignment of links, rules, and weights is optional