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FIRST

QUARTERLY PROGRESS REPORT

For

THE IMPROVEMENT OF PRODUCTION TECHNIQUES
TO INCREASE THE RELIABILITY OF
DIFFUSED SILICON CONTROLLED SWITCHES
Types 2N689

Period: 1 July 1963 through 30 September 1963

Contract Nr.: DA-36-039-AMC-03619(E)

U. S. ARMY ELECTRONICS MATERIAL AGENCY
Philadelphia, Pa.

RECTIFIER COMPONENTS DEPARTMENT

GENERAL ELECTRIC COMPANY
WEST GENESEE STREET
AUBURN, NEW YORK

(5) 351 960

(6) A PRODUCT ENGINEERING MEASURE
FOR THE IMPROVEMENT OF PRODUCTION TECHNIQUES TO
INCREASE THE RELIABILITY FOR DIFFUSED
SILICON CONTROLLED SWITCHES TYPES 2N689 ,

~~FIRST~~

~~QUARTERLY PROGRESS REPORT~~

For

~~Period 1 July 1963 — 30 September 1963~~

(9) Quarterly progress rept. no. 1 1 Jul - 30 Sep 63,

OBJECTIVE

To increase the reliability level of silicon controlled switches through work
which encompasses, but is not limited to, improvement in the main seal weld,
tubulation crimp and weld, surface stabilization, cathode junction formation and
control of silicon growth and diffusion processes.

(15) CONTRACT NR: DA-36-039-AMC-03619 (E)
ORDER NR: 21061-PP-63-81-81

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ABSTRACT

The first quarterly progress report of a ~~Production~~ Engineering Measure (PEM) for the improvement of production techniques to increase the reliability of a diffused silicon controlled switch, of the 2N689 type, ~~under the USAEMA Contract No. DA-36-039-AMC-03619 (E) of 22 June 1963~~, covers the work performed on an all-diffused rectifier subassembly, the device package, reliability testing equipment, and the materials complying with pre-established parameters. A PERT analysis depicts the progress of this program and provides certain conclusions on the work performed.

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SECTION II

PURPOSE

The purpose of this program is to improve the processes to fabricate
an all-diffused, medium-current, silicon controlled switch with superior
electrical characteristics to the present alloy-diffused device. The
applicable items of work for this quarterly progress report are: (1)
theoretical design of diffused emitter structure and diffusion process
established; (2) diffused wafers available for contact work and early
sample preparation; (3) tools and equipment designed; (4) surface con-
tour selected; (5) contouring equipment designed; (6) optimum di-electric
coating determined; (7) atmosphere control equipment designed; and, (8)
first Engineering Samples delivered.

SECTION III

NARRATIVE AND DATA

CHAPTER 1 -- ALL DIFFUSED DEVICE PROGRAM

THEORETICAL DESIGN OF AN ALL-DIFFUSED EMITTER STRUCTURE

Three basic factors influence the design of an all-diffused Silicon Controlled Rectifier (hereinafter, SCR) of the 2N689 type. First, superior electrical parameters are desired; specifically, in the area of surge and dv/dt capability and in a faster switching (short turn-off time) device with increased capability to handle surge currents during the turn-on period of the SCR (di/dt). Second, increased stability is desired and believed possible with the elimination of a stress-sensitive alloyed junction. Third, for military and heavy industrial applications, a device exhibiting thermal fatigue-free characteristics is deemed desirable.

Surge

A calculation of the cathode emitter area was made based upon the current density measurements of the existing all-diffused structures on other product lines, in order to accomplish the desired surge capability. A surge-current density value of 10,000 amperes per square inch of emitter area was used to establish geometric limits, for the cathode junction.

Dv/dt - Rate of Rise of Reapplied Forward Voltage

The dv/dt capability of an SCR is controlled by the following factors:

1. The "effective" emitter efficiency of the emitter junctions at low current density levels.

2. The "effective" base widths and lifetimes of minority carriers within the device.

3. The capacitance of the center junction.

4. The uniformity of the junctions.

The dv/dt effect in an SCR can be observed by applying a rapidly rising voltage across the structure in the forward blocking direction.[1] If the voltage pulse is of sufficient magnitude and has a sufficiently steep wave front (dv/dt), then the device will switch to the conducting state. This phenomenon is most troublesome when SCR circuits are first energized.

When a positive voltage is applied between anode and cathode of the device the extreme end junctions become forward biased, whereas the center junction is reverse biased. This junction acts as a non-linear capacitor. To charge this capacitance, current must flow through the forward biased junctions. Current flow through these two end junctions result in minority carrier injection into the base regions of the device. Since the alphas of an SCR are dependent upon current density (i.e., as current density increases, alphas increase), the device will not trigger as long as the current density remains low. When the current density rises, however, the SCR will trigger into the conducting state when the sum of the alphas approached unity, according to the equation

$$ I = \frac{I_s}{1 - (\alpha_1 + \alpha_2)} , \tag{1} $$

where $\alpha = \gamma \beta$, in which γ represents the emitter efficiency of a junction and β represents the transport factor. The two-transistor analogy of an SCR is described in the foregoing, and in Figure 1. To prevent the rise of emitter efficiencies and, as a result, an increase in alphas with increasing current, the use of a "shorted emitter" is employed as shown in Figure 2. At low-current densities the current required to charge the blocking junction (J_2) will now bypass junction J_3 so that the effective emitter efficiency is essentially zero. At high current levels, the lateral voltage drop in the "P" base will be high enough so that some current will now prefer to pass through J_3, thus increasing the NPN alpha, and accomplish the necessary feedback for turn-on of the device. By controlling the spacing and amount of emitter shorting, the lateral voltage drop in the "P" base can be adjusted for various current levels, thus controlling the ultimate dv/dt of the device.

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This device has been designed to yield 200 volt/μ second dv/dt values.

Turn-Off Time

Turn-off time is primarily a function of the minority carrier lifetime in the device. All minority carrier devices need a period of elapsed time after the forward voltage is removed or reversed before forward voltage can be reapplied without triggering the SCR.[2] Immediately after forward conduction, both base regions are saturated with excess carriers, and the numbers of excess holes and electrons are essentially equal for each base region.

When the voltage is reversed those minority carriers near the end junctions are swept out of the bases and the end junctions become reverse biased (Figure 3). As holes are swept out of N_1, they leave behind excess electrons which increase the potential difference between N_1 and P_2, resulting in J_2 being forward biased so that holes are injected from P_2 into N_1. Therefore, holes are injected into base N_1 from one side and leave N_1 from the opposite side. In diffusing across the base, holes and electrons recombine at a rate proportional to the minority carrier lifetime. Since the current flow is proportional to excess charge in the base, the current decay with time is dependent upon lifetime according to the relation

$$I = K_1 + K_2 \exp (-t/\tau), \qquad (2)$$

where K_1 and K_2 are constants and τ is the minority carrier lifetime.

To decrease the decay time, the carrier lifetime must be reduced. This is accomplished by means of diffusing gold into the base regions of the device. In order to keep the forward conducting voltage drop of the gold-doped device within practical limits, the N_1 base width was reduced which limited the maximum blocking voltage attainable, but is sufficient to produce a 500 volt class device.

Turn-On Surge Capability (di/dt)

The turn-on mechanism of an SCR has been studied[3], and it has been found that the most practical method of improving the switching current capability of an SCR in high frequency applications is by means of distributing the switching current over more of the emitter periphery. The present 2N689-type SCR incorporates an off-center gate design (Figure 4a) which is not capable of handling enough current during turn-on so that these devices are practical for use in inverter circuits. To increase the current carrying emitter area during turn-on, a center gate configuration (Figure 4b) was chosen for the all-diffused structure. Decrease of minority carrier lifetime does adversely affect di/dt capability, and these two parameters will be balanced in the final design. Initial design configuration is shown in Figure 5.

DIFFUSED WAFERS AVAILABLE

Several lots of diffused silicon have been made for contact work and early sample preparation. The contact work began with the following prerequisites:

1. The solder construction must be thermal fatigue-free, and the unit must be as stress-free as possible which necessitates the use of backup plates.

2. The contact material shall not penetrate the silicon to such an extent that alteration of the impurity level distribution occurs.

3. The contact material will be used as a connecting shunt from the "P" surface to the diffused "N" emitter for the "shorted emitter" structure.

Early contact work was done on a variety of materials of which three show the most promise: (1) Aluminum plating to both anode and cathode silicon pellet surfaces; (2) Pure gold vapor deposited to the silicon pellet surfaces; and, (3) Nickel plating of the silicon surface by an electroless method.

Results of Contact Work

Evaluation of aluminum plating to silicon showed a partial conversion of the cathode emitter diffused region when the diffused emitter junction depth was shallow (Figure 6a, 6b) or the "N" dopant concentration was below 10^{21} atoms/cm^3. Since aluminum is a P-type dopant in silicon, its N-type penetration into silicon was deep enough to create a high resistance layer resulting in increased forward voltage drops of the device. Pure gold plating by the vapor deposition method gave an excellent bond to the silicon surface by means of the gold-silicon eutectic formation during the plating operation. The major disadvantage to this plating technique was the digestion of the phosphorus impurity on the surface of the diffused cathode emitter by the liquid gold-silicon eutectic and the transfer or mixing of this dopant with adjacent P-type gold-silicon eutectic mixtures in a manner that negated the shunt or "shorted emitter" during recrystal- lization. See Figure 7. There are plating conditions which will not result in the "mixing" of the dopant, but these conditions must be controlled with such precision that manufacturability on a large scale seemed doubtful.

The electroless (chemical) plating[4] of nickel on silicon yielded a good solderable surface, but not without disadvantages. Adherence of the plating to silicon was found to be sporadic and extremely dependent upon pellet cleanliness and surface preparation treatments. The solder chosen to bond to the nickel plating and to the backup plates was an alloy of gold and germanium of eutectic composition. This fatigue-free ("hard") solder was chosen over other hard solders because of its low melting point (356°C), and its very good wettability to a nickel-plated surface. The low melting point had the advantage of easier fabrication, and in minimiz- ing the "poisoning" effects or diffusing of impurities into silicon from fixture materials which has been observed when soldering or alloying is performed at temperatures of 700°C or more.[5] Early samples of this contact process (Figure 8) were made and evaluated. There were two basic faults to the process. First, the nickel plating of P-type silicon was not reproducible from lot-to-lot of silicon, and some areas of unplated silicon were evident. Adhesion of the plating to the silicon was variable with some backup discs separating from the silicon under moderate stress.

Sintering of the nickel plate to the silicon at 650°C was done to improve adhesion. Adhesion results were good, but the sintering operation reduced the ability of the solder to wet the nickel plate. Replating of the sintered, nickel-plated silicon was attempted with another layer of electroless nickel plating. This procedure was not satisfactory since the bonding of the two nickel plating layers was mechanically weak. Again, the disc attachment to the silicon could be broken with the cleavage plane being the interface of the two nickel layers. The nickel plating sintering step had one further disadvantage, in that elemental phosphorus which is present in the plating interacted with the silicon P-type surface causing conversion of the P-type surface to N-type, thus making a shorted emitter structure impossible. The second basic fault of this process is its inability to control the degree of run-out, or flow, of gold-germanium solder across the plated surface. Since the design of this structure called for a peripheral shorted emitter (Figure 9a), it was necessary to insure solder flow beyond the cathode emitter periphery. Slight variations in solder temperature resulted in significant differences in flow out, and thus, in the degree of shorting.

Maintaining the advantages of nickel plating and the elimination of at least one disadvantage, vapor-deposited nickel on silicon was attempted with repeated success. Vapor-deposited nickel contained no phosphorus, and thus had no tendency to dope the silicon surface when bonded to the silicon. Bonding was accomplished during the plating operation by utilizing the radiant heat from the filament, to raise the temperature of the silicon as plating proceeded.

Variations in solder flow still existed with vapor-plated nickel parts, coupled with a relatively high percentage of units exhibiting complete digestion of the nickel plating by the gold-germanium eutectic solder, and subsequent alloying or penetration of the solder into the body of the silicon pellet.

Attempts to increase the nickel plate thickness failed, due to the bi-metallic action of the nickel-silicon. Heavy coatings of nickel exhibited

a shear or a "peeling" effect in the plated nickel layer, with the bulk of the nickel plate curling away from the pellet upon cooling, leaving behind a thin layer of nickel plate still attached or bonded to the silicon surface.

A buffer layer of plating was deemed necessary to prevent the digestion of nickel by the gold-germanium. Several combinations were tried and the greatest success was obtained with a multi-layer of vapor deposited metals. This plating controls more closely the flow of gold-germanium solder and, at the same time, is resistant to attack by acids used to etch the silicon subassembly junctions during processing. This plating is presently under test and further results should be available by the next report period.

TOOLS AND EQUIPMENT

Tools and equipment have been designed, or are available, for the fabrication of devices. Those presently operable include: a vacuum coater for deposition of the tri-layer plating on the silicon pellet; a tunnel oven for soldering back-up plates to the silicon; silicon wafer beveling equipment; an ultrasonic bonder for gate lead attachment; a tunnel oven for soldering subassemblies to the studs; and associated resistance welders for hermetic sealing of the package.

The fixture necessary for soldering parts into subassemblies has been designed (refer to Figure 10a), and the prototypes have proved feasible. Several different mount-down fixture designs (i.e., subassembly to stud operation) have been tried, and one design has been approved (see Figure 10b). Small fixtures necessary for processing, such as etch fixtures, are available from similar size product lines and are being used with satisfactory results.

Masks for pelletizing the diffused wafer have been received and are presently being used. The mask for etching the cathode pattern on the silicon wafer is now undergoing design changes to facilitate subsequent processing and registration. Final design should be completed during the next report period.

SURFACE CONTOUR

To minimize surface field effects, a surface contour was deemed necessary on this device. Because of gross imperfections and the inability to remove all exterior disturbances from the junction surfaces, surface breakdown will occur with destructive effects in a device which has not been surface contoured. By use of a properly contoured junction surface, it is possible to

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lower the field in the junction region by lengthening the distance over which the voltage is spread. The field then will be lower than it is in the body of the device. This results in a more stable device with surface effects greatly reduced. The particular surface contour designed is shown in Figure 9b.

CONTOURING EQUIPMENT SELECTION

Initial contour work was performed by using a rotating, diamond-impregnated tool to grind the silicon pellet to the proper shape. Subsequent etching of the silicon removed the damaged surface to achieve good voltages from the device. Early processing showed several areas of processing problems. First, the silicon pellet surface must be concentrically aligned with the contouring tool to achieve an evenly cut bevel. Non-parallel or non-concentric alignment results in an "egg-shaped" or oval cut which yields a surface sensitive device due to the change of contour. A fixture to assure this alignment has been designed and is being fabricated. Second, the grinding of silicon in an area over which gold-germanium solder has been deposited results in a "tearing out" of the silicon or localized pellet fracture. This effect has been greatly reduced by the flow-out control of the solder as mentioned previously. Total elimination of this problem is being contemplated by means of an alternate beveling procedure. Feasibility of beveling by errosion of the silicon with sandblasting has been demonstrated on small samples, and more work is planned in investigation of this technique during the next report period.

DIELECTRIC COATING

In order to protect the exposed, cleaned junctions from ambient contamination, a dielectric coating on the silicon surface is required. A theoretical ideal coating would be one which has an atomic spacing in its molecular structure which matches that of the silicon lattice, and one which will chemically bond to silicon and thus render the surface inert to the influence of contaminants.

Silicon oxide approaches this theoretical goal, but the application has yet to be proven feasible for high-voltage devices. All attempts to coat silicon with its oxide by electrolytic deposition have yielded permeable coatings susceptible to the influence of moisture. High-temperature oxidation for junction passivation yielded "poisoned" high-voltage characteristics which

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rendered the devices unsuitable because of the resultant "soft" or high
leakage current characteristics. Silicone products, such as varnishes
and rubber compounds, have proven satisfactory as dielectric materials
on silicon junctions. Varnishes of various compositions have been tried
and found to have very good adherence to silicon but require complex
application and care conditions which need close control and monitoring.
This problem has been overcome by the use of silicon rubber compounds,
which are easily applied to the device in liquid form and then easily
cured into a solid, elastic coating.

Stability of this dielectric is extremely good when the proper cure cycle
is employed and when the necessary catalyst for cure has been removed from
the finished product. Preliminary results show this method to be the most
feasible and promising path to follow.

CURING OF SILICONE RUBBER

Curing of silicone rubber compounds require heat and moisture for specified
times. An oven to accommodate this cycle has been obtained and is in
operation.

Inert atmosphere boxes for final seal operation are to be standard dry
boxes of an existing design. The use of these boxes is compatible with the
dielectric coating chosen, and they are now in existing facilities.

TABLE OF DATA

A table of data of the first electrical samples is included in this report.
This data is representative of the capabilities and distribution of the
present alloy-diffused 2N689 device presently in production. Major product
improvement areas expected on the all-diffused structure have been already
discussed.

DATA SHEET

2N689

Lot No. _____   Date _____

Serial No.	T_J = -25°C ± 3°						T_J = 125°C ± 3°						T_J = 25°C ± 3°				T_J = 125°C ± 3°	

Serial No.	V(BR)RO or V_RO (volts) [-25°C]	I(BR)RO or i_RO (mA)	V(BR)FO or V_FO (volts)	I(BR)FO or i_FO (mA)	I_GT (mA)	V_GT (volts)	V(BR)RO or V_RO (volts) [125°C]	i(BR)RO or i_RO (mA)	V(BR)FO or V_FO (volts)	i(BR)FO or i_FO (mA)	I_GT (mA)	V_GT (volts)	V_F (a) (volts)	V_F (b) (volts)	t_q on (µ sec)	I_H (mA)	t_{off}/v_{app} (µsec)	t_{off}/v_{app} (volts)	$d(v_{FO})/dt$/v_{app} (µ sec)	$d(v_{FO})/dt$/v_{app} (volts)
1	500	.1	500	.1	16.0	1.20	500	.30	500	.25	4	.70	.80	1.42	1.30	7.5	29	500	4.0	500
2	500	.1	500	.1	26.0	1.10	500	.50	500	.50	7	.70	.75	1.25	1.25	8.0	100	500	9.0	500
3	500	.1	500	.1	27.0	1.60	500	.35	500	.20	10	.85	.60	1.41	1.12	10.5	19	500	2.0	500
4	500	.1	500	.1	29.0	1.60	500	.65	500	.50	9	1.10	.80	1.39	1.54	11.5	28	500	.6	500
5	505	.1	500	.1	16.0	1.10	500	.70	500	.10	4	.80	.80	1.49	1.10	6.0	28	500	9.0	500
6	500	.1	500	.1	11.0	1.00	500	.25	500	.20	4	.70	.90	1.55	.96	17.0	11	500	2.5	500
7	500	.1	500	.1	8.5	.85	500	.35	500	.25	3	.70	.87	1.60	.96	11.0	12	500	.6	500
8	500	.1	500	.1	32.0	1.30	500	.30	500	.15	10	1.00	.85	1.72	1.30	16.0	20	500	.6	500
9	500	.1	500	.1	13.0	.80	500	.40	500	.10	4	.55	.90	1.58	1.30	21.0	18	500	1.2	500
10	500	.1	500	.1	21.0	1.15	500	.20	500	.15	5	.90	.85	1.49	1.18	19.0	25	500	.6	500
11	500	.1	500	.1	7.0	.85	500	.50	500	.30	3	.70	.80	1.52	.88	10.5	22	500	5.0	500
12	500	.1	500	.1	8.0	.85	500	.20	500	.15	2	.55	.83	1.48	.96	11.5	19	500	2.5	500

NOTES: (a) I_F = 0.5 amperes
(b) i_F = 50 amperes

Table 1 - Data of first electrical samples

12
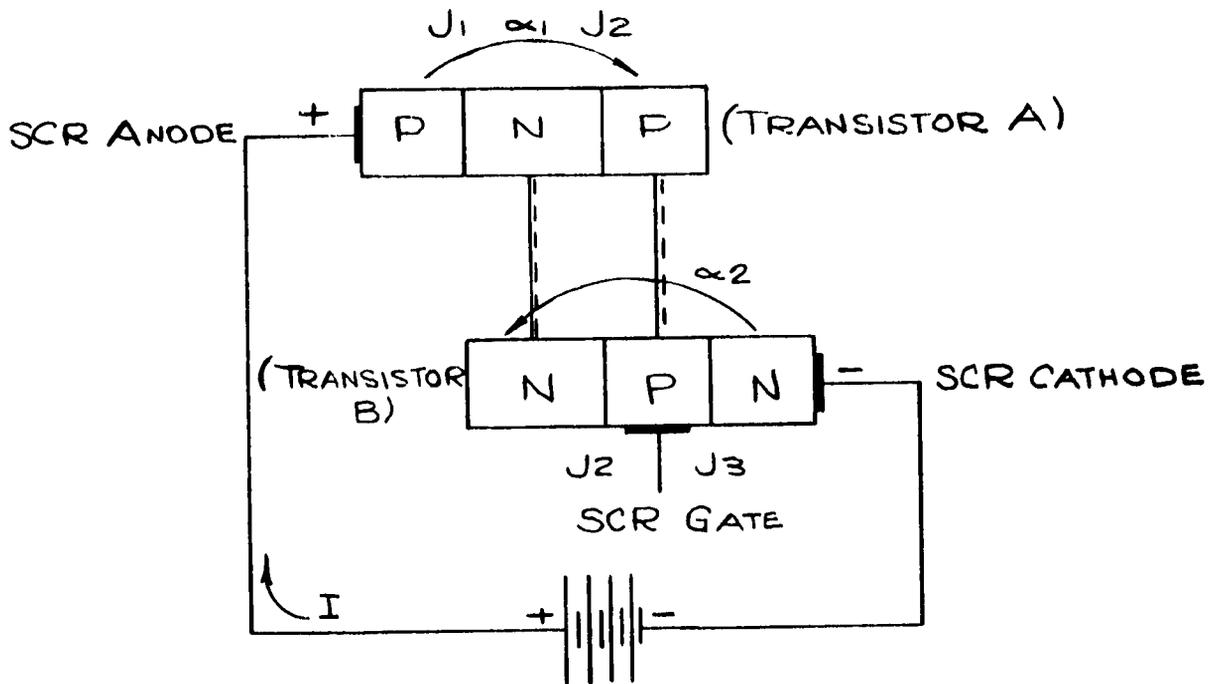
$I_{\text{holes across } J_2} = \alpha_1 I$ (Transistor A)

$I_{\text{electrons across } J_2} = \alpha_2 I$ (Transistor B)

$I_{\text{total across } J_2} = \alpha_1 I + \alpha_2 I + I_{CO}$ (Leakage Current)
For the SCR.

Since $I_{J_2} = I$, $\quad I = \dfrac{I_{CO}}{1 - (\alpha_1 + \alpha_2)}$

Figure 1 - Two transistor analogy for an SCR

13
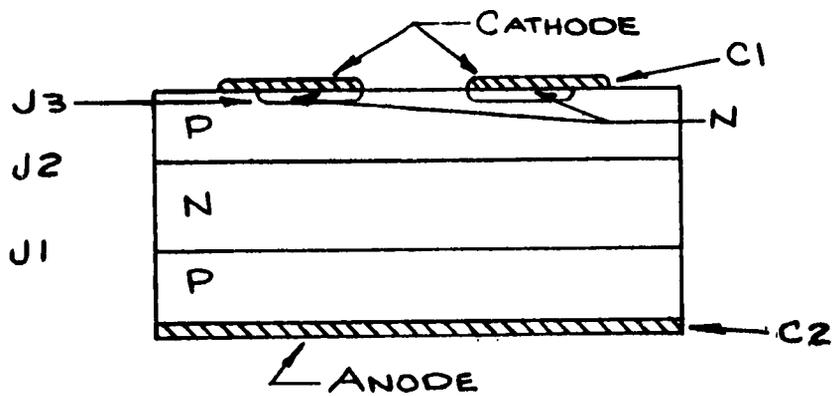
Figure 2 - Shorted emitter configuration
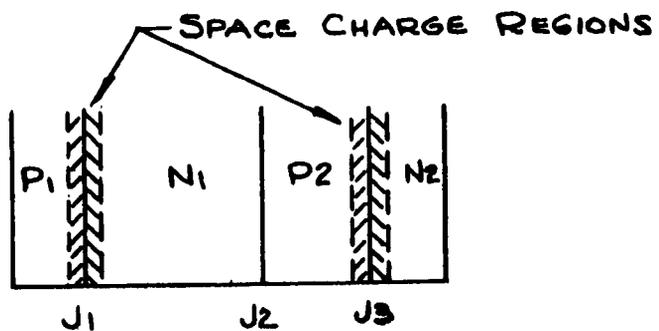
Figure 3 - Reverse biased SCR

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TOP VIEW

P-N-P SILICON PELLET

"N" EMITTER

GATE

TURN-ON AREA

SIDE VIEW

N

GATE

| P |
| N |
| P |
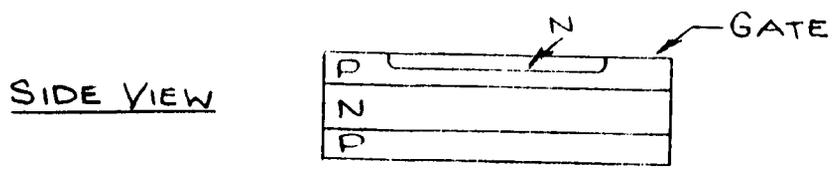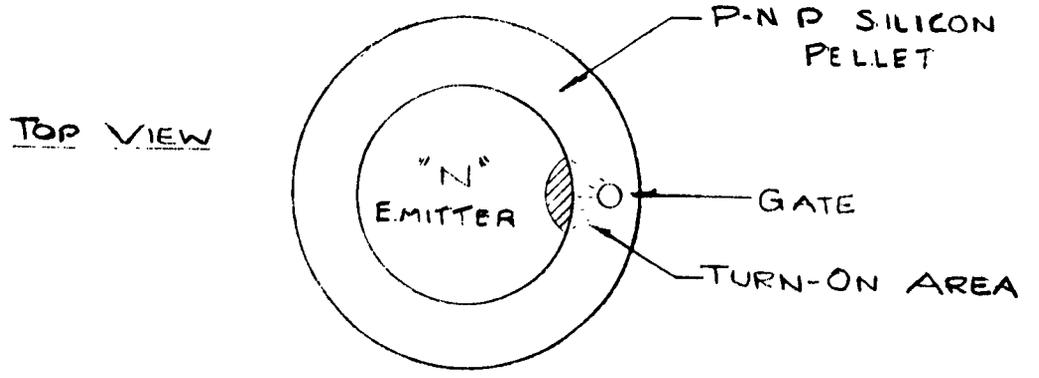
Figure 4a - Offset gate design

"N" EMITTER

TOP VIEW

P-N-P SILICON PELLET

TURN-ON AREA

GATE AREA

SIDE VIEW

GATE AREA

| P | N | N |
| N |
| P |
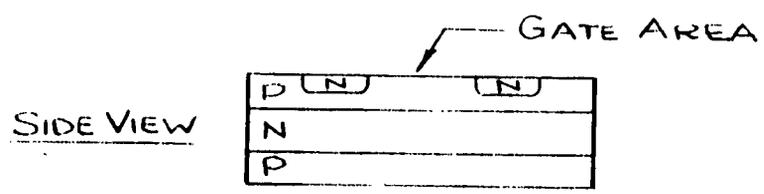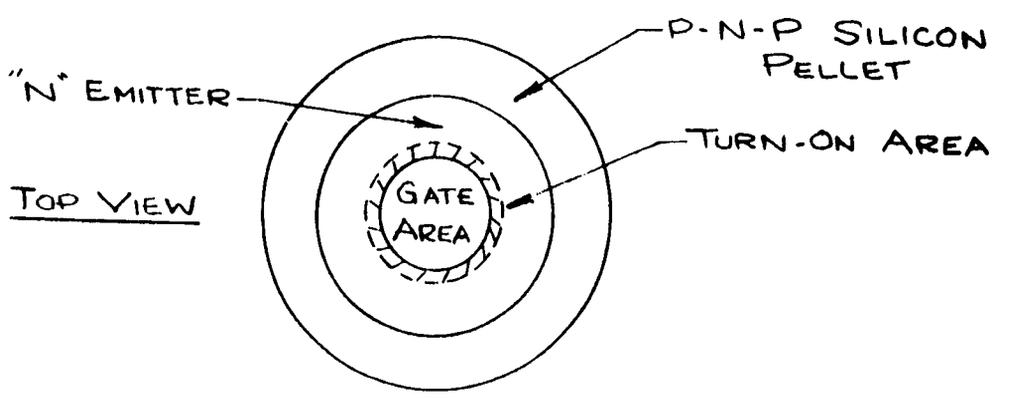
Figure 4b - Center gate design

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TOP VIEW
PELLET

TOP TUNGSTEN

BASE TUNGSTEN
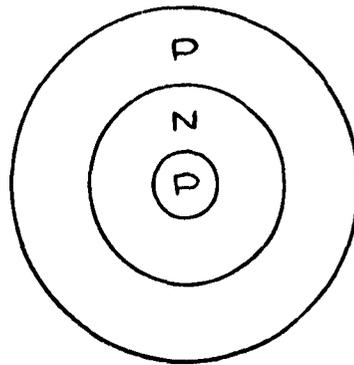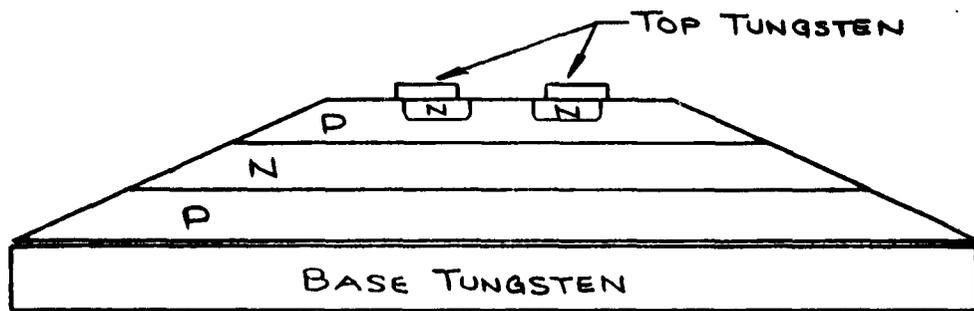
SIDE VIEW
SUB ASSEMBLY

Figure 5 - Device subassembly

16
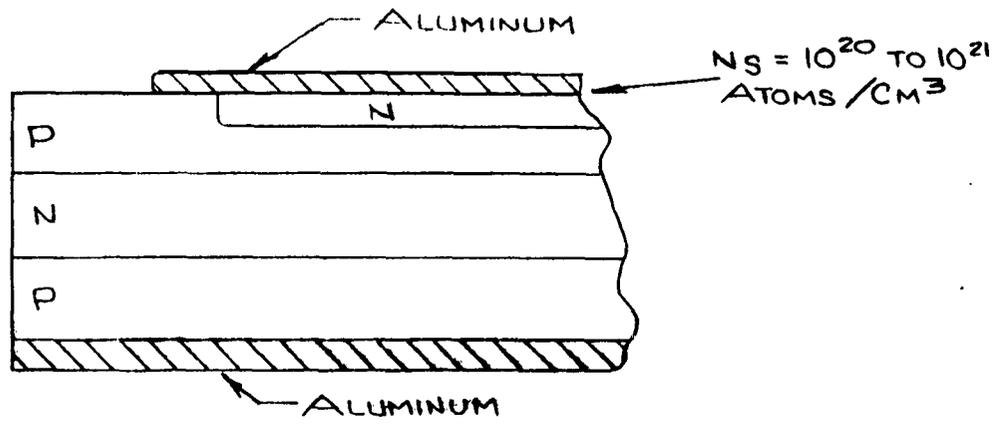
Figure 6a - Plating before contact plate attachment
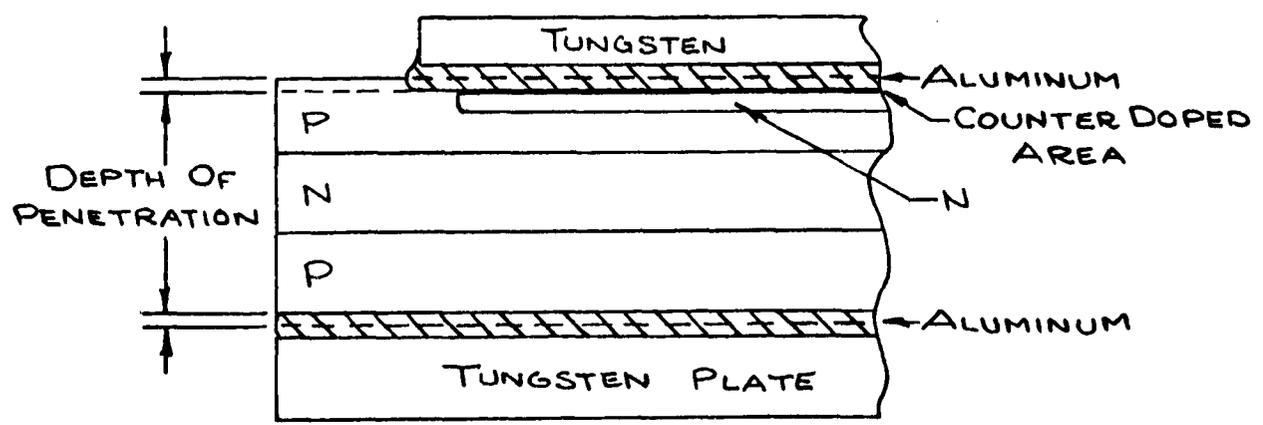
Figure 6b - Contact penetration after tungsten plate attachment

17
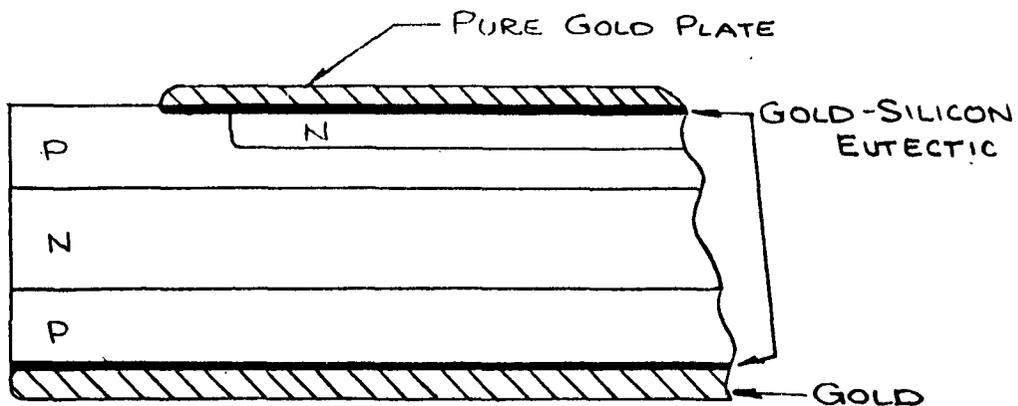
Figure 7a - Digestion and redeposition of phosphorous
by molten gold-silicon eutectic alloy
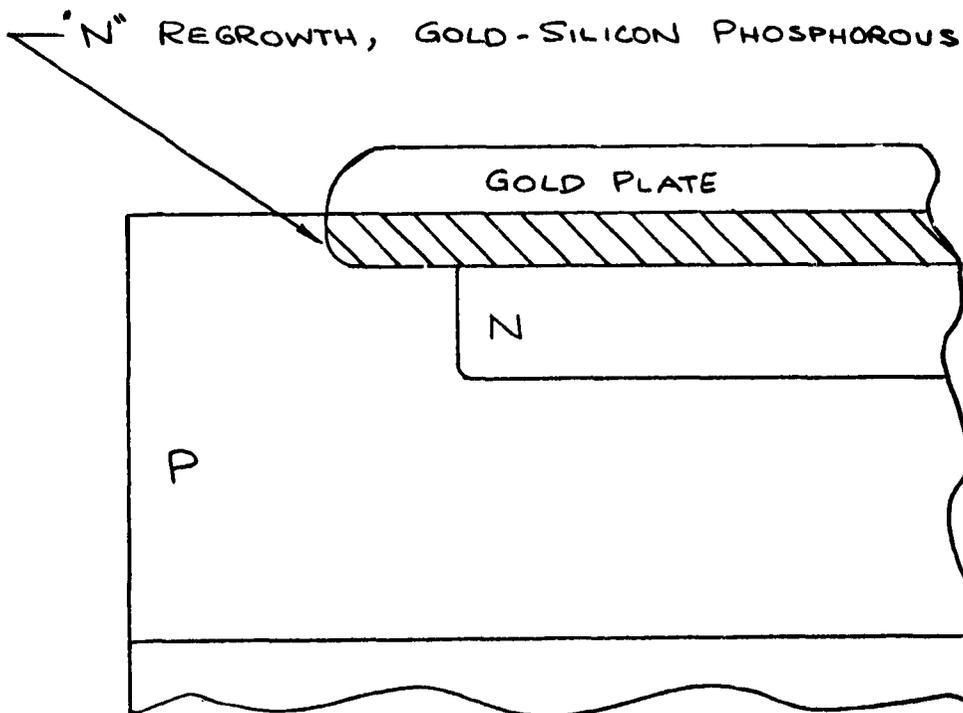
Figure 7b - Enlarged view gold-silicon eutectic alloy
showing N regrowth

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TOP TUNGSTEN

GOLD-GERMANIUM

NICKEL PLATING

SILICON

GOLD GERMANIUM

BASE TUNGSTEN
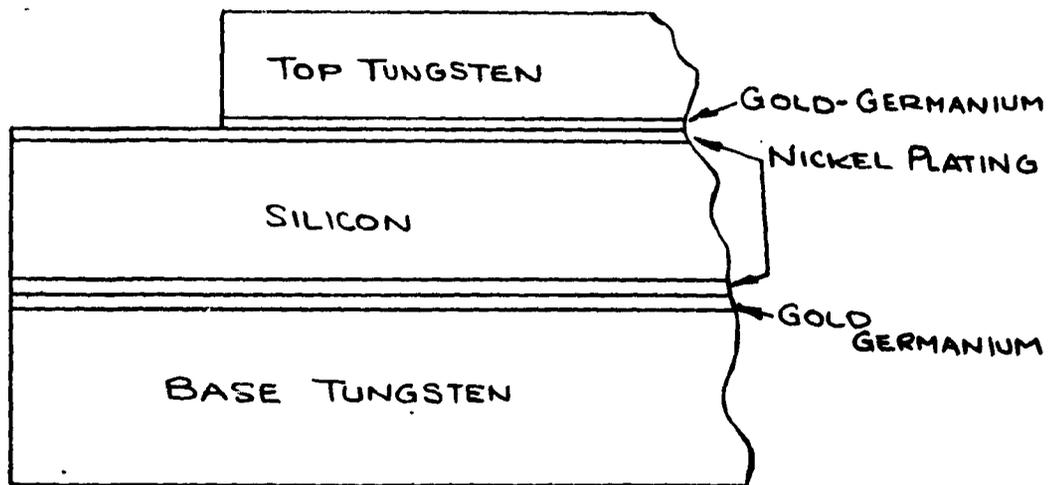
Figure 8 - Early contact process

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PERIPHERAL SHORTED EMITTER

GATE AREA

P

N

P

BASE TUNGSTEN
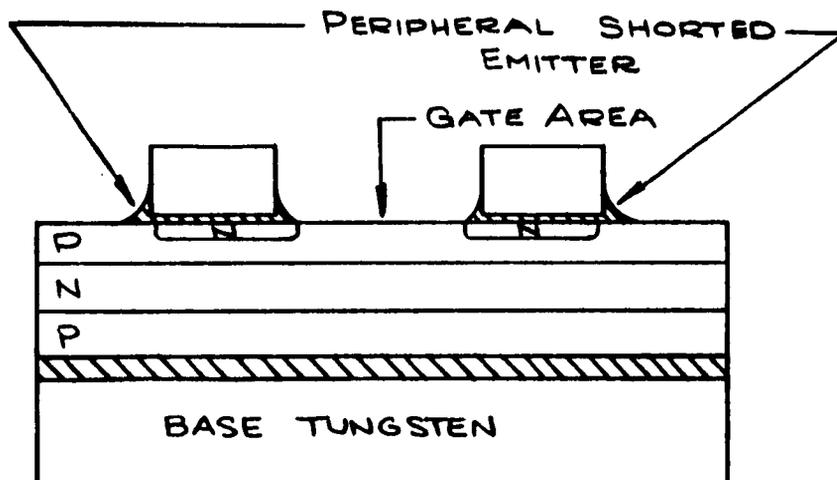
▨▨▨▨ GOLD-GERMANIUM SOLDER

Figure 9a - Cross section of ZJ255 subassembly

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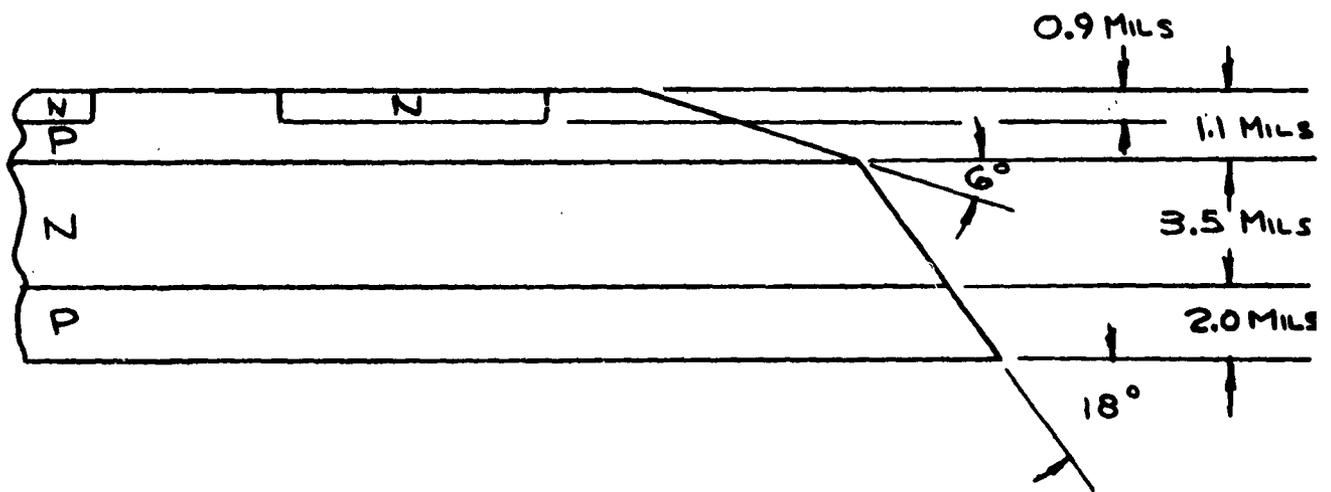
Figure 9b - Contour design for 2J255

21
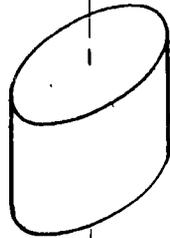
WEIGHT

WEIGHT HOLDER
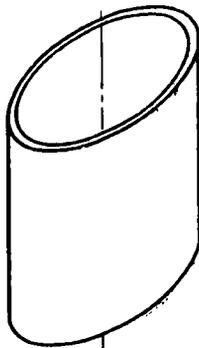
HOLDER
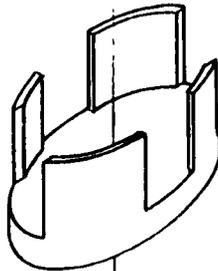
Figure 10a - Subassembly fixture

STUD-HOLDER
STAINLESS STEEL

F.H.S.
STAINLESS STL.

WEIGHT-
STEEL

LEAD-
HOLDER-
GRAPHITE

LOCATING
RING-
GRAPHITE

LOCATION
FOR STUD
F. SUB-ASM.
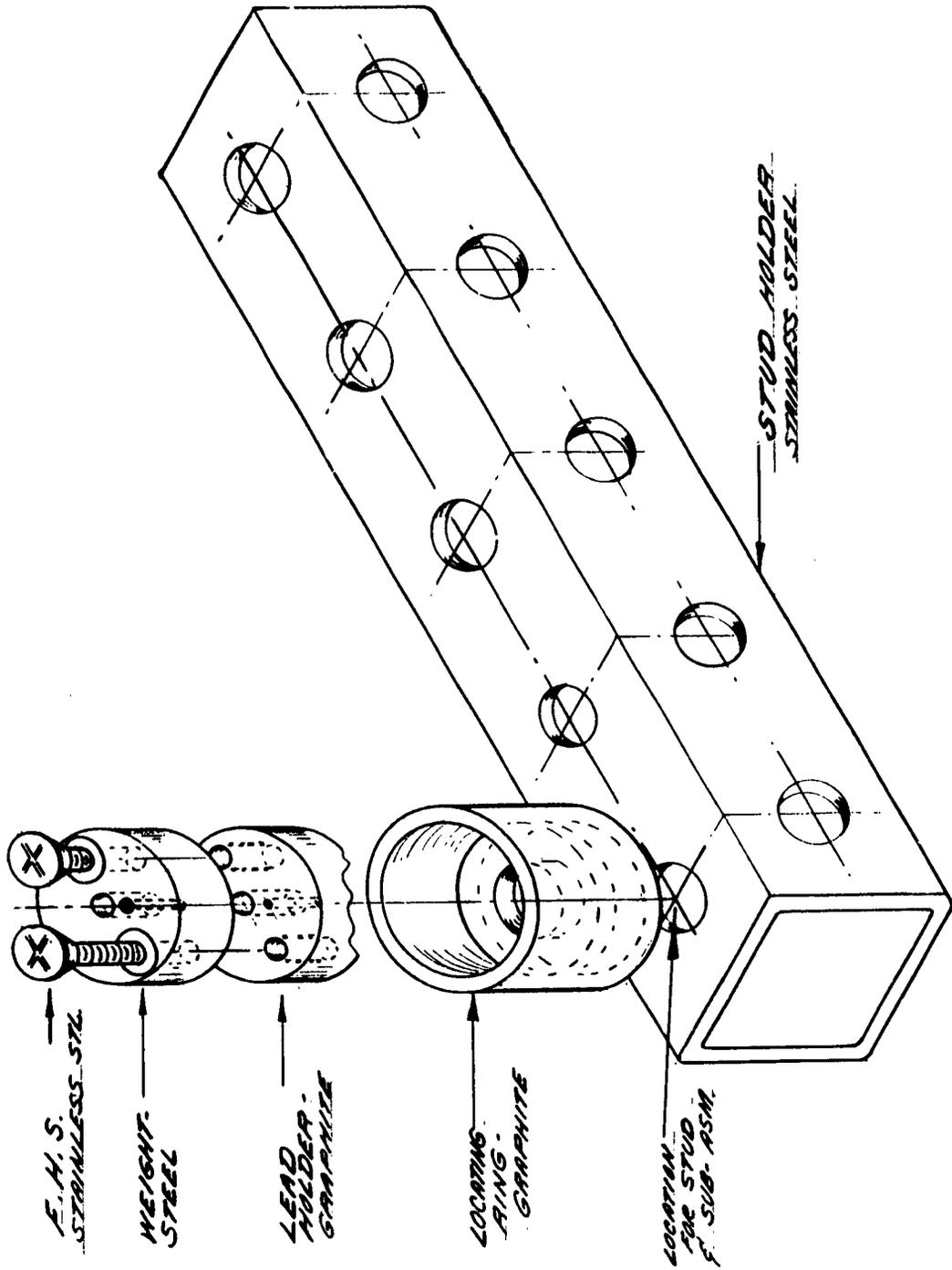
Figure 10b - Mount-down fixture

CHAPTER 2 - DEVICE STUD AND HOUSING PROGRAM

Introduction

The applicable items of work on the mechanical packaging of the 2N689 type, Silicon Controlled Switch, and as covered in this report are: (1) The selection of materials for stud and housing; (2) The design of a new stud and housing within the JEDEC TO-48 package outline; and, (3) The investigation of ultrasonic torsional welding of the housing to the stud forming the package "main seal".

The new design must meet, or exceed, the requirements of MIL-S-19500/108A. In addition, it will be necessary to eliminate all sources of metallic, or gaseous, contamination of the electrical junction; such as, resistance welds, arc welds, brazed joints, or soldered joints.

Material Selection

All materials used in the present mechanical package were examined from a cost, function, and strength standpoint. Because of its excellent electrical and thermal conductivity, OFHC copper is being retained as the stud material. Copper was also selected for the housing flange and eyelet material; however, due to the softness of copper, damage to the flanges before welding was common. Copper also had a tendency to adhere to the welding tip of the ultrasonic welder. For these reasons, the copper flange was discarded, and in its place a copper-clad steel (30% copper, 70% steel) has been chosen. Steel gives the required strength, while the copper permits a copper-to-copper ultrasonic weld. This copper-to-copper combination, as shown in earlier testing, is most reliable and requires the least weld energy. Since Kovar metal is not needed for a matched seal, a less expensive nickel-iron alloy has been selected for the gate and cathode tubes, in the initial design. This new material permits the use of the existing gate and cathode terminals. In order to reduce the stress on the insulating material, the portion of the heavy-walled cathode tube going through the insulator was changed to copper.

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This copper will anneal and stress-relieve itself before it can damage the insulator. An alternate design will change both of the tubes to copper, and will combine the tube and terminal into a one-piece construction. This alternate has the advantage of: (1) lowering the forward drop in the device; (2) providing a material which is easier to tin and solder; and, (3) providing more reliable terminals.

The materials considered for the housing insulator were high strength glass, ceramic and glass combination and all ceramic. The high strength glass was discarded because the initial samples indicated a high electrical leakage, and since the design of the new housing was to be appreciably larger than the existing design a housing of proportionally greater strength is required. The ceramic and glass combination was also ruled out, since this combination required a compression seal on the glass which limited the leakage path and did not permit the design of a satisfactory ultrasonic weld flange. The ceramic and glass insulator also exhibits less than satisfactory breakover voltages. Considerable experience on larger devices presently in manufacture dictates the use of a ceramic housing containing a high alumina (94%), all-ceramic insulating material.

Stud and Housing Design

The redesigned stud (Figure 11) has been simplified and improved over the existing version (Figure 12). Since a copper-to-copper joint of the housing to the stud is desired, the steel weld ring and the braze ring are eliminated. For ease of housing assembly, the stud hex thickness is increased to 0.180 inches which will give a greater mass of copper for thermal surges and present a wider wrenching surface. It is then possible to eliminate the pedestal because of the expulsionless ultrasonic weld. The housing (Figure 13) is designed to give the maximum possible area on a 9/16 inch hex stud in order to permit ultrasonic welding of the main seal and tubulations, and to have the strength necessary to meet MIL-S-19500/108A. A "T"-butt braze was selected for the eyelet-to-ceramic joint with tubes brazed through the thickness of the ceramic. The eyelet diameter is enlarged slightly more than the ceramic to permit locating and holding the housing during the main seal

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weld. With this design, it is possible to enclose pellets up to appro-
ximately 0.475 inches in diameter. A second design features one-piece
gate and cathode tube terminals. All leads are to be fed into the blind
holes and the tubes crimped. Since the tubes are already closed, a hermetic
sealing weld will not be necessary. A crescent-shaped crimp is planned
for each tube. This shape will aid in giving the tubes the required
strength to withstand centrifuge testing and customer soldering. See Figure 14.

Ultrasonic Torsional Welding

The ultrasonic torsional welder on which the initial tests were performed
has a three-transducer, hydraulic-pressure welding head which is powered
by a 2000 watt ultrasonic generator. Prior experiments on this machine
have shown that a JEDEC TO-5 Outline package, of approximately 0.350 inches
diameter, can be successfully welded in a variety of materials (e.g., copper,
aluminum, steel, nickel and kovar). Copper-to-copper or aluminum-to-
aluminum prove to be the easiest to weld and yield the most consistent
results. A copper-to-copper joint was chosen for this new package, since
it would eliminate the need for any weld ring on the stud.

Using the torsional welder, the housing and stud were welded with satis-
factory strengths obtained. However, consistently reliable hermetic seals
could not be obtained. The best welds were made at machine settings of
400-lbs. pressure and 1900 watts power for 1.5 seconds. Since these are
the limits of the welder, any further work on this machine is considered
useless. The next group of units was welded on a six-transducer machine
in the manufacturer's factory. Optimum welds were obtained at settings
of 700-lbs. pressure, 1600 watts power for one (1) second. A group of
parts welded in this manner were helium leak tested and found to be leak
tight. These units were then tube welded, had terminals attached, and
re-tested for leaks. All welds were leak-tight. The units were then sub-
jected to five temperature cycles, from -65°C to +200°C, and then centri-
fuged at 5000 G's. Again, there were no failures and no leakers. Four
units of this group were then centrifuged at 10,000 G's. There were no
failures and no weld leaks; however, two units developed slight leaks at
the tube-to-ceramic joint. All units were then sheared open at the main

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seal weld. The welds broke at an average strength of 190 lbs. All units pulled a copper nugget out of the housing flange.

Based on this experience, a new welder is being designed which will have four transducers, a weld force of 1000 lbs., and a 2000 watt power supply. A wooden mock-up of the welder has been made and specifications for the final design agreed upon. This machine is scheduled for test, in the manufacturer's plant, during December, 1963.

Surface to be flat within
.003 & free of any plating.
May be 32/

.556

.180

.437

90°

1/4 - 28 UNF 2A
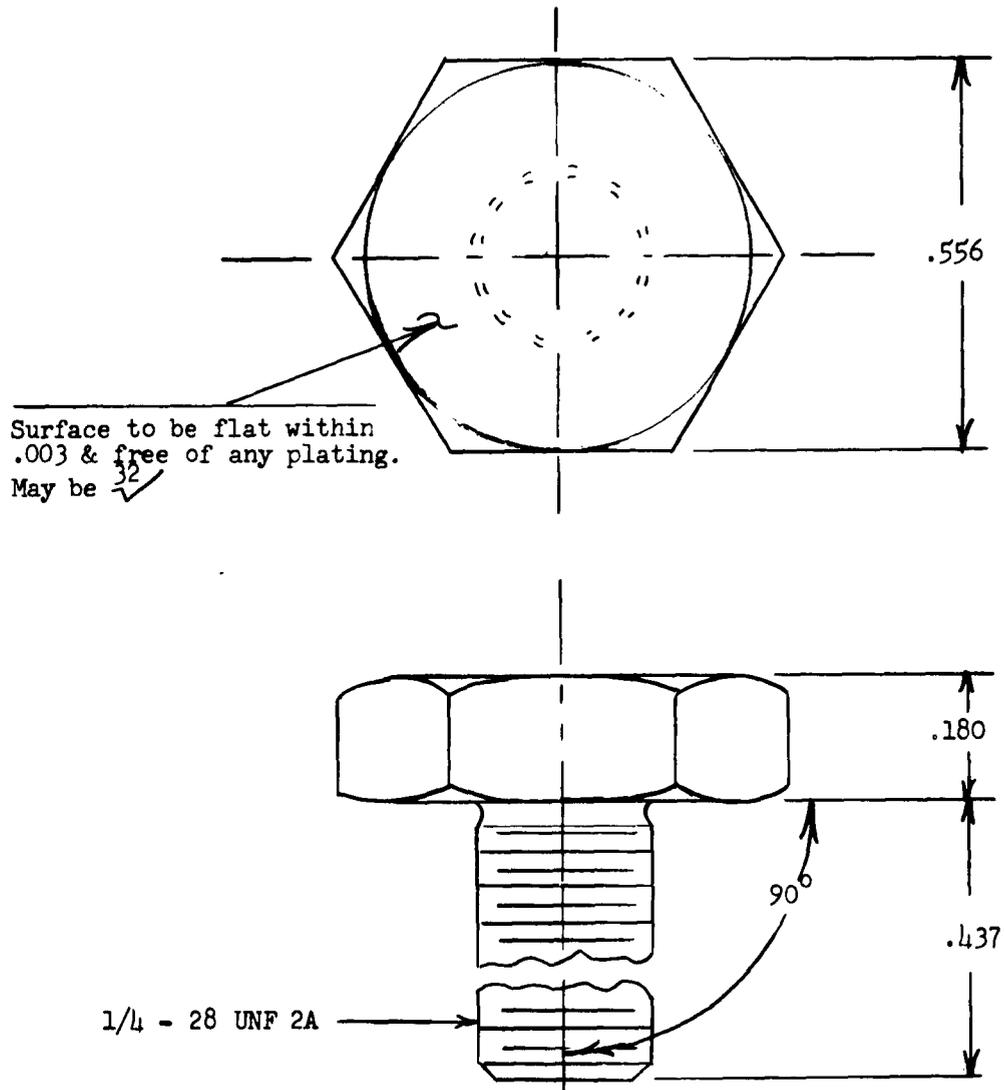
Mat'l: Copper alloy M-156 or equiv.

Finish: Dull sulfamic nickel, .0002 to .0003 thk.

Figure 11 - Redesigned stud

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.515
Dia. of weld ring

.556

.030 →| |← .010
         .012

.007

Weld Projection
Detail

Top surface of .305 dia
to be bare (not Ni plated).
May be .125

|← .455 →|

|← .305 →|

Braze must be a
hermetic seal.
Mat'l: Silver-copper

.060

.120

90°

1/4 - 28 UNF 2A ──→

.437

Mat'l: Stud to be copper alloy M-156.
Finish: Dull sulfamic nickel.

Mat'l weld ring: L.C.S. BℓA1B.
Finish: Same as for stud.

Thickness of plating: .0003 to .0006

Figure 12 - Existing stud

.540 Dia.

Mat'l: 42.6 Ni-Fe
(both tubes)

OFHC copper tube
approx .170 long

Alumina
94%

.480 Dia.

.500 Dia.

.090

.020

.060

.012

.090 Min.

90°

.656

.516

.281

.156

.093

.175

.340

.141

Mat'l: (1) OFHC tellurium copper, .012 thk.
        (2) Copper clad steel, 30% Cu 70% steel
            Cu on inside dia. to be .012 thk.

Figure 13 - Redesigned housing

Figure 14 - Alternate design housing

CHAPTER 3 - RELIABILITY TEST PROGRAM

Purpose

The purpose of this evaluation is to provide a feedback to the production line on the process and control changes concerning product distribution and reliability, and to provide a final measure of product distribution and reliability after all improvements have been implemented.

The evaluation consists of several parts:
1. An identification and measurement of failure mechanisms.
2. A measurement of product capabilities.
3. The determination of product distribution.
4. The estimation of long-term reliability.

It is understood that within funding limitations of this contract the actual demonstration of the reliability goal of 0.05% per 1000 hours failure rate will not be possible at the recommended maximum conservative design conditions. It is planned, therefore, to estimate this failure rate by suitable extrapolation from the increased stress condition.

Determination of failure mechanisms and product capabilities will be accomplished by a series of step-stress tests until at least 63% of the devices have been destroyed. These tests will be performed at first on the initial product, and then again on the improved product. They will be the primary means used to demonstrate product improvement.

A failure rate verification test will also be performed on the improved product at several stress levels of temperature and voltage, so that a regression analysis will permit a strong basis for extrapolation to the failure rate at the recommended conservative design conditions as well as verifying the conclusions indicated by the step-stress tests.

Progress

It was anticipated that special equipment and procedures would be required
to achieve the objective of this program. These include: (1) Automatic
Test Equipment; (2) Machine Data Processing Procedures; and, (3) Stress
Equipment for step-stress tests and life tests which are discussed in the
following sections.

1.   Automatic Test Equipment

In order to produce good statistical results from the step-stress and
life test experiments, it is necessary to acquire measurements at fre-
quent intervals in spite of the large number of units on test. Therefore,
in order to perform the hundreds of thousands of measurements prescribed
by the test plan, an automatic measuring and recording device is needed.
Such a machine has been developed for this program; the objectives incor-
porated into its design are as follows:

A.   To measure parameters such as:

1) Forward drop within the range of 0.1 to 100 amperes (2 msec
   sinusoidal pulse).

2) Forward leakage current at constant voltage within the range
   of 10^{-9} to 10^{-2} amperes, at 0 to 1600 volts dc.

3) Reverse leakage current at constant voltage within the range
   of 10^{-9} to 10^{-2} amperes, at 0 to 1600 volts dc.

4) Forward leakage current at constant power within the range
   of 10^{-9} to 10^{-2} amperes, at 1 to 25 watts reverse power dc.

5) Reverse leakage current at constant power within the range
   of 10^{-9} to 10^{-2} amperes, at 1 to 25 watts reverse power dc.

6) Forward blocking voltage at constant current within the
   range of 0 to 1600 volts at 10 uA to 100 mA dc.

7) Reverse blocking voltage at constant current within the
   range of 0 to 1600 volts at 10 uA to 100 mA dc.

8) Gate voltage to fire, within the range of 0 to 5 volts dc.

9) Gate current to fire, within the range of 0 to 100 mA dc.

10) V_{BO} within the range of 0 to 2000 volts dc.

B.   To make measurements accurately and rapidly.

C.   To produce data in a form which will be adaptable to computer
     processing.

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A block diagram for the system is shown in Figure15. The timer is the heart of the system, and its control circuit provides signals to each of the other circuits at the proper intervals to insure the correct sequence of operation.

The first signal of each cycle goes into a stepper that switches each unit on the test tray into the test circuit, consecutively. The next signal from the timer circuit applies power to the test circuit. Different test circuits are used for each parameter to be measured; for example, to measure reverse current the voltage drop across a resistor in series with the test device is measured. For forward voltage drop, the voltage across the unit is measured. The timer circuit then triggers the digital voltmeter to measure the test voltage. This voltmeter consists of a voltage-to-frequency converter and a frequency converter. This then feeds into a serial converter. The output, in the binary form, is then available for recording.

Because the blocking currents of a tray of silicon controlled switches may vary over two or three decades, it is necessary to incorporate a circuit which inserts a series resistor that can give the most significant voltage reading. After the voltage reading is taken across the series resistor, the logic circuit is energized. By observing the number of zeroes to the left of the first significant digit, the circuit inserts a resistor which provides a more significant reading. When the proper resistor is selected, the voltmeter is again triggered to take the final reading. Following this reading, a serial converter is actuated to scan each digit of the reading, convert the binary code to a Flexowriter* code, and enter this reading into the automatic typewriter. In addition to entering the three digits from the voltmeter, a decimal point indicator is also entered. This is obtained from the configuration of the logic circuit.

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*Registered Trade Mark of Friden, Inc.

In the event that a reading is larger than the range of the voltmeter, an over-range indication is obtained. This is also entered into the automatic typewriter. After the converter enters the information into the Flexowriter, the timer removes the test voltage and the cycle is complete. The next signal from the timer advances the scanner and repeats the cycle on the next device. Then, when the scanner has measured the twenty-fifth unit, it provides a signal which disables the timer. In order to start another test run, the timer must be re-activated by a push button.

The Flexowriter, a programmatic typewriter manufactured by Friden, Inc., has a manual keyboard and a tape reader so that information may be inserted at various points to identify the data before each test run. The data is then presented in two forms, as a printed paper tape and as an eight-channel punched tape.

The check out procedure consists of performing the various measurements on a tray of resistors, representing typical devices, on sequential days until there is substantial agreement on the individual readings for three days in a row. The computer is then used to normalize the data on a percent shift basis. Thus, it is possible to prepare statistics for the percent error of the automatic tester. Thus far, several of the measurement circuits had to be reworked and random errors appear due to burn-in of components in the tester. These are being corrected but the check out is taking longer than anticipated, and will delay the test start date by approximately five weeks.

2.   Data Processing

Identification data is manually placed on an eight-channel paper tape through manual operation of the automatic typewriter. Following this, the test data is automatically punched on the paper tape, and the arrangement is such that the tape-to-card converter is able to follow the format in producing the data cards for the computer. The printed paper tape which is also generated by the Flexowriter enables inspection of the data for obvious errors as the data is recorded.

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The IBM-type data cards are then analyzed on a General Electric Model
225 Computer, using a Statistical Analysis Program written especially
for this program. The computer program calculates mean, standard
deviation, and variance for data that is normally distributed. For
non-parametric data, it will classify the data into 40 cells which can
be pre-defined to produce frequency, relative frequency, and cumulative
increasing and decreasing relative frequency. Life test data can then
be compared with the initial data to produce the above statistics on a
delta shift, or on a percent shift basis.

Typical data have been analyzed to establish the cell grouping intervals;
thus, this portion of the program is completed.

3.   Stress Equipment

Stress equipment has now been exposed to the first operational check out.
The several faults found are now being repaired.

Four trays of "load" units are assembled for use in the final evaluation
of the stress equipment. The actual test samples are mounted on heat-
sink plates, and will be wire checked using the automatic tester.
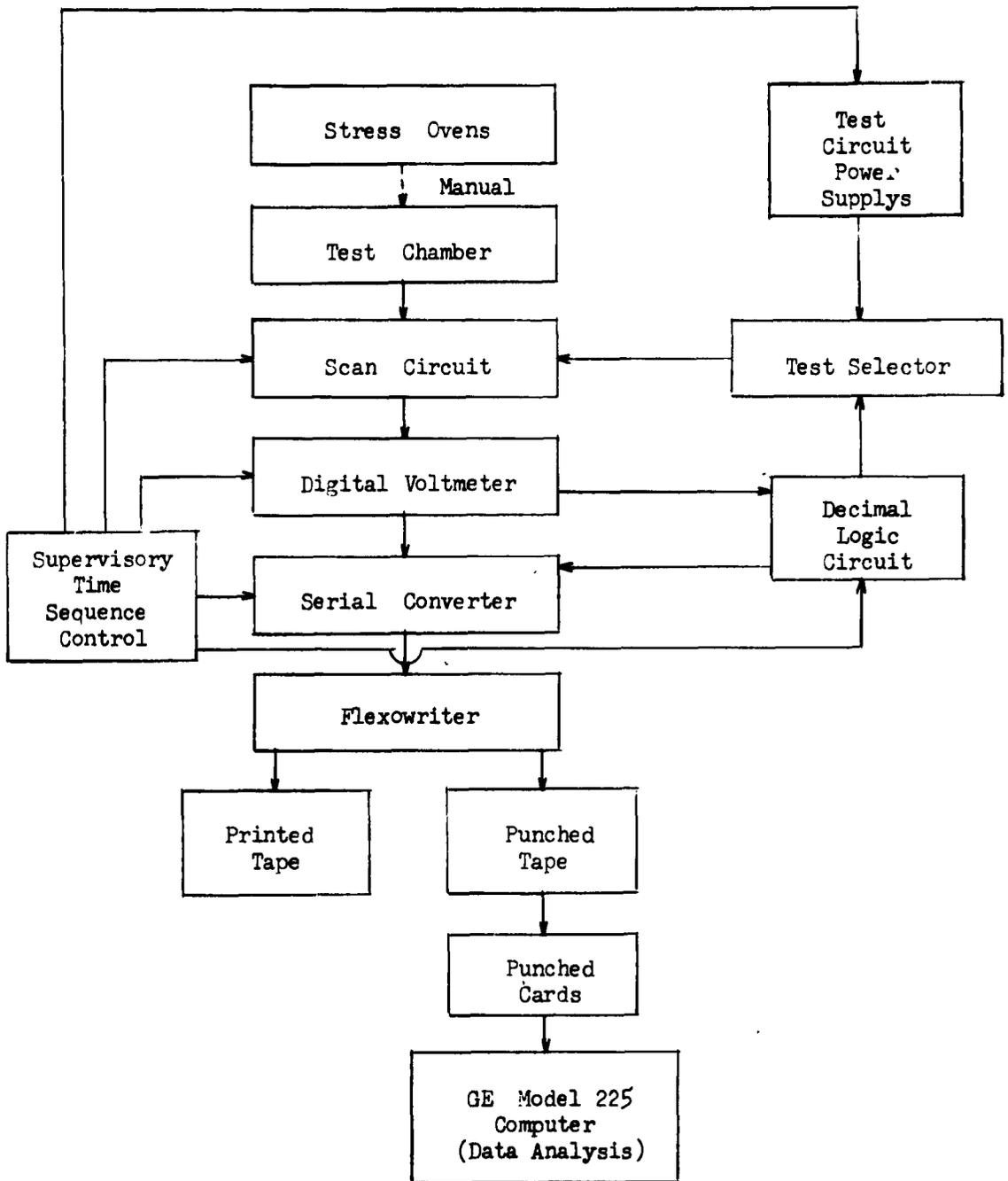
Figure 15 - Matrix life test flow chart, ADPS

CHAPTER 4 -- SEMICONDUCTOR MATERIALS IMPROVEMENT PROGRAM

Introduction

Little has been published concerning the effect of dislocation and arrays of dislocations upon the electrical behavior of semiconductor devices. It has been postulated that dislocations, because of their associated stress field, could cause an enhanced diffusion, and also provide preferential sites for the clustering of impurity atoms and the subsequent nucleation of undesirable second phases. The enhanced diffusion of impurity atoms along the dislocations could produce in an all-diffused device an undesirable diffusion profile, which could reflect in poor device characteristics. The clustering of the impurity atoms and/or the subsequent precipitation of unwanted second phases at dislocations could cause some localized electric field perturbations during the operation of the semiconductor device which result in erratic electrical behavior or total failure. These interactions of the impurity atoms with dislocation stress fields undoubtedly do occur, but the question remains as to whether or not the consequences of these interactions are of sufficient magnitude to reflect in the gross electrical behavior of semiconductor devices.

It is the purpose of this investigation program to determine the effect of the dislocations, and the unique arrays of dislocations upon the electrical behavior of a high-speed, all-diffused, silicon controlled rectifier.

Material Evaluation

Different lots of 2N689 type silicon controlled rectifiers will be fabricated by using the standard diffusion process and standard mount-down procedures for this device. The only difference between the lots will be the silicon crystal starting material; each lot will constitute either a different degree of crystal perfection or a different crystal growth ambient. Each set of devices will be subjected to identical electrical performance tests. The data will then be used to establish any existing correlation between device quality and the degree of crystal perfection of the starting material.

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The following different floating-zone silicon crystal starting materials will be evaluated:

1. Dislocation-free or silicon containing a vanishingly-low dislocation density.

2. Silicon containing nominally 20,000 to 30,000 dislocations per cm^2, randomly distributed. This silicon is to be grown in a vacuum.

3. Silicon containing nominally 20,000 to 30,000 dislocations per cm^2, randomly distributed. This silicon is to be grown in an argon ambient.

4. Silicon containing lineal arrays of dislocations (lineage) which has been grown in a vacuum.

5. Silicon containing lineal arrays of dislocations (lineage) which has been grown in an argon ambient.

In addition, it is intended to evaluate low dislocation, relatively high oxygen content Czochralski silicon in our Materials Laboratory which is equipped to conduct failure analysis of any device that exhibits serious deviations in electrical behavior. Attempts will be made to determine failure mechanisms, and to establish a correlation between failures and crystal imperfections.

Two lots of silicon wafers are presently being diffused for future fabrication of 2N689 type devices. These two lots constitute silicon containing nominally 20,000 to 30,000 dislocations per cm^2, randomly distributed. One silicon crystal lot has been grown in a vacuum, and the other in an argon ambient. Other classes of silicon materials are being requisitioned, and will be processed upon receipt.

In order to make certain evaluations, the following equipment and techniques are presently available in the Materials Laboratory for analysis purposes:

1. Optical Microscopy - A Leitz-Wetzler Metallograph capable of 1500 magnifications.

2. Infrared Microscopy ·· Employing a low-distortion infrared converter tube in conjunction with the Leitz Metallograph, it is possible with the use of transmitted infrared radiation to see through relatively thick sections of silicon.

3. Standard X-Ray Diffraction - This equipment is presently being modified to yield x-ray extinction photograms. Upon completion, the x-ray facility will provide a technique capable of clearly revealing internal crystal imperfections and such phenomena as impurity clustering and precipitation.

4. A technique for visually observing temperature distributions in a device during actual biasing conditions, when the device is in the sandwich state.

5. A technique for retrieving the whole silicon pellet from a finished device without any mechanical damage to the pellet. This is a valuable technique which will facilitate failure analysis.

SECTION IV

CONCLUSIONS

PERT Analysis

I. Ultrasonic Torsional Welder

Mainseal welding of the newly designed ceramic package was done in
the laboratory on a three-transducer welder. This machine was
borderline and did not supply enough energy for a strong and reliable
weld. This possibility was considered and is reflected in the PERT
chart submitted to USAEMA on 23 July 1963 where the earliest allowable
time between "Torsional Welder Parts Designed" and "Weld Process
Established" was two weeks and the latest allowable time was given
as 32 weeks. The anticipated difficulty became a reality. Experi-
ments were performed at a vendor's plant on a six-transducer welder.
With only the mechanical results available from the three- and six-
transducer welders, the General Electric Company has contracted for
the design and manufacture of a new four-transducer welder. This
represents a risk that must perforce be made so that the ultrasonic
torsional welder will be operable on the production line before
June, 1964. We could not wait for detailed electrical life test
results before unequivocally determining the new package design.

II. One-Piece Tubulation Terminal Design

Until the ultrasonic mainseal tests at the vendor's plant were made,
there was no point in ordering parts for the one-piece terminal.
These tubulation-terminal pieces were designed for an expensive
ceramic housing and if the ultrasonic technique for mainseal welding
failed, there would be no need to alter the housing material. The
use of the one-piece terminal would also require some major process
innovations; for example, we would have to eliminate a final 24-hour
nitrogen bake since the housing tubulations would enter the line as
sealed parts. Therefore, in order to evaluate the use of a one-piece
terminal, extensive life tests would be required. This would preclude

the installation of all process innovations on the line within the 12-month period specified by the contract. Consequently, we shall proceed with the alternative path which utilizes the open tubulations for gate and cathode and two-piece terminals.

The revised PERT diagram is shown in Figure 16 with the new critical path and includes the program for making the four-transducer welder operational. For a comparison, the one-piece terminal PERT program is given by Figure 17 and is longer by nearly 20 weeks. The General Electric Company will continue to develop the one-piece terminal for improved reliability and performance but, of course, on an unscheduled basis.

III. Surface Stabilization

The surface stabilization program as depicted on the critical path in Figure 16 becomes ready for engineering pilot operation 32.8 weeks after the "Start". By utilizing the experience and knowledge gained on a U.S. Naval Research and Development Contract*, we will shorten this time by 9.1 weeks. In addition, the aforementioned development contract has increased our confidence of passing the "Continuous Blocking Life Test" which is also on the critical path. The estimated time between this event and completion of the "Surface Stabilization Program" has been reduced from 18 to 12.3 weeks. The length of the critical path becomes 85 weeks which is in good statistical agreement with the time specified by the present contract.

IV. Reliability Test Program

The automatic test equipment was to have been installed and debugged 13.8 weeks after the "Start". The machine has been built and we expect to complete the troubleshooting by the 19th week. This delay of 5.2 weeks should not affect the termination date of the overall program since this particular event is not on the critical path.

* "Research and Development of High Current & High Voltage Silicon Controlled Rectifiers", Navy Department Bureau of Ships Contract # NObsr-87648.

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Figure 16 – PERT program using two piece tubulation-terminal

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SECTION V

PROGRAM FOR NEXT INTERVAL

ALL-DIFFUSED DEVICE PROGRAM

Programmed work will continue on the evaluation of contact plating and
the solders used to attach the backup plates to the silicon pellet; as
well as, the chemical etch procedure, parts preparation and cleaning
cycles involved in the step-by-step processing of the all-diffused device.

Some tools and equipment for processing are presently in operation. These
include "alloy" or solder fixtures, stud mounting fixtures, and bevel
cutting fixtures. Work is also continuing on those items not available
at this time.

The first Engineering samples of an all-diffused SCR will be delivered
during the next quarterly report period.

DEVICE STUD AND HOUSING PROGRAM

Additional samples containing actual silicon subassemblies will be welded
on the vendor's six-transducer welder while waiting completion of the new
welder. Tests using the new welder are expected to be performed in
December, 1963. Tests made on the new samples will be performed to deter-
mine whether, or not, ultrasonic energy causes any damage to the pellet.
Since these samples must be welded outside a dry box atmosphere, a control
group of devices will be exposed to the same conditions and then resis-
tance welded.

RELIABILITY TEST PROGRAM

Reliability test plans for the next quarter include the performance of
the step-stress tests, in accordance with the schedule, with a major effort
devoted to the recovery of time lost.

SEMICONDUCTOR MATERIALS IMPROVEMENT PROGRAM

The anticipated activity for the next quarter will include the fabrication of two lots of devices which will be subjected to electrical performance tests. Additional sets of silicon wafers will be processed as they become available.

SECTION VI

PUBLICATIONS AND REPORTS

REFERENCES

1. F. W. Gutzwiller, et al, <u>Silicon Controlled Rectifier Manual</u>,
   Rectifier Components Department, General Electric Company, 1961,
   para. 3.7.5.

2. R. F. Dyer and G. K. Houghton, "Turn-Off Time Characterization
   and Measurement of Silicon Controlled Rectifiers", A.I.E.E. Con-
   ference Paper, CP 61-301.

3. R. L. Davies, "Data and Calculations of the SCR Turn-On Mechanism",
   Advance Engineering, Rectifier Components Department, General
   Electric Company, August 1963.

4. M. V. Sullivan and J. H. Eigler, "Electroless Nickel Plating for
   Making Ohmic Contacts to Silicon", Journal of Electrochemical
   Society, Vol. 104, No. 4, pp 226-230.

5. Quarterly Progress Report, 30 June 1962 to 30 September 1962,
   Contract Number NObsr-87648, Project Serial Number SF-013-11-05,
   page 8, Navy Department Bureau of Ships.

MEETINGS AND CONFERENCES

On 20 August 1963, a meeting with U.S. Army Signal Corps personnel
was held at the Rectifier Components Department of the General Electric
Company at Auburn, New York to discuss the contract requirements and
to reach a mutual understanding of the objectives of the program. The
following personnel were in attendance:

J.	Bressler, USAEMA, Philadelphia, Pa.
H.	DePol, USAEMSA, Ft. Monmouth, N.J.
E. B.	Hakim, USAERDA, Ft. Monmouth, N.J.
N.	Lipman, USAEMSA, Ft. Monmouth, N.J.
B.	Reich, USAERDA, Ft. Monmouth, N.J.
A. S.	Rugare, G.E. - SPD, Syracuse, N.Y.
T. F.	Kendall, G.E. - SPD (Govt. Relations), Syracuse, N.Y.
H.	Fishman, G.E. - RCD, Auburn, N.Y.
W. R.	Comstock, G.E. - RCD, Auburn, N.Y.
J. N.	Frank, G.E. - RCD, Auburn, N.Y.
A.	Hishta, G.E. - RCD, Auburn, N.Y.
J.	Moyson, G.E. - RCD, Auburn, N.Y.
R. C.	Rome, G.E. - RCD, Auburn, N.Y.

PATENT DISCLOSURE

From entries made in Patent Notebook No. 025, page 2, dated 14 August 1963, a patent disclosure letter was prepared on 29 August 1963. This disclosure, properly authenticated and witnessed on 30 August 1963, documents a plating procedure to prevent the fracturing and penetration of a 2N689 type switch pellet by hard solder, during the alloying cycle, through separation of the solder by multi-layer of vapor deposited metals.

This invention, conceived and developed by J. N. Frank and R. A. Stott of the Engineering Section, Rectifier Components Department, General Electric Company, at Auburn, New York, under the auspices of this contract, will be utilized in the production improvement program for the 2N689 type SCR.

SECTION VII

IDENTIFICATION OF TECHNICIANS

TECHNICAL PERSONNEL

The names of the engineers performing work on this contract for the
first quarter are as listed below. Included herein is the summary of
manhours of work performed by engineers and technicians.

Project Director - H. Fishman, Manager - Low and Medium Current Product
Engineering, Rectifier Components Department, General
Electric Company, Auburn, New York

1. Technical Personnel

                    Engineers

          W. R. Comstock
          G. W. Fabel
          J. N. Frank
          A.   Hishta
          R. C. Rome
          H.   Wawrousek

2. Manhours Expended

Engineers	Technicians	Shopwork
1,181.0 hrs.	2,087.6 hrs.	516.5 hrs.

BIOGRAPHIES

Biographical Sketches of the key technical personnel (listed above) who
have performed work under this contract during the first quarter are as
follows:

W. R. Comstock - BSEE, 1945, Cornell University.

Mr. Comstock joined the General Electric Company on the Test Engineering Program following his graduation.

In 1949, he was assigned to the Transformer Division working on lightning arrester development.

Then, in 1955, he transferred to the Semiconductor Products Department with an assignment in the Rating and Evaluation Engineering unit of the Rectifier Products Section.

In 1959, he moved with this engineering group to the Auburn Plant where he performed evaluation work on medium-current rectifiers, zener diodes, and controlled avalanche rectifiers.

Since January of 1962, he has been assigned as a Reliability Evaluation Engineer for the Rectifier Components Department.

G. W. Fabel - 2 years, R.C.A. Institutes - Electrical Engineering International Correspondence School - Mechanical Eng'g.

Mr. Fabel joined the General Electric Company in 1942 with the Electronics Department working on development and product design of military electronic equipment. He continued work on product design when this Department became the Radio and Television Department, and transferred to Syracuse, New York.

In 1960, he transferred to the Rectifier Components Department and was assigned to the Mechanical Development Engineering group. His work has been in the area of device packaging, ultrasonic welding, and leak detection.

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H. Fishman   - AB (Physics), 1949, Brooklyn College.

MS (Physics), 1951, University of Rochester.

Prior to joining the General Electric Company on the physics program in 1951, Mr. Fishman was a research and teaching assistant at the University of Rochester. He joined the Semiconductor Products Department in 1952 as an engineer in Rectifier Engineering with assignments that included development work on ceramic diodes and silicon low-current rectifiers. In 1955, he transferred to the Department's Transistor Engineering group where he worked on the design, development and pilot line production of silicon unijunction transistors. A year later, he was assigned to the Single Crystal Engineering unit where his prime responsibility was to coordinate the semiconductor material needs of the device areas within the crystal growing operation.

Just prior to his promotion as a consulting engineer in 1959, Mr. Fishman was engaged in the development of the germanium high-speed mesa transistor and was responsible for performance analysis studies. In 1960, he was promoted to the position of Manager of the Germanium Mesa Transistor Engineering unit. Then, in 1962, he was transferred to the position of Manager of Advanced Pellet Engineering with responsibilities for the advance design and development of structures for planar passivated silicon transistors in very high frequency applications.

Then, on February 11, 1963, Mr. Fishman transferred to the Rectifier Components Department as Manager of Low and Medium Current Product Engineering with responsibility for low and medium current product designs which meet the Department's production timing and cost objectives. In his present position, he has been appointed Project Director for Item 4 of the USAEMA Contract DA-36-039-AMC-03619 (E).

J. N. Frank   - BSChemE, 1951, Washington University.

Mr. Frank joined the Aircraft Nuclear Propulsion Department of the General Electric Company in 1952 as an engineer. In 1953, he transferred to General Electric's Knolls Atomic Power Laboratory as a research assistant.

In 1959, he transferred to the Semiconductor Products Department as an engineer in the Rectifier Products Section. He is presently a Product Engineer in the Rectifier Components Department working in the Rectifier Components Department working on medium current silicon controlled rectifiers.

A. Hishta   - BSChemE, 1948, Pennsylvania State College.

Following his graduation, Mr. Hishta joined the General Electric Company on the Chemical - Metallurgical Test Program. After various assignments, he joined the Plastics Division at Decatur, Illinois.

Then, in 1950, he transferred to the Semiconductor Products Department as a Project Engineer working on controlled rectifiers for the Rectifier Products Section. Since 1960, he has been working as a Product Engineer in the Rectifier Components Department on low-current, light sensitive, and gate turn-off silicon controlled rectifiers.

R. C. Rome   - BSME, 1951, Polytechnic Institute of Brooklyn.

Mr. Rome joined the Pratt and Whitney Aircraft Corporation as a production engineer following his graduation.

In 1956, he joined the Jet Engine Department of the General Electric Company as a producibility engineer. Then, in 1960, he transferred to the Rectifier Components Department as a Mechanical Development Engineer. His present area of work concerns device packaging development, printed circuit boards, stack and assembly design, and development work in the area of welding, brazing and soldering.

H. W. Wawrousek -BSMetE, 1951, Rensselear Polytechnic Institute.

MSMetE, 1953, Rensselear Polytechnic Institute.

PhD (Met), 1957, Rensselear Polytechnic Institute.

Following his graduation in 1951, Mr. Wawrousek was employed by Rensselear Polytechnic Institute as a research associate working on a welding project subcontracted by the Knolls Atomic Power Laboratory of the General Electric Company. Results of this work were reported in his masters thesis.

In 1953, he started work on his doctorate degree under an Alleghany-Ludlum Steel Company industrial fellowship. Mr. Wawrousek's PhD thesis was based on "Micro-Creep in Molybdenum Single Crystals at Room Temperature".

In 1957, he joined the laboratory of the Transformer Division of the General Electric Company where his work involved the application of modern research techniques to the metallurgy of silicon-iron alloys in order to gain a basic understanding of the metallurgical mechanisms which promote the highest magnetic quality.

Since 1961, Mr. Wawrousek has been associated with the Rectifier Components Department in the Materials Engineering unit where his work has been in the areas of epitaxial growth and crystal imperfections.

APPENDIX

CONTRACT TASK CROSS REFERENCE

The following table identifies the appropriate chapter of Section III of this Quarterly Report with the tasks shown under Item 4 of the contract, and lists the Project Engineer responsible for each task:

Contract Task Item 4	Quarterly Report Section III	Project Engineer
a. Main seal weld	Chapter 2	R.C. Rome
b. Tubulation crimp and weld	Chapter 2	R.C. Rome
c. Surface stabilization	Chapter 1	A. Hishta
d. Cathode junction formation	Chapter 1	J.N. Frank
e. Control of silicon growth and diffusion processes	Chapter 4	H. Wawrousek
f. Reliability test program*	Chapter 3	W.R. Comstock

*Note: This task is part of the overall program but is not indicated in Item 4 of the contract.