# SIXTH QUARTERLY REPORT
COMPATIBLE TECHNIQUES
FOR
INTEGRATED CIRCUITRY

U. S. AIR FORCE
CONTRACT NO. AF33(616)8276

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1 August 1962 to 31 October 1962

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AERONAUTICAL SYSTEMS DIVISION

WRIGHT-PATTERSON AIR FORCE BASE, OHIO

MOTOROLA Semiconductor Products Inc.

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U. S. AIR FORCE

AERONAUTICAL SYSTEMS DIVISION

WRIGHT-PATTERSON AIR FORCE BASE, OHIO

Prepared by . . . .

MOTOROLA, INC.

SEMICONDUCTOR PRODUCTS DIVISION

PHOENIX, ARIZONA

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APPENDIX

1.0   INTRODUCTION

This report covers the 6th quarter's efforts in developing Compatible Techniques for Integrated Circuitry on contract AF 33(616)-8276.

Most of the effort to date has been spent in developing process techniques which are necessary for Integrated Circuit fabrication. This effort has been both in morphological areas and thin film as applied to semiconducting substrate.

The program is continuing to develop and fabricate typical circuits which are practical for a wide range of high and low frequency amplifier applications as well as logic circuits.

2.0   THIN FILM TECHNOLOGY

2.1   Deposition of Glass Films

The purpose of this task is to develop means for depositing glass films onto semiconductor substrates utilizing the technologies which are compatible with semiconducting materials and with other thin films. The films are under investigation for use as: (a) dielectric films for capacitors, and (b) electrical insulating films for conductor crossover insulation.

In a continuation of studies of the effects on the properties of deposited glass films for various deposition temperatures, a number of aluminosilicate capacitors were deposited at a substrate temperature of 300°C, and the aging characteristics of these capacitors at a high humidity room temperature environment were observed. The changes in capacitance and dissipation factor after 90 hours exposure at 97% R.H. are shown in Table I.

TABLE I

Average absolute change in $Al_2O_3 \cdot SiO_2$ Capacitors (300°C deposition) after 90 hours exposure 97% R.H. 25°C
Typical values: C = 150 mmf, D.F. = 0.5%.

F	ΔC	ΔDF
30 cps	mmf	%
100 cps	<0.4	0.5
1 KC	<0.4	0.13
10 KC	<0.4	0
100 KC	<0.4	0
300 KC	<0.4	0

During this recording period, studies to determine the optimum composition of the $SiO_2 \cdot Al_2O_3$ dielectric films were completed. This work consisted of the fabrication of a number of films with various ratios of silicon dioxide to aluminum oxide. The characteristics of capacitors fabricated from these films of various composition are shown in Table II. It will be noted that the D.C. leakage current of the capacitors, the stability of the films in a high humidity environment, and the dissipation factor of the capacitors are strongly affected by variations in the dielectric film composition. The results indicate that the best characteristics are obtained with a 6:4 ratio of silicon to an aluminum compound during deposition, while a 4:6 ratio gives D.C. leakage current and stability under high humidity conditions which are almost as good, with a higher capacitance per unit area.

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TABLE II

Ratio Si:Al Starting Compound	DC Leakage Amp	$Cmmf./mm^2$	DF % 1 kc	Stability at 97% RH
10:0	10V Short	125	5.0	Unstable - crazed
9:1	10V 12×10^{-5} 20V Short	159	4.3	Unstable - crazed
8:2	10V 1×10^{-5} 20V Short	100	1.1	Unstable
7:3	10V 6×10^{-6} 20V 18×10^{-6}	112	1.0	Unstable
6:4	10V 8×10^{-13} 50V 62×10^{-13}	100	.3	Stable
5:5	10V 7×10^{-9} 30V 13×10^{-9}	100	.47	Slightly unstable
5:6	10V 2×10^{-12} 50V 4×10^{-11}	140	.30	Very small change C & DF

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Ten capacitor units have been prepared with the optimum dielectric composition for purposes of reliability evaluation.

Future effort in this area will be directed toward the development of masking techniques for vapor deposited dielectric films, and the evaluation of reproducibility of these films.

2.2   Tantalum Oxide Capacitors

The new tantalum evaporating system was completed during this reporting period, and a few trial runs were made resulting in tantalum films of very good quality as judged by visual inspection. After a short time of operation, however, a number of leaks developed in the aluminum tubing which is used for cooling a part of the apparatus. These leaks apparently resulted from corrosion due to the comparatively high PH of the tap water which was used as the cooling agent. In order to rectify this situation, the aluminum tubing is presently being replaced by copper tubing, which is much less susceptible to corrosion. Following these repairs, the apparatus will be calibrated, and optimum deposition parameters determined.

During this reporting period, research was initiated into a new concept in anodizing of tantalum films. This new technique consists of oxidation of the film in a low pressure oxygen glow discharge, rather than in the conventional liquid electrolyte. The technique is essentially one of placing the tantalum film near the positive column of a low pressure glow discharge, with the tantalum film at a positive potential with respect to the anode of the discharge. The positive film apparently attracts negative oxygen ions from the discharge plasma, resulting in oxidation of the surface of the film. Initial efforts have

shown that this technique will result in surface oxidation to a fair degree of uniformity of oxide thickness, as judged from the color of the oxide film.

If this technique proves feasible, it is expected to yield considerable advantage over the wet electrolyte method of anodizing since it is an essentially clean process and should result in smaller impurity content in the oxide film and should alleviate problems of undesirable effects on the semiconductor substrate.

Development of techniques for making electrical contact to tantalum film during anodizing are continuing. The current approach involves the attachment of the small diameter aluminum wire to the tantalum film by ultrasonic bonding techniques. This technique appears at present to offer a great improvement over previous methods of establishing contact. Aluminum wires have been bonded to tantalum film, and the bond strength appears to be excellent; the wire will break before the bond fails. Tantalum film anodized by the utilization of this type of contact appeared to be satisfactory.

2.3 Summary of Capacitor Properties

The properties of typical thin film capacitors utilizing silicon monoxide, tantalum oxide, and aluminum silicate dielectric films are shown in Table III.

2.4 Low Temperature Deposition of Tin Oxide Resistors

A cursory examination of X-ray diffraction patterns of various undoped tin oxide films has revealed a polycrystalline

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TABLE III

THIN FILM CAPACITORS TYPICAL PROPERTIES

Diel.	Electrodes	Diel. Thickness	Cap. uuf/mm²	T.C. ppm/°C 1 kc	Lkg. @ 10 V 150 uuf u Amp Typ.	V Rating	Max T Operating	D.F. 150 uuf			30°C	
								100 C	1 kc	100 kc	1 mc	10 mc
SiO	Al	3 u	17.7	+400	.005	25	85°C	5%	2.5%		0.7%	2.5%
Ta_2O_5 (Anodized)	Ta-Au	25 V. Anod.	4000	+400	$<10^{-4}$	6	125C	1%	1%	1.5%	10%	
		100 V. Anod.	1000	+275	$<10^{-4}$	25	125C	0.4%	0.4%	1%	5%	
Al_2O_3	Al	3000 Å	850		$<10^{-4}$		<125C	0.5%	0.4%	0.3%	1%	
$.SiO_2$		6000 Å	425		$<10^{-4}$		<125C	0.5%	0.4%	0.3%	1%	

nature of the film and identified it as tin oxide. Films have been prepared under two different vapor flow conditions and in two different atmospheres (He and CO_2). X-ray diffraction measurements have been completed and give no indications that the two deposition parameters mentioned above affect the physical or chemical properties of the film. It is questionable, however, that any difference would be revealed by this technique.

A similar set of films is now ready for tcr evaluation. These measurements have been delayed, however, due to the necessity of making certain modifications in the tcr measuring equipment. Completion of this work should be effected during the next reporting period.

Past experience has indicated that the shorting out of chromium gold solder tabs to the silicon dioxide dielectric occurs when the passivated layer is defective, or is less than the recommended thickness of 1 to 2 microns. The shorting observed in the current work can be alleviated by using the silicon wafers with thicker thermally grown passivated surfaces, i.e., 1 to 2 microns, or an alternative approach which would involve the vapor deposition of a glass film over the passivated wafer surface.

During this reporting period, efforts consisted primarily of investigation of techniques for doping tin oxide films with phosphorus and antimony. Initial attempts to dope with antimony have not been successful. Films of measurable resistance have been produced, however, by doping tin oxide films with phosphorus. These were produced by the hydrolysis of mixed vapors of PCl_3 and $SnCl_4$ picked up by a carrier gas passed through a reservoir containing a solution of PCl_3 and $SnCl_4$.

It has been determined that films with measurable sheet resistance (10^8 ohms per square) can be deposited from a solution of $SnCl_4$ and PCl_3 containing no more than 1% (by volume) PCl_3.

Starting with the 1% PCl_3 - $SnCl_4$ solution, a series of films having a thickness of approximately 3000 Å were deposited. As the concentration of PCl_3 was decreased, the film sheet resistivity decreased from a maximum of 10^8 ohms per square, went through a minimum of 400 ohms per square, and then increased to approximately 1000 ohms per square as the PCl_3 concentration approached zero.

During the next reporting period, a new flow system will be incorporated into the deposition apparatus to facilitate positive control over dopant concentration in the carrier gas stream. Doping agents will be evaluated by comparison of the relative resistivities of doped and undoped tin oxide films. In addition, X-ray diffraction and spectrochemical analysis, temperature and aging stability tests, and tcr measurements will be made on successfully doped tin oxide films as the facilities become available.

2.5   Packaging Research

Efforts devoted towards the development of techniques for depositing metallic conductive aluminum films at low temperatures for purposes of submodule interconnection were continued. It was found possible to vapor plate aluminum films of good appearance and adhesion at substrate temperatures as low as 265 °C. However, when deposition had progressed to the point where films were opaque, subsequent deposition was granular and not adherent. This granular

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layer could be easily removed to reveal the initially deposited smooth films underneath. Efforts to produce films of sufficient thickness to become completely opaque have been thus far unsuccessful.

2.6   Interconnections

The equipment for ultrasonic bonding of aluminum foil connectors has been placed in operation. A device to test the strength of the bonds has been designed and is near completion of construction. This device will have a capability of testing joint strength from 0 to 2 grams in milligram increments.

A module, concluding six functional electronic blocks has been interconnected using thin two sided printed circuit boards, and is now undergoing evaluation.

A survey of materials is in process to improve the status of the foil interconnect processing. The objective is to establish connections by bonding aluminum foil to connection points in a module containing several FEB's, and then remove the foil from unwanted areas by ultrasonic means. Difficulties are being encountered in stripping excess foil at the present time. The surface condition of the plastic may contribute to the difficulties. This point is under investigation.

Samples will be fabricated during the next reporting period for your use in the evaluation of deposited aluminum conductors.

3.0   THIN FILM FABRICATION

Tin oxide resistors have been made both as a separate chip and as an integral part of circuit elements. They are being grown in a new spray atomizer system that is producing, with antimony doping, films of 100 $\Omega/\square$ with thickness about 2000 Å. The photoresisting and etching of the tin oxide is done with 20% HCl and zink powder sprinkled onto the film. Tests are being run with the tin oxide resistors protected by a deposit of either room temperature grown SiO_2 or reactive sputtered SiO_2.

Difficulties were encountered in making ohmic contact to the tin oxide with aluminum metal. The problem was that aluminum in contact with SnO_2 will form Al_2O_3 at temperatures of 400°C. This Al_2O_3 layer was thick enough so that several hundred volts were required to break through. A solution to this difficulty has been in using an intermediate layer of metal between the tin oxide and the aluminum.

Several resistors made with nichrome have been deposited. Rough ceramics were used in one test to study the depositioned problems upon this type of material. These are now on test to determine the life of such elements. Methods of forming nichrome resistors by photoresist methods compatible with integrated circuits are now under investigation.

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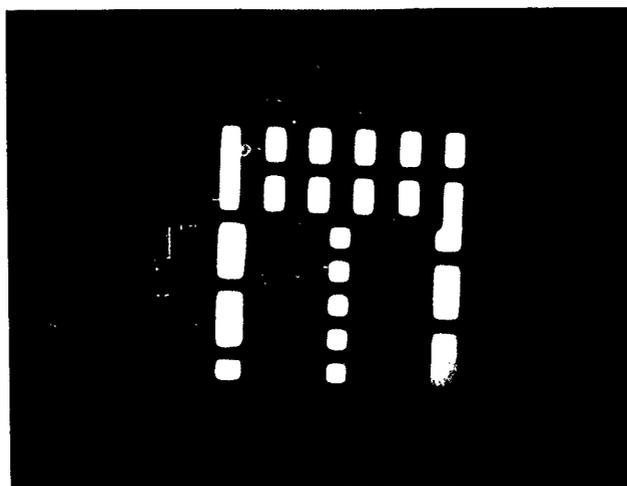
Tin Oxide Resistors with Aluminum Metallization
Deposited on a Silicon Substrate

4.0   DESIGN OF INTEGRATED RADIO FREQUENCY AMPLIFIERS

4.1   Introduction

The design and construction of functional electronic blocks (hereafter referred to as FEB) has previously been limited to medium speed digital logic circuits and low frequency amplifiers. The section will review the design and construction problems in the frequency range from 0.5 to 120 Mc.

The work was supported by the U. S. Air Force as part of a program to study Compatible Techniques for Integrated Circuit Functions.

A very successful design procedure has been evolved using four principal steps:
1. The design of a conventional receiver and transmitter.
2. The adaptation of this design using components available from the functional electronic block processes, such as diffused resistors, junction capacitors, etc.
3. The packaging of the entire receiver in TO-5 cans using a "hybrid" approach. This allows the checking of all systems problems, such as AGC and thermal stability.
4. The design and construction of the functional electronic blocks.

The use of this four step procedure has considerably simplified the design procedure and has successfully combined the skills of the circuit design engineer with those of the semiconductor device engineer.

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4.2   Design

Because of the difficulty in fabricating high Q
inductors in electronic silicon integrated circuits, an RC
amplifier design was selected. The selectivity of the receiver
is then determined entirely by quartz and ceramic filters oper-
ating at 120 Mc and 455 Kc. Quartz crystal filters were
utilized for two higher frequencies and ceramic for 455 Kc.
Tests on an RC amplifier using discrete components ("The Design
of an RC High Frequency Amplifier", Internal Communications
from W. Rheinfelder) indicate performance possibilities to 120 Mc.

The common emitter configuration was selected as the
only way of providing a cascaded gain with no impedance trans-
formation. The power gain per stage is then the produce of
voltage gain and current gain. At low frequencies, these are
equal and gain per stage is h_{fe}^2. At high frequencies, the gain
is reduced by feedback and shunt capacity. The feedback is
similar for discrete components and the problem becomes one of
reducing a shunt capacity to the silicon substrate.

The usual methods of isolation in integrated circuits
have been two back-to-back diodes and the use of resistive
isolation where the silicon bar is used as a circuit component.
The first of these methods is unsatisfactory for high frequency
amplifiers because of the shunt capacity effect of the diodes;
the second has the unsatisfactory temperature coefficient of bulk
silicon and the dependency on mechanically shaping the silicon
for accurate resistor values. A new method for providing
isolation was developed which eliminates both of these problems.
In the actual structure, a 50 x 100 mil silicon block, 6 mils

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thick, of high resistivity n-type silicon forms the substrate. The resistors are formed by diffusion and do not have the mechanical shaping or temperature coefficient problems of the bulk silicon. Two identical amplifier circuits, shown schematically in Figure 1, are built into the block by a series of masking, photo-etching, diffusion and metallizing techniques. The bar may be considered as having an RF ground in the center and each end of the bar is at the individual collector voltage potential. Thus, the coupling capacitor to the next stage is located at each end of the bar. Figure 2 shows the design layout of the amplifier.

4.3   Fabrication

As the first part of the fabrication process, a photographic mask set is designed. This mask set forms the collector, base, emitter, resistor and capacitor patterns. The mask is drawn accurately to a scale of 200:1 and then is photographically reduced. Each image is multiplied and the final processing mask set produced. A single wafer contains approximately 100 amplifier circuits.

To provide resistive isolation, high resistivity (100 Ωcm or more) n-type silicon was used for the substrate. The first mask pattern used is shown in Figure 3. This mask forms the collector, resistor and capacitor areas. The second mask, Figure 4 forms the base of the transistor as well as the required bias resistors. In this design, the resistor patterns were also made available on a separate mask, so that experiments using tin oxide resistors could be conducted. The purpose of this experiment was to investigate the compatibility of thin films and semiconductor technology. The next pattern used, Figure 5, forms the transistor emitters and the capacitors, as well as areas of high conductivity

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for contacts. The last step in the process consists of etching holes in the silicon dioxide (SiO_2) passivating layer and connecting the circuit elements by means of a thin film conductor, as shown in Figure 6. The amplifiers are then packaged in the multi-lead TO-5 header (or other suitable packages), the leads are thermo-compression bonded and the package sealed.

4.4   Electrical Test

The two-stage FEB high frequency linear amplifier thus produced has the circuit configuration shown conventionally in Figure 1. These circuits require the addition of emitter bypass capacitors to make them complete; these were not included in this first design because the practical minimum value of 500 to 1000 pf requires too much space. Future designs will unquestionably include these essential elements in some form on the FEB structure.

Complete single and double amplifiers have been fabricated in the TO-5 can by the addition of 1000 pf silicon junction capacitors and hybrid fabrication techniques. Typical mounts of this nature are shown in Figure 7.

A series of electrical tests on these amplifiers has been made as summarized on the following curves.

Figure 8 shows the voltage gain vs. frequency for four single-amplifier stages. These super-imposed curves show a remarkable uniformity in this characteristic.

A similar curve for two stages cascaded in the same TO-5 can is given in Figure 9. Note the remarkably good gain of 20 db at 50 Mc.

Y11 and Y22 admittance characteristics are shown in
Figures 10 and 11 and the reverse gain for two individual
amplifiers in Figure 12.

Finally the matched power gain of two different
amplifier units is shown in Figure 13. Here again the consistency
is most pronounced.

4.5   Conclusions

The remarkably good high frequency performance of these
amplifiers does confirm the theoretical considerations already
pointed out: That this design is inherently virtually parasitic
free and therefore suited for very high frequency FEB circuits.

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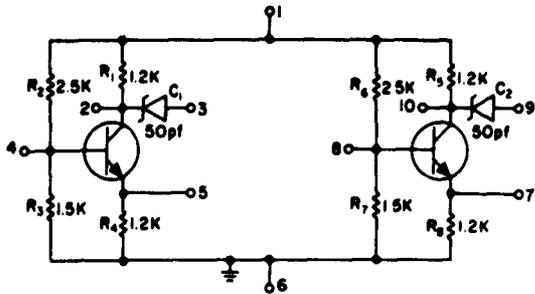
FIG. 1. SCHEMATIC OF HIGH
FREQUENCY AMPLIFIER.
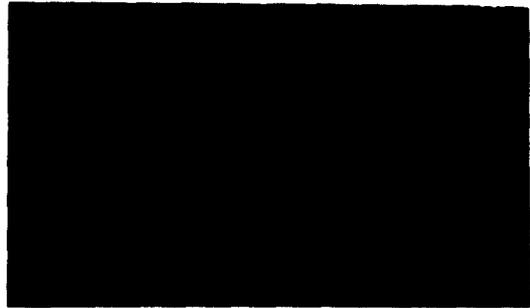
FIG. 4B. TIN OXIDE RESISTOR PATTERN
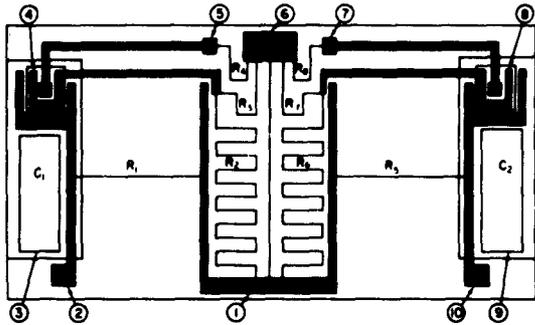
FIG. 2. INTEGRATED LINEAR AMPLIFIER
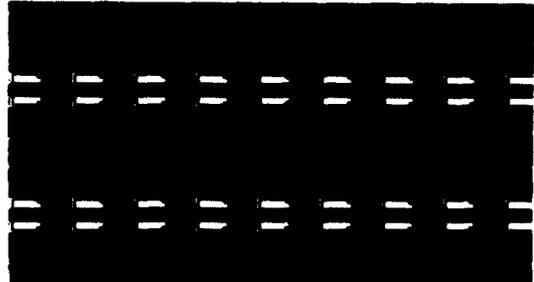
FIG. 5. EMITTER
DIFFUSION PATTERN.
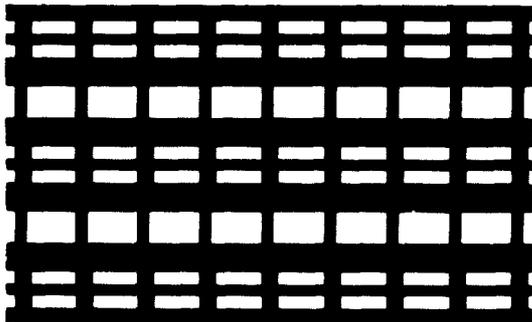
FIG. 3. COLLECTOR FORMATION
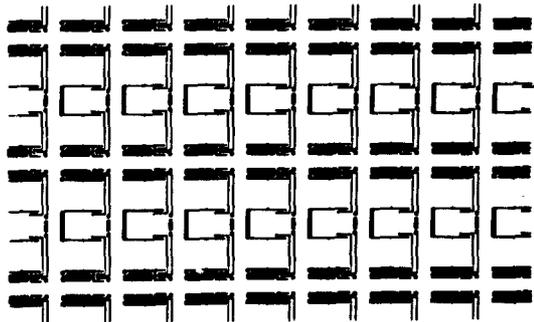
FIG. 6. METALIZATION.
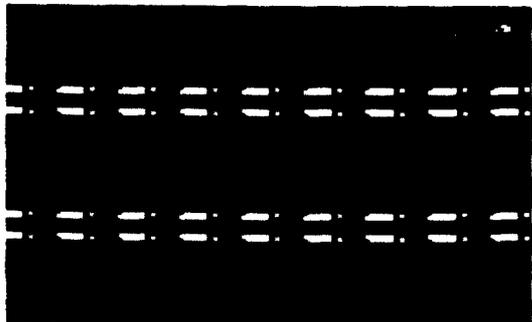

FIG. 4A. BASE PATTERN AND
DIFFUSED RESISTORS.
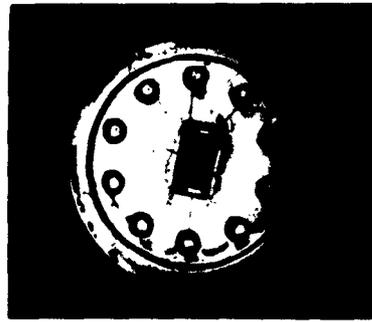
FIG. 7. COMPLETED HIGH FREQUENCY
INTEGRATED LINEAR AMPLIFIER.
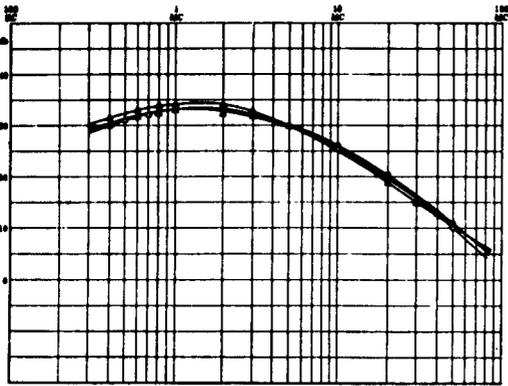
FIG. 8.   VOLTAGE GAIN OF SINGLE UNITS
SHOWING UNIFORMITY.
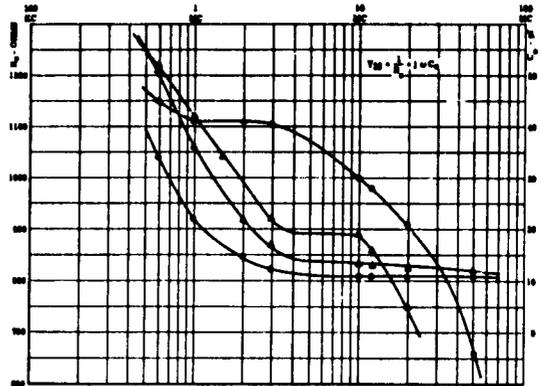
FIGURE 11.
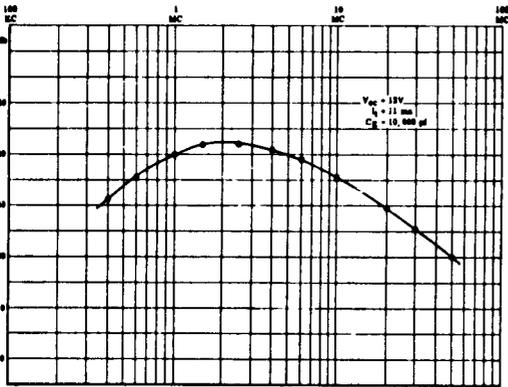
FIG. 9.   CASCADED AMPLIFIER
VOLTAGE GAIN.
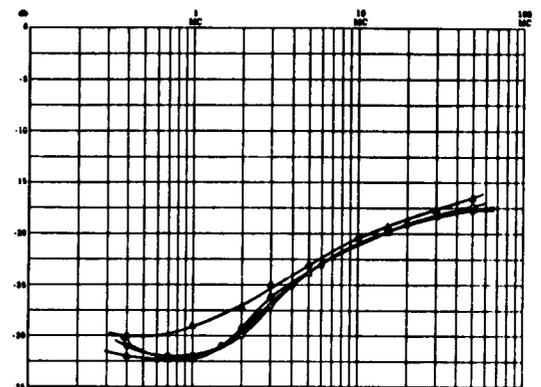
FIG. 12.   REVERSE GAIN MEASUREMENT.
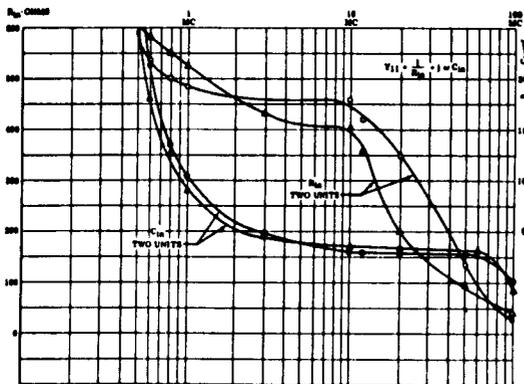
FIGURE 10.
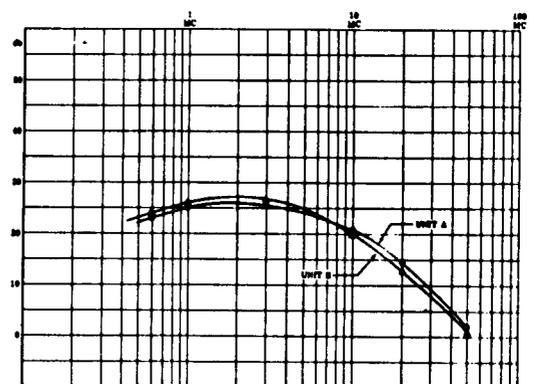
FIG. 13.   MATCHED POWER GAIN.
(One Stage.)

5.0   METHODS OF ISOLATION OF ACTIVE ELEMENTS IN INTEGRATED CIRCUITS

The semiconductor integrated circuit is based upon the technology developed for the double diffused silicon planar transistor. In the planar transistor, however, the substrate (the collector material) is common, and the collectors of these transistors are electrically connected to each other. (See Figure 1)

This type of device may constitute an integrated circuit, if properly interconnected. The darlington amplifier and the emitter follower are examples of common-collector circuitry. However, the usefulness of this type of device is quite limited.

Therefore, one basic problem in building a wide variety of integrated circuits is to achieve isolation of one transistor (or other components) from another. Once the circuit elements are isolated from each other, these elements may be interconnected in such a manner as to perform a useful circuit function. Since the transistor is the component of major interest in most integrated circuits, and since the other components (diffused resistors, junction capacitors) in the circuits are actually "portions" of transistors, the discussion will be limited to the isolation of two transistors from each other.

The isolation of one transistor from another consists of forming a region of high impedance between the collectors of the devices. (See Figure 2) One method of accomplishing the isolation of two transistors is to place two diodes back-to-back between the collectors. As long as the voltage swing from collector-to-collector is less than the breakdown voltage of these diodes, one is always operating in the reverse direction, which is a region of

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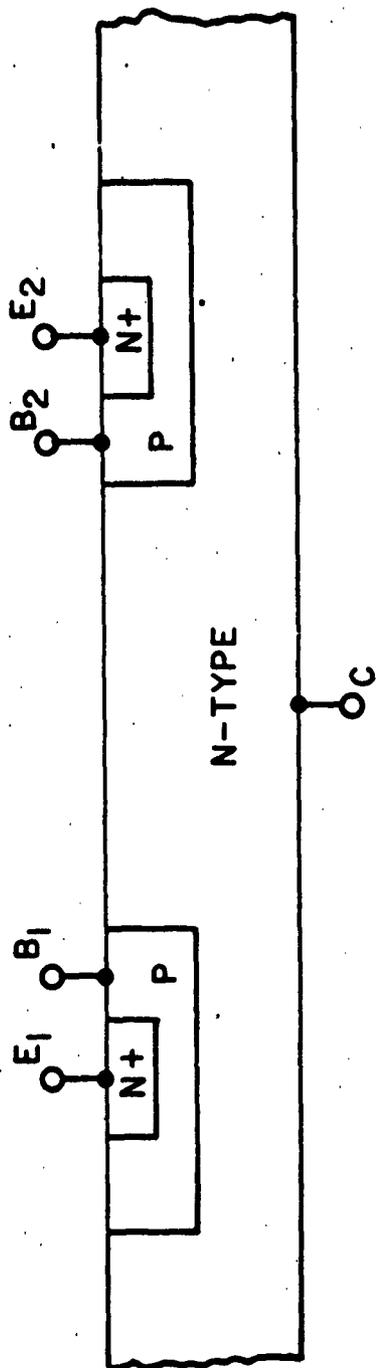
CONVENTIONAL DOUBLE-DIFFUSED PLANAR
TRANSISTOR STRUCTURE
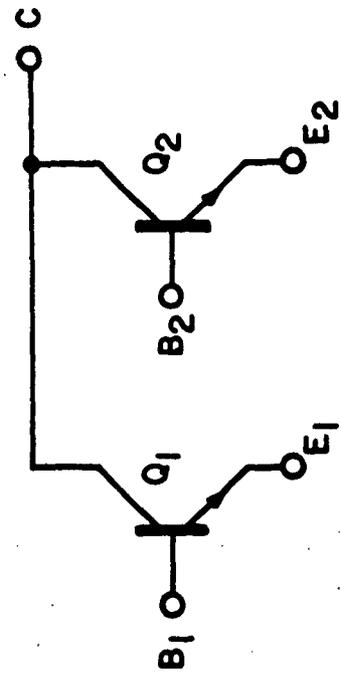
EQUIVALENT CIRCUIT

FIGURE 1

D_1, D_2 — ISOLATING DIODES
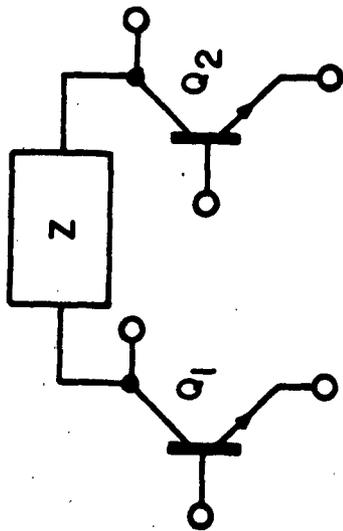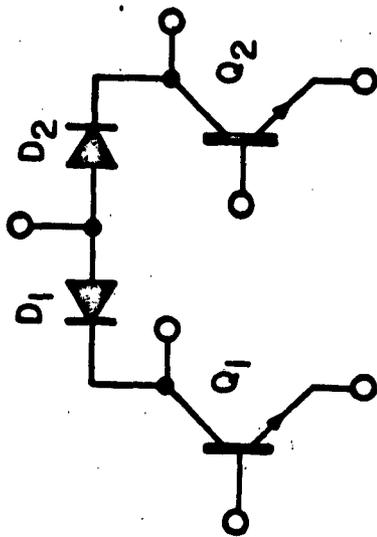
DIODE ISOLATING SCHEME

FIGURE 2

high resistance. There is a degree of high frequency interaction between devices, due to the parasitic capacitance across these diodes. However, this effect may be minimized by (1) geometry control and (2) control of the impurity distributions in the p and n regions of the diode.

There are several ways to achieve an efficient isolation structure and the section will discuss four of the most promising ones. Two methods to be discussed utilize only planar diffusion techniques, while two other methods use the epitaxial growth technique in conjunction with planar diffusion techniques.

(See Figure 3). N-type silicon with a bulk resistivity of 1.0 ohm-centimeter is polished on both sides to a thickness of 0.004". The wafer is thermally oxidized and a pattern for an isolating grid is formed by standard photoresist techniques on one side of the wafer. P-type impurities (boron) are predeposited on both sides of the wafer. A high temperature diffusion cycle is used to diffuse the two regions of p-type impurity into the wafer until the diffusion fronts meet. One side of the wafer is masked by the pattern of silicon dioxide. This masking grid forms the isolated n-type regions which are to be the collector areas of the transistors.

(See Figure 4). The silicon dioxide layer covering these n-type regions is selectively removed by standard photoresist techniques for the diffusion of the p-type base region of the transistor. A p-type base layer is diffused into the device to a depth of about 3 microns with a sheet resistance of 100 ohms/square. This provides a concentration level in the vicinity of 3×10^{18} atoms/cm^3. The diffused resistors of these integrated circuits are

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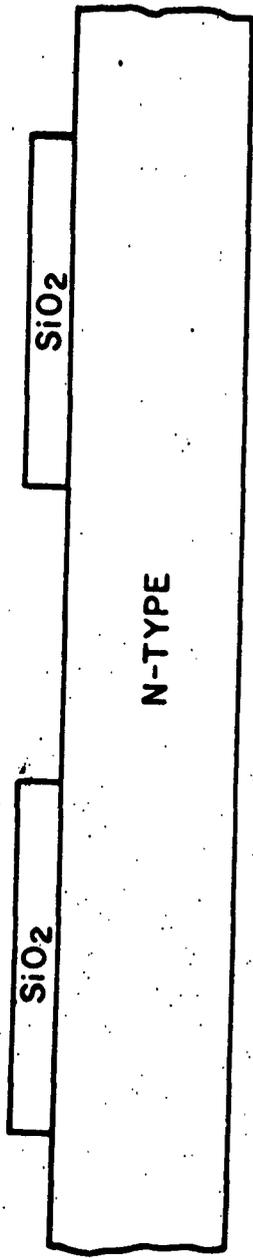
ISOLATION BY DIFFUSING FROM BOTH SIDES OF AN N-TYPE WAFER
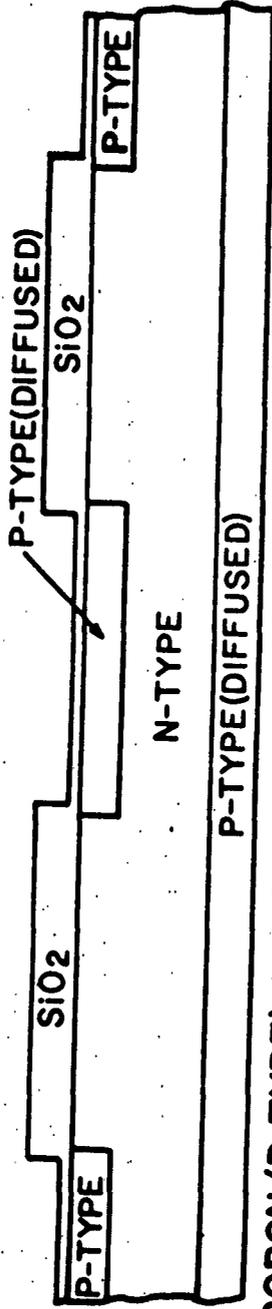
BORON (P-TYPE) LAYERS ARE PREDEPOSITED ON BOTH SIDES OF THE N-TYPE WAFER
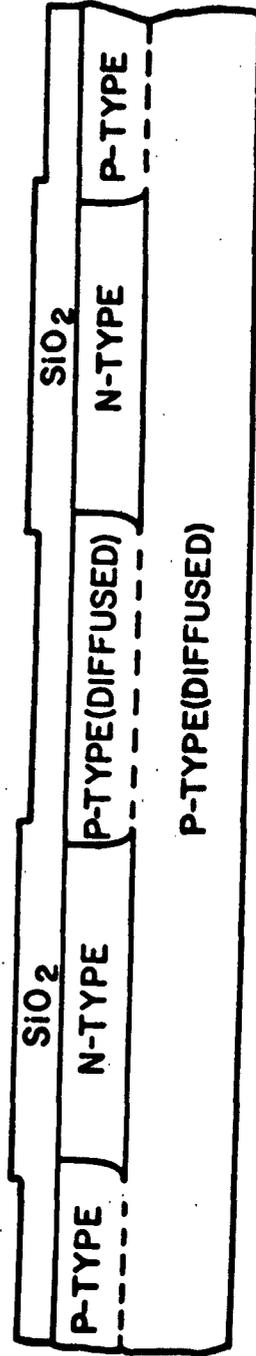
HIGH TEMPERATURE DIFFUSION COMPLETES ISOLATION OF N-TYPE MATERIAL

FIGURE 3
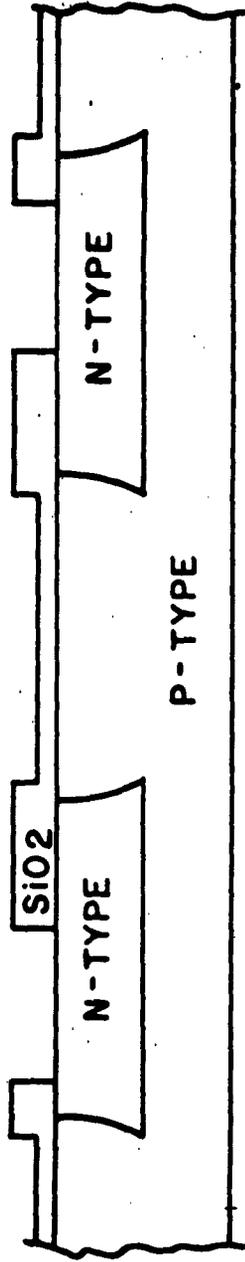
WINDOWS OPENED FOR BASE (OR RESISTOR) FORMATION
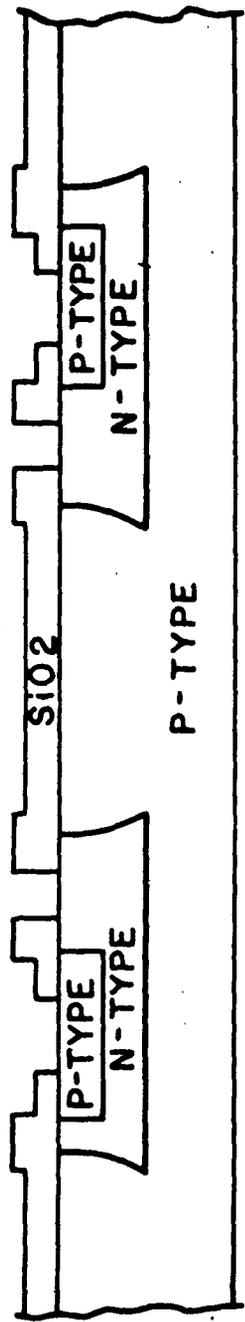
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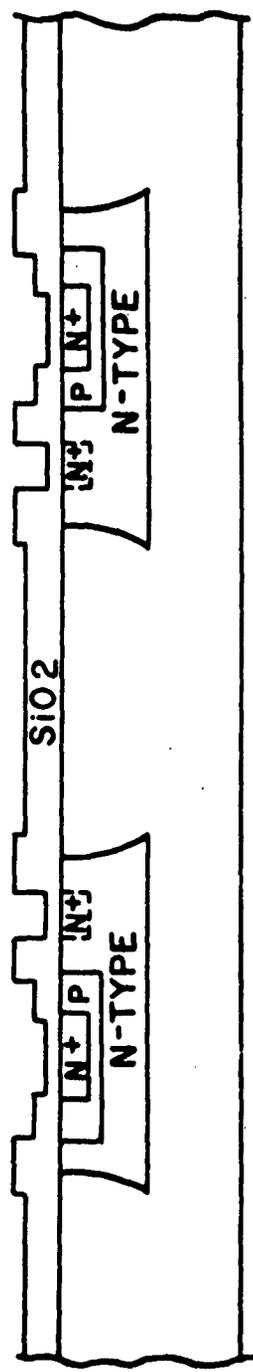
PHOSPHORUS EMITTER DIFFUSION COMPLETES JUNCTION FORMATION

FIGURE 4

formed during the diffusion of the base layer of the transistor. The temperature coefficient of these diffused resistors is dependent upon the concentration in this diffused region, in this case being about 3000 ppm/°C. This concentration level was chosen to provide a reasonable temperature coefficient of resistance and also to a proper impurity distribution for the base layer of a high frequency transistor.

Windows are then opened for the diffusion of the heavily doped emitter of the transistor, and also for the diffusion of heavily doped degenerate regions in the collector of the transistor. These degenerate regions are placed in the collector region in order to facilitate the use of aluminum as an interconnecting medium. At this point in the fabrication of the device, the junction formation is complete. Windows are selectively etched from the passivating silicon dioxide layer in those areas where the silicon is to be contacted. A film of aluminum is vacuum-deposited over the wafer and is selectively removed to form the interconnection pattern for the device.

This particular method of building integrated circuits has several limitations. (1) The sheet resistance of the collector region will be highly dependent upon the initial wafer thickness. The control over series collector resistance will be limited by the method used to establish the final wafer thickness. (2) The handling of 0.004" thick silicon wafers can present wafer breakage problems unless caution is exercised in wafer handling and processing. (3) Collector base capacitance and collector substrate capacitance, to be low, require high collector resistivity which is compromised for low series collector resistance. BV_{CBO} is also compromised.

The planar diffusion technique in conjunction with the epitaxial growth technique, provide a much more flexible system for building integrated circuits. (See Figure 5). The next method to be discussed entails isolation by diffusing p-type impurities through an n-type layer which has been epitaxially grown upon a very lightly doped p-type silicon substrate. The n-type epitaxial layer is 25 microns thick and has a resistivity of 0.5 ohm-centimeter. The wafer is thermally oxidized and a pattern for the isolating grid is formed by standard photoresist techniques. P-type impurities are pre-deposited on the n-type epitaxial layer, and a high temperature diffusion cycle is used to diffuse the p-type impurities through to the p-type substrate.

This completes the isolation of the n-type regions from each other. The base and emitter regions are diffused in a fashion similar to that which has been previously discussed. Windows are selectively etched through the passivating silicon dioxide layer over those areas on the device to be contacted. Vacuum-deposited aluminum is selectively removed to form the metal interconnection pattern.

The advantages of this system over the first method discussed are that wafers of any practical thickness may be used in the fabrication of these devices. The sheet resistance of the collector region is controlled by the epitaxial growth process. The sheet resistance of a phosphorus-doped n-type epitaxial layer may be controlled to a variation of less than $\pm 5\%$. The resistivity variation across the individual wafer is generally 5%. A shorter diffusion cycle is required, and lower collector substrate capacitance is obtained for comparable collector doping.

The formation of junctions by the epitaxial growth process entails the hydrogen reduction of ultra-pure silicon tetrachloride, and the introduction of phosphine as a doping agent during the growth of the n-on-p type layer. This technique has been discussed previously in several papers.

The third method to be discussed uses the combination of diffusion and epitaxy in a different fashion. Instead of diffusing p-type impurities through a previously grown n-type epitaxial layer, p-type impurities are diffused out from the substrate through a subsequently grown n-type epitaxial layer. (See Figure 6). In this process, the p-type starting material is thermally oxidized, and a pattern for the isolating grid is formed by standard photoresist techniques. A very heavily doped layer of p-type impurities is introduced into the wafer during a boron pre-deposition. The silicon dioxide layer covering the wafer is completely removed. (See Figure 7). An n-type epitaxial layer is then grown over the diffused p-type to the desired thickness and sheet resistance. During the growth of this n-type epitaxial layer, the diffused p-type impurities out-diffuse into the epitaxial layer. The extent of this out-diffusion is dependent upon the temperature of the wafer during the epitaxial growth, and upon the time required to grow the layer. With an epitaxial layer thickness of 25 microns, the p-type impurities do not out-diffuse to the surface of the wafer. Therefore, the wafer is subjected to a short high temperature diffusion cycle, and the p-type impurities are brought to the surface of the wafer, completing the formation of the isolated n-type regions. During this diffusion cycle, a silicon dioxide layer is thermally grown on the wafer to provide a mask for the diffusion of the base and emitter regions of the device. The completion of the junction formation and the metallic interconnection is performed in a fashion similar to that discussed previously.
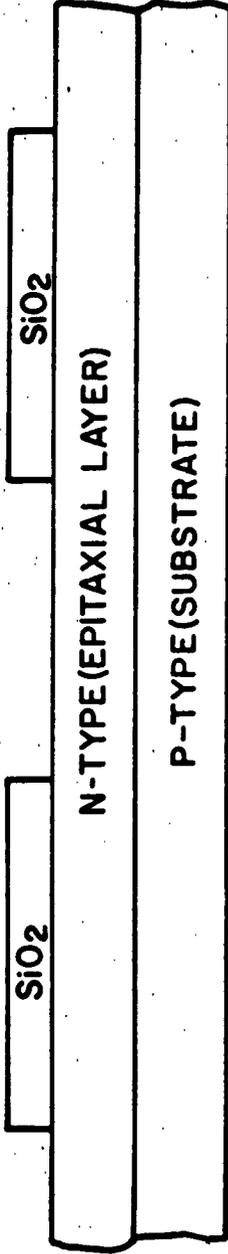
ISOLATION BY DIFFUSING FROM THE SURFACE OF AN
N-TYPE EPITAXIAL LAYER
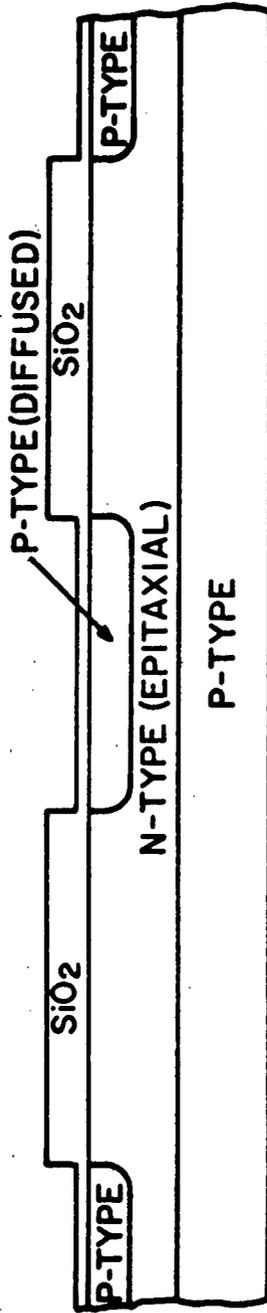
BORON (P-TYPE) LAYER IS PREDEPOSITED ON N-TYPE
EPITAXIAL LAYER
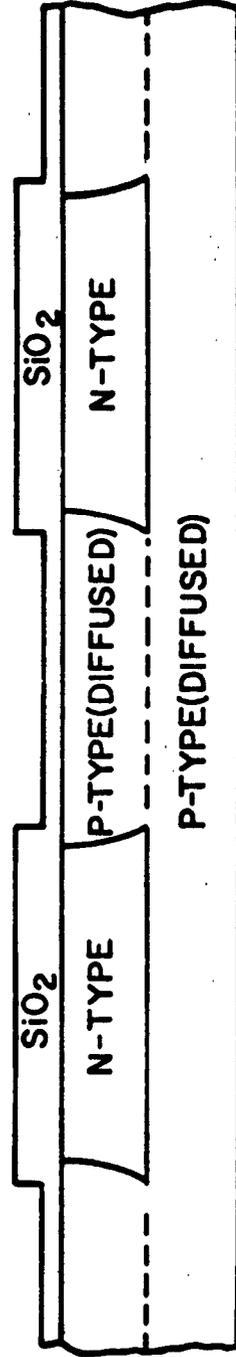
BORON (P-TYPE) IMPURITIES ARE REDISTRIBUTED THROUGH
THE N-TYPE EPITAXIAL LAYER

FIGURE 5

SiO$_2$

SiO$_2$

P
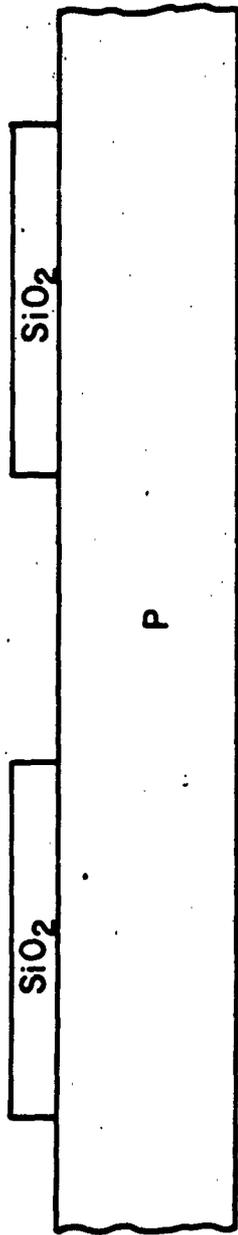
ISOLATION BY OUT DIFFUSING THROUGH AN N-TYPE EPITAXIAL LAYER

P-TYPE

P-TYPE(DIFFUSED)

P-TYPE

P
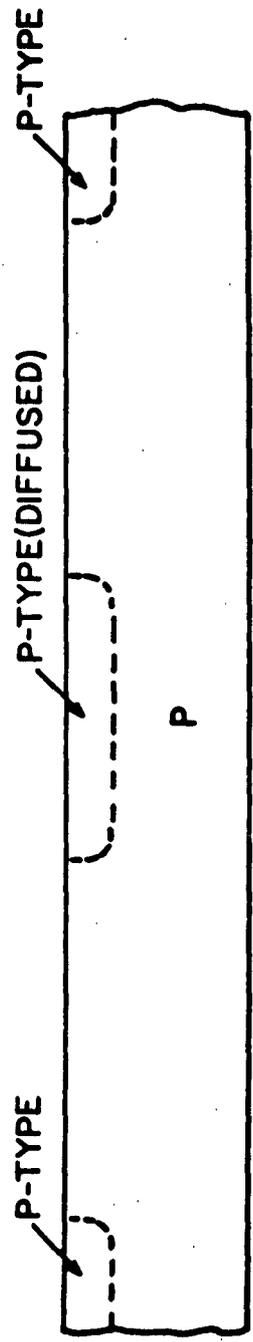
OXIDE IS REMOVED AFTER PREDEPOSITION OF HEAVY DOPED BORON LAYER

FIGURE 6
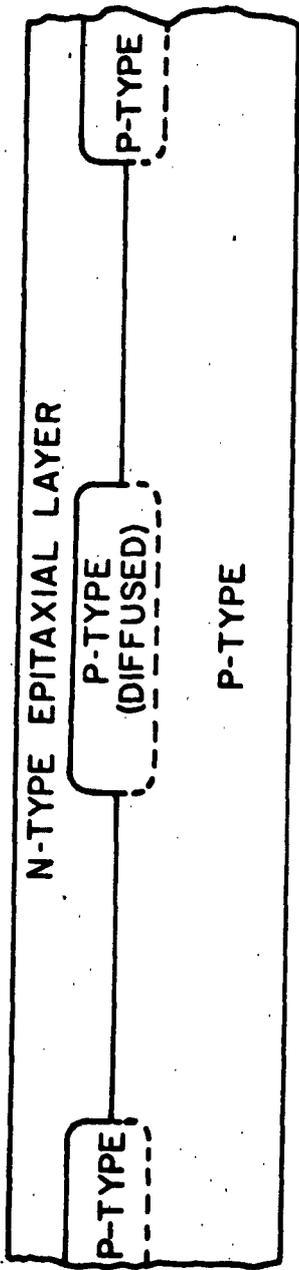
N-TYPE EPITAXIAL LAYER IS GROWN ON P-TYPE SUBSTRATE
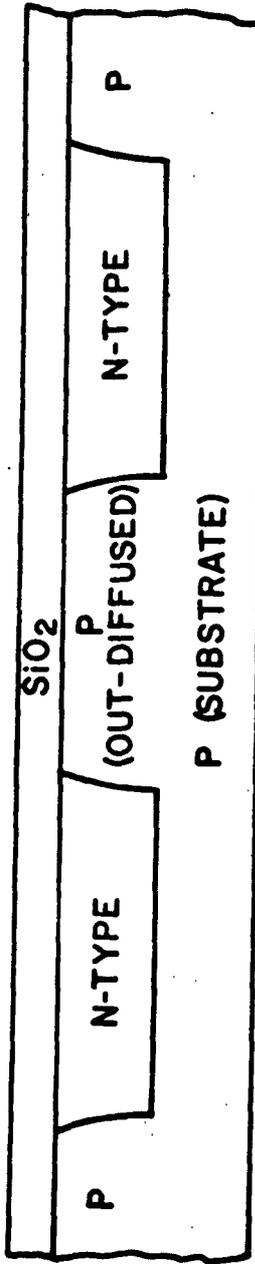
OXIDATION, OUT-DIFFUSION COMPLETES FORMATION OF ISOLATED N-TYPE REGIONS.

FIGURE 7

The pattern diffused into the substrate is reflected in the epitaxial layer and subsequent patterns may be aligned to it. However, the gas flow during epitaxial growth causes a degree of distortion, or "snowdrift" of the pattern. (See Figure 8). As a result, the geometry control which may be exercised is considerably less than that obtainable by the method employing the diffusion of impurities through the epitaxial layer to the substrate.

Once again, a shorter diffusion cycle may be used, and the epitaxial layer may be graded to reduce series collector resistance, while maintaining a low collector capacitance.

All three systems discussed up to this point have one drawback in common. The parasitic capacitance from collector-to-substrate places an upper lmit upon the high frequency performance of the device. The next system to be discussed does not use reverse-biased silicon diodes to provide the high impedance between collector regions. This system does lend itself more readily to high frequency linear circuits than to digital circuits, and its use is somewhat restricted.

In this system, the transistors are formed in the ends of a high resistivity silicon wafer. (See Figure 9). Since the impedance between collectors is formed by the resistance of a silicon bar, rather than p-n junctions, this resistive isolation scheme is essentially parasitic-free.

However, the use of high resistivity silicon as an isolating medium has one severe drawback. This isolating resistor must also act as the collector load resistor. The substrate

22
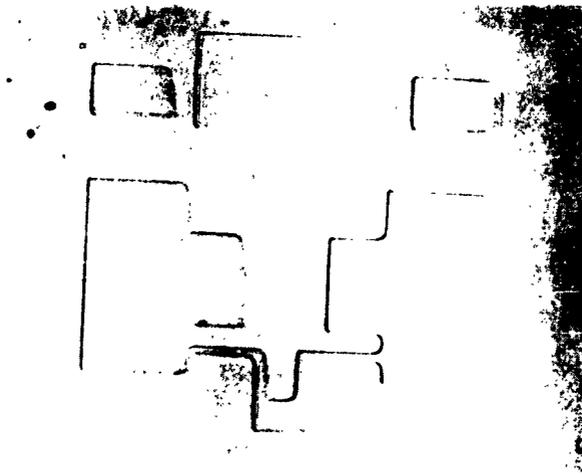
FIGURE 8

Rs—Substrate Resistor
Temperature coefficient
approximately 12,000 ppm/°C

R_D— Diffused resistor in parallel
with substrate resistance
Temperature coefficient
approximately 3,000 ppm/°C

Temperature
Compensated
Resistive
Isolation
Scheme
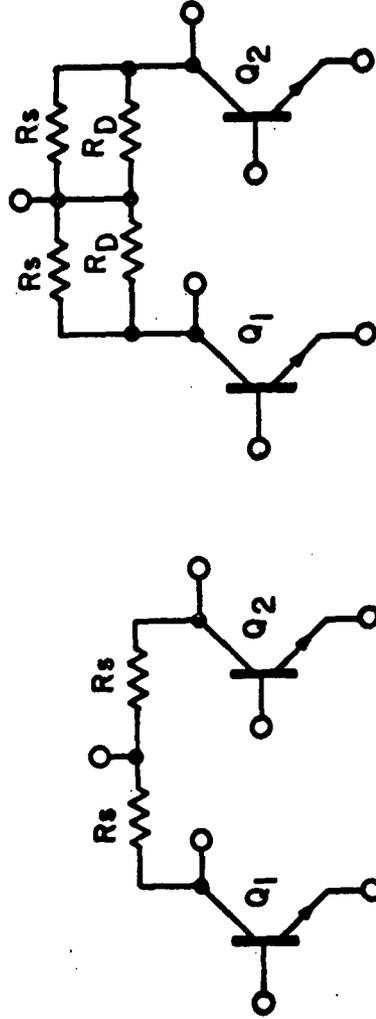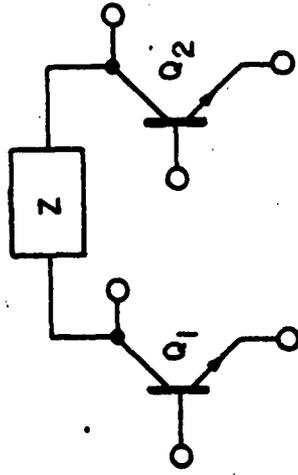
RESISTIVE ISOLATION SCHEME

FIGURE 9

resistor R_s can have a temperature coefficient of resistance in excess of 12,000 ppm/°C. The variation of this resistor with temperature places severe restrictions upon any circuit fabricated in this fashion.

However, a system has been devised so that the temperature limitations on these devices may be overcome. If the substrate resistor R_s is paralleled by a diffused resistor R_D, and if the diffused resistor has a much lower temperature coefficient of resistance, the parallel combination of R_s and R_D will yield a collector load resistor with a temperature coefficient of resistance between that of R_s and R_D. In a parallel combination of resistors, the dominant value is the lowest value. In this type of device, the diffused resistor must be designed to be as low as possible compared to the substrate resistor.

The diffused resistor presents no parasitic capacitance to the substrate. The junction is an equipotential line, since the diffused resistor and substrate resistor are a physical parallel combination.

The starting material for this type of device is very high resistivity n-type silicon (100-1000 ohm-centimeter). The high resistivity silicon is thermally oxidized and a pattern for the diffusion of low resistivity n-type collector regions are formed by standard photoresist techniques. (See Figure 10). N-type impurities (phosphorus) are pre-deposited on the wafer and diffused to a depth of 10 microns with a concentration of 8×10^{16} atoms/CM^3. These degenerate n-type regions are diffused into the wafer in order to reduce the series collector resistance.

SiO2

N-TYPE
(VERY HIGH RESISTIVITY)

TEMPERATURE-COMPENSATED RESISTIVE ISOLATION SCHEME

N-TYPE
DIFFUSED

SiO2

N-TYPE
(VERY HIGH RESISTIVITY)

N-TYPE
DIFFUSED

COLLECTOR DIFFUSED WAFER

N-TYPE
DIFFUSED

SiO2

N-TYPE

N-TYPE
DIFFUSED

N-TYPE
DIFFUSED

WINDOWS OPENED FOR BASE LAYERS AND TEMPERATURE
COMPENSATING RESISTORS
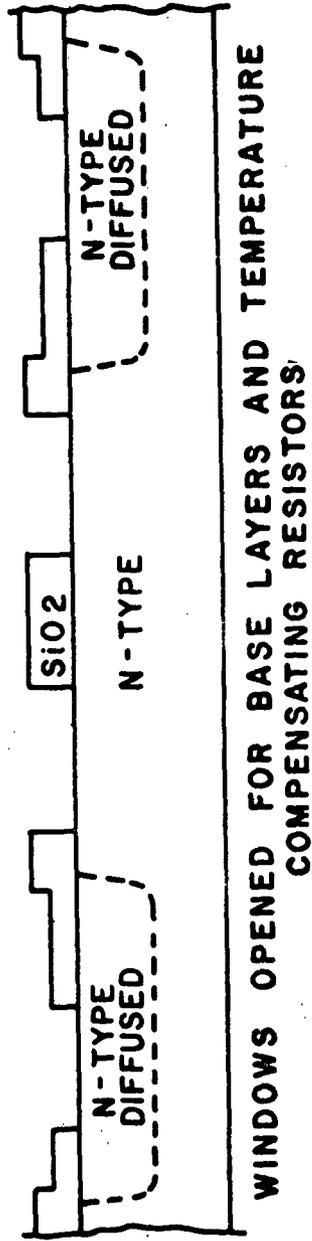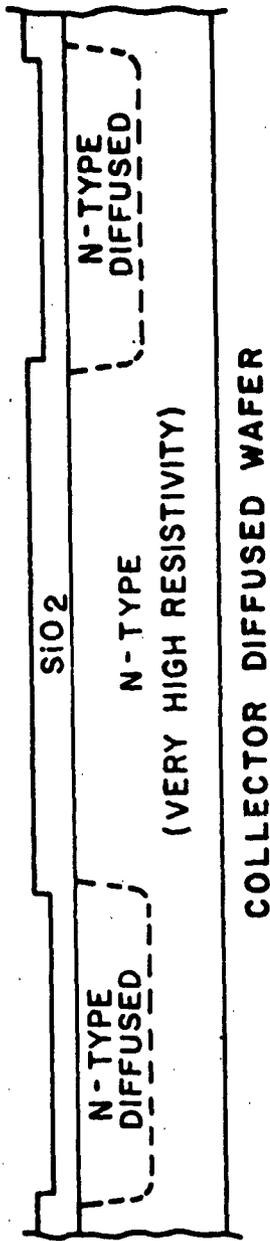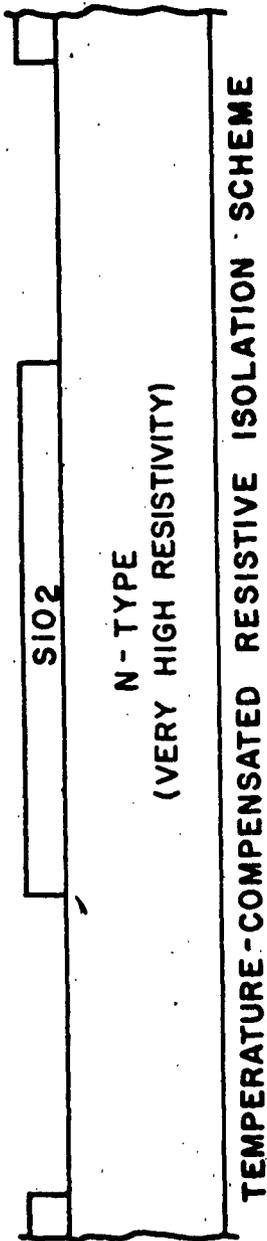
FIGURE 10

Windows are opened over the n-type diffused regions so that a p-type base region may be formed for the transistor, and simultaneously the diffused resistor R_D is formed. In a fashion similar to that previously discussed, windows are opened and phosphorus is diffused for the formation of the emitter-base junctions. (See Figure 11).

Figure 12 is a schematic of a two-stage 12 megacycle linear amplifier, Figure 13 is a photograph of a finished integrated amplifier with the aluminum interconnections. Figure 14 shows the cascaded gain versus frequency for this device.

Figure 15 is a schematic of an integrated bistable multivibrator. Figure 16 is a photograph of a completed multivibrator. Figure 17 is a schematic of an integrated three-input NAND gate, and Figure 18 is a photograph of a completed device. Both the NAND gate and the multivibrator were fabricated using technique number 2, the diffusion of p-type impurities through an n-type epitaxial layer. The other two techniques were evaluated using these two devices as test vehicles.

Each technique will form a process by which integrated circuits may be made. However, the method using diffusion of p-type impurities through an n-type epitaxial layer has been found to be the most useful in light of the following considerations.

(1) Control of series collector resistance
(2) Reduction of collector-substrate capacitance to a minimum
(3) Control of minimum device tolerances
(4) Non-rigorous isolation diffusion cycle
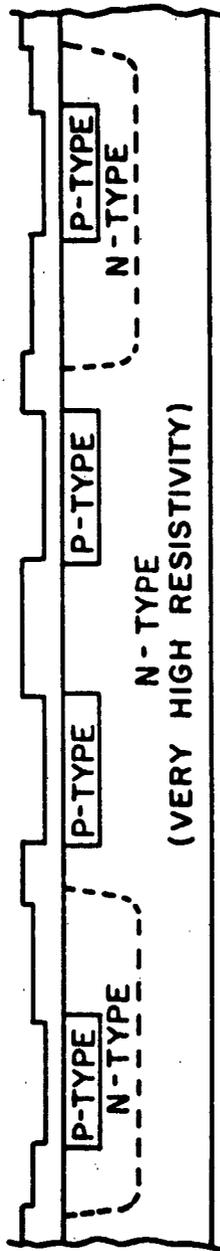
BASE AND RESISTOR DIFFUSED WAFER

P-TYPE P-TYPE P-TYPE P-TYPE

N-TYPE
(VERY HIGH RESISTIVITY)

N-TYPE   N-TYPE

EMITTER DIFFUSED WAFER

P N+ N+ P-TYPE N+ P-TYPE N+ P

N-TYPE
(VERY HIGH RESISTIVITY)

N-TYPE   N-TYPE

FIGURE 11

R2 2K
R1 5K
C1 50pf
R4 2K
R3 2.5K
C2

R2 2K
R1 5K
C1 50pf
R4 2K
R3 2.5K
C2

C2 = EMITTER BY-PASS
HYBRID 10,000pf
T1 = 2N834 EQUIVALENT

SILICON INTEGRATED CIRCUIT HIGH FREQUENCY AMPLIFIER
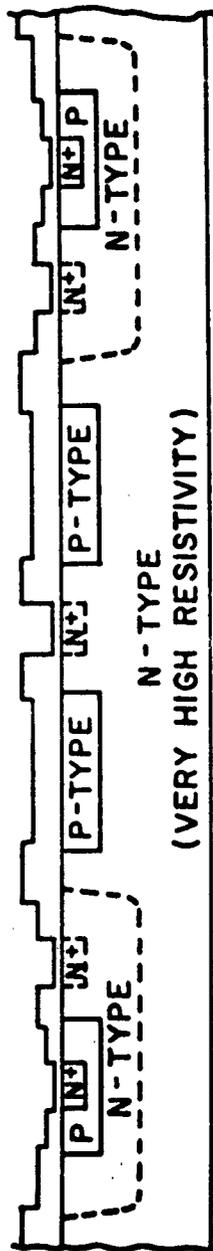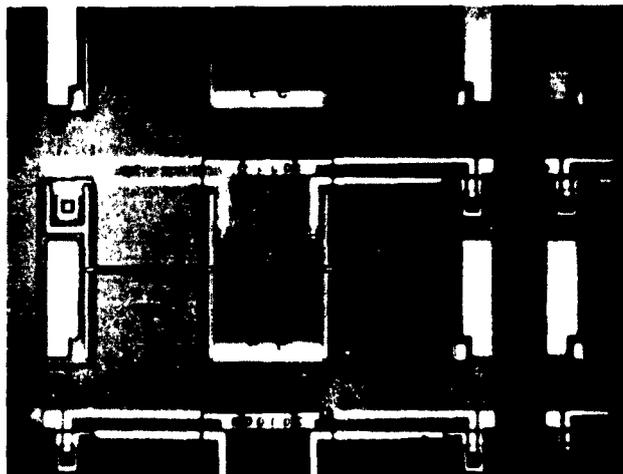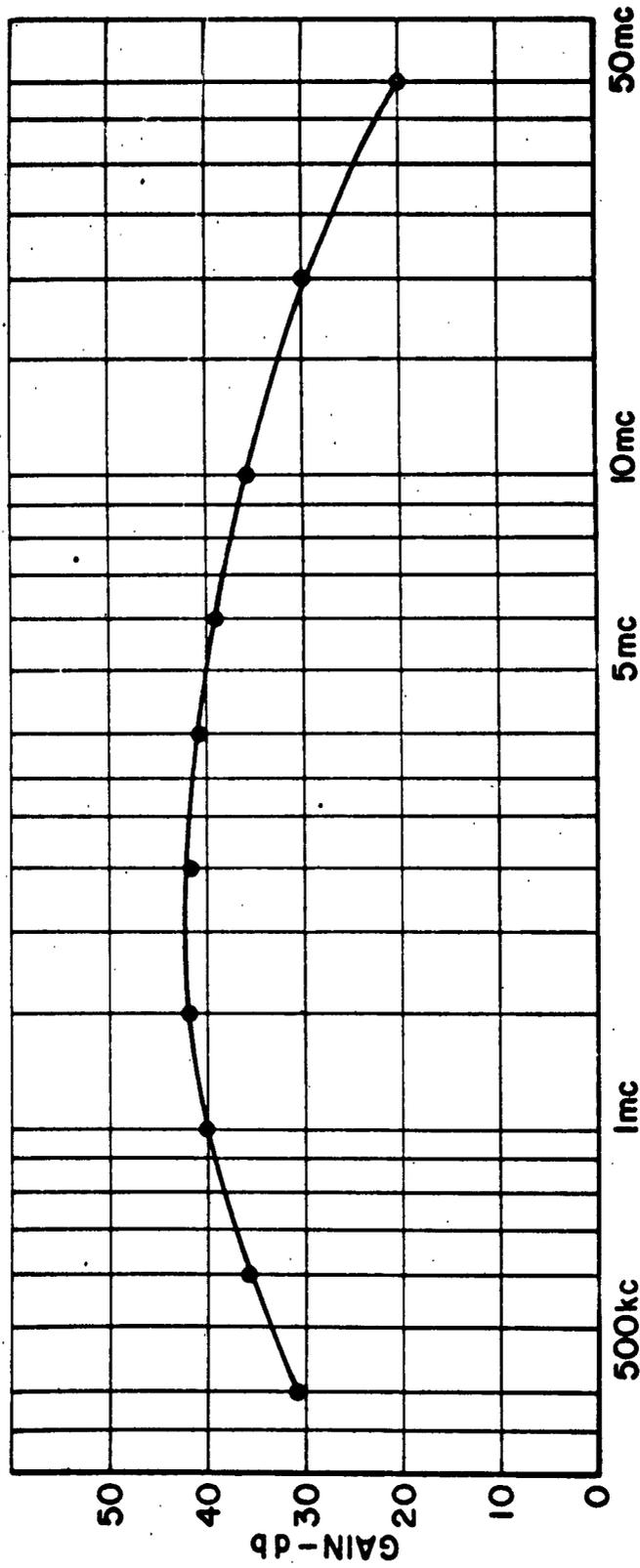
FIGURE 12

FIGURE 13

GAIN OF CASCADED STAGES OF INTEGRATED LINEAR AMPLIFIER
HYBRID CAPACITOR C_2, 10,000 pf
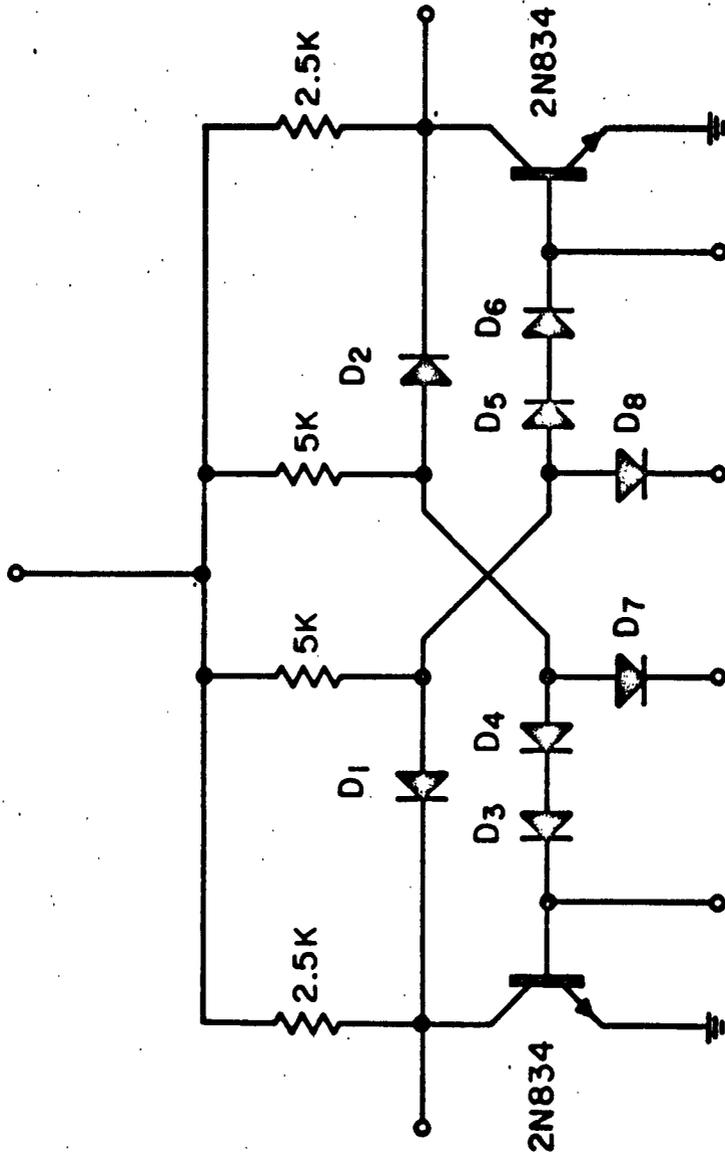
FIGURE 14

INTEGRATED FLIP FLOP

$D_1 - D_8 = 1N914$

FIGURE 15

FIGURE 16

1K

2N834

10K

D5

D4

2K

D1

D2

D3
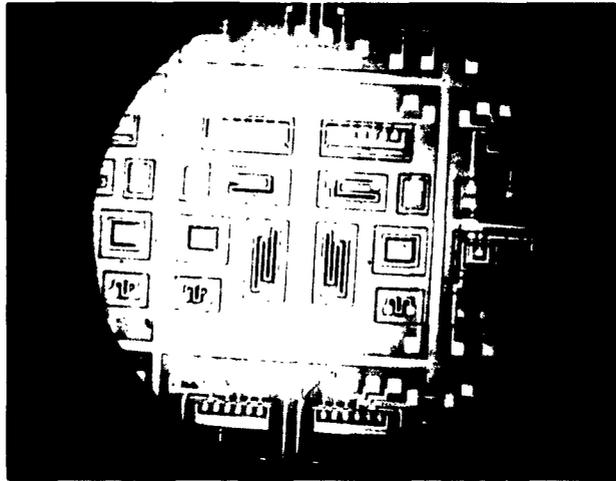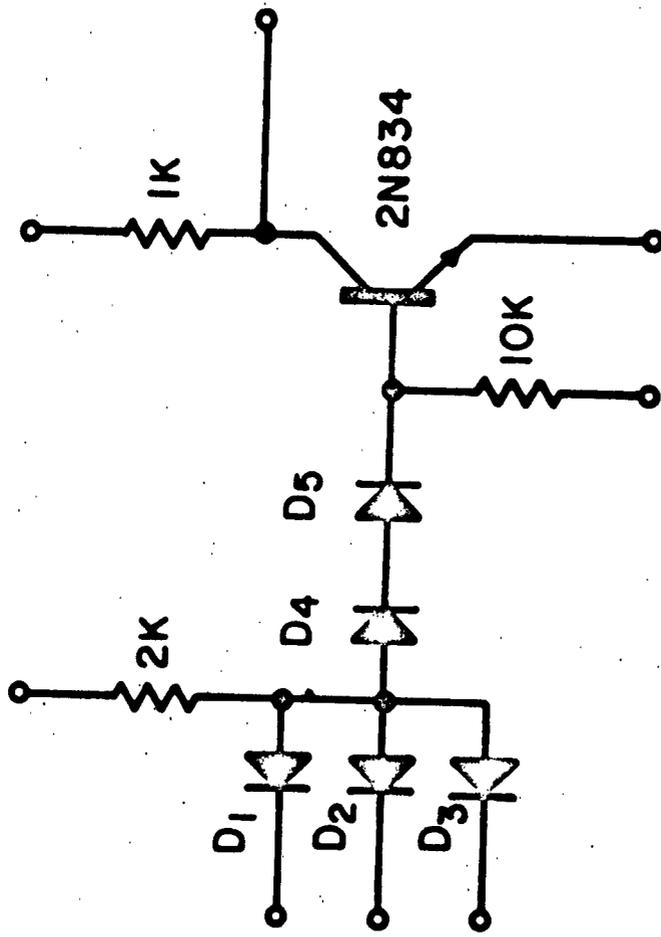
D1–D5 = 1N914

INTEGRATED NAND GATE

FIGURE 17
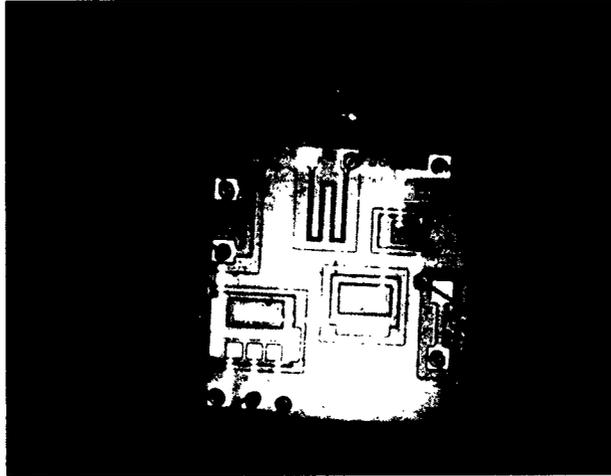
FIGURE 18
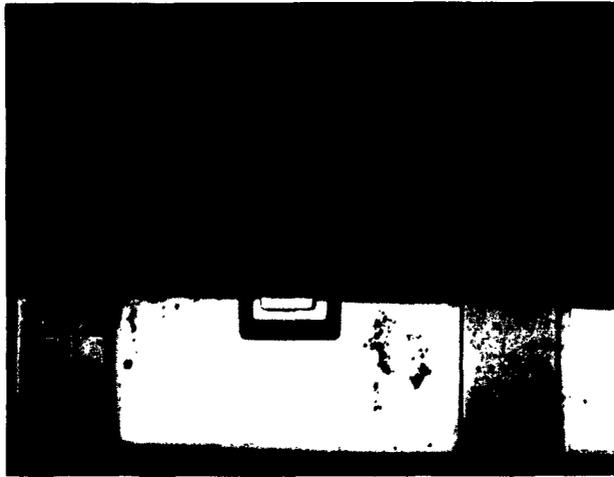
FIGURE 19

6.0   INTEGRATED DEVICES FOR HYBRID CIRCUITS

A new form of circuit construction has been developing during the past year. This method, which utilizes diffused integrated devices, may be called Hybrid Integrated Circuitry. In this technique, the individual circuit components consisting of the integrated silicon devices are all mounted on a ceramic wafer with a special metallization pattern to provide many of the interconnections and thus eliminate some of the interconnecting wire bonding. Figure 1 illustrates a typical example of this type of construction.

The following section describes these available integrated devices and their application to a hybrid operational differential amplifier. The advantages of these integrated devices for this type of application are also discussed.

6.1   Definition

A definition of integrated devices would include the following circuit elements: resistors, capacitors, diodes, zener diodes and transistors. In general, these devices are formed by the same planar, passivated diffusion techniques as the fully integrated circuits, except for the method of isolation. Devices for the hybrid circuits are physically isolated on a ceramic wafer and thus do not require the extra diffusion to produce the diode type of isolation. Thus, these integrated devices will have the same electrical characteristics as those in a fully integrated circuit without some of the parasitic effects of the substrate material. The following sections will describe some of these electrical characteristics.
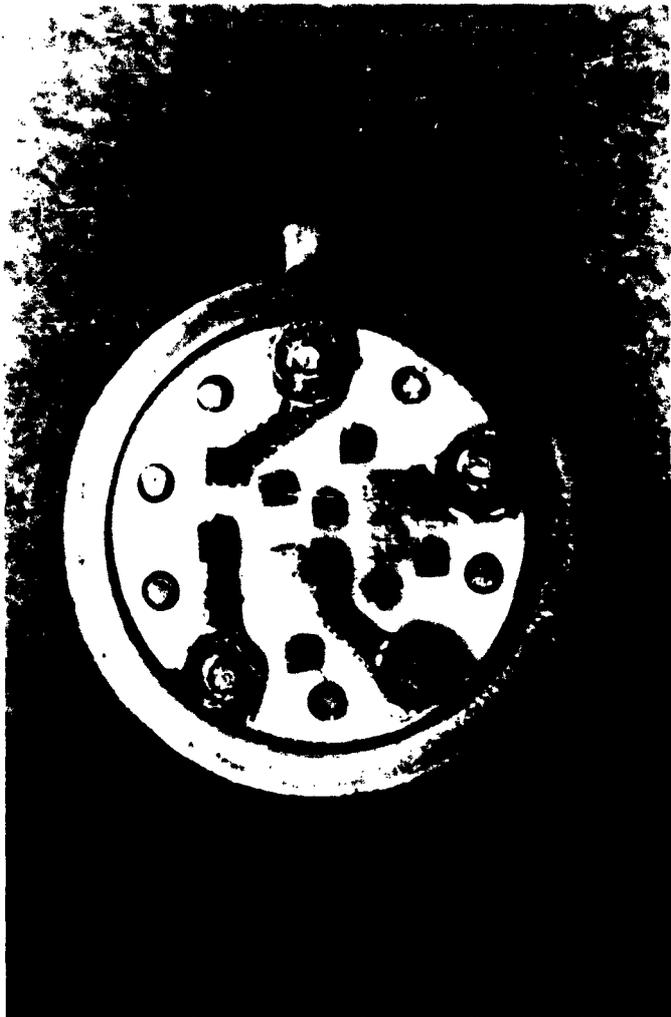
AN EXAMPLE OF HYBRID INTEGRATED
CIRCUIT CONSTRUCTION

FIGURE 1

6.2   Devices

Diffused Resistors:

In integrated circuits, the resistor probably differs
more from its conventional counterpart than the other components,
such as the diodes and transistor, thus we will go into greater
detail on this device. This type of resistor is obtained by dif-
fusing a thin layer of p-type impurity (boron) into a substrate
of n-type material. The resistance of this layer will depend on
the concentration profile of the impurity in the diffused material,
the depth of diffusion, and the length-to-width ratio of the dif-
fused area. For a uniformly doped diffused layer, the end-to-end
resistance R is given by:

$$R = \frac{\rho}{t} \frac{l}{w}$$

where

ρ = the resistivity of the material (ohm-cm)

l = length of the diffused area (cm)

w = width of the diffused area (cm)

t = depth of diffusion (cm)

With these diffused devices, the diffusion depth is
extremely small (3μ) and is relatively constant; thus, the resistance
value of the diffused area can be stated in terms of the sheet re-
sistance (R_s) of the material, measured in ohms/sq., and the l/w
ratio of the diffused area as:

$$R = \left(\frac{\rho}{t}\right)\left(\frac{l}{w}\right) = R_s \frac{l}{w}$$

Figure 2 is a cross-sectional view of an integrated resistor. The n-type substrate of .5 to 5 ohm-cm provides the physical mounting and the isolation, while the p-type layer, approximately 3 microns deep, determines the resistance value. The equivalent circuit of the resistor is shown in Figure 3. A diode and the distributed capacitance of the p-n junction is available if a contact is made to the substrate material. The reverse breakdown voltage of the diode is approximately 50 volts, while the leakage current of the junction is normally less than 10 nano amps. The value of the distributed capacitance is approximately 0.1 pf/sq. mil of diffused area. These values should be considered in the circuit application, as the maximum voltage across the resistor is limited by the reverse breakdown voltage of the diode. The distributed capacitance effect would also be a factor above 10 Mc.

The temperature coefficient is another variable which should be considered in the application of these devices to hybrid circuits. One of the most critical parameters affecting the value of the temperature coefficient is the surface impurity concentration of the diffused area. From semiconductor theory, it has been shown that in a highly concentrated p-type layer, the total resistance R is an inverse function of the hole mobility, μ_p as:

$$R = \frac{1}{q \, \mu_p \, p \, t \, w}$$

where

q = electron charge
p = hole concentration
μ_p = hole mobility

AI METALIZATION

SiO2

P-TYPE Si

N-TYPE Si
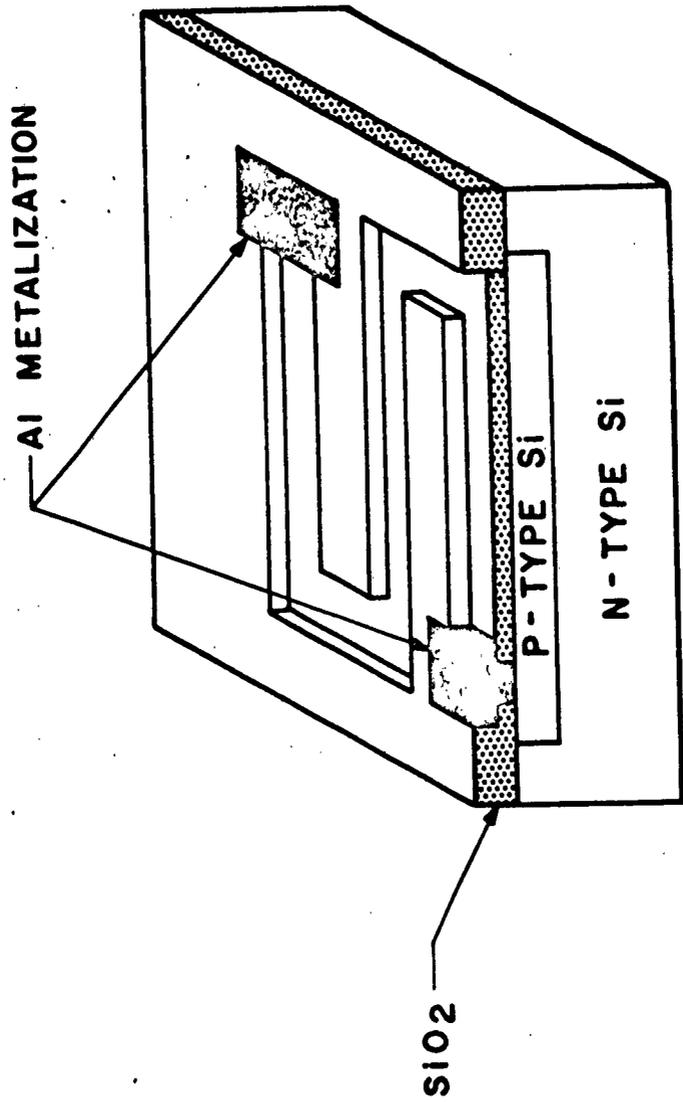
CONSTRUCTION OF A DIFFUSED RESISTOR

FIGURE 2
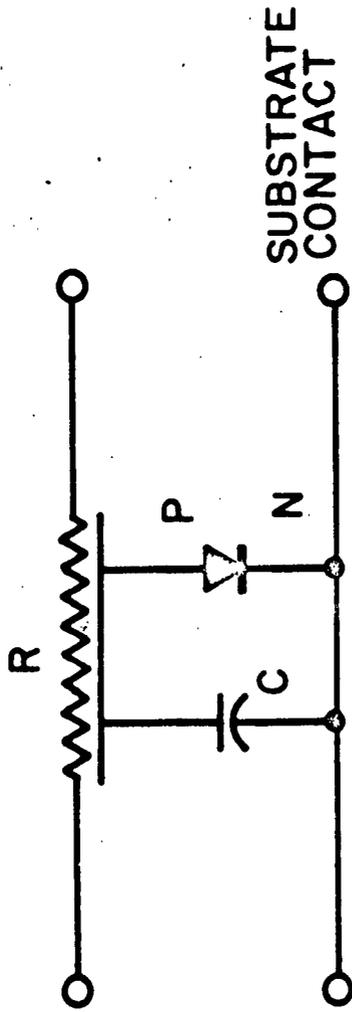
EQUIVALENT CIRCUIT OF A
DIFFUSED RESISTOR

FIGURE 3

and the remainder are as given above. Gartner shows how the
temperature variation of the hole mobility is a function of the
impurity concentration, becoming less temperature dependent with
the higher concentrations. The mobility normally decreases with
temperature, thus giving a positive temperature coefficient for
the total resistance of the unit. This effect is shown in Figure
4, where various sheet resistances are plotted as a function of
temperature. Thus, the temperature coefficient of the diffused
resistor may be controlled to a great extent by the initial surface
impurity concentrations of the diffused area.

Several designs and sizes of diffused resistors are
available for hybrid construction. Figure 5 is a microphoto of
a design to obtain the standard 20% RTMA values. The die is a
25 mil square. Other designs, which permit adjustments to within
1% during wire bonding by means of metallized taps, are available.

6.3   Capacitors

Capacitors may be formed by two different techniques:
First, by utilizing the associated capacitance of a large area p-n
junction and second, by utilizing the thin film of silicon dioxide
between the silicon substrate and the aluminum metallization.
Figure 6 is a cross-sectional view of the junction type of capacitor.
This type has the advantage of having a relatively large value of
capacitance per area (approximately 1.1 pf/sq. mil of junction area
is possible). However, the total value of capacitance is a function
of the applied reverse voltage across the junction as:

$$C = KV^{-1/3}$$

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DIFFUSED RESISTORS
(RESISTANCE AS A FUNCTION OF TEMPERATURE FOR VARIOUS RESISTIVITIES)
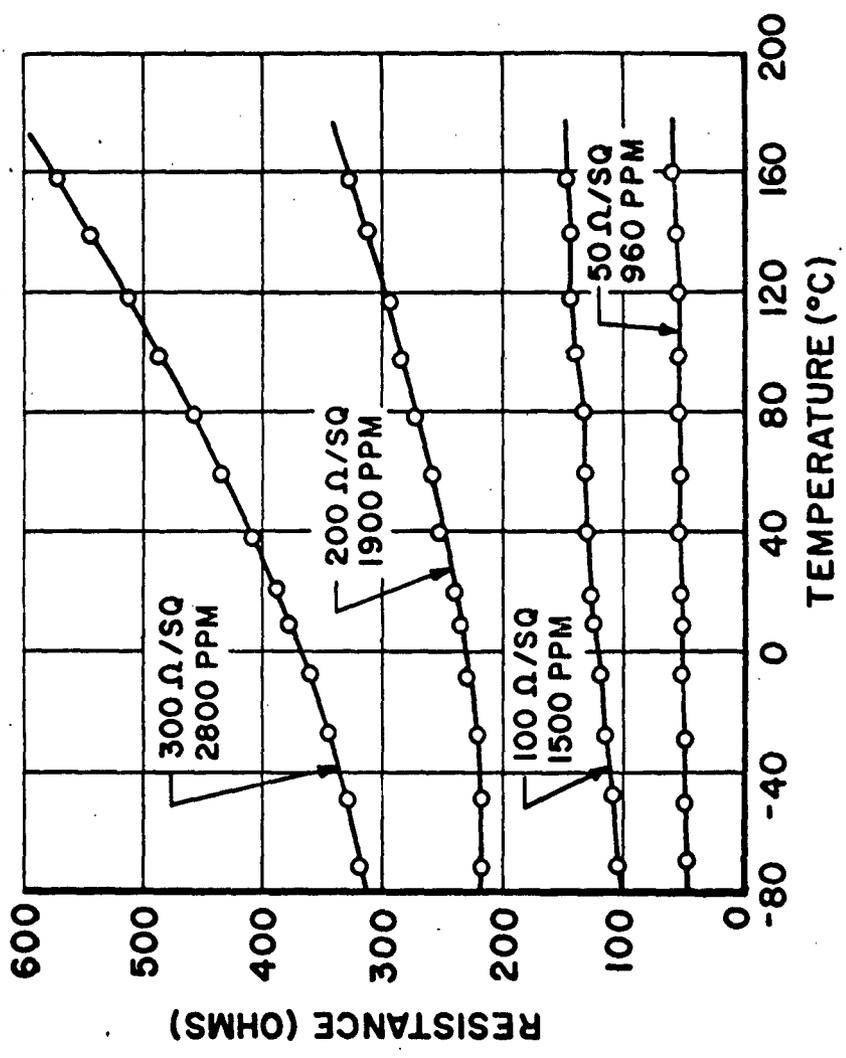
FIGURE 4
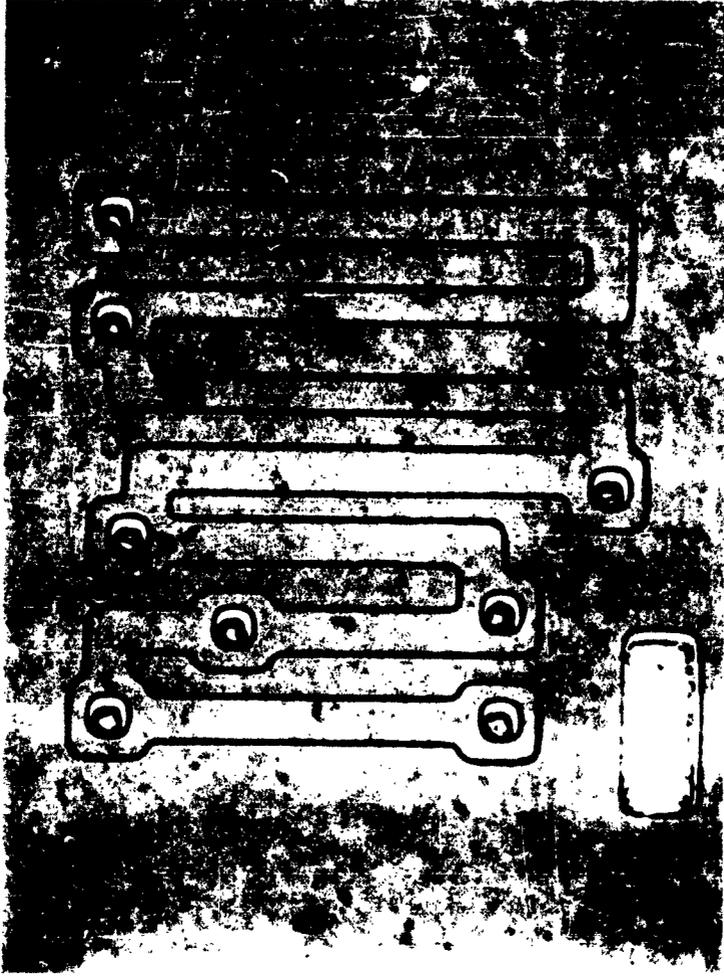
PHOTO OF AN INTEGRATED DEVICE
RESISTOR

FIGURE 5

SiO2

SiO2

AI METALIZATION

P-TYPE DIFFUSION

N-TYPE SUBSTRATE .01-.05 Ω Cm
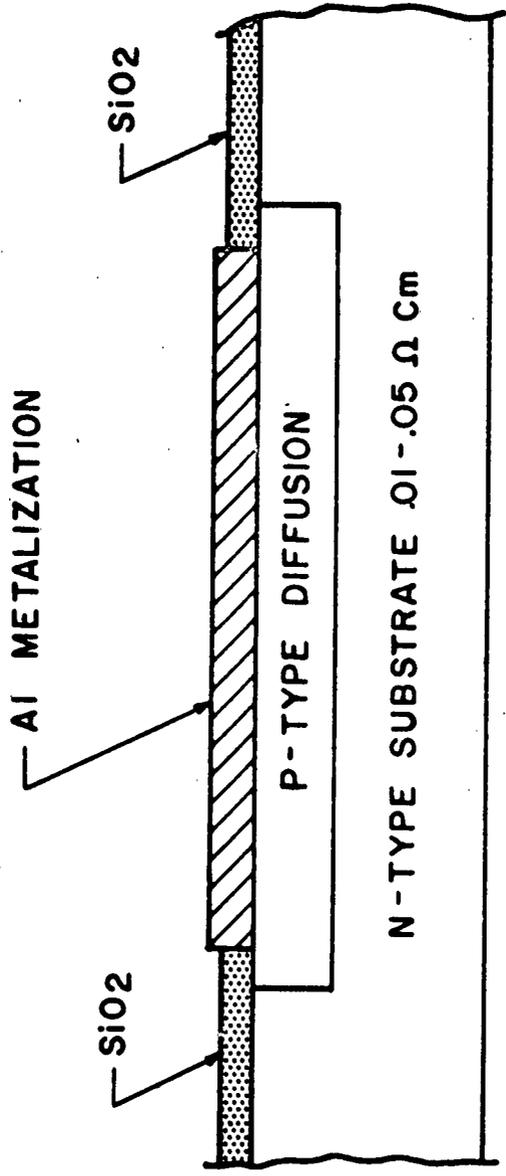
A CROSS-SECTIONAL VIEW OF
A JUNCTION TYPE CAPACITOR

FIGURE 6

These capacitors are polar and must operate under a reverse bias condition. The maximum reverse voltage ranges from 5 to 10 volts, depending on the impurity concentration of the material.

Figure 7 is a cross-sectional view of the oxide type of capacitor. The construction is such that the silicon dioxide (SiO_2) forms the dielectric between two conductors; the low resistivity substrate material and the aluminum metallization. This unit may be used as any non-polar conventional capacitor and is particularly suited for high frequency applications. Using a 500 $\overset{\circ}{A}$ oxide thickness, approximately 0.25 pf/sq. mil of metallized area is obtained. The maximum working voltage is $\pm$ 30 volts.

6.4   Diodes

In general, any commercially available silicon planar diode, including the zener type, may be used in hybrid integrated circuit construction. In addition, there is the advantage of grouping diodes in clusters of common n or common p type, with the resultant matched characteristics.

A typical diode cluster is shown in Figure 8. The reverse breakdown voltage is greater than 30 volts, while the reverse leakage current is less than 10 nano amps. Forward conduction is rated at less than 1 volt at 10 ma. The recovery time is approximately 5 nanoseconds.

APPROX. 500 Å

AI METALIZATION

10,000 Å

SiO_2

.05 Ω - Cm N OR P MATERIAL
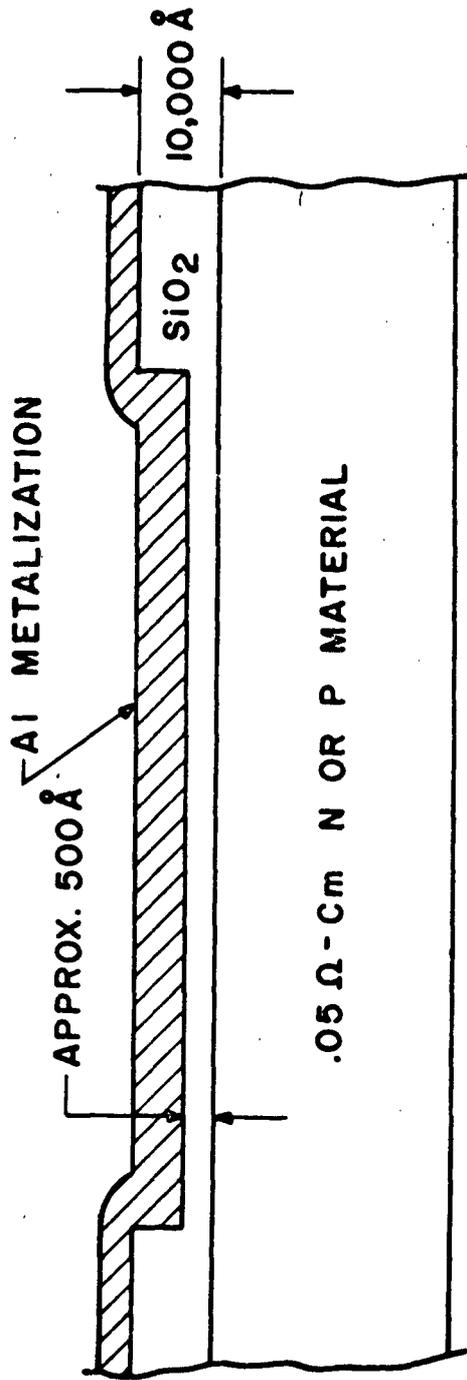
A CROSS-SECTIONAL VIEW
OF AN OXIDE TYPE CAPACITOR

FIGURE 7
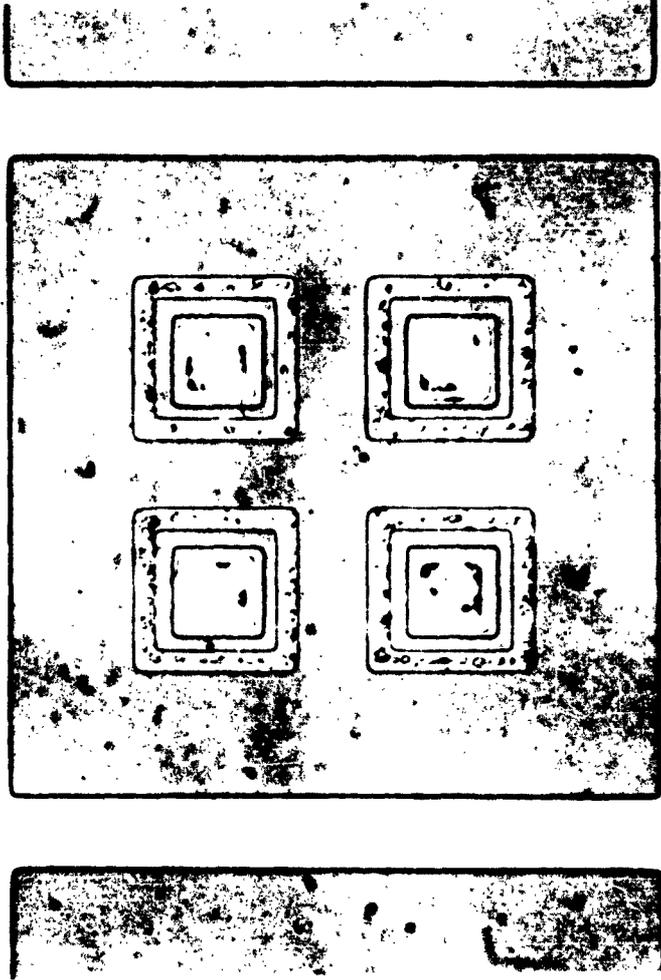
PHOTO OF INTEGRATED CIRCUIT
DIODES

FIGURE 8

6.5   Transistors

The advantages of hybrid circuit construction are apparent in the selection of transistors. As with diodes, any commercially available silicon planar transistor may be used. These units will then have the same electrical characteristics as given in the specification sheet of the conventional unit. In this way, the newest designs and techniques are available for the circuit designer.

As with diodes, transistors may be cut or scribed from the wafer in any configuration. As shown in the following section, this technique of obtaining a matched pair of transistors has a direct application in the design of differential amplifiers. Because the transistors are diffused in the same silicon crystal within a few thousands of an inch of each other, better electrical and thermal tracking will result. Figure 9 illustrates a typical unit.

6.6   Applications

An operational type dc amplifier is an excellent method of illustrating the application of integrated devices. The amplifier described in this section is of the differential, operational type, designed for amplifying signals down to a 0.1 millivolt level. The primary considerations for design of such an amplifier are:

    a.   Drift and offset components should be minimized.
    b.   High common mode rejection should be provided.
    c.   Inputs and outputs should be referenced to zero.

The other considerations are: That the unit be as small as economically feasible; that it utilize common values of supply
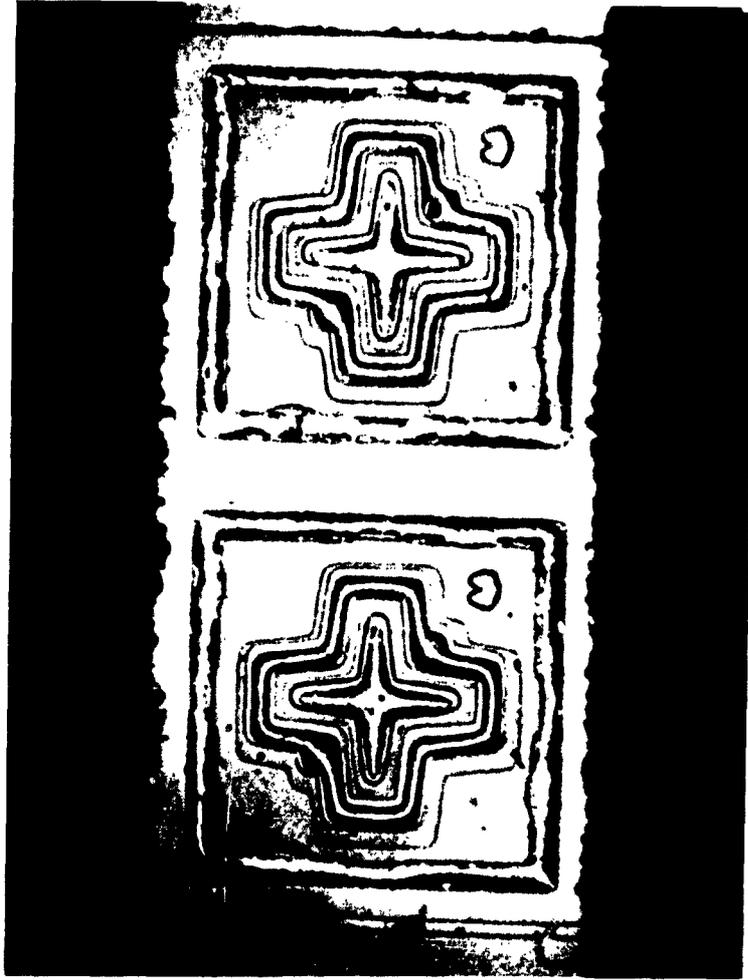
PHOTO OF A MATCHED PAIR OF
INTEGRATED DEVICE TRANSISTORS

FIGURE 9

voltage; that the power dissipation be compatible with the small
size, and that it be capable of operating over a fairly wide
temperature range. With these guidelines, an amplifier was de-
signed and fabricated in a TO-5 can using the integrated devices
described above.

Electrical Advantages of the Hybrid Approach

It has been shown that input offset, and drift of the
differential amplifier is a function of how well the input charac-
teristics of the first differential stage are matched. The hybrid
approach allows the input transistors to be taken from the same
wafer of silicon and be electrically matched for dc transconductance,
or built on one chip and sorted according to match. Either method
yields excellent temperature tracking since the two transistors are
"blood brothers", meaning the materials and diffusions are nearly
identical. Another advantage of the hybrid method is the control
of resistor values, specifically the ratios between two values.
Absolute values can be held to $\pm$ 5% and ratios can, in extreme
cases, be held to as close as 1%. Differential amplifier circuit
ratios are quite critical if low offset is desired. The collector
resistors of the first differential stage are the most critical,
which for the amplifier described are held to a ratio of 1%. The
target for maximum equivalent input offset for the design was set
at 1 mv. The other consideration of the resistors is the temperature
coefficient. The small physical size of the silicon resistor is
paid for in designing around the temperature coefficient. The temp-
erature coefficient for the silicon diffused resistors used in the
amplifier is 1000-1500 ppm/C^o. The differential amplifier approach

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reduces the sensitivity to temperature coefficient due to the dependence on the resistor ratios rather than the absolute value. Therefore, if the temperature coefficients of the two resistors are alike, the equivalent drift will be a result of the error in the tracking of the coefficient with temperature. Therefore, the resistors are either taken from the same wafer of silicon, or center tapped to provide the two resistors. Both of these methods yield excellent temperature tracking (low drift) and low dc offsets.

6.7   The Amplifier

Figure 10 is the schematic of the amplifier. The matched pair of NPN (Q_1 and Q_2) transistors are used in the input at a collector current of 0.1 ma. The low collector current was chosen as a compromise for low noise, low base current (to minimize drift due to base current) and reasonable gain. The voltage gain of the first differential stage is approximately 10. PNP planar devices in the common emitter connection (Q_3 and Q_4) were used in the second stage to provide voltage gain and dc translation to provide the output at zero dc. Emitter followers were used in the output to provide a reasonable amount of output power, and to provide high voltage gain from the PNP stage. The input characteristics of the PNP stage are also matched, but to a lesser degree than the input stage. Tests on this circuit indicate an open loop voltage gain of over 55 db at 20 kc.

Figure 11 is a photograph of the constructed amplifier. A two layer assembly technique was used on a TO-5 can to obtain the required packaging density.

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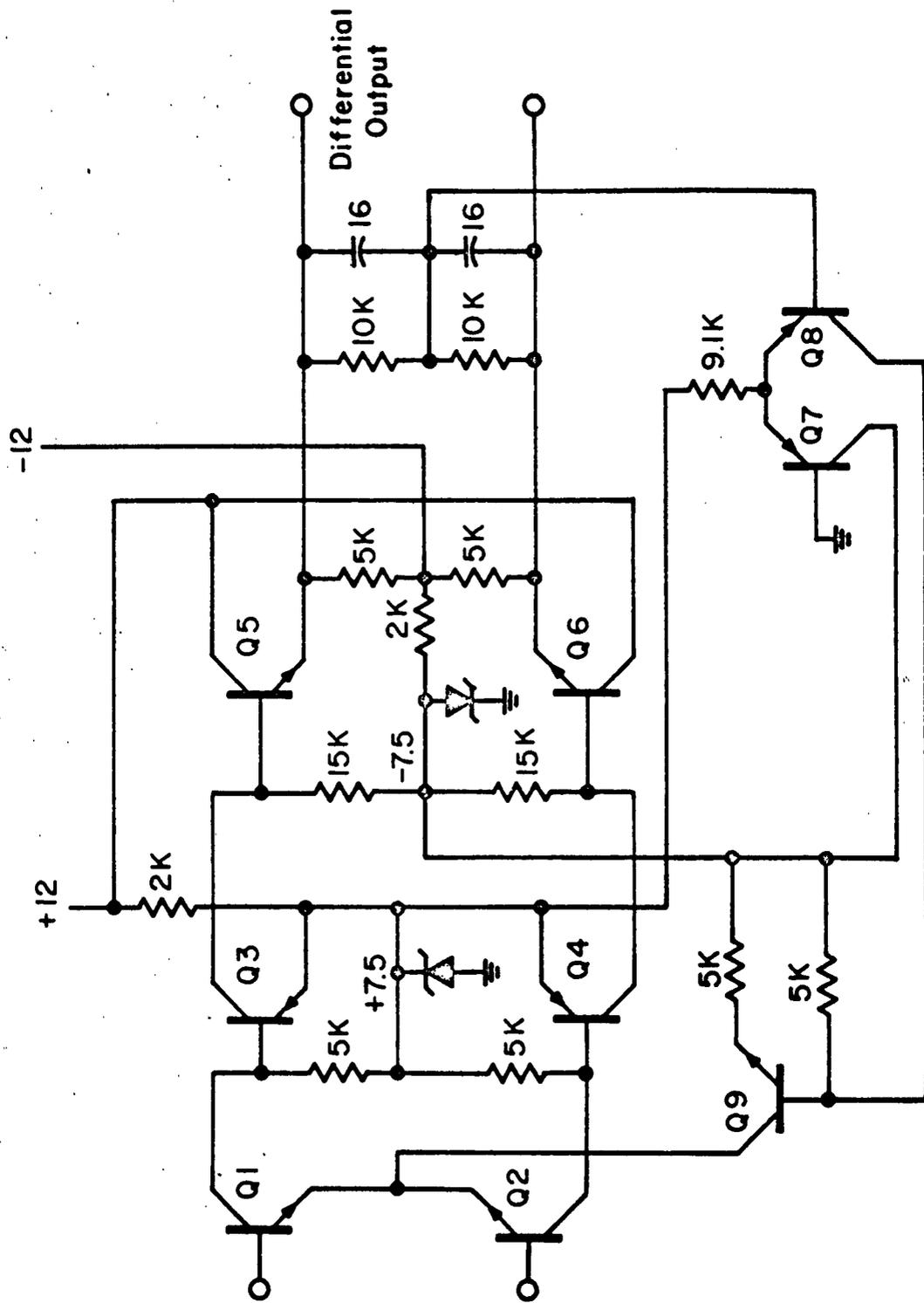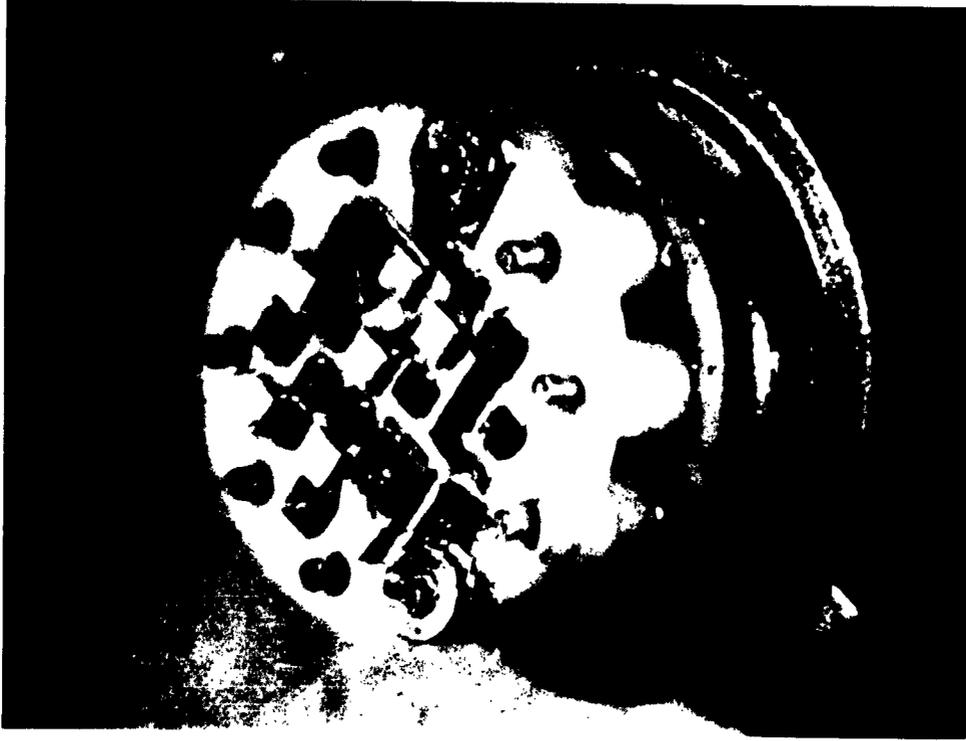
-FIGURE 10

PHOTOGRAPH OF OPERATIONAL
AMPLIFIER

FIGURE 11

6.8   <u>Summary</u>

Hybrid Integrated Devices are now available for most
standard circuit elements, except inductors. These devices have
the advantages of being physically isolated on a ceramic substrate,
thus eliminating most of the parasitic effects associated with the
fully integrated circuits. Although the characteristics of some
integrated devices differ from conventional components, these
effects may be minimized by proper circuit design as shown in this
example.

The operational amplifier constructed by this technique
retains all the performance characteristics of the conventional
circuit version with the advantages of being completely contained
in a TO-5 size package.

7.0 DIGITAL SYSTEM DESIGN

7.1 Introduction

A limited investigation of building an Integrated Circuit digital communications system is presently underway at our Western Military Electronics Center.

7.2 Summary of Work

1. The general transmission format was finalized in a manner compatible with IRIG standards and our system coding scheme.
2. The chopper switches to stabilize the isolation amplifier have been developed with Motorola Model III Field Effect Transistors.
3. The Programmer and Reed-Muller Encoder logical design is finished and construction will start as soon as hardware is available.
4. The comparator amplifier design is complete.
5. The PC art work and parts procurement necessary for system breadboard construction has started.
6. MECL circuits are being investigated for application to the system. Interfaces were considered and are being defined. A buffer has been designed to satisfy the interface between the MECL circuits and the multiplexer switches.

7.3   General

A study was made and the transmission format was modified to be compatible with our coding scheme and require a minimum amount of hardware. The transmitted frame will consist of eight words, one frame sync word, six data words and one subcommutated word. The subcommutation sequence will consist of an identity word and seven data words. If the subcommutated word is sent immediately after the sync word, there is a two word sequence every seven frames during which the isolation amplifiers may be stabilized.

Since it is possible to encode 128 discrete words and only 127 are used for the transmission of data ($\pm$ 63 and a zero indication) it is possible to send the sync word as a minus zero, if the data value of zero is sent as a plus zero. This scheme allows for a much simpler decoding circuit.

7.4   Commutator Subsystems

The design of the isolation amplifier has proceeded during this period with major effort on the development of a Field Effect Transistor input stage because of its inherently high input impedance. The decision to stabilize the amplifier against drift by periodically chopping the input and output to ground removed the severe drift requirement but gain stability input impedance and bandwidth still present a considerable problem.

The series switches and those used to chop the amplifier to ground have been designed using the Model III Field Effect Transistor.

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7.5 Programmer and Reed-Muller Encoder

The encoder input gating was modified to allow a constant frame sync and subcommutate channel identifier word.

A functional block diagram of the encoder has been derived and the implementation will start when the details of the circuit to be used are better defined.

The Encoder and programmer sections of the system have been modified to use the 2mc family of logic circuits. Several changes and redesigns were required to accommodate the delays, drive capabilities, etc. of the specific circuits.

The card layout and wiring lists for the breadboard were completed.

7.6 Binary to Binary Encoder

Information on the logic circuits to be used was received during this period. The drive capabilities, loading characteristics, operating speed, and propagation delays necessitated several changes in this unit.

Gates are specified not to be used to process clock pulses, thus, the circuitry was changed to provide processing of clock pulses only by drivers.

Loading considerations and drive capabilities were
such that the entire reset circuitry of the "basis vector"
generator outputs and programmer outputs to only the toggle
inputs of the "basis vector" generator flip-flops to accomplish
both counting and reset functions. This redesign removed one
level of logic at this point and allowed this level to be
introduced at the mod 2 adder level. This removed the necessity
of forming the function and its complement in parallel,
allowing a reduction in complexity at that point.

Following this redesign, the card layout in the rack
was accomplished, and wiring lists for the encoder were completed.
Wiring of this unit was begun.

7.6.1   Programmer

Specifications of the loading effect of the flip-flop
inputs and control points required addition of two drivers
to this unit. The clock shaper at the input to the programmer
has been built on the breadboard p.c. cards. With an input
sine wave (frequency 100 kc to 2.5 mc) the output is an inverted
clock pulse having rise time less than 40 nanoseconds from
0 V to +5.6V, fall time of less than 40 nanoseconds from
+5.6 V to 0 V, and a pulse width of approximately 150 nanoseconds.
The card layout and wiring list for this unit were completed,
and wiring has begun.

7.6.2   Binary to Binary Decoder

The design of this unit was reviewed in the light of
the logic circuit specifications. The changes required have
not yet been completed.

7.7   Breadboard

The printed circuit art work for three card types has been completed. These cards will accommodate the 2mc family of logic circuits. The fabrication of these cards is under way.

All components for constructing these circuits for the breadboard have been placed on order pending contract approval.

The wiring of the breadboard for the programmer has been completed.

A testing fixture for the digital modules has been designed and constructed.

7.8   Reference Switch

There are three switches needed to switch the input to the ladder summing network in the A to D converter. The plus 15 volt reference switch has been designed and has an on resistance of 20 to 35 ohms using 2N2219 transistors. The schematic of this switch is shown in Figure 1. The on resistance is a function of the h_{fe} of Q_1 and Q_2 with an h_{fe} of 200 required for 20 ohms. The dynamic performance of the switch at room temperature is excellent, requiring 0.3 microsec to turn on and 0.4 microsec to turn fully off.
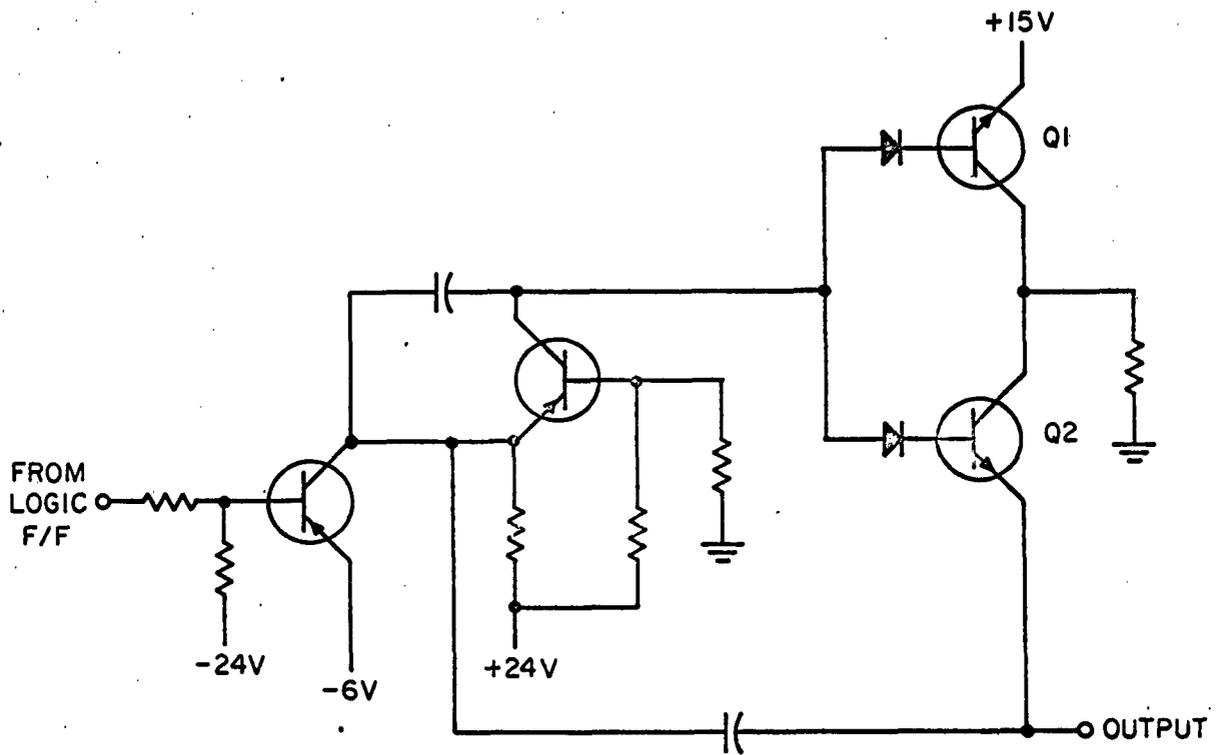
FIGURE 1

REFERENCE SWITCH

7.9   Multiplexer Switch

The multiplexer switch shown in Figure 2 is a field
effect device. This switch and its drive circuit have been
designed so that they can be fully integrated. There is no
transformer or large capacitor needed in the drive circuitry
and matching of transistor characteristics is not required.
This switch will have an off-set voltage of approximately
10 microvolts, a leakage current of 13×10^{-9} amperes and
a saturation resistance of approximately 500 ohms.

7.10   Comparator Amplifier

The comparator amplifier has been redesigned so that
the circuits are all amenable to integrated circuits. This
amplifier has a gain of approximately 1000 and a 3 db band-
width of 230 kc. The schematic of this amplifier is shown
in Figure 3.

7.11   System Design Adapted to Current Mode Logic

The Demonstration System has been modified to take
maximum advantage of the MECL digital circuits which are
being developed. The Demonstration System used DTL NAND
logic and the modification to use MECL circuits requires
the use of a buffer which translates the low voltage swings
to large volume swings for driving multiplexer and Digitizer
switching circuits.

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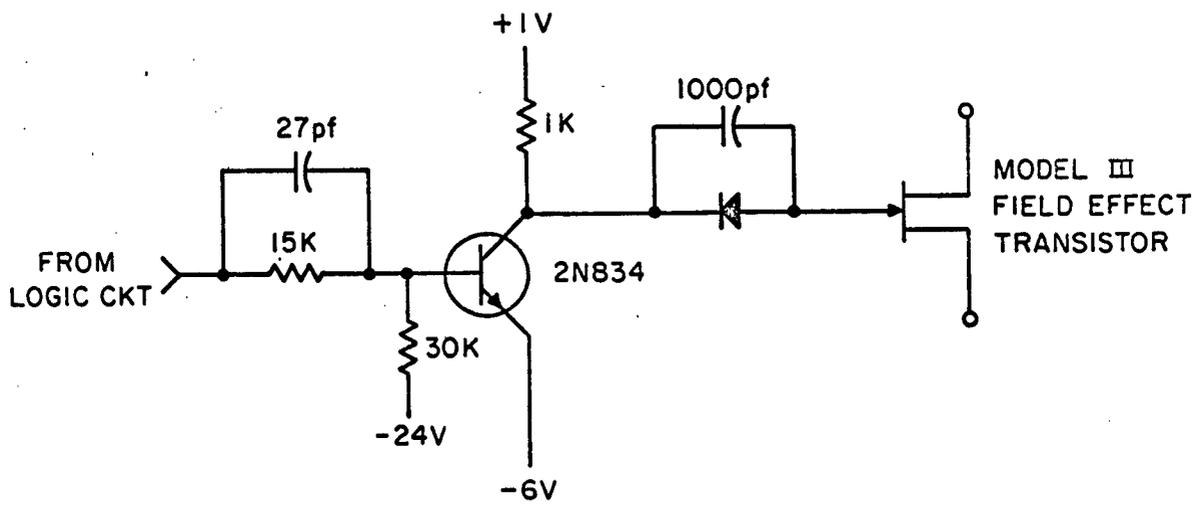
FIGURE 2

MULTIPLEXER SWITCH
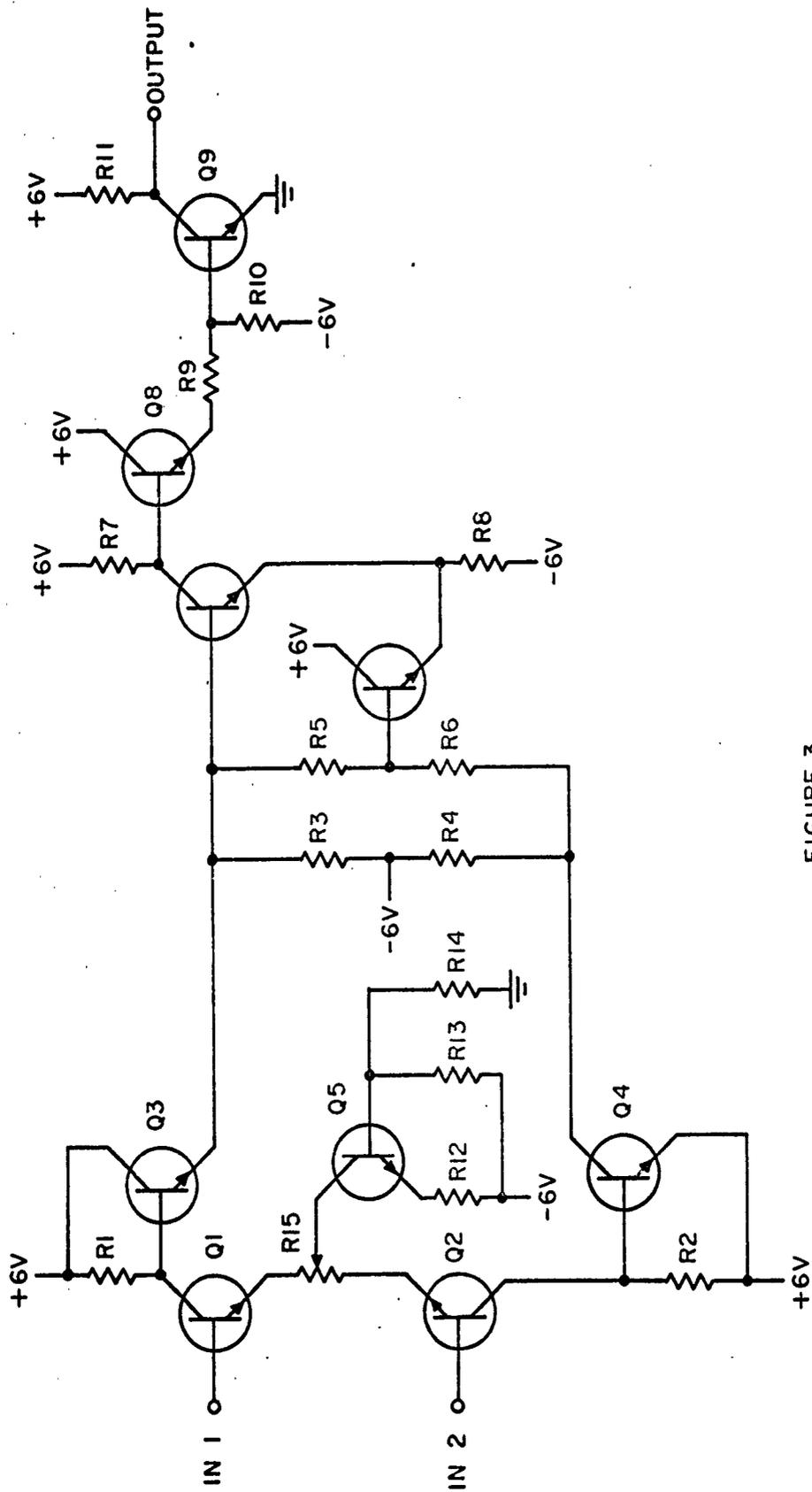
FIGURE 3

COMPARATOR AMPLIFIER

A buffer design is in progress. The paper design
illustrated in Figure 4 will be breadboarded with both
standard and chipped up integrated circuit components
to verify adequacy before final integration is attempted.

The power supply requirements are being investigated.
Only one supply voltage is necessary for the MECL circuits,
and decoupling requirements are minimized because MECL circuits
use a constant current from the power supply.

An investigation is in progress to define the clocking
capability of the MECL circuits and methods of operating
with synchronous logical techniques.

The digitizer comparator amplifier design has been
modified to simplify it and make it more amenable to inte-
gration. The design will be tested with standard and
integrated circuit components before final integration is
attempted.
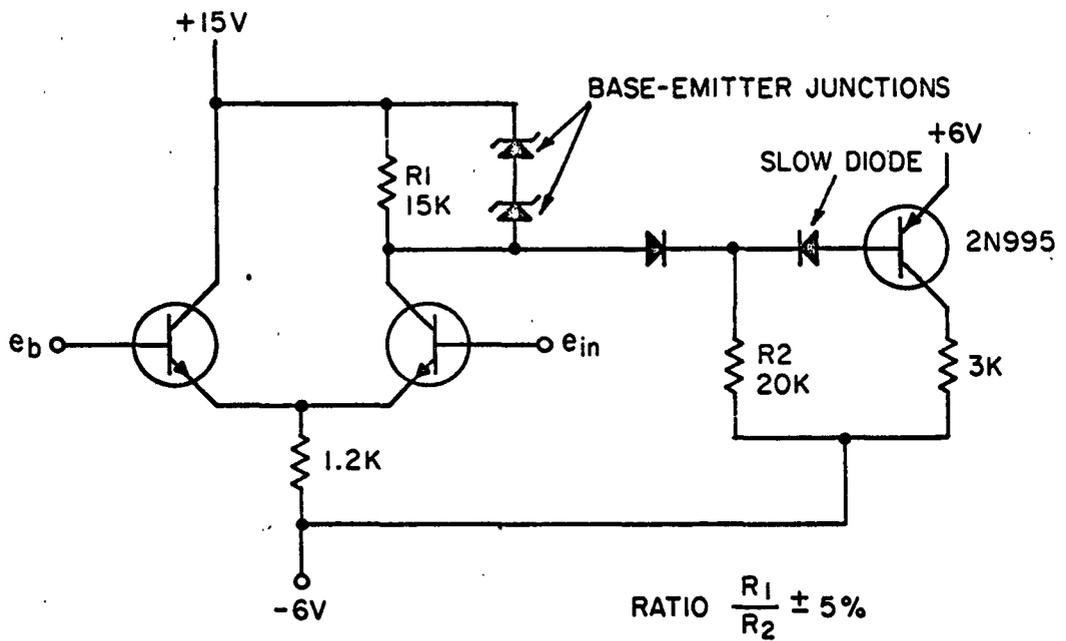
FIGURE 4
MECL BUFFER

The receiver has a sensitivity of 1-2 microvolts and the transmitter approximately 100 mW of amplitude RF modulated carrier.

8.2   General Design Considerations

The design of the transreceiver units is illustrated in the schematic diagram of Figure 1. Figure 2 and 3 illustrate the Model I transreceiver. The object of the design has been to assemble operative circuits for the entire system in discrete, complete modules.

The industry standard TO-5 transistor can with a modified 10 lead header is the basic complete circuit module. At the present state-of-the-art, it has proven possible to completely encapsulate in the TO-5 module approximately 12 circuit stages. In other circuits, parts of the circuit are encapsulated in conjunction with certain discrete components which are located externally to the TO-5 cans. These components include crystals, toroid inductors, high Q RF capacitors, trimmer capacitors, etc.

The original design of this transreceiver called for highly sophisticated crystal filter elements, in conjunction with broadband amplifiers to obtain selectivity and gain. It has proven impractical at this state-of-the-art to obtain reliable crystal filters in the small size modules required in this design. For this reason, in these two particular models, a band pass LC element has been incorporated in the 12 Mc filter position. No input filter is used.

Figure 1

FIGURE 2
Model I Transreceiver

FIGURE 3
Model I Transreceiver

8.3   The Nature of the Hybrid Integrated Circuits

The circuits integrated into the TO-5 modules are known
as hybrid integrated circuits. These consist of internally
connected semiconductor elements designed to perform the functions
of transistors, resistors, capacitors, diodes, etc. The complete
modules include the linear amplifiers in the entire 12 Mc and
455 Kc IF sections, the audio section and part of the AGC system.
Also, in the high RF sections, such as the 120 Mc input stage, the
108 Mc local oscillator and the transmitter stages, substantial
parts of the circuits are integrated, but must include certain
external elements as already enumerated. Typical hybrid integrated
circuits are mostly multi-layer constructions, in which the bottom
levels contain and connect the bypass and filter capacitors and the
top level, the transistor and resistive components. A combination
of thermocompression wire bonding and post connections completes
the entire circuit.

8.4   Transreceiver Functions

The functional two-way communication units are properly
called trans-receivers, rather than transceivers, since the former
term is more descriptive of the operative function, i.e., the
transmitter and receiver are separate assemblies. The push-to-talk
switch switches both the antenna and the power from one unit to
the other. A separate miniature dynamic microphone is used for
voice pick-up in the transmitter and a somewhat larger speaker-
type dynamic for the voice reproduction.

8.5   The Receiver Functions are as Follows:

In the receiver, a signal impressed on the antenna is

injected into the (624) tuned 120 Mc amplifier stage. A diode mixer couples this output to the 108 Mc crystal controlled local oscillator, (621). The mixture signal is amplified by the buffer stage, (631) and the 12 Mc difference component isolated by the narrow band 12 Mc filter (683).

The filter output is coupled to the two stage 12 Mc IF amplifier (631's) through a follower stage, (626).

At the output of the 12 Mc amplifier a second mixing takes place from an injected signal from the 11.545 Mc local oscillator. This is a Pierce type configuration consisting of a fundamental mode crystal and a completely integrated special purpose amplifier (625). This mixture signal is amplified in a buffer stage (631), and injected into a 455 Kc resonant ceramic filter (684). This is a commercial filter unit (Sonics Corp.) which has been remounted into a TO-5 can. This filter excludes all signals other than the 455 Kc difference signal in a very narrow pass band and accounts in a large measure for the high selectivity obtained.

This filter is followed by a two stage IF amplifier (631's). The signal is next injected into a dual diode detector circuit (622). Part of the rectified signal is coupled to the special audio amplifier stage (627) and thence to the speaker output.

Another part is further filtered to DC through an R/C section. In this filter, in the present models, standard components are used, since the built-in filters composed of resistors and zener diode capacitors were not satisfactorily operative, due to excessive diode leakage.

The DC signal developed for AGC is amplified in a Darlington stage (623) and fed back through the AGC line to all of the IF amplifier stages, as well as the 120 Mc head-end stage.

This AGC is extremely effective within a large dynamic control range. For this reason, no manual volume control is required, since the voice reproduction never becomes too loud or distorted even in close proximity between the transreceiver sets.

The maximum audio signal developed by the speaker is approximately 40 milliwatts.

8.6 The Transmitter Functions are as Follows:

The master oscillator is controlled at 120 Mc with a fifth mode crystal. This circuit is the same as the 108 Mc oscillator in the receiver section and the same (621) HIC module is used with altered external components.

This 120 Mc RF is injected into the collector-tuned modulator stage (651), and thence, into the power amplifier antenna coupling stage (652). In these models a standard 2N618 transistor is used pending further development of the (652) HIC stage.

The modulator (651) is driven by a special buffering stage (653) imparting emitter injected current modulation to the (651) stage.

The (653) is driven by the audio amplifier stage, a slightly modified (627) stage. This is directly driven by the miniature dynamic microphone, M_1.

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The maximum unmodulated carrier is approximately 100 mW and the maximum modulation is about 30 to 50% in the system as designed. The voice quality is excellent and easily understandable.

8.7   Summary of Pertinent Data on 120 Mc UHF Transreceiver Models

Physical   Weight, complete with   11 ounces
              batteries
              Dimensions of case   4 5/8" x 2 1/16" x 1 3/8"
              Length of antenna   21 inches
              extension
              External controls   Rotate button to turn on
                                           receiver. Push same
                                           button to talk.
              Volume control   None - AGC controlled

Electrical   Replacement batteries   Mallory T135R
              Battery life   Approximately 20 hours

Receiver   Battery drain, standby   20 Ma
              Battery drain, signal   22 Ma
              Sensitivity   1 u volt for threshold
                                           audible signal
              Bandwidth   35 Kc
              Frequency stability   .005%

Transmitter   Current drain, standby   40 Ma
              Current drain, signal   50 Ma
              Power output, unmodulated   100 mW
              Modulation, amplitude   30 - 50%
              Stability   .005%

FREQUENCY SELECTIVE AMPLIFICATION
FOR
INTEGRATED CIRCUITS

Co-Authors

Dr. D. J. Hamilton
J. E. Thompson

PART I
A PARTICULAR CLASS OF LUMPED ACTIVE-RC NETWORKS

I.   Introduction

A major obstacle in the development of integrated semi-
conductor communication circuits is the fabrication of devices for
frequency-selective amplification. Fundamental problems encount-
ered in the development of an inductance element per se have all
but eliminated this component from consideration in the present
state of semiconductor technology. Accordingly, methods other
than LC for obtaining frequency selectivity are sought.

From a long-range point of view, one desires new and
radically different methods which will lend themselves well to
the ultimate morphologic functional electronic block. This en-
tails major research and development effort in the areas of cir-
cuits, devices, and materials; a major breakthrough in concept,
as well as in technology, is required. From a short range point
of view one desires methods which can be immediately adapted to
the present technology of microminiaturization; this includes
both the "multiple-chip" and the "single-chip" multiple-process
approaches. It is well known that lumped RC networks in combina-
tion with active devices can produce frequency selective amplifi-
cation; a cursory examination of such networks leads one to believe
that they might be easily adapted to the presently available tech-
nology. However, while much has been done regarding the synthesis
of network functions using RC networks with negative impedance

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converters, gyrators, etc., very little has been reported regarding the fundamental limitations of RC networks with active devices.

The purpose of this paper is to examine a particular class of RC-active networks; namely, RC networks which, when combined with an ideal active device, produce a single pair of complex natural·frequencies. The topics receiving particular attention are:

(1) Maximum obtainable Z (selectivity ratio)
(2) Sensitivity to component tolerance variations
(3) Instability resulting from sensitivity
(4) Sensitivity to active device gain

The general conclusion of this study is that the tolerance requirements imposed upon both passive components and active device are so severely stringent as to make this class of networks unworthy of further consideration with any of the present technologies, or with any technologies forseeable in the future.

The paper proceeds as follows:

(1) General observations are made regarding the reciprocity of RC networks and the use of RC networks with different types of ideal active devices.

(2) Expressions are derived for the theoretical
maximum obtainable Q for RC networks with
ideal active devices.
(3) Networks are synthesized in general terms
(4) The effects of component tolerances and non-ideal
active devices are discussed.
(5) Several active device circuits are compared.
(6) Experimental results and conclusions are
presented.

II. Some General Considerations

A. The RC Network

The network configuration which is considered in this
paper consists of an RC network in parallel with an active device,
as shown below. The active device is
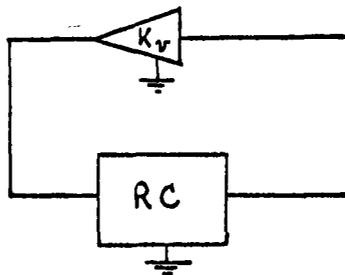
assumed to be an ideal voltage amplifier having infinite input
impedance, zero output impedance, and voltage gain Kv, which is
assumed to be real and time-invariant. It will be noted that no
input or output terminals are shown for the overall configuration;
it is assumed that these will be connected at convenient points
determined by the nature of the RC network, the driving source,

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and the load. For example, if the driving source is a current
source, it may be connected across any convenient node pair;
if it is a voltage source, it may be connected in series with any
loop.

It is easily shown that the natural frequencies of the
above system are found by solving the equation:

$$1 - K_v \left[\frac{-y_{21(p)}}{y_{22(p)}} \right] = 0$$

where the y's are the y parameters of the RC network and are
functions of the complex frequency variable p. In order to
consider systems with minimum complexity, we shall restrict the
RC network to one which produces a single pair of complex nat-
ural frequencies as solutions to the above equation. This re-
stricts the transfer function to be of the form:

$$A(p) = \frac{-y_{21}}{y_{22}} = \frac{a_o p^2 + a_1 p + a_z}{b_o p^2 + b_1 p + b_z}$$

Since the RC network is assumed to be composed of
linear passive elements, it obeys the reciprocity theorem. The
implications of reciprocity is that any RC network having a trans-
fer function which yields complex natural frequencies when used
with an ideal voltage amplifier of gain Kv will produce the same
natural frequencies when properly connected to an ideal current
amplifier with gain $K_i = K_v = K$.

Thus either of the configurations shown below may be used, provided that the RC network has the same transfer function A(p) in both cases.
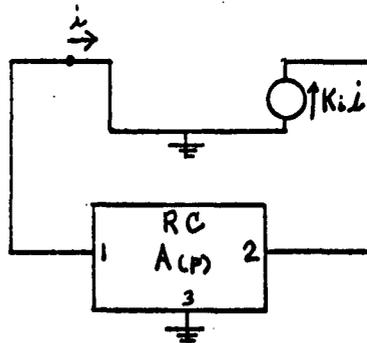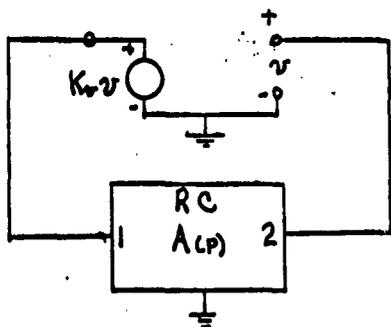
B. **Active Devices**

We next consider what properties the ideal active device, viewed as a 3-terminal network, exhibits when we re-define the terminal connections. The ideal voltage amplifier with gain Kv is characterized as follows:
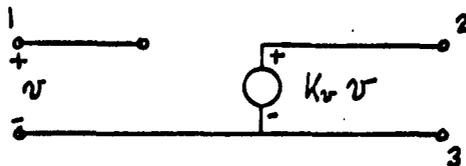
$(v_2 - v_3) = Kv(v_1 - v_3) = Kv(v_1 - v_2 - v_3 + v_2)$ when the v_i is the voltage at the $\underline{ith}$ terminal relative to some common reference point.

Suppose we interchange terminals 2 and 3 as shown below, and redefine the gain as $K_v' /$
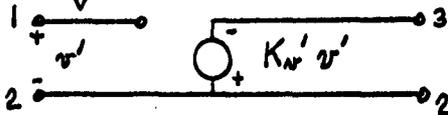
From the above equation we have:

$$(v_2 - v_3) = K_v(v_1 - v_2) - K_v(v_3 - v_2) \quad \text{or}$$

$$\frac{v_3 - v_2}{v_1 - v_2} = \frac{-K_v}{1 - K_v}$$

But $v_1 - v_2 = v'$ and $v_3 - v_2 = -K^o{}_v v'$

Thus we have:

$$K_v' = \frac{K_v}{1 - K_v}$$

Similarly, we may redefine the terminals of the ideal current amplifier as shown below, and it is easily shown that $K_i' = \frac{K_i}{1 - K_i}$.
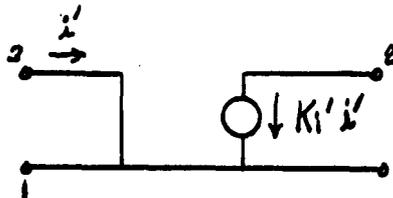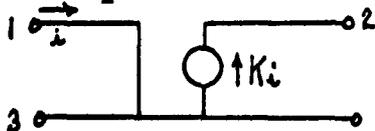
By considering these results, together with the reciprocity of passive RC networks, we note that if an RC network can be found which produces the desired natural frequencies when

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combined with one of the four active devices below, then the
same network may be used with any of them to produce the same
natural frequencies.
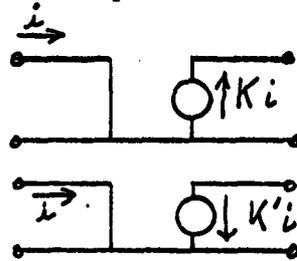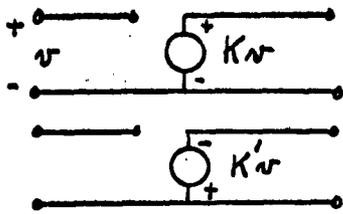
$$K' = \frac{K}{1-K}$$

As an example, we consider the so-called Wein-bridge
configuration shown below. This circuit
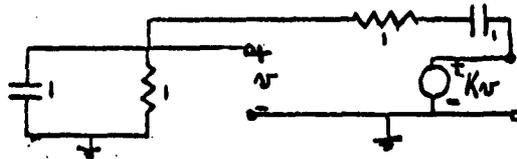
exhibits a pair of imaginary natural frequencies at $p = \pm j$ when
the active device gain is K=3. By making use of the above re-
sults, we can find four configurations for the Wein-bridge circuit:

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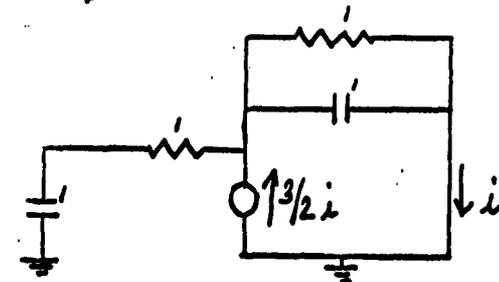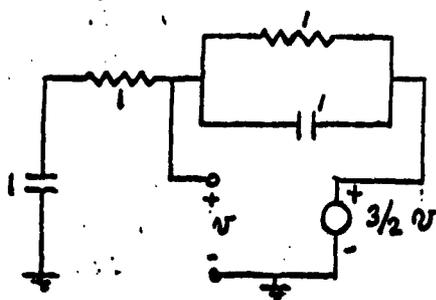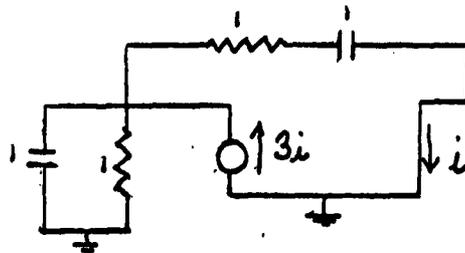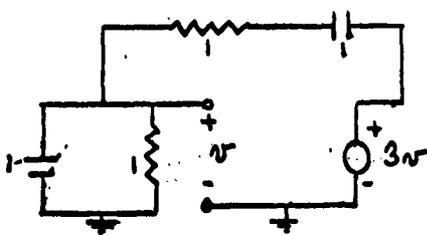
It is interesting to note that if the critical gain, i.e., the gain required to produce inifinite Q, is greater than unity, the active device is always non-inverting.

These results are quite important practically because certain of the active device configurations are more easily realized than others in terms of bias considerations. For example, it is more convenient to bias a single transistor for small-signal common base operation than for common emitter operation.

For practical reasons, we shall impose a further restriction on the RC-active system: no critical gain other than unity is permitted. By using two transistors in a feedback configuration, it is possible to construct an amplifier which closely approximates the ideal active device, and in which the gain approaches unity with only minor dependence upon transistor parameters and bias resistors. However, if a gain other than unity is required, it is necessary to fix the gain by the ratio of passive components such as resistors. Since these passive components exhibit tolerance variations, the gain of the amplifier is also subject to variation. Furthermore, the input and output characteristics of the amplifier become less ideal as the gain departs from unity. The two small-signal circuits shown below are both feedback circuits designed to approximate the ideal voltage amplifier.

(a)   (b)

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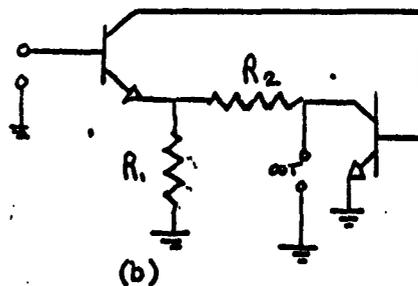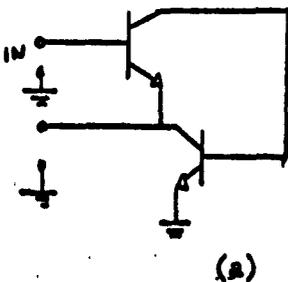
Circuit (a) has an open-circuit voltage gain of unity, while the gain of circuit (b) is $1 + \frac{R_2}{R_1}$. In the latter case the gain is seen to vary directly with the resistors, while the input and output impedances are also functions of the resistors.

Since it is difficult to maintain close tolerances in integrated circuits, it is thus essential that the active device parameters be as free as possible from susceptance to tolerance variations; hence, the restriction of critical gain to the value unity. It is to be noted in passing that a system which exhibits unity critical gain also has critical gain infinity if the terminals are redefined.

C. Summary

In this section, we have discussed the general RC-active network problem with the following restrictions and results:

(1) The system configuration consists of a three terminal linear RC network connected in parallel with a three terminal active device.

(2) The transfer function of the network is assumed to be the ratio of two polynomials of degree no greater than 2.

(3) No systems requiring critical gains other than unity (or infinity) are to be considered.

(4) If a system can be found which meets the above
restrictions, then by making use of reciprocity
and by redefining terminals, the RC network
may be used with four connections of ideal active
devices to produce the same natural frequencies.

III.   Theoretical Considerations

In this section we examine the form of the general
RC transfer function and obtain an expression for the Q of the
RC-active system in terms of the RC transfer function and the
amplifier gain. All possible transfer functions for the RC
network being considered are then examined and the Q calculated
for each. Finally, the equivalence of certain cases is demon-
strated.

A. RC Transfer Functions and Q

We postulate the transfer function of the RC network
as $A(p) = C \dfrac{N}{D} = \dfrac{C(p^n + A_1 p^{n-1} + A_2 p^{n-2} + \ldots + A_n)}{p^m + B_1 p^{m-1} + B_2 p^{m-2} + \ldots + B_m} = \dfrac{-y_{21}}{y_{22}}$

$$= \frac{a_0 p^n + a_1 p^{n-1} + \ldots + a_n}{b_0 p^m + b_1 p^{m-1} + \ldots + b_m}$$

Fialkow and Gerst have shown[1] that the necessary and sufficient
conditions that A(p) be the transfer function of an RC network are:

_____

1. A. Fialkow & I. Gerst, "The Transfer Function of General Two-
Terminal-Pair Networks," Quart. App. Month. Vol.X,No.2,1952,pp..
113-127

(1) The roots of D are distinct negative numbers.

(2) The roots of N are not positive real but are
     otherwise arbitrary.

(3) $M \geq N$

(4) The number C satisfies the inequalities
     $0 < C < C_o$ where C_o is the least of the three
     quantities. C_d, Bm/An(if An$\neq$0), 1 if m=n;
     and of the first two quantities if m n.
     If $C_o \neq C_d$ then C may equal C_o. Here C_d is
     the least positive value of γ (if it exists)
     for which the equation D-γN=0 has a non-
     negative multiple root.

A result of these conditions[2] is that all coefficients
a_i and b_i are non-negative, and

$$b_i \geq a_i$$

It will be recalled that the equation to be solved for
the natural frequencies of the system under consideration is

$$1 + K \frac{y_{21}}{y_{22}} = 0 \tag{1}$$

or $1 - KA(p) = 0$

where K is the gain of the ideal active device. Since we are

2. M. E. VanValkenburg, Introduction to Modern Network Synthesis,
    John Wiley, New York, 1960.

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restricting attention to the case which produces a single pair
of complex natural frequencies, this equation must be quadratic,
and the transfer function in the general case thus has the form

$$A(p) = \frac{a_0 p^2 + a_1 p + a_z}{b_0 p^2 + b_1 p + b_z}$$

for K real and positive.

Furthermore, equation (1) has the form

$$\sigma_0 p^2 + \sigma_1 p + \sigma_2 = 0$$

where $\sigma_i \geq 0$ if $0 \leq K \leq 1$.

The natural frequencies may be found in terms of the σ's by the
quadratic formula.

We define the Q of the system as the ratio of the center
frequency to the bandwith for $p = jw$. For large Q, this reduces to
the ratio of the imaginary part of the natural frequency to twice
its real part. Thus for the high-Q approximation we have

$$\text{center frequency} \quad \omega_0 \cong \sqrt{\frac{\sigma_2}{\sigma_0}}$$

$$Q \cong \frac{\sigma_0}{\sigma_1} \sqrt{\frac{\sigma_2}{\sigma_0}} = \frac{1}{\sigma_1} \sqrt{\sigma_2 \sigma_0}$$

In terms of the transfer function of the RC network and
the gain of the active device, we have

$$(b_0 - Ka_0)p^2 + (b_1 - Ka_1)p + (b_2 - Ka_z) = 0 \tag{2}$$

and

$$Q = \frac{\sqrt{(b_2 - Kaz)(b_0 - Kao)}}{b_1 - Ka_1} \tag{3}$$

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In order that complex natural frequencies exist, it is required that

$$(b_1 - Ka_1)^2 < 4(b_z - Ka_z)(bo - Kao)$$

We now define the <u>critical gain</u> K_c of the system as that value of K which produces a single pair of purely imaginary natural frequencies; i.e., the value of gain which produces infinite Q. Thus we obtain

$$K_c = \frac{b_1}{a_1}$$

It is to be noted that since $b_1 \cdot a_1$, the minimum value that K_c can have is Kc=1. If we demand that no finite critical gains exist other than K_c=1, we are forcing the restriction that b_1=a, for $a_1 \neq o$.

B. <u>Optimum Transfer Function</u>

It is now of interest to determine the particular form which the RC transfer function should have to produce the maximum value of Q. This is done by considering the values which the transfer function coefficients may take on if the network is to be RC-realizable. A number of different cases are examined in order to determine the maximum Q and the transfer function required to produce this Q. According to equation 3, the general form for Q is

$$Q = \frac{\sqrt{(b_z - Ka_2)(bo - KA_o)}}{b_1 - Ka_1}$$

Since the zeros of y_{22} must be negative real and distinct, the b's are related by

$$b_1^2 > 4bob_2 \tag{4}$$

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In the cases considered below, we shall assume that the inequality $K < K_c$ is maintained.

Case 1 $a_0 = a_2 = 0$, $A(p) = \dfrac{a_1 p}{b_0 p^2 + b_1 p + b_2}$ $= A_1(p)$

For this case, if Q exists it is given by

$$Q_1 = \sqrt{\dfrac{b_0 b_1}{b_1 - Ka_1}}$$

For the transfer function to be RC, it is required that $b_1 \geq a_1$. Since we do not permit finite critical gains other than unity, we must choose $b_1 = a_1$, and we obtain

$$Q_1 = \sqrt{\dfrac{b_0 b_2}{b_1 (1-K)}}$$

Applying inequality (4), we note that the obtainable Q for this case is

$$Q_1 < Q_1 = \dfrac{1}{2(1-K)} \tag{5}$$

Case 2 $a_1 = 0$, $A(p) = \dfrac{a_0 p^2 + a_2}{b_0 p^2 + b_1 p + b_2}$ $= A_2(p)$

For this case, Q is given by

$$Q_2 = \dfrac{\sqrt{(b_2 - Ka_2)(b_0 - Ka_0)}}{b_1}$$

We see that for large Q, K must be large and negative; i.e., the critical gain becomes infinite. To obtain maximum Q_2, we require that a_2 and a_0 take on their maximum values; namely, $a_2 = b_2$ and $a_0 = b_0$. Thus we obtain

$$Q_2 = \dfrac{\sqrt{b_2 b_0 (1-K)^2}}{b_1}$$

Applying inequality (4), we obtain

$$Q_2 < Q_{m2} = \frac{(1-K)}{2} \tag{6}$$

Case 3 $a_1 = a_2 = 0$, $A(p) = \dfrac{a_o p^2}{b_o p^2 + b_1 p + b_2} = A_3(p)$

In this case we obtain

$$Q_3 = \sqrt{\frac{b_2(b_o - Ka_o)}{b_1}}$$

For large Q, K must be large and negative, and we require a_o to have its maximum value $a_o = b_o$. Again applying inequality (4) we find that

$$Q_3 < Q_{m3} = \frac{1}{2}\sqrt{1-K} \tag{7}$$

Case 4 $a_o = 0$, $a_2 = b_2$ $A(p) = \dfrac{a_1 p + b_2}{b_o p^2 + b_1 p + b_2} = A_4(p)$

Here we obtain

$$Q_4 = \sqrt{\frac{b_2(1-K)b_o}{b_1 - Ka_1}}$$

For this case we note that for unity critical gain, it is required that $a_1 = b_1$. If inequality (4) is then applied one obtains

$$Q_4 < Q_m 4 = \frac{1}{2\sqrt{1-K}} \tag{8}$$

Case 5 $a_o = a_1 = 0$ $A(p) = \dfrac{a_2}{b_o p^2 + b_1 p + b_2} = A5(p)$

In this case we have

$$Q_5 = \sqrt{\frac{b_o(b_2 - Ka_2)}{b_1}}$$

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This is similar to case 3 in that K must be large and negative. To obtain large Q, we also require a_2 to be maximum; combining this with inequality (4) we find

$$Q_5 < Q_{m5} = \frac{1}{2}\sqrt{1-K} \tag{9}$$

which is the same result as was obtained in case 3.

<u>Case 6</u> $a_2 = 0$, $a_0 = b_0$ $A(p) = \dfrac{b_0 p^2 + a_1 p}{b_0 p^2 + b_1 p + b_2} = A_6(p)$

For this case,
$$Q_6 = \sqrt{\frac{b_0(1-K)(b_2)}{b_1 - Ka_1}}$$

Here again we see that for large Q and critical gain unity, it is necessary that $a_1 = b_1$. With the use of inequality (4) we obtain

$$Q_6 < Q_{m6} = \frac{1}{2\sqrt{1-K}} \tag{10}$$

which is the same result obtained for case 4.

Two other cases are possible; $a_2 = 0$ and a_0 small but not zero, and $a_0 = 0$ with a_2 small but not zero. These are degenerate forms of cases 1 and 2, and it is easily seen from eq.(3) that they yield lower values of Q than cases 1 or 2. Hence they will not be treated further.

Comparing the results of cases 1 through 6, we note that the maximum theoretically obtainable Q is

$$Q_1 < \frac{1}{2(1-K)}$$

$$\text{or} \quad Q_2 < \frac{(1-K)}{2}$$

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The optimum transfer function which must be used for maximum Q
is therefore

$$A(p) = \frac{b_1 p}{b_o p^2 + b_1 p + b_z} = A_1(p)$$

$$\text{or} \quad A(p) = \frac{b_o p^2 + b2}{b_o p^2 + b_1 p + b_2} = A_6(p)$$

C. Application of the Indefinite Admittance Matrix

Without loss of generality, we may normalize the center
frequency and let $b_o = b_z = 1$ in the above transfer functions. For
convenience we let $b_1 = k$, and we note from inequality (4) that

$$k > 2$$

The indefinite admittance matrix for a passive network
having transfer function $A(p) = \dfrac{kp}{p^2 + kp + 1}$ is

$$Y = \begin{vmatrix} \dfrac{N_{..}}{D_1} & -\dfrac{kp}{D_1} & -\left(\dfrac{N_. - kp}{D_1}\right) \\[2ex] \dfrac{-kp}{D_1} & \dfrac{p^2 + kp + 1}{D_1} & -\dfrac{(p^2 + 1)}{D_1} \\[2ex] -\dfrac{N_.. - kp}{D_1} & -\dfrac{p^2 + 1}{D_1} & \left(\dfrac{p^2 + 1 - kp + N_.}{D}\right) \end{vmatrix}$$

We note that if we reconnect the terminals of the network corres-
ponding to $A(p) = \dfrac{kp}{p^2 + kp + 1}$, interchanging terminals 1 and 3, the

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transfer function $\dfrac{v_2-v_1}{v_3-v_1}$ becomes $\dfrac{(p^2+1)}{p^2+kp+1}$. Thus we may show

that the only difference between cases 1 and 2 is the definition
of terminals. This fact is further verified as follows:

Let the network of case 1 be connected to an ideal
current amplifier as shown below:
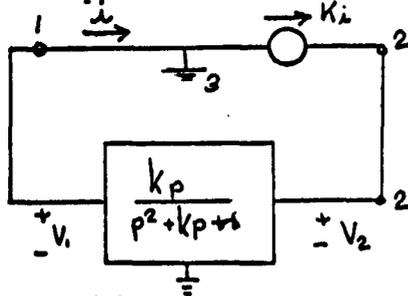
$$\dfrac{V_2}{V_1} = \dfrac{kp}{p^2+kp+1}$$

If we let terminal 1 be common, we have
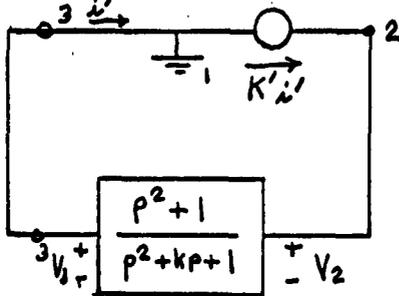
$$\dfrac{V_2}{V_3} = \dfrac{p^2+1}{p^2+kp+1}$$

With terminal 3 common, the Q is

$$Q = \dfrac{1-K'}{k}$$

But if $K' = \dfrac{-K}{1-K}$, we obtain

$$Q = \dfrac{1}{k(1-K)}$$

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Thus it is seen that cases 2 and 1 are the same, case 2 being obtained merely by redefining the terminals of case 1.

By using the indefinite admittance matrix, one can also show that case 4 is the same as case 3, and case 6 is the same as case 5. Thus there are only three transfer functions which we need consider:

$$A_1(p) = \frac{kp}{p^2+kp+1}$$

$$A_4(p) = \frac{kp+1}{p^2+kp+1}$$

$$A_6(p) = \frac{p^2+kp}{p^2+kp+1}$$

From the point of view of obtaining maximum Q, the first of these is the optimum transfer function; the remaining two will also be considered because they exhibit other interesting properties.

D. Realization of the Optimum Transfer Function

Having determined the form of the optimum transfer function, we now wish to synthesize an RC network having that transfer function. It is of interest to note that while several synthesis procedures are available,[3,4,5] most of them yield networks which produce the desired transfer function with an arbitrary multiplicative constant. For our purposes, these methods are not adequate; we require that the network have exactly the optimum transfer function

3. E. A. Guillemin, Synthesis of Passive Networks, John Wilen, New York, 1960
4. M. E. Van Valkenburg, op. cit.
5. J. E. Storer, Passive Network Synthesis, McGraw Hill, New York 1957

previously derived. Fortunately, a synthesis procedure has been
developed by Fialkow and Gerst[6] which realizes exactly the specified
transfer function. The procedure may be described qualitatively
as follows:

The given transfer function is decomposed into two
transfer functions which are realizable as L networks. An ad-
ditional series arm is then chosen for each network to produce
a particular y_{zz}. The two resulting T networks are connected in
parallel to produce the desired transfer function.

In this section we give only the results of the synthesis;
for the details of the procedure the reader is referred to the
paper by Fialkow and Gerst. The element values of the RC network
may be obtained in terms of the coefficient k in the transfer func-
tion, and an arbitrary constant B; the resulting network is shown
below.

$$\frac{1}{k-1} < \beta < 1 \quad \text{and} \quad k > 2$$
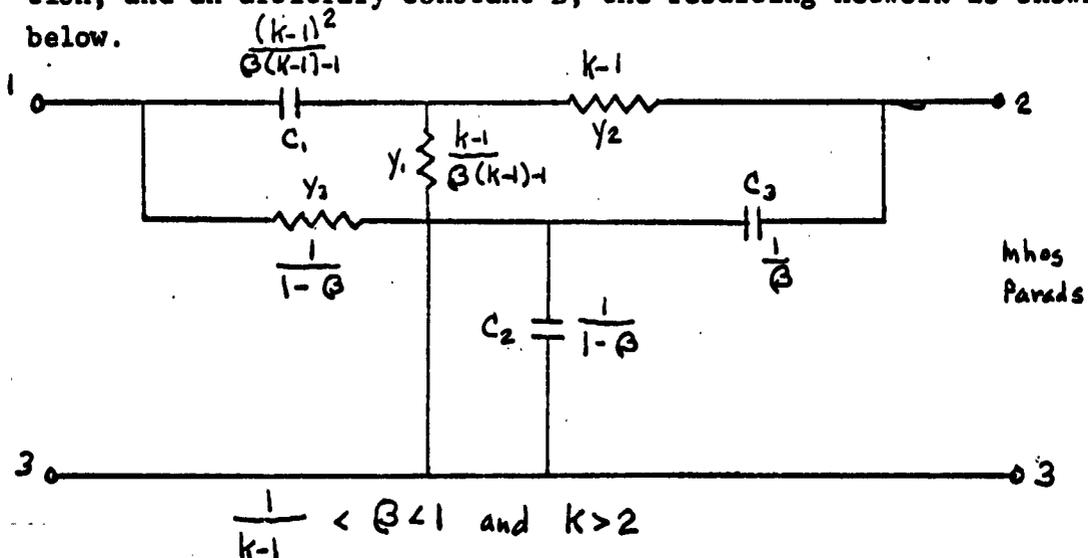
6. D. Fialkow and J. Gerst, op. cit.

At this point we note that if we interchange terminals 1 and 3, making 1 common, the circuit has the same configuration as the familiar "twin T" network. However, in most applications the Twin T is made symmetrical, with values as shown below. It will be noted that the transfer function

(circuit diagram showing terminals 3 and 2, with resistors R, capacitor 2C, capacitors C, and R/2, terminals 1)
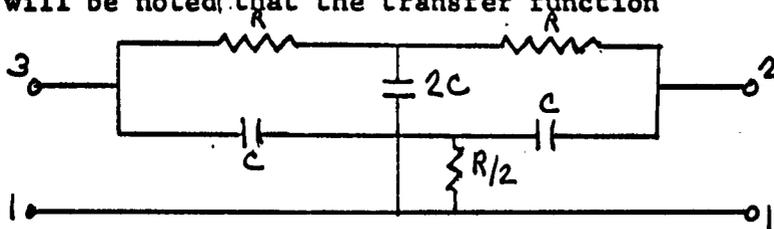
of this network is

$$\frac{v_2 - v_3}{v_1 - v_3} = \frac{p^2 + 1}{p^2 + 4\,p + 1}$$

where p is the complex frequency normalized by the factor $1/RC$. The Q which can be obtained with the symmetrical twin T connected in parallel with an ideal voltage or current amplifier having gain K is

$$Q < \frac{1-K}{4}$$

Thus we see that the symmetrical case does not lead to the maximum obtainable Q. Rather, one should use the network values obtained from the above synthesis, letting k be arbitrarily close to 2.

A further comment is in order regarding the configuration synthesized above. The network contains three capacitors, but the transfer function has only two poles. It is thus apparent that with the element values shown, cancellation of a pole by a zero is occurring in the transfer function. We may therefore expect

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that the system incorporating this network will exhibit considerable
sensitivity of Q to component values, since slight detuning may
eliminate the pole-zero cancellation and produce a consequent
shift of the natural frequencies of the system. Furthermore
the system is now potentially unstable, and detuning can cause
a shift of the natural frequencies into the right half of the
complex frequency plane.

E. Synthesis of Alternate Transfer Functions

Applying the same synthesis procedure to the transfer
function $A(p) = \dfrac{p^2+kp}{p^2+kp+1}$ we obtain the network below.
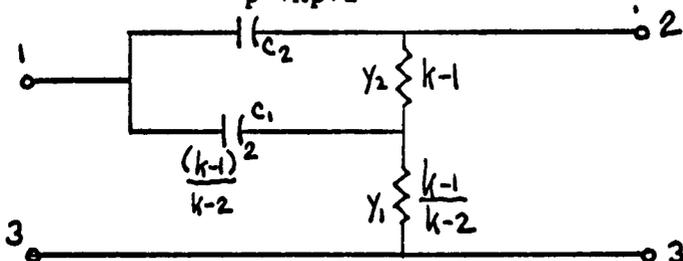
This network in combination with an ideal active device
gain K produces a Q of

$$Q = \frac{1}{k\sqrt{(1-K)}}$$

but the center frequency is

$$\omega_o = \sqrt{\frac{1}{1-K}}$$

The synthesis of the transfer function $A(p) = \dfrac{kp+1}{p^2+kp+1}$

yields the network below which has the same Q;

$$Q = \frac{1}{k\sqrt{1-K}}$$

but which has center frequency

$$\omega_0 = \sqrt{1-K}$$
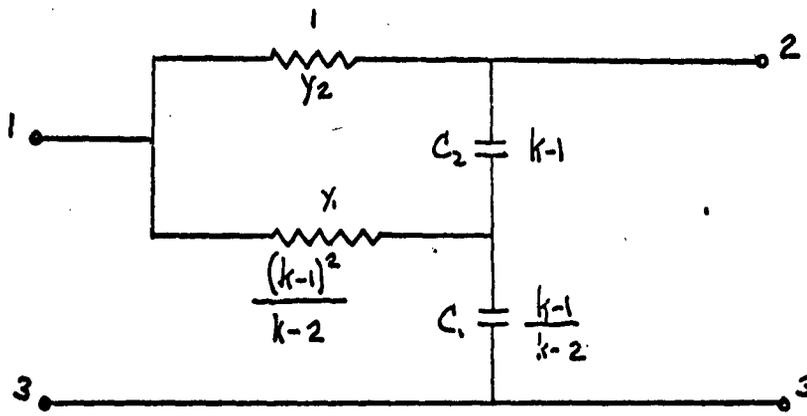
While the maximum obtainable Q with these networks is considerably lower than that of the network with optimum transfer function, it will later be shown that a system employing these networks is not potentially unstable. It is to be emphasized, however, that from a practical point of view their usefulness is severely limited by the heavy dependance of both Q and center frequency ω_o on the gain K.

IV.   Sensitivity

In order to evaluate the networks of the previous section with regard to their usefulness in integrated circuits, it is of paramount importance to determine the effects of tolerance variation of components and active device gain on the system performance. In this section, we shall show that for the system using a network with the optimum transfer function, component variations can lead to instability; whereas in the four-element networks, they cause only a degradation of Q and center frequency. In order to avoid undue mathematical complexity, we shall consider separately the effects of gain variations and component variations.

A. Gain Sensitivity

1. The Parallel T

For the parallel T resulting from the synthesis of the optimum transfer function, we have, when the network is perfectly tuned

$$Q = \frac{1}{k \ (1-K)}$$

We define a sensitivity factor S_K^Q as

$$S_K^Q = \frac{\partial Q}{\partial K} \quad \frac{K}{Q}$$

In terms of the active device gain, we obtain for the parallel T

$$S_K^Q = \frac{K}{1-K}$$

and in terms of the system Q,

$$S_K^Q = kQ-1$$

For the perfectly tuned network, the center frequency
is

$$j\omega_o = \frac{1}{2}\sqrt{k^2(1-K)^2-4}$$

which, for large values of Q is very nearly unity. Then

$$\frac{\partial \omega_o}{\partial K} = \frac{-k^2}{4\omega_o}(1-K) = \frac{-k}{4\omega_o Q}$$

and the sensitivity of the center frequency to variations of gain
is

$$S_K^{\omega_o} = \frac{kK}{4Q\omega_o{}^2}$$

For the high Q approximation, we recall that $\omega_o \simeq 1$ and $K \simeq 1$; thus we may write

$$S_K^{\omega_o} \simeq \frac{k}{4Q}$$

2. Four-element networks

For both 4-element configurations, the Q is

$$Q = \frac{1}{k\sqrt{1-K}}$$

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In terms of the gain, the sensitivity is

$$S_K^Q = \frac{\frac{1}{2}K}{1-K}$$

which may also be written in terms of the Q as

$$S_K^Q = \frac{1}{2}(k^2Q^2-1)$$

For one of the 4-element networks the center frequency is

$$\omega_0 = \sqrt{1-K}$$

while for the other it is

$$\omega_0 = \frac{1}{\sqrt{1-K}}$$

In both cases the sensitivity $S_K^{\omega_0}$ is the same:

$$S_K^{\omega_0} = \frac{\partial \omega_0}{\partial K} \frac{K}{\omega_0} = \frac{\frac{1}{2}K}{1-K} = \frac{1}{2}(k^2Q^2-1) = S_K^Q$$

These relationships illustrate that for large values of Q, the 4-element networks exhibit a very heavy dependence of both center frequency and Q upon the active device gain, whereas the center frequency of the parallel T network is virtually independent of gain, while the variation of Q with gain, for any given value of Q, is much less than that of the 4-element networks.

B. Component Sensitivity

1. The parallel T

Since the parallel T network contains three capacitors, we may expect that when the network is detuned, the characteristic equation for the RC-active system will be cubic rather than

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quadratic. The procedure for determining the sensitivity of the system to component values is as follows:

      (1) The components are assigned literal nominal values and tolerance variations, and the characteristic equation is obtained.

      (2) The component values in terms of the transfer function coefficient k and the synthesis parameter β are substituted and the cubic equation is solved literally by an approximation method.

      (3) k and β are forced to take on limiting values and expressions for ω_0 and Q are obtained in terms of the tolerance parameters and gain.

We draw the network with general components as shown below. Solving for the characteristic
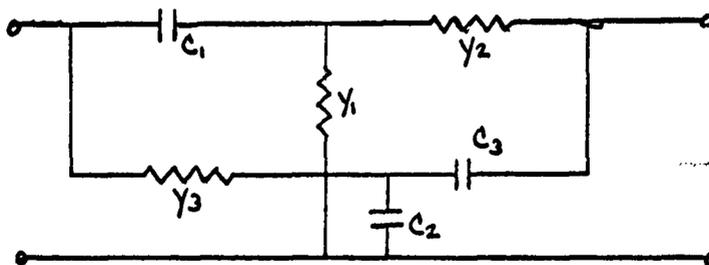
equation, we obtain

$$0 = s^3 + \left\{ \frac{y_1 + y_2}{C_1} + (1-K)\left[\frac{y_3(C_2 + C_3)}{C_2 C_3} + \frac{y_3}{C_2} \right] \right\} s^2$$

$$+ \left\{ \frac{y_1 y_2 (C_2 + C_3)}{C_1 C_2 C_3} + (1-K)\left[\frac{y_2 y_3}{C_2 C_3} + \frac{y_3(y_1 + y_2)}{C_1 C_2} \right] \right\} s$$

$$+ \frac{y_1 y_2 y_3}{C_1 C_2 C_3}$$

where S is the complex frequency variable (we reserve $\overset{.}{p}$ and p^1 for the normalized complex frequency variables). We now assign tolerance parameters $\delta, \zeta, \tau, \alpha, \gamma, \theta$ to the components and let each component take on the literal value derived from the synthesis procedure:

$$C_1 = \frac{(k-1)^2}{\beta(k-1)-1}(1+\delta)$$

$$C_2 = \frac{(1+\zeta)}{1-\beta}$$

$$C_3 = (1+\zeta)$$

$$y_1 = \frac{(k-1)(1+\alpha)}{\beta(k-1)-1}$$

$$y_2 = (k-1)(1+\gamma)$$

$$y_3 = \frac{(1+\theta)}{1-\beta}$$

where it is assumed that the tolerance parameters may be either positive or negative, but have magnitude much less than unity.

Investigation shows that in the perfectly tuned case, both y_{21} and y_{22} of the network have a pole at $p = -\beta$. When the transfer function is formed, poles of y_{22} become zeros of the transfer function; poles of y_{21} are poles of the transfer function. Thus the common factors $(p +\beta)$ cancel. We reason that for sufficiently small detuning this cancellation no longer occurs, but that the resulting pole and zero move only a short distance from their original position on the real axis. Thus, we make the approximation that one factor of the cubic equation is

$$(p +\beta +\lambda)$$

where λ is a small real quantity which approaches zero when the network approaches perfect tuning. We substitute $p = (\beta + \lambda)$ in the cubic equation, discard higher order powers of λ, and higher order powers of tolerance parameters, and solve for λ. The cubic equation is then divided by $(p + \beta + \lambda)$, and the resulting quadratic equation may easily be solved for ω_0 and Q. The quadratic equation is

$$0 = p^2 + \left[(\gamma - \delta) + \frac{(\alpha - \gamma)}{k-1} + k(1-K) - \frac{\beta(\theta - \tau + \frac{\alpha - \gamma}{k-1}) + \beta^2 (\tau + \epsilon + \gamma - \delta)}{(\ +1)} \right] p$$

$$+ \left[1 + \alpha + \gamma - \delta - \epsilon - \theta \ (\tau + \epsilon + \gamma - \delta) - \frac{(\alpha - \gamma)}{k-1} \right.$$

$$\left. + \frac{\beta(\theta - \tau \ \cdot \ \frac{\lambda - \gamma}{k-1}) + \beta^2 (\tau + \epsilon + \gamma - \delta)}{(\beta + 1)} \right] \qquad (11)$$

where we have made use of the approximation

$$\frac{1}{1 + \lambda} \qquad 1 - \lambda \ \text{etc.}$$

The effect of the tolerance variation of each component is represented in eq. (11) by the tolerance parameter of that component.

We now let k and β approach the values which yield maximum Q in the perfectly tuned case:

$$k \longrightarrow 2$$
$$\beta \longrightarrow 1$$

The quadratic equation becomes:

$$0 = p^2 + \left[2(1-K) - \frac{(\theta - \alpha + \epsilon - \delta)}{2} \right] p + \left[1 + \tau + \gamma - \frac{3}{2} \epsilon + \frac{(\theta + \lambda - \delta)}{2} \right] \quad (12)$$

We now let all components have the same magnitude of tolerance variation, $100\lambda\%$, and we let each component take on its "worst

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case" condition. We then obtain

$$Q \cong \frac{1}{2(1-K) \pm 2 |k|} \qquad \text{for high Q}$$

$$\omega_o \cong 1 \pm 2.5 \alpha$$

An important result which may be noted in eq. (12) is that if

$$\alpha > (1-K)$$

in the worst case the system becomes <u>unstable</u>. If we design the network so that with an ideal amplifier having exactly unity gain, the system is unconditionally stable, we see that the Q of the system may vary between the limits.

$$\frac{1}{4\alpha} < Q < \infty$$

As an example of the extreme gravity of the instability problem, consider a network which is designed to produce a Q of 200 when perfectly tuned. The required gain will be minimum when $k \rightarrow 2$, for which it is required that

$$Q = 200 = \frac{1}{2(1-K)} \quad ;$$

hence $K = .9975$

and $1-K = .25 \times 10^{-2}$

Now if all components vary in the worst case direction by an amount greater than 0.25%, the system becomes unstable. If the components vary 0.25% in the opposite direction, the obtainable Q is

$$Q = \frac{1}{.5 \times 10^{-2} + .5 \times 10^{-2}} = 100$$

It is to be emphasized that these results apply to the RC network with an ideal active device. When the non-ideal nature of the active device is taken into account, together with parasitic capacitances, etc., which will be encountered in the integrated circuit environment, the situation is sure to be worse. It thus appears that the extreme sensitivity of the parallel-T system to component variations rules it out as a means of frequency selective amplification.

2. Four-element networks

In analyzing the component sensitivity of the 4-element networks we follow essentially the same procedure as has been outlined above, except that our task is much easier since only quadratic equations result.
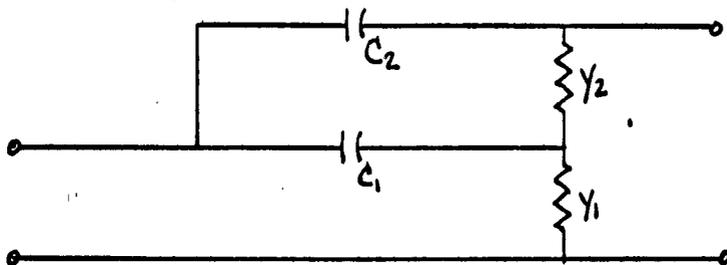
For the above network with an ideal active device, we obtain the characteristic equation

$$s^2 C_1 C_2 (1-K) + S(1-K) [C_2(y_1+y_2) + C_1 y_2] + y_1 y_2 = 0 \qquad (13)$$

We note immediately that this system can never become unstable for any variations of component values. We next assign tolerance parameters, and component values obtained from the synthesis procedure:

$$y_1 = \frac{(k-1)}{(k-2)}(1+\lambda)$$

$$y_2 = (k-1(1+\delta)$$

$$c_1 = \frac{(k-1)^2}{(k-2)}(1+\epsilon)$$

$$c_2 = (1+\gamma)$$

Letting $k \longrightarrow 2$ for maximum Q, we obtain

$$Q \approx \left[\frac{1}{2+\alpha-\epsilon}\right]\sqrt{\frac{1+\alpha+\delta-\epsilon-\gamma}{(1-K)}}$$

$$\omega_0 \approx \sqrt{\frac{1+\alpha+\delta-\epsilon-\gamma}{1-K}}$$

If all components have the same magnitude of tolerance variation and all vary in the worst case direction, we have

$$Q \approx \frac{(1+\alpha)}{2\sqrt{1-K}}$$

$$\omega_0 \approx \frac{(1+2\delta)}{\sqrt{1-K}}$$

It is to be noted that these results are valid only for $\alpha \ll 1$.

C. General

The analysis of this section indicates that the parallel-T system is much less sensitive to gain variations than the 4-element networks, but much more sensitive to component variations. Furthermore, the parallel-T system is potentially unstable. This seems to rule out use of the parallel-T, while the extreme gain

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sensitivity of the 4-element networks makes them all but useless. For comparison, we note the component sensistivity of a single tuned RLC network:

$$S_R^Q = -1 \qquad\qquad S_L^{\omega_o} = -\tfrac{1}{2}$$

$$S_L^Q = \tfrac{1}{2} \qquad\qquad S_C^{\omega_o} = -\tfrac{1}{2}$$
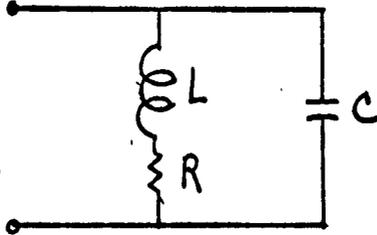
$$S_C^Q = -\tfrac{1}{2} \qquad\qquad S_R^{\omega_o} \cong 0 \text{ for high Q}$$

V.   Effects of Non-Ideal Active Devices

A. Theoretical considerations

In preceding sections, we have concentrated primarily on the behavior of RC networks with active devices which depart from ideal only in that their voltage or current gains are different from unity. In this section, we consider the effects of non-ideal active devices; to prevent the complexity of the mathematics from obscuring the results, we assume the network to be a perfectly tuned parallel-T configuration derived by the synthesis of the optimum transfer function.

In general terms, if we let network parameters be y_{ij}, and Y_{ij} be the amplifier parameters normalized to the impedance level of the network, the characteristic equation for the system becomes

$$(y_{11} + Y_{11})\ (y_{22} + Y_{22})\ -\ (y_{12} + Y_{12})\ (y_{21} + Y_{21}) = 0$$

For the perfectly tuned parallel-T we have y parameters

$$y = \frac{Xp}{p+\beta} \qquad \text{where} \quad X = \frac{\beta(k-1)^2}{\beta(k-1)-1}$$

$$y_{12} = y_{21} = \frac{-kp}{p+\beta}$$

$$y_{22} = \frac{p^2+kp+1}{p+\beta}$$

We make the assumption that the Y's are real; the characteristic is thus

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$$(Y_{11} + x) \ p^3$$
$$+ \left[\beta Y_{11} + (Y_{11} + x)(Y_{22} + k) - (Y_{12} - k)(Y_{21} - k)\right] \cdot p^2$$
$$+ \left\{\beta\left[Y_{11}(k+Y_{22}) + Y_{22}(Y_{11}+x) + Y_{12}(k-Y_{21}) + Y_{21}(k-Y_{12})\right] + (Y_{11}+x)\right\} p$$
$$+ \ \beta\left[\beta(Y_{11} Y_{22} - Y_{21} Y_{12}) + Y_{11}\right]$$
$$= 0$$

(14)

It will be noted that we usually define ports 1 and 2 for the active devices as shown below
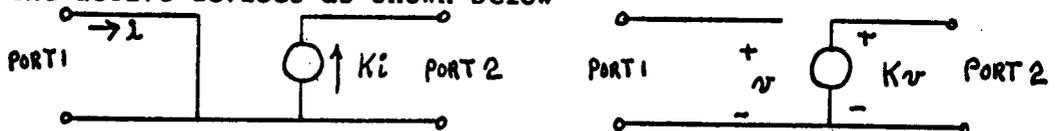
If the active device to be used is a current amplifier, the above equation applies as it stands. If a voltage amplifier is to be used, port 2 of the amplifier must be connected to port 1 of the network. This causes the Y parameters in the characteristic equation to have their subscripts 1 replaced by 2 and vice versa. Since the equation is symmetrical with respect to Y_{12} and Y_{21}, the only change occurring is the interchange of Y_{11} and Y_{22}.

In the active device configurations which will be considered in this paper, it is found that a very good approximation is

$$Y_{11} Y_{22} - Y_{12} Y_{21} = 0$$

Using this in (14) we obtain

$$\left(1 + \frac{x}{y_{11}}\right) p^3$$
$$+ \left[(\beta + k) + \frac{k(Y_{21} + Y_{12} + x-k) + xY_{22}}{Y}\right] p^2$$
$$+ \left[(\beta k +1) + (\beta Y_{22} +1) x + \beta k (Y_{21} + Y_{12})\right] p$$
$$+ \beta = 0$$

(15)

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It is clear that solution of (15) to obtain Q in terms of the active device parameters would be extremely tedious. Therefore, we shall consider the parameters separately, and attempt to combine the results.

Case 1 - $y_{11} \longrightarrow \infty$, $y_{22} = 0$, $y_{12} \longrightarrow \infty$, $y_{21} \longrightarrow \infty$, $\dfrac{y_{21} + y_{12}}{y_{11}}$ = finite

Making the further approximation that $k \rightarrow 2$ and $\beta \longrightarrow 1$, we obtain

$$Q_1 \approx \frac{1}{2(1 + \dfrac{y_{12} + y_{21}}{y_{11}})}$$

Case 2 $y_{22} = 0$, y_{11} finite, $y_{12} = 0$, $\dfrac{y_{21}}{y_{11}} = 1$

In this case a cubic equation results. Making the approximation that one factor is $(p + \beta + \lambda)$ we find

$$\lambda \cong 2/y_{11} \text{ as } \beta \longrightarrow 1, \ k \longrightarrow 2$$

Substituting this value of λ in the quadratic factor, we obtain

$$Q_2 \cong \sqrt{\frac{Y_{11}(Y_{11} + x)}{4 + x}}$$

We assume that $Y_{11} >> x$, then

$$Q_2 \cong \frac{Y_{11}}{4 + x}$$

Case 3 y_{22} finite, $y_{11} \longrightarrow \infty$, $y_{12} = 0$, $\dfrac{y_{21}}{yu} = 1$

For this case we obtain

$$Q_3 = \sqrt{\frac{1 + Y_{22}}{Y_{22}}}$$

as $k \to 2$ and $\beta \longrightarrow 1$. For practical amplifiers, a reasonable approximation is $Y_{22} \ll 1$; thus

$$Q_3 \approx \frac{1}{Y_{22}}$$

To find the total effect of the amplifier, we assume that the total Q is given approximately by

$$\frac{1}{Q_T} \approx \frac{1}{Q_1} + \frac{1}{Q_2} + \frac{1}{Q_3}$$

$$Q_T \approx \frac{1}{2\left(1 + \frac{Y_{12} + Y_{21}}{Y_{11}}\right) + \frac{4+x}{Y_{11}} + Y_{22}} \tag{16}$$

It is to be noted that the Y's are the normalized values of active device parameters. Let Y_{ij}^a be the actual active device parameters and b be the normalizing factor such that

$$\frac{Y_{ij}^a}{b} = Y_{ij}$$

We may then write (16) as

$$Q_T \approx \frac{1}{2\,\dfrac{\left(1 + Y_{21}^a + Y_{12}^a\right)}{Y_{11}^a} + \dfrac{(4 + x)b}{Y_{11}^a} + \dfrac{Y_{22}^a}{b}} \tag{17}$$

Equation (17) indicates that there is an optimum value for b; this is intuitively correct because scaling the network values by too small a factor makes y very important, while scaling them by too large a value makes y dominant. The optimum b is

$$b = \sqrt{\frac{Y_{11}^a \, Y_{22}^a}{4+x}}$$

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which produces

$$Q_T \simeq \cfrac{\frac{1}{2}}{1 + \cfrac{Y^a_{12} + Y^a_{22}}{Y^a_{11}} + \sqrt{\cfrac{(4+x)Y^a_{22}}{Y^a_{11}}}} \qquad (18)$$

It is to be noted that this result applies for current amplifiers; for voltage amplifiers the subscripts 1 and 2 are interchanged.

B. Practical Active Devices

A number of transistor circuits have been investigated which provide good approximations of ideal unity-gain voltage or current amplifiers. The expression for Q_T given in eq. (18) provides a convenient means for evaluating these devices on a comparative basis. For the particular application discussed in this paper, we shall define an active device figure of merit as

$$F = Q_T \; \frac{w_o}{w_\lambda}$$

where w_o is the active device half-power frequency and w_λ is the common base cutoff frequency of the transistors used in the active device. To represent the transistor, we shall use the simplified small-signal equivalent circuit shown below
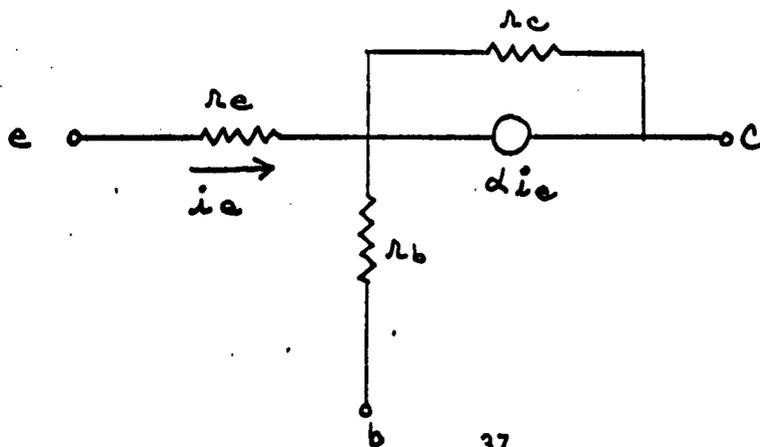
We let $\quad y_{ib} = r_e + r_b(1-\alpha)$

$$y_{ie} = r_6 + \frac{re}{1-\alpha}$$

$$\alpha = \frac{\alpha_o}{1 + \frac{s}{w_\alpha}}$$

$$B = \frac{\alpha}{1-\alpha}$$

The amplifier circuit configurations, together with their y parameters and figures of merit, are given in tabular form below. It is to be noted that all bias resistors, coupling capacitors, etc. have been omitted. For convenience of comparison, we have included numerical values of the figure of merit assuming the values

$$k = 2.1$$
$$\beta = 1$$
$$B_o = 100$$
$$r_e = 30\,\Omega$$
$$r_b = 100\,\Omega$$
$$rc = 10^6$$

| CONNECTION	y	y	$y.$	y		Q_T	F
	$\dfrac{y_{ie}}{B+2}$	$\dfrac{-y_{ie}}{B+2}$	$\dfrac{(B+1)^2 y_{ie}}{B+2}$	$\dfrac{(B+1)^2 \cdot y_{ie}}{B+2}$	$\dfrac{0.64}{B_o+1}$	12.7	0.08
	$\bar{y}_{ia}$	$-y_{ie}$	$-(B^2+B+1)y_{ie}$	$(B^2+B+1)y_{ie}$	$\dfrac{1}{\sqrt{B_o}}$	12.5	1.25
	$(B^2+B+1)y_{ie}$	$-(B+1)g_c$	$-B^2 y_{ie}$	$(B+1)g_c$	$\dfrac{1}{y_{ib}r_e} \approx 1$	49.5	49.5
	$\dfrac{B^2+B+1}{2B^2+3B+2}y_{ib}$	$-g_c$	$\dfrac{B(B+1)}{2B^2+3B+2}y_{ib}$	g_c	0.61	16.1	9.8
	$\dfrac{B+1}{B+2}\,y_{ib}$	$-g_c$	$\left(\dfrac{-B}{B+1}\right)y_{ib}$	$\left(\dfrac{B+2}{B+1}\right)g_c$	0.414	23.0	9.5
	$(1+\delta B)y_{ib}$	$-(B+1)g_c$	$-\alpha(B+1)y_{ib}$	$(B+1)g_c$	1	22.7	22.7
	y_{ib}	$-g_c$	$-y_{ib}$	g_c	1	15.6	15.6
	y_{ie}	$-y_{ie}$	$-(B+1)y_{ie}$	$(B+1)y_{ie}$	$\dfrac{1}{(B_o+1)}$	1.28	0.013

B_o = D.C. Base to Collector Current Gain

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A word of caution is necessary in applying the figures
of merit shown in the table. In some of the configurations, when
the necessary bias resistors are included they have a serious
detrimental effect on the figure of merit. This is particularly
true of circuits 1, 3, and 5. It is of particular interest to
note that the single-transistor common-base current amplifier
has a reasonably high figure of merit and also has only minor
bias restrictions. These features, together with its extreme
simplicity, make it very attractive as an active device in this
application.

VI.   Experimental Results

In order to obtain some feeling for practical problems,
an RC network was synthesized and a bandpass amplifier with
electronic tuning was constructed. The basic circuit is shown
below.

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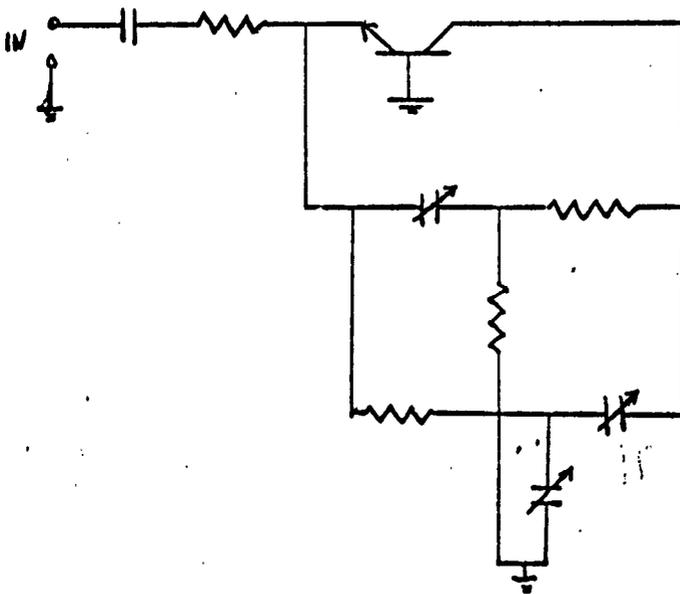
The network values were obtained by synthesizing the transfer function $L(p) = \dfrac{3p}{p^2+3p+1}$ with $= .833$.

The actual circuit is shown on the next page; zener diodes D_1, D_7 and D_9 were used as voltage-variable capacitors, while the other zener diodes were used to provide voltage reference levels for bias and tuning. The system is tuned by varying the three power supply voltages until maximum Q is obtained at the center frequency. Transistor T_2 is used as an isolation amplifier.

The experimental circuit confirmed at least qualitatively the results of the analytical study. With sufficient care, the circuit could be tuned to produce a Q of 400 at 455KC, but at that value of Q, small changes resulting from component drift even at room temperature, caused the circuit to break into oscillation. It is estimated that a Q of 30 might be obtained with reasonable sensitivity to tuning and without instability resulting from component drift, etc.

The four-element networks were also constructed and tested with various active devices; the best Q obtained was 3.

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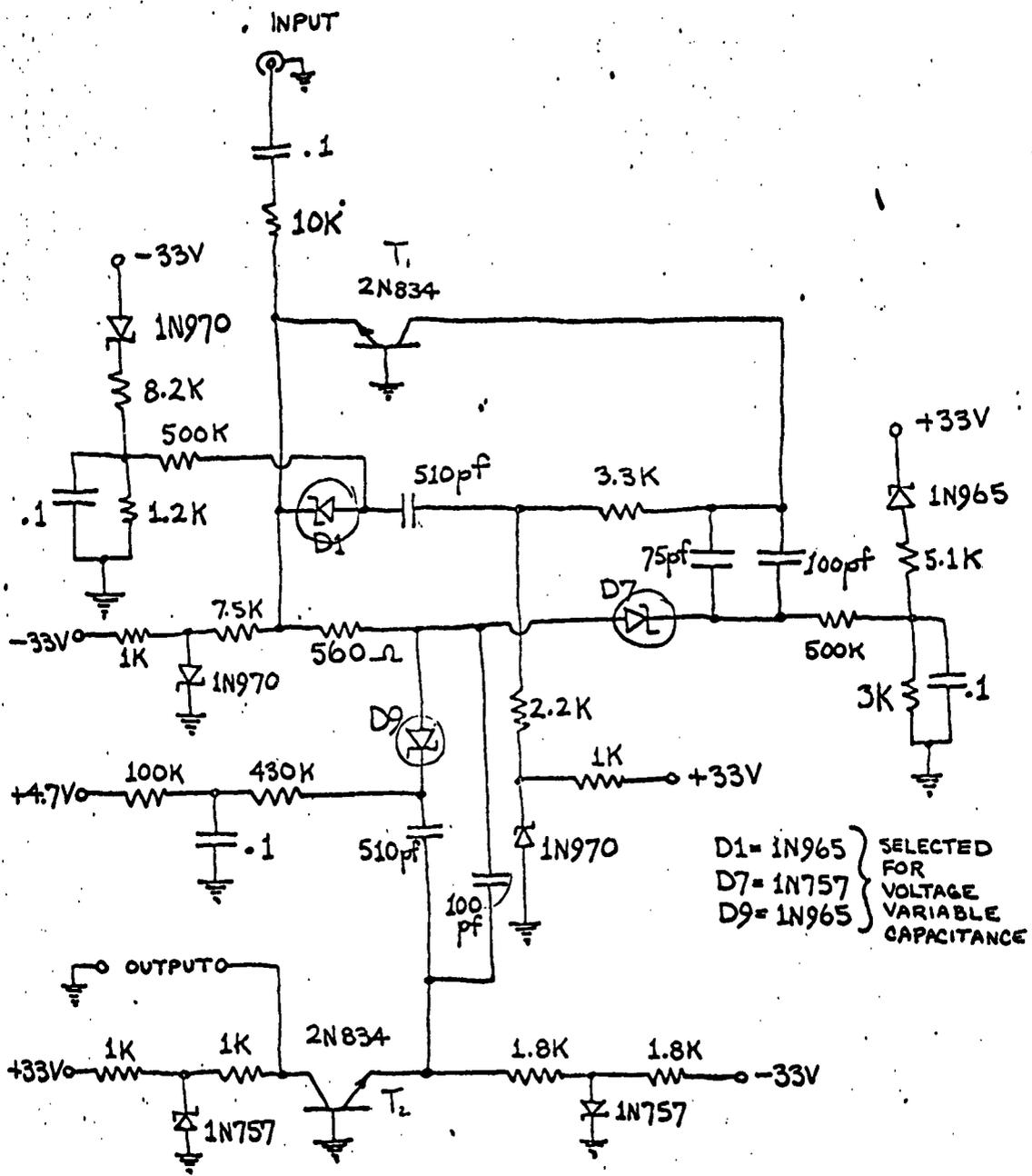
ELECTRONICALLY TUNED BANDPASS AMPLIFIER
Q ≈ 225 @ 455 KC

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BANDPASS CHARACTERISTICS
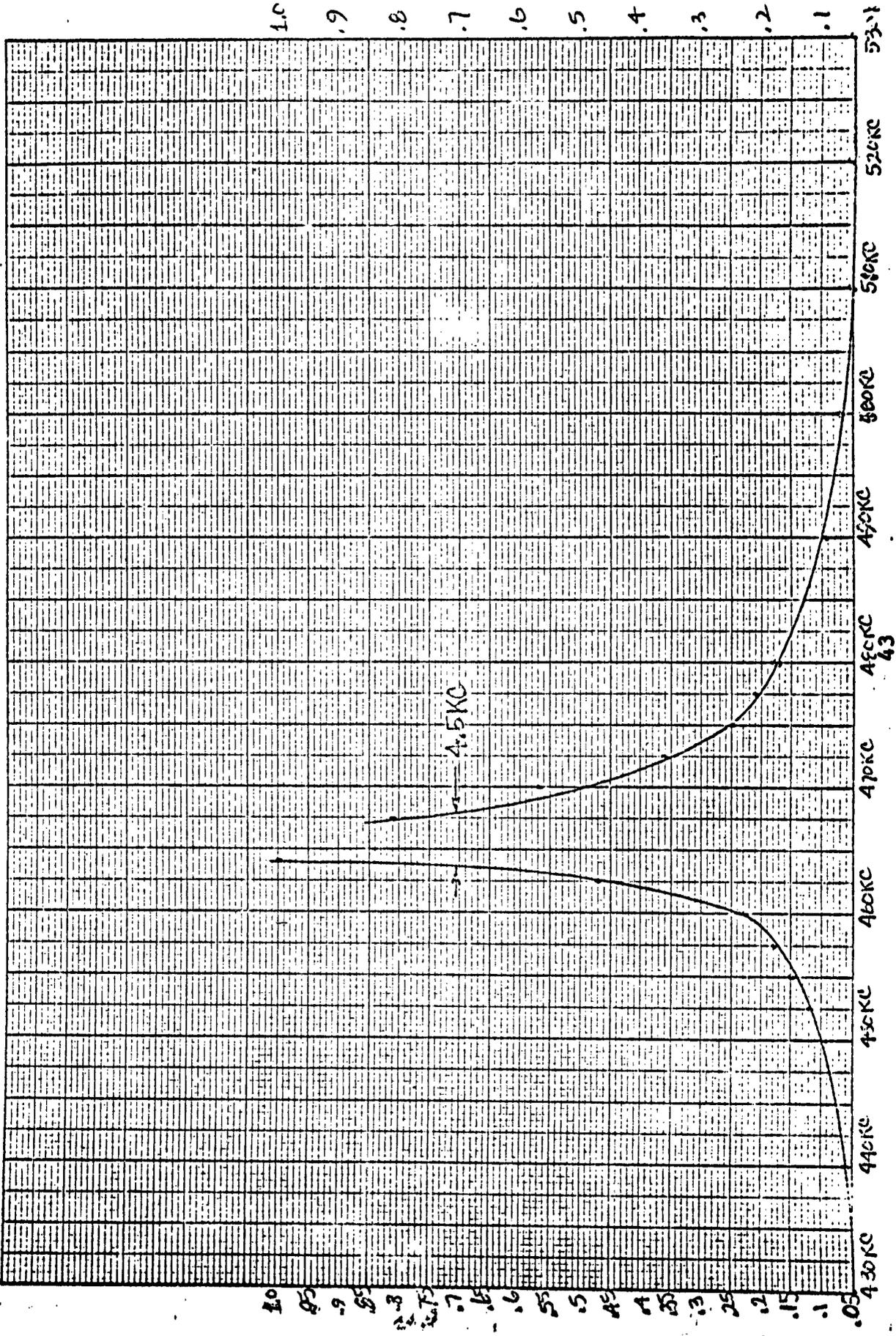
VII.   Conclusions

. In this report we have investigated a particular class
of lumped RC-active networks for use in frequency selective am-
plification: the class of networks consisting of a three-terminal
lumped, linear, passive, time invariant network connected in para-
llel with a three terminal active device which closely approximates
an ideal voltage or current amplifier with real, linear, time
invariant parameters. Attention has been restricted to RC net-
works which, when properly tuned for selective amplification,
have voltage transfer functions in which the degree of numerator
and denominator does not exceed 2.

RC circuits have been synthesized to yield the maximum
obtainable Q for this class of networks; effects of non-ideal
active devices have been analyzed; and a practical configuration
has been constructed and tested.

The general conclusion of this study is that this class
of networks is not suitable for use with present or forseeable
integrated circuit technology, due to the extremely stringent
requirements which the components must meet in order to maintain
reasonable sensitivity and stability ranges. Particular con-
clusions regarding individual networks, active devices, etc.,
have been given in the body of the report and will not be repeated
here.

<center>APPENDIX</center>

Gain Stability in Feedback Amplifiers

Justification for the use of unity gain amplifiers to create bandpass characteristics may be found if we investigate the properties of the following feedback amplifier.
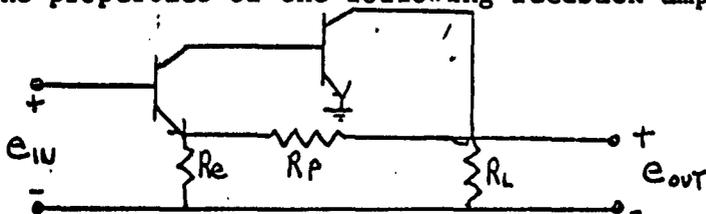
The voltage gain of the circuit is

$$G_1 = \frac{\rho^2 R_L (R_e + R_f)}{h_{ie}(R_e + R_f + R_L) + \beta R_e (\beta R_L + R_f)}$$

Let us now consider two limiting cases for G. First assume $R_f = 0$, then the voltage gain expression reduces to

$$G_{1\ R_f=0} = 1 - \frac{h_{ie}(R_e + R_1)}{\beta^2 R_e R_1} = 1 - \frac{h_{ie}}{\beta^2 R_p}.$$

where $R_p = \frac{R_e R_L}{R_e + R}$. Typical gain, with $h_{ie} = 400\Lambda$, $R_p = 3K$, and $\beta = 20$, is 0.999675 or very close to unity.

The second limiting case occurs when R_f and $R_e \gg \frac{h_{ie}}{\beta}$, and $\beta R_L \gg R_f$. The gain expression then reduces to

$$G_{1 \ne R_f \ 0} = \frac{1 + \frac{Rf}{Re}}{1 + \frac{Rf}{\beta R_1}}$$

The gain is therefore determined primarily by the ratio of two resistors. $G_{R_f \neq 0}$ may range as high as $\dfrac{\beta^2 R_L}{h_{ie}}$

In the first case with $R_f \equiv 0$ the gain approaches arbitrarily close to unity, while no such stable limit exists for the second case with $R_f > 0$. It will now be shown that in addition to approaching a limiting gain the unity gain amplifier is much less sensitive to component and transistor changes. Relating the percentage change in gain to circuit variations we find the following:

$$\underline{R_f \equiv 0} \qquad\qquad\qquad \underline{R_f > 0}$$

$$\frac{dG}{G} = \frac{-h_{ie}}{\beta R_p}\left(\frac{dh_{ie}}{h_{ie}}\right) + \frac{2h_{ie}}{\beta^2 R_p}\frac{d\beta}{\beta} \qquad \frac{dG}{G} = -\left(\frac{R_f}{R_e + R_f}\right)\left(\frac{dR_e}{R_e}\right)$$

$$+ \frac{h_{ie}}{\beta^2 R_p}\left(\frac{dR_p}{R_p}\right) \qquad\qquad + \left(\frac{R_f}{R_e + R_f} - \frac{R_f}{R_i + R_f}\right)\frac{dR_f}{R_f}$$

$$+ \left(\frac{R_f}{\beta R + R_f}\right)\left(\frac{d\beta}{\beta}\right)$$

$$+ \left\{\frac{R_f}{\beta(R + R_f)}\right\}\left(\frac{dR_i}{R_i}\right)$$

Inserting typical values such as

$$h_{ie} = 400\,\Omega, \qquad R_p = 3K, \qquad p = 20,$$
$$R_f = 20K, \qquad R_e = 3.5K, \quad R_L = 20K$$

we find

$$\frac{dG}{G} = -6.7\times10^{-3}\left(\frac{dh_{ie}}{h_{ie}}\right) \qquad\quad \frac{dG}{G} = -(0.85)\left(\frac{dR_e}{R_e}\right) + (0.80)\left(\frac{dR_f}{R_f}\right)$$

$$+6.7\times10^{-4}\left(\frac{d\beta}{\beta}\right) \qquad\qquad\qquad + 4.7\times10^{-2}\left(\frac{d\beta}{\beta}\right)$$

$$+1.3\times10^{-3}\left(\frac{dR_p}{R_p}\right) \qquad\qquad\qquad + 2.5\times10^{-2}\left(\frac{dR_f}{R_f}\right).$$

Note the two orders of magnitude difference in sensitivity to changes of β. The unity gain amplifier is at least one order of magnitude less sensitive than the other amplifier to all component changes.

From the foregoing, it is easily seen that gains other than unity cannot be maintained to the critical degree required by RC bandpass techniques.

NETWORK-AMPLIFIER CHARACTERISTICS

Configuration / Characteristic				
Gain Restrictions for Stability	$K > 1.5$ or $K < 1.0$	$K \leqslant 1$	$K \leqslant 1$	$K \leqslant 1$
Gain Restrictions for Imaginary Pole Location	$K > 1.25$	$K > 0$	$K \leqslant 1$	$K \leqslant 1$
Sensitivity of Q to Gain, K $S = \dfrac{dQ}{Q} \cdot \dfrac{K}{dK}$	$S = -6Q$	$S = \dfrac{1}{(1-K)}$	$S = -\dfrac{1}{2(1-K)}$	$S = -\dfrac{1}{2(1-K)}$
Sensitivity of Q to Component Tolerance, (some Components cause factor of 2 difference) [Sensitivity of av. component]	$\dfrac{\Delta Q}{Q} = \dfrac{-\alpha Q}{1+Q}$	$\dfrac{\Delta Q}{Q} = \dfrac{1}{1+\dfrac{(1-K)}{\alpha}}$ $(1-k) \approx 0.999$	$\dfrac{\Delta Q}{Q} = \dfrac{\alpha}{2}$	$\dfrac{\Delta Q}{Q} = \dfrac{\alpha}{2}$
Center Freq. Shift with Gain	$\dfrac{\Delta \omega}{\omega_o} = \dfrac{3}{2Q} \cdot \dfrac{K}{K}$	$\dfrac{\Delta \omega}{\omega_o} = \dfrac{1}{2}\dfrac{\Delta K}{K}$	$\dfrac{\Delta \omega}{\omega_o} = -\dfrac{1}{2}\dfrac{\Delta K}{K}$	$\dfrac{\Delta \omega}{\omega_o} = -\dfrac{1}{2}\dfrac{\Delta K}{K}$
Center freq. Shift with Component Tolerance,	$\dfrac{\Delta \omega}{\omega_o} = \dfrac{\alpha Q}{2Q+1}$	$\dfrac{\Delta \omega}{\omega_o} = \dfrac{1}{2}\alpha$	$\dfrac{\Delta \omega}{\omega_o} = \dfrac{\alpha}{2}$	$\dfrac{\Delta \omega}{\omega_o} = \dfrac{\alpha}{2}$

Calculation with $\beta \to 1$, $k \to 2$

FREQUENCY SELECTIVE AMPLIFICATION FOR INTEGRATED CIRCUITS
PART 2

PRELIMINARY INVESTIGATION OF DISTRIBUTED RC NETWORKS

I. SUMMARY

Illustrated here are analytical techniques appropriate to those distributed networks which, when combined with active devices, create bandpass amplifier characteristics. A preliminary two transistor circuit is shown with $Q = 7$ at 800kc.

II. INTRODUCTION

Circuit designers must consider the characteristics of distributed parameter networks when developing integrated circuits due to the inherent distributed nature of all integration techniques - purely lumped circuit elements do not exist. Often, also, it is possible to create effects not easily realizable with lumped networks alone.

The progress of integrated circuits has been hindered, however, by the difficulty of microminiaturizing the inductor with presently available techniques. Resistors and capacitors are easily integrated because their values are primarily dependent on aspect ratios. Inductor values are fixed by internal volume. The general physical characteristics of inductors do not lend themselves to the integration techniques of diffusion, depositation, growing, and etching, while resistors and capacitors are easily formed in this manner.

Due to the lack of suitable inductors there have been few solutions to the integrated bandpass amplifier problem. Separately mounted crystal filters have been used but no technique is yet available for directly integrating quartz structures.

Lacking LC networks and crystal substitutes at this time, most work in this area has hinged on the bandpass effects created by lumped RC networks in appropriate positive and negative feedback loops. It has been shown in a companion paper [1] that lumped RC structures can be made to yield bandpass characteristics but that component tolerance is hypercritical for high Q systems.

Since the ultimate aim is to develop techniques suitable for integrated circuits, the characteristics of distributed resistors are being investigated. Distributed resistors are simply back-biased junctions with a high sheet resistance layer.
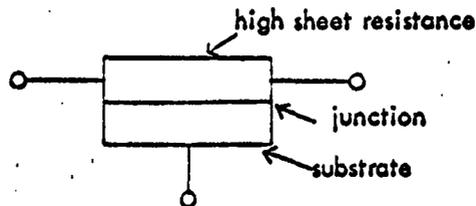

The resistive material and the back-biased junction act as an infinite RC ladder.
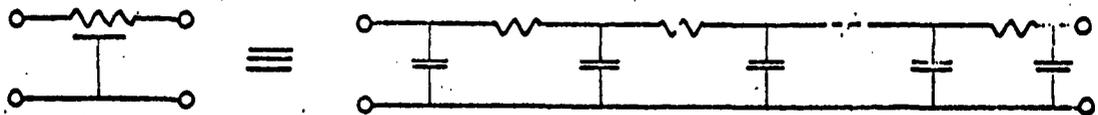
Therefore the network "y" parameters are hyperbolic in nature. The distributed ladder character suggests the addition of a lumped R or C to form a twin "T" characteristic.
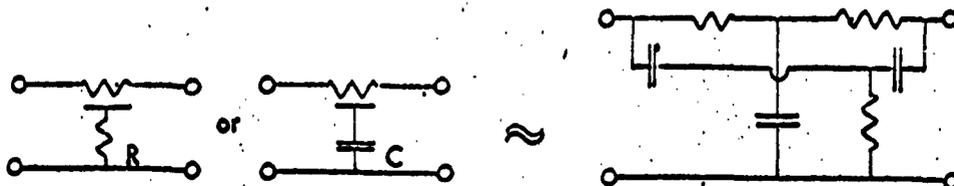
The distributed resistor is essentially a series of perfectly matched RC sections due to the high uniformity of the diffusion process used. Control during manufacture and adjustment of an external R or C should produce a good twin "T" effect without the usual six critical components.

In the analysis to follow the distributed twin "T" is shown to yield a maximum $Q = 0.155K$ where K is the gain of the amplifier used. The lumped twin "T" has a maximum $Q = 0.25K$ – higher than the distributed network but with much greater tolerance problems.

Present experimental work has produced $Q = 7$ at 800kc with predicted $Q = 155$ but further work is needed to show whether the network analysis is faulty or if a non-ideal amplifier can produce such detrimental effects.

DISTRIBUTED TWIN "T" ANALYSIS

The "y" parameters of the distributed resistor are:

$$\mathcal{T} = R_t\, C_t$$
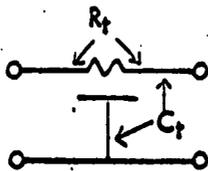
$$y_{ij} = \frac{\sqrt{\mathcal{T}s}}{R_t} \begin{vmatrix} \text{COTH } \sqrt{\mathcal{T}s} & -\text{CSCH } \sqrt{\mathcal{T}s} \\ -\text{CSCH } \sqrt{\mathcal{T}s} & \text{COTH } \sqrt{\mathcal{T}s} \end{vmatrix} \qquad (1)$$

Addition of an external R yields composite "y" parameters
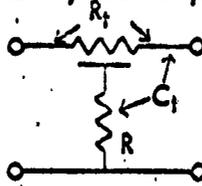
$$y_{11} = y_{22} = \frac{y_{11} + (y_{11}^2 - y_{12}^2)\, R}{1 + 2\,(y_{11} + y_{12})\, R} \qquad (2)$$

$$y_{12} = y_{21} = -\frac{y_{11}^2 - y_{12}^2)\, R - y_{12}}{1 + 2\,(y_{11} + y_{12})\, R} \qquad (3)$$

The short-circuit current or open-circuit voltage transfer ratio is then

$$T = -\frac{y_{21}}{y_{22}} \qquad \frac{(y_{11}^2 - y_{12}^2)\, R - y_{12}}{y_{11} + (y_{11}^2 - y_{12}^2)\, R} \qquad (4)$$

Substituting for the y_{ij} and setting $\mathcal{T}_s = p$

$$T = \frac{\dfrac{p}{R_t^2}\left(COTH^2\sqrt{p} - CSCH^2\sqrt{p}\right)R + \dfrac{\sqrt{p}}{R_t}\,CSCH\sqrt{p}}{\dfrac{p}{R_t^2}\left(COTH^2\sqrt{p} - CSCH^2\sqrt{p}\right)R + \dfrac{\sqrt{p}}{R_t}\,COTH\sqrt{p}} \qquad (5)$$

Eliminating $COTH^2\sqrt{p} - CSCH^2\sqrt{p} = 1$

$$T = \frac{\dfrac{R}{R_t} + \dfrac{CSCH\sqrt{p}}{\sqrt{p}}}{\dfrac{R}{R_t} + \dfrac{COTH\sqrt{p}}{\sqrt{p}}} \qquad (6)$$

Since we expect a twin "T" effect we set the numerator of (6) equal to zero and solve for the natural frequencies:

$$\frac{R}{R_t} + \frac{CSCH\ \sqrt{p}}{\sqrt{p}} = 0 \tag{7}$$

If we let $p = i\omega$, $\sqrt{p} = (1+i)\sqrt{\frac{\omega}{2}}$, and substituting this in (7), we obtain:

$$\frac{R}{R_t} + \frac{1}{(1+i)\sqrt{\frac{\omega}{2}}\ SINH\ \left[(1+i)\sqrt{\frac{\omega}{2}}\right]} = 0 \tag{8}$$

Making the further substitution

$$SINH\left[(1+i)\sqrt{\frac{\omega}{2}}\right] \approx COSH\sqrt{\frac{\omega}{2}} \cdot \left[COS\sqrt{\frac{\omega}{2}} + i\ SIN\sqrt{\frac{\omega}{2}}\right]$$

we can see that $\frac{R}{R_t}$ will be real only if

$$SINH\left[(1+i)\sqrt{\frac{\omega}{2}}\right] = (-1+i)\ COSH\sqrt{\frac{\omega}{2}} \tag{10}$$

The smallest ω meeting this condition is $\omega_c = 2(\frac{3\pi}{4})^2 = 11.12$. The rescaled center frequency is then $\omega_o = 11.12/\tau$.

Solving (8) for the ratio R/R_t yields $R/R_t = 0.0396$ for a zero at the null frequency.

The same basic analysis can be applied to the following networks:

$$\frac{C}{C_t} = 0.0396$$

$$\omega_o = 11.12/\tau$$
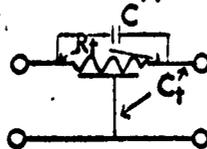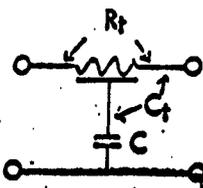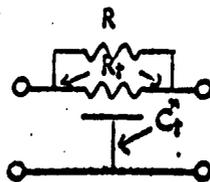
 $\frac{C}{C_t} = 6.3$ $\frac{R}{R_t} = 6.3$ $\omega_o = \frac{30.8}{\tau}$

These analyses apply to the lowest null frequency. Higher frequency nulls exist with different R/R_t or C/C_t.

Expansion about Center Frequency and Estimated Q.

The functions

$$T = \frac{\frac{R}{R_t} + \frac{CSCH \sqrt{p'}}{\sqrt{p'}}}{\frac{R}{R_t} + \frac{COTH \sqrt{p'}}{\sqrt{p'}}} \qquad (6)$$

may be expanded about $\omega_c = 11.12$ (the normalized center frequency) using standard Taylor series techniques. Making the approximation $\frac{\Delta\omega}{\omega_c} \ll 2\sqrt{\frac{2}{\omega_c}}$

$\left(\frac{\Delta\omega}{\omega_c} \ll \frac{8}{3\pi}\right.$ in this case$\left.\right)$, we find

$$T = -\frac{(1+j)\frac{\omega c}{2}}{4\,COS\,\sqrt{\frac{\omega c}{2}}\,\,COSH\sqrt{\frac{\omega c}{2}}\,\left[1 + \frac{R}{R_t}\sqrt{\frac{\omega c}{2}}\,(1+j)\right]} \cdot \frac{\Delta\omega}{\omega_c} \qquad (11)$$

For $R/R_t = 0.0396$ and $\omega_c = 11.12$ in the following configuration,
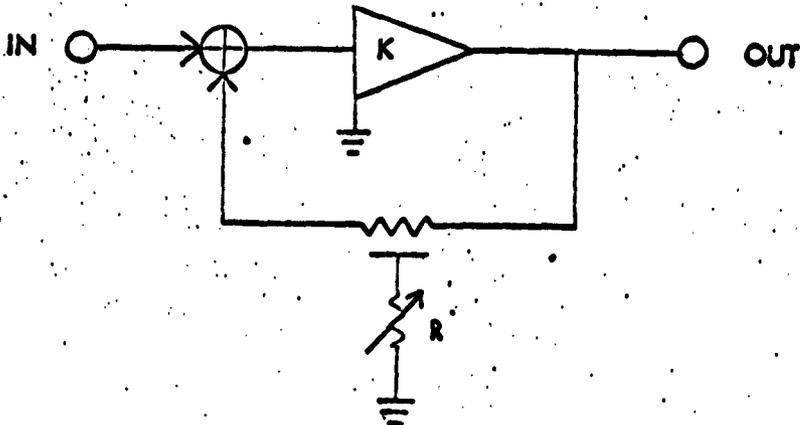
and from (11) the maximum Q = 0.155K. For the lumped twin "T", Q max = 0.25K.

...... work has been done with the dist.

It has been shown [1] that a network requiring a gain K can have its inp-... :put terminals rearranged so that it requires a gain $K' = \dfrac{-K}{1-K}$; i.e., K' can a... unity. A distributed twin "T" was used with the following unit gain circuit develo... by Hamilton.
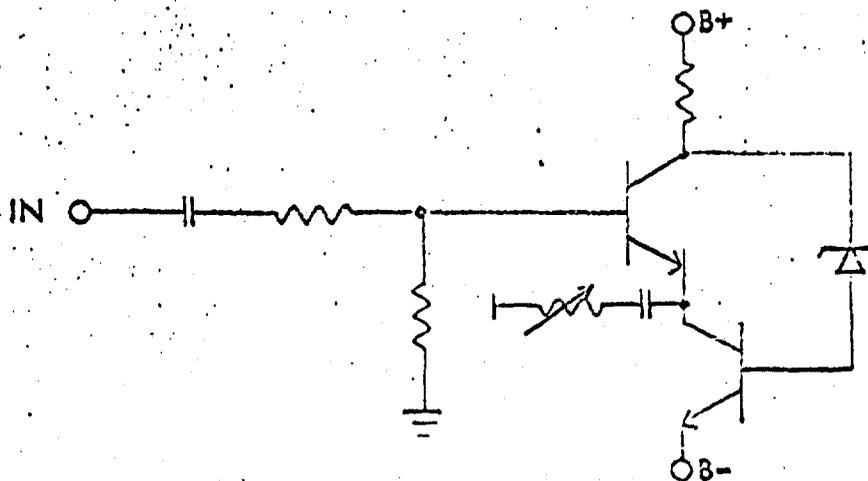
Expected Q was 155 while measured Q = 7 at 800KC. It is not known at th... time whether the amplifier or the network or both are contributing to this anomoly.

CONCLUSIONS

From the limited data available at this time it appears that the distribute... t... "T" may have possibilities for use in bandpass amplifiers. It is easily integratab... to within 5% tolerances and requires tuning only one element. Future investigatio... is expected to yield a method of adjusting the notch frequency. It is hoped that s...me electrical means of adjusting the junction depletion layer may allow precise tur...

1. Hamilton, D.J. & Thompson, J.E.,
   Frequency Selective Amplification for Integrated Circu...
   1, A Particular Class of Lumped Active-RC Networks.