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INTEGRATED SILICON DEVICE TECHNOLOGY

Volume I----Resistance

TECHNICAL DOCUMENTARY REPORT NO. ASD-TDR-63-316, Volume I

June 1963

Electronics Technology Laboratory
Aeronautical Systems Division
Air Force Systems Command
Wright-Patterson Air Force Base, Ohio

Project No. 4159, Task No. 4159-05

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FOREWORD

This report was prepared by the Research Triangle Institute, Durham,
North Carolina on Air Force Contract AF 33(657)-10340, "Design Parameters
and Procedures for Functional Electronic Structures." This work was
administered under the direction of the Electronic Technology Laboratory,
Aeronautical Systems Division. Howard H. Steenbergen was project
engineer for the Laboratory.

The studies presented began in January 1963, were concluded in
April 1963, and were performed by the Solid State Laboratory of the
Research Triangle Institute under the general direction of R. M. Burger.
While R. P. Donovan was the author of this report, the entire technical
staff participated in the compilation of results which represent the
efforts of many organizations and scientists. Specific credits are noted
by reference.

This report is the first volume of a series of reports on Integrated
Silicon Device Technology and is Unclassified.

PREFACE

This series of reports on the design of silicon integrated devices and the processes necessary for their realization is being prepared in an attempt to aid design and process engineers. A silicon integrated device is defined here as a structure formed of a number of distinct elements or regions inseparably associated on or within a continuous body of silicon material. Although original data and calculations are included, a preponderance of the material is obtained from the open literature, ASTIA documents, and personal communications. It is intended that each report be self-contained for the particular device, structure, or process being treated. The variety of techniques available and the dynamic nature of the microelectronic device field insure that this objective will only be approximated. It is requested that omissions, errors, and new information be brought to our attention. A partial listing of reports which are planned for this series is given below. Any information which can be made available for inclusion in these reports will be appreciated.

Planned reports in the Integrated Silicon Device Technology series:

Resistance	Bipolar Transistors
Capacitance	Unipolar Transistors
Diodes	Design and Material Parameters
Diffusion	Topological Design
Epitaxy	Interconnection Techniques
Oxidation	Reliability
Photoengraving	Thermal Design and Encapsulation

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Abstract

Both conventional and unconventional methods of achieving the
resistive function in integrated silicon devices are discussed in this
report. The properties and types of resistors made of silicon are
considered in some detail as well as general design procedures. Many
charts and graphs are reproduced in the hope of providing a convenient
source of information pertinent to the design of resistors for
integrated silicon devices.

The more recent trend toward combining thin film passive components
on a silicon substrate containing the active elements is discussed in
less detail, not because this technique is felt to be less important
but because information is sparse on such devices and their fabrication.

From the assembled data, the following conclusions are drawn:

1. The diffused silicon resistor is currently the most popular
    type of integrated silicon resistor but has a relatively poor
    TCR and introduces unwanted capacitances into the equivalent
    circuit of the device.

2. The thin-film resistor on an oxidized silicon substrate requires
    more processing steps but appears to combine the best attributes
    of the thin-film technology with the best of the planar silicon
    technology to form a combination superior to either one alone.

3. At their present stage of development, neither of these types
    of resistors possesses all the properties desired of integrated
    circuit resistors. The limitations are fundamental and the
    development of a new type of resistor, such as an element
    utilizing the reverse resistance of a p-n junction, seems
    desirable.

4. A re-examination of circuit functions in an effort to reduce
    the required resistor performance or to eliminate resistors
    completely seems justified in light of the silicon planar tech-
    nology.

5. The concept of molecular electronics in which circuits are
    designed from material parameters seems superior to the
    technique of fabricating a series of conventional circuit
    elements which must be isolated and coupled according to a
    conventional schematic. More research in this area is
    required before practical structures will be available.

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1. INTRODUCTION

The purpose of this report is to review the techniques that have been used to build resistors into functional electronic blocks and to present the design and performance data of these resistors in a single reference. The techniques considered will be limited to those that are compatible with the integrated circuits of silicon planar technology. Only two general types of resistors meet this restriction - the silicon resistor and the thin-film resistor deposited on silicon dioxide covering a silicon substrate. These resistors are discussed in Sections 2 and 3, respectively, and general design considerations, applicable to both types of resistors, are covered in Section 4.

During the preparation of this report, a number of silicon integrated structures were available. Those on which descriptive information was provided utilized silicon diffused resistors almost exclusively. Announcements of the laboratory demonstration of thin film resistors on silicon substrates were, however, so plentiful that momentary commercial announcement was expected. Care must be taken in analyzing this trend because of the various factors involved. Experience with silicon resistors has revealed techniques for avoiding their detrimental temperature variation and their limited range of values. New circuit techniques are rapidly being developed which take advantage of the inverted economics of active and passive components in integrated devices. The all-silicon structure in which only the interconnections (and passivation) are accomplished by materials other than silicon possesses the advantages of simplicity and proven operational success. Thus, while the several techniques described in this report are being examined, care must be taken to evaluate in one's own mind the relative merits of each and, above all, the economic and fabricational practicality of suggested modifications of the integrated silicon structure.

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2. SILICON RESISTORS

Types of silicon resistors, their properties and design are discussed in this section.

An imperative property of any resistor used in integrated circuitry is that its fabrication be compatible with the fabrication of all other elements on the same block. No degradation of other components is tolerable. A very desirable property is that its fabrication require no processing additional to that required in the fabrication of the active elements of the circuit. Resistors made of silicon seem ideally suited to meet this requirement. For example, a conventional planar transistor can be built on an n-type substrate in two diffusion steps and one evaporation step (to provide metallic contacts). A typical cross section appears in Figure 2-1 along with the conventional schematic representation.

(a.)   (b.)
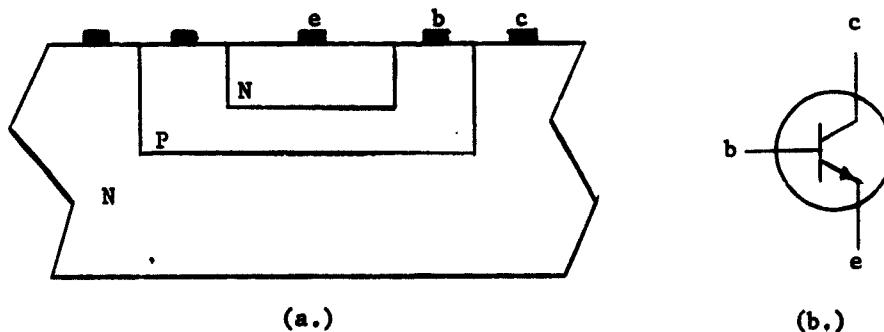
Fig. 2-1. A Conventional Planar n-p-n Transistor (collector contact is on top surface).
  (a) Cross-section
  (b) Schematic

The same processing steps can also build a transistor with a collector resistor by adding one ohmic contact as shown in Figure 2-2. The resistance of the bulk silicon between terminal B^+ and c consitutes the R_c of the schematic.
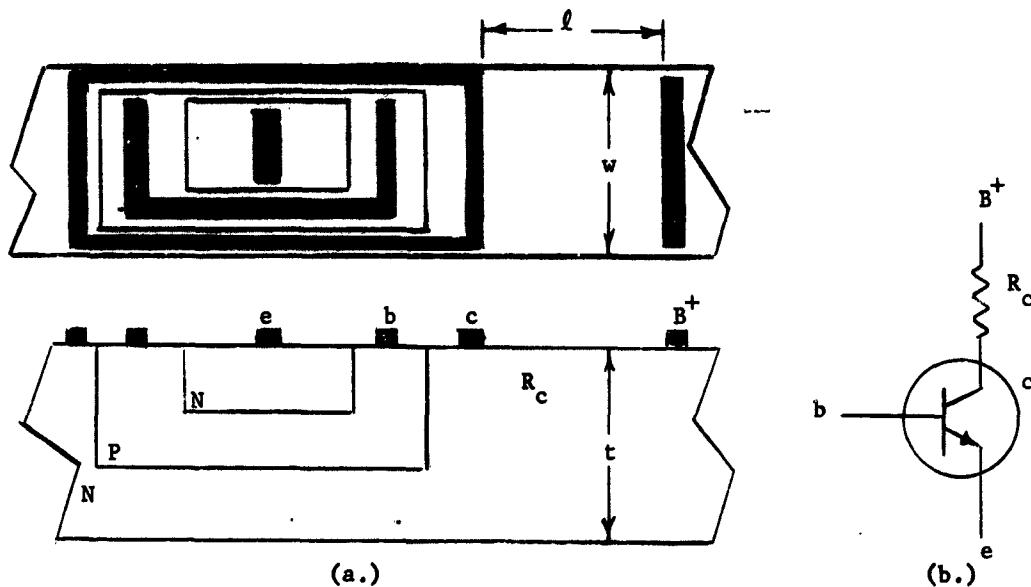
Fig. 2-2. Monolithic Planar n-p-n Transistor and Collector Resistor
(a) Cross-section
(b) Schematic

The addition of the extra contact in Figure 2-2 involves only the exchange of one or two processing masks from those used to fabricate the transistor of Figure 2-1 and requires no extra steps. Although this illustration is of one particular type of silicon resistor, the advantage of little or no additional labor is characteristic of all silicon resistors when used in functional electronic blocks.

2.1 Variables Determining Resistivity

The various environmental factors and material properties which determine the resistivity of silicon are discussed in this section.

The value of the resistor R_c, shown in Figure 2-2, is determined by its geometry and its resistivity as shown in Equation (2.1)

$$R_c = \frac{\rho \ell}{wt}, \quad \ell \gg t \ .$$

(2.1)

where ℓ, w, t are the dimensions shown in Figure 2-2 and ρ is the resistivity. The resistivity, based on a two carrier model, can be calculated from Equation (2.2)

$$\rho = \frac{1}{nq\mu_n + pq\mu_p} \tag{2.2}$$

n = electron concentration (cm^{-3})

p = hole concentration (cm^{-3})

q = electronic charge = 1.6×10^{-19} coulombs

μ_n = electron mobility

μ_p = hole mobility $\qquad (\frac{cm^2}{volt\text{-}sec})$

Any parameter which changes the value of any of these quantities also changes the value of resistivity as given by Equation (2.2).

2.1.1 Impurity Concentration*

A distinctive feature of semiconductors is the extreme sensitivity of resistivity to impurity concentration. Theory cannot satisfactorily predict this dependence because the mobility factor in Equation (2.2) is itself a complex function of impurity concentration and structure and is not fully understood. Experimental measurements and empirical calculations of resistivity vs impurity concentrations are combined in Figure 2-3. The data for impurity concentrations greater than 10^{14} are taken from Irvin [1] and data for concentrations less than 10^{14} are computed from Equation (2.2) where n is set equal to the donor impurity concentration, p is set equal to the acceptor impurity concentration and the mobilities are assumed to be the constants [2]:

$$\mu_n = 1350 \ \frac{cm^2}{volt\text{-}sec} \ ,$$

$$\mu_p = 480 \ \frac{cm^2}{volt\text{-}sec} \ .$$

There is a slight mismatch at 10^{14} where the two portions of the curves join.

*   All concentrations are expressed in cm^{-3}.
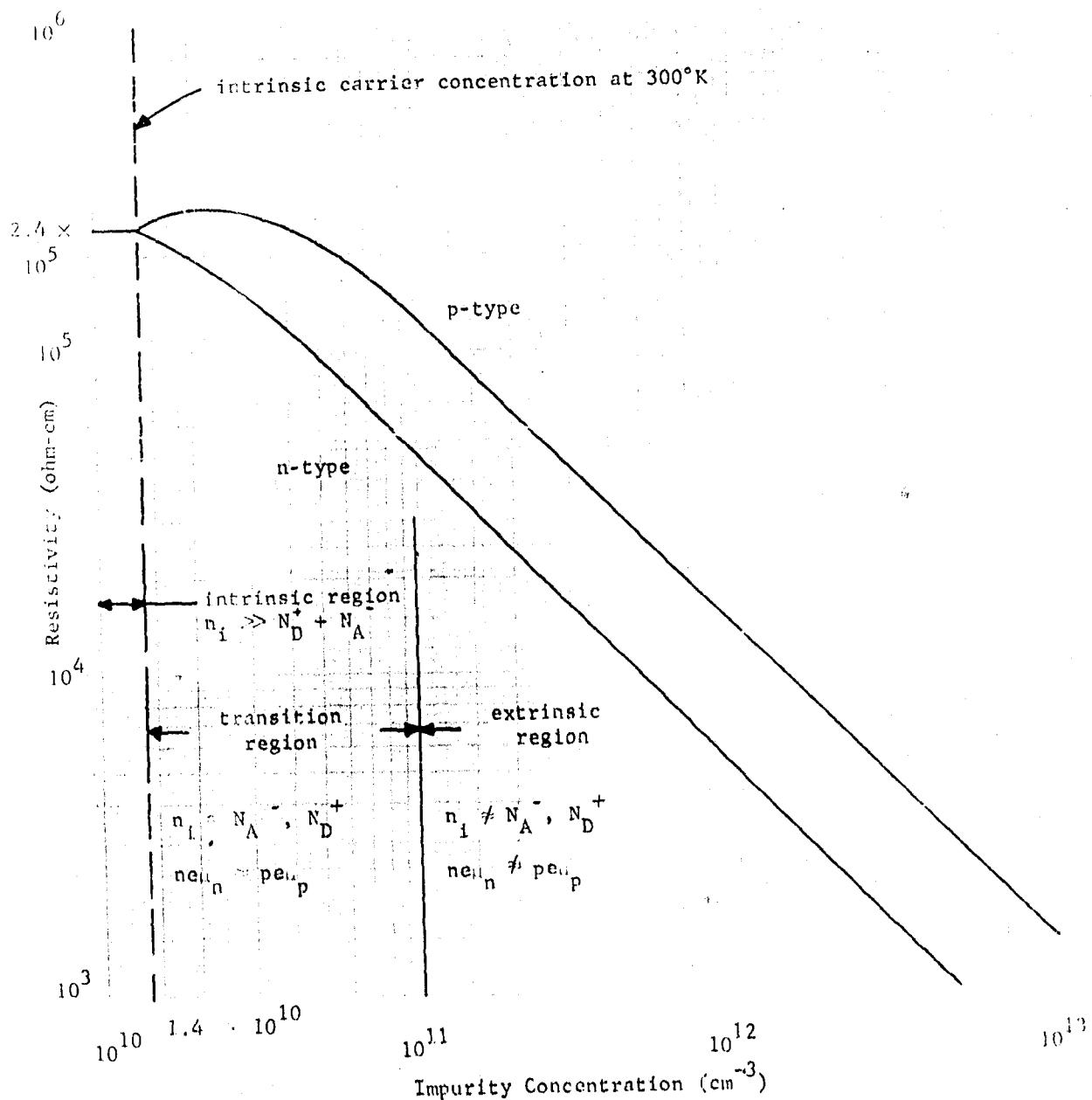
Fig. 2-3. Resistivity of Silicon at 300°K as a Function of Impurity Concentration.
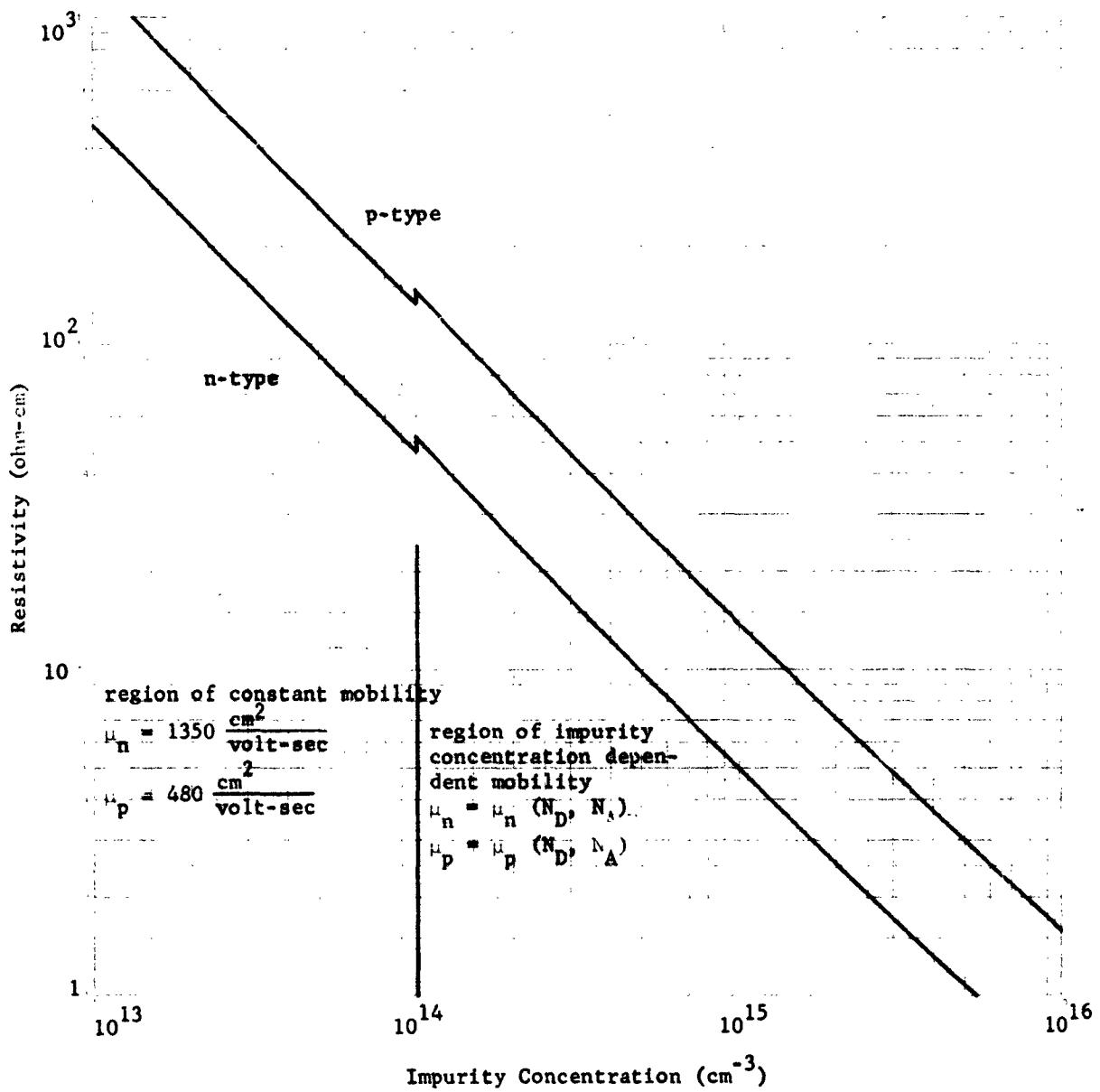
Fig. 2-3. (Continued)
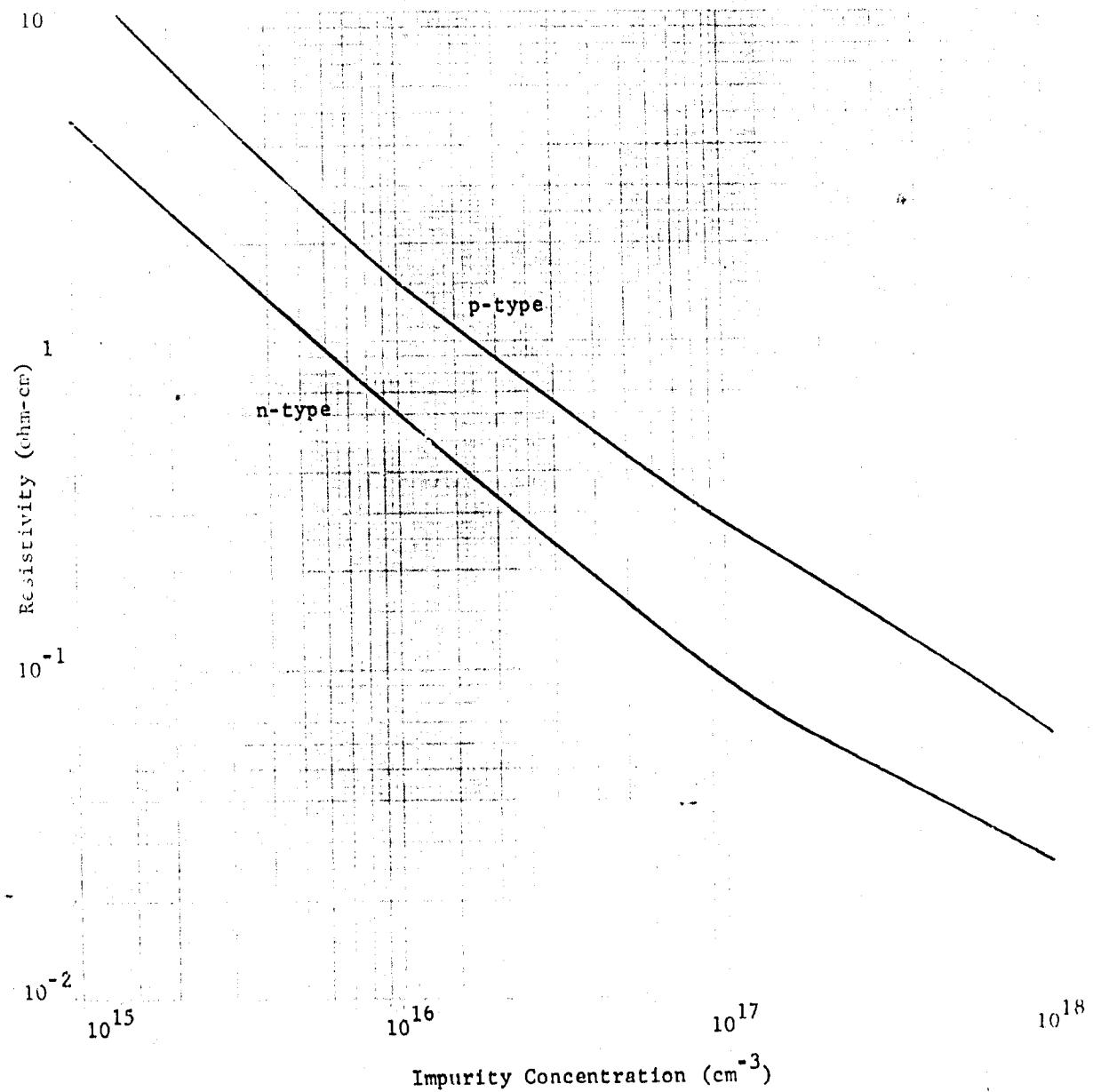
Fig. 2-3. (Continued)
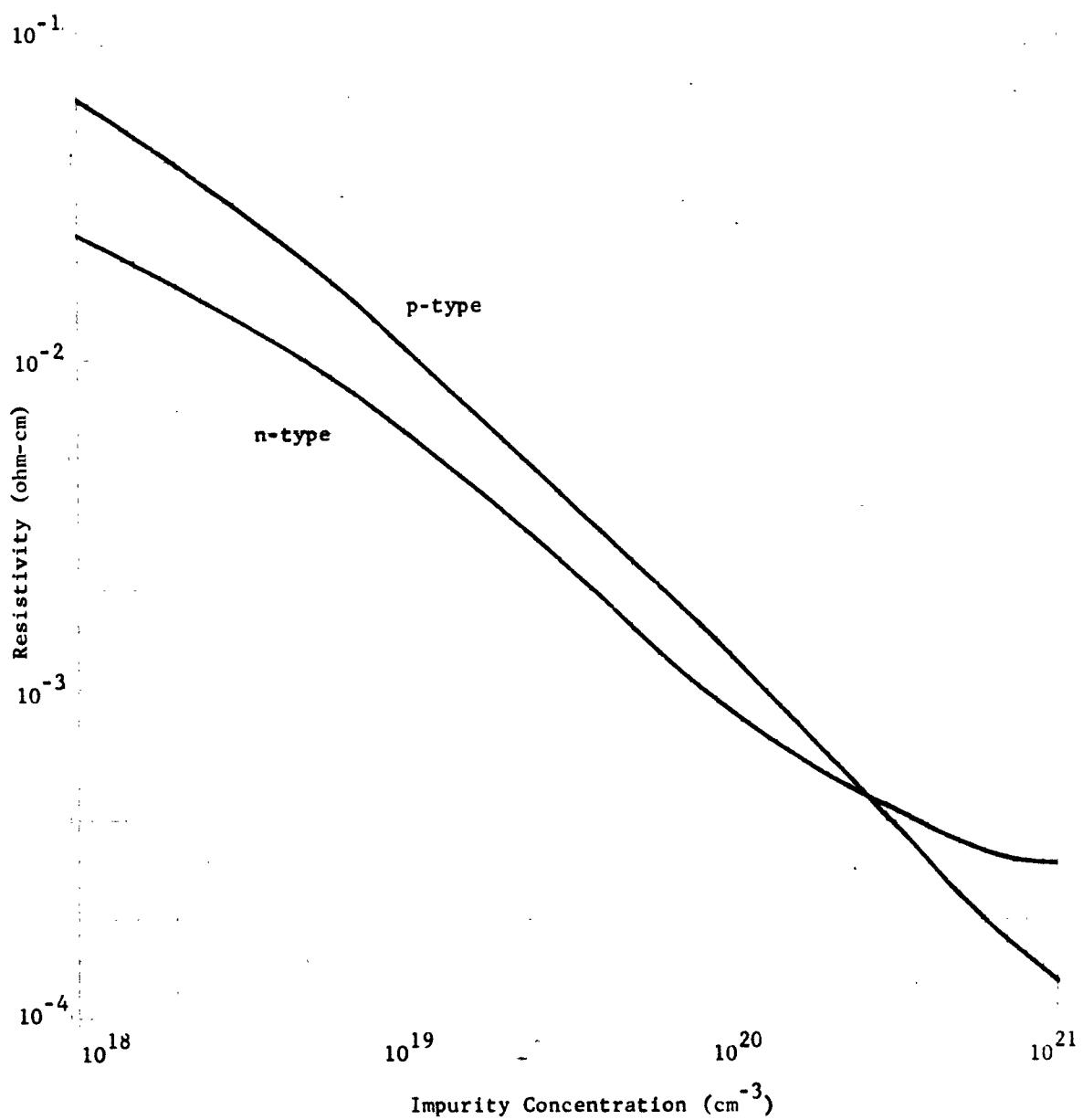
Fig. 2-3. (Continued)

The dashed line at 1.4×10^{10} in Figure 2-3 represents the concentrations of intrinsic carriers at T = 300°K as calculated from Equation (2.3) [3]

$$n_i^2 = 1.5 \times 10^{33} \ T^3 \ \exp \ (- \frac{1.21 ev}{kT}) \ \text{°K}^{-3} \ \text{cm}^{-6} \ . \tag{2.3}$$

The transition from impurity conduction to intrinsic conduction is the transition from a one carrier mode of conduction to a two carrier mode. The curve near the intrinsic region was computed from Equations (2.2), (2.3), and (2.4)

$$np = n_i^2 \ . \tag{2.4}$$

The curves in Figure 2-3 can be classified into regions according to the carrier concentration (intrinsic, two carrier-extrinsic, and one carrier-extrinsic regions) and mobility (constant mobility and an impurity dependent mobility region). All these regions are indicated in the figure.

The minority carrier concentration has been neglected in all regions of Figure 2-3 except in the transition region.

2.1.2 Temperature

The energy band description of silicon predicts an exponential dependence of carrier concentration upon reciprocal temperature in both the high temperature, intrinsic region and, for certain impurity concentrations, the low temperature, extrinsic region (below 77°K). Between the two temperature extremes lies a region of constant carrier concentration. Resistivity is not constant in this region, because the mobility is temperature dependent. Figures 2-4 and 2-5 are semi-log plots of resistivity vs $\frac{1}{T}$ for various impurity concentrations. The exponential dependence in the intrinsic region is clearly seen but the low temperature exponential regions are not shown. The data are taken from Morin and Maita [4], Pearson and Bardeen [5], Hoffman et al [6], Ioffe and Regel [7], Long [8], and Paul and Pearson [9]. The dashed curves in both figures are the
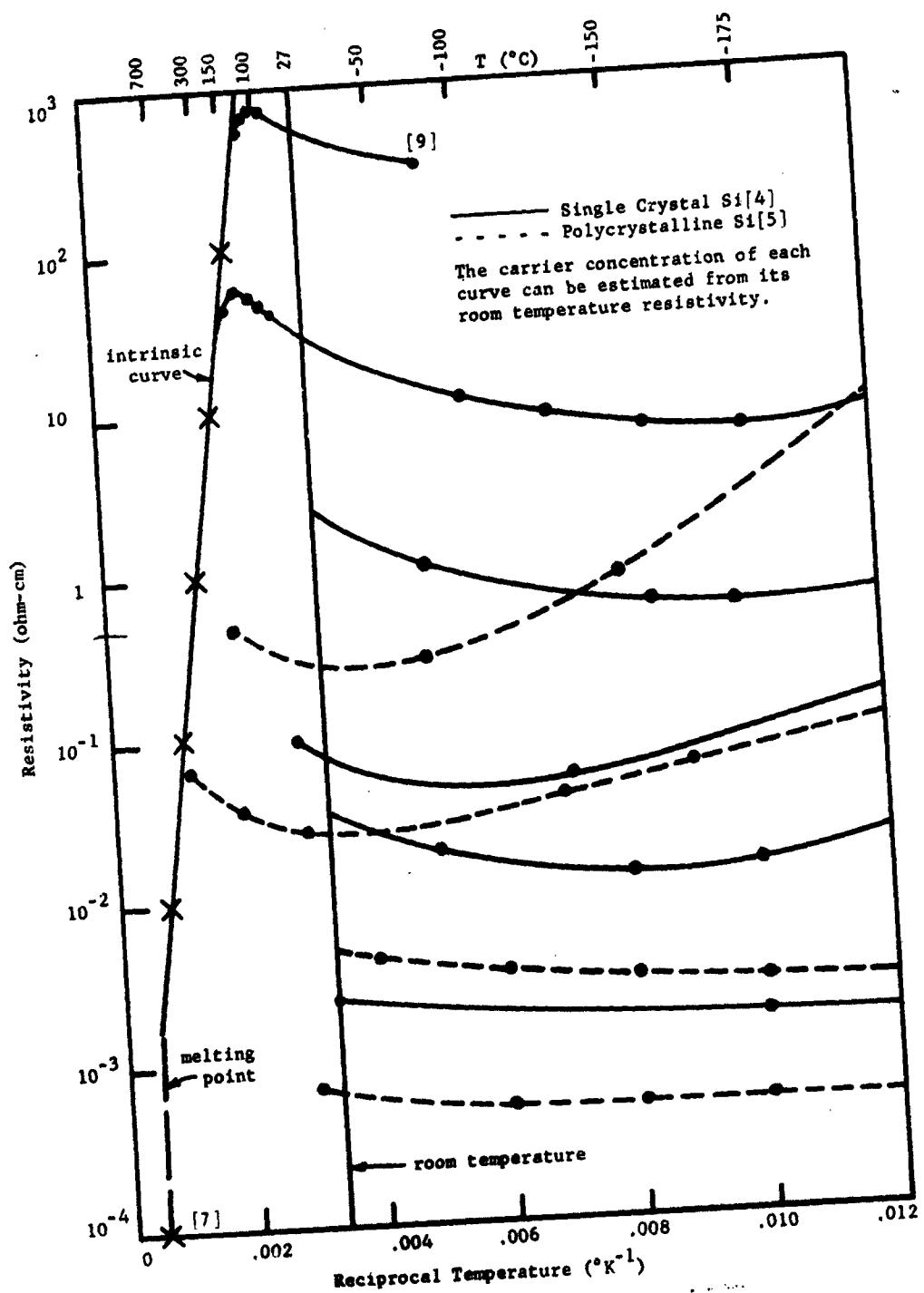
Fig. 2-4. The Temperature Dependence of Resistivity for n-type Si
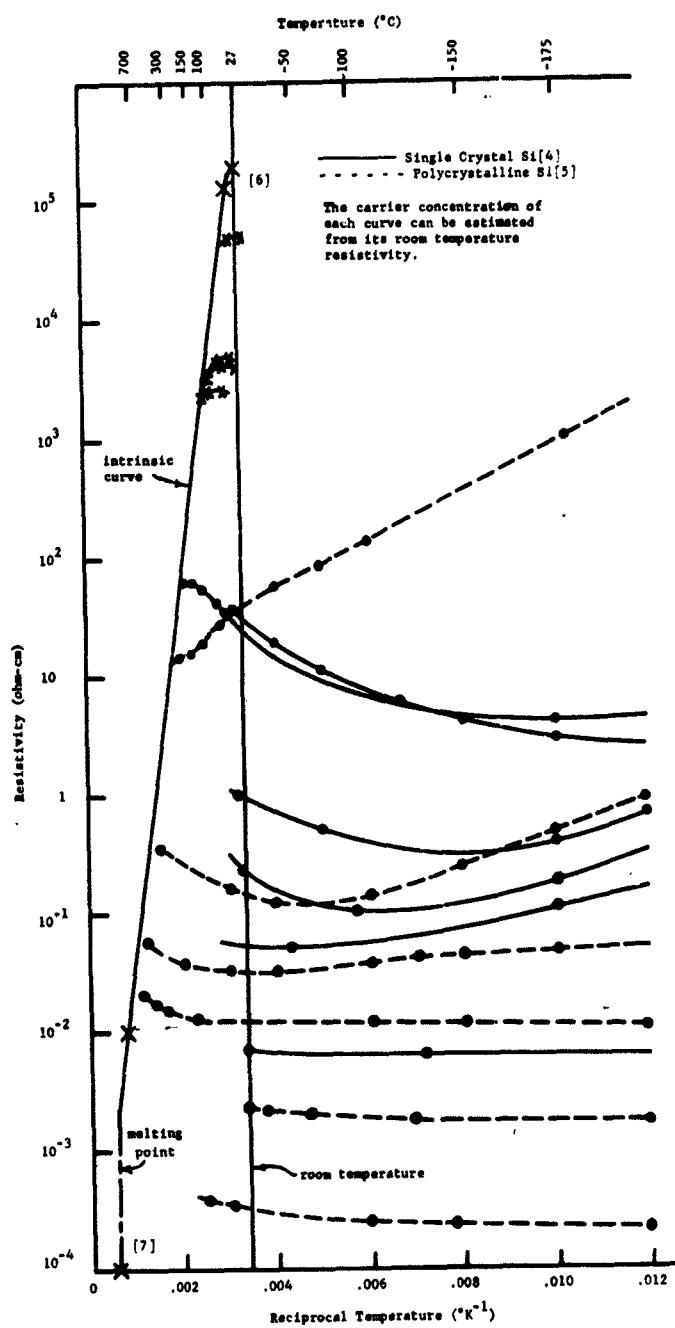
Fig. 2-5. Temperature Dependence of Resistivity for p-type Silicon

early measurements of Pearson and Bardeen which were taken on polycrystalline samples; all other data were taken on single crystal samples except for the measurements on liquid silicon reported by Ioffe. At high impurity concentration there is good agreement between the single and polycrystalline measurements; but as the concentration decreases, a pronounced difference appears.

2.1.3 Structural Defects

As noted in 2.1.2, Figures 2-4 and 2-5 illustrate a dependence of resistivity upon crystalline structure. Other structural imperfections also influence resistivity; although few quantitative measurements from which general relationships can be deduced exist for silicon. Dislocations have been studied experimentally in n-type germanium [10] and found to change the room temperature resistivity by an order of magnitude. In p-type germanium, dislocations have no effect. In this experiment the dislocations were introduced by plastic deformation and a model of dislocation-introduced acceptor levels verified. No comparable data exist for silicon but similar qualitative behavior is reasonable; that is, dislocations probably introduce energy levels into the forbidden gap.

2.1.4 Thermal History

Heat treatment of silicon has been found to increase the concentration of conduction band electrons [11] [12] as shown in Figure 2-6. These data show the effect of prolonged heating at 430°C, followed by heating at 590°C. The added n-type doping has been related to the oxygen content of rotated, pulled crystals. Float zone silicon generally has insufficient oxygen content to exhibit similar behavior [13], although conversion of p-type surfaces under a layer of SiO_2 has been reported [14] during the fabrication of planar structures. Floating zone silicon, after heating in oxygen at 1385°C for 91 hours, shows the added donor concentration in the surface layers where the oxygen content is quite high as shown in Figure 2-7. In the planar process this source of doping may be important.
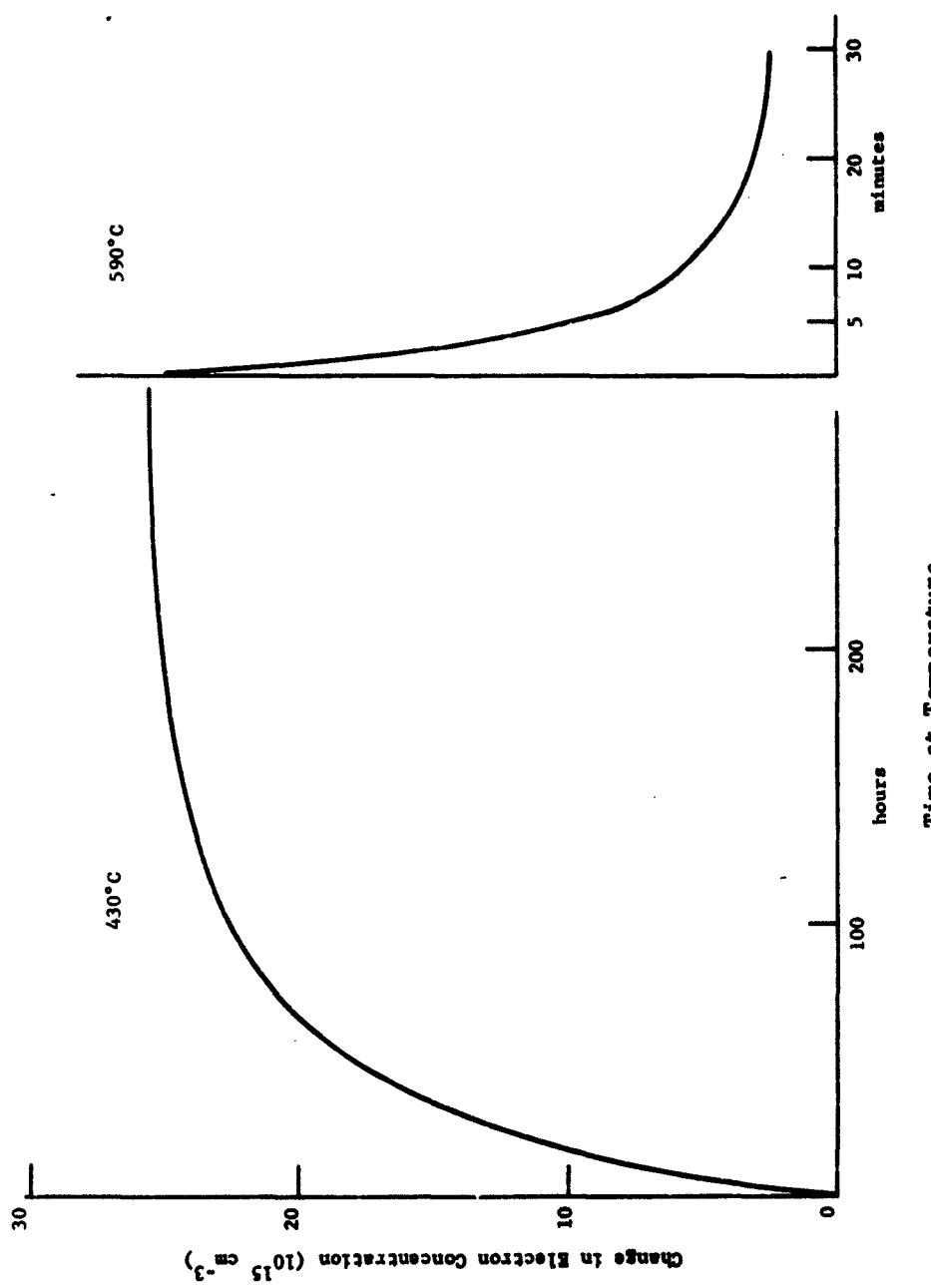
Fig. 2-6. Effect of Heating on Electron Concentration [11]
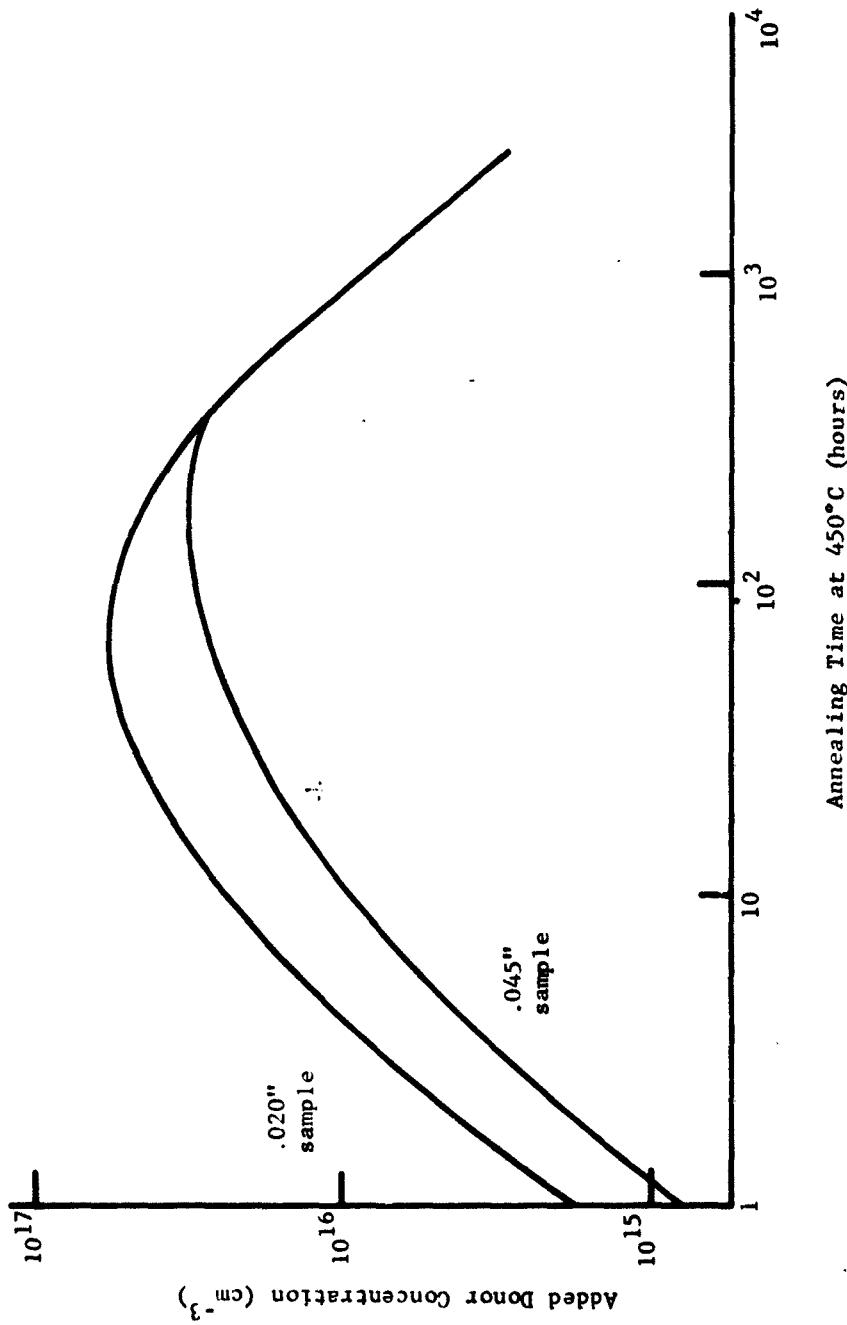
Fig. 2-7. Effect of Annealing for Samples of Floating Zone Silicon Heated in O_2 for 91 Hours at 1385°C. [13]

2.1.5 Surface and Environment

In electrical measurements of insulators and semiconductors, the observations are affected by thin surface films, the composition and resistivity of which depend on the surrounding atmosphere. Measurements of the surface resistivity of chemically prepared surfaces [15], of ion-bombarded surfaces [16], and of thermally oxidized surfaces [17] have been made as a function of environment or surface charge. Representative data appear in Figures 2-8 and 2-9. In these curves the contribution to the conductivity of a surface layer, isolated from the bulk by a space charge layer, is plotted as a function of surface condition. This conductivity change is given by:

$$\Delta\sigma_s = q\mu_n \text{ (eff) } \Delta n + q\mu_p \text{ (eff) } \Delta p = \frac{1}{\Delta\rho_s} \quad , \qquad (2.5)$$

where Δn and Δp represent the added carrier concentrations in this isolated surface layer and μ_n(eff) and μ_p(eff) the effective carrier mobilities in that layer [18]. Curve A of Figure 2-8 indicates the chemical treatment used to produce a given surface potential on an etched surface. Curve B shows data in which the chemical potential is built into an oxide layer. Subsequent chemical treatments do not produce measurable changes in the surface chemical potential of B. Figure 2-9 shows the relationship between surface conductivity and the fraction of the surface covered with hydrogen atoms. These data differ in that an attempt has been made to start with an atomically clean surface and measure the changes introduced by known quantities of specific atoms.

2.1.6 Orientation

The anisotropy of the energy bands of silicon predicts a dependence of resistivity upon orientation. In general no such dependence has been observed at room temperature and pressure and it can be ignored.

2.1.7 Electric Field

Two mechanisms cause a dependence of resistivity upon electric field. The first results from a reduction in mobility caused by
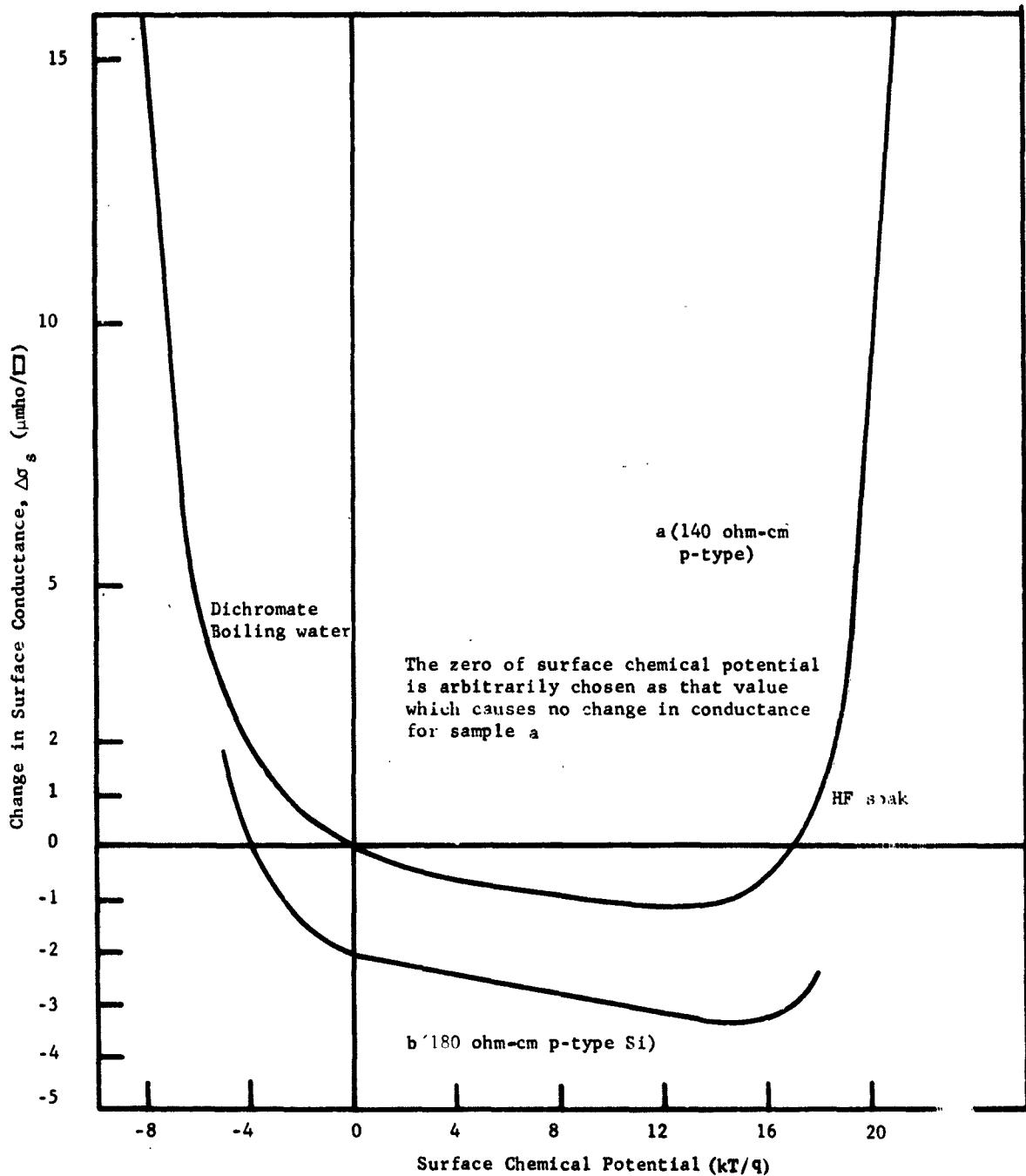
Fig. 2-8. The Effect of Surface Chemical Potential on Surface Conductance
    (a) Etched Surface [15]
    (b) Thermally Oxidized Surface [17]
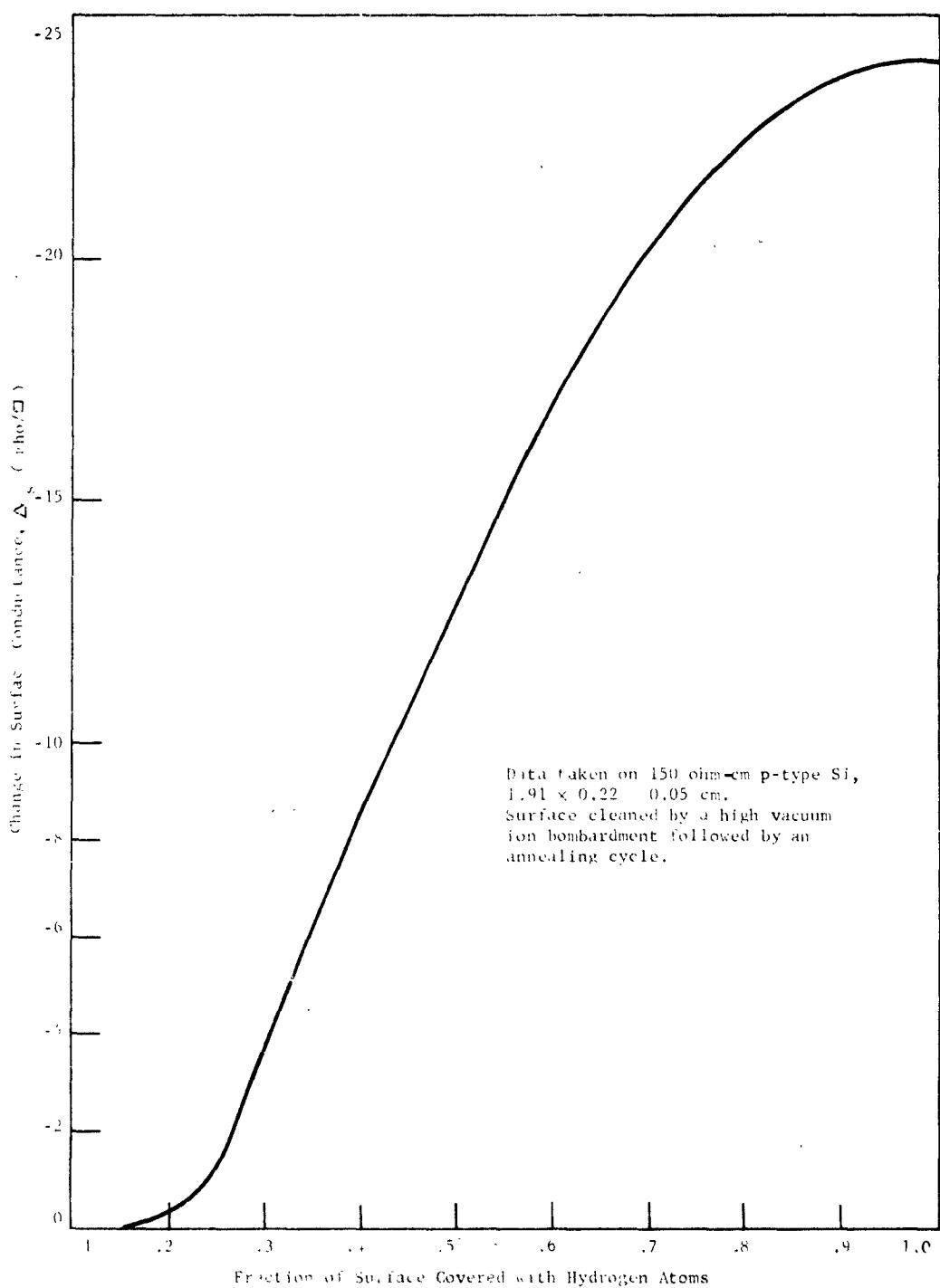
Fig. 2-9. **The Effect of Hydrogen Adsorption on Surface Conductance** [16]

increased phonon scattering [19]; the second is the increase in carrier
density caused by impact ionization. Figure 2-10 shows the increase in
resistivity as a function of applied field. This is the region of
decreasing mobility. At field strengths of about 2×10^4 volts/cm
impact ionizations begin to be effective [20]. The value of field at
which ionization of impurity levels becomes important depends upon
impurity type and concentration and has not been fully determined.

2.1.8 Magnetic Field

The dependence of resistivity on magnetic field strength varies
with orientation and with the angle between the direction of the magnetic
field and the direction of the current density. Figure 2-11 summarizes
data taken on n-type Si of different zero field resistivities [23]. The
change is small and only in special applications would the presence of
a magnetic field be a major factor in the value of resistivity.

2.1.9 Pressure

The dependence of resistivity on pressure for two different samples
of n-type Si is shown in Figure 2-12. The high pressure transition [24]
of Curve B looks similar to that reported by Ioffe [7] for the transition
from solid to liquid silicon as shown in Figures 2-4 and 2-5. The
lower pressure data are from Pearson and Paul [9]. Again for all normal
operating pressures the change in resistivity is negligible.

2.1.10 Incident Radiation

The resistivity of silicon is sensitive to incident radiation by
either photons or particles. Incident photons with energies exceeding
the energy band gap create hole-electron pairs. These added free carrier
densities change the resistivity. For silicon, the threshold is at a
wavelength of approximately 1.1 microns. Silicon is transparent to
photons with longer wavelengths. Due to the variety of spectral distri-
butions in light sources and the difficulty in characterizing the optical
properties of silicon surfaces, it is not practical to make assumptions
about the photon flux in a given environment. If, however, it is
assumed that f electron-hole pairs are produced per second in a unit
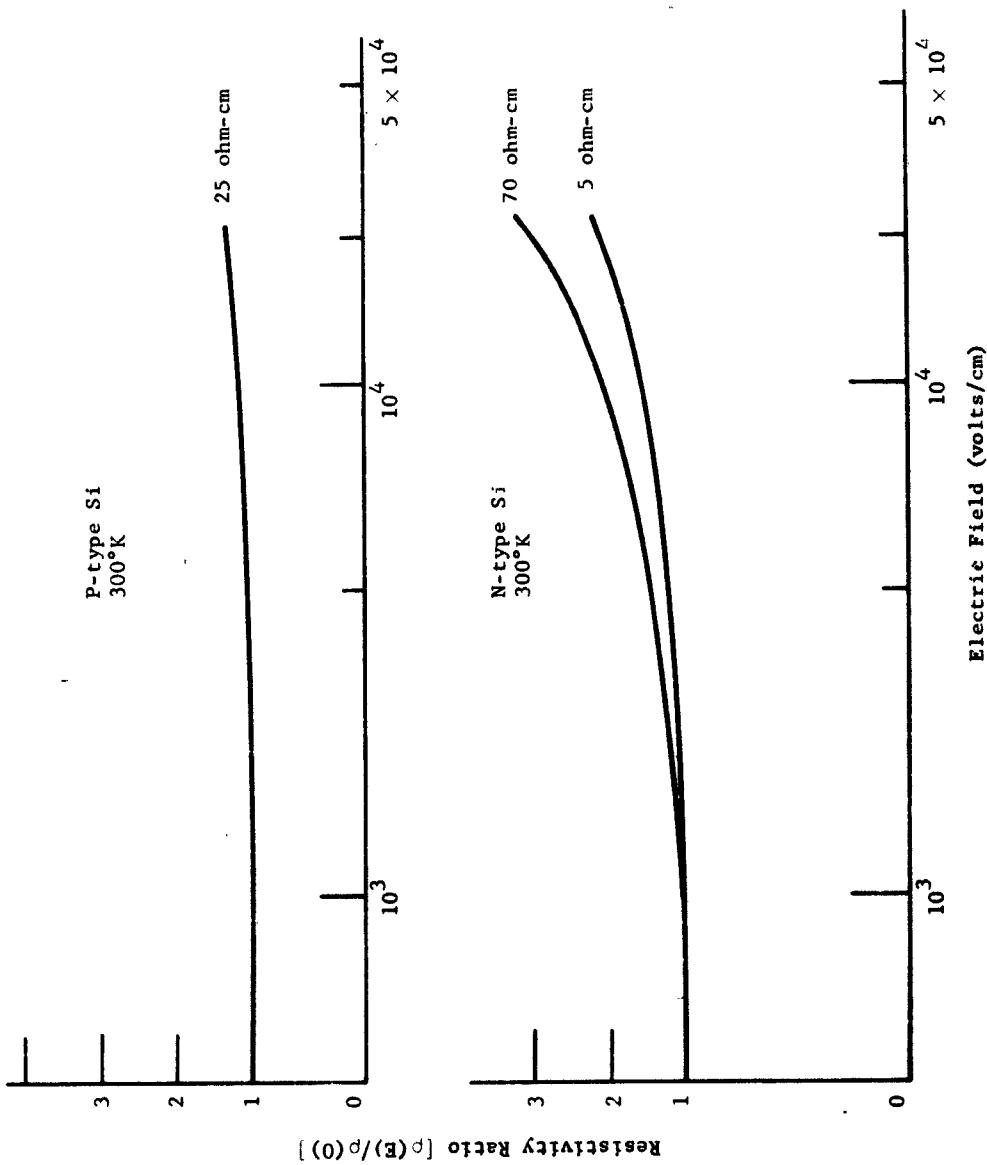
Fig. 2-10. Electric Field Dependence of Resistivity [21] [22]
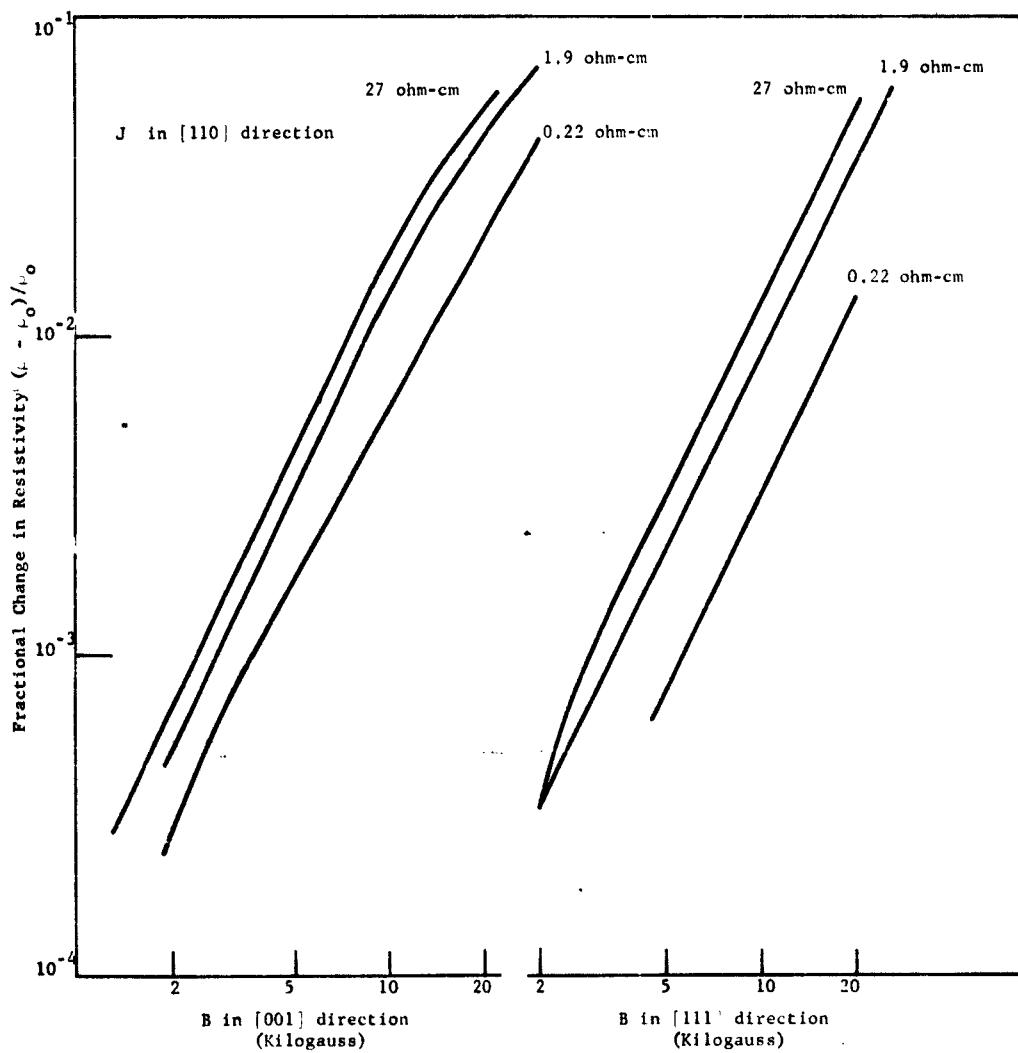
Fig. 2-11. Magnetoresistance of n-type Silicon at 300°K [23]
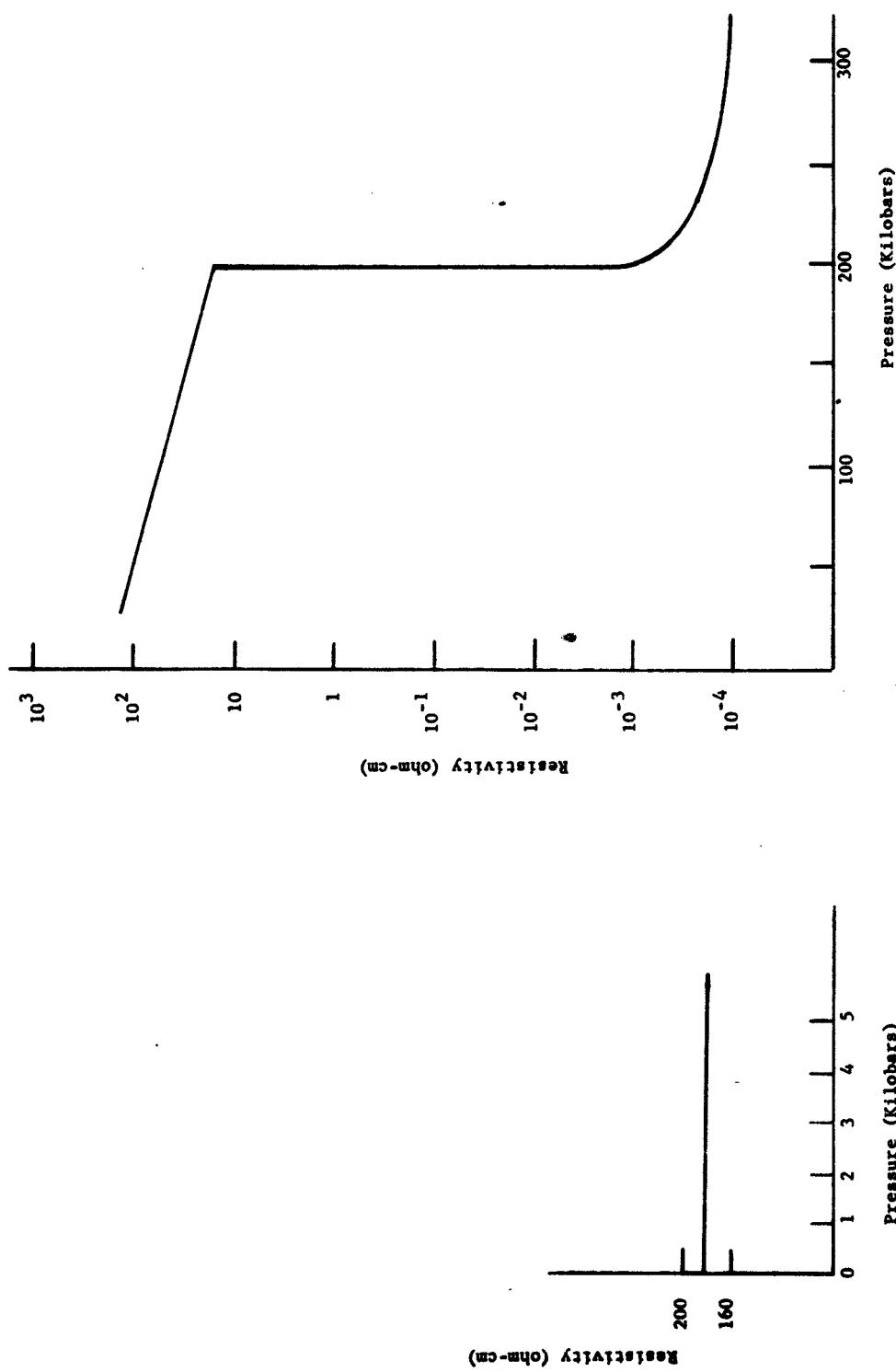
Fig. 2-12.   Pressure Dependence of the Resistivity of Silicon

volume by irradiation, then the increase in the carrier densities is:

$$\Delta n = \Delta p = f\tau, \qquad (2.6)$$

where τ is the effective lifetime which in silicon is 10^{-3} to 10^{-7} seconds [25]. The resulting change in conductivity is

$$\Delta\sigma = qf\tau \ (\mu_n + \mu_p). \qquad (2.7)$$

This increase in conductivity may be difficult to observe in heavily doped materials such as the surface of a diffused wafer. In higher resistivity regions the change can be large.

High energy particle irradiation may produce a similar conductivity modulation in the absence of permanent damage. The number of ionized pairs due to charged particle irradiation can be determined from the experimental relationship [26]

$$N = \frac{E}{3.6} \times 10^6, \qquad (2.8)$$

where

N is the number of hole-electron pairs,
E is the incident particle energy in Mev.

Since excess carriers disappear due to recombination, mainly by capture at defect energy levels, there is no permanent material damage due to ionization.

The displacement of atoms due to direct interaction of the incident particle with nuclei does result in permanent damage. The extent of this damage depends upon the nature and energy of the incident particle and the energy required to remove an atom from its lattice site. It is convenient to characterize permanent damage in terms of the energy density of the incident radiation.

An effect due to permanent damage is shown in Figure 2-13 where
bombardment of 7 ohm-cm n-type silicon samples at 60°C by 700 kev
electrons resulted in a change in resistivity which has been charac-
terized by the fraction of carriers removed due to defect energy
levels [27]. These energy levels are associated with the diffusion
and trapping of vacancies created by the incident radiation. The data
in Figure 2-13 also characterize the bombardment of 5 ohm-cm p-type
silicon at 60°C by 700 kev electrons. Since the initial hole concen-
tration is 3.5 times the initial electron concentration, the coincidence
of the curves in Figure 2-13 indicates that the rate of hole removal in
the p-type crystal is 3.5 times the rate of electron removal in the
n-type crystal for this particular radiation environment. From these
curves one can find the rate of hole or electron removal as a function
of bombardment. Assuming the mobility remains constant, the increase
in resistivity for an integrated bombardment can be calculated.

Another method for inducing radiation damage in silicon is
exposure of the sample to a neutron flux [28]. A general characteri-
zation for neutron radiation is shown in Figure 2-14 where the resistivity
of both n- and p-type silicon rapidly approaches that of intrinsic silicon.
From the shape of the curve one would suspect that carrier removal due to
neutron irradiation is at least a few orders of magnitude larger than
that due to equal integrated electron bombardment.

In this discussion only two types of irradiation have been consider-
ed; however, in general, all types of radiation tend to increase resistiv-
ity and reduce carrier lifetime. In addition there is some evidence
that radiation damage in silicon is not dependent upon the rate of
bombardment but is more sensitive to the integrated bombardment.

2.2 Types of Silicon Resistors

The various types of silicon resistors and their properties are
discussed in this section.

Resistors are easy to fabricate in silicon as illustrated by R_c
in Figure 2-2. The quality of a silicon resistor used in integrated
circuitry or functional electronic blocks must be determined not only
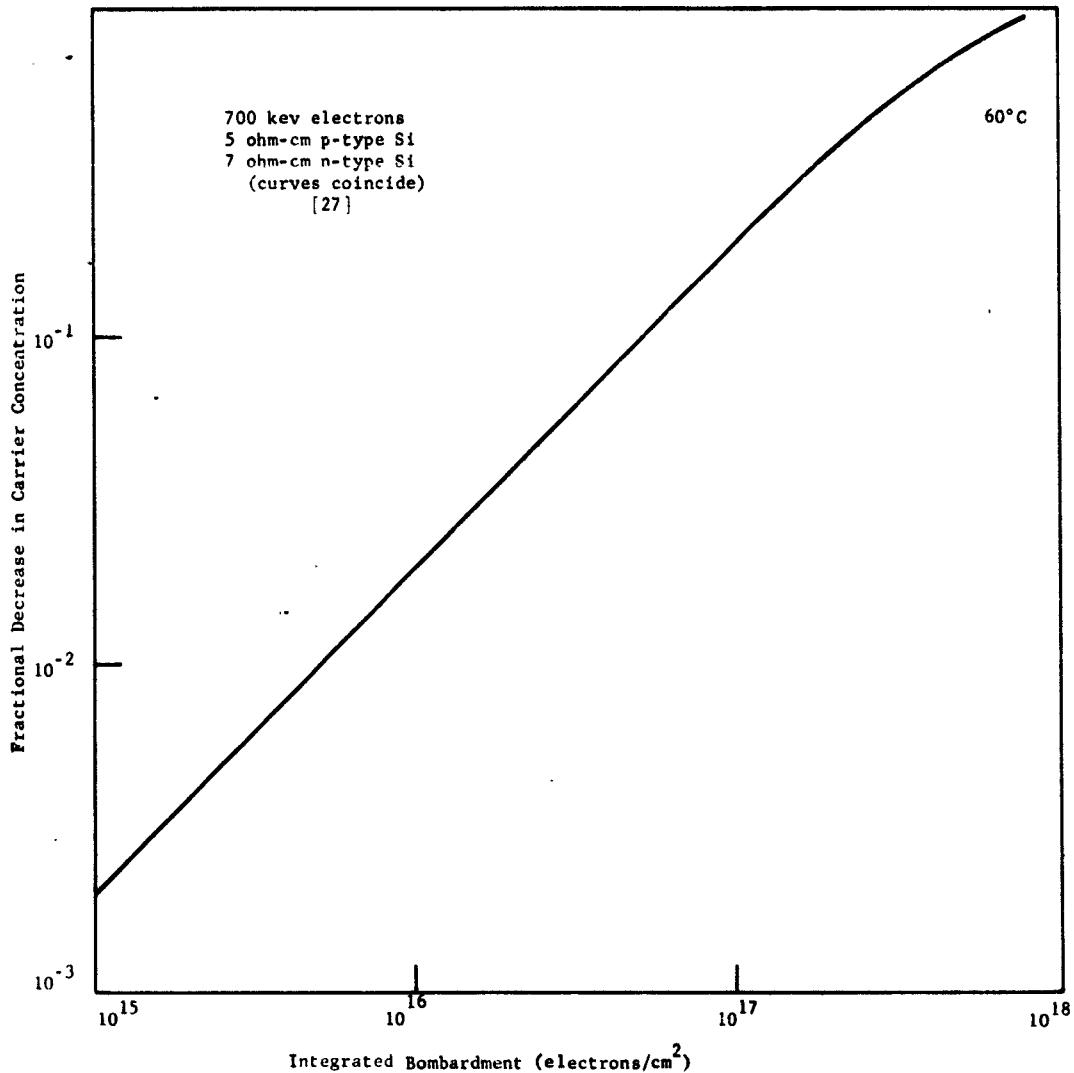
Fig. 2-13. Effect of Electron Bombardment on Carrier Concentration
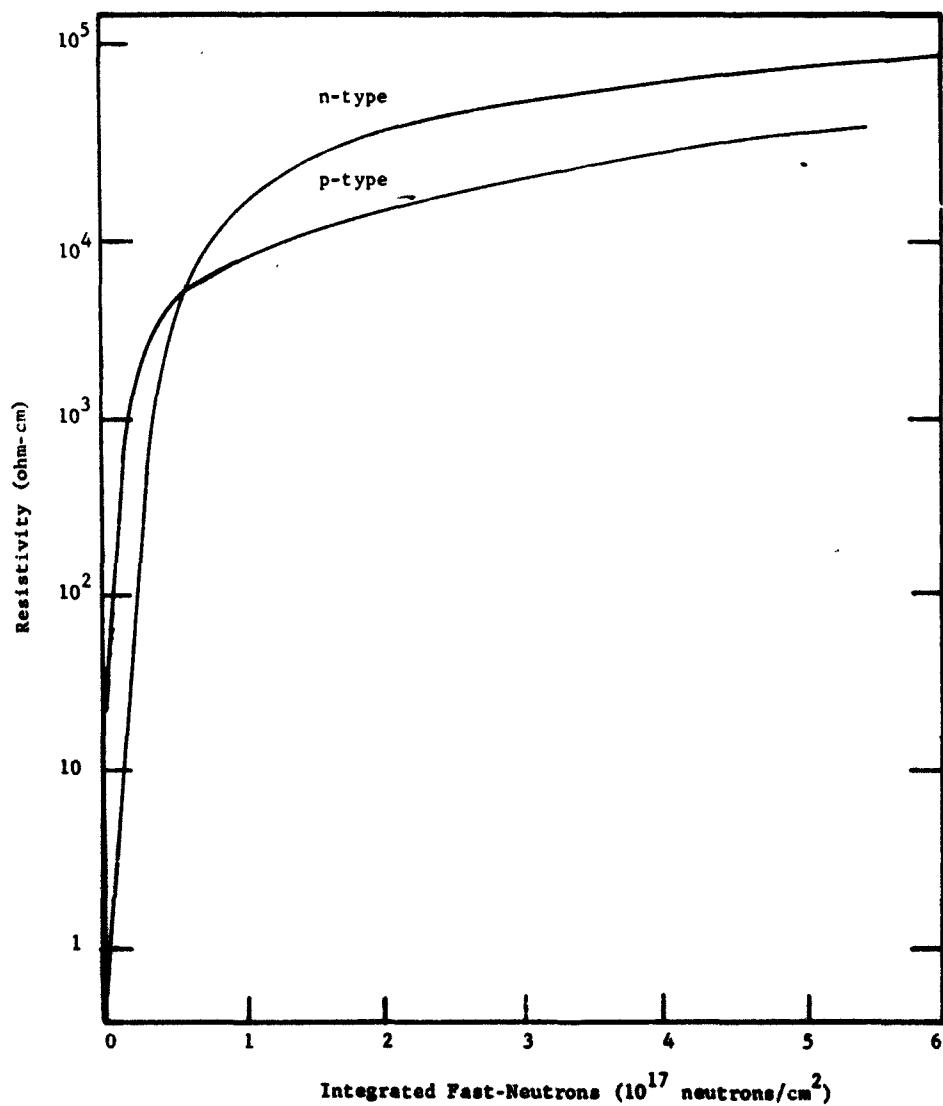
Fig. 2-14. The Effect of Integrated Fast-Neutron Bombardment [28]

by the usual criteria of resistor quality such as tolerance in value,
temperature coefficient of resistance, load life stability, environmental
stability and noise [29] but also by criteria peculiar to functional
electronic blocks such as isolation, coupling, power dissipation, size,
and circuit function. To optimize various properties of an integrated
circuit resistor, various types of silicon resistors have been built or
proposed.

2.2.1 Bulk Resistors

A bulk resistor is made by providing ohmic contact to any two
points of a homogeneous, uniformly doped crystal of silicon. R_c in
Figure 2-2 is an example. The value of R_c depends upon the geometry
and the resistivity according to Equation (2.1). The accuracy obtained
in shaping the geometry of the resistor by such methods as lapping,
etching, and scribing is directly reflected in the tolerance of the
resistor. Sheet resistivity, ρ_s, is a convenient quantity used to
design the shape of resistors. It is defined in Equation (2.9)

$$\rho_s = \frac{\rho}{t} \quad (\text{ohms/square} = \text{ohms/}\square),$$

where   (2.9)

$$t = \text{thickness of resistor.}$$

For a four mil thick wafer ($t = 10^{-2}$ cm) $\rho_s = 100\rho$ cm^{-1}; there-
fore, a bulk resistor could have any value of ρ_s between 10^{-1} and
10^7 ohms/$\square$, according to resistivity data of Figure 2-3. In practice
ρ_s seldom exceeds 10^4. The temperature coefficient of resistance (TCR)
of high resistivity silicon in the temperature range 150°C to -50°C is
large as seen in Figures 2-4 and 2-5. Few applications can tolerate a
magnitude change in R_c per 50°C which is characteristic of resistors
fabricated in high resistivity silicon. At lower values of resistivity
the value of R_c changes only by a factor of 5 or so between -50°C and
150°C. This, too, is prohibitively large. Not until the lowest values
of ρ are used does the TCR become reasonable. Unfortunately, at these
values of ρ, the total value of R_c is also restricted to small values.

A further problem of a bulk resistor is that it is restricted in
its circuit role without some type of isolation. R_c in Figure 2-2 could

not be used as an emitter or a base resistor because it is internally
connected to the collector.

2.2.2 Diffused Layer Resistor

A diffused layer resistor is formed by diffusing a junction into
bulk silicon and making ohmic contact at two points of the diffused layer.
Generally, this is done at the same time an active region of the circuit
is fabricated. The junction formed by the diffusant also provides dc
isolation between the resistor and the substrate as long as the operating
voltages are of the proper polarity to keep the junction reverse biased.
When the operating voltages are not properly polarized, an additional
junction must be inserted to isolate the resistor from the substrate.
Figure 2-15 shows a typical cross section of each type.
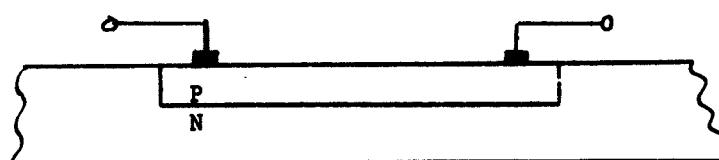
(a) Isolated by Operating Voltages
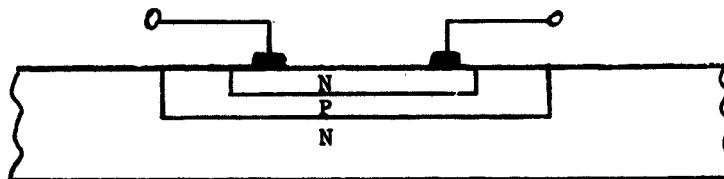
(b) Additional Junction to Achieve Isolation

Fig. 2-15. Diffused Layer Resistors

The primary advantage of this type of resistor over the bulk type
is that the thickness, $t = x_j$, can be one to two orders of magnitude
less than that of the bulk type and, therefore, low values of resistivity,
with the more favorable TCR, can be used to attain reasonable values of
ρ_s. The other dimensions, ℓ and w, can be controlled by the accurate
photoengraving process.

Plots of resistance vs temperature for various diffused resistors
are shown in Figure 2-16 [30]. The difference in the ionization energies
of gallium and boron are reflected in this plot. Ionization of the
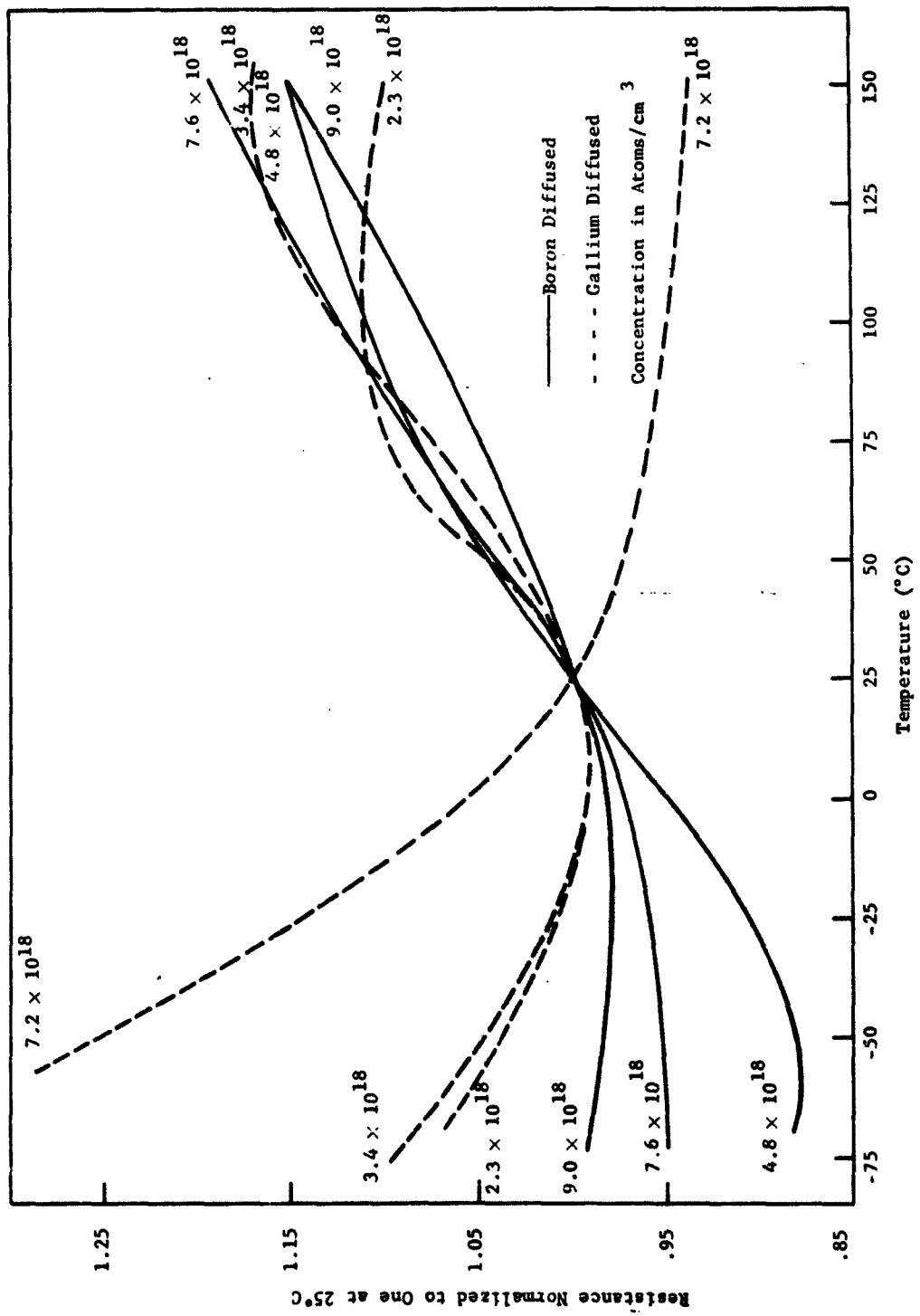
Fig. 2-16. Temperature Dependence of Diffused Silicon Resistors [30]

boron impurities is essentially complete below room temperature as
indicated by the positive slopes of the experimental curves for the
boron samples. Gallium, having a larger ionization energy (a "deeper"
impurity level), has the resistivity minimum close to room temperature
and for one sample, suspiciously above room temperature.

   The ionization energies of the acceptors are measured from the
edge of the valence band; the donors, from the edge of the conduction
band as shown in Figure 2-17. Obviously, aluminum should result in a
resistivity minimum at a temperature between that of gallium and boron.
The ionization energies of the n-type impurities are much closer together
and do not exhibit the different temperature dependences.
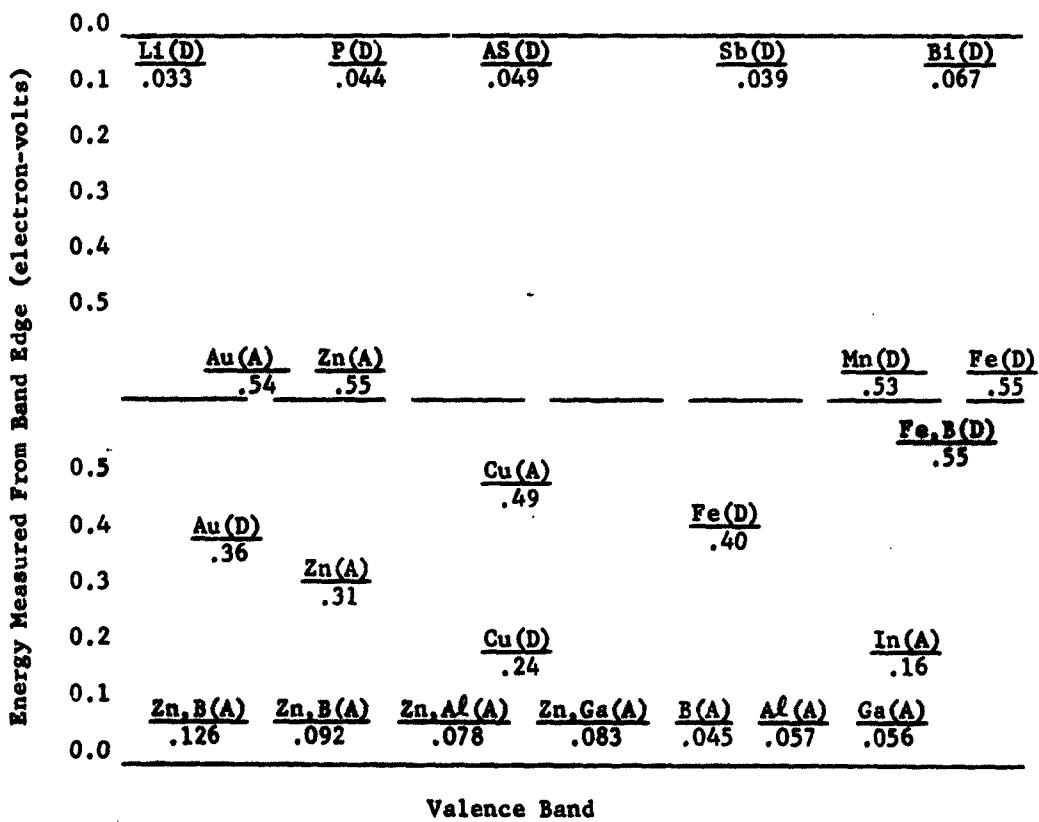
Figure 2-17. Energy Levels of Impurities in Silicon [3].

Correlation of the data of Figure 2-16 and Figure 2-5 is complicated by the non-uniform impurity distribution characteristic of diffused layers. The concentrations describing each curve of Figure 2-16 are surface concentrations while those of Figure 2-5 are bulk concentrations. With contacts to the top surface of the diffused layer, current flow is crowded into the top layers as determined by the impurity distribution. To compare these curves, an effective value of resistivity $\bar{\rho}$ must be used to describe the diffused layers. Tables 2.1 - 2.4 are taken from the calculated data of Irvin [1] and show the effective resistivity of diffused layers for a complementary error function distribution (Tables 2.1 and 2.2) and a Gaussian distribution (Tables 2.3 and 2.4).

The sheet resistivity of a diffused layer can be computed from the effective resistivity by Equation (2.9). The resistance of a diffused resistor is determined by geometry as in Equation (2.10)

$$R = \frac{\bar{\rho}\ell}{wx_j} = \rho_s \frac{\ell}{w} \ . \qquad (2.10)$$

The length of the resistor is the distance between the contacts. As long as the length is an order of magnitude greater than the junction depth x_j, this assumption introduces no appreciable error (see Section 4.2.3).

The equivalent circuit of a diffused resistor must include the capacitance and the rectifying properties of the p-n junction. A possible schematic appears in Figure 2-18 in which these distributed parameters are represented by an infinite number of lumped components.

R_D and R_S represent the diffused resistance and substrate resistance, respectively. At low frequency an input signal sees only the diffused resistor R_D, but at higher frequencies the distributed capacitance creates other low impedance current paths and the value of the resistor decreases. Figure 2-18 illustrates the frequency dependence of a five kilohm resistor [31]. Poor rectifying properties anywhere along the resistor to substrate junction alter the value of resistance even in dc operation. For this reason small area resistors are more desirable than large area resistors.

Table 2.1

AVERAGE RESISTIVITY ($\bar{\rho}$) OF N-TYPE COMPLEMENTARY

ERROR FUNCTION DIFFUSED LAYER IN SILICON (ohm-cm)

Surface Donor Concentration (cm^{-3})	Background Concentration of Acceptor Impurities (cm^{-3})						
	10^{14}	10^{15}	10^{16}	10^{17}	10^{18}	10^{19}	10^{20}
10^{21}	.0011	.0010	.00095	.00083	.00071	.00062	.00062
5×10^{20}	.0016	.0015	.0013	.0011	.0010	.00083	.00095
2×10^{20}	.0029	.0026	.0023	.0020	.0017	.0014	.0025
10^{20}	.0048	.0042	.0038	.0033	.0028	.0024	
5×10^{19}	.0083	.0077	.0067	.0055	.0045	.0045	
2×10^{19}	.017	.014	.012	.010	.010	.014	
10^{19}	.025	.022	.020	.016	.017		
5×10^{18}	.037	.032	.027	.024	.028		
2×10^{18}	.059	.050	.042	.038	.077		
10^{18}	.083	.067	.063	.059			
5×10^{17}	.12	.10	.083	.091			
2×10^{17}	.21	.17	.14	.25			
10^{17}	.33	.26	.23				
5×10^{16}	.56	.42	.42				
2×10^{16}	1.1	.83	1.3				
10^{16}	1.8	1.4					
5×10^{15}	3.2	2.9					
2×10^{15}	7.7	10.					
10^{15}	14.						

$$\rho_s = \bar{\rho}/x_j$$

Table 2.2

AVERAGE RESISTIVITY ($\bar{\rho}$) OF P-TYPE COMPLEMENTARY

ERROR FUNCTION DIFFUSED LAYER IN SILICON (ohm-cm)

Surface Acceptor Concentration (cm^{-3})	Background Concentration of Donor Impurities (cm^{-3})						
	10^{14}	10^{15}	10^{16}	10^{17}	10^{18}	10^{19}	10^{20}
10^{21}	.00087	.00080	.00065	.00062	.00051	.00043	.00035
5×10^{20}	.0016	.0015	.0013	.0011	.00095	.00077	.00074
2×10^{20}	.0038	.0036	.0029	.0026	.0022	.0017	.0025
10^{20}	.0069	.0065	.0056	.0049	.0039	.0032	
5×10^{19}	.013	.012	.010	.0087	.0069	.0067	
2×10^{19}	.029	.026	.022	.019	.015	.024	
10^{19}	.050	.047	.037	.030	.028		
5×10^{18}	.083	.071	.062	.050	.056		
2×10^{18}	.145	.125	.10	.091	.17		
10^{18}	.22	.19	.16	.15			
5×10^{17}	.33	.29	.24	.27			
2×10^{17}	.59	.48	.40	.74			
10^{17}	.87	.71	.67				
5×10^{16}	1.4	1.1	1.2				
2×10^{16}	2.6	2.1	3.7				
10^{16}	4.8	3.8					
5×10^{15}	9.1	29.					
2×10^{15}	20.						
10^{15}	38.						

$$\rho_s = \bar{\rho}/x_j$$

Table 2.3

AVERAGE RESISTIVITY ($\bar{\rho}$) OF N-TYPE GAUSSIAN DIFFUSED

LAYER IN SILICON (ohm-cm)

Surface Donor Concentration (cm^{-3})	Background Concentration of Acceptor Impurities (cm^{-3})						
	10^{14}	10^{15}	10^{16}	10^{17}	10^{18}	10^{19}	10^{20}
10^{21}	.00090	.00083	.00077	.00067	.00058	.00050	.00048
5×10^{20}	.0012	.0011	.0010	.00090	.00077	.00070	.00077
2×10^{20}	.0021	.0020	.0017	.0016	.0013	.0011	.0020
10^{20}	.0033	.0031	.0029	.0025	.0022	.0020	
5×10^{19}	.0059	.0050	.0048	.0040	.0037	.0036	
2×10^{19}	.012	.011	.010	.0091	.0077	.011	
10^{19}	.020	.017	.015	.013	.013		
5×10^{18}	.029	.025	.023	.020	.023		
2×10^{18}	.045	.038	.033	.030	.062		
10^{18}	.067	.055	.048	.048			
5×10^{17}	.091	.077	.067	.077			
2×10^{17}	.15	.12	.11	.20			
10^{17}	.25	.20	.17				
5×10^{16}	.40	.33	.33				
2×10^{16}	.83	.67	1.1				
10^{16}	1.3	1.2					
5×10^{15}	2.4	2.4					
2×10^{15}	5.0	7.7					
10^{15}	10.						

$$\rho_s = \bar{\rho}/x_j$$

Table 2.4

AVERAGE RESISTIVITY ($\bar{\rho}$) OF P-TYPE GAUSSIAN

DIFFUSED LAYER IN SILICON (ohm-cm)

Surface Acceptor Concentration (cm^{-3})	Background Concentration of Donor Impurities (cm^{-3})						
	10^{14}	10^{15}	10^{16}	10^{17}	10^{18}	10^{19}	10^{20}
10^{21}	.00056	.00050	.00048	.00043	.00037	.00032	.00027
5×10^{20}	.0011	.00095	.00087	.00027	.00069	.00059	.00057
2×10^{20}	.0025	.0022	.0020	.0019	.0016	.0013	.0019
10^{20}	.0048	.0042	.0038	.0033	.0029	.0025	
5×10^{19}	.0091	.0077	.0071	.0065	.0056	.0051	
2×10^{19}	.020	.017	.016	.014	.012	.017	
10^{19}	.034	.030	.028	.024	.022		
5×10^{18}	.059	.050	.045	.039	.042		
2×10^{18}	.11	.091	.080	.096	.14		
10^{18}	.17	.14	.12	.11			
5×10^{17}	.24	.21	.19	.20			
2×10^{17}	.42	.37	.33	.59			
10^{17}	.67	.56	.53				
5×10^{16}	1.0	.88	.91				
2×10^{16}	1.9	1.6	2.8				
10^{16}	3.2	2.9					
5×10^{15}	6.3	5.9					
2×10^{15}	14.	20.					
10^{15}	29.						

$$\rho_s = \bar{\rho}/x_j$$

(a) Frequency Dependence of a 5 k ohm Diffused Silicon Resistor
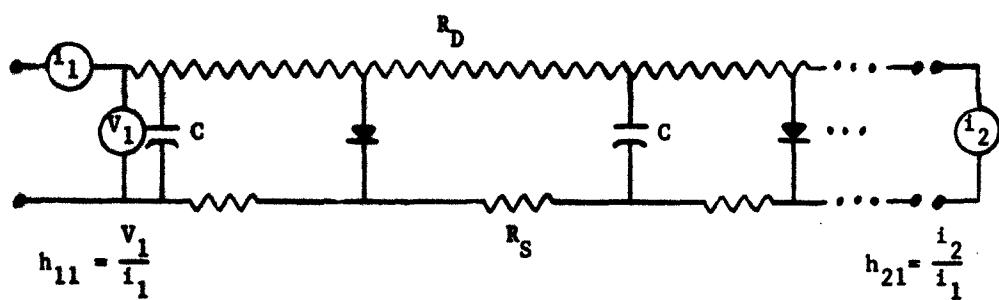
(b) Schematic Representation of a Diffused Layer Silicon Resistor

Fig. 2-18. Performance Properties of a Diffused Layer Silicon Resistor [31]

2.2.3 Epitaxial Layer Resistors

An epitaxial layer resistor is formed in an epitaxial layer of
silicon upon a substrate of opposite type conductivity silicon as shown
in Figure 2-19a. The lack of reliable techniques for masking during
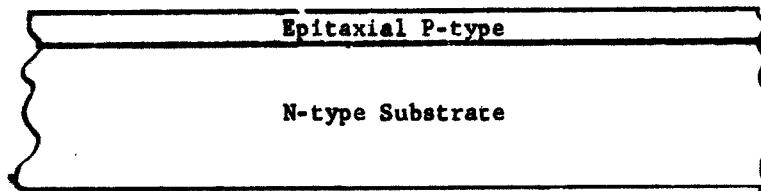
(a) After growth
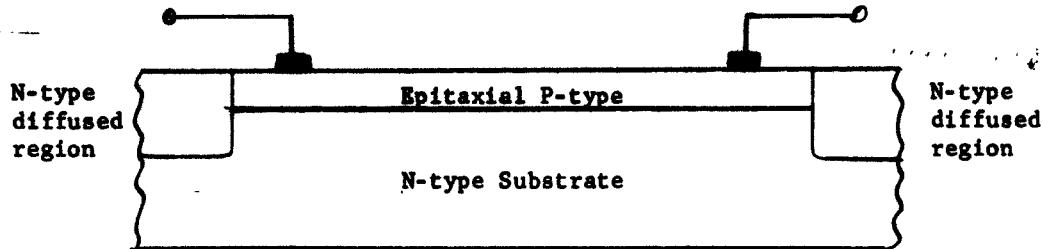
(b) After diffusion for definition

Fig. 2-19. Epitaxial Layer Resistors

epitaxial growth necessitates an extra step in which the resistors are
defined in area by masked diffusions using the same conductivity type
of diffusant impurity as that of the substrate. These diffusions must
penetrate through the epitaxial layer as shown in Figure 2-19b. Contacts
are alloyed to the surface of the epitaxial region and the spacing
between them is used to compute the resistor value just as was done for
the diffused resistor. The major difference between the two is that
the impurity distribution of an epitaxial layer approaches a uniform
distribution. Figure 2-20 shows a comparison of resistance vs tempera-
ture between a diffused boron resistor and an epitaxial boron resistor
of similar surface concentrations. The difference in these characteristics
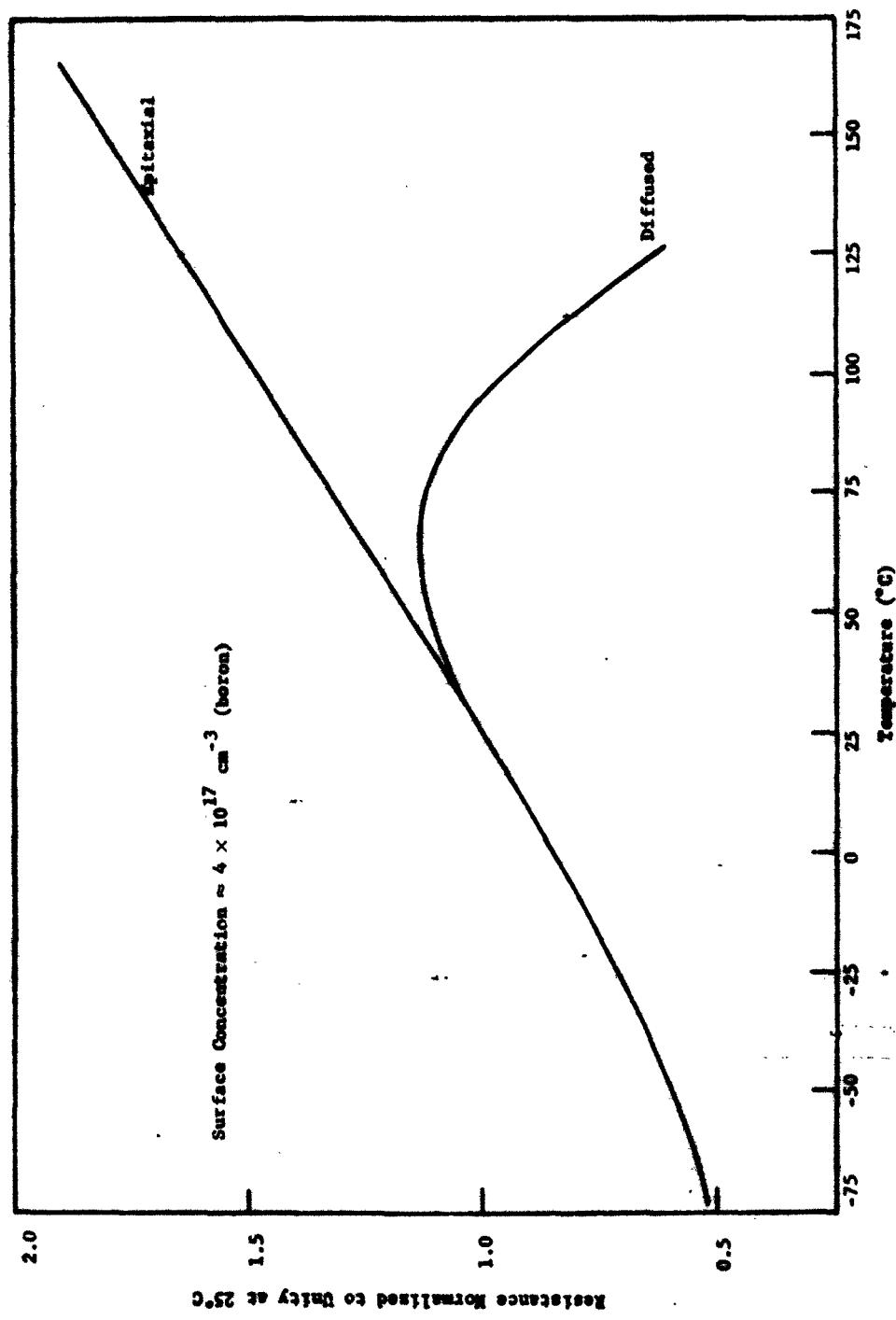
Fig. 2-20. Relative Temperature Dependence of Silicon Diffused and Epitaxial Layer Resistors [30]

at high temperature can be explained on the basis of carrier ionization
from the different doping levels. For shallow, low-gradient, diffused
junctions an area of high compensation near the junction gives rise
to a region of high room temperature resistivity. The reason for the
high resistivity of heavily compensated silicon is that a large
fraction of the majority carriers are trapped in minority impurity
levels. The energy difference between a free carrier and a carrier
trapped in a minority impurity level is less than the energy gap between
the conduction and valence bands; and the ionization of a trapped
carrier from a minority impurity level requires less thermal energy
than the ionization of an intrinsic carrier. The band structure
representation of a heavily-compensated, diffused resistor is shown
in Figure 2-21a. and that corresponding to a lightly-compensated,
epitaxial resistor is shown in Figure 2-21b.

$$E_c$$

$$E_{majority}$$

Many occupied minority levels $\quad E_{minority} \quad$ Few minority levels

$$E_v$$

(a) Diffused Resistor　　　　　　　　　　　(b) Epitaxial Resistor
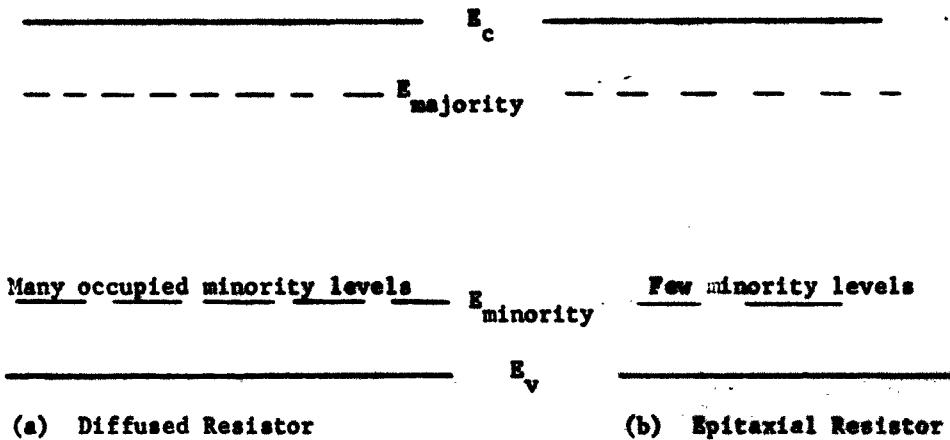
Fig. 2-21. Energy Band Structure of Silicon Resistors

The thermal activation energy in the temperature range $100° - 150°C$,
where all majority levels are ionized, depends primarily on the energy
difference between E_c and $E_{minority}$ for the diffused resistor and
between E_c and E_v for the epitaxial resistor. For this reason, the

resistivity of the diffused resistor decreases while that of the epitaxial resistor increases in the 100°-150°C temperature range.

For very thin epitaxial resistors the large density of dislocations present at the interface between the epitaxial layer and the substrate becomes an important, although little understood, factor (see 2.1.3). Conduction in a high dislocation region is probably different in detail from that in a dislocation free region. Evidence to support this conclusion is presented in Figure 2-22 [32], showing the temperature dependence of the resistance of two similarly doped epitaxial resistors which vary only in thickness. The higher ρ_s resistor has a small TCR probably because the thin layer has more crystalline defects than the thicker layer which corresponds to a less temperature dependent mode of conduction.

2.2.4 Vapor Deposited Silicon Resistor

This resistor is formed by the same process as the epitaxial resistor except that the silicon substrate now has a layer of SiO_2 on it. The effect of the layer of SiO_2 is to prevent epitaxy and to cause a randomly oriented polycrystalline layer to form as the silicon atoms condense. The resistor geometry must be controlled by a subsequent operation such as etching. Figure 2-23 illustrates two steps in the fabrication of such a vapor deposited resistor of silicon.

The difference in the conductive properties of polycrystalline silicon from those of single crystal silicon is shown in Figures 2-4 and 2-5. Figure 2-24 shows that the temperature dependence of polycrystalline resistors is similar to that of the upper dashed curve in Figure 2-5. Again heavier doped polycrystalline silicon displays a lower TCR.

The minimum thickness for satisfactory performance is probably greater for a polycrystalline resistor than for either a diffused or an epitaxial resistor. Since the resistor structure is no longer monocrystalline, more inhomogeneities and local defects are present. The influence of the lack of uniformity is diminished as the layer thickness grows. Figure 2-25 [33] shows a plot of resistance vs
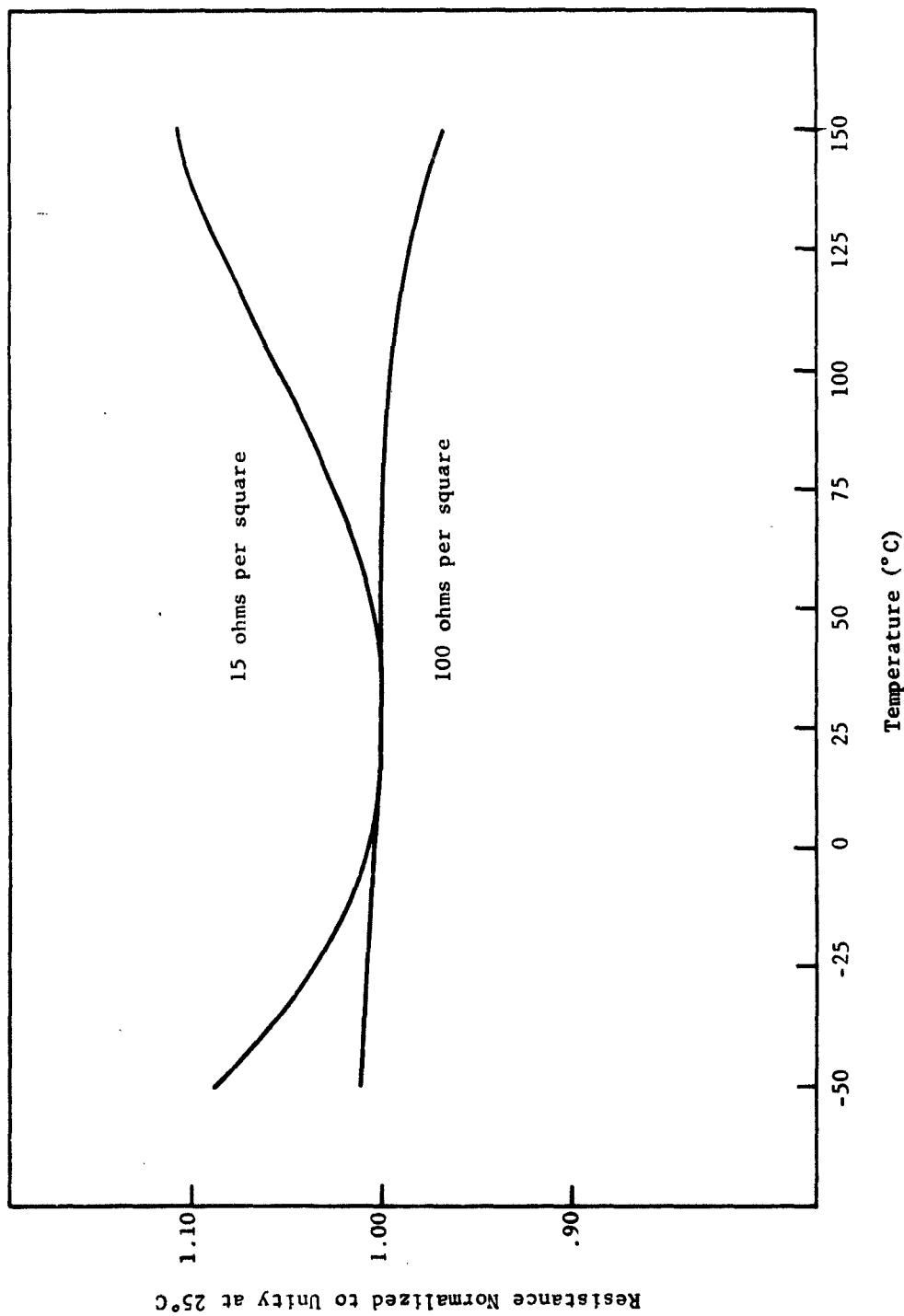
Fig. 2-22. Temperature Dependence of Resistance for Two Epitaxial (Phosphorus) Silicon Resistors of Different Sheet Resistivities [32]
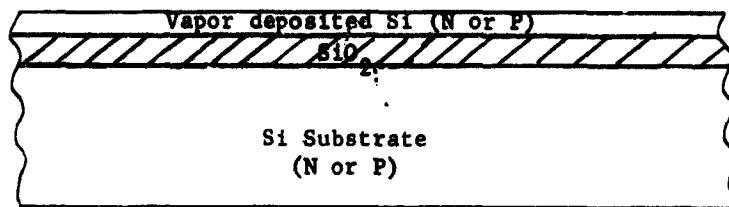
(a) After deposition
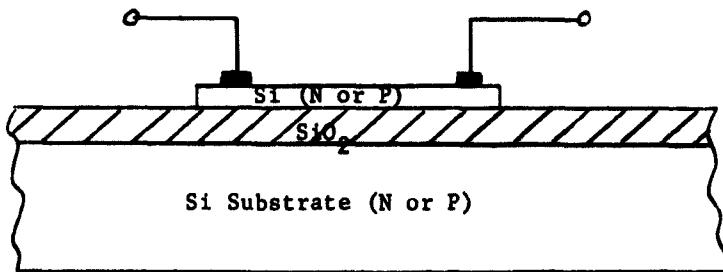
(b) After etching

Fig. 2-23. Vapor Deposited Si Resistor on SiO_2 Covered Si Substrate

temperature of a vapor deposited polycrystalline resistor on a ceramic
substrate with $\rho_s \approx 13$ ohms/□ . This can be compared with the 15 ohms/□
epitaxial resistor of Figure 2-22. Phosphorous is the doping impurity
of both resistors. In general the large density of grain boundaries of
the vapor deposited polycrystalline silicon resistor results in lower
values of the TCR than for similarly doped epitaxial layers. TCR's of
≈ 150 PPM/°C over the temperature range of -50° to 150°C have been
observed on polycrystalline silicon layers. The best TCR observed with
single crystal layers, with the exception of the extremely thin layers
where the effect of dislocations is dominant, is ≥ 220 PPM/°C [32].
Probably the mechanism that reduces the TCR of a thin epitaxial resistor
(100 ohms/□) below that of a thicker epitaxial resistor (15 ohms/□)
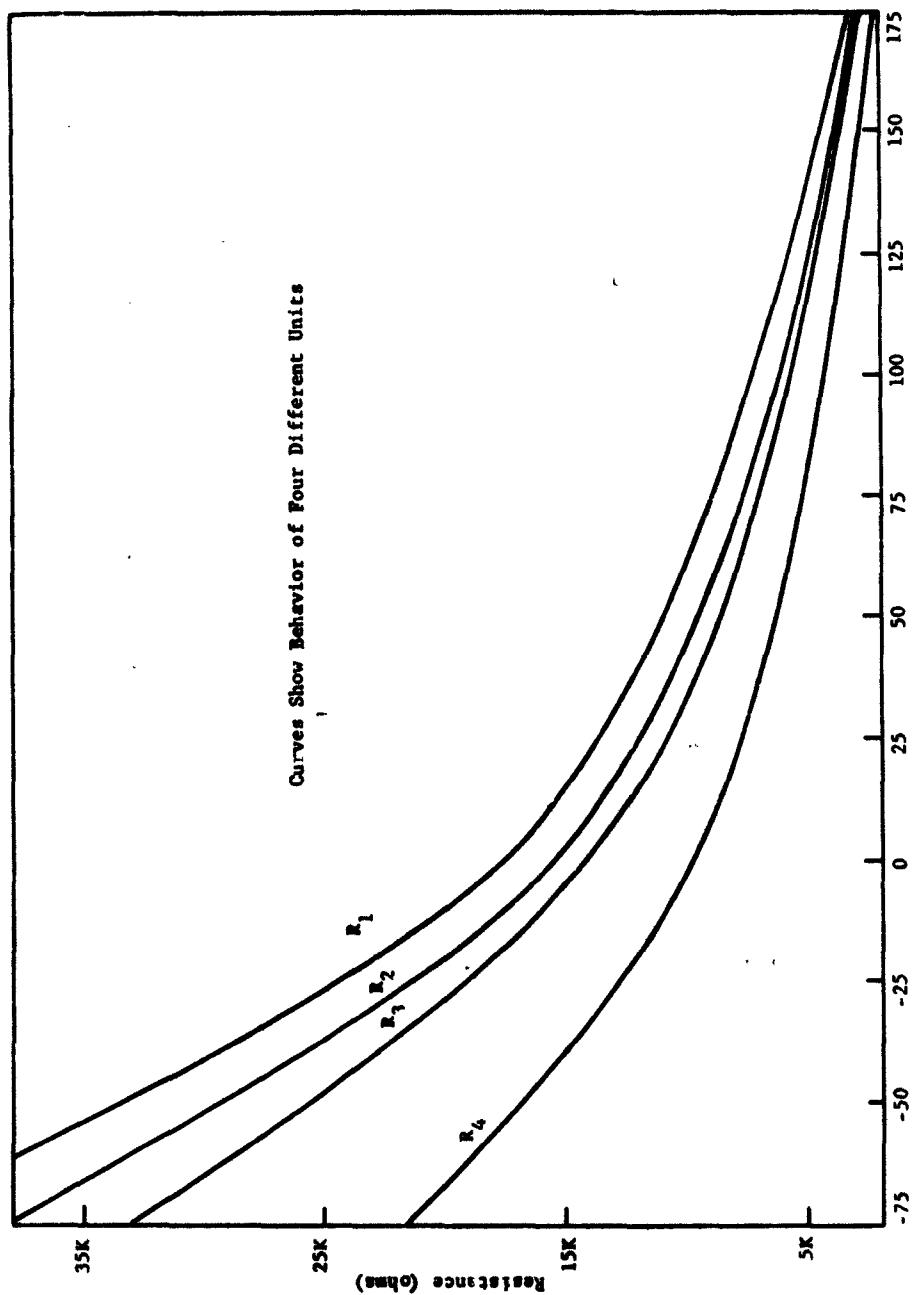
Fig. 2-24. The Temperature Dependence of Resistance for Polycrystalline Gallium Doped Silicon Deposited on Ceramic [30]
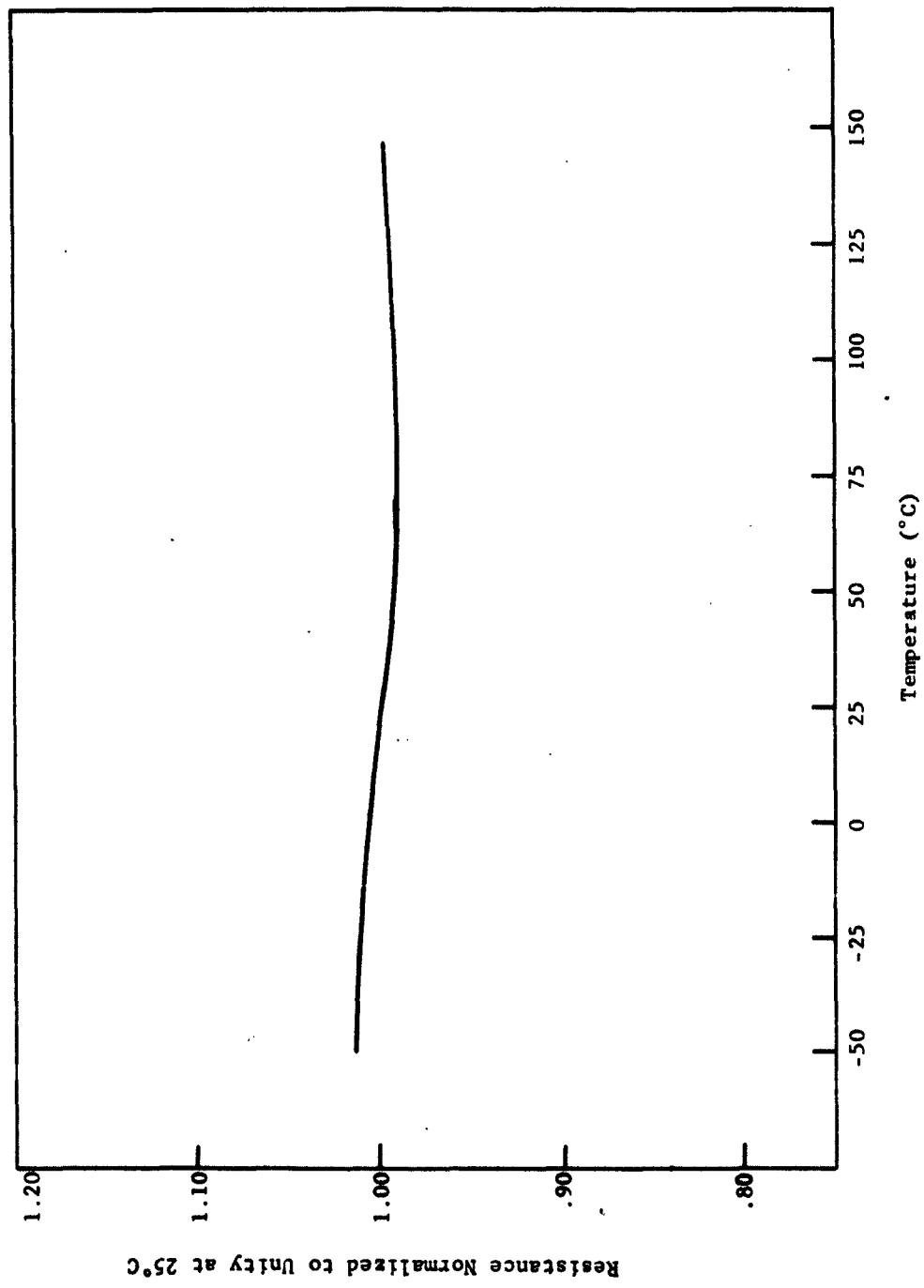
Fig. 2-25. Temperature Dependence of Vapor Deposited Polycrystalline Silicon Resistors (Phosphorous Doped, 13 ohms/sq.) [33]

as illustrated in Figure 2-22 is the same that lowers the TCR of the polycrystalline layers. In both cases the conduction is limited by scattering from imperfections or structural defects rather than by phonon or impurity scattering. The change of the TCR with impurity content is particularly interesting, however. Figures 2-4 and 2-5 show that the polycrystalline samples of low impurity concentration are more temperature dependent than the single crystal samples in the temperature range between 27 and -175°C. At high impurity concentrations the difference disappears. A comparison of Figure 2-24 and Figure 2-25 also shows that the temperature dependence of polycrystalline resistors is strongly dependent upon the impurity concentration--even more than is true for the single crystal resistors. No quantitative data exist relating resistance to structural defects.

An advantage inherent in the vapor deposited resistor is high dc isolation from the substrate without regard to operating potential. A capacitive coupling, similar to that of the diffused junction shown in Figure 2-18, certainly exists and can be analyzed analogously to the capacitance of MOS[*] structures. No actual measurements now exist of the distributed capacitance between a polycrystalline resistor and the oxidized silicon substrate but from data on the capacitance of conductors on the oxide and on the oxide thickness, it is known to be much less than for diffused or epitaxial layer resistors.

2.2.5 Series or Parallel Combination of Elements

If a resistor, R, is broken into two components, R_1 and R_2, one of which has a positive TCR and the other, a negative TCR, a lower value of TCR for a given value of R can be achieved by connecting R_1 and R_2 in either series or parallel as shown in Figure 2-26. Figure 2-28 [30] shows that two of the diffused resistors of Figure 2-16 have this property over the temperature range -50° to 150°C. By connecting these two resistors in series a lower value of TCR is achieved as shown in Figure 2-27. Writing for the series combination:

[*] Metal-Oxide-Silicon

$$R_T = R_1 + R_2 , \qquad (2.11)$$

$$\frac{\partial R_T}{\partial T} = \frac{\partial R_1}{\partial T} + \frac{\partial R_2}{\partial T} .$$

The TCR of R_T is defined as

$$TCR \equiv \frac{1}{R_T} \frac{\partial R_T}{\partial T} = \frac{1}{R_T} \left(\frac{\partial R_1}{\partial T} + \frac{\partial R_2}{\partial T} \right) . \qquad (2.12)$$
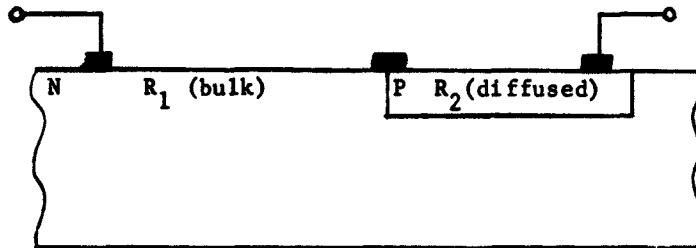
(a) Series
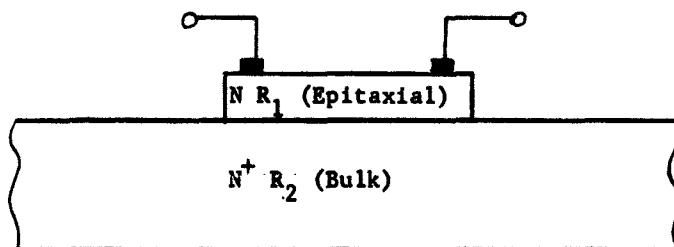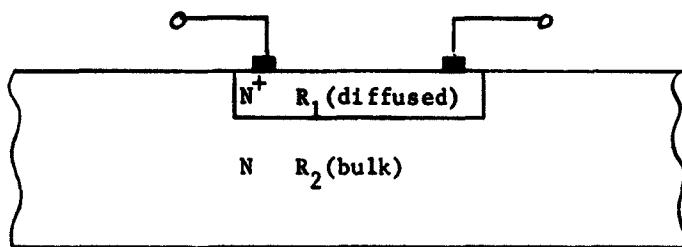
(b) Parallel

Fig. 2-26. Combinations of Resistors to Achieve Lower TCR

Resistance Variation (100 ohms/division)

(d) Gallium Diffused and Boron Epitaxial Resistors in Series
$R_{25°C}$ = 2100 ohms

(b) Gallium Diffused Resistor from Fig. 2-16
$R_{25°C}$ = 1920 ohms

(c) Gallium and Boron Diffused Resistors (a + b in Series)
$R_{25°C}$ = 2440 ohms

(a) Boron Diffused Resistor from Fig. 2-16
$R_{25°C}$ = 522 ohms

-25   0   25   50   75   100   125   150
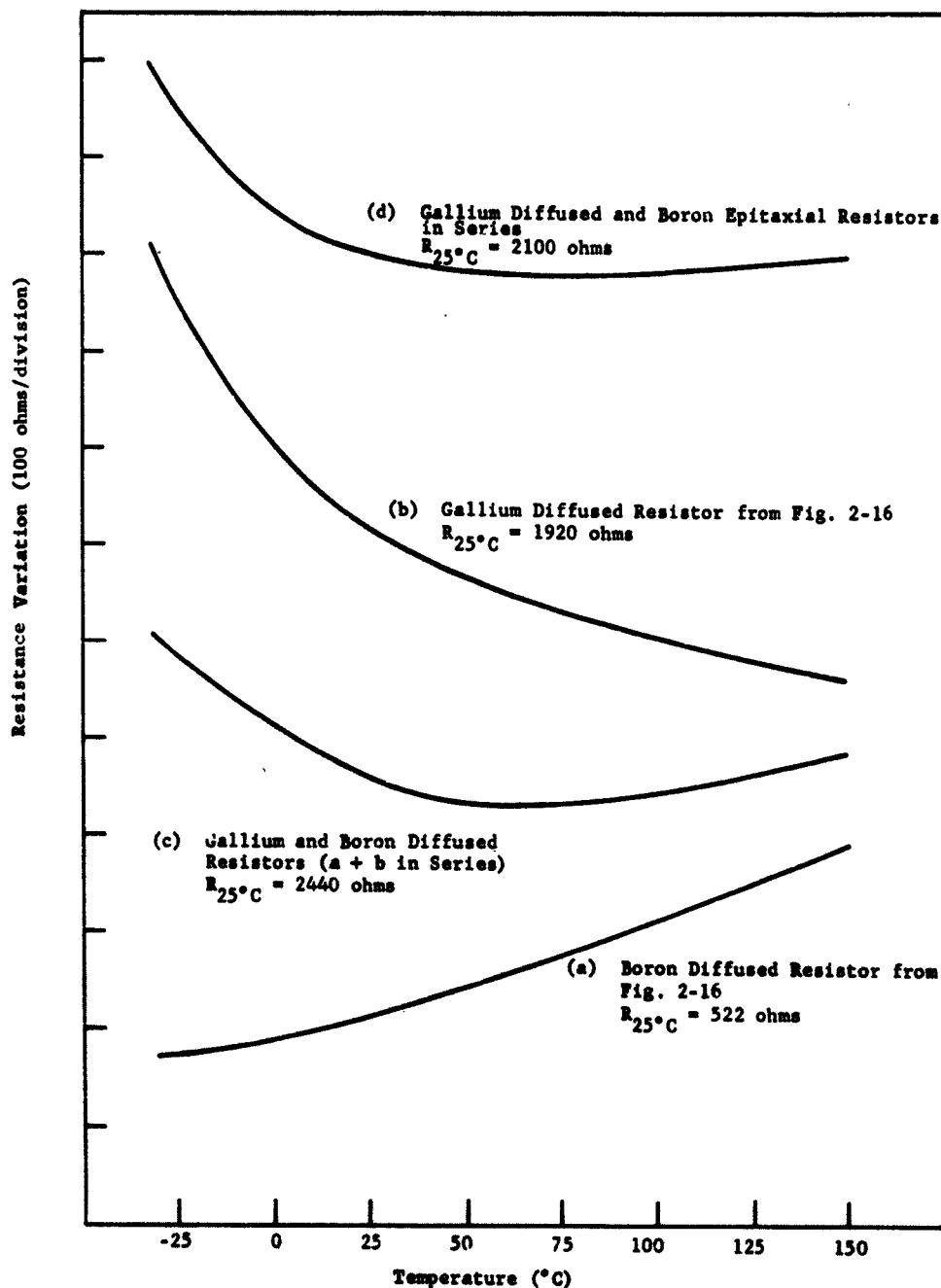
Temperature (°C)

Fig. 2-27. A Comparison of the Temperature Dependence of Individual Resistors with that of their Series Combination [30]

If $\frac{\partial R_1}{\partial T}$ and $\frac{\partial R_2}{\partial T}$ are of opposite signs, the value of $\frac{1}{R_T} \frac{\partial R_T}{\partial T}$ must be less

than $\frac{1}{R_T} \frac{\partial R_1}{\partial T}$ or $\frac{1}{R_T} \frac{\partial R_2}{\partial T}$ alone.

Similarly, if the parallel connection of Figure 2-26b is used, the equations become the following:

$$R_T = \frac{R_1 \, R_2}{R_1 + R_2} \qquad (2.13)$$

$$\frac{\partial R_T}{\partial T} = \frac{R_2^{\,2}}{(R_1 + R_2)^2} \frac{\partial R_1}{\partial T} + \frac{R_1^{\,2}}{(R_1 + R_2)^2} \frac{\partial R_2}{\partial T}$$

and

$$TCR \equiv \frac{1}{R_T} \frac{\partial R_T}{\partial T} = \left(\frac{R_2}{R_1 + R_2}\right) \frac{1}{R_1} \frac{\partial R_1}{\partial T} + \left(\frac{R_1}{R_1 + R_2}\right) \frac{1}{R_2} \frac{\partial R_2}{\partial T} \qquad (2.14)$$

Figure 2-28 shows a special case plot for $\partial R_1/\partial T = -\partial R_2/\partial T$ where the value of $\partial R_T/\partial T$ is plotted as a function of R_1/R_2. The case $\partial R_1/\partial T = -\partial R_2/\partial T$ can occur in nature. For example, Figure 2-5 shows that p-type silicon of 20-40 ohm-cm resistivity reverses the sign of TCR on going from single to polycrystalline structure. The magnitudes of the TCR are certainly of the same order.

Practically, both of these combinations are simple to realize as shown in Figure 2-26. Figure 2-26b actually is a N^+ on N diffusion where no space charge region is created by the diffusion. This type of resistor has been incorporated into functional electronic blocks [34]. R_1 is a substrate of 800 - 1000 ohm-cm n-type silicon on which R_2 is a phosphorous diffused 10μ layer with a surface concentration of 8×10^{16} cm^{-3}. A transistor can be fabricated by standard procedures on this layer to build the structure shown in Figure 2-29. The circuit is the same as that of Figure 2-2 but the TCR of the collector resistor is improved by dividing it into two components.

Assumptions:

1. $R_T = \dfrac{R_1\,R_2}{R_1 + R_2}$

2. $\dfrac{\partial R_1}{\partial T} = -\dfrac{\partial R_2}{\partial T}$

Ratio of Paralleled Resistances (R_1/R_2)

Temperature Dependence of the Total Resistance, $\dfrac{\partial R_T}{\partial T}$ (normalized to the value of $\dfrac{\partial R_1}{\partial T}$)
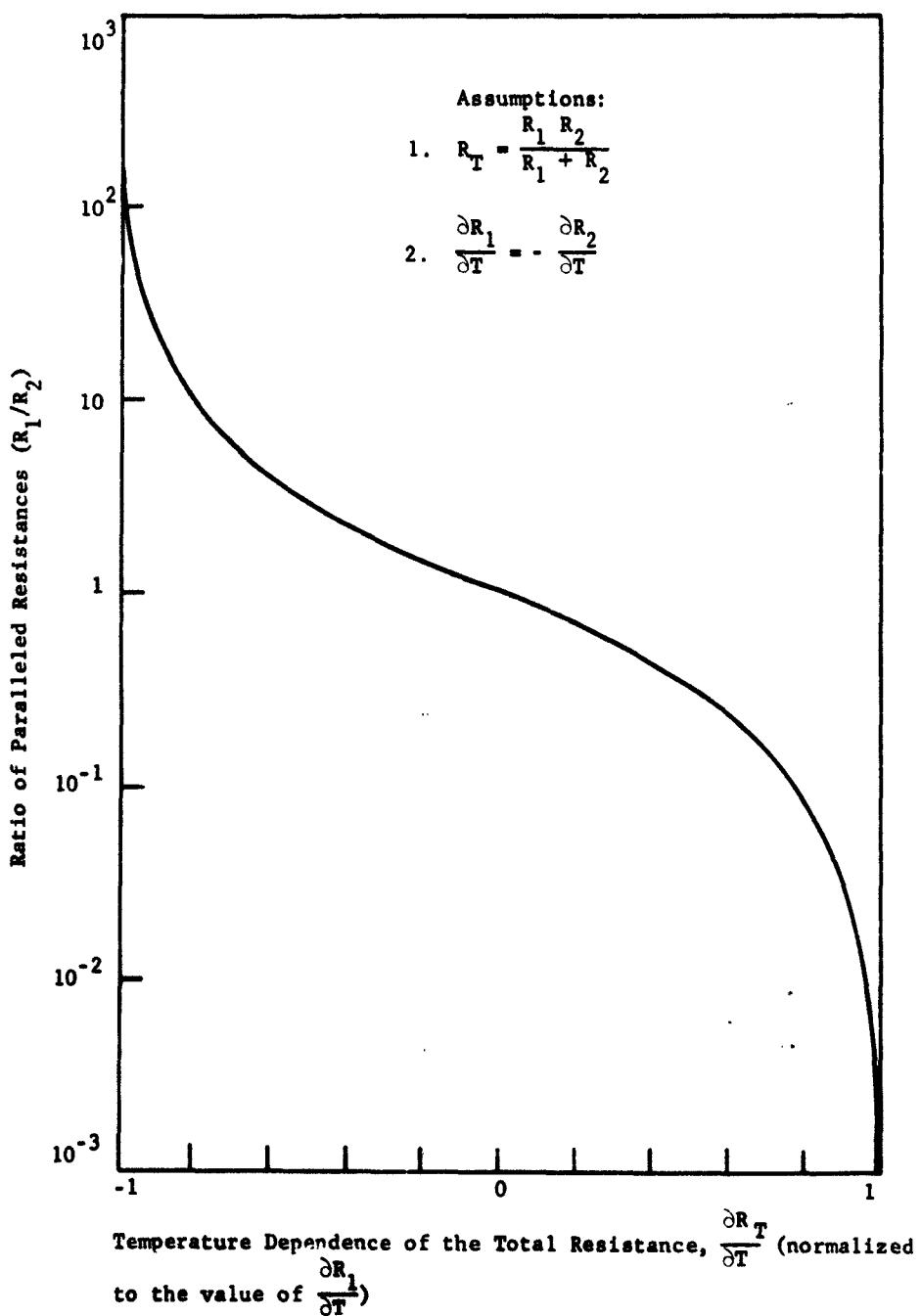
Fig. 2-28.   Reduction in Temperature Dependence Achieved by Building a Resistor from two Parallel Components whose Rates of Change of Resistance with Temperature are Equal and Opposite

2-47
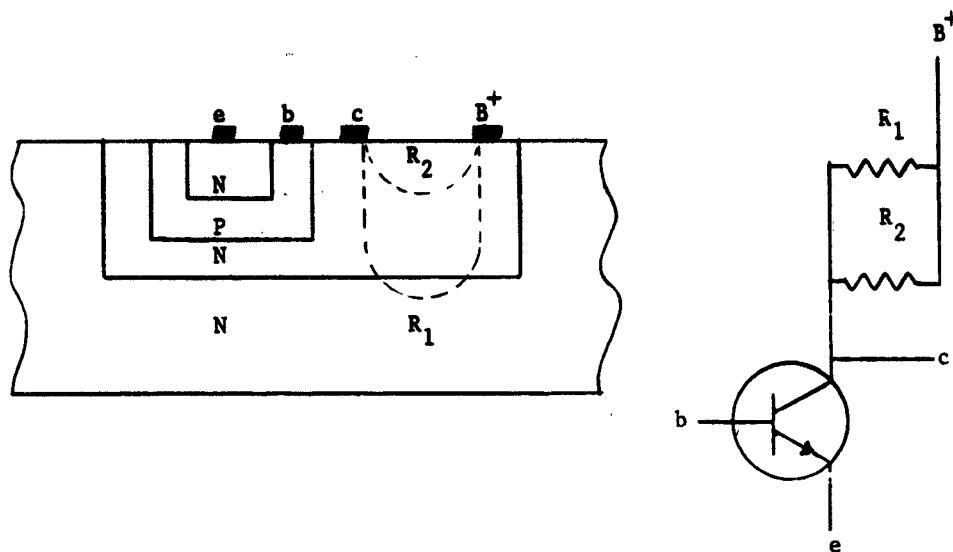
Fig. 2-29. Collector Resistor Formed by a Parallel Combination of Diffused
(R_2) and Bulk (R_1) Silicon Resistors

2.2.6 The Impurity Compensated Resistor

The principles of the gold doping technique [35], employed by various
manufacturers to increase substrate resistance, reduce lifetime and
alter other properties, suggest another solution to the problem of
building a silicon resistor of low TCR but high sheet resistivity. If
a degenerately doped silicon region is highly compensated by the presence
of a similar number of opposite type impurities, both the acceptor and
donor levels merge with the adjacent band edges to form what is effec-
tively a smaller band-gap semiconductor [36]. That the impurity levels
have overlapped into the conduction bands removes the impurity activation
energy. This explains the small TCR characteristic of heavily doped
silicon. With high compensation, however, the number of carriers in
the conduction band will be small at room temperature so that a high
value of sheet resistivity is achieved while maintaining the low TCR.

Because of its limited solubility in silicon, gold is not the most
suitable compensating impurity for this process. Impurities with higher
solid solubilities such as phosphorous and boron are better. To solve
the control problems of producing accurately compensated, heavily doped

regions of silicon probably requires a better technology than is presently available. Some effort to develop such a technology may be worthwhile, for in principle the impurity compensated resistor seems capable of extending the range of feasible values of silicon resistors.

2.2.7. The Reverse Resistance of a p-n Junction

All the resistors discussed so far with the possible exception of the impurity compensated resistor are limited to a maximum value of about 1 megohm or less. The trend to nanowatt circuits [37] demands values of resistance larger than this. Since power dissipation is no problem here, at nanowatt levels, a logical source of such resistances is the reverse resistance of a p-n junction. The reverse resistance of a planar p-n junction typically is of the order of 10^9 - 10^{10} ohms. With appropriate controls these values may possibly be reduced to yield values in the 10^5 - 10^8 ohm range much the same as has been demonstrated on germanium p-n junctions [38]. Two approaches are possible.

The first is to decrease the junction bulk resistance by introducing metallic impurities into the region of the junctions. Such treatments are known to produce "soft" junctions [39]. If this process could be controlled, as has been demonstrated for germanium [38], the reverse resistance could well be reduced to useable values even without fully understanding the mechanism.

A second approach is to alter the surface conduction of the junction by control of the surface potential at the silicon-silicon dioxide interface. With proper surface potential, an inversion layer resistor such as illustrated in Figure 2-30 could achieve resistance values of megohms and greater. The structure is that described as a surface-field-effect transistor [40] except that the control electrode is made optional. If the control electrode is included, it can be connected to some point of the circuit to create a voltage feedback. If it is not included, the magnitude of the inversion layer resistance will depend upon the surface potential as indicated in Figure 2-8 and also upon the geometrical dimensions and the doping levels of the p-type substrate.

2.2.8 Channel Resistance of Field Effect Transistor

A method of achieving high values of resistance similar to that just described in 2.2.7 is to utilize the field effect transistor as a voltage variable resistor. As shown in Fig. 2-31, there are actually two regions of relatively linear operation available:

1. The region between 0 V and some voltage below V_{po}, the channel pinch-off voltage. In this region the values of resistance realizable are low (k ohm range) and the range of linear operation is restricted to low values of V_{SD} (typically less than 5 V).

2. The region between V_{po} and the breakdown voltage. In this region high values of resistance (megohms) are realizable. For relatively linear operation V_{SD} must always be above V_{po}. The gate voltage permits some control of V_{po} but at the same time it influences BV_{SD} as well.

This type of resistor is currently in use on various functional electronic blocks.
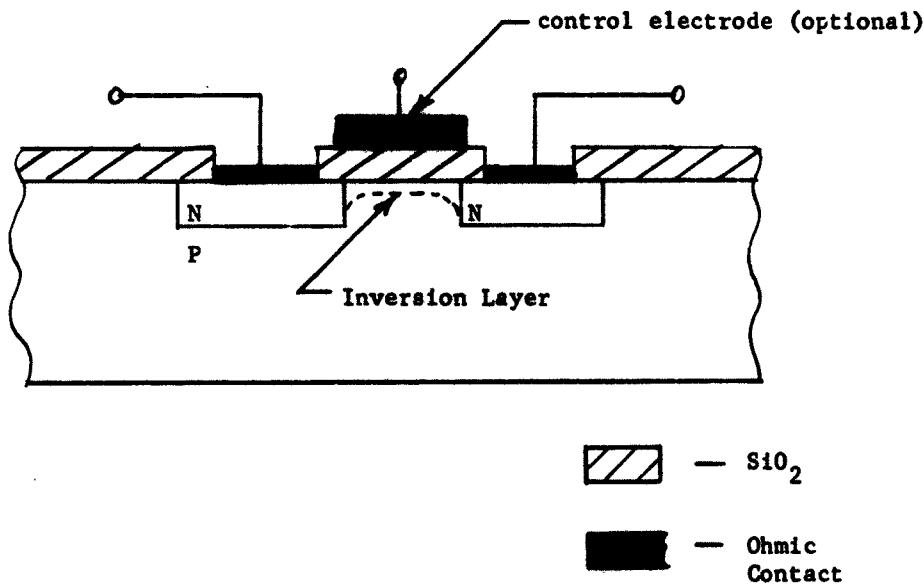
Fig. 2-30. Inversion Layer Resistor
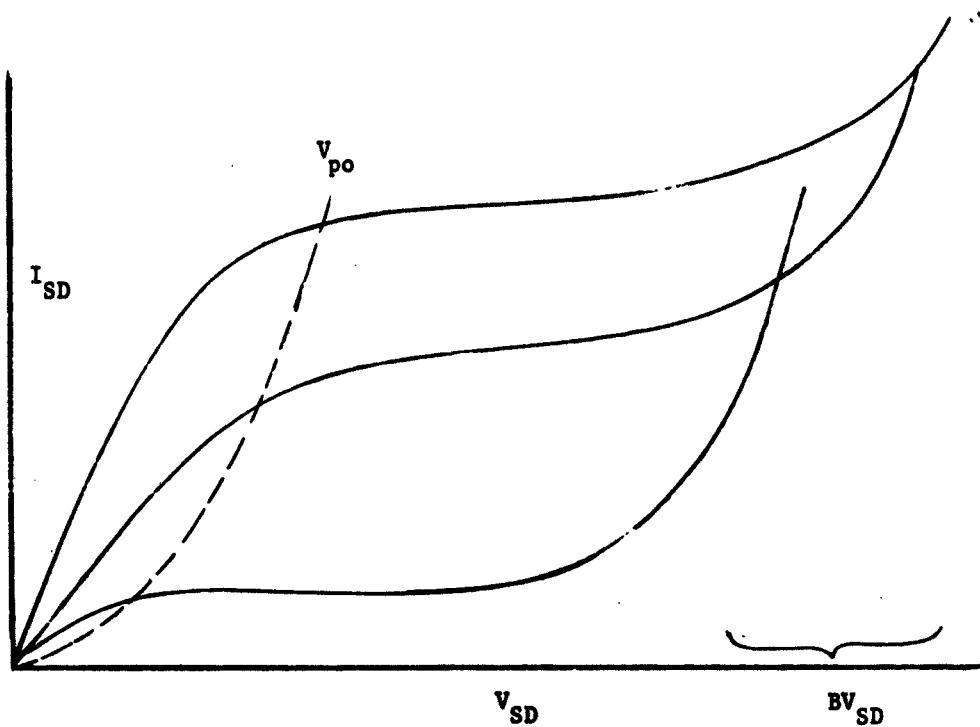
Fig. 2-31. The Electrical Characteristics of a Field Effect Transistor

2.2.9 Summary

Table 2.5 summarizes the types and properties of the silicon resistors discussed in this section.

2.3 Design Considerations

The purpose of this section is to discuss the design of silicrn resistors as regions of integrated device structures.

The design of a silicon resistor for an integrated circuit must be made with a specific integrated circuit in mind. The requirement of compatibility with the rest of the functional block, in operation as well as in fabrication, dictates that the basic design be that of a complete block rather than that of a component. Nevertheless, some principles of design are unique to the resistor. No attempt is made to be exhaustive in this section for each new application creates new problems requiring new solutions. What is presented here is simply one

Table 2.5 - Types and Properties of Silicon Resistors

Type	Max. Reasonable ρ_s(ohms/□)	Typical Tolerances (%)	Min. TCR(ppm/°C)	Advantages	Disadvantages
Bulk	10^4	±30%	High ($>10^3$)	1) Easy to build 2) Certain interconnections internally made	1) Very high TCR 2) Poor tolerance 3) Additional isolation often required
Diffused	10^3	±10%	200	1) Good dimensional control 2) Flexible size and shape 3) Junction isolation possible by operating voltages	1) Dependent on large area p-n junction for isolation 2) Capacitance of isolating junction added to circuit
Epitaxial	2×10^3	±15%	200	1) Nearly homogeneous impurity distribution	1,2) Same as for diffused layer 3) Geometry must be defined by additional diffusion 4) Limited to the impurity concentrations obtainable by vapor deposition

Type					Advantages	Disadvantages
Vapor Deposited Layer	•	—	—	100-150	1) DC isolation is independent of operating voltage and polarity 2) Less capacitive coupling than junction isolated resistors	1) Adherence and uniformity poorer than epitaxial layer 2) Capacitance of MOS structure added to circuit 3,4) Same as for epitaxial layer
Series or Parallel Combination	—	—	—	—	1) Reduces TCR	1) Analysis is difficult 2) Reproducibility poor
Compensated Impurity Resistor	—	High ($>10^4$)	—	Low (<300)	1) High sheet resistivity with low TCR	1) Fabrication technology is not presently available
Reverse Biased Junction	—	10^3 to 10^{10} Ω Resistance	—	High (?)	1) High values of resistance 2) Small area	1) Control is not yet demonstrated 2) TCR may be high without some form of temperature compensation 3) Dc and ac resistances may be quite different
Channel Resistance of FET	—	10^8 Ω Resistance	—	High	1,2) Same as reverse biased junction 3) Well established technology	1) Restricted operating ranges 2,3) Same as reverse biased junction

approach to the design of the resistive regions of a functional block. This method, while perhaps successful for a particular application, could be quite inappropriate for a different application. Clearly, the optimum design is a custom design, tailored to the characteristics of a specific circuit.

The basic problem of a designer is recognition of the point of diminishing returns so that a block is neither over-designed nor inadequately designed.

2.3.1 General Procedure

To design a resistor into a functional electronic block, certain basic starting information must be known about the resistor:

1. Value
2. Tolerance
3. Operating potential
4. Power dissipation and ambient temperature
5. Isolation required
6. TCR
7. Power dissipation of the functional block.

The last requirement, power dissipation, is usually the primary factor for determining the size and type of package for the circuit which in turn defines the area available for the resistors. The specific choice of resistor type is determined by requirements 1 to 6. Since the tolerances associated with the fabrication processes are often large, a desirable design feature is the ability to alter the value of a resistor after some preliminary testing. The techniques for doing this vary with the type of resistor but in general are limited to an alteration in the geometrical dimensions of the resistor. The final test of the design is its operational success or an analysis of its shortcomings.

2.3.2 Specific Steps

2.3.2.1 Circuit Schematic and Breadboard

All of the information needed for starting the design, as listed in 2.3.1, can be obtained from a conventional schematic diagram of

the integrated circuit. The circuit should be breadboarded from the schematic using the conventional active components that appear the closest in characteristics to those that are anticipated in the integrated circuit. The transistors and diodes of one's own laboratory are probably the best to use in this breadboard. If these are not available, the next best choice is to select commercial transistors fabricated by the same process as will be used in the integrated circuit and with the same general design parameters that appear adequate for the anticipated device properties. Such a procedure is unsatisfactory in those applications where optimum circuit performance is achieved by individually matching resistors to active devices. Only by providing a means of altering the values of resistance over as large a range as possible can a near optimum performance be achieved in such circuits. A desirable step is to redesign the conventional circuit in such a way as to take advantage of unique attributes of integrated structures and the inverted cost factors of elements in the integrated device.

Having decided upon the component values of the schematic, the required power ratings of the resistors can be computed.

2.3.2.2 Package Type and Size

The power level of the circuit usually dictates the minimum package size. The block must be able to operate with the designed power supplies with a specified quality of performance. Special packages are sometimes necessary to make this possible. Although the effectiveness of a given package depends upon many indefinite quantities such as uniformity of contact between the package and the block, the criteria for packaging power transistors and diodes are transferable to integrated circuits. A package that dissipates one watt as a transistor package will do the same as a functional block package. Typical power dissipation of a transistor in a TO-5 package is shown in Figure 2-32 [45].

The size and shape of the silicon die are limited by the package. The area devoted to resistors should be proportional to the power dissipated by them. The size of an individual resistor is scaled by its anticipated power dissipation with respect to the total.
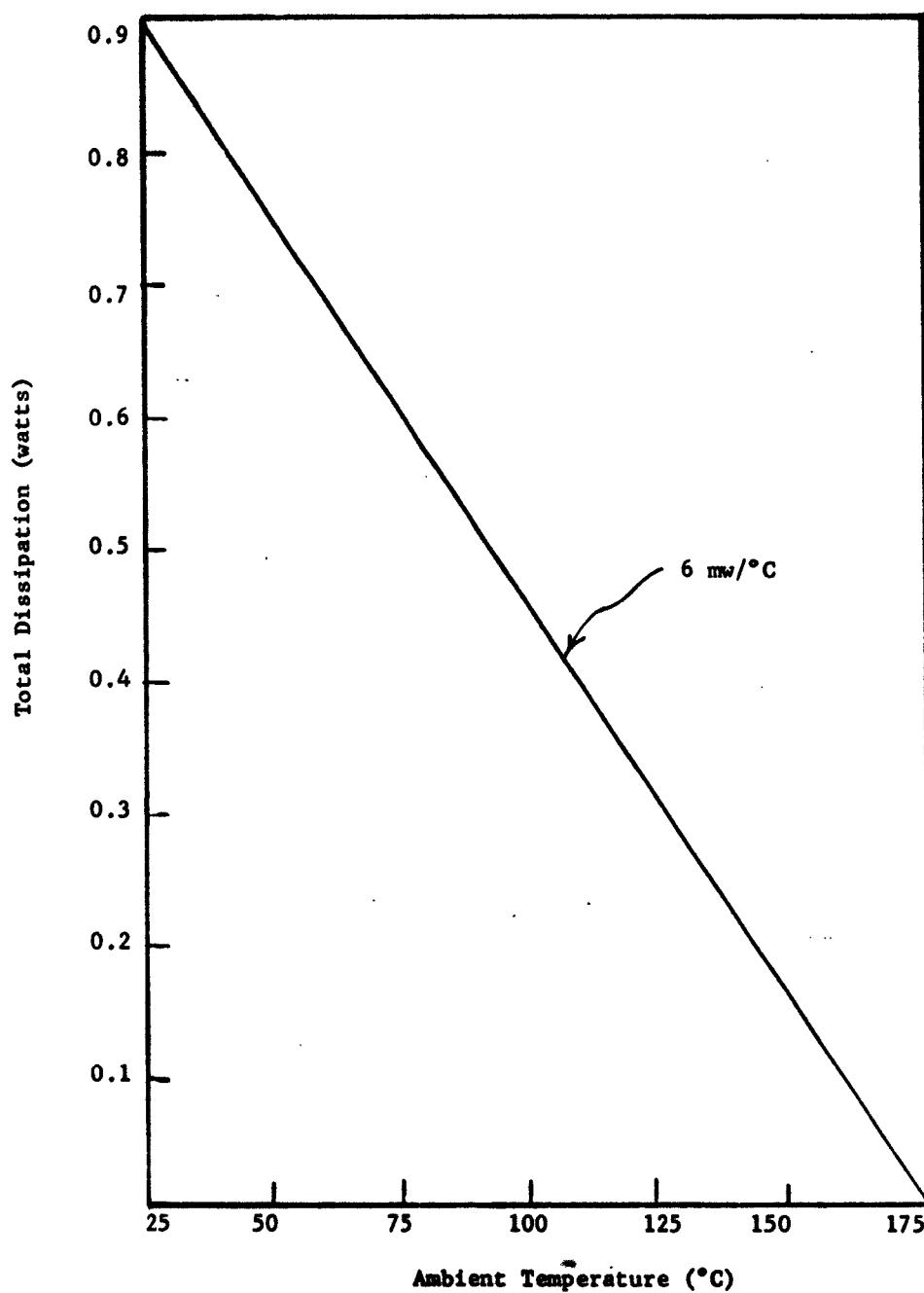
Fig. 2-32.   Free-Air Power Derating Curve for Typical Transistor in TO-5
Package [61]

The small differences in power capabilities that exist among the different types of resistors are of secondary importance and can be neglected. A maximum power dissipation, for a diffused resistor mounted in a standard TO-18 can, has been experimentally measured to be of the order of 3 m w /mil^2 of diffused area [31].

2.3.2.3 Resistor Types and Topology

The properties of the types of resistors listed in 2.2 must be matched against the requirements of the integrated circuit as determined by 2.3.2.1. In addition to selecting the type of resistor that will best meet these requirements, the fabrication process as a whole must be considered. Although one particular type of resistor appears to offer an advantage in performance, the added complexity of fabricating it may make it not the best choice. A second best type of resistor may require no extra processing and perform adequately. Only in circuits in which the quality of performance is limited by the resistor performance is the choice of the former over the latter justified. Such circuits are probably the least attractive to integrate.

The sheet resistivity of the layers of the active regions of the circuit are dictated by the properties of the active components; but these same layers are readily available for building resistors in other areas of the block. The value of the sheet resistivity of a layer restricts the value of resistance conveniently achieved in that layer. For example, a ten ohm resistor is much easier to build in a layer of sheet resistivity of 3 ohms/square than from a layer with sheet resistivity of 400 ohms/square and the reverse is true for a 40 k ohm resistor. If the advantage of no extra processing is to be preserved, a classification according to value in ohms dictates almost immediately which region of the silicon must contain what resistors. It is recommended that a minimum of 10 squares be used in a resistor design.

When matching of sheet resistivity to value in ohms is not completely definitive and some choice remains, a selection according to operating potential generally recommends one conductivity type layer over another in order to obtain the maximum isolation. This criterion is of secondary

importance, since isolation can usually be achieved by one added diffusion step when so required.

Another criterion, whose importance varies from circuit to circuit, is the temperature behavior demanded of the resistor. One region, because of its resistivity (as shown in Figures 2-4 and 2-5) may be superior to another. If the important property is not an absolute value of resistance but a ratio between two resistances, the design must insure that these resistors are fabricated in the same layer. Then, as long as any temperature change is uniform throughout the block, the ratio between the two resistors remains constant in spite of individual changes in value.

The layout of all the elements on the substrate should be such as to minimize the magnitude of all electric fields. A simple ordering of elements on the substrate according to operating potential achieves this objective. If one corner of a rectangular substrate is arbitrarily made the point of highest positive potential, the corner diagonally across from it should be the most negative, and the elements arranged between these corners in order of value of operating potential. An overriding consideration, however, is still that all junctions be properly biased, and nothing recommended here is intended to alter this essential requirement. Some resistors must be isolated from the substrate by a reverse biased p-n junction. These are placed on an area of the substrate at which the substrate potential guarantees that a reverse biased junction will always exist. It is generally preferable to minimize the magnitude of the reverse bias and the element should be so located.

Recapitulating briefly, the number of squares of any given resistor has been determined by the sheet resistivity of the layer in which it is to be fabricated. The size of the square is adjusted so that the total area of the resistor will have the same ratio to the total area of all resistors as its power dissipation has to the total power dissipation of all resistors, i.e.,

$$\frac{\text{Area of Resistor } R_1}{\text{Total Area of all Resistors}} = \frac{\text{Power Dissipation of } R_1}{\text{Power Dissipation of all Resistors}} \quad \cdot$$

The shape of the resistor is now determined by fitting all the elements
together into the required shape and area of the block and placing them
according to the desired substrate potential. To keep the interconnection
paths as short as possible, the ends of each resistor are arranged to
be immediately adjacent to the element to which they are to be connected.
Multiple contacts, representing, for example, 1%, 2%, 5%, 10% changes
in the total length of the resistor may be included to provide a conven-
ient method of trimming if this is required.

2.3.2.4 Fabrication and Test

Once the block is fabricated, but before encapsulation, the
operation should be checked, using probes to make contact to the proper
regions. The optimum operating values of each resistor should be ascer-
tained from among the available taps and the interconnection completed
using these particular values. The interconnection versatility needed
to do this may be a problem, depending on the technique. If wires are
used for all interconnections, no problem exists. When evaporated
interconnections are used, certain additional steps are required. Either
a photo mask is made for several paths of interconnection or a method exists
of making and breaking interconnections made from one mask.   More
discussion of this follows in a later report.

Large increases in values of resistance can be made by thinning
the resistor. This technique is most effective for those resistors
whose thicknesses is of the order of one to three microns. The
technique is to oxidize the top layers of the silicon by one of the
well-controlled oxidation techniques [41] [42] which have been developed
especially for small incremental removal of silicon. The sheet resistiv-
ity of the layer is changed by this process as indicated in Equation (2.9).

The boiling water technique [41] is simply to immerse the silicon
in boiling water, converting a thin surface layer of silicon to silicon
dioxide which is subsequently removed by an HF etch. The reaction is
dependent upon surface potentials but, at distances far removed from

the junction, has been calibrated to remove 34 Å of silicon per step. The removal can be restricted to the resistor area alone by conventional photo masking. Figure 2-33 shows a typical plot of changes in ρ_s vs number of boiling water-HF etches [43].

The anodic oxidation technique [42] for removal of small increments of silicon is similar but the size of the increment removed with each step is controlled by the anodizing voltage. Much larger increments - hundreds of angstroms - can be removed by this technique. Both techniques are low temperature processes that do not cause appreciable impurity diffusion-unlike the thermal oxidation process which also could be used.

The effectiveness of this removal is most pronounced on thin diffused layers whose impurity distributions are either a Gaussian or a complementary error function type. For example, Table 2.1 lists the average resistivity of a diffused n-type complementary error function layer as .0026 ohm-cm when the surface concentration* is 2×10^{20} and the background concentration is 10^{15}. If the junction depth is 1.0 micron, ρ_s must be 26 ohms/□ by Equation (2.9). Removing 1000 Å from the surface increases $\bar{\rho}$ to .0040 ohm-cm and, of course, changes the junction depth to 0.9 micron. Using these values in Equation (2.9) gives a ρ_s of 44 ohms/□. For this particular diffused layer, a 10% change in thickness results in a 70% change in ρ_s.

2.3.2.5 Performance Evaluation

If the resistance value is different from the design value, process failure modes must be evaluated. Likely modes of failure can be associated with each type of resistor in advance and have been listed under disadvantages in Table 2.5. For example, the most likely cause of failure in a layer-type resistor is poor rectifying properties of the large area junctions by which the resistors are isolated. Present technology cannot guarantee the high yields for large area junctions that are expected for small area, high frequency transistors. The bulk resistor on the other hand does not suffer from this mode of failure at all.

* Concentrations are given in cm^{-3}.
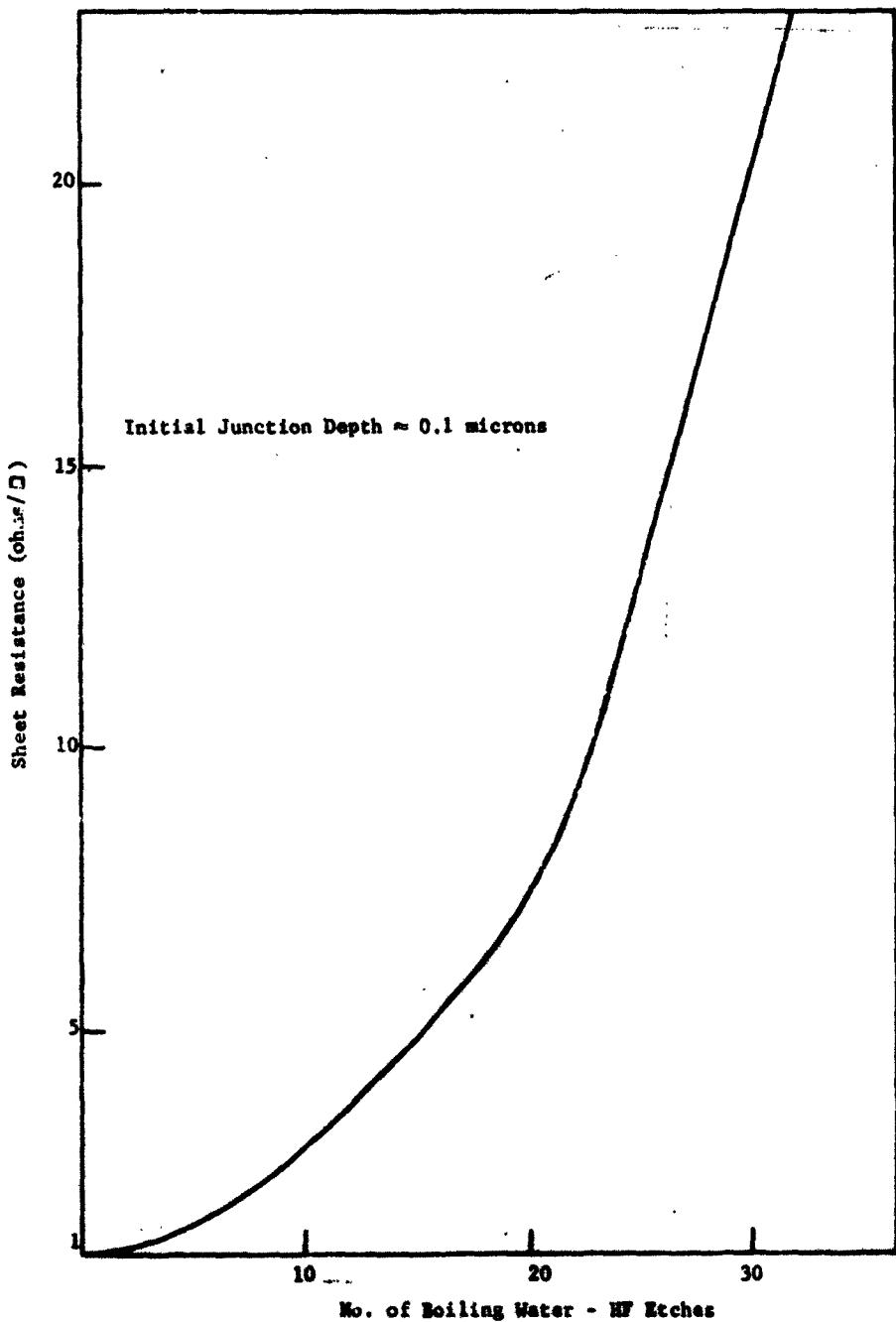
Fig. 2-33. Increase in Sheet Resistance of a Thin Phosphorous Diffused
Layer Caused by Incremental Removal of Silicon, using the
Boiling Water - HF Etch Technique [41]

Statistical tabulation of various failure modes aids in the identi-
fication of unanticipated modes of failure in addition to confirming the
expected. From this knowledge a redesign is possible.

2.3.3 Illustrative Example
    2.3.3.1 Circuit Schematic and Breadboard
        Assume the circuit of Figure 2-34 has been breadboarded and the
given values of resistance and power dissipation were obtained. Assume
further that the minimum isolation resistances shown by the dashed paths
in Figure 2-34 have been established experimentally from the breadboarded
circuit. These values are determined by placing external resistors
between the indicated points and recording the minimum value of resistance
at which the circuit still operates according to specifications. This
value becomes the minimum isolation resistance between those points.

The transistor characteristics establish doping levels of the
various regions and are assumed to be the following:

Regions	Sheet Resistance
n-type emitter (phosphorous)	10 ohms/□
p-type base (boron)	400 ohms/□
n-type collector	100 ohms/□

Resolution limitations, as dictated by the photo engraving process,
are arbitrarily assumed to be:
    1. A minimum line width of one mil.
    2. A minimum area for lead attachment of four square mils.

    2.3.3.2 Package Type and Size
        The power dissipation of the circuit is essentially that of the
transistor so that a standard transistor package should be adequate.
Since four leads are required, an acceptable package is a four pin
transistor header, all leads of which are insulated from the header.
For this package the shape of the block should be square ≈ 110 mils on
a side for the TO-5 header. The size of the transistor is determined
from transistor performance data; for illustrating the example it can

Small Signal Amplifier
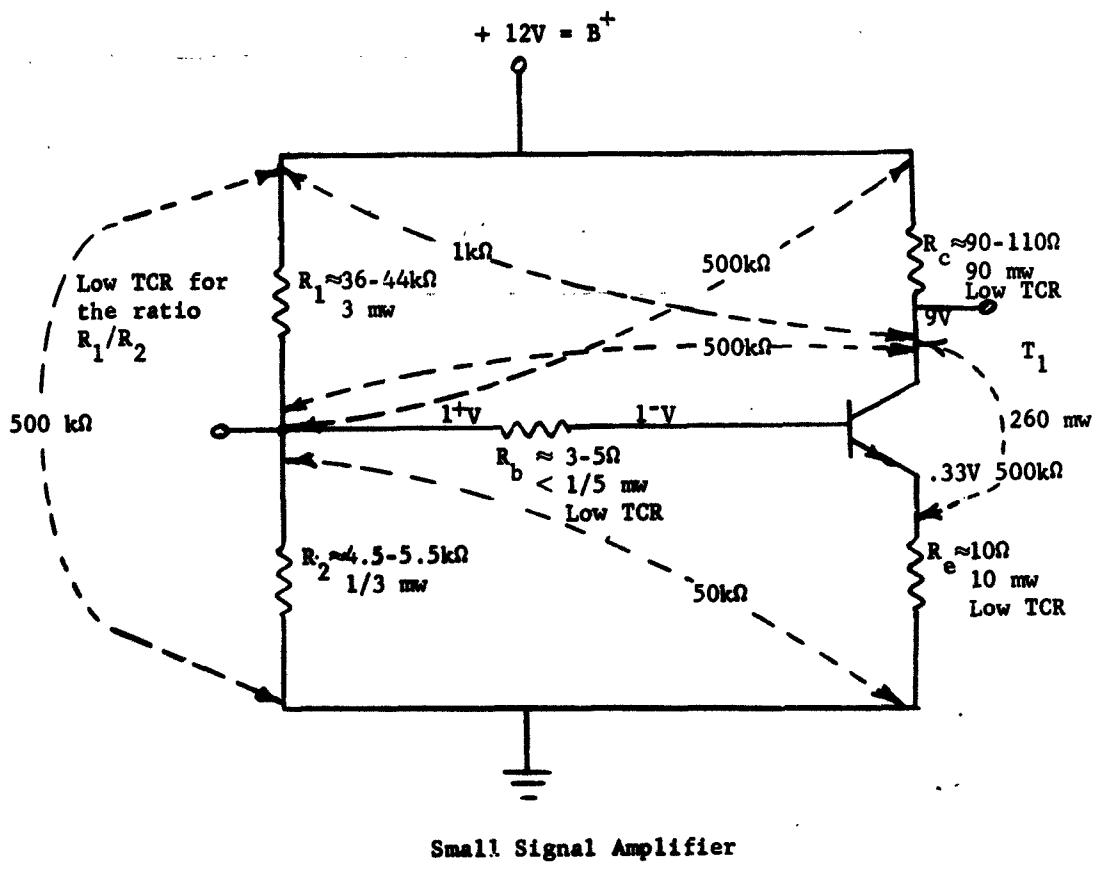
(The resistors have been chosen to have a wide variety
of values, operating potentials and couplings. The
transistor beta must be in excess of 100 for operation
at the indicated levels.)

Fig. 2-34. Schematic Circuit of the Illustrative Example. The Resistive
Values Shown by the Dashed Lines are the Minimum Isolation
Resistances Required Between the Points Indicated

be set at some arbitrary value, say 13 mils by 30 mils. The ratio of power dissipation between the resistors and transistors places a minimum desired value of area on the resistors of:

$$\frac{\text{Resistor Dissipation}}{\text{Transistor Dissipation}} = \frac{\text{Resistor Area}}{\text{Transistor Area}}$$

$$\frac{104}{260} = \frac{\text{Resistor Area}}{390}$$

$$\text{Resistor Area} = 157 \ \text{mils}^2$$

2.3.3.3 Resistor Types and Topology

The transistor of the circuit includes a p-type base region with ρ_s equal to 400 ohms/$\square$, an n-type emitter region with ρ_s equal to 10 ohms/$\square$, and a substrate with ρ_s equal to 100 ohms/$\square$ (1 ohm-cm bulk resistivity, 4 mils thick). These are arbitrary but typical values of a double diffused transistor. The exact values are unimportant and do not alter the procedure. By matching the available sheet resistivities with the desired values of resistance, the following conclusions can be made: R_e and R_b must be fabricated in the emitter layer; R_c can be fabricated in either the n-type emitter layer or the n-type substrate; and R_1 and R_2 can be fabricated in either the p-type base layer or the n-type substrate. The only consideration used to draw these conclusions is the feasibility of achieving a given value of resistance from the sheet resistances of the available regions. Less than one square amplifies geometrical errors and has been avoided whenever possible.

The operating potential of R_c is between 12v and the collector voltage which is around 9v as shown on the schematic. A logical choice then is to select the n-type emitter layer to make this resistor so that the resistor is reverse biased with respect to the p-type region isolating it from the substrate. Its cross section can be depicted as shown in Figure 2-35. The two contacts to the n-type layer are the resistor electrodes. The isolating p-type layer is shown shorted to the substrate by an ohmic contact at the surface. The purpose of this is to prevent a large voltage from building up across this junction and to avoid any transitor coupling between the resistor and the substrate. If no

■ — ohmic contact
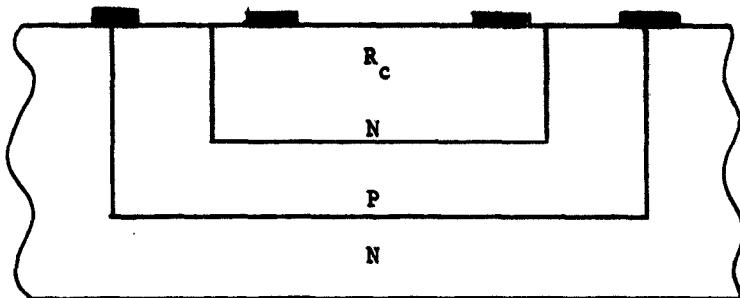
Fig. 2-35. R_c in n-type Emitter Layer With Ohmic Contacts Shorting the
p-type Base Region to the n-type Substrate

contact were included, the p-type layer would be floating as shown in
Figure 2-36. The schematic representation of this structure is shown
in Figure 2-37. Shorting the p-type isolation layer to the substrate
short circuits the base collector junctions of all the transistors
shown in the equivalent circuit so that the equivalent circuit becomes
similar to that drawn for a single diffused layer in Figure 2-18, even
though there is a second junction. The effect of the extra region is
only to alter the values of R_S and C in the equivalent circuit of
Figure 2-18.
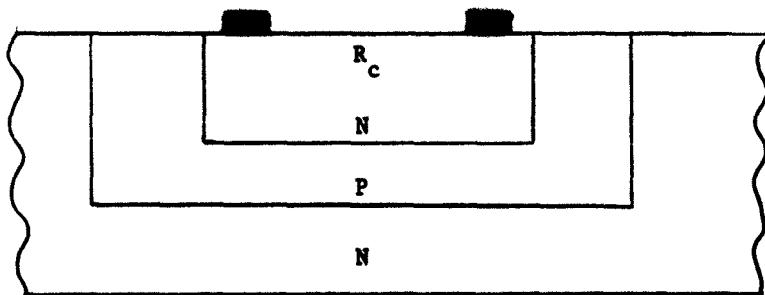
Fig. 2-36. Same as Structure of Fig. 2-35 Without Shorting Contacts
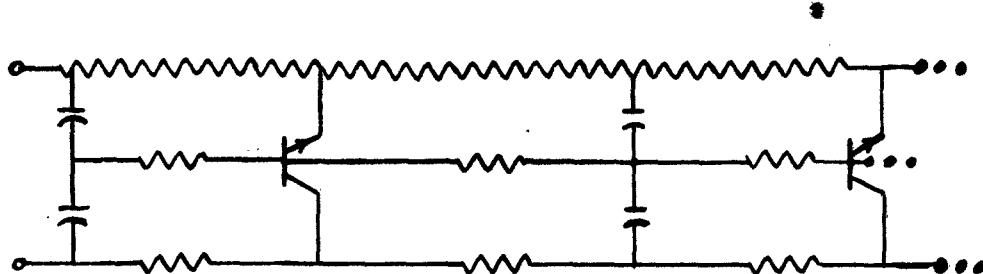
Fig. 2-37. Equivalent Circuit for a Resistor Formed by the Same Diffusion as the Emitter of a n-p-n transistor (Structure shown in Fig. 2-36.)

The breakdown voltage of the junction between the n-type layer and the p-type layer is low - typically about 5-8 volts, since it is the same as the transistor BV_{EBO}. With the junction shorted, the p-region is fixed at the substrate voltage which should be close to the collector voltage of 9v. Since one terminal of R_c will also be at the collector voltage, the position of R_c on the substrate must be over a region of potential less than the collector voltage; that is, the substrate should be operating at slightly less than collector voltage in the vicinity of R_c to assure that the p-n junction defining R_c is always reverse biased.

When no region of the substrate is operating below the collector voltage, one end of the resistor can be shorted to the substrate as shown in Figure 2-38. Contact c is the resistor contact, the collector contact, and the interconnection between them - three functions in one contact.
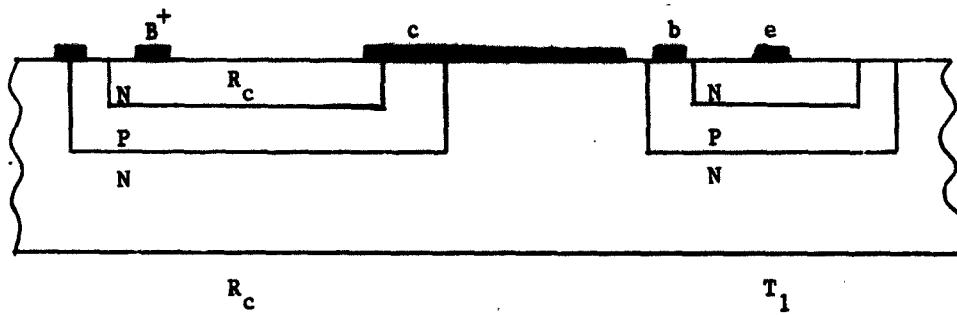
Fig. 2-38. The Use of a Shorting Contact, c, to Fix the Potential of an Isolating Region and at the Same Time Make the Circuit Connection from R_c to the Collector of T_1

The operating potential of R_1, the upper base bias resistor, is between 12v, the supply voltage, and 1v, the nominal value of the base voltage as shown in the schematic; and the operating potential of R_2, the lower bias resistor, is between 1v and ground. The high sheet resistance of the substrate seems well suited for these resistors. The usual objection to such layers is that the TCR is high ≈ 5000 ppm/°C. For this particular circuit, however, the primary temperature requirement is that the ratio of $\frac{R_1}{R_2}$ be constant with temperature. If the block can be assumed to be isothermal in operation, the objection to a high TCR no longer exists. The only design restriction imposed by the temperature requirement is that R_1 and R_2 be fabricated in the same regions.

Two further objections exist to using the substrate for R_1 and R_2. The first is simply the areas involved. The 400 squares of substrate needed to form R_1 are prohibitively large; even if one side of the square is taken to be the smaller of the two transistor dimensions, an impractically large structure is needed (400 × 13 mils = 5200 mils). The problem can be lessened by reducing the thickness of the n-type substrate below the four mils used to calculate the sheet resistance. A very convenient technique for accomplishing the reduction in thickness is to make the n-type collector region an epitaxial layer on a p-type substrate. The electrical properties of the substrate are unimportant except that a good quality p-n junction be formed with the epitaxial layer. If the epitaxial n-region is made 10 microns thick, the sheet resistance becomes 1000 ohms/□ and only 40 squares are needed for R_1 and 5 squares for R_2.

A second objection still remains - the use of R_1 and R_2 in the base circuit of the schematic necessitates additional isolation as discussed in 2.2.1. An encircling portion of the n-type epitaxial region must be completely converted to p-type so that the resistor is bordered on five sides by a p-type region (the sixth side is the top surface to which contact is made). A common technique for accomplishing this selective conversion is to diffuse a p-type impurity through an appropriate oxide mask so as to cause conversion to a depth at least as great as that of the epitaxial layer. This is shown in Figure 2-39. Regardless of the

ohmic contacts
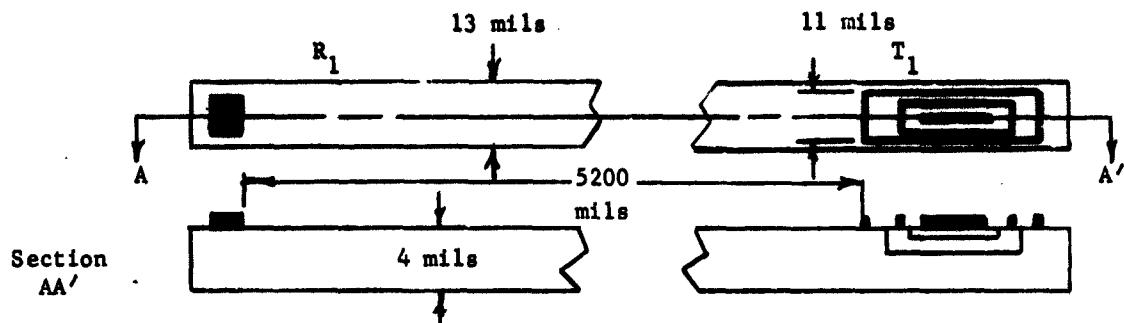
(a) Fabrication of R_1 (= 40K) in 1 ohm-cm n-type Substrate
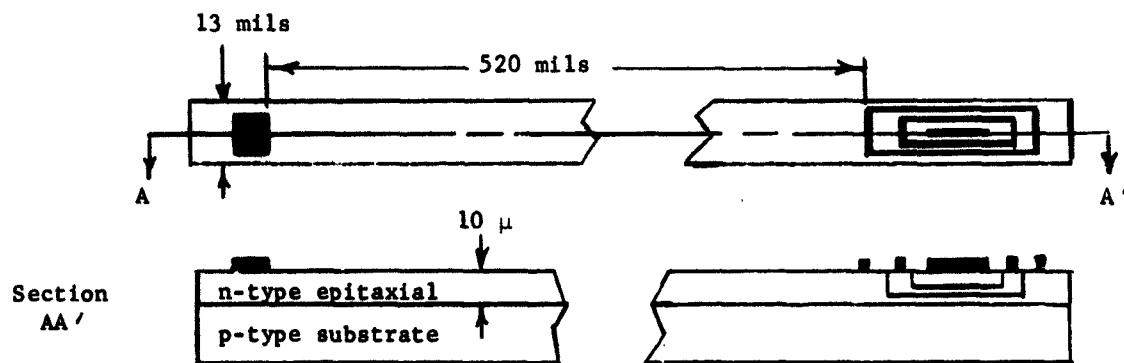
(b) Fabrication of R_1 in 1 ohm-cm n-type Epitaxial Layer
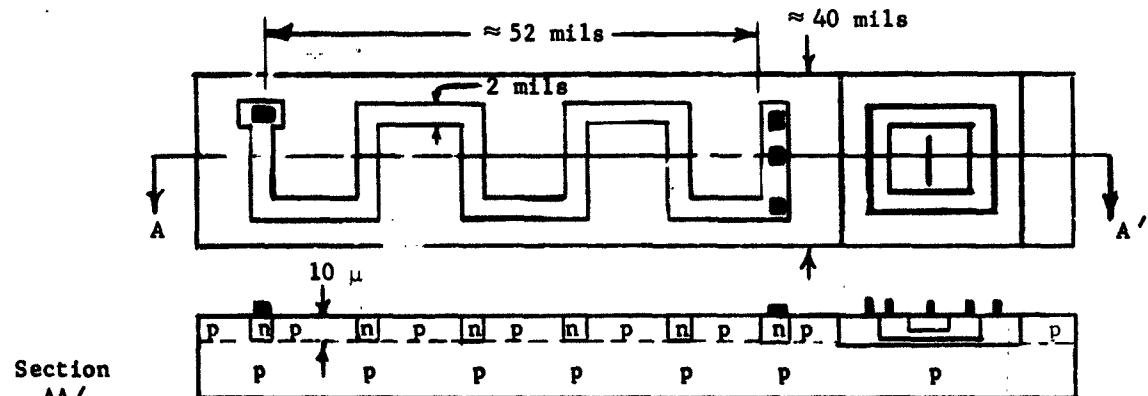
(c) Same as (b) with the Addition of a p-type Diffusion for Isolation

Fig. 2-39. Design Methods for R_1

potential of the p-region between the collector region and the resistor region, the reverse resistance of a junction will separate them. However, the most stable design is one that avoids floating potentials; and whenever possible, all regions should be tied to a fixed value of potential or else to the potential of a certain point of the circuit. Circuit performance should be more reproducible when this is done than when regions are left floating. Fluctuations in reverse bias may not alter the reverse resistance of an isolating junction appreciably but other parameters such as capacitance may vary. In general the p-type substrate of epitaxial blocks should be at the lower potential of the circuit to insure the existence of a reverse bias on the junction between the n-type epitaxial layer and the p-type substrate. In the structure of Figure 2-39 the lowest potential is zero so the substrate should be grounded.

An added advantage of the isolating step is that the flexibility and accuracy of the photo engraving process can be added to the n-type epitaxial layer and the size of a square can be greatly reduced. Forty squares is now a very practical size. An arbitrary geometry becomes possible rather than the elongated geometries shown in Figure 2-39a and b.

The conclusion is that R_1 and R_2 can be formed in the n-type collector silicon only as epitaxial resistors involving the additional steps just outlined. To avoid the use of epitaxy, although it may be desirable for other structure elements, the p-type base region of the original double diffused structure should be investigated as a source region for R_1 and R_2.

If fabricated in the 400 ohms/□ p-type base layer, R_1 must be 100 squares and R_2, 12.5 squares. This is no problem because the size of a square is limited only by the photo-masking and the allowable tolerance. The area of one square could be one square mil, since the power dissipation would then only be $40\mu watts/mil^2$. This is a modest requirement in view of reported values [31] of 3 milliwatts/mil^2. The operating potential, however, is such that the portion of the isolating junction of R_1 above the collector voltage will be forward biased. This introduces another path between the B^+ supply and the collector contact. This new path is in parallel with R_c previously planned. Several alternatives exist:

1.) If the B^+ contact is made so as to short the end of the p-region of
R_1 to the substrate as shown in Figure 2-40, the resistance between
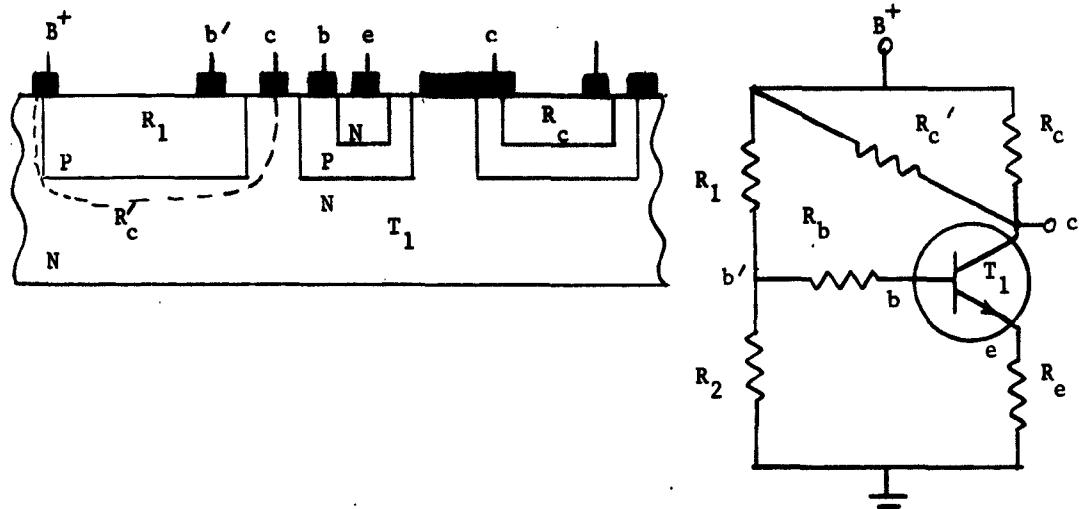
Fig. 2-40. Placement of B^+ Contact to R_1 so as to Make the Collector Resistor
a Parallel Combination

B^+ and the collector contact c appears in parallel with the
previously planned R_c. R_c' represents the added resistance in
parallel. In this design the collector resistance of the circuit
is a parallel combination of R_c and R_c'.

2.) If the B^+ contact is placed totally within the p-region as shown
in Figure 2-41, the path placed in parallel with the original R_c
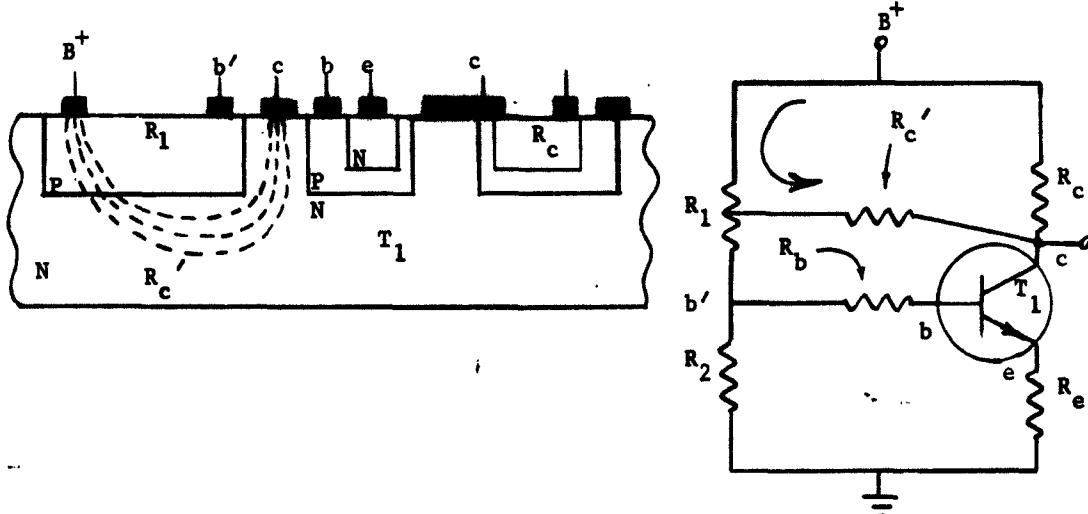
Fig. 2-41. Placement of B^+ Contact to R_1 so as to Make the Collector Resistor
a Series Parallel Combination

is a series combination of a portion of R_1 and an n-type bulk resistor; and the collector resistance becomes a series parallel combination type resistor.

3.) Still another alternative is to eliminate the originally planned R_c and replace it with one of these paths that arise naturally as a result of fabricating R_1 in the p-region. Planning R_c totally in the bulk could be accomplished easily enough by arranging to have one square of substrate between B^+ and c as shown in Figure 2-42 for the general case.
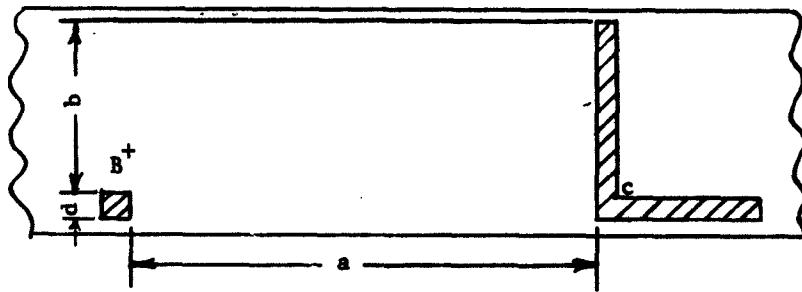
Fig. 2-42. By Varying the Dimensions a and b, the Effective Number of Squares Between the Electrodes can be Adjusted

Given the collector contact length and the size of the contact between B^+ and the substrate, the dimensions a and b can be adjusted to yield one square of effective resistance. The simplest method of determining the values of a and b is to cut the pattern out on a resistance paper such as Teledeltos* and measure the value directly as a function of a,b. For one square, a ≈ d.

Principal shortcomings of building R_c by this method alone are the failure to meet the requirement of a low TCR and the tolerance limitation when using one square resistors.

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* Trade name, Western Union. Available from Art Cote, 390 Coit Street, Irvington 11, New Jersey.

The second fabrication scheme, in which the B^+ contact is totally within the p-region (illustrated in Figure 2-41), results in a resistive path which can be broken into two series components as discussed in 2.2.5. The first portion is in the p-region; the second, in the bulk n-region. If the p-region were gallium doped, the combination would produce a very satisfactory TCR over a limited temperature range as indicated in Figure 2-28. The temperature dependence of the n-type substrate is similar to that of a boron doped epitaxial layer; so that the top curve of Figure 2-28, showing the variation with temperature of a series combination of a gallium-doped, diffused resistor and a boron-doped, epitaxial resistor, is a reasonable approximation of the temperature dependence of R_c when fabricated as shown in Figure 2-41 (if the p-type dopant is   gallium).

4.) Another possible solution is to accept the parallel combination of elements such as shown in Figure 2-40 or 2-41 but to make R_c' so high as to be negligible. The simplest, practical way to insure such a high value of R_c' is to build the circuit on an n-type epitaxial layer instead of on the n-bulk region directly. The value of R_c' then should be one to two orders of magnitude higher than R_c.

R_2, operating between 1 volt and ground, is always at a lower potential than the substrate and can be fabricated in 12.5 squares of p-layer and is placed over the lowest substrate voltage available.

Typical layouts for these combinations are shown in Figure 2-43 (using an epitaxial substrate) and Figure 2-44 (using a homogenous n-type substrate). In both illustrations R_b and R_e are formed in the n-type emitter region. The size of both these resistors is limited not by power dissipation but by the technology of the processes. For these illustrations one mil is taken as the minimum dimension of diffused regions. A resistor width of one mil is approaching the dimensional magnitude of the diffusions depths so that allowance for lateral spreading under the oxide mask becomes of geometrical importance [44]. The lateral spreading can be assumed to be equal to the junction depth of
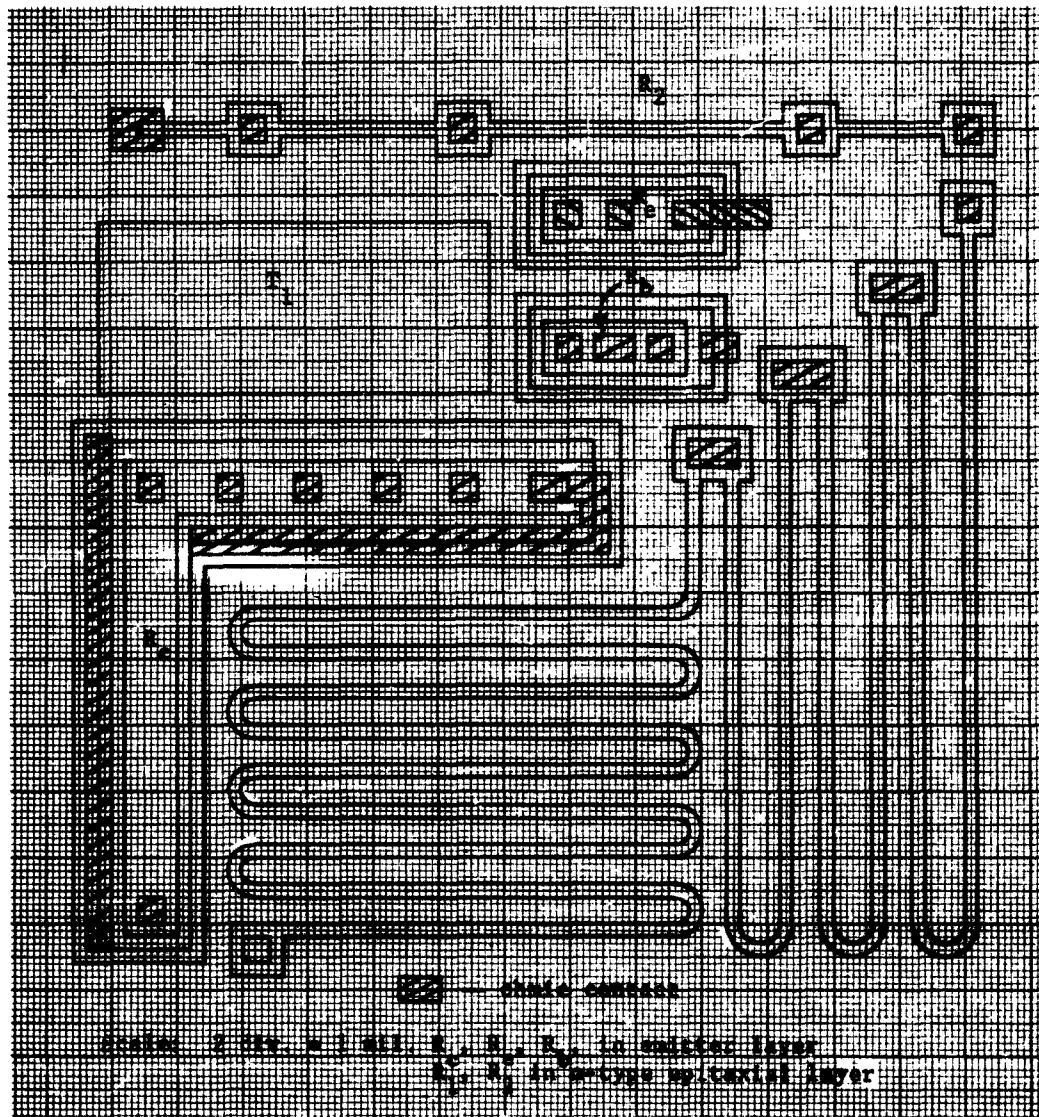
Fig. 2-43. A Possible Design of the Circuit of Fig. 2-34 Utilizing an
n-type Epitaxial Layer on a p-type Substrate
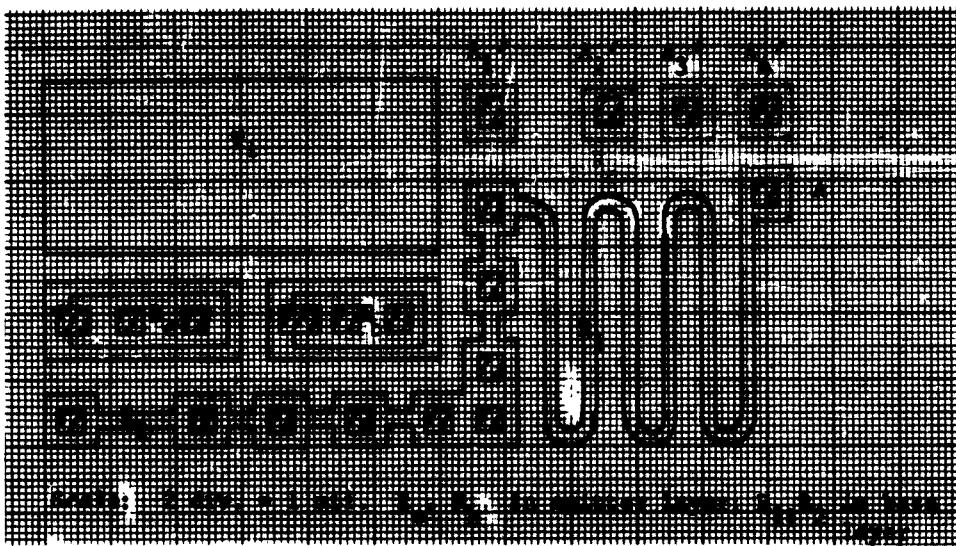
Fig. 2-44. A Possible Design of the Circuit of Fig. 2-34 utilizing a
1 ohm-cm n-type Substrate

the diffused layer, and the change in dimensions can be calculated in
advance. The dimensions of the photo masks should be altered to allow
for the calculated spreading. A second size limitation arbitrarily
assumed, is that all contact areas are required to be at least two mils
in each dimension. Many techniques exist that can hold considerably
finer tolerances than this. Areas as small as .3 mil stripes have
been successfully bonded with .2 mil diameter wire [45]. The use of
an evaporated lead to connect a small area to a large metal area
suitable for easy bonding has permitted contacts to be made to areas
as small as 1/4 mil by 3 mils [46]. While these techniques do not
affect the resistor properties directly, they are factors in the design.
Obviously the resistor is worthless if no contact can be made to it.
The restrictions in size illustrated in Figures 2-43 and 2-44 are undoubt-
edly conservative.

R_c in Figure 2-43 is in the n-type emitter region. R_1 and R_2 are
in the epitaxial n-region. To avoid floating junctions and undesired

couplings between the resistors and the regions isolating the resistors, ohmic contacts are placed so as to short some of the junctions. As shown in Figure 2-45, the contact to the collector end of R_c is shorted to three regions. The purpose of the shorting contact is:

(1) To prevent transistor or switching action occuring between the regions.

(2) To fix the potential of the isolating regions at the collector potential.

The shorting contact surrounds the entire resistor but includes only the two middle regions away from the collector end of the resistor. The B^+ end of R_c is more positive than the collector end so that the n-region in which R_c is realized is more positive than the p-region beneath it (except at the collector end where the two regions are biased to some known value). The substrate is grounded.

To calculate the value of the half circular turns of R_1, Equation (4.2) is used, setting A = r and B = 2r where r is the inside radius, 2r the outside radius, and r = w, the resistor width. The result follows immediately:

$$R = \rho_s \frac{\pi}{\ln B - \ln A} = \frac{\rho_s \pi}{\ln \frac{B}{A}} = \rho_s \frac{\pi}{0.69} \approx 4.5 \, \rho_s \qquad (2.15)$$

The effective number of squares of each 180 degree turn is 4.5.

With the epitaxial type structure, there is no need for arranging elements according to operating potential since the substrate is generally inactive. Its only function is to provide electrical isolation and mechanical strength. Ideally, it should be an equipotential and have no current flow within it. Under these conditions the placing of elements on the substrate is unimportant so far as biasing for isolation goes (the shorting contacts have ensured the isolation) and the elements can now be arranged so as to best fit into a given area and to minimize the length of the conducting interconnections.
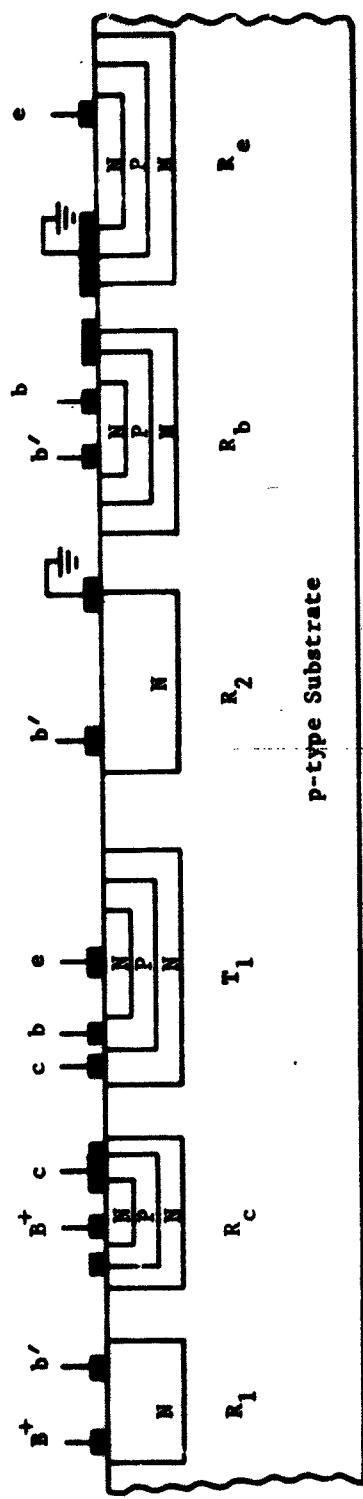
Fig. 2-45. The Cross Section of Each of the Elements of Fig. 2-43
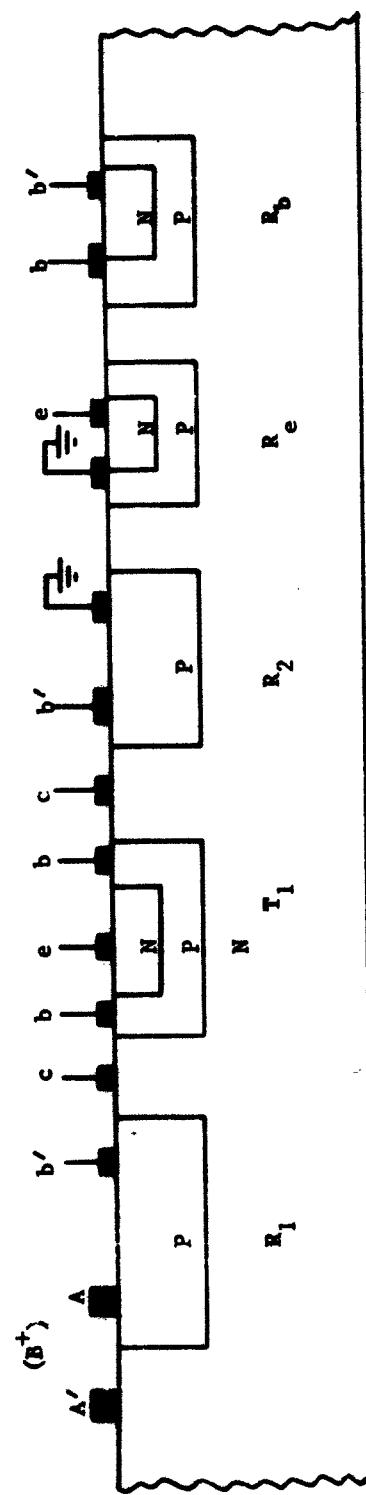
Fig. 2-46. The Cross Section of Each of the Elements of Fig. 2-44

Multiple contacts are shown on each resistor so that the value can be trimmed simply by changing conductor patterns from one contact to another. This flexibility allows some redesign after the circuit is fabricated and can also compensate for minor variations in the sheet resistivity of the diffusions.

The use of an epitaxial substrate can be avoided by building R_1 and R_2 into a p-type layer formed during the same diffusion as the base region of the transistor. R_c can be fabricated the same as before (with contacts placed as in Figures 2-35 or 2-38) or it can be fabricated in the substrate as a bulk resistor (Figure 2-40) or a series combination of p-layer and substrate (Figure 2-41). These last two possibilities are illustrated in Figure 2-44, employing a 1 ohm-cm n-type substrate. The choice of taps determines whether R_c is a bulk resistor (Figure 2-40) or a series combination (Figure 2-41). If the B^+ lead is brought into point A only, the path constituting the resistance R_c between A and the collector contact is partly in the p-region of R_1 and partly in the substrate, making a series combination type of resistor. If the B^+ lead is also brought to points A_1', A_2', A_3', or A_4' the resistor R_c will be completely in the substrate since the p-region of R_1 will be reverse biased everywhere except at the contact.

Since the substrate is active in this design, the placing of elements according to operating potential is an important consideration. To minimize the magnitude of the reverse bias on the junctions isolating R_2, R_e, and R_b from the collector, these resistors should be placed over the lowest substrate voltage available. Since the collector voltage is the lowest substrate potential and the region under the B^+ contact is the highest, R_e, R_b, and R_2 should be placed on the opposite side of the transistor from the B^+ contact.

The low voltage ends of R_b and R_e are shorted to the p-regions separating the resistors from the substrate. As before, the reason for this shorting contact is to remove unwanted transistor coupling and to fix the potential of the otherwise floating p-type regions.

Taps A_1', A_2', A_3', A_4' for R_c are simply ohmic contacts to the substrate at various distances from the transistor. If silicon is heavily

doped, the problem of making an ohmic metal-semiconductor contact is reduced. This heavy doping of N^+ on the n-type substrate can be conveniently achieved by a masked diffusion during the same step that forms the n-type emitter of the transistor. The areas of N^+ surrounding all substrate contacts are shown as dashed lines. Only two diffusions are needed for the structure of Figure 2-44, as shown in Figure 2-46. It is small and simple to make but its performance is limited by the tolerances and the TCR of R_c.

2.3.4 Commercial Examples
2.3.4.1 Conventional Approach

Among the earliest commercially available integrated circuits were Texas Instruments' Series 50 solid circuits and Fairchild's micrologic blocks. The SN-504 is a diode-resistor gate sold by TI which employs a gallium diffused silicon resistor of 2kΩ nominal value. Typical plots of resistance versus temperature for these resistors are shown in Figure 2-47. Figure 2-49 is a photomicrograph of Fairchild's half shift register, one of the micrologic blocks. The collector node resistors are nominally 600 Ω and are the diffused p-type regions at the right of the photo. The bottle shaped base region of each transistor is a 300 Ω base resistor. A schematic of this block is sketched in Figure 2-48.

Later examples of silicon resistors in integrated circuits are shown in Figures 2-50 to 2-57. These are all epitaxial-type structures in that the substrate region is inactive and contributes only mechanical strength and electrical isolation to the block.

The equivalent circuit of the amplifier block shown in Figure 2-51 is drawn in Figure 2-50. All resistors have multiple taps, some of which are located at corners. The contacts at the corners serve not only as taps but also as low resistance regions which prevent the high current densities that could otherwise exist in the neighborhood of a sharp turn. Various ohmic contacts to the regions isolating the resistors have been included, permitting external control of the bias across the isolating junctions. All resistors except the emitter resistor are in p-type layers diffused the same as the base region of the transistor. The emitter

resistor is an n-type layer diffused at the same time as the transistor emitter. The number 33 identifies the position of this circuit on the silicon wafer.

Figure 2-52 is an equivalent circuit of the logic block shown in Figure 2-53. The layout of elements is illustrated in Figure 2-58. Resistors R_1 and R_2 have circular corners to avoid high current densities. The elements are arranged according to operating potential even though the block is an epitaxial type substrate. The point of highest potential B^+ is at the top of the block and the lowest potential, 0 v, appears on the emitter on the transistor T_2 shown at the bottom. The regions of transistor T_1 operate at various levels between the two extremes so T_1 is placed in the center of the block.

The equivalent circuit in Figure 2-52 depicts the capacitance and rectification of the diffused resistors similar to that shown in Figure 2-18. The symbol for distributed capacitance in Figure 2-52 has replaced the infinite series of parallel capacitors of Figure 2-18. From Figure 2-52 the inference is that the rectifier is in series with the distributed capacitance. What is meant is that the rectification and capacitance are distributed in parallel as shown in Figure 2-18.

Figure 2-55 shows a section of an integrated circuit which can be presented schematically as in Figure 2-54. The emitter resistors are the dumbell shaped regions in the center of the photograph. The oxide covering the resistors provides dc isolation between the leads deposited on top of the resistors and the resistors themselves. However, additional ac coupling does exist because of the MOS type structure formed between the leads, oxide, and silicon resistors.

Figure 2-56 shows a differential amplifier block and schematic. The collector resistors at the top of the photo have nominal values of 10 k ohm and must be as closely matched in value as possible. The emitter resistors in the center of the photo should also be closely matched. The use of a fraction of a square shown here sometimes makes such matching difficult. Figure 2-57 is a photomicrograph of a binary element. The schematic includes two capacitors which appear at the top of the photo and are probably of the MOS variety. The area of the block
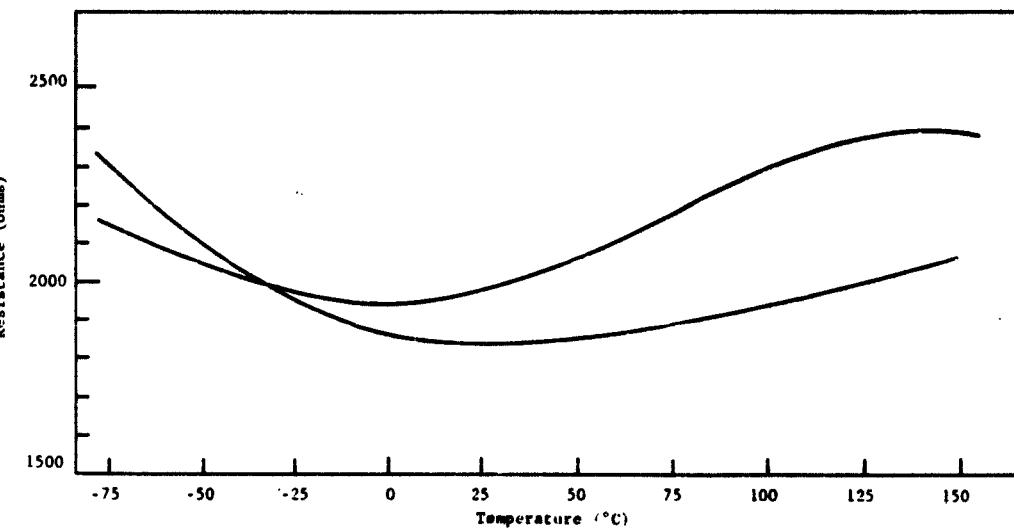
Fig. 2-47. The Temperature Dependence of Diffused Silicon Resistors for
Diode-Resistor Gate SN-504 [30]
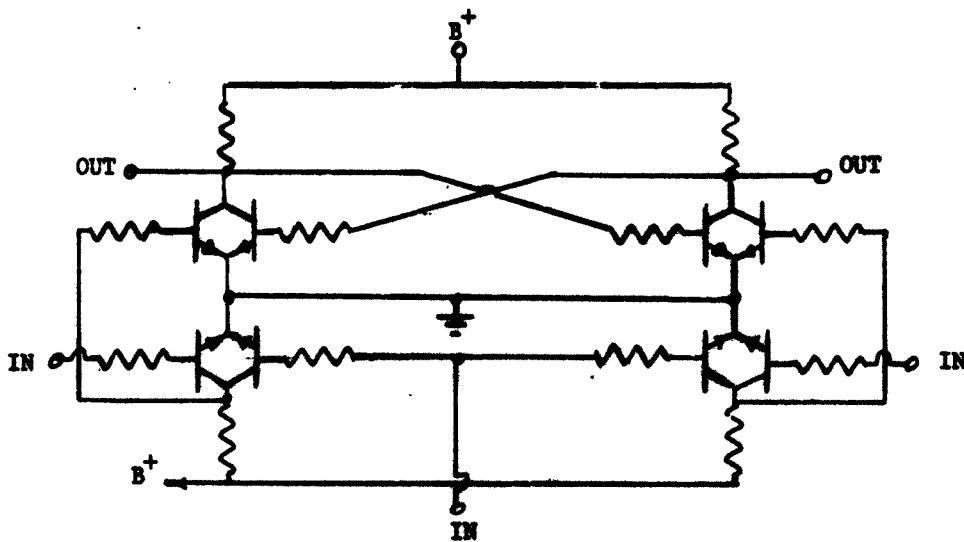
Fig. 2-48. Schematic of Fairchild's Half Shift Register Micrologic Block
(pictured in Fig. 2-49)
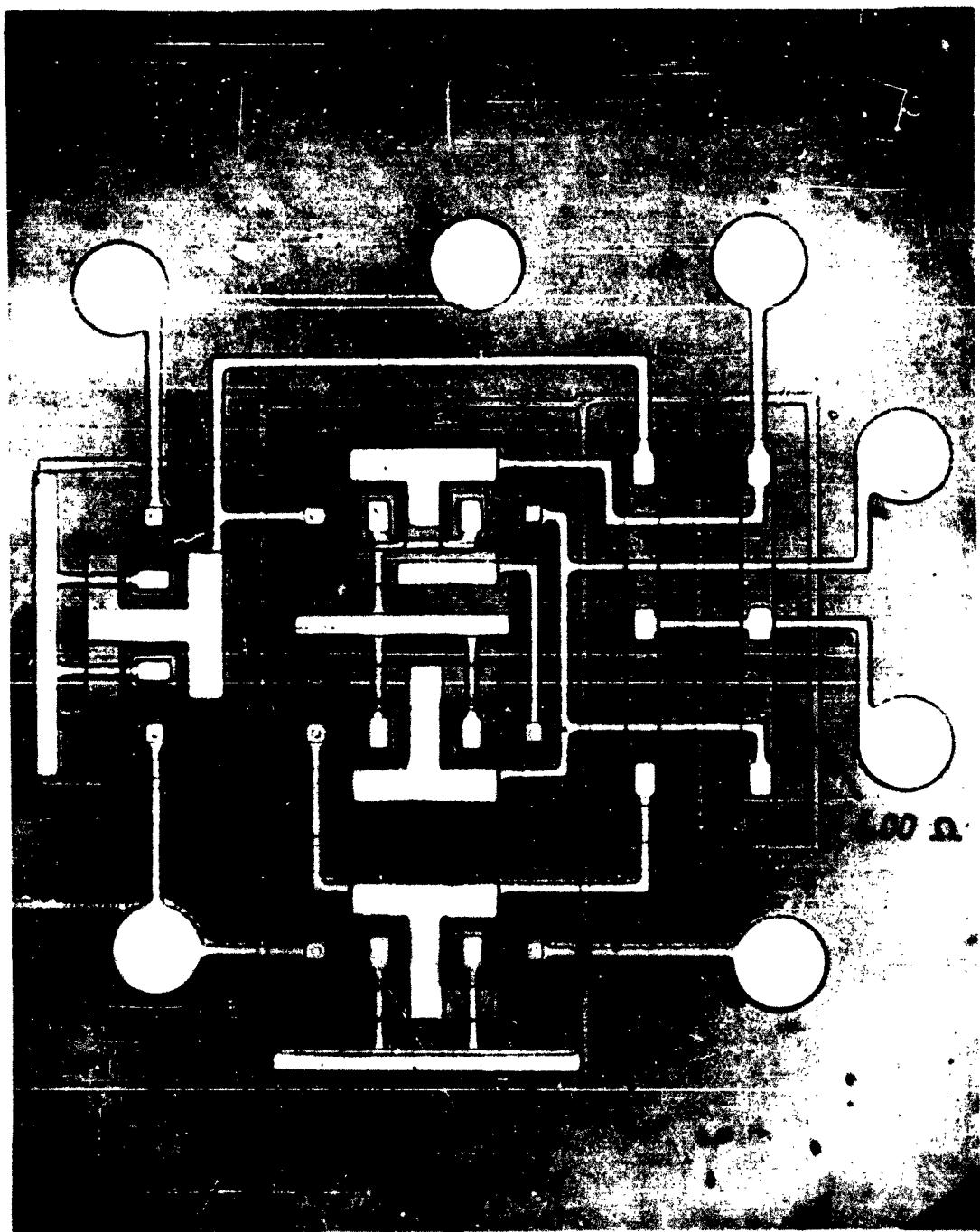
Fig. 2-49. Half Shift Register Element (courtesy of P. N. Schink,
Fairchild Semiconductor Corp., Mountain View, California
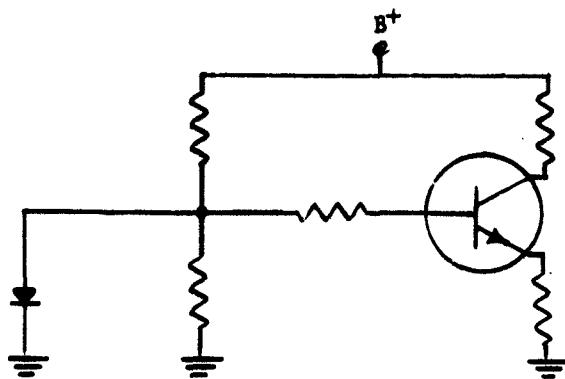
Fig. 2-50. Schematic Diagram of Block Pictured in Fig. 2-51
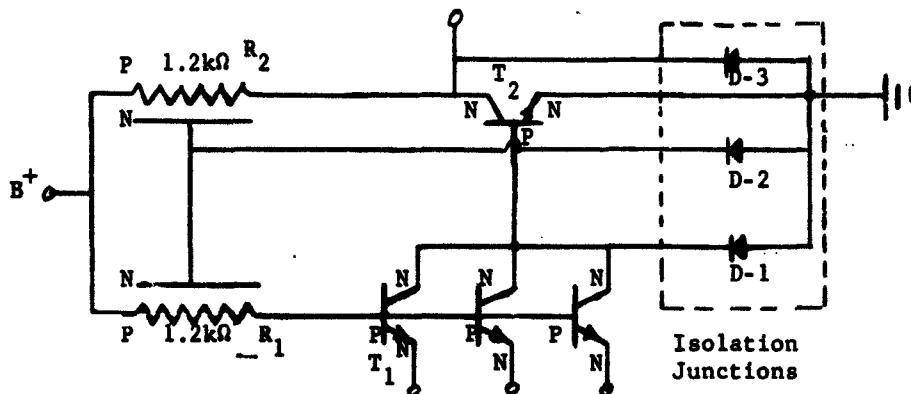
Fig. 2-52. TTL Logic Block-Equivalent Circuit of One Section. (Courtesy
of E. G. Shower, Sperry Semiconductor Division of Sperry Rand
Corp., Norwalk, Conn.
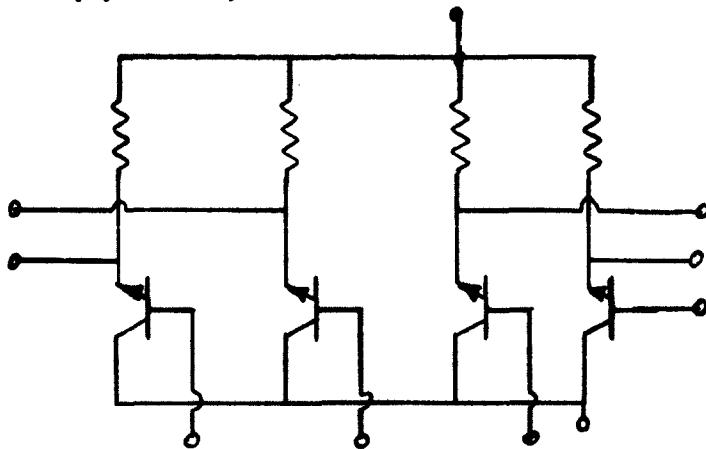
Fig. 2-54. Schematic of the Integrated Circuit Pictured in Fig. 2-55

Fig. 2-51. Low Level Amplifier
(Courtesy of M. N. Giuliano,
Westinghouse Air Arm Division,
Baltimore, Maryland)
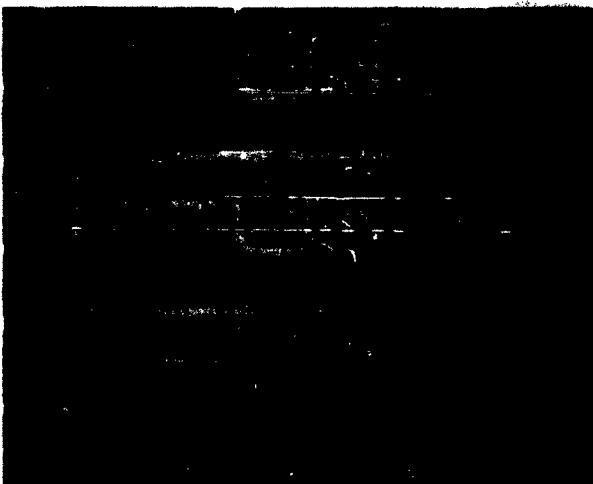
Fig. 2-53. TTL NOR Gate Block
(Courtesy of E. G. Shower,
Sperry Rand Corp., Norwalk,
Connecticut)
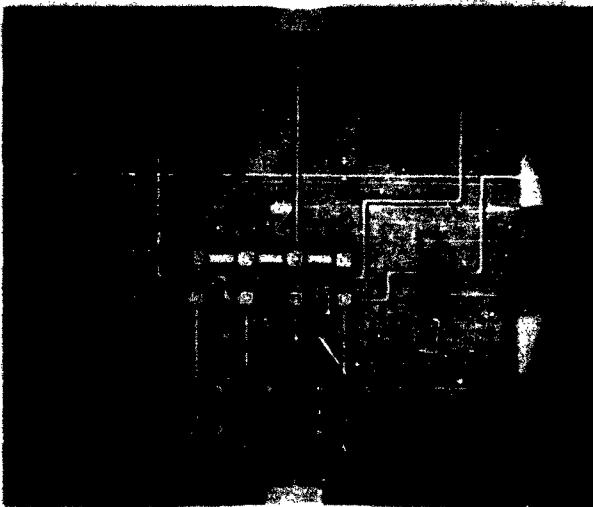
Fig. 2-55. Integrated Logic
            Circuit
(Courtesy of H. K. Dicken,
Motorola Semiconductor Pro-
ducts Division, Phoenix,
Arizona.)
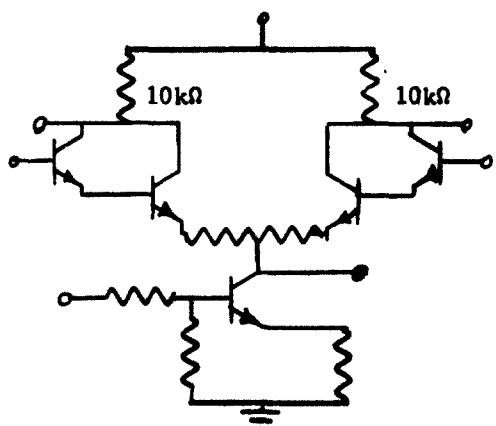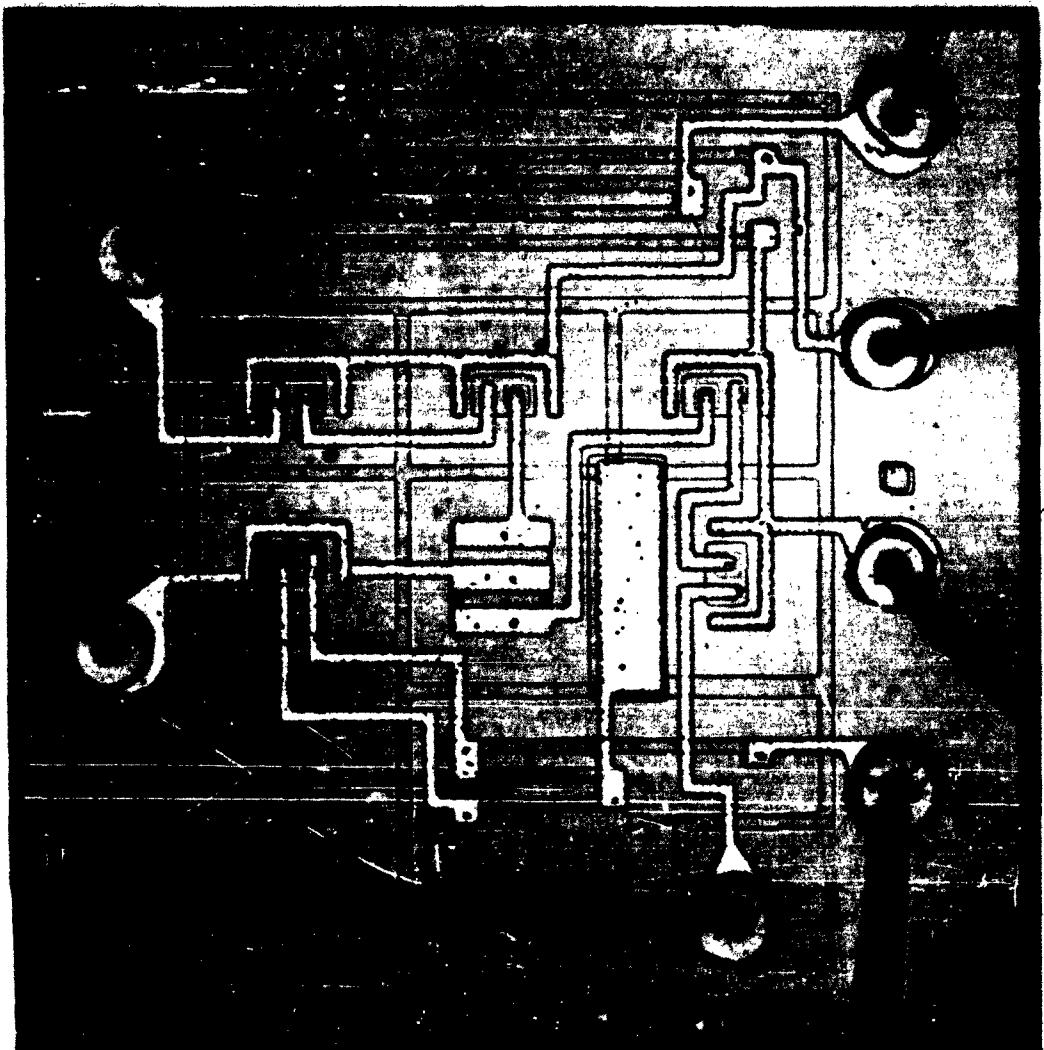
Fig. 2-56. DA 101 Integrated
Differential Amplifier
(Courtesy of P. N. Schink,
Fairchild Semiconductor Corp.,
Mountain View, California)
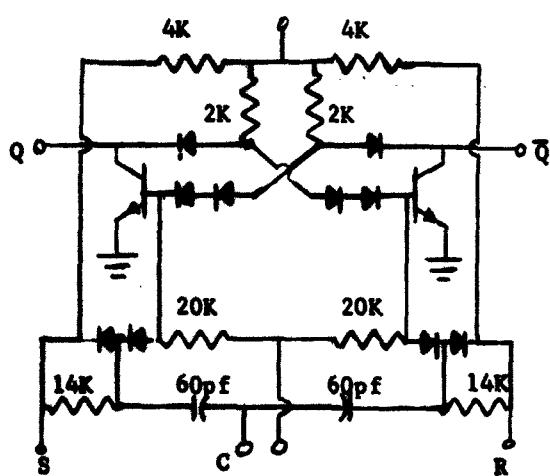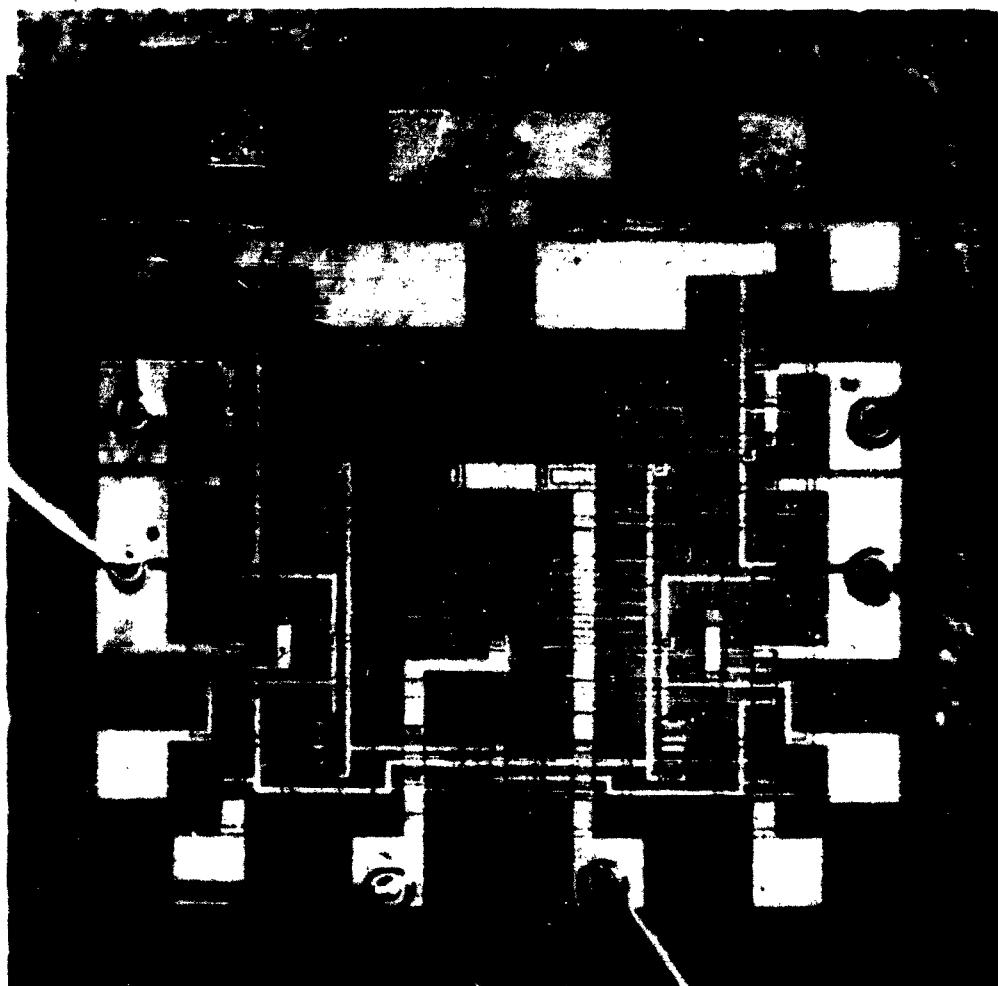
Fig. 2-57. Binary Element
(Courtesy of J. E. Fulton,
Signetics Corporation,
Sunnyvale, California

(K = kilohm)
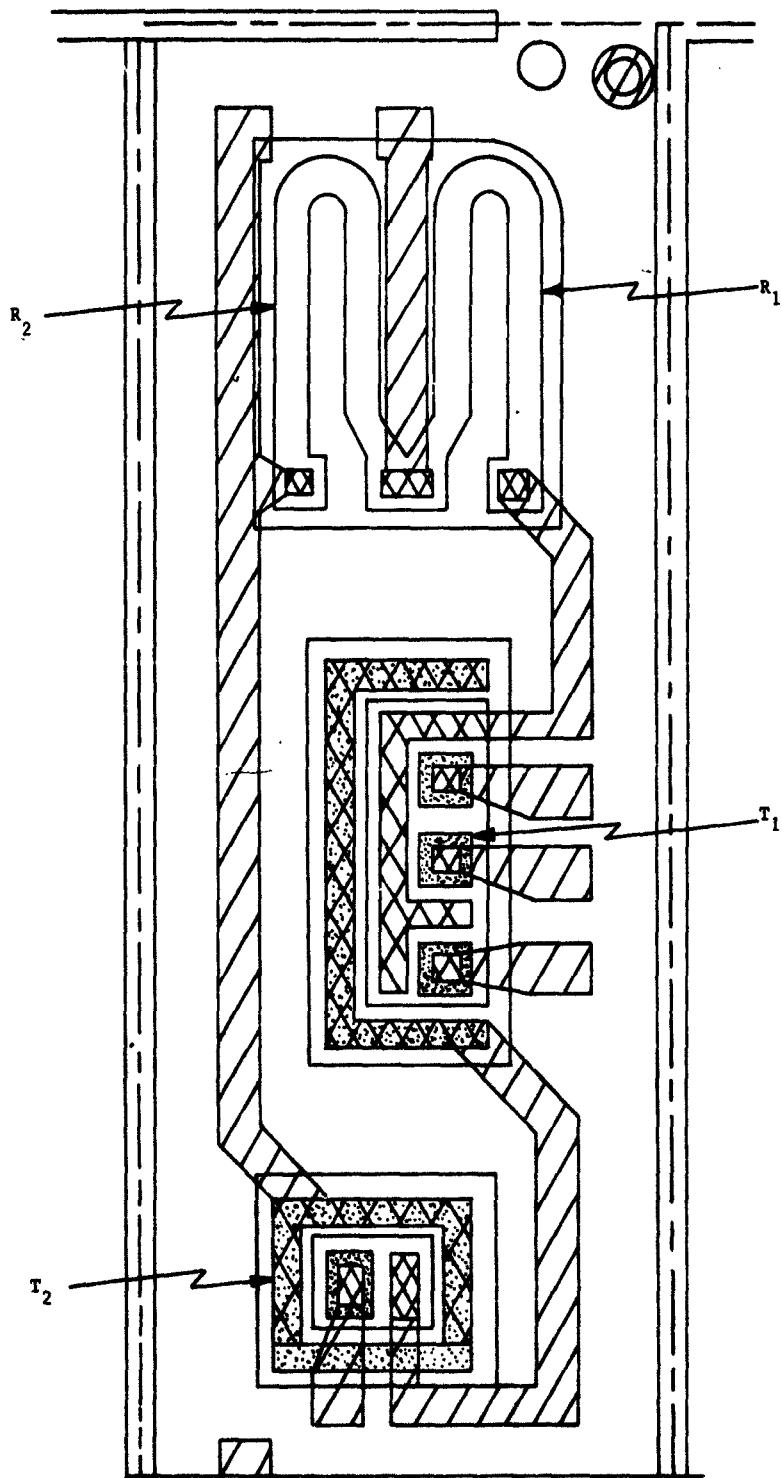
Fig. 2-58. TTL NOR Gate Block. (Courtesy of E. G. Shower, Sperry Semicon-
ductor Division of Sperry Rand Corp., Norwalk, Conn.)

required for the six resistors and 2 capacitors is clearly much greater
than that needed for the 10 diodes and 2 transistors.

2.3.4.2 Building Block Concept

The building block concept (Texas Instruments' "Master Slice,"
General Electric's "Matrix") represents a different design approach
from that presented here. The philosophy of this approach is that if
certain specific circuits can be built from standard storeroom components
and these same standard components can be fabricated on a single wafer of
silicon, then these circuits can also be built on that wafer. The first
design problem is to select the best range of typical components to
build on a wafer. The choice does not depend on a specific circuit
application but probably on a general type of application. The building
block wafer contains a large number of compatible transistors, diodes, and
assorted resistors which are well isolated from each other. These compo-
nents can then be custom "wired" to form a specific circuit much the same
as conventional components are. Usually the wiring on the silicon block
is some form of deposited conductor, as shown in Figure 2-59. This
photomicrograph shows a portion of GE's M1 matrix wafer which has been
scribed and wired for a specific application. From among the repetitive
pattern of elements a number have been selected to perform the circuit
function. The other elements are not used and may even have leads or
contact areas deposited on top of them (they are electrically insulated
from such areas by an intervening oxide). Each full M1 wafer contains
about 1100 transistors and 4200 resistors so that there is usually some
selectivity possible from among the available elements.

The primary advantage of this approach is that the wafers can be
mass produced independent of a specific application - quite unlike the
design approach discussed previously. Only the interconnection mask
is changed from one circuit to another. In many applications the loss
of design freedom is small and production gains large so that the
approach is economically attractive.

The restrictions and considerations discussed previously still
apply and the designer is now building a circuit not just from

transistors, diodes, resistors, and capacitors but from specific transistors, diodes, resistors, and capacitors the value of which are pre-determined.

2.4 Conclusions

Silicon is not a very good material for making conventional resistors and not until the advent of integrated circuits did anyone attempt to do so. The physical properties of silicon are much better adapted for use as a thermistor than as a low TCR resistor. Nevertheless, the designs of integrated circuits have created structures in which silicon resistors operate adequately. Often these designs are awkward and compromise the circuit performance, but in other applications they are completely satisfactory.

As attempts are made to extend the functional block technology over a wider range of circuits, the limitations of the silicon resistor will become more objectionable. Already the passive resistive regions cause as many rejects in block production as do the active regions. The high proportion of block area devoted to resistors seems way out of balance as the examples illustrate. What can be done?

2.4.1 Molecular Electronics

A possible solution is to eliminate all conventional circuitry from the designs of integrated circuits and build up a theory of distributed parameters based on the observed properties of semiconductors. Functions similar to those required in conventional electronic systems can then be performed by functional blocks designed, not to exhibit the properties required of the components of conventional circuitry, but to utilize efficiently the properties of semiconductors. The problem of adapting a silicon resistor to a circuit is changed to that of adapting an electronic function to the properties of silicon. This new structure will probably bear little resemblance to conventional lumped parameter circuits.

This general approach is called molecular electronics but because of the enormous difficulties associated with such a basic reform, widespread practical application is uncertain and unpredictable.
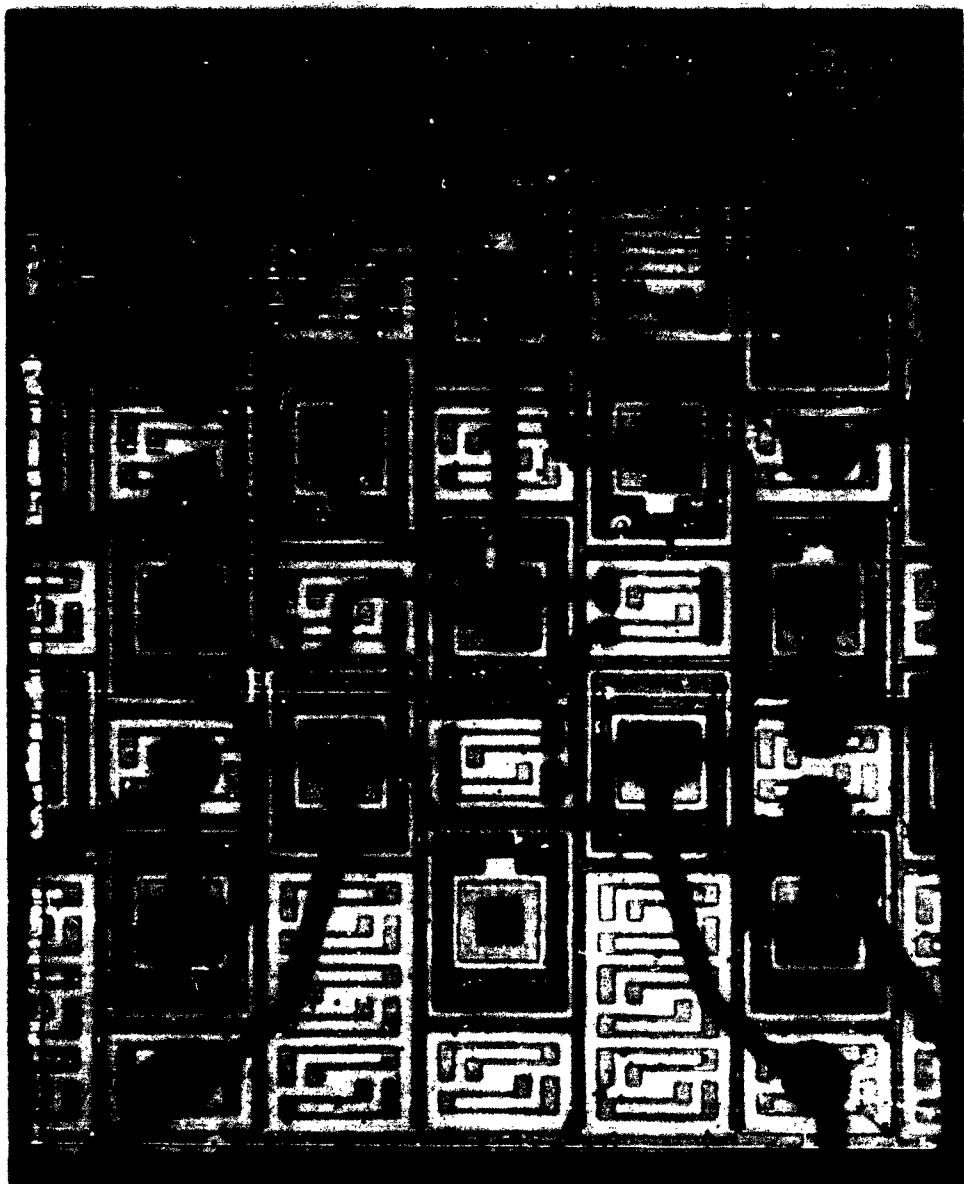
Fig. 2-59.   Circuit Fabricated on a Building Block Wafer.   (Courtesy of
R. W. Sollinger, Jr., General Electric Co., Syracuse, New York)

2.4.2 Conventional Circuit Redesign

A more practical approach is to retain the conventional circuitry but to redesign and eliminate components that are difficult to build. Inductances have been "designed out" by this technique and are never found in the schematics of functional blocks. Large values of resistance which are difficult to build also can be replaced by redesign of the circuit. Figure 2-60 illustrates an example of this technique in which large values of resistance are replaced by smaller values [48].

(a) Conventional Darlington   (b) Functional Block Darlington
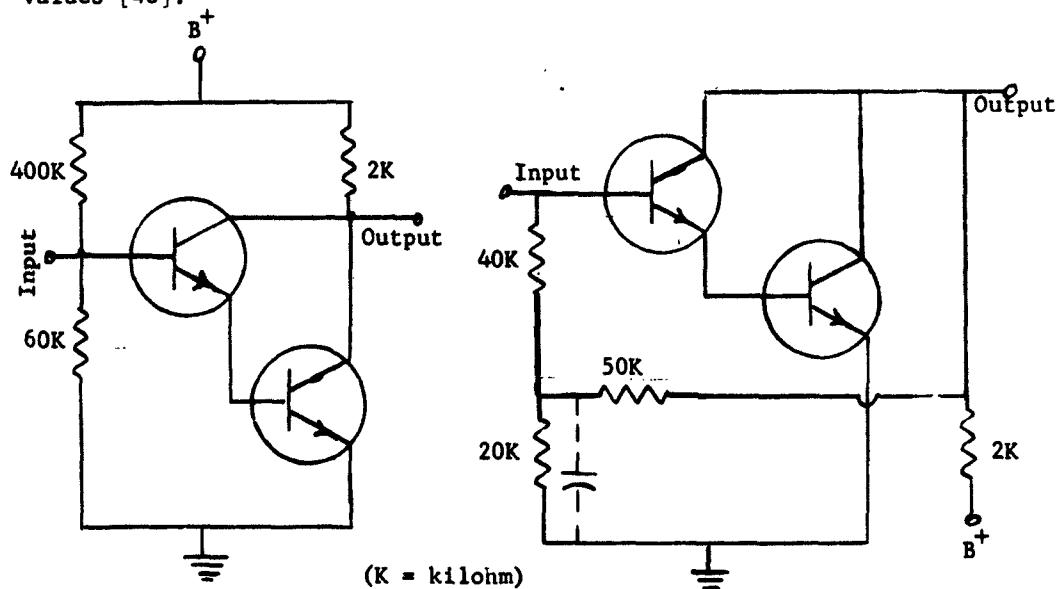
Fig. 2-60.   Redesign of Darlington Circuit to Eliminate Large Values of Resistance [48]

An even more attractive redesign is one in which resistors are
replaced by diodes or transistors. Logic functions in particular can
often be performed by transistors and diodes alone, eliminating the need
for resistors altogether. The resistor in integrated circuits is not the
cheap reliable component that most electrical engineers visualized when
they were designing the circuits which have now become standards. A
redesign of the accepted circuits in light of this change of technology
seems quite worthwhile.

2.4.3 Resistor Redesign

The ways of achieving "resistance" are not limited to the types
of resistors listed so far, particularly if non-linear V-I curves are
desired. In many circuit designs a resistor is used because the optimum
V-I curve does not exist in a feasible device. For example, the device
in Figure 2-61a has the V-I curve shown in Figure 2-61b.
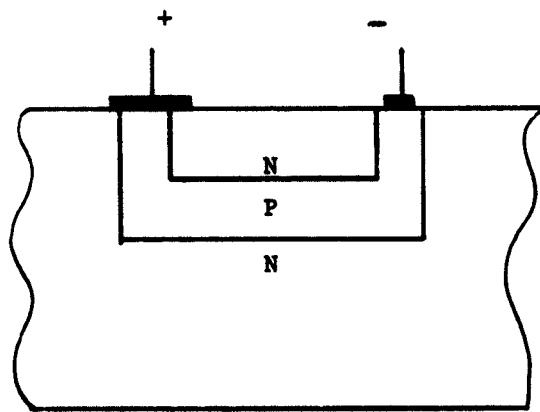
(a) Cross-section
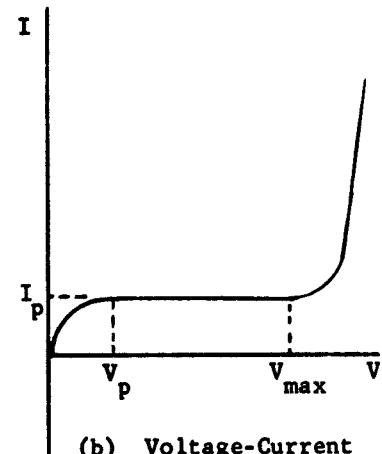
(b) Voltage-Current
     Characteristics

Fig. 2-61. Current Limiter Device

It is "pentode-like" in that it has a low dc resistance and a high ac
resistance. In a microelectronic structure it is more desirable than
the usual resistor. Some examples of its use are:

1. As a current limiter. If the effective supply voltage is less
   than V_{max} and the normal current is well below I_p, the device
   can be put in series with the item to be protected from excess
   current. During normal operation the voltage drop will be
   quite small ($<V_p$) but the current can never exceed I_p, even
   if portions of the circuit are shorted.

2. As a low voltage drop, high resistance. The device can be used
   as the emitter coupling resistor in an emitter coupled flip-flop.
   The voltage drop, normally, will be between V_p and V_{max}. During
   switching the emitter resistance appears to be very high. It
   can be used as an emitter resistor in almost any circumstance.

3. As part of a logic element. If the maximum voltage is below
   the rating of the device it can be used as a collector load
   resistor (either bipolar or field effect transistors). It
   can, perhaps, also be used as a coupling resistor in fan-in/out
   logic.

4. . As a current divider. Where very low impedance devices are
   put in parallel, such as base emitter junctions, resistors are
   often used to force proper sharing of the current. These
   devices will perform the function better.

There are capacitive effects associated with the device which must
be taken into account in high speed circuits. Also, in some circuits,
a substitute resistor such as this device may be acceptable even when it
is not superior to an ordinary resistor.

3. THIN FILM RESISTORS
(DEPOSITED ON A SUBSTRATE OF OXIDIZED SILICON)

This section considers the application of thin film resistors which are deposited on the surface of the oxidized silicon.

The properties of thin films of various materials have been studied intensively in the last decade with the hope of incorporating them into microcircuitry. Notable success has been achieved in fabricating resistors and capacitors but the absence of a satisfactory active element has restricted the widespread use of such thin film circuits.

That the strength of this approach is the weakness of the all semiconductor approach and vice versa suggests that a combination of the two might yield a technology more powerful than either one alone. Consequently, many groups are currently investigating the possibilities of using the planar silicon technology to fabricate the active regions of a circuit and the thin film technology to deposit all or a portion of the passive components on the silicon dioxide layer that is normally found on planar silicon devices [50] [51]. Presumably the established thin film technology can be transferred in toto to this type of structure since the silicon dioxide layer seems well suited to serve as a substrate (see Table 3.1). The use of thin films should be approached with some caution since the additional process steps required and the additional device complexity may add to the cost and detract from the reliability. Careful consideration should be given to trade-offs involved and possible alternative designs. This section describes the properties and performance to be expected based on observations in which other substrates were employed.

3.1 Properties of Thin Film Resistors
The important variables affecting the resistivity of a thin film are discussed in this section.

The electrical properties of thin films differ from those of bulk materials of the same composition. The resistivity is usually higher and depends upon the film preparation and substrate properties. The effects of impurities upon resistivity are much less pronounced than for silicon resistors.

Table 3.1

Properties of Substrate Materials*

	Si	SiO_2	TiO_2	Al_2O_3	BeO
Density (gm/cm^3)	2.33	2.32	4.24	3.96	3.03
Melting Point (°C)	1420	1728	1920	2.040	2550
Boiling Point (°C)	2600	dec.	dec.	dec.	4120
Thermal Coef. (10^{-6}/°C) of expansion	4.2	0.5	9.1	8.0	7.5
Thermal Conductivity (cal/sec cm°C)	0.20	0.003	0.01	0.01	0.20
Resistivity (ohm-cm)	10^{-3}-10^5	10^{14}	$10^{14\text{-}25}$	10^{11}	10^{18}
Dielectric Constant (relative)	12	4.5	100	10	11.8

* These are crystalline properties and may not be accurate for amorphous materials.

dec. decomposes first

3.1.1 Composition

The resistivity of a thin film is a function of the chemical composition and the physical properties of the film. In general, it is a very difficult task to determine the composition and an even more difficult task to control the composition of a thin film. It is for this reason that little quantitative data can be given without reference to a specific film. The chemical and physical reactions caused by heat and oxygen are usually the most important manifestations of composition.

3.1.2 Film Thickness

Three distinct regions of resistivity dependence upon film thickness have been observed [52]. The first region is that in which the resistivity is that of the bulk material. The film thickness of this region must be greater than 1000 Å. For films in the second region, with thickness in the hundreds of angstroms range, the resistivity increases over the bulk resistivity and the TCR approaches zero. The third region, corresponding to the thinnest films (less than several tens of angstroms), is characterized by a very high resistivity and a negative TCR. Equation (3.1) is generally used to describe the resistivity of a thin film as a function of the bulk resistivity [53]:

$$\rho_f = \rho \ (1 + A/t), \tag{3.1}$$

where ρ and ρ_f are the resistivities of the bulk and thin film material, respectively; t is the film thickness; and A is a constant which is a function of the mean free path of the electrons. The value of A is usually determined experimentally for a particular film.

3.1.3 Thermal History

The effect of heating upon the resistivity of a thin film is often quite pronounced and somewhat unpredictable. Mechanisms responsible for these changes are thought to be annealing, agglomeration and corrosion [54]. The annealing action removes vacancies, dislocations, and occluded gas pockets from the film, reducing the resistivity.

Agglomeration which describes the gathering into small islands that certain films have been observed to undergo with heating greatly increases the film resistance. This redistribution of material occurs for films only several hundred angstroms thick at temperatures slightly above the recrystallization temperature of the metal of the film. Most metals oxidize before agglomeration occurs. Three notable exceptions are gold which agglomerates at about 450°C, platinum which agglomerates at about 600°C and silver which agglomerates at about 300°C.

The effect of corrosion is also to increase the film resistance since the chemical reaction usually replaces a metallic atom by a non-conductive oxide of salt molecule. At 600°C corrosion deteriorates all films except platinum and gold. A layer of silicon monoxide or other overcoating can afford some protection against corrosion.

Table 3.2 lists the resistivity and TCR of various metal films.

3.2 Types of Thin Film Resistors

Six different types of thin film resistors are described in this section.

Film resistors have been made of many types of materials - semiconductors, metals, and cermets (a mixture of a metal and nonmetal) and deposited by various techniques - silk screening, electroless plating, vacuum evaporation or sputtering. The success of a particular process is related to the application and also to the experimental technique employed. The types examined in this section have been selected because of their apparent compatibility with an active substrate of silicon and because of their advanced technology as evidenced by the quantity of published work on them.

3.2.1 Thin Film Carbon Resistors

Thin film carbon resistors have been fabricated by decomposition of various organic materials, painting with colloidal carbon, bombardment of carbon by high energy electrons, and by rapid evaporation of bulk carbon. The last technique, while difficult (the sublimation temperature of carbon is above 3900°C), has been used to form the thin films whose properties are listed in Table 3.3 [55].

Table 3.2

Resistivity and TCR of Various Metal Films[*] [54]

Metal	ρ_f(before annealing)	ρ_f(after annealing at 600°C)	TCR	Bulk TCR (0-100°C)	Ratio of film TCR to bulk TCR
Au	22.2	4.95	2800	3400	.82
Pt	8.7	15.65	2500	3900	.64
Ir	12.8	42.5	1800	4000	.45
Rh	17.3	15.8	2000	4600	.43
Pd	20.3	20.8	2300	3700	.62
Ni	28.5	41.0	5000	6400	.78
Cr	172.5	62.0	600	-	-
Ti	67.1	59.9	700	5400	.13
Zr	134.0	-	<100	4400	.02
Mo	99.5	49.0	200	3300	.06
Ta	768.0	-	<100	3100	.03
W	4390.0	422.5	<100	4800	.02
Al	.41	.36	2800	4300	.65

* Units are: ρ_f ohm-cm

TCR ppm/°C

Table 3.3

Resistivity of arc-evaporated carbon films at 23°C as a
function of film thickness [55]

Thickness (Å)	Resistance (megohms)	Resistivity (ohm-cm)
106	10^8	5×10^7
128	3380	1440
276	5.44	5.00
284	23.3	2.21
309	3.94	4.06
405	2.38	3.22
405	4.89	6.60
992	10.8	1.77
553	0.141	2.61
920	0.737	2.26
1290	0.299	1.28
2362	0.165	1.30

The thinnest films (less than 200 Å) clearly show the effects of agglomera-
tion and the resulting high resistivity, and the thicker films (200-2000 Å)
show typical intermediate region electrical behavior, having resistivities
three orders of magnitude higher than ordinary fine particle carbon blocks.
With subsequent annealing cycles the resistivity decreases as shown in
Figure 3-1. Reproducibility is poor from film to film and the TCR is
large and unstable. These thin carbon films seem to have limited
integrated circuit applications.

3.2.2 Evaporated Nichrome Resistors

The use of thin films of nichrome to form microcircuit resis-
tors has been reported by various groups [51, 56-60]. The deposition
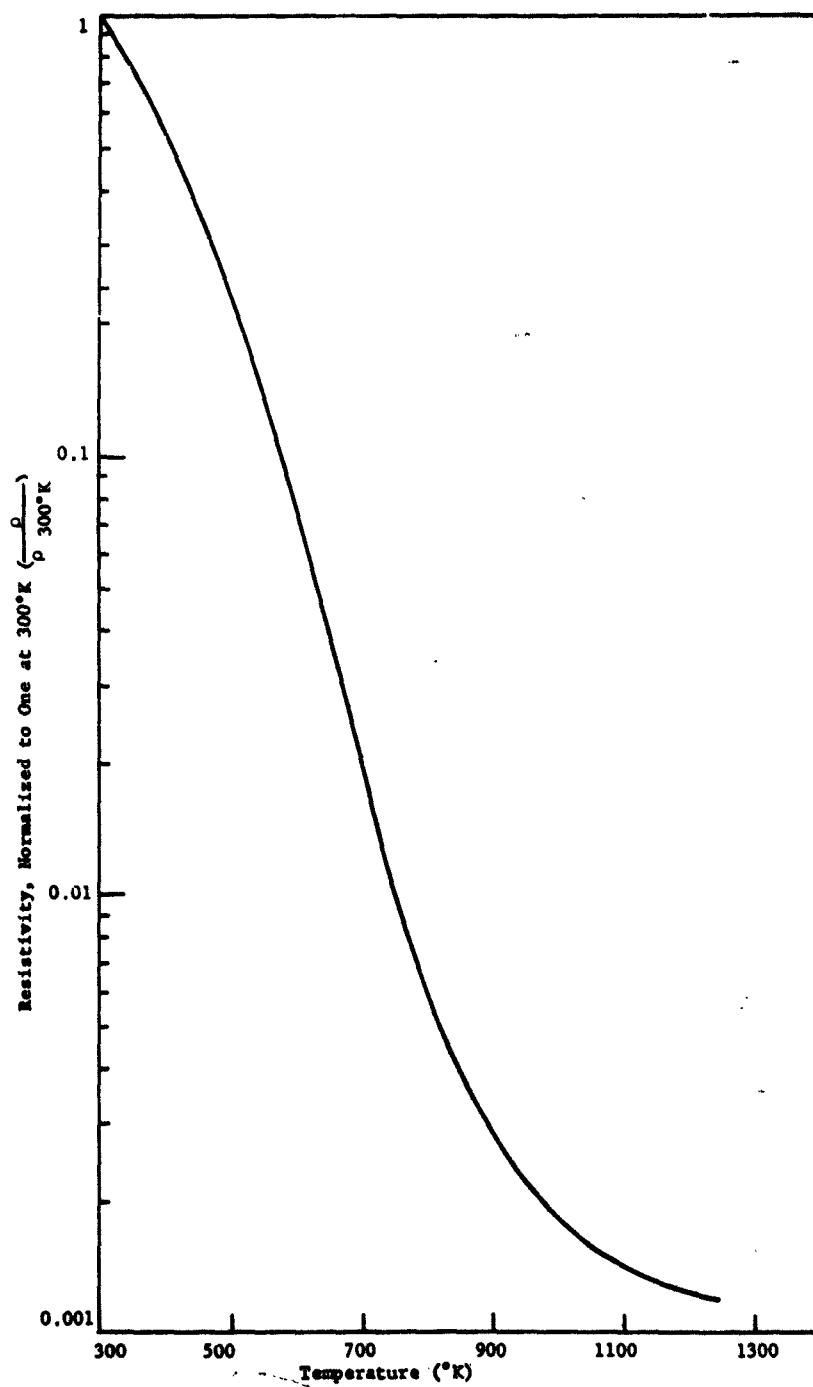
Fig. 3-1. Room Temperature Resistivity of Evaporated Carbon Film as a
Function of Highest Temperature Reached During Annealing [59]

technique is vacuum evaporation using either a tungsten heating coil or an electron bombardment method. The latter method usually yields superior homogenity and purity in the films [59].

The films are defined by masking during the deposition or afterwards by etching away the unwanted nichrome. Film thickness, substrate temperature, and aging are important parameters as shown in Figure 3-2 and 3-3.
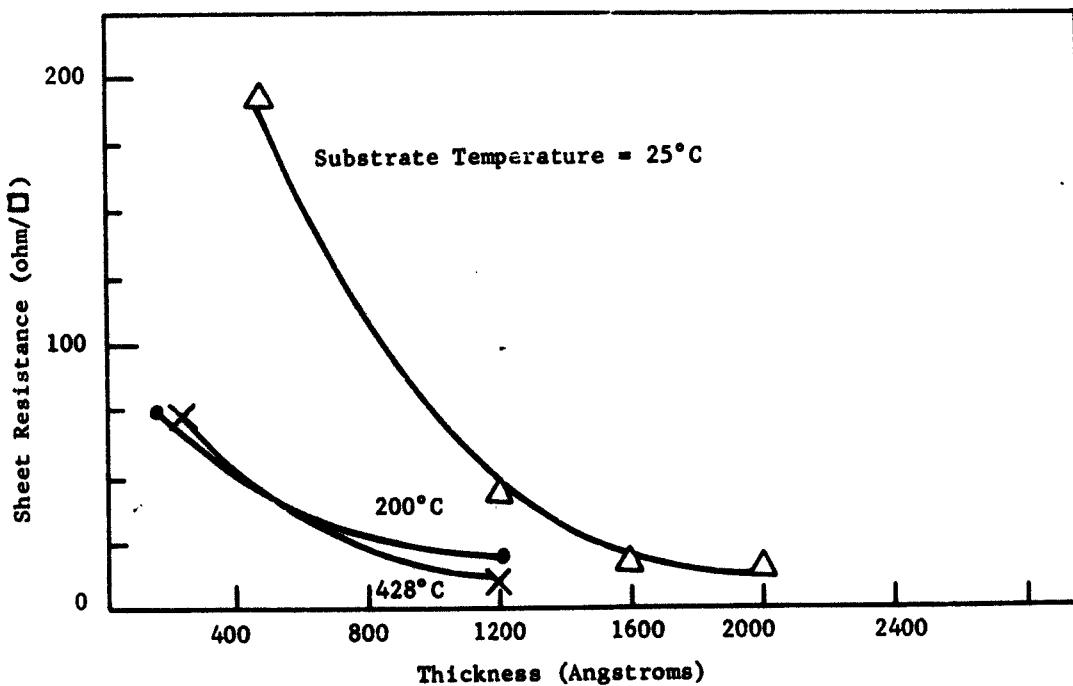
Fig. 3-2. The Dependence of the Sheet Resistance of Nichrome Resistors
           Upon Thickness and Substrate Temperature [56]

The relatively advanced state-of-the-art for building resistors from nichrome films makes this technique attractive.

3.2.3 Sputtered Tantalum Resistors

As shown in Table 3.2, tantalum has a reasonably high sheet resistivity and a low TCR. In addition, its oxide can be used as the dielectric in a capacitor. These properties make it attractive for integrated circuitry.
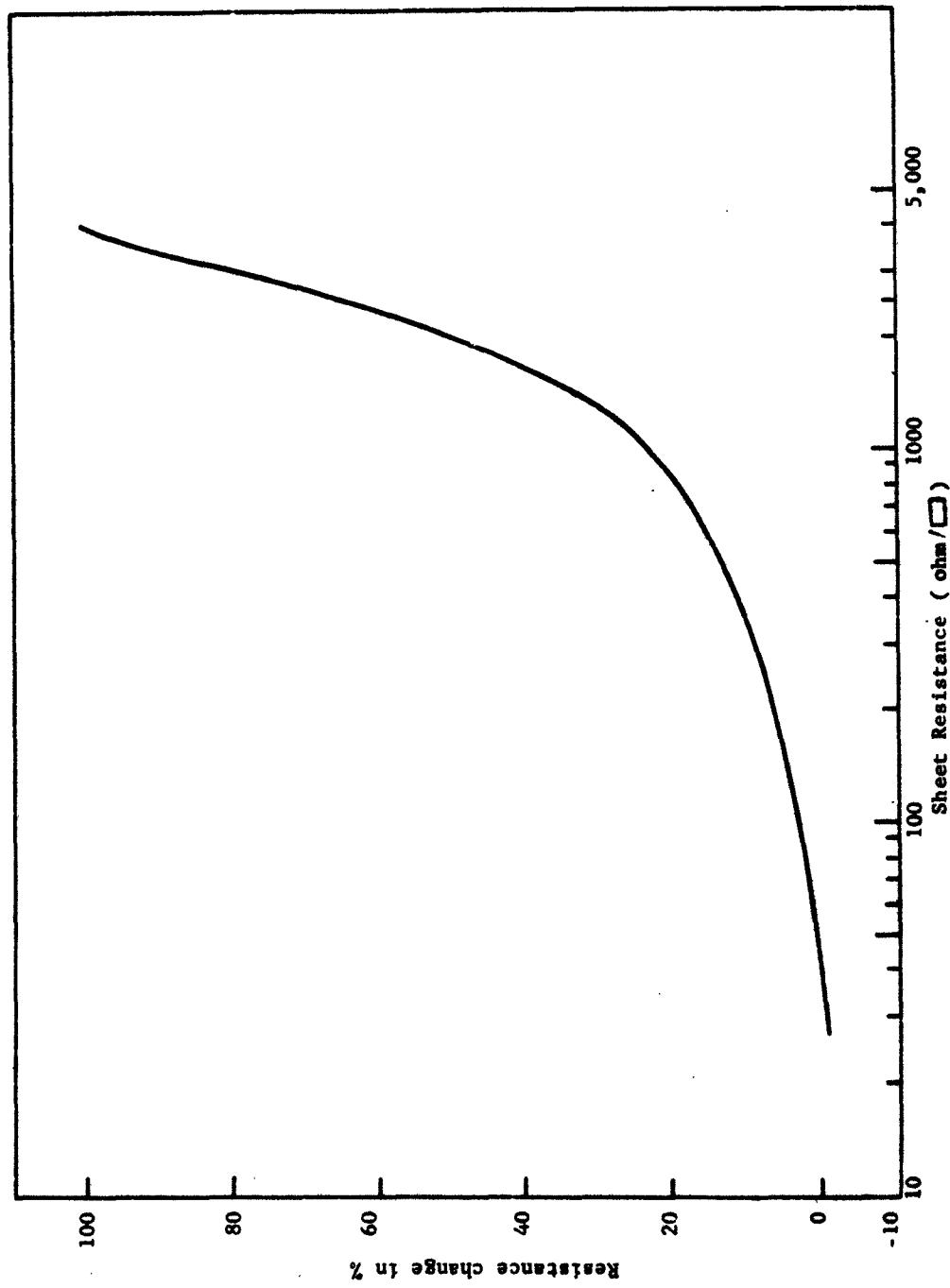
Fig. 3-3. The Resistance Change of Nichrome Resistors Due to Heating in Air at 250°C for 10 min vs Sheet Resistance [52]

Cathodic sputtering in which high electric fields are used to
remove positive metallic ions from the cathode is the preferred method
of depositing tantalum films - primarily because of the difficulties of
evaporating a refractory metal. The apparatus is arranged so that a
conductive contact can be made to the tantalum deposits without breaking
the vacuum and before any oxidation occurs. Gold is a suitable material
for contacts.

The oxidation of tantalum produces a protective oxide whose forma-
tion also influences the resistivity of the film as mentioned in 3.1.3.
A heat cycle in air to a temperature in excess of its anticipated
operating temperatures in any circuit is an adequate stabilization cycle.
The sheet resistivity must be designed to its value after aging to allow
for the change caused by oxidation. The change of sheet resistivity
with time at 250°C is shown [61] in Figure 3-4. Resistors aged by
this cycle have been shown to change their value by only 1% after
operation at 150°C for 2000 hours.

3.2.4 Electroless Deposition of Nickel

Electroless nickel plating has often been used to form ohmic
contacts to both p- and n-type silicon surfaces [62]. Recently techniques
for   electroless deposition of nickel on smooth glass microscope
slides have been perfected [63] and the extension to deposition on SiO_2
covered silicon substrates appears direct. This technique could be used
to form resistors, contacts and interconnections simply by varying the
thickness of the layers.

The process avoids the vacuum requirement which is expensive,
difficult to control and probably a partial cause of the non-reproduci-
bility sometimes encountered with the previously discussed thin film
resistors. Plots of temperature vs resistance are shown in Figure 3-5,
for non heat treated electroless nickel resistors and in Figure 3-6 for
two thicknesses of aged resistors.

3.2.5 Cermets

One of the disadvantages of a metal film is the relatively
low value of sheet resistivity attainable. Only by making the films
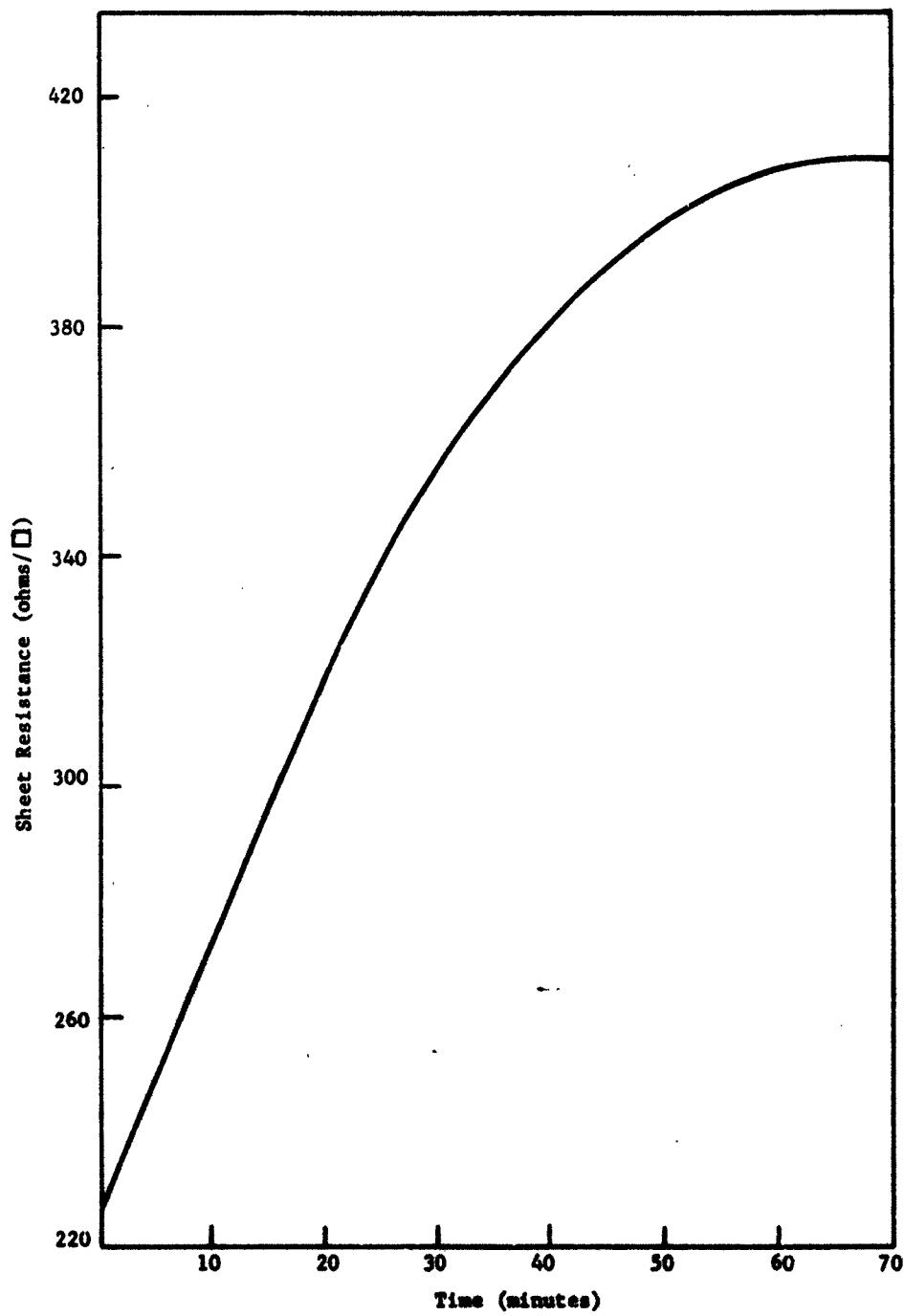
Fig. 3-4. Stabilization of Tantalum Resistors, Held at 250°C in Air
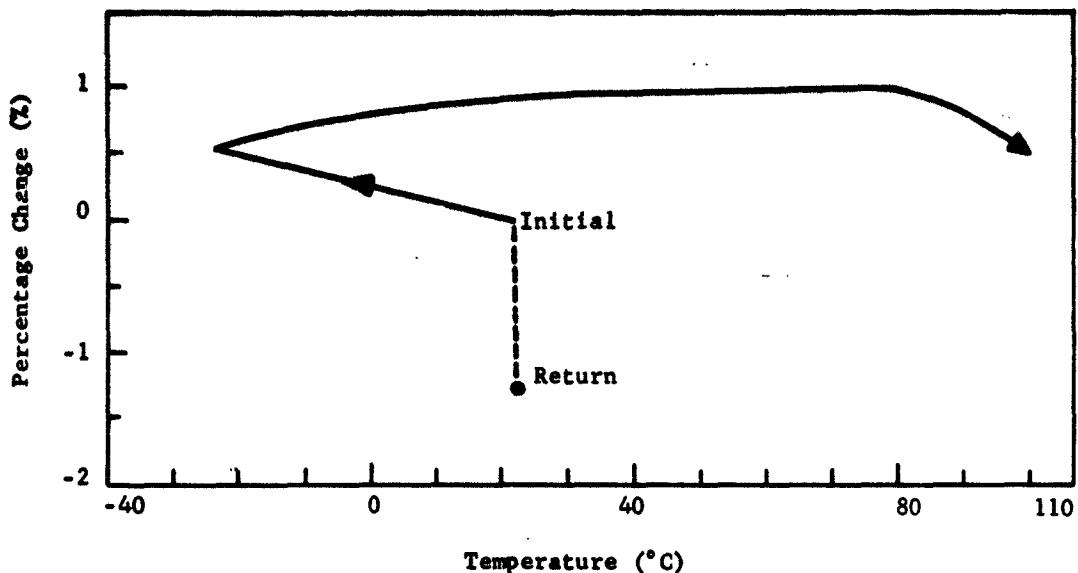
Fig. 3-5. Resistance-Temperature Characteristics for Six 800 ohm/square
Electroless Nickel Resistors Prior to Any Heat Treatment
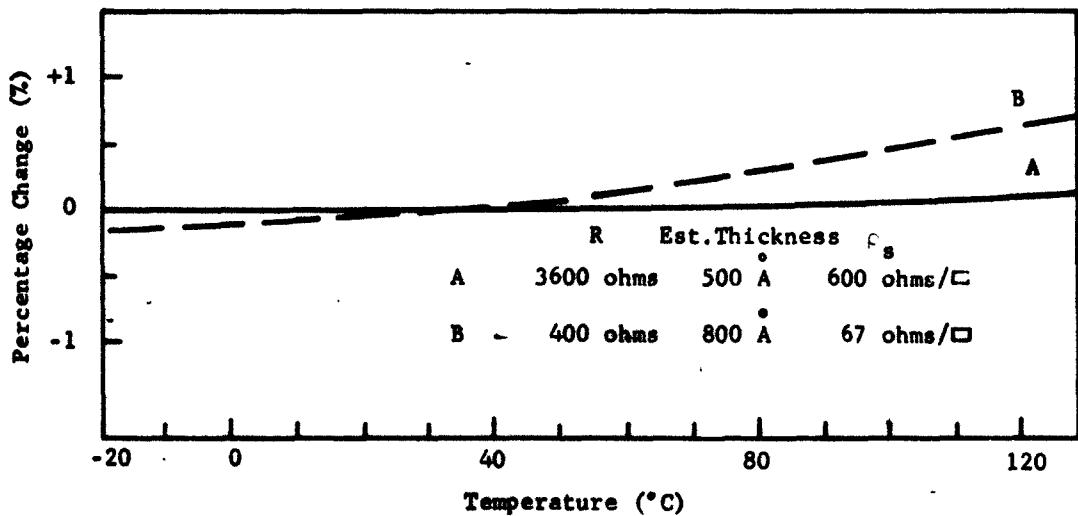
Fig. 3-6. Resistance-Temperature Characteristics of Electroless Nickel
Resistors, Heat Treated Overnight at 200°C

extremely thin (less than 100 Å) does the sheet resistivity rise to high
values (greater than 1000 ohms/square). The added control problems in
doing so lead to poor reproducibility and unsatisfactory performance.
Generally the maximum practical limit of sheet resistivity is set in
the range of 200 to 600 ohms/square. An obvious technique for increasing
resistance without decreasing the film thickness is to raise the resistiv-
ity of the film by mixing metal with an insulator. This composition film
is called a cermet. A large number of combinations are possible, the
most common being either an oxidation of a metal whose oxide is a non-
conductor or the simultaneous evaporation of a metal and an insulator
such as SiO.

Early data [64] on the chromium-silicon dioxide cermet are shown in
Table 3.4. These resistors were fabricated on a glass microscope slide
by simultaneous evaporation of chromium and silicon dioxide in the
approximate proportions of 80% and 20%, respectively. The substrate
temperature was 450°C and bell jar pressure, 2×10^{-4} torr of oxygen.
Following deposition the resistors were annealed at 450°C for one hour
in an atmosphere of 2×10^{-4} torr of oxygen.

Under subsequent temperature cycling both the value of the resistor
and the magnitude of the TCR become large and somewhat unpredictable.
A critical temperature, between 150° and 200°C for these particular
resistors, marks the division between reversible and irreversible
temperature dependence of these parameters.

A later variation of the composition of this cermet has been found
to remove the instability [65]. The source of evaporation consists of:

> 70 at. % Cr
> 30 at. % SiO
> 0.5% by weit   ···'dal SiO_2 (Cab-o-sil)*

During the evaporation the substrate is at 220°C, 18.5 inches from the
source. The heating filament is 5 mil tantalum ribbon, 1.5" long and
1" wide which is operated at a power input of 1200 watts. The source
constituents are thoroughly mixed and fed toward the hot filament down
a tantalum chute whose exit is 2" above and 1/4" away from the side edge

---

*   Cabot Chemical Company.

Table 3.4

Resistance Change of Chromium-Silicon Dioxide Cermet Materials While Aging at 25°C [64]

Resistor No.	Initial Sheet Resistance (ohms/□)	Total Increase After 8 days (%)	Total Increase After 28 days (%)	Approx. Film Thickness (Å)	Ave. Temp. Coef. of Resistivity (ppm/°C)	Approx. Stability of Nichrome Resistors of about the same sheet resistivity
R_2	230	-2	+5	1625	-320	
R_3	200	-2.5	±0	1520	0	+10% after 7 days
R_4	540	+2.0	+2.0	168	-280	
R_5	1,760	+4.0	+5.2	113	-250	+25% after 2 days
R_6	2,950	+10.0	+11.5	100	0	+50% after 7 days

of the filament. The source material is flash evaporated by the hot filament and deposits on the substrate. The bell jar pressure is 5×10^{-5} to 10^{-4} torr. Figure 3-7 shows that the resulting resistors are quite stable--unlike the earlier resistors. The sheet resistivity of these particular resistors is 250 ohms/square. Much higher values of sheet resistivity are possible with cermets but the control problems are difficult and the reproducibility poor. Consequently the anticipated high value of sheet resistivity of cermets is still not a practical reality.

3.2.6 Tin Oxide Film Resistors

Another material investigated for its high sheet resistivity is tin oxide. Sheet resistivity values as high at 5000 ohms/square have been reported. Experimentally, tin-oxide antimony-oxide films have been produced which are stable up to 500°C in a nuclear environment [66].

The fabrication technique is to spray a solution containing tin and antimony salts onto a hot substrate, leaving a thin film deposit. A solution consisting of 86 gm $SnCl_4 \cdot 5H_2O$, 4.7 gm $SbCl_3$, 100 cc conc. HCl, 50 cc of water and 2.0 cc of formaldehyde produces the most stable films. The substrate temperature is quite high, 1000°C - 1200°C which may or may not be objectionable for integrated circuit application.

Figure 3-8 shows the temperature behavior and stability at elevated temperatures of resistors prepared by the spray technique.

3.2.7 Summary

The properties of the resistors discussed in this section are summarized in Table 3.5.

3.3 Design Techniques

The design and procedures for obtaining thin film resistors on a silicon substrate are described here.

Once the decision is made to use a deposited film resistor, the choice of a particular type of film is not so closely related to the block fabrication and operation as it is to the techniques available. Typically
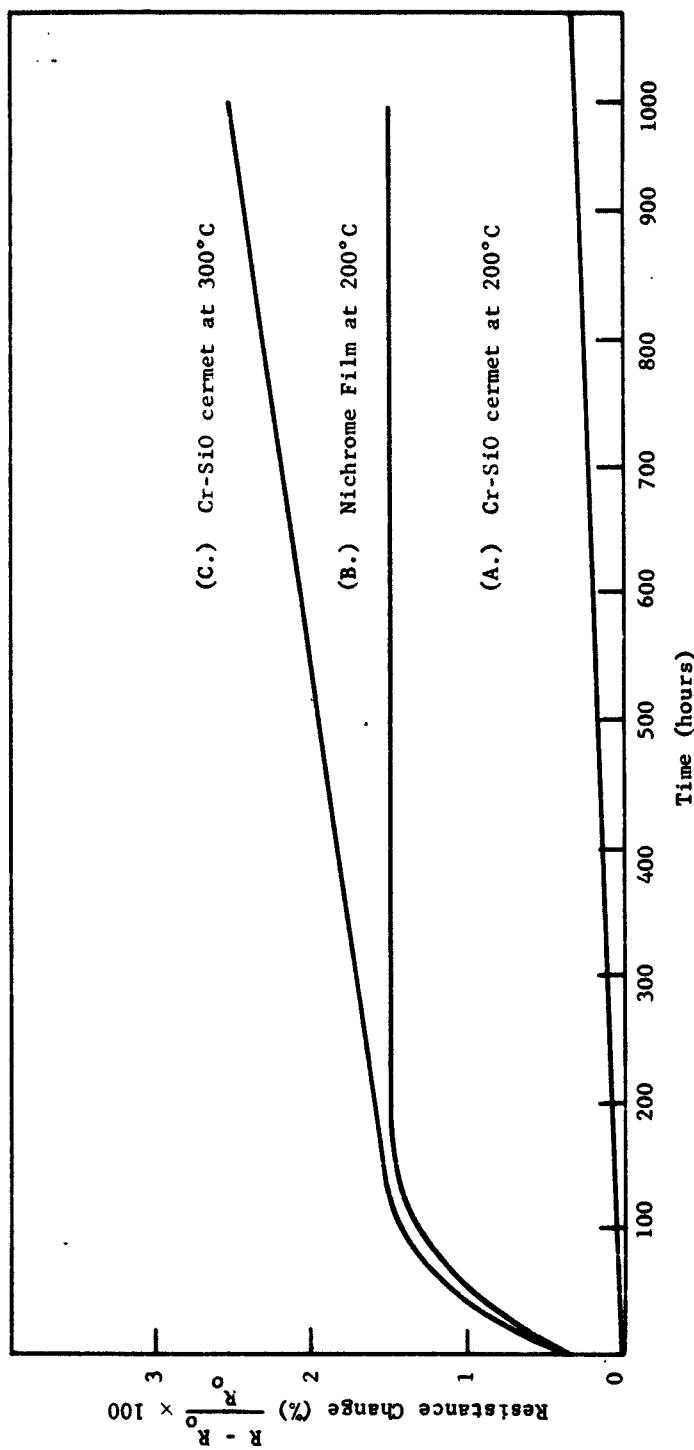
Fig. 3-7. Comparative Stability of Cermet and Nichrome Films [60]
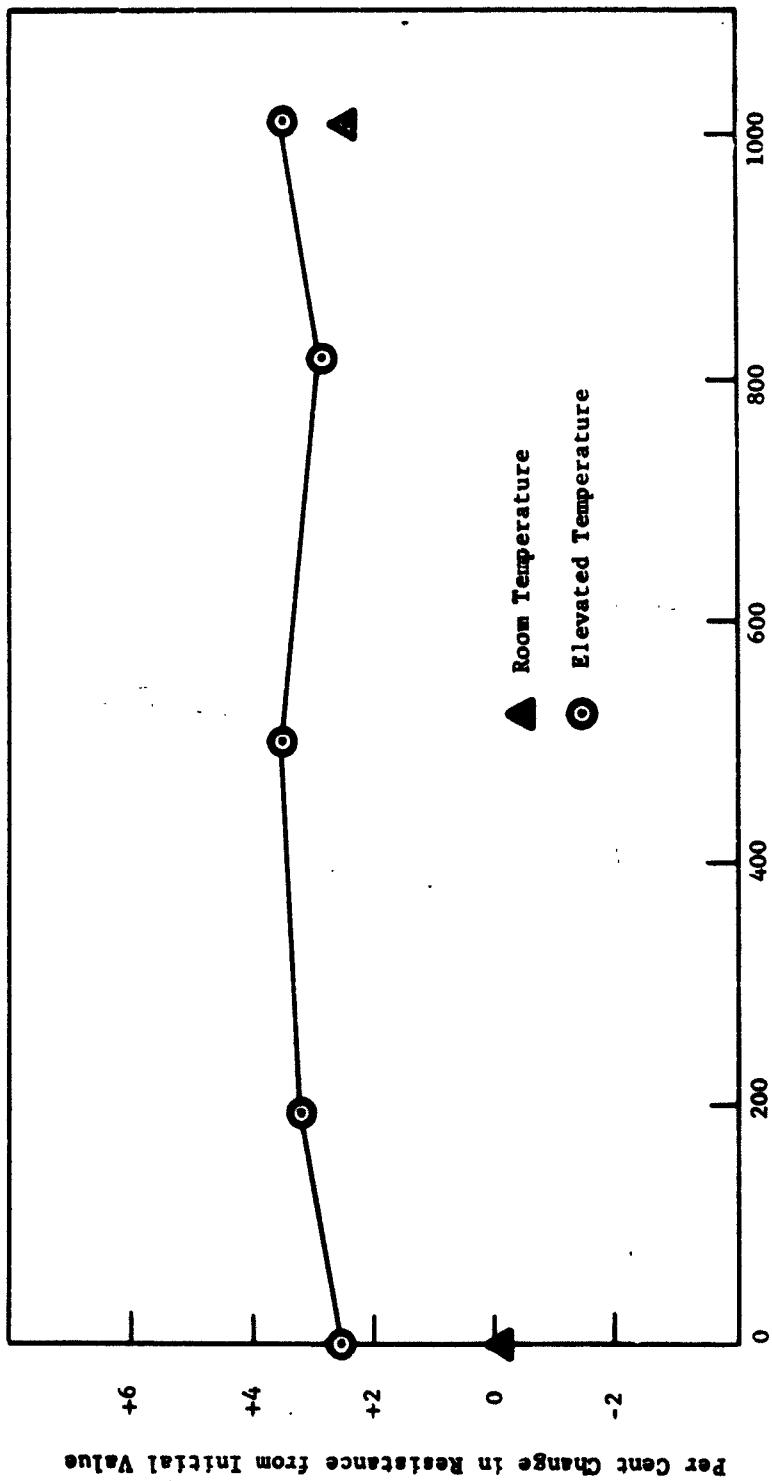
Fig. 3-8. Resistance Stability of 7.5% Sb_2O_3 - 92.5% SnO_2 Film Deposited at 1000°C

Table 3.5

Electrical and Physical Properties of Thin Film Resistors

	Fabrication Techniques	Sheet Resistance (ohms/□)	TCR (ppm/°C)	Linear Coef. of Expansion (°C)$^{-1}$	Stability (% drift in 1000 hrs. at a given temperature)
Carbon	vacuum or vapor dep.	$10\text{-}10^7$	-500	2.9×10^{-6}	-
Nichrome	vacuum dep.	$10\text{-}10^4$	+50	13×10^{-6}	2% at 200°C
Tantalum	vacuum sputtered	$10\text{-}10^4$	±200	6.6×10^{-6}	1% at 150°C
Electroless Nickel	chemical dep.	$20\text{-}10^5$	±250	-	1% at 70°C
Tin Oxide	vapor decomposition	$10\text{-}5000$	±250	-	4% at 500°C
Cermet (Cr-SiO)	vacuum dep. (flash evaporation)	$200\text{-}10^5$	±250	-	3% at 300°C

organizations, needing a thin film resistor capability, survey a number
of possible techniques, choose a particular one, and proceed to develop
it to the exclusion of others. This chosen technique is obviously the
one that that particular organization should use for fabricating resistors
on the surface of planar silicon structures. The performance of the
various resistors considered seems equivalent so that no one type is
superior to another.

The relative temperatures of the processes dictate that the deposition
of the thin film resistors follow the diffusion of all active elements.
Contacts to the silicon and the thin films can be made simultaneously
in some processes. Other than that they constitute completely distinct
processing steps, requiring only that the films adhere to the silicon
dioxide and avoid contamination of the diffused regions. Of the resistive
films considered here, there is no clear preference of one over another
in either fabrication or performance.

3.3.1 General Procedure

The required starting information is the same as for the silicon
resistors and is the following:

1. Value
2. Tolerance
3. Operating Potential....
4. Power Dissipation and Ambient Temperature
5. Isolation
6. TCR
7. Power Dissipation of the Functional Block

Requirement 6 is probably the factor that dictated the use of a
film resistor in the first place. Once this design feature is
established, requirement 6 can be considered satisfied, for the TCR
of all film resistors is much smaller than that of even conventional
bulk carbon resistors.

The power dissipation of each resistor is the primary control of
resistor size.

In the absence of other information describing realistic values of
power dissipation, an arbitrary maximum such as shown in Figure 3-9,
should be assumed initially. The chart should be experimentally checked
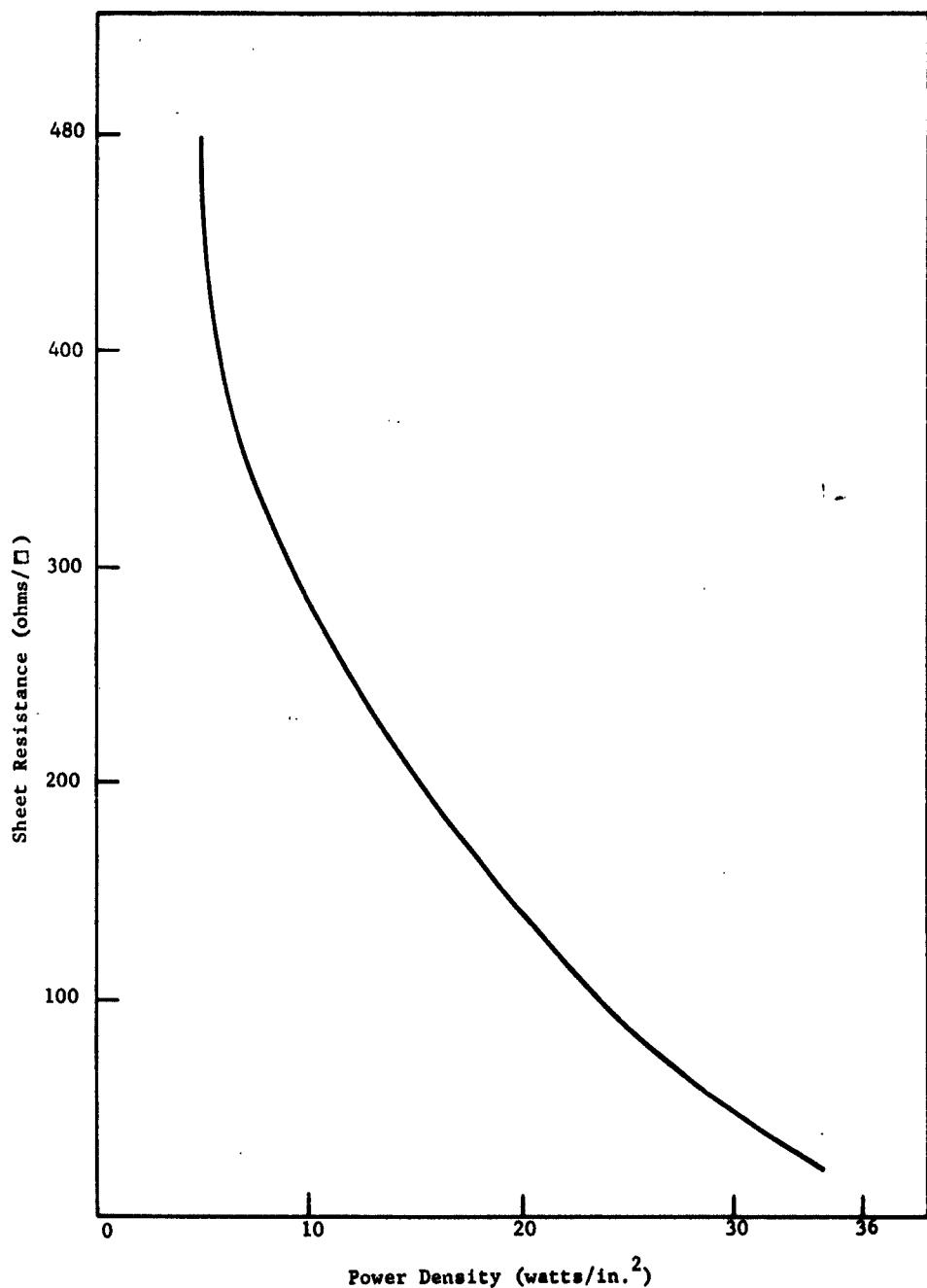
Fig. 3-9. Permissible Loading in watts/inch^2 for Reasonable Stability
of a Thin Film Resistor at Ambient Temperature of 25°C [58]

as early as possible for each different technique and substrate. The use of oxidized silicon as a substrate is an unknown and such factors as oxide layer thickness will probably influence the power handling capability.

From Figure 3-9 or a similar chart, the minimum area of each resistor can be calculated from the power dissipation required of it.

The sheet resistivity of the film should be chosen so that all needed values of resistance can be easily achieved. The number of squares should not be less than one and should not exceed a practical upper limit of about 1000. When the range of required resistances is so large that no value of sheet resistivity can cover all these values, one end of the spread must be designed as silicon resistors. Two different resistive films are quite undesirable simply because of the additional steps and inevitable reduction of yield.

Although the design is restricted to only one value of sheet resistivity (as opposed to the 3 or 4 choices of sheet resistivity available for designing similar resistors in silicon), the fact that this value can be chosen to be the optimum value for each specific circuit (unlike silicon where no choice exists) gives about the same degree of flexibility as found with silicon resistors.

Once having established the film sheet resistivity and the minimum resistor size, a package is selected. Then it is advantageous to re-design the thin film resistive regions so that the entire area available in the package is occupied. The absence of large area p-n junctions whose yield is inversely proportional to some power of the area removes one of the major objections to over-sized resistors. The MOS type of resistor envisioned here has a much smaller dependence of yield upon area. The most serious objection to using larger resistor areas than necessary arises from the larger capacitive reactances thereby introduced, the importance of which varies from circuit to circuit.

The primary advantage of large area resistors is the cooler operation as shown in Figure 3-10. Two resistors of equal total value and the same sheet resistivity but different areas, operate at different temperatures under the same load. Figure 3-10 shows a solid, one square resistor
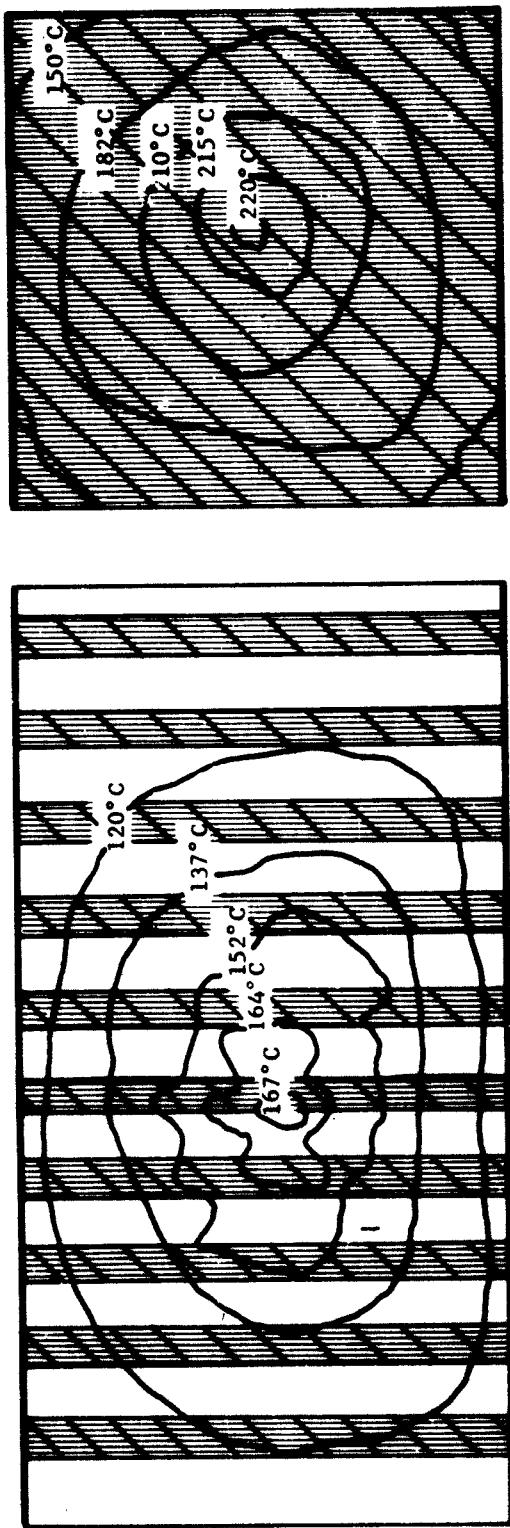
Fig. 3-10. The Effect of Area on Operating Temperature of a Thin Film Resistor. [67]

under load having a temperature of 220°C in the center. In Figure 3-10 this same square has been divided into equally spaced strips. The dimensions of the resistor are the same but the area of substrate covered is doubled. Under the same load this resistor reaches a highest temperature of 167°C.

Two factors determine the topological layout of the elements--ac isolation and operating temperature. DC isolation is primarily dependent upon the oxide quality and is not a factor. At high frequency the resistance of the substrate becomes the dominant term in the expression for reactance between elements. In such applications the arrangement of elements is based primarily on this consideration. For low frequency operations, where the substrate resistance is unimportant, the thermal dissipation is the primary factor in topological layout; the elements should be arranged so as to avoid concentrating the power dissipation in one area. The power resistors should be far removed from each other, separated by regions of small heat generation.

If necessary, thin film elements can be deposited directly on top of silicon elements with the oxide isolating them. The capacitive coupling will be complex and most easily determined experimentally.

Interconnections and contacts to the resistive regions should be put down after the resistive films rather than before. The thicker films are much less likely to develop hot spots than a thin film when crossing a ridge such as occurs on joining the resistive film with the conductive film.

3.3.2 Specific Illustration

No specific steps or design examples are included since experience with these structures is very limited. A typical fabrication cycle is outlined in Figure 3-11 [68].

3.4 Conclusion

There is no clear advantage of one film resistor over another. The choice seems to be based on an organization's capabilities and previous experience. The problems and performance of various techniques
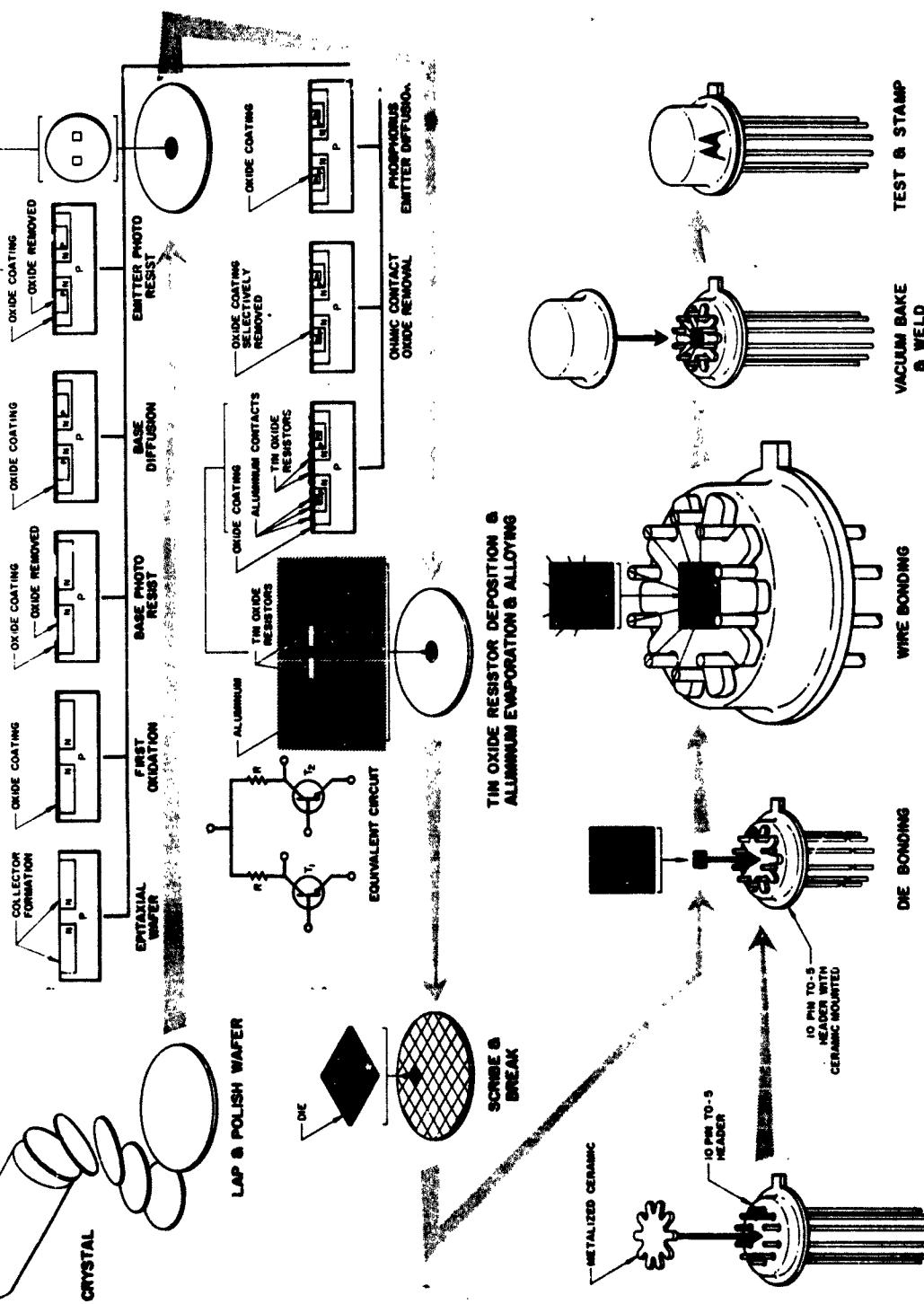
Fig. 3-11. Silicon Planar Epitaxial Integrated Circuit Fabrication (courtesy of H. K. Dicken, Motorola Inc., Phoenix, Arizona)

are similar. The compatibility with oxidized silicon as a substrate has been demonstrated for nichrome films [51], the tin oxide films [51] and the Cr-SiO cermet films [65] but all films discussed in this section should be equally compatible with the SiO_2 covered silicon substrate.

4. RESISTANCE CALCULATIONS

In this section methods are given for the calculation of resistance for irregular geometries.

A basic design consideration is the geometrical shape of the resistor structure. Odd-shaped geometries are necessarily encountered if the space available is utilized to its fullest extent. For example, it is not always possible to design a resistor such that it is a straight strip with a contact at each end. The resistor probably will consist of a strip that makes several turns between the contacts. This brings up the problem of predicting the resistance of and the current density in such a structure. A typical problem might be that of determining the contribution of a square or rounded corner to the total resistance of an element. Many of the problems that arise in resistor design are not solvable by elementary methods and one must turn to more sophisticated methods, several of which are discussed in this section.

4.1 Conjugate Functions

The conjugate function method is introduced in this section.

A mathematical tool that has proven to be very useful in the solution of many electrostatic and fluid flow problems is that of conjugate functions. This allows the transformation of odd-shaped geometrical patterns into geometrical shapes that have known solutions. Resistors with odd-shaped geometries may be solved if a method is found to transform the odd configuration into a rectangular configuration for which we know the resistance. As an example of such an operation, consider the calculation of the resistance between the two contacts (DE and AB) along the circular strip as shown in Figure 4-1. Here the resistive strip is the area enclosed by the lines ABCDEF in the complex plane $Z = X + jY = re^{j\theta}$. If $W = \ln Z$ where $W = U + jV$, then the boundary of the Z-plane describing the circular strip is transformed into the rectangle in the W-plane as shown in Figure 4-1. The line AB is transformed into the line A'B' in the W-plane. Likewise DE, DFB, and EFA are transformed into the lines D'E', D'B' and E'A', respectively. Since the lines AB and DE are equipotential lines in the Z-plane, the lines
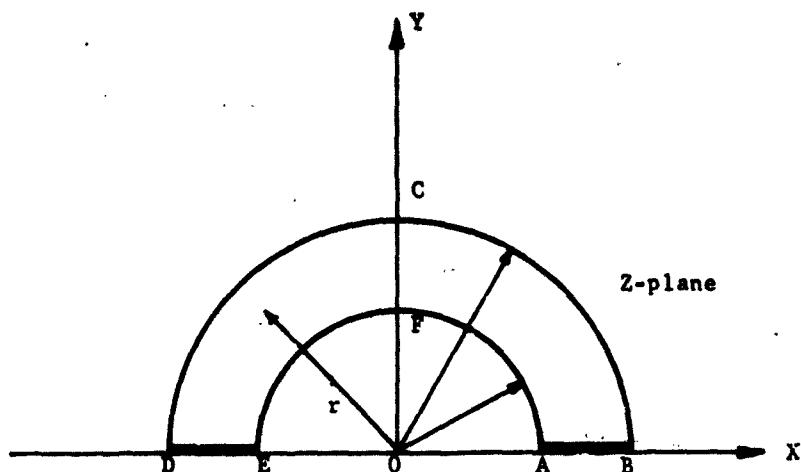
(a) A Circular Conducting Strip in The Z-plane
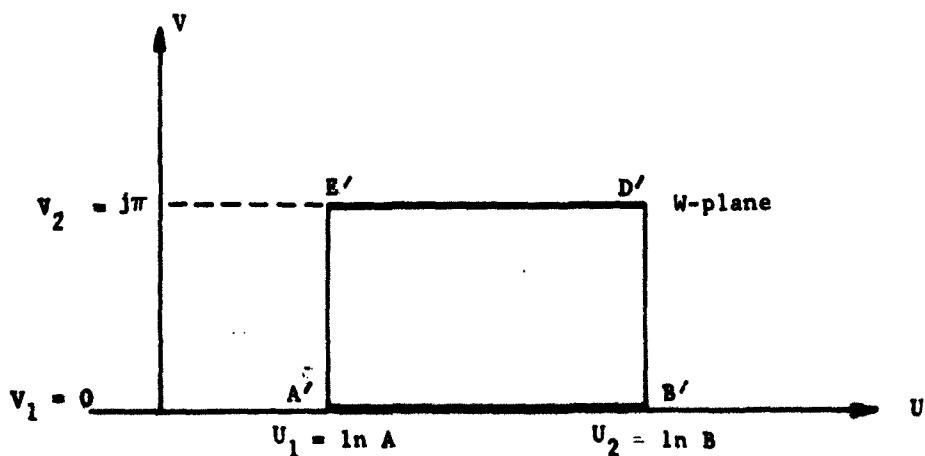
(b) The Strip in (a) Transformed to the W-plane by W = ln Z

Fig. 4-1. Logarithmic   Transformation of a Curved Resistor

A'B' and D'E' are equipotential lines in the W-plane. Note that the equipotential lines in the W-plane are represented by V = constant and likewise the flow lines are given by U = constant. The resistance in the W-plane is then:

$$R = \frac{\rho \ell}{tw} = \rho_s \frac{\ell}{w} = \rho_s \frac{V_2 - V_1}{U_2 - U_1} , \qquad (4.1)$$

where ρ_s is the sheet resistivity and V_1, V_2, U_1, and U_2 describe the geometrical boundaries. The term $V_2 - V_1/U_2 - U_1$ is the effective number of squares in Z-space. The resistance of the strip for the example is then:

$$R = \rho_s \pi / (\ln B - \ln A) . \qquad (4.2)$$

Let the current density be normalized to unity in the W-plane. The current density, at any point in the Z-plane, is [69]:

$$J = \left| \frac{dW}{dZ} \right| . \qquad (4.3)$$

Note that the total normalized current (in both W- and Z-planes) is $U_2 - U_1$. For the example the current density is:

$$J = \left| \frac{d(\ln Z)}{dZ} \right| = \left| \frac{1}{Z} \right| = \frac{1}{r} . \qquad (4.4)$$

The normalizing factor, N, which was used to make Z and W dimensionless and current density (W-plane) unity, must be reintroduced: $I = N(U_2 - U_1)$; convenient units for N are milliamperes, for example . As shown above, it is possible to calculate the effective resistance and the current density for a circular strip of conducting material. Many of the geometries encountered in the design of resistors for micro-structures can be solved by taking advantage of standard transformations employed in the conformal mapping of complex functions.

4.2 Schwarz-Christoffel Transformation

This section describes the Schwarz-Christoffel transformation and uses it to solve several typical problems.

A transformation that has proven to be a valuable tool is the general transformation of Schwarz-Christoffel. This transformation will transform any polygon in the Z-plane into the real axis of another complex plane Z_1. The transformation is given by [70]:

$$\frac{dZ}{dZ_1} = C_1 \, (Z_1 - a_1)^{(\alpha_1/\pi - 1)} \, (Z_1 - a_2)^{(\alpha_2/\pi - 1)} \dots \tag{4.5}$$

$$(Z_1 - a_n)^{(\alpha_n/\pi - 1)} \, ,$$

where C_1 is a constant and is determined by the boundary conditions, a_1 is the transformed point on the real axis of the Z_1-plane corresponding to a corner of the polygon in the Z-plane that is being transformed, and α_1 is the internal angle of the polygon in the Z-plane at the point associated with a_1. The area included inside the polygon is transformed into the upper half of the Z_1-plane. A requirement is placed on the a_1's such that $a_1 < a_2 < a_3 < \dots < a_n$. Any three of the a_1's can be chosen arbitrarily so long as the above condition is met. Although the transformation can always be formulated, the derivative dZ/dZ_1 must be integrated before the transformation can be performed. Even after the Schwarz-Christoffel transformation has been made, the problem is not solved. One must transform from the Z_1-plane into a plane in which the geometry of the problem assumes the configuration of a known solution.

4.2.1 Square Corner

The above procedures can best be demonstrated by an example. Consider the geometrical configuration shown in Figure 4-2. If the lengths of the branches are large compared to their widths, then in the limiting case the problem can be reduced to a four-angle polygon as shown in Figure 4-2a. by the broken lines. The transformation is then written as:
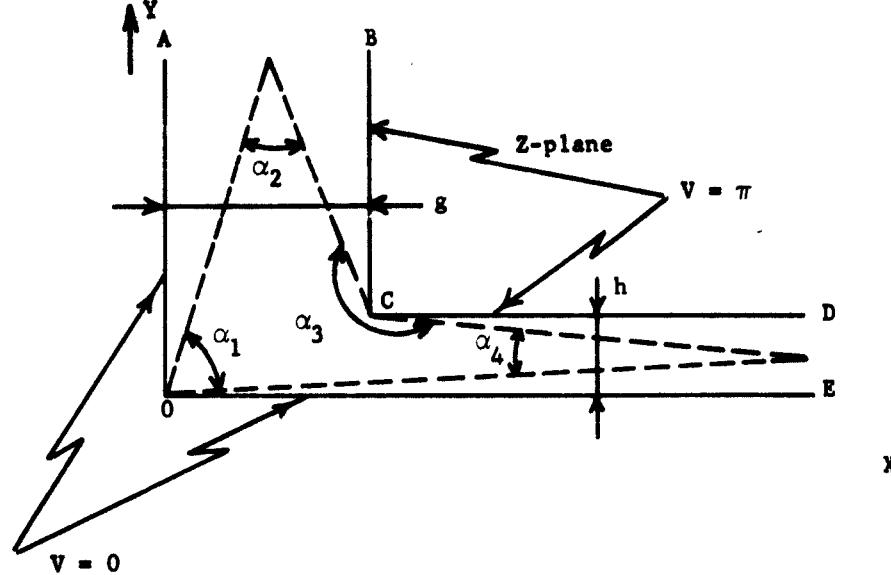
(a) A Right Angle Conducting Strip in the Z-plane
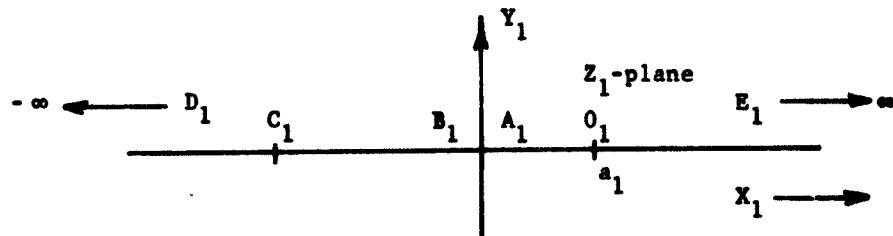
(b) The Strip in (a) Transformed to the Z_1-plane
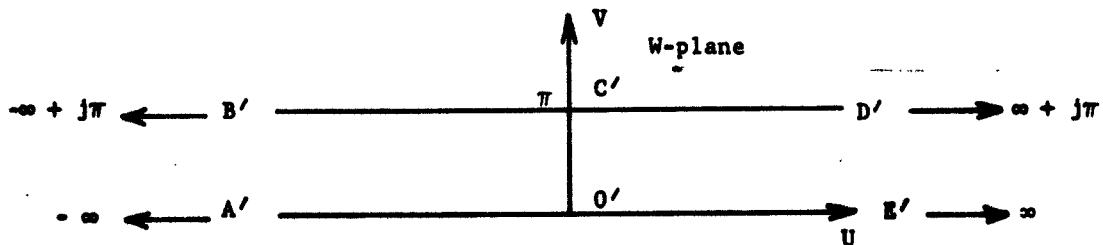
(c) The Strip in (a) Transformed to the W-plane

Fig. 4-2. Transformations of a Right Angle Bend Resistor

$$\frac{dZ}{dZ_1} = C_1(Z_1 - a_1)^{-1/2} (Z_1 - a_2)^{-1} (Z_1 - a_3)^{1/2} (Z_1 - a_4)^{-1} . \quad (4.6)$$

Since three of the four a_1's can be chosen arbitrarily, let $a_2 = 0$, $a_3 = -1$, and $a_4 = -\infty$. Equation (4.6) is reduced to:

$$\frac{dZ}{dZ_1} = \frac{C_1 (Z_1 + 1)^{1/2}}{Z_1 (Z_1 - a_1)^{1/2}} . \quad (4.7)$$

The boundary of the polygon in the Z-plane is then transformed into the real axis of the Z_1-plane as shown in Figure 4-2b. In order to evaluate the constants C_1 and a_1, consider the transition of Z_1 from the left side of the orgin to the right side by a minute semicircle of radius r, let:

$$Z_1 = r \exp (j\theta) ,$$

and then

$$dZ_1 = jr \exp (j\theta) d\theta .$$

Substituting into Equation (4.7) with $Z_1 \ll 1$ and $Z_1 \ll a_1$ yields

$$\int_g^0 dZ = jC_1 \ (-a_1)^{-1/2} \int_{-\pi}^0 d\theta ,$$

so that

$$a_1 = \frac{C_1^2 \pi^2}{g^2} .$$

Similarly the transition of Z_1 from $+\infty$ to $-\infty$ by a semicircle of infinite radius through an angle π yields

$$\int_0^{jh} dZ = \int_0^{\pi} C_1 jd\theta ,$$

so that

$$C_1 = h/\pi .$$

Therefore,

$$a_1 = (h/g)^2 .$$

Making the substitution $Z_1 = (u^2 + a_1) / (1 - u^2)$ and integrating
equation (4.7) yields: (U $\neq$ u which is a convenient integrating variable)

$$Z = \frac{2h}{\pi} \left\{ \frac{1}{\sqrt{a_1}} \tan^{-1} \frac{u}{\sqrt{a_1}} + 1/2 \ln \left(\frac{1 + u}{1 - u}\right) \right\} + C_2 . \qquad (4.8)$$

From the boundary condition $Z = 0$, $Z_1 = a_1$, $u = 0$, C_2 is found to be zero.

Notice that the line AOE has been transformed into the positive
real axis of the Z_1-plane and that the line BCD has been transformed
into the negative real axis of the Z_1-plane. The transformation

$$W = \ln(Z_1/a_1) \qquad (4.9)$$

will transform the real axis of the Z_1-plane into a strip as shown in
Figure 4-2c. Substituting Equation (4.9) into equation (4.8) yields:

$$Z = \frac{2h}{\pi} \left\{ \frac{1}{\sqrt{a_1}} \tan^{-1} \sqrt{\frac{e^W - 1}{a_1 e^W + 1}} + \right.$$

$$\left. 1/2 \ln \left[\frac{1 + \sqrt{a_1} \left(\frac{e^W - 1}{a_1 e^W + 1}\right)^{1/2}}{1 - \sqrt{a_1} \left(\frac{e^W - 1}{a_1 e^W + 1}\right)^{1/2}} \right] \right\} . \qquad (4.10)$$

For the special case of a square corner (g = h), $a_1 = 1$ and

$$Z = \frac{2h}{\pi} \left\{ \tan^{-1} \sqrt{\frac{e^W - 1}{e^W + 1}} + \tanh^{-1} \sqrt{\frac{e^W - 1}{e^W + 1}} \right\} . \qquad (4.11)$$

Differentiating Equation (4.11) implicitly and solving for $\left| \frac{dW}{dZ} \right|$ gives the current density:

$$J = \left| \frac{dW}{dZ} \right| = \left| \pi/h \left(\frac{e^W - 1}{e^W + 1} \right)^{1/2} \right| . \qquad (4.12)$$

When $Z = h + hj$, $W = 0 + j\pi$ and $dW/dZ \longrightarrow \infty$. This situation should be avoided in a good resistor design. This can be accomplished by rounding the inside corner as discussed in Section 4.2.2.

In order to calculate the resistance of the square corner, Equation (4.11) must be solved for the constant flow lines and the equipotential lines. Figure 4-3 is a plot of either U vs X/h or Y/h for V = 0 and V = π near the square corner. In order to compute the effective number of squares contributed by the corner, one needs only to read the value of U_2 and U_1 from the curve. As an example, suppose we wish to know the effective number of squares between X/h = 3 and Y/h = 3. Referring to Figure 4.2, we see that $V_2 = \pi$ and $V_1 = 0$. From Figure 4-3 we see that for X/h = 3, $U_2 = 7.3$ and for Y/h = 3, $U_1 = -7.3$. The effective number of squares is then:

$$R/\rho_s = \frac{U_2 - U_1}{V_2 - V_1} = \frac{14.6}{\pi} = 4.65 .$$

It turns out that many problems involving unique geometries can be solved by first applying the Schwarz-Christoffel transformation and secondly applying a logarithmic transformation. Although experience is the best indicator of the usefulness of the above transformations, a few guide lines can be suggested. Since there is flexibility in the Schwarz-Christoffel transformation, in many instances it is possible to transform
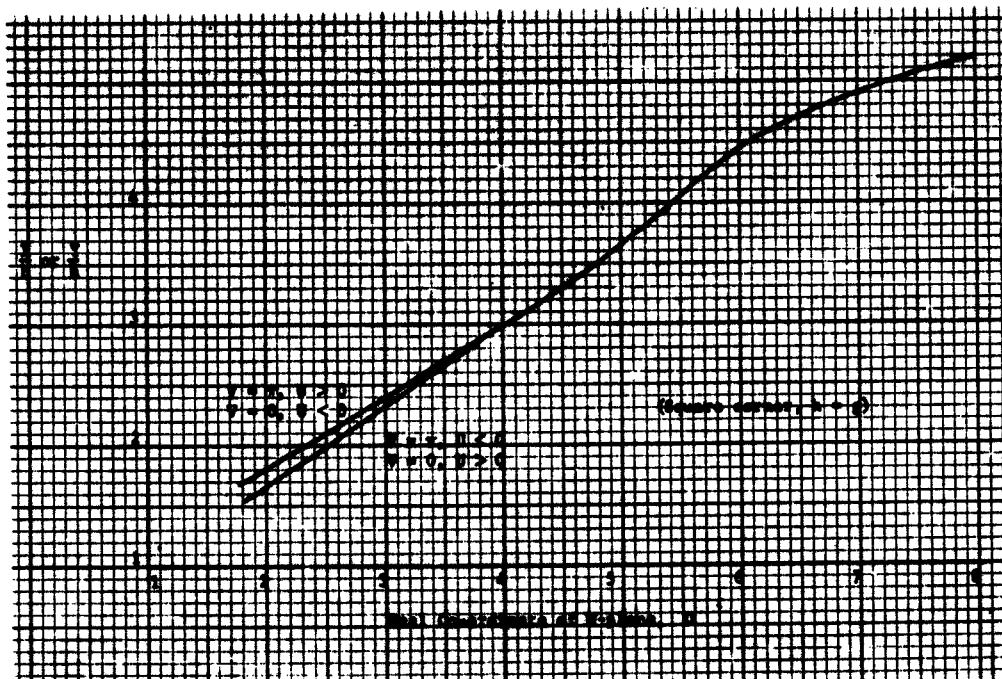
Fig. 4-3. Dependence of Real Co-ordinate of W-plane on Normalized Components of Z-plane

either the constant potential or constant flow boundaries in the Z-plane into the real axis of the Z_1-plane in such a manner that the logarithmic transformation is a natural second transformation. In other cases it is necessary to apply two successive Schwarz-Christoffel transformations in order to solve the problem. In any case, it is desirable to take advantage of symmetry and limiting situations where possible.

4.2.2 Rounded Corner

As mentioned earlier, the right-angle bend in a conducting strip leads to an infinite current density at the inside corner. The problem can be eliminated by rounding the inside corner. A theoretical treatment has been given the rounded corner case by Dow [71]. The following discussion is a summary of his work. The right-angle bend with the inside corner rounded is shown in Figure 4-4. The Schwarz-Christoffel transformation can be made to take into account a rounded corner at the origin of the Z-plane by replacing the term $(Z_1 - 0)^{(\alpha/\pi - 1)}$ by
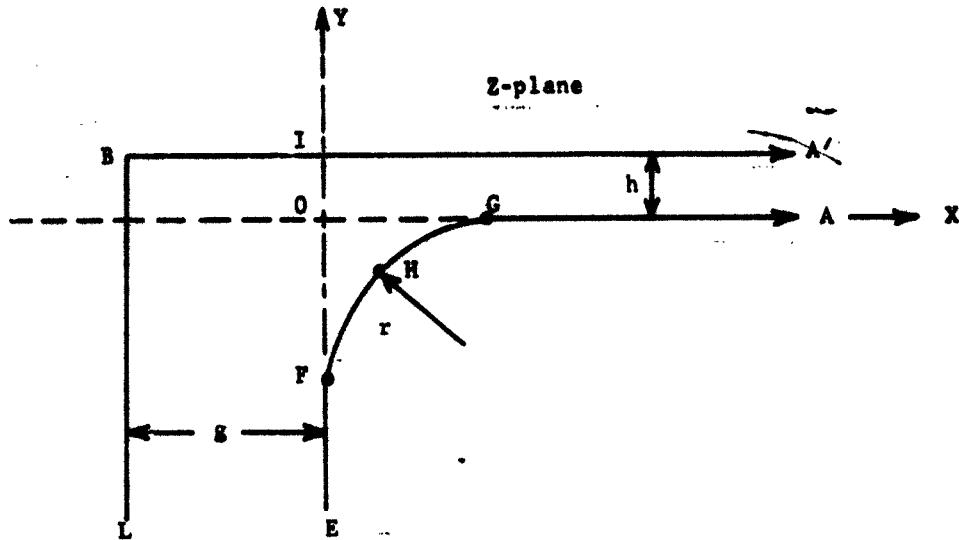
(a) A Rounded Corner Conducting Strip in the Z-plane
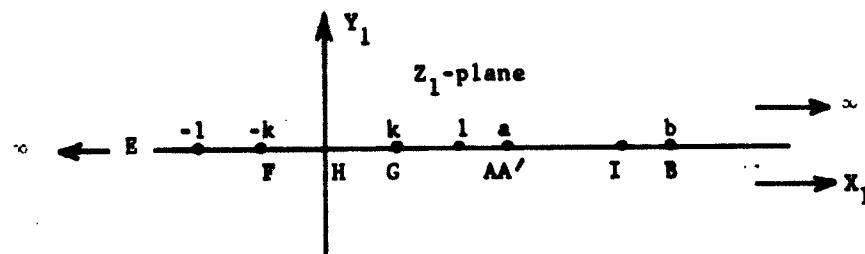
(b) The Strip in (a) Transformed to the Z_1-plane
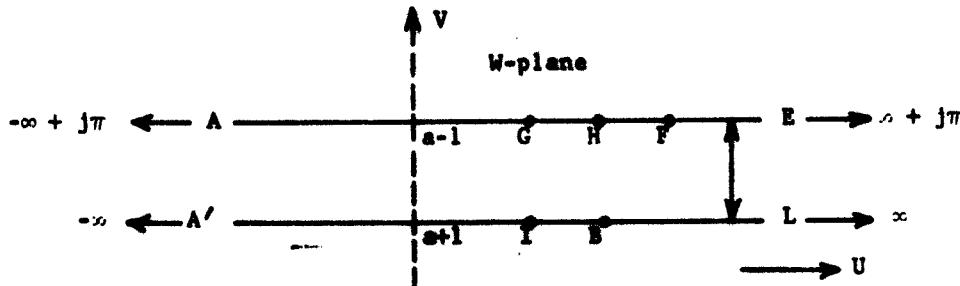
(c) The Strip in (a) Transformed to the W-plane

Fig. 4-4. Transformations of a Rounded Corner Resistor

$$(Z_1 + k)^{(\alpha/\pi - 1)} + \lambda \ (Z_1 - k)^{(\alpha/\pi - 1)} \ ,$$

where k is a constant and has much the same role as the a_i's. The factor λ can be used to adjust the shape of the curve between $Z_1 = k$ and $Z_1 = -k$. When the above substitution is made, the Schwarz-Christoffel transformation for the geometry shown in Figure 4-4 reduces to the following:

$$\frac{dZ}{dZ_1} = -j \ \frac{(Z_1 + k)^{1/2} + \lambda \ (Z_1 - k)^{1/2}}{(Z_1 - a) \ (Z_1 - b)^{1/2}} \ . \qquad (4.12)$$

If λ is chosen to be $\sqrt{(b + k) \ / \ (b - k)}$, then the flow lines are constant around the corner. Integrating Equation (4.12) and applying the boundary conditions yield:

$$Z = 2 \ \sqrt{\frac{a + k}{b - a}} \ \tanh^{-1} \sqrt{\frac{Z_1 + k}{b - Z_1} \cdot \frac{b - a}{a + k}} - 2 \ \tan^{-1} \sqrt{\frac{Z_1 + k}{b - Z_1}}$$

$$- \ 2 \ j\lambda \ \left\{ \tanh^{-1} \sqrt{\frac{k - Z_1}{b - Z_1}} - \sqrt{\frac{a - k}{b - a}} \ \tan^{-1} \sqrt{\frac{k - Z_1}{b - Z_1} \cdot \frac{b - a}{a - k}} \right\} \ .$$

As a second transformation, let $Z_1 = a + e^W$. The original geometry is then transformed as shown in Figure 4-4c. The current density is given by:

$$\left| dW/dZ \right| = \left| \frac{\sqrt{Z_1 - b}}{\sqrt{Z_1 + k} + \lambda \ \sqrt{Z_1 - k}} \right| \ . \qquad (4.13)$$

Figure 4-5 is a plot of the ratio $J_c \ / \ J_o$ vs r/g for the special case of equal strip widths, $(g = h)$ where J_c is the current density along the inside of the rounded corner and J_o is the current density at a large distance away from the bend. As the radius r approaches zero, the current density along the curved corner approaches ∞. As shown in
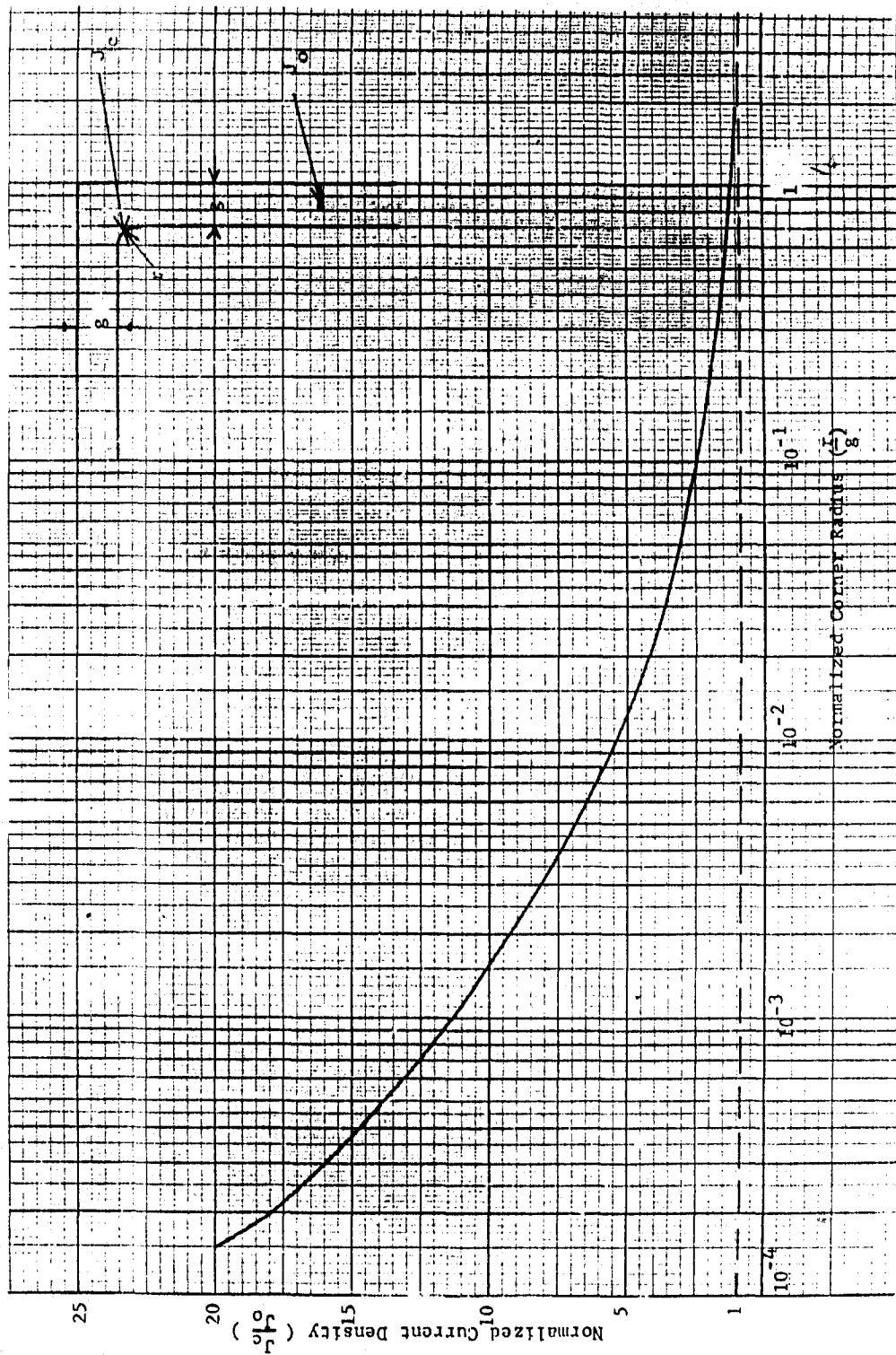
Fig. 4-5. Maximum Current Density (J_c) Achieved by Rounding the Corner of a Right Angle Turn

the figure, only a very small rounding will reduce the current density to a reasonable magnitude. For the case where r = g the current density along the curved corner has increased only about 25% over that in the leg.

The calculations necessary to determine the resistance of the rounded corner as a function of dimensions constitute a laborious task; however, experimental results have shown that the resistance of the rounded corner differs only by a few per cent from that of the right-angle case when the radius is less than or equal to the dimension of a leg. Figure 4-6 shows the equipotential and constant flow lines for the case of a right-angle bend. Figure 4-7 is the same as that of Figure 4-6 except the inside corners have been rounded.

The current crowding problem in a right-angle bend can be avoided by placing a contact (tap) over the corner as shown in Figure 4-8. This approach offers the additional advantage of resistance adjustment.

4.2.3   Contacts to a Conductive Sheet

Another geometry that is frequently encountered in microsystem resistor design is shown in Figure 4-9a. This two dimensional arrangement could, for example, represent the cross-section of a bulk silicon resistor, i.e., a resistor that is formed by simply placing contacts on the surface of a silicon block. An approximation that is commonly made is that the resistance of the element is equal to ρ d/wt, where d is the distance between contacts, w is the width of the contact,* and t is the thickness of the block or film. This assumption is not always valid as shall be shown in the following discussion.

This problem can be solved analytically by first performing a Schwarz-Christoffel transformation and secondly performing an inverse Schwarz-Christoffel transformation. Referring to Figure 4-9, the region of interest in the Z-plane as shown in Figure 4-9a is transformed into the Z_1-plane as shown in Figure 4-9 b by the transformation:

$$\frac{dZ}{dZ_1} = \frac{1}{(Z_1 - a_1)(Z_1 + a_1)} \qquad (4.14)$$

* Note: w is not W.
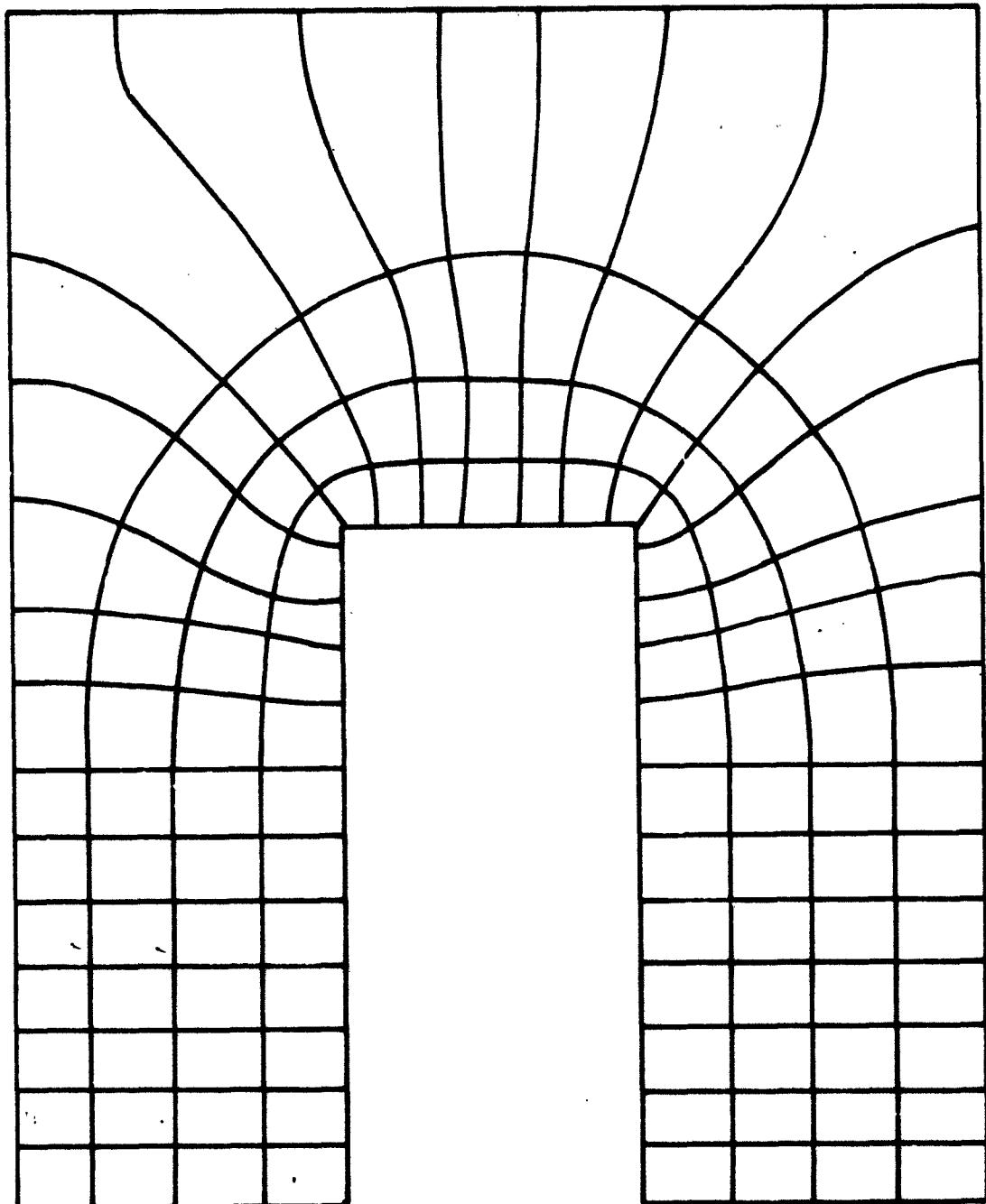
Fig. 4-6. Equipotential and Equiflow Lines for Right Angle Corner
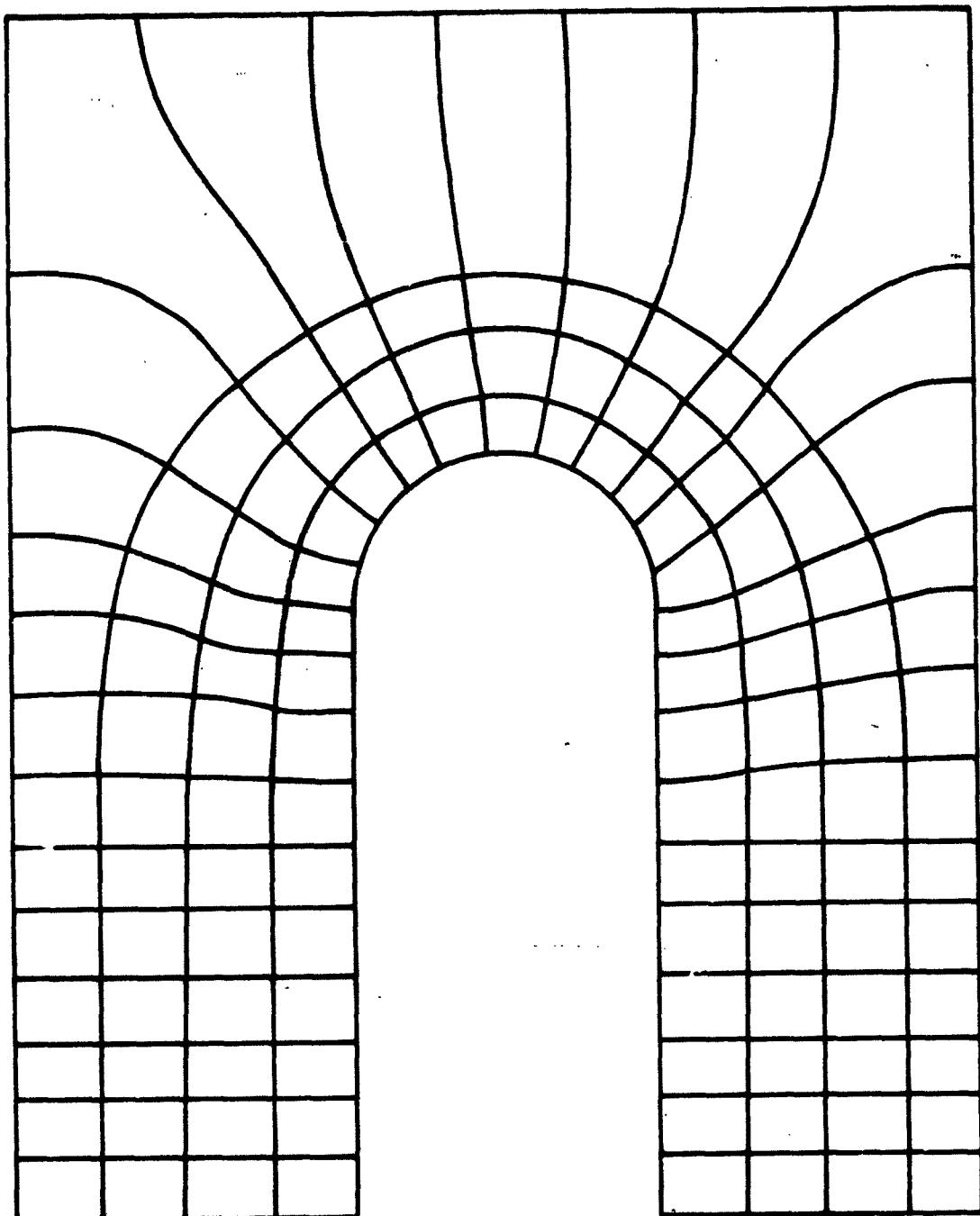
Fig. 4-7. Equipotential and Equiflow Lines for Rounded Corner

resistive region

contacts
(good conductor)
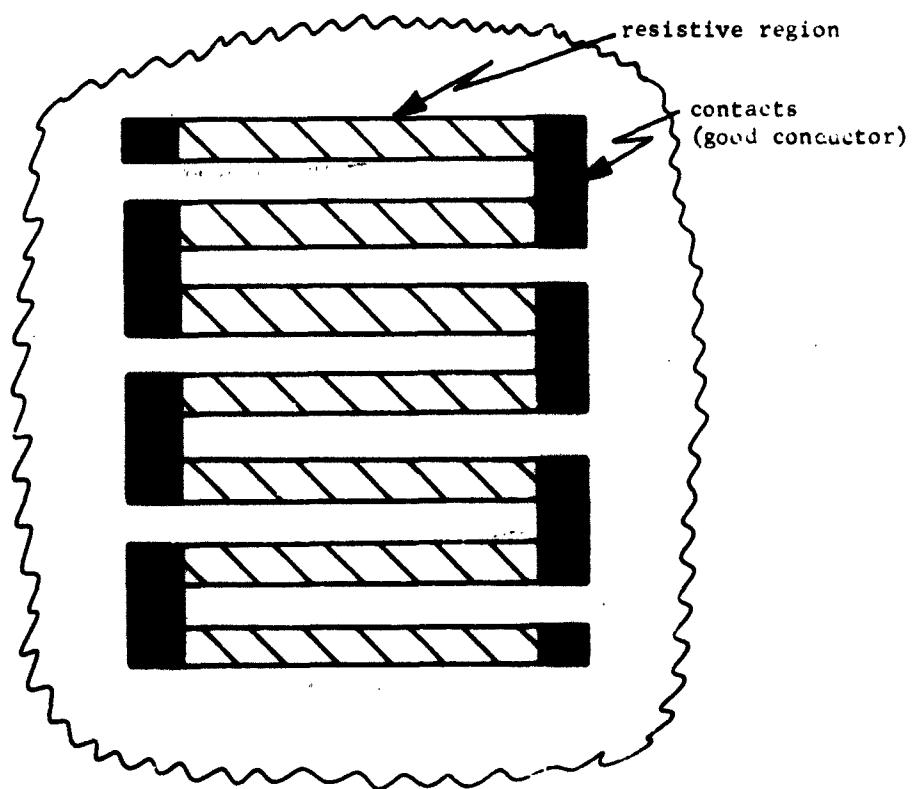
Fig. 4-8. An Alternate Method for Avoiding the High Current Densities
Normally Associated with Right Angle Turns
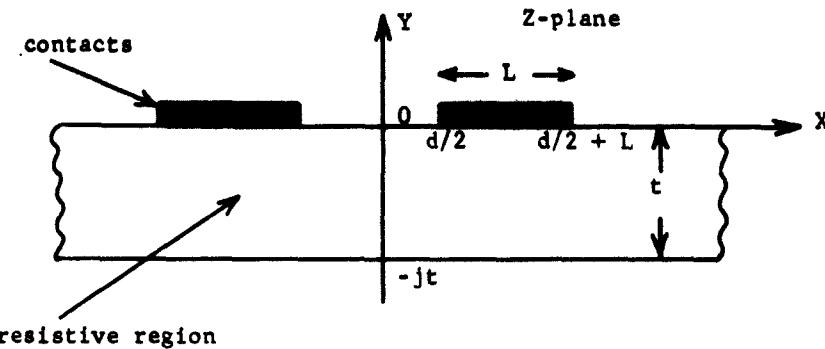
(a) Ohmic Contacts on a Block of Material in the Z-plane
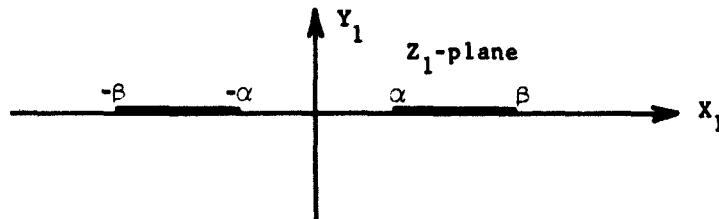
(b) The Geometry in (a) Transformed to the Z_1-plane
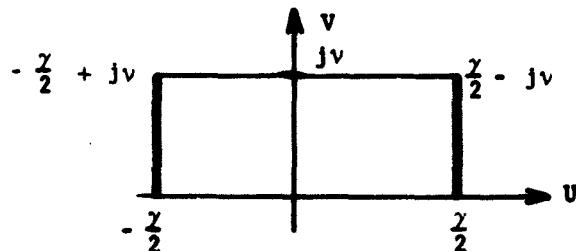
(c) The Geometry in (a) Transformed to the W-plane

Fig. 4-9. Transformations of a Diffused or Bulk Resistor

When the assumption is made that the conducting medium is an infinite strip, integrating (4.14) yields:

$$Z = \frac{1}{2a_1} \ln \frac{(Z_1 - a_1)}{(Z_1 + a_1)} + C_1 \, , \qquad (4.15)$$

applying the boundary condition $Z_1 = 0$ when $Z = 0$ gives the result: $C_1 = -j\pi/2a_1$. Applying the boundary condition $Z_1 = \infty$ when $Z = -jt$ yields: $a_1 = \pi/2t$. Solving Equation (4.15) for Z_1 gives:

$$Z_1 = -\pi/2t \tanh \frac{\pi Z}{2t} \, , \qquad (4.16)$$

for which the points α and β in the Z_1-plane as shown in Figure 4.9b, are given by:

$$\alpha = -\pi/2t \tanh \frac{\pi d}{4t} \qquad (4.17)$$

and

$$\beta = -\pi/2t \tanh \left(\frac{\pi L}{2t} + \frac{\pi d}{4t} \right) \, . \qquad (4.18)$$

The inverse Schwarz-Christoffel transformation

$$W = \int_0^{Z_1} \frac{dZ_1}{\sqrt{(\alpha^2 - z_1^2)(\beta^2 - z_1^2)}} \qquad (4.19)$$

transforms the upper half of the Z_1-plane into the W-plane as shown in Figure 4-9c. Solving Equation (4.19) for the real and imaginary parts of W yields:

$$U = \int_0^{\alpha} \frac{dZ_1}{\sqrt{(\alpha^2 - z_1^2)(\beta^2 - z_1^2)}} \qquad (4.20)$$

and

$$V = \int_\alpha^\beta \frac{dZ_1}{\sqrt{(Z_1^2 - \alpha^2)\,(\beta^2 - Z_1^2)}} \quad \bullet \qquad (4.21)$$

Equations (4.20) and (4.21) are elliptic integrals which can be evaluated with the aid of elliptic integral tables.

The resistance is then given by:

$$R = \rho_s \frac{U_2 - U_1}{V_2 - V_1} = \rho_s \frac{\gamma}{\nu} \, , \qquad (4.22)$$

where

$$\gamma = 2 \int_o^\alpha \frac{dZ_1}{\sqrt{(\alpha^2 - Z_1^2)(\beta^2 - Z_1^2)}} \qquad (4.23)$$

and

$$\nu = \int_\alpha^\beta \frac{dZ_1}{\sqrt{(Z_1^2 - \alpha^2)\,(\beta^2 - Z_1^2)}} \quad \bullet \qquad (4.24)$$

The current density is:

$$J = \left| \frac{dW}{dZ} \right| = \left| \frac{dW}{dZ_1} \right|\left| \frac{dZ_1}{dZ} \right| = $$

$$(4.25)$$

$$\frac{\tanh^2 \frac{\pi z}{2t} - 1}{\sqrt{(\tanh^2 \frac{\pi d}{4t} - \tanh^2 \frac{\pi z}{2t})\,(\tanh^2 [\frac{\pi z}{2t} + \frac{\pi d}{4t}] - \tanh^2 \frac{\pi z}{2t})}} \quad \bullet$$

Figure 4-10 is a plot of γ/ν vs d/t. Note that when $d/t \geq 10$, $\gamma/\nu \approx d/t$. It should also be kept in mind that the approximation has been made that the conducting medium extends a few thicknesses beyond the contacts.

In passing it might be noted that the capacitance of the structure shown in Figure 4-9a is given by:

$$C = \epsilon_o K \frac{V_2 - V_1}{U_2 - U_1} = \frac{\epsilon_o K \nu}{\gamma} \,, \tag{4.26}$$

where K is the dielectric constant of the conducting medium.

The discussion as presented above is that of a two dimensional system and does not offer a complete solution to the bulk resistor problem since it is a three-dimensional system. It does however give some insight as to the nature of a solution. For the case of a diffused resistor the two-dimensional solution is a very good approximation and in some cases is exact. The latter being the case for a conducting strip which is thin and bounded by a "non-conducting" medium.

4.2.4 Other Geometries

The following are the transformations and solutions for the geometry as shown in Figure 4-11:

$$\frac{dZ}{dZ_1} = \pm \frac{2jk}{\pi} \frac{(Z_1^2 - a^2)^{1/2}}{Z_1(Z_1^2 - 1)^{1/2}} \,, \tag{4.27}$$

$$Z \approx \frac{2}{\pi}\left\{ k \tan^{-1} \left(\frac{e^{2W} - a^2}{1 - e^{2W}}\right)^{1/2} + h \tan^{-1} a\left(\frac{1 - e^{2W}}{e^{2W} - a^2}\right)^{1/2}\right\}, \tag{4.28}$$

$$\frac{dW}{dZ_1} = \frac{1}{Z_1} \,, \tag{4.29}$$
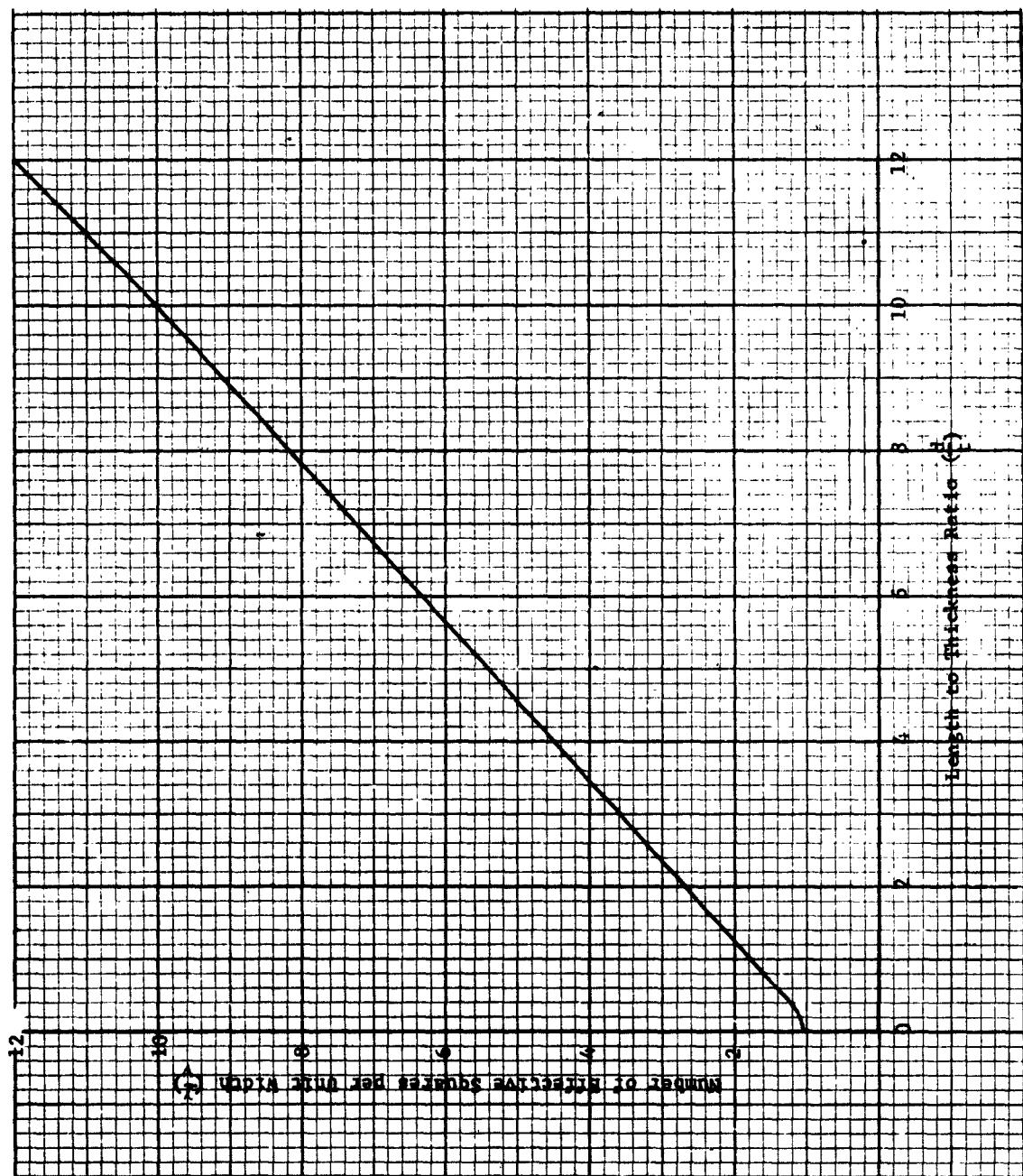
Fig. 4-10. The Dependence of the Effective Number of Squares Between Ohmic Contacts on the Surface of a Conductive Sheet upon the Length to Thickness Ratio
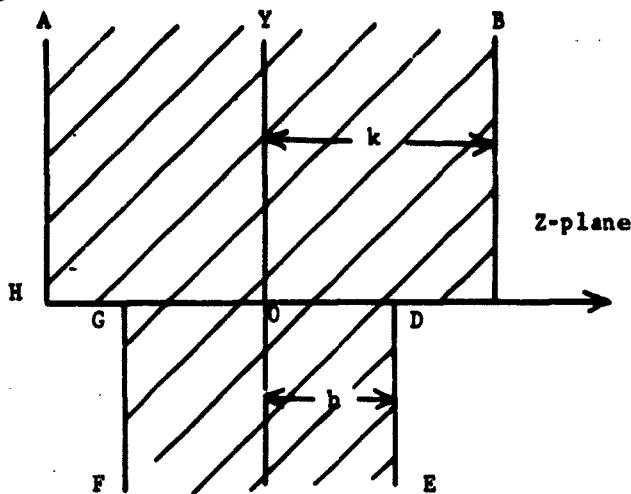
(a) Reduced Conducting Strip in the Z-plane
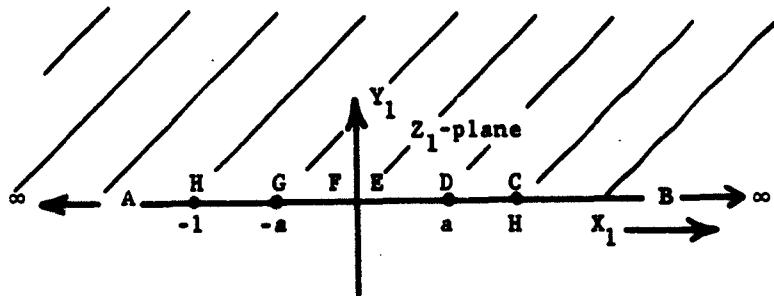
(b) Geometry in (a) Transformed to the Z_1-plane
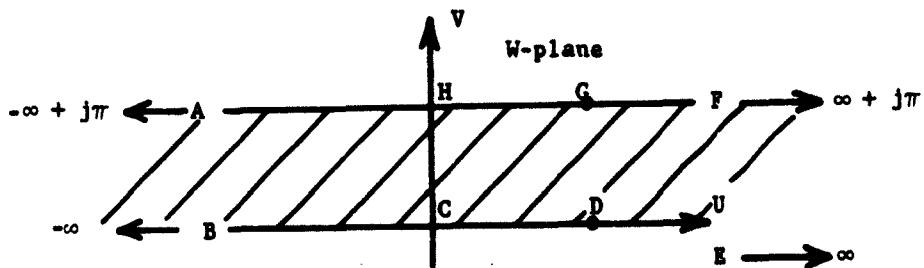
(c) Geometry in (a) Transformed to the W-plane

Fig. 4-11. Transformations of a Reduced Section Resistor
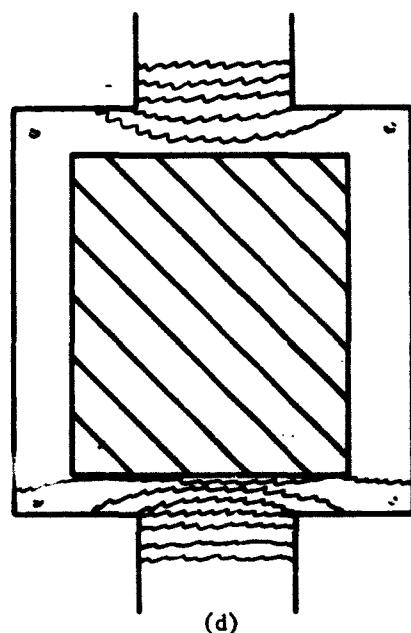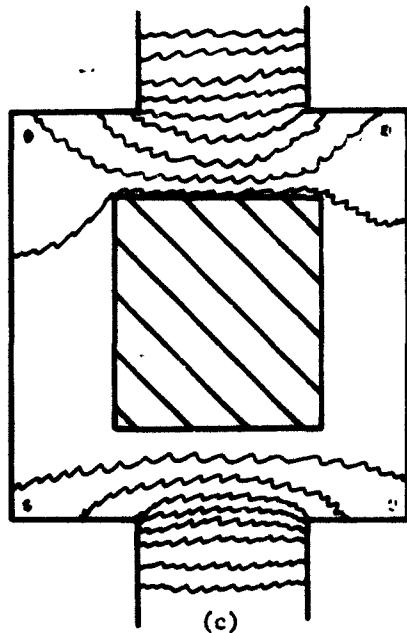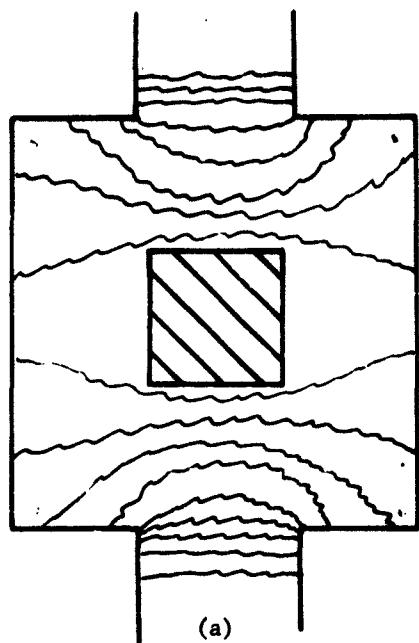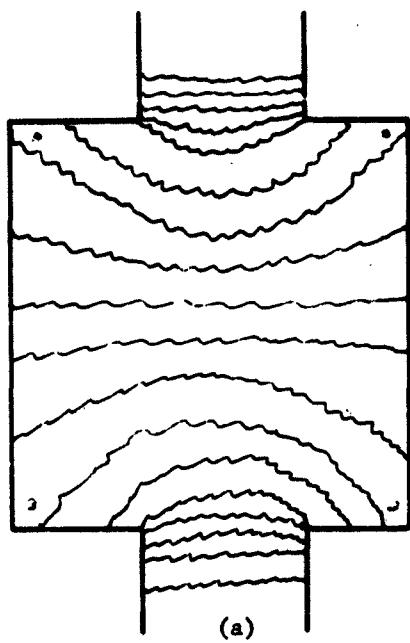
☐ –resistive region   ▧ –conducting region

Fig. 4-12.   Equipotential Plot of Geometry Shown for Various Sizes of
Conducting Squares in the Center

4-23

$$J = \frac{\pi}{2k} \left| \frac{(z_1^2 - 1)^{1/2}}{(z_1^2 - a^2)^{1/2}} \right| \cdot \qquad (4.30)$$

A technique that has been used very successfully for obtaining empirical solutions of two-dimensional resistance problems is the use of resistance paper which has been cut into the desired geometrical configuration on which equipotential plots can be made. An example of its usefulness is shown in Figure 4-12. In this case it was of interest to determine the effect of placing a square conductor or a tap of varying area in the center of the large square as shown in the figure. Equipotential plots were made which demonstrate quite clearly the effect on the resistance and the field of placing a center tap in the large square.

4.3 Conclusion

The preceding discussion of geometries applicable to resistor design is by no means complete. It is the intent of the discussion to introduce some of the more common designs and to indicate a method of solution. The methods used in solving the particular applications are not unique. Another powerful tool that has not been discussed is that of "images" as applied in the study of field theory. The method of images is best suited for problems that have either a point source or point sink, i.e. contacts with negligible dimensions. See references [72] and [73] for examples of the method.

5. CONCLUSIONS AND RECOMMENDATIONS

In the integrated silicon devices which are now available, the
diffused resistor is generally employed. Usually this resistor utilizes
the impurity diffusion which forms the base region of the transistor
structures and is characterized by a sheet resistivity of 100-500 ohms/
square. Isolation is obtained by diffused barriers through the epitaxial
layer on which the integrated structure is formed. A diffused resistor
of this type has a high TCR, a limited range of resistance values, poor
high frequency isolation from other elements of the structure, and a
tolerance determined by the precision of the base diffusion and the
precision of the photoengraving process. Diffused resistors, on the
other hand, do not require additional process steps and can be made to
acceptable tolerances. The temperature dependence is unimportant in
some applications and can be compensated in others.

Some of the disadvantages of the diffused resistor are not found in
the thin film resistor formed on the surface of the oxide. Current efforts
toward this resistance element indicate early availability of integrated
structures utilizing it. It will consist of either metal or metal-oxide
films formed by vacuum or chemical deposition and photoengraving. Advan-
tages of this design are a much lower TCR, a wider range of values and
perhaps improved isolation. The primary disadvantages are the extra
process steps required and the somewhat intangible effects on reliability
and yield when additional chemical species and processes are introduced
into an integrated device.

Most of the integrated silicon devices of the immediate future will
employ either the diffused silicon resistor or the thin-film resistor or
both. Some applications will require modification of conventional circuits,
while others will require a redefinition of electronic functions in terms
of the new technology. New design will probably reduce the use of the
high cost integrated resistors in favor of the less expensive diodes
and transistors.

While the diffused silicon resistor has been and will continue to
be used successfully for many applications and while the addition of the
thin-film resistor seems assured of providing even more capability and

versatility, the size limitations of these resistors, both electrical and physical, make them unsatisfactory for certain applications. Technology capable of controllably and reproducibly fabricating layers with sheet resistivity in the neighborhood of 10^5-10^7 ohms/square is necessary. Improvements in present techniques may be able to achieve this goal or perhaps radically different types of resistors must be developed such as those employing the reverse (or forward) resistance of a p-n junction.

This is most important for the high resistance, low power elements required for nanowatt devices.

Specifically, this study has indicated the following recommendations in the consideration of resistance for integrated silicon devices:

1. Improve diffused resistor techniques through better process control.

2. Continue development of compatible thin-film resistors.

3. Re-examine functional design to minimize use of resistors.

4. Perform research directed toward controlling resistance of diodes or other junction structures.

The ultimate solution to the resistance problem lies in the introduction of distributed parameter structures and the gradual evolution to the "molecular electronic" device wherein the conventional elements lose their identity.

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Unclassified Report

Both conventional and unconventional methods of achieving the resistive function in integrated silicon devices are discussed in this report. The properties and types of resistors made of silicon are considered in some detail as well as general design procedures. Many charts and graphs are reproduced in the hope of providing a convenient source of

(over)

1. Resistors
2. Molecular Electronics
3. Resistance
4. Silicon Resistors
I. AFSC Project 4159, Task 4159-05
II. Contract AF 33 (657)-10340
III. Research Triangle Institute, Durham, North Carolina
IV. R. P. Donovan
V. Not aval for OTS
VI. In ASTIA collection

information pertinent to the design of resistors for integrated silicon devices.

The more recent trend toward combining thin film passive components on a silicon substrate containing the active elements is discussed in less detail, not because this technique is felt to be less important but because information is sparse on such devices and their fabrication.