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DEVELOPMENT OF
C- AND X-BAND
POWER GENERATORS

Report No. 3

Contract DA-36-039-SC90757

Technical Requirement SCL7629A

Dated 7 November 1961

Project 3A99-21-002

Third Quarterly Period
1 December 1962 to 28 February 1963

The objective of this program is to conduct research work leading to development of C-Band, 10 watt; and X-Band, 2.5 watt, solid-state pulsed-power generators.

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1.0 PURPOSE

The purpose of the program under Signal Corps Contract DA-36-039-SC90757 is to conduct research work leading to the development of the following solid-state pulsed-power generators:

- 1) A C-Band, 5 gc, 10 watt generator
- 2) An X-Band, 10 gc, 2.5 watt generator.

2.0 ABSTRACT

This report (Report No. 3) covers the third quarterly period (1 December 1962 to 28 February 1963) of Sylvania's program to develop C- and X-band, solid-state, pulsed-power generators for the Signal Corps under Contract DA-36-039-SC90757.

Implementation of the "indirect" power generation technique employing a transistorized exciter and a cascaded chain of six frequency multipliers was continued during this period. The feasibility of obtaining a transistorized exciter output of 60 w at 156 mc to drive the cascaded chain of frequency multipliers was verified.

Design of the intermediate- and high-power amplifiers was completed. Marriage testing of the transistorized exciter modules was performed and the desired power output of 60 w was achieved using the breadboard models.

The bridge-type circuit has been successfully implemented in the lumped-element and distributed-element harmonic generators. A conversion efficiency of -1.75 db has been obtained for a four-diode bridge doubler with an output power of 27.2 w

2.0
(Cont.)

at an input frequency of 156 mc; a conversion efficiency of -3.8 db has been obtained for a two-diode bridge doubler circuit with an output power of 3.3 w at an input frequency of 1.25 gc. Efforts to increase the efficiency of the high-frequency multiplier are continuing.

3.0

CONFERENCES

A project conference was held on 19 February 1963, at Fort Monmouth, New Jersey. Participants were Messrs. R. McIntyre and T. Leonard representing Sylvania, and Messrs. V. Boxer, G. Hambleton, and K. Klohn representing USASRD. The technical requirements of the program and its status to date were reviewed and the availability of state-of-the-art diodes required for the harmonic multipliers was discussed.

4.0

FACTUAL DATA

4.1

Introduction

This section contains the results obtained during the third quarterly period of Sylvania's C- and X-band pulsed-power generator program conducted under Signal Corps contract DA-36-039-SC90757.

4.2

General Consideration

The approach utilizing the "indirect" power generation technique was continued throughout this reporting period. Investigation of available characteristics and circuit techniques makes the planned utilization of two-diode bridge circuits in all but the first diode multiplier, which will use four diodes, appear practical.

4.3 Transistorized Exciter

Development of the 60-w transistorized exciter (shown in figure 1) was completed. The major engineering effort during this reporting period was expended on the development and testing of the intermediate- and high-power amplifiers and the low-power oscillator-amplifier.

Design objectives for the transistorized exciter are:

| | | |
|-----------------------|---|--------------------------|
| Power output | : | 60 w |
| Frequency | : | 156 mc |
| Temperature range | : | -40 to 60°C |
| Frequency stability | : | 5×10^{-5} mc/°C |
| Pulse repetition rate | : | 100 - 4000 cps |
| Pulse rise time | : | 50 nsec. |

The output power and pulse repetition rate of the exciter were verified and documented in laboratory tests. Further testing to determine compliance with the remaining objectives will be conducted in a pulsed mode of operation.

4.3.1 Intermediate-Power Amplifier Development

With a nominal 170 mw input from the oscillator-amplifier, the intermediate-power stages are required to provide 16 w to the high-power amplifier.

The amplifier employs two transistors (2N1562) in parallel in the first stage amplifying the 170 mw input power to a 1-w level. The following stage utilizes an SN103 to provide a nominal power output of 4.5 w and the last stage uses a parallel configuration of 2-SN103's to provide a 16-w output to the high-power amplifiers. Table I lists the performance of each stage in the module.

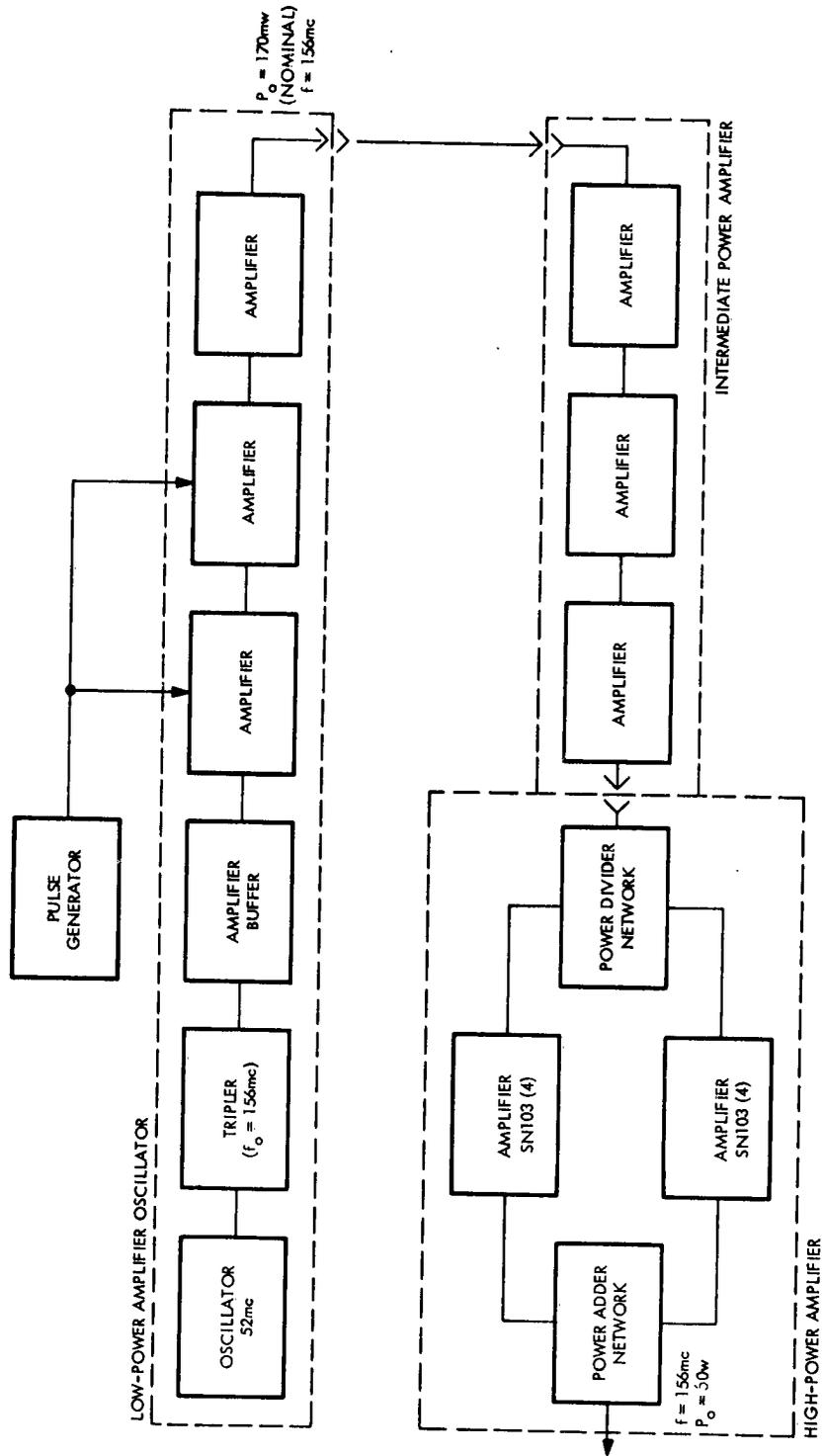


Figure No. 1
Transistorized Exciter, Block Diagram

4.3.1
(Cont.)

Table No. I

Intermediate-Power Amplifier Performance

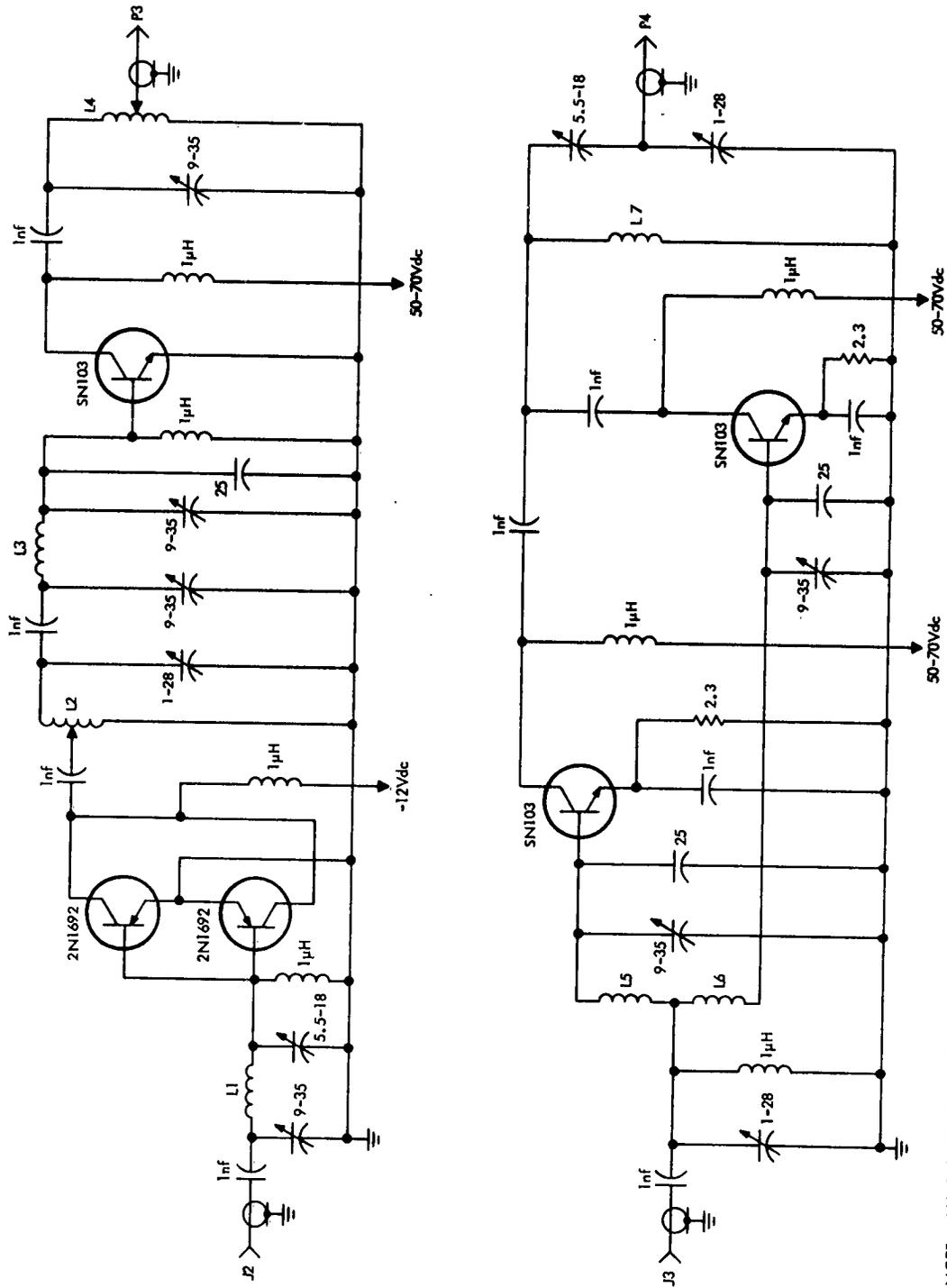
| Stage | P _{in} (w) | P _{out} (w) | V _{cc} (Vdc) | I _c (ma) |
|-------|------------------------|-------------------------|--------------------------|------------------------|
| 1 | 0.2 | 1.1 | 12 | 185 |
| 2 | 1 | 4 | 50 | 165 |
| | 1 | 5.4 | 65 | 170 |
| 3 | 4 | 12 | 50 | 190 |
| | 4 | 16 | 65 | 205 |

The amplifier circuitry is designed to employ a low-loaded Q (Q_1) in the input and output circuits to enable the circuits to amplify the pulsed r-f energy with a minimum of degradation in the rise time (t_r) and fall time (t_f) of the pulse envelope. The second harmonic content of the amplifier is -16 db when referenced to the fundamental frequency output power. A further reduction in the second harmonic will be realized because the power divider and the input matching circuits of the high-power amplifiers are pi networks. A schematic of the intermediate-power amplifier is shown in figure 2.

4.3.2 High-Power Amplifier Development

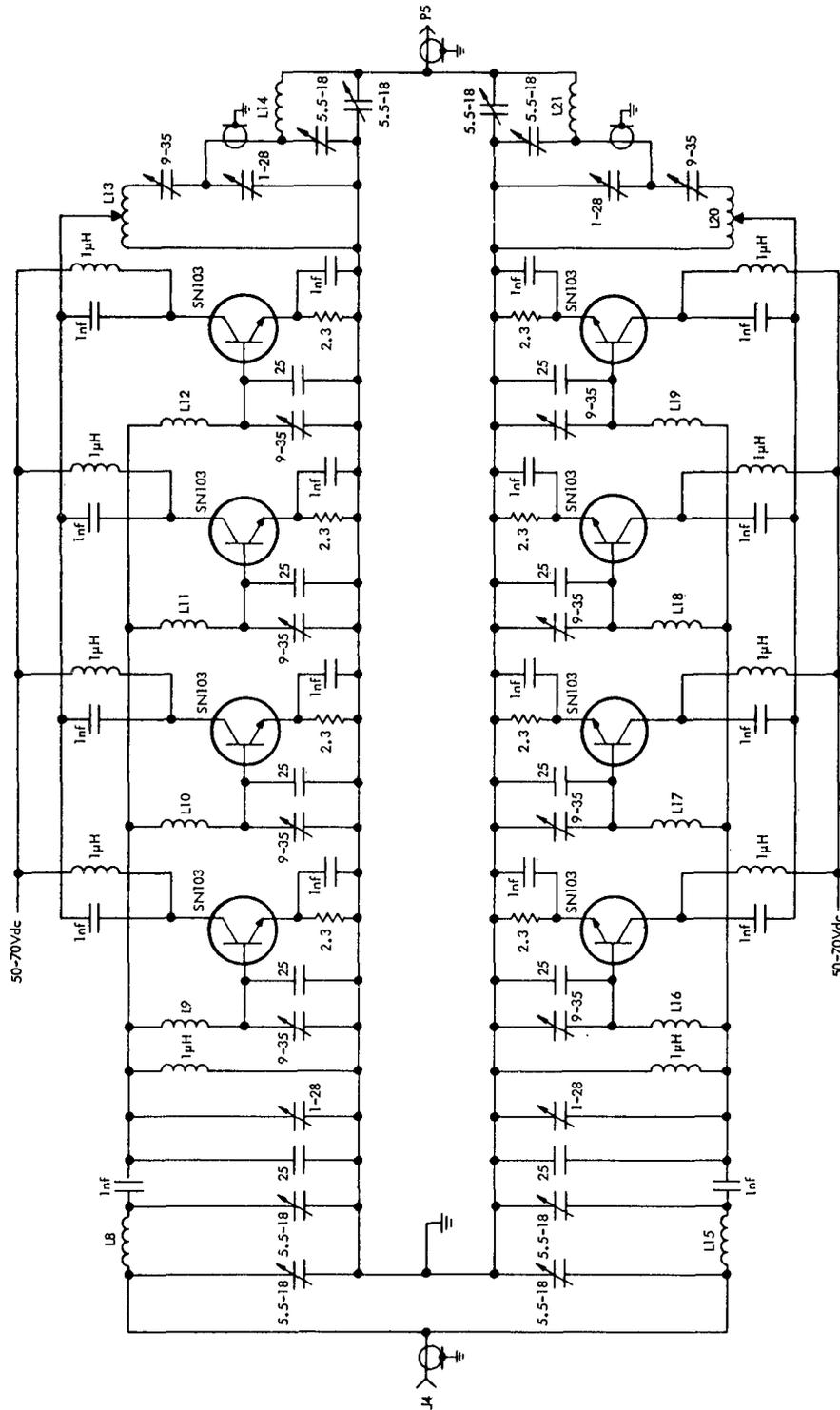
The high-power amplifier provides 6 db of gain at 156 mc with an input of 16 w supplied by the intermediate-power amplifiers yielding a nominal 60-w output. This gain is achieved by operating the collector of the device at a 70Vdc level. Operation of the device at this voltage level has been discussed previously in the second quarterly report (pages 10 to 14)(Ref. 1). Table II lists the performance of this stage at 50 and 70Vdc levels.

1. Development of C- and X-Band Power Generators, Report No. 2, Sylvania Rpt. no. A35-5-5. 0-15, 31 December 1962.



NOTE: ALL CAPACITORS IN pf UNLESS OTHERWISE INDICATED.

Figure No. 2
Intermediate-Power Amplifier Schematic



NOTE: ALL CAPACITORS IN pf UNLESS OTHERWISE SPECIFIED.
ALL RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.

Figure No. 3
High-Power Amplifier Schematic

4.3.2
(Cont.)

Table No. II
High-Power Amplifier Performance

| P_{in} (w) | P_o (w) | V_{cc} (Vdc) | I_c per unit (ma) | Efficiency (%) |
|-----------------|--------------|-------------------|------------------------|-------------------|
| 8 | 24 | 50 | .175 | 69 |
| 8 | 32 | 70 | 185 | 62 |

Two paralleled amplifiers (8-SN103's), a power divider network, and a power adding network comprise the high-power amplifier shown in figure 3. The input power is divided in the power divider resulting in 8 w being supplied to each of the parallel amplifiers (four transistors each). The 30-w output of each amplifier is summed in the power adder network to yield a total power output of 60 w.

The power adder and divider networks, being bilateral in nature and having equal input and output impedances are interchangeable. Basically, the power divider or adder is two pi networks having an impedance transformation of 100 ohms to 50 ohms. Two of these pi networks are combined to yield the network shown in figure 4.

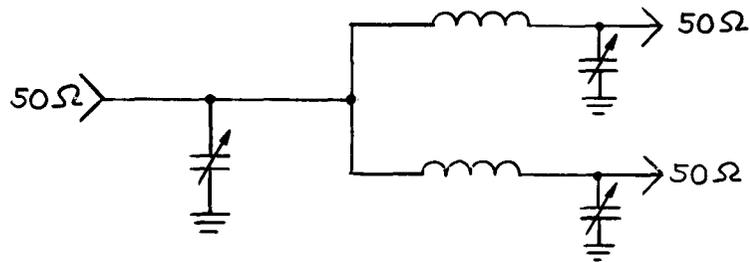


Figure No. 4
Power Adder or Divider Network Schematic

4.3.2
(Cont.)

The network has a Q_1 of less than 5, thereby providing three immediate advantages:

- 1) High efficiency, where the efficiency of a coupling network is given by

$$\eta = 1 - \frac{Q_1}{Q_{\text{unloaded}}}$$

- 2) Easy tuning.
- 3) Minimum phase variation due to a center frequency shift caused by component variations as a function of temperature.

The amplifier configuration used in the final stage consists of 4 - SN103 transistors connected in parallel. This circuit resulted from extensive evaluations of several configurations and was selected because:

- 1) It was easily tuned.
- 2) It had high efficiency (66%).
- 3) Implementation was readily accomplished.
- 4) Input and output shielding is inherent in circuit implementation.

Balancing the d-c collector currents was accomplished by utilizing the input matching network shown in figure 5. This method of coupling allowed for a close match of the impedance of each amplifier to the 50 ohm output impedance of the power divider network. The r-f power supplied to each amplifier controls the amount of dc current flowing in the device and when the average current of

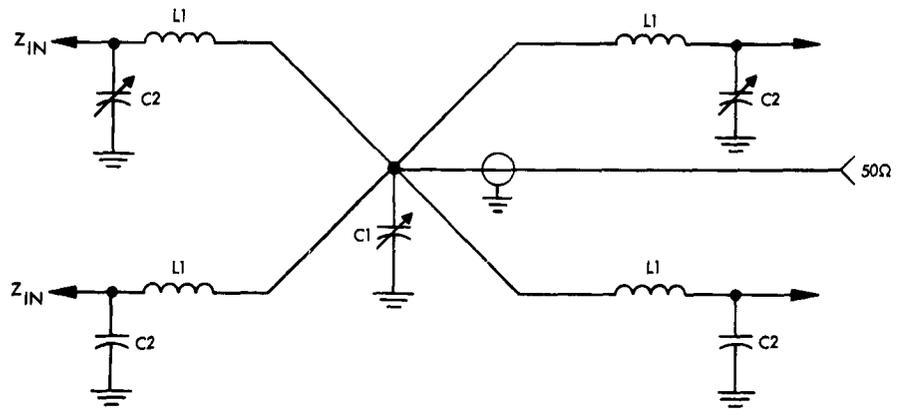
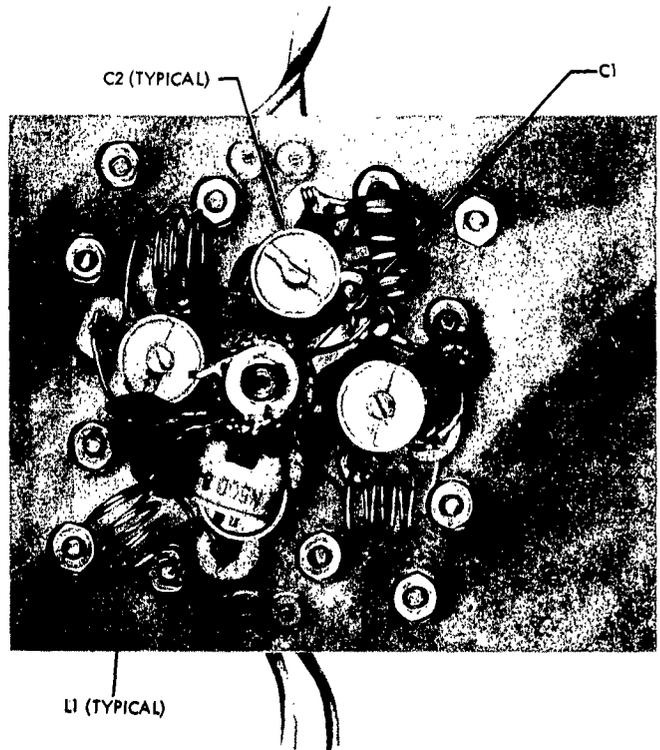


Figure No. 5 Input Matching Network

4.3.2
(Cont.)

each transistor is equal, the d-c input power to each device is equal. To determine total device dissipation (P_{dt}) it is assumed that the gain and power output of all transistors are equal. This assumption is permissible in a pulsed mode of operation when the total dissipation is very much less than the maximum allowable collector dissipation for the transistor used.

However, for continuous operation, the measuring technique must be further elaborated to provide an accurate indication of the power contributed by each device and its gain. The necessity for this can readily be seen if the equation for P_{dt} is considered:

$$P_{dt} = I_c V_{cc} + P_{in} - P_o$$

where:

| | | |
|----------|---|-----------------------|
| I_c | = | D-C Collector Current |
| V_{cc} | = | Collector Voltage |
| P_{in} | = | Input Power, RF |
| P_o | = | Output Power, RF |

Thus, to accurately predict the P_{dt} for each transistor its input and output power levels must be known.

4.4 Frequency Multipliers

4.4.1 Bandwidth Considerations

Three primary performance parameters which must be considered in the design of frequency multipliers are: (1) the power level of operation, (2) the efficiency of frequency conversion and (3) the bandwidth. Power level and efficiency have been discussed in the second quarterly report (Ref. 1) and numerous references discussing

4.4.1
(Cont.)

the predictions are available; therefore, some attention will now be given to the third parameter - bandwidth.

The frequency multiplier bandwidth is the most difficult parameter to evaluate because it is dependent upon the inherent properties of the diode and the manner in which it is incorporated into the multiplier circuit. Comments on bandwidth expressed in literature (Ref. 2) have been limited to cursory observations and suggestions for higher-order frequency multipliers.

Definitions used in linear circuit analysis ($BW = f_o/Q = f_2 - f_1$) are not directly applicable to strongly nonlinear problems. In the frequency multiplier, static Q is not an important parameter in limiting the bandwidth as indicated by both theoretical considerations and laboratory measurements. When the varactor is operated in a dynamic frequency multiplier, the nonlinear capacitance presents a resistive load to the source so that the dynamic Q is quite low. The bandwidth is related to a dynamic Q rather than a static Q but the exact relation is not clearly understood. Experimentally, frequency doublers with a 25 percent bandwidth in the 100 to 600 mc range have been fabricated utilizing diodes with large static Q 's ($\omega_c/\omega_{in} = 500$) as measured at voltage breakdown. However, doublers in the C- and X-band region exhibit bandwidths of a few percent with diodes having static Q 's of 30. Even if an appropriate Q could be found, the center frequency (f_o) is in question in the multiple frequency device.

The fundamental difference in bandwidth between frequency multipliers has been the technique of circuit implementation. Two

2. J. McDade, "Varactor Microwave Frequency Multipliers", Diamond Ordnance Fuze Laboratories, 18 July 1962.

4.4.1
(Cont.)

specific areas in the design of typical frequency multipliers contribute to narrowing the response of the device (figure 6). These are the input/output matching networks and the resonant traps which prohibit unwanted frequencies from entering the input or output ports. Both of these networks are usually single-tuned because of the ease of design; however, bandwidth and tunability of the multiplier suffer considerably.

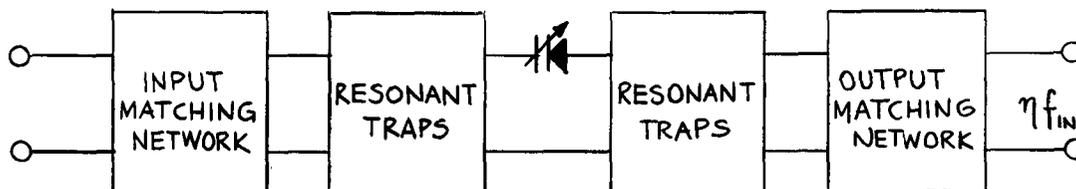


Figure No. 6
Typical Single-Diode Frequency Multiplier,
Block Diagram

The second approach to defining the bandwidth ($f_2 - f_1$), can be misleading unless caution is exercised. McDade (Refs. 2 and 3) has shown that varactor diode circuits can exhibit a "jump" effect due to severe distortion of the response curve, (figure 7). Both theoretical considerations and laboratory measurements verify the possibility of the occurrence of a triple-valued function (figure 7b);

3. J. McDade, "Jump Phenomena in Varactor Diode Circuits", Diamond Ordnance Fuze Laboratories, 10 January 1962.

4.4.1
(Cont.)

consequently, there is a region in the response which is unstable so a "jump" effect may occur. This effect has not been verified theoretically for a frequency multiplier, but the "jump" phenomenon is observed in tuning frequency doublers resulting in input power, bias voltage, and impedance variations. The -3 db bandwidth for the distorted response curve provides useless information if any point on the curve within the -3 db points is triple valued since the point could represent unstable operation.

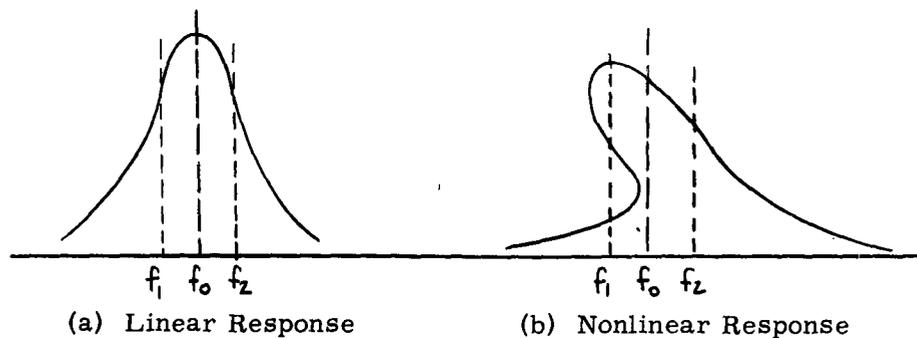


Figure No. 7
Diode Circuit "Jump" Effect

The preceding comments indicate that the linear definitions are inadequate for predicting the bandwidth of frequency multipliers. A usable bandwidth can be determined by plotting the response curve for the operative frequency doubler. If the response yields a triple-valued function, the usable bandwidth must be limited to the stable region of the curve. In addition, it should be assumed that the fundamental bandwidth of the diode is known. The general approach

4.4.1
(Cont.)

to determining the response curve is to write the differential equation describing the doubler, and to impose restrictions and boundary values which are compatible with maximum performance.

4.4.2 Frequency Doublers (156, 312.5, and 625 mc)

Selection of the frequency doubler circuits was made by considering the bandwidth and power requirements of the chain. The bandwidth should be 15-20 mc to prevent degradation in the r-f pulsed waveform. Power handling requirements of the first two doublers are shown in figure 8. Balanced-bridge configurations have yielded bandwidths exceeding 20 percent. The balanced circuit accomplished frequency separation by symmetry rather than tuned resonant traps so that significant bandwidth improvements may be anticipated. (Ref. 4).

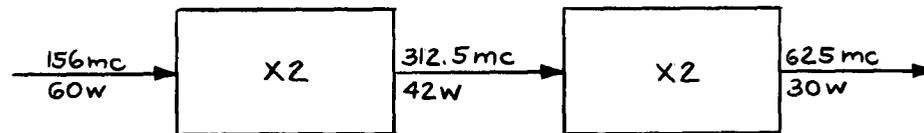


Figure No. 8
Frequency Doubler Power Requirements

Successful implementation of the frequency multiplier chain strongly depends on the fundamental concept of the balanced-bridge configuration. All of the known balanced-bridge frequency doublers can be considered special cases of the basic bridge circuit (figure 9).

4. P. Penfield, Jr., "Frequency Separation by Symmetry", M. I. T. Internal Memo No. 70, Energy Conversion Group, 13 August 1962.

4. 4. 2
(Cont.)

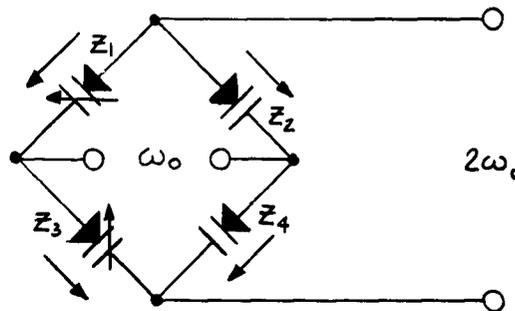


Figure No. 9
Basic Balanced-Bridge Circuit

A source at ω_o is applied to the bridge circuit containing four identical nonlinear circuit elements as shown. Since diode combinations 1-2 and 3-4 reflect equal impedances to the source from each branch, identical currents flow through the two branches. Consequently, diodes 1 and 4 are driven in phase as are diodes 2 and 3, but the two sets are driven 180° out of phase respect to each other and, due to the nonlinearity, currents at harmonic frequencies will occur. The currents can be defined as:

$$i_1 = i_4 = I_1 \sin \omega_o t + I_2 \sin (2\omega_o t + \theta_2) + I_3 \sin (3\omega_o t + \theta_3) + \dots$$

$$i_2 = i_3 = I_1 \sin (\omega_o t + \pi) + I_2 \sin (2\omega_o t + \theta_2 + 2\pi) + I_3 \sin (3\omega_o t + \theta_3 + 3\pi) + \dots$$

Inspection of these current equations indicates that only the odd-harmonic currents flow through the source and only the even-harmonic currents flow through the load. Two primary advantages of this circuit are the increased power conversion capability and

4.4.2
(Cont.)

the enhanced bandwidth. Both of these improvements can be made without sacrificing efficiency.

Many variations of the basic bridge circuit can be made while retaining the desired circuit properties. For example, two of the voltage-dependent capacitors can be replaced with fixed capacitors as shown in figure 10. This is the desired approach if only two diodes are required to convert the incident power to the desired harmonic.

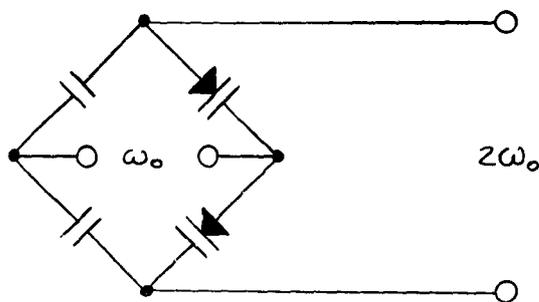


Figure No. 10
Balanced-Bridge with Two Diodes
(Two Fixed Capacitors)

Fixed inductances can also replace two of the diodes as shown in figure 11.

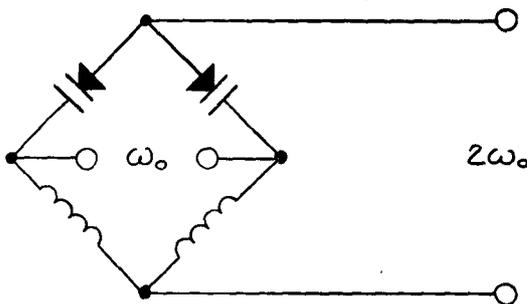


Figure No. 11
Balanced-Bridge with Two Diodes
(Two Fixed Inductances)

4.4.2
(Cont.)

In each of the bridge circuits described, a balanced input circuit results in an unbalanced output and vice versa. Using an unbalanced input circuit (figure 10) permits both diodes to be conveniently placed on the chassis thereby achieving optimum heat transfer. The resultant second harmonic output is balanced. The configuration shown in figure 11 has the output port unbalanced; therefore, a balanced input is required to drive the frequency doubler. A convenient method of supplying the required balanced input is shown in figure 12 (the conventional push-push doubler).

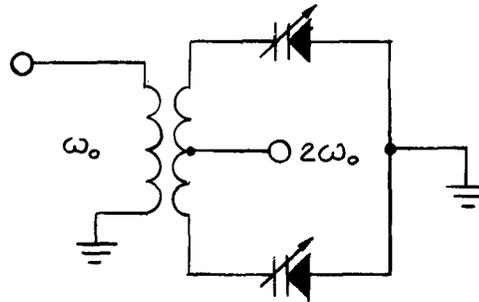


Figure No. 12
Push-Push Frequency Doubler Schematic

Various balanced-bridge circuit configurations were evaluated. Based on this evaluation, the circuit used in the 156.25 to 312.5 mc multiplier is shown in figure 13.

The varactors had balanced static characteristics so shunt capacitors were not required to balance the bridge and the d-c blocking capacitor was replaced with a trimmer capacitor to improve the input circuit matching. The circuit was adjusted for a 36-w cw input level and a 60 percent efficiency, and the power level was increased to demonstrate the power conversion capability of the circuit. Representative data is shown in (a) of table III.

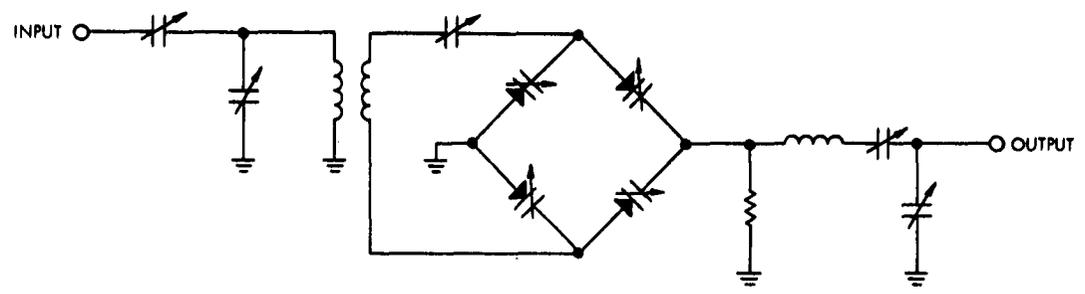


Figure No. 13
Four-Diode Bridge Doubler with
Unbalanced Output

4.4.2
(Cont.)

Table No. III
Four-Diode Balanced-Bridge Doubler cw Performance

| | P_{in} (w) | P_{out} (w) | Efficiency (db) | | |
|-----------------------------------|-----------------|------------------|--------------------|-------------|--------|
| a | 36 | 21.6 | -2.20 | R (ohms) | |
| | 46.8 | 28.4 | -2.16 | | |
| | 53.2 | 31.2 | -2.33 | | |
| b | 35.8 | 22.4 | -2.04 | | 200 k |
| | 35.4 | 22.2 | -2.04 | | 560 k |
| | 35.6 | 22.6 | -1.98 | | 1000 k |
| | 35.4 | 24.1 | -1.67 | | 00 |
| c | 40.8 | 27.2 | -1.75 | | |
| | *47.6 | 30.4 | -1.98 | | |
| | *54.8 | 33.6 | -2.18 | | |
| *Difficulty encountered in tuning | | | | | |

Once the feasibility was demonstrated, steps were taken to improve the efficiency. Variations of efficiency with the ohmic value of the bias resistor were noted as shown in (b) of table III. Indications were that the best performance was achieved when the self-bias resistor was removed. Other data taken at higher power levels is shown in (c) of table III. Considerable difficulty was encountered at higher power levels because of the sensitivity of the source to changes in the load; therefore, the efficiencies shown may not be representative of the maximum circuit performance.

4.4.2 (Cont.) A balanced-bridge, two-diode structure is expected to be used in the frequency range of 312.5 to 625 mc if the diodes can handle the input power. If a two-diode structure cannot accommodate the power level, a four-diode circuit similar to the first multiplier (156.25 to 312.5 mc) will be incorporated.

4.4.3 Distributed-Element Frequency Multipliers

Prior to diode selection, theoretical calculations were made to determine the desired parameters to insure device performance that would be compatible with generator requirements. The method used to predict the performance of the selected diodes evolved during the second quarterly period (Ref. 1) is described in the following paragraphs. γ nominally is assumed to be 0.42 and the input and output matching networks are each 90 percent efficient. The power output of the device can be predicted from the following equation:

$$P = A \frac{f_{in}}{f_c} \frac{V_b^2}{R_s}$$

where: A = Constant (0.1 for the overdriven condition)
f_{in} = Input frequency
f_c = Diode cutoff frequency
R_s = Diode spreading resistance
V_b = Diode breakdown voltage

4. 4. 3
(Cont.)

The efficiency of the stage as a multiplier can be calculated:

$$\epsilon = \frac{1 - B \frac{f_{in}}{f_c}}{1 + B \frac{f_{in}}{f_c}}$$

where: B = A constant equal to 11.7 for $\gamma = 0.42$

ϵ = Efficiency

The L-band stage uses a pair of RCA V521 diodes with parameters: $C_{min} = 1.6$ pf; $V_b = 150$ V; $f_{c-6} = 22.2$ gc. The theoretical efficiency is 67 percent or a 1.7 db conversion loss with each diode converting 14 w of power. The input power requirement at 625 mc is 30 w.

The L- to S-band stage uses two Sylvania D4264A diodes with parameters: $C_{-6} = 5$ pf; $f_{c-6} = 25$ gc; $V_b = 93$ V. The theoretical efficiency is 54.8 percent or a 2.6 db conversion loss with each diode being capable of converting 11.35 w. The input power requirement at 1.25 gc is 20 w.

Diodes for the S- to C-band multiplier were ordered, however, the manufacturer is experiencing technical difficulties with his manufacturing process and cannot meet the required specifications. A Sylvania D4253B was substituted, the parameters are: $C_{-6} = 3$ pf; $V_{b min} = 60$ V; $f_{c-6} = 40$ gc min.

The theoretical efficiency of the S- to C-band multipliers is 45 percent or a 3.47 db conversion loss with each diode being capable of handling 6.5 w. The input power requirement at 2.5 gc is 11 w.

4.4.3
(Cont.)

During the development phase it was found that the conversion loss in previous lower power S- to C-band multipliers could be reduced by 0.7 db if the output center conductor diameter was increased. The conversion gain for this modified doubler was -2.3 db and the efficiency of the diode was calculated to be 70 percent requiring an efficiency of 90 percent in the input and output circuits.

A bridge-type doubler breadboard model was developed and incorporated the above findings in the design. Preliminary testing showed a 3.8 db conversion loss for an 8 w input power at a 1.15 gc input frequency when doubling to 2.3 gc.

It is felt that this 3.8 db conversion loss will be reduced when the breadboard model is driven by the required 17 w since only at this higher input power level will the varactors be fully driven.

5.0

SUMMARY AND CONCLUSIONS

The transistorized exciter design was successfully completed. The main effort during this reporting period was expended in development of the intermediate- and high-power amplifiers. These stages amplify the pulsed r-f energy with a minimum amount of degradation in rise and fall time by employing low Q input and output circuits.

An output power of 60 w was obtained at 156 mc by paralleling transistors. This represents an increase of 8 over the output power obtainable with a single device. The exciter operates in a pulsed mode; however, increasing the dissipating capability of the thermal mount would enable continuous operation.

5.0
(Cont.)

Lack of a complete characterization of the varactor harmonic generator's bandwidth response has been considered and a general approach was outlined for determining the bandwidth response curve of the multipliers.

Various balanced-bridge circuit configurations were evaluated for the 156.25 to 312.5 mc frequency multiplier before the four-diode, balanced configuration was selected and demonstrated to be feasible. In the 312.5 to 625 mc multiplier, a balanced-bridge, two-diode configuration is expected to be incorporated in the final engineering model.

Development of the balanced-bridge technique in distributed-element circuits has resulted in a definite increase in state-of-the-art power outputs. Power outputs exceeding 10 w have been measured at 2.3 gc in experimental circuits. With the implementation of more effective thermal mounts, operation of these multipliers in a cw mode is possible.

Performance predictions of selected diodes were made utilizing the method evolved during the second quarterly period of this program.

6.0

PROGRAM FOR NEXT QUARTER

The deliverable equipment will be completed and tested to determine compliance with the requirements established for the pulse generator and to define the final performance characteristics.

Effort will be completed on the development of the 312.5 to 625 mc multipliers and distributed-element harmonic generators.

The final report will be generated.

7.0 IDENTIFICATION OF PERSONNEL

Key personnel contributing to this project are listed below, along with the approximate number of man-hours of effort expended by each during the period covered by this report.

- | | | | |
|----|-------------|---------------------------|-----------|
| 1) | J. Kellett | - Adv. Research Engineer: | 56 hours |
| 2) | T. Leonard | - Research Engineer: | 428 hours |
| 3) | R. McIntyre | - Research Engineer: | 378 hours |
| 4) | J. Keptner | - Electrical Engineer: | 461 hours |

Respectfully submitted



R. McIntyre
Project Engineer
Sylvania Electronic Systems-Central

AD-

Abstract Card Info.
Div. 5/2, 8/2, 5, 6

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Sylvania Electric Products Inc., Amherst Laboratories, Buffalo, N. Y.

DEVELOPMENT OF C- AND X-BAND POWER GENERATORS

Rept. for 1 Dec 62 - 28 Feb 63 on r-f Power Generators

by R. McIntyre 1 Apr 63, 31 p. incl. 13 illus, 3 tables, 4 ref.

(Rept. No. A35-5-5.0-25)

(Contract DA -36-039-SC90757)

Unclassified report

DESCRIPTORS: Electronic Circuits, *Microwave Networks, *Oscillator Circuits, *Tuned Circuits, *Frequency Stabilizers, *Microwave Equipment, *Radiofrequency Generators, *Micro-waves, *Radiofrequency Oscillators, *Radiofrequency Power, Crystal Oscillators, *Microwave Oscillators, Oscillators, *Radio-frequency Oscillators, Radio Equipment, Radio Transmitters, Electronics, *Semiconductors, *Transistors, Transmission Lines, Waveguides.

Implementation of the "indirect" power generation techniques was continued throughout this reporting period. A 60 w pulsed-output power level at 156.25 mc was achieved for the transistorized exciter and the frequency multiplier configuration was established as a cascaded chain of six frequency doublers. Design of the intermediate- and high-power amplifiers was completed. Marriage testing of the transistorized exciter modules was performed and the desired power output of 60 w was achieved using the breadboard models. The bridge-type circuit has been successfully implemented in the lumped-element and distributed-elements harmonic generators. A conversion efficiency of -1.75 db has been obtained for a four-diode bridge with an output power of 27.2 w at an input frequency of 156 mc; a conversion efficiency of -3.8 db has been obtained for a two-diode bridge circuit with an output power of 3.3 w at an input frequency of 1.25 gc. Efforts to increase the efficiency of the high-frequency multiplier are continuing.

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