

**UNCLASSIFIED**

---

---

**AD 401 183**

*Reproduced  
by the*

**DEFENSE DOCUMENTATION CENTER**

FOR

**SCIENTIFIC AND TECHNICAL INFORMATION**

CAMERON STATION, ALEXANDRIA, VIRGINIA



---

---

**UNCLASSIFIED**

NOTICE: When government or other drawings, specifications or other data are used for any purpose other than in connection with a definitely related government procurement operation, the U. S. Government thereby incurs no responsibility, nor any obligation whatsoever; and the fact that the Government may have formulated, furnished, or in any way supplied the said drawings, specifications, or other data is not to be regarded by implication or otherwise as in any manner licensing the holder or any other person or corporation, or conveying any rights or permission to manufacture, use or sell any patented invention that may in any way be related thereto.

63-3-2

# PLANAR INTEGRATION OF THIN FILM FUNCTIONAL CIRCUIT UNITS

CATALOGED BY ASTIA  
AS AD 401183

Signal Corps Contract Number DA-36-039-sc-87246

401183

**FINAL REPORT**

1 May 1961

to

31 December 1962

**REPORT NO. 4**

ASTIA  
APR 10 1963  
ASTIA

Department of the Army	Project No.	3G26-14-001
Department of the Army	Task No.	3G26-14-031-01

IBM COMMAND CONTROL CENTER  
FEDERAL SYSTEMS DIVISION  
KINGSTON, NEW YORK

U.S. ARMY ELECTRONICS RESEARCH AND DEVELOPMENT LABORATOR  
FORT MONMOUTH, NEW JERSEY

**"QUALIFIED REQUESTORS MAY OBTAIN COPIES OF THIS REPORT FROM ASTIA"**

<p>AD _____ Accession No. _____</p> <p>International Business Machines Corporation, Federal Systems Division Command Control Center, Kingstom, New York</p> <p>PLANAR INTEGRATION OF THIN FILM FUNCTIONAL CIRCUIT UNITS</p> <p>R. L. Bullard - W. N. Carroll - R. Ghaag - P. C. Marr - A. E. Lessor - F. L. Sautz</p> <p>Final Report, Report No. 4, 1 May 1961 to 31 December 1962, pp-Ilus-Graphs, Signal Corps Contract DA 36-039-sc-87246, Unclassified Report</p> <p>The investigation of practical methods of integrating functional micro- miniature semiconductor devices to vacuum deposited planar thin film networks. The method selected is to provide a means for rapidly connecting devices to film panels, and to allow the removal and replacement of these devices at high maintenance schedules.</p> <p>The improvement of processes and controls for the fabrication of multilayer film circuits and interconnections.</p> <p>The fabrication, and demonstration of a functional multilayer thin film electronic assembly employing the techniques and processes developed in Phases I and II. The demonstration assembly is to contain approximately fifty circuits with appropriate film interconnections to perform a representative digital function, and to achieve a parts density of approximately 600,000 components per cubic foot.</p>	<p>Unclassified</p> <ol style="list-style-type: none"> <li>1. Integration Techniques</li> <li>2. Process Controls</li> <li>3. Functional Assemblies</li> </ol>	<p>AD _____ Accession No. _____</p> <p>International Business Machines Corporation, Federal Systems Division Command Control Center, Kingstom, New York</p> <p>PLANAR INTEGRATION OF THIN FILM FUNCTIONAL CIRCUIT UNITS</p> <p>R. L. Bullard - W. N. Carroll - R. Ghaag - P. C. Marr - A. E. Lessor - F. L. Sautz</p> <p>Final Report, Report No. 4, 1 May 1961 to 31 December 1962, pp-Ilus-Graphs, Signal Corps Contract DA 36-039-sc-87246, Unclassified Report</p> <p>The investigation of practical methods of integrating functional micro- miniature semiconductor devices to vacuum deposited planar thin film networks. The method selected is to provide a means for rapidly connecting devices to film panels, and to allow the removal and replacement of these devices at high maintenance schedules.</p> <p>The improvement of processes and controls for the fabrication of multilayer film circuits and interconnections.</p> <p>The fabrication, and demonstration of a functional multilayer thin film electronic assembly employing the techniques and processes developed in Phases I and II. The demonstration assembly is to contain approximately fifty circuits with appropriate film interconnections to perform a representative digital function, and to achieve a parts density of approximately 600,000 components per cubic foot.</p>	<p>Unclassified</p> <ol style="list-style-type: none"> <li>1. Integration Techniques</li> <li>2. Process Controls</li> <li>3. Functional Assemblies</li> </ol>
<p>AD _____ Accession No. _____</p> <p>International Business Machines Corporation, Federal Systems Division Command Control Center, Kingstom, New York</p> <p>PLANAR INTEGRATION OF THIN FILM FUNCTIONAL CIRCUIT UNITS</p> <p>R. L. Bullard - W. N. Carroll - R. Ghaag - P. C. Marr - A. E. Lessor - F. L. Sautz</p> <p>Final Report, Report No. 4, 1 May 1961 to 31 December 1962, pp-Ilus-Graphs, Signal Corps Contract DA 36-039-sc-87246, Unclassified Report</p> <p>The investigation of practical methods of integrating functional micro- miniature semiconductor devices to vacuum deposited planar thin film networks. The method selected is to provide a means for rapidly connecting devices to film panels, and to allow the removal and replacement of these devices at high maintenance schedules.</p> <p>The improvement of processes and controls for the fabrication of multilayer film circuits and interconnections.</p> <p>The fabrication, and demonstration of a functional multilayer thin film electronic assembly employing the techniques and processes developed in Phases I and II. The demonstration assembly is to contain approximately fifty circuits with appropriate film interconnections to perform a representative digital function, and to achieve a parts density of approximately 600,000 components per cubic foot.</p>	<p>Unclassified</p> <ol style="list-style-type: none"> <li>1. Integration Techniques</li> <li>2. Process Controls</li> <li>3. Functional Assemblies</li> </ol>	<p>AD _____ Accession No. _____</p> <p>International Business Machines Corporation, Federal Systems Division Command Control Center, Kingstom, New York</p> <p>PLANAR INTEGRATION OF THIN FILM FUNCTIONAL CIRCUIT UNITS</p> <p>R. L. Bullard - W. N. Carroll - R. Ghaag - P. C. Marr - A. E. Lessor - F. L. Sautz</p> <p>Final Report, Report No. 4, 1 May 1961 to 31 December 1962, pp-Ilus-Graphs, Signal Corps Contract DA 36-039-sc-87246, Unclassified Report</p> <p>The investigation of practical methods of integrating functional micro- miniature semiconductor devices to vacuum deposited planar thin film networks. The method selected is to provide a means for rapidly connecting devices to film panels, and to allow the removal and replacement of these devices at high maintenance schedules.</p> <p>The improvement of processes and controls for the fabrication of multilayer film circuits and interconnections.</p> <p>The fabrication, and demonstration of a functional multilayer thin film electronic assembly employing the techniques and processes developed in Phases I and II. The demonstration assembly is to contain approximately fifty circuits with appropriate film interconnections to perform a representative digital function, and to achieve a parts density of approximately 600,000 components per cubic foot.</p>	<p>Unclassified</p> <ol style="list-style-type: none"> <li>1. Integration Techniques</li> <li>2. Process Controls</li> <li>3. Functional Assemblies</li> </ol>

PLANAR INTEGRATION OF THIN FILM

FUNCTIONAL CIRCUIT UNITS

FINAL REPORT

REPORT NO. 4

May 1, 1961 to December 31, 1962

The object of this program is the development of a multilayer thin film planar integration technique and the establishment of a practical method for interconnecting microminiature semiconductor device packages.

Signal Corps Contract No.  
Signal Corps Specification  
Department of the Army Project No.  
Department of the Army Task No.

DA-36-039-sc-87246  
SCL 7586 20 October 1960  
3G26-14-001  
3G26-14-031-01

R. L. Bullard - W. N. Carroll - R. Glang - P. C. Karr - A. E. Lessor - F. L. Stutz

International Business Machines Corporation  
Federal Systems Division  
Command Control Center  
Kingston, New York

## TABLE OF CONTENTS

		<u>Page</u>
SECTION 1.	PURPOSE	1
	1.0 Objectives	1
	1.1 Related Projects	1
SECTION 2.	ABSTRACT	3
SECTION 3.	PUBLICATIONS, LECTURES, REPORTS, AND CONFERENCES	4
SECTION 4.	FACTUAL DATA	6
	4.1 INTEGRATION TECHNIQUES (PHASE I)	6
	4.1.1 History of Development	6
	4.1.2 Design of Test Assembly	7
	4.1.3 Theory	7
	4.1.4 Solder Tinning Method	8
	4.1.5 Solder Reflow Method	10
	4.1.6 Special Problems	10
	4.1.7 Test Results and Evaluation	11
	4.2 PROCESS CONTROLS (PHASE II)	11
	4.2.1 Vacuum Equipment	11
	4.2.2 Materials and Processes	12
	4.2.3 Process Evaluation	27
	4.2.4 Masking Techniques	42
	4.2.5 Instrumentation and Process Control	43
	4.3 FUNCTIONAL ASSEMBLIES (PHASE III)	44
	4.3.1 Functional Assembly Design	45
	4.3.2 Functional Assembly Fabrication	46
	4.4 TEST RESULTS AND EVALUATION	51
	4.4.1 Component Evaluation	52
	4.4.2 Functional Assembly Test and Evaluation	57
	4.4.3 Functional Assembly Test Unit	60
	4.4.4 Functional Assembly Environmental Tests	60
	4.5 MATERIALS AND PROCESSES	68
SECTION 5.	OVERALL CONCLUSIONS	81
SECTION 6.	RECOMMENDATIONS	83
SECTION 7.	IDENTIFICATION OF KEY TECHNICAL PERSONNEL	85
SECTION 8.	REFERENCES	89

## LIST OF ILLUSTRATIONS

<u>Figure No.</u>	<u>Title</u>	<u>Page</u>
4-1	Configuration of Functional Device	90
4-2	Multilayer Panel Land Arrangement	91
4-3	Schematic Diagram for Test Assembly	92
4-4	Diagram Showing Solder Joint Geometry	93
4-5	Schematic Drawing of Molten Solder Technique	94
4-6	Aluminum Substrate Holder	95
4-7	Photograph of Panel Moving Over Solder Drum	96
4-8	Evaporated Chromium Copper Lands Before and After Pretinning with the Rotating Drum	97
4-9	Close-Up View of Fixture for Attaching Functional Devices	98
4-10	Functional Device Positioning Fixture and Heat Reservoir	99
4-11	Functional Device Locating Fixture	100
4-12	Rotating Substrate Holder for Resistor Deposition	101
4-13	Powder Feed Source Arrangement	102
4-14	Effects of Process Changes on Resistor Quality	103
4-15	Tantalum Baffled Carbon Crucible Source	104
4-16	Film Thickness Distribution	105
4-17	Hollow Crucible Source with Floating Shield	106
4-18	Evaporation Rate Monitor Sensing Element	107
4-19	TRL Circuit Schematic	108
4-20	Basic TRL Circuit Layout	108
4-21	Film Panel Layout (Evaporation-Etched)	109
4-22	Logic Diagram of Integrated Counter Assembly	110
4-23	Substrate Lamination Fixture	111
4-24	Functional Assembly Unit with Frame and Connector	112
4-25	24 Hour Temperature/Humidity Cycle According to MIL-STD 202 Method 106, Test Condition A	113
4-26	Assembly Containing 772 Probes for the Four Point Probe Measurement of the 224 Resistors on a 56 Circuit Thin-Film Panel	114
4-27 A and B	Computer Printout of Resistance Characteristics for the 224 Resistors of a Functional Assembly	115-116
4-28	Distribution of Lowest and Highest Resistance Values for the 56, 1000 ohm Resistors on Each of 79 Thin-Film Circuit Panels	117

List of Illustrations (continued)

<u>Figure No.</u>	<u>Title</u>	<u>Page</u>
4-29	Distribution of Lowest and Highest Resistance Values for the 168, 4000 ohm Resistors on Each of 79 Thin-Film Circuit Panels	118
4-30	Distribution of Total Resistance Spreads for 1000 ohms and 4000 ohm Resistors on 79, 56 Circuit Panels	119
4-31	Distributions of Resistance Spreads for 56, 4000 ohm Resistor Triplets on 3 Deposited Thin Film Panels	120
4-32	Composite Resistance Characteristics for 224 Resistors on 96 Consecutively Fabricated 56 Circuit Thin Film Panels	121
4-33	56-Transistor Probe and 44 Pin Edge Connector in a Standard Test Fixture for the Operational Test of a Thin Film Panel	122
4-34	Logic of Electronic Comparator for Functional Assembly Test	123
4-35	Functional Assembly Test Unit	124
4-36	Functional Assembly Test Unit Wiring Diagram	125

## SECTION I

### PURPOSE

#### 1.0 Objectives

The objective of this contract is to develop the processes and techniques required for the fabrication of complex functional electronic assemblies employing the latest advances in multilayer thin film technology and integrated devices, such as transistors and diodes. The program is being conducted in three phases.

##### PHASE I - INTEGRATION TECHNIQUES

The investigation of practical methods of integrating functional micro-miniature semiconductor devices to vacuum deposited planar thin film networks. The method selected is to provide a means for rapidly connecting devices to film panels, and to allow the removal and replacement of these devices at high maintenance echelons.

##### PHASE II - PROCESS CONTROLS

The improvement of processes and controls for the fabrication of multilayer film circuits and interconnections.

##### PHASE III - FUNCTIONAL ASSEMBLIES

The fabrication, and demonstration of a functional multilayer thin film electronic assembly employing the techniques and processes developed in Phases I and II. The demonstration assembly is to contain approximately fifty circuits with appropriate film interconnections to perform a representative digital function, and to achieve a parts density of approximately 600,000 components per cubic foot.

#### 1.1 Related Projects

Projects within IBM which are related to this contract are:

A Film Electronics Airborne Computer (N163-10563(x) ) under contract to the U. S. Naval Avionics Facility, Indianapolis, Indiana.

Thin Film Binary Coded Decimal to Decimal Converter (N123(953)30599A) Navy Electronics Laboratory, San Diego, California

Thin Film Production Technique (N163-9142(x) ) under contract to the U. S. Naval Avionics Facility, Indianapolis, Indiana.

In addition to the above contracts, IBM maintains a large research and development program on thin films which is jointly sponsored by the Department of Defense and IBM.

Some of the work reported on in this report, although conducted under one or both of the above projects, is included in the interest of completeness.

## SECTION 2

### ABSTRACT

This report summarizes the design, history of development, and final processes used in the performance of each of the three phases of the program; Integration Techniques, Process Controls, and Functional Assemblies. Details are presented concerning the equipment used, the methods selected, the specifications established and the evaluations performed.

Descriptions of the solder tinning method and solder reflow process used to attach functional devices to multilayer thin film circuit panels is presented along with photographs and drawings describing the equipment used.

A description of the vacuum equipment used to fabricate the thin film circuit panels is presented with details concerning masking techniques, instrumentation, and process control. A detailed section on the latest process evaluation is included.

The electrical, logical and mechanical design of the functional assemblies is described as well as the fabrication steps necessary to construct these units.

Electrical, environmental, and mechanical test data is presented for both functional assemblies and solder attachment test assemblies, along with details concerning the test procedures used and the analysis of the data obtained.

A step by step outline of the materials, procedures, and process parameters used in the fabrication of the delivered film panels is included.

### SECTION 3

#### PUBLICATIONS, LECTURES, REPORTS and CONFERENCES

Technical papers and/or lectures relating to this contract were presented at the following technical conferences:

- . "Film Electronics Airborne Computer" by W. N. Carroll, presented at the Navy Laboratory Microelectronics Program Conference September 24, 1962, Washington, D. C.
- . "Materials and Processes for the Production of Film Electronic Circuitry" by W. Himes, B. F. Stout and F. L. Stutz, presented at the Navy Laboratory Microelectronics Program Conference, September 24, 1962, Washington, D. C.
- . "Production Equipment for Thin Film Circuitry Panels" by W. Himes, B. F. Stout and R. E. Thun, presented at the 9th National meeting of the American Vacuum Society, October 31, 1962 to November 3, 1962, Los Angeles, California.
- . "A Study of Evaporated Chromium Films" by K. B. Scow and R. E. Thun, presented at the 9th National meeting of the American Vacuum Society, October 31, 1962 to November 3, 1962, Los Angeles, California.
- . "Integrated Film Panels" by F. F. Jenny, presented at a faculty-sponsored Electrical Engineering Seminar held at Iowa State University, Ames, Iowa, on February 6, 1962.
- . "Circuit Design and Parameters in Thin-Film Technology" by F. F. Jenny, presented at the International Solid-State Circuits Conference, Philadelphia, Pennsylvania, February 16, 1962.
- . "Thin Film Systems" by F. F. Jenny, presented at the Meeting of the Solid State Circuitry Committee of the IRE held at the University of Washington, Seattle, Washington, August 23-24, 1962.

. "Thin Films" by A. E. Lessor, presented at the National Sales Meeting of the Consolidated Vacuum Corporation, July 11, 1962 at Rochester, New York.

. "~~Thin~~ Film Technology" by W. N. Carroll and E. S. Wajda, presented to the advanced Studies Group Rome Air Development Center, Rome, New York, July 13, 1962.

. In addition to the above technical papers and lectures, A. E. Lessor was a member of a panel discussing Microminiaturization at the 9th Annual East Coast Conference on Aerospace and Navigational Electronics held October 22-24, 1962 at Baltimore, Maryland.

] During the final period, the following Technical Meetings pertaining to this contract were held between USAELRDL and IBM personnel:

July 18, 1962	-	At Fort Monmouth
August 27, 1962	-	At Fort Monmouth
October 11, 1962	-	At Kingston
January 3, 1963	-	At Fort Monmouth

## SECTION 4

### FACTUAL DATA

#### 4.1 INTEGRATION TECHNIQUES

The objective of this phase is to develop a practical method of rapidly and reliably attaching functional devices such as transistors and diodes to evaporated multilayer circuit panels.

##### 4.1.1 History of Development

The initial work performed under this contract established the feasibility of a batch solder reflow process for attaching functional devices to evaporated thin film lands. In this method an assembly consisting of substrate, functional devices, and a positioning fixture was heated in an oven to a temperature just below the melting point of the solder. The solder was reflowed by applying a thermal pulse to the substrate from a preheated metal block placed in contact with the back surface of the multilayer film panel. This early study pointed out the desirability of precisely controlling solder thickness and the magnitude and duration of the temperature cycle.

Various methods were investigated for pretinning the lands and controlling the amount of solder for each joint.

The methods investigated were vacuum deposition of solder, melting prepositioned solder balls in an oven, and a molten solder process. Of these three methods the molten solder process was found to be the most practical. Pretinning of excellent quality could be accomplished rapidly and inexpensively with simple equipment.

The methods investigated for reflowing the solder to form a solder joint between the thin film lands and the functional devices were spot soldering, heated gas jet soldering, and hot plate soldering. A batch process using the hot plate technique was chosen because satisfactory assembly was rapid and simple. Jigs and fixtures for the hot plate soldering process were considerably simpler to fabricate than for the other methods, and adequate control of the time-temperature cycle could easily be maintained.

#### 4. 1. 2 Design of Test Assembly

A test subassembly utilizing multilayer vacuum deposited circuitry on a 2.5 inch by 3.5 inch substrate was designed to evaluate the planar integration technique. The interconnection pattern was chosen for the specific purpose of electrically testing the solder joints. The land area, spacing, panel size and materials are identical to the functional assemblies fabricated for this contract (see Section 4. 2).

The functional device to be attached is shown in Figure 4-1. The configuration of the ribbon leads permits precise alignment with the circuit land pattern at the point of attachment. In the case of functional device failure, removal is accomplished by clipping the leads near the case. A replacement can be soldered to the leads originally attached to the lands. The lead shape also allows an organic protective coating, applied at a later fabrication step, to completely cover the surface of the film panel; transistor replacement without rupturing or puncturing the protective coating is also possible.

The multilayer panel land arrangement is shown in Figure 4-2. The 2.5 inch by 3.5 inch by .040 inch borosilicate glass substrate contains 168 lands for attaching 56-2N744 type planar transistors. For the test subassembly the multilayer connection shown schematically in Figure 4-3 is used to measure and evaluate solder joints.

To provide for evaluation of the overall integration technique, dummy transistor units have been used. These dummy units include both completed micromesa units with defective transistors mounted within, and gold plated Kovar stampings with a lead geometry identical to the dummy units. The Kovar stampings were used for electrical evaluation while the defective units were used for mechanical shock and vibration tests.

#### 4. 1. 3 Theory

Soldering was chosen to attach the functional devices because its temperature requirements are compatible with multilayer film panels and the mechanical stress on the substrate is not excessive.

It can be easily adapted to make several connections at once, thus permitting the use of a batch process. Visual inspection is generally adequate to determine the joint quality.

The joint geometry is shown in Figure 4-4. The transistor lead material is gold plated Kovar, .025 inches wide and .003 inches thick. The joint material is a solder of 60% tin and 40% lead. The land material is an evaporated copper film 10,000 Å thick with an adhesion-increasing undercoat of chromium about 200 Å thick. Underneath the chromium is 15,000 Å undercoat of silicon monoxide deposited on the borosilicate glass substrate.

This geometry allows the joint to be made easily by bringing the two surfaces together and heating. It allows disassembly before covering with the organic protective coating by applying heat from the top of the joint with a small soldering iron and lifting the ribbon with tweezers. Batch transistor salvage can be accomplished by heating the entire panel and lifting off the transistors.

The forces applied to the solder joint under various mechanical stresses are difficult to compute because the step geometry does not allow easy resolution of forces applied to the transistor body. It is estimated that the .030 inch by .025 inch lead requires a tensile force of 5.7 pounds or a shear force of 4.0 pounds to separate it from the land. These figures are based on the assumption that the solder material is the weakest part of the system. The shear strength for this solder is 5400 psi and the tensile strength is 7600 psi.

Additional strength is provided by the organic protective coating. Under the stress of shock and vibration, the organic coating will supply a damping force to suppress the effects of resonance.

The solder (60% tin, 40% lead) has a fusion temperature of 190°C. This temperature is low enough to tin and reflow the joints without damaging the multilayer film circuitry. It is high enough to allow reliable operation of the assembly at temperatures in excess of 100°C.

#### 4. 1. 4

#### Solder Tinning Method

The formation of the copper-solder interface and the application of a definite amount of solder to the land area (pretinning) is accomplished by the molten solder technique shown schematically in Figure 4-5. The integrated circuit panel with clean lands is coated with flux and passed at a speed of .32 inches per second

over an iron drum immersed in molten solder and rotating at a speed of 22 rev. per minute. The weight of the aluminum holder shown in Figure 4-6 (approximately 11 ounces) holds the panel in intimate contact with the solder on the surface of the drum and heat is applied by the molten solder which is held at a temperature of 210°C. A small amount of solder adheres to each land area on the panel as it is passed over the rotating drum.

To insure uniform wetting of all copper lands, a flux is required. The purpose of the flux is to provide a tarnish-free surface to influence the surface tension at the solder-copper interface so that the solder will spread to provide a good heat transfer medium and to protect the solder surface during cooling.

Since the vacuum deposition process generally leaves clean tarnish-free copper lands, a mild fluxing material is adequate. Triethanolamine has been found satisfactory for this application.

Figure 4-7 is a photograph of a panel moving over the rotating drum. In this process, the temperature of the solder, the speed of the panel, the size of the land area, and the thermal characteristics of the substrate determine the amount of solder held by the land. Briefly, the influence of these variables on the result of the tinning process is as follows. Increasing solder temperature and increasing panel speed permit satisfactory copper-solder bond formation, but enhance the risk of substrate breakage because of the greater temperature gradient. Lowering of the panel speed while maintaining the solder temperature at 210°C dissolves the entire copper land leaving only a thin film of chromium. Increasing the speed excessively while maintaining constant temperature does not allow the land to reach a temperature high enough for uniform tinning. The thermal conductivity of the substrate determines the relative amount of time required for the land to reach its tinning temperature, provided all other variables are held constant.

For the size of lands used on the multilayer film panels fabricated for this contract, the parameters described are entirely satisfactory. Sufficient solder, 0.002 to 0.003 inches, remains on the copper lands to form the solder joint and the copper-solder interfaces appear to be excellent (Figure 4-8).

#### 4. 1. 5

#### Solder Reflow Method

The attachment of functional devices is shown in Figure 4-9. The devices with preformed leads are loaded into a jig which properly positions each lead to coincide with a tinned land on the multilayer film panel. The panel and the tinned lands are coated with a thin layer of flux and clamped in registration with the leads in the locating jig (Figure 4-10). The entire unit (functional devices, jig, and multilayer panel) is placed on a stainless steel heat reservoir preheated to a temperature of 230°C until the solder is molten. A force of 40 pounds is applied to the back of the jig to insure close contact of the leads with the pretinned lands. This force, which is required to overcome the surface tension of the molten solder, is applied from the back of the jig to the silicon rubber pad, through the small pins to the back of the lead. A spring arrangement allows the multilayer panel to be gently held in place prior to the application of the 40 pound force. After the force is applied the springs allow the pressure to be distributed through the 168 steel pins to the transistor leads.

The locating fixture is made of Invar to closely match the linear expansion of the borosilicate glass substrate. The aligning grooves shown in Figure 4-11 are machined to allow .005 inches clearance between the edge of the ribbon leads and the wall of the groove to prevent binding. The plate was electropolished to further aid the free movement of the leads.

Approximately 1 minute of heating is sufficient to wet the transistor leads with solder. After cooling, the finished panel is gently lifted off the locating plate.

After removal, the remaining flux is flushed from the panel with methanol and by gentle abrasion with a small brush or a rubber policeman. The panel is dried after a methanol rinse by a short bake in a forced convection oven maintained at 40°C.

A detailed step-by-step description of the attachment process is included in Section 4.5.

#### 4. 1. 6

#### Special Problems

During the final phase of development, process changes have been made in the soldering method to increase the yield. Failure to achieve 100% yield of good solder joints has been caused by binding of the Kovar ribbon transistor leads in the aligning

groove. This has been corrected by more careful lead alignment during the locating jig loading operation.

After extended use of the locating jig, a tendency for the solder to wet the Invar jig surface was found. This condition was corrected by applying a thin coat of n-dodecyl alcohol to the front surface of the ground metal plate jig. The excess is removed by wiping. The alcohol prevents the solder from forming a bond to the Invar.

A few panels broke during the tinning or solder reflow operations. All failures of borosilicate glass panels were due to imperfections in the glass (chips, bubbles, cracks, etc.) which seem to nucleate a crack when the panel is subjected to a temperature gradient. More careful selection of substrates was required to prevent this failure.

Several hundred functional devices have been salvaged from defective panels and have been re-assembled to new panels. Of the salvaged units, failure due to broken leads is less than 5%. Some functional devices have been re-used three times.

#### 4. 1. 7 Test Results and Evaluation

Test results and evaluation of the test assemblies are contained in section 4. 4 of this report.

### 4. 2 PROCESS CONTROLS (PHASE II)

The work conducted under this phase of the contract has been directed toward the improvement and refinement of vacuum deposition techniques. In keeping with this objective, IBM has continued to develop more advanced and efficient methods of fabricating thin films. Improvements have been made in both the materials and the equipment used, which has resulted in more uniform reproducible film components.

#### 4. 2. 1 Vacuum Equipment

The vacuum units used on this project are modified conventional vacuum coaters upgraded to improve pumping speed, pressure and process control. Two general types are used. The first type has a 19 inch diameter, 30 inch high bell jar chamber, pumped with a 6 inch oil diffusion pump. The second type has a 36 inch diameter horizontal tank. One 36 inch chamber is pumped with a 10 inch oil diffusion pump, and the other

with a 16 inch oil diffusion pump. All systems are equipped with liquid nitrogen cold traps to reduce the back-streaming of the pump oil. These systems are capable of maintaining a vacuum pressure in the low  $10^{-6}$  torr range during the deposition cycles.

Two basic fabrication methods are available in the vacuum deposition of thin film circuits. The first is the batch mode of operation where each deposition is made on one or more substrates in a single pumping cycle, and the second is the closed cycle mode where all evaporations are completed within one pumping cycle. The latter mode of operation requires a mechanism for changing masks and/or substrates in the vacuum chamber as well as several evaporation sources.

Although some consideration had been initially given to the use of a changer mechanism, it became evident, as the fabrication techniques had been further developed, that the batch method was more adaptable to process development. The development of the pattern etching technique, while significantly reducing the number of masks required for circuit fabrication, added a non-vacuum step. In addition, other steps in the process are done outside the vacuum chamber, such as resistor annealing and in process testing. These steps are so distributed throughout the deposition sequence that the effective use of a mask changer is limited.

Other important advantages such as minimizing the cross contamination of evaporant materials and simplifying vacuum chamber tooling were also realized by the batch method. Vacuum fixtures allowing four substrates to be processed simultaneously offset the yield advantage of a changer mechanism. When depositing resistors, however, only two substrates were processed in a single pumping cycle. A rotating substrate holder shown in Figure 4-12 allowed two resistor depositions to be performed while providing the necessary control to obtain maximum uniformity of resistor values.

#### 4. 2. 2 Materials and Processes

A minimum number of materials and components have been used as evaporants and for packaging. Criteria for their selection have been, among others, cost and availability, corrosion resistance and mutual compatibility.

### Substrates

The substrate material selected was Corning 7740 Pyrex glass, 2.5 x 3.5 x .040 inches. The substrates must be free of defects such as pit marks, cracks and surface crazing. Bubbles or voids formed during manufacturing must be kept to a minimum and in no case exceed 0.5 mm in diameter with a maximum incidence of 2 per square inch of substrate area. Surface requirements are that irregularities such as scratches shall not exceed 300 Å in depth, and that the overall flatness of the substrate must be within 0.0015 inches across the diagonal of the substrate rectangle.

The substrate is required to withstand 450°C process temperatures without distortion, and thermal shock properties must be such that the substrate will not crack when subjected to a 200°C gradient across the 0.040 inch thickness dimension.

Applicable MIL standard specifications for shock and vibration are covered under the "Functional Assembly Environmental Performance" section (4.3.4) of this report.

Other substrate materials evaluated included glazed and unglazed ceramics, glass-ceramic composites and porcelainized and glass coated metals. Only the glass, glazed ceramics and the glass ceramics met the surface requirements. The flatness requirement eliminated all but ground and polished glass substrates. Machine drawn glass was smooth enough, but did not meet the flatness specification.

In the early stages of the program, 0.020 inch thick substrates were specified in order to achieve maximum component density. Corning Glass "Vycor" was chosen to meet the thermal shock requirements. However, two problems were encountered: fragility and procurement. The 20 mil substrates in the 2.5 x 3.5 inch size presented handling difficulties and a high breakage rate was experienced during both the deposition processes as well as the packaging and lamination procedure. Only six of over 30 vendors contacted would quote on substrates of this thickness. Of these six vendors, only three could meet the quality specifications. Even these vendors had a 50% rejection rate upon inspection of delivered substrates.

The fragility problem was overcome by selecting 40 mil Pyrex substrates and component density goals were met by modifying the first level package design (section 4. 3. 2). The choice of thicker substrates coupled with modifications of the original surface quality specifications eased the procurement problem. The specifications listed above were found to be adequate after evaluating the influence of surface roughness, flatness and undercoating on resistor tolerances.

Due to its low surface mobility, silicon monoxide forms an ideal undercoating for the circuit network by effectively smoothing out minor surface irregularities.

To evaluate the ability of the undercoat to effectively cover scratches, the areas under the thin resistor depositions were scored with a ruling engine to depths varying up to 300 Å. Substrate scratches 300 Å and deeper are readily discernible by eye, using an edge lighting inspection technique.

The scratched samples were coated with the regular 15,000 Å silicon monoxide undercoat followed by the functional circuit resistor deposition. The thin ( $\sim 250$  Å) resistor film is most sensitive to surface imperfections, and provides an effective method of evaluation. There was no detrimental effect on the resistor spread and these samples were completed as acceptable functional circuits.

A significant number of substrates ( $\approx 15$ ), flat within 0.0015 inches, were sampled to determine the effect of their curvature on shadowing (the dispersion of the deposited film beyond the mask openings). It was found that this flatness tolerance could be used if the resistor and land masks were in contact with the substrate, and if the insulator and conductor jumper masks were spaced .004 inches off the substrate surface.

This work resulted in a revision of the substrate specifications. Acceptable substrates are to be free of scratches deeper than 300 Å and flat within 0.001 inches over 3 linear inches; vendors have had no difficulty in meeting this flatness. The acceptance rate from the vendors rose to over 90% and the inspection time was radically reduced.

#### Film Resistors

Resistor requirements for film electronic applications have made necessary the development of processes for the production of reliable thin film resistors of high quality. Design

specifications to be met by the resistor process for this contract were as follows: resistivity of 250 ohms/square, reproducibility of  $\pm 7\%$  over the circuit panel, low temperature coefficient of resistance and long term stability in the temperature range -55 to 165°C.

Initial work on resistor fabrication was carried out using nickel-chromium as the resistor material. The evaporant material was in wire form, having a 75% nickel-25% chromium composition and was flash evaporated from a tungsten filament. Spectrographic analysis of the resulting deposit showed the composition to be 65% nickel-35% chromium. The use of nickel-chromium, which is a fairly good conductive material resulted in films of less than 200 Å in thickness at the desired resistivity value. To assure film uniformity, a nucleating film of titanium, a few angstrom units in thickness, was deposited. The deposition rate and thickness of this film were monitored by a crystal oscillator counter<sup>(1)</sup>.

After the nickel-chromium was deposited, the resistors were heat treated prior to removal from the vacuum chamber. An additional stabilizing heat treating cycle in a controlled oxidizing atmosphere was performed after the deposition of gold land areas.

Although all evaporation and process parameters were closely controlled, it was not possible to reproducibly deposit nickel-chromium resistors, with tolerances of  $\pm 7\%$ , at a substrate yield of higher than 10%. Nickel-chromium resistors, when subjected to temperature-humidity cycling (MIL STD 202, Method 106A), catastrophically failed after 18 cycles. Because of this lack of uniformity, reproducibility and stability under stress, nickel-chromium was abandoned as a resistor material in favor of the superior chromium-silicon monoxide cermet.

The cermet resistor material, consisting of approximately 70 atomic percent chromium and 30 atomic percent silicon monoxide, is deposited by flash evaporation through a suitable mask onto the glass substrate which has been coated with a silicon monoxide underlay. During the evaporation, the temperature of the substrate is maintained at 200°C. The deposition is terminated when a resistivity value of about 1.2 to 1.5 times the desired resistivity value is reached. This monitor-stop value is chosen so that the deposited films may be annealed to the final desired resistivity and remain stable after anneal. Since the resistor film cannot be monitored directly during deposition, a monitor slide is placed adjacent

to the substrate holder, and the resistance of the film deposited on this slide is continuously monitored with a digital ohmmeter. The monitor slide is equipped with pre-formed lands and is held in place behind the monitor mask. Contacts to the lands are made by bonding gold wires directly to them. These wires are then attached to suitable connection leads from the digital ohmmeter. After cooling to 80°C, the substrate is transferred to other vacuum chambers for land and silicon monoxide overcoat depositions. The resistors are then annealed in 10% hydrogen to 90% argon gas at a temperature of 425°C until the desired resistance value is reached. The final resistance value is determined by the anneal process, thus permitting considerable variation of the initial value obtained in the vacuum chamber. In practice, it has been found that a stop-value of 1.2 to 1.5 times the final desired resistivity will allow annealing to the desired value in 2 to 5 hours. Small variations in substrate temperatures during deposition steps cause variations in the annealing times. However, these variations are small enough to be neglected.

The flash evaporation source for the cermet material consists of a worm-drive powder feed, a tantalum chute, and a heated tantalum filament (Figure 4-13). The material from the powder feed is directed onto the filament by the chute and is immediately vaporized. The thickness distribution over the 2.5 x 3.5 inch substrate area is within 2% at an 50 cm source to substrate distance.

The reproducibility and spread of resistance values are influenced by the particle size of the chromium-silicon monoxide powder. The particle size range for both materials, which gives good results, is between 325 mesh and 400 mesh. The presence of larger material tends to cause uneven feeding while smaller material causes excessive spattering of the cermet powder mixture.

During the early stages of the cermet resistor fabrication program it was difficult to reproduce resistor values. As the various process parameters were brought under closer control, the average monthly yield rose from 30% to greater than 90%. Figure 4-14 shows the average yield and deviation spread as related to process improvements.

The most significant process changes have been those that have minimized any pre-oxidation of the film resistor prior to the annealing operation. Experience has shown that when resistors were removed from the vacuum chamber at temperatures  $> 80^{\circ}\text{C}$ , the annealing process was retarded. Similarly, when the subsequent silicon monoxide overcoat was deposited at temperatures  $> 200^{\circ}\text{C}$ , the annealing process was erratic. Both of these conditions may be attributed to a partial oxidation of the deposited resistor. The first condition was easily alleviated by using Helium gas to bring the vacuum chambers to atmospheric pressure.

To prevent oxidation of the unannealed resistor during terminal lead and protective overlayer depositions the vacuum chambers were flushed with helium before evaporations were made. In addition, at any process step where the unannealed resistors are brought from vacuum to atmospheric pressure, helium is used to flush the tanks.

The present resistor process has been evaluated in the fabrication of 92 resistor panels, and the yield has been 82.3%.

Significant improvements in the temperature coefficient of resistance (TCR) have been concurrent with the process improvements shown in Figure 4-14. A reproducible TCR is essential for accurate control of the annealing process. Low TCR values are desirable for greater circuit stability during operating temperature changes. TCR data representative for the process prior to the installation of an annealing gas dryer are shown in Table 4-1; the average TCR was 79.6 ppm. The maximum figures of 190 and 194 ppm shown in this table were due to an extended annealing period which tended to increase the TCR and caused a general deterioration of the panels. The final fabrication process has eliminated the necessity of long annealing periods.

TABLE 4-1  
TCR Data for Unimproved Resistor Process

Panel #	$R_c$	$R_t$	$\Delta R$	$\Delta t$	TCR x $10^{+6}$
<u>RT 16</u>	(n)	(n)	(n)	(°C)	(degree <sup>-1</sup> )
45	3939	3907	32	390	21
49	4020	3920	100	360	69
52	4095	3907	188	375	122
55	4027	3902	125	330	94
57	5012	4652	360	380*	190
59	4275	3953	322	390*	194
<u>RT 18</u>					
01	4004	3780	220	410	134
02	3864	3847	17	395	11
03	4366	4207	159	440	83
05	4025	3850	175	425	102
07	3928	3910	18	400	11.5
11	3904	3853	51	380	34
15	4146	3937	209	412	123
19	3900	3892	8	410	5
20	4029	3950	79	340	57.5
21	4089	4057	32	360	22

\*Anneal longer than 48 hours.

The resistance of a conductor at a temperature  $t^{\circ}\text{C}$  is calculated from  $R_t = R_c [1 + \alpha (\Delta t)]$  where  $R_t$  is the resistance at the maximum anneal temperature,  $R_c$  is the resistance at the reference to temperature, and  $\alpha$  is the temperature coefficient of resistance (TCR).

The dry atmosphere obtained when using a Deoxo Puridryer\* in the resistor annealing process reduced the average TCR to 32.8 ppm as shown in Table 4-2.

TABLE 4-2  
TCR Data for Improved Resistor Process

Panel #	R <sub>c</sub>	R <sub>t</sub>	Δ R	Δ t	TCR x 10 <sup>+6</sup>
<u>RT 16</u>	(n)	(n)	(n)	(°C)	(degree <sup>-1</sup> )
78	3974	3907	85	360	59
79	3945	3909	34	345	25
<u>RT 18</u>					
41	3911	3904	7	360	5
42	4036	3953	83	394	52
43	3861	3852	9	374	6.2
44	3958	3917	41	394	26
45	3989	3916	73	375	49
47	3930	3867	63	370	43
48	3930	3911	19	390	12.5
49	3796	3770	26	420	16.3
51	4027	3919	108	400	67

Table 4-3 shows the further reduction of the average TCR to 22.9 ppm and is representative of the high degree of annealing control afforded by the final resistor fabrication process which incorporates helium flushing.

\*Trademark of Engelhardt Industries, Incorporated.

TABLE 4-3  
TCR Data, Final Resistor Process

Panel #	R <sub>c</sub>	R <sub>t</sub>	R	t	TCR x 10 <sup>+6</sup>
<u>RT 27</u>	( $\Omega$ )	( $\Omega$ )	( $\Omega$ )	(°C)	(degree <sup>-1</sup> )
06	4014	3963	51	375	34
08	3994	3928	66	395	42
10	3970	3930	40	385	26
13	3957	3936	21	370	15
16	3999	3946	53	386	34
21	3965	4010	45	385	30
28	3963	3999	36	400	23
30	3951	3975	24	395	15.5
35	3962	4030	68	385	44.5
37	3965	3992	27	380	18
43	3942	3955	13	375	8.8
57	3966	3992	26	350	19
59	3950	3962	12	355	8.6
67	3912	3929	17	375	12
70	3950	3983	33	381	22
79	3952	3977	25	390	16
86	3963	4000	37	395	24
95	3926	3973	47	393	30
98	3960	3995	35	390	23
101	3927	3941	14	375	9.5
108	3977	4032	55	395	35
110	3955	3975	20	420	12
112	3960	3999	39	400	24

## Film Conductors

Electrical connections between passive components and circuits are made with copper. Copper provides good electrical conductivity, lends itself well to conventional chemical etching techniques, and allows low resistance film-film contacts to be made.

Copper films are deposited from thoroughly outgassed, radiantly-heated crucible sources (Figure 4-15). Considerable work was done earlier with intermittent and continuous wire-feed copper sources. However, with this type source, the evaporant outgasses and evaporates simultaneously, thus depositing onto the substrate particles ejected from the source. The copper films so deposited were difficult to insulate. Optimizing the wire feed rates and filament temperature reduced but did not eliminate these difficulties. The replacement of the wire-feed source with a crucible source produced smoother films and allowed the use of an ionization gauge rate monitor<sup>(2)</sup> to control the evaporation rate. Recrystallized alumina crucibles were evaluated in the initial stages of the program. Their lifetime was limited to a few depositions. The rapid expansion of the solidified copper evaporant, upon reheating, fractured the crucible. Minimizing the residual melt by evaporating nearly to completion did not appreciably extend the crucible life. However, the gassy nature of the porous carbon also caused erratic ejection of copper particles. These difficulties were finally eliminated by the use of molybdenum crucibles. Several of these molybdenum crucibles have been extensively used and show no signs of deterioration.

The ability to deposit repeatedly good insulating SiO films is highly dependent on the surface smoothness of the underlying conductive film. Copper films with rough surfaces are difficult to insulate. Highly oriented copper films of good surface smoothness can be obtained by maintaining the substrate temperature below 170°C at the onset of the deposition<sup>(3)</sup>. Good adhesion is achieved by depositing an underlayer of chromium a few hundred angstroms thick. These techniques coupled with the stress relief which occurs during subsequent insulator depositions at 350°C, assure a smooth, adherent conductive film.

An early process improvement was the introduction of chemical etching techniques as a method of forming part of the interconnection pattern. The electro-etching and ultrasonic cleaning steps required as a result of this process change have not adversely affected the copper films.

Initially, the sequence of procedures was as follows: After the film resistors were annealed and tested, the entire substrate was covered with a chromium underflash and with a copper film. The chromium underlayer in this case must be a distinct and separate layer since any alloy formed between chromium and copper is not readily etched away. The usual printed circuit etching procedures were applied (Ref. Section 4.5). After applying a photo-resist in the desired conductor pattern configuration, the excess copper was first etched in a ferric chloride solution and then the chromium "adhesion layer" was etched in an aluminum chloride-zinc chloride etch bath, using a piece of zinc to depassivate the chromium layer. Finally, the resist was stripped off and the panel cleaned and made ready for further processing. The etched lines, however, proved difficult to insulate.

Difficulties in insulating etched patterns arise from the sharp rectangular cross-section of the photo-etched lines, and from surface projections of sub-micron dimensions resulting from particle impingement on the evaporated copper surfaces. Under electrical stress, the fields concentrated at such sharp edges and at surface projections can exceed the breakdown strength of the dielectric.

It was found that subjecting the etched copper lines to an electrolytic micro-etch removed both sharp edges and surface projections, and the occurrence of insulation failures was reduced by an order of magnitude. According to these results, a modified etching sequence has been established. After etching the copper conductor pattern in the normal way, the resist was stripped off while the chromium "adhesion plane" was still intact. Contact was made to the edges of the panel, and using the chromium plane to distribute current to all isolated copper lines on the panel, the copper lines were electro-etched. The electrolyte may be a solution of ortho-phosphoric acid with certain viscosity-increasing additives such as sodium lauryl sulphate or sodium carboxymethylcellulose. For the sake of convenience, a proprietary copper-cleaning bath Metex L-5\* is now used as the polishing electrolyte.

Optimum electro-etching procedure required determining the following parameters for best result:

1. Thickness of chromium "current distribution" plane.
2. Electro-etching current density and time.
3. Final thickness of electro-etched conductor lines.
4. Removal of oxide formed on electro-etched conductor lines.

\*Trade mark of MacDermid, Incorporated.

1. Thickness of chromium "current distribution" plane.

The thickness of the chromium plane must be held within certain fairly critical limits for satisfactory electro-etching results. Chromium thicknesses of less than 200 Å were found to be too thin for adequate current carrying capacity to insure complete electro-etching of all isolated copper lines. Films thinner than 200 Å are also difficult or impossible to remove after electro-etching, because local discontinuities in the chromium film occur.

Chromium film thicknesses greater than 400 Å are undesirable because undercutting of the copper conductor lines may occur when the chromium plane is etched. This difficulty is aggravated if the chromium film has been strongly passivated by the electro-etch and requires a chemical etch time longer than usual.

Best results are obtained if the chromium thickness is held between 200 and 400 Å. This range permits complete and uniform electro-etching of all isolated copper lines, as well as easy and complete removal of the chromium plane in the subsequent chromium etch, without undercutting. Chromium thicknesses from 150 to 600 Å can be tolerated if necessary, with the possibility of some reduction in yield.

2. Electro-etching current density.

A current of 2.0 amperes D-C in 100% Metex for 8 seconds with an electrode spacing of 2 inches has been empirically established as the optimum for the functional circuit panels. In order to determine the current density and to be able to convert the process data for other circuit layouts, the functional circuit pattern was etched on 1/32" 1-oz. copper clad epoxy paper laminate cut to 2 1/2 x 3 1/2 inch size. The clean, dry cards were weighed before KPR coating, after etching the circuitry and stripping the KPR, and after etching off the circuitry. From the weight losses, the area of copper to be electro-etched could be calculated. The area of electro-etched circuitry was determined by this method to be 12.18 cm<sup>2</sup> for the functional panel, which indicates a current density of 0.165 A/cm<sup>2</sup>.

3. Final thickness of electro-etched conductor lines.

Some copper is removed during the electro-etch process. Measurement of copper conductor line thicknesses before electro-etching is not possible by the Tolansky method because

of the very steep line profile characteristic of etched lines. The copper line thicknesses before and after electro-etching have been measured with a Taylor-Hobson "TALYSURF" surface gauge. Results show that approximately 2500 Å of copper are removed during the electro-etch under the standard condition previously established. These results correlate well with results obtained from resistance measurements made on copper lines before and after electro-etch. The resistance of 10 mil wide copper lines 10,000 Å thick is approximately 2.8 Ω/in. and increases to approximately 3.6 Ω/in. after electro-etching. The thickness of copper removed will be constant for a given time and current density; therefore, the deposition thickness of the copper etch plane should be increased from 10,000 Å to 12,500 Å to give a copper line thickness of 10,000 Å after electro-etching.

#### 4. Removal of oxide formed on electro-etched conductor lines.

There is a strong tendency for etched copper surfaces to oxidize during the cleaning and drying procedure following the etching. This tendency is increased when the copper lines have been electro-etched. Chemical means of removing this oxide have been unsatisfactory because of the difficulty of drying the films without oxidation. The presence of an oxide layer can be detrimental in later stages of fabrication when film-to-film connections are made, due to the electrical resistance of the copper oxide and poor adherence of other films to copper oxide.

Copper oxide can be removed by annealing the clean, dry panel in argon-10% hydrogen forming gas for 15 minutes at 300°C. The effect of this procedure on resistor values has been investigated and found to cause less than 1/2 percent change, which can be tolerated.

#### Film Insulation

Silicon monoxide is vacuum deposited from sources of two different designs, the "Drumheller" hollow crucible source<sup>(4)</sup> and a baffled crucible type. Substrate temperature for silicon monoxide deposition is 350°C. This temperature produces an adherent, abrasion-resistant film. SiO is used to provide a reproducible undercoating for resistor deposition, a protective overcoat for both resistors and circuit lines, an insulator between conductor crossover points and the dielectric between capacitor plates. The ionization gauge rate monitor<sup>(2, 5)</sup> controls the deposition rate within 5%.

According to Holland<sup>(6)</sup> evaporation from a small area source is governed by Knudsen's cosine law<sup>(7, 8)</sup> the thickness distribution will be given by

$$\frac{t}{t_0} = \frac{1}{\left[ 1 + \left( \frac{\delta}{h} \right)^2 \right]^2}$$

where

$t$  = thickness of deposit at a distance  $\delta$  off the substrate center

$t_0$  = thickness just above the source center

$h$  = source to substrate distance

Figure 4-16 shows the measured distribution from a hollow crucible source and, for comparison, the theoretical distribution calculated from the above equation. The deviation of the experimental curve from the predicted behavior may be considered as improved performance and is due to the deviation of the actual source from an ideal point source.

On a 2.5 x 3.5 inch<sup>2</sup> substrate, thickness variations have been found to be within 2% for source to substrate distances of 30 cm. Practical film thicknesses range from 10,000 to 30,000 Å. The 30,000 Å film used for insulation must have a minimum non-fluctuating resistance of 1 x 10<sup>7</sup> ohms at 15 v dc for long term stability.

One of the limitations of the original design of the hollow crucible source was the occurrence of filament fracture when recharging the source with fresh evaporant. The residue of encrusted silicon monoxide, which forms in the top portion of the source had to be loosened with a probe before reloading. The tantalum filament, recrystallizing under the effect of high temperatures, tends to be brittle after several evaporations and is easily broken. A simple modification to the source design, as shown in Figure 4-17 eliminated this mechanical breakage. By inserting a piece of 3 mil thick coiled tantalum sheet inside the source between the evaporant and the first heat shield, the filament and the coiled floating shield can be removed as a unit. The floating shield can then be uncoiled, and the encrusted silicon monoxide residue breaks away easily, leaving the filament undamaged. Comparative tests have also indicated that the additional heat baffle allows closer control of the source temperature, resulting in more reproducible film thickness.

The ejection of fine particles is a basic problem with all sources for powder type evaporants where powder cannot be melted down and thoroughly outgassed prior to the film deposition. Although the hollow crucible design alleviates this problem, there still was evidence of fine particle impingement on the substrate. This condition was brought under control by grading the solid evaporant material in the range between 20 and 3.5 mesh before charging the crucible. This also allowed a deposition rate increase from 20 to 30 Å/sec.

The resulting silicon monoxide films have been smooth and nearly free of ejected particles. Although the insulating film is still deposited in two independent steps, (see Table 4-12, page 48, steps 9 and 10) microscopic inspection between steps has revealed no visible structural faults.

Extensive experience in the deposition of silicon monoxide has provided no conclusive evidence of the existence of pin holes or actual voids in the film. Considerable evidence (Section 4.2.3), however, exists to show the insulation breakdown can be attributed to dust, contamination, particle impingement and conductor plane projections.

The latter two difficulties have been brought under a high degree of control. Dust, however, is an inherent problem of the batch mode of operation, some improvement is possible by depositing the insulation film in two separate evaporations. This allows microscopic inspection of the first layer and removal of contaminants, if necessary.

The use of silicon monoxide as an underlayer for the circuit network not only covers minor surface imperfections but also acts as a barrier against contamination by out-diffusion from the substrate. It has also been used with good results as a protective coat over the interconnecting circuit pattern as well as the resistors.

The evaporation rate and vacuum pressure are extremely critical parameters affecting the structural density of the deposit. Although slower evaporation rates at higher vacuum pressures tend to produce silicon oxide films possessing greater dielectric strength<sup>(8)</sup>, they are also less dense because of their higher oxygen content, and thus are more pervious to water vapor. It was found that silicon monoxide films deposited at vacua below  $2 \times 10^{-6}$ /torr were more resistant to water vapor penetration while still meeting the circuit insulation and dielectric requirements.

#### 4. 2. 3 Process Evaluation

The fabrication methods and conditions presently used and described in the preceding sections are the result of a thorough process investigation which was initiated to reduce the rate of crossover insulation failures. This investigation has shown that insulation failures can be reduced by at least one order of magnitude if the processing scheme used in the early stage of the contract was altered in two respects. One change was the incorporation of electro-etching to round the profile of the conductor line pattern under the silicon monoxide insulator film. The other change refers to the deposition conditions of silicon monoxide insulator films; it was found that film condensation at 350°C instead of 300°C substrate temperature, and in vacua below  $10^{-6}$  torr increased the insulation stability of crossovers. Because of the significant improvement achieved in respect to the final yield, the following summary of the investigation and findings is included in this report.

##### Crossover test panel fabrication

To study the influence of individual process steps and parameters on insulation properties, 60 test panels were fabricated under systematically varied conditions. Standard size 2 1/2 x 3 1/2 inch Pyrex glass substrates were used to deposit a simple pattern consisting of 30 crossovers per panel. The crossover lines were .020 in. wide. In each experiment, a batch of four substrates was processed to duplicate the arrangement during actual circuit panel fabrication and to exclude accidental results.

The sequence of evaporations, (although limited to the steps necessary for crossovers), and the deposition conditions were identical to the procedures used in the fabrication of functional circuit panels. The standard fabrication procedure involved the following steps

- a) Deposition of a silicon monoxide undercoat at 300°C substrate temperature in vacua between  $2$  and  $6 \times 10^{-6}$  torr. Film thicknesses varied from run to run between 4000 and 19,000 Å.
- b) Deposition of 300 to 500 Å of chromium plus 10,000 Å of copper at 165°C substrate temperature in vacua below  $1 \times 10^{-5}$  torr. Both films were sequentially deposited in one pump-down. Evaporation rates were not controlled but set by adjusting the power input of the sources to empirically established values. The chromium film thickness was not measured after initial calibrations. Copper film thicknesses in all experiments ranged from 5,000 to 22,000 Å. The Cr-Cu film covered the entire substrate surface.

- c) The lower conductor lines were produced by the pattern etching technique. After etching and KPR removal, the surfaces were thoroughly cleaned and dried. The final surfaces of the copper lines were always oxidized to varying degrees, but even heavy oxide films did not have a deteriorating effect on the crossover insulation.
- d) Two layers of silicon monoxide of 15,000 Å each, evaporated in two separate pump-downs through masks were deposited at 300°C substrate temperature in vacua of  $2 \text{ to } 7 \times 10^{-6}$  torr. These vacua were obtained by repeated silicon monoxide gettering evaporations prior to deposition. The total silicon monoxide film thickness varied from run to run between 25,000 and 41,000 Å.
- e) Deposition of the upper conductor lines through masks under conditions very similar to those listed for step (b). The only difference was the evaporation of copper, which started while the chromium source was still evaporating, thus forming an intermixed Cr-Cu alloy film at the interface to enhance adhesion. Two of these evaporations were made at pressures as high as  $8 \times 10^{-5}$  torr without producing any detrimental effects. Film thicknesses, since not rate-controlled, varied from run to run between 5000 and 38,000 Å.

A matrix experiment was run in order to study the effect of those factors considered responsible for insulation failures. In each experiment, only one process step was changed so that the effect of this deviation from standard practice could be identified unambiguously.

The first series of experiments was aimed at improving step (b) of the standard procedure, the fabrication of the lower conductor lines. Instead of fabricating the conductor lines by KPR processing and etching, an identical pattern was directly deposited through masks. This method would eliminate failures due to left-over KPR, moisture or chemicals absorbed during the etching.

Another variation was tried on etched conductor lines with the objective of rounding the line edges and reducing the surface roughness. This was accomplished by electro-etching as outlined in section 4.2.2

One experiment was made to investigate possible damage of the crossover insulation due to the deposition of chromium in the final step (e). To evaporate chromium, source temperatures of 1600 to 1800°C are required. Therefore, the chromium vapors striking the silicon monoxide insulator surface have a high kinetic energy, and chromium atoms may penetrate the film. If there are regions where the insulation is unusually

thin, the penetration depth could be sufficient to form localized shorts or, after applying an external voltage, to establish an electric field high enough to cause breakdown. In order to test this hypothesis, the upper conductor lines were deposited without the chromium underlayer.

Another series of experiments was conducted to determine the influence of deposition conditions on the insulation quality of silicon monoxide films. In these experiments, silicon monoxide films were deposited at various pressures at substrate temperatures from 250 to 350°C. The vacuum system was pumped down to at least  $3 \times 10^{-6}$  torr. Prior to deposition, the silicon monoxide was evaporated to outgas the source and getter residual gases. This operation produced vacua of  $2$  to  $3 \times 10^{-7}$  torr which could be maintained indefinitely without further gettering. To establish gas pressures in the  $10^{-6}$  and  $10^{-5}$  torr range, a controlled leak was installed and connected to a sealed container with water. Thus it was possible to evaporate silicon monoxide at well defined pressures of water vapor.

The condensation rates in these experiments were kept constant at about 20 Å/sec. At each pressure-temperature combination, 2 test panels with chrome-copper lines evaporated through masks and 2 panels with etched but not electro etched lines were simultaneously coated with silicon monoxide.

#### Crossover panel testing

Immediately after fabrication, the crossover panels were submitted to a series of test operations to determine the effect of electrical and thermal stresses on the number of insulation defects. The electrical testing involved three different procedures:

- a) Measurement of the insulation resistance of each crossover individually with a tube electrometer.
- b) Electrical stress periods during which 1 Megacycle pulsed d. c. of 15 volts was applied simultaneously to all crossovers on one card. The current limiting resistance was 500 ohms. The stress was repeated each time with reversed polarity and represents about 2 1/2 times the voltage which the crossovers on the functional circuit panel would experience while performing a logic function. Pulse d. c. was chosen to duplicate the operating conditions of circuit cards as closely as possible.
- c) Each panel was connected to a counter which was set to register current pulses produced by intermittent insulation breakdowns below a threshold value of 7.5 megohm. Permanent shorts of lower resistance were identified and disconnected from the counter as soon as they occurred.

These tests and two thermal stress cycles were applied to all panels in the following sequence:

- (1) insulation resistance measurement
- (2) 1 hour test on counter
- (3) 4 hours of electrical stress, polarity changed after 2 hours
- (4) insulation resistance measurement
- (5) tinning of all upper conductor lines by contacting the entire panel surface with molten lead-tin eutectic of about 230°C in the presence of flux (triethanolamine).
- (6) insulation resistance measurement
- (7) 1 hour test on counter
- (8) 2 hours of electrical stress, polarity changed after 1 hour
- (9) insulation resistance measurement
- (10) heating of panels in air for about 40 sec. to 250°C to re-melt solder, followed by rapid cooling on a metal block, (simulated solder reflow process).
- (11) insulation resistance measurement
- (12) 1 hour test on counter
- (13) 2 hours of electrical stress, polarity changed after 1 hour
- (14) insulation resistance measurement

#### Characterization of crossover insulation defects

A crossover was considered satisfactory if its insulation resistance was greater than  $1 \times 10^9$  ohms at 15 volts and gave stable non-fluctuating readings during every measurement with the electrometer. The majority of crossovers had insulation resistances between 1 and  $6 \times 10^{10}$  ohms. Very few stable crossovers were found in the range from  $10^9$  to  $10^{10}$  ohms and none below  $1 \times 10^9$  ohms. Crossovers with silicon monoxide deposited at 250°C in the presence of  $2 \cdot 10^{-5}$  torr of water vapor had unusually high insulation resistances in the order of  $1 \times 10^{12}$  ohms. All insulation resistances changed, but only within one order of magnitude, after having been submitted to the various tests.

The crossovers which did not meet the two criteria for satisfactory performance are listed in table 4-4 and are broken down into 13 categories according to their resistance values. Each defective crossover is listed in the category representing its minimum resistance. There are two major types of crossover failures:

- A. Low-ohmic permanent shorts. These crossovers had insulation resistances below 100 ohms. Most of these defects were found in the initial measurement, although some occurred during the testing. Their resistances changed little and usually toward lower values. Only 2 out of the 44 low-ohmic shorts repaired themselves and assumed a high stable resistance after additional stress.
- B. Unstable crossovers. There are 212 crossovers of this type listed in table 1, covering a resistance range from  $10^3$  ohms to  $10^{12}$  ohms. When these crossovers were measured with the electrometer between the test procedures, their resistances were fluctuating. 139 of these crossovers never showed resistances below  $10^9$  ohms. The other 73 crossovers broke down to lower values but did not always remain low. Some of the electrical and thermal stresses brought the resistances up above the  $10^9$  ohm limit and very often resulted in stable readings. However, every crossover giving a fluctuating reading at any one of the measurements was counted as a defect regardless of its final condition.

As previously mentioned, silicon monoxide films deposited at  $250^\circ\text{C}$  and  $2 \times 10^{-5}$  torr of water vapor had unusually high insulation resistances. Table 4-4 shows, however, that this deposition condition causes a great number of crossover instabilities

The main result obtained from the counter tests is that test panels without crossover defects did not register any counts. This leads to the reassuring conclusion that crossover panels judged satisfactory on the basis of repeated but short-time resistance measurements are also free from intermittent breakdowns.

#### Influence of lower conductor line fabrication

According to the method of preparing the lower conductor line pattern, there are 3 different types of panels which were fabricated under identical conditions during all the other steps. The results of this experimental series are shown in Table 4-5.

Table 4-4: Number of defective crossovers listed according to their lowest insulation resistance

	batch number	number of defective crossovers (resistance ranges in ohms)											total number of crossovers in batch				
		0.1-1	1-10	10 <sup>1</sup> -10 <sup>2</sup>	10 <sup>2</sup> -10 <sup>3</sup>	10 <sup>3</sup> -10 <sup>4</sup>	10 <sup>4</sup> -10 <sup>5</sup>	10 <sup>5</sup> -10 <sup>6</sup>	10 <sup>6</sup> -10 <sup>7</sup>	10 <sup>7</sup> -10 <sup>8</sup>	10 <sup>8</sup> -10 <sup>9</sup>	10 <sup>9</sup> -10 <sup>10</sup>		10 <sup>10</sup> -10 <sup>11</sup>	> 10 <sup>11</sup>		
lower conductor lines evaporated through mask standard procedure	56-10	2			1						3	2	2	1	1		90
lower conductor lines etched and slightly electro-etched	57-12				2	1	1				1	10	18				90
lower conductor lines etched and heavily electro-etched	57-13						2							1	1		90
1 panel standard procedure 2 panels etched and electro-etched	57-14	2	3			1	1					8	3		1		90
SiO insulator deposited at 250°C- 2 x 10 <sup>-7</sup> torr	57-17					2						1	5	5	1		90
SiO insulator deposited at 300°C- 2 x 10 <sup>-7</sup> torr	58-01	3	9			1								3	2		120
SiO insulator deposited at 350°C- 3 x 10 <sup>-7</sup> torr	58-02	1	3											3	2		120
SiO insulator deposited at 250°C- 7 x 10 <sup>-6</sup> torr	58-03														1	2	120
SiO insulator deposited at 300°C- 7 x 10 <sup>-6</sup> torr	58-04			2	1	3	2	5	3	10	8	7					120
SiO insulator deposited at 250°C- 2 x 10 <sup>-5</sup> torr	58-05										1			3	7		120
SiO insulator deposited at 350°C- 2 x 10 <sup>-5</sup> torr	58-06		1											1	6	37	120
SiO insulator deposited at 250°C- 2 x 10 <sup>-5</sup> torr	58-07	1	16	1							1	2	3	2	19		120
Total		9	32	3	0	4	8	6	11	17	27	35	67	37			1290

Table 4-5: Crossover defects as related to lower conductor line fabrication.

lower conductor lines	test schedule applied	number tested	of crossovers found defective	defects %	defect-free panels
evaporated through masks	complete	45	8	16	0 out of 3
	complete, but heat cycled without tinning	30	4		
etched	complete	45	15	24	0 out of 3
	complete, but heat cycled without tinning				
etched and electro-etched	complete	165	4	2.4	5 out of 8
	complete, but heat cycled without tinning	30	0		

Little significance should be attached to differences in crossover defects between directly evaporated and etched lines as listed in table 4-5 because the number of crossovers tested and the differences found are too small.

Table 4-5 shows, however, the substantial reduction of crossover defects which can be achieved by electro-etching of the lower conductor line pattern. Under conditions where directly evaporated or merely etched lower conductor lines produce about 20% crossover defects, the additional operation of electro-etching reduces these defects by one order of magnitude. Upon closer examination it was found that a very slight electro-etch rounding only the top corners of the line edges was sufficient to produce the desired effect. The same result was obtained by prolonged etching which rounded the line edges all the way down to the substrate surface.

#### The effect of omitting chromium during the second metal evaporation

Two panels with the lower conductor patterns evaporated through masks and two panels with etched (but not electro-etched) lines were finished in one batch by depositing an upper conductor pattern of copper alone. As shown in table 4-6, the omission of chromium reduces the number of crossover defects substantially regardless of the method applied in fabricating the lower conductor pattern. However, when it was attempted to tin these chromium-free copper lines, more than half of them were completely stripped from the panel.

Table 4-6: Crossover defects found on panels without chromium in upper conductor lines.

lower conductor lines	test schedule applied	number of crossovers		defects %	defect-free panels	stripped crossovers	
		tested	found defective			(no.)	%
evaporated through masks	discontinued after tinning	60	1	0.8	3 out of 4	33	55
etched	discontinued after tinning	60	0			31	52

Apparently, the deposition of a chromium film enhances the probability of forming crossover shorts and instabilities. However, the experiment also re-emphasizes the need for the chromium underflash to strengthen film adhesion, and omission of the chromium is not possible without finding a substitute interface material.

Influence of Silicon Monoxide deposition conditions

The rate of crossover defects on panels with silicon monoxide insulation made under different deposition conditions is shown in Table 4-7. Each figure was obtained from 120 crossovers, half of which were evaporated through masks and half of which were etched. Electro-etching was not applied.

Table 4-7: Crossover defects on panels with different silicon monoxide deposition conditions.

pressure during SiO deposition (torr)	Crossover defect rate (%) at substrate temperature (°C)		
	250	300	350
1.5 to $2.5 \cdot 10^{-5}$	37%	not tried	37%
6 to $8 \cdot 10^{-6}$	34%	9%	not tried
2 to $3 \cdot 10^{-7}$	16%	7.5%	2.5%

The data show a sharp increase of crossover defects, regardless of pressure, if the deposition temperature drops only 50°C below the former standard 300°C. Optimum results have been obtained with an increased deposition temperature of 350°C at pressures in the  $10^{-7}$  torr range. More recent experiments with functional circuit panels indicate that vacua around  $1 \times 10^{-6}$  torr combined with 350°C substrate temperature produce equally good insulation.

The detrimental effect of water vapor was expected and is quite evident from table 4-7. It is noteworthy, however, that the combination of 250°C with  $2 \times 10^{-5}$  torr of water vapor resulted in crossover resistances of several thousand  $\times 10^9$  ohms (see table 4-4). Although many of these were unstable, only one crossover broke down to a value below  $10^{10}$  ohms, and it returned to a stable  $34 \times 10^{11}$  ohms reading after solder reflow heating.

#### Comparison of panels with evaporated vs. etched lower conductor lines

The study of silicon monoxide deposition conditions involved a sizable quantity of panels with evaporated and with etched lower conductor lines in equal numbers and of identical preparation. Therefore, differences between the two methods of fabricating the lower conductor patterns can be deduced on a more reliable basis than before.

The number of crossovers with insulation defects of both kinds are listed in table 4-8, showing the data for evaporated and etched lower conductor lines separately for each experiment.

Table 4-8: Comparison of crossover defects on panels with evaporated vs. etched lower conductor lines.

batch number	SiO deposition		lower conductor lines	number of crossovers			
	pressure (torr)	temp. (°C)		tested	found defective		total
				low ohmic perm. shorts	unstable resistances		
58-01	2 x 10 <sup>-7</sup>	250	evaporated	60	5	3	8
			etched	60	7	4	11
58-02	2 x 10 <sup>-7</sup>	300	evaporated	60	3	3	6
			etched	60	1	2	3
58-03	3 x 10 <sup>-7</sup>	350	evaporated	60	0	3	3
			etched	60	0	0	0
58-04	7 x 10 <sup>-6</sup>	250	evaporated	60	1	10	11
			etched	60	0	30	30
58-05	7 x 10 <sup>-6</sup>	300	evaporated	60	0	10	10
			etched	60	0	1	1
58-06	2 x 10 <sup>-5</sup>	250	evaporated	60	0	21	21
			etched	60	1	23	24
58-07	2 x 10 <sup>-5</sup>	300	evaporated	60	17	9	26
			etched	60	0	19	19
Total:			evaporated	420	26	59	85
			etched	420	9	79	88

Comparing only the total numbers without differentiating between low ohmic shorts and unstable resistances, panels with an evaporated pattern have an average of 20% defects, whereas etched patterns produce 21% defects. These figures are very similar to the 16% and 24% listed previously in Table 4-5. These data prove that the etching procedures instituted to simplify the formation of the interconnection pattern do not introduce additional crossover defects.

Closer examination of the data in Table 4-8 shows that under certain conditions, line patterns evaporated through masks are inferior to etched line patterns. For example, of all the panels fabricated in batch 58-07, only those with evaporated lines had permanent shorts. The panels with etched lines from the same run had unstable resistances, of which only one dropped below the  $10^9$  ohm limit. Microscopic examination of samples from all runs listed in Table 4-8 revealed that small copper spheres had been ejected from the source and hit the substrate surfaces. This phenomenon was unusually severe on substrates processed in batch 58-07 and initiated a closer investigation of the conditions causing ejection of copper particles as well as their influence during further processing steps.

#### The effect of particle ejection from copper sources.

Through systematic microscopical examination, it was established that ejection of copper spheres occurred in practically every evaporation run, but to varying degrees. To give a better idea of this phenomenon, four types of evaporated copper surfaces are described:

- a) A very poor surface shows copper spheres visible with the naked eye; it has an appearance like very fine abrasive paper. The number of spheres per  $\text{cm}^2$  surface area is in the order of several thousand, their sizes vary up to 600,000 Å.
- b) A typical poor surface shows spheres mostly between 50,000 and 200,000 Å, some up to 300,000 Å in diameter. There are several hundred spheres per  $\text{cm}^2$  of surface area.
- c) A fair surface has an average of 10 to 100 spheres per  $\text{cm}^2$ . Most particles are 10,000 to 20,000 Å in diameter, but some may be as large as 50,000 Å.
- d) A good surface has no spheres larger than 20,000 Å and no more than 1 per  $\text{cm}^2$ .

It was found later that outgassing from the carbon crucibles was mainly responsible for the ejection of particles. Poor surfaces were always associated with new carbon crucibles, and only after at least 3 evaporations had been made out of the same source could fair surfaces be obtained. Also, copper evaporation rates significantly higher than the standard rate of 20 Å/sec. added to the problem.

The copper spheres did not adhere firmly to the surface. Mechanical action such as brushing, registration of masks in contact with the substrate surface, and possibly heat cycling during subsequent operations caused the particles to fall off. Test panels having evaporated line patterns showed practically no particles left under the insulating silicon monoxide film. Instead, there were numerous craters in the copper film with irregular edges and rough bottoms. Although the silicon monoxide films replicated the surface of the underlying metal film, the insulation at these points seemed to be poor.

It has been found repeatedly that these wrinkled areas in silicon monoxide films were easily penetrated by ferric chloride etch dissolving the copper film underneath, whereas a smooth silicon monoxide film protected the metal from attack for at least 24 hours. In addition, the large number of permanent shorts on test panels with evaporated lines in run number 58-07 (table 4-8) strongly suggests a correlation between insulation failure and surface damage due to particle ejection.

With etched conductor line patterns, different effects have been found. Here, the copper spheres were quantitatively removed from the surface while the KPR-coated lines were etched in ferric chloride solution. The etch attacked these unprotected copper film areas and produced holes about 5 to 10 times the diameter of the original spheres. These holes were circular, had smooth edges and flat bottoms formed by the silicon monoxide undercoat. The insulating silicon monoxide film subsequently deposited over these holes was smooth, firmly adherent and not penetrated by ferric chloride etch. Many crossovers had these etched holes in the lower metal conductor without showing insulation defects. This behavior explains why etched copper patterns were sometimes found superior to evaporated patterns.

Another problem arises from copper spheres on surfaces to be etched. When the glass mask with the image of the line pattern is brought in contact with the substrate surface, and also when these surfaces are wiped during the etching, the spheres are rolled over the film. This action scratches the copper film, and some of these scratches interrupt the line pattern and cause open circuits.

All these problems associated with copper particles impinging upon the film surface during deposition have finally been eliminated by substituting molybdenum crucibles for the carbon sources and by evaporating copper with close rate control. With molybdenum crucibles, deposition rates of at least 30 Å/sec., probably higher, can be achieved without ejecting copper particles from the source.

The effect of electrical and thermal stresses on the frequency of crossover insulation defects.

On all crossover panels, the insulation resistances have been measured immediately before and after the various stresses applied during the test procedure. Therefore, it is possible to evaluate the ability of crossovers to withstand the soldering and solder reflow operations used to attach transistors, and their stability under electrical stress.

A comparison of crossover stability for three types of panels is shown in table 4-9. The first row refers to panels with electro-etched copper lines under the insulator. The second row lists those panels where the silicon monoxide insulator had been deposited under optimum conditions. All the other panels, having neither electro-etched lines nor insulating films made under optimum deposition conditions, are included in the third group.

Table 4-9: Increase of crossover defects after having been submitted to various stresses.

Method of fabrication	crossovers tested	Crossover Defects					
		before 1st pulse	increase after d. c. stress *	before tinning	increase after	before solder reflow	increase after
Lower conductor lines <u>electro-etched</u> , standard SiO deposition conditions.	135	0	+1	1	+1	1	+0
Lower conductor lines <u>not electro-etched</u> , SiO insulator deposited at $350^{\circ}\text{C}$ , $3 \times 10^{-7}$ torr.	120	0	+0	0	+0	1	+2
Lower conductor lines <u>not electro-etched</u> , SiO insulator deposited at $T$ $350^{\circ}\text{C}$ or $p$ $3 \times 10^{-7}$ torr	840	75	+5	49	+33	106	+34

\*Voltage Stress = 15v

The results show that panels with a large number of initial defects as represented by group 3 are very susceptible to insulation breakdowns caused by the two heat cycling operations. In contrast to this behavior, panels with electro-etched copper lines, or with an insulator film deposited under optimum conditions may be submitted to any of the stress operations with little or no effect on their insulation resistance. The conclusion to be drawn is that the tinning and the solder reflow processes are compatible with film evaporation techniques, provided the crossovers are properly fabricated.

In this connection it should be mentioned that crossovers with unstable resistances sometimes assume stable values above  $10^9$  ohms after having been submitted to electrical or thermal stresses. This process of self-repair under stress was also found almost exclusively on panels of group 3. The frequency of these events is shown in table 4-10.

Table 4-10: Self repair of crossovers under stress.

Method of Fabrication as in table 6	crossovers tested	CROSSOVER DEFECTS					
		before 1st pulsed	repaired after d. c. stress	before tinning	repaired after	before solder reflow	repaired after
Group 1	135	0	0	1	1	1	0
Group 2	120	0	0	0	0	1	0
Group 3	840	75	31	49	3	106	42

In particular, the electrical stress and the solder reflow heat cycling have a stabilizing influence on weak crossover insulations. The mechanism of this repairing action is unknown.

Crossover test panels fabricated by a modified process.

In order to test the combined effect of electro-etching and increased silicon monoxide deposition temperature, 8 crossover panels with 30 crossovers each were made by incorporating the two changes in the method of preparation. In contrast to the fabrication schedule given previously, the lower copper conductor was electro-etched.

Furthermore, the silicon monoxide insulator films were deposited at 350°C, and in vacua below instead of above  $1 \times 10^{-6}$  torr.

The results of this series confirmed the expected effects of the modified process on crossover insulation quality. The 8 crossover panels were submitted to a test procedure essentially the same as outlined before, but omitting the first two counter tests and reducing the electrical stress periods to half the duration. During the entire test operation, not a single unstable insulation resistance was found among the 240 crossovers involved. Consistent with this situation is the fact that no counts indicating intermittent insulation breakdowns were registered. There were 3 low-ohmic shorts immediately after fabrication which did not change during the entire test. These have been carefully examined microscopically by etching away one metal film after another.

It has been established that these shorts are related to abnormal defects of the substrate or copper film surfaces, which can be avoided by careful preparation. Significantly, 2 of these shorts occurred on a substrate which was accidentally used on the unpolished side, and the crossover areas covered several chipped-out spots. The fractured glass surface was replicated by all films, and the silicon monoxide insulation was pervious to ferric chloride etch. The 3rd short involved a crossover with a heavily distorted and wrinkled insulator film, which was rapidly penetrated by the copper etch solution. The distorted silicon monoxide film replicated a large area on the copper surface which looked recrystallized, forming many laminated crystallographic twins. The cause of this irregularity in the copper film is not known, but it must be a very rare event since it was observed only once. A 4th low-ohmic short occurred during the testing after one of the substrates broke into two pieces, separating several crossovers. One of these crossovers was fractured in such a way that the upper tinned conductor film was bent around the broken edge and touched a protruding piece of the lower copper film.

No insulation defects other than this one mechanical short developed during the test procedure. It is concluded that unstable crossovers and insulation breakdowns due to tinning, re-heating of panels, or electrical stress are eliminated completely by introducing electro-etching and different silicon monoxide deposition conditions. This conclusion was largely supported by experiences made during the fabrication of functional circuit panels following this investigation.

#### 4. 2. 4 Masking Techniques

While the resistors and capacitors have been formed with standard masking techniques, the interconnection film patterns are best produced by masking techniques or a combination of pattern etching and masking. In the first method, the circuit interconnections are broken down into multilayers of conducting and insulating films vacuum deposited through appropriate masks. In the second method, the interconnecting circuitry is etched from a previously vacuum-deposited film covering the entire substrate, and only the line crossings and their insulation are deposited through masks. This method is particularly advantageous when circuit density makes masking tolerances and mask registration impractical.

Both methods require the same initial layout and photo reduction techniques. A 10x scale layout of the selected circuitry is first drawn as a composite on a coordinate graph (Figure 4-2). This complete layout is then broken down into the individual mask designs for depositing the segmented horizontal and vertical interconnecting conductor and resistor lines, lands and passive elements.

The masks are fabricated by any of the following three methods depending on the required precision: photo-etched glass, machined or arc eroded metal.

For photo-etched glass masks, appropriate photographic art work is furnished to Corning Glass Works and the masks are etched from "FOTOFORM B"\* glass, 0.015 to 0.030 inch thickness.

Etching tolerances are dependent on mask thickness, line opening uniformity, line length and overall pattern density. The longer lines, generally used for conductor depositions, range from 0.005 to 0.020 inch in width. These line widths may be held within  $\pm 0.001$  inch to 0.025 inch thick masks. However, the shorter line lengths and the uniform pattern used for resistors, coupled with mask selection, can provide mask openings within  $\pm 0.0003$  inch in the same glass thickness. Thinner masks, while allowing even closer tolerances, would sacrifice mask rigidity. Line to line center spacings are held to  $\pm 0.002$  inch over a 3 inch length.

Arc eroded masks are more readily adaptable to a complex repetitive pattern such as resistors, requiring precise dimensional control over a large number of similar lines or patterns. In this

\*Trade Mark, Corning Glass Works.

machining process the metal mask blank is submerged in an oil. An eroding arc bridges from the tool head to the work piece, reproducing the tool shape in the mask. A minimum of tool wear and the overall machine tool precision allow the tool pattern to be accurately reproduced many times over the mask blank. Resistor areas of 0.015 x 0.260 inch can be held to  $\pm 0.0003$  inch on a 3 inch surface. The relative location of each group of patterns on the same surface may vary by only  $\pm 0.001$  inch, which is superior to glass mask tolerances. Greater accuracy is also realized for a multiple number of identical masks.

Operational experience has shown that the breakage rate of glass masks offsets their initial lower cost relative to arc eroded metal masks. The use of conventional machined metal masks is restricted to less critical patterns. Although the line to line location tolerance can be machined within  $\pm 0.001$  inch, the tolerance on a typical 0.010 inch wide line opening may easily vary as much as 25%.

Since both mask and substrate have to be located from common points to maintain proper registration of the multilayered depositions, the linear coefficient of expansion of the materials used is critical. The expansion difference between "FOTOFORM B" masks and the pyrex glass substrate (mounted on an Invar holder) at 300°C causes a registration error of 0.003 inches in 3 linear inches. Invar metal masks under similar conditions cause a registration error of 0.0035 inch in 3 linear inches. However, no appreciable misregistration due to differences of expansion are experienced at 150°C. Allowances for expansion misregistration are made in the circuit layout.

Progress in this area has centered around the optimization of circuit and masking layouts to ease the registration tolerance by increasing insulation and conductor film connection areas. Wherever possible, sharp corners in mask openings have been eliminated to relieve stress in the glass masks and reduce breakage. Silk screen edge lands, originally used, were discarded in favor of vacuum deposited chromium-copper lands. This eliminated a registration problem, as well as a fabrication step. In addition, the evaporated lands are more easily tinned by the drum soldering technique.

#### 4.2.5 Instrumentation and Process Control

The required reproducibility from deposition to deposition necessitates precise control over the many parameters involved in the vacuum deposition process. Vacuum chamber pressures are monitored by conventional ion gauge circuits. Safety interlock systems have been installed to provide continuous operation of the vacuum pumps.

The atmosphere in the annealing furnaces is 10% hydrogen - 90% argon, to prevent oxidation of the copper lands. The substrate must be cooled to 80°C before allowing air to contact the lands. A flow rate of one liter/minute has been found satisfactory to prevent oxidation due to backstreaming.

A de-oxidizer-drier unit was installed to further control the reducing atmosphere used in the resistor annealing operation. Some improvement in keeping the lands bright and clean was noted during the normal annealing cycle (~ 4 hours). However, during extended annealing cycles, (greater than 10-12 hours) the lands may become discolored. Extended anneal cycles are required only if the initial resistor values exceed 1.5 times the desired final anneal value. Since only the exposed portions of the copper lands showed any signs of discoloration, an analysis of the annealing atmosphere was made by gas chromatography. Besides argon and hydrogen, traces of nitrogen were detected, but no trace of free oxygen. Dew point measurements to detect water vapor showed the dew point to be approximately -45°C ±10°C. This dew point is adequate to prevent oxidation of the copper. However, during excessively long annealing cycles or with inadequate copper film thicknesses, the chromium diffuses to the surface of the copper. When this condition occurs the water vapor content is high enough to oxidize the chromium. Since the final resistor fabrication process has eliminated the need for excessive annealing times, land oxidation has been essentially eliminated.

The evaporation rate of both the silicon monoxide and the copper is controlled by an ionization gauge rate monitor<sup>(5)</sup>. An ionization tube type element (Figure 4-18) senses an ionized portion of the vapor stream. The output of this sensing element is partially compensated by the ionization current of a regular vacuum gauge which indicates the background pressure. The current difference of the two gauges feeds into a recorder-controller regulating the power input to the source and thus controlling the evaporation rate<sup>(2)</sup>. Film thicknesses were deposited within 5% of the desired values. Actual thickness measurements were taken from monitor slides for each deposition. The conventional Tolansky interferometric technique was used.

#### 4.3 FUNCTIONAL ASSEMBLIES (Phase III)

The objective of this phase of the contract is to fabricate an operational thin film assembly which will demonstrate the capability of the techniques and processes developed under Phase I and Phase II.

#### 4.3.1 Functional Assembly Design

Detailed design information pertaining to the functional assemblies fabricated under this contract is contained in section 4.3 of the first quarterly report. A summary of this design information is presented below.

##### Circuit Design

The functional assembly utilizes a single transistor resistor logic circuit (TRL) (Figure 4-19) employing the basic NOR function. This circuit was selected as a result of a study which considered factors pertaining to both electrical performance and thin film fabrication compatibility. Having selected the basic TRL-NOR circuit as the most compatible type, an electrical design procedure was utilized which would enable the circuit to perform properly under extreme worst case conditions. As an example of this design technique, the circuits would operate correctly with resistors having  $\pm 15\%$  tolerances.

##### Circuit Topological Layout

The topological layout used for the TRL - NOR is shown in Figure 4-20. The resistor material for this design has a resistivity value of 250 ohms per square. Distributed overdrive capacitors are provided in the layout to increase the circuit speed and to minimize circuit delays. 0.025 inch wide land areas are provided in the layout for attaching the transistor to the circuit. The transistor utilized in this design is the 2N853 micro mesa device from Texas Instruments, Incorporated. The basic layout includes two TRL - NOR circuits within a 0.435 inch by 0.310 inch area.

##### Functional Assembly Panel Design

A basic substrate size of 2.5" by 3.5" was selected for the functional assemblies. The size of the substrate was influenced by (1) the placing of the circuit interconnection burden on the circuit panel thereby minimizing back panel interconnections, (2) the component design goal of at least 6000,000 components/ft.<sup>3</sup> for a functional electronic assembly, (3) the necessity of transistor replacement at high maintenance echelons, (4) the capability of the design to meet a wide range of airborne or ground based military applications, (5) the size and cost of a throw-away package and (6) the maximum area over which the required degree of control in the fabrication of film components could be attained. The total panel design as shown in Figure 4-21 contains 28 pairs of 56 identical TRL-NOR circuits.

Space is provided on the panel for six vertical and four horizontal 0.010 inch wide interconnection conductors on 0.025 inch centers. Connections can be made to these conductors at any point on the panel and crossovers can be obtained by insulating the lower conductor layer with silicon monoxide. The lower edge of the panel contains 44 input output connections spaced on 0.075 inch centers.

#### Logic Design

The logic selected for the functional assembly is shown in Figure 4-22 and contains a 4 stage binary counter, necessary control circuits and a self contained two speed oscillator. This logic was selected as a representative example of computer logic and circuit interconnection complexity. All 56 circuits contained on the panel are utilized with this design.

#### 4.3.2 Functional Assembly Fabrication

##### Fabrication

In the early stages of the program the complete functional circuit pattern was deposited entirely through masks. The fabrication steps, the materials, and the vacuum parameters are tabulated in Table 4-11. When the insulation patterns were evaporated in two independent 15,000 Å deposition steps, 14 different mask patterns were used for 17 separate evaporations.

An early material change was the substitution of copper lands for gold. Gold has a high surface mobility and is known for its poor adhesion. In addition, it is readily scavenged by the solder in the tinning operation. This raises the melting point of the tinned lands and impedes the solder reflow process during the transistor assembly operation. Adhesion of solder joints to gold lands is also poorer than with copper lands.

By utilizing the pattern etching technique, the interconnection circuit is fabricated in one step leaving only the jumpers and capacitor plates as additional conductor depositions. Although the capacitor plates could be combined with the jumper pattern in a single mask, they were purposely separated to provide flexibility for circuit analysis. With this approach only 13 evaporation steps, including the overlays, using 10 masks were required. Table 4-12 shows the simplified fabrication sequence.

TABLE 4-11

## Functional Assembly Fabrication Steps

Step	Material	Thickness (Å)	Deposition Temp. (°C)	Pressure (torr)	Time (min)	Usage or Remarks
1.	SiO	15,000	350	$1 \times 10^{-6}$	15	Undercoat
2.	Cermet	_____	220	$1 \times 10^{-4}$	5	Resistors -250 ohms/square 70% Cr 30% SiO
3.	Cr-Au	5,000-10,000	220	$5 \times 10^{-6}$	10	Land areas for resistors, conductors, and transistors
4.	SiO	5,000	300	$1 \times 10^{-6}$	5	Resistors overcoat prior to anneal
5.	_____	_____	425	_____	_____	Anneal and test resistors in air or forming gas
6.	SiO	10,000	300	$1 \times 10^{-6}$	10	Resistor overcoat after anneal
7.	Cu	15,000	220	$5 \times 10^{-6}$	15	Ground plane
8.	SiO	30,000	250	$1 \times 10^{-6}$	30	Ground insulation
9.	Cu	15,000	220	$5 \times 10^{-6}$	15	Signal interconnection
10.	SiO	30,000	250	$1 \times 10^{-6}$	30	Insulation
11.	Cu	15,000	220	$5 \times 10^{-6}$	15	Voltage plant
12.	SiO	30,000	250	$1 \times 10^{-6}$	30	Insulation for voltage
13.	Cu	15,000	220	$5 \times 10^{-6}$	15	Signal interconnections
14.	Cu	10,000	220	$5 \times 10^{-6}$	30	Capacitor plate (this compo- nent was not placed on prelim- inary units.)
15.	SiO	20,000	250	$1 \times 10^{-6}$	20	Overcoat
16.	SiO	20,000	250	$1 \times 10^{-6}$	20	Overcoat (two masks required for final overcoat)
17.	_____	_____	_____	_____	_____	Final test of resistors, Insulation and connections
18.	_____	_____	_____	_____	_____	Attach semiconductors
19.	_____	_____	_____	_____	_____	Final test Operational Unit

TABLE 4-12

Functional Assembly Fabrication Steps Using  
the Combined Evaporation-etch Process

Step	Material	Thickness ( $\text{\AA}$ )	Temp. ( $^{\circ}\text{C}$ )	Pressure torr	Deposition Rate	Usage or Remarks
1	SiO	15,000	350	$2 \times 10^{-6}$ max.	$20 \text{\AA}/\text{sec.}$	Undercoat
2	Cermet	--	200	$1 \times 10^{-4}$ $5 \times 10^{-5}$	$1 \text{\AA}/\text{sec.}$	Resistors 250 ohms/sq.
3	Cr-Cu	10,000	150	$2 \times 10^{-6}$ max.	Cr=3 $\text{\AA}/\text{sec.}$ Cu= 20 $\text{\AA}/\text{sec.}$	Land areas for resistors, con- ductors and transistors
(NOTE: Cr is an underflash of 200-400 $\text{\AA}$ )						
4	SiO	5,000	350	$2 \times 10^{-6}$ max.	$20 \text{\AA}/\text{sec.}$	Resistor over- coat prior to anneal
5	--	--	425-450	--	--	Anneal resistors 2-5 hrs in form- ing gas, test resistors
6	SiO	20,000	350	$2 \times 10^{-6}$ max.	$20 \text{\AA}/\text{sec.}$	Resistor over- coat after anneal and complete capacitor dielectric
7	Cr-Cu	12,500	150	$2 \times 10^{-6}$ max.	Cr= 3 $\text{\AA}/\text{sec.}$ Cu= 20 $\text{\AA}/\text{sec.}$	Voltage, ground, and interconnec- tion etch plane
8	--	--	--	--	--	Etch interconnec- tion pattern & voltage & ground distribution using KPR etch techniques
(NOTE: For copper etch with $\text{FeCl}_3$ , $30^{\circ}\text{Be}$ . For chromium etch with $\text{AlCl}_3$ , $32^{\circ}\text{Be}$ + Solid $\text{ZnCl}_2$ to $41^{\circ}\text{Be}$ ; add 1-4 oz. concentrated $\text{H}_3\text{PO}_4/\text{gal.}$ )						
9	SiO	15,000	350	$2 \times 10^{-6}$ max.	$20 \text{\AA}/\text{sec.}$	Insulation for jumpers (1st step)
10	SiO	15,000	350	$2 \times 10^{-6}$ max.	$20 \text{\AA}/\text{sec.}$	Insulation for jumpers (2nd step)
11	Cr-Cu	20,000	150	$2 \times 10^{-6}$ max.	Cr= 3 $\text{\AA}/\text{sec.}$ Cu= 20 $\text{\AA}/\text{sec.}$	Jumpers
12	Cr-Cu	10,000	150	$2 \times 10^{-6}$ max.	Cr= 3 $\text{\AA}/\text{sec.}$ Cu= 20 $\text{\AA}/\text{sec.}$	Capacitor plates
13, 14, 15	SiO	20,000 ea.	350	$2 \times 10^{-6}$ max.	$20 \text{\AA}/\text{sec.}$	Overcoat (Three masks required for final overcoat)
16	--	--	--	--	--	Final test of resistors, insulation & connections
17	--	--	--	--	--	Attach semiconductors
18	--	--	--	--	--	Final test of operational unit
19	--	--	--	--	--	2 Conformal coatings (Sylkyd 1400*)

\*Trade name - Dow Corning

Figure 4-21 shows an integrated counter functional circuit card fabricated by the evaporation-etch process. The voltage and ground distribution networks on the panel were altered from the all-mask version in order to realize the simplified fabrication procedure. In the all-mask version, power is distributed by means of a deposited transmission line running between each pair of circuits on the panel. However, in the pattern-etch version of the functional assembly the voltage and ground lines are etched side by side. Evaporated jumpers are used to bring voltage and ground to each film circuit.

### Packaging

It was readily apparent during the initial phases of the program that mechanical tests of the substrate alone would provide little useful data. Film circuitry is deposited within 50 mils of three substrate edges and immediately up to the fourth edge. Since the substrates alone would neither meet the mechanical tests for shock and vibration nor could they be used without further packaging, a first level assembly was developed. Two substrates were laminated back to back with an epoxy core in between. The core material was a 50-50 mixture by weight of Dow Corning #334 Epoxy resin and reactive "Versamid"\* #125. The core epoxy was filled with 20% by weight of glass microballoons (Cuming Eccospheres Si).

This material was precast into sheets and cured at 150°F for 2 hours. The substrates were bonded to this core by using the 1:1 resin mixture as an adhesive. Core thicknesses ranged from 36 to 95 mils and were adjusted by appropriate shims in a hot-press die (Figure 4-23). The core thickness could be maintained within ±2 mils over the 2.5 x 3.5 inch substrate area. Testing of an early lamination sample with the 95 mil core showed no resonance frequency below 2000 cps. However, the thickness of this laminated structure reduced the overall component density, and thinner core samples were fabricated.

A sandwich of two 40 mil substrates with a 38 mil core of stainless steel mesh and epoxy-amide filler was evaluated. It was found that the natural resonance frequency of the laminated package increased from 880 cps to 1400 cps. However, the band width of the resonance peak decreased significantly, and calculation of the energy dissipated due to the damping of the core showed that the structure containing the wire mesh dissipated about 50% less energy than a similar one having a core but no mesh. The increase in the spring constant of the structure as reflected in the increase of the resonance frequency offers no advantage when compared with the detrimental effects of band-width decrease and loss of damping efficiency.

\*Trade Mark, General Mills, Incorporated.

Additional test samples were fabricated using a 45 mil core with an embedded aluminum honeycomb. This laminate still had resonance frequencies below 2000 cycles.

In addition, the honeycomb, like the wire mesh produced a loss of damping compared with the unstiffened core. Consideration was given to 0.020 inch substrates and 0.088 inch core material. This approach met density goals and showed no mechanical resonance below 2000 cycles. However, the use of 0.020 inch substrates increased the cost and resulted in fabrication difficulties which drastically reduced the yield (see section 4.2.2).

The testing of 0.020 inch substrates with an unreinforced 0.045 inch core showed a resonance point at 950 cycles, but the vibration was not of a magnitude great enough to cause mechanical failure of the assembly, and it was decided to use this approach for the final assembly package. Encasing the laminated substrates in a light-weight aluminum frame and adding a connector completed the package. The 44 edge lands of each of the two circuit panels in the laminated assembly core are connected to an 88 pin male connector. The aluminum frame is attached to this connector providing direct coupling of the insertion and removal forces. The assembly consisting of the two conformally coated laminated panels, the frame and the connector, is bonded together with the same visco-elastic adhesive used in the core.

This adhesive acts as a resilient buffer for the forces imposed upon the package during thermal cycling and mechanical stressing. Preliminary vibration tests of the completed package indicated that the natural resonance frequency approaches 3000 cycles. Figure 4-24 is a photograph of the fully integrated functional assembly. A mirror image of the reverse side of the assembly appears in the background of the photograph.

#### Protective Overcoating

For environmental protection of thin film circuit panels, some form of a conformal overcoat is necessary. The requirements to be met by this protective coating are mechanical strength and chemical and thermal stability in the temperature range from -55 to 160°C; it should also be an electric insulator and impervious to moisture. Finally, the coating should be thin enough to permit selective removal and replacement of individual active elements soldered to the film circuit network.

Evaluation of several protective coatings has been made in this laboratory during previous IBM thin film programs. Of eight conformal coatings tested, Sylkyd 1400, has proven to be the best in MIL-STD 202 Method 106A environmental stresses (Figure 4-25). When applied on top of an evaporated SiO overcoat, it has protected operational thin film circuit modules against the effects of temperature and humidity and power (bv) cycling for 1600 hours or approximately 70 cycles of the above mentioned military environmental test.

This period is ten times longer than that obtainable with evaporated SiO overcoats alone. Based on these results, it was decided to use Sylkyd 1400 as the conformal coating for protecting the test assemblies and functional assemblies against the effects of environmental stresses. The detailed procedure for coating the finished assembly is given in Section 4-5.

The method of applying and curing Sylkyd 1400 has considerable influence on its properties. In order that the solvents can be removed prior to curing without forming pores or imperfections, the Sylkyd should be applied in films 0.002 to 0.003 inches thick. After drying, the coating is cured for 1 hour at 150°C. This treatment does not cure the polymer completely, but produces a firm and nonsticky surface. Next, a second coat of Sylkyd is applied and treated similarly. If the first coat has been completely cured, the second film does not wet or adhere to the surface of the first one. Total film thickness is a critical parameter. It has been observed that films .010 inch thick have a tendency to crack and lift up during temperature cycling. Therefore, a total maximum thickness of 0.006 inches is recommended.

The finished Sylkyd coat, if properly treated and cured, is hydrophobic and visco-elastic enough to allow small dimensional changes of the finished panel due to temperature changes. It can be softened with a soldering iron so that defective transistors may be removed from the functional panels. The effectiveness of the coating with regard to protection against the environmental stresses specified for the functional assemblies will be discussed in Section 4.4.

#### 4.4 TEST RESULTS AND EVALUATION

This section compiles the test data and evaluations performed for all phases of the program. Due to the close interrelationship between test data pertaining to integration techniques, process controls and functional assemblies, it was considered more appropriate to compile this data

into one complete section. The primary objective of this contract was to demonstrate with the functional assemblies the processes and techniques developed under Phase I (Integration Technique) and Phase II (Process Controls). Therefore, emphasis has been placed on the test data which pertain to the functional assemblies.

#### 4.4.1 Component Evaluation

##### Resistors

The thin film resistors produced under this contract were evaluated using the four-point-probe technique and the semi-automated measuring and recording system described in section 4.2.5 of the First Quarterly Report. Microminiature probe assemblies have been designed for use in special test stations to permit the automatic recording of values for all resistors on a thin film panel. An IBM 1401 Data Processing System was used to aid in the evaluation of the data obtained.

The equipment used to obtain the data is as follows: a modified Electronic Measurements constant current generator model C612A, a Leeds and Northrup 1000-ohm 0.02% resistor, type 4035B, and a John Fluke DC voltmeter, type 801H. The unknown resistor value was read on an Electro Instruments model 3500, 5-digit, self-nulling direct-reading digital voltmeter calibrated in ohms. The voltmeter output can be processed by a code converter which drives an IBM type 526 card punch to allow the direct recording of data in the form of punched cards.

Functional assembly panels containing 224 film resistors are read with a 772-probe assembly which permits 4-point-probe measurement of all resistors with one setting of the probes (Figure 4-26).

The data obtained from the IBM 1401 Data Processing System are briefly described as follows. Resistor values and their location on the film panel are automatically recorded on punched cards and can be read and placed in one of two expandable tables in memory. One table is used for the 1000-ohm resistors and the other for the 4000-ohm resistors. When all values for the 2 resistor types have been placed in the correct memory table, the resistor values of each table are sorted into an ordered sequence. The system computes the median value of the resistors in both tables and moves the 6 highest, the 6 lowest and the 6 middle resistor values to a condensed table. The system then determines the total number of

resistors contained in each table which are above or below specified maximum percentage deviations from the median for unannealed resistors, or from a constant value for annealed resistors. This and other related information concerning the whole panel is obtained from the system in the form of printed pages and summary cards for each resistor type. The printed output contains the condensed tables of the 1000-ohm and 4000-ohm resistors, the resistor locations, percentage deviation of each resistor, the total of the lowest and highest percentage deviation, the calculated medians and the total number of resistors per panel. The printed outputs for the two functional assemblies which were subjected to the 1000-hour, 85°C operational life test and delivered to the U. S. Army Electronics Research and Development Laboratory under the terms of this contract are reproduced as Figures 4-27a and 4-27b. Seventy-nine thin film circuit panels have been evaluated by use of the resistor measurement and data reduction facilities described above. Since 56 1000-ohm resistors and 168 4000-ohm resistors on a panel must all meet specifications to establish the existence of an acceptable fabrication process, the data obtained were analyzed by considering the lowest and highest resistances for both resistor types on each panel. The distribution curves shown in Figure 4-28 and 4-29 show that the process developed is capable of producing large film panels containing 224 resistors of 2 types within  $\pm 10\%$  limits.

The nature of these distributions prohibits the direct derivation of the total spread in resistances on any one panel for either resistor design value, but the separately calculated spreads have been plotted in distribution form as percent of design value in Figure 4-30. The approximate 2:1 ratio of total spreads for the two resistor types may be partially attributed to shadowing, or the affect of mask fabrication tolerance on the dimensionally smaller 4000-ohm resistors. The total spread for all resistors on a panel is less than 15%. In addition, the capability of the process to produce a large number of panels having resistors with a high degree of uniformity, particularly the 4000-ohm values, is evidenced by the nearly normal straight line distributions.

The narrow range of resistance values for 1 panel was shown in section 4.2.5 of the Third Quarterly Report. To further demonstrate single panel resistor uniformity, 3 panels were selected from the extremes and center of the distribution for total resistance spreads, (Figure 4-30) and analyzed by considering 3, 4000-ohm resistors (a triplet) which are associated with each of the 56 separate circuits per panel. The resistance spreads were calculated, and only 4 of the 168 triplets were found to exceed 3%. Nearly two-thirds of

of the triplets exhibited spreads of 1% or less, and on Panel A, for which the total variation was 6.8%, the spreads of 83.8% of the triplets were within 1% (see Figure 4-31).

The yield of panels for the most recent run is described by the composite characteristics of the resistors for 96 consecutive starts, which include every glass substrate placed in the cermet evaporator for resistor deposition. For simplification, distributions of the lowest and highest resistance values are plotted for those panels containing resistance spreads within  $\pm 10\%$  limits, and the remaining panels are identified by percentages (Figure 4-32). Inspection of the data for the resistors shows that the lowest values are among the 1000-ohm resistors and the highest values among the 4000-ohm resistors. It was found that 3% of the panels contained low-value resistors with 1% resulting from a low deposition stop value, and the remainder being caused by over-anneal. Of the 14 panels which were rejected for high-value resistors, 3 were due to high deposition stop values and 3 were mechanically defective. In summary, these data show that a process has been developed to simultaneously deposit 224 thin film resistors of 2 types of a 2.5" by 3.5" glass substrate having resistivities of 250 ohm/square and dimensions of 0.015" x 0.240" or 0.0465" x 0.186" respectively which are within  $\pm 10\%$  of design, at a yield of 82.3%.

#### Conductors and Insulators

Methods for evaluating the resistance of deposited thin film conductors and insulators as used in test assemblies and functional assemblies are discussed in this section along with the results of measurements obtained. The continuity of conductors may be determined through simultaneous access to any two circuit or edge lands on a panel with the aid of two pairs of specially designed and mounted probes. The equipment which is used for this evaluation is similar to that described for the resistor measurements. Insulation resistances to  $1.5 \times 10^{+12}$  ohm may be read directly from the Mid-Eastern Electronics model 710 megatrometer, which contains a low-energy 15-volt source of DC potential. For 10 of the 12 test assemblies which were delivered under this contract, data were obtained by measurements between the pairs of edge terminals listed in Table 4-13. Data were not obtained on the 2 units mounted and delivered with the functional assemblies. The wiring diagram of the test assemblies is shown schematically in Figure 4-3. Each path for the continuity measurements included 4 dummy transistors (approximately 2.5 milliohms each) and 8 solder joints, plus the deposited chrome-copper conductors. For

each group of 8 circuits, which are arranged vertically on a panel, a left-hand path and a right-hand path were measured. For example, the edge terminals corresponding to these paths in the first group of circuits are 1-2 and 5-6. The lowest and highest resistance values for both paths on the 10 test assemblies are listed in Table 4-14. The average path length for the left and right paths on a panel was found to be  $3 \frac{5}{8}$  inches and  $3 \frac{7}{8}$  inches respectively. Except for one initial open resulting from a conductor defect, the few high values recorded were consistently found on the right-hand side of the panels. These higher values are due to the difference in conductor path length. Overall resistances were found to vary from 0.95 ohms/inch to 2.29 ohms/inch.

The measured insulation resistance values result from series/parallel combinations of insulated crossovers and reflect the value of the poorest insulator for each measurement. Nevertheless, after all depositions, the combined resistances of the insulators on the same test assemblies were found to vary from  $9 \times 10^9$  ohms to  $150 \times 10^9$  (see Table 4-14).

Table 4-13 Edge Terminal Identifications for Measurements of Insulators and Conductors on Test Assemblies

		6	7	8	12	13	14	15	18	19	20	25	26	31	32	37	38	39
Insulators	7		x															
	13					x												
	19									x								
	38																x	
Conductors		1-2	5-6	8-9	11-12	14-15	17-18	20-21	24-25	26-27								
		30-31	32-33	36-37	39-40	43-44												

Table 4-14 Resistance Values for Conducting Paths and Combined Insulating Areas on Test Assemblies

Panel No.	Conductors (Ohms)				Insulators ( $\times 10^9$ Ohms)	
	Left Paths		Right Paths		Lowest	Highest
	Lowest	Highest	Lowest	Highest		
1	3.54	3.72	3.67	4.50	16	45
2	4.18	4.42	4.63	5.32	16	42
3	4.30	4.75	4.48	5.61	18	45
4	3.87	4.44	4.13	Open	9	36
5	3.56	6.41	3.74	6.06	17	60
6	3.82	4.15	4.02	4.74	9	24
7	4.62	7.01	4.77	8.89	54	150
8	5.15	5.72	5.52	7.06	36	100
9	5.10	5.54	5.30	6.94	15	36
10	3.45	4.15	3.62	5.40	15	100

#### 4. 4. 2 Functional Assembly Test and Evaluation

To decrease the time required to test a completed functional assembly, sample measurements of the interconnection films was made, followed by an operational test which utilizes transistors temporarily placed in contact with the panel.

Fully evaporated film circuit panels which have not been populated with transistors are operationally tested by utilizing a set of transistors which have been assembled into a special probe. The probe allows miniature transistors to be precisely registered with the land areas on the film panel. The probe assembly is shown in Figure 4-33.

The logic tester design was determined by the logical functions performed by the functional assembly and by the layout of interconnections. A schematic drawing of the logic tester design is shown in Figure 4-34. The functional assembly consists of a 4 stage binary counter, control circuits and a self-contained two-speed oscillator, as schematically shown in Figure 4-22. The logic tester includes necessary circuitry and switches to completely test the functional assembly. Since the film interconnections are complex, it was necessary to assure the absence of extraneous communication between the circuit groups contained on the panels. For this purpose, an electronic comparator was designed as a portion of the tester, to directly check 42 of the 56 NOR circuits.

Indirectly, it will also detect crosstalk from the internal oscillator and counter reset circuits as well. The logic tester will accept complete functional assemblies, or may be used in conjunction with the transistor fixture described previously for operationally testing film circuit panels during fabrication.

The test method employed in the comparator causes an external pulse generator to synchronously drive the film panel under test together with a conventional-component duplicate of the panel such that the output of both counters is continuously and electronically compared for differences which will result in the lighting of error indicators.

#### Functional Assembly Electrical Performance

The electrical tests performed on Functional Assemblies include measurement of oscillator frequency, supply voltage margins and operation in the logic tester.

Four complete functional assemblies were tested for oscillator frequency and the results are tabulated in Table 4-15. At 85°C ambient, oscillator frequencies on panels 1 and 4 were found to decrease approximately 16% for low frequency operation and 20% for high frequency operation. During these tests all other circuits on the panels operated properly at the frequencies shown.

To determine the minimum supply voltage at which the four functional assemblies operate properly, voltage margins were taken with the +6-volt DC supply. In the high frequency mode of operation, the panels functioned normally at +4.2 volts, and in the low-frequency mode, +3.7 volts. Table 4-15 tabulates the voltage at which normal operation ceased. According to the worst-case design, the voltage was 5.76 volts (-4%). However, the nearly 30% decrease required to cause failure is due to the use of transistors and resistors which were not at worst case tolerances.

The logic tester was used to insure intermittent-free operation of functional assembly panels throughout various processing stages. Approximately 48 test hours were accumulated on panels tested before transistors were attached. For this purpose, the logic tester was used in conjunction with the special transistor probes. After permanent transistor attachment, a total of 450 hours of testing on the electronic comparator was accumulated. In addition, the two functional assemblies which were subjected to 1000-hour life tests at 85°C were tested at 25°C for 16 and 22 hours each, and found to be devoid of any errors.

The turn-on and turn-off delays and transitions for representative TRL circuits have been reported in detail for several functional assemblies in section 4.3.2 of the Second Quarterly Report and the Third Quarterly Report. Typical average delays and transitions for assemblies are listed in Table 4-16.

Table 4-15 Oscillator Frequency and Supply Voltage Margins

Assembly No.	Oscillator Frequency (mc)		Lowest Supply Voltage for Operation (Volts)	
	Low	High	Low Freq.	High Freq.
1	1.68	2.97	3.7	3.9
2	1.84	3.44	3.6	3.9
3	1.78	3.08	3.4	4.2
4	1.82	3.48	3.2	3.4

Table 4-16 Average Resolution Times for Functional Assemblies

Fan In	Fan Out	Average Delay (msec)		Average Transitions (msec)	
		On	Off	On	Off
1	1	30	42	31	80
1	2	30	52	50	50
2	1	30	48	28	48
3	3	42	30	40	42

#### 4.4.3 Functional Assembly Test Unit

A functional assembly test unit (Figure 4-35) was constructed which allows easy operation of the functional assembly. Figure 4-36 is a wiring diagram of this unit. With a functional assembly plugged into the test unit, proper inputs are supplied to the assembly and several outputs are available. The selector switch allows operation either at the high or low frequency, single pulse, or single pulse automatic. Push buttons are available for single step and reset. A cycle control switch allows the functional assembly counter to run continuously or to halt when the counter is full. A slow speed multivibrator is contained within the test unit to automatically step the counter at very slow speeds. Two 2N501 transistors are used for this purpose. Four Kay Pinlite indicator lamps, type 15-15, are used to display the counter output in slow speed operation, and test points are brought out to permit viewing waveshapes with an oscilloscope.

Power is supplied to both the test unit and the functional assembly through jacks mounted at the rear of the unit. A 6-volt supply will operate the unit with red terminal serving as the positive input and the black terminal accepting the negative input. The chassis is not grounded. Total power supply current to a functional assembly and the test unit is 220 milliamperes DC for the internal oscillator mode of operation. In the single pulse mode, supply current is 200 milliamperes DC at a count of 0000 with all indicators extinguished or 250 milliamperes DC at a full count of 1111.

#### 4.4.4 Functional Assembly Environmental Tests

The environmental tests specified by Signal Corps Technical Requirement SCL-7568, dated 20 October 1960, the equipment used, and the test results obtained on 5 functional assemblies are described in this section.

Two functional assemblies were sequentially subjected to the specified shock, vibration, temperature cycling and moisture tests. A Jolta Shock Tester, model 500, equipped with a 1 millisecond shock pad, was used to subject the functional assemblies to 500 g shocks of 1 millisecond duration with 5 shocks in both directions along each of three mutually perpendicular axes for a total of 30 shocks.

The high-frequency vibration test was performed by using an MB Electronics Co., dynamic shaker model C10 to provide the vibration over the frequency range of 10 to 2000 cps and return to 10 cps in a total elapsed time of 20 minutes. The cycle was performed 12 times in each of 3 mutually perpendicular directions.

The temperature cycling test used a Conrad, Inc. controlled temperature chamber model FB8222 and an Electric Hotpack Co., Inc. model 1302 oven for the extreme temperatures of  $-55 \pm 3^{\circ}\text{C}$  and  $85 \pm 3^{\circ}\text{C}$ . The assemblies were held at each temperatures for 30 minutes with an intermediate storage of 15 minutes at  $25 \pm 10^{\circ}\text{C}$  for each cycle which was repeated for a total of 5 cycles.

The moisture resistance test utilized an American Instrument Co., Inc., model 4 5503 Climatolab to provide the 90-95% relative humidity over the  $25^{\circ}\text{C}$  to  $65^{\circ}\text{C}$  temperature range as shown by the time/temperature/humidity diagram in Figure 4-25. Chart type temperature recorders and mercury thermometers were used to monitor all tests which included thermal conditions.

To establish that the two assemblies were functioning correctly prior to the series of environmental tests, both were completely checked by use of the logic tester. In addition, the assemblies were operated with the logic tester in the comparator mode so that missing or extra pulses could be electronically detected. A total of 82.4 hours was accumulated by Assembly #1 and 36 hours by assembly #2. Panel #1 was also subjected to  $85^{\circ}\text{C}$  operational storage for 288 hours while attached to the electronic comparator. No malfunctions were detected during this time. The assemblies were then environmentally tested and it was found that #2 developed a crack during the temperature cycling which was due to inadequate clearance between the connector and frame, and the panel. The expansion tolerance required for the temperatures excursions was not sufficient and the connector and panels fractured. Assembly #1 which completed all environmental tests was checked in the logic tester and found to operate almost identically to that observed prior to the environmental stressing. After completing the environmental tests, assembly #1 accumulated 264 hours of error free room ambient operation in the electronic comparator.

Two additional functional assemblies were subjected to operational storage tests at  $85^{\circ}\text{C}$  for 1000 hours. During the storage period, indicator lamps were attached to the indicator drivers contained on the assemblies to monitor the panel performance. The assemblies were completely checked by use of the logic tester

both before and after the test. No significant difference in performance was observed. In addition, the assemblies were operationally tested by use of the electronic comparator for 6.5 hours and 16.4 hours each prior to the storage test, and 22.5 hours and 33 hours respectively subsequent to the storage test without the detection of any errors.

To insure that thin film circuit assemblies can be stored at very low temperatures, a test assembly and a functional assembly were stored at  $-55^{\circ}\text{C}$  for 1000 hours. As in the above environmental tests, the logic tester was employed to verify the operational capability of the functional assembly with 2.5 hours of comparator operation prior to the  $-55^{\circ}\text{C}$  storage, and 16 hours of error free operation afterwards. Resistance measurements for the conducting paths on the Test Assembly were made from the gold wires which had been attached at the edge lands. A 50 to 120 milliohms resistance change was noted as a result of the  $-55^{\circ}\text{C}$  Storage Test. A portion of the change apparently resulting from the storage test can be attributed to the variability introduced by the use of the attached gold wire used during this measurement. Table 4-17 tabulates the results of this test.

Table 4-17 Resistance Values for the Conducting Paths of the Test Assembly Stored at  $-55^{\circ}\text{C}$ .

Terminal Pair (No.)	Before Test (Ohms)	After Test (Ohms)	Change (%)
2-5	1.36	1.46	7.3
9-11	1.28	1.34	4.7
15-17	1.31	1.38	5.3
20-21	3.96	4.04	2.0
21-24	1.37	1.43	4.4
27-30	1.35	1.47	8.9
33-36	1.46	1.51	3.4

A summary of data obtained on the 5 functional assemblies which were environmentally tested is given in Table 4-18. The internal oscillator frequencies, voltage margins and power supply current drains were obtained with the panels inserted in the Test Unit which is described in section 4.4.3. The resistance for sample areas of insulation was obtained from measurements at the edge terminals, and is included along with the time each assembly accumulated while operating under the control of the electronic comparator, both before and after environmental tests. These data show that the functional assemblies operated successfully after all environmental tests.

Table 4-18 Characteristics of Environmentally Tested Functional Assemblies

	Shock, Vibr., T cycle & Moisture		-55°C Storage	85°C Operational Storage	
	Assy. 1	Assy 2.	Assy. 5	Assy. 3	Assy. 4
<b>Oscillator Freq. (Mc)</b>					
Low	1.78	1.8	1.98	1.82	1.81
High	3.1	*	3.55	3.48	2.95
<b>Power Supply Margin (Volts)</b>					
Low Freq.	3.4	*	3.6	3.2	3.7
High Freq.	4.2	*	4.0	3.4	3.9
<b>Power Supply Current (Ma.)</b>					
1111 Count	200	*	192	208	180
Oscillator	223	*	210	232	205
0000 Count	252	*	240	260	230
<b>Insulation Resistance (Ohms)</b>					
Gnd. / Voltage	$7.4 \times 10^3$	$7.5 \times 10^3$	$7.4 \times 10^3$	$73 \times 10^3$	$7.5 \times 10^3$
1-14	$105 \times 10^9$	$90 \times 10^9$	$33 \times 10^9$	$150 \times 10^9$	$30 \times 10^9$
1-26	$0.6 \times 10^9$	$30 \times 10^9$	$8.4 \times 10^9$	$24 \times 10^9$	$7.5 \times 10^9$
1-38	$6 \times 10^9$	$30 \times 10^9$	$18 \times 10^9$	$27 \times 10^9$	$16 \times 10^9$
<b>Comparator Operation (hrs.)</b>					
Before Env. Test	82.4	36	2.5	6.5	16.4
After Env. Test	264	*	16	22.5	33

\*Data not recorded.

### Test Results and Evaluation of Test Assemblies

The electrical resistance of conducting paths on test assemblies which include the solder joints as shown schematically in Figure 4-3 was determined from measurements performed at the connector pins. Measurements were taken both before and after sequentially subjecting two of the test assemblies to the specified shock, vibration, temperature cycling and moisture tests. The reproducibility of initial resistance measurements made at the connector pins for Panel 1 and Panel 2 was found to be much poorer than those obtained for Panels 3 and 4. On panels 3 and 4, the 4-point-probe measurements were made directly on the film connector edge lands. Both contact placement and contact resistance affected measurements at the pins, and repositioning of probes on the lands appeared as the limiting factor for reproducibility of measurements in the latter case. However, the data obtained for both tests is considered to be indicative of actual conditions. Since test assemblies fabricated by the processes described in the Third Quarterly Report and subjected to the environmental tests were found to be deficient in path resistance and overcoat adherence, 4 test assemblies were produced using the new processes described in section 4.2.3 of this report and environmentally tested. These showed changes in path resistance in relation to the severity of test but the total resistances did not exceed 8 ohms, or 2.6 ohms/inch including the connector pins, solder joints and thin film conductors. Table 4-19 includes the resistance changes as a function of initial value. Two other assemblies were tested for resistance to thermal shock by subjecting them to 13 cycles of  $-55^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  temperatures as shown in Table 4-20. A maximum of one minute was permitted for the transition of assemblies between the chambers.

Table 4-19 Resistance Values for the 14 Conducting Paths for 4 Test Assemblies, Measured Before and After Environmental Test

Term. Pair (No.)	Shock - Moisture						Temperature Cycle					
	Panel 1			Panel 2			Panel 3			Panel 4		
	B Ohms	A	%	B Ohms	A	%	B Ohms	A	%	B Ohms	A	%
1-2	3.64	4.90	35	5.30	5.33	0.6	3.85	3.81	1.0	3.64	3.62	0.5
5-6	3.46	4.74	37	5.35	5.82	8.8	3.78	3.76	0.5	3.78	3.76	0.5
8-9	3.30	3.65	1.5	5.38	5.58	3.7	3.61	3.59	0.6	3.61	3.60	0.3
11-12	3.47	3.47	0	5.50	5.52	0.4	3.77	3.75	0.5	3.88	3.86	0.5
14-15	3.34	3.36	0.6	5.20	5.22	0.4	3.57	3.54	0.8	3.52	3.50	0.6
17-18	3.69	5.10	38	5.28	5.29	0.2	3.76	3.73	0.8	3.96	3.94	0.5
20-21	3.28	3.35	0.2	5.19	7.47	44	3.46	3.43	0.9	3.50	3.90	11
24-25	3.62	3.99	1.0	5.68	5.89	3.7	3.92	3.89	0.8	3.85	3.84	0.3
26-27	3.88	6.05	56	5.10	5.16	1.2	3.54	3.51	0.8	3.61	3.61	0
30-31	4.21	7.85	86	5.84	5.90	1.0	*	---	---	4.06	4.04	0.5
32-33	3.85	3.86	0.3	5.32	5.32	0	3.54	3.52	0.6	3.62	3.62	0
36-37	4.90	4.90	0	6.32	6.40	1.3	4.17	4.15	0.5	4.28	4.27	0.2
39-40	4.72	4.85	2.7	5.51	6.40	17	3.71	3.65	1.6	4.46	4.45	0.2
43-44	5.62	5.61	0.9	4.40	4.36	0.9	4.40	4.36	0.9	4.80	4.80	0

B - Before Test

A - After Test

\* - Initial conductor defect of known cause.

Table 4-20 Time/Temperature Relation for Thermal Shock Test

<u>Step</u>	<u>Temperature (°C)</u>	<u>Time</u>
1	-55 ±0/ -3	1/2 hr.
2	±25 ±10/ -5	1 minute
3	±85 ±3/ -0	1/2 hr.
4	±25 ±10/ -5	1 minute
5	Repeat steps 1 through 4 for a total of 8 times	
6	±25 ±10/ -5	16 hrs.

#### 4.5 MATERIALS AND PROCESSES

This section represents a step by step outline of the materials, procedures, and process parameters used in the fabrication of thin film circuit panels.

##### 1. SUBSTRATES

- 1.1 Material "PYREX" glass, 2.5 x 3.5 in<sup>2</sup> (Corning 7740)  
.040 in ±.005 in.
- 1.2 Surface requirements: surface shall be free of cracks, bubbles, and pit marks. Scratches shall not exceed 300 Å in depth. Overall curvature must not exceed 0.001" at any point in the surface plane.
- 1.3 Cleaning Procedure
  - 1.3.1 Clean ultrasonically in 1 part Oakite\* - 8 parts hot water for 5 minutes.
  - 1.3.2 Rinse in hot running water for 5 minutes.
  - 1.3.3 Clean ultrasonically in 1 part Orvis\*\* - 8 parts distilled water for 30 minutes.
  - 1.3.4 Rinse three times in distilled water, using vigorous agitation by hand with each change of water.
  - 1.3.5 Rinse ultrasonically in distilled water for 20 minutes.
  - 1.3.6 Repeat steps 1.3.4 and 1.3.5 until the ultrasonic rinse water shows 1 megohm resistivity.
  - 1.3.7 Rinse ultrasonically in reagent grade methanol for 3 minutes.
  - 1.3.8 Repeat step 1.3.7 using fresh methanol.
  - 1.3.9 Store in dust-free glass container and seal until ready for use. This last step should be done in a dust-free atmosphere.

\* Oakite Products, Inc.

\*\* Soalco Products Company

2. SILICON MONOXIDE UNDERCOAT DEPOSITION

- 2.1 Substrate surface temperature: 350°C
- 2.2 Evaporation pressure:  $2 \times 10^{-6}$  torr, maximum
- 2.3 Evaporation rate: 20 Å/sec., controlled by ionization rate monitor
- 2.4 Thickness: 15,000 Å
- 2.5 Source: Hollow crucible (Drumheller type)
- 2.6 Source to substrate distance: 18 inches
- 2.7 Source material particle size between 20 and 3.5 mesh

3. SURFACE CLEANING

- 3.1 Clean ultrasonically in 8 parts distilled water and 1 part Orvis for 10 minutes.
- 3.2 Rinse in distilled water, changing the water three times
- 3.3 Agitate ultrasonically in fresh distilled water for 10 minutes.
- 3.4 Repeat step 3.2
- 3.5 Repeat step 3.3, but only for 3 minutes.
- 3.6 If rinsed water shows a resistance lower than 1 Megohm, repeat 3.4 and 3.5.
- 3.7 Agitate ultrasonically in methanol for 3 minutes.
- 3.8 Repeat 3.7 using fresh methanol
- 3.9 Store panel in methanol in a sealed container until ready for further processing. Remove panel slowly from methanol so that the solvent evaporates continuously and evenly.

#### 4. CHROMIUM-SILICON MONOXIDE CERMET RESISTOR DEPOSITION

4.1 Materials: Chromium - 99.8% purity, particle size between 325 and 400 mesh

SiO - vacuum degassed, particle size between 325 and 400 mesh

SiO<sub>2</sub> - colloidal (Cab-o-sil\*)

4.2 Composition of mixed Cr-SiO-SiO<sub>2</sub> powders for flash evaporation of 250 ohm per square resistors

65 at. % Cr

35 at. % SiO

0.5% by weight colloidal SiO<sub>2</sub> (Cab-o-sil)

4.3 Constituents must be thoroughly mixed prior to evaporation.

4.4 Substrate surface temperature: 200°C

4.5 Evaporation pressure  $2 \times 10^{-5}$  to  $1 \times 10^{-4}$  torr.

4.6 Source to substrate distance: 50 cm

4.7 Source design: flash evaporation source is a Ta ribbon 1.5" x 1.0" x 0.005" curved to fit between electrode posts 1 1/4 inches apart, operated at a power input of 1200 watts. The pre-mixed powder mixture is delivered to the hot filament by a worm-drive powder feed and tantalum chute. The exit aperture of the chute is positioned approximately 2" above and 1/4" away from the side edge of the filament.

4.8 Evaporation Rate  $\approx 1 \text{ \AA}/\text{sec.}$

NOTE: A vibrating powder feed is not suitable for the mixed cermet powder.

4.9 Monitor stop value: approximately 1.3 times the desired final resistance value. The monitor slide should be placed as close to the substrate area as possible. Two or three pilot runs should be sufficient to establish the monitor slide - substrate resistance ratio for accurate stop values.

4.10 After this deposition, when the substrate temperature has dropped to 100°C, the system is filled with 1 atmosphere of helium. At 80°C or below, the panels are taken out.

\*Cabot Chemical Company

5. CHROMIUM-COPPER RESISTOR LAND DEPOSITION

- 5.1 Substrate surface temperature: 150°C. In no case should this temperature exceed 165°C at the start of the deposition of copper.
- 5.2 Evaporation pressure:  $2 \times 10^{-6}$  torr, maximum.
- 5.3 Rate: Cr - 3 Å per second, controlled by power input to source.  
Cu - 20 Å per second, controlled by ionization rate monitor.
- 5.4 Thickness: Cr - 200 to 300 Å  
Cu - 10,000 Å
- 5.5 Sources: Cr - open tungsten boat (sublimation)  
Cu - baffled carbon crucible

5.6 Source to substrate distance: 18 inches.

5.7 Deposition sequence:

After about 50 Å of chromium have been deposited, the temperature of the copper source is raised to start the evaporation of copper. As soon as the desired Cr Cu-alloy film has been formed, i. e., after 1-2 minutes, the chromium source is turned off, and the deposition of pure copper is continued.

NOTE: Both sources must be completely outgassed before the shutter is opened for chromium deposition.

5.8 Helium flush (see section 4.9)

6. FIRST SILICON MONOXIDE RESISTOR OVERCOAT

- 6.1 Substrate surface temperature: 350°C
- 6.2 Evaporation pressure:  $2 \times 10^{-6}$  torr maximum.
- 6.3 Evaporation rate: 20 Å per second, controlled by ionization rate monitor.
- 6.4 Thickness: 5,000 Å
- 6.5 Source: Hollow crucible (Drumheller)
- 6.6 Source to substrate distance; 18 inches.

7. PRE-ANNEAL RESISTOR TEST

8. RESISTOR ANNEAL

- 8.1 When the resistors have been measured, a "mean value" resistor is selected for monitoring during anneal. Gold wires (0.003") are thermocompression bonded to the lands for electrical connections. If a digital ohmmeter is used, the monitoring must be intermittent; continuous monitoring results in a more rapid anneal of the monitor resistor due to the current and voltage applied by the ohmmeter.
- 8.2 Annealing temperature: 425 - 450°C.
- 8.3 Annealing atmosphere: 10% H<sub>2</sub>, 90% A (forming gas).
- 8.4 The TCR of -25 ppm/°C must be taken into account when setting the anneal stop value.
- 8.5 Annealing time: 2 to 5 hours, depending on monitor stop value and fine details of experimental procedure.

9. POST-ANNEAL RESISTOR TEST

10. SURFACE CLEANING

To remove residues or contaminants from handling the panels in the preceding operations, a cleaning procedure identical to the one in Step 3 is applied.

11. SECOND SILICON MONOXIDE RESISTOR OVERCOAT

Same procedure as in Step 6. Thickness - 20,000 Å.

12. CHROMIUM - COPPER ETCH PLANE DEPOSITION

- 12.1 Substrate surface temperature: 150°C. In no case should this temperature exceed 165°C at the start of the deposition of copper.
- 12.2 Evaporation pressure:  $2 \times 10^{-6}$  torr, maximum.
- 12.3 Rate: Cr - 3 Å per second, controlled by power input to source.  
Cu - 20 Å per second, controlled by ionization rate monitor.

- 12.4 Thickness: Cr - 200 to 400 Å  
Cu - 12,500
- 12.5 Sources: Cr - open tungsten boat (sublimation)  
Cu - baffled carbon crucible
- 12.6 Source to substrate distance: 18 inches.
- 12.7 Deposition sequence:

The chromium film is deposited without evaporating any copper. After the chromium source has cooled below the sublimation temperature, pure copper is deposited at the desired rate. There is no alloyed transition region between the two metal films.

### 13. COPPER CONDUCTOR LINE ETCHING

- 13.1 The substrate is covered with one coat of Eastman Kodak KPR and spun dry in a centrifuge at 300 rpm. The substrate is then dried at 40°C for one hour.
- 13.2 The KPR is exposed through appropriate art work for four minutes at a 24" distance from a 20 amp arc source.
- 13.3 The exposed KPR is developed for 3 minutes in KPR developer without agitation.
- 13.4 The developed KPR is treated with KPR black dye for 10 seconds and the unexposed KPR removed by rinsing in a jet of water regulated at 40°C.
- 13.5 The substrate is dried for 5 minutes at 110°C.
- 13.6 The surface of the substrate is cleaned by dipping in Metex L-5 diluted with an equal amount of water for no more than 5 to 10 seconds and rinsed in running water.
- 13.7 The KPR line pattern is inspected microscopically. Should there be scratches or open sections in the KPR film they are repaired at this time.
- 13.8 The uncoated copper areas are etched away either by spraying the panel with a solution of 60 g/ℓ FeCl<sub>3</sub> in water, or by immersing the panel in a solution of 300 g/ℓ FeCl<sub>3</sub> in water. The panel is thoroughly rinsed in running water of 40°C.

- 13.9 The panel is rinsed in methanol and dried at 40°C.
- 13.10 The KPR is removed by immersion in a commercial stripper solution. To insure complete removal, the operation is repeated with fresh stripper solution.
- 13.11 The stripper solution is rinsed off with running water, simultaneously wiping the surface gently with a cotton swab.

#### 14. ELECTRO-ETCHING OF CONDUCTOR LINES

- 14.1 The wet panel is mounted in a frame providing electrical connection along all edges of the substrate. It is immersed in Metex L-5 opposite a copper counter electrode spaced 2 in. away from the panel. The copper lines are anodically etched by passing a current of 2 amperes through the electrolyte for 8 seconds.
- 14.2 After removal from the holder, the substrate is rinsed in running water of 40°C.
- 14.3 The dried substrate is placed into the furnace used for resistor annealing in an atmosphere of 10% hydrogen 90% argon. A temperature of 300°C is maintained for 15 minutes.

#### 15. ETCHING OF THE CHROMIUM FILM

- 15.1 Preparation of the chromium etch:

1 lb. of  $\text{AlCl}_3 \cdot 6\text{H}_2\text{O}$  is dissolved in 400 ml of water. The density of this solution is 32° Be. By adding 136 g of  $\text{ZnCl}_2$ , the solution density increases to 40° Be. Finally, 30 ml of phosphoric acid are added.

- 15.2 The panel is immersed in this etch, and a zinc pellet is placed in contact with the chromium film to depassivate the surface. The removal of the chromium is usually completed in about 30 sec.
- 15.3 The chromium etch is rinsed off in running water of 40°C.
- 15.4 The panel is rinsed in methanol and dried at 40°C.

#### 16. SURFACE CLEANING

- 16.1 Clean in a saturated solution of sodium bicarbonate in distilled water with ultrasonic agitation for 4 minutes.

- 16.2 Rinse with 5 changes of running water.
  - 16.3 Agitate ultrasonically for 4 minutes in distilled water containing 1 cm<sup>3</sup> of BLAST No. 1\* in 100 cm<sup>3</sup>.
  - 16.4 Rinse with 5 changes of tap water, then 1 change of distilled water.
  - 16.5 Agitate ultrasonically for 4 minutes in distilled water.
  - 16.6 Repeat 16.5 in fresh distilled water.
  - 16.7 Agitate ultrasonically for 4 minutes in Fisher "Spectroanalyzed" methanol.
  - 16.8 Withdraw panel slowly from methanol and let it dry.
17. FIRST SILICON MONOXIDE INSULATOR DEPOSITION
- 17.1 Substrate surface temperature: 350°C.
  - 17.2 Evaporation pressure: below  $1 \cdot 10^{-6}$  torr.
  - 17.3 Evaporation rate: 20 Å/sec., controlled by ionization rate monitor.
  - 17.4 Thickness: 15,000 Å
  - 17.5 Source: Hollow crucible (Drumheller)
  - 17.6 Source to substrate distance: 18 inches.
18. SECOND SILICON MONOXIDE INSULATOR DEPOSITION
- Same procedure as 17.
19. CHROMIUM-COPPER JUMPER DEPOSITION
- Same procedure as in step 5 except for copper film thickness which is 20,000 Å.
20. ELECTRICAL TEST
21. THIRD SILICON MONOXIDE RESISTOR OVERCOAT
- Same procedure as in step 6 except for film thickness which is 10,000 Å.

\*A commercial liquid detergent from Ultrasonics Corporation, Westbury, L. I., N. Y.

22. **CHROMIUM-COPPER CAPACITOR TOP PLATE DEPOSITION**  
Same procedure as in step 5 except for copper film thickness which is 20,000 Å.
23. **ELECTRICAL TEST**
24. **FIRST SILICON MONOXIDE OVERCOAT**  
Same procedure as in step 6 except for film thickness which is 15,000 Å. This covers the capacitor plates.
25. **SECOND SILICON MONOXIDE OVERCOAT**  
Same as Step 24, but using different masks. This covers the horizontal conductor channels.
26. **THIRD SILICON MONOXIDE OVERCOAT**  
Same as steps 24 and 25, but using a different mask. This covers the vertical conductor channels.
27. **ELECTRICAL TEST (Performance)**
28. **TINNING**
- 28.1 Remove oxide from copper lands by immersing panel in Metex for 5-10 sec.
- 28.2 Rinse-off Metex in running water of 40°C.
- 28.3 Rinse in methanol and dry at 40°C.
- 28.4 Apply a thin coat of triethanolamine to the front surface of the film panel.
- 28.5 Pass film panel through the drum solder apparatus at a rate of .32 in./sec. The solder is kept at a temperature of 210°C, and the drum is turning with 22 r. p. m.
- 28.6 After the panel has cooled down to room temperature, it is immersed in fresh methanol three times, and the surfaces are wiped clean with a rubber policeman.
29. **ELECTRICAL TEST (Ground-to-Voltage insulation resistance)**

**30. TRANSISTOR ATTACHMENT**

- 30.1 The gold plated Kovar leads of the 56 transistors to be attached are preformed and trimmed. No tinning is necessary.
- 30.2 The front surface of the positioning fixture is coated with a thin layer of n-dodecyl alcohol.
- 30.3 The preformed transistors are loaded into the positioning fixture.
- 30.4 Both surfaces of the panel are coated with a thin film of triethanolamine.
- 30.5 Insert panel into positioning fixture and register the tinned lands on the panel to the transistor leads.
- 30.6 The completed assembly is placed on a heat reservoir kept at 230°C by a hot plate. To insure uniform pressure on all the leads, a force of about 40 lbs. is applied to the back of the positioning fixture.
- 30.7 After about 60 sec., the assembly is removed from the heat reservoir and placed on a cold metal plate.
- 30.8 As soon as the solder has solidified, the panel with the transistors attached to it is taken out of the positioning fixture.
- 30.9 The panel surface is cleaned as in Step 28. 6.

**31. ELECTRICAL TEST (Performance)**

**32. FIRST CONFORMAL COATING**

- 32.1 The panel is placed into a vapor degreaser containing boiling isopropanol for 15 minutes.
- 32.2 A coat of Sylkyd No. 1400\* is applied with a brush on the panel surface.
- 32.3 The varnish is left to dry in air overnight and then baked at 150°C for 1 hour.

\*A silicone varnish from Dow Corning Corporation.

33. ELECTRICAL TEST (Performance)

34. MOUNTING AND FRAMING

Two panels with a core of plastic material between them are to be prepared in the following manner.

34.1 PREPARATION OF CORE

34.1.1 Equal weights of DER 334\* and Versamid 125\*\* are mixed and stirred together.

34.1.2 100 g of this resin are mixed with 30 g of Eccospheres SI\*\*\*.

34.1.3 This mixture is poured on a metal surface and cured at 85°C for 1 hour to yield sheets about .100 in. thick.

34.1.4 The sheets are machined down to about .035 in. thickness and cut to the size of the substrate.

34.2 PREPARATION OF PANELS

34.2.1 Preparation of adhesive:

Approximately 10 g of Versamid 125 and an equal amount of DER 334 are heated separately to 100°C for 5-10 minutes, then poured together and mixed thoroughly.

34.2.2 Both panels and the core are heated under an infra-red lamp. The warm adhesive is painted on the back surfaces of both panels and on both sides of the core while they are warm.

NOTE: Care must be taken to avoid spreading of the adhesive to the front surfaces of the panels. Masking of these surfaces with an adhesive tape is recommended.

34.2.3 The panels and the core are placed into the assembly fixture, where the edges are automatically aligned by means of pins. The entire assembly is heated in an oven of 85°C for 1 hour. During this period, a force of approximately 1 lb. is applied to the assembly.

\*An epoxy resin from Down Chemical Company

\*\*A polyamide resin from General Mills, Incorporated

\*\*\*Thin walled hollow silica spheres of 30-125  $\mu$  diameter from Emerson and Cuming, Incorporated, Canton, Mass.

34. 2. 4 After curing, the masking tape and excess adhesive along the edges are removed. Then, the laminated panels are cleaned by rinsing in acetone and wiping the surfaces with cotton swabs. Finally, the panels are put into a vapor degreaser with boiling isopropanol for no longer than 10 minutes.

### 34. 3 FRAMING

34. 3. 1 The grooves of the frame are coated with the adhesive described in 34. 2. 1.

34. 3. 2 The laminated panels are inserted into the grooves of the frame.

34. 3. 3 The Amphenol connector\* is put into the frame and secured by two rivets.

34. 3. 4 The adhesive in the frame is cured at 85°C for 1 hour.

34. 3. 5 The connector pins are individually soldered to the copper edge lands of the panels.

### 34. 4 ELECTRICAL TEST (Performance)

### 34. 5 FILLING OF THE CONNECTOR

34. 5. 1 The framed panels are put into a vapor degreaser with boiling isopropanol for no longer than 10 minutes.

34. 5. 2 Preparation of filling material.

100 g of Epon 828\*\*, 4 g of Pigment Hysol 5606B\*\*\*, and 12 g of Curing Agent D\*\*\*\* are thoroughly mixed.

34. 5. 3 This mixture is filled into the space between connector and panel surface to cover the pins where they are soldered to the edge lands.

\*A plastic multiple pin connector made by Amphenol-Borg Electronics Corporation, Broadview, Ill.

\*\*An epoxy resin made by Shell Chemical Company

\*\*\*Pigment material made by Hysol Corporation

\*\*\*\*Product of Shell Chemical Company

34.5.4 The framed panels are put under an infra-red lamp until the filler has assumed a jelly-like state.

35. SECOND CONFORMAL COATING

35.1 The entire assembly is dipped into Sylkyd No. 1400. The excess of the varnish is allowed to drip off. Furthermore, the varnish film is wiped off the metal frame surface. To evaporate the solvent, the assembly is placed under an infra-red lamp for about 1 hour.

35.2 With the assembly in a horizontal position, the varnish is cured in air at 150°C for 16 hours. This step also completes the curing of the filler.

36. FINAL ELECTRICAL TEST (Performance)

## SECTION 5

### OVERALL CONCLUSIONS

#### 5.1 Phase I (Integration Techniques)

1. A satisfactory method for rapidly and reliably attaching functional devices such as transistors and diodes to evaporated multilayer circuit panels has been developed. The method includes several process steps for which individual conclusions have been reached.
  - a. A solder tinning method for tinning the evaporated copper lands prior to attaching functional devices has been developed.
  - b. A special jig for positioning 56 functional devices in registration with evaporated lands on thin film circuit panels has been fabricated and successfully used.
  - c. A solder reflow method has been developed for simultaneously attaching 56 functional devices to thin film circuit panels. This method has been found to be superior to spot soldering and heated gas jet soldering.
2. Solder joints formed by use of the solder tinning and batch solder reflow techniques can successfully withstand high shock (600 g's) and vibration (2000 cycles at 55 g's) environments.
3. Temperature cycling (-55 to +85°C), and high humidity (95%) conditions have not shown detrimental effects on the solder joints.

#### 5.2 Phase II (Process Controls)

1. Surface requirements for acceptable substrates have been established (Section 4. 2. 2).
2. Cermet (Cr-SiO) resistors are more stable and more easily fabricated than nickel-chromium resistors.
3. A satisfactory process has been developed to simultaneously deposit 224 cermet resistors over a 2.5" by 3.5" area consistently within  $\pm 10\%$  of the design value.

4. A pattern etching technique for film conductors has been developed which significantly reduces the number of evaporation steps required to fabricate complex interconnection patterns.
5. Process parameters have been established for the deposition of short free silicon monoxide insulation.
6. Arc Eroded metal masks are superior to glass masks for repetitive patterns, such as resistors.

### 5.3 Phase III (Functional Assemblies)

1. A complete process has been developed for the fabrication of complex electronic assemblies having parts densities of approximately 600,000 components per cubic foot, which meet military environmental specifications. The process includes steps developed under Phase I and Phase II in addition to those specifically developed under Phase III. Conclusions pertaining to these particular items are given below.
  - a. Packaging techniques have been developed which enable thin film circuit substrates to meet high shock (600 g's) and vibration (2000 cycles at 55 g's) requirements.
  - b. A conformal coating has been selected which provides additional environmental protection to the functional assemblies.
  - c. Functional assemblies will successfully operate after being subjected to military environmental tests.

## SECTION 6

### RECOMMENDATIONS

Since an acceptable process has been developed for the fabrication of complex thin film electronic assemblies using attached discrete active elements, further efforts should now follow in two directions (1) improvements to the present package and early application in military equipment, and (2) continued process refinement and development, particularly in the area of thin film active elements, to provide a fully optimized microminiature electronic technology capable of meeting all military requirements.

Specifically, the following recommendations are made.

1. The number of circuits on a thin film integrated functional assembly should be reduced to minimize the number of different panel types required to construct a particular piece of equipment. Panels containing 32 circuits per substrate are already in use and appear more favorable.
2. Component densities should be increased to provide increased microminiaturization and to reduce costs. Fabrication costs are based on the surface area coated per evaporation, and therefore, the costs per circuit can be reduced by including more circuits per evaporation area.
3. Thin film circuit panels containing digital circuitry should utilize a universal interconnection grid to minimize the number of different evaporation masks required to form complex interconnection networks. Techniques have already been established along these lines, however, further improvements and refinements are required to provide an optimized pattern.
4. Process steps should be developed for the attachment of semiconductor chip devices to thin film circuit assemblies. These devices which will offer for several years significant performance advantages over thin film active elements, will allow reductions in size and cost of present thin film assemblies, and permit the use of packaging techniques which provide increased reliability. Initial investigations suggest that the solder reflow method of attaching functional devices to thin film circuits, which was developed under this contract, could be easily modified to include semiconductor chip attachment as well. By using chip active elements to replace the presently used hermetically sealed devices, unit throw away costs could be substantially reduced, allowing the use of heavy potting to provide the thin film panels with additional moisture resistance.

5. Connector designs for thin film circuit panels must be improved to increase reliability and reduce size.
6. Further studies are required to develop and test improved conformal coatings to provide long term environmental protection for thin film panels.
7. Prototype equipment for the semi-automatic production of thin film circuit panels is presently undergoing initial evaluation. This equipment should be optimized and its processing rate increased to improve yields and reduce costs. Studies should be conducted to determine the necessary process controls and evaporation techniques to be utilized, as well as developing supplementary processes and equipment which are necessary to augment the basic evaporation technology.
8. To establish an overall capability to produce microminiature electronic equipment meeting military requirements, developments in peripheral areas such as power supplies, memories, analog to digital converters, and output equipment must keep pace with the miniaturization achieved in digital and communication type circuitry. To meet this objective, parallel studies in these areas should be conducted.
9. To provide a fully optimized thin film technology capable of meeting all military microelectronic goals, research and development activities must be continued in the area of thin film active elements.

## SECTION 7

## KEY TECHNICAL PERSONNEL

During the final quarter, the following personnel took part in the work covered by this report.

TABLE 7-1

## KEY TECHNICAL PERSONNEL

<u>Name</u>	<u>Title</u>	<u>Man Hours Contract Funded</u>	<u>Man Hours IBM Funded</u>
W. N. Carroll	Senior Engineer	72	
D. C. Wheeler	Associate Engineer	168	314
K. B. Scow	Staff Engineer	221	392
F. L. Stutz	Project Engineer	80	326
F. S. Maddocks	Staff Engineer		400
E. C. Hallee	Jr. Engineer		395
P. S. Schlemmer	Associate Engineer		392
P. C. Karr	Staff Engineer		160
R. Glang	Advisory Physicist		352
A. E. Lessor	Senior Chemist	—	<u>40</u>
Technical Personnel		541	2771
			<u>2753</u>
			5524
Funded 1st Quarter		950	
Funded 2nd Quarter		994	
Funded 3rd Quarter		<u>903</u>	
Total Key Personnel Man Hours		3388	

RESUME - Dr. R. Glang

Dr. R. Glang is manager of Materials and Process Development, Film Electronics Department. He is responsible for the refinement of existing processes and the development of new materials and processes for thin film passive components. He graduated as a Diplom Chemist from the University of Greifswald, Germany, in 1952. In 1955 he received the doctorate in Physical Chemistry from the Technische Hochschule Darmstadt, Germany. He became a group leader at the Degussa Metal Research Laboratory, Hanau, Germany, in 1956, where he investigated new refining methods for platinum metals and a fabrication process for pure silicon. In 1958, he joined Diamond Ordnance Fuze Laboratories, in Washington, D. C. Here, he was responsible for processing germanium from zone purification to pn-junction fabrication and the related materials analyses. Dr. Glang joined IBM in January 1960 and participated in the development of epitaxial growth processes for silicon. Subsequently, he investigated the vacuum evaporation of semiconductor compound films. He is a member of the Electrochemical Society.

RESUME - Mr. F.S. Maddocks

Mr. Maddocks graduated from Northeastern University, Boston, Massachusetts in 1952 with a B.S. degree in chemistry. From 1953 to 1958 he was employed by the M. I. T. Lincoln Laboratory, where he worked until 1956 on the development of ferrite computer memory cores and from 1956 to 1958 on the development of evaporated nickel-iron films for computer memory applications.

Mr. Maddocks came to IBM Federal Systems Division in 1958 where he continued work on development of evaporated nickel-iron films. Since 1960, he has been engaged in the development of circuit components for room temperature evaporated film computers. His most recent assignment has been the development of techniques for photo-etching conductor patterns on evaporated copper films.

Mr. Maddocks is the co-author of three published papers on evaporated metal and dielectric films, and is co-inventor of three inventions on file for patents. The most recent of these was filed in January, 1963, and concerns improvements to photo-etched copper conductor patterns by an electro polishing technique.

RESUME - Mr. P.S. Schlemmer

Mr. Schlemmer is responsible for the test and evaluation of thin film components and the logic test of thin film circuit panels. He received a BSEE degree from the Pennsylvania State University in 1957 and matriculated in the SAGE I Systems school after joining IBM. He has engaged in the design of logic circuits including the development of high speed tunnel diode circuits as a member of the Exploratory Circuits Development Group. He has also had considerable experience in the specification, selection, evaluation and application of semiconductors and other electronic components to digital computers such as the RELIABILITY TEST ASSEMBLY and the FIELD DATA INFORMER.

## SECTION 8

### REFERENCES

1. Behrndt, K. H., and Love, R. W., "Control of Deposition Rate and Film Thickness with the Crystal Oscillator".
2. Giedd, G. R., and Perkins, M. H., "Evaporation Rate Monitor", Rev. Sci. Instr., Vol. 31, July 1960.
3. Thin Film Production Technique, Final Report, June 15, 1961 to October 31, 1962, Contract N163-9142(x), U. S. Naval Avionics Facility, Indianapolis, Indiana.
4. Drumheller, C. E., "Silicon Monoxide Evaporation Techniques", Proceedings of the 7th National Symposium, American Vacuum Society, October 1960.
5. Perkins, M. H., "An Evaporation Rate Control System Employing a Heated Electrode Sensing Gauge", American Vacuum Society, 8th National Vacuum Symposium, 1961.
6. Holland, L., "Vacuum Deposition of Thin Films", p. 142, J. Wiley, 1936.
7. Knudsen, M., "Ann. Phys.", 1p2 28 (1909), 999.
8. Mayer, M., "Z. Phys", 52 (1928) 235.
9. Siddal, G., "Vac. Deposition of Dielectric Films for Capacitors", Vacuum, Vol. 9, No. 5/6, 1960.

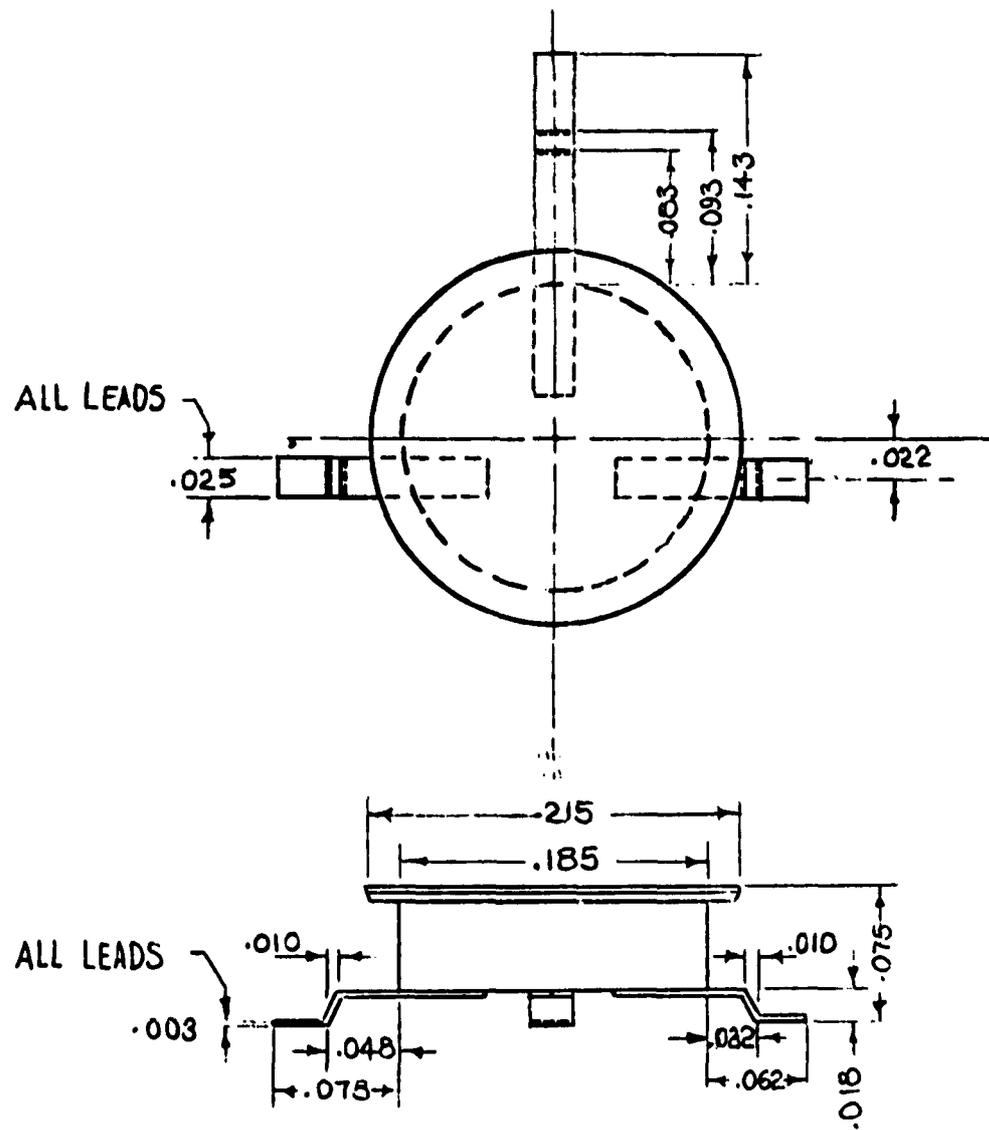


Figure 4-1: Configuration of Functional Device

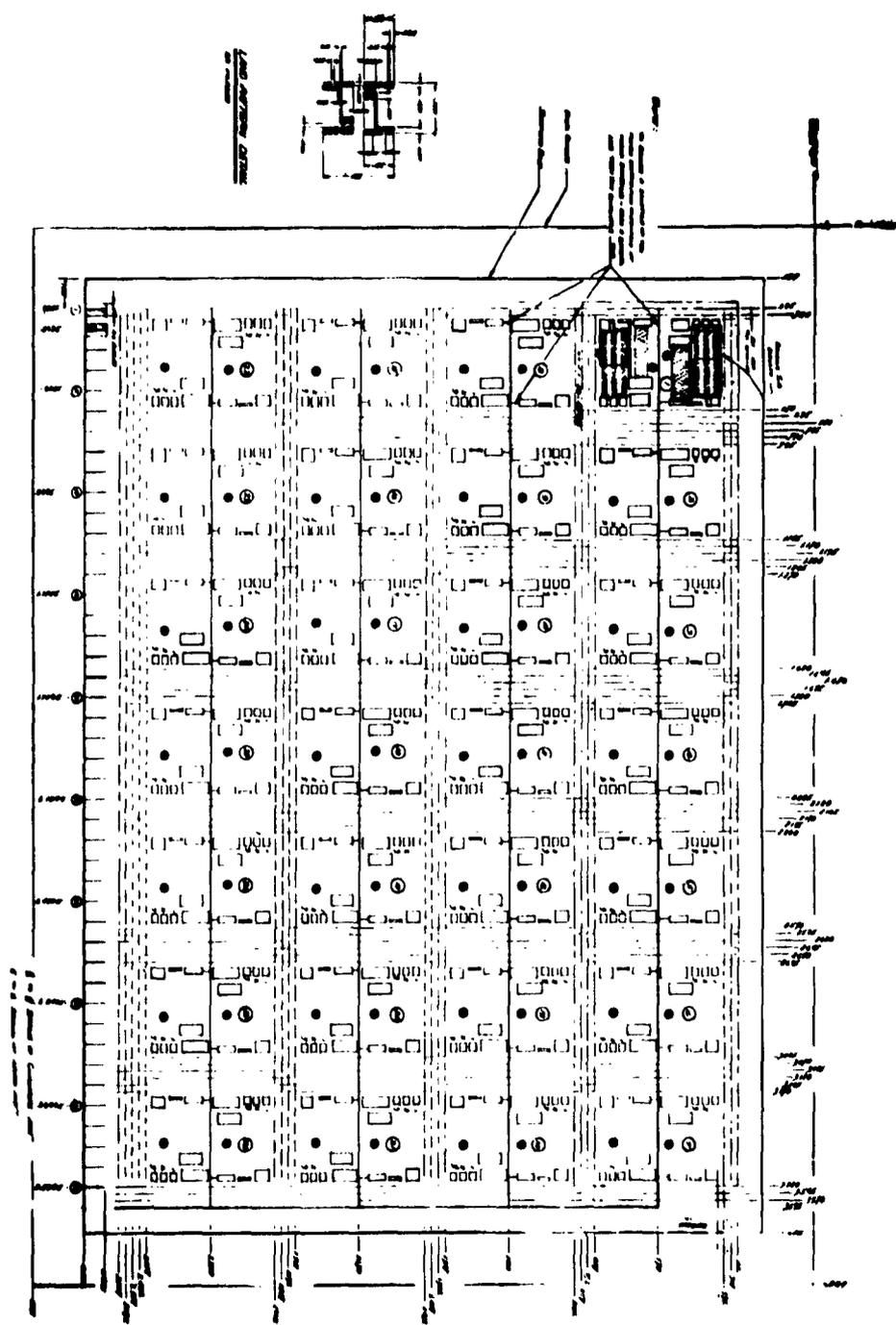


Figure 4-2: Multilayer Panel Land Arrangement

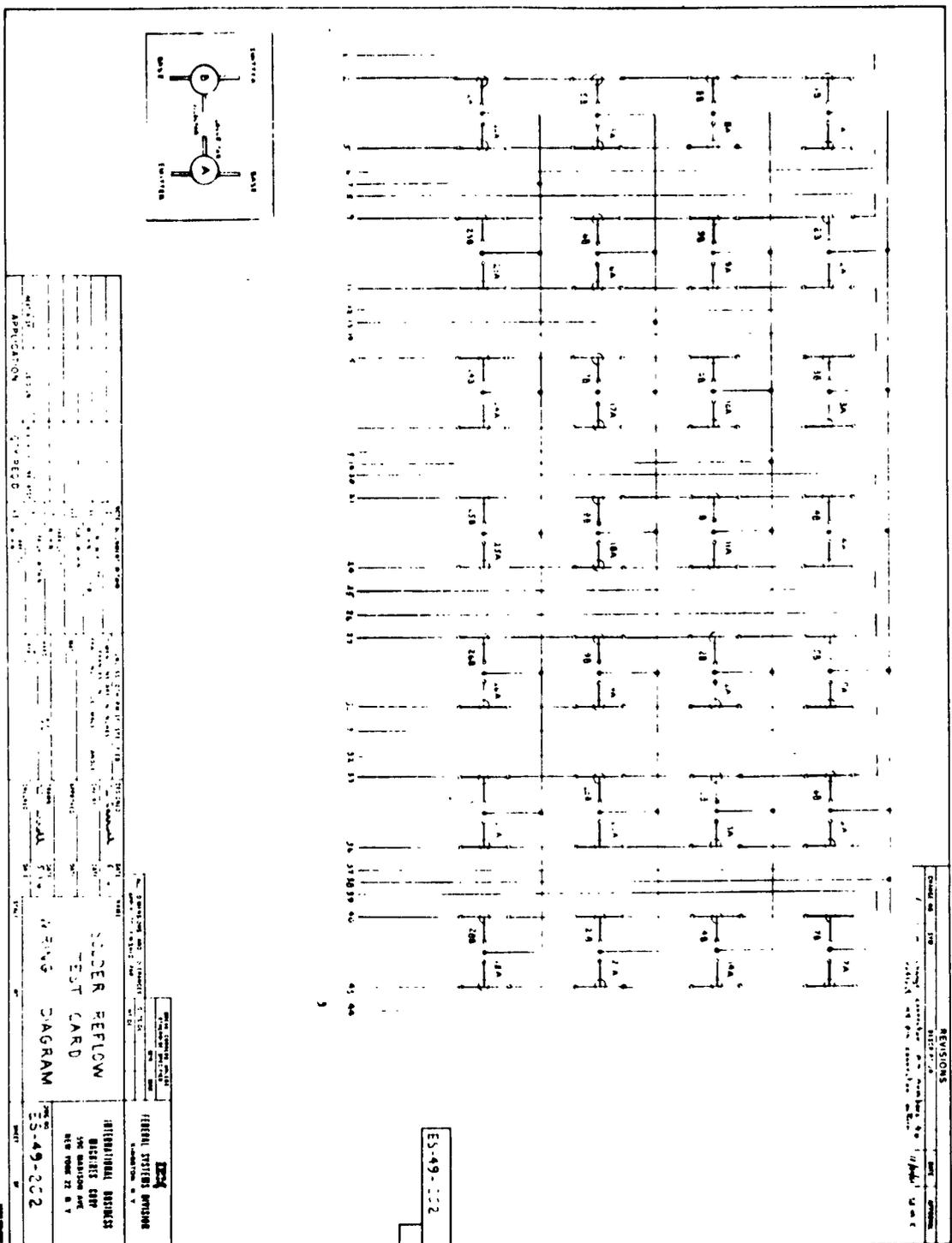


Figure 4-3: Schematic Diagram For Test Assembly

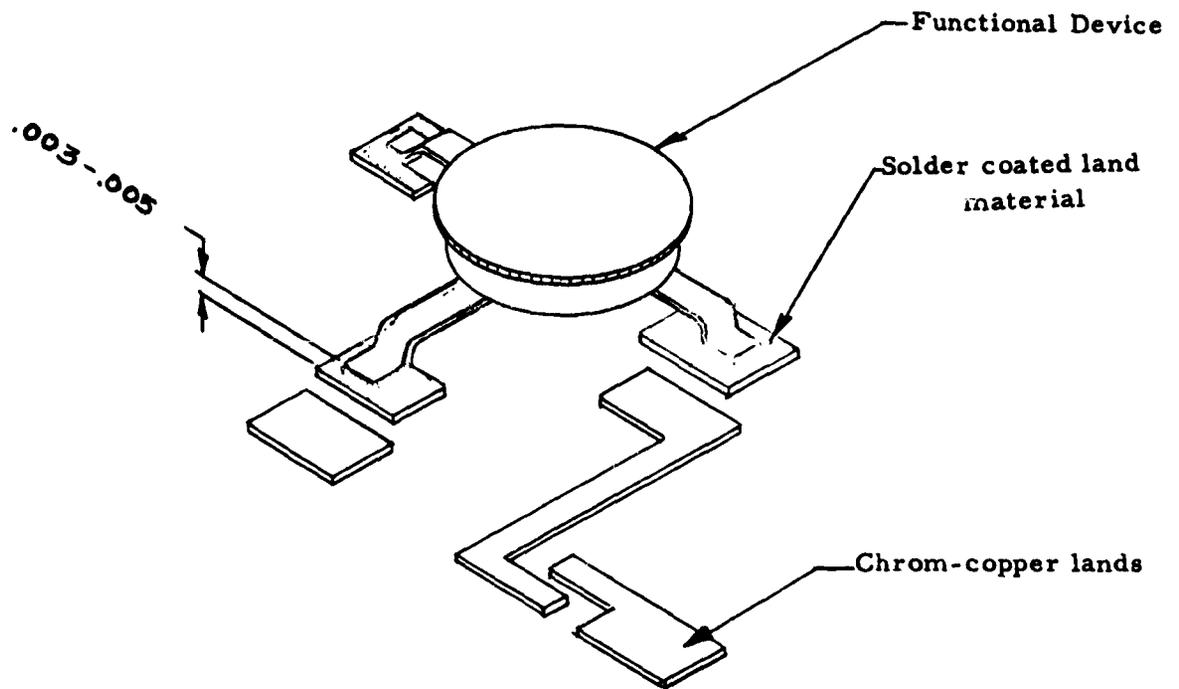
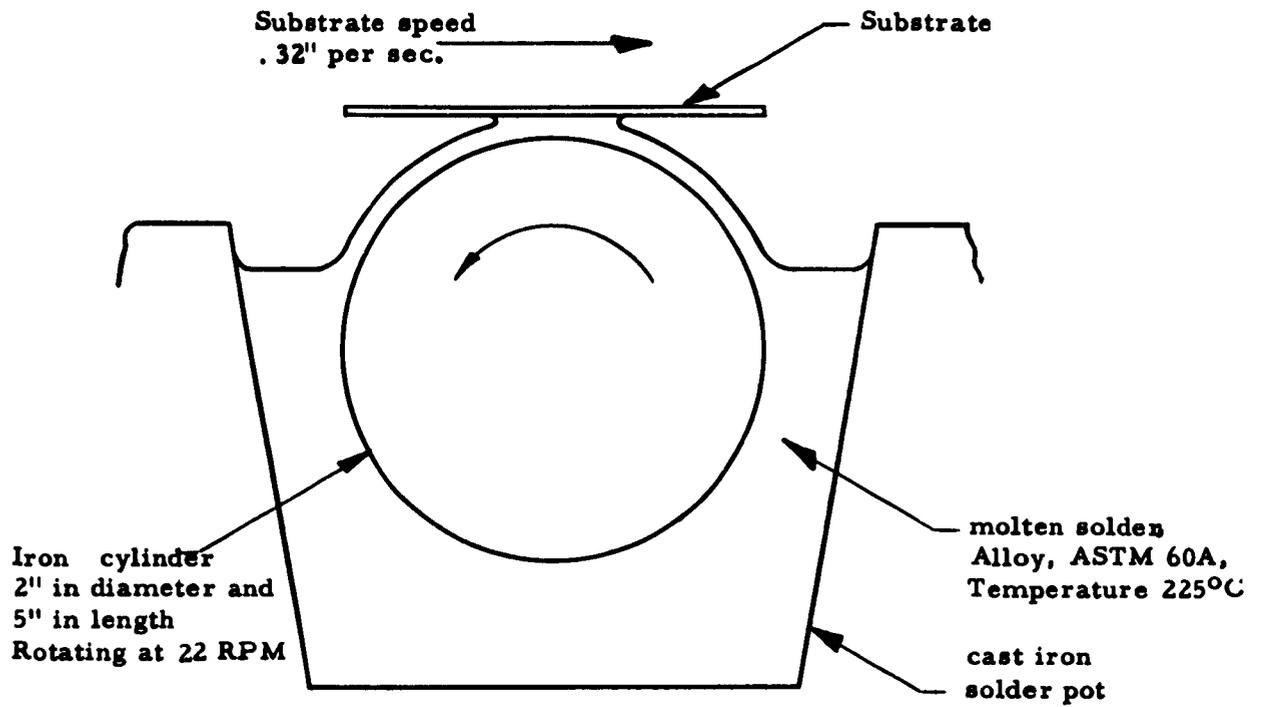


Figure 4-4  
Diagram Showing Solder Joint Geometry



**Figure 4-5: Schematic of Molten Solder Technique**



Figure 4-6: Aluminum Substrate Holder

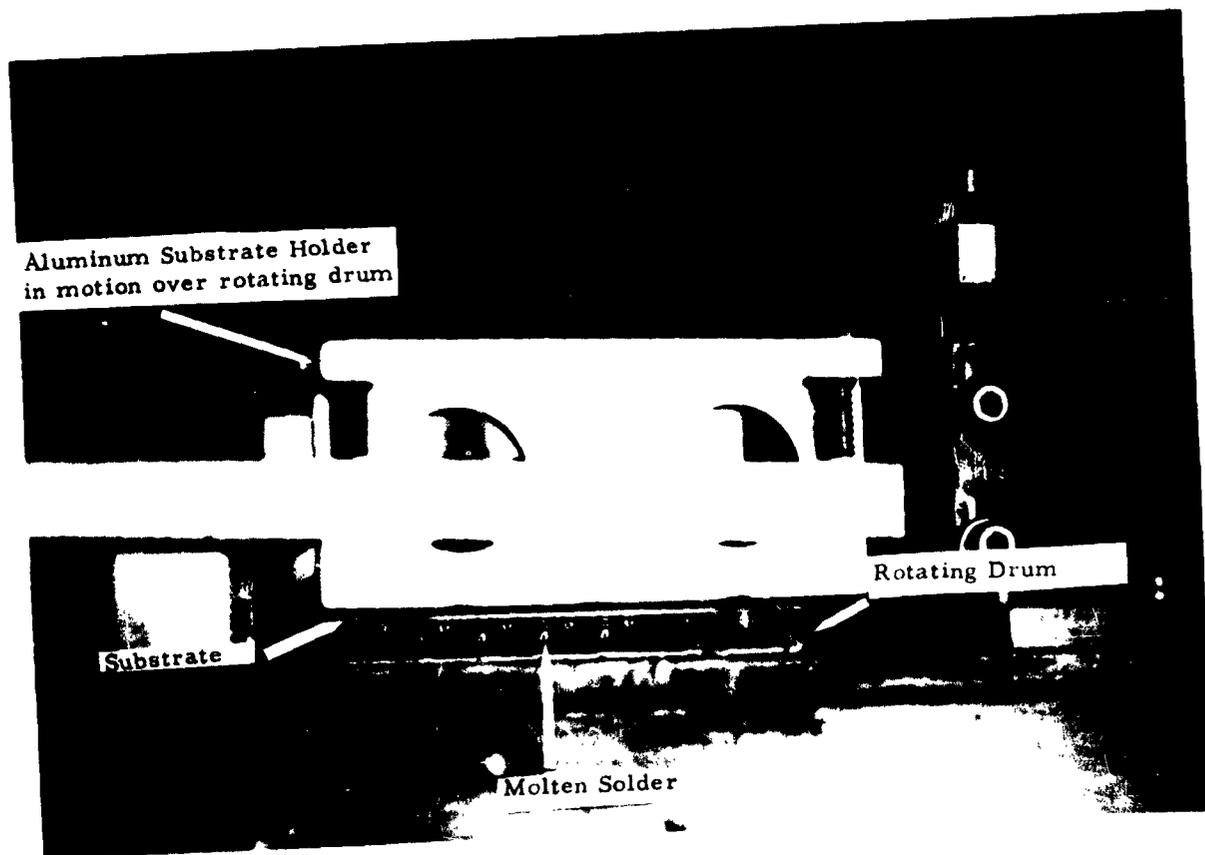


Figure 4-7  
Photograph of Panel in Motion Over  
Solder Drum



Figure 4-8: Evaporated chromium-copper lands before and after pretinning with the rotating drum.

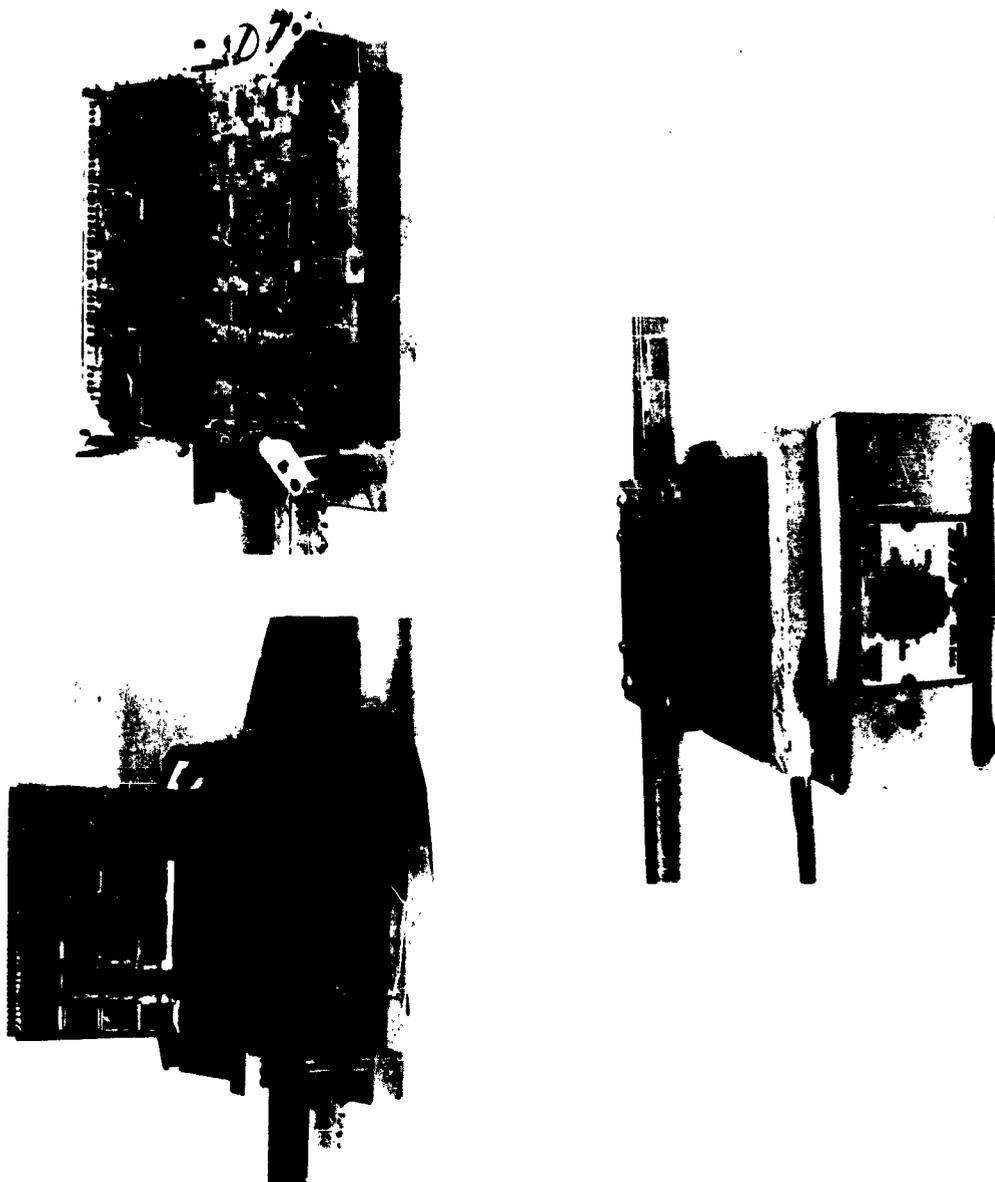
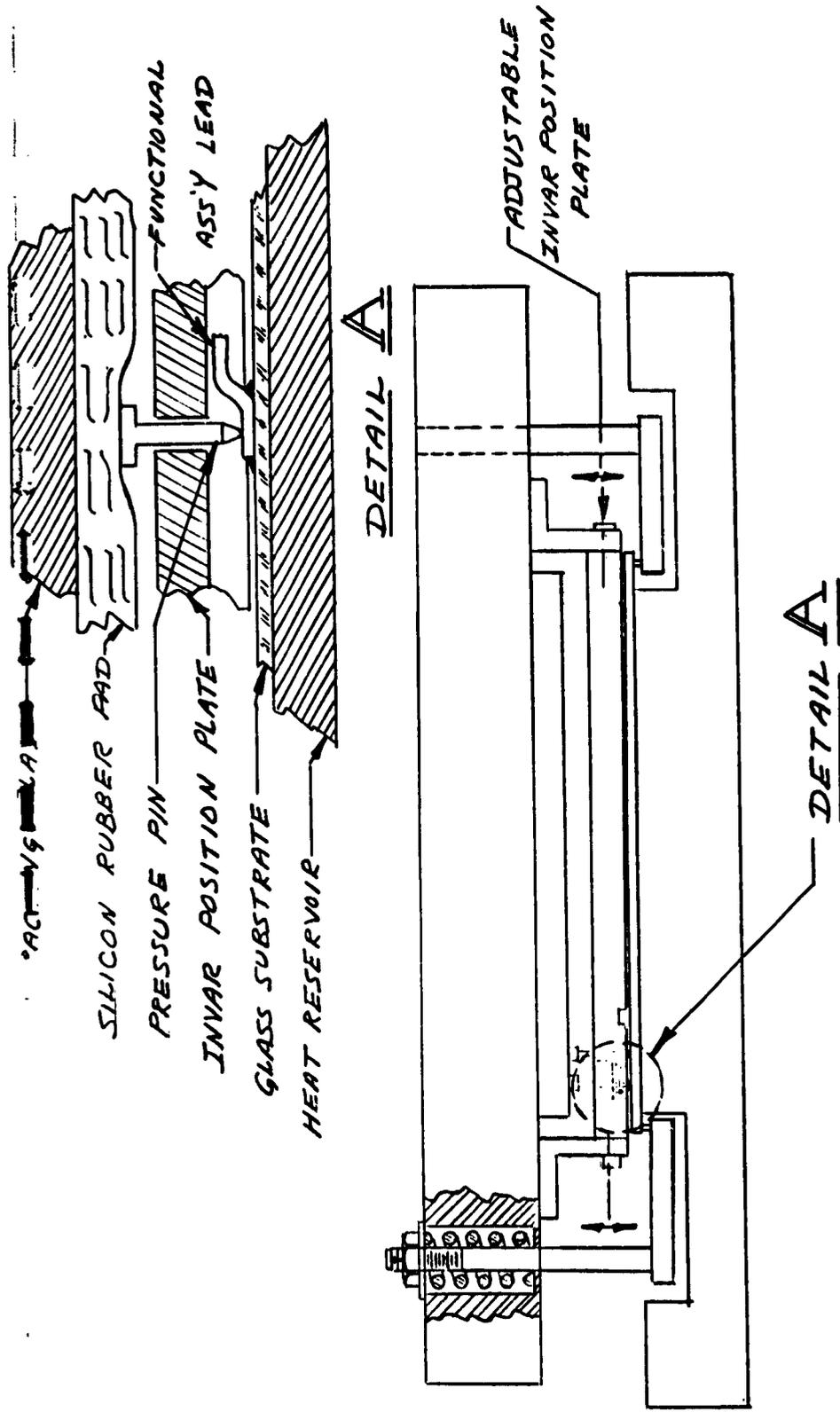
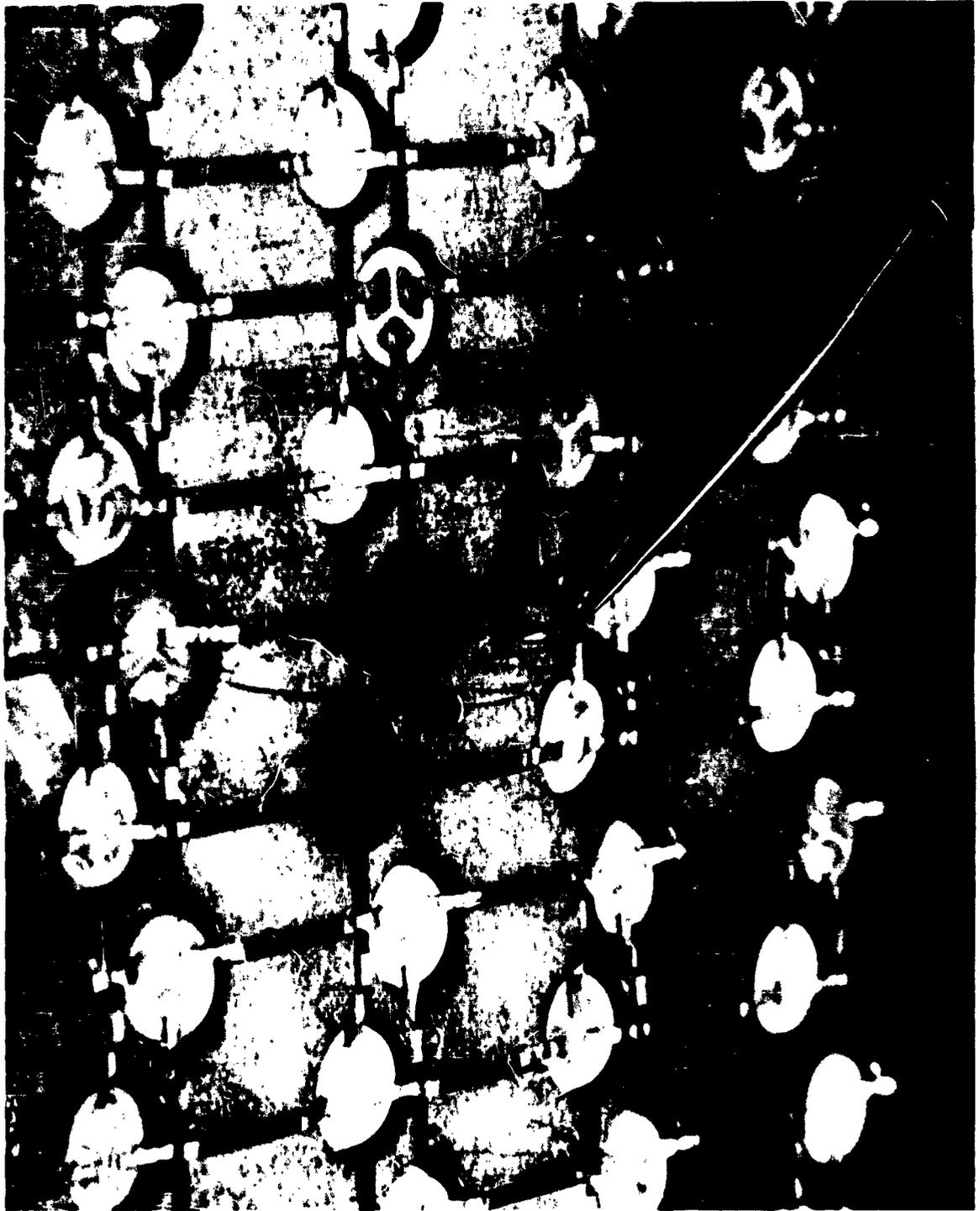


Figure 4-9: Pictorial Drawing of Attached Functional Device

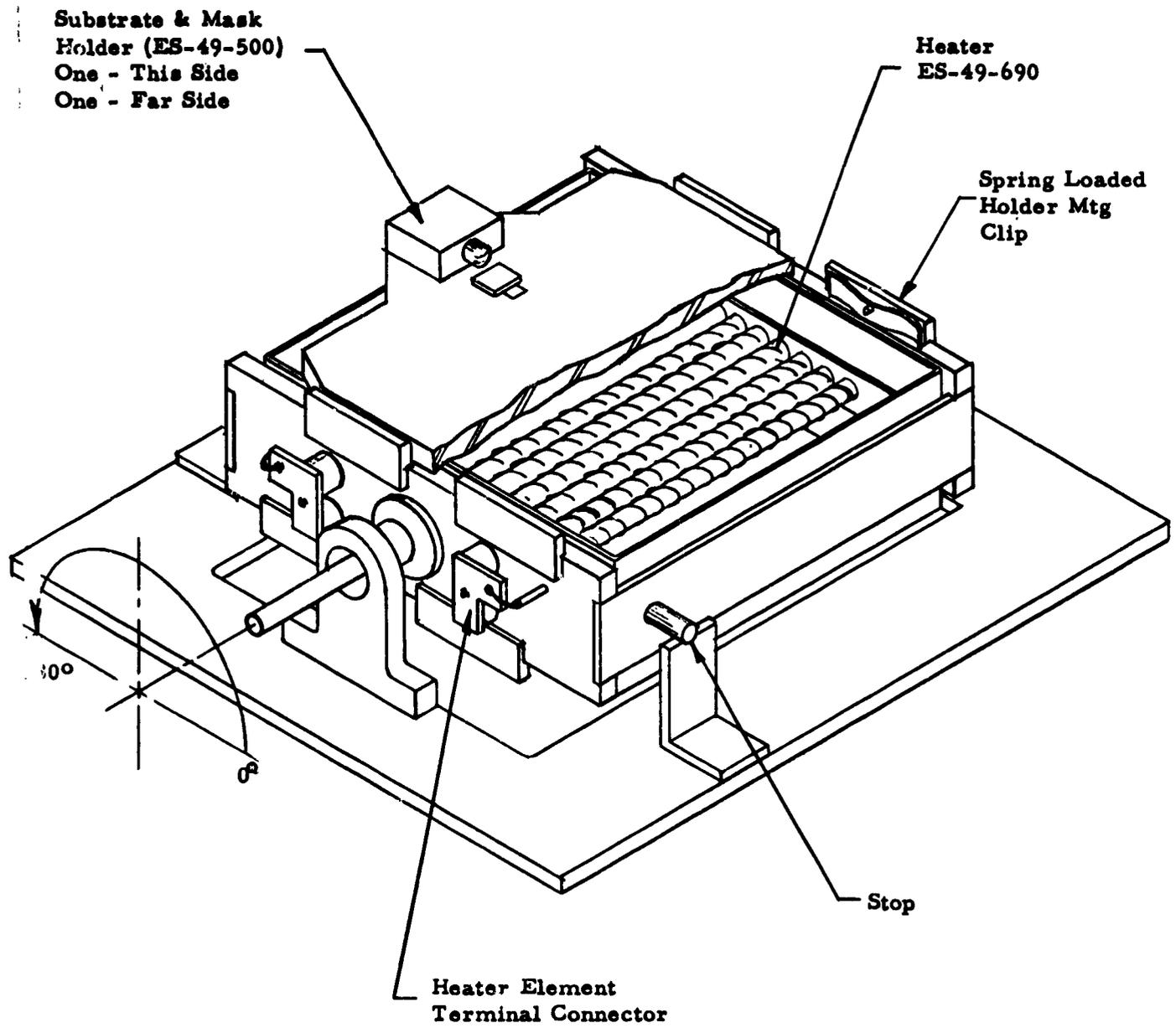


FUNCTIONAL ASSEMBLY POSITIONING FIXTURE &  
 HEAT RESERVOIR FIG 4-10

NO SCALE



**Figure 4-11: Close Up of Functional Device Positioning Unit  
and Heat Reservoir**



**ROTATING SUBSTRATE HOLDER-RESISTOR**

Figure 4-12:

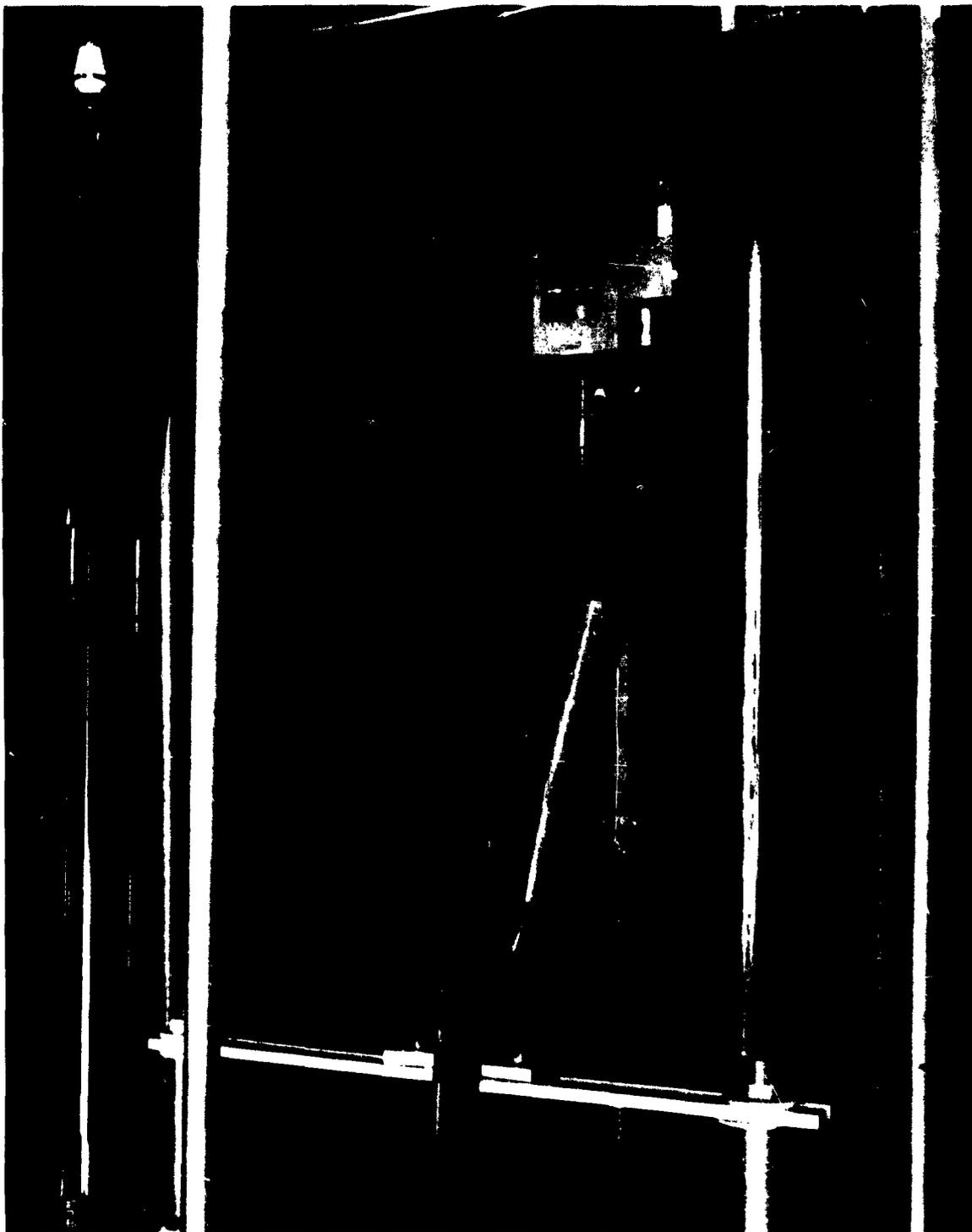


Figure 4-13: Powder Feed Source Arrangement

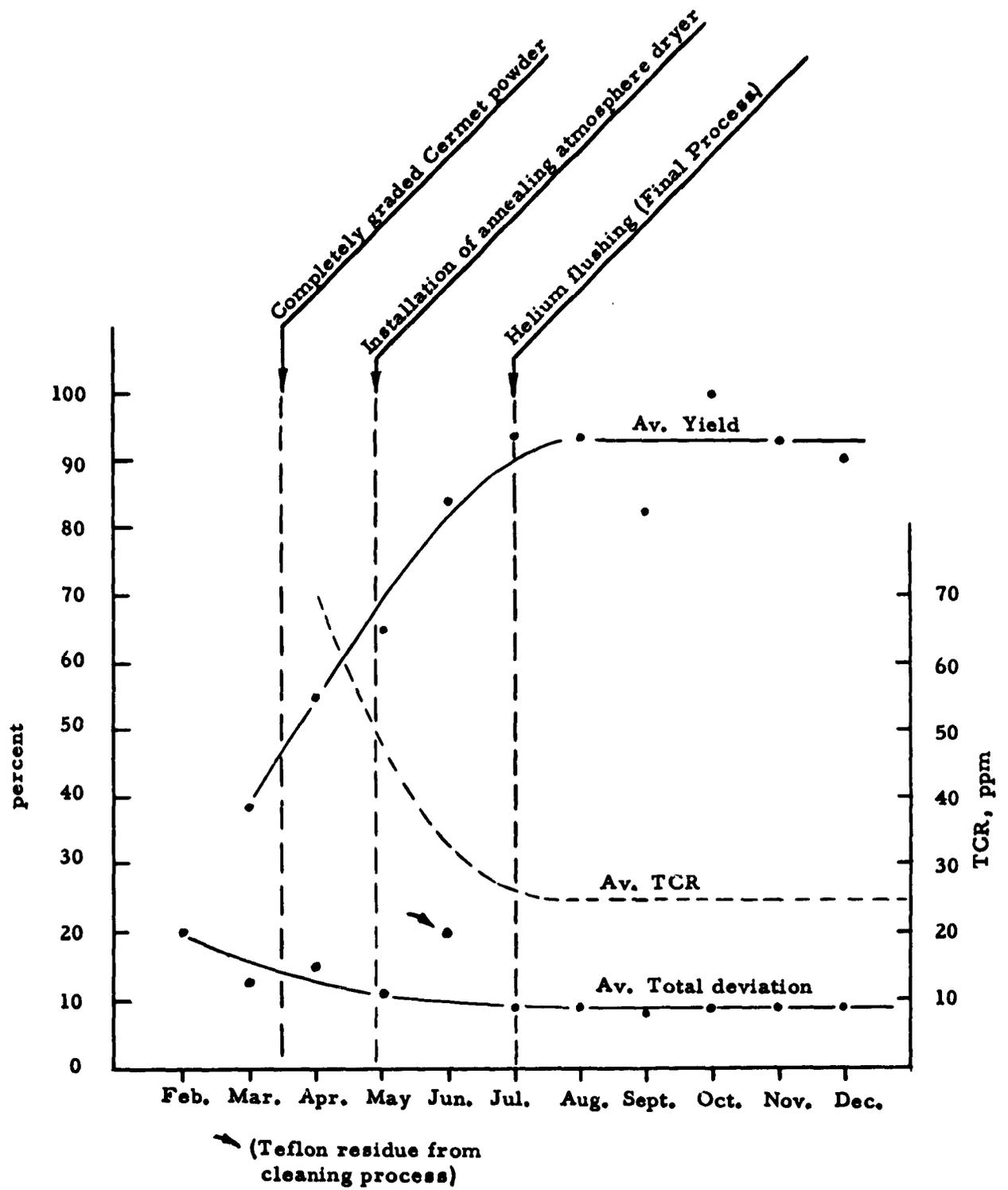


Figure 4-14: Effects of Process Changes on Resistor Quality.

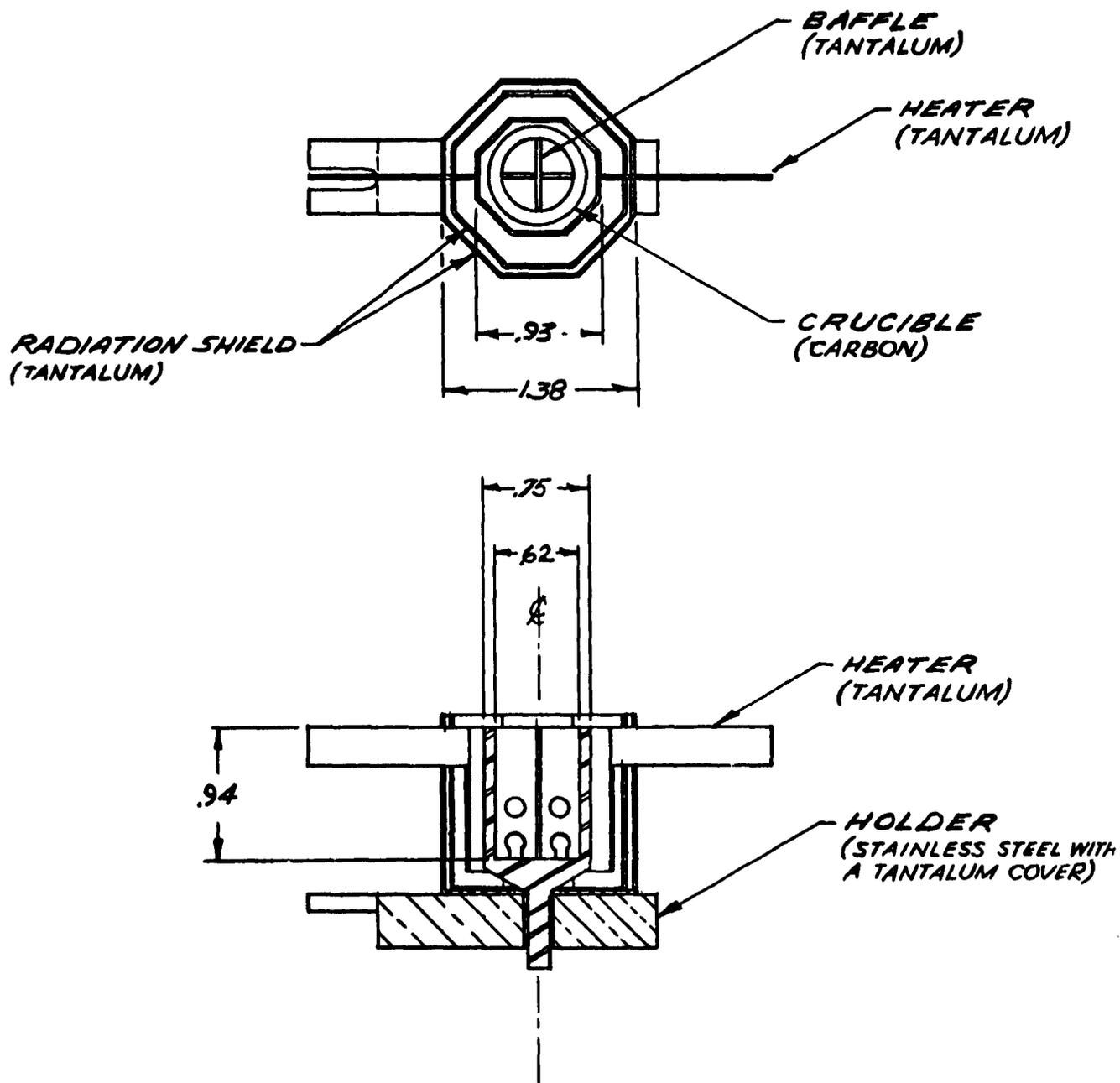
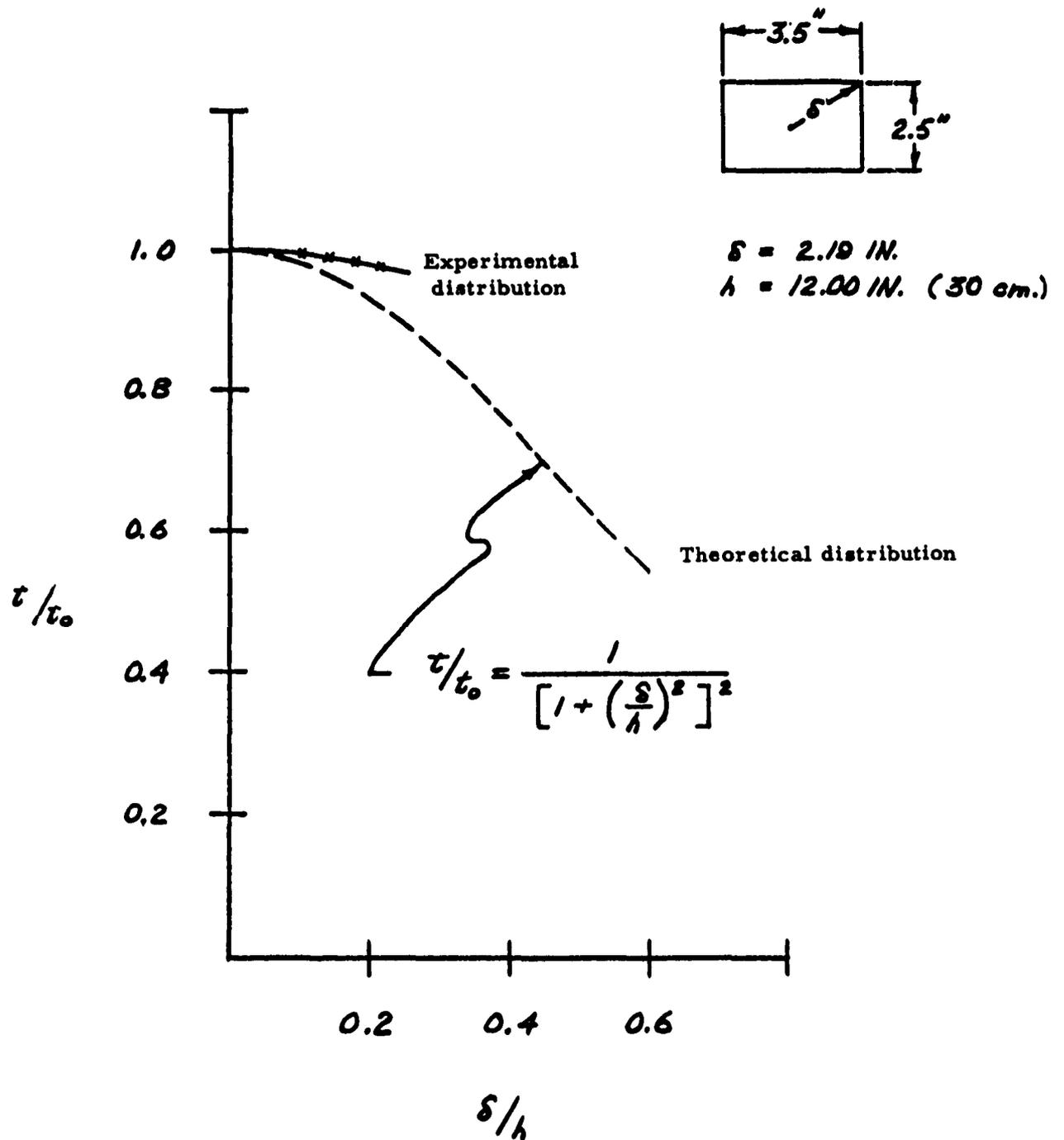
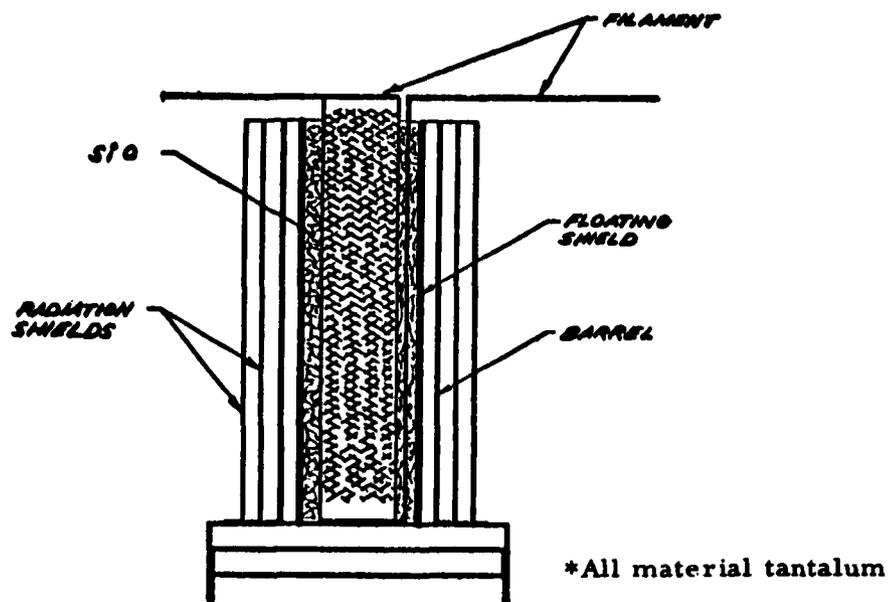


Figure 4-15: Tantalum Baffled Carbon Crucible Source



FILM THICKNESS DISTRIBUTION

FIG. 4-16



**Figure 4-17: Hollow Crucible Source with Floating Shield.**

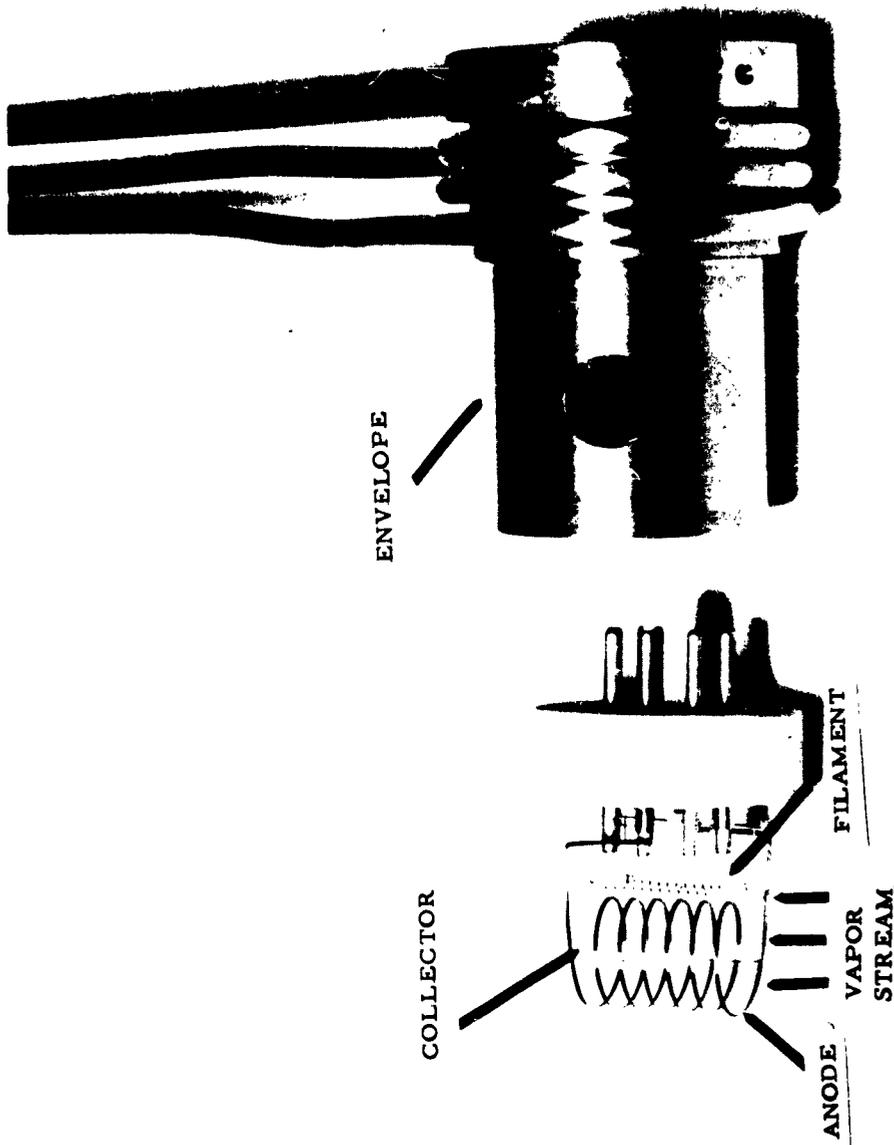


Figure 4-18: Evaporation Rate Monitor Sensing Element

Figure 4-19: TRL Circuit Configuration

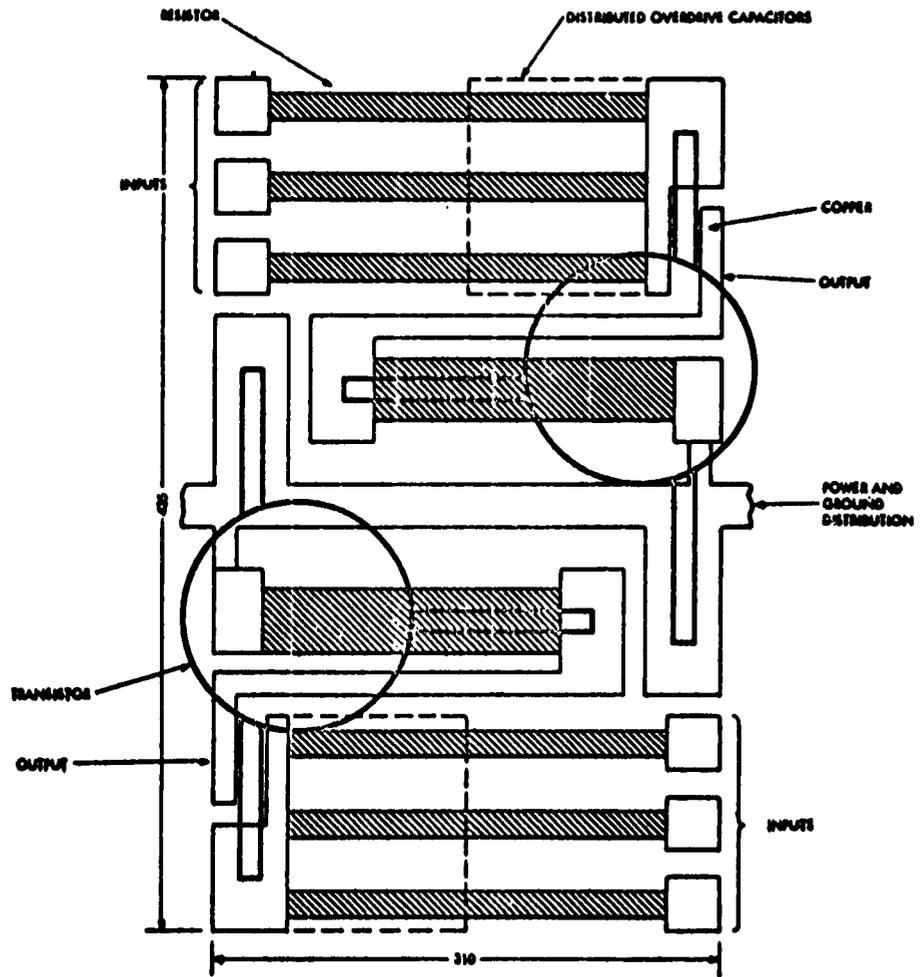
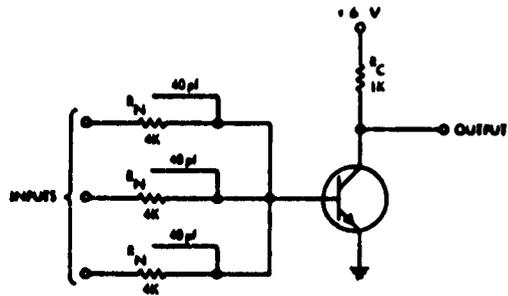


Figure 4-20: Basic TRL Circuit Layout

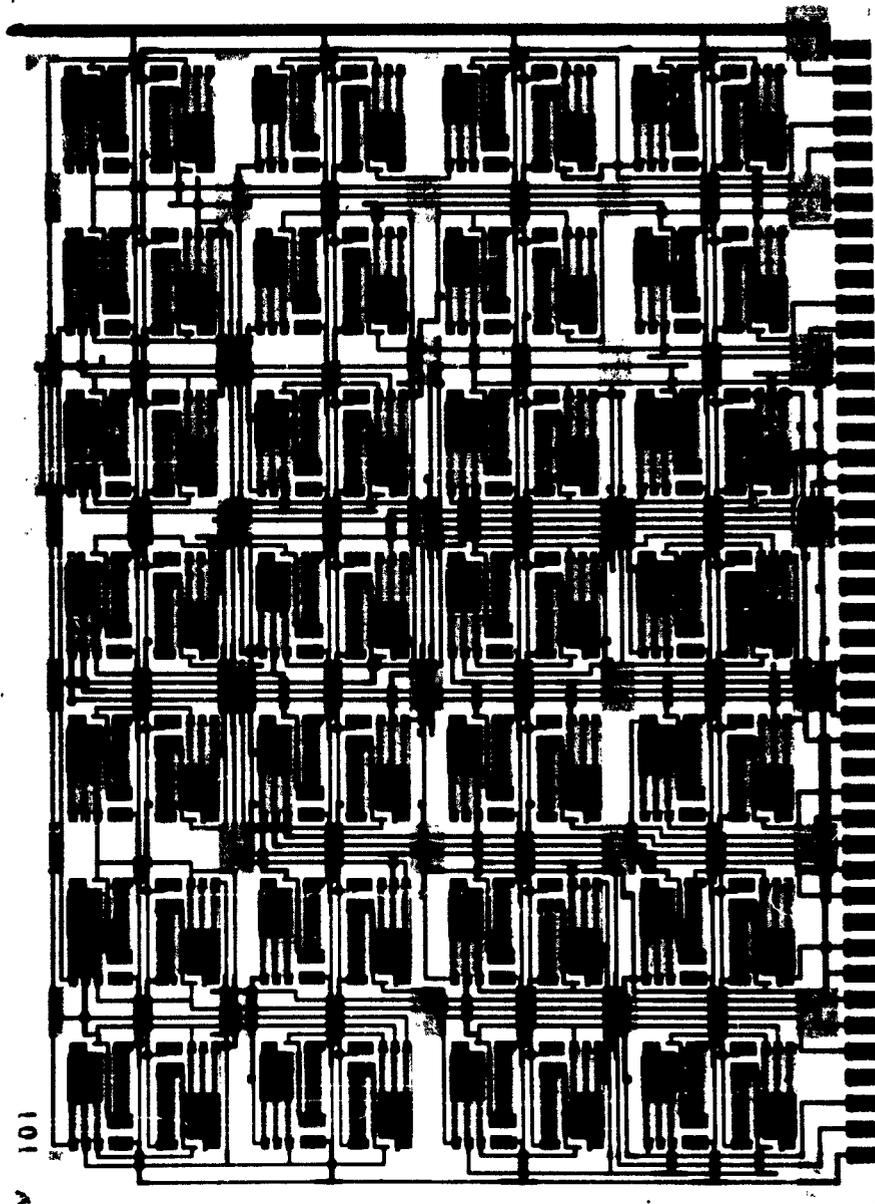


Figure 4-21: Film Panel Layout  
Evaporation etched-3.5" x 2.5" panel

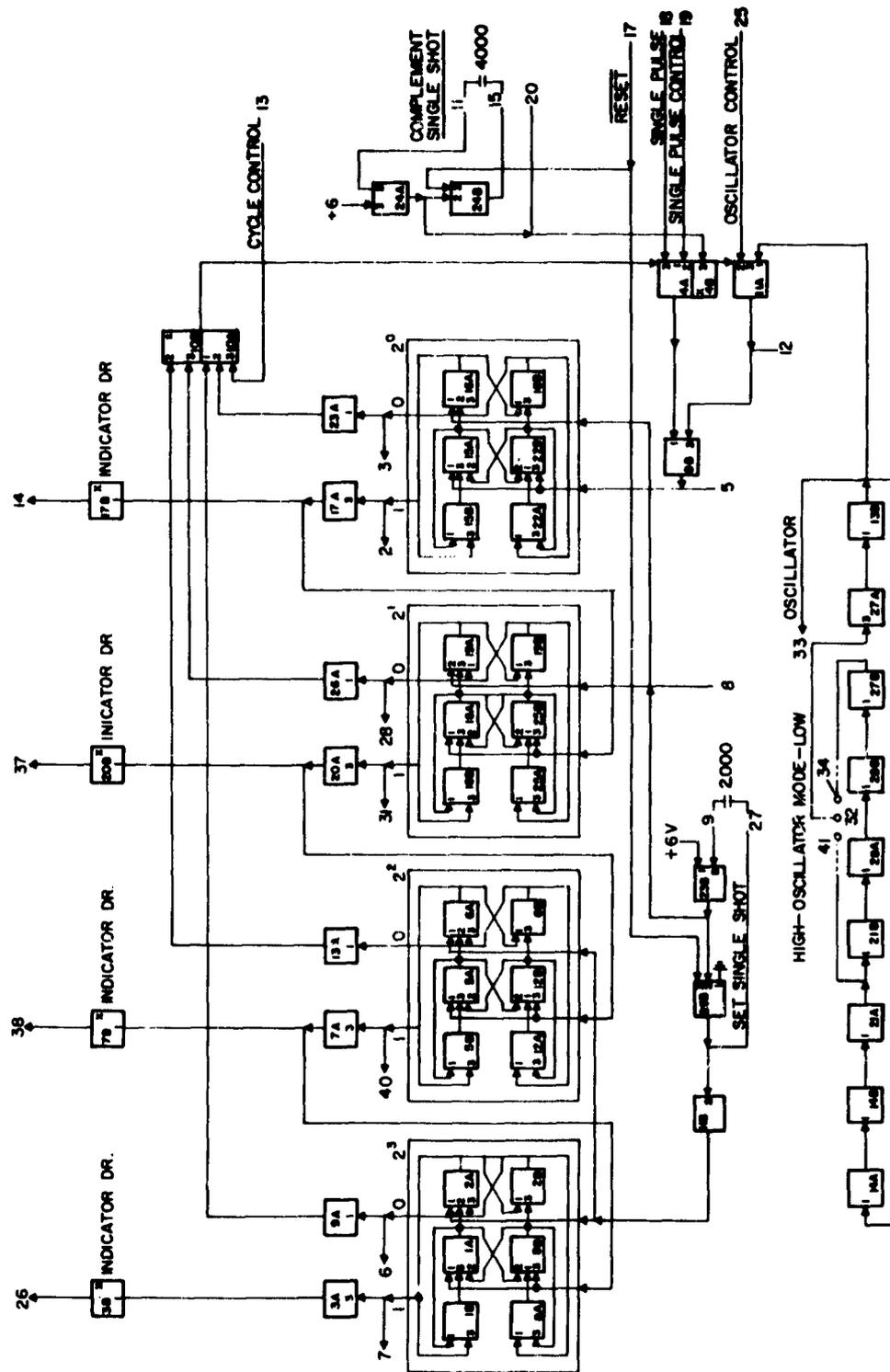
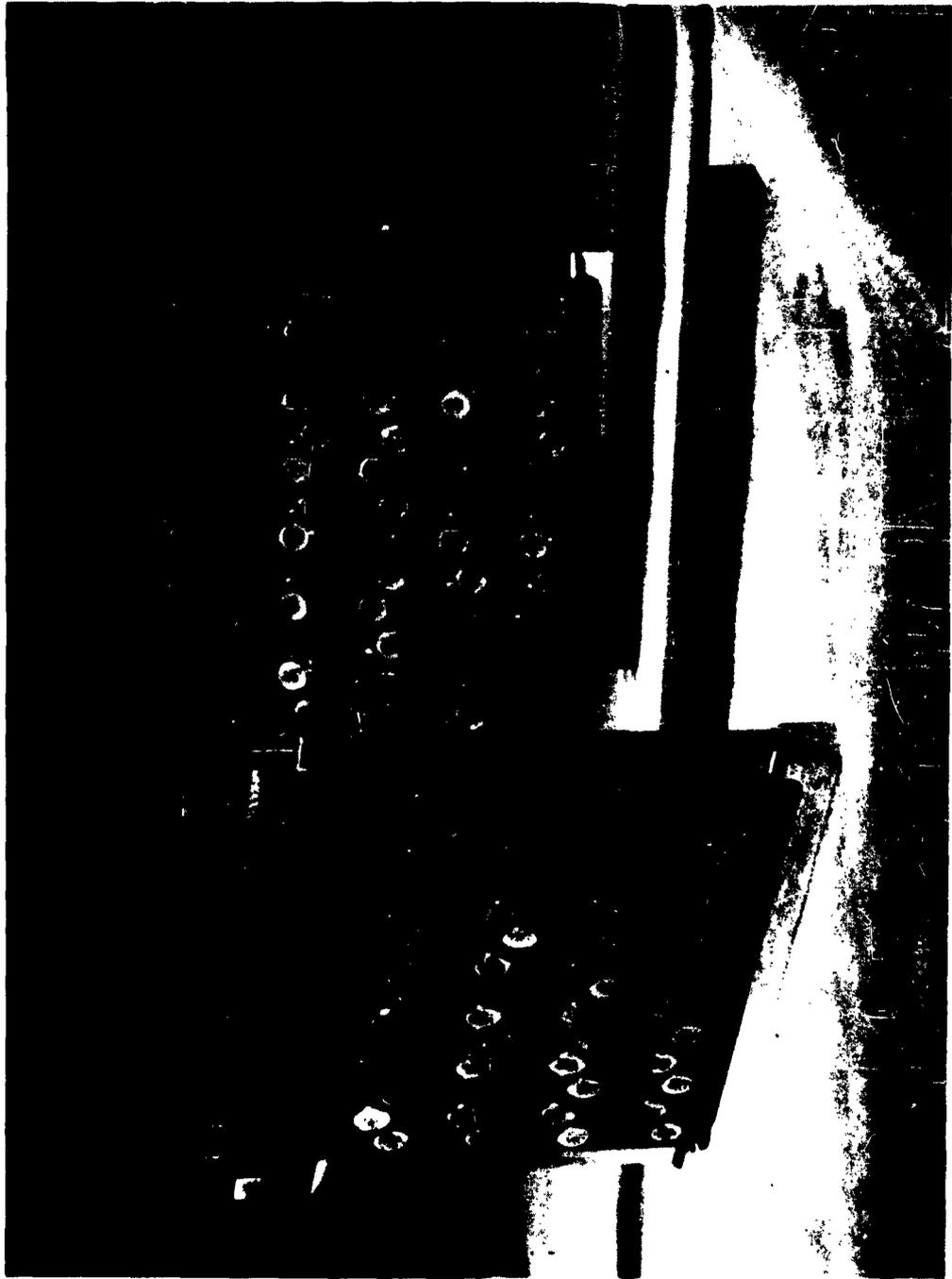


Figure 4-22: Logic Diagram of Integrated Counter Assembly



Figure 4-23: Substrate Lamination Fixture



**Figure 4-24: Functional Assembly Unit Incorporating Special Frame and Connector**

FIG. 4 -- 25

# 24 HOUR TEMPERATURE/HUMIDITY CYCLE

ACCORDING TO MIL - STD 202, METHOD 106, TEST CONDITION A

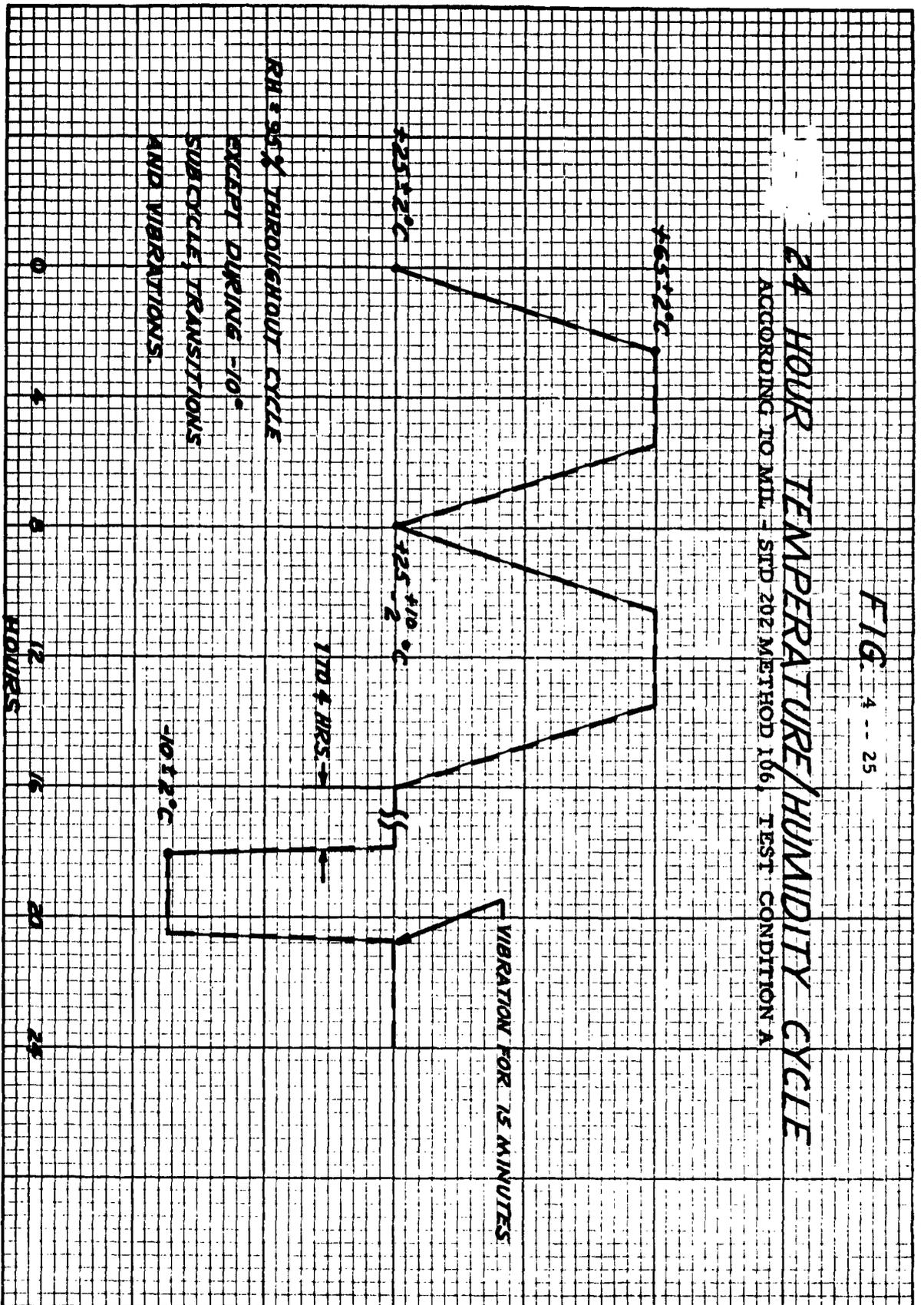




Figure 4-26

Assembly containing 772 probes for the four point probe measurement of the 224 resistors on a 56 circuit thin film panel.

COMPONENTS DIVISION - DEPT. 576  
 THIN FILM EVALUATION GROUP  
 PANEL SERIAL NUMBER RT27-086 DATE 10/31

POST-ANNEALED VALUES

1K RESISTOR VARIATIONS

MEDIAN VALUE IS 00970 OHMS

TOTAL RESISTORS 056

TOTAL RESISTORS ABOVE ALLOWABLE LIMITS 000

LOWEST VALUES			MEDIUM VALUES			HIGHEST VALUES		
LOC	VALUE	% DEV	LOC	VALUE	% DEV	LOC	VALUE	% DEV
10-4	00954	-04.6	25-4	00968	-03.2	01-4	00984	-01.6
11-5	00954	-04.6	13-4	00968	-03.2	01-5	00985	-01.5
10-5	00957	-04.3	14-5	00970	-03.0	15-5	00987	-01.3
11-4	00957	-04.3	24-4	00970	-03.0	28-5	00988	-01.2
12-4	00957	-04.3	02-5	00971	-02.9	22-4	00989	-01.1
12-5	00957	-04.3	20-4	00971	-02.9	22-5	00997	-00.3

HIGHEST % DEVIATIONS

LOC	VALUE	% DEV
10-4	00954	-04.6
22-5	00997	-00.3
TOTAL 04.3%		

4K RESISTOR VARIATIONS

MEDIAN VALUE IS 04026 OHMS

TOTAL RESISTORS 168

TOTAL RESISTORS ABOVE ALLOWABLE LIMITS 000

LOWEST VALUES			MEDIUM VALUES			HIGHEST VALUES		
LOC	VALUE	% DEV	LOC	VALUE	% DEV	LOC	VALUE	% DEV
12-8	03873	-03.1	16-6	04025	000.6	22-6	04174	004.3
25-1	03911	-02.2	05-2	04025	000.6	25-8	04175	004.3
11-2	03912	-02.2	02-6	04026	000.6	28-8	04181	004.5
11-7	03920	-02.0	24-1	04026	000.6	23-8	04191	004.7
12-2	03922	-01.9	24-2	04026	000.6	22-7	04197	004.9
11-1	03929	-01.7	26-1	04026	000.6	22-8	04247	006.1

HIGHEST % DEVIATIONS

LOC	VALUE	% DEV
12-8	03873	-03.1
22-8	04247	006.1
TOTAL 09.2%		

Figure 4-27A

$\epsilon$  = + Sign

COMPONENTS DIVISION - DEPT. 576  
 THIN FILM EVALUATION GROUP  
 PANEL SERIAL NUMBER RT27-087 DATE 11/02

POST-ANNEALED VALUES

1K RESISTOR VARIATIONS

MEDIAN VALUE IS 00971 OHMS  
 TOTAL RESISTORS 056  
 TOTAL RESISTORS ABOVE ALLOWABLE LIMITS 000

LOWEST VALUES			MEDIUM VALUES			HIGHEST VALUES		
LOC	VALUE	% DEV	LOC	VALUE	% DEV	LOC	VALUE	% DEV
10-4	00958	-04.2	25-4	00968	-03.2	04-4	00987	-01.3
17-4	00958	-04.2	27-4	00968	-03.2	07-5	00990	-01.0
18-4	00958	-04.2	15-5	00971	-02.9	22-5	00991	-00.9
19-4	00958	-04.2	23-4	00971	-02.9	07-4	00993	-00.7
11-5	00959	-04.1	25-5	00971	-02.9	01-5	00993	-00.7
18-5	00959	-04.1	26-5	00971	-02.9	01-4	00994	-00.6

HIGHEST % DEVIATIONS

LOC	VALUE	% DEV
10-4	00958	-04.2
01-4	00994	-00.6
TOTAL 03.6%		

4K RESISTOR VARIATIONS

MEDIAN VALUE IS 04029 OHMS  
 TOTAL RESISTORS 168  
 TOTAL RESISTORS ABOVE ALLOWABLE LIMITS 000

LOWEST VALUES			MEDIUM VALUES			HIGHEST VALUES		
LOC	VALUE	% DEV	LOC	VALUE	% DEV	LOC	VALUE	% DEV
12-8	03888	-02.8	27-2	04024	±00.6	01-2	04170	±04.2
12-2	03929	-01.7	28-3	04027	±00.6	07-1	04173	±04.3
11-2	03931	-01.7	06-8	04029	±00.7	25-8	04173	±04.3
11-7	03934	-01.6	02-8	04029	±00.7	22-7	04184	±04.6
13-7	03937	-01.5	19-6	04029	±00.7	01-1	04188	±04.7
25-1	03938	-01.5	26-3	04030	±00.7	22-8	04209	±05.2

HIGHEST % DEVIATIONS

LOC	VALUE	% DEV
12-8	03888	-02.8
22-8	04209	±05.2
TOTAL 08.0%		

Figure 4-27B

± = + Sign

Figure 4-28

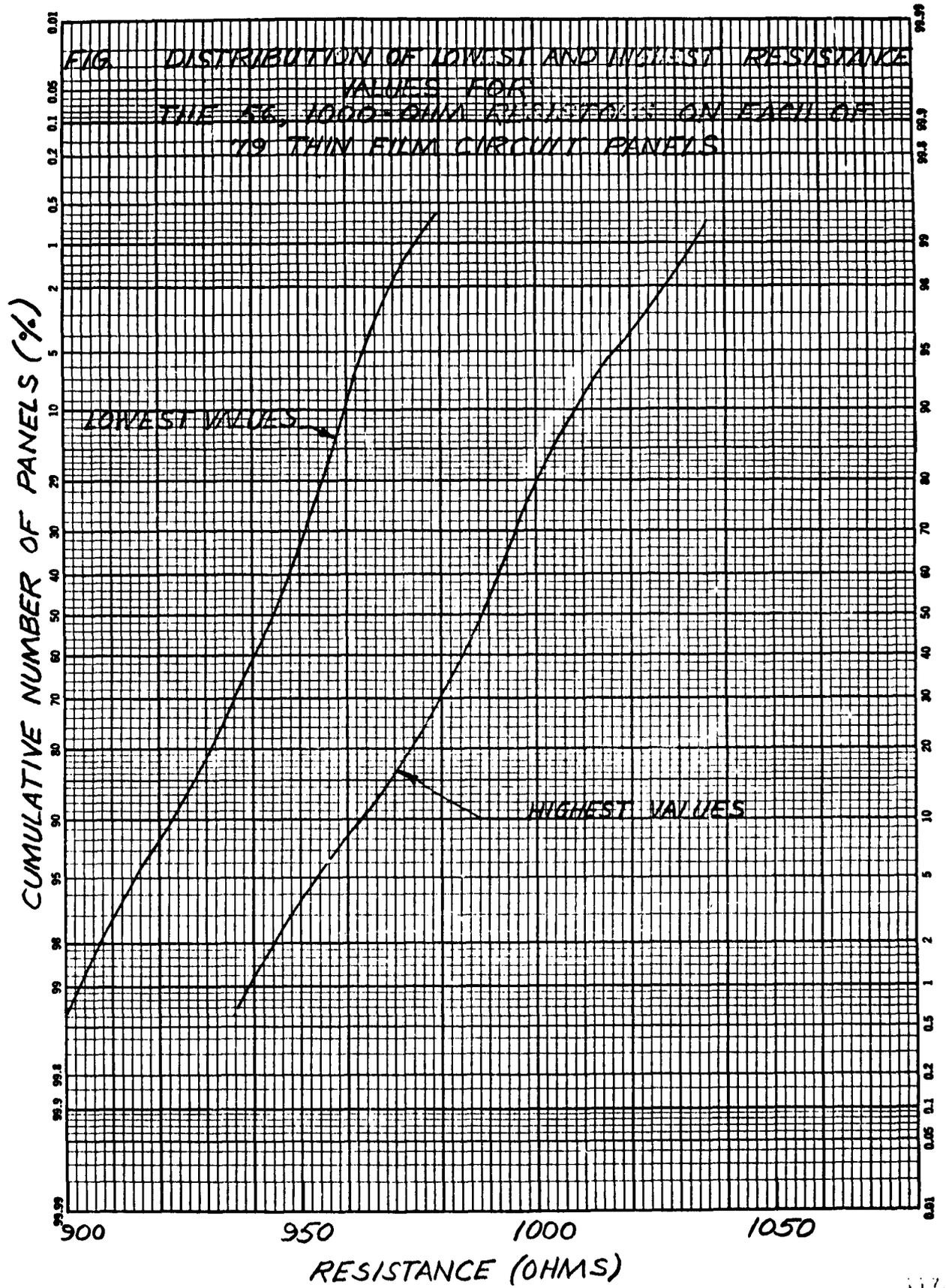


Figure 4-29

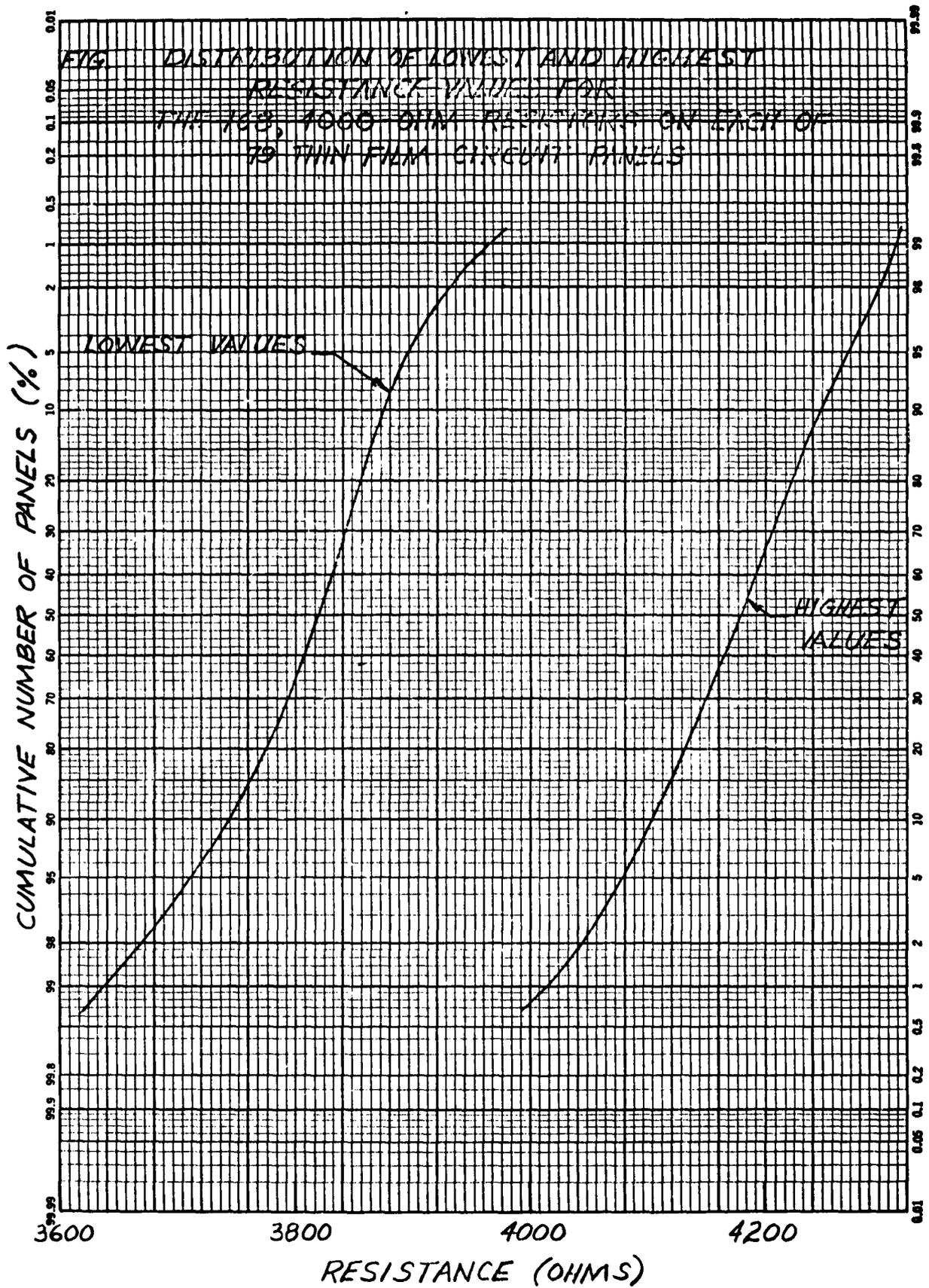
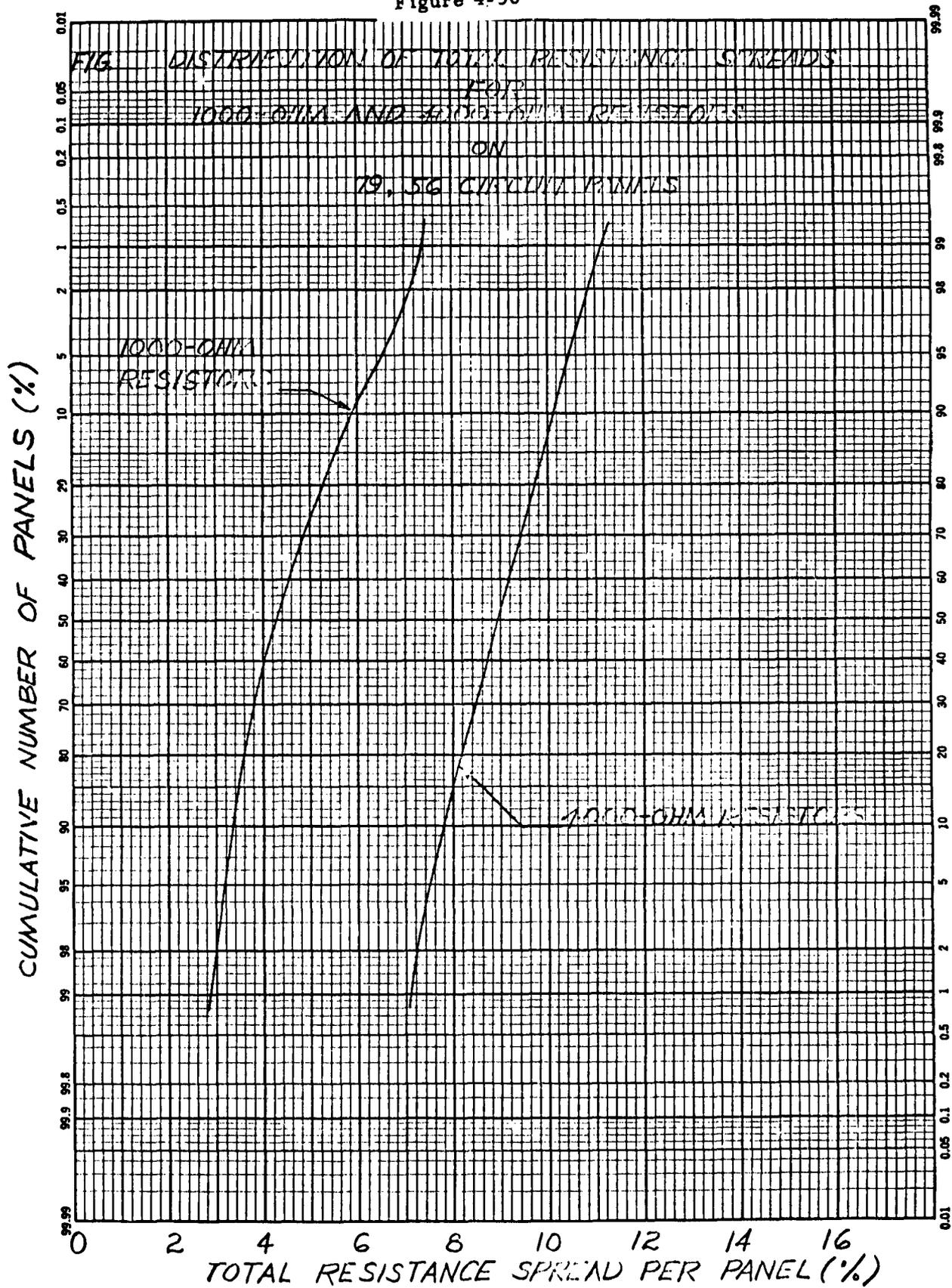
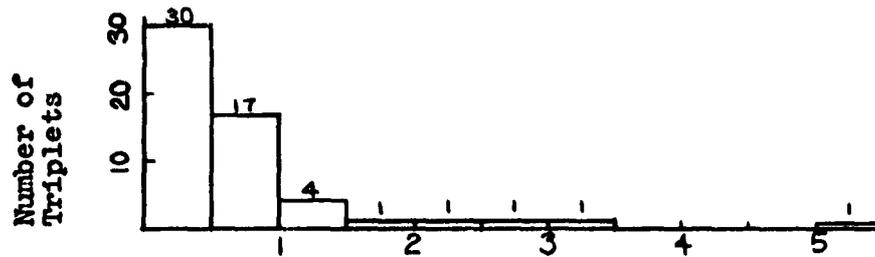


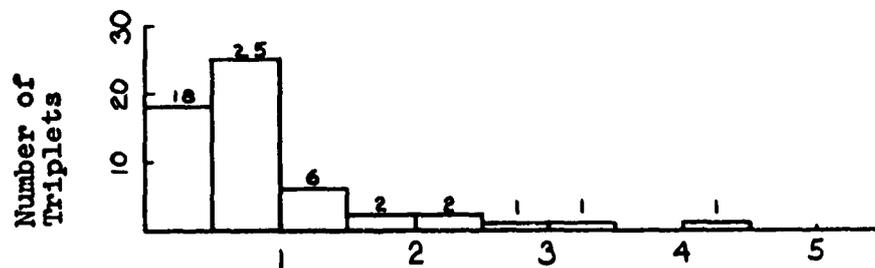
Figure 4-30



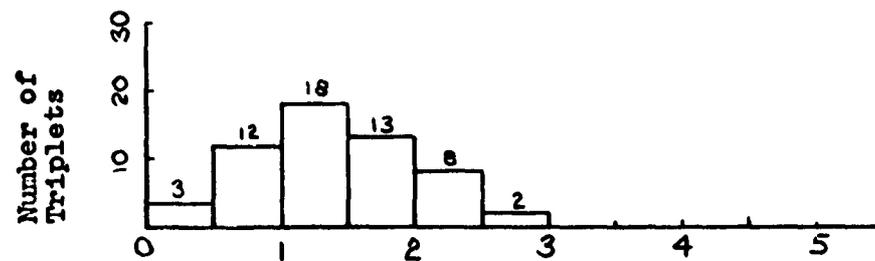
Total Resistance  
Spread of 168,  
4000-Ohm Resistors



Panel A: 6.8%



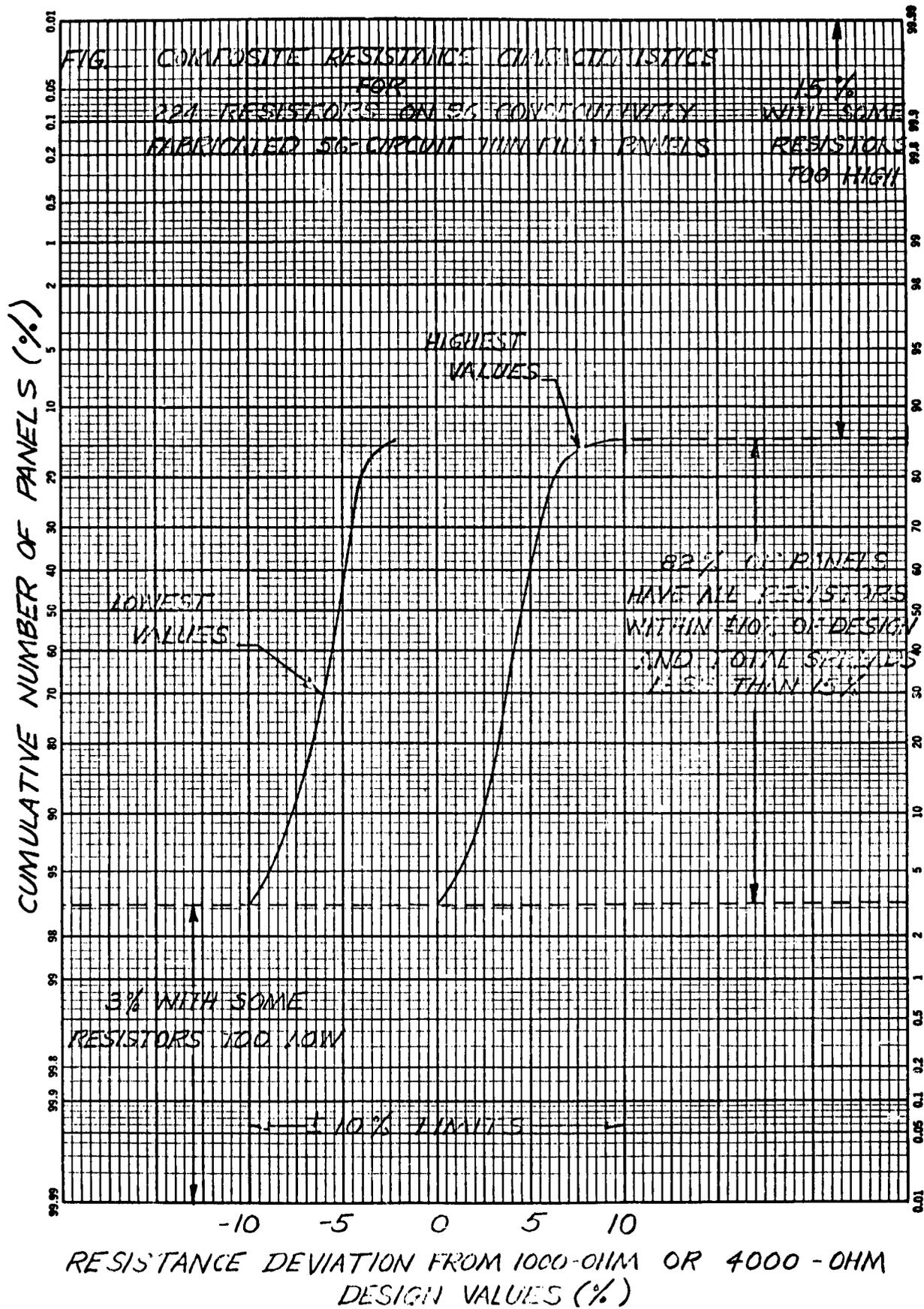
Panel B: 9.2%



Panel C: 11.2%

Resistance Spread of Triplets (%)

Fig. 4-31 Distributions of Resistance Spreads for 56, 4000-Ohm  
Resistor Triplets on 3 Deposited Thin Film Panels



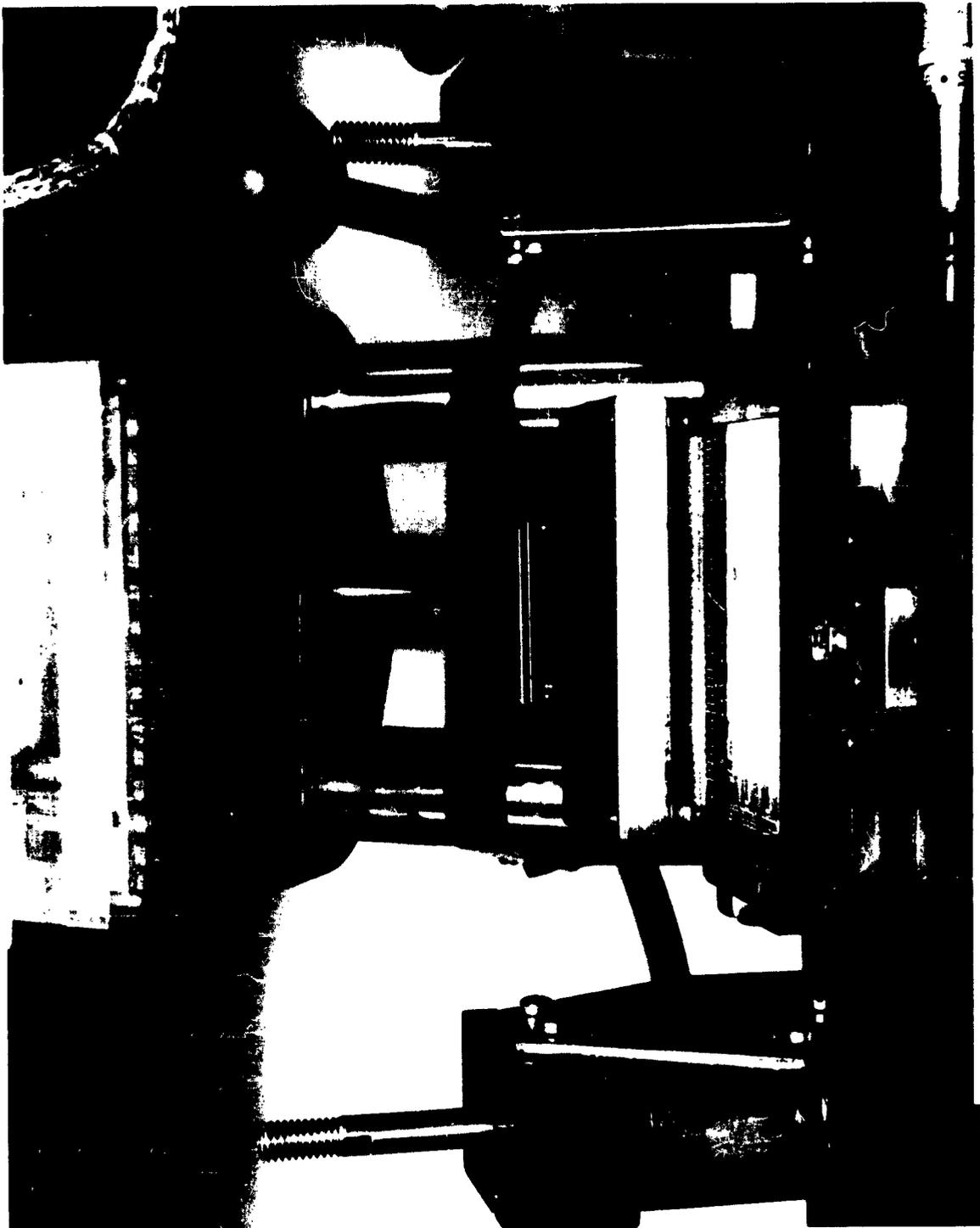


Figure 4-33: 56 Transistor Probe and 44-Pin Edge Connector in a Standard Test Fixture for the Operational Test of a Thin Film Panel

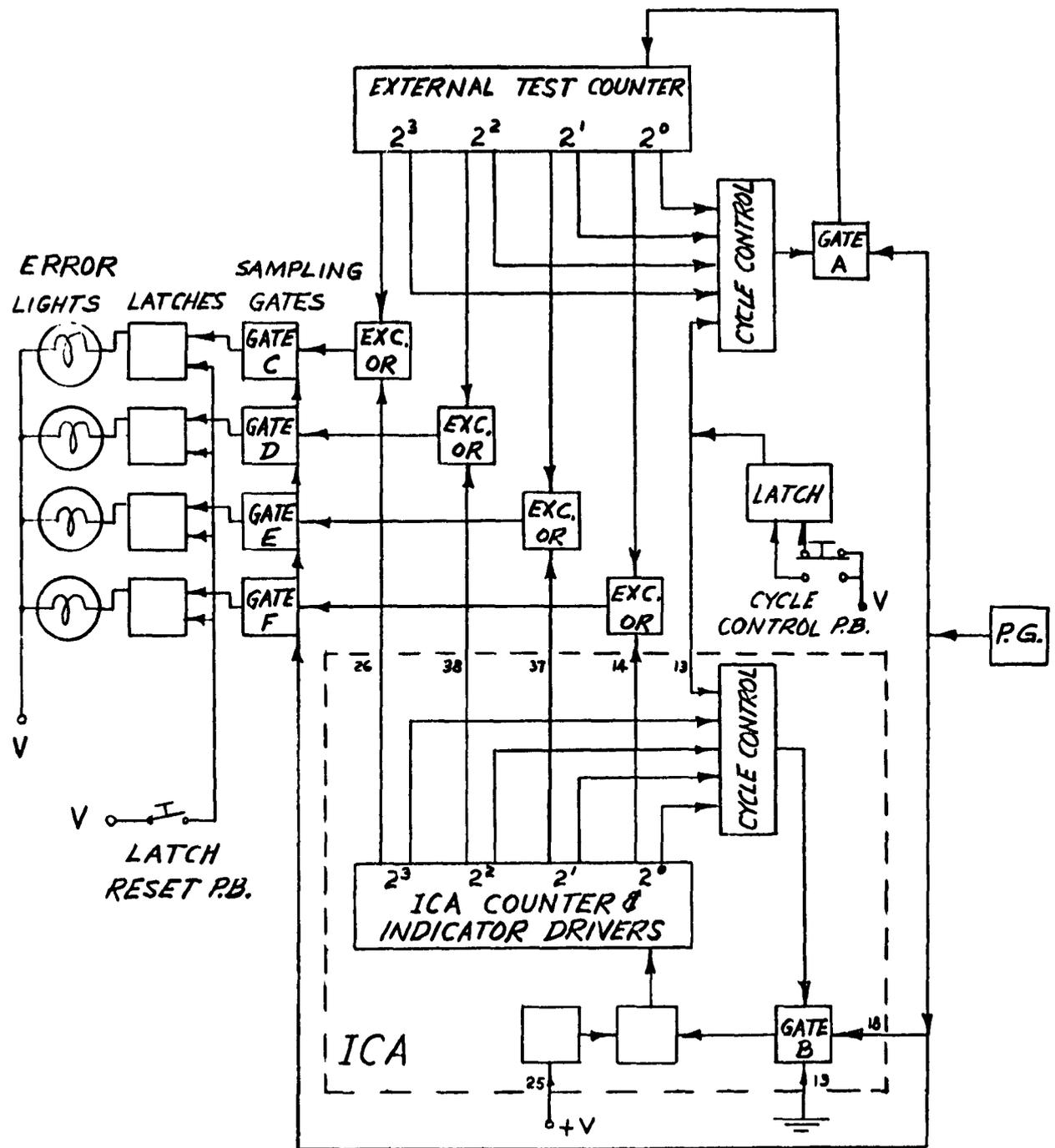
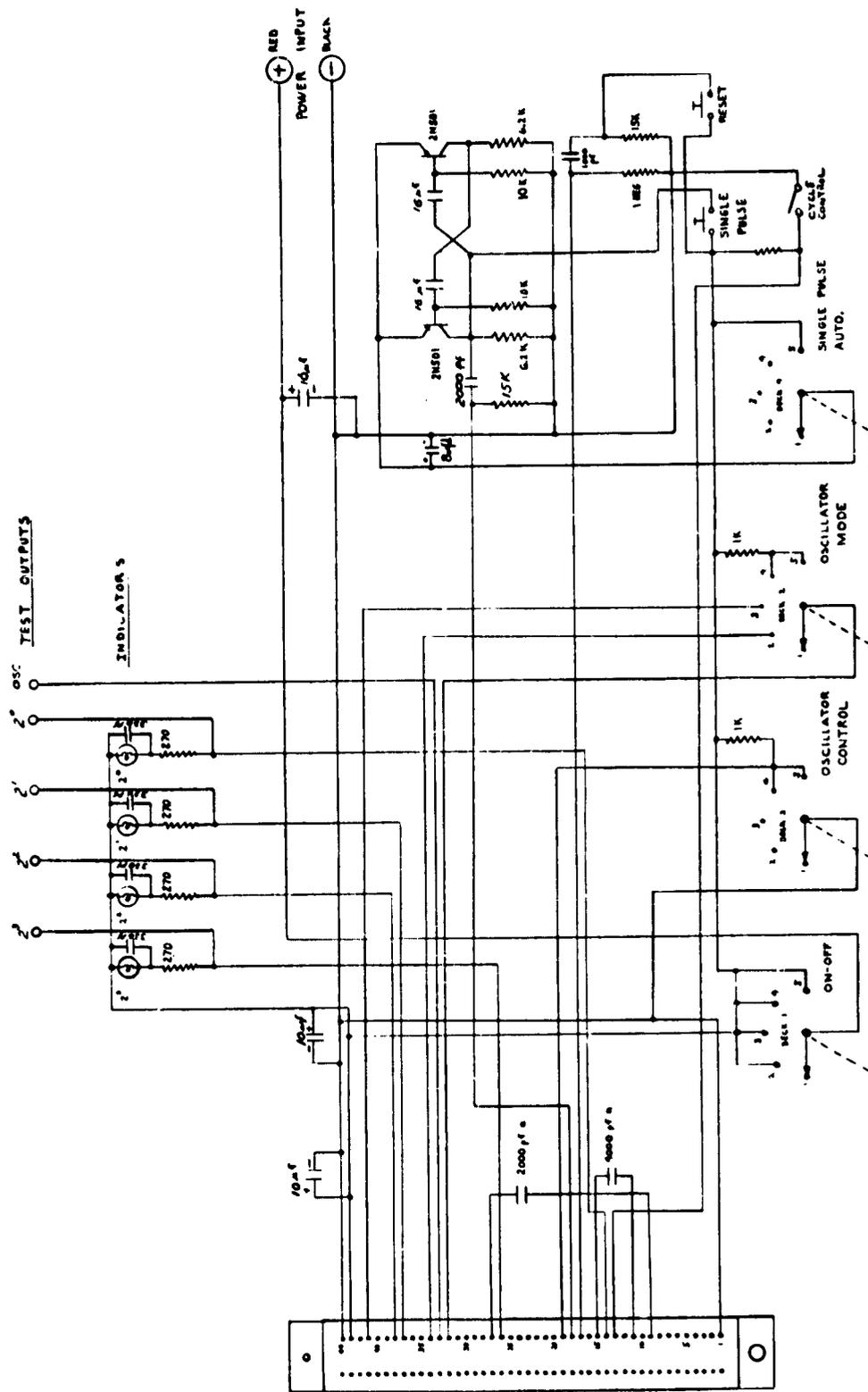


FIG. 4-34 LOGIC OF ELECTRONIC COMPARATOR FOR FUNCTIONAL ASSEMBLY TEST



Figure 4-35: Functional Assembly  
Test Unit



FUNCTIONAL Assembly Test Unit Fig 4-36

\*THESE COMPONENTS ARE PART OF THE CIRCUITRY CONTAINED ON THE FILM UNIT

International Business Machines  
DA 36-039-sc-87246

Final Report  
1 May 61 - 31 December 62

Distribution List

	<u>No. of Copies</u>
OASD (R&E) ATTN: Technical Library Room 3E1065 The Pentagon Washington 25, D. C.	1
Chief of Research and Development OCS, Department of the Army Washington 25, D. C.	1
Commanding General U. S. Army Material Command ATTN: R&D Directorate Washington 25, D. C.	1
Commanding General U. S. Army Electronics Command ATTN: AMSEL-AD Fort Monmouth, New Jersey	1
Director, U. S. Naval Research Laboratory ATTN: Code 2027 Washington 25, D. C.	1
Commander, Aeronautical Systems Division ATTN: ASAPRL Wright-Patterson Air Force Base Ohio	1
Hq., Electronic Systems Division ATTN: ESAL L. G. Hanscon Field Bedford, Massachusetts	1
Commander, Air Force Cambridge Research Laboratories ATTN: CRO L. G. Hanscon Field Bedford, Massachusetts	1

International Business Machines  
DA 36-039-sc-87246  
Final Report

-2-

Distribution List

	<u>No. of Copies</u>
Commander, Air Force Command & Control Development Division ATTN: CRZC L. G. Hanscon Field Bedford, Massachusetts	1
Commander, Rome Air Development Center ATTN: RAALD Griffiss Air Force Base, New York	1
Commander, Armed Services Technical Information Agency ATTN: TISIA Arlington Hall Station Arlington 12, Virginia	10
Chief, U. S. Army Security Agency Arlington Hall Station Arlington 12, Virginia	2
Deputy President U. S. Army Security Agency Board Arlington Hall Station Arlington 12, Virginia	1
Commanding Officer Harry Diamond Laboratories ATTN: Library, Room 211, Building 92 Washington 25, D. C.	1
Corps of Engineers Liaison Office U. S. Army Electronics Research and Development Laboratory Fort Monmouth, New Jersey	1
AFSC Scientific/Technical Liaison Office U. S. Naval Air Development Center Johnsville, Pennsylvania	1
Commanding Officer U. S. Army Electronics Material Support Agency ATTN: SELMS-ADJ Fort Monmouth, New Jersey	1

International Business Machines  
DA 36-039-sc-87246  
Final Report

-3-

Distribution List

No. of Copies

Marine Corps Liaison Office U. S. Army Electronics Research and Development Laboratory ATTN: SELRA/LNR Fort Monmouth, New Jersey	1
Commanding Officer U. S. Army Electronics Research and Development Laboratory ATTN: Director of Research or Engineering Fort Monmouth, New Jersey	1
Commanding Officer U. S. Army Electronics Research and Development Laboratory ATTN: Technical Documents Center Fort Monmouth, New Jersey	1
Commanding Officer U. S. Army Electronics Research and Development Laboratory ATTN: SELRA/ADJ (FU #1) Fort Monmouth, New Jersey	1
Advisory Group on Electron Devices 346 Broadway New York 13, New York	2
Commanding Officer U. S. Army Electronics Research and Development Laboratory ATTN: SELRA/TNR Fort Monmouth, New Jersey (FOR RETRANSMITTAL TO ACCREDITED BRITISH AND CANADIAN GOVERNMENT REPRESENTATIVES)	3
Commanding General U. S. Army Combat Developments Command ATTN: CDCMR-E Fort Belvoir, Virginia	1
Commanding Officer U. S. Army Communications-Electronics Combat Development Agency Fort Buachuca, Arizona	1

International Business Machines  
DA 36-039-sc-87246  
Final Report

-4-

Distribution List

No. of Copies

Director, Fort Monmouth Office U. S. Army Communications-Electronics Combat Development Agency Building 410 Fort Monmouth, New Jersey	1
AFSC Scientific/Technical Liaison Office U. S. Army Electronics Research and Development Laboratory Fort Monmouth, New Jersey	1
Commanding Officer and Director U. S. Navy Electronics Laboratory San Diego 52, California	1
Westinghouse Electric Corporation Air Arm Division, P. O. Box 746 ATTN: Dr. M. Lauriente, Materials & Processes Baltimore 3, Maryland	1
Commander, ASD ATTN: Mr. N. DiGiacomo, ASRNE Wright-Patterson Air Force Base, Ohio	1
Servomechanisms, Inc. Research & Development Center ATTN: Mr. N. Weber Santa Barbara Airport Goleta, California	1
United Aircraft Corporation Hamilton Standard Division ATTN: Mr. L. Ullary Windsor Locks, Connecticut	1
P. R. Mallory & Company, Inc. ATTN: C. Baetten 3029 East Washington Street Indianapolis, Indiana	1

**International Business Machines  
DA 36-039-sc-87246  
Final Report**

-5-

**Distribution List**

**No. of Copies**

<b>Illinois Tool Works Paktrom Division ATTN: Mr. R. E. Henry 1321 Leslie Avenue Alexandria, Virginia</b>	<b>1</b>
<b>Commanding Officer Harry Diamond Laboratories ATTN: Mr. N. Doctor Connecticut and Van Ness Streets, N. W. Washington 25, D. C.</b>	<b>1</b>
<b>Sylvania Electric Products ATTN: J. E. Thomas, Jr. 100 Sylvan Road Woburn, Massachusetts</b>	<b>1</b>
<b>Chief, Bureau of Ships Department of the Navy ATTN: Mr. A. H. Young, Code 691A1A Washington 25, D. C.</b>	<b>1</b>
<b>Director National Security Agency ATTN: Mr. J. D. Moskowitz, R13 Fort George Meade, Maryland</b>	<b>1</b>
<b>Radio Corporation of America ATTN: Mr. C. Rammer Building 1-4 Front &amp; Copper Streets Camden, New Jersey</b>	<b>1</b>
<b>Texas Instruments, Inc. Semiconductor Components Library P. O. Box 312 Dallas 21, Texas</b>	<b>1</b>
<b>International Resistance Company ATTN: Dr. J. Bohrer 401 North Broad Street Philadelphia 8, Pennsylvania</b>	<b>1</b>

International Business Machines  
DA 36-039-sc-87246  
Final Report

-6-

Distribution List

	<u>No. of Copies</u>
AMP, Incorporated ATTN: Mr. W. J. Hudson Harrisburg, Pennsylvania	1
The Bendix Corporation Research Laboratories Division ATTN: Mr. W. M. Spurgeon Southfield, (Detroit), Michigan	1
Philco Corporation Communications and Weapons Division ATTN: Mr. J. Schiller 4700 Wissahicken Avenue Philadelphia 44, Pennsylvania	1
Commander Naval Avionics Facility ATTN: Code 902 Indianapolis, Indiana	1
Commanding General U. S. Army Ordnance Missile Command ATTN: ORD IM-IEP (Bldg 4500) Huntsville, Alabama	1
Commanding Officer U. S. A. Electronics Research & Development Laboratory Fort Monmouth, New Jersey ATTN: SELRA/PEM	1
Commanding Officer U. S. A. Electronics Research & Development Laboratory Fort Monmouth, New Jersey ATTN: SELRA/PF	1
Commanding Officer U. S. A. Electronics Research & Development Laboratory Fort Monmouth, New Jersey ATTN: SELRA/PEP (Mr. R. Geisler)	14

**International Business Machines  
DA 36-039-sc-87246  
Final Report**

-7-

Distribution List

No. of Copies

Honeywell Aeronautical Division  
ATTN: Mr. G. W. Gruber  
13350 U. S. - 19  
St. Petersburg, Florida

1

Philco Corporation  
ATTN: Mr. C. D. Simmons  
Manager, Microelectronics Department  
Lansdale Division  
Lansdale, Pennsylvania

1

Stanford Research Institute  
ATTN: Dr. Saul W. Chaiken  
Material Sciences Division  
Menlo Park, California

1

Commanding Officer  
U. S. Naval Avionics Facility  
ATTN: Code D/130 - Library  
Indianapolis 18, Indiana

1