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FINAL REPORT
FOR
SEMICONDUCTOR RESISTIVE ELEMENT

This report covers the period 1 January 1961 to 31 December 1962

TEXAS INSTRUMENTS INCORPORATED
13500 N. CENTRAL EXPRESSWAY
DALLAS, TEXAS



NAVY DEPARTMENT BUREAU OF SHIPS ELECTRONICS DIVISION

NObsr-85406

SR-0080302, ST-9607

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A B S T R A C T

THIS FINAL ENGINEERING REPORT FOR PHASE II OF THE CONTRACT COVERS A TWELVE-MONTH PERIOD. SOME BACKGROUND INFORMATION FROM PHASE I HAS BEEN INCLUDED AS REFERENCE. THE GENERAL OBJECTIVE OF PRODUCING A LOW TEMPERATURE COEFFICIENT OF RESISTANCE (TCR) DEVICE FROM A SEMICONDUCTOR MATERIAL WAS ONLY PARTIALLY SUCCESSFUL. TYPICAL TCR DEVICE VALUES ABOVE ROOM TEMPERATURE WERE NEVER MUCH LOWER THAN 150 PPM/°C FOR THE SILICON RESISTIVE ELEMENT INVESTIGATED. LOW TEMPERATURE TCR VALUES (AT -50°C) WERE AROUND 500 PPM/°C. LOAD-LIFE STABILITY AND RESISTANCE TO ENVIRONMENTS (MOISTURE, OXIDATION) PROVED AS GOOD AS OR BETTER THAN THIN-FILM RESISTORS ON THE MARKET.

SPECIFIC PROBLEMS ENCOUNTERED (SUCH AS OHMIC CONTACTS, RESISTANCE ADJUSTMENT, JUNCTION EFFECTS, ETC.) AND THEIR SOLUTIONS HAVE BEEN DISCUSSED IN DETAIL. A MANUFACTURING PROCEDURE FOR PRODUCING A POLYCRYSTALLINE SILICON DEVICE HAS BEEN INCLUDED IN THIS REPORT.

A PROBLEM OF TCR SHIFT RELATED TO THE PIEZORESISTIVE EFFECT IN THE SILICON ELEMENT, THROUGH STRESS INDUCED BY THE MOLDING EPOXY, BECAME CRITICAL BUT WAS SOLVED DURING THE LAST QUARTER. DATA ON LOAD-LIFE AND ENVIRONMENTAL TESTS WERE ACCUMULATED ON 150 FINISHED DEVICES WHICH ACCOMPANIED THIS REPORT. POTENTIAL APPLICATIONS FOR POLYCRYSTALLINE SILICON RESISTORS WERE SUGGESTED, BUT ADDITIONAL R&D WORK ON THIS APPROACH TO A LOW TC, STABLE RESISTIVE ELEMENT WAS NOT RECOMMENDED.

THE DEVELOPMENT WORK PERFORMED UNDER THIS R&D CONTRACT IS BELIEVED TO

HAVE IMPROVED THE "STATE-OF-THE-ART" OF SEMICONDUCTOR RESISTIVE ELEMENTS
IN GENERAL, AND IS BELIEVED TO HAVE CONTRIBUTED TO A BETTER UNDER-
STANDING OF SILICON AS A RESISTIVE MATERIAL.

I. PURPOSE

AN ATTEMPT HAS BEEN MADE UNDER THIS CONTRACT TO DEVELOP A SEMI-CONDUCTOR RESISTIVE ELEMENT WITH A MINIMUM TEMPERATURE COEFFICIENT OF RESISTANCE (TCR) WHICH WOULD EXHIBIT GREATER RELIABILITY THAN METAL-FILM RESISTORS PRESENTLY ON THE MARKET. SPECIFIC OBJECTIVES WERE TO PRODUCE A RESISTOR WITH < 50 PPM/ $^{\circ}$ C TCR (FROM -50° C TO $+175^{\circ}$ C) AND WITH LOAD-LIFE STABILITY CHARACTERISTICS COMPARABLE TO THOSE SPECIFIED BY MIL-R-10509D FOR PRECISION FIXED-FILM RESISTORS.

THE FIRST APPROACH WAS TO CONSIDER BULK SEMICONDUCTOR ELEMENTS IN ORDER TO GAIN AN ADVANTAGE OVER THE INHERENTLY UNRELIABLE NATURE OF THIN-FILM ELEMENTS. THE RESISTIVITY OF BULK-TYPE ELEMENTS WOULD NEED TO BE LARGE IN COMPARISON WITH METALS* USED IN THIN-FILM DEVICES. LIMITATIONS ON GEOMETRY OF THE ELEMENT, I.E. CROSS-SECTIONAL AREA AND EFFECTIVE LENGTH, ARE IMPOSED BY PRACTICAL CONSIDERATIONS. UNFORTUNATELY THERE IS A LARGE VARIATION OF CONDUCTIVITY WITH CHANGING TEMPERATURE ASSOCIATED WITH HIGH RESISTIVITY IN SEMICONDUCTOR MATERIALS. THUS, IT WAS FUNDAMENTAL TO RESTRICT THE STUDY TO RELATIVELY LOW RESISTIVITY MATERIAL, WHICH, IN TURN, PRE-DETERMINED TO A LARGE EXTENT CONFIGURATION OF THE RESISTIVE ELEMENT.

FROM THE RESISTANCE EQUATION, $R = \rho (L/A)$, IT MAY BE SHOWN THAT FOR LOW VALUES OF " ρ " (RESISTIVITY) THE ALLOWED L/A (EFFECTIVE LENGTH

* BULK RESISTIVITY VALUES OF ALLOYS USED FOR METAL-FILM RESISTORS ARE APPROXIMATELY 100 MICRO OHM-CM.

1. PURPOSE (CONTINUED)

OVER CROSS-SECTIONAL AREA) MUST BE LARGE TO OBTAIN REASONABLY LARGE VALUES OF RESISTANCE. CONSIDERING RESISTIVITIES IN THE RANGE OF .00X Ω -CM, THE MATHEMATICS DICTATES THAT THE ELEMENT GEOMETRY MUST BE OF A LAYER CONFIGURATION FOR PRACTICAL RESISTANCE VALUES. THE THICKNESS OF SUCH A SEMICONDUCTOR RESISTIVE LAYER WILL BE MUCH GREATER (BY AT LEAST TWO MAGNITUDES) THAN METAL-FILM RESISTIVE ELEMENTS. IN FACT, IT WOULD BE TECHNICALLY SOUND TO ASSUME THAT THE BULK PROPERTIES OF THE SEMICONDUCTOR MATERIAL WOULD PREDOMINATE OVER ANY POSSIBLE THIN-FILM CHARACTERISTICS.

BASED ON THE CONCLUSIONS REGARDING TCR CHARACTERISTICS OF SEVERAL MATERIALS (TITANIA, SILICON CARBIDE, SILICON BORIDE) INVESTIGATED IN PHASE I, IT WAS THOUGHT THAT A GREATER AMOUNT OF RESEARCH AND DEVELOPMENT WOULD BE NECESSARY TO ACHIEVE THE OBJECTIVES OF THE CONTRACT THROUGH SEMICONDUCTOR BULK-TYPE ELEMENTS THAN BY IMPROVING SEMICONDUCTOR-LAYER ELEMENTS. SILICON WAS CHOSEN FOR INVESTIGATION AS THE SEMICONDUCTOR RESISTIVE MATERIAL PRINCIPALLY BECAUSE A GREAT DEAL OF BACKGROUND INFORMATION ON DOPING PROCEDURES, VAPOR DEPOSITION, DIFFUSION TECHNIQUES, ETC. WAS AVAILABLE AT TEXAS INSTRUMENTS INCORPORATED. SILICON WAS CHOSEN FOR INVESTIGATION IN PREFERENCE TO GERMANIUM BECAUSE OF ITS HIGH TEMPERATURE LIMITATION AROUND 80°C, AT WHICH TEMPERATURE THE RESISTIVITY DECREASES RAPIDLY WITH FURTHER INCREASE IN TEMPERATURE. THIS IS THE "INTRINSIC" CONDUCTION REGION FOR THIS MATERIAL. SILICON'S INTRINSIC REGION FOR THE HIGHLY DOPED ($>10^{18}$ ATOMS/CC OF IMPURITY) CONCENTRATION DOES NOT BECOME PREDOMINANT UNTIL ABOUT 500°C.

I. PURPOSE (CONTINUED)

A. DISCUSSION OF IMPURITY CONDUCTION MECHANISMS

AT THIS POINT IT WOULD BE APPROPRIATE TO DISCUSS THE ELECTRICAL BEHAVIOR OF SILICON IN RELATION TO TEMPERATURE. FIGURE 1 IS A FAMILY OF RESISTIVITY TEMPERATURE CURVES FOR "N-TYPE" SILICON OF VARYING IMPURITY CONCENTRATION. THESE CURVES WERE PLOTTED FROM CALCULATED VALUES OF RESISTIVITY FOR VARIOUS TEMPERATURES AT AN ASSUMED ACTIVATION ENERGY FOR AN "N-TYPE" IMPURITY. THE TEMPERATURE RANGE OF INTEREST HAS BEEN OUTLINED ON THE GRAPHS. WITHIN THIS RANGE IT CAN BE SEEN THAT ONLY THE HIGHLY DOPED ($10^{18} \rightarrow 10^{20}$ AT./CC) MATERIAL EXHIBITS A MINIMUM CHANGE OF RESISTIVITY WITH TEMPERATURE. THIS MINIMUM RESISTIVITY CHANGE WITH TEMPERATURE OF HIGH IMPURITY CONCENTRATION IS RELATED TO CARRIER MOBILITY AS SHOWN IN FIGURE 2.

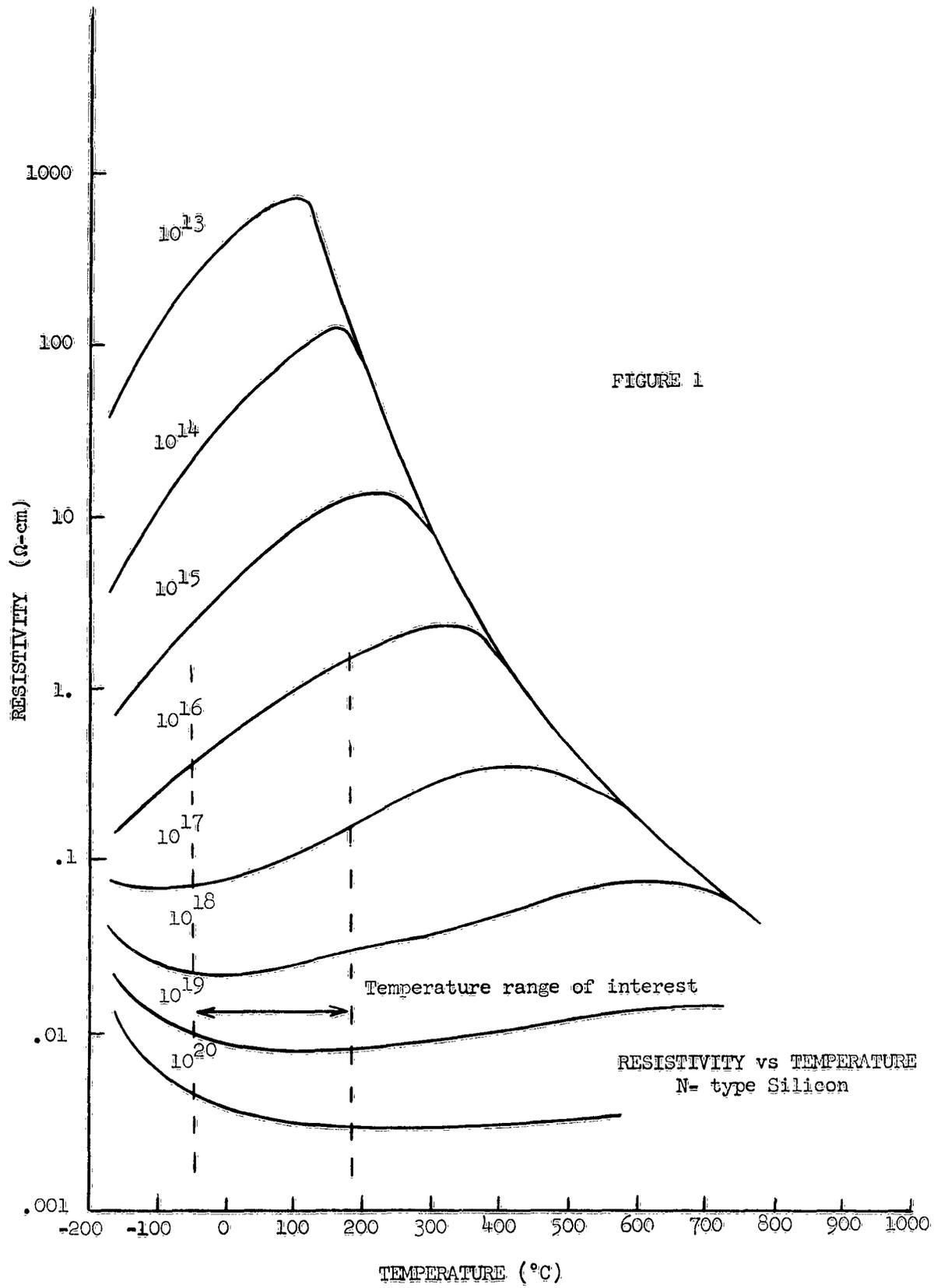


FIGURE 1

FIGURE 1

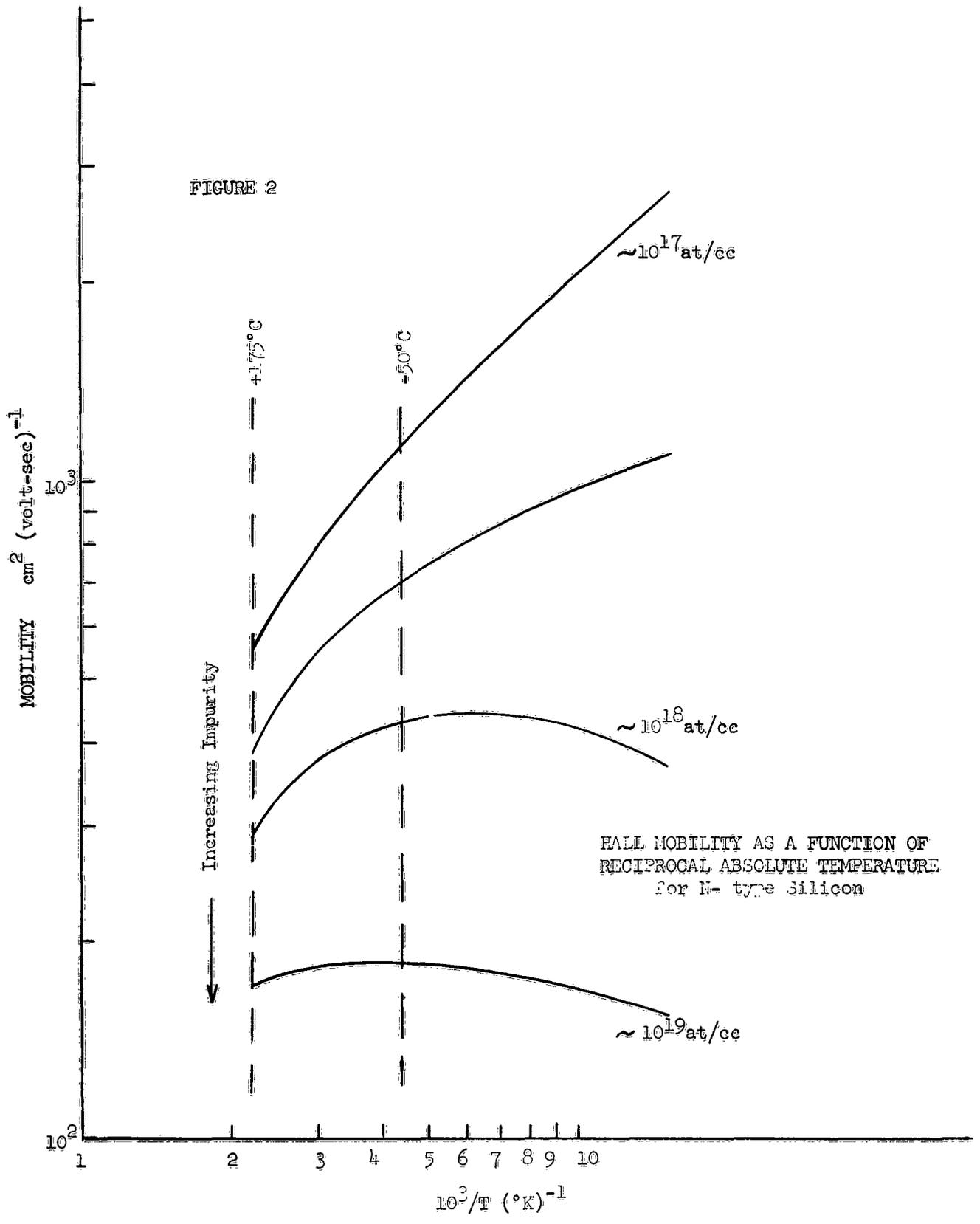


FIGURE 2

A. DISCUSSION OF IMPURITY CONDUCTION MECHANISMS (CONT'D)

FIGURE 3 IS A HYPOTHETICAL CURVE, FOR "N-TYPE" OR "P-TYPE" MATERIAL, WHICH IS AN ENLARGEMENT OF THAT SEGMENT OF THE OVERALL CURVE WITHIN THE TEMPERATURE RANGE AND IMPURITY LEVEL OF INTEREST. THE DISCUSSION WHICH FOLLOWS WILL EXPLAIN IN GREATER DETAIL THE CONDUCTION MECHANISMS WHICH TAKE PLACE IN THIS "EXTRINSIC" OR IMPURITY-DEPENDENT REGION.

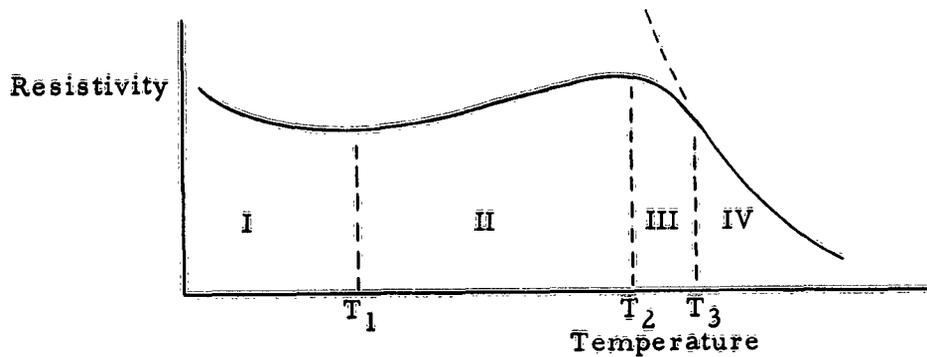


FIG. 3

THERE ARE FOUR GENERAL REGIONS INTO WHICH THE RESISTIVITY-TEMPERATURE CURVE MAY BE DIVIDED FOR PURPOSES OF DISCUSSION. IN EACH REGION THE TEMPERATURE COEFFICIENT IS DETERMINED BY CONDUCTION MECHANISMS WHICH MAY BE DESCRIBED IN FAIRLY SIMPLE TERMS.

AT SOME ARBITRARILY LOW TEMPERATURE, THE RESISTIVITY IS DECREASING AS TEMPERATURE IS INCREASED AS A RESULT OF IMPURITIES BEING CONTINUOUSLY IONIZED. MORE CARRIERS ARE THUS MADE AVAILABLE FOR CONDUCTION. AS TEMPERATURE T_1 IS REACHED, THE NEGATIVE SLOPE OF THE CURVE BECOMES LESS AND THEN GOES POSITIVE BECAUSE ALL THE IMPURITIES HAVE BEEN IONIZED AND THE MOBILITY IS BEING

A. DISCUSSION OF IMPURITY CONDUCTION MECHANISMS (CONT'D)

DECREASED DUE TO LATTICE VIBRATION OF THE CRYSTAL.

THE TEMPERATURE T_1 , AT WHICH THIS OCCURS IS DETERMINED FOR A GIVEN SEMICONDUCTOR BY TWO THINGS: (1) THE DOPING LEVEL, (2) THE ACTIVATION ENERGY OF THE IMPURITY. IN GENERAL, AS THE DOPING LEVEL INCREASES, THE TEMPERATURE T_1 AT WHICH ALL IMPURITY ATOMS ARE IONIZED WILL INCREASE. FOR A GIVEN IMPURITY CONCENTRATION, T_1 WILL ALSO INCREASE AS THE ACTIVATION ENERGY OF THE IMPURITY INCREASES. THE REASON FOR THE DEPENDENCE OF T_1 ON ACTIVATION ENERGY IS THAT BEFORE AN IMPURITY ATOM CAN BE IONIZED AND AID IN CONDUCTION, IT MUST ACQUIRE SUFFICIENT ENERGY FROM SOME SOURCE. THIS ENERGY IS KNOWN AS THE ACTIVATION ENERGY OF THE IMPURITY. GALLIUM, FOR INSTANCE, HAS A HIGHER ACTIVATION ENERGY THAN BORON, BOTH OF WHICH ARE USED TO DOPÉ SILICON TO MAKE IT P-TYPE. IF TWO SILICON SAMPLES ARE TAKEN, ONE DOPED WITH GA TO 5×10^{18} AND ANOTHER DOPED WITH B TO 5×10^{18} , T_1 WILL BE HIGHER FOR THE GA-DOPED SAMPLE. THE THERMAL ENERGY GIVEN UP TO THE SEMICONDUCTOR IONIZES THE IMPURITIES, HENCE A HIGHER AMOUNT OF THERMAL ENERGY IS REQUIRED TO IONIZE A GA IMPURITY ATOM THAN IS REQUIRED FOR A B IMPURITY ATOM. SINCE THERMAL ENERGY IS PROPORTIONAL TO TEMPERATURE, T_1 INCREASES AS ACTIVATION ENERGY INCREASES.

AT T_1 ALL IMPURITY ATOMS ARE CONSIDERED IONIZED. SINCE A CONSTANT NUMBER OF CARRIERS ARE PRESENT, THE RESISTIVITY WILL INCREASE AS

A. DISCUSSION OF IMPURITY CONDUCTION MECHANISMS (CONT'D)

THE MOBILITY IS DECREASED DUE TO LATTICE VIBRATIONS OF THE CRYSTAL. THE MOBILITY CAN BE THOUGHT OF AS THE AVERAGE DRIFT VELOCITY WHICH A CARRIER (OR THE WAVE ASSOCIATED WITH IT) ACQUIRES IN THE DIRECTION OF AN APPLIED ELECTRIC FIELD OF ONE VOLT PER CENTIMETER. THE LATTICE VIBRATIONS DECREASE THE MEAN FREE PATH OF THE WAVES ASSOCIATED WITH THESE CARRIERS AND HENCE DECREASE THE MOBILITY.

AS THE TEMPERATURE IS INCREASED FROM T_1 , CARRIERS FROM THE SEMICONDUCTOR ATOMS ARE ACTIVATED DUE TO THE INCREASED THERMAL ENERGY AVAILABLE. THE IMPURITY CONDUCTION DOMINATES UNTIL THE NUMBER OF CARRIERS FROM THE SEMICONDUCTOR ATOMS APPROACHES THE NUMBER OF CARRIERS FROM THE IONIZED IMPURITIES. THIS OCCURS IN THE REGION OF T_2 . AS MORE AND MORE CARRIERS ARE ACTIVATED FROM THE SEMICONDUCTOR ATOMS, THE RESISTIVITY STARTS TO DROP SINCE THE NUMBER OF CARRIERS IS INCREASING AT A FASTER RATE THAN THE MOBILITY IS DECREASING DUE TO LATTICE VIBRATIONS. AT SOME TEMPERATURE, T_3 , THE POINT IS REACHED WHERE THE SEMICONDUCTOR GOES INTRINSIC. THIS MEANS THAT ABOVE THIS TEMPERATURE THE TEMPERATURE COEFFICIENT OF RESISTANCE IS HIGHLY NEGATIVE AND DEPENDENT ONLY ON THE SEMICONDUCTOR BAND GAP. THE TEMPERATURE T_3 , AT WHICH THE MATERIAL BECOMES INTRINSIC IS DEPENDENT ON THE DOPING LEVEL AND DOPING TYPE AS SEEN FROM THE PRECEDING DISCUSSION.

I. PURPOSE (CONTINUED)

B. APPROACHES TO DEVELOPMENT OF LOW TCR ELEMENT

IN GENERAL, THREE APPROACHES WERE CONSIDERED IN PHASE II FOR DEVELOPING THE SILICON LAYER ELEMENT. THE FIRST OF THE TECHNIQUES INVESTIGATED WAS DIFFUSION, WHERE THE RESISTIVE LAYER IS FORMED BY DIFFUSING IMPURITIES INTO HIGH RESISTIVITY SINGLE-CRYSTAL SUBSTRATES. THE OTHER TWO APPROACHES WERE VAPOR DEPOSITION TECHNIQUES FORMING SINGLE-CRYSTAL (EPITAXIAL) ELEMENTS OR POLYCRYSTALLINE LAYERS DEPOSITED ON CERAMIC SUBSTRATES.

SOME OF THE ADVANTAGES AND DISADVANTAGES OF THE THREE APPROACHES MAY BE REITERATED.

ADVANTAGES

DISADVANTAGES

1. DIFFUSED

A.) THE LAYER IS AN INTEGRAL PART OF THE SUBSTRATE, I.E., IT IS A MONOLITHIC STRUCTURE.

A.) DOPING TO AN EXACT CONCENTRATION (E.G., 4.5×10^{18} AT./CC) BY DIFFUSION MIGHT NOT BE EASILY PRODUCED.

B.) SHEET RESISTANCE MAY BE RAISED TO A REASONABLE MAGNITUDE (500 OHMS PER SQUARE) WITHOUT ENCOUNTERING PROBLEMS ASSOCIATED WITH THIN-FILM ELEMENTS. THIS GOES BACK TO THE FACT THAT THE RESISTIVE LAYER IS PHYSICALLY THE SAME AS THE SUBSTRATE.

B.) JUNCTION CONFIGURATIONS ARE SENSITIVE TO SURFACE CONTAMINATION WHICH OFTEN CAUSES CURRENT LEAKAGE ACROSS THE JUNCTION.

C.) SINGLE-CRYSTAL SILICON SUBSTRATE WOULD BE MORE EXPENSIVE THAN CERAMIC.

2. EPITAXIAL (VAPOR DEPOSITED ON SINGLE CRYSTAL SUBSTRATE)

A.) THE LAYER IS AN INTEGRAL PART OF THE SUBSTRATE, I.E., IT IS A MONOLITHIC STRUCTURE.

A.) JUNCTION CONFIGURATIONS ARE SENSITIVE TO SURFACE CONTAMINATION WHICH SOMETIMES CAUSES CURRENT LEAKAGE ACROSS THE JUNCTION.

2. EPITAXIAL (VAPOR DEPOSITED ON SINGLE CRYSTAL SUBSTRATE) (CONT'D)

- | | |
|--|--|
| B.) SHEET RESISTANCE MAY BE RAISED TO A REASONABLE MAGNITUDE (500 OHMS PER SQUARE) WITHOUT ENCOUNTERING PROBLEMS ASSOCIATED WITH THIN FILM ELEMENTS. THIS GOES BACK TO THE FACT THAT THE RESISTIVE LAYER IS PHYSICALLY THE SAME AS THE SUBSTRATE. | B.) ADJUSTMENT OF RESISTANCE VALUE WILL BE DIFFICULT (ETCHING TO A PRESCRIBED GEOMETRY OR ELECTRON BEAM CUTTING ARE TWO POSSIBLE METHODS). |
| C.) DISTRIBUTION OF IMPURITY ATOMS CLOSELY APPROXIMATES THAT OF CRYSTALS GROWN FROM MELT, HENCE A UNIFORMITY WITHIN THE LAYER IS OBTAINED. THIS MEANS THAT THE ELEMENT COULD BE ETCHED TO REDUCE LAYER THICKNESS (RAISING SHEET RESISTANCE) YET RETAIN THE SAME TCR CHARACTERISTICS. | C.) SINGLE CRYSTAL SILICON SUBSTRATE WOULD BE MORE EXPENSIVE THAN CERAMIC. |

3. POLYCRYSTALLINE (VAPOR DEPOSITED ON CERAMIC SUBSTRATE)

- | | |
|---|---|
| A.) A THICK-LAYER HAS LESS CHANCE FOR DEVELOPING HOT SPOTS WHICH COULD CAUSE CATASTROPHIC FAILURE. | A.) NOT MONOLITHIC WITH SUBSTRATE. SILICON AND ALUMINA CERAMIC HAVE DIFFERING THERMAL EXPANSION COEFFICIENTS ($\sim 1:2$). |
| B.) THERMAL CONDUCTIVITY OF THE CERAMIC SUBSTRATE IS GREATER THAN SILICON, HENCE WOULD SHOW GREATER DISSIPATION OF POWER. | B.) POLYCRYSTALLINE LAYER WOULD NOT BE AS EASILY CONTROLLED FROM A RESISTIVITY STANDPOINT AS WOULD EPITAXIAL. |
| C.) THE CERAMIC MATERIAL IS A LESS EXPENSIVE SUBSTRATE AND ALLOWS MORE FLEXIBILITY IN DESIGN. | C.) THE MINIMUM LAYER THICKNESS IS LIMITED FOR PRACTICAL REASONS TO GREATER THICKNESSES THAN EITHER DIFFUSED OR EPITAXIAL; THIS MEANS A LOWER POSSIBLE SHEET RESISTIVITY. |
| D.) RESISTANCE ADJUSTMENT IS MORE PRACTICAL. | |

THE MAJOR EFFORT OF THE DEVELOPMENT WORK HAS BEEN WITH THE VAPOR-DEPOSITION APPROACH. EARLY IN THE SECOND PHASE OF THE WORK IT BECAME APPARENT THAT THE DIFFUSED-LAYER APPROACH HAD MANY INHERENT PROBLEMS AND LIMITATIONS. THE FOREMOST OF THESE WAS THE JUNCTION EFFECT AND ITS ASSOCIATED TEMPERATURE DEPENDENCY, I.E., THE PROBLEM OF CURRENT LEAKAGE ACROSS THE P-N JUNCTION. THE ELECTRICAL ISOLATION

B. APPROACHES TO DEVELOPMENT OF LOW TCR ELEMENT (CONT'D)

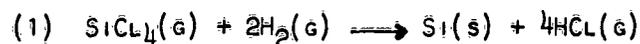
OF THE MORE CONDUCTIVE LAYER FROM ITS SUBSTRATE IS DEPENDENT UPON THE EFFECTIVENESS OF THE JUNCTION TO PREVENT CURRENT PASSAGE THROUGH OR ACROSS THE SURFACE OF THE JUNCTION. CONDUCTION ACROSS THE SURFACE WHICH EXPOSES THE LAYER-SUBSTRATE JUNCTION IS GREATLY INFLUENCED BY CLEANLINESS. CONTAMINATION REMAINING ON THE SURFACE OF P-N JUNCTIONS IS ONE OF THE MOST CRITICAL PROBLEMS IN THE FABRICATION OF SEMICONDUCTOR DEVICES. THE EFFECT OF JUNCTION LEAKAGE OF THE HIGH TEMPERATURES (ABOVE 100°C) SEVERELY AFFECTED THE TCR AT THE DIFFUSED ELEMENTS AND WOULD HAVE LIMITED THEIR USEFULNESS AT THESE ELEVATED TEMPERATURES. THE INABILITY TO REPRODUCE THE EXACT DOPING LEVEL OF THE DIFFUSED LAYER (HENCE ITS TCR CHARACTERISTICS) WAS ANOTHER MAJOR PROBLEM WITH THIS APPROACH.

VAPOR DEPOSITION BY PYROLYTIC REDUCTION OF A SILICON HALIDE WAS A MUCH MORE PRACTICAL APPROACH. THICKNESS OF THE SILICON LAYER AND CONCENTRATION OF THE IMPURITY (BORON FOR P-TYPE, PHOSPHORUS FOR N-TYPE) WAS MORE EASILY CONTROLLED THAN BY DIFFUSION. POLYCRYSTALLINE LAYERS GAVE INDICATION AT THE EARLY STAGES OF DEVELOPMENT OF HAVING MORE PROMISING TCR CHARACTERISTICS THAN THE SINGLE CRYSTAL (EPITAXIAL) MATERIAL. THERE WAS NOT THE PROBLEM OF JUNCTION EFFECTS WITH SILICON DEPOSITED ON INSULATING SUBSTRATES AND OHMIC CONTACTS TO THE ELEMENT COULD BE MADE MORE STABLE (MECHANICALLY). PRESENTED UNDER THE DETAILED FACTUAL DATA SECTION OF THIS REPORT WILL BE A DISCUSSION OF MORE SPECIFIC PROBLEMS ENCOUNTERED IN THE DEVELOPMENT OF THE SILICON LAYER ELEMENT.

I. PURPOSE (CONTINUED)

C. CHEMISTRY OF VAPOR DEPOSITION

AS IS WELL KNOWN, SILICON CAN BE PRODUCED BY THE HIGH TEMPERATURE REDUCTION OF SILICON HALIDES BY HYDROGEN. THE SIMPLIFIED EQUATION IS SHOWN BELOW:



IN A KINETIC SYSTEM SUCH AS THE SYSTEM USED IN THIS STUDY, THE REACTION IS COMPLICATED BY SEVERAL SIDE REACTIONS. THE TWO MOST PREVALENT SIDE REACTIONS ARE THE FORMATION OF CHLOROSILANES ($\text{SiH}_x\text{Cl}_{(4-x)}$) AND CHLOROSILANE POLYMERS $[\text{H}(\text{SiH}_x\text{Cl}_{2-x})_y\text{H}]$.

THE FORMATION OF CHLOROSILANES CAUSES NO DIFFICULTY IN THE FORMATION OF SILICON DEPOSITS SINCE THE CHLOROSILANES ARE GASEOUS IN THE REACTION SYSTEM AND ARE READILY SWEEPED FROM THE REACTION ZONE.

THE FORMATION OF CHLOROSILANE POLYMERS, HOWEVER, IS DETRIMENTAL TO THE FORMATION OF SILICON DEPOSITS SINCE THE POLYMERS MAY CODEPOSIT WITH THE SILICON AND CONTAMINATE THE DEPOSITED SILICON LAYER.

BOTH SIDE REACTIONS CAN BE CONTROLLED BY A JUDICIOUS CHOICE OF REACTION CONDITIONS. AT TEMPERATURES BELOW APPROXIMATELY 1050°C , POLYMERIC CHLOROSILANES ARE READILY FORMED. ABOVE 1050°C POLYMER FORMATION IS REDUCED TO A NON-DETECTABLE LEVEL IN THE SILICON DEPOSIT. THEREFORE, IF THE SILICON DEPOSITION IS CARRIED OUT AT TEMPERATURES IN EXCESS OF 1100°C , HIGH QUALITY SILICON DEPOSITS

C. CHEMISTRY OF VAPOR DEPOSITION (CONT'D)

FREE OF POLYMERIC CONTAMINATION ARE FORMED.

ACCORDING TO EQUATION (1) ABOVE, A MOLAR RATIO OF 2:1 OF HYDROGEN TO SILICON TETRACHLORIDE IS REQUIRED FOR THIS REACTION. A MOLAR RATIO LESS THAN 2:1 WOULD, OF COURSE, HINDER THE FORMATION OF SILICON AND TEND TO PRODUCE UNDESIRABLE BY-PRODUCTS. A MOLAR RATIO OF $H_2:SiCl_4$ GREATER THAN 2:1 WOULD BE EXPECTED TO "FORCE" THE REACTION TO THE RIGHT FAVORING THE FORMATION OF $Si(s)$.

ALTHOUGH THE HIGHER MOLAR RATIOS OF $H_2:SiCl_4$ MIGHT BE EXPECTED TO PROMOTE THE FORMATION OF SILANE (SiH_4), THIS POSSIBILITY CAUSES NO PROBLEMS. IF SILANE WERE FORMED IT IS A GASEOUS MATERIAL AND WOULD BE SWEEPED OUT OF THE REACTOR IN THE FLOWING GAS SYSTEM. ALSO, SILANE AND ITS HIGHER HOMOLOGS (E.G., Si_2H_6 , Si_3H_8 , ETC.) ARE THERMALLY UNSTABLE AND WOULD DECOMPOSE AT THE TEMPERATURES ENCOUNTERED IN THE REACTION ZONE TO FORM SILICON AND HYDROGEN.

IN PRACTICE A MOLAR RATIO OF HYDROGEN TO SILICON TETRACHLORIDE GREATER THAN TWENTY (20) IS EMPLOYED. NORMALLY, A SILICON TETRACHLORIDE CONCENTRATION BETWEEN ONE (1) AND FOUR (4) MOLE PER CENT IN HYDROGEN IS USED.

SAMPLE CALCULATION OF IMPURITY DOPING LEVEL FOR $SiCl_4$:

IF THE DESIRED IMPURITY LEVEL IS 5.0×10^{19} AT./CC P IN SI, (SEE FIGURE 4), THIS WOULD BE EQUIVALENT TO APPROXIMATELY .002 OHMS-CM MATERIAL.

C. CHEMISTRY OF VAPOR DEPOSITION (CONT'D)

$$\text{Si: } \frac{2.33 \text{ g/cc}}{28.09 \text{ g/g-ATOM}} \times 6.02 \times 10^{23} \text{ AT./G-ATOM} = 5.00 \times 10^{22} \text{ AT./CC}$$

$$\frac{5.0 \times 10^{19} \text{ AT./CC (P)}}{5.0 \times 10^{22} \text{ AT./CC (Si)}} \times 100 = .10 \text{ MOLE \% P IN Si}$$

$$\text{SiCl}_4: \frac{1.48 \text{ g/cc}}{169.89 \text{ g/MOLE}} \times 6.02 \times 10^{23} \text{ MOLECULES/MOLE} =$$

$$5.24 \times 10^{21} \text{ MOLECULES/CC OR } 5.24 \times 10^{24} \text{ MOLECULES/LITER.}$$

$$\text{PCl}_3 \text{ NEEDED TO DOPE SiCl}_4 \text{ TO THE PREDETERMINED LEVEL } .10 \times 10^{-2} \times \\ 5.24 \times 10^{24} \text{ MOLECULES/LITER} = 5.24 \times 10^{21} \frac{\text{MOLECULES OF PCl}_3}{\text{LITER OF SiCl}_4}.$$

$$\text{PCl}_3 \frac{1.57 \text{ g/cc}}{137.39 \text{ g/MOLE}} \times 6.02 \times 10^{23} \text{ MOLECULES/MOLE} =$$

$$6.88 \times 10^{21} \text{ MOLECULES/CC.}$$

$$\frac{5.24 \times 10^{21} \text{ MOLECULES OF PCl}_3/\text{LITER OF SiCl}_4}{6.88 \times 10^{21} \text{ MOLECULES OF PCl}_3/\text{CC OF PCl}_3} =$$

$$0.76 \text{ CC OF PCl}_3/\text{LITER OF SiCl}_4.$$

THIS CALCULATION ASSUMES THAT THE MOLAR RATIO OF PCl₃ IN SiCl₄ IN THE FEED MIXTURE WILL BE DUPLICATED AS A P IN Si RATIO IN THE PYROLYTIC DEPOSIT.

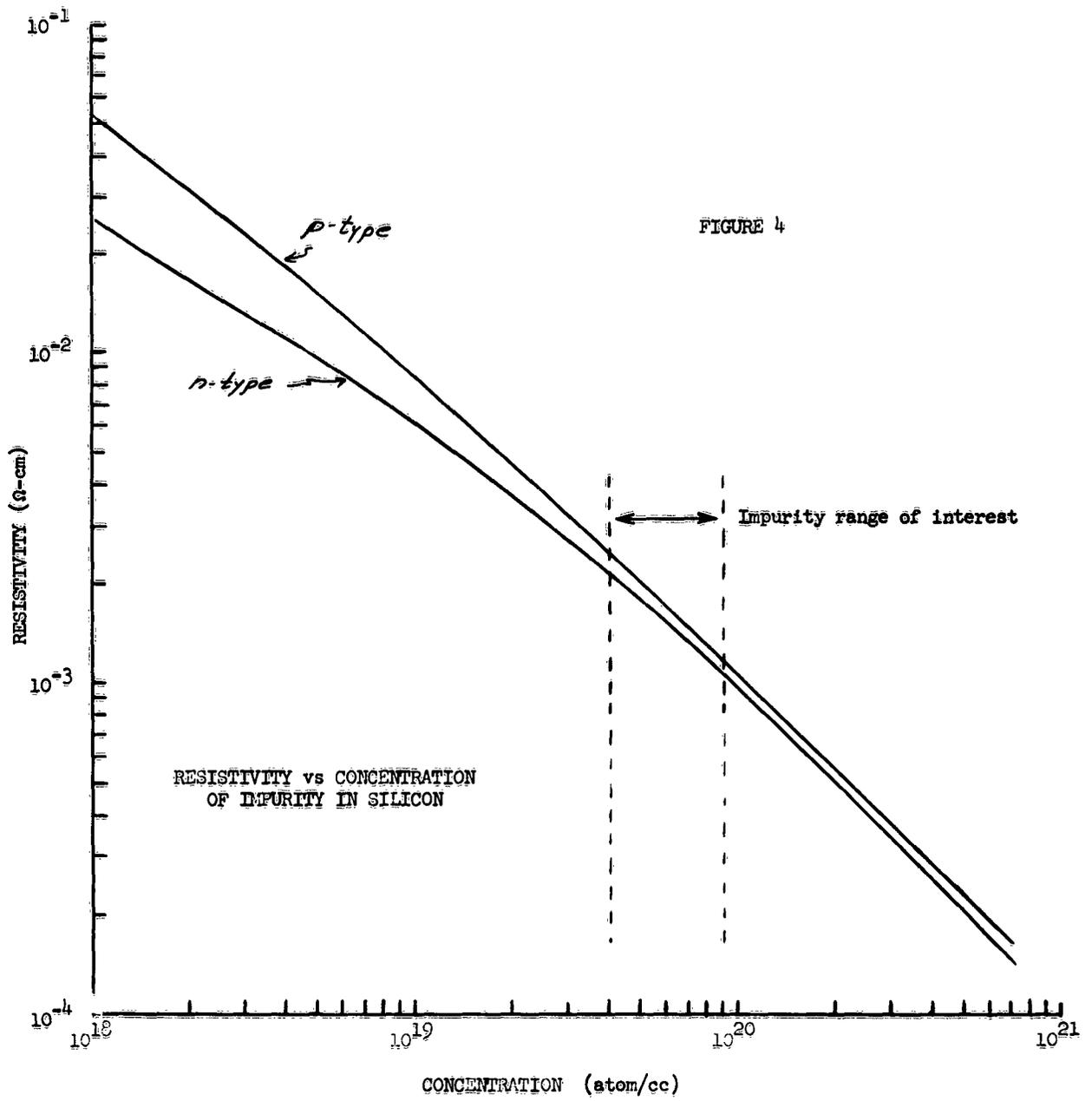


FIGURE 4

FIGURE 4

II. GENERAL FACTUAL DATA

A. IDENTIFICATION OF TECHNICAL CONTRIBUTORS

<u>ENGINEERS</u>	<u>MAN HOURS, LAST QUARTER</u>
R. W. WESTBROOK	555
R. A. ROQUES	486
B. L. KENNIMER	212
B. G. CARBAJAL	140

<u>TECHNICIANS</u>	
J. K. HOCKER	382

<u>ASSEMBLERS</u>	
N. R. RICHARDSON	232
W. B. HALDEMAN	169
J. A. DAVIS	140
C. M. SHOTWELL	133

B. REFERENCES

FIRST, SECOND (FINAL FOR PHASE I), THIRD, FOURTH, AND FIFTH
QUARTERLY REPORTS FOR THIS CONTRACT:

- BACKENSTOSS, G., "EVALUATION OF SURFACE CONCENTRATION OF
DIFFUSED LAYERS IN SILICON", BELL SYSTEMS TECHNICAL JOURNAL,
37 699-718 (1958)
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II. GENERAL FACTUAL DATA

C. MEASUREMENT PROCEDURES

MIL-R-10509D, CHARACTERISTIC C, HAS BEEN USED AS A GUIDE IN TESTING FINISHED DEVICES. FOR EVALUATION OF THE RESISTIVE ELEMENT THE FOLLOWING SPECIAL EQUIPMENT WAS USED:

<u>TEST</u>	<u>EQUIPMENT</u>
1. SHEET RESISTANCE	FOUR-POINT PROBE TEST SET,
2. THICKNESS OF LAYER	LAPPING APPARATUS, MICROSCOPE
NOTE: AN EXAMPLE OF A SILICON LAYER PHOTOGRAPHED UNDER SODIUM LIGHT FOR THICKNESS MEASUREMENT MAY BE SEEN IN THE SUPPLEMENTARY DATA SECTION.	WITH CAMERA ATTACHMENT, SODIUM LIGHT SOURCE.
3. TCR	SILICONE OIL BATHS, TEMPERATURE CONTROLS, CHAMBER FOR LOW TEMPERATURES.

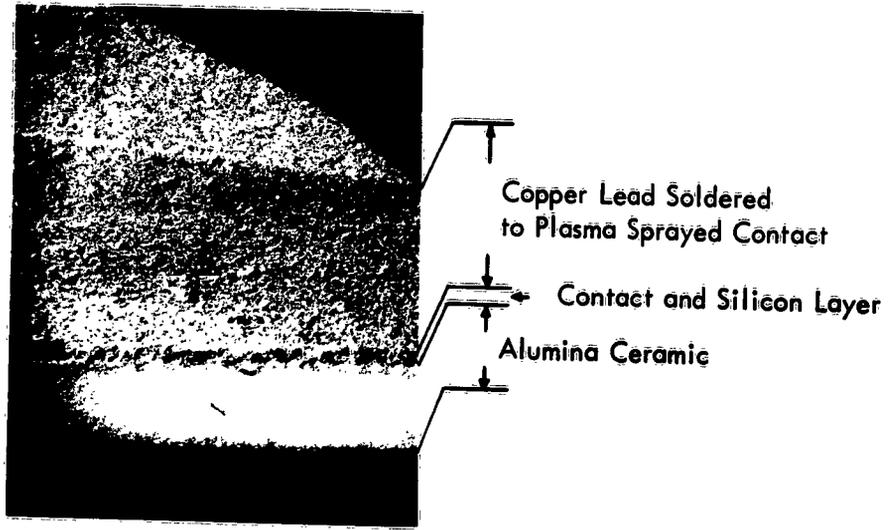
III. DETAILED FACTUAL DATA

A. SPECIFIC PROBLEM AREAS

1. OHMIC CONTACTS:

PERHAPS THE MOST CRITICAL PROBLEM TO BE SOLVED IN THE DEVELOPMENT OF THE SILICON RESISTIVE ELEMENT, OTHER THAN THE FUNDAMENTAL PROBLEM OF MINIMIZING TCR, WAS THAT OF PROVIDING ELECTRICALLY AND MECHANICALLY STABLE CONTACTS. MOST OF THE VARIATION IN RESISTANCE UNDER LOAD CONDITIONS RELATED TO INSTABILITY OF THE OHMIC CONTACT TO THE SILICON ELEMENT.

THREE METHODS FOR MAKING OHMIC CONTACT WERE EVALUATED; NICKEL PLATING, GOLD AND PALLADIUM EVAPORATION, AND PLASMA SPRAYING OF ALUMINUM AND COPPER. OF THESE, THE PLASMA-SPRAYED AL-CU AND SOLDERED LEAD ATTACHMENT PROVED TO BE THE MOST RELIABLE. THE OTHER TWO METHODS, PLATING AND EVAPORATION, RESULTED IN OHMIC CONTACTS BUT DID NOT HAVE THE NECESSARY MECHANICAL STRENGTH FOR GOOD STABILITY. LEAD WIRES ARE NORMALLY BALL-BONDED, A THERMOCOMPRESSION-TYPE BOND, TO THE EVAPORATED METAL AREAS. THIS TECHNIQUE IS USED FOR MAKING OHMIC CONTACT TO SILICON NETWORK DEVICES BUT WAS NOT SUFFICIENTLY SUBSTANTIAL FOR THE HIGHER POWER REQUIREMENTS OF A DISCRETE RESISTOR. LOAD LIFE DATA AND NOISE MEASUREMENTS WERE USED TO EVALUATE THE CONTACT METHODS (SEE SUPPLEMENTARY DATA SECTION). A MICROPHOTOGRAPH OF A CROSS-SECTION THROUGH THE PLASMA-SPRAYED SOLDER CONTACT MAY BE SEEN IN FIGURE 5.



Cross-Section of Contact Area
Polycrystalline Silicon on Ceramic
(50 X)

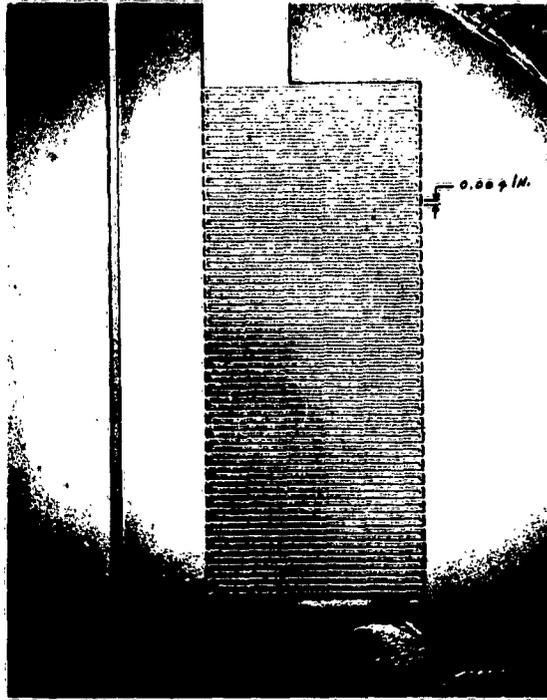
FIGURE 5

A. SPECIFIC PROBLEM AREAS

2. RESISTANCE ADJUSTMENT:

THE DEVELOPMENT OF THE SEMICONDUCTOR ELEMENT WAS TO BE DIRECTED TOWARD A MORE RELIABLE METHOD OF ADJUSTING THE VALUE OF RESISTANCE THAN BY PURELY MECHANICAL MEANS (SUCH AS SPIRALLING WITH AN ABRASIVE WHEEL) WHICH IS STANDARD PRACTICE FOR CARBON AND METAL FILM RESISTORS. TWO TECHNIQUES FOR ADJUSTING THE RESISTANCE OF THE SILICON ELEMENT WERE INVESTIGATED. THE FIRST WAS A STANDARD TECHNIQUE EMPLOYED IN MOST SEMICONDUCTOR DEVICE FABRICATION WORK; I.E., MASKING AND ETCHING. THE SECOND WAS THE MORE NOVEL APPROACH OF ELECTRON BEAM SCRIBING.

THE PHOTO-MASKING AND ETCHING TECHNIQUE WAS DESCRIBED IN DETAIL IN PREVIOUS REPORTS. TO PRODUCE A PREDETERMINED RESISTANCE VALUE REQUIRED A PRESCRIBED PATTERN ON THE PHOTOGRAPHIC MASK. CHEMICAL ETCHING SIMPLY REMOVES THE SILICON WHICH HAS NOT BEEN PROTECTED BY THE EXPOSED AND DEVELOPED RESIN (KMER, KODAK METAL ETCH RESIST). KMER IS A PHOTO-SENSITIVE RESIN WHICH, AFTER POLYMERIZATION, HAS EXCELLENT ACID RESISTANCE. USING THIS TECHNIQUE IT WAS POSSIBLE TO OBTAIN PATTERNS WITH LINES AND SPACINGS AS NARROW AS 2 MILS (.002") WITH GOOD DEFINITION. BASE VALUES OF APPROXIMATELY 50 OHMS COULD BE ETCHED TO VALUES OF 100K AND ABOVE. (SEE MICROPHOTOGRAPHS OF ETCHED PATTERNS ON SINGLE-CRYSTAL AND POLYCRYSTALLINE SILICON IN FIGURES 6 AND 7 RESPECTIVELY.)



Etched Pattern of Single (Epitaxial) Crystal Silicon Layer
FIGURE 6



Etched Pattern of Polycrystalline Silicon Layer
FIGURE 7

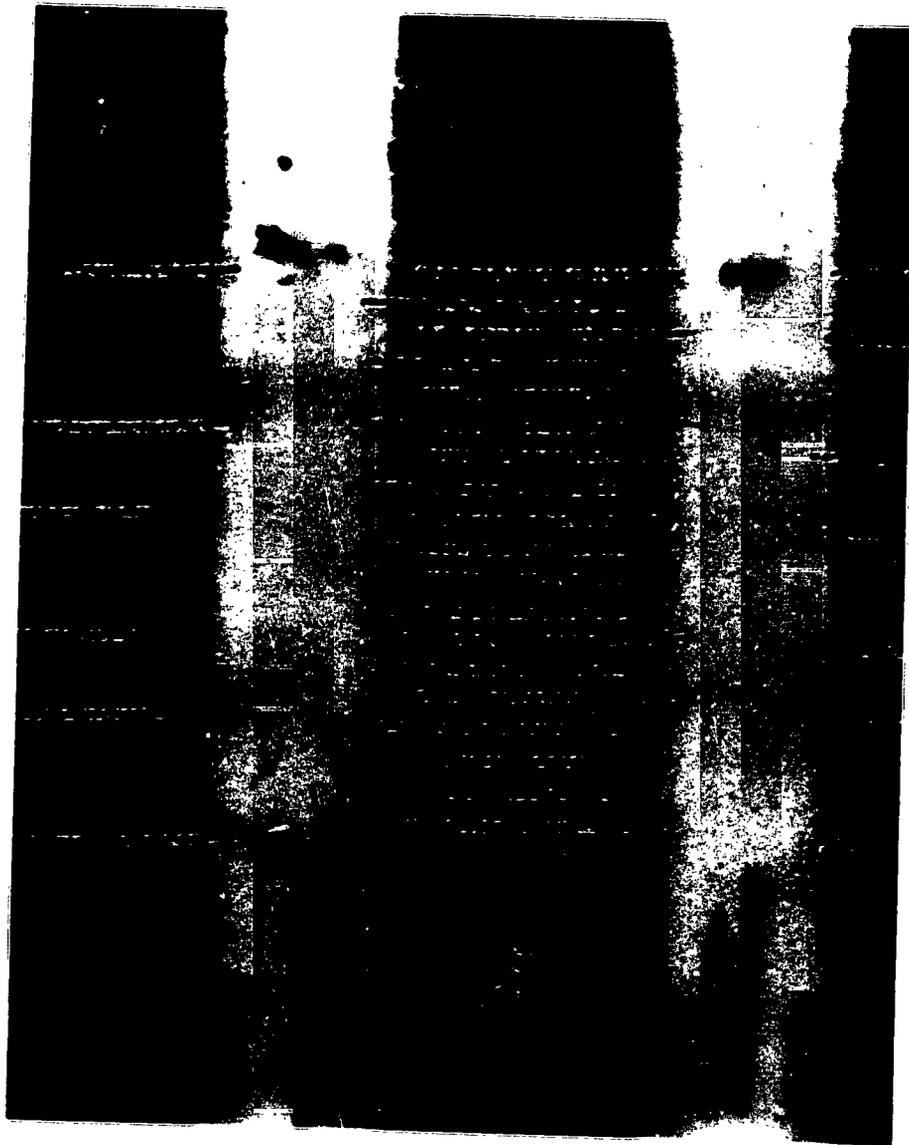
A. SPECIFIC PROBLEM AREAS (CONT'D)

ELECTRON BEAM SCRIBING WAS DONE WITH A MACHINE BUILT BY THE ZEISS COMPANY IN GERMANY. THE TECHNIQUE COMBINES MELTING AND EVAPORATION BY A HIGH-INTENSITY ELECTRON BEAM WHICH CAN BE FOCUSED IN A CONTROLLABLE MANNER. THE EQUIPMENT ALLOWS THE SUBSTRATE TO BE MANEUVERED FOR SCRIBING (OR WELDING) PRE-DETERMINED PATTERNS. BOTH SINGLE AND POLYCRYSTALLINE ELEMENTS WERE SCRIBED BY THIS TECHNIQUE TO LENGTHEN AND NARROW THE RESISTANCE PATH, THUS INCREASING THE RESISTANCE VALUE OF THE ELEMENT. FIGURE 8 SHOWS AN EXAMPLE OF SCRIBING POLYCRYSTALLINE SILICON (DEPOSITED ON AN ALUMINA CERAMIC SUBSTRATE).

OF THE TWO METHODS, PHOTO MASKING AND ETCHING WAS EMPLOYED AS THE PRINCIPAL MEANS OF INCREASING THE RESISTANCE ABOVE BASE VALUES, SINCE THE TECHNIQUE WAS ALREADY KNOWN AND PRACTICED IN THE IMMEDIATE LABORATORY AREA. THE POTENTIAL ADVANTAGE OF ELECTRON BEAM SCRIBING AS A METHOD OF ADJUSTING THE RESISTANCE WHILE MONITORING THE VALUE WAS NOT OVERLOOKED. THE ZEISS ELECTRON BEAM EQUIPMENT WAS A RESEARCH MODEL WHICH WAS NOT READILY AVAILABLE. THE SCRIBING OF ANY LARGE NUMBER OF ELEMENTS WOULD NOT HAVE BEEN AS PRACTICAL AS THE ETCHING TECHNIQUE.

3. INCREASED SHEET RESISTANCE:

ONE SERIOUS LIMITATION OF THE SILICON RESISTIVE ELEMENT WAS THE LOW RESISTIVITY NECESSARY FOR LOW TCR, WHICH IN TURN YIELDED LOW SHEET RESISTANCE OF THE DEPOSITED LAYER. BULK RESISTIVITY OF



Electron-Beam Scribed Polycrystalline Silicon Layer
FIGURE 8

3. INCREASED SHEET RESISTANCE (CONT'D)

MATERIAL FOUND TO BE OPTIMUM FOR GOOD TCR CHARACTERISTICS WAS APPROXIMATELY .002 OHM-CM. SHEET RESISTANCE VALUES FOR THICKNESSES OF ABOUT THREE MICRONS (APPROX .12 MILS) WAS ABOUT EIGHT (8) Ω /SQ ON SINGLE CRYSTAL (EPITAXIAL) LAYERS. THE POLYCRYSTALLINE MATERIAL OF COMPARABLE THICKNESS GAVE HIGHER SHEET RESISTANCE VALUES (APPROX 20 Ω /SQ) FOR THE SAME DOPING LEVEL.

ATTEMPTS WERE MADE TO INCREASE THE SHEET RESISTANCE OF DIFFUSED LAYER ELEMENTS BY MORE SHALLOW DIFFUSIONS INTO THE SILICON SUBSTRATE. VALUES AS HIGH AS 300 Ω /SQ WERE OBTAINED ON DIFFUSED ELEMENTS, BUT THE UNCERTAINTY OF REPEATING THESE RESULTS COUPLED WITH GENERALLY UNSTABLE RESISTANCE VALUES MADE THESE ATTEMPTS UNFRUITFUL.

THE PROBLEM OF INCREASING THE SHEET RESISTANCE OF DEPOSITED SILICON LAYERS WAS NEVER SATISFACTORILY RESOLVED. THE QUESTION STILL UNANSWERED IS, WHAT MINIMUM THICKNESS OF SILICON MAY BE DEPOSITED WITHOUT SACRIFICING RELIABILITY OF THE RESISTIVE ELEMENT. IMPROVED STABILITY OF THE SEMICONDUCTOR LAYER ELEMENTS IS BASED ON GREATER THICKNESS OF THE SILICON RELATIVE TO METAL OR CARBON FILM ELEMENTS. TO DECREASE THICKNESS WOULD PRESUMABLY REDUCE THE RELIABILITY OF THE ELEMENT, SINCE THE MAGNITUDE OF THICKNESS WOULD APPROACH THAT OF THIN FILM ELEMENTS AND NOT BE ANY MORE RELIABLE FROM THE STANDPOINT OF OVERLOAD CAPABILITIES.

A. SPECIFIC PROBLEM AREAS (CONT'D)

4. JUNCTION PROBLEMS:

MENTIONED EARLIER WERE THE DIFFICULTIES ENCOUNTERED WITH DIFFUSED AND EPITAXIAL ELEMENTS DUE TO THE P-N JUNCTION SURFACE EFFECTS. THE REVERSE CURRENT LEAKAGE, UNRELATED TO ZENER OR AVALANCHE BREAKDOWN, IN A P-N JUNCTION CAN BE APPRECIABLE IF THE SURFACE OF THE SEMICONDUCTOR MATERIAL IS CONTAMINATED WITH RESIDUAL CHEMICALS (METALLIC SALTS, ETC.) WHICH ARE CONDUCTIVE. IN THE MANUFACTURE OF DIODES, RECTIFIERS, ETC., EXTREME CARE MUST BE EXERCISED TO KEEP THE JUNCTION SURFACE CLEAN AND TO PASSIVATE THE SURFACE (BY THERMAL OXIDATION, FOR EXAMPLE) OF THE MATERIAL. THE PROBLEM OF INSTABILITY OF RESISTANCE, IN THE EVALUATION OF DIFFUSED ELEMENTS, WAS BELIEVED TO BE RELATED TO THE SENSITIVITY OF THE JUNCTION WHICH ISOLATES THE MORE HIGHLY DOPED LAYER FROM ITS SUBSTRATE. SURFACE PROTECTION WITH SILICONE VARNISH HELPED MINIMIZE THE CURRENT LEAKAGE AT HIGHER TEMPERATURES, BUT ROOM TEMPERATURE INSTABILITY REMAINED A PROBLEM.

OHMIC CONTACTS TO THE DIFFUSED AND EPITAXIAL ELEMENTS WERE ALSO COMPLICATED BY THE PRESENCE OF THE P-N JUNCTION. IN SOME CASES THE ALLOYED CONTACT WOULD PENETRATE THE LAYER TO THE SUBSTRATE AND THUS INTRODUCE A PARALLEL RESISTANCE WITH THE RESISTIVE LAYER ITSELF. ELEMENTS WHICH WERE FORMED BY VERY SHALLOW DIFFUSIONS WERE ESPECIALLY PRONE TO DO THIS. THIS CONTACT PROBLEM DID NOT EXIST WITH ELEMENTS DEPOSITED

4. JUNCTION PROBLEMS (CONT'D)

ON INSULATING SUBSTRATES.

5. SHIFTING TCR ON PACKAGING:

A PROBLEM OF NON-REPRODUCIBILITY OF TCR CHARACTERISTICS BECAME CRITICAL IN THE LAST QUARTER. THE TCR UNENCAPSULATED ELEMENTS WERE FOUND TO INCREASE AS MUCH AS 125 PPM/°C (AT 65°C AND 175°C) AFTER MOLDING IN THE FINAL PACKAGE. THE INCREASE IN RESISTANCE AND TCR WAS DUE TO A PIEZORESISTIVE EFFECT CAUSED BY AN INDUCED STRESS IN THE SILICON ELEMENT. THE STRESS RESULTED FROM CONTRACTION OF THE EPOXY POTTING COMPOUND AS THE DEVICE WAS COOLED FROM 200°C (FINAL CURE TEMPERATURE) TO ROOM TEMPERATURE.

EVIDENCE OF THE PIEZORESISTIVE EFFECT IN THE SILICON ELEMENTS MAY BE SEEN FROM PLOTS OF RESISTANCE VERSUS TEMPERATURE BEFORE AND AFTER ENCAPSULATION. (SEE FIGURE 9) THE SOLUTION TO THE PROBLEM WAS TO USE A RESILIENT, LOWER SHRINKAGE, EPOXY AS THE FINAL ENCAPSULATION.

B. RESISTANCE-TEMPERATURE CHARACTERISTICS

1. DIFFUSED ELEMENTS:

TYPICAL R-T CURVES FOR GALLIUM DIFFUSED ELEMENTS OF VARYING SURFACE CONCENTRATION MAY BE SEEN IN FIGURE 10. THE SHEET RESISTANCE OF THESE ELEMENTS RANGED FROM 50 TO 100 Ω/SQ.

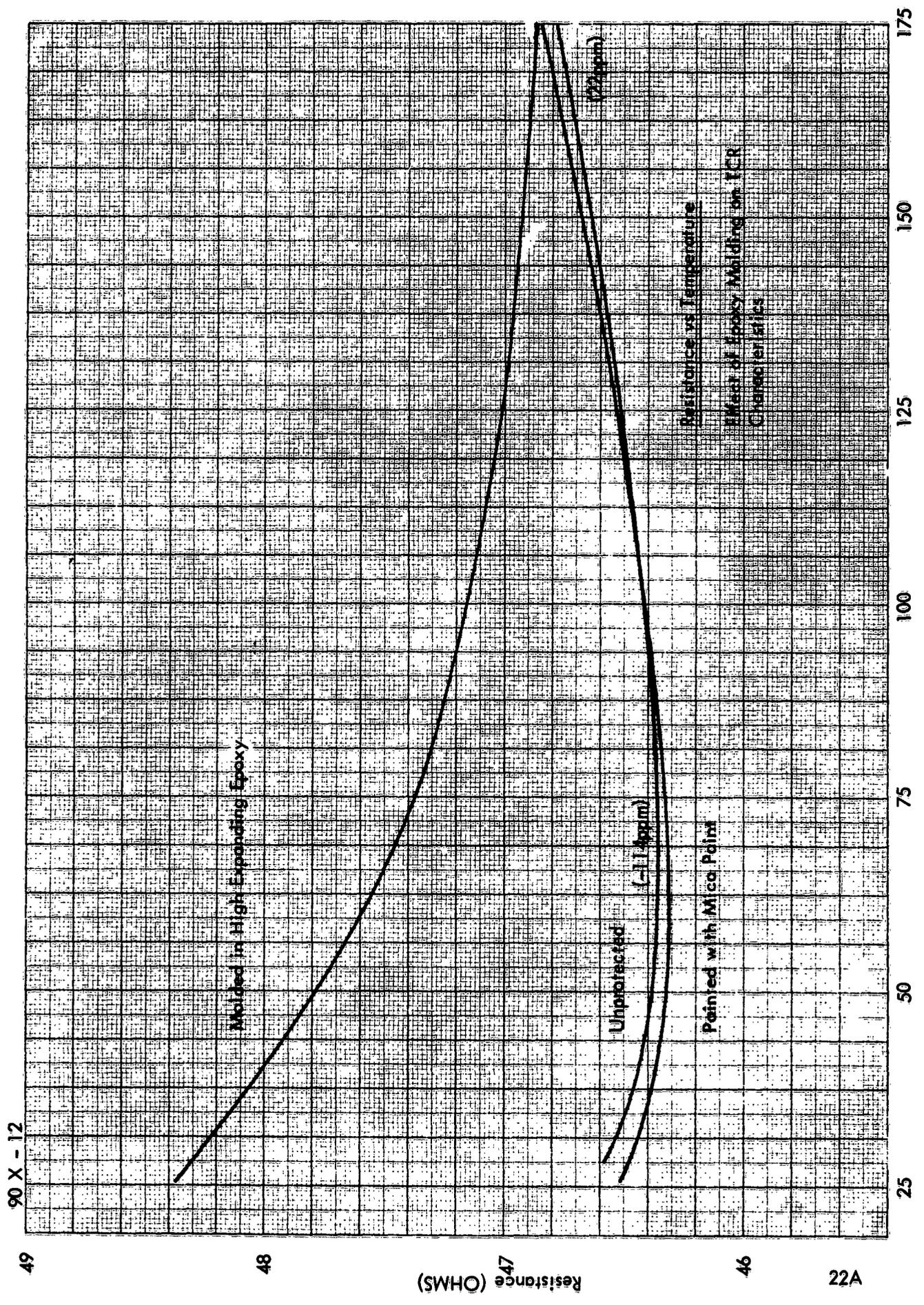
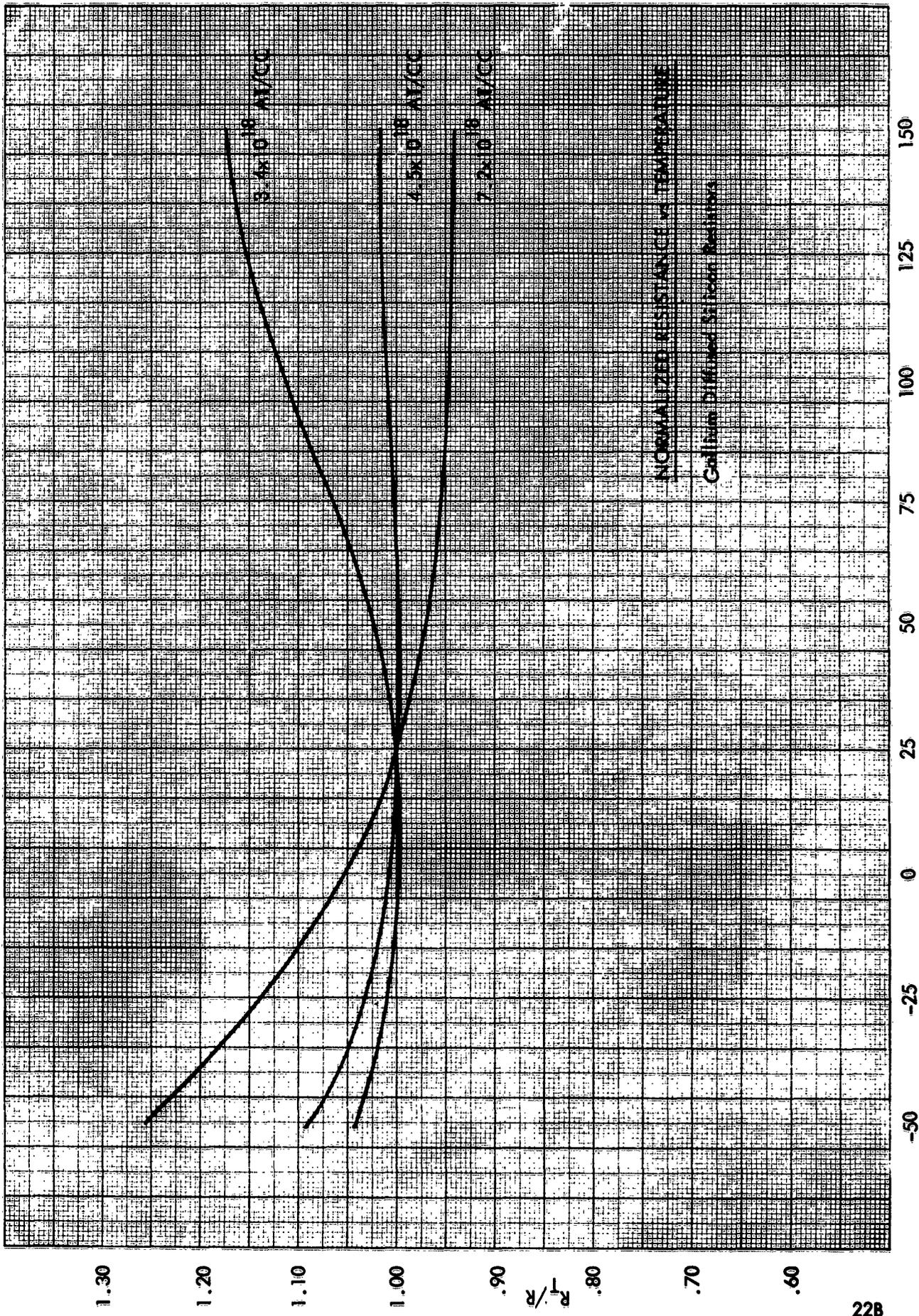


FIGURE 9 TEMPERATURE (°C)



NORMALIZED RESISTANCE vs TEMPERATURE
 Chromium Diffused Silicon Resistors

FIGURE 10 TEMPERATURE ($^{\circ}\text{C}$)

1. DIFFUSED ELEMENTS (CONT'D)

JUNCTION DEPTH WAS APPROXIMATELY 0.3 MILS (.0003"). MINIMUM TCR VALUES WERE OBSERVED AT GA CONCENTRATIONS OF APPROXIMATELY 5×10^{18} ATOMS/CC. A HIGHLY NEGATIVE TCR BELOW ROOM TEMPERATURE WAS CHARACTERISTIC FOR ALL CONCENTRATIONS OF GA INVESTIGATED. THIS LOW TEMPERATURE BEHAVIOR IS A FUNCTION OF THE ACTIVATION ENERGY OF THE MAJORITY CARRIERS IN THE SEMICONDUCTOR MATERIAL. AS THE IMPURITY ATOMS ARE IONIZED WITH INCREASING TEMPERATURE, THE RESISTIVITY DECREASES RAPIDLY FROM -50°C TO 25°C .

THE RATE OF DECREASE IN RESISTIVITY WITH TEMPERATURE IN THIS LOW TEMPERATURE REGION IS PROPORTIONAL TO THE AMOUNT OF THERMAL ENERGY NEEDED TO COMPLETELY IONIZE THE CARRIERS - WHICH, IN TURN, IS A FUNCTION OF THE THERMAL ACTIVATION ENERGY OF PRE-DOMINANT IMPURITY ATOMS. GALLIUM HAS AN ACTIVATION ENERGY IN SILICON OF .065 EV.

2. EPITAXIAL ELEMENTS:

FIGURE 11 SHOWS RESISTANCE-TEMPERATURE CURVES FOR EPITAXIAL SILICON OF APPROXIMATELY THE SAME PHOSPHORUS DOPING LEVEL DEPOSITED AT TWO THICKNESSES. BY GROWING A VERY THIN (APPROXIMATELY 0.1 MIL, .0001") LAYER EPITAXIAL ELEMENT, THE SHEET RESISTANCE WAS INCREASED TO ABOUT $100 \Omega/\text{SQ}$. THE IMPROVEMENT IN TCR CHARACTERISTIC IS BELIEVED TO BE DUE TO THE HIGH DISLOCATION DENSITY AT THE INTERFACE OF THE THINNER LAYER. IN THE THINNER LAYER, MOST OF THE CONDUCTION OCCURS IN THIS HIGH DISLOCATION

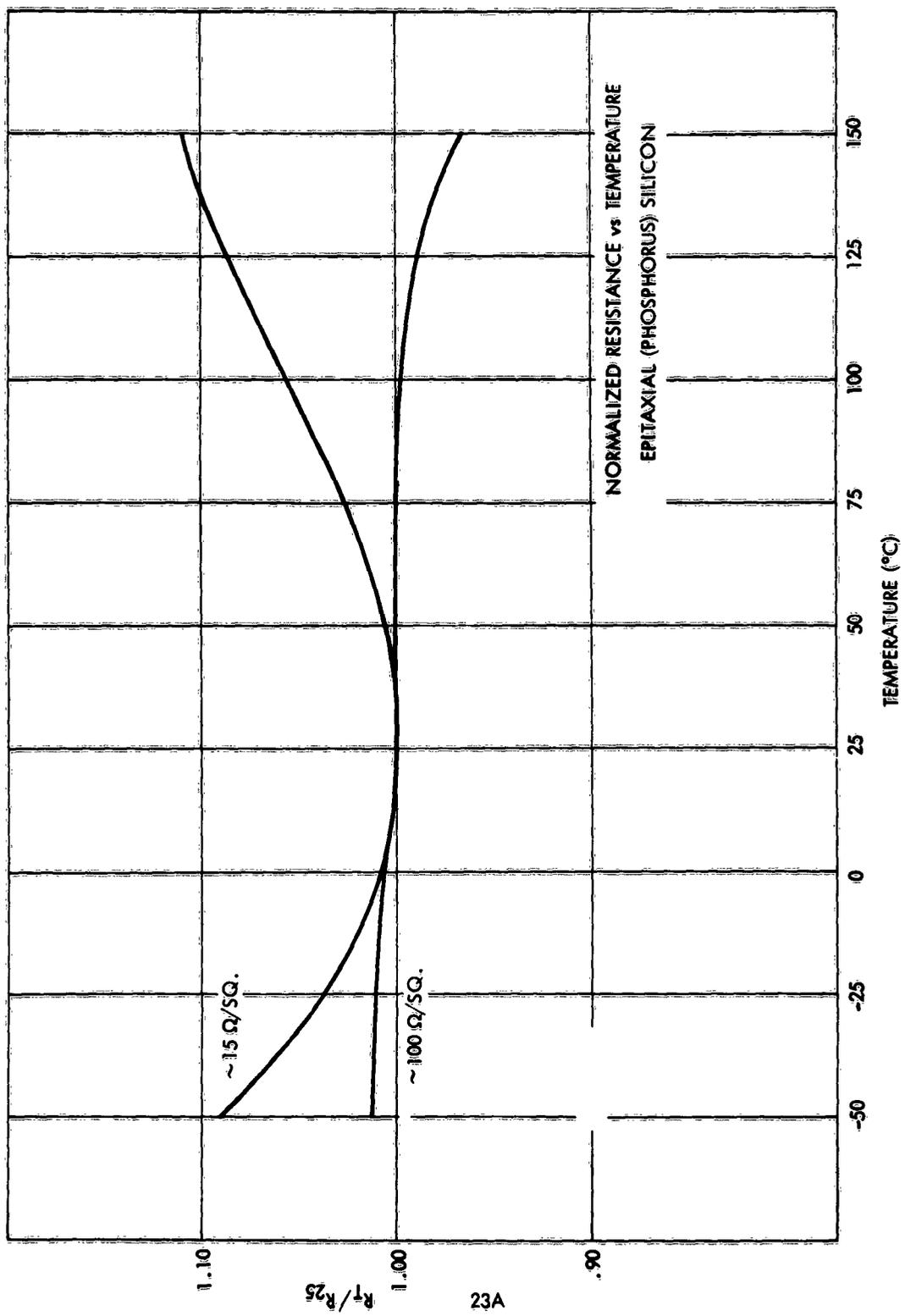


FIGURE 11

2. EPITAXIAL ELEMENTS (CONT'D)

REGION AND THE CONDUCTION MECHANISM IS DETERMINED MAINLY BY THE DISLOCATIONS. IN THE THICK LAYER MOST OF THE CONDUCTION OCCURS AWAY FROM THE INTERFACE AND THE CONDUCTION MECHANISM, WITH REFERENCE TO TEMPERATURE CHANGES, IS MORE TYPICAL OF BULK ELEMENTS. AS STATED PREVIOUSLY, THE TEMPERATURE DEPENDENCE OF THE JUNCTION LEAKAGE ALSO HAS AN EFFECT ON THE BEHAVIOR OF THE RESISTANCE AT THE HIGHER TEMPERATURES.

IN THE COURSE OF THE WORK IT BECAME APPARENT THAT THE TCR CHARACTERISTICS OF SINGLE CRYSTAL LAYERS WERE NOT SUFFICIENTLY REPRODUCIBLE, NOR WERE TCR VALUES AS LOW AS COULD BE OBTAINED WITH POLYCRYSTALLINE ELEMENTS.

3. POLYCRYSTALLINE ELEMENTS:

FIGURE 12 IS A TYPICAL CURVE FOR AN N-TYPE POLYCRYSTALLINE SILICON ELEMENT. MINIMUM TCR VALUES FOR POLYCRYSTALLINE ELEMENTS WERE OBTAINED AT DOPING LEVELS OF APPROXIMATELY 5×10^{19} ATOMS/CC OF PHOSPHORUS. FURTHER INCREASE IN DOPANT DID NOT IMPROVE THE OVER ALL CHARACTERISTICS OF THE TCR CURVE. THE SHAPE OF THE CURVE (NORMALIZED RESISTANCE VS TEMPERATURE) APPEARED TO BE AN INHERENT CHARACTERISTIC OF ALL THE POLYCRYSTALLINE ELEMENTS EVALUATED. VARYING THE AMOUNT OF DOPANT IN THIS HIGHLY DOPED REGION (10^{19} TO 10^{20} AT./CC) TENDED TO SHIFT THE MINIMUM POINT ON THE CURVE BUT DID NOT IMPROVE THE OVER ALL TCR CHARACTERISTICS. FIGURE 13 IS A CONTINUOUS PLOT

77x-6

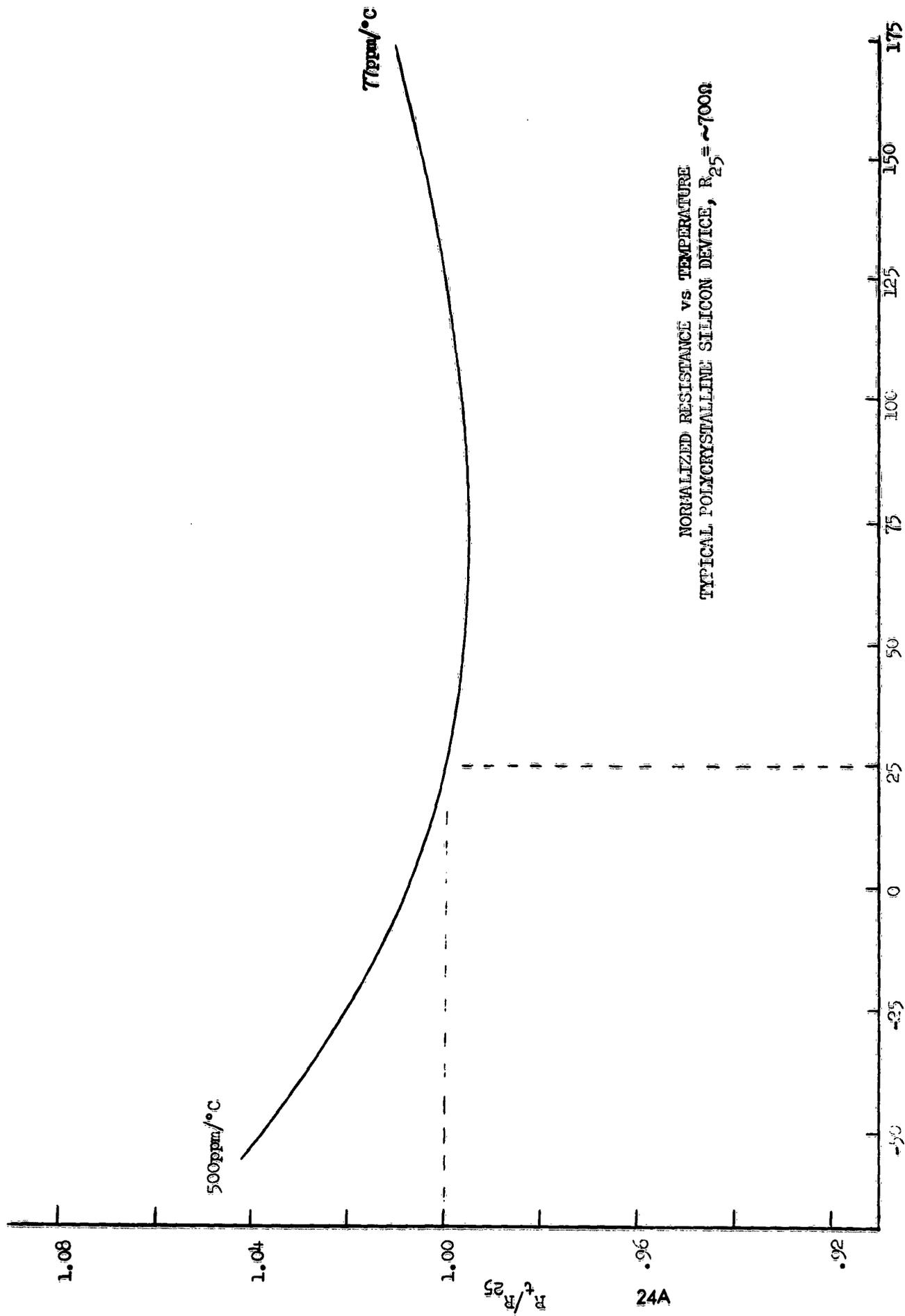


FIGURE 12

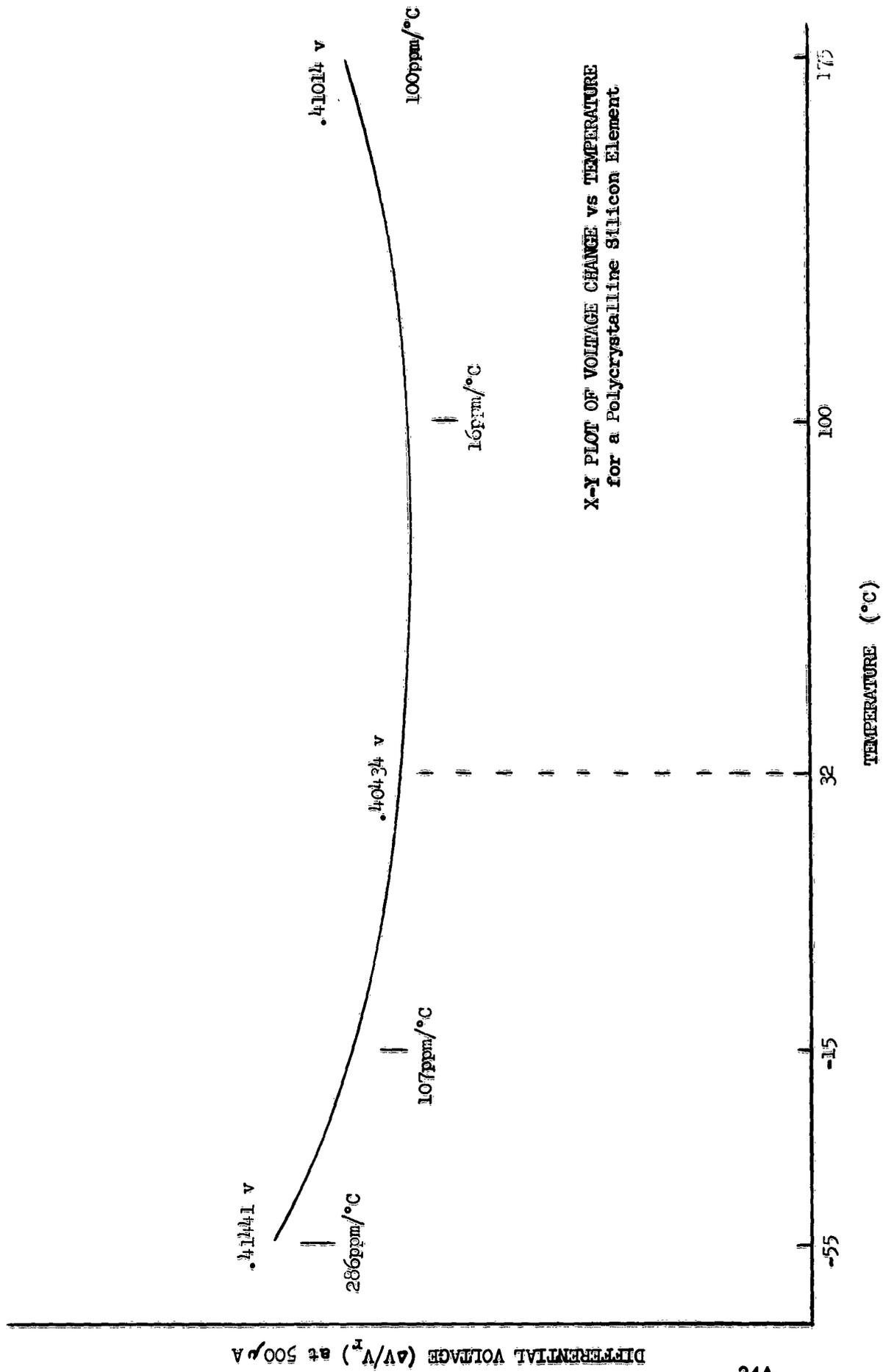


FIGURE 13

3. POLYCRYSTALLINE ELEMENTS (CONT'D)

OF DIFFERENTIAL VOLTAGE VS TEMPERATURE FOR ONE OF THE POLYCRYSTALLINE ELEMENTS.

A STUDY WAS MADE OF TCR AS A FUNCTION OF SHEET RESISTANCE. SHEET RESISTANCE IS DEPENDENT UPON BOTH DOPING LEVEL (BULK RESISTIVITY) AND THICKNESS.

THE TABLE BELOW LISTS THE SHEET RESISTANCE VALUES MEASURED ON A SERIES OF DEPOSITION RUNS AND SHOWS THE TCR OBTAINED FROM THE ELEMENTS. DEPOSITION CONDITIONS OF TEMPERATURE, CONCENTRATION, AND TIME WERE HELD CONSTANT IN THESE RUNS.

SHEET RESISTANCE <u>Ω/sq</u>	TCR	
	<u>AT 65°C</u>	<u>AT 175°C</u>
16.9	- 42	+171
14.9	+ 58	+229
13.3	+ 65	+195
14.4	- 21	+161
17.5	- 53	+135
14.4	- 47	+138
17.6	+ 63	+206
13.2	+105	+237
18.6	-100	+ 82
15.8	+ 42	+230

THERE APPEARS TO BE NO CORRELATION IN SHEET RESISTANCE WITHIN THE LIMITED Ω/sq VALUES OBTAINED AND THE TCR ABOVE ROOM

3. POLYCRYSTALLINE ELEMENTS (CONT'D)

TEMPERATURE.

OF INTEREST WAS THE TCR OF A SINGLE CRYSTAL ELEMENT AND A POLYCRYSTALLINE ELEMENT DEPOSITED AT THE SAME TIME IN THE REACTOR. THE SINGLE CRYSTAL SLICE (ETCH-POLISHED SURFACE) WAS PLACED ADJACENT TO AN ALUMINA CERAMIC SUBSTRATE IN THE REACTOR AND SILICON WAS DEPOSITED. THE SHEET RESISTANCE OF THE SINGLE CRYSTAL ELEMENT WAS APPROXIMATELY ONE HALF THE VALUE OF THE POLYCRYSTALLINE ELEMENT. MEASURED RESISTANCE CHANGES WITH INCREASING TEMPERATURE SHOWED THAT THE SINGLE CRYSTAL ELEMENT HAD A HIGH POSITIVE TCR (APPROX 1200 PPM/°C AT 175°C) WHILE THE POLYCRYSTALLINE ELEMENT SHOWED A TYPICAL TCR VALUE FOR THIS DOPING LEVEL, I.E. APPROX 150 PPM/°C.

GRAIN BOUNDARIES IN POLYCRYSTALLINE MATERIAL WERE BELIEVED TO HAVE A SIGNIFICANT EFFECT ON THE ELECTRICAL BEHAVIOR OF THE RESISTIVE ELEMENTS. AT THE BOUNDARY OF EACH CRYSTALLITE, THERE WOULD BE A CONCENTRATION OF PHYSICAL DEFECTS (DISLOCATIONS) AS WELL AS A GREATER CONCENTRATION OF IMPURITY ATOMS. THE INTERFACE BETWEEN THIS MORE HIGHLY DOPED BOUNDARY AREA AND THE CRYSTALLITE ITSELF WOULD CONSTITUTE A POTENTIAL BARRIER. THIS COULD EXPLAIN THE RELATIVELY GREATER SHEET RESISTANCE OF POLYCRYSTALLINE OVER SINGLE CRYSTAL LAYERS OF COMPARABLE DOPING LEVEL. THE TEMPERATURE DEPENDENCE OF THE CONDUCTIVITY WOULD BE A FUNCTION OF THE CRYSTALLITE, ITS GRAIN BOUNDARY,

3. POLYCRYSTALLINE ELEMENTS (CONT'D)

AND THE INTERFACE BETWEEN. THE POTENTIAL BARRIER ACROSS THE INTERFACES WOULD HAVE A TEMPERATURE-DEPENDENT CONDUCTIVITY SIMILAR TO A LOW BREAKDOWN DIODE. A MULTITUDE OF THESE CRYSTALLITES AND INTERFACES RANDOMLY ORIENTED WOULD BEHAVE ELECTRICALLY LIKE BACK-TO-BACK DIODES WITH LOW BREAKDOWN POTENTIALS IN EITHER DIRECTION OF POLARITY. IT HAS BEEN THEORIZED THAT THE EFFECTS OF THE GRAIN BOUNDARIES IN THE POLYCRYSTALLINE LAYERS HAVE BEEN TO "SMOOTH OUT" THE RESISTANCE-TEMPERATURE CURVE BY COMPENSATING TCR OF THE CRYSTALLITE WITH TCR OF THE BOUNDARY.

TWO ELECTRON MICROSCOPE PHOTOGRAPHS OF THE POLYCRYSTALLINE LAYER STRUCTURES (ETCHED AND AS-DEPOSITED) WHICH SHOW GRAIN STRUCTURE HAVE BEEN INCLUDED IN THE SUPPLEMENTARY DATA SECTION. ALSO SHOWN IS A LAPPED CROSS-SECTION THROUGH THE SILICON LAYER AND ALUMINA SUBSTRATE. THE PENETRATION OF THE ALUMINA CERAMIC BY THE PYROLYTICALLY DEPOSITED SILICON, AS OBSERVED IN THE MICRO PHOTOGRAPH, PROVIDES AN EXCELLENT BOND BETWEEN THE RESISTIVE LAYER AND ITS SUBSTRATE.

III. DETAILED FACTUAL DATA (CONTINUED)

C. RELIABILITY INFORMATION:

THE FOLLOWING TABLE LISTS SOME OF THE MIL-R-10509D REQUIREMENTS AND THE ACTUAL RESULTS OBSERVED IN TESTING THE MOLDED POLY-CRYSTALLINE SILICON DEVICES.

<u>TEST PERFORMED</u>	<u>MIL-R-10509D REQUIREMENT CHAR. C</u>	<u>RESULTS</u>
RESISTANCE-TEMPERATURE CHARACTERISTIC	± 50 PPM (-55°C TO 175°C)	TYPICAL ±500 PPM AT -55°C ±150 PPM AT 175°C
TEMPERATURE CYCLING	0.25%	.30 MAX .12 AVG
LOW-TEMPERATURE OPERATION	0.25%	.07 MAX .02 AVG
SHORT-TIME OVERLOAD	0.25%	.07 MAX .04 AVG
OVERLOAD (5x) FOR 18 HOURS	-	1.0 MAX
MOISTURE RESISTANCE (10 DAY)	0.5%	.21 MAX .10 AVG
LOAD LIFE (1000 HOUR)	0.5%	.41 MAX .17 AVG (40 DEVICES TESTED AT 1/2W)

DATA IN THIS SECTION INCLUDES:

1. LOAD LIFE DATA FOR 40 MOLDED DEVICES TESTED AT 125°C AND 1/2 WATT POWER FOR 1000 HOURS.



TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR COMPONENTS DIVISION
POST OFFICE BOX 5017 • DALLAS 22 TEXAS

RESISTOR QUALITY ASSURANCE
DATA SHEET
GROUP IV TESTS, MIL-R-10509D

TI-1967
RESISTOR TYPE
MPG. DESIGNATION
1/2 W
PERSON PERFORMING TEST
Raymond L. Lawrence
PART GRAPH

WITNESSED BY
DATE STARTED
10-29-62
DATE COMPLETED
12-10-62
JOB NUMBER
5-1607
PAGE OF
DAILY LOG

4.6.13

TEST	LOAD LIFE AT 125 °C										LOAD VOLTAGE	SEAL	
	INITIAL RESIS. AT 8 HOURS	RESIS. AT 100 HOURS	% RESIS. CHANGE	RESIS. AT 250 HOURS	% RESIS. CHANGE	RESIS. AT 500 HOURS	% RESIS. CHANGE	RESIS. AT 750 HOURS	% RESIS. CHANGE	RESIS. AT 1000 HOURS			% RESIS. CHANGE
MEASUREMENT	V=3.0	V=3.0	V=3.0	V=3.0	V=3.0	V=3.0	V=3.0	V=3.0	V=3.0	V=3.0	V=3.0		
SPEC. REQ'T			± .5		± .5		± .5		± .5		± .5		± .5
STANDARD RES. READING													
TEST SAMPLE	331.33	331.43	+ .03	331.46	+ .04	332.34	+ .03	332.36	+ .03	334.60	+ .09	331.80	+ .14
	384.27	384.28	+ .01	384.42	+ .04	384.37	+ .03	384.60	+ .09	384.50	+ .06	384.50	+ .06
	446.98	447.33	+ .08	447.58	+ .13	447.57	+ .12	447.81	+ .19	447.74	+ .17	447.74	+ .17
	424.29	424.59	+ .07	424.89	+ .14	425.02	+ .17	425.36	+ .25	425.22	+ .22	425.22	+ .22
	472.62	472.78	+ .03	472.93	+ .07	473.39	+ .16	472.95	+ .07	472.66	+ .01	472.66	+ .01
	460.25	460.16	- .02	460.32	+ .02	460.38	+ .03	460.60	+ .08	460.42	+ .04	460.42	+ .04
	461.05	461.15	+ .02	461.28	+ .05	461.30	+ .05	461.46	+ .09	461.57	+ .07	461.57	+ .07
	428.87	429.16	+ .07	429.47	+ .14	429.68	+ .19	430.04	+ .27	429.82	+ .22	429.82	+ .22
	396.91	397.23	+ .08	397.51	+ .15	397.66	+ .19	398.17	+ .32	397.76	+ .21	397.76	+ .21
AVERAGE	487.84	488.08	+ .05	488.33	+ .10	488.58	+ .15	489.02	+ .24	488.89	+ .22	488.89	+ .22

MEASURING EQUIPMENT:
REMARKS:
NOTE: Resistances exceeding 100 Ohms are recorded as percent from nominal resistance.



TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS 22 TEXAS

RESISTOR QUALITY ASSURANCE
DATA SHEET
GROUP IV TESTS, MIL-R-10509E

Sheet 2 of 2
WITNESSED BY: _____
DATE STARTED: 10-29-62
DATE COMPLETED: 12-10-62
JOB NUMBER: 5-1607
PAGE OF: _____
DAILY LOG: _____

TI-1967
RESISTOR TYPE: _____
MFG. DESIGNATION: 1/2 W
PERSON PERFORMING TEST: *Joseph L. Summers*

TEST	LOAD LIFE AT 125 °C										SEAL	
	INITIAL RESIS. AT 8 HOURS	RESIS. AT 100 HOURS	% RESIS. CHANGE	RESIS. AT 250 HOURS	% RESIS. CHANGE	RESIS. AT 500 HOURS	% RESIS. CHANGE	RESIS. AT 750 HOURS	% RESIS. CHANGE	RESIS. AT 1000 HOURS		% RESIS. CHANGE
MEASUREMENT			±.5									
SPEC. REQ'T			±.5									
STANDARD RES. READING												
TEST VOLTAGE	V=3.0	V=3.0		V=3.0		V=3.0		V=3.0		V=3.0		
SAMPLE												
284-8	566.42	566.70	+ .05	566.86	+ .08	567.63	+ .21	567.31	+ .16	567.01	+ .10	
284-9	533.39	533.54	+ .03	533.77	+ .07	533.63	+ .04	533.87	+ .09	533.94	+ .10	
285-3	512.48	512.73	+ .05	512.94	+ .09	512.94	+ .09	513.18	+ .14	513.29	+ .16	
286-22	557.37	557.70	+ .06	557.89	+ .09	558.00	+ .11	558.41	+ .19	558.29	+ .17	
296-2	574.56	575.12	+ .10	575.34	+ .14	575.96	+ .24	575.98	+ .25	575.85	+ .22	
298-10	533.89	534.18	+ .05	534.25	+ .07	534.15	+ .05	534.34	+ .08	534.34	+ .08	
11-299	567.96	568.25	+ .05	568.56	+ .11	568.77	+ .14	569.23	+ .22	569.23	+ .22	
301-2	490.71	490.71	- .01	490.67	- .01	490.55	- .04	490.72	- .01	490.49	- .05	
301-9	560.50	560.42	- .01	560.67	+ .03	560.86	+ .06	561.30	+ .17	560.77	+ .06	
303-5	549.09	549.30	+ .04	549.65	+ .10	550.10	+ .18	550.71	+ .29	550.68	+ .29	
AVERAGE	544.64											

MEASURING EQUIPMENT: _____
REMARKS: _____

NOTE: Resistances exceeding 100 Ohms are recorded as percent from nominal resistor. e.



TEXAS INSTRUMENTS
 INCORPORATED
 SEMICONDUCTOR COMPONENTS DIVISION
 POST OFFICE BOX 5017 • DALLAS, TEXAS

TI-1967 RESISTOR TYPE _____ MFG. DESIGNATION 1/2 W Sheet 2 of 2

PERSON PERFORMING TEST Raymond L. Lawrence JOB NUMBER 5-1607

DATE STARTED 10-29-62 DATE COMPLETED 12-10-62 PAGE OF 5

DATE STARTED 10-29-62 DATE COMPLETED 12-10-62 DAILY LOG

RESISTOR QUALITY ASSURANCE
 DATA SHEET
 GROUP IV TESTS, MIL-R-10509C

4.6.13

TEST	LOAD LIFE AT <u>125</u> °C										LOAD VOLTAGE	SEAL	
	INITIAL RESIS. AT 8 HOURS	RESIS. AT 100 HOURS	% RESIS. CHANGE	RESIS. AT 250 HOURS	% RESIS. CHANGE	RESIS. AT 500 HOURS	% RESIS. CHANGE	RESIS. AT 750 HOURS	% RESIS. CHANGE	RESIS. AT 1000 HOURS			% RESIS. CHANGE
MEASUREMENT													
SPEC. REQ'T	V=3.0	V=3.0	±.5	V=3.0	±.5	V=3.0	±.5	V=3.0	±.5	V=3.0	±.5	V=	
STANDARD RES. READING													
SAMPLE													
288-5	622.72	623.16	+ .07	623.44	+ .11	624.27	+ .25	624.24	+ .24	623.91	+ .19		
295	630.42	630.93	+ .08	631.18	+ .12	631.10	+ .11	631.67	+ .20	631.58	+ .18		
298-7	617.54	617.99	+ .07	618.22	+ .11	618.10	+ .09	618.59	+ .17	618.20	+ .11		
301-8	592.15	592.25	+ .02	592.60	+ .08	592.82	+ .11	593.54	+ .23	593.36	+ .20		
307-5	587.60	587.75	+ .03	587.91	+ .05	588.32	+ .12	588.22	+ .11	588.02	+ .09		
314	661.04	661.31	+ .04	661.87	+ .13	662.32	+ .19	663.37	+ .35	662.47	+ .37		
AVERAGE	618.58												

MEASURING EQUIPMENT:

REMARKS:

NOTE: Resistances exceeding 100 Ohms are recorded as percent from nominal resistance.



TEXAS INSTRUMENTS
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TI-1987

RESISTOR TYPE _____ MFG. DESIGNATION 1/2 W
 PERSON PERFORMING TEST [Signature]
 PARAGRAPH _____

RESISTOR QUALITY ASSURANCE
DATA SHEET
GROUP IV TESTS, MIL-R-10509E

WITNESSED BY _____ JOB NUMBER 5-1607
 DATE STARTED 10-29-62 DATE COMPLETED 12-10-62 PAGE OF 4.63
 DAILY LOG

TEST	LOAD LIFE AT <u>125</u> °C		LOAD VOLTAGE		4.63		SEAL				
	INITIAL RESIS. AT 8 HOURS	% RESIS. CHANGE	RESIS. AT 100 HOURS	% RESIS. CHANGE	RESIS. AT 500 HOURS	% RESIS. CHANGE					
MEASUREMENT	RESIS. AT 100 HOURS	% RESIS. CHANGE	RESIS. AT 250 HOURS	% RESIS. CHANGE	RESIS. AT 750 HOURS	% RESIS. CHANGE	RESIS. AT 1000 HOURS	% RESIS. CHANGE	RESIS. AT HOURS	% RESIS. CHANGE	EVIDENCE OF LEAKAGE
SPEC. REQ'T		±.5		±.5		±.5		±.5		±.5	
STANDARD RES. READING											
TEST VOLTAGE	V= 3.0		V= 3.0		V= 3.0		V= 3.0		V=		
SAMPLE											
298-3	741.33	+ .07	742.17	+ .11	742.72	+ .19	743.46	+ .29	743.12	+ .24	
298-4	748.54	+ .11	749.85	+ .18	750.06	+ .20	750.89	+ .31	750.53	+ .27	
317-3	772.02	+ .08	773.82	+ .10	773.76	+ .10	773.92	+ .12	773.93	+ .12	
284-4	782.04	+ .10	782.97	+ .12	782.87	+ .11	783.38	+ .17	783.91	+ .14	
298-11	852.02	+ .08	853.08	+ .12	853.59	+ .18	854.06	+ .24	853.60	+ .19	
309-4	838.81	+ .04	840.13	+ .16	841.11	+ .27	842.89	+ .49	842.48	+ .44	
AVERAGE	789.29										
MEASURING EQUIPMENT:											

REMARKS:

NOTE: Resistances exceeding 100 Ohms are recorded as percent from nominal resistance.

POWER CONDITION DATA
(2.5 WATT LOAD FOR 18 HOURS)

BUS	BEFORE Ω	AFTER Ω	% SHIFT	BUS	BEFORE Ω	AFTER Ω	% SHIFT
115X10	681.16	781.53	+0.5	114X4	526.30	527.93	-0.7
115X11	698.27	698.71	+0.6	114X5	509.28	508.46	-1.6
116X9	685.40	685.66	-0.3	114X9	537.46	537.39	-0.1
114X12	702.69	706.97	-1.0	115X6	551.06	551.50	+0.9
115X3	687.85	688.06	+0.3	114X6	431.18	ERR	
17	665.16	666.15	+0.4	93X11	72.406	72.722	+1.43
118X10	638.07	638.15	+0.1	108X6	441.50	443.93	+1.46
114X1	638.47	638.22	-0.3	70X11	80.807	80.853	+0.6
118X11	592.34	591.10	-1.2	19	991.87	995.06	+1.32
118X7	617.01	617.31	+0.4	20	991.64	992.24	+0.8
115X7	622.20	623.07	+1.4	21	967.53	967.99	+0.7
118X6	569.40	568.71	-1.2		121.12	120.650	-0.39
116X5	639.65	639.24	-0.6	85X12	74.560	74.785	+2.8
114X11	649.00	649.23	+0.4	85X1	76.989	77.258	+3.5
115X4	641.67	641.52	-0.2	64X2	83.670	83.816	+1.7
115X5	623.55	623.56	-0.7	92X5	32.074	32.072	-0.1
8	799.74	799.82	+0.1	18	1285.1	1285.0	-0.1
10	752.50	751.01	-2.0	69X10	55.409	55.440	+0.7
11	750.00	747.78	-3.0	108X11	84.439	840.84	-4.3
12	786.60	784.19	-3.1	5	905.18	903.86	-1.5
13	802.07	802.72	+0.8	6	855.66	853.67	-2.4
14	757.37	750.14	-1.6	7	883.96	882.09	-2.1
79X4	668.33	670.58	+3.4	118X1	772.51	771.53	-1.3
80X3	635.10	ERR		115X1	816.63	814.97	-2.0
59X6	628.80	627.86	-1.5	118X12	711.26	711.42	+0.2

Power Condition Data
(2.5 watt load for 18 hours)

Bus	BEFORE Ω	AFTER Ω	% SHIFT	Bus	BEFORE Ω	AFTER Ω	% SHIFT
81X3	667.43	666.63	-0.12	55X7	38.098	38.160	+0.16
74X3	673.16	673.03	-0.02	57X3	700.04	701.64	+0.23
81X6	640.93	643.03	+0.33		695.71	696.16	+0.06
74X3	677.77	678.99	+0.19		39.708	39.670	-0.10
81X3	619.15	617.53	-0.20	57X6	685.86	686.83	+0.14
91X1	661.43	661.90	+0.07	57X7	708.04	707.80	-0.03
72X-9	618.47	618.20	-0.04	57X10	750.44	750.31	-0.02
72X-4	628.50	628.05	-0.07		37.328	37.410	+0.22
80X10	735.27	734.90	-0.04	59X1	716.90	719.18	+0.32
83X5	740.41	738.31	-0.32	59X9	728.40	728.85	+0.05
82X6	698.57	697.60	-0.13	59X10	735.90	736.80	+0.12
81X1	728.27	729.87	+0.22	57X1	755.30	755.27	-0.04
82X3	735.03	737.31	+0.31	57X11	775.05	775.40	+0.05
82X4	752.28	755.49	+0.11	59X11	758.77	759.15	+0.05
81X11	779.20	777.31	-0.24	60X6	839.57	831.45	+0.10
82X7	729.17	728.10	-0.15	56X10	909.87	910.04	+0.02
82X5	789.00	790.01	+0.13	59X12	860.80	860.39	-0.05
74X6	714.20	717.34	+0.44	60X7	849.49	850.04	+0.01
72X11	724.15	722.27	-0.26	61X11	908.84	909.54	+0.08
81X10	702.88	701.90	-0.14		760.48	758.98	-0.20
79X5	724.20	722.45	-0.25	16	791.84	789.40	-0.30
83X7	719.28	717.36	-0.27				
83X6	753.50	754.11	+0.08				
83X3	750.60	750.87	+0.03				
	39.35	39.40	+0.18				



TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR DIVISION
POST OFFICE BOX 5012 - DALLAS 22, TEXAS

TI SQ120 4/61
RESISTOR TYPE

MANUFACTURER'S DESIGNATION
PCCYCR45TALCINE
SILICON

PERSON PERFORMING TEST

Bill Malek

RESISTOR QUALITY ASSURANCE
DATA SHEET

GROUP II TESTS, MIL-R-10509D

WITNESSED BY

JOB NUMBER
S-1541

DATE STARTED
8-1-62

DATE COMPLETED
8-7-62

PAGE
5-1541

OF
100

DEPT
LOG

Sheet 1 of 1

PARAGRAPH TEST	4.6.4 TEMPERATURE CYCLING			4.6.5 LOW TEMPERATURE OPERATION			4.6.6 SHORT-TIME OVERLOAD			4.6.7 TERMINAL STRENGTH			SEAL EVIDENCE OF LEAKAGE
	INITIAL RESISTANCE READING	FINAL RESISTANCE READING	% RESISTANCE CHANGE										
SPEC REQUIREMENT													
STANDARD RES. READING													
TEST VOLTAGE	V=	V=											
SAMPLE	623.6	623.8	+ .03	623.8	624.26	+ .07	624.06	623.81	- .04				
	311.68	311.74	+ .06	311.74	311.74	± 0	311.86	311.74	- .04				
	457.66	458.03	+ .08	457.93	457.93	- .02	458.10	457.78	- .07				
	303.16	304.57	+ .30	304.53	304.53	- .01	304.16	303.99	- .06				
	416.55	417.74	+ .29	417.73	417.73	- .01	417.91	417.92	- .07				
	423.54	424.87	+ .26	424.64	424.64	- .03	424.78	424.61	- .03				
	287.83	287.84	± .01	287.84	287.79	- .02	287.83	287.69	- .06				
	423.63	423.29	- .04	423.29	423.20	- .02	423.30	423.20	- .02				
	463.69	463.81	+ .03	463.81	463.78	- .01	463.79	463.87	+ .02				
	463.54	463.71	+ .08	463.71	463.68	- .01	463.74	463.75	+ .01				
AVERAGE													

MEASURING EQUIPMENT:

REMARKS:

SAMPLE CALCULATION

% Resistance Change = $\frac{100(\text{Final Resistance} - \text{Initial Resistance})}{\text{Initial Resistance}}$

Initial Resistance = 39.590, Final Resistance = 39.526

% Resistance Change = $\frac{100(39.526 - 39.590)}{39.590} = -.161$

NOTE: Resistances exceeding 100 Ohms are recorded as percent from nominal resistance.

8H

NA

C. RELIABILITY INFORMATION (CONT'D)

2. RESULTS OF POWER CONDITIONING DEVICES AT 2.5 WATTS FOR
18 HOURS.

3. TEMPERATURE CYCLING, LOW-TEMPERATURE OPERATION, SHORT-
TIME OVERLOAD DATA ON TEN DEVICES.

4. MOISTURE RESISTANCE DATA ON TEN MOLDED DEVICES.

SEVERAL ELEMENTS TO WHICH SPECIAL LEADS WERE ATTACHED WERE OPERATED
AT 20 WATTS FOR FIVE MINUTES DURATION WITH AN OBSERVED RESISTANCE
SHIFT OF LESS THAN 0.5%. THE SILICON WAS UNPROTECTED FROM THE
ATMOSPHERE. THIS TEST INDICATED THE INHERENT STABILITY OF THE
SILICON ELEMENT WITH REGARD TO ELEVATED TEMPERATURE AND OXIDIZING
AMBIENTS.

D. MANUFACTURING PROCEDURE:

A PROCESS AND MATERIAL FLOW CHART AND A PHOTOGRAPH OF A DISPLAY
SHOWING STEPS IN FABRICATING THE POLYCRYSTALLINE SILICON DEVICE
MAY BE SEEN ON THE FOLLOWING PAGES.

DETAILED MANUFACTURING SPECIFICATIONS FOR AN EPOXY MOLDED DEVICE
HAVE BEEN OUTLINED IN THIS SECTION OF THE REPORT.



ALUMINA SUBSTRATE



VAPOR DEPOSITED SILICON



K.M.E.R. APPLIED & DEVELOPED

VALUE ADJUSTED (PHOTO ETCHED)



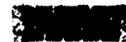
LOW VALUE



HIGH VALUE



OHMIC ALUMINUM CONTACT



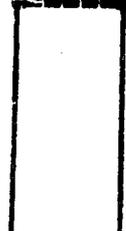
COPPER OVERCOAT



LEAD ATTACH (SOLDER)



EPOXY UNDERCOAT



EPOXY ENCAPSULATED
SILICON RESISTOR

D. MANUFACTURING PROCEDURE (CONT'D)

PREPARATION OF SUBSTRATE

EQUIPMENT

1. PYREX BEAKERS
2. GLASS STIRRING RODS
3. ULTRASONIC CLEANER
4. HOT PLATE
5. PLASTIC BEAKERS

MATERIALS

1. TRICHLOROETHYLENE
2. ACETONE
3. DEIONIZED WATER
4. NITRIC ACID
5. METHYL ALCOHOL
6. ALUMINA SUBSTRATES

PROCEDURE

1. PLACE SUBSTRATES IN BEAKER OF METHYL ALCOHOL AND PUT IN ULTRASONIC CLEANER FOR A MINIMUM OF THIRTY (30) MINUTES. REPLACE METHYL ALCOHOL EVERY TEN (10) MINUTES UNTIL IT REMAINS CLEAN.
2. RINSE IN ACETONE.
3. WASH IN DEIONIZED WATER.
4. HEAT IN 50% SOLUTION OF NITRIC ACID UNTIL BOILING IS REACHED. REMOVE AND LET SET FOR FIVE (5) MINUTES. PUR OFF ACID.
5. RINSE IN DEIONIZED WATER.
6. STORE IN ACETONE UNTIL REQUIRED FOR DEPOSITION.

D. MANUFACTURING PROCEDURE (CONT'D)

VAPOR DEPOSITION PROCEDURE

PRELIMINARY ADJUSTMENTS

(SEE FIGURE 14, VAPOR DEPOSITION SYSTEM)

1. CHECK VALVE "E". VALVE MUST BE IN POSITION NUMBER 1.
2. TURN FOUR-WAY VALVE "D" TO POSITION NUMBER 3.
3. TURN ON SWITCH "M" TO ACTIVATE EXHAUST FAN.
4. OPEN VALVE "L" AND IGNITE PILOT LIGHT.
5. ADJUST POWERSTAT "O" TO APPROXIMATELY 45%.

NOTE: TEMPERATURE ON FLASH EVAPORATOR HEATING TAPE SHOULD BE APPROXIMATELY 50°C.

6. TURN ON VALVE "G", COOLING AIR.
7. TURN ON SWITCH "F", COOLING WATER.

NOTE: CHECK DRAIN FOR PROPER FLOW.

8. TURN ON VALVES "I", "J", AND "K". ADJUST "K" TO APPROXIMATELY 15 PSIG; ADJUST "J" TO 8 PSIG; ADJUST "I" TO 20 PSIG.

REACTOR OPERATING PROCEDURE

1. ADJUST FLOWRATERS "B", "C" TO INDICATE 13 SLM FLOW, HE.
2. ALLOW HE TO FLOW FIVE (5) MINUTES.

NOTE: CHECK EXHAUST TO ASSURE UNIMPEDED FLOW OF GAS.

3. POSITION SUBSTRATES ON QUARTZ BOAT.
4. OPEN REACTOR AND PLACE BOAT ON ELECTRODE IN CENTER OF HEAT ZONE.
5. CLOSE REACTOR AND ALLOW HE TO FLOW ONE (1) MINUTE.
6. ADJUST POWERSTAT "N" TO CONTROL ELECTRODE TO APPROX 250°C.
ALLOW HE TO CONTINUE FLOWING FOR FOUR (4) MINUTES MINIMUM.

D. MANUFACTURING PROCEDURE (CONT'D)

7. TURN ON EMERGENCY SWITCH "H".
8. TURN VALVE "E" TO POSITION NUMBER 2.
NOTE: EXHAUST MUST IGNITE WITHIN APPROX TWO (2) SECONDS.
IF IT DOES NOT IGNITE, TURN VALVE "E" TO POSITION
NUMBER 1 AND CHECK EQUIPMENT FOR GAS SUPPLY OR OBSTRUCTED
EXHAUST LINE. WITH ASSURANCE OF PROPER EQUIPMENT SETUP,
REPEAT STEP 8.
9. ADJUST FLOWRATERS "B" AND "C" TO INDICATE 15 SLM FLOW, H₂.
10. ADJUST POWERSTAT "N" TO CONTROL ELECTRODE TO APPROX 600°C.
11. ADJUST FLOWRATER "A" TO INDICATE 1.5 ML/MIN. FLOW,
SiCl₄ (L).
12. ADJUST POWERSTAT "N" TO CONTROL ELECTRODE TO 1150°C ±10°C.
13. TURN FOUR-WAY VALVE "D" TO POSITION NUMBER 4 STARTING
DEPOSITION AND ALLOW TO CONTINUE FOR DEFINED TIME.
14. TURN VALVE "D" TO POSITION NUMBER 3 STOPPING DEPOSITION.
15. CLOSE FLOWRATER "A".
16. ALLOW ONE-HALF (1/2) MINUTE MINIMUM TO CLEAR SYSTEM.
17. ADJUST POWERSTAT "N" TO ZERO.
18. ALLOW ONE-HALF (1/2) MINUTE TO COOL.
19. TURN VALVE "E" TO POSITION NUMBER 1 AND ALLOW HE TO FLOW
FOR FIVE (5) MINUTES.

PREPARATION OF SILICON ELEMENT

EQUIPMENT

1. PYREX BEAKERS
2. GLASS STIRRING RODS
3. PLASTIC BEAKER

VAPOR DEPOSITION DIAGRAM

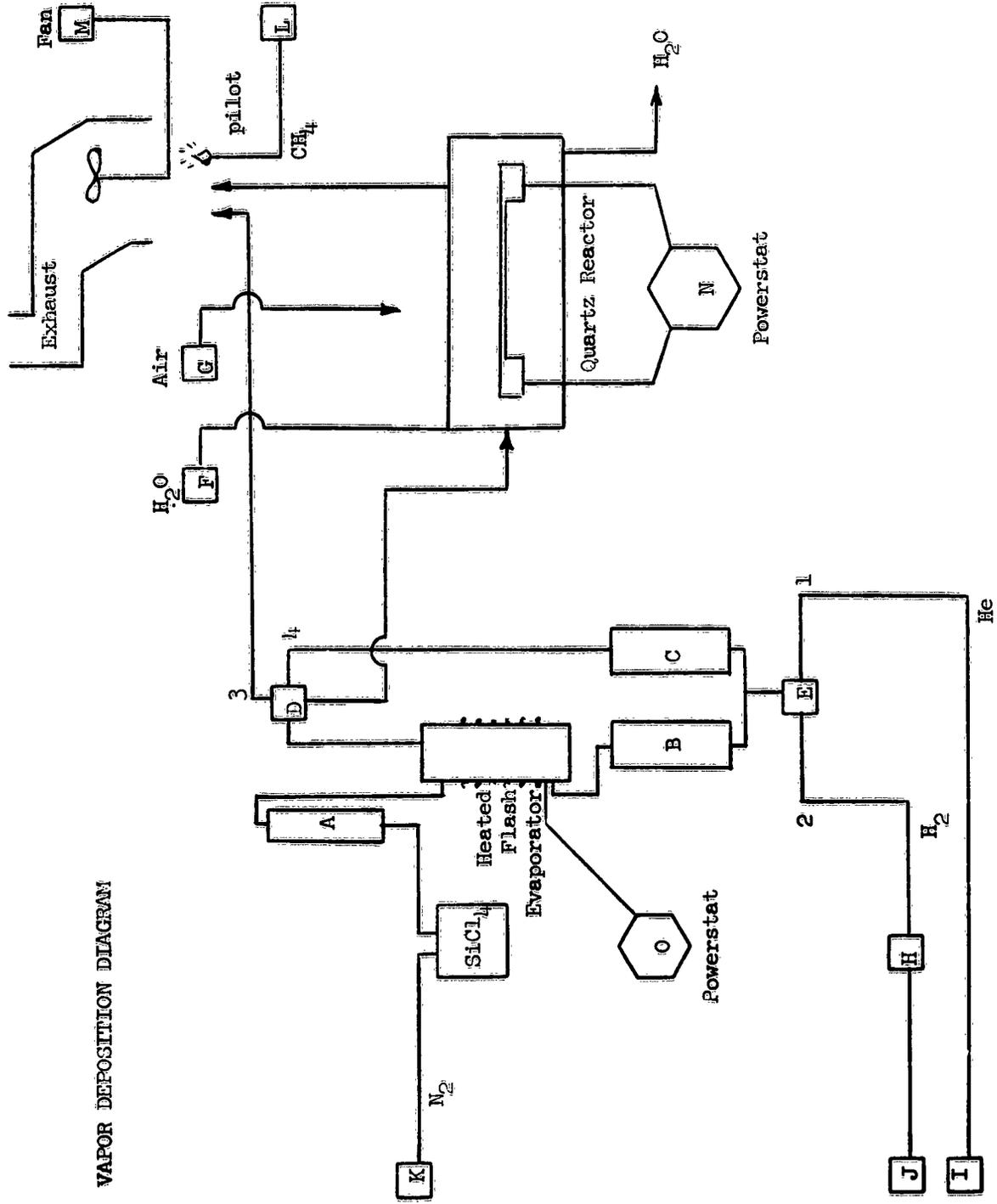


FIGURE 14

D. MANUFACTURING PROCEDURE (CONT'D)

MATERIALS

1. TRICHLOROETHYLENE
2. HYDROFLUORIC ACID
3. DEIONIZED WATER
4. ACETONE
5. VAPOR DEPOSITED SILICON ELEMENTS

PROCEDURE

1. RINSE IN ACETONE.
2. RINSE IN DEIONIZED WATER.
3. WASH IN 10% SOLUTION OF HYDROFLUORIC ACID FOR FIVE (5) MINUTES. POUR OFF ACID.
4. RINSE IN DEIONIZED WATER.
5. STORE IN ACETONE UNTIL REQUIRED FOR OHMIC CONTACT APPLICATION.

VALUE ADJUSTMENT (PHOTO ETCH)

EQUIPMENT

1. CENTRIFUGAL SPINNER
2. DRYING OVEN CAPABLE OF MAINTAINING 120°C
3. LIGHT EXPOSURE TOWER
4. PHOTO PATTERN
5. HOT PLATE
6. PLASTIC BEAKERS
7. GLASS BEAKERS

D. MANUFACTURING PROCEDURE (CONT'D)

MATERIALS

1. KODAK METAL ETCH RESIST (KMER)
2. PHOTO DEVELOPER
3. SILICON ETCHANT NUMBER 39E
4. TRICHLOROETHYLENE
5. HYDROFLUORIC ACID
6. DEIONIZED WATER
7. ACETONE
8. METHYL ALCOHOL
9. PREPARED SILICON ELEMENTS

PROCEDURE

CAUTION: ALL KMER WORK MUST BE KEPT AWAY FROM DIRECT LIGHT UNTIL ELEMENTS ARE EXPOSED AND DEVELOPED.

1. PLACE PREPARED SILICON ELEMENTS ON THE CENTRIFUGAL SPINNER (SILICON SIDE UP).
2. APPLY KMER IN DROPS ON THE ELEMENT (COVER ELEMENT COMPLETELY).
3. TURN SPINNER ON AND ALLOW THE EXCESS KMER TO BE THROWN OFF. A UNIFORM THIN LAYER IS DESIRED. DO NOT INCREASE SPINNER ACTION ENOUGH TO MOVE ELEMENTS.
4. CURE AT ROOM TEMPERATURE FOR A MINIMUM OF TEN (10) MINUTES.
5. BAKE AT 120°C FOR TEN (10) MINUTES. ALLOW TO COOL.
6. PHOTO MASK WITH DESIRED PATTERN AND EXPOSE FOR 2-1/2 MINUTES. MAKE SURE MASK IS HELD TIGHT AGAINST THE ELEMENT.

D. MANUFACTURING PROCEDURE (CONT'D)

7. SPRAY DEVELOPER ON ELEMENTS UNTIL PATTERN IS CLEAR.
DRY WITH AIR SPRAY TO ASSURE COMPLETE DEVELOPMENT.
8. BAKE AT 120°C FOR TWENTY (20) MINUTES. ALLOW TO COOL.
9. ETCH IN SILICON ETCHANT NUMBER 39E UNTIL PATTERN IS
CLEAN AND SHARP. DO NOT PROLONG ETCHING. PROLONGED
ETCHING WILL UNDERCUT KMER AND DESTROY PATTERN. POUR
OFF ACID.
10. RINSE IN DEIONIZED WATER.
11. CLEANING PROCESS:
 - 11.1 BOIL ELEMENTS IN TRICHLOROETHYLENE FIVE (5)
MINUTES TO REMOVE KMER. MAKE SURE ALL KMER
IS REMOVED.
 - 11.2 RINSE IN METHYL ALCOHOL.
 - 11.3 RINSE IN 10% SOLUTION HYDROFLUORIC ACID.
(USE PLASTIC BEAKER.) POUR OFF ACID.
 - 11.4 BOIL IN DEIONIZED WATER FIVE (5) MINUTES.
12. STORE IN ACETONE UNTIL READY FOR APPLICATION OF OHMIC
CONTACT.

APPLICATION OF OHMIC CONTACT

EQUIPMENT

1. MASKING JIG
2. PLASMA SPRAY GUN (PLASMADYNE CORPORATION, SANTA ANA,
CALIFORNIA) (SEE FIGURE 15)



Plasma Spray Gun and Masking Jig
FIGURE 15

D. MANUFACTURING PROCEDURE (CONT'D)

MATERIALS

1. ALUMINUM POWDER (-325 MESH)
2. COPPER POWDER (-325 MESH)
3. ARGON
4. ARGON-HYDROGEN 95/5
5. PREPARED SILICON ELEMENTS

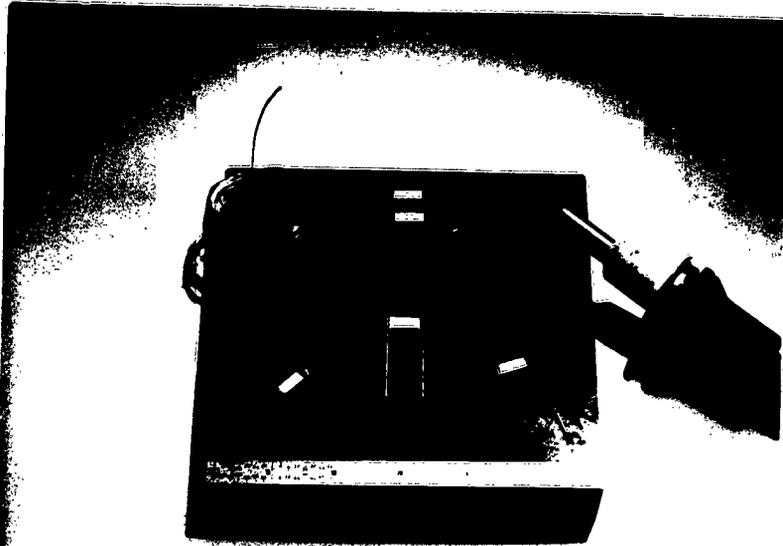
PROCEDURE

1. MOUNT SILICON ELEMENTS ON MASKING JIG.
2. PLACE A .500" METAL MASK ON THE ELEMENTS ALLOWING APPROXIMATELY .075" OF ENDS EXPOSED ON EACH SIDE.
3. SPRAY THE EXPOSED END WITH ALUMINUM POWDER USING THE MANUFACTURER'S INSTRUCTION FOR OPERATION OF THE PLASMA SPRAY GUN (SG-3). AMPERES SETTING OF 375.
4. SPRAY ALUMINUM CONTACT WITH AN OVERCOAT OF COPPER POWDER USING MANUFACTURING INSTRUCTIONS MENTIONED IN PARA. 3. AMPERES SETTING OF 250.
5. REMOVE ELEMENTS FROM JIG AND STORE IN PROPER CONTAINERS UNTIL REQUIRED FOR LEAD ATTACHMENT.

LEAD ATTACHMENT

EQUIPMENT

1. SOLDER IRON (40 WATT)
2. LEAD ATTACHMENT HOLDING JIG (SEE FIGURE 16)
3. CERAMIC PLATES



Lead Attachment Holding Jig
FIGURE 16

D. MANUFACTURING PROCEDURE (CONT'D)

MATERIALS

1. SOLDER SN/AG 95/5
2. SOLDER FLUX
3. DEIONIZED WATER
4. ACETONE
5. COPPER LEADS (OFHC)
6. OHMIC CONTACT APPLIED ELEMENTS

PROCEDURE

1. DIP END OF ELEMENT INTO SOLDER FLUX.
2. PLACE ON CERAMIC PLATE AND APPLY HOT SOLDERING IRON WITH EXCESS SOLDER ON TIP TO THE COPPER-COATED AREA. ALLOW THE SOLDER TO FLOW AND COVER THE OHMIC CONTACT AREA.
3. REPEAT STEPS (1) AND (2) FOR OPPOSITE END OF ELEMENT.
4. PLACE TINNED ELEMENT INTO HOLDING JIG.
5. DIP END OF LEAD WIRE IN SOLDER FLUX AND PLACE IN LEAD GROOVE ALLOWING THE FLUXED END TO EXTEND THE FULL LENGTH OF THE TINNED AREA.
6. APPLY HOT SOLDER IRON WITH EXCESS SOLDER ON TIP TO LEAD WIRE. ALLOW SOLDER TO FLOW AROUND WIRE AND COVER TINNED AREA. REMOVE SOLDERING IRON. DO NOT MOVE UNIT UNTIL SOLDER HAS SET.
7. REPEAT STEPS (5) AND (6) FOR OTHER END OF ELEMENT.
8. WASH ELEMENTS IN DEIONIZED WATER TO REMOVE FLUX.
9. RINSE IN ACETONE AND ALLOW TO DRY.
10. STORE IN PROPER CONTAINER TO PREVENT CONTAMINATION UNTIL REQUIRED FOR EPOXY UNDERCOATING.

D. MANUFACTURING PROCEDURE (CONT'D)

TIN DIPPING

EQUIPMENT

1. SOLDER POT CAPABLE OF MAINTAINING 200°C.

MATERIALS

1. SOLDER PB/SN 70/30
2. SUPERIOR FLUX NUMBER 30
3. TWEEZERS
4. METHYL ALCOHOL
5. EPOXY UNDERCOATED ELEMENTS

PROCEDURE

1. GRASP ELEMENT WITH TWEEZERS
2. DIP APPROXIMATELY 1/2 THE DISTANCE OF LEAD WIRE INTO SOLDER FLUX.
3. DIP FLUXED LEADS IN MOLTANT SOLDER UP TO THE PAINTED ELEMENT. DO NOT PROLONG TIME IN SOLDER POT. REMOVE FROM THE SOLDER AT A STEADY RATE.
4. WASH UNITS IN METHYL ALCOHOL TO REMOVE FLUX.
5. ALLOW TO DRY AND STORE IN PROPER CONTAINER UNTIL REQUIRED FOR EPOXY CASTING.

D. MANUFACTURING PROCEDURE (CONT'D)

EPOXY UNDERCOATING

EQUIPMENT

1. PAINT BRUSH

MATERIALS

1. EPOXY PAINT (MICA FILLED) (2 PARTS PAINT:1 PART -13 MESH MICA BY WEIGHT)
2. EPOXY PAINT THINNER (1:1 CELLOSOLVE ACETATE AND ISOPROPYL ALCOHOL = BE WEIGHT)
3. LEAD ATTACHED ELEMENTS

PROCEDURE

1. MIX PAINT THOROUGHLY UNTIL MICA IS WELL IN SUSPENSION.
2. APPLY A COAT OF PAINT TO THE SILICON ELEMENT SIDE OF THE SUBSTRATE. MAKE SURE THE CONTACT IS COMPLETELY COVERED.
3. AIR DRY A MINIMUM OF THIRTY (30) MINUTES AT 38°C.
4. BAKE FIFTEEN (15) HOURS AT 200°C.
5. ALLOW UNITS TO COOL TO ROOM TEMPERATURE.
6. STORE UNITS UNTIL REQUIRED FOR TIN DIPPING.

MOLDING

MANUFACTURER'S SPECIFICATIONS FOR CASTING A SEMIFLEXIBLE EPOXY MOLDING COMPOUND WERE FOLLOWED FOR FINAL ENCAPSULATION OF THE DEVICE. SILICONE RUBBER MOLDS WERE USED FOR BOTH IN-LINE AND RADIAL-LEAD CONFIGURATIONS.

IV. RECOMMENDATIONS

THE PYROLYTIC SILICON RESISTOR DEVELOPED UNDER THIS CONTRACT DID NOT COME UP TO EXPECTATIONS WITH RESPECT TO TCR (OVER THE TEMPERATURE RANGE OF -50°C TO $+175^{\circ}\text{C}$). IN FACT, THE TCR IN THE LOW TEMPERATURE REGION WAS GREATER THAN THAT NORMALLY EXHIBITED BY CARBON-FILM RESISTORS. THE TCR ABOVE ROOM TEMPERATURE, AT 65°C AND 175°C , AVERAGED APPROXIMATELY $150 \text{ PPM}/^{\circ}\text{C}$. TO SUBSTANTIALLY IMPROVE THESE TCR CHARACTERISTICS, I.E. FLATTEN THE R VS T CURVE, WOULD REQUIRE CONSIDERABLY MORE FUNDAMENTAL RESEARCH EFFORT THAN THAT EXPENDED IN THIS CONTRACT.

A POSSIBLE APPROACH TO BE CONSIDERED IN ANY FUTURE RESEARCH EFFORT WOULD BE TO DOP THE SILICON WITH MORE THAN ONE IMPURITY OF THE SAME TYPE, E.G., PHOSPHORUS AND ARSENIC, IN HOPE OF MINIMIZING THE SLOPE OF THE RESISTIVITY CURVE IN THE LOW TEMPERATURE REGION. THIS, IN EFFECT, MIGHT BE EQUIVALENT TO DOPING WITH AN IMPURITY OF VARYING ACTIVATION ENERGY. SUCH A PROGRAM WOULD BE VERY EXTENSIVE AND HAD TO BE CONSIDERED OUTSIDE THE REALM OF THIS CONTRACT. JUSTIFICATION OF SUCH AN EFFORT WOULD REST MAINLY UPON THE ADDITIONAL ADVANTAGES (OTHER THAN TCR) WHICH MIGHT ENSUE. ONE OF THE ADVANTAGES ALREADY DEMONSTRATED WITH THE PRESENT DEVICE IS ITS RESISTANCE TO OXIDATION AND HIGH TEMPERATURE CAPABILITIES. EVEN SO, CONTINUATION OF THE R&D EFFORT TO REDUCE THE TCR OF THE SILICON DEVICE IS NOT ADVISED. NEITHER IS A MANUFACTURING-METHODS TYPE CONTRACT RECOMMENDED FOR EXPLOITING THE PROCESS THUS FAR EVOLVED.

IV. RECOMMENDATIONS (CONTINUED)

IN SPITE OF THE INABILITY TO MEET THE CONTRACT OBJECTIVES WITH THE SILICON LAYER RESISTIVE ELEMENT, SOME THOUGHT WAS GIVEN TO PILOT-LINE OR COMMERCIAL-SCALE PRODUCTION. PYROLYTIC DEPOSITION OF SILICON BY HYDROGEN REDUCTION OF THE HALIDE IS A WIDELY USED PROCESS IN THE SEMICONDUCTOR INDUSTRY, AND CONTINUOUS DEPOSITION SYSTEMS HAVE BEEN PROPOSED.

THE SILICON RESISTOR AT THIS STAGE OF ITS DEVELOPMENT HAS CERTAIN PROPERTIES WHICH SUGGEST POTENTIAL USES. ONE OF THESE IS STABILITY AT ELEVATED TEMPERATURES. IT WAS RECOMMENDED THAT A PYROLYTIC (POLYCRYSTALLINE) SILICON DEVICE UNPROTECTED FROM THE ATMOSPHERE WOULD OPERATE AT POWER LEVELS SUFFICIENT TO RAISE ITS TEMPERATURE TO RED HEAT. ONLY A SMALL CHANGE IN RESISTANCE ($\sim 1.0\%$) RESULTED FROM THIS TREATMENT. THIS WOULD SUGGEST THE POSSIBILITIES OF THE SILICON RESISTIVE ELEMENT FOR HIGH-TEMPERATURE DEVICES.

FINALLY, THE HIGH-TEMPERATURE CAPABILITIES OF THE DEVICES WOULD REQUIRE A PACKAGE WHICH COULD WITHSTAND THE ABUSE OF EXCESSIVE HEAT AND OXIDATION. THE PACKAGING MATERIAL SHOULD ALSO PROVIDE GOOD HEAT DISSIPATION FOR THE ELEMENT. COMBINATIONS OF CERAMICS AND GLASS COULD BE DESIGNED TO PROVIDE A FINAL ENCAPSULATION FOR THIS DEVICE.

PACKAGES SIMILAR TO THOSE PRESENTLY USED FOR POWER RECTIFIERS MIGHT ALSO BE APPLICABLE.

SUPPLEMENTARY DATA

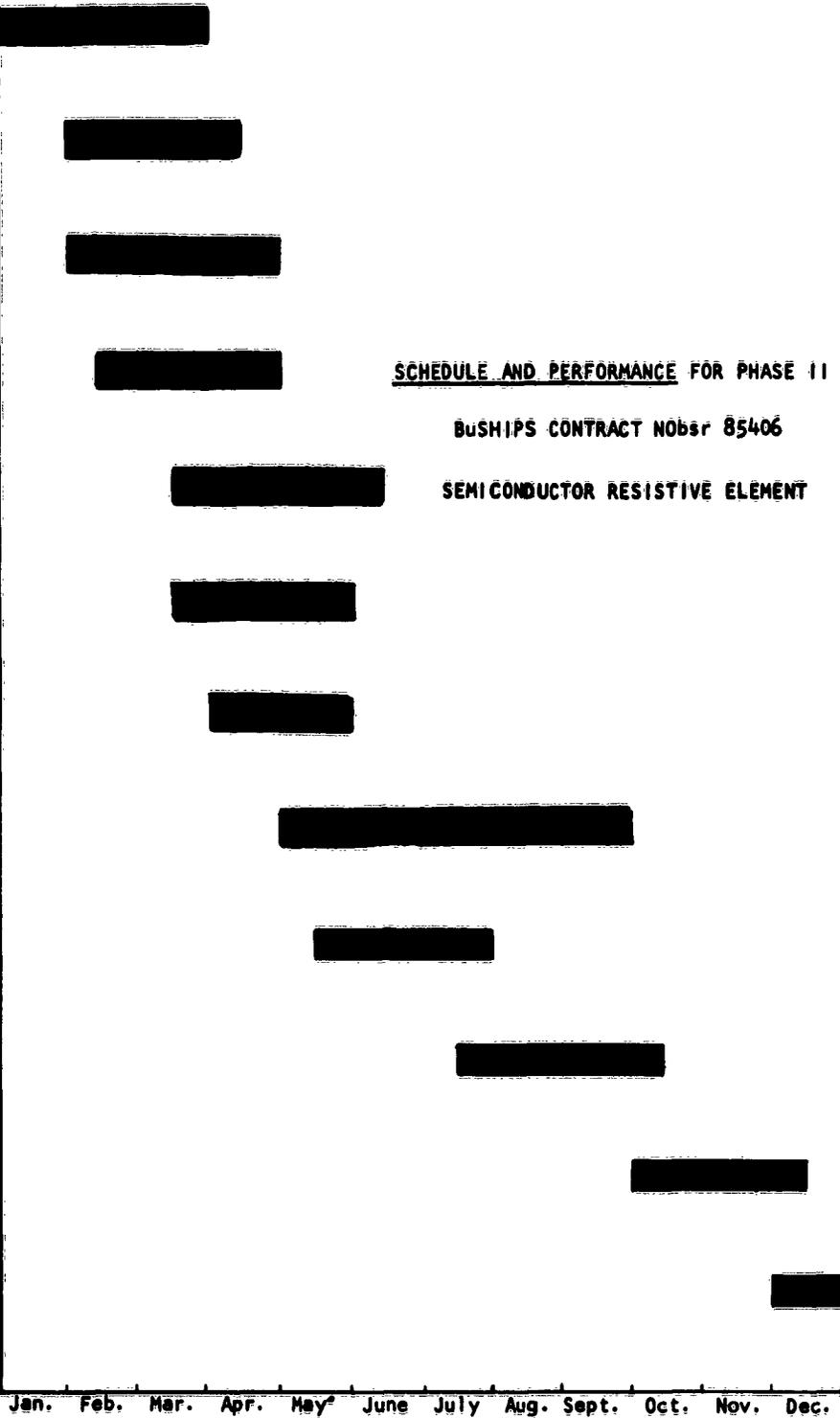
153870 DATA SHEET (16-25)

TAKEN BY: Hooker DATE: 9-20-67 PAGE OF: 1

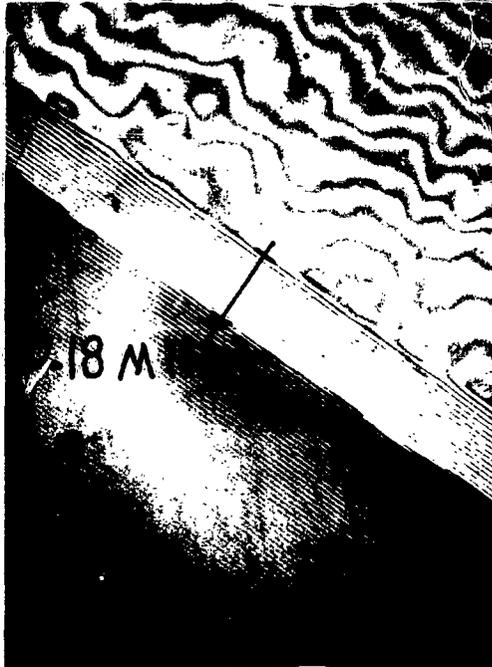
IX Power Rating Test (2.5 WATTS)
 COMPARISON OF SPRAYED AL-CU, NICKEL PLATED CONTACTS

Bus #	PLATED NICKEL		≈ SX Power 6HR		≈ SX Power 12HR		≈ SX Power 24HR	
	R.R.	AR %	R.R.	AR %	R.R.	AR %	R.R.	AR %
275-2	707.70	-.39	704.99	-.39	703.61	-.58	702.54	-.73
279	530.40	-.32	528.71	-.32	527.81	-.49	527.81	-.49
279-2	579.00	.21	580.20	.21	579.30	.05	57.880	-.03
305-2	651.10	.28	652.92	.28	651.65	.08	651.54	.13
306	835.80	-.13	834.69	-.13	832.60	-.38	832.21	-.43
309 A	529.40	-.03	527.60	-.03	526.73	-.51	526.09	-.63
275	745.40	-.51	741.60	-.51	739.90	-.73	739.04	-.86
	SPRAYED AL-CU							
296	513.60	-.01	513.54	-.01	512.79	-.16	512.95	-.13
294	614.10	-.05	613.82	-.05	610.95	-.35	610.44	-.60
264	688.60	-.92	675.40	-.92	666.90	-.35	669.50	-.285
262	818.80	-.04	818.51	-.04	818.83	.003	818.81	.001
297	646.24	.11	646.95	.11	646.11	-.02	646.57	.05
317	584.20	-.16	583.30	-.16	582.40	-.22	584.40	.03
288	801.30	.24	803.20	.24	802.63	.17	801.81	.06

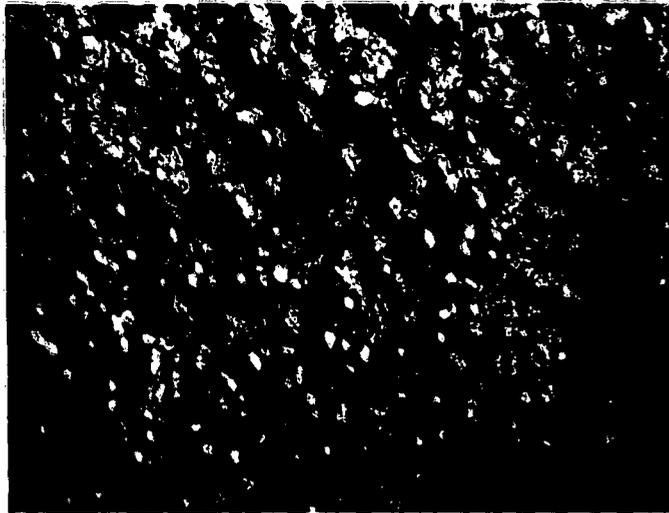
Optimize conditions of vapor-deposition process for controlable runs
Adjust resistance by electron beam scribing and photo-resist etching
Improve ohmic contacts for greater mechanical strength and power dissipation
Determine effect of substrate resistivity on TCR of epitaxial layer elements
Increase sheet resistivity of diffused and vapor-deposited elements
Investigate effect of thermal history and layer thickness on TCR of vapor-dep elements
Design a package for encapsulation of elements for environmental testing
Lower TCR of elements to meet contract objective performance (or request change in specs)
Fabricate and test a sufficient number of finished devices for reliability information
Build, test and submit 20 of best (lowest TCR most stable, etc.) elements to BuShips
Evaluate and furnish 150 engineering samples of low TCR devices to BuShips
Complete final engineering report



Jan. Feb. Mar. Apr. May June July Aug. Sept. Oct. Nov. Dec.



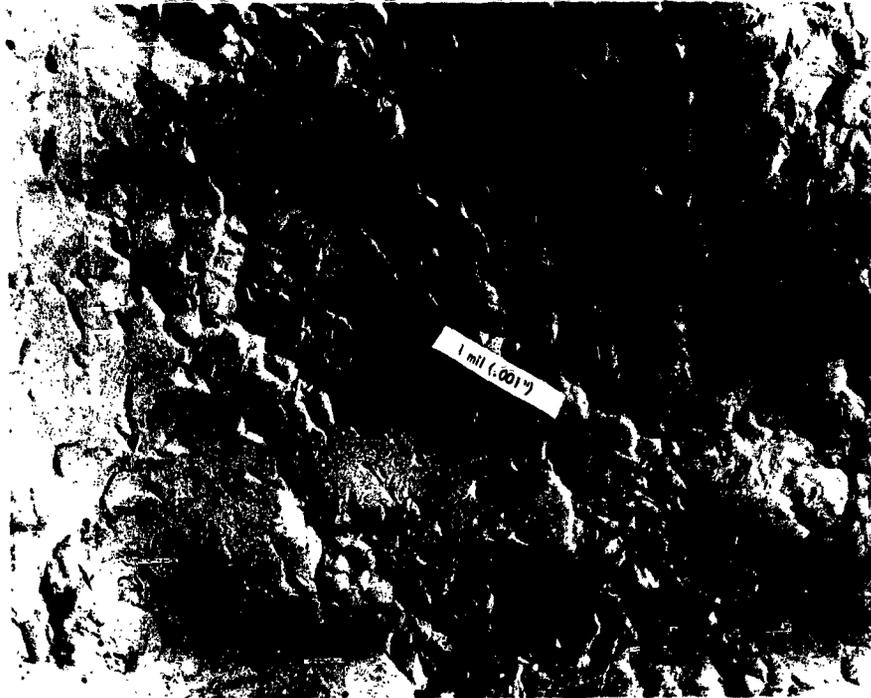
A. Micro Photograph of Epitaxial Silicon Layer,
Stained and Viewed under Sodium Light



Polycrystalline Silicon
1000x



Etched Alumina Substrate
1000x



Polycrystalline Silicon (6000x)
As - Deposited Surface



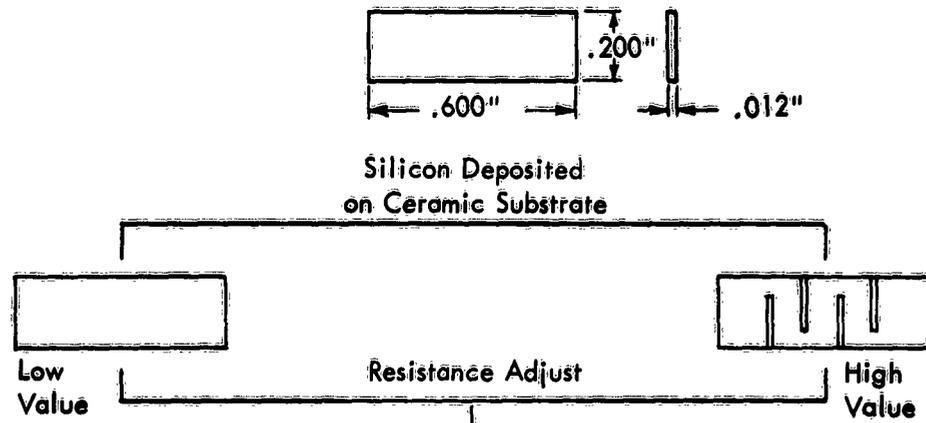
Polycrystalline Silicon (6000x)
Etched Surface



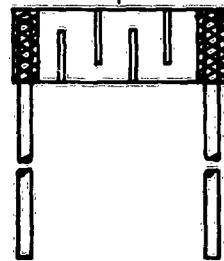
↑
↓
.39 mils
10 microns
Silicon

Alumina Ceramic

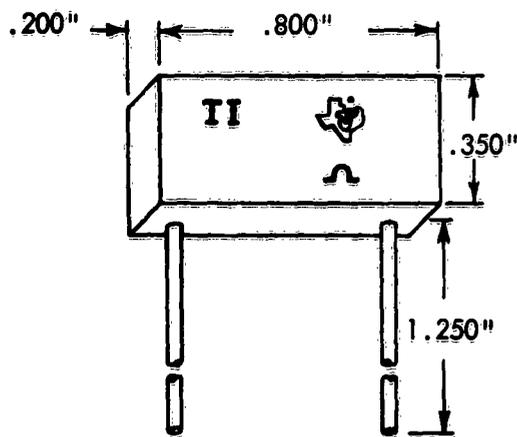
Lapped Cross-Section Through
Silicon Layer - Alumina Substrate
(400x)



Ohmic Contacts Applied

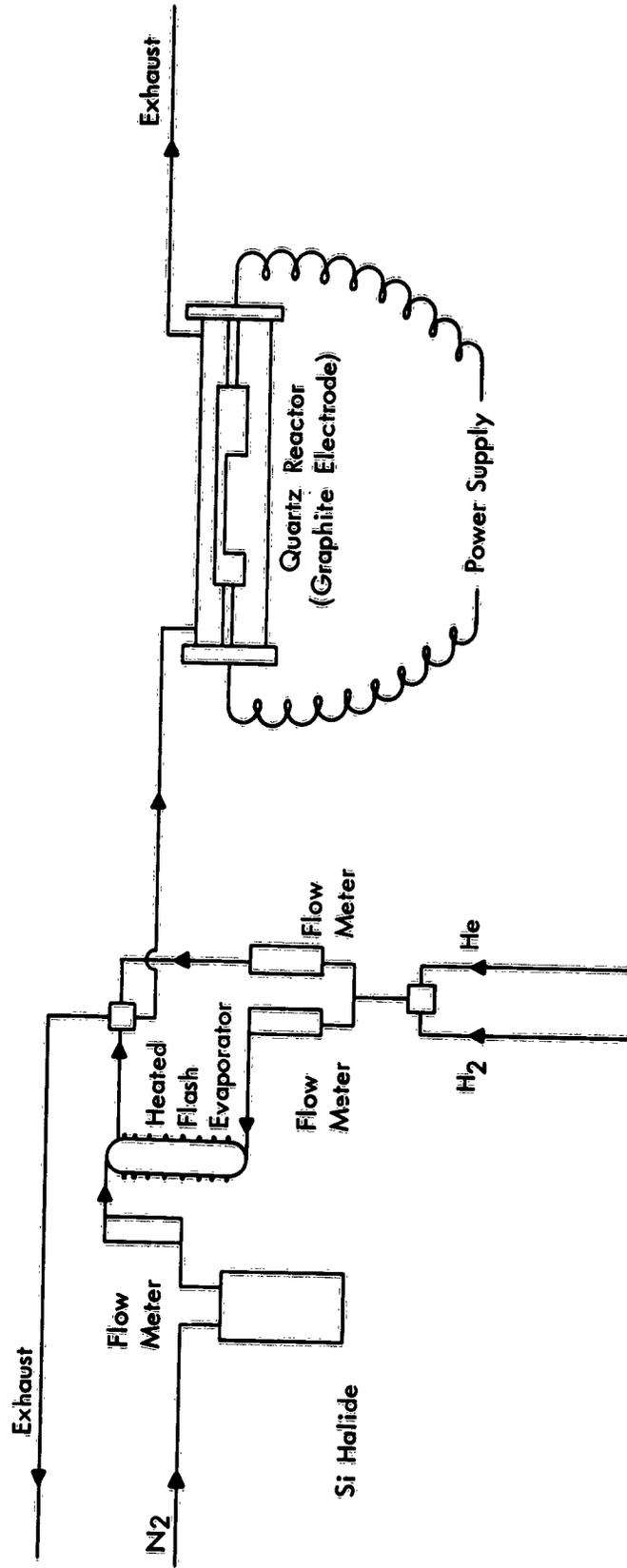


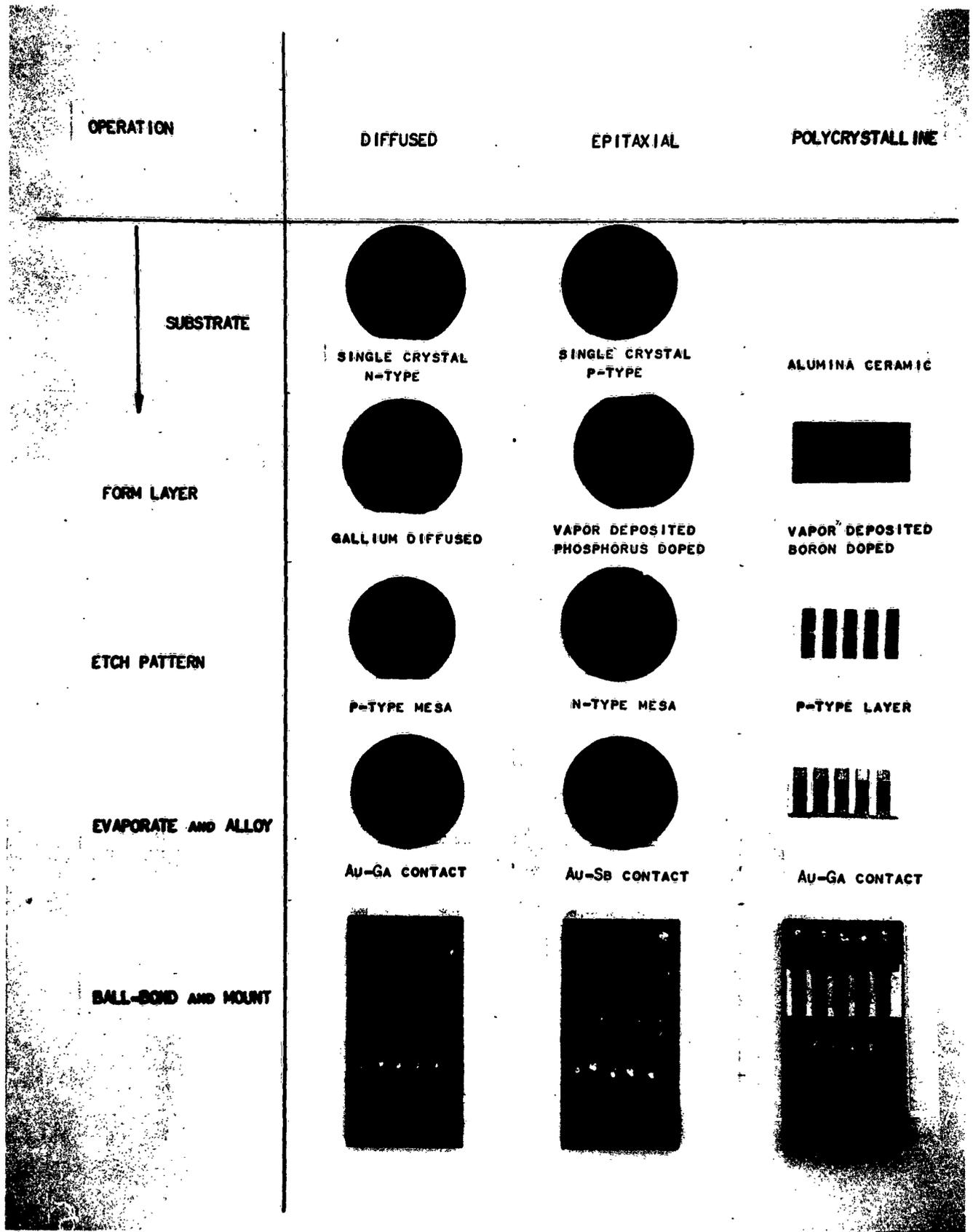
Lead Attachment



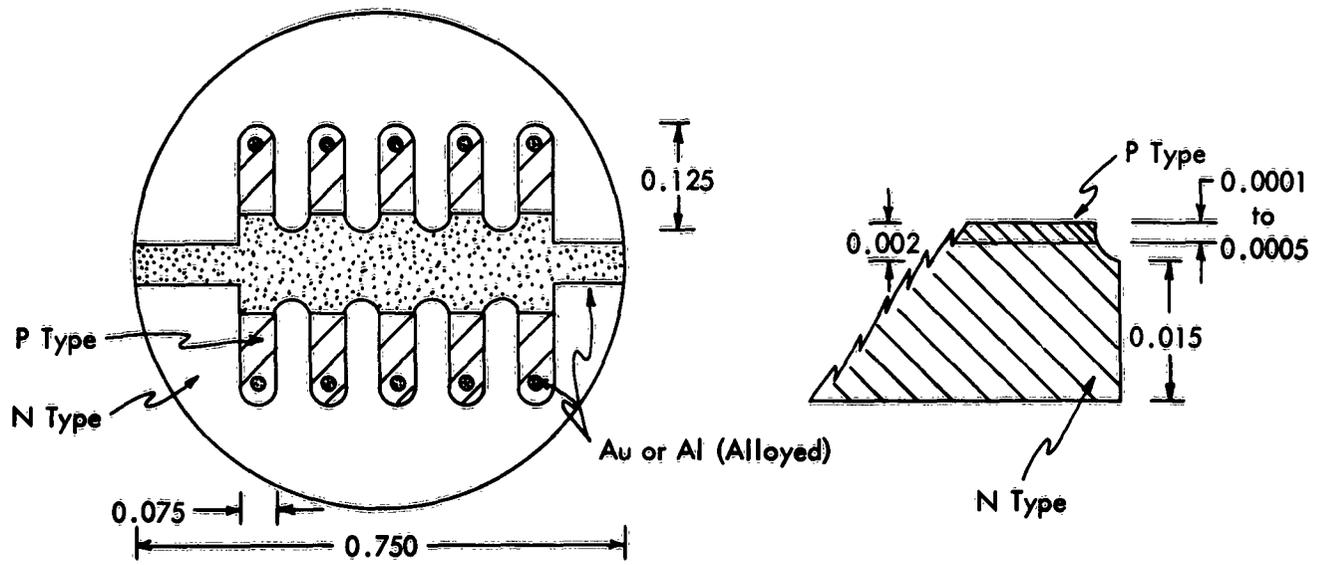
ASSEMBLY AND PACKAGING FLOW DIAGRAM

SILICON DEPOSITION SYSTEM

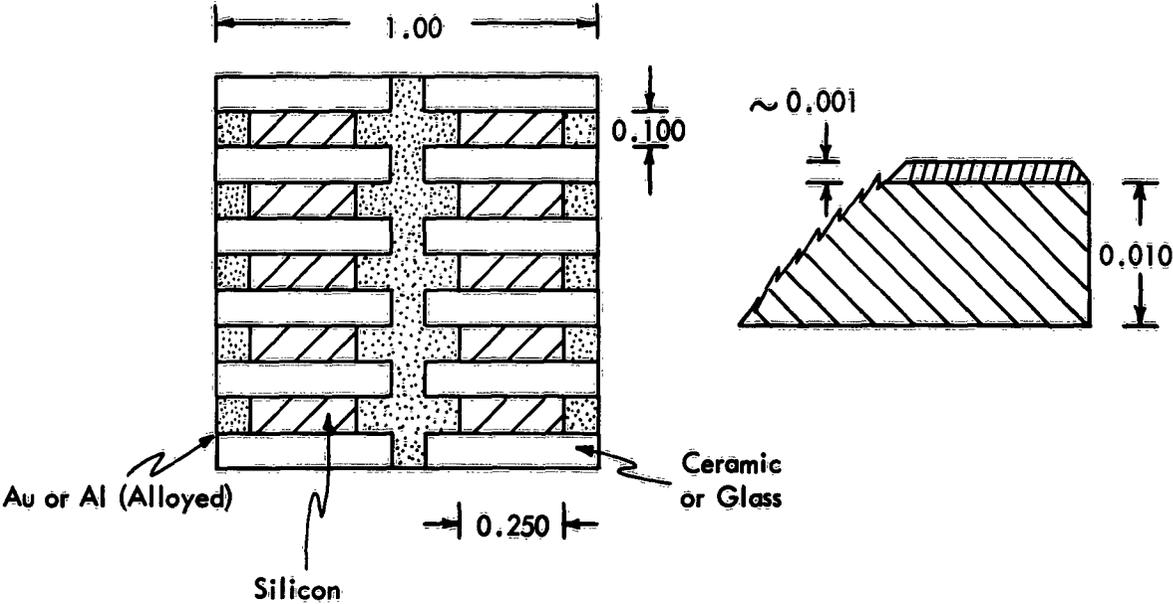




CONFIGURATION FOR EPITAXIAL AND DIFFUSED SILICON ELEMENTS

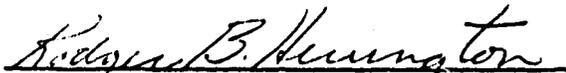


CONFIGURATION FOR POLYCRYSTALLINE ELEMENTS



SIGNATURES

THIS CONCLUDES THE FINAL ENGINEERING REPORT FOR SEMICONDUCTOR RESISTIVE
ELEMENTS UNDER CONTRACT NOBSR-85406.


RODGER B. HERRINGTON
OPERATIONS CONTRACT MANAGER


OLIN B. CECIL
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RESISTOR DEPARTMENT


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