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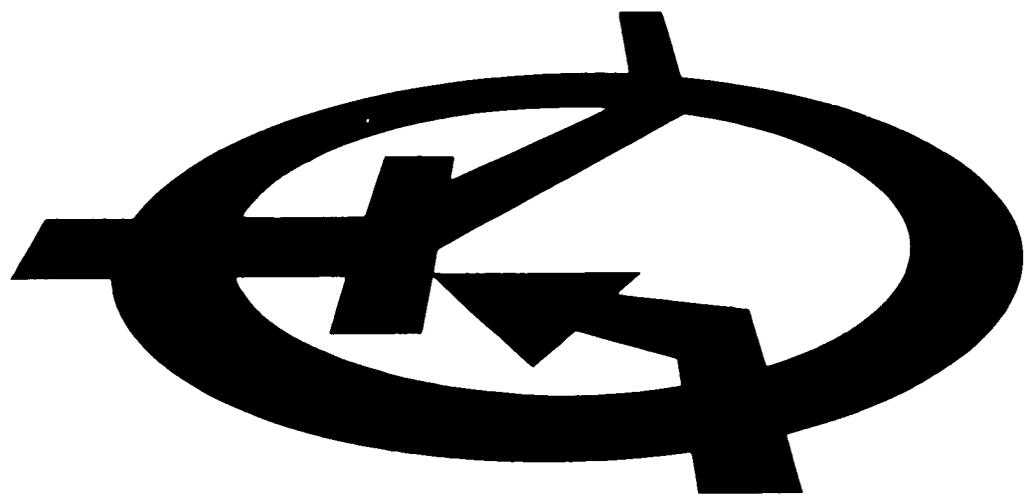
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QUARTERLY REPORT NO. 2
PRODUCTION ENGINEERING MEASURE
ON
2N1708 SILICON PLANAR EPITAXIAL TRANSISTOR

CONTRACT NO. DA-36-039-SC-86729

FOR

U.S. ARMY ELECTRONICS MATERIAL AGENCY
PHILADELPHIA, PENNSYLVANIA

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ABSTRACT

Engineering Samples and Reliability Tests

The second group of twelve engineering samples was shipped to the Signal Corps on August 15, 1962. Step-stress tests were performed on a corresponding lot of 24 units. The majority of failures were not attributable to failure mechanisms which occur at any of the reliability test or operating conditions.

A matrix test was performed on factory units, each cell representing various combinations of power and ambient temperature. Units in each cell were tested for 1,000 hours. Known device failures occurred in those cells representing the maximum stress conditions. The acceleration factors as indicated by the test were within the control limits.

One thousand hour life and mechanical and environmental tests are being run weekly. On the basis of limited results, no failures have occurred except among those units subjected to 300 mw. Steps are being taken to eliminate these failures.

Stem Development

Stem development is proceeding in two directions. Considerable engineering effort is being devoted to solving production problems which have arisen in the manufacture of the ceramic stem. In addition, a TO-46 stem of the stamped design with a Kovar to glass seal has been established which will meet reliability requirements.

Device Processing

Further modifications and improvements have been made in the pilot line which has been established to manufacture high reliability units.

Effort is continuing in the preparation of revised standards.

Striations believed due to micro impurity segregations have been observed in the surface of substrate wafers. These striations result in an undesirable surface after the epitaxial deposition process. Tests are being performed to improve the surface of substrate wafers.

Process improvements have been introduced into the epitaxial deposition operation. Improved methods of process control have been established.

Studies have been made of oxide growth as a function of temperature, time and atmosphere. Studies have also been made of the oxide thickness necessary to prevent phosphorus diffusing into the silicon under various conditions.

An evaluation of methods of removing photo-resist after the photo-resist operation has been undertaken. Studies of the purity of liquid material used in photo resist have indicated the benefits of filtration.

Methods of reducing surface contamination during wafer processing, have been studied. It has been found that certain high molecular weight alkyl-or aryl-substituted polymeric ethylene glycol derivatives may be substituted for waxes used in lapping, polishing, and scribing wafers. In addition, an acidic hydrogen peroxide solution is being used in cleaning substrates. This has demonstrated more complete removal of metallic trace impurities. Further, container purity has to be studied and those with less impurities have been designated for particular uses, as appropriate.

A detailed study was made of one aspect of the phosphorus diffusion process, i.e., the P_2O_5 carrier gas system. The effect of source depletion, source temperature, carrier gas and carrier gas flow rate was determined. It has been established in the laboratory that a fresh P_2O_5 source should

be used for each run and the optimum source temperature is $220^{\circ}\text{C} \pm 5^{\circ}\text{C}$. The present nitrogen carrier gas system and flow rates are satisfactory.

The formation of contacts by the evaporation of gold and gold alloy has been evaluated to eliminate the formation of "purple plague". Initial samples are encouraging and further testing will be performed.

An improvement in the mounting technique has been achieved by evaporation of gold on the back of the pellet to improve wetting. Studies are being made of temperature profiles on the K and S Mounter. Studies are also being made of continuous furnace mounting.

Tests are being run on bonding wires of various compositions other than the present gold to inhibit formation of "purple plague". None of these wires have been successfully bonded using present processing techniques.

Gold plated Kovar shells have been found to produce the most consistent seal; and welding conditions have been found less critical when this material is used. The shells will be marked with an indelible individual code to assure identification through all processing and testing subsequent to sealing.

I. PURPOSE

The objective of this contract is to improve the reliability of the RCA 2N1708 epitaxial, planar, silicon switching transistor. The failure rate goal, at a 90 percent confidence level, is 0.0011 percent per thousand hours at a junction temperature of 50°C.

To attain this objective, design and process improvements will be evaluated and put into effect. A system of process controls will be established.

Various reliability tests will be performed. These will include step stress tests, matrix tests, temperature and power aging tests, and life and mechanical and environmental tests.

A 9 to 12 month development period followed by a 6-month production phase will be undertaken. During this latter period, life testing will be employed to establish the actual failure rate of the improved 2N1708.

II. DELIVERY OF ENGINEERING SAMPLES

State-of-the-art samples were shipped to the U.S. Army Supply Agency as shown below:

Number	Date of Shipment
12	1 June 1962
12	15 August 1962

The electrical characteristics of the 12 samples shipped 15 August 1962 are shown in Table I. The electrical characteristics of the 12 samples shipped 1 June 1962 were provided in Quarterly Report No. 1. The 2N1708 Electrical Specifications are shown in Table II.

TABLE I
RCA 2N1708 STATE OF THE ART SAMPLES, AUGUST 15, 1962

	I_{CBO}		I_{CEX} μa	BV_{CBO} v	BV_{EBO} v	V_{CERL} v	V_{BE} 10ma v	V_{CE}		C_{ob} pf	h_{FE} 10ma	h_{fe} 100mc	T_S nsec	T_{ON} nsec	T_{OFF} nsec
	25°C μa	150°C μa						10ma v	50ma v						
1.	.003	5.80	05.4	68.0	6.60	20.5	.803	.186	.330	4.10	36.0	3.20	10.0	18.0	28.0
5.	.005	7.60	11.8	73.0	8.00	20.5	.819	.172	.332	3.25	100.	3.60	10.0	15.0	29.0
6.	.003	3.70	06.6	74.0	7.50	20.5	.760	.169	.295	3.60	53.3	3.10	13.0	16.0	34.0
8.	.003	4.10	06.8	68.0	7.20	20.5	.790	.172	.310	4.00	53.3	3.60	12.0	17.0	31.0
9.	.004	5.80	08.1	58.0	8.00	20.5	.782	.162	.262	4.50	61.0	3.60	09.0	18.0	28.0
10.	.004	4.80	09.2	62.0	8.20	20.5	.790	.160	.272	4.10	74.5	3.60	10.0	17.0	30.0
13.	.004	5.60	05.0	55.0	7.00	20.5	.771	.188	.325	3.75	41.0	2.40	11.0	17.0	30.0
15.	.004	5.20	06.7	56.0	6.50	20.5	.810	.165	.310	4.70	46.4	4.10	09.0	19.0	29.0
17.	.004	5.90	06.6	61.0	7.80	20.5	.802	.175	.302	4.50	54.3	3.60	08.0	18.0	28.0
18.	.004	4.70	06.7	56.0	7.00	20.5	.808	.169	.296	4.80	57.5	3.70	09.0	19.0	29.0
19.	.003	4.00	07.5	75.0	7.00	20.5	.759	.166	.277	3.70	61.4	3.80	13.0	16.0	33.0
20.	.006	5.50	06.5	55.0	7.60	20.5	.818	.181	.331	4.90	36.5	3.60	09.0	26.0	22.0

TABLE II

2N1708 ELECTRICAL SPECIFICATIONS

T_J	V_{CBO}	V_{CEO}	V_{EBO}	I_C	P_d ($T_A=25^\circ\text{C}$)
-65°C to 175°C	25v (max)	12v (max)	3v (max.)	200ma (max.)	3 watts (max.)

Characteristics $T_A = 25^\circ\text{C} +$	Conditions	Limits		Units
		Min.	Max.	
I_{CBO}	$V_{CB}=15\text{v}, I_E = 0$		0.025	μa
I_{CBO}	$V_{CB}=15\text{v}, I_E = 0, T_A = 150^\circ\text{C}$		15.0	μa
I_{CEX}	$V_{CE}=10\text{v}, V_{BE} = .025\text{v}, T_A = 100^\circ\text{C}$		15.0	μa
BV_{CBO}	$I_C = 100\mu\text{a}$	25.0		v
BV_{EBO}	$I_E = 100\mu\text{a}$	3.0		v
BV_{CEO}	$I_C = 10\text{ma}$	12.0		v
$V_{BE}(\text{Sat.})$	$I_C = 10\text{ma}, I_B = 1\text{ma}$	0.7	0.9	v
$V_{CE}(\text{Sat.})$	$I_C = 10\text{ma}, I_B = 1\text{ma}$		0.22	v
$V_{CE}(\text{Sat.})$	$I_C = 50\text{ma}, I_B = 5\text{ma}$		0.35	v
C_{ob}	$V_{CB} = 10\text{v}, I_B = 0, f = 140\text{kc}$		6.0	pf
h_{FE}	$I_C = 10\text{ma}, V_{CE} = 1\text{v}$	20.0		
h_{fe}	$I_C = 10\text{ma}, V_{CE} = 10\text{v}, f = 100\text{mc}$	2.0		
t_s	$I_C = I_{B1} = I_{B2} = 10\text{ma}$ $R_C = 1000\Omega, V_{CE} = 10\text{v}$		25.0	n sec.
t_{on}	$I_C = 10\text{ma}, I_{B1} = 3\text{ma}, I_{B2} = 1\text{ma}$ $V_{CC} = 3\text{v}, R_C = 270\Omega$		40.0	n sec.
t_{off}	$I_C = 10\text{ma}, I_{B1} = 3\text{ma}, I_{B2} = 1\text{ma}$ $V_{CC} = 3\text{v}, R_C = 270\Omega$		75.0	n sec.

[†]Unless otherwise specified

III. STEM DEVELOPMENT (G. Granger)

A. Ceramic Stem

As stated in the First Quarterly Report, an order was placed for 5,000 ceramic stems. When the supplier increased production to satisfy the requirements of this order, production problems developed. Considerable engineering effort is being devoted to solving these problems because of the many advantages of a stem of this design as discussed in the previous report.

B. Glass to Metal Stem

Because of the production problems associated with the ceramic stem immediate steps were taken to establish a specification for a suitable glass to metal stem which will meet the reliability requirements of the contract. The stem which has been ordered for this program is a TO-46 stem of the stamped design with a Kovar to glass seal. The specification includes the use of clear glass and a bubble criteria to eliminate any inherent weakness in the seal.

IV. DEVICE PROCESSING

A. Introduction (P. Grenier)

The pilot line has been changed from that previously reported, as shown in Figures (1) and (2). The following is a summary of these changes.

- 1) The crystal growing and substrate preparation sections have been omitted. The important technical requirements for these sections have been included in the parts standard for Polished Substrates (1).
- 2) Many process control and quality audit steps have been added.
- 3) The assembly and testing sections, beginning with Mounting (58) have been expanded.

A major effort is in progress to prepare standards for each step shown on the flow chart. The present standards are being reviewed, expanded and improved commensurate with high reliability. Particular effort is being expended as follows:

- 1) Materials standards for all chemicals, gases, etc. consumed in the manufacture of the transistor.
- 2) Inspection criteria for wafers-both visual and electrical

B. Crystal Substrate Growth (R. Czorny, P. Grenier)

The techniques for growing silicon crystal and preparing substrates for silicon planar epitaxial transistors are considered satisfactory for production of a high reliability 2N1708. The specifications for procurement have been expanded and improved and visual limit samples for substrates established.

One difficulty that has been investigated is the appearance of striations on the surface of substrates. These striations are believed to be due to micro impurity segregations (1). This is objectionable because it affects pattern definition in the photo resist process.

The crystal is grown by the vertical Czachrolski method. Changes in

(1) Meltzer G "Minute Resistivity Variations in Germanium Crystals and Their Effect on Device", J. Elec. Chem. Soc. 109 No. 10 - Oct. 1962, Pg.47.

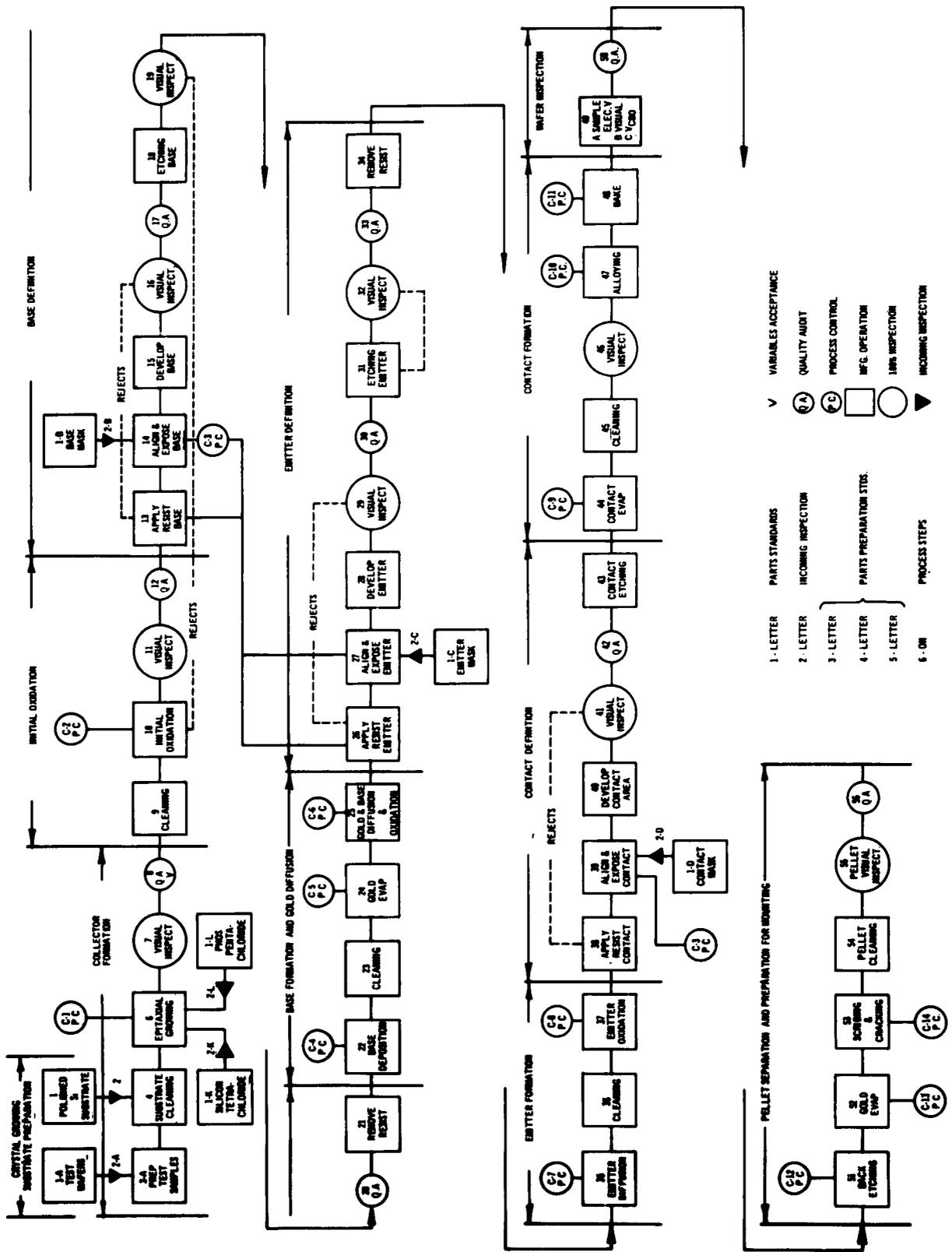


FIGURE 1 - FLOW CHART RELIABILITY IMPROVEMENT PROGRAM TA2100A - WAFER PROCESSING

crystal growth conditions, particularly in reducing cup and seed rotation rates, have improved this condition.

An alternate approach being investigated is the use of mechanically polished wafers followed by a light etch to remove the work damaged surface. Preliminary results indicate excellent surfaces.

C. Epitaxial Layer Preparation (U. Roundtree, P. Grenier)

Various processing improvements have been introduced to improve reliability of the device as described below. The revised standard for the process is being prepared together with procedures for process control.

Epitaxial layers with controlled thickness and resistivity have been grown using the hydrogen reduction of silicon tetrachloride doped to the required level with phosphorus pentachloride. To achieve the best possible control, it was necessary to hold constant several of the critical variables: deposition temperatures, growth rate, and hydrogen flow rates. For the ranges of interest, i.e., layer thickness of 0.4 - 0.55 mil and layer resistivity of 0.4 - 0.7 Ω -cm, these variables were optimized. For this relatively wide resistivity range, it was felt that solution doping (PCl_5 in SiCl_4) would be adequate.

The resistivity of the epitaxial layers was determined from a four point sheet resistance measurement times layer thickness on opposite conductivity control samples (P-type). This method of determining resistivity is in agreement with capacitance voltage measurements made on N on N^+ wafers.

The thickness of the epitaxial layer is measured on N^+ control samples by an infrared spectro photometer. This method is a non-destructive test and is made on a sample rather than on the wafer itself to reduce the possibility of contamination of the wafer surface through handling.

D. Oxide Growth and Surface Passivation (W. Greig, L. Pomante, A. Miller)

Standards for the oxidation operation are being revised, as necessary,

to insure high reliability. Studies in this area have been undertaken as described below:

1. Growth rate of SiO_2 on Si as a function of temperature, time and ambient.

Growth rates have been determined for a temperature range of 900°C - 1300°C oxidation times have been varied from 15 minutes to 16 hours. Oxidizing ambients investigated were dry oxygen and steam. For the case of steam oxidations a carrier gas was used which passed through the steam generator. The results obtained are shown in Figure (3) and Figure (4).

It can be seen from comparison of the figures that the rate of oxide growth is more dependent on atmosphere than on temperature. Steam oxidation is employed on the 2N1708 because of the higher growth rate. Further growth rate as a function of the oxidation time follows a parabolic law.

To obtain oxide thickness under the various conditions, the following procedure is used: A portion of the oxidized wafer is masked by coating it with apiezon wax. The partially masked wafer is then etched in a dilute solution of HF to remove the SiO_2 from the unmasked areas. Upon removal of the wax, a well defined "step" is evident between the oxide and the bare silicon surface.

Measurements of the height of the "step", which represents the thickness of the oxide, are made using an interference microscope. For accuracy of this measurement it is necessary to have an opaque surface. This is accomplished by evaporating a uniform layer of Au (or Al) over the whole wafer.

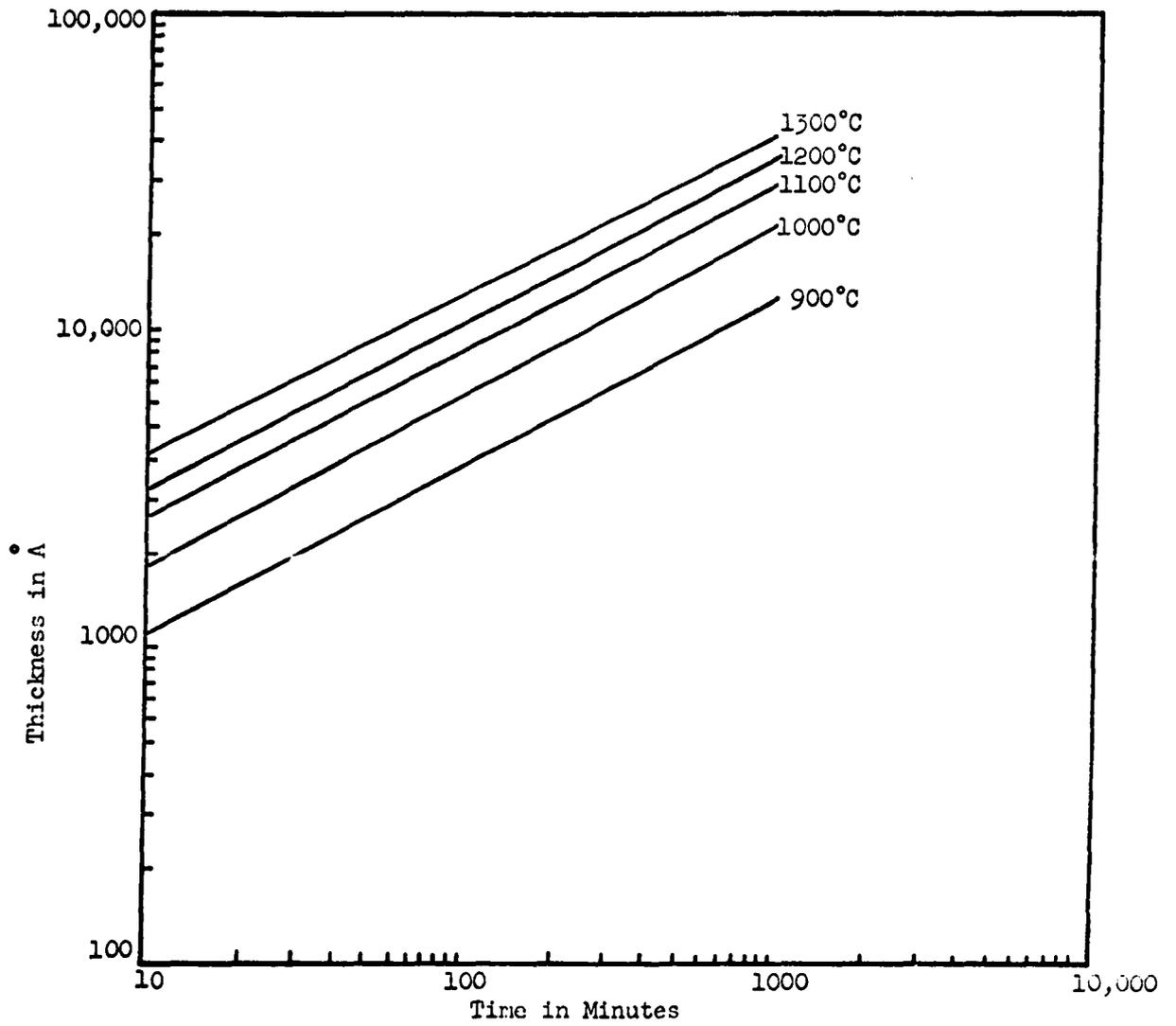


FIGURE 3 GROWTH RATE USING STEAM

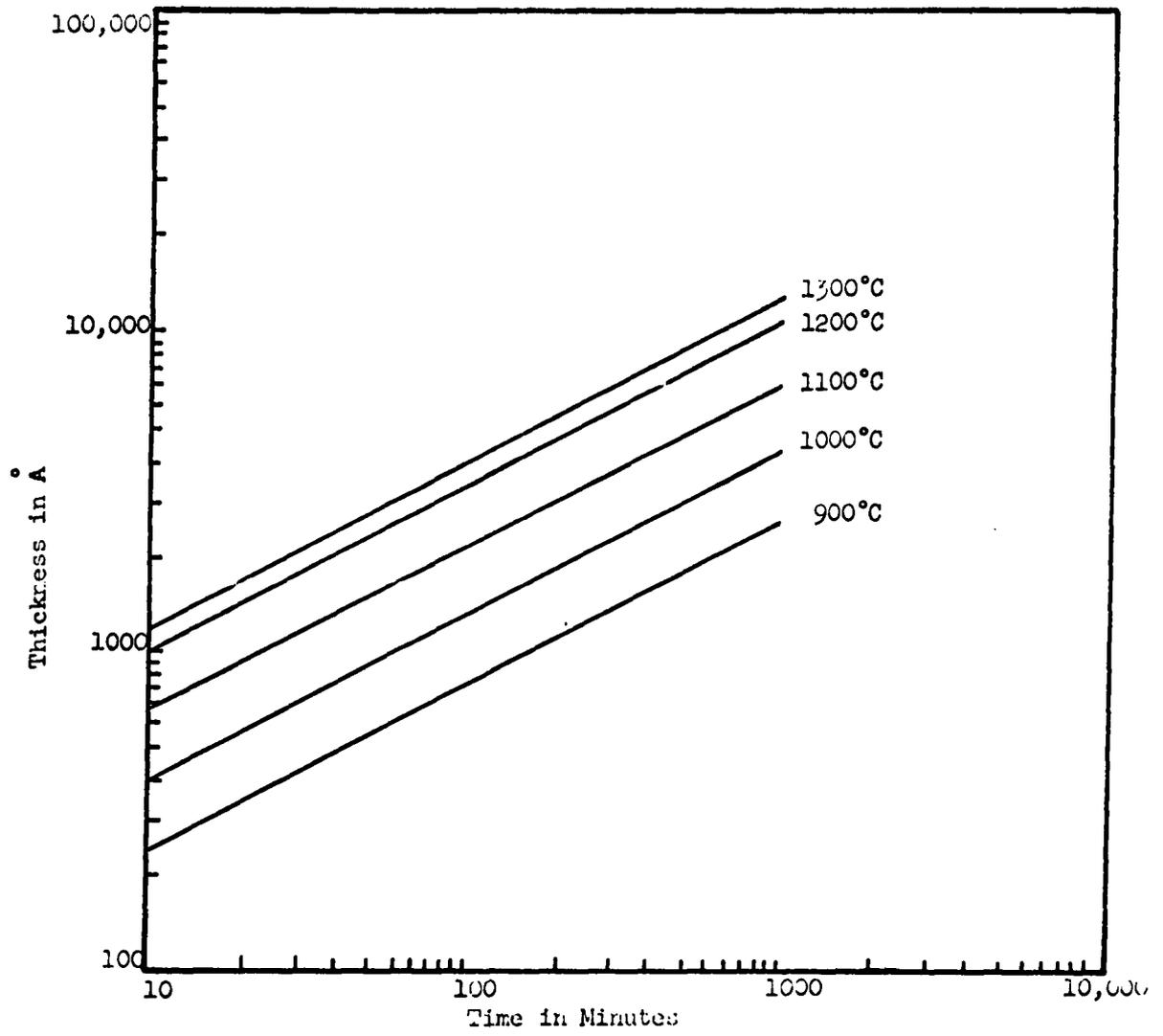


FIGURE 4 GROWTH RATE USING DPM OXYGEN

2. Oxide masking against phosphorus diffusion

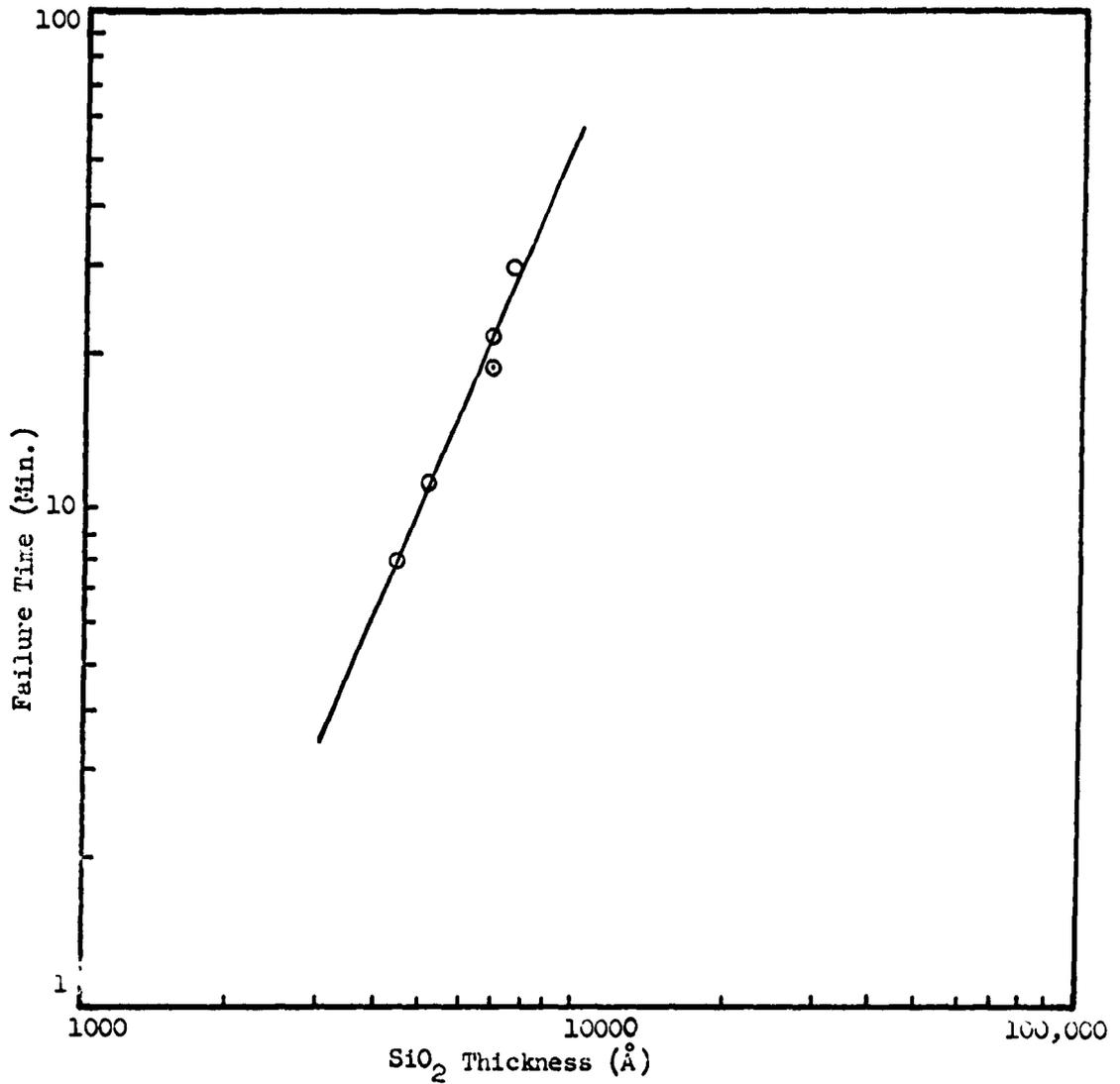
The masking capabilities of SiO_2 during phosphorus diffusion were studied. The results are shown in Figure (5) where mask failure time is plotted versus oxide thickness.

From these data the oxide thickness can be optimized according to the time of phosphorus diffusion under the conditions employed for the 2N1708. For example, with the present base oxide thickness of 8,000 Å, it can be seen that oxide mask failure will occur after 33 minutes of phosphorus diffusion time. This is considerably in excess of the present times utilized for emitter diffusion.

The determination of masking capability was made as follows: Using a P_2O_5 open tube carrier gas system under conditions simulating those of the phosphorus emitter diffusion, wafers having oxides of various thicknesses were subjected to the P_2O_5 vapors at a temperature of 1100°C . Penetration of the phosphorus diffusion through the SiO_2 was determined by removing the oxide and thermal probing the surface to determine conductivity type. Since the wafers were p-type conductivity, presence of an n-type layer on the surface following diffusion was indicative of SiO_2 mask failure. This procedure was repeated in order to obtain a relationship between the oxide thickness and mask failure time, i.e., the time of which phosphorus will have diffused through a given oxide thickness.

E. Photo-Resist and Etching Technique (J. Emanuel, W. Kern)

Detailed standards have been prepared for the photo-resist and etching techniques. The present process is satisfactory for production of high reliability transistors. However, work is proceeding in two major areas to further insure reliability. These are: improved method of removing



Silicon Temperature - 1100°C P₂O₅ Open Tube

FIGURE 5 MASK FAILURE TIME VERSUS OXIDE THICKNESS

photo-resist; improved process controls and inspection criteria.

The present methods of removing polymerized photo-resist films include spray-cleaning with methylene chloride and combustion. These techniques may have certain detrimental effects. Because of the pressures required, spray-cleaning may cause the SiO_2 surface to be torn and pitted. Also, combustion removes the bulk of the organic material but leaves an ash which contains metallic impurities which are fairly certain to contribute to electrical degradation.

Many organic chemicals have been tested as removal agents for photo-resist films. A group of organic nitrogen compounds show the strongest attack. Listed in order of their effectiveness they are hexahydropyridine, phenylhydrazine, aminobenzene and n-methylacetamide. Tests are being run in order to determine the effect, if any, these compounds have on the electrical characteristics of the device.

Photo-resist can be completely removed by immersion in a sulfuric acid-hydrogen peroxide solution or in a sulphuric acid-potassium bi-chromate solution. Both of these solutions result in quick and certain removal. Tests are now in progress to determine their effects, if any, on the electrical characteristics of the device.

The liquid materials used in the photo-resist process are being studied. Filtration has disclosed the presence of considerable foreign matter. The solvents have been filtered through a 1.5μ filter. The photo-resists have been filtered through 10μ filters. Residue-after-evaporation tests run on both filtered and non-filtered material show that filtration removes between 50 and 90% of the foreign matter. Controlled tests are in progress to determine the effect of these filtered reagents on the electrical properties of the 2N1708.

F. Surface Preparation and Cleaning (W. Kern)

1. Introduction

The extreme importance of the semiconductor surface of a solid state device with respect to its performance and reliability is well recognized, but not generally given the degree of attention it deserves in device technology. Nearly every one of the numerous processing steps that are required in manufacturing a device affects the semiconductor surface intentionally or inadvertently to some degree by physical or chemical actions and must therefore be strictly controlled. Surface contamination plays an important part in considerations of this nature and requires not only advanced analytical and technological methods, which are being developed and applied in the course of this project, but also requires a critical attitude and work philosophy of its own.

Investigations carried out during this reporting period have been primarily directed towards the early stages of device processing and the following is a summary to date of these investigations.

2. Mounting of Semiconductor Wafers

A variety of natural and synthetic waxes are conventionally being used for mounting semiconductor wafers in lapping, polishing, scribing, and etching operations. The bulk of the wax is later removed by rinsing with organic solvents. However, it was found that monomolecular layers of residues always remain on the semiconductor surfaces, even after extensive solvent extraction treatments. These residues constitute one of the serious sources of contamination which may lead to adverse device effects. A substitute was therefore sought that has none of the undesirable properties of waxes while retaining some of their adhesive characteristics. Preferably, the substitute should be water soluble,

have a non-ionic molecular structure that has no adsorption affinity to semiconductor surfaces, should be sufficiently resistant against the usual chemical etching solutions, and have convenient melting properties. An extensive search showed that certain high-molecular weight alkyl-or- aryl-substituted polymeric ethyleneglycol derivatives are excellently suited for this purpose. Some of these non-ionic compounds show also outstanding detergent activity so that they have a double effect as adhesive and surface cleaning agent. The method has been applied in the present reliability improvement program for mounting silicon wafers for etching, with excellent results.

3. Substrate Etching and Rinsing Treatments

The silicon wafers used in this project as substrate material are mounted on Teflon blocks by the above method and treated with a CP4-type etch in a rotary system. After the work damaged surface layers are removed the wafer surface has a mirror finish. The etchant is diluted rapidly with deionized water, and the wafers are thoroughly rinsed in cold and hot deionized and distilled water. They are visually clean at this stage. However, radio chemical studies recently conducted at RCA have demonstrated that metallic trace impurities contained in the original electronic grade etch reagents at parts-per-billion concentration levels deposits on semiconductor surface during etching. The significant observation is the fact that impurities usually become concentrated on the sample surfaces to an extent that will deleteriously affect device characteristics on subsequent processing.

For example, silicon wafers etched for 60 seconds in an iodine-containing CP4 type etch to which 5 ppm of gold-198 had been added showed surface concentrations in the range 10^{13} to 10^{14} atoms per cm^2 , or about one tenth of one monatomic layer. Similar results were obtained .

with other metals and etchants. The decontaminating effects of various chelating and complexing agents in treating such wafers were examined in a quantitative study. One of the best systems found is hydrogen peroxide containing a small amount of distilled hydrochloric acid. Three typical desorption curves for this system are presented in Figure (6); these were obtained with wafers that had been etched in reagents labelled with radioactive gold (10 to 30 ppm). In addition, trace analysis of spent desorption solutions have shown significant concentrations of copper, chromium and iron.

This purification treatment, followed up with hot rinses of deionized and doubly quartz distilled water, has been incorporated in the substrate preparation schedule of the present project and is considered an important improvement.

4. Container Purity

The nature and purity of the container material used in processes where trace impurities are of concern must be compatible with the purity objectives. Radiochemical analyses and solubility calculations have shown that sufficient amounts of impurities can be leached out of Pyrex glass even with water, contaminating semiconductor surfaces to a serious extent.

Generally, in the reliability program, the liquid-storage containers are made of polyethylene and the high temperature containers of natural fused silica. However, for certain purposes synthetic fused silica is used which has orders of magnitude lower impurity concentrations than the ordinary silica as stated in a recent RCA publication (W. Kern, Neutron Activation Study of Gallium Arsenide Contamination by Quartz, J. Electrochem. Soc. 109, 700 (1962)). The normal processing vessels

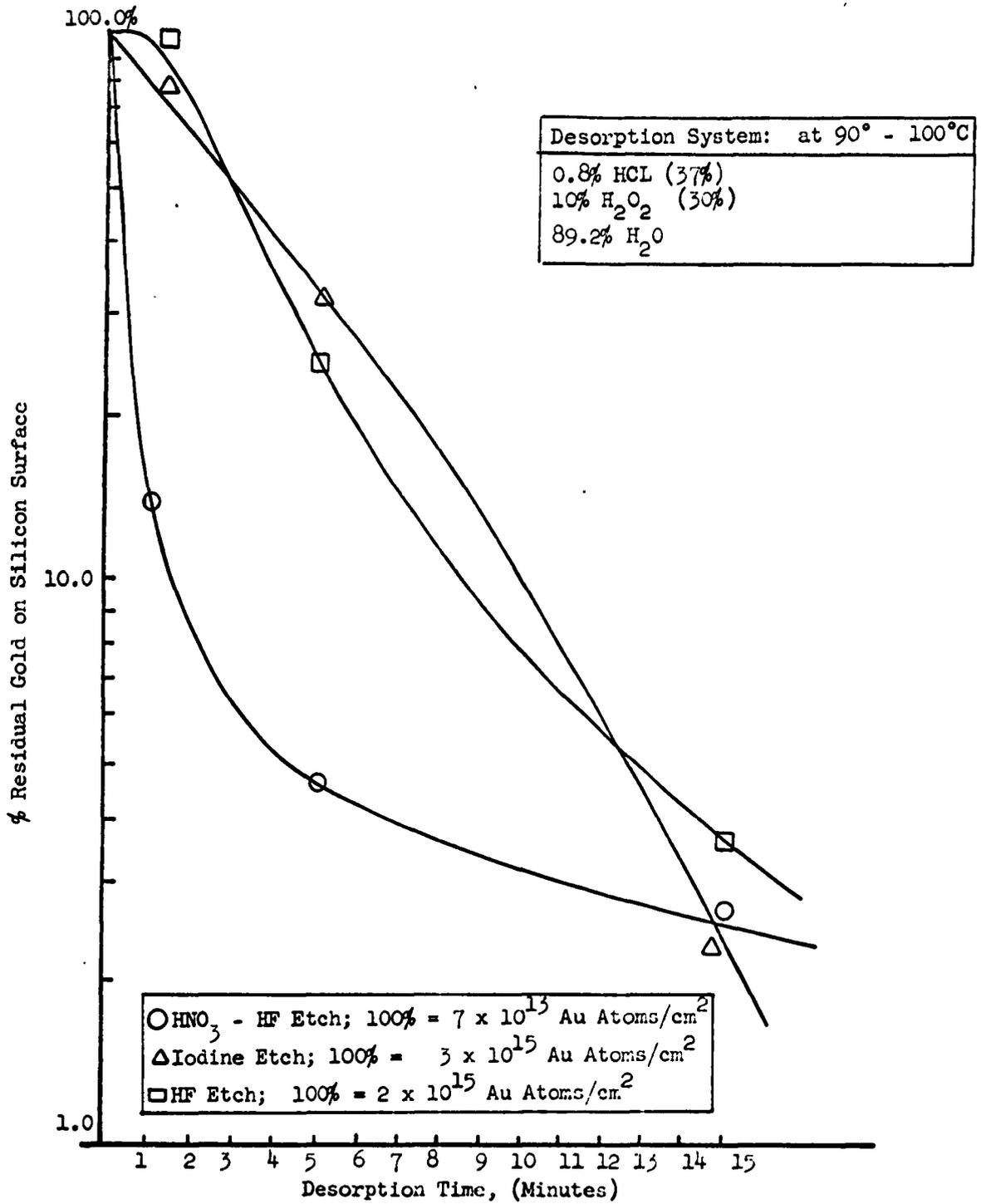


FIGURE 6 DESORPTION OF GOLD LAYERS FROM SILICON SURFACES

are made from either natural fused silica or polyethylene.

G. Diffusion Processing (W. Greig, S. Policastro)

Revised standards, which are more specific and detailed, are essentially completed for the diffusion processing operation.

One of the important engineering efforts in this area has been a detailed study of the P_2O_5 carrier gas system. This study was concerned with determining the variables inherent in the system, particularly with respect to 2N1708 process requirements.

The following system variables were found to effect the reproducibility and controllability of the resulting diffusion parameters:

- (1) Source depletion
- (2) Source temperature
- (3) Carrier gas
- (4) Carrier gas flow rate

The effects of each of these variables are discussed briefly below:

(1) Source depletion

It has been determined that an apparent depletion of the P_2O_5 source takes place the longer it remains in the furnace. This is demonstrated by a significant increase in sheet resistance (decrease in surface concentration) on test wafers diffused successively using the same source. This difficulty can be avoided by using a fresh source for each phosphorus diffusion.

(2) Source temperature

The source temperature controls the vapor pressure of the P_2O_5 which in turn affects the surface concentration of the phosphorus in the silicon. Experiments have shown that control of the source temperature is essential for reproducibility of the diffusion parameters.

It was also found that the source depletion problem was dependent upon the source temperature with depletion being more rapid at higher temperatures.

An optimum source temperature of $220^{\circ}\text{C} \pm 5^{\circ}\text{C}$ was established which minimized the stability problems yet provided surface concentration sufficiently high to meet device requirements. Several wafers have been processed under these conditions in the laboratory.

(3) Carrier gas

Both N_2 and O_2 have been used as the carrier gas. Above a source temperature of 250°C no difference was noted between the two gases. At lower temperatures, however, e.g. 220°C , higher sheet resistance is obtained with O_2 than N_2 .

(4) Carrier gas flow rate

Using quartz tubes of approximately 1 1/2" diameter, flow rates of 2, 4, and 8 cfh were investigated. Little or no effect was noted of 2 and 4 cfh; at 8 cfh an increase in sheet resistance was obtained.

H. Contact Preparation (G. Granger, W. Triggs)

The primary objective in the study of contact preparation and bonding (See Section IV-J) is the elimination of a condition known as "purple plague". This term aptly describes the condition and, therefore, it has become common terminology in the industry.

The "purple plague" is an intermetallic compound of aluminum and gold which forms when the finished device is subjected to temperature above 200°C . The formation of this compound has two effects on device performance:

1. It degrades the electrical characteristics, particularly saturation voltage, because of the high series resistance caused by the formation of this compound.
2. It reduces the mechanical strength of the contact due to the reduction

of wire size resulting from the diffusion of gold into the aluminum contact.

To inhibit the formation of this compound, the amount of aluminum used in making the contacts is kept to a minimum and an encapsulant is required to reinforce the aluminum to gold contacts.

Further improvement is needed to meet the high reliability goals of this contract. To accomplish this end, gold and other contact materials are being investigated.

Initial samples were fabricated with gold contacts to determine the processing problems encountered with gold. The results obtained on this test were encouraging. An improvement in bond strength was made with no initial degradation of electrical characteristics due to processing. A designed experiment has been planned to procure a more comprehensive statistical evaluation of gold contacts.

I. Mounting of Pellet to Stem (W. Preston, G. Granger)

(1) Metal evaporation on back of pellet

An evaluation of metal evaporation on the back of the silicon pellet has been completed. Because of the reduction in oxide thickness on the back of the pellet, a significant improvement in the wetting of the pellet to the stem was achieved. This process has now been adopted as a standard procedure for all pellets processed through the reliability line.

(2) K and S Mounter

A study of the temperature profile during mounting is being conducted.

(3) Continuous Furnace Mounting

An initial evaluation of furnace mounting was made. The advantages derived from the use of this process are improved

atmosphere and temperature control, reduced thermal stress on the device and the stem, and a reduction of handling of the pellet during mounting. Special preforms and stems are required for further evaluation and these have been ordered.

J. Wire Bonding (G. Granger)

(1) Thermal compression bonding-wires of various metal compositions

In order to eliminate or inhibit the growth of the "purple plague", engineering tests have been run on the use of aluminum and gold alloy wire for making the thermal compression bond to the aluminum metallized contact area.

The tests were made to evaluate the visual effect of high temperature storage on the bonds. Small quantities of devices were bonded using various bonding forces. The bonds were examined visually and with a pull test. The optimum bonding conditions were selected which produced the combination of best visual bond and maximum pull strength. Ten units were bonded under the conditions outlined for evaluation of high temperature storage. These units were not sealed.

(a) Aluminum wire

It is impossible to break through the oxide layer and obtain satisfactory bonds using conventional bonding techniques. Most of the wires lifted off without disturbing the aluminum contact.

Visual examination of the mechanical samples subjected to high temperature storage showed no evidence of "purple plague" on the stem-wire bond after 1100 hours.

(b) Gold alloy wire

The bond strength with gold alloy wire was extremely

variable with aluminum contact thickness in the range of 1000 Å. The force required to obtain a satisfactory bond was large enough to chip the silicon beneath the aluminum contact in this thickness range. When the aluminum thickness was increased to 50,000 Å, satisfactory bonds were obtained which are comparable to bonds with pure gold wire.

The results of high temperature storage on the bonds made with gold alloy wire showed no significant formation of "purple plague" after 1100 hours.

(2) Ultrasonic Bonding

A vendor of ultrasonic bonding equipment has been consulted on the problem of bonding small diameter wires to the contacts. A sample of units was provided for a study of the feasibility of making the bond with ultrasonic equipment.

K. Sealing (G. Granger)

An evaluation of shell material was made to determine the optimum material for a reliable resistance weld. It was found that gold plated Kovar produced the most consistent seal and the welding conditions were less critical when this material is used. Gold plated Kovar shells have now been adopted as standard for this program.

A coding standard has also been incorporated. All units are now marked with an indelible individual code so that identification is assured through all processing and testing subsequent to sealing.

L. Automatic Test Equipment

An automatic test set has been modified to test for I_c , V_{CBO} , and V_{EBO} . Tests for I_{CBO} will be made individually using a micro-micro ohmmeter. Such tests will be made prior, during and after aging and also

of the various down periods during life testing.

The units for power tests are being soldered into printed circuit boards. The units for high-temperature tests are being inserted in receptacles soldered into printed circuit boards. All tests are being performed on these boards thus reducing the possibility of damage due to handling and the possibility of mixing units.

The data for each transistor is being punched on its own individual data card. The cards may be used for obtaining a "run-off" of data for each transistor, a failure search and a statistical analysis using a program plan for the RCA 301 computer.

V. TEST PROGRAM

A. Step-Stress Tests (A.A. Dunham, G. Granger)

The first step stress tests were performed on 24 units as reported in Quarterly Report No. 1 (See Table III and Table IV). These units correspond to the 12 state-of-the-art samples submitted to the U.S. Army Signal Supply Agency on June 1, 1962. Temperature was employed as the sole stress on 12 of the units, while power was the stress employed on the remaining 12 units.

The second step stress tests were performed on 24 units corresponding to the 12 state-of-the-art samples submitted on August 15, 1962. (See Section II). The procedure and results obtained and a comparison with the first step stress test are discussed below.

1. Step-Stress Test-Temperature (See Table III)

Twelve units were stored for 20 hour periods instead of 3 hours as in the first test at each of the temperature steps. Also, since the gold-silicon eutectic is 372°C additional steps were added of 350°C and 370°C.

Two units survived the first 370°C period. These were then returned to the oven for an additional 20 hours after which they also failed.

The cause of failure was the same as in the first step-stress test, namely, alloying of the gold from the connector wires over the surface of the pellet.

2. Step-Stress Test-Power (See Table IV)

Twelve units were operated at room temperature for two hours at each of the power steps. A $V_{CB} = 10$ volts instead of $V_{CB} = 20$ volts, as in the first test, was applied.

TABLE III
Step-Stress Test-Temperature

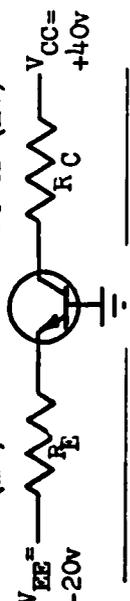
<u>Step Temperature °C</u>	<u>Hours at Temperature</u>	<u>Cumulative * % Failures</u>	<u>Manifestations</u>
<u>First Test (See Quarterly Report No. 1)</u>			
250	3	0	-
300	3	0	-
320	3	0	-
340	3	0	-
360	3	17%	1 short 1 high I_{CBO}
380	3	100%	7 open base collector to emitter short 3 shorts
<u>Second Test</u>			
250	20	0	-
300	20	0	-
320	20	0	-
340	20	0	-
350	20	0	-
360	20	0	-
370 (1st.)	20	83%	2 collector to base shorts 8 complete shorts
370 (2nd.)	20	100%	2 complete shorts

* Failure $I_{CBO} (V_{CBO} \text{ @ } 15 \text{ v}) \geq 0.5 \mu\text{a}$
or $h_{fe} (I_c \text{ @ } -10\text{ma}, V_{CE} \text{ @ } 1\text{v}) \geq 15$

TABLE IV

Nominal Power (mw)	Step-Stress Test Power			Manifestations *
	AVG. Actual Power (mw)	RE (ohms)	RC (ohms)	
200	190	2000	2000	0
400	390	1000	1000	0
500	470	800	800	0
600	570	670	670	0
700	640	570	570	0
800	760	500	500	0
1000	860	400	400	25
1200	1020	330	330	92
				100

First Test (See Quarterly Report No. 1)

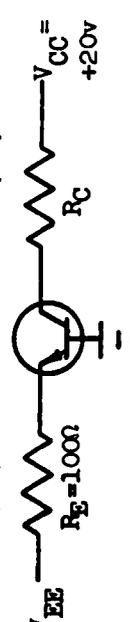


* Failures: - I_{CBO} ($V_{CBO} @ 15v$) $\leq 0.5 \mu a$ or
 h_{fe} ($I_C @ - 10ma, V_{CE} @ 1v$) 15

1 h_{fc} failure
 2 collector-emitter shorts
 8 collector-emitter shorts
 1 collector-emitter shorts

TABLE IV (Cont.)

Nominal Power (mw)	Avg. Actual Power (mw)	Step-Stress Test Power		Cumulative % Failures	Manifestations
		V_{EE} (v)	RC		
200	208	2.6	500	0	2 lost-testing error
400	418	4.6	250	0	
600	585	6.5	167	10	1 high I_{CBO} ^{**} ①
700	709	7.3	143	10	
800	862	6.8	125	70	1 high I_{CBO} } ② 1 open } 1 coll to em short } ③ 1 high I_{CBO} } ④ 2 high I_{CBO} } ⑤ 1 low β } ⑥
900	973	9.0	111	80	
1000	1409	10.0	100	100	2 high I_{CBO} ⑦



* Failures: - I_{CBO} ($V_{CBO} @ 15v$) $\leq 0.5 \mu a$ or h_{fe} ($I_C @ - 10ma, V_{CE} @ 1v$) ≥ 15

**See Text

The cause of failures are noted as follows.

<u>Nominal Power</u>	<u>Note (See Table IV)</u>	<u>No. Units</u>	<u>Failure Mechanism</u>
600 mw	①	1	unknown
800 mw	②	2	connector wire burnt, excessive base current
800 mw	③	1	"purple plague"
800 mw	④	1	gold from collector wire alloyed with silicon
800 mw	⑤	2	unknown
900 mw	⑥	1	gold from collector wire alloyed with silicon
1000 mw	⑦	1	gold from collector wire alloyed with silicon
1000 mw	⑦	1	thin aluminum contact

The failure mechanism of "gold from collector wire alloyed with silicon" was the same as those observed in the step-stress test-temperature. This would be expected since 800 mw corresponds to a junction temperature of 360-380°C at the thermal dissipation of the units. Unit variation results in some units surviving at higher dissipation.

3. Conclusion

The step stress tests performed above have not resulted in an acceleration of the normal failure mechanisms which occur at any of the reliability test or operating conditions with the exception of the one unit failing for "purple plague" in the power test. Recommendations have been made and accepted by the Signal Corps to discontinue tests of this form. Emphasis will be placed on various temperature and/or power aging tests which

is believed will be more rewarding in accelerating meaningful failure mechanisms.

B. Matrix Test

A matrix test was performed on 2N1708 units produced by the factory process. These units were not from the reliability pilot line (See Section IV-A). A second matrix test will be performed when significant process improvements have been completed and put into effect in the pilot line. It is considered advisable to delay this test somewhat beyond the data originally stated.

The matrix test and the known device failure in each cell are shown in Figure (7). Other failures were generated in each cell, however, careful failure analysis has indicated that these were probably testing errors and therefore they are not shown. Immediate action has been taken to insure that all testing errors will be eliminated on all future tests. The known device failures have fallen into a basic pattern and steps are being taken to improve this condition.

By reference to Figure (7), it may be seen that all device failures occurred in Cells 9, 6, 2 and 4. These are the cells with the highest junction temperatures considering the combined effects of power and ambient temperature. Among these cells they may be listed in decreasing order of severity as follows: 9, 6, 2, 4 and with cell No. 9, the 300° Shelf Life Test, representing the most severe test.

Cell No. 6 had the most failures. The analysis of these failures showed that three were due to foreign matter in or under the encapsulant. If these failures are eliminated there is no significant difference between failures in Cells 9, 6, 2 and 4 at the 95 percent confidence

level. In addition the results are not inconsistent with past factory life test history.

The acceleration factors as indicated by the matrix test are within the control limits. It is apparent, however, that the cell size is too small to provide much information on acceleration factors. Additional data from the second test will be helpful but the primary source for development of acceleration factors will be the Shelf and Operating Life Tests being run each week. (See below).

Power (mw)	<u>Junction Temperature</u>			
	25°C	100°C	200°C	300°C
0	Cell No.8 0	Cell No.7 0	Cell No.5 0	Cell No.9 2
150	Cell No.10 0	Cell No.1 0	Cell No.6 8	
300	Cell No.3 0	Cell No.2 1		
450	Cell No.4 2			

Note: The number of device failures are shown in each cell

FIGURE 7 FIRST MATRIX TEST

C. Life and Mechanical and Environmental Tests (A.A. Dunham, J. Vance G. Granger)

In accordance with the terms of the contract proposal samples of units from the pilot line are being subjected to Life and Mechanical Electrical Tests as shown below:

- 300°C shelf, no power - 1000 hours - 25 units/week
- 200°C shelf, no power - 1000 hours - 25 units/week
- 300 mw operating, 25°C - 1000 hours - 25 units/week
- Mechanical and Electrical ----- 35 units/week

The life and Mechanical and Electrical Test end points for the device are:

	<u>Limits</u>
	<u>Min.</u> <u>Max.</u>
h_{fe} ($I_c = -10$ ma, $V_{CE} = 1v$)	15
I_{CBO} ($V_{CB} = 15v$, $I_E = 0$)	0.5µa

Other tests being performed are:

V_{CBO} ($I_c = 5$ µa)	25v
V_{EBO} ($I_E = 100$ µa)	3v

The units subjected to Life Tests are tested to the above criteria at various down periods and at the completion of tests as shown in Figure (8). The units subjected to Mechanical and Electrical Tests are tested to the same criteria after completion of tests.

The failures, according to the end point criteria for the initial lot of units are shown for Life Tests in Figure (8) and for Mechanical and Electrical Tests in Figure 9. There were no failures after 100 hours for 200°C and 300°C Shelf Tests. There were five failures after 100 hours for the 300 mw Operating Test. There were no failures after completion of Mechanical and

Electrical Tests.

The units which failed after 100 hours at 300 mw failed for $I_{CBO} > .5\mu a$.
Analysis disclosed similar reasons for failure as observed in the matrix
test (see below). Steps are being taken to eliminate the cause of the failures.

Down Period	48 hours		100 hours		250 hours		500 hours		1000 hours	
	Total Hours	Defects								
200°C Shelf	-	-	-	-	-	-	-	-	-	-
Prior Periods	-	-	-	-	-	-	-	-	-	-
This Period	-	-	2500	0	-	-	-	-	-	-
Total	-	-	2500	0	-	-	-	-	-	-
300°C Shelf	-	-	-	-	-	-	-	-	-	-
Prior Periods	-	-	-	-	-	-	-	-	-	-
This Period	-	-	2500	0	-	-	-	-	-	-
Total	-	-	2500	0	-	-	-	-	-	-
300 mw Operating	-	-	-	-	-	-	-	-	-	-
Prior Periods	-	-	-	-	-	-	-	-	-	-
This Period	-	-	2500	5	-	-	-	-	-	-
Total	-	-	2500	5	-	-	-	-	-	-

FIGURE 8 PILOT LINE-2N1708 RELIABILITY IMPROVEMENT PROGRAM SAMPLE SHELF AND OPERATING LIFE TESTS

	Subgroup I Temperature Cycling (200°C max.) Moisture Resistance		Subgroup II Constant Acceleration (2000G) 6 Planes Shock (500G)- X ₁ , Y ₁ , Z blows in each Vibration Fatigue Vibration Variable Frequency		Subgroup III Salt Atmosphere		Subgroup IV Lead Fatigue	
	8 Units		9 Units		8 Units		10 Units	
	No. Units Tested	No. Defects	No. Units Tested	No. Defects	No. Units Tested	No. Defects	No. Units Tested	No. Defects
Prior Periods	-	-	-	-	-	-	-	-
This Period	8	0	9	0	8	0	10	0
Total	8	0	9	0	8	0	10	0

FIGURE 9 PILOT LINE-2N1708 RELIABILITY IMPROVEMENT PROGRAM SAMPLE MECHANICAL AND ENVIRONMENTAL TEST

VI. CONCLUSIONS

- A. The step-stress tests as performed have not proved successful in accelerating normal failure modes. Emphasis will be placed on various temperatures and/or aging tests of another form.
- B. The acceleration factors as indicated by the first matrix test of factory units are within the control limits. A second matrix test will be run on units from the reliability line when basic engineering improvements are completed. Due to limitations on cell size, the primary source of information on acceleration factors is expected to be the weekly life tests.
- C. Due to manufacturing problems associated with the ceramic stem a stamped design with a Kovar glass seal has been established. Work will continue on the ceramic stem.
- D. Improved methods of oxide growth and the minimum oxide thickness to mask against phosphorus diffusion has been established.
- E. Contamination of substrate and/or wafer surfaces is reduced by:
1. Substitution of certain high molecular weight alkyl- or aryl-substituted polymeric ethylene glycol derivatives for waxes used in mounting wafers in lapping, polishing, and scribing operation.
 2. Use of acidic hydrogen peroxide to remove trace metals.
 3. Use of particular containers for certain purposes.
- F. It has been established in the laboratory that a fresh P_2O_5 source should be used for each run. The optimum source temperature is $220^\circ\text{C} \pm 5^\circ\text{C}$.
- G. An improvement in the mounting technique has been achieved by evaporation of gold on the back of the pellet to improve wetting.
- H. Gold plated Kovar shells have been found to produce the most consistent seal and welding conditions have been found less critical when this material is used.

VII. PROGRAM FOR NEXT INTERVAL

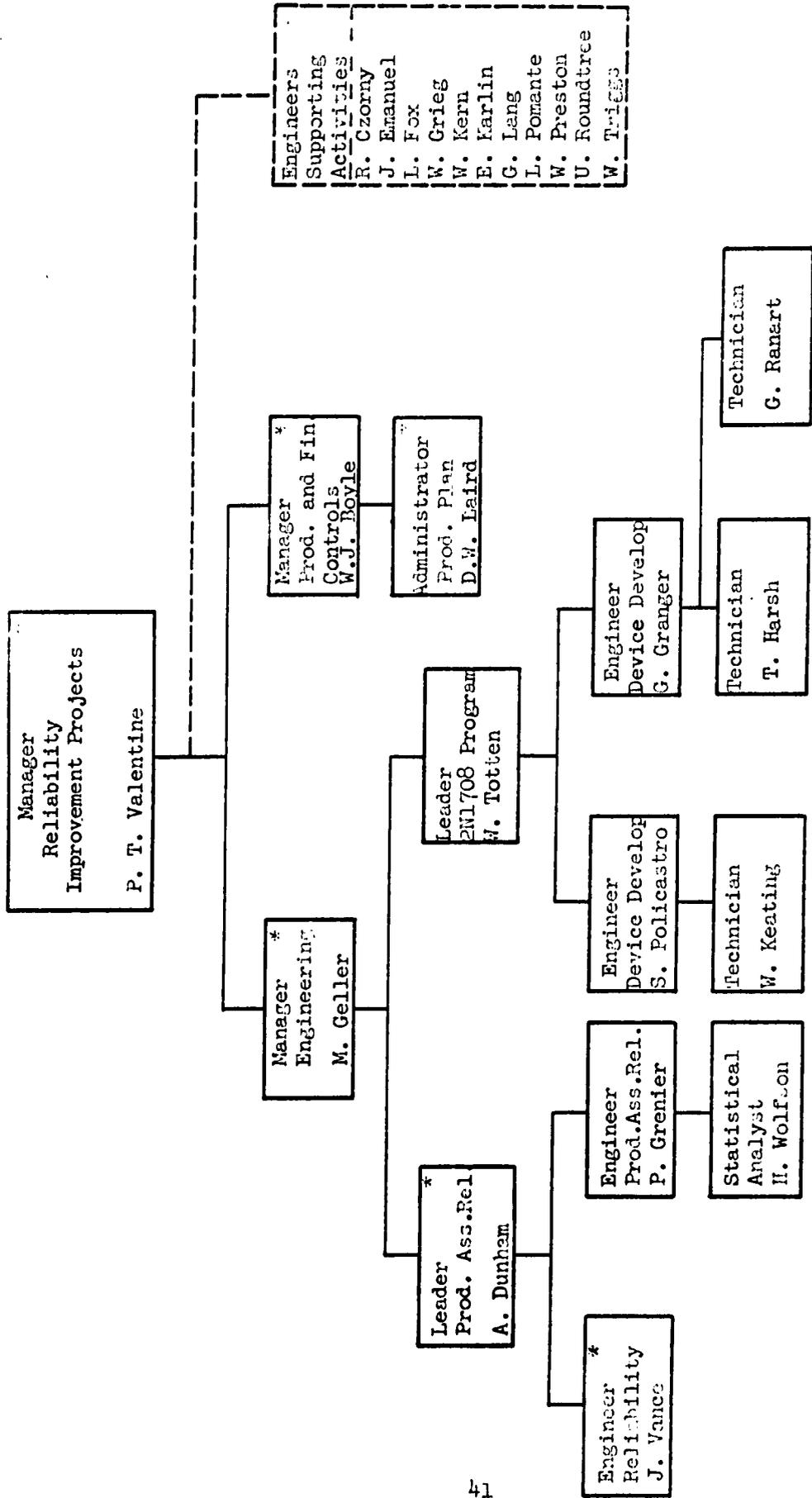
- A. Eliminate or inhibit formation of "purple plague".
- B. Evaluate various power and/or temperature aging conditions on sealed units to permit removal of questionable product prior to sampling for life and mechanical and environmental tests.
- C. Continue studies of oxides and their ability to protect the surface of the pellet.
- D. Improve phosphorus and boron diffusion techniques.
- E. Continue studies of surface contamination on substrates and on wafers and methods of reducing contamination.
- F. Improve inspections and process controls.
- G. Complete revised standards for the high reliability pilot line.

VIII. PERSONNEL AND MAN-HOURS

The engineering personnel contributing to this program during this quarter are listed in Table 5. Also indicated is a tabulation of the man hours expended on the contract. Figure (10) depicts the 2N1708 Reliability Improvement Project Organization.

TABLE V
MANHOURS FOR THE SECOND QUARTER

Name	August	September	October	Total
<u>Engineers</u>				
R.C. Pinto	184	-	-	184
W.L. Totten	184	152	184	520
G.F. Granger	184	152	184	520
A.A. Dunham	184	38	46	268
J.F. Vance	-	-	10	10
P.J. Grenier	-	152	184	336
E.W. Karlin	46	-	-	46
W. Kern	64	32	24	120
L. For	-	46	35	81
W. Triggs	-	4	9	13
G. Lang	-	16	-	16
J. Emanuel	-	-	7	7
U. Roundtree	-	-	13	13
Total Engineers	846	592	696	2134
<u>Technicians</u>				
Manufacturing Services	408	473	602	1483
Testing Services	113	30	51	194
Total Technicians	521	508	653	1682
Total	1367	1100	1349	2816



*Part Time 2N1708

FIGURE 10 2N1708 RELIABILITY IMPROVEMENT PROJECT ORGANIZATION CHART