Full Spectrum Conversion Using Traveling Pulse Wave Quantization

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Abstract: Disclosed is a new class of ultra-high-speed, low-power, full spectrum analog-to-digital conversion based on a novel temporal-domain quantization technique called Traveling Pulse Wave Quantization (TPWQ). Full spectrum conversion is defined as the complete digitization of the electromagnetic spectrum from DC up to 30-GHz. Subsequent digital processing of a full spectrum converter thus enables truly complete software defined radios, phased array antenna processors, or a myriad of other systems that previously had required extensive analog signal processing. TPWQ is implemented with pre-dominantly digital gates that favor ever advancing CMOS processes and can outperform conventional architectures by a factor of more than 4X when used in commercially available FinFet processing nodes at 16nm and below. The novel architecture is capable of achieving unprecedented state-of-the-art performance and Figures of Merit (FoM) for ultra high speed (>10 Gsps) converters.

Keywords: Data conversion; Analog to Digital; ADC; Time-to-Digital; TDC.

Introduction

The evolution of microprocessor architectures has benefitted from transistor scaling that has led to ever greater signal processing capabilities through both greater circuit density and faster device speeds. When demand for faster signal processing exceeded the capabilities of raw transistor speed the solution presented to continue increasing computational power was parallel processing with the introduction of multicore processing. The same evolutionary step has occurred for ultra high speed analog-to-digital converters (ADCs) with the advent of time interleaving architectures. This architecture, where multiple low rate ADC cores take turns sampling the analog input signal, is the basis of virtually all ADCs with sample rates in excess of 1 Gigasample per second and is depicted in Figure 1. It is advantageous to increase the sample rate of the ADC core to afford the smallest possible interleaving factor as typically >50% of the power in an interleaved ADC is used on clock distribution, signal distribution and digital interleaving correction that increases non-linearly with the interleaving factor.

The current state of the art in ultra high speed interleaved ADCs leverages one of the oldest and simplest core ADC architectures known as Successive Approximation Register (SAR)[2]. While the SAR ADC core, shown in Figure 2, has the advantage of being very simple, it relies on serial signal processing operations that determine its update rate. An 8-bit converter for instance typically requires a minimum of 10 steps at 1-bit/step with two steps used for redundancy and error correction.

The TPWQ Architecture

As modern CMOS processes favor increasing digital gate density and tighter control on timing of events, the use of temporal domain processing of analog signals becomes more attractive. TPWQ leverages temporal signal processing and moves the process of quantization from the voltage domain to the time domain. TPWQ relies on successive time pulse width measurements that are continuously generated hence the name “traveling” pulse wave quantization.

Our TPWQ-based ADC is composed of a cascade of a voltage-to-time converter (VTC) and a time-to-digital converter (TDC) that comprise a voltage-to-time-to-digital converter (VTDC) as shown in Figure 3. The function of the VTC is to convert the analog input signal in the voltage or current domain to a clock pulse where the analog signal is encoded in the pulse width. The VTC bears resemblance to the SAR architecture but since it performs a single step without recursion, it is significantly faster.
A simplified schematic example of a VTC circuit is shown in Figure 4 and its operation is detailed in Figure 5. It has a sampling capacitor to which the input signal is sampled through a sampling switch and held as a charge on the capacitor. Immediately after the sampling event a current discharge path is enabled to discharge the capacitor at a constant rate. This voltage ramp on the capacitor is monitored with a comparator that generates a digital signal edge thereby coding the analog voltage into a pulse. The pulse is then passed to the TDC. It is interesting to observe that while the VTC and TDC perform distinct functions, there is no need for a sample/hold function to pass a signal from one to the other and they may operate at independent rates.

An effective technique for a high resolution TDC is the Vernier Delay Line (VDL) TDC. It is based on two tapped delay lines where one is used as a reference path and another as a signal path. The signal delay line is built or tuned to be slightly faster than the reference delay line and the reference pulse precedes the signal pulse. A differential edge comparator is then used to determine the instant in time when the signal edge catches up to the reference edge. The resolution of the TDC is then determined by the difference of two delay lines and the effective time measurement can be made much smaller than the delay of a unit delay element.

Traditionally VDL TDCs have been employed in applications aimed at measuring precise time intervals, such as measuring the distance traveled by a reflected laser pulse in a range finder. While the measurement accuracy achieved is in the sub-picosecond range, the application did not require repeated measurements at very high rates and this shortcoming has stunted the development of VDL TDCs for high sample rate applications. The primary limitation of the conventional VDL TDC is that the pulse pair passes through the entire length of the delay lines before the next pulse pair enters the delay line. The maximum update rate is then limited by the latency of the delay line making the TDC the speed bottleneck in a VTDC architecture.

An alternative approach to the conventional VDL TDC leverages the understanding that unlike an array of comparators in a voltage-domain quantizer, the time domain equivalent of arrays of simple latches can support multiple signals simultaneously in the delay chains without interference. TPWQ makes use of an event detector that captures the pulse wave at the outputs of the delay line elements with two clock phases, detects pulse boundaries, and properly realigns the different data bits. This technique allows signals to be continually cascaded in the delay lines and fundamentally maximizes the update rate of the TDC. The TPWQ architecture shown in Figure 6 can be designed to operate at clock rates limited fundamentally by the delay of just 2 logic gates. The circuitry in the TPWQ is fully digital in nature and enjoys the full benefits of advanced CMOS technologies. Combining the VTC described earlier with this novel TDC yields a VTDC that can fundamentally achieve higher core rates than a SAR architecture and is thus better suited for interleaved ADCs.

Figure 7 shows a comparison of the resolution vs. sampling rate between the new VTDC architecture and the state of the art SAR based design\(^2\). For a given sampling capacitor size the maximum resolution is ultimately limited by thermal noise and represented by a horizontal \(kT/C\) noise line. For the VTDC, the maximum possible sampling rate is limited by the speed of the limiting amplifier and the delay of the VTC ramp, while for the SAR the sample rate is limited by the comparator latency multiplied by the number of conversion cycles required for 8-bit resolution. The curves showing the resolution versus sampling rate scalability highlight the advantage of our VTDC versus the SAR.

Using this new innovative architecture we can design a >4X faster core ADC than the state of the art in SAR ADC cores\(^3\). This reduces the interleaving factor required for a given sampling rate by the same factor leading to a simplified ADC front-end, which in turn leads to improved dynamic performance, lower overall power consumption and a significantly improved Walden Figure of Merit (Figure 8). Furthermore the design builds upon the strengths of leading edge digital CMOS technologies and will continue to benefit from future technology advances driven by the demand for faster and more efficient digital signal processing.

Figure 3. ADC constructed from cascaded voltage-to-time and time-to-digital converters.

Figure 4. Voltage to time converter (VTC).
Figure 5. Voltage to Time Conversion Example.

Figure 6. Proposed Traveling Pulse Wave Quantizer.

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References