Modeling, and Experimental Measurements, of the SER Critical Charge (Qcrit) in Scaled, SOI, CMOS Devices

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Abstract: Trends in modeling and measurements of the Soft Error Rate (SER) critical charge (Qcrit) for recent generation CMOS SOI devices are reviewed. Modeling and measurements as a function of voltage on 65, 45, 32 and 22 nm planar, SOI devices will be presented. The modeling techniques used will be reviewed and, where possible, compared to experimental measurements. Finally modeling of new device structures (e.g., multi-fingered FinFET devices) will also be discussed.

Keywords: SER Modeling, SET, Planar SOI Scaling, FinFETs

Introduction

For semiconductor manufacturers, the sensitive volume in which charge must be generated to produce single-event effects is an important technology parameter. Recent work shows that tri-gate technology reduces charge collection compared to planar technology. Moreover, the combination of a buried oxide layer, Silicon-on-Insulator (SOI), with FinFET technology leads to high performance devices with reduced silicon volume. FinFET technology is an excellent candidate for applications in which radiation-induced soft errors are a significant constraint. In bulk planar Si devices, charge generation, caused by impinging particles in the substrate, can collect in the drain, causing enough current to upset the storage node. In contrast, in bulk FinFETs, the conduction path is confined to a narrow channel. Therefore, much of the charge dissipates in the substrate (not collecting in the device) making the probability of SER much lower (e.g., 17X in a recent publication [1]).

In this paper we will review the state of the art in planar SOI Soft Error Rate (SER) device modeling and, where possible, compare to experimental results. This work will include scaling the voltage to determine the impact of low voltage operation on SER. We will include modeling of 65, 45, 32 and 22 nm SOI device nodes with a discussion about the role of geometry and doping profiles. Selected examples will be shown. In the second part of this paper we will extend this modeling work to SOI, CMOS FinFETs.

FinFET's are a promising device technology for extending scaling. They offer excellent solutions to the problems of sub-threshold leakage, poor short-channel electrostatic behavior, and high device parameter variability (a common problem in planar CMOS devices with scaling). The ability to operate at much lower supply voltage extends voltage scaling and allows for the possibility of both static and dynamic power savings. It is the superior control of the potential inside the channel in a FINFET, compared to planar devices, that reduces short channel effects. One example to be discussed is what happens to the collected charge if one uses SOI FinFET's? Modeling of the single event sensitivity in a Bulk vs. SOI FinFET was undertaken for a terrestrial environment. For this exercise (see Figure 1, below) a single fin, 2-stage inverter pulldown device was investigated (with a fan out (FO) = 1). Multiple fins would lead to even more robust SER behavior. The first stage was modeled as a full 3D (bulk or SOI) FinFET while, for ease of modeling, the second stage was a 2D SOI device in both cases. The Vdd = 0.9 V and the single event occurred in the NFET pulldown while monitoring both Vout1 and Vout2. The dielectrically isolated Fin’s (SOI) show advantages over a wide range of generated charge up to 2 fC.

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Summary

Deposited charge and circuit response determine the Qcrit for a technology or design (see Figure 2). Designs can be sensitive to low LET and high LET particles, just high LET particles or neither based upon the Qcrit. Parasitic bipolar amplification increases the amount of charge collected, yet it is not known how big a factor this will be in future scaled devices. Single Event Transients (SET) are less of an issue at low voltage (where the SEU rate increases), but questions still remain regarding susceptibility of hardened latches to SET effects at low V. A simulation of SETs in a 32 nm PD SOI device (not shown), found, for an inverter chain, that SETs could not propagate below 0.7 V. SETs are best mitigated by lowering the operating voltage; since the minimum propagating pulse width changes much faster than the SET pulse width. However, SEU rates should increase with lower voltages, so an optimum operating voltage needs to be carefully selected.

References