Modular and Scalable Firmware for Infrared LED Scene Projectors

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Abstract: Infrared scene projectors (IRSPs) are a critical laboratory tool for setup, test and calibration of infrared imaging systems. InfraRed Light Emitting Diodes (IRLEDs) are a new emitter technology for building IRSP systems with higher resolution and faster frame rates. This paper describes a scalable firmware architecture that meets the performance requirements of emerging IRLED IRSP systems. Our firmware enables the ability to add hardware modules to the TCSA system (Two-Color SLEDs Array) to increase performance or add functionality as needed by the customer.

Keywords: Infrared LED scene projector; FPGA; Modular and scalable firmware; VHDL

Introduction
In 2014, our team built the world’s first IRSP utilizing a MWIR 512x512 single-color, 48-micron pitch superlattice light-emitting diodes (SLED) array driven from a DVI computer interface at a frame rate of 100Hz displayed in Figure 1.

Since the completion our first generation SLEDs projector, we have been developing several follow-on projector systems with higher resolutions, faster frame rates and additional functionality. To reduce cost associated with building support electronics for multiple projectors our team has designed a modular and scalable electronics system [2]. This paper describes a modular and scalable firmware that controls the operation of this hardware platform.

TCSA IRSP Hardware
Designing a building block type architecture allows one to customize a projector regardless of the requirements. Customizable projector architecture is displayed in Figure 2 and consist of the following:

- TB-6V-LX760-LSI (TB6) motherboard FPGAs contain an array of programmable logic blocks, and a hierarchy of reconfigurable interconnects that allow the blocks to be wired together, like many logic gates that can be inter-wired in different configurations [4]
- FPGA (Field Programmable Gate Array) mezzanine card (FMC) with two, dual-channel 16-bit Digital to Analog converters (DACs)
- Riser cards with two, dual-channel amplifiers (AMPs)
- One to two TB-FMCL-HDMI (HDMI card) which provide the system with a scene to be displayed in one or two color
- One to two interface boards per TB6 that provide power to the DACs and amplifiers and collect the drive signals to send to the array.

![Figure 1. CSE for first generation 512x512 system. Inset: Donald Duck in “Der Fuehrer's Face” (1943 Disney Pictures and RKO Radio) (Top) displayed on the projector and captured with an IR camera (Bottom).]

![Figure 2. Scalable support electronics system for IRLED IRSP systems]
Scalable Firmware Architecture
For the next generation IRLED IRSP systems we wanted a design that would scale to higher resolutions, faster frame rates and be able to provide additional functionality without having to rewrite code from scratch for different versions of IRLED IRSPs. In order to accomplish our design criteria we had to design our firmware architecture to be scalable to accommodate the modular electronics. We currently deal with three languages: Python, C and VHDL (VHSIC (Very High Speed Integrated Circuit) Hardware Description Language). Python is the interface the user interacts with on a computer, allowing them to pick their desired resolution, speed of operation and many other features that are available. Using the user input, the C code decides how to achieve the desired resolution, and forwards the information to the VHDL code, which is the code the FPGA TB6 runs off of. This is also the base code for the IRSP system. The VHDL pushes out data out of the TB6 FPGA to however many DAC channels are required to achieve the desired resolution. By utilizing more DAC channels, the IRSP system is able to run at higher resolution. Figure 4a and 4b illustrate the relationship between DAC channels and resolution where each channel is represented by a color. In Figure 4a, we are utilizing only two channels to draw a full image. The red is the first channel and the green is the second channel. By doing this, we are able to run the system twice as fast as compared to if we were only utilizing one channel. Now we can reduce the time it takes the IRSP to draw a full frame just by increasing the number of DAC channels. In Figure 4b, the IRSP is being drawn using 16 channels, which greatly increases the speed of drawing a full frame. Once again, each color is representing a channel. After 16 rows are drawn, the channels repeat until the full frame resolution is displayed. Utilizing 16 channels increases our drawing speed by a factor of 16 compared to using only one channel. We are able to accomplish this by making sure we do not have to rewrite code to incorporate the added hardware. We are able to use existing code and scale it by adding additional BRAMS and outputting it to as many channels as desired by the user. However, once the number of DAC channels exceeds the limit of one TB6 board, another TB6 FPGA is required to accommodate the additional DAC boards. By utilizing or adding, more DAC channels to the IRSP system we are able to divide how many lines each channel is drawing in order to display one full frame. Doing this allows the IRSP to run at faster frame rates and higher resolution. This is a key focus in the progression of the IRSP, which increases productivity and decrease delays. Before fabricating the full 512x512 Read-In Integrated Circuit (RIIC), testing is accomplished using a smaller scale replica of the RIIC. This is to ensure the architecture of the whole system is working before we fabricate the final version of the system.
RIIC. A test RIIC uses the same hardware and firmware architecture as the full 512x512 RIIC, but the firmware is scaled down to display on a 16x16 or 1x1 RIIC.

Uniformity Corrections (NUC) is not utilized for this test. The scene generation computer to provide two inputs that would come from one video card that went into The HDMI cards pass that data to the TB6. These two inputs to the TB6 FPGA are identical/clone copies of each other but each being a different color. This allows us to provide two inputs to the system just as the final version of the projector. Making sure the data going into the HDMI card and being stored into the BRAM is correct is crucial to the effectiveness of the IRSP system. We test this by displaying a black image as the background (choosing a dark image displays no heat as if nothing was on or nothing was being displayed) and for the foreground, a mouse cursor was used as it is white which will give us a very high DAC value and will stand out from the background. This mouse cursor is moved across the monitor, as the location of the mouse changes, the corresponding address on the oscilloscope will rise indicating the mouse’s location and DAC value/brightness. At the end of the system is a scaled down version of the RIIC, which is on a test board for small scale testing. Instead, we connect macro LEDs to the RIIC test board to replicate the final version. Once the cursor moves to an address of a specific pixel, the corresponding led would light up. Each pixel consists of two LEDs that must stay in sync with each other. To confirm both LEDs are in sync we are able to trigger on one of the color inputs, this would allow us to move the mouse cursor across the screen. Once the cursor reaches the trigger, it will freeze the image and allow us to view the second color address location. The second color is located at the same address location as the first color. Figure 5 displays both colors at the same address location being turned on. Figure 6 shows the rise time of the LED with the IRSP system running at 1KHz.

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Figure 6. IRSP system running at 1 KHz with Rise time of LED at 20

Conclusion
Scalability is key to the progression of this IRSP system, because it allows us to focus on the real task which is how we can greater improve this technology and will allow us to efficiently and inexpensively design other variations of the IRSP system for specific applications for numerous customers.

Acknowledgments:
(a) “This project is funded by the Test Resource Management Center (TRMC) Test and Evaluation/Science & Technology (T&E/S&T) Program through the US Army Program Executive Office for Simulation, Training and Instrumentation (PEO STRI) under Contract No. W91ZLK-06-C-0006.” (b) “Any opinions, findings and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the Test Resource Management Center (TRMC) Test and Evaluation/Science & Technology (T&E/S&T) Program and/or the US Army Program Executive Office for Simulation, Training and Instrumentation (PEO STRI).”

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